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A statistical study of time dependent reliability degradation of nanoscale MOSFET devices

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the degree of Doctor of Philosophy.

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Abstract

Charge trapping at the channel interface is a fundamental issue that adversely affects the reliability of metal-oxide semiconductor field effect transistor (MOSFET) devices. This effect represents a new source of statistical variability as these devices enter the nano-scale era. Recently, charge trapping has been identified as the dominant phenomenon leading to both random telegraph noise (RTN) and bias temperature instabilities (BTI). Thus, understanding the interplay between reliability and statistical variability in scaled transistors is essential to the implementation of a ‘reliability-aware’ complementary metal oxide semiconductor (CMOS) circuit design. In order to investigate statistical reliability issues, a methodology based on a simulation flow has been developed in this thesis that allows a comprehensive and multi-scale study of charge-trapping phenomena and their impact on transistor and circuit performance. The proposed methodology is accomplished by using the Gold Standard Simulations (GSS) technology computer-aided design (TCAD)-based design tool chain co-optimization (DTCO) tool chain. The 70 nm bulk IMEC MOSFET and the 22 nm Intel fin-shape field effect transistor (FinFET) have been selected as targeted devices.

The simulation flow starts by calibrating the device TCAD simulation decks against experimental measurements. This initial phase allows the identification of the physical structure and the doping distributions in the vertical and lateral directions based on the modulation in the inversion layer’s depth as well as the modulation of short channel effects. The calibration is further refined by taking into account statistical variability to match the statistical distributions of the transistors’ figures of merit obtained by measurements. The TCAD simulation investigation of RTN and BTI phenomena is then carried out in the presence of several sources of statistical variability. The study extends further to circuit simulation level by extracting compact models from the statistical TCAD simulation results. These compact models are collected in libraries, which are then utilised to investigate the impact of the BTI phenomenon, and its interaction with statistical variability, in a six transistor-static random access memory (6T-SRAM) cell. At the circuit level figures of merit, such as the static noise margin (SNM), and their statistical distributions are evaluated. The focus of this thesis is to highlight the importance of accounting for the interaction between statistical variability and statistical reliability in the

simulation of advanced CMOS devices and circuits, in order to maintain predictivity and obtain a quantitative agreement with a measured data. The main findings of this thesis can be summarised by the following points:

- Based on the analysis of the results, the dispersions of V_T and ΔV_T indicate that a change in device technology must be considered, from the planar MOSFET platform to a new device architecture such as FinFET or SOI. This result is due to the interplay between a single trap charge and statistical variability, which has a significant impact on device operation and intrinsic parameters as transistor dimensions shrink further.
- The ageing process of transistors can be captured by using the trapped charge density at the interface and observing the V_T shift. Moreover, using statistical analysis one can highlight the extreme transistors and their probable effect on the circuit or system operation.
- The influence of the passgate (PG) transistor in a 6T-SRAM cell gives a different trend of the mean static noise margin (\overline{SNM}) Due to the trade-off between the ageing process and the driveability between PG and pull down (PD) transistors.
- Our analysis of the results also shows less variability in SNM of SRAM cells using FinFETs when compared to SRAM cells using planar transistors. This observation is attributed to the fact that variability in FinFETs has less impact on static noise margin (SNM) variability. Also, circuits with FinFETs show more SNM stability when compared to circuits with the bulk MOSFET.

The results obtained in this thesis are of great importance for a physics-based understanding of reliability in nano-CMOS devices and to guide the development of circuit compact models for reliability prediction in very large-scale integrated circuits.

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Publications

Journal Publications

- [RH-1] Louis Gerrer, Andrew R. Brown, Campbell Millar, **Razaidi Hussin**, Salvatore Maria Amoroso, Binjie Cheng, Dave Reid, Craig Alexander, David Fried, Michael Hargrove, Ken Greiner, Asen Asenov: Accurate Simulation of Transistor-Level Variability for the Purposes of TCAD-Based Device-Technology Cooptimization. IEEE Transactions on Electron Devices 06/2015; 62(6):1-1. DOI:10.1109/TED.2015.2402440
- [RH-2] **Razaidi Hussin**, S.M. Amoroso, Louis Gerrer, Ben Kaczer, Pieter Weckx, Jacopo Franco, Annelies Vanderheyden, Danielle Vanhaeren, Naoto Horiguchi, Asen Asenov: Interplay Between Statistical Variability and Reliability in Contemporary pMOSFETs: Measurements Versus Simulations. IEEE Transactions on Electron Devices 09/2014; 61(9):3265-3273. DOI:10.1109/TED.2014.2336698
- [RH-3] Louis Gerrer, Salvatore Maria Amoroso, **Razaidi Hussin**, Asen Asenov: RTN distribution comparison for bulk, FDSOI and FinFETs devices. Microelectronics Reliability 08/2014; 54(9-10). DOI:10.1016/j.microrel.2014.07.013
- [RH-4] Salvatore Maria Amoroso, Louis Gerrer, **Razaidi Hussin**, Fikru Adamu-Lema, Asen Asenov: Time-dependent 3-D statistical KMC simulation of reliability in nanoscale MOSFETs. IEEE Transactions on Electron Devices 06/2014; 61(6):1956-1962. DOI:10.1109/TED.2014.2318172
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- [RH-6] Louis Gerrer, Jie Ding, Salvatore Maria Amoroso, Fikru Adamu-Lema, **Razaidi Hussin**, Dav Reid, Campbell Millar, Asen Asenov: Modelling RTN and BTI in nanoscale MOSFETs from device to circuit: A review. Microelectronics Reliability 04/2014; 54(4). DOI:10.1016/j.microrel.2014.01.024

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- [RH-7] M. Duan, J. F. Zhang, A. Manut, Z. Ji, W. Zhang, A. Asenov, D. Reid, **H. Razaidi**, D. Vigar, V. Chandra, R. Aitken, B. Kaczer, G. Groeseneken, "Hot carrier aging and its variation under use-bias: Kinetics, prediction, impact on Vdd and SRAM," *2015 IEEE International Electron Devices Meeting (IEDM)*, Washington, DC, 2015, pp. 20.4.1-20.4.4. doi: 10.1109/IEDM.2015.7409742
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- [RH-9] **Razaidi Hussin**, Louis Gerrer, Jie Ding, Salvatore Maria Amaroso, Liping Wang, Marco Semicic, Pieter Weckx, Jacopo Franco, Annelies Vanderheyden, Danielle Vanhaeren, Naoto Horiguchi, Ben Kaczer, Asen Asenov: Reliability aware simulation flow: From TCAD calibration to circuit level analysis. Simulation of Semiconductor Processes and Devices (SISPAD), 2015; 09/2015
- [RH-10] **Razaidi Hussin**, Louis Gerrer, SM Amoroso, Liping Wang, Pieter Weckx, Jacopo Franco, Annelies Vanderheyden, Danielle Vanhaeren, Naoto Horiguchi, Ben Kaczer, Asen Asenov: TCAD-based methodology for reliability assessment of nanoscaled MOSFETs. 11th Conference on Ph.D. Research in Microelectronics and Electronics (PRIME), 2015; 06/2015
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- [RH-12] Louis Gerrer, Salvatore Maria Amoroso, **Razaidi Hussin**, Fikru Adamu-Lema, Asen Asenov: 3D Atomistic Simulations of Bulk, FDSOI and Fin FETs Sensitivity to Oxide Reliability. Simulation of Semiconductor Processes and Devices (SISPAD), 2014;09/2015

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Abbreviations

6T-SRAM	6 Transistor-Static Random Access Memory
ADM	Access Disturb Margin
AFM	Atomic Force Microscopy
API	Application Programmed Interface
BEOL	Back End Of Line
BL	Bit line
BSIM4	Berkeley Short-channel IGFET Model version 4
BTE	Boltzmann Transport Equation
BTI	Bias Temperature Instability
CM	Compact Model
CMOS	Complementary Metal Oxide Semiconductor
COBYLA	Constrained Optimisation BY Linear Approximation
DD	Drift Diffusion
DG	Density Gradient
DIBL	Drain-Induced Barrier Lowering
DMG	Device Modelling Group
DoE	Design of Space
ER	Edge Roughness
FER	Fin Edge Roughness
FinFET	Fin-Shaped Field Effect Transistor
FoM	figure of merit
GER	Gate Edge Roughness
GIDL	Gate Induced Drain Leakage
GSS	Gold Standard Simulation
HCI	Hot Carrier Injection
HP	High Power
HPC	High-Performance-Computer
IC	integrated circuit
imec	Interuniversity Microelectronics Centre
I_{OFF}	OFF current
I_{ON}	ON current
ITRS	International Technology Roadmap for Semiconductors
IV	Current Voltage
IWT	Intrinsic Write Time
LER	Line Edge Roughness
LP	Low Power
MC	Monte Carlo
MGG	Metal Gate Granularity
MOL	Middle of Line
MOS	Metal Oxide Semiconductor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MP	Medium Power
NBTI	Negative Bias Temperature Instability
nfet	Negative Channel Field Effect Transistor
NGEF	Non-equilibrium Green Function
NPM	Nonlinear Power method
OPC	Optical Proximity Correction
P/MGG	Polysilicon/Metal Gate Granularity
PBTI	Positive Bias Temperature Instability

PCA	Principal Component Analysis
PD	Pull Down
pfet	Positive Channel Field Effect Transistor
PG	Pass Gate
PSG	Poly-Silicon Granularity
PSP	Penn State-Philips
PU	Pull Up
RD	Reaction Diffusion
RDD	Random Discrete Dopants
RMS	Root Mean Square
RTN	Random Telegraph Noise
SADP	Self-Aligned Double Patterning
SBD	Soft Breakdown
SCE	Short Channel Effect
Si/SiO ₂	Silicon/Silicon Dioxide
SIA	Semiconductor Industry Association
SISPAD	Simulation of Semiconductor Process and Devices
SNM	Static Noise Margin
SP	Standard Power
SPICE	Simulation Program with Integrated Circuit Emphasis
SRAM	Static Random Access Memory
SRH	Schockley-Read-Hal
SS slope	Subthreshold Slope
SSRM	Scanning Spreading Resistance Microscopy
STD	standard deviation
STI	Shallow Trench Isolation
SV	Statistical Variability
TAT	Trap Assisted Tunneling
TCAD	Technology Computer-Aided Design
TDDS	Time Dependent Defect Spectroscopy
TDV	Time Dependent Variability
TEM	Transmission Electron Microscopy
TMA	Technology Modelling Associate
V _T	Threshold Voltage
WF	Work Function
WL	Word Line
WRM	Write Margin
ΔV _T	threshold voltage shift

Chapter 1: Introduction

Background

The main challenge of the contemporary technology is to continue improving transistor performance with scaling. One of the red-brick wall along this path is related to the discreteness of charge and the granularity of matter, resulting in a rapid increase in transistor variability. Simultaneously, the transistor reliability associated with discrete charge trapping in the gate stack has become a significant contributor to transistor variability. It affects circuits and systems over their lifetime and needs to be taken into account in their design (Kaczer et al., 2011). Following the recent paradigm change in understanding of gate oxide reliability (Tibor Grasser, Kaczer, et al., 2011), several oxide ageing phenomena, e.g. Random Telegraph Noise (RTN) or Bias Temperature Instability (BTI), are now understood in terms of discrete charge trapping in the gate oxide (Kaczer et al., 2010). The impact of the charge trapping depends on trap position both energetically and spatially in respect to the other sources of Statistical Variability (SV). Therefore it is of paramount importance to study trap related effects in a 3D framework including SV. The following sections present the research motivation and objectives as well as the structure of this thesis.

1.1 Motivation

Among the key growth drivers in the global semiconductor industry is the continuous demand for higher component densities and greater chip functionality, which can only be achieved by scaling down the transistor-size. As a result, the switching speed increases significantly and inversely with the channel length (L_G), which allows the circuit to operate

at high frequency (Nowak, 2002). Another growth driver, which is no less important to the industry and consumers, is the overall manufacturing cost per transistor.

In 1971, the Intel Microprocessor 4004 was assembled using 2300 transistors (Faggin, Hoff, Mazor, & Shima, 1996), but today personal computers are made from large-scale integrated circuits with billions of transistors. The advancement in semiconductor technology is captured by Moore's Law (Moore, 1998) which states that the transistors inside chips are doubled every 18 months. The Era of Happy Scaling (Baccarani, Wordeman, & Dennard, 1984) rigorously followed the Moore's Law prediction until the scaling limitation started to threaten the traditional microelectronic industry pathway, around 45 nm technology and beyond. This scaling limitation is currently dictating the industry shift from the traditional planar Metal Oxide Semiconductor Field Effect Transistor (MOSFET) to innovative transistor architecture including FDSOI MOSFETs and FinFETs.

Studies have shown that Statistical Variability (SV) (Declerck, 2005) and performance degradation due to stress (Schroder & Babcock, 2003) has become a critical factor affecting the scalability of the planar MOSFET. The SV refers to the stochastic dispersion in electrical characterisation due to the atomic scale variation in the transistor structure. This is partially due to the relative reduction in the number of random discrete dopants (RDD) in the channel transistor that control the electrical properties (K. J. Kuhn, 2007). Metal gate granularity (MGG) and line edge roughness also have an impact on the SV (Reid, Millar, Roy, & Asenov, 2010; X. Wang, Brown, Cheng, & Asenov, 2011).

The introduction of high- κ gate stack in mass production of the 45 nm CMOS technology generation increases the performance of the transistor. However, this cannot compensate for the significant increase in the bulk MOSFET SV fluctuation with scaling (Asenov, 1998). Published simulation studies have shown that more than 60% of the threshold voltage variation at 45 nm technology is due to RDD (K. J. Kuhn, 2007). The significant increase in SV has a dramatic impact on the yield of the Static Random Access Memory (SRAM) (Cheng, Roy, Roy, Adamu-Lema, & Asenov, 2005) and creates a problem in logic circuit timing closure (Kamsani, Cheng, Roy, & Asenov, 2008).

Experimental data described in (Fantini et al., 2007; Kurata et al., 2007) and 3D simulation studies in (Salvatore Maria Amoroso, Compagnoni, et al., 2013; Asenov, Balasubramaniam, Brown, & Davies, 2003; Ashraf & Vasileska, 2010) have verified that even a single charge trapping at the interface of the transistor channel can result in a dramatic change in the

electrical characteristic of the transistor. Threshold voltage shifts in excess of 0.24 V in 65 nm flash memory has been reported in (Cai, Song, Kwon, Lee, & Park, 2008) which poses a significant challenge in the memory circuit design (Tega et al., 2008).

1.2 Objective

The aim of this PhD is to investigate the interplay between statistical reliability and SV in scaled planar MOSFET and FinFETs. In order to achieve this aim, the research has been performed according to the following objectives:

1. Perform TCAD modelling and calibration based on measured or published MOSFET and FinFETs to get realistic and representative structures that will be used in the atomistic simulation of reliability and variability.
2. Perform a comprehensive simulation study of SV effects due to charge and matter granularity in the calibrated testbed MOSFET and FinFETs.
3. Perform a comprehensive statistical simulation study of reliability in the presence of SV in the calibrated and scaled transistors. Gain deep understanding of the time dependent variability effects including the impact on the distributions and the correlations between the key transistor figures of merit.
4. Investigating the impact of variability and reliability on transistor performance in 6T-SRAM circuits by using accurate statistical compact models extracted from the calibrated TCAD simulation results of planar MOSFET and FinFETs.

1.3 Thesis outlines

The thesis is divided into seven chapters. Chapter 2 and Chapter 3 explain the background and simulation methodology used respectively in this research work. Chapters 4, 5 and 6 contain the simulation result and analysis. The conclusions are presented in Chapter 7.

Chapter 2 presents an overview of MOSFET scaling and the related variability and reliability issues. The fundamentals and background of the SV and statistical reliability in MOSFETs are described. Insight of the important TCAD modelling and simulation is discussed and the link to circuit simulation is established.

Chapter 3 presents the methodology adopted throughout this research. This includes the description of the simulation tool chain, followed by the TCAD simulation tool and its capability to accurately predict the statistical variability and reliability in the investigated transistors. This is followed by the compact model extraction tool and the corresponding compact model extraction strategies. Finally the circuit simulation tool and methodology are explained in detail.

Chapter 4 presents the calibration of a 70 nm planar technology MOSFET model fabricated at the Interuniversity MicroElectronics Center (imec). This includes the physical device structure and doping calibration and the current-voltage (IV) characteristics calibration. After the successful calibration TCAD analysis was carried out of SV and the impact of trapped charge on RTN amplitude distribution and the impact of BTI on the progressive increase of the statistical variability with ageing.

In Chapter 5, the TCAD calibration and the simulation of a 22 nm Intel technology FinFET are presented. The calibration process starts with the matching of the device structure and doping profile against the published experimental data and is followed by the mobility calibration to achieve a good agreement with the IV characteristic. The simulation investigation of the impact of SV which is defined by RDD, gate edge roughness (GER) and MGG on device characteristics is presented, followed by the simulation of the device degradation with respect to the BTI phenomenon.

The compact model (CM) extraction for the planar MOSFETs and FinFETs is presented in Chapter 6. This extraction follows a step-by-step strategy starting with uniform CM extraction followed by the extraction of the statistical CM of the fresh device and the degraded device with a different level of degradation. The utilisation of the extracted CM in the analysis of the BTI degradation on the 6T-SRAM static noise margin (SNM) is also presented.

Finally, Chapter 7 draws the main conclusion of this research and makes some remarks, suggestion and proposals for future research in this area.

Chapter 2: Literature Review

Background

This chapter provides the background for the research presented in this thesis. This includes the intrinsic variability and the statistical reliability related to the gate stack defects of the Metal Oxide Semiconductor Field Effect Transistor (MOSFET). Firstly, the origins and the impact of statistical variability are discussed. Then, a classification of the degradation mechanisms related to the charging and discharging process is presented.

2.1 MOSFET scaling and reliability issues

In 1965 Gordon Moore made an important observation that the increase of the number of transistor per integrated circuit (IC) was estimated to be doubled every two years (Moore, 1998). Because of the accuracy in predicting the growth of IC complexity, Moore's observation known as Moore's Law, became a benchmark rule for the semiconductor industry, governing the increase in the number of integrated transistors, the wafer size upscaling and the exponential reduction of production cost per transistor. Although this law was defined more than 50 years ago, it still motivates the semiconductor industry. Regardless of the increasing complexity of the challenges facing the semiconductor industry, Moore's observation remained instrumental in maintaining the semiconductor industry dynamics over the years. Continuous efforts have been made and will continue to be made to keep the pace of increasing the integration and improving performance (Gargini, 2000).

The path of the semiconductor industry is outlined by the Semiconductor Industry Association (SIA) in the International Technology Roadmap for Semiconductors (ITRS) document. The purpose of this document is to guide the advancements in semiconductor technology and highlight the essential research and development issues to keep the continuation of Moore's projection. Each year, ITRS identifies technology challenges and needs that must be faced by the semiconductor industry in the next 15 years. The latest edition of ITRS in 2015 showed the targets and requirements to maintain the integration progress at a pace defined by the growth requirements of the semiconductor industries.

In respect of the research needs and physical limitations as described by the ITRS, the conventional approach of scaling and historically Moore's projection are no longer practical and achievable. The drastic increase in the transistor process complexity drives the increase of the manufacturing investment costs. For example, the manufacturing cost related to lithography has increased exponentially up to \$35 million per lithography station in 2008 (Scott E. Thompson & Parthasarathy, 2006). Despite these significant efforts and the astonishing achievements in the process and yield improvement, some challenges remain unchanged due to systematic and stochastic process variability. For example, dopant concentrations are not the same between the beginning and at the end of the wafer ingot. They also vary from the middle of the wafer towards its edge. These processes induce variability in transistor performance dispersion.

However, a concern arises as the transistor dimensions have reached the critical limit where the granularity of charge and matter introduce uncontrollable parameter fluctuations. The active region of the transistor is approximately a couple of atomic layers thick. Therefore, the random number and positions of the atoms can lead to the drastic variation of the performance from transistor to transistor. This statistical variability is an important issue, which accelerates the end of the Happy Scaling Era (Schaller, 1997; Wulf & McKee, 1995). Random discrete dopants (RDD), polysilicon/metal gate granularity (P/MGG) and line edge roughness (LER) are the main contributing source of statistical variability, which will be discussed in Section 2.2.2.

This has raised new challenges for transistor design and technology, leading to the introduction of innovative metal oxide semiconductor (MOS) transistors to reduce the variability impact. New fin-shaped field effect transistor (FinFET) were adopted that tolerate low doped channels reducing the RDD variability (Declerck, 2005; Iwai & Ohmi, 2002). However, the innovative transistor design effort may not be enough to overcome the

challenges mentioned earlier. The circuit designers are facing new challenges mitigating the impact of the variability during the design and implementation process. Figure 2-1 illustrates how static random access memory (SRAM) circuit design margins are reduced from one technology node to another due to the different variability components of transistor parameters, whereas the process induces variability (marked as global V_T) and the static noise impact remain almost unchanged.

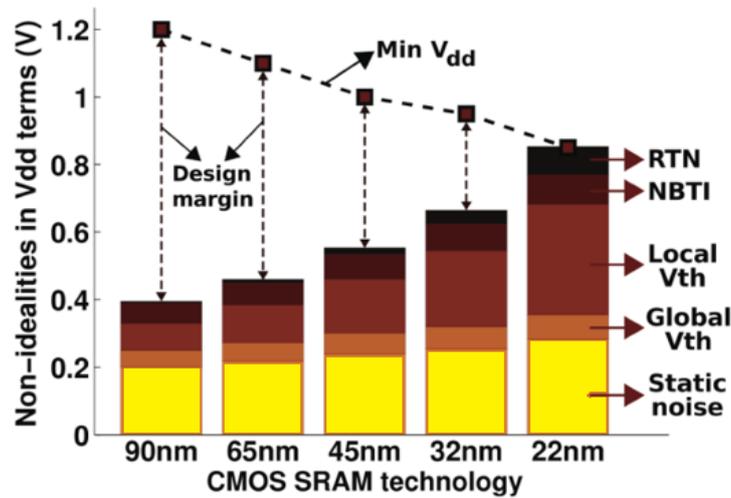


Figure 2-1: The evolution of CMOS SRAM technology with variations of V_{dd} input yields reduction in design margin as well as the statistical variability. After ref (Aadithya, Demir, Venugopalan, & Roychowdhury, 2011).

Apart from variability issues, time dependent variability (TDV) is one of the major challenges of the semiconductor industry. One of the most important factors in this TDV reliability is the gate oxide integrity. Phenomena such as random telegraph noise (RTN), bias temperature instability (BTI) and trap assisted tunnelling (TAT) have been recognised as responsible for the transistor performance degradation. These phenomena are related to trap formation at the interface or in the oxide and the subsequent charging and discharging mechanisms. As a result of the MOS gate capacitor decreasing with downscaling, a single trap can now induce significant changes in transistor performance through time. Therefore, it is great importance to properly address these new concerns by extensive research effort in modelling and simulation from the atomistic transistor simulator level up to circuits.

Since the statistical reliability has become a major concern in the semiconductor industry, a lot of research has been done on this topic using various approaches and models. The first realistic approach presented in (Asenov, 1998) used atomistic simulations of large transistor samples. In this work, the compact model (CM) is extracted at different operating times to corresponding to the increase of the trap densities in the transistors with ageing. The major

advantage of this approach is that it can be applied for every transistor architecture (L. Gerrer et al., 2013), providing realistic interactions between traps and statistical variability sources. This approach provides the worst-case design by assuming the same age for every transistor in a given circuit, which is not necessarily the case as one given transistor could be used intensively whereas another one may not be used at all.

Another transistor to circuit approach recently presented by the Interuniversity Microelectronics Centre (imec) (Weckx et al., 2013), assumed an exponential distribution of single trap impact on the threshold voltage, V_{th} and incorporates this into a Verilog-A component inserted in the circuit, together with measured distributions of trap dynamics to simulate workload dependent circuit ageing. However, the use of Verilog components strongly limits the number of simulated transistors to around 100, which represents a major limitation for industry needs. As reported in (T. Grasser et al., 2009; T. Grasser et al., 2013), researchers introduced a multi-state model to capture more accurately the trap behaviour (about 30% of the traps are said to be multi-state traps). According to the observation, trapping and de-trapping models were directly based on adiabatic potentials obtained from accurate first principle simulations. This makes the approach more realistic for the simulation of trap dynamics.

At the present time, limited research related to the stochastic property of statistical reliability as well as the difficulties in performing large sample statistical measurements leads to a lack of widely available experimental data. In addition, very few companies have the resolve and the resources for making statistical measurements of large samples. Furthermore, most of them treat such measurements as confidential and do not share them with others. Hence, no extensive comparisons have ever been made between simulation and experimental data.

At present, there is no consensus on the simulation approach, including atomic level models of degradation; reliable statistical variability simulators as well as circuit simulation capacities that should be used jointly to fully address the problem. For example, the tool discussed in (T. Grasser et al., 2009; T. Grasser et al., 2013) related to the charge trapping in switching oxide traps lacks the statistical simulation capabilities in respect of the combination of variability sources. To address this challenge, the interplay between reliability and statistical variability in scaled transistors will be investigated in detail by means of a 3D statistical atomistic simulation on large samples.

2.2 Variability

Taking into account the variability in a circuit design is very important because of the significant impact on transistor performance. The impact becomes worse when the transistors are scaled down, resulting in circuit layout and electrical parameters departures from the design specification. The CMOS variability can be broadly classified into two categories, namely global and local variability (Nassif et al., 2007; Samar, 2010).

Global variability refers to transistor variations across or between fabricated wafers, including for example gate length/width, oxide thickness and doping concentration. Normally, this kind variation is related to the variations of process parameters and the imperfection of the equipment used in the fabrication process. The global variability can be improved or controlled by using better manufacturing equipment and accurate process control. Figure 2-2 illustrates the global variation of threshold voltage measured in a single wafer

The local variability on the other hand, reflects the stochastic variations of the electrical parameters between neighbouring transistors on the same chip. The local variability can be classified as systematic or statistical variability.

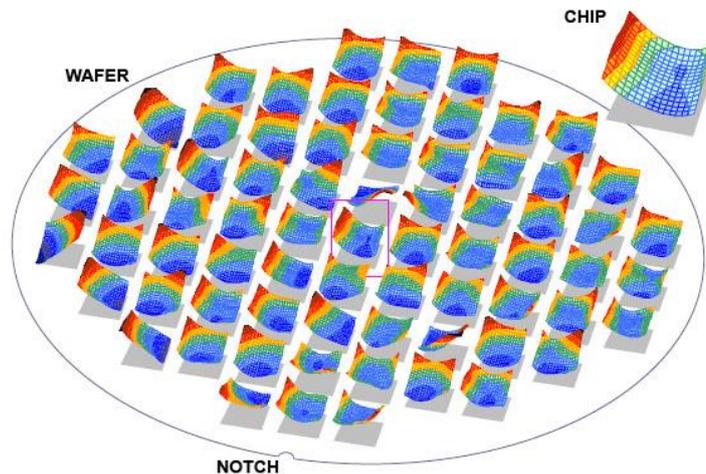


Figure 2-2: Chip-to-chip variation in single wafer due to systematic and statistical variability, after (Masuda, Ohkawa, Kurokawa, & Aoki, 2005).

2.2.1 Systematic Variability

The systematic variability conforms to a well-understood behaviour and it can be predicted or modelled up-front. Examples of systematic variability are the patterning proximity effect

(Kanamoto et al., 2007; Randall & Tritchkov, 1998) and the layout induced stress variation (Morifuji et al., 2009).

One of the main sources of systematic variability is the lithography process. Transistor 30 nm characteristic dimensions are still printed with 193 nm lithography equipment (Zell, 2006). As a result, the original pattern design is dissimilar to the printed geometry of the actual transistor due to proximity and fringing effect.

Several techniques can be applied to mitigate imperfections of the lithography process and to reduce the corresponding variability. One of the most useful patterning solutions involves optical proximity correction (OPC) (Capodieci, 2006). This can be achieved by calculating the lithography-induced distortion pattern and correctional accordingly the mask shapes resulting in a correct shape transfer onto the wafer.

Although the OPC can mitigate the lithography effect, the introduction of strain (Antoniadis et al., 2006) results in additional transistor variability effects. The process induces strain initially introduced at the 90 nm technology node for a better carrier mobility and becomes an essential component in the subsequent CMOS technology generations (S. E. Thompson, 2005; S. E. Thompson et al., 2004). However, the induced strain is layout dependent and resulting in layout dependence of the transistor characteristics (Xingsheng, Binjie, Roy, & Asenov, 2008).

2.2.2 Statistical Variability

Recently, statistical variability (SV) became a primary concern due to its effect on design, and the fact that it creates circuit simulation difficulties in contemporary and future technology nodes. RDD, PSG or MGG and LER are considered as SV sources. Extensive work has been carried out in respect of these SV sources for bulk transistors for many years, becoming industrially relevant as the transistors reached the sub-micron regime. Therefore, the issue regarding SV is impossible to ignore and must be included in circuit design and the corresponding circuit simulation and verification process.

2.2.2.1 Random Discrete Dopant

RDD introduces a variation in the transistor characteristic, including the threshold voltage, V_T . Experimental studies performed by Wong and co-researchers (Wong & Taur, 1993) reported that RDD has an effect on the transistor performance, where apart from the well-

known V_T fluctuation, there is an average shift in the V_T value due to the inhomogeneity of the channel potential.

The RDD variability is due to two factors. Firstly, the variation in the numbers of dopants in the active region of the transistors and secondly the different dopant configurations in the individual transistors. Therefore, transistors with similar numbers of dopant but with different dopant configurations will have different IV characteristics. Figure 2-3 shows Technology Computer Aided Design (TCAD) simulation example taking into account the random number and position of dopants in a transistor. It illustrates the necessity to perform a 3D simulation for the accurate prediction of statistical variability.

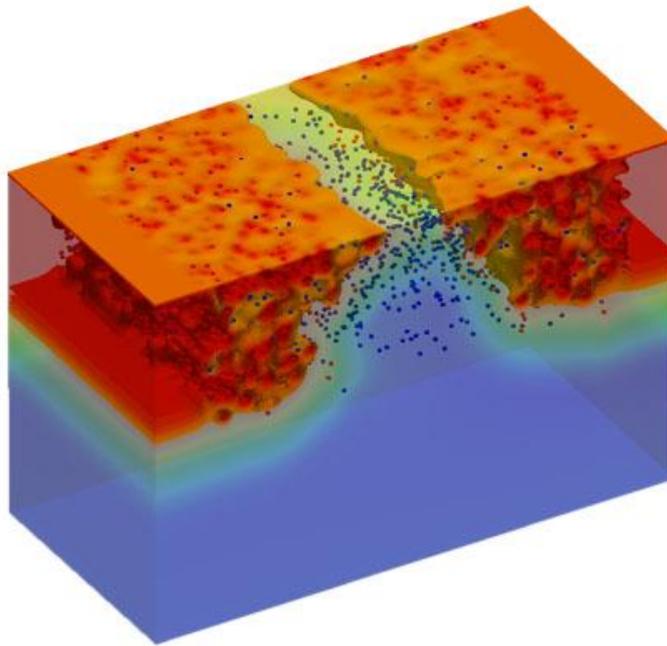


Figure 2-3: Simulated TCAD transistor with a configuration of random number and position of dopants (L. Gerrer et al., 2013).

Based on the fact that the number of dopants followed a Poisson distribution (Lakshmikumar, Hadaway, & Copeland, 1986; Stolk, Widdershoven, & Klaassen, 1998; Takeuchi, Tatsumi, & Furukawa, 1997) a simple formula has been derived, allowing the estimation of the RDD induced threshold voltage standard deviation σV_T (Stolk et al., 1998).

$$\sigma V_T = \frac{qt_{ox}}{\epsilon_{ox}} \sqrt{\frac{N_A W_d}{4L_{eff}W_{eff}}} \quad (2.1)$$

The threshold voltage standard deviation σV_T is directly proportional to the electron charge q , the square root of the depletion width W_d and is inversely proportional to the oxide

capacitance, ($c_{ox} = \epsilon_{ox}/t_{ox}$). Thus, a reduction in the gate capacitance will reduce the dispersion of V_T in the transistor scaling process. Clearly the channel doping increase in order to control short channel effect (SCE) leads to a significant increase in the V_T variability.

According to (Asenov, Brown, Davies, & Saini, 1999), the RDD impact can only be simulated in 3D. This is because the configuration of the dopant essentially contributes to the fluctuation of the transistor characteristics. The dopant configurations create specific current percolation paths, which are different from transistor to transistor. For instance, dopants which are located close to the centre of the channel have the greatest impact for V_T (Kufluoglu & Alam, 2007).

As the CMOS technology scales, RDD becomes the major source of variability in the sub 0.1 μm bulk transistors. Previous researchers (Asenov, 1998; Wong & Taur, 1993) have investigated the implication of RDD when the transistor dimension shrinks beyond 60 nm. They found that it is difficult to rely on the uniform doping approximation when calculating the IV characteristic. In order to accurately predict the IV characteristic, it is proposed to use statistical ‘atomistic’ simulations. This is because it can capture the effect of the discrete dopants in terms of their stochastic numbers and positions in the channel.

By using ion implantation, impurities are introduced into the silicon substrate to form the required doping profile. During this process, a series of atomic collisions occur until the implanted impurity atoms arrive at equilibrium, resulting in a random position of a dopant in the transistor. Figure 2-4 shows the experimental image of random dopant configuration in a transistor.

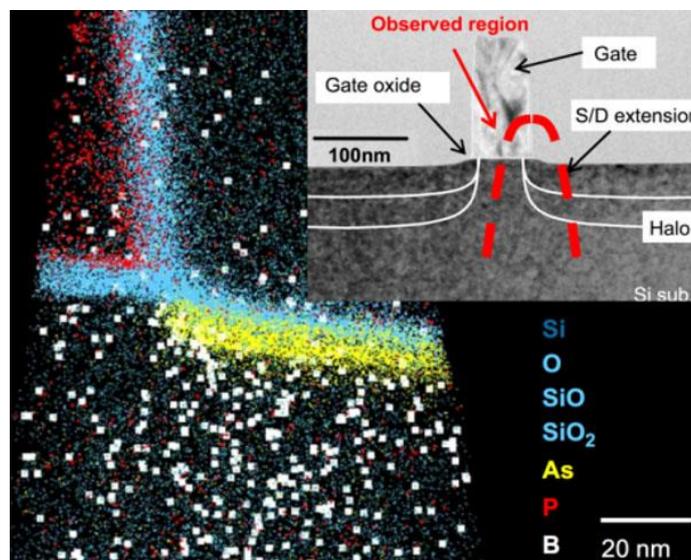


Figure 2-4: Experimental observation of discrete dopants (Inoue et al., 2009)

This randomness in the numbers and configurations of dopants creates percolation paths at the interface. It has been reported in (Kirton & Uren, 1989; Masuduzzaman, Islam, & Alam, 2008; McWhorter, Meyer, & Strum, 1957) that the effect of inducing the source to drain percolation paths leads to significant random threshold voltage shift in the individual transistors. Simultaneously, the presence of the percolation paths also results in drive current variability. Figure 2-5 shows TCAD simulation result illustrating a source to drain percolation path.

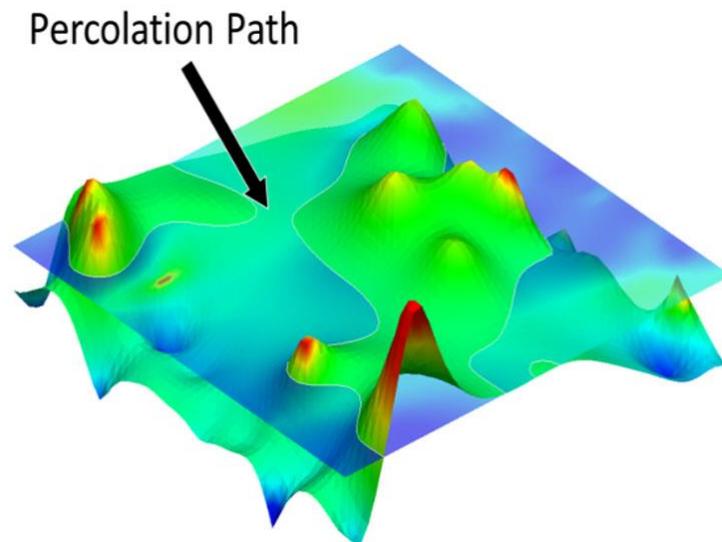


Figure 2-5: Source to drain percolation path behaviour (L. Gerrer et al., 2013)

2.2.2.2 Poly and Metal Gate Granularity (PSG/MGG)

In addition to RDD, PSG and MGG are other major contributors to variability in contemporary transistors. PSG is associated with the boundaries between polysilicon grains that create non-uniform doping and surface potential pinning in the polysilicon gate (Hane, Ikezawa, & Ezaki, 2003). On the other hand, the MGG is a result of the grain formation with different crystal orientations after the annealing process in high-k/metal gate CMOS transistors.

In PSG case, the gates boundaries are formed between grains and result in Fermi level pinning and non-uniformity in the doping profile due to the rapid diffusion along the grain boundaries. First principle simulations show that the average pinning potential is approximately 0.35 eV below the conduction band edge. The average grain size for a well-

controlled poly-silicon gate CMOS process at 45 nm and 32/ 28 nm technology nodes is 40 nm (A. R. Brown, Roy, & Asenov, 2007).

Metal gate was introduced as a replacement to polysilicon gate material with the intention of high- κ gate dielectric in order to increase the transistor performance and to suppress tunnelling leakage current through the gate dielectric. The introduction of a high- κ metal gate stack not only reduces the gate leakage current, but also eliminates the polysilicon related variability (Mistry et al., 2007). However, during the post metal gate deposition using high temperature processing, the initially nominal amorphous metal becomes polycrystalline as illustrated in Figure 2-6. This results in metal gate granularity with the individual grains having different crystallographic orientations with different work functions. For example, as reported in (Andrew R Brown, Idris, Watling, & Asenov, 2010) TiN has two dominant metal grain orientations with the first $\langle 200 \rangle$ orientation appearing with probability of 60% and having 200 mV higher WF compared to the second one. The effect of MGG on the potential profile is illustrated in Figure 2-7.

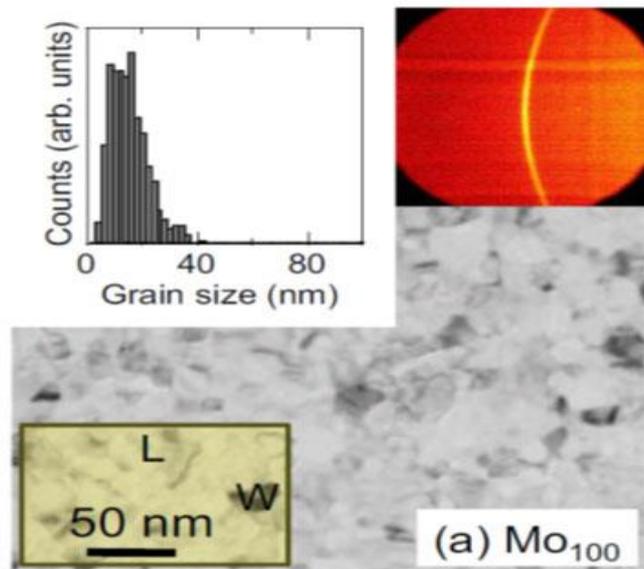


Figure 2-6: TEM image and histograms of grain size shows an impact from MGG (Ohmori et al., 2008)

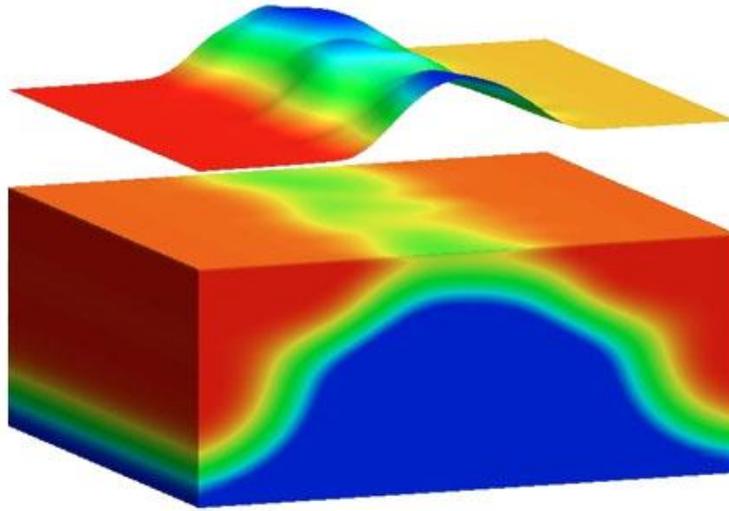


Figure 2-7: Image illustrating the 3D potential distribution along the carrier transport direction with the impact of MGG as statistical variability sources (L. Gerrer et al., 2013)

2.2.2.3 Line Edge Roughness

In bulk CMOS transistors, LER has a relatively smaller impact compared to other sources of variability in a conventional transistor. Fin edge roughness (FER) and gate edge roughness (GER) are major contributors to the local, statistical variability in FinFETs. Edge roughness (ER) arises due to the imperfection of the processing techniques including lithography material deposition and processing. LER cannot be underestimated as it leads to a serious variability when the transistor dimensions shrink to few decanometres. Figure 2-8 shows the origin of LER in the lithography process with a different resist flavours. Fig. 2-8 (a) shows the effect of negative resist when unexposed regions are removed while Fig. 2-8 (b) shows the effect of positive resist when the exposed region is retained. These images show that the photoresist edge is defined by the polymer granularity. The gate etching process transfers the photo resist pattern into the gate material.

LER is defined by two important parameters: the Root Mean Square (RMS) magnitude of the line edge variation from the mean Δ and the correlation length Λ (Asenov, Kaya, & Brown, 2003a). LER implemented in the 3D GARAND code is based on the 1D Fourier synthesis method using the power spectrum of Gaussian or exponential autocorrelation functions. The equations are expressed as follows:

$$S_G(k) = \sqrt{\pi}\Delta^2\Lambda e^{-(k^2\Lambda^2/4)} \quad (2.2)$$

$$S_E(k) = \frac{2\Delta^2\Lambda}{1+k^2\Lambda^2} \quad (2.3)$$

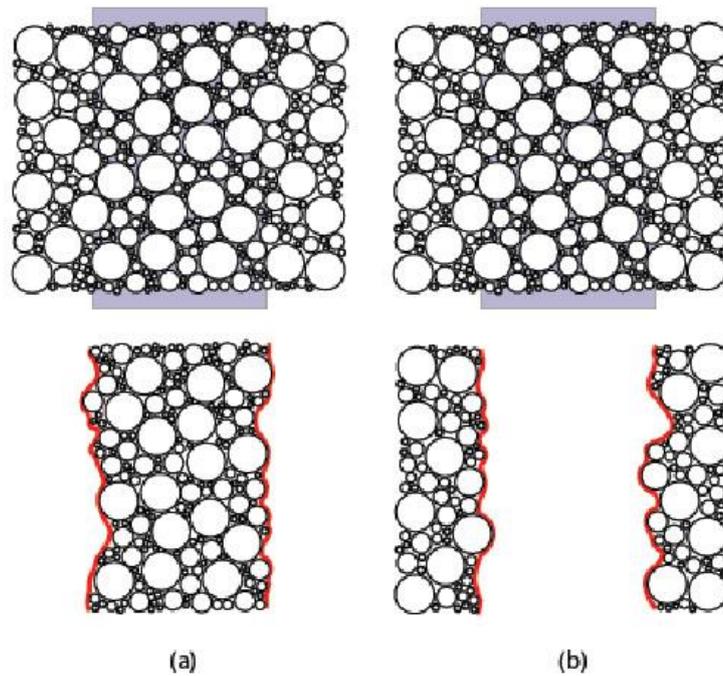


Figure 2-8: The impact of LER when using (a) positive and (b) negative, resist (G. D. Roy, 2005)

where $k = i(2\pi/N dx)$, dx is the discrete spacing used for generating the rough edge along the gate width in the range of $i=0$ to $N/2$ and N is the number of equally spaced samples along the channel width. In the simulator, the RMS value is defined as three times the RMS amplitude. Based on the equations 2.2 and 2.3, the line generated using Gaussian autocorrelation is smoother compared to the line generated using exponential autocorrelation, which is mainly due to the lack of higher frequency components in the Gaussian power spectrum. Figure 2-9 (a) shows the transmission electron microscopy (TEM) image of pattern transfer in sub-100 nm technology node illustrating the effect of LER. Figure 2-9 (b) clearly shows the impact of LER in the TCAD simulation transistor while Figure 2-10 illustrates the effect of ER in the simulation of a FinFET.

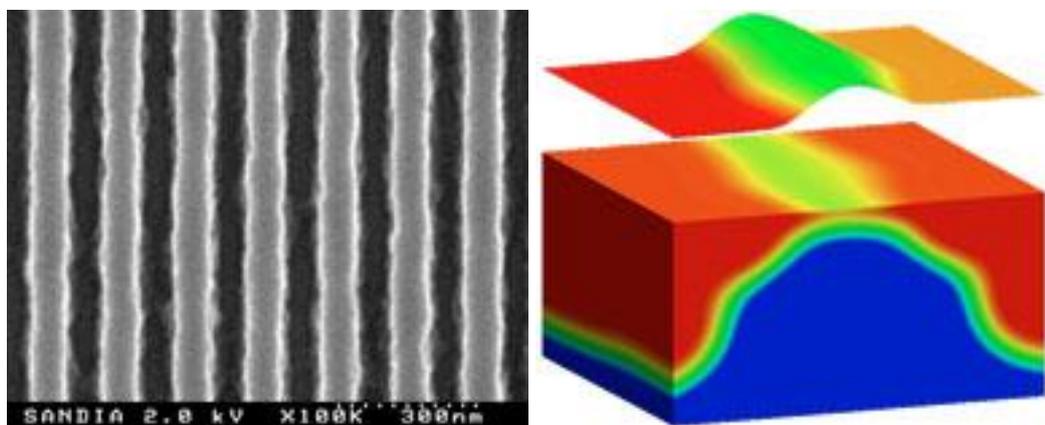


Figure 2-9: (a) TEM image of LER (Cardinale et al., 1999) and (b) effect on structure and potential in nanoscale MOSFET.

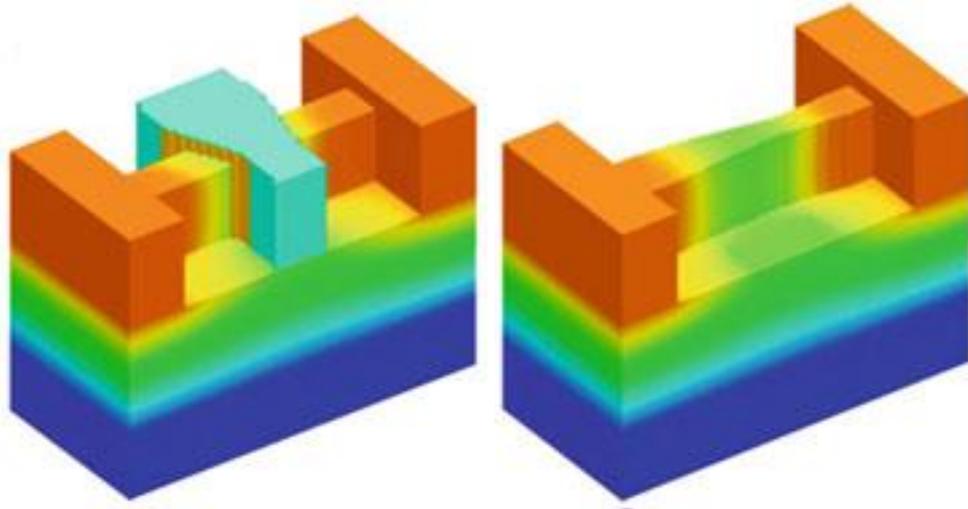


Figure 2-10: The effect on structure and potential electrostatics for (a) GER in FinFET and (b) FER in FinFET.

Previous experimental work on the 90 nm technology generation has found out that the impact of LER increases with the reduction of the channel length (Kim et al., 2004). An LER study reported in (Xingsheng, Brown, Idris, et al., 2011) shows that the impact on 14 nm bulk MOSFET is small compared to RDD. However, the LER effect becomes more significant in FinFET with the reduction of the doping concentration in the channel (Xingsheng, Brown, Binjie, & Asenov, 2011).

2.3 Oxide Reliability

Transistor reliability or ageing is due not only to nano wear-out defects, but also to built-in pre-existing oxide defects. Therefore, in new process technologies great attention is paid to the reduction of the defect density, especially by the enhancement in the quality of the oxide interface. If there is even a small number of defects in the gate dielectric in a deeply scaled transistor, it may introduce an intolerable malfunction in the corresponding circuit (N. Zanolla, D. Siprak, P. Baumgartner, E. Sangiorgi, & C. Fiegna, 2008). Therefore, oxide reliability becomes one of the essentials in the development figures of merit of new CMOS technologies. In the next subchapter, oxide defects will be discussed in conjunction with the reliability phenomena that contribute to the time dependent variability.

2.3.1 Oxide Defects

The SiO₂ gate oxide thickness of deeply scaled MOSFETs has reached its physical limits, in terms of leakage current and intrinsic reliability. Thus, the introduction of high- κ material (for example hafnium-oxide) becomes necessary in order to exploit further the advantages

of scaling. Transistors with high- κ gate dielectric have lower leakage current and improved gate dielectric reliability.

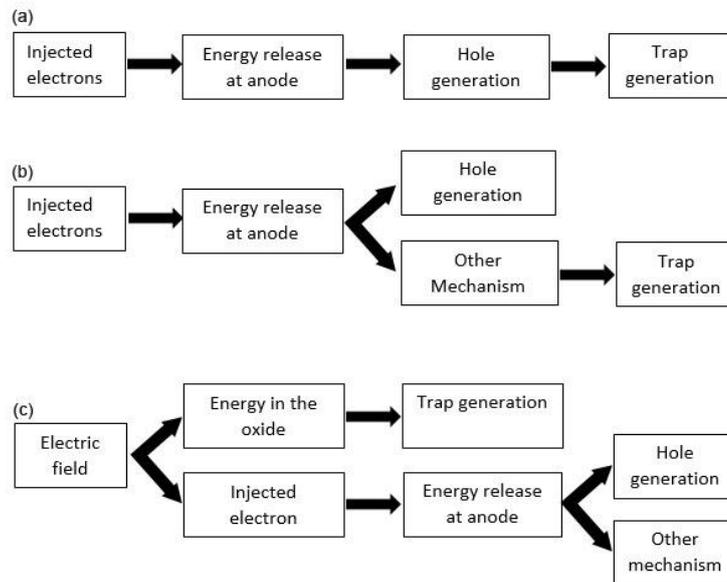


Figure 2-11: Outline of defect generation under stress. After ref (Degraeve, Kaczer, & Groeseneken, 1999)

There are three types of oxide degradation model to consider namely the anode hole injection, hydrogen release and electric field energy model, as illustrated in Figure 2-11. In the anode hole injection model (Schuegraf & Hu, 1994) an electron trap can be created by a hole tunnelling back to the cathode, resulting in the capturing of an electron in the high- κ dielectric conduction band. Several studies have shown that the interaction between holes and electrons in oxide results in a trap creation (Satake, Takagi, & Toriumi, 1997).

In the second model, the trap generation is determined by hydrogen release as shown in Figure 2-11 (b). In this model, the moving electron reaches the anode by tunnelling through the oxide potential barrier. This process produces sufficient energy to release a hydrogen atom from the oxide interface. The discharged hydrogen diffuses through the oxide and forms a trapped charge.

In the third model, the oxide defect is caused by the electric field itself, depositing enough energy to the oxide to create an electron trap. At present, the issue related to the energy released is independent from the charge trapping phenomenon.

2.3.2 Reliability Phenomenon

Electrically-active defects in the oxide are created mainly as a result of the disorientation of atoms which creates a new interface configuration in the amorphous band gap material. In order to understand this phenomenon, the basic nature of reliability should be understood. Silicon has a four valence electron in the outer shell. Therefore the silicon atom requires four bonds to make the outer shell saturated. For bulk crystalline structure, the silicon atom established their bond with its four neighbouring atom. This leads the outer shell of silicon atom saturated. However, at the bare surface, some of silicon atoms are missing. This will results unsaturated condition in the outer shell or creates electrically active dangling bonds which is known as interface trap as illustrated in Figure 2-12.

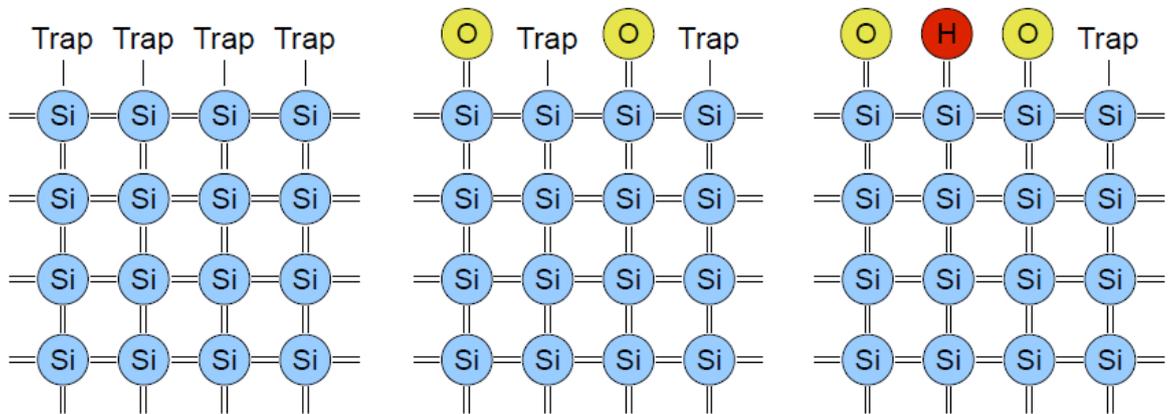


Figure 2-12: (a) unsaturated outer shell of silicon atom at the surface. (b) Thermal oxidation pairs for most of silicon atom at the interface with oxygen atom. (c) Some of empty bonds are filled with the hydrogen after annealing with the hydrogen ambient

The number of traps located at the interface varies statistically and commonly follow a Poission distribution. The Poission distribution characterize the probability that a number of events are happening for a certain period of time, if these events are happened with certain average rate and independently of time elapsed since the last event. For a given average number of traps, and the actual number of traps generated are random in nature for each simulation. Based on the mean of Poison distribution, each trapped charge is independently assigned to a random position at the interface between the oxide and the semiconductor. The next subchapter summarises the existing view of the reliability phenomenon in the MOSFET gate oxide.

2.3.2.1 Random Telegraph Noise (RTN)

RTN or “popcorn” noise, termed in reference to the shape of the signal, was initially observed in MOSFETS in 1984 (Ralls et al., 1984). RTN is manifested in switching current in the transistor between a high and low state as shown in Figure 2-13. RTN can be expressed by three parameters, which are the emission time (t_e), the capture time (t_c) and the amplitude ΔI_D . The emission and capture parameters are stochastic in their nature. The amplitude of the current change is a fixed quantity and can be determined by monitoring the signal output.

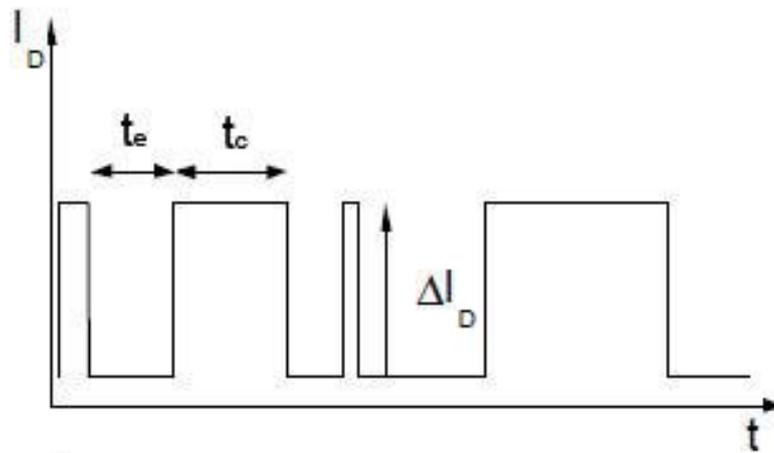


Figure 2-13: Schematic representation of a two level RTN defining the main parameters.

During transistor operation, traps located at the interface of SiO_2 can capture and discharge the charge carriers into the channel. If the trap captures a carrier, this will affect the number of carriers available for transport in the vicinity of the trapped charge. This will lead to a fluctuation in the drain current.

The impact of RTN can be expressed in the form of threshold voltage shift (ΔV_T) at a given fixed drain current as illustrated in Figure 2.14. This ΔV_T can be approximated by (Ghibaudo & Boutchacha, 2002; Simoen, Dierickx, Claeys, & Declerck, 1992; Sonoda, Ishikawa, Eimori, & Tsuchiya, 2007);

$$\Delta V_T = \frac{q}{C_{ox}WL} \quad (2.4)$$

where q is the electron charge, C_{ox} is the gate oxide capacitance per unit area and W and L are the channel width and channel length of the transistor respectively (Bu et al., 2000; Tsai & Ma, 1994). The impact of RTN increases when the transistor dimensions are scaled down

due the increase in ΔV_T which is inversely proportional to the channel length and width as shown in Equation 2.4.

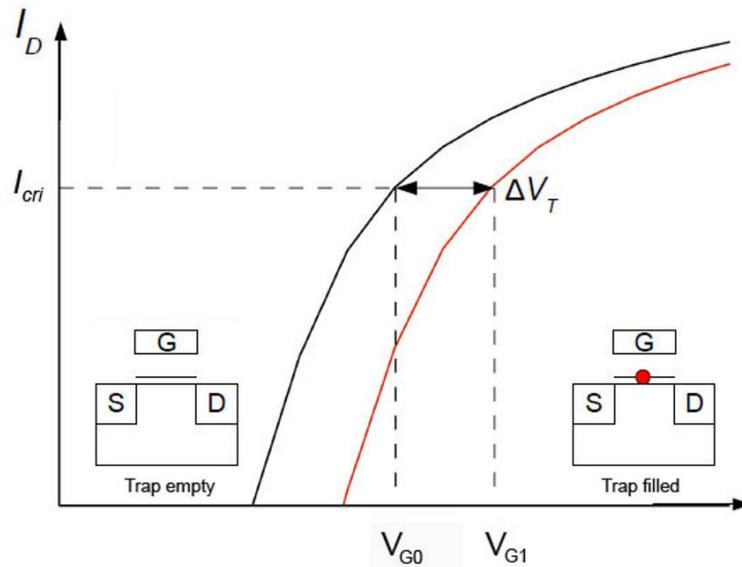


Figure 2-14: Definition of threshold voltage shift at a specific current criterion by RTN phenomenon (Ghibaudo & Boutchacha, 2002).

The impact of RTN on SRAM and flash memory becomes a major concern as the fluctuation of the threshold voltage compromises the performance of the read and write process (Kurata et al., 2007; Spinelli, Compagnoni, Gusmeroli, Ghidotti, & Visconti, 2008; Tega et al., 2006). RTN amplitude is experimentally shown to be widely scattered in otherwise identical transistors (Mueller & Schulz, 1997; Tsai & Ma, 1994). In reality, due to the interactions of the trapped charge and the rest of the variability sources the RTN amplitudes are higher than the simplified formula described above (Cai et al., 2008; Fantini et al., 2007; Ohata, Toriumi, Iwase, & Natori, 1990).

The unexpected behaviour of RTN, termed as a giant RTN, has been observed and several factors associated with this behaviour have been identified. The high amplitude of RTN fluctuation is partially due to the Coulomb scattering of trapped charge (Alexander, Brown, Watling, & Asenov, 2005; Hung, CHENMING, & CHENG, 1990; Simoen et al., 1992). Conventionally RTN is modelled as the charging and discharging of a single trap. However, the trapping of multiple discrete charges have also been suggested in (Tega et al., 2006) to describe large RTN magnitude. The inhomogeneous channel conduction conditions are also a significant factor in spreading the RTN amplitude creating high amplitude instances in the RTN distributions (Mueller & Schulz, 1998) (Simoen et al., 1992).

In recent studies into understanding the RTN in its interaction with statistical variability, the statistical spreading in the RTN amplitudes is reported to be dominated by RDD leading to anomalously high RTN amplitudes. The 3D simulation approach in (Asenov, Balasubramaniam, Brown, & Davies, 2000; Asenov, Balasubramaniam, et al., 2003; Fantini et al., 2007; Ghetti et al., 2008; A. Lee, Brown, Asenov, & Roy, 2003; Sonoda et al., 2007) demonstrated that a trapped charge in the critical percolation path induced by statistical variability can result in higher RTN amplitudes, compared to the predictions of simple 1D approximations such as Equation 2.4. BTI phenomena can also contribute to RTN, where the BTI recovery process can result in RTN events (Tibor Grasser, Aichinger, et al., 2011; S Mahapatra et al., 2007; S Mahapatra et al., 2011).

2.3.2.2 Bias Temperature Instability (BTI)

BTI is another type of degradation phenomenon, which is related to charge trapping and interface trap creation at the SiO₂ interface (V Huard, Denais, & Parthasarathy, 2006; Schroder, 2007). During CMOS fabrication, a post oxidation annealing process is performed in ambient hydrogen to passivate the dangling interface bonds. This reduces the interface trap concentration. However, over the lifetime of transistor operation, these passivated bonds are slowly broken leading to degradation in transistor performance. The impact of BTI becomes a significant concern for digital and analogue circuit designers as the transistor dimensions are scaled down. In particular, the aggressive scaling of the oxide thickness leads to an increase in the oxide field in the transistors in conjunction with the increasing operating temperature due to increasing power dissipation density. This results in the acceleration of bond breaking at the interface (M. A. Alam, Kufluoglu, Varghese, & Mahapatra, 2007; Schroder & Babcock, 2003).

The BTI phenomenon happens in both p-channel and n-channel transistors. In the p-channel transistor, this phenomenon is known as negative bias temperature instability (NBTI) which it is more pronounced in polysilicon gate transistors (V Huard et al., 2006). Figure 2-15 shows a CMOS inverter operating in high and low input states. The NBTI phenomenon corresponds to operating the CMOS inverter at low input bias and results in the generation of a positive charge at the interface of the p-channel MOSFET that leads to the degradation in transistor performance. On the other hand, the high input bias causes a stress which leads to the positive bias temperature instability (PBTI) phenomenon in the n-channel MOSFET (J. Zhang & Eccleston, 1998).

In the 45 nm CMOS technology with the introduction of high- κ gate dielectric, PBTI becomes compatible in magnitude and importance to NBTI (Hicks et al., 2008; Ioannou, Mitt, & LaRosa, 2008). This part is related to the particularly high electron trap density in the high- κ gate stack (Houssa et al., 2006; Zafar, Callegari, Gusev, & Fischetti, 2002).

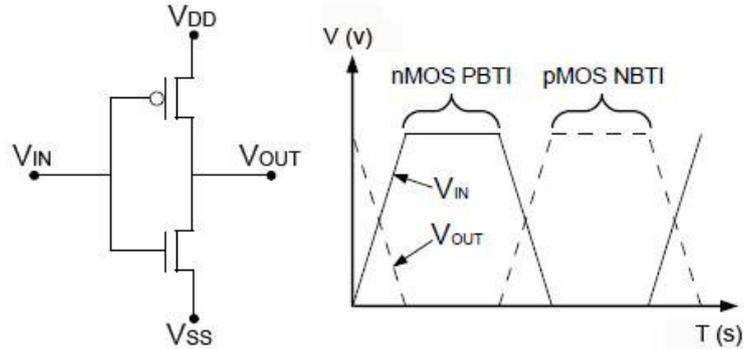


Figure 2-15: Circuit of CMOS inverter schematic (left) and timing diagram which illustrates the CMOS inverter operation (right).

The reaction diffusion (RD) theory initially proposed in (Jeppson & Svensson, 1977) has become the most prevalent description of BTI (M. A. Alam et al., 2007; Souvik Mahapatra et al., 2005; Ogawa & Shiono, 1995; Schroder & Babcock, 2003; J. Yang, Chen, Tan, & Chan, 2006). This model represents well the stress time dependence of transistor ageing due to the NBTI phenomenon. Later, the hydrogen diffusion model where a defect at the interface can capture the trap charge and result in a threshold voltage shift was reported (Tibor Grasser, Gös, & Kaczer, 2008; Houssa et al., 2005; Islam, Kufluoglu, Varghese, Mahapatra, & Alam, 2007; Kaczer, Arkhipov, Degraeve, et al., 2005; D Varghese et al., 2005; Zafar, 2005).

In more recent publications, Huard *et al.* (V Huard et al., 2006) suggested that the NBTI phenomenon was caused by a permanent reaction-controlled interface state creation phenomenon in (Haggag et al., 2001). Tewksbury in 1992 interpreted the NBTI phenomenon using recoverable elastic hole trapping (Tewksbury III, 1992).

2.3.2.3 Hot Carrier Injection

The degradation from Hot Carrier Injection (HCI) has been subject to numerous studies in the past (Hu et al., 1985; G.-H. Lee, Su, & Chung, 1995; Papadas, Revil, Ghibaudo, &

Vincent, 1995; Saks & Klein, 1993; Tam, Ko, & Hu, 1984) because it results in long term instability (Abbas, 1975; Hu et al., 1985), and is manifested by a threshold voltage shift contributing to a significant drive current degradation.

During the circuit operation, high electric fields occur in the transistor channel near the drain substrate junction due to the formation of the pinch-off region. At high drain bias, carriers traversing the high field region constitute a non-equilibrium energy distribution with a high energy tail (Duncan, Ravaioli, & Jakumeit, 1998) and as a result, the high concentration of energetic carriers leads to injection into the oxide near the SiO₂ interface causing trapping and new defect state generation (Baba, Kita, & Ueda, 1986).

The HCI modelling approach explains the degradation of the Si/SiO₂ interface with the creation of interface trapped charge because of Si-O bond breaking. The Lucky Electron model proposed in (Hu et al., 1985) is most widely adopted to capture the impact of HCI degradation. It is based on a lucky hot electron being accelerated by the electric field without suffering collisions and so acquiring very high energy.

The HCI phenomenon has been mitigated by the reduction in the drain voltage in the advanced technology nodes where due to the low voltages, the carriers cannot overcome the energy barrier at the interface to cause the bond dissociation (Bravaix et al., 2009). However, the impact of HCI has also been observed at lower voltages [103] and is still a relevant event in nanoscale transistors.

2.3.2.4 Soft Breakdown

Soft Breakdown (SBD) also known as quasi-breakdown is another type of dielectric failure. SBD is defined as current leakage below the predetermined level, which causes relatively little damage to the dielectric material. The SBD is associated with trap generation during the transistor operation which forms a conducting path which connects the channel and the gate (Degraeve, Groeseneken, Bellens, Depas, & Maes, 1995).

SBD is less pronounced in long channel transistors. It usually occurs near the drain, increasing the gate induced drain leakage (GIDL) up to a five-order magnitude (Pompl, Wurzer, Kerber, Wilkins, & Eisele, 1999). The impact of SBD is more severe in scaled down transistors. This can result in the trans-conductance gm drop by 50% and an ON current drop of about 30% from the fresh transistor values (Cester, Cimino, Paccagnella, Ghidini, &

Guegan, 2003). However, the understanding of the effect of SBD on gm, voltage shift or ON current drop is insufficient to explain the impact of SBD on small transistors. Therefore, extensive studies have been done on SBD by using scaled transistors, including oxide thickness and voltage scaling, which show that SBD is the primary mode of transistor failure for scaled ultrathin oxide transistors, and operating at low power. This is because of the significant power consumption during the breakdown process (Muhammad Ashraful Alam, Weir, & Silverman, 2002).

2.3.3 Time Dependent Variability

In the past, the transistor performance for relatively large MOSFETs in circuits was expected to degrade in a similar fashion, uniformly, when transistors were biased in similar conditions. Therefore, in the past, time dependent variability was not taken into account during transistor characterisation, measurements, modelling and simulation efforts. However, in short channel transistors, statistical ageing variability cannot be ignored. The variation in the number of trapped charges and their spatial positions from transistor to transistor becomes relatively higher, and continuously increases in the degradation process. The progressive stochastic behaviour of the electrical parameters in an otherwise identical transistor is a significant reliability concern in analogue and digital circuits. For example, in a current mirror circuit, it is important that both transistors remain closely matched (Rauch III, 2002). In digital circuit the degradation can affect the signal propagation resulting in timing violations.

Recently, several groups have proposed an advanced measurement technique to characterise more accurately the time dependent statistical variability (Denais, Huard, et al., 2004; Denais, Parthasarathy, et al., 2004; Rangan, Mielke, & Yeh, 2003; D Varghese et al., 2005; T. Yang et al., 2005). This phenomenon is dependent on the stress bias condition, stress time and stress temperature. The degradation in transistor performance can be described by a power law dependence on stress time (Goetzberger, Lopez, & Strain, 1973; Schroder & Babcock, 2003) and in accordance with the Si/SiO₂ interface RD model (Ogawa, Shimaya, & Shiono, 1995). The power law is expressed below:

$$\Delta V_T = A \exp(\beta V_G) \exp\left(-\frac{E_a}{kT}\right) t^{0.25} \quad (2.5)$$

where V_G is the applied gate bias, E_a is an activation energy, A and β are fitting coefficients.

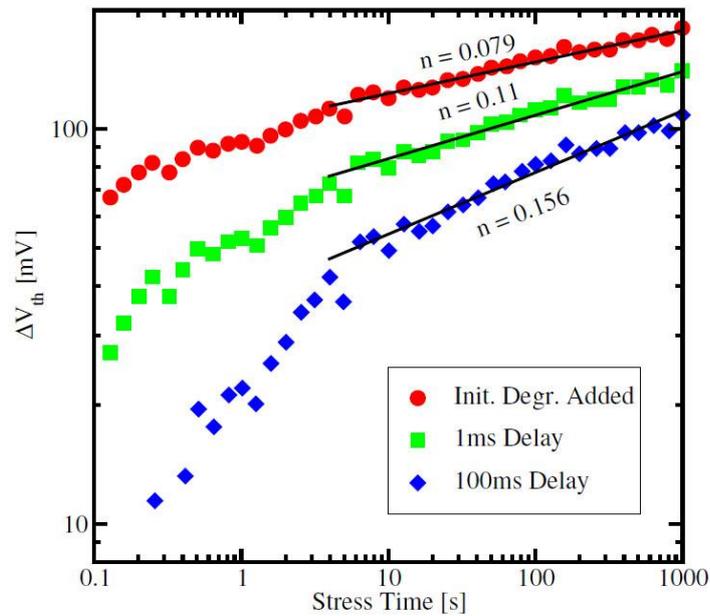


Figure 2-16: Initial threshold voltage shift measurement with the slow determination method after ref (Shen et al., 2006). Shows that the initial measurement has degradation and as a result the threshold voltage shift is underestimated.

In 2006, Shen identified the initial degradation stages using a slow measurement method (Shen et al., 2006). The ΔV_T is extracted by comparing the initial measurement and subsequent measurements. The initial measurements, showed that the transistor was already subject to a certain level of degradation, which means that the overall degradation is underestimated. Figure 2-16 shows the apparent ΔV_T with respect to time on a logarithmic scale. The measured distribution of ΔV_T at long delay (100 ms), shows clearly a kink in the power law. Further analysis has been done with respect to the temperature dependence (Muhammad Ashraful Alam & Mahapatra, 2005; Kaczer, Arkhipov, Jurczak, & Groeseneken, 2005; D. Varghese et al., 2005). Since the time dependence and temperature activation are not mutually consistent (M. A. Alam et al., 2007) the model is less accurate compared to the model described in (Vincent Huard, 2010; Kaczer et al., 2010; Teo, Ang, & See, 2009). However, recent studies based on many experimental observations, suggested that hole trapping is the major contributor to the degradation process (Ang, 2006; Tibor Grasser et al., 2009; V Huard et al., 2007; Reisinger, Blank, Heinrigs, Gustin, & Schlünder, 2006; Shen et al., 2006).

Numerical simulation studies show that the interplay between statistical variability effects and reliability phenomenon are essential for reproducing both the shape and magnitude of the distribution of the experimental data [RH-2]. The interaction between SV and the trapped charge in the CMOS transistor imprints a distinct statistical signature for the reliability phenomenon. Based on this concept, reliability simulation frameworks [RH-3, RH-4, 2-10]

were developed for better accuracy in understanding the time dependent statistical degradation. Figure 2-17 shows the distribution of time to failure obtained from the simulations of an uniform transistor and from simulations including SV sources (L. Gerrer et al., 2013). Therefore, the prediction of the degradation in the transistor performance is underestimated if the impact of statistical variability is neglected.

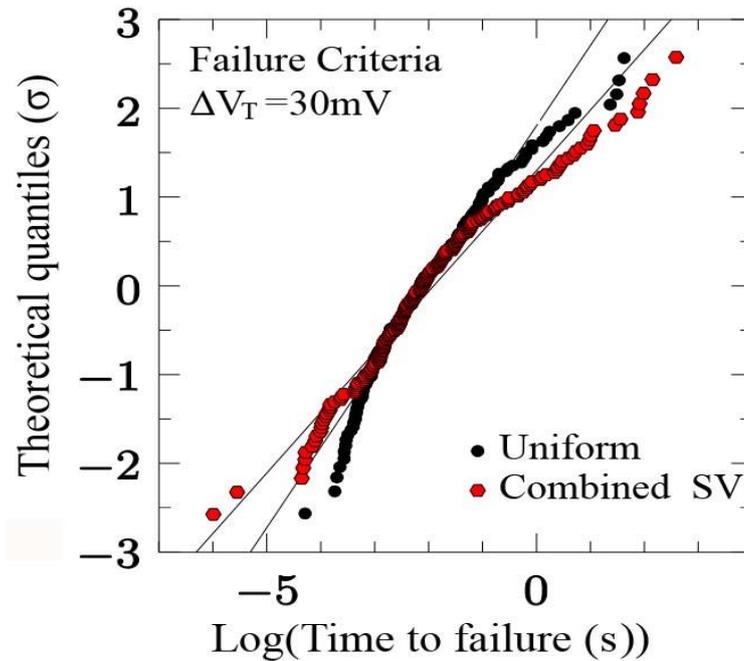


Figure 2-17: Distribution of threshold voltage for transistor failure at 30 mV in uniform transistor and combined SV [RH-3].

2.4 Modelling

State-of-the-art reliability modelling covers a wide range of areas related to the entire process of transistor manufacturing and circuit integration. The following are some of the main aspects of modelling typically covered by the TCAD simulation tools employed in this research (simulator).

There are three stages of simulations utilised in this work. The initial part includes the TCAD transistor design and characterisation using 3D simulation which are essential when statistical variability and reliability are taken into account. In the past, several approaches have been developed to include the time dependent variability (TDV) at circuit level (Martin-Martinez et al., 2009; Nafria et al., 2011), but they fail to capture the correlation between SV and statistical reliability. Therefore, a CM extraction technology is used to preserve a correlation between important transistor parameters. Finally, the circuit simulation is based

on the CM library extracted from the TCAD simulations employing advanced model generation technology ("GSS simulator,").

2.4.1 TCAD Simulation

In 1979, the commercial TCAD tools began with the formation of the Technology Modelling Associate (TMA), with process and advice simulation software developed under the supervision of Professors Dutton and Plummer. SUPREME3 and SUPREME4 (Dutton; Dutton) were the first one-dimensional and two-dimensional process simulators while PISCES (Dutton) was one of the first two-dimensional transistor simulators. However, due to the statistical nature of atomistic transistions, 3D simulations are necessary to capture the physicals of the different variability sources. The capability of the TCAD simulator should take into account the granularity of charge and matter. The 3D ‘atomistic’ simulator GARAND is the first simulator focused on statistical variability based on the diffusion approach to solve the semiconductor equations with a density gradient quantum correction (Asenov, 1998).

As the number of transistors in chips double roughly every two years, according to Moore’s Law (Moore, 1998), the need to use TCAD simulations become essential. The TCAD simulations provide deep insight and better understanding of the physical processes governing the operation of the modern semiconductor devices. The TCAD simulations reduce the time required for the development of new generations of the transistor. With the currently available computational resources, it is possible to have a virtual fabrication laboratory, which can predict the behaviour of a new transistor and its electrical characteristics resulting from a particular fabrication process with a reasonable degree of accuracy. This capability allows the optimisation of prototype transistors and technology within a short period of time as well as the reduction of the development costs.

The TCAD simulations have also become a vital tool in failure analysis, troubleshooting and performing reverse engineering. Failure analysis and reliability testing can be done realistically by incorporating statistical functionality into the TCAD tools.

2.4.2 Compact Modelling

The accuracy of any nodal-based circuit simulator is limited by the accuracy of the circuit component representation. Using some passive components such as a capacitor and resistor

to describe a complex and non-linear transistor is impossible and the MOSFET needs to be represented in circuit simulations using a computationally efficient compact model. A compact model consists of quasi-physical equations to describe the operation of a specific device or circuit element. The behaviour of the compact model can be tuned using the compact model parameters. Generally, in a compact model, transistors are treated as a 'black box' with input and output terminals. The functionality of the CM should capture the performance of the transistor in steady state and transient operation in all possible modes of operation including gate, drain and body bias dependences, channel length and width dependences, as well as temperature dependence. Apart from capturing the basic behaviour of an ideal MOSFET in which the transistor is considered as uniform, the compact model has to capture variability and reliability in order to fully represent realistic transistor performance and ensure accurate circuit simulation.

In the late 1980s, researchers from the University Berkeley in California developed the Berkeley short-channel IGFET model (BSIM) compact model, to allow accurate integrated circuit simulation and design. The main reason for the BSIM introduction was to incorporate the complex short channel effects (SCE) as a result of a rapidly changing transistor technology (Sheu, Scharfetter, Ko, & Jeng, 1987). Several improvements in the BSIM model have been introduced in order to match the advanced technology implemented in the transistor fabrication including halo doping and the inclusion of the stress.

Recent compact model development includes the introduction of surface potential compact model based in order to achieve a better physical representation of MOS transistor operation. The Penn State-Philips (PSP) model ("Psp model manual,"), has become the most popular one benchmarked to BSIM, that shows a few advantages (T. Zhang, Subramanian, & Haase, 2010), especially when considering statistical variability in circuit simulations (Moezi, Dideban, Cheng, Roy, & Asenov, 2013). The introduction of new transistor architecture, especially the 3D FinFET necessitates the development of a corresponding CM such as Tri-Gate architectures compact models (BSIM-CMG (Dunga, Lin, Niknejad, & Hu, 2008)) and SOI transistor compact model (BSIM-SOI, BSIM-IMG (Chen et al., 2011), UTSOI (Rozeau, Jaud, Poiroux, & Benosman, 2011)).

2.4.3 Circuit Simulation

A simulation program with integrated circuit emphasis (SPICE) or a SPICE derivative is the most widely used dynamic circuit simulator. There are the well-known SPICE-based

simulators such as Eldo from Mentor Graphics ("Mentor Graphics. Eldo,"), Spectre from Cadence ("Cadence. Spectre,") and Hspice from Synopsys ("Synopsys. Hspice,") and the open source simulator ngSpice ("ngSPICE. ngspice,") which are all derivatives of Berkely's SPICE.

The SPICE simulation concept is based on modelling the behaviour of an integrated circuit element with a set of first-order differential equation. The non-linear differential equations at each sampling point are discretised into time independent non-linear algebraic equations. Finally, these equations are iteratively solved by using the Newton-Raphson method until it reaches a required precision level.

A netlist or circuit description file is used to represent the circuit by using circuit components and connection nodes. In industrial practice, the netlist is extracted after layout optimisation steps; at this stage the netlist does not just consist of all circuit elements but also components from the interconnect parasitic extraction. The SPICE simulators can simulate a wide range of circuit modes of operation, such as transient analysis, DC analysis and noise analysis. At the moment, the SPICE simulation is the most accurate method for circuit simulation and verification depending on the accuracy of the compact model and the parasitic interconnection extraction. However, there are limitations in using such simulators related to the size of the circuit, and the corresponding computational (CPU) cost.

During this study, ngSPICE has been used as a back-end circuit simulator for RandomSpice. ngSPICE is an open source version of Berkeley's SPICE3 which is relatively slower compared to the industrial equivalents. One of the advantages of ngSPICE is that, as an open source software it is not limited by the licence cost and can be used in parallel on high performance computer (HPC) clusters, which dramatically speeds up the simulation for large statistical data sets.

For the purpose of statistical analysis, some results are illustrated in the standard deviation or sigma value. The sigma value is a measure value to quantify the dispersion of a data value, for example dispersion of threshold voltage σV_T or dispersion of ON Current σI_{ON} . Due to limitation in TCAD simulation time, only 1000 device per TCAD device simulation are being simulated. This number is good enough to analyze the trend for a specific parameter. This value corresponds to a 3σ value which is the TCAD simulations cover almost 99.73% of the probability. For industrial practice, it should cover up to 5σ or beyond. Figure 2-18 illustrated sigma value in a normal distribution.

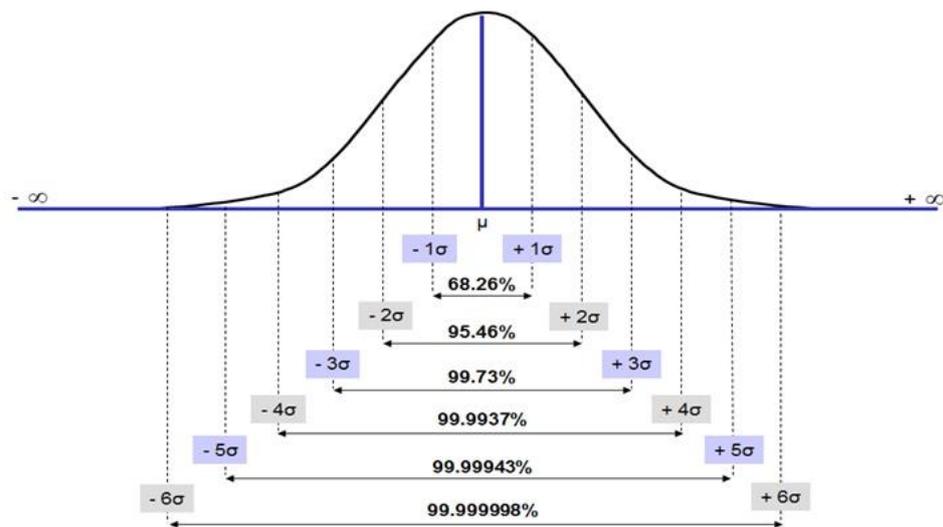


Figure 2-18: Sigma value for a uniform distribution

The data set in Figure 2-18 can also be represented in a theoretical quantiles plot. This plot helps to determine the shape of the distribution, based on properties such as location, scale, and the skewness of the distribution. Theoretical quantiles are a sorted set of data in ascending order. Then this data is plotted versus the theoretical distribution. A quantile is a fraction where some value falls below that quantile. For example, the median is a quantile where half of the data set falls below that point and the remaining are above it. Figure 2.17 illustrates the example of a qq plot.

2.5 Summary

In this chapter, an extensive overview of the CMOS transistor variability was presented. The stochastic nature of the 'atomistic' transistor where variability plays an important role has been discussed. The effect of transistor scaling and its impact on statistical variability becomes more severe. Oxide reliability is another crucial phenomenon in determining transistor performance and also becomes vitally important when transistor dimensions are shrinking. The simulation of the oxide reliability phenomenon is not accurate enough without the inclusion of statistical variability into the transistor and circuit simulation. Finally, the importance and the need for accurate statistical simulation in the TCAD and in the circuit simulation domain have been discussed with respect to the compact model extraction methodology.

Chapter 3: Methodology

Background

The simulation methodologies adopted throughout this research are discussed in this chapter. Technology computer aided design (TCAD) tool chains, have been employed for the purpose of calibrating the test device, perform physical device simulation of statistical variability and statistical reliability, statistical CM extraction, and statistical circuit simulation. Chapter 3 is organised as follows. Section 3.1 discusses the overall simulation flow based on the Gold Standard Simulation (GSS) TCAD tool chains. The corresponding device and circuit simulations are presented in 3.2.

3.1 GSS Simulation tool chain

Figure 3-1 illustrates the simulation tool chain used in this research. It comprises a device structure generator Monolith with an analytical process simulator Anadope, 3D statistical ‘atomistic’ TCAD simulator GARAND, the statistical CM extractor and generator Mystic, and the statistical circuit simulator engine RandomSpice. The tools are executed on high performance clusters in order to efficiently manage the computational resources so that thousands of submitted jobs can run at any one time to deliver speed for larger statistical simulation data. The main reason of this tools chain have been chosen for this project is the ability to perform a statistical analysis in the circuit simulation domain which are not supported yet from any commercialized tool.



Figure 3-1: GSS tool chain simulator from technology definition to the statistical circuit simulation (simulator).

3.1.1 The automation tool Enigma

Enigma is an automation tool for TCAD environment. It provides the capability to efficiently evaluate the technology changes and their impact on device performance in TCAD simulation and circuit performance in circuit simulation. This tool can be programmed to automate the calibration on the generation of uniform and statistical TCAD data, nominal and statistical CM extraction, library generation and circuit simulation based on the simulation data. In addition, the statistical device and circuit simulations and the statistical reliability simulation can be added into Enigma flow. Figure 3-2 shows the schematic diagram of the workflow of Enigma with all of the important TCAD steps, which are fully integrated and automated for efficiency, and speedy analysis of the important design figure of merits. The other important aspect of the Enigma workflow is the management of the database. All device parameters and simulation data are stored in the database under a specific project. This makes it easy to fetch the data for analysis and visualisation. However, during the time when the work presented in this thesis was performed, the Enigma automation tool was in its early development stage. The calibration of the TCAD deck has been performed manually from a doping profile using Anadope and the calibration of $I_D V_G$ simulation data against experimental data using the Drift Diffusion simulator.

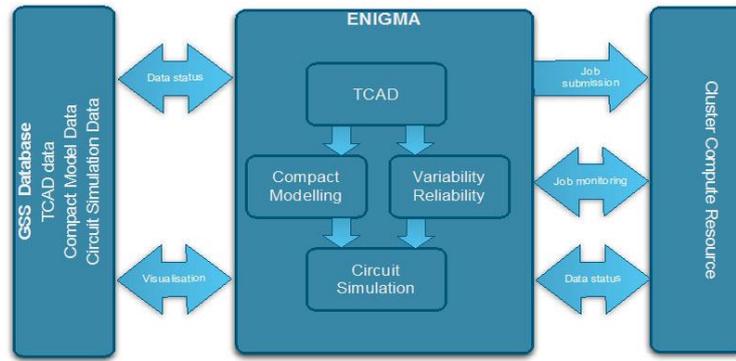


Figure 3-2: Enigma Simulation tool chain developed by GSS (simulator)

Anadope is an analytical process simulator, allowing the doping profile to be introduced in the simulation structure (L. Wang, Brown, Cheng, & Asenov, 2012, 2013). It has an analytical implantation module using a Pearson's distribution function (Wilson, 1980) taking into account the ion implantation in the 3D structure. The advantages of using Pearson distribution is the more realistic doping distribution in both source/drain regions, extension, halo and retrograde channel doping.

3.1.2 3D Density Gradient corrected Drift Diffusion simulator

The workhorse of this research is, the 3D atomistic simulator GARAND which will be discussed briefly in this section. Several techniques can be used to study the characteristics of semiconductors, including Non-equilibrium Green Function (NGEF), Monte Carlo (MC) or Drift Diffusion (DD) (Ravaioli, 1998). Each of these is based on different approximations to the charge transport module and therefore a trade-off between computational effort and the ability of the simulator to predict accurately the device transport properties and to predict the current voltage characteristics.

The DD simulator GARAND, has been developed in the Glasgow Device Modelling Group and lately by GSS. It solves the Poisson equation self-consistency with the current continuity equations. The Poisson equation is shown below.

$$\nabla \cdot (\epsilon \nabla \psi) = q(n - p + N_A^- - N_D^+) \quad (3.1)$$

Where ϵ is the dielectric permittivity, ψ is the electrostatic potential, q is the elementary charge, n and p are the electron and hole carrier densities and N_A^- and N_D^+ are the ionised acceptor and donor doping concentration, respectively. The current continuity for electrons given in equation 3.2,

$$\nabla \cdot J_n = 0 \quad (3.2)$$

Where J_n is the current density. In the DD approximation, the electron current density is approximated by carrier drift and diffusion terms.

$$J_n = qD_n \nabla n - qn\mu_n \nabla \psi \quad (3.3)$$

Where μ is the carrier mobility and D_n is the diffusion coefficient. The first term on the right represents the diffusion current, which is a motion of carriers due to the concentration gradients in the system. The second term on the right represents the drift current, which is a motion of carriers in response to electric field applied to the system.

The DD simulation approach is a charge transport model derived from the Boltzmann transport equation (BTE) (Tibor Grasser, Tang, Kosina, & Selberherr, 2003) which is based on approximations and simplifications. The DD approach cannot capture accurately nonequilibrium carrier transport. The DD relies upon carrier mobility models, which take into account channel doping and electric field dependencies (Shapiro, 1967).

The incorporation of quantum corrections (Ancona & Tiersten, 1987) into the drift diffusion approach facilitates the simulation of contemporary nanoscale devices. The DD approach assumes local relation between mobility and electric field and therefore cannot capture non-equilibrium transport effects. In reality, for a short channel device, the lateral field varies rapidly, and the carriers require a finite time and distance to respond to the field. Therefore, carrier velocity overshoots the saturation velocity, which cannot be taken into account in the DD approach (Tibor Grasser et al., 2003; Lundstrom & Datta, 1990).

The capability of DD simulation to capture quantum confinement effects extends to aggressively scaled technology nodes by using density gradient (DG) corrections. The DG quantum corrections improve the accuracy of the simulation results in the deep submicron regime where the effect of quantum confinement has a significant impact on the device characteristics. The introduction of DG corrections to the DD approach involves the introduction of an additional term to the current density equation based on the so called ‘effective quantum potentials’. The current density equation is shown in equation 3.4,

$$J_n = qD_n \nabla n - qn\mu_n \nabla \psi + 2qn\mu_n \nabla \left(b_n \frac{\nabla^2 \sqrt{n}}{\sqrt{n}} \right) \quad (3.4)$$

Where b is related to the density gradient effective mass and has at the form of ($b_n = \frac{\hbar^2}{4m^*qr}$). The introduction of DG corrections into the DD approach capture accurately quantum confinement and tunnelling (Tibor Grasser et al., 2003). The simulation results based on the DD model and DG corrections have been shown to be sufficiently accurate for a device in the 22 nm technology generation (G. Roy, Brown, Adamu-Lema, Roy, & Asenov, 2006).

The combination of Poisson's equation (Equation 3.1), the current continuity equation (Equation 3.2) and the DG correction equations are solved by using the Gummel iteration method (Gummel, 1964). The advantage of this approach lies in its efficiency and ease of simulator development. The relatively low simulation time required to produce a current - voltage characteristic for a single transistor clearly make a DD simulator a suitable tool suited for the simulation of a larger statistical ensembles of microscopically different transistors.

3.1.3 Mystic: compact model extraction

Mystic is a compact model (CM) extraction tool developed by GSS. It is designed to capture the effects of process and statistical variability in transistor performance at circuit level. There are typically two CM extraction types that we have used in this work, which are uniform and statistical CM extraction. During uniform CM extraction, the model extraction process starts with the low drain electrostatic and is followed by a low drain transport parameter. The extraction continues with the high drain region and finally with the fitting of the $I_D V_D$ characteristic. This uniform CM will become a based model for the statistical CM extraction at different time-dependent statistical variability. The statistical variability CM extraction follows a similar process of parameter extraction as the uniform CM extraction. However, since this stage is using parameters generated during the uniform extraction stage, the process becomes simple and involves just one stage of extraction. The statistical extraction process can capture accurately TCAD simulation results in fresh device or ageing device. With the combination of the advanced GSS ModelGEN, statistical CM generation technology, this tool provides the capability to capture the complex correlation between CM parameters with transistor figure of merits. The ModelGEN also allow an interpolation at any arbitrary level of degradation for a proper statistical reliability circuit simulation. Thus, this makes the Mystic tools the only CM extraction tool which can provide a statistical simulation in circuit level. Figure 3-3 shows the process flow of the Mystic operation followed in this work.

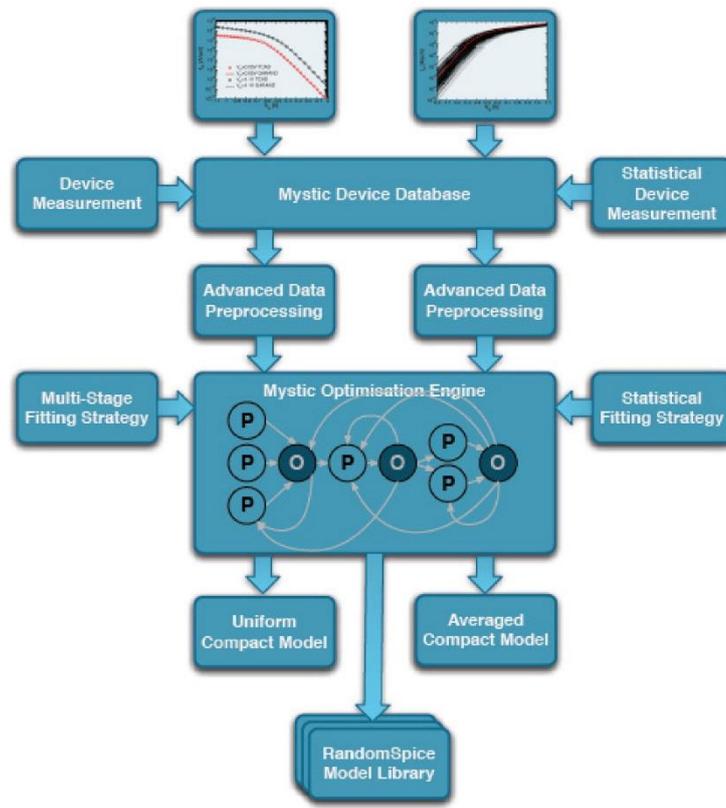


Figure 3-3: Compact model extraction strategy flow to generate the CM library using TCAD simulation results (simulator).

3.1.4 RandomSpice

RandomSpice is an advanced statistical circuit simulator. It is based on the Monte Carlo principle (Mooney, 1997), and supports multiple simulation programs with integrated circuit emphasis (SPICE) backend tools including HSPICE, Eldo and the open source simulator ngSPICE. RandomSpice is capable of handling the statistical circuit simulation of a transistor with the presence of process and statistical variability, which can accurately predict circuit behaviour and the highlight extreme cases that could characterise circuit failure mode. RandomSpice can also be employed in very large-scale circuit simulations in parallel using a high performance computer (HPC) cluster, which can save simulation time for a very large number of jobs that are required to accurately study the impact of variability and reliability on the circuit. In order to reproduce statistical variability and reliability simulation results, CM technology libraries are specifically generated to be used in RandomSpice. The CM is extracted directly from TCAD simulation results, as described earlier. RandomSpice also supports the CM generated by experimental data or CM generation methods including Gaussian V_T generation, principal component analysis (PCA) and the nonlinear power method (NPM).

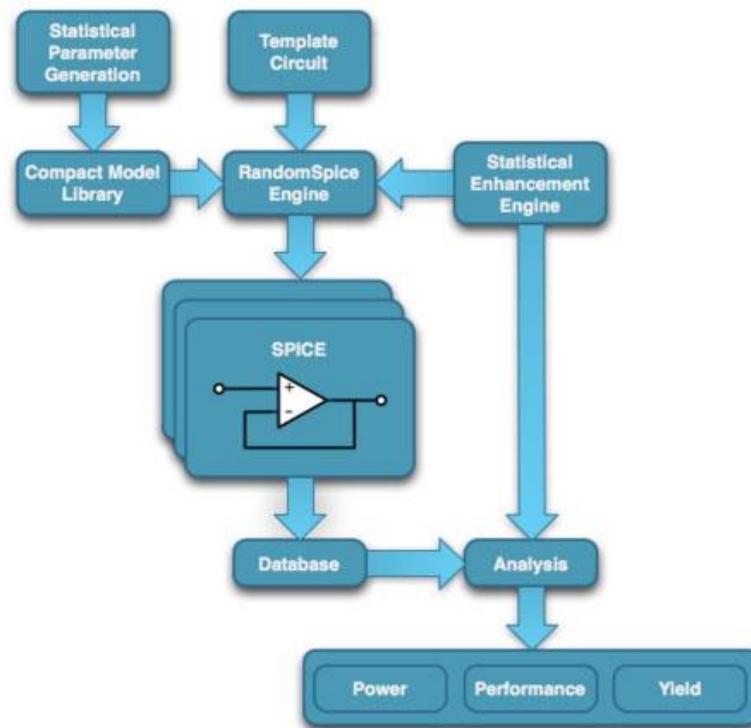


Figure 3-4: RandomSpice flowchart (simulator)

Figure 3-4 shows the RandomSpice methodology adopted in this work, which involves the creation of a basic template of a SPICE netlist. Through the integration with Mystic, GSS ModelGEN provides accuracy in high sigma simulation of modern designs utilising advanced algorithms. This gives an advantage for this RandomSpice to perform a statistical analysis much faster compare to FastSPICE Monte-Carlo without sacrificing the accuracy. It also provides an interface, which allows the annotation of a SPICE netlist for variability and time dependent variability simulation and generate extremely large ensembles of simulations. The flexible data-processing interface has the capability to intercept the simulation result and calculate and analyse performance figures of merit or interest at a particular given state. RandomSpice also provides an application programmed interface (API) for direct integration with databases and data management framework, allowing complex behavioural characterisation to be performed.

3.2 TCAD Simulations

This section focuses on the capabilities of the TCAD simulation tools used in this work to perform simulation of the continuously doped, ‘atomistic’ device at time zero (fresh device) and the time dependence variability. In this simulation, the statistical 3D atomistic simulator has been employed. In the following subsection, the inclusion of the different SV source in the fresh device simulation and the statistical reliability simulation are described.

3.2.1 Statistical variability simulation

Several works have been carried out in the Device Modelling Group at the University of Glasgow to investigate the impact of SV on the main parameters of device performance (Asenov, 1998; Asenov, Brown, Davies, Kaya, & Slavcheva, 2003; Asenov & Saini, 2000; G. Roy et al., 2006). The continuously doped uniform device is used to create a statistically significant sample of the device containing variability sources, namely RDD, LER and PSG or MGG (depending on the gate material used in fabrication). These SV sources have become important in the last two decades, as the device dimensions have headed into the nanoscale region. They will affect the design and yield and this is a major problem in circuit and system level operations in the current and future technology nodes. Therefore, due to their atomistic nature, it is important to incorporate them in the simulation.

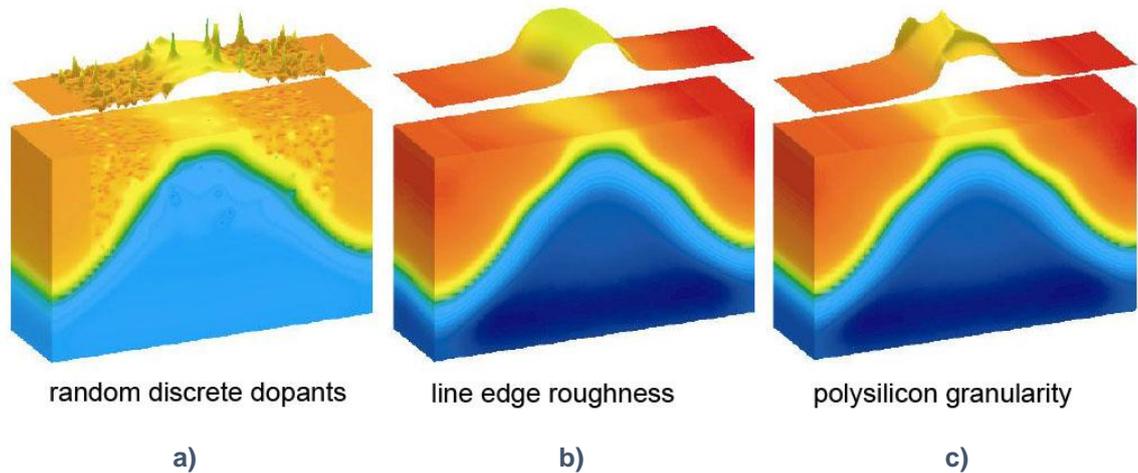


Figure 3-5: Show the impact of individual SV sources, namely (a) RDD, (b) LER and (c) PSG (Asenov, Roy, et al., 2008).

Figure 3-5 shows the individual impact of SV source having a different impact on the potential profile and carrier distribution. The RDD is introduced based on the continuous doping profile obtained from conventional process simulation. A standard method to assign discrete dopants according to the continuous concentration involves visiting, one by one, each site of the Si lattice covering the device (Frank, Taur, Jeong, & Wong, 1999). A Von Neumann rejection technique is used to decide whether to introduce a dopant at the Si site. Finally, the discrete dopants are transformed into a doping density assigned to the neighboring mesh nodes using the charge assignment scheme. In DD simulations this results in artificial charge trapping wells which in physical reality would be prevented due to a quantisation. To avoid this problem, attempts are made to split the Coulomb potential into long-range and short-range parts (Ezaki, Ikezawa, Notsu, Tanaka, & Hane, 2002; Sano,

Matsuzawa, Mukai, & Nakayama, 2000) . Density gradient quantum corrections are the physical way to avoid artificial carrier trapping.

The LER is introduced in GARAND by using 1-D Fourier synthesis, as described in (Asenov, Kaya, & Brown, 2003b). The two parameters controlling the LER are RMS amplitude (Δ) and correlation length (Λ). Following the usual LER definition, the values for LER magnitude correspond to $3\Delta = 4$ nm and correlation length, $\Lambda = 30$ nm have been used to generate random source/drain and gate edges introduced by the roughness of the resist and the following gate patterning process which is a reasonable approximation in contemporary CMOS technology.

The PSG is introduced by including a pinning of the potential and the doping nonuniformity in the poly-Si gate along the grain boundaries. At this stage, it is assumed that the density of pinning states is sufficiently high, and therefore, the Fermi level is firmly pinned in the silicon band gap at the position of the pinning states, independently of the poly-Si doping concentration and applied gate and drain voltages. To introduce a realistic random grain structure in the simulations, a large atomic force microscopy (AFM) image of polycrystalline silicon grains has been used as a template. This poly-Si grain-size distribution depends strongly on the deposition and annealing conditions. Therefore, in the simulations, the image is scaled so that the average grain diameter can replicate an experimentally observed average diameter, and then, a rasterized template image is saved in a format that is readable by the simulator.

Within this SV parameter, RDD makes a major contribution effect to nano-scaled devices, followed by PSG and LER. The overall impact of statistical variability in device performance cannot be assumed directly by the summation of all SV sources. Therefore, it is important to introduce the SV systematically individually and in a combined manner.

3.2.2 Statistical Reliability Simulation

Degradation in device performance is one of the major issues in the semiconductor industry (K. Kuhn et al., 2008; Tuinhout, 2002). The degradation associated with the charge trapping in the stress-generated defect state at the interface of the channel and/or deep into the gate stack dielectric has become more concerning (Fischer, Amirante, Hofmann, et al., 2008; Rauch III, 2007) and their relative impact has also become intolerable (N Zanolla, D Siprak, P Baumgartner, E Sangiorgi, & C Fiegna, 2008) in particular when devices are scaled down.

Therefore, the oxide reliability has become a vital issue that needs to be addressed as device dimensions shrink.

For this study, both random telegraph noise (RTN) and bias temperature instability (BTI) are analysed in a steady state conditions. In RTN simulation, a single charge trap is introduced at the interface between the channel and gate oxide, following a uniform statistical distribution across the channel area. In order to performed this simulation, a kinetic Monte Carlo (KMC) which is coupled to GARAND as described in (Salvatore M Amoroso, Gerrer, Markov, Adamu-Lema, & Asenov, 2012) has been used. The interaction between SV and TDV led to a drastic performance shift when a trap happened to be located in the primary current percolation path. The cumulative distribution of traps that induced threshold voltage shifts ΔV_T is compared to the experimental data obtained from time dependent defect spectroscopy (TDDS) from which individual trap impact on the threshold voltage has been extracted (Asenov, Cathignol, et al., 2008; Franco et al., 2012; Tibor Grasser, Reisinger, Wagner, & Kaczer, 2010).

In the statistical BTI steady state analysis, the average trapped charge density associated with the threshold voltage shift observed in BTI measurements of large self-averaging structures are translated into discrete trapped charges in a microscopically different ensemble. With the assumption that all the charges are trapped at the Si/SiO₂ interface, a fine, auxiliary 2D mesh is imposed at the interface. A rejection technique is used at each node of this mesh to determine if a single positive charge is located at that node or not based on a given real charge sheet density. If it is determined that a single charge should be placed there, then the charge is assigned to the surrounding nodes of the 3D discretisation mesh using a cloud-in-cell charge assignment scheme. The average trapped charge density is evaluated with the increase of an average trap sheet density from 10^{11} to 10^{12} cm⁻² following the experimental result from (Toledano-Luque et al., 2011). The distribution of trap density used in this simulation is Poissonian.

3.3 Compact model extraction using Mystic

The simulation results of the statistical TCAD simulations can be used directly to generate the CM library. For this purpose, the statistical CM generator from GSS, Mystics, provides a scriptable option, which can use several optimisation algorithms such as Levenberg-Marquardt (Moré, 1978), Bounded Trust Region (Alexandrov, Dennis Jr, Lewis, & Torczon, 1998) and derivative free optimisation methods such as Constrained Optimisation BY Linear

Approximation (COBYLA) (Marazzi & Nocedal, 2002). In order to develop the extraction strategy using Mystic, a deep understanding of the behaviour and limitation of the CM is essential in conjunction with underlying device physics. Mystic also allows the use of multiple extraction strategies, which are needed for statistical CM accuracy by using different parameters and device operation targets. This extraction strategy for the nominal CM and a statistical CM will be described in the next section.

At this extraction stage, a Berkeley Short-channel IGFET Model (BSIM) CM is used. Numerous iterations of BSIM model have been introduced to facilitate the advancement in fabrication technology. This BSIM model also includes a tri-gate architecture (BSIM-CMG) and SOI transistor (BSIM-IMG). In this thesis, BSIM4 is used as outline in ("BSIM 4," 2016) for the bulk MOSFET and BSIM-CMG for the FinFET.

3.3.1 Uniform compact model extraction

The uniform CM is a base model for a specific MOSFET, which can later be updated using variability sources for the purpose of statistical simulation. This model represents an ideal device performance, based on uniform doping condition as well as ideal device geometry. The CM library can also be extracted based on average device measurement or results data from a simulation of the calibrated device. The CM takes into account several dependencies, such as drain bias dependence, gate bias dependence, temperature dependence, channel length dependence and channel width dependence. Since the variability is not taken into account at this stage, the 2D simulation of the TCAD device is enough for the purpose of the CM extraction. In order to start the CM extraction, basic and physical parameters need to be incorporated in BSIM4 with sensible initial conditions. For example, the V_{TH0} (long channel threshold condition) parameter is initialised at 0.5 V at low drain threshold voltage.

In order to obtain the nominal set of BSIM4 parameters which can accurately capture the behaviour of a targeted device, a combination of local optimisation and a group extraction strategy is employed. The extraction is based on a simulation result from a set of devices with a drain current response, substrate bias response as well as gate bias response. It is important for the extraction strategy to retain as many physically relevant parameters as possible. The physical parameter introduced at an early stage should be preserved if possible throughout the extraction process and the optimisation process is achieved by using the availability of fitting parameters. The basic idea of optimisation in a fitting parameter is based on the effects they have on a specific region during the device operations.

The process of extraction of an accurate nominal CM poses several challenges, which are strongly related to the specific technology being used and which CM implementation have been adopted. This is because there are many physical parameters that can be used as a fitting parameter. It is often difficult to disentangle a correlated parameter in order to provide a stable solution. For example, the physical effects in a short channel device negates the simplification that has been made in the long channel device, with non-equilibrium transport effect and quantum mechanical effect giving serious impact to the device performance. While an advanced SPICE model such as BSIM4 provides the ability to model these effects, it is difficult to accurately capture their relative importance based on transistor performance.

The large number of optimisation parameters also raises another challenge as well as the complex correlation between them and the corresponding transistor characteristics. The combination of a larger number of fitting parameters and a large set of data in the optimisation process produces a highly complex parameter search space and many possible intermediate solutions. Therefore, the numerical optimisation is steering towards a global minimum solution with relevant physical parameters, which are suitable for a statistical extraction, and such optimisation process involves compromises and a large number of iterations.

3.3.2 Statistical compact model extraction and generation

This is the second stage of compact modelling. It involves the statistical variability due to the discreteness of charge and matters captured in the statistical TCAD simulations (Cheng et al., 2010). First, analysis of the available parameters which can be used in the optimisation is required. Based on a sensitivity analysis, a set of CM parameters is chosen for the statistical extraction process and then using the BSIM4 model, it is necessary to re-extract for each microscopically different device simulation. This results in a statistical library in the form of a lookup table which can be used for statistical circuit simulations. The accuracy of the statistical CM depends on the choice and the number of statistical parameters used and the specific extraction strategy adopted in the extraction process. The strategy proposed by Cheng (Cheng et al., 2010) is statistical parameter extraction based on a global optimisation that uses the least mean square algorithm approach. The results of using this method show good agreement with the targeted data. However, the drawback of this method is that it does not always capture the device performance figure of merit accurately and is not suitable for advanced accurate CM generation strategies.

Another drawback of the direct use of the extracted statistical CMs relates to the number of microscopically different devices physically simulated. The sub-sampling problem occurs in the Monte Carlo-based circuit simulation, which introduce unphysical artefacts. However, this problem can be avoided by using the CM generation approach. In this approach, the extracted statistical parameter distributions are used by statistical generation strategies to generate new random devices by replicating the extracted parameter distribution whilst taking into account the correlation between extracted parameters. The accuracy of the generation strategy is essential in replicating an infinite ensemble of devices, which will accurately reproduce the statistical results of the targeted device.

The CM generation can achieve simple methods such as principal component analysis (PCA) (Jackson, 2005), but this approach has an intrinsic limitation. In PCA methods, the variables are assumed to follow a Gaussian distribution where the mean and standard deviation are matched while retaining the correlation between parameters. Therefore, this method is only accurate as long as the targeted device has a Gaussian or near Gaussian distribution for extracted statistical parameter sets. The most advanced NPM approach is a moment matching technique where the parameter distribution matches accurately the first four moments (mean, standard deviation, skew and kurtosis). The advantages of generating the statistical distribution using the NPM method become apparent when the extracted statistical CM parameter has a non-Gaussian distribution. However, this method suffers from stability issues and has a limit in terms of the shape of the parameter distribution.

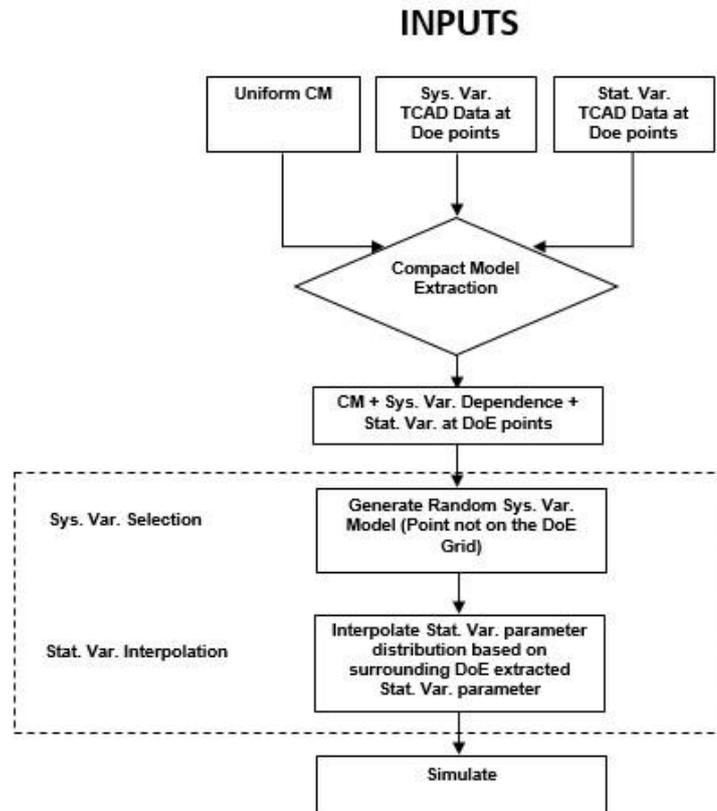


Figure 3-6: Flowchart for Statistical CM extraction and generation ensuring the accuracy across the whole Systematic Variability space and capturing the Statistical Variability correlation at arbitrary points (X. Wang et al., 2015).

The limitation in the PCA and NPM approach has been resolved in the latest GSS ModelGen technology by employing more flexibility in the distribution fitting method. Figure 3-8 shows the flowchart for the CM extraction and generation statistical model. The method of statistical CM generator is based on two steps, which consider the impact of Systematic Variability in isolation to generate a random Systematic Variability model. The accuracy of generating random Systematic Variability is based on the response surface of the CM. At this stage, the Statistical Variability Model extraction is assumed to be dependent on the geometry of the device such as length, width and height. Secondly, both Systematic Variability and Statistical Variability are included together in the generation process. The Statistical Variability model parameter is dependent on the specific process variable. The approach of GSS ModelGen to generate accurate statistical CM capturing the statistical variability at specific points of the process variation space is done by extracting the statistical parameter distributions at each point of the nearest node of the DoE space while their correlation is interpolated to the specific process geometry. This approach can be used to generate an arbitrary number of Statistical CM, which accurately reproduces the non-Gaussian statistic parameter distribution and their correlations.

3.4 Circuit Simulations

In this section, the circuit simulation tools used in this work are described together with the method for the 6T-SRAM circuit performance evaluation. The RandomSpice circuit simulator has been employed for the simulation.

3.4.1 Circuit Simulation using Random Spice

The RandomSpice circuit simulator which has been used is capable of simulating the circuit associated with the presence of process and statistical variability as well as statistical reliability. The Monte Carlo simulation engine in the RandomSpice simulator supports various SPICE simulations such as Mentor Graphic Eldo, Synopsys HSPICE and ngSPICE. This tool also allows a large-scale parallel simulation on a high performance computer (HPC) using a large number of circuit simulations. This capability gives advantages in the statistical simulation, simplifies the study of a large sample of circuits and speeds up the design process.

In order to reproduce the statistical variability and reliability of the calibrated device, a specific CM library is needed. These specific compact models can be extracted directly from the electrical measurement or TCAD simulation results from a well calibrated device.

A standard 6T- SRAM cell circuit is used in this simulation together with the specific CM library extracted from the TCAD simulation results. The fabricated SRAM usually has a trade-off between cell stability, the ability to read and write, leakage and cell area, which can be evaluated accurately with the presence of statistical variability and reliability for ageing devices. The analysis of SRAM performance can be evaluated by static noise margin (SNM) (Lohstroh, Seevinck, & De Groot, 1983), write margin (WRM) (J. Wang, Nalam, & Calhoun, 2008), read current (Fischer, Amirante, Huber, et al., 2008) and access disturb margin (ADM) (Wann et al., 2005). However, for the purpose of this work, only SNM, is considered when studying the SRAM performance. Details of the simulation setup will be explained in detail in Chapter 6.

3.4 Summary

In this chapter, the comprehensive simulation methodology used in this thesis has been outlined. These include the TCAD simulation flow focusing on statistical variability and

statistical reliability, followed by the extraction process for the uniform and the statistical CM. Finally the simulation process performed in the circuit simulation is described.

The CM parameter extraction is performed using GSS Mystic starting from the nominal CM extraction and based on a calibrated uniform device including drain gate and back bias dependencies. For the statistical CM extraction, the atomistic device simulation results are used. Parameters to corresponding atomistic devices are extracted separately in order to preserve the correlation between them.

The 3D atomistic simulator, GARAND, is adopted for drift-diffusion simulation for both calibration purposes and to analyse the performance of the device. RandomSpice is used for circuit simulation and to evaluate circuit performance. The following chapter will examine the result of the calibration of a 70 nm planar MOSFET.

Chapter 4: 70 nm Bulk imec MOSFET TCAD Model

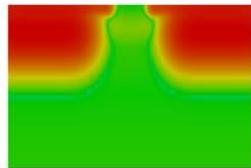
Background

The degradation of device performance in contemporary MOSFETs has become critically important over recent years (Hicks et al., 2008; Schroder & Babcock, 2003). The scaling of device dimensions has exacerbated this problem. This has resulted in the increase of random telegraph noise (RTN) (Salvatore Maria Amoroso, Adamu-Lema, Markov, Gerrer, & Asenov, 2012; Asenov, Balasubramaniam, et al., 2003; Ghetti et al., 2008; Kirton & Uren, 1989) and bias temperature instability (BTI) (Muhammad Ashraf Alam & Mahapatra, 2005; Tibor Grasser, Kaczer, et al., 2011; Kaczer et al., 2010; Rauch III, 2007; Schroder, 2007; Stathis & Zafar, 2006; Toledano-Luque et al., 2011), which are related to gate stack material defects. In order to investigate these phenomena, a transistor corresponding to 70 nm technology node developed at the Interuniversity Microelectronics Centre (imec) is used in this study. The first section of this chapter, presents the uniform device calibration with respect to the structure and electrical measurements resulting in good agreement with the targeted device data. The second stage follows with the atomistic calibration needed to accurately capture the statistical variability. In the third stage, a comparison of RTN distribution obtained from technology computer aided design (TCAD) simulation and experimental measurements is performed to validate the accuracy of calibration. Based on this calibrated TCAD device, the RTN and BTI degradation are studied in detail.

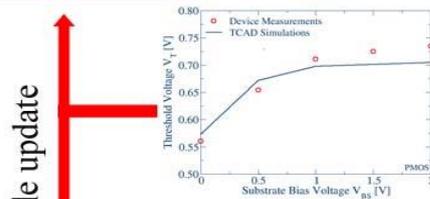
4.1 Uniform Device Calibration

The calibration methodology starts with the calibration of a continuously doped transistor, as illustrated in Figure 4-1. In the first step, the physical structure from the experimental data is extracted in order to define the simulation domain. By using analytical doping profile simulator AnaDope (L. Wang et al., 2012, 2013), a doping profile is generated and used in the 3D simulator, GARAND (simulator), to provide the current voltage (IV) characteristic. In the second step, the doping profile is further refined using an iteration against the back-bias dependence, whereas the channel length dependence is optimised based on the roll-off analysis in the third step. The degree of accuracy in both steps (substrate dependence and roll-off analysis) indicates that the calibrated device has an accurately estimated doping profile. This doping profile is refined in the vertical direction by modulating the depth of the inversion layer. The roll-off analysis ensures that the device has a realistic lateral doping profile including source/drain extensions, halo implantation and channel doping levels. The calibration of the continuous doping profile is continued with improving the fit of the ON current (I_{ON}) characteristic by tuning the mobility parameters. The aim of the uniform transistor calibration is to deliver a TCAD transistor with accurate doping profile and I_D - V_G characteristic fitted closely to the average measured characteristics.

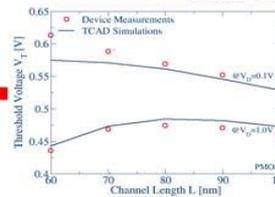
generate doping profile by Anadope



substrate analysis



roll-off analysis



mobility calibration

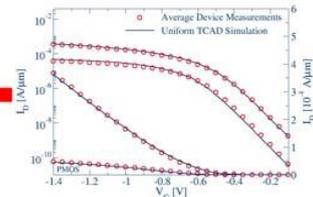


Figure 4-1: Calibration process flow in uniform device.

4.1.1 Device Structure

This section introduces the structure of a 70 nm technology node imec p-channel transistor which is provided by imec. The simulation structure of the device is developed by using an analytical doping implantation simulator, AnaDope (L. Wang et al., 2012, 2013). Phosphorus (P) and an arsenic (As) form the vertical channel doping profile. Boron is used to form the source and drain regions. In order to improve the short channel effects (SCE), arsenic (As) doping is used as a halo implantation.

The targeted device features a poly-Silicon gate having a 2.2 nm SiON gate oxide. The reason that this device has a higher thickness is to minimise screening and to highlight the interaction between percolation path and trapped charge.

A significant effort has been made in reproducing a realistic device structure using experimentally feasible process simulation steps. Figure 4.2 shows the Transmission Electron Microscopy (TEM) cross-section of the imec transistor having a 60 nm physical gate length. The extracted data are essential for the calibration process but insufficient for generating a full TCAD model. Complementary data are obtained from a Scanning Spreading Resistance Microscopy (SSRM) image. Figure 4.3 shows an SSRM image of 2D transistor narrowing the location of the halo profile and the structural dimensions.

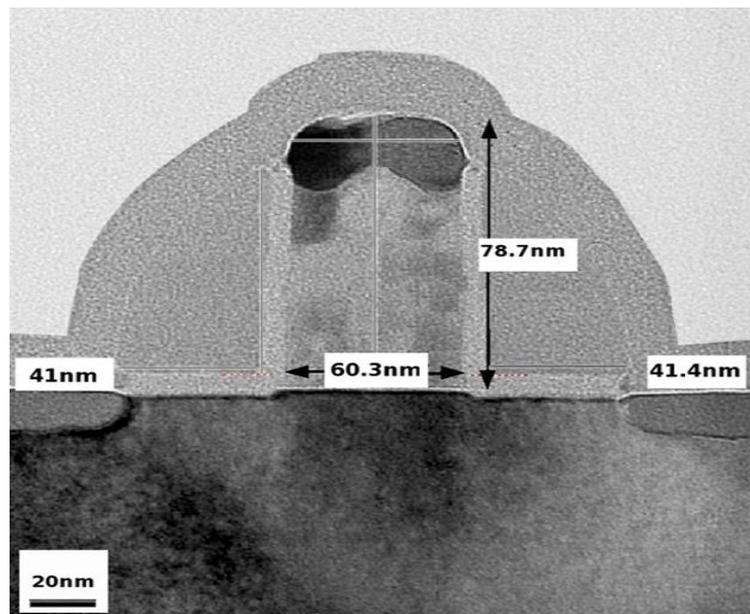


Figure 4-2: Transmission Electron Microscopy (TEM) image of the p-channel device [RH-2].

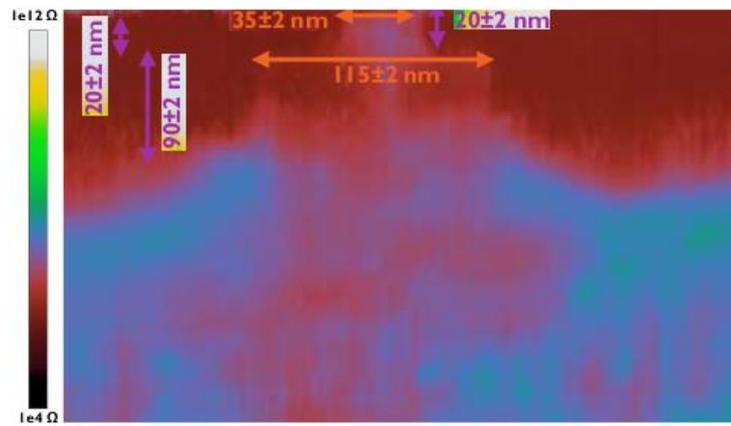


Figure 4-3: Scanning Spreading Resistance Microscopy (SSRM) image of the targeted device [RH-2].

4.1.2 Doping structure

This section describes the reverse engineering of the doping profile of the targeted transistor. The TCAD simulation structure is generated based on the extracted data from TEM and SSRM image. This structure dimension information is used to further define the opening window for the ion implantation process in the AnaDope simulator. Information for ion implantation, doping dose and energy is provided by imec. Table 4-1 shows the simplified version of the fabrication steps for the 70 nm technology node imec device, highlighting the parameters used in AnaDope. Based on the extracted structural dimensions and the fabrication steps, the initial doping profile is simulated. Due to simplifications used in the AnaDope the doping profile needs to be calibrated against measurement result.

Table 4-1: Fabrication steps used for producing the p-channel device. This information is used to develop a TCAD doping profile as a starting point.

Steps		Description
7000	Product Info	
7001	Compose lot	P type
Channel Doping		
6401	Lithoduv248	Nwell litho
3005	Implantation	phosphorus (p 31), 420 KeV, Dose 8.0e12 /cm2, Q4, Tilt 7, Twist 0
3006	Implantation	phosphorus (p 31), 310 KeV, Dose 1e13 /cm2, Q4, Tilt 7, Twist 0
3007	Implantation	phosphorus (p 31), 120 KeV, Dose 1e12 /cm2, Q4, Tilt 7, Twist 0
3008	Implantation	arsenic (as 75), 90 KeV, Dose 2.5e12 /cm2, Q4, Tilt 7, Twist 0
Gatepat 193nm hm 1000nm poly		
2210	Deposition FEOL dielectric cvd	Poly Hardmask: C-OX400-60
4105	Etchgate	
1104	Deposition nitridation anneal	Poly reox
Exthalo pmos		
6403	implantation	PMOS Ext
3015	implantation	arsenic (as 75), 40 KeV, Dose 2.7e13 /cm2, Q4, Tilt 20, Twist 0
3017	implantation	germanium (ge 72), 12 KeV, Dose 5.0e14 /cm2, Q1, Tilt 0, Twist 0
3018	implantation	carbon (c 12), 3 KeV, Dose 1.0e15 /cm2, Q1, Tilt 0, Twist 0
3021	implantation	boron (b 11), 0.5 KeV, Dose 7.0e14 /cm2, Q1, Tilt 0, Twist 0

The measurement of the spreading resistance profile from SSRM analysis can be used to refine further the doping profile. The local spreading resistance profile is inversely proportional to the local doping profile. On top of that, a conversion factor needs to be applied, as reported in (Treberspurg et al., 2012). Based on this measurement, the vertical projection range of the implant can be identified. This projection range is important in determining the doping profile and the corresponding depletion region.

The projection range is determined by the implantation energy. Based on this, the doping profile introduced in the TCAD simulation will show good agreement with the resistive measurement profile from SSRM images, as illustrated in Figure 4-4 (left). The spreading resistance profile is extracted from the SSRM measurements illustrated in Figure 4-4 (right).

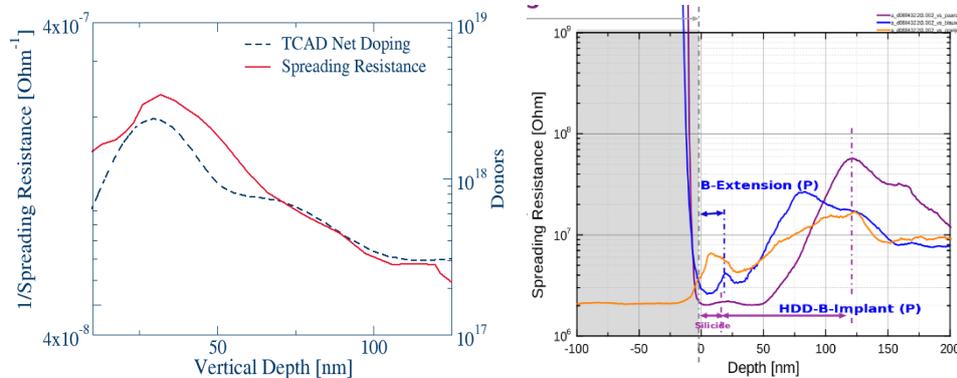


Figure 4-4: The comparison between sheet resistance and doping profile at the centre of channel (right) [RH-2] and 1D Resistance measure along the Z-axis at 3 different locations (left).

4.1.3 Substrate bias analysis

The doping profile in the vertical direction is refined by modulating the depth of the depletion region. The accuracy of the doping profile needs to be validated in respect the experimental data to produce an identical depletion region width compared to the fabricated device. This depletion region evolution can also be tracked by the electron density distribution inside the device, as illustrated in Figure 4-5.

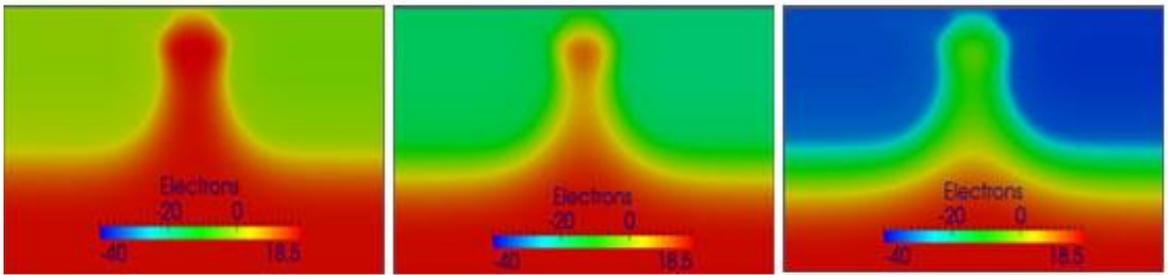


Figure 4-5: Impact on the back bias on the simulated electron density (left) 0V (centre) 1V and (right) 2V substrate bias.

The substrate analysis is performed for a long channel transistor in order to avoid the SCE effect and the impact of the halo implantation. As the available electrical measurements are for 60 nm channel length only, the calibration is performed for this channel length.

I_D - V_G curves are simulated in the bias range of 0V to 2V with an increment of 0.5V at different back biases. The validation of TCAD simulations are based on the agreement of the subthreshold Slope (SS slope) and the OFF current (I_{OFF}). The threshold voltage has been measured by using a current criterion of 0.16 μ A.

When a transistor is calibrated at the targeted channel length of 60 nm, the depletion region is determined by the interactions between halo doping and substrate doping implantation.

The halo doping implantation consists of 3 important parameters: dose, energy and angle of implantation. The variation of halo dose and energy, has an impact on the projection range which determines the depletion region width. A good estimation of the depletion region width leads to a good estimation of the doping profile in the vertical direction. Therefore, it is important to identify the best halo distribution in the transistor.. Figure 4-6 shows the threshold voltage simulated with a different level of substrate bias, achieving a acceptable agreement with the experimental results.

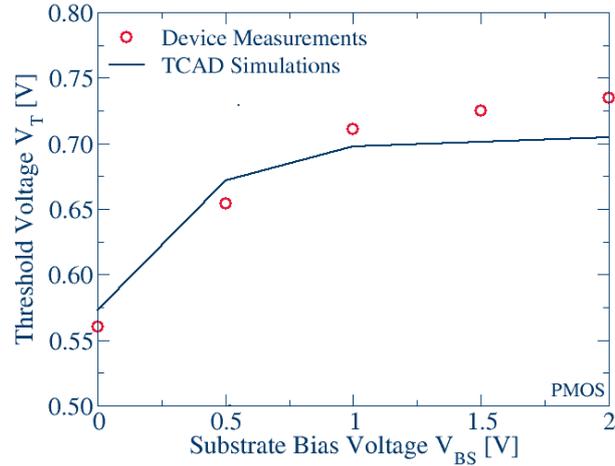


Figure 4-6: V_T roll-off for TCAD simulation and measurement result [RH-2].

4.1.4 V_T roll-off analysis

The main approach for suppressing short channel effects is to increase the local doping concentration around the source/drain p-n junctions using also doping implantation in conjunction with optimum channel doping profile engineering. It is therefore very important for the calibration of the electrostatic integrity to obtain the correct channel doping profile from realistic process simulations.

The calibration is performed at channel lengths varying from 60 nm to 100 nm, with a step size of 10 nm. The simulation is performed at both high and low drain biases. The calibration is based on a good agreement of I_{OFF} , SS slope and drain-induced barrier lowering (DIBL). The threshold voltage of each transistor is measured using a current criterion 0.16 μA . Figure 4-7 shows a V_T roll-off analysis for the p-channel transistor, comparing the experimental and simulation results.

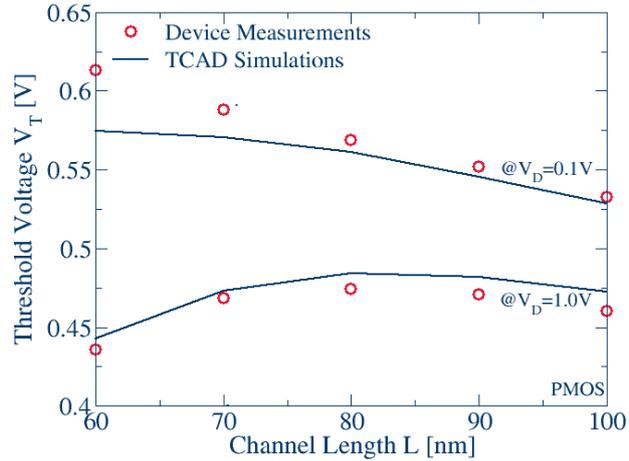


Figure 4-7: Threshold voltage versus channel length for high and low drain voltage of p-channel device [RH-2].

At this stage, the location of the doping halo is critical, especially at shorter channel lengths. The operation of tuning the location of the halo doping by changing dose, energy and angle of implantation leads to an optimised doping profile. However, the updated doping profile needs to be revalidated in respect to simulation results. The final doping provides for all the stages of an acceptable simulation result. For the n-channel transistor, a similar calibration process has been implemented. Figure 4-8 shows the roll-off analysis result after few calibration.

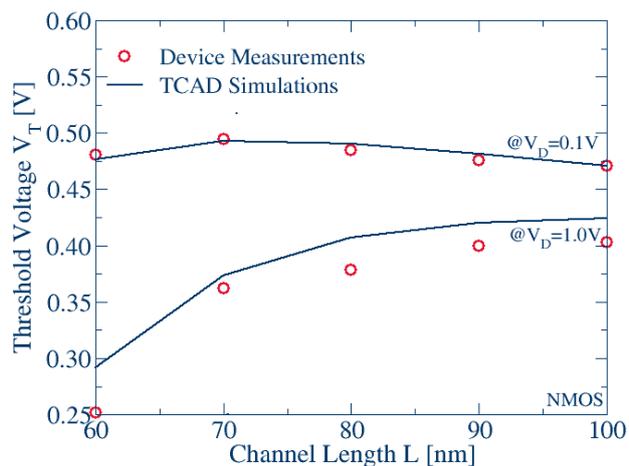


Figure 4-8: Threshold voltage versus channel length for high and low drain voltage of n-channel device [RH-9].

4.1.5 Mobility calibration

The uniform device calibration shows good agreement of the IV characteristics between the experimental measurements and the TCAD simulation suggesting an accurate estimation of the doping profile. The previous two stages, i.e the substrate analysis stage and roll-off analysis stage were focused more on refining the doping profile in a vertical and lateral direction using the subthreshold part of the IV characteristics. At these stages, the calibration process is focused on the agreement of I_{OFF} , SS slope and DIBL. To finalise the calibration, the IV characteristics above threshold voltage need to be calibrated against the experimental results.

In the following simulations, the perpendicular electric field dependence, the parallel electric field dependence and the concentration dependent mobility models were used. The RSX and the strain parameter in the concentration dependent Masseti mobility model were chosen for fine-tuning I_{ON} . The calibration is done by performing a small adjustment to the mobility model by increasing or decreasing the phonon mobility in the ranges of min-max terms of the Masseti model. Figure 4-9 shows the calibrated IV characteristics of the uniform p-channel device (left) and n-channel (right) transistor having a good agreement in both cases.

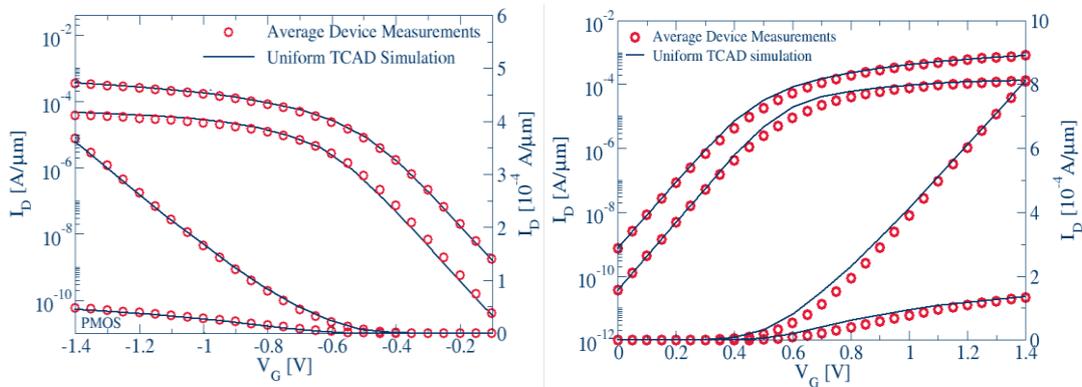


Figure 4-9: Calibration results for p-channel device (left) and n-channel device (right) [RH-9].

4.2 Statistical Variability

The calibration in the previous stage is performed against the average measurement characteristic by using a continuous doping profile. However, in the nanoscale transistor, the granularity of charge and matter must be taken into account. At this calibration stage, random discrete dopant (RDD) and line edge roughness (LER) are considered as statistical variability (SV) sources for both n-channel and p-channel MOSFETs. The poly-silicon granularity (PSG), a source of SV is considered for the n-channel transistor only.

A typical simulation domain used in the simulation of the 70 nm technology node imec deviec is illustrated in Figure 4-10. From the potential landscape, the position of RDD and impact of LER as SV sources is clearly seen.

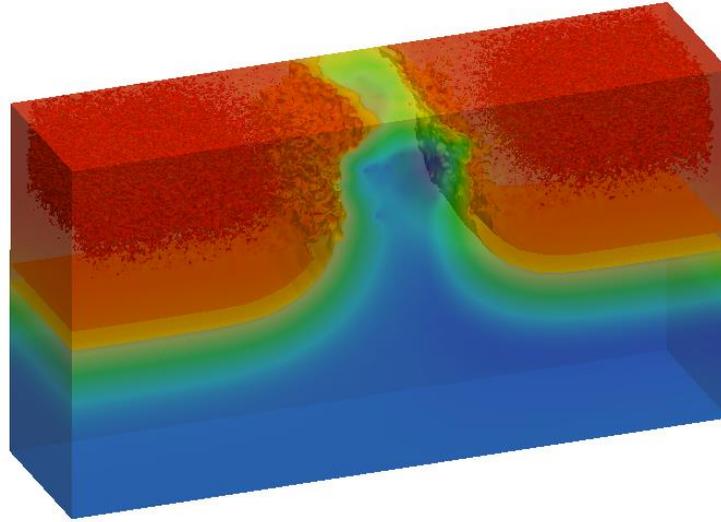


Figure 4-10: Image of 3D atomistic of p-channel device illustrating the position of dopants in the channel (Arsenic) and source/drain (phosphorus/arsenic) [RH-2].

The spread of the I_D - V_G characteristic of a sample of 1,000 microscopically different devices is illustrated in Figure 4-11. The red line represents the uniform device calibrated in the previous stage. The transistors have been simulated at a low drain bias of 0.1V. The distribution of I_D - V_G characteristics around the uniform result shows the impact of SV sources.

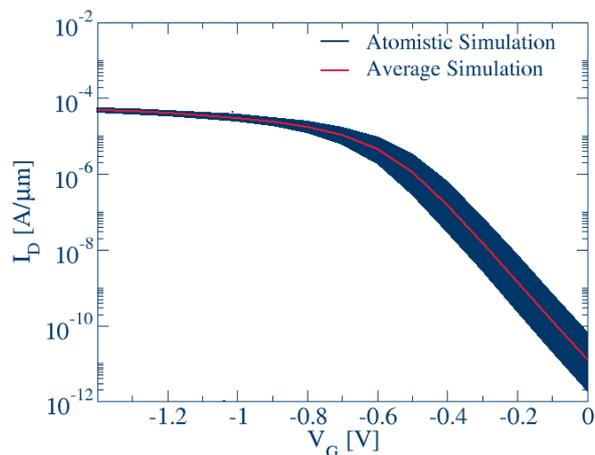


Figure 4-11: TCAD device simulation of 1,000 microscopically different devices having a different characteristic due to the SV source included in the simulation [RH-10].

The SV analysis calibration involves the fine-tuning in each individual SV source (RDD, LER and PSG). The aim of this calibration is to have a similar dispersion of threshold voltage

as the measurement results. The calibration starts with the RDD which have a major impact on the SV of planar bulk transistors. The doping profile, particularly near the interface, is tuned to match the V_T measured dispersion. The calibration in LER and PSG follows to further fine-tune the V_T dispersion results. However, for these sources, the parameters should be close to published data (Salvatore Maria Amoroso, Gerrer, Adamu-Lema, Markov, & Asenov, 2013; Asenov, Brown, et al., 2003; A. R. Brown et al., 2007; Reid et al., 2010).

Figure 4-12 shows the calibration results based on 100 atomistic TCAD devices. It shows that the V_T dispersion obtained from the TCAD simulations is 24.1 mV, which is close to the measurement dispersion at 26mV. This indicates that the continuous and ‘atomistic’ TCAD simulation captures accurately the statistical variability for the imec 70 nm technology node.

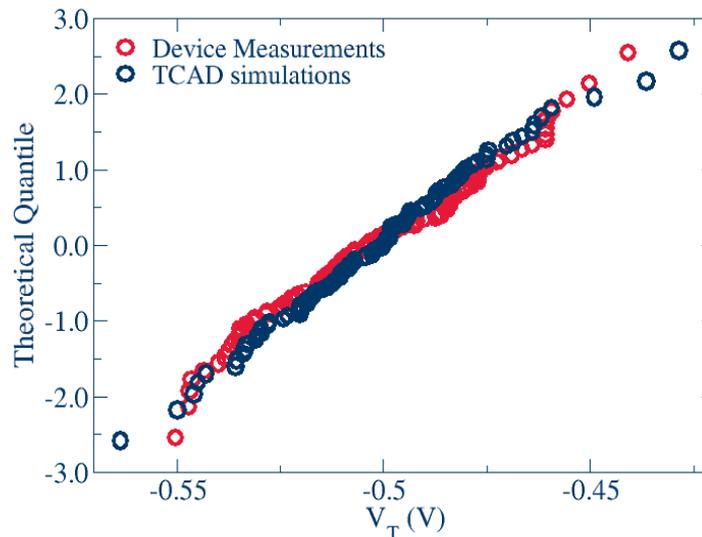


Figure 4-12: Normal distribution of the threshold voltage of TCAD simulation having a good agreement with the experimental result [RH-2].

For an accurate analysis of individual SV sources, the number of samples needs to be increased up to 1,000 different microscopic devices. Figure 4-13 shows the dispersion of V_T for the p-channel and n-channel MOSFETs individual and combined variability sources. However, due to the lack of data for the dispersion of threshold voltage of the n-channel transistors, the LER parameters mirror the LER parameter used in the p-channel MOSFET. Finally, for the PSG are adopted the parameter in (A. R. Brown et al., 2007). Due to the fact that the n-channel device suffers the impact of PSG, the variability is higher compared with the p-channel MOSFET.

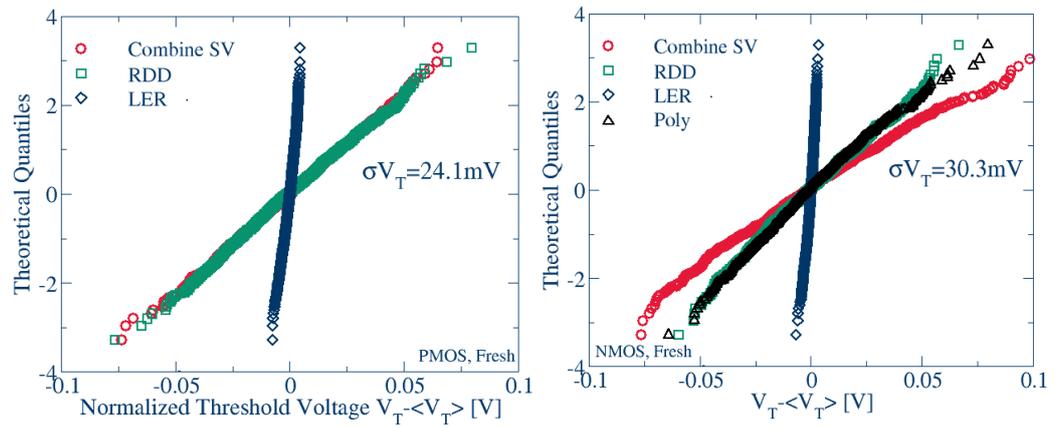


Figure 4-13: Threshold voltage distribution of p-channel device (left) and n-channel device (right) for individual and combined variability sources [RH-9].

4.2.1 RDD

Random Discrete Dopants (RDD) are the major contributor to SV for 70 nm technology node IMEC transistors. RDD introduces inhomogeneity in the electrostatic potential landscape of the transistors (Slavcheva, Davies, Brown, & Asenov, 2002). This results in different V_T of the microscopically different transistors, associated with different percolation paths.

In the early stages of the microelectronic technology, where the average number of dopants in the active region is a thousand or more, the impact of RDD was significant only for analogue applications. However, as the dimensions are scaled down, the device characteristic is determined by a small number of dopant atoms in the active region. Figure 4-14 shows the reduction in the average number of dopants with scaling of the CMOS transistors. The number of dopants is reduced to a level where there is a significant increase of stochastic spread in the dopant numbers. For example, if the distribution of dopants in the transistors follows approximately a Gaussian distribution, for a 10 μm technology, an average number of 10^5 dopants leads to standard deviation ($\sqrt{10^5}$) of a $\sim 0.3\%$. Meanwhile, for a 100 nm technology with an average number of 100 dopants, the standard deviation technology is approximately 10%.

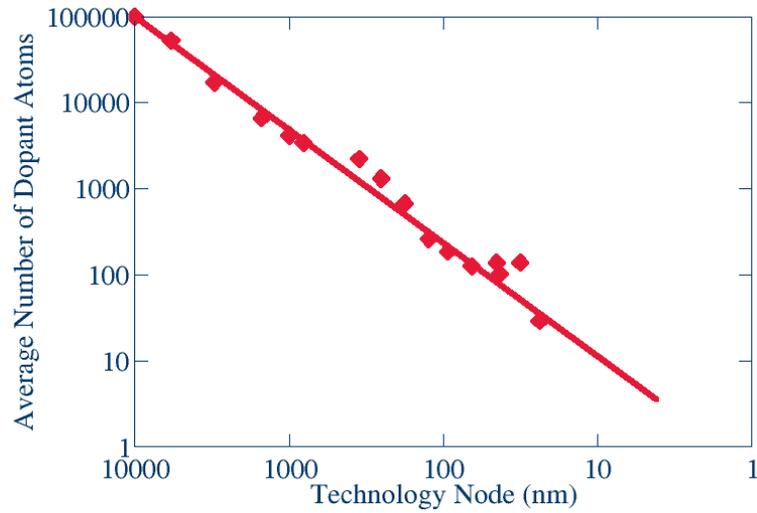


Figure 4-14: Average number of dopants in the active region with respect to the technology node. After ref (K. Kuhn et al., 2008).

The calibrated continuous doping profile from the previous calibration stages is a starting point for the SV calibration. In GARAND, the random dopants are assigned based on the continuous doping profile using a rejection technique (Asenov et al., 1999). The variation in the numbers and the positions of the dopants in the active region results in microscopically different transistors. In the calibration of the atomistic TCAD simulations, only RDD was taken into account. A further fine-tuning of the doping profile near the interface is performed in order to match the statistical variability simulation. Figure 4-15 shows a dispersion of IV characteristic from a 1,000 samples for both p-channel and n-channel transistors. The dispersion of threshold voltage measured using a current criterion at $0.16 \mu\text{A}$ is 21.8 mV for p-channel device and 20.98 mV for n-channel transistor.

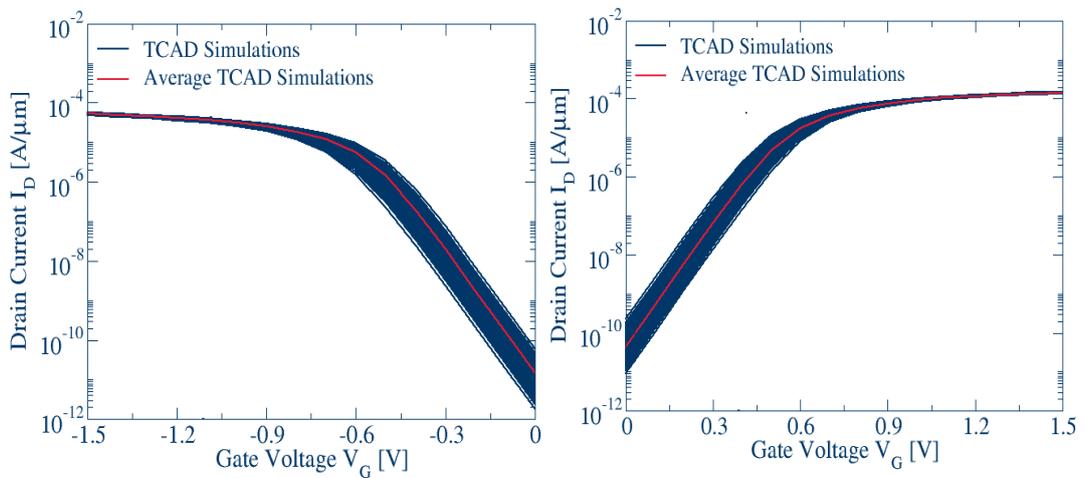


Figure 4-15: Variability in atomistic TCAD device simulations due to the RDD impact in p-channel device (left) and n-channel device (right). Shows the major influence in variability for 70 nm technology node of imec device.

4.2.2 LER

Line edge roughness (LER) has a small impact on the statistical variability analysis of the simulated bulk transistors. LER is a result of the molecular resist granularity during the lithography process. In GARAND the LER model is based on a Fourier synthesis approach (Howell, 2001). There are two important parameters controlling the LER, the root mean square (RMS) magnitude of LER, Δ and the correlation length as Λ . The value of LER is defined as 3Δ which in the simulations is 4 nm and the correlation length Λ is in the range of 10 nm to 50 nm, which depends on the nature and the accuracy of the lithography process being used in the fabrication.

The devices are simulated for a set of LER parameters. After a few iterations, the LER parameters are fixed to an RMS value of 4 nm and a correlation length of 25 nm. The implementation of LER in the atomistic TCAD simulation results in local fluctuations in the channel length resulting in variations of the I_D - V_G characteristics shown in Figure 4-16. For ensembles of 1,000 transistors, by having only LER in the TCAD simulations, at the current criterion $0.16 \mu\text{A}$, the dispersion of threshold voltage for p-channel transistor is 2.1 mV and for n-channel transistor is 1.5 mV.

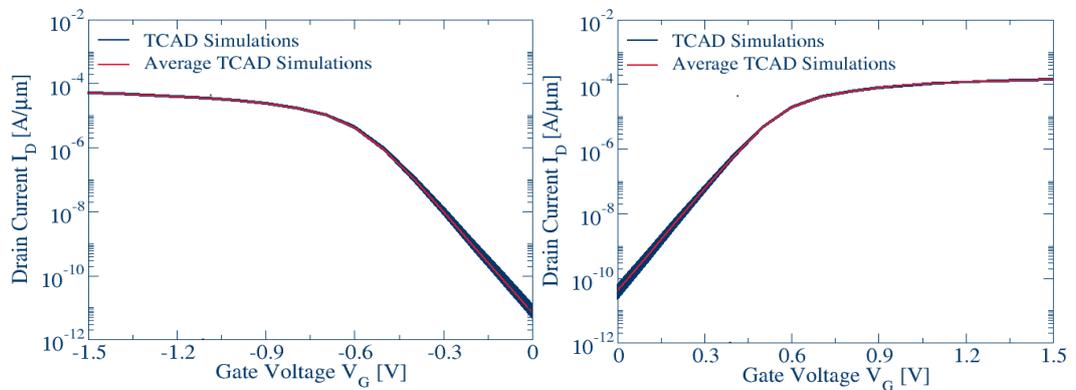


Figure 4-16: Variability in atomistic TCAD device simulations due to the LER impact in p-channel device (left) and n-channel device (right). Shows the minor influence in variability for 70 nm technology node of imec device.

4.2.3 PSG

In this section, the poly-silicon granularity (PSG) as SV source is considered. This SV source has almost the same impact compared with RDD. However, this source only affects the n-channel transistors and plays no role in the p-channel transistors due to the absence of the corresponding donor type interface states in the lower part of the silicon bandgap (Asenov, Cathignol, et al., 2008).

PSG is characterised of two parameters; namely Fermi level pinning energy and poly-silicon grain distribution. A previous study shows that the Fermi level pinning at 0.3 eV and the average diameter of poly-silicon grains is 40 nm (A. R. Brown et al., 2007). However, the grain size strongly depends on the fabrication process, which gives latitude for fine-tuning of the PSG parameters. The grain template of poly-silicon as illustrated in Figure 4-17 (right) is used in the GARAND simulator. The grain template can be scaled with respect to the average grain size. This grain template is based on AFM measurement results illustrated in Figure 4-17 (left). The Fermi level is pinned at the boundaries between the grains (Cathignol, Rochereau, & Ghibaud, 2006) and the pinning energy can go up to 0.6 V.

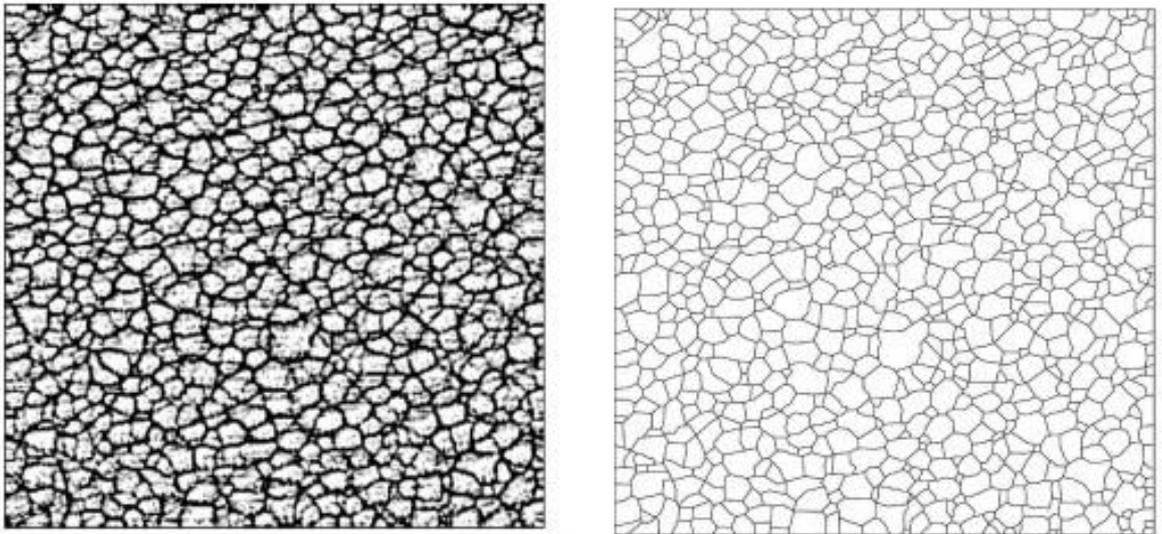


Figure 4-17: AFM image of poly-silicon grain measured (left) by (Uma, McConnell, Asheghi, Kurabayashi, & Goodson, 2001) and corresponding image (right) of grain boundaries used in simulator. The image can be rescaled and serve the average diameter for a proper PSG simulation.

For the purpose of calibration, the PSG parameters used in (A. R. Brown et al., 2007) pinning level 0.3 eV and 40 nm poly grain diameter resulted in variability accurately matching the measurements. Therefore, the suggested PSG parameter is used in this study where Fermi level pinning is defined at 0.3 eV and 40 nm poly grain diameter. Figure 4-18 shows the statistical IV characteristics for the n-channel transistor with a dispersion 20.69 mV.

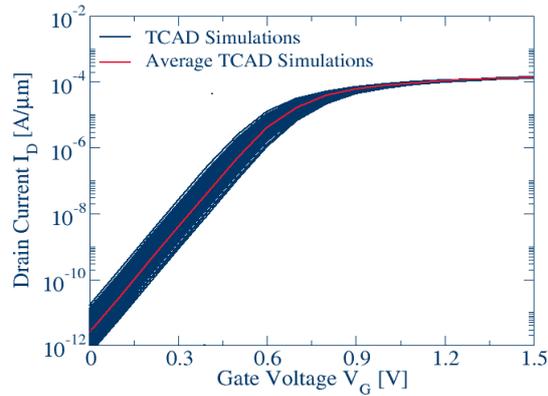


Figure 4-18: Variability in atomistic TCAD device simulations due to the PSG impact in n-channel device. Shows the major influence in variability for 70 nm technology node of imec device.

4.3 Reliability

The reliability of the transistors is related to existing and built in oxide defects. Innovations in technology help to reduce the defect density. Still the remaining defects present in the active transistor region are relatively low and their impact may become intolerable with scaling (N. Zanolla et al., 2008). Therefore, the defect state related reliability becomes vital as the device dimensions become smaller. There are two important reliability phenomena that affect the device performance, namely the random telegraph noise (RTN) and the bias temperature instability (BTI). The impact of these phenomena on the calibrated TCAD transistor model will be discussed in this section.

4.3.1 RTN

In this section, the impact that a single charge electron trapped at the interface of the imec 70 nm technology transistors is investigated. The calibrated TCAD device is simulated with GARAND using the drift diffusion (DD) module. Even though the DD module does not capture the non-equilibrium and ballistic transport, the capability to capture accurately the electrostatic effects in the subthreshold and the linear region of transistor operation is well suited for the purposes of this study.

The well calibrated TCAD transistor in the previous stage are microscopically different in terms of number and position of dopants and the other variability source in the ensemble. Each microscopically different transistor has a different performance.

Here we investigate the impact of a single trapped charge which is responsible for the RTN phenomenon. A random single charge is assigned at the interface of the device according to

a uniform distribution. The mismatch of the threshold voltage between the fresh device and the device that has trapped charge is recorded.

Figure 4-19 shows the carrier density distribution in one 3D atomistic device. Encircled is the percolation path between the source and the drain and the impact of the trapped charge blocking this percolation path.

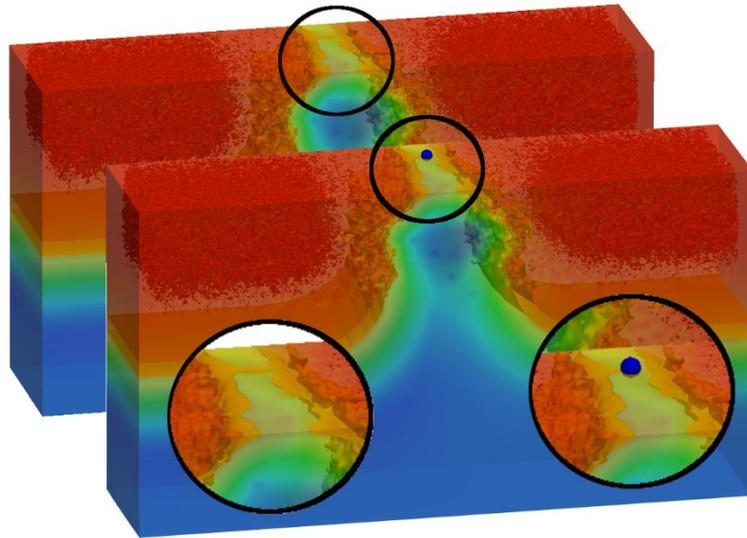


Figure 4-19: Electron concentration at threshold voltage conditions in the case of fresh device (back) and filled with a single trap (front). The main percolation path blocked by the trapped charge as shown in zoomed-in view [RH-2].

The threshold voltage distribution is used to validate the RTN simulations in respect to measurements. The mismatch between the degraded and the fresh transistor is measured by using a current criterion at $0.16 \mu\text{A}$. The impact of RTN is measured using time dependent defect spectroscopy (Tibor Grasser, Reisinger, Wagner, Schanovsky, et al., 2010) on 100 p-channel devices as illustrated in Figure 4-20. This results indicates that the calibrated doping profile reproduces accurately the RTN amplitudes distribution.

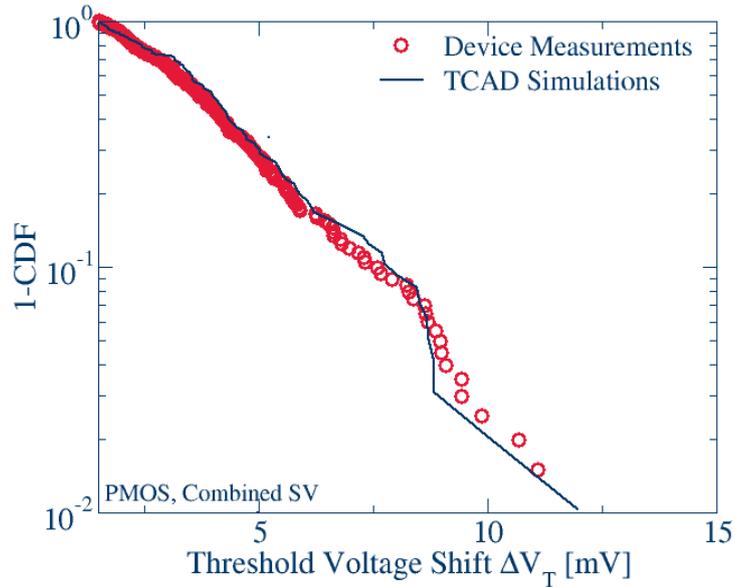


Figure 4-20: The threshold voltage shift versus Cumulative Distribution Function (CDF) of measured and simulated RTN [RH-2].

The threshold voltage shift distribution is related to the interaction between the trapped charge and the percolation paths at the interface of the channel. Figure 4-21 shows that there is no correlation between the threshold voltage shift and the threshold voltage itself which is in agreement in (Toledano-Luque et al., 2013).

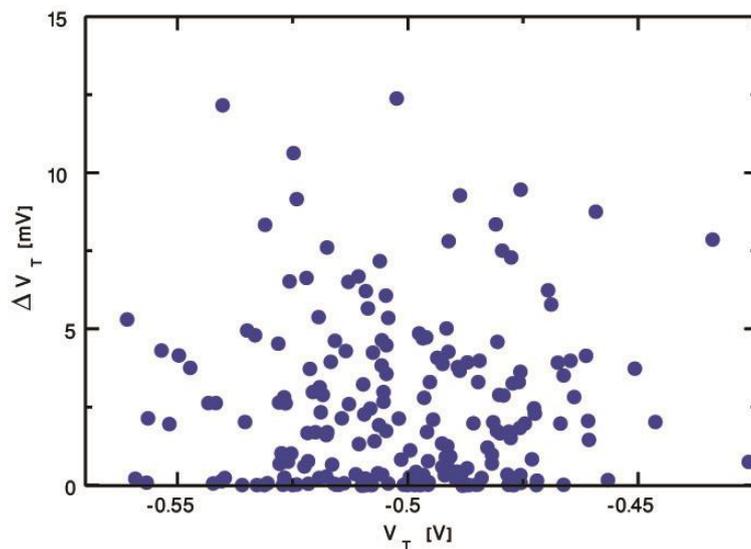


Figure 4-21: The uncorrelated distribution of corresponding V_T and ΔV_T pairs in TCAD simulation [RH-2].

The RTN phenomenon is further analysed by simulating an ensemble of 200 devices before and after degradation. The single trapped charge is induced following uniform probability distribution, at the interface of the channel. Figure 4-22 shows the gate bias dependence of

the fractional ΔV_G change for an ensemble of 200 transistors indicating that the average ΔV_G is occurring at gate bias equal to the V_T . ΔV_G reduces with the increase in the gate bias due to screening. However, some of the devices display anomalous behaviour with the ΔV_G increasing at higher voltage and having a weaker effect at lower gate bias.

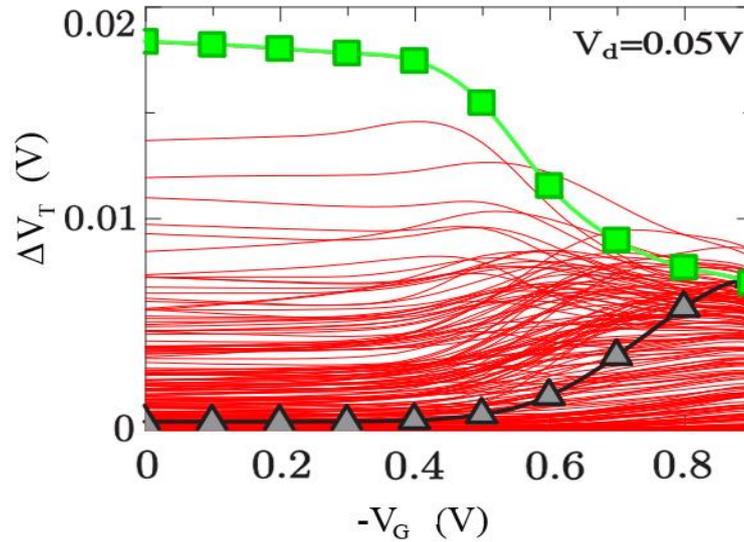


Figure 4-22: Extreme device A (triangle shape) and B (square shape) having an impact of single trap charge at the interface of the channel showing a different behaviour due to the interaction between percolation path and trapped charge [RH-11].

Two extreme devices named A and B are further analysed in detail. These devices are simulated at a gate bias equal to the threshold voltage ($V_G = V_T$) and drain bias ($V_G = 1.0$ V) in both conditions (fresh and degraded devices). Figure 4-23 shows the location of the trapped charge and the effective percolation path for these devices. It is clear that the conduction path can be shifted by the gate bias and or the percolation path becomes less localised with the increase of the gate bias. As a result, for device A, the ΔV_G is larger at the threshold voltage due to the location of the trapped charge blocking the percolation path and having a lesser impact of ΔV_G . However, for device B, the trapped charge is far away from the percolation path when the gate bias is at the threshold voltage, but close enough to produce visible impact when gate bias at V_{DD} .

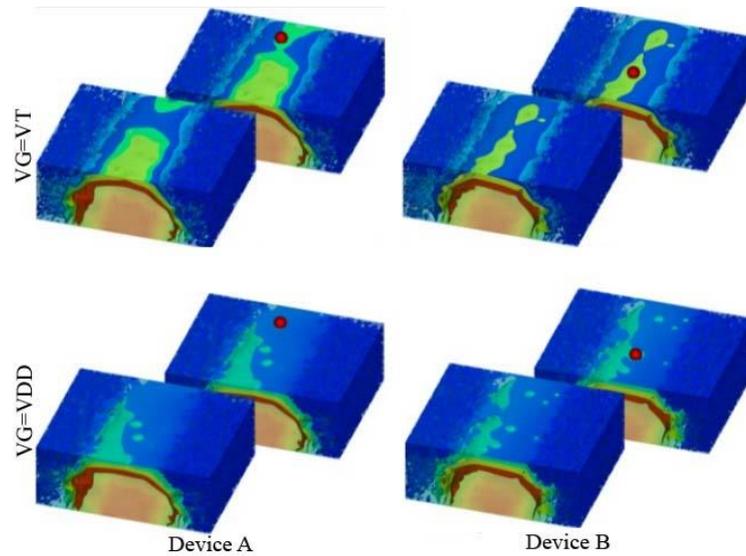


Figure 4-23: The extreme devices A and B illustrated by potential at the 1nm below interface, which corresponds to the extreme result [RH-11].

After achieving accurate results for the time zero and time dependent variability, the p-channel transistor is further analysed at different drain biases. The number of simulations is increased to 1,000 devices for more accurate statistical result. The device is simulated at $V_D=0.1V$, $V_D=V_T$ and $V_D=1.0V$. Figure 4-24 (left) shows that the average threshold voltage is reduced as the drain bias increases. This is due to DIBL. Simultaneously, the dispersion of the threshold voltage increases when the drain bias increased, partially because of the reduction of the effective channel length. Figure 4-24 (right) shows clearly the difference in the dispersion at different drain biases.

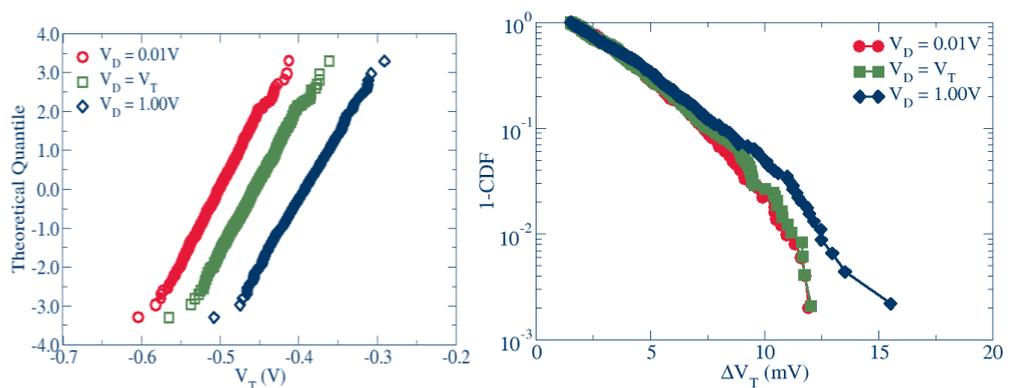


Figure 4-24: Distribution of threshold voltage of p-channel at different drain biases [RH-2].

The impact of the drain bias on the RTN distribution is further clarified in Figure 4-25, which shows the position of the single trapped charge induced at the interface at several drain biases. The impact of the trapped charge is stronger at the centre of the channel and decreases towards the source and drain. Simultaneously with the increase in the drain bias, the

electrostatic impact of the traps located at the drain side is reduced. The peak of the ΔV_T distribution is therefore shifted towards the source of the channel.

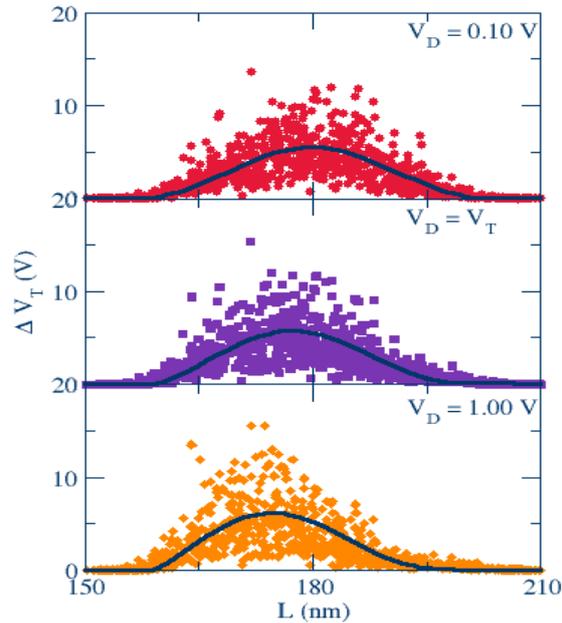


Figure 4-25: The impact of simulated RTN as a function of the trap position along the channel length for several applied drain biases [RH-2].

The substrate bias dependence of the time-zero variability and the time dependent variability is further analysed. The transistor is simulated under substrate bias ranging from 2.00 V to -0.55 V. In agreement with the calibration results in Figure 4-7, the average V_T increases as the substrate bias is increased. Figure 4-26 (left) shows that the V_T dispersion increases with the substrate bias due to the depletion width modulation.

The impact of a single trap charge in the channel and the corresponding dispersion of ΔV_T increased with the increase in the substrate bias, similar to the reported in (Franco et al., 2013), while the average of ΔV_T is only slightly affected. The change in the dispersion of ΔV_T with the increase of the substrate bias is illustrated in Figure 4-26 (right) below.

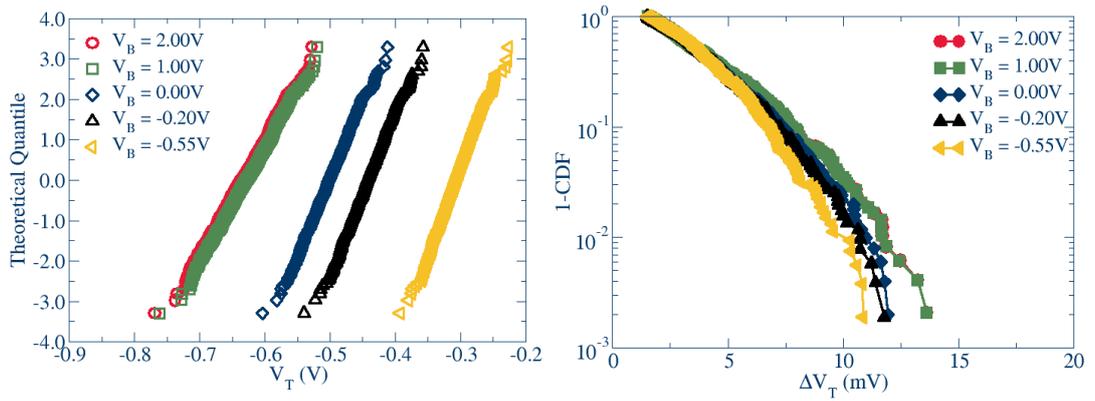


Figure 4-26: The distribution of V_T dispersion (left) and cumulative distribution of ΔV_T due to single trapped charge (right) with respect to the substrate bias-dependence [RH-2].

The impact of the channel length on the RTN distribution is also analysed. Transistors with gate length varying from 60 nm down to 30 nm are simulated. Due to the increasing SCE, the distribution of threshold voltage illustrated in Figure 4-27 (left) shows deviation from a normal distribution for the transistor shorter than 40 nm. Figure 4-27 (right) shows the cumulative distribution of threshold voltage shift ΔV_T at different gate lengths. Clearly, the reduction of gate length results in an increase of ΔV_T dispersion. At 30 nm gate length, more than 6 devices have ΔV_T larger than 40 mV.

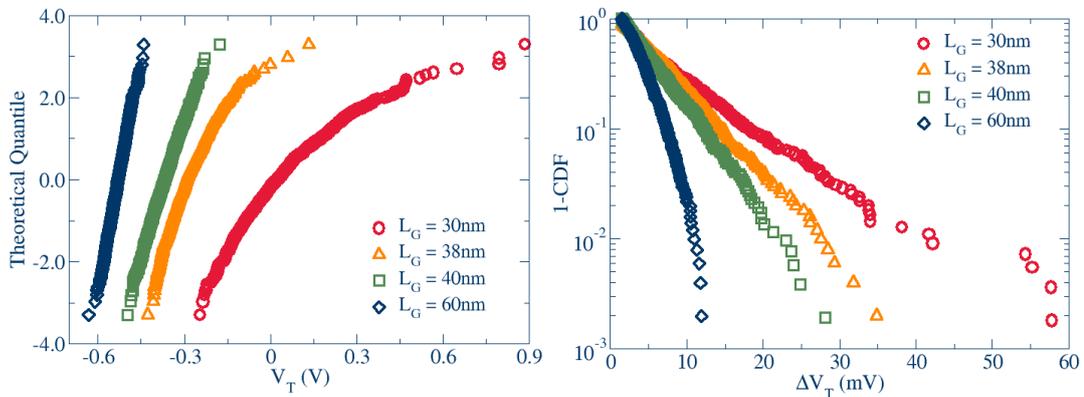


Figure 4-27: Dispersion of threshold voltage (left) and cumulative distribution of ΔV_T due to single trapped charge (right) with respect to the channel length dependence.

Figure 4-28 shows the relationship between dispersion of V_T and dispersion of ΔV_T due to the drain bias, substrate bias and channel length dependence, having a nearly universal trend except for relatively large body bias.

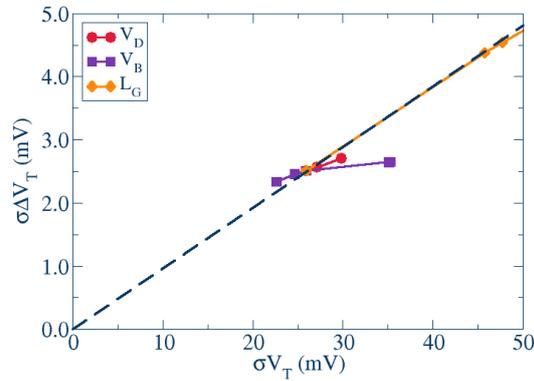


Figure 4-28: The relationship between dispersion of V_T and ΔV_T as a function of drain bias, substrate bias and channel length dependence indicates the variability and reliability impact for the 70nm technology node of IMEC device [RH-2].

4.3.2 BTI

In the previous section, the impact of a single trapped charge or RTN amplitude distribution was discussed. The introduction of statistical variability including RDD, LER and PSG in 70 nm imec technology node transistors results in significantly larger threshold voltage shifts compared to the simulations for the uniform transistor. This is related to the interaction between the percolation paths which are produced by the SV source with the trapped charge event.

In the RTN simulation, the device performance is based on a single trapped charge induced at the interface. However, in reality in BTI degradation the number of trapped charges varies in each of the devices, statistically following a Poisson distribution. Therefore, in realistic simulation condition, the transistor may have more than a single trapped charge or may have no trapped charges. This will affect the transistor parameter distribution including that of the threshold voltage shift due to the interaction of the trapped charges with the intrinsic variability sources.

For the purpose of the steady state BTI simulation analysis, the ageing transistor is simulated by using an ensemble of 1,000 microscopically different transistor including SV sources and with average trap density increasing from 10^{11} cm^{-2} to 10^{12} cm^{-2} following the experimental result from (Toledano-Luque et al., 2011). The degradation of the device performance is based on the average trap density. The trapped charge numbers in the individual transistors follow a Poisson distribution. For each level of trapped charge induced in the device, the IV characteristics are simulated for a gate voltage ramping from 0 up to 1.5 V.

The evolution of threshold voltage from the statistical simulation of 1,000 p-channel transistors corresponding to the progressive increase of the charged trap is plotted in Figure 4-29 and summarised in Figure 4-30. It can be seen that, for a fresh device, the threshold voltage has a wide distribution (24.1 mV) due to the impact of statistical variability sources. The progressive degradation of the device including increasing the trapped charge density, increases the average threshold voltage from 0.54 V to 0.65 V and the dispersion of threshold voltage from 24 mV to 35 mV.

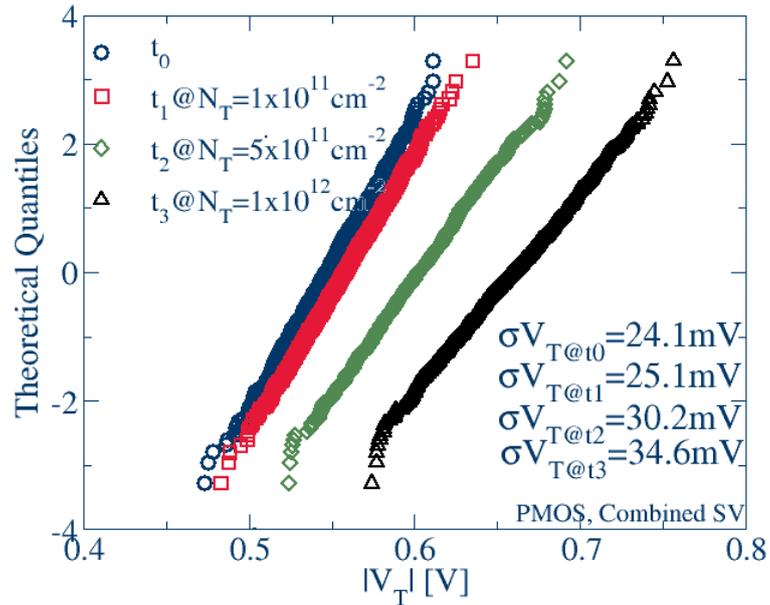


Figure 4-29: Distribution of threshold voltage for fresh and ageing p-channel device [RH-9].

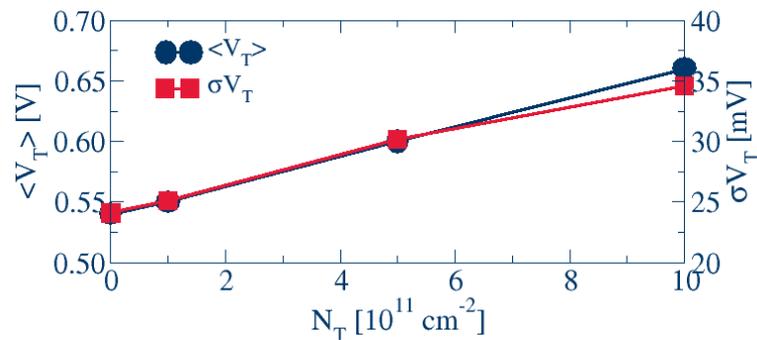


Figure 4-30: Summary of ageing device at different level of degradation for p-channel device.

BTI simulations have also been performed for the IMEC n-channel transistor of the 70 nm technology node. Using statistical simulation an ensemble of 1,000 devices at different levels of ageing, with increasing of trapped charge from 10^{11} cm^{-2} up to 10^{12} cm^{-2} was studied.

Figure 4-31 shows the distribution of the threshold voltage for the fresh and the aged n-channel transistor.

The statistical variability source results in up to 30.3 mV dispersion of threshold voltage, which is noticeably higher compared with the p-channel device due to the PSG which only affects the n-channel transistor. The progressively increasing trapped charge density up to 10^{12} cm^{-2} results in 39.1 mV dispersion of the threshold voltage. Simultaneously the average threshold voltage increases from 0.55 V for a fresh device to 0.66 V for a transistor after degradation. Figure 4-32 summarises the ageing transistor characteristics at different levels of degradation.

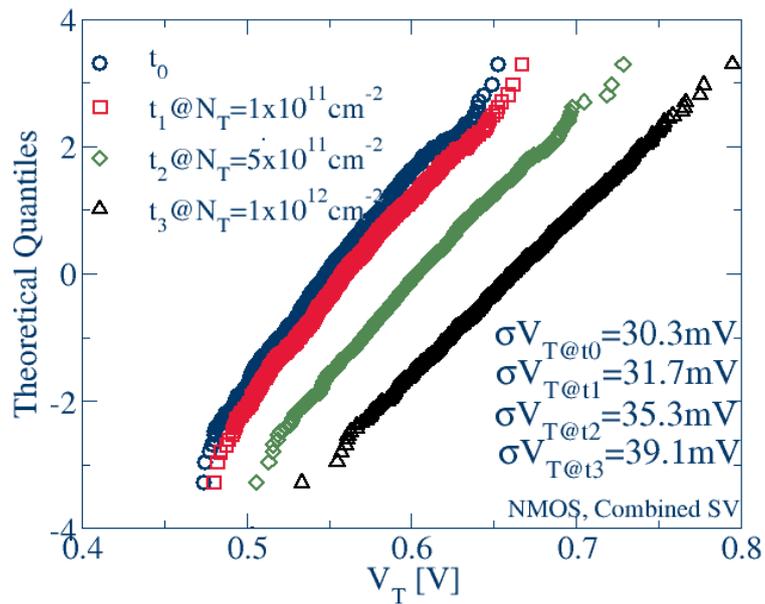


Figure 4-31: Distribution of threshold voltage for fresh and ageing n-channel device [RH-9].

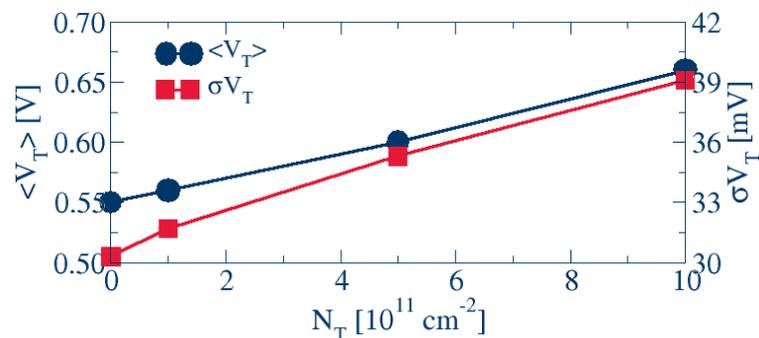


Figure 4-32: Summary of ageing device at different levels of degradation for n-channel device.

Next the BTI impact on drive current which is responsible for timing variations in circuit simulations is analysed. Figure 4-33 (left) shows the drive current distribution for a fresh p-

channel transistor having a dispersion of $1.77 \mu\text{A}$ associated only with the original statistical variability sources. The progressive trapping results in reduction of the average drive current from $52 \mu\text{A}$ for a fresh device to $46 \mu\text{A}$ for a device with average trapped charge density 10^{12}cm^{-2} . Simultaneously the dispersion of drive current increases from $1.8 \mu\text{A}$ at time zero up to $2 \mu\text{A}$ for average trapped charge density 10^{12}cm^{-2} . BTI has a similar impact on the average drive current and the dispersion of the drive current in the n-channel transistor, as shown in Figure 4-33 (right). The average of the drive current is reduced from $138 \mu\text{A}$ to $124 \mu\text{A}$ at an average trapped charge level of 10^{12}cm^{-2} , while the dispersion of the drive current, increases from $3.6 \mu\text{A}$ to $4.7 \mu\text{A}$ correspondingly. This impact is related to interaction of the trapped charge at the interface with the ionized dopants in the channel (G. Roy et al., 2006). The impact on the average and the dispersion of the drive current is summarised in Figure 4-34 for both the p-channel and the n-channel transistors.

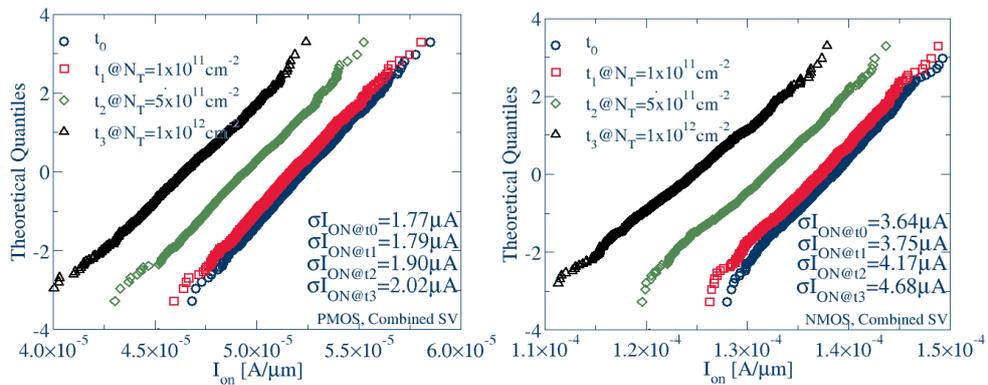


Figure 4-33: The impact of the ageing device in terms of drive current was illustrated by a normal distribution for the p-channel device (left) and the n-channel device (right). The criterion for drive current is measured at gate voltage at 1.5V [RH-9].

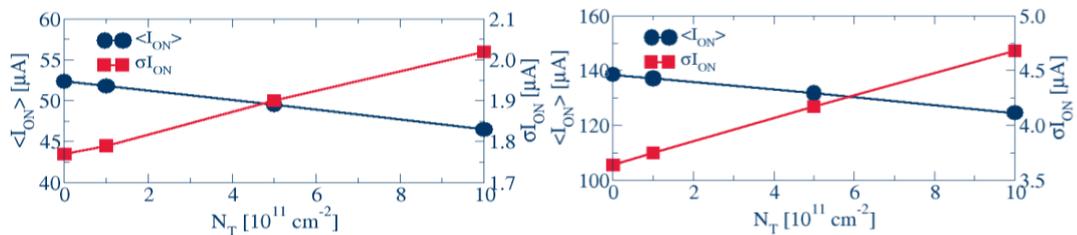


Figure 4-34: Summary of ageing device at different levels of degradation for p-channel device (left) and n-channel device (right).

The BTI phenomenon is further analysed for an extreme device at different levels of trap degradation. The main objective is to identify the conditions for the device to exhibit an extreme threshold voltage. The threshold voltages for the fresh transistor and the aged transistor are measured at a current criterion of $0.16 \mu\text{A}$. From the normal probability

distributions, extreme devices were identified from the fresh and the degraded ensembles. Figure 4-35 shows the normal distribution of the p-channel transistor with the extreme devices in its tail. It is clear that the extreme device after degradation is not the same extreme initial device. The most extreme fresh device is device number 837. However, after degradation at trap density of 10^{11} cm^{-2} , the most extreme device is device number 5. Meanwhile, the least extreme fresh device is device number 855. After the degradation it has been replaced by device number 29.

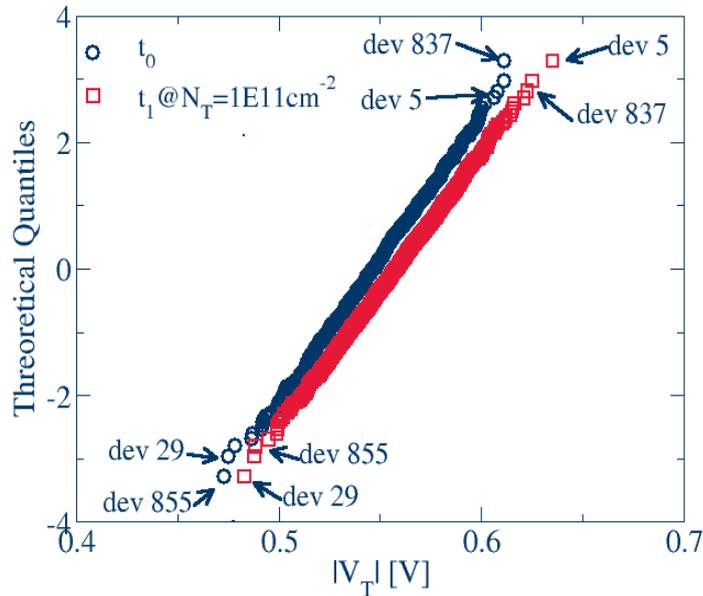


Figure 4-35: Distribution of threshold voltage for fresh and ageing device at t_1 , indicating that the extreme device in both cases is not represented by the same device number.

The most and least extreme devices in both cases have been analyzed graphically. The corresponding current density distribution in the active region is illustrated in Figure 4-36. It shows the percolation path which occurs caused by the statistical variability sources and the interaction between the trapped charges induced as a result of degradation. This indicates that the extreme device is not necessarily associated with the largest number of traps occurring in the channel, but rather by the effectiveness of the trapped charge in blocking the percolation path.

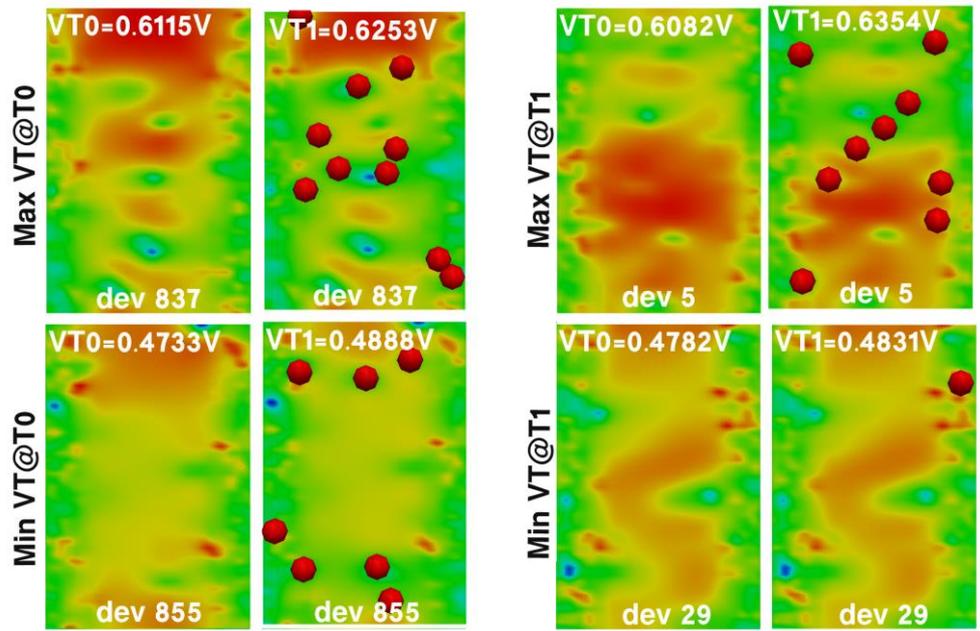


Figure 4-36: Extreme device having most and least threshold voltage at t0 and t1 [RH-9].

4.4 Summary

In this chapter, a comprehensive TCAD calibration methodology was developed and applied to a 70 nm imec technology node transistor with poly-silicon gate. The calibration using the uniform transistor, includes structural measurements and doping structure adjustment based on substrate bias analysis, V_T roll-off and mobility calibration. Good agreement was achieved with the experimental results. The transistor structure was deduced from TEM images and SSRM measurement. The back-bias dependence of the transistors has been used to refine the vertical doping profile, while the threshold voltage roll-off is used to deduce the lateral 2D doping profile distribution. The output of the calibration delivers a good agreement in respect of the substrate bias dependence, the V_T roll-off dependence and the average IV characteristic.

The calibration of the statistical variability sources delivers good agreement between the simulated and the measured dispersions of the threshold voltage, both evaluated at the threshold voltage at current criterion of $0.16 \mu\text{A}$. The fine calibration of the doping near the interface improves the simulated dispersion of the threshold voltage associated with RDD, while LER and PSG parameters remain close to the parameters used in previous research.

After careful calibration the simulated RTN distribution shows good agreement with the experimental results. Using the calibrated TCAD device, full NBTI and PBTI analysis are performed for p-channel and n-channel transistors corresponding to the 70 nm imec CMOS

technology. For the p-channel transistor, the NBTI results in an average threshold voltage shift from 0.54 V in the fresh transistor to 0.65 V in a transistor exposed to a maximum level of degradation. The corresponding dispersion in the threshold voltage increase from 24 mV to 35 mV. For the n-channel transistor the PBTI results in an average threshold voltage shift from 0.55 V in the fresh transistor to 0.66 V in a transistor exposed to a maximum level of degradation. The corresponding dispersion in the threshold voltage increase from 30.3 mV to 39.1 mV.

Chapter 5: FinFET BTI Reliability

Background

The Intel 22 nm Fin-Shaped Field Effect Transistor (FinFET), was the first CMOS technology generation to use a 3D transistor structure ("22nm Intel FinFET,"). This enabled the Intel processors to deliver 37% transistor performance increase, using half the power compared to the previous technology generation ("22nm Intel FinFET by ZDnet,").

The scaling of the planar MOSFET CMOS technology is facing acute problems related to process induced variability (Andrew R Brown, Watling, & Asenov, 2002; Damaraju et al., 2012; G. Roy et al., 2006; X. Wang et al., 2013) and statistical variability (SV) (Boeuf, Sellier, Farcy, & Skotnicki, 2008). The introduction of the new 3D FinFET transistor architecture has lead to a reduction in SV, as a result of improvement in electrostatic integrity that allows significant reduction in the channel doping and the corresponding random discrete dopants (RDD) SV (X. Wang et al., 2011). However, although the SV has been reduced, the problems due to the gate stack defects still exist including bias temperature instability (BTI) [RH-2](Kaczer et al., 2010) and hot carrier injection (HCI) (Schlunder et al., 2012).

This chapter focuses on the importance of BTI degradation on the 22 nm Intel FinFETs. In order to evaluate the impact of the BTI, the corresponding transistor needs to be carefully calibrated with respect to the structural and electrical data. The transistor structure used in

this study is based on the information extracted from published data (Auth et al., 2012; Jan et al., 2012). The FinFET structure has been imported into the gold standard simulation (GSS) 3D simulator GARAND and calibrated against the published characteristics of FinFETs with a continuously doped medium power (MP) transistors. Subsequently, the MP transistor is modified into the standard power (SP) and low power (LP) transistor by modifying the channel doping concentration. Finally, the impact of BTI degradation on the MP and LP transistors is studied in detail.

5.1 Uniform Device Calibration

The calibration process for 22 nm Intel FinFET technology involves three stages, namely device structure, doping distribution and IV calibration. The following sections discuss in detail each of the stages, starting with device structure which was developed by collaborators at Coventor based on published SEM images of Intel 22 nm FinFETs. Subsequently, the reverse engineering of the doping profile will be discussed, which involves ion implantation and diffusion. Finally, the calibration will be in respect to the published IV characteristics further described. This section also presents the transformation of the MP device into the SP and LP devices.

5.1.1 Device Structure

The structure of the 22 nm Intel FinFETs is now discussed. This is the first fully depleted tri-gate 3D transistor, featuring a third generation of high- κ metal gate technology and fifth generation of strain technology (Jan et al., 2012). The structure of the device is imported from the SEMulator3D simulations ("Semulator3d,") provided by Coventor. The primary focus is the analysis of statistical variability and statistical reliability.

Figure 5-1 shows a transmission electron microscopy (TEM) image of a 22 nm Intel FinFET (Auth et al., 2012). The transistor has a trapezoidal shape fin, which is markedly different from the conventional bulk metal oxide semiconductor field effect transistor (MOSFET) (see Chapter 4). This shape is due to silicon (Si) loss during the wet cleaning, oxidation and dry etching processes (Chi, 2012; Kanarik, Kamarthy, & Gottscho, 2012). The information in respect of this device is limited and therefore, several assumptions have been made in order to develop the structure of the technology computer-aided design (TCAD) simulation domain. Table 5-1 summarises the structure of the 22 nm Intel FinFET technology from published data (Auth et al., 2012; Jan et al., 2012).

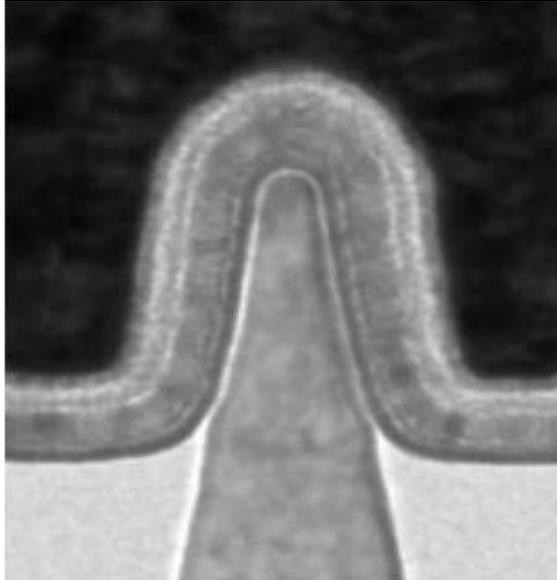


Figure 5-1: TEM image of the 22 nm Intel FinFET device illustrating the fin shape of the 3D device (Jan et al., 2012).

Table 5-1: Summary of the structure of the 22 nm Intel FinFET technology (Auth et al., 2012).

Properties	Value
LG	20.00 nm
EOT	00.90 nm
Fin Height	34.00 nm
Fin Thick	8.00 nm

The initial structure was developed using the Coventor 3D virtual fabrication platform SEMulator3D. This simulation platform adopts a process emulation approach in which the actual fabrication process is performed virtually. Figure 5-2 illustrates the SEMulator3D process flow used in the FinFET development. The process involves the transfer of the fin pattern onto the (100) silicon substrate, before the gate sacrificed process. This stage is followed by the source/drain doping and the gate replacement modules. The fabrication is finished by using middle of line (MOL) and back end of line (BEOL) metallization. The fin is developed by using a self-aligned double patterning (SADP) method (Du et al., 2013; Kodama et al., 2015). This method enables the fabrication of smaller features without the need for advanced technology, by utilising the disposal mandrel and sidewall spacer. Once the side wall spacer is defined, the mandrel is removed, leaving the spacer which will be used as a hard-mask for etching the fin pattern process. The final definition of the fin profile is established by using several process parameters, such as the mandrel height, the thickness of the spacer deposition, and the integrated etch process, as well as shallow trench isolation (STI) etch back which reveals the top of the fin device.

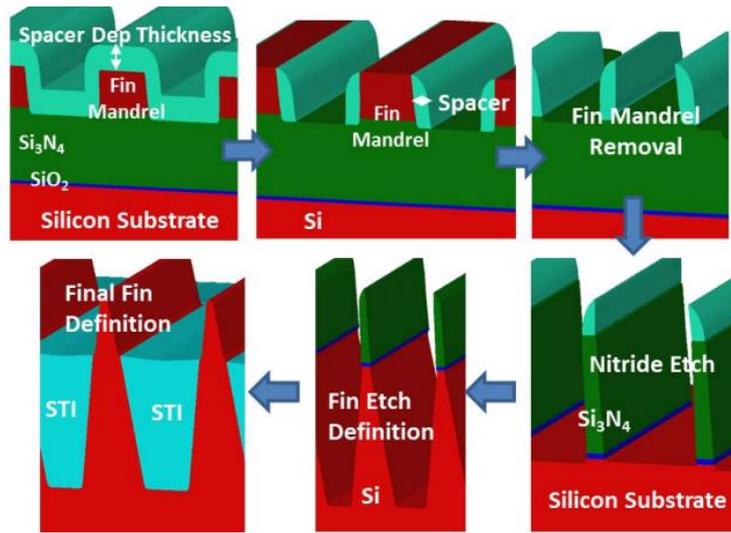


Figure 5-2: The process flow of 22 nm Intel FinFET technology developed with Coventor tools [RH-3].

Figure 5-3 shows that, in comparison to the TEM image [13], the fin profile modelled by SEMulator3D has an identical trapezoidal fin shape with similar dimensions. The modelled fin thickness and height are at 8 nm and 34 nm respectively. The overall width for this 22 nm Intel FinFET technology is defined by the following ratio (Kawasaki et al., 2009):

$$W = 2H + T$$

Where:

H is the fin height

T is the thickness of the device.

For this device, the overall width is 76 nm.

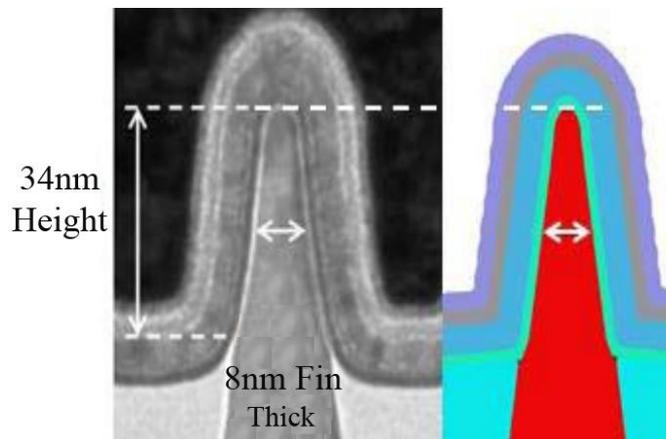


Figure 5-3: Comparison of the SEMulator 3D fin profile with the published SEM cross section (Louis Gerrer et al., 2015)

After the fin module and STI module are completed, the process continues with the development of the sacrificial gate, spacer formation and the source/drain formation. For a p-channel field effect transistor (pfet), the source/drain region is modelled by using the crystalline cavity etch, followed by silicon germanium (SiGe) selective epitaxial growth. On the other hand, for the n-channel field effect transistor (nfet), the source/drain region is modelled by silicon recess followed by silicon selective epitaxial growth.

The simulation continues with the metal gate replacement process, which involves the replacing of the sacrificial gate with the high- κ dielectric material and gate metal layer. The high- κ dielectric material comprises hafnium oxide (HfO_x) with a thickness of 2 nm and is deposited on a very thin oxide interface layer. The gate stack process continues with a thin TiN/TaN metal layer for the pfet and TiAl/TaN metal layer for the nfet. Both types of transistors (pfet and nfet) are filled with a WF gate metal layer. The fabrication follows the standard NiSi MOL steps in the final fabrication stage.

5.1.2 Doping Structure

In the previous section, the structure of the 22 nm Intel FinFET was simulated using SEMulator3D. The modelled FinFET pfet and nfet structures were then exported into a GARAND compatible format. The TCAD structure was then imported into GARAND for a statistical variability and statistical reliability analysis.

Figure 5-4 shows the TCAD structure modelled by the SEMulator3D (left) and TCAD device structure definition in GARAND mapped by the electron density (right). Due to the limited data available for this device, the doping concentration of the source/drain was implanted by using simple implantation simulation using maximum doping in the source drain region $2 \times 10^{20} \text{ cm}^{-3}$ and a Gaussian doping distribution in the extension regions.

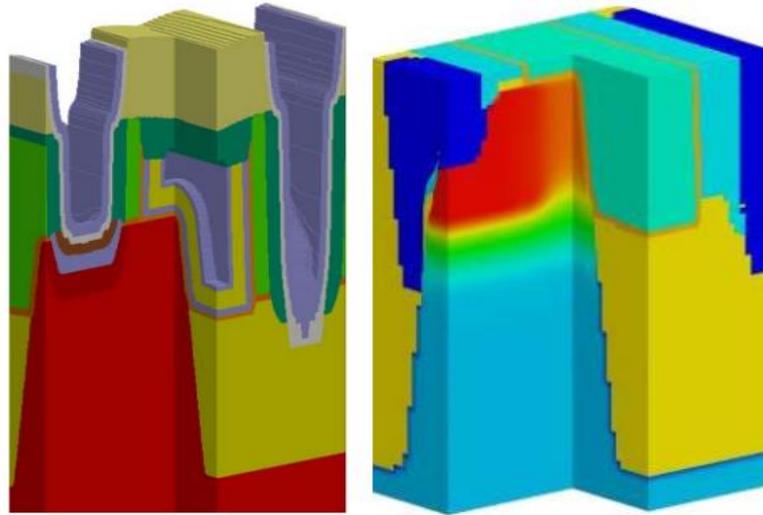


Figure 5-4: Structure definition of the FinFET device imported from the SEMulator3D (left) and the structure of the GARAND simulation mapped by electron density (right) [RH-3].

5.1.3 Device Calibration

The calibration of the FinFET simulation in respect of measurement IV characteristics includes two parts. The first part identifies the channel doping concentration, which produces the measured “off” current (I_{OFF}), sub-threshold slope (SS) and drain-induced barrier lowering (DIBL). The second part calibrates the mobility model to match the low and high drain bias of ON current (I_{ON}). The IV characteristics of the MP device are extracted from the published paper (Auth et al., 2012). The goal of the doping calibration is to accurately match the electrostatic integrity of the FinFET by adjusting the doping profile concentration to match SS, the leakage current and DIBL.

For the calibration, the following assumptions have been adopted. Firstly, the calibration of the MP device is based on the work function (WF) engineering, where the doping profile in the channel is kept as low as possible. Secondly, the threshold voltage and the leakage current in the SP, and LP FinFETs are reduced by increasing the channel doping concentration.

Several iterations of WF engineering and channel doping concentration improvement are performed during the simulation to produce good agreement between the TCAD simulation result and the published data in terms of the SS, leakage current and DIBL. The calibration continues with the velocity adjustment of the Caughey-Thomas mobility model (Caughey & Thomas, 1967) to ensure agreement with the IV characteristics at high drain biases. Finally, the drive current is further calibrated by a mobility adjustment using the RSX and the strain

parameters in the Massetti mobility model (Masetti, Severi, & Solmi, 1983). The calibration was performed by making incremental adjustment to the mobility model parameters. In order to match the figures of merit for the FinFET electrostatic integrity, as summarized in Table 5-2, the required channel doping concentration was found to be $1 \times 10^{17} \text{ cm}^{-3}$ with a WF engineering at 4.808 eV. Figure 5-5 shows that the agreement of the calibration results of the MP transistor in comparison with the experimental data.

Table 5-2: Figure of merit Intel 22nm FinFET technology extracted from the IV characteristics.

Properties	Value
SS	72 mV/dec
DIBL	56 mV/V
I_{ON}	136 nA/ μm
I_{OFF}	1490 $\mu\text{A}/\mu\text{m}$

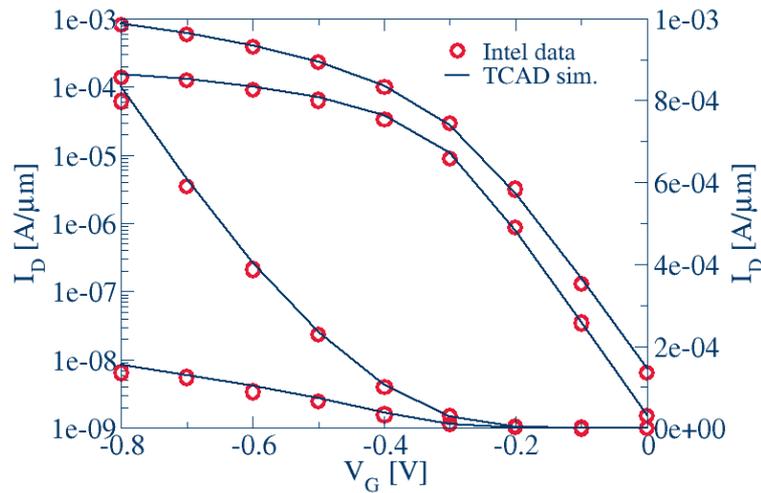


Figure 5-5: The calibration result of the TCAD simulation and experimental result for the MP device which show good agreement [RH-3].

5.1.4 Transforming the MP device into the SP and LP transistors

The transformation process of the calibrated MP transistors into the SP and LP transistors is presented in this section. Due to the limited information on the device's properties, the transformation process is based solely on the channel doping concentration.

The MP FinFET calibration was achieved using a low doping concentration resulting in leakage current of $1490 \mu\text{A}/\mu\text{m}$. In order to reduce the leakage current, the channel doping profile concentration was increased to an appropriate value to achieve a specific leakage current target. Based on the published data, the I_{OFF} at high drain bias ($V_{\text{D}}=0.75 \text{ V}$) for the

SP and LP FinFETs are 1 nA and 30 pA respectively. It was found that, increasing the doping concentration from $1 \times 10^{17} \text{ cm}^{-3}$ to $2 \times 10^{18} \text{ cm}^{-3}$ will transform the MP device into the SP device with a leakage current at 1 nA.

Subsequently, increasing the channel doping up to $5 \times 10^{18} \text{ cm}^{-3}$ will transform the MP FinFET into the LP FinFET with a leakage current of 30 pA. Figure 5-6 shows the IV characteristics of the SP and LP device following the corresponding adjustment of the channel doping concentration. The remaining parameters used in the MP FinFET simulation remain the same in the SP and LP simulations. Table 5-3 summarises key figures of merit for the 22 nm Intel FinFET technology characteristics for the SP device and the LP device.

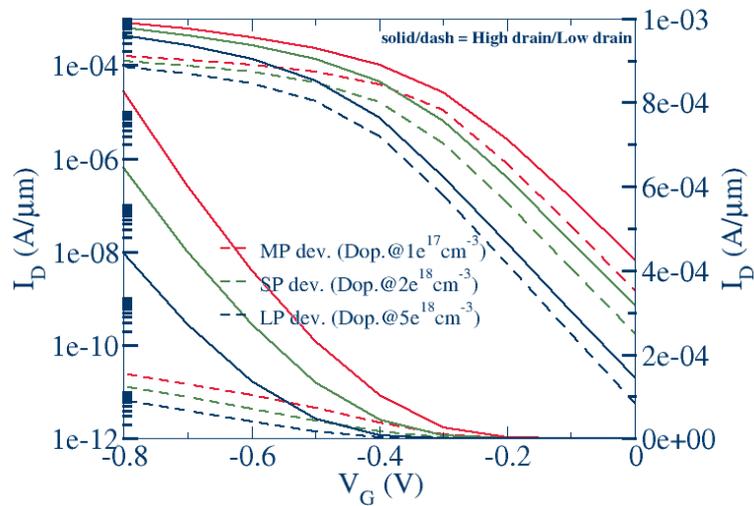


Figure 5-6: Transforming the MP device into SP and LP devices by increasing the channel doping concentration.

Table 5-3: The Intel 22nm FinFET technology characteristics for SP and LP devices (Jan et al., 2012).

Transistor Type	Standard Power (SP)	Low power (LP)
I_{D sat}	0.59 μA	0.37 μA
I_{D off}	1 nA	30 pA
Drain bias	0.75 V	0.75 V

5.2 Statistical Variability

In this stage, the calibration process must taken into account the impact of the statistical variability introduced by the granularity of charge and matter. Random discrete dopants (RDD), gate edge roughness (GER) and metal gate granularity (MGG) are considered as statistical variability (SV) sources for both n-channel and p-channel FinFET. At the time this study was performed, there was no statistical variability data published for the 22 nm Intel

FinFET technology. The technology used in the fabrication of the FinFETs utilising a sidewall definition of the spacer to define the fin, results in a correlation in the fin edge roughness (FER) and for this reason the impact on the statistical variability is very little.

In contrast with the FER the gate edge roughness (GER) is modelled using $3\Delta = 2$ nm rms and a correlation length Λ of 25 nm. This parameter reflects the current state of the art in well-tuned CMOS technology. The RDD is mainly defined by the doping concentration in the channel delivering a different impact for the MP and LP FinFETs. Finally, for the TiN gate metal used, it has been assumed that the metal gate granularity (MGG) has 0.2 V of WF difference between two major grain orientations with a probability of 0.4/0.6 for a lower and higher WF respectively. The average grain size used in this MGG simulation is 5 nm (Xingsheng, Brown, Binjie, et al., 2011).

A typical domain used in the simulation of the 22 nm Intel FinFET technology is illustrated in Figure 5-7. This figure shows only the fin of the FinFET and maps the potential distribution impact of RDD, GER and MGG as statistical variability sources.

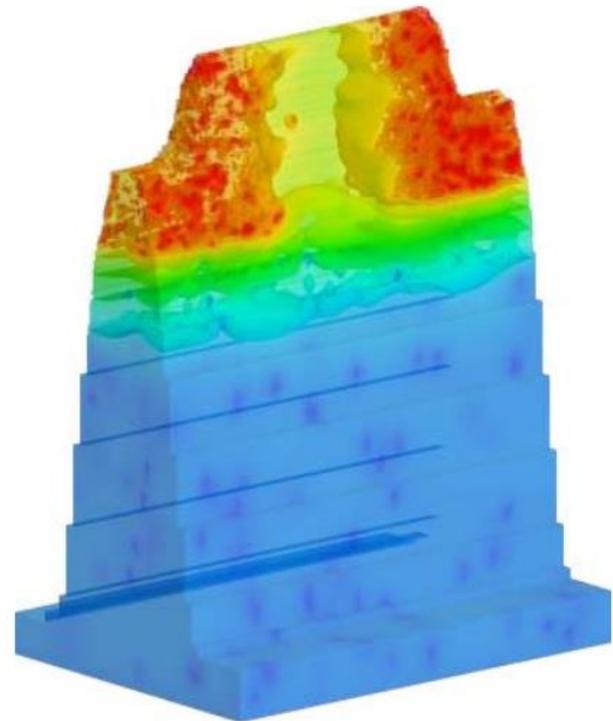


Figure 5-7: 22 nm Intel FinFET technology mapped by potential distribution subject to the simultaneous action of statistical variability induced in the device. Only the silicon fin is shown in this figure [RH-3].

The SV in the 22 nm Intel FinFET technology is simulated for both the MP and LP devices. The wide dispersion of the I_D - V_G characteristic of a sample of 1,000 microscopically

different devices is illustrated in Figure 5-8 (left) for the MP device and (right) for the LP device. The IV characteristics are simulated at both low and high drain biases of 50 mV and 0.8 V respectively. The distribution of the atomistic $I_D V_G$ characteristics around a uniform device shows the impact of the SV sources.

It is clear that the LP FinFET has more dispersion compared to the MP FinFET due to the higher dopant concentration inside the channel. This can be attributed to the transformation process of the LP from the MP FinFET which requires an increase in the doping concentration in the channel.

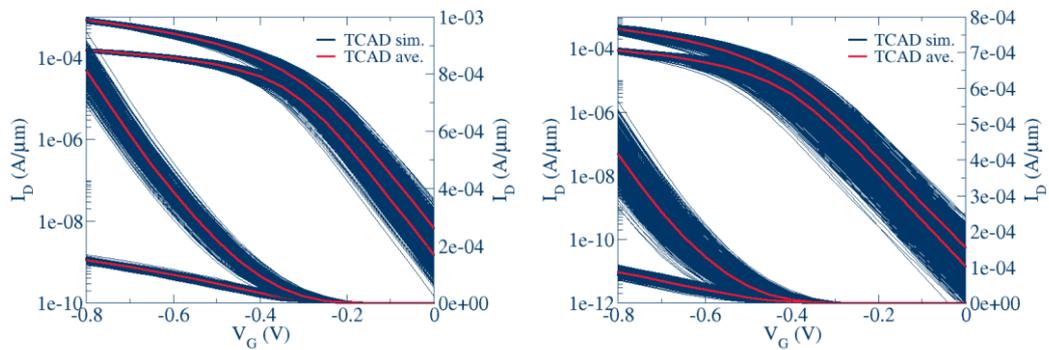


Figure 5-8: An atomistic simulation of 22 nm Intel FinFET for the MP FinFET (left) and LP FinFET (right) after inducing statistical variability in the calibrated uniform device.

One of the advantages of using the TCAD simulator is the ability to analyse the impact of individual SV sources on the device. Based on the SV parameters used in the 22 nm Intel FinFET technology, the impact of the combined SV and individual SV sources for both the MP FinFET and the LP FinFET are illustrated in Figure 5-9. In order to have a similar threshold voltage criteria in both devices, the threshold voltage for MP and LP FinFETs have been calculated at 1.48×10^{-8} A/ μ m and 6.5×10^{-7} A/ μ m respectively.

Based on these analysis, the MP FinFET has a threshold voltage dispersion of 17 mV compare the LP FinFET dispersion of 30 mV, resulting from the fact that the LP FinFET has a greater channel doping concentration when compared to the MP device. The simulated dispersion of the LP FinFET at 30 mV is consistent with recently published measurement data (Natarajan et al., 2014).

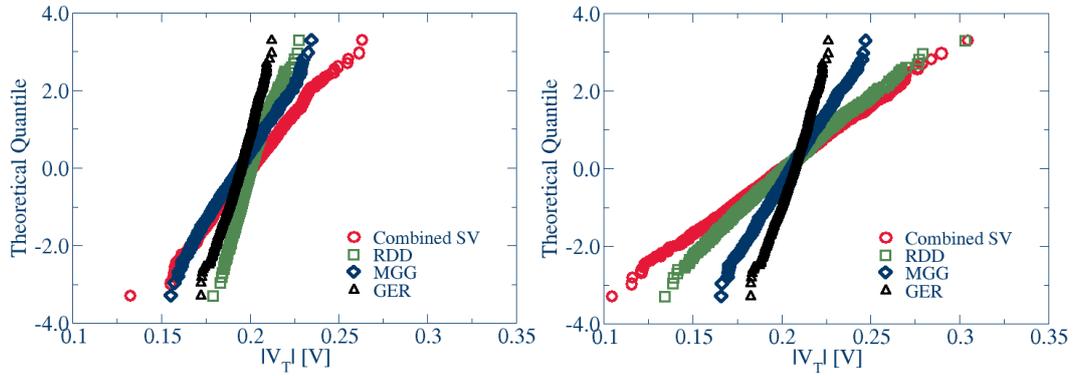


Figure 5-9: The threshold voltage distribution of the MP FinFET (left) and the LP FinFET (right) for separate and combined variability sources for the p-channel FinFET [RH-3].

The I_{ON} - I_{OFF} ratio is another important parameter in a digital logic circuit governing the switching activity. A poor I_{ON} - I_{OFF} ratio can result in an impractical low output swing, whilst an appropriate I_{ON} - I_{OFF} ratio can improve the speed and leakage current. The OFF current is measured when the gate voltage is equal to 0 V and the ON current is measured when the gate voltage is equal to the supply voltage which in this case is 0.8 V. Figure 5-10 shows the average I_{ON} - I_{OFF} ratio over 1,000 TCAD FinFET simulations. These results are in close agreement with the experimental data where the average I_{ON} - I_{OFF} ratio is located inside the distribution cloud of the I_{ON} - I_{OFF} ratio published results (Jan et al., 2012).

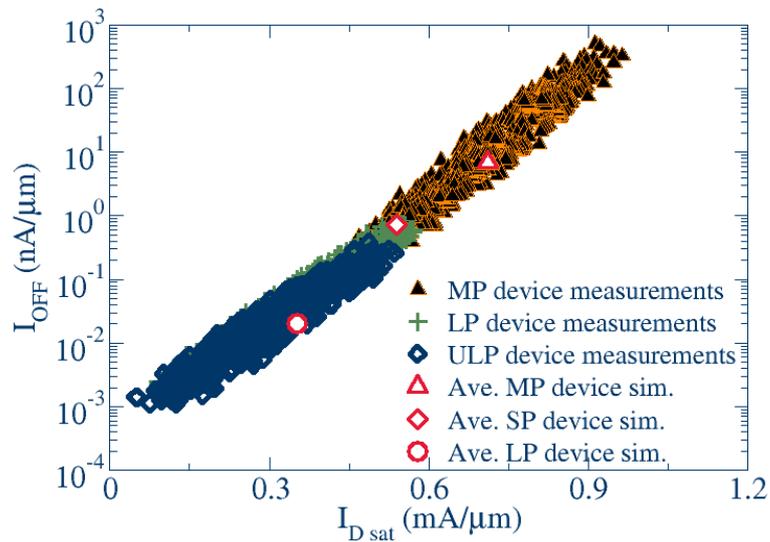


Figure 5-10: Simulated and published I_{ON} - I_{OFF} ratios for the various p-FinFETs [RH-3].

5.2.1 Random Discrete Dopants

Random discrete dopants (RDD) play a significant role in SV for 22 nm Intel FinFET technology which introduces inhomogeneity in the electrostatic potential landscape of the

transistors. This results in different V_T of the microscopically different transistors, associated with different percolation paths. As described in the previous section, the channel doping concentration in the MP FinFET is $1 \times 10^{17} \text{ cm}^{-3}$, whereas in the LP device, the channel doping concentration is $5 \times 10^{18} \text{ cm}^{-3}$. The significant increase in doping concentration between the MP FinFET and LP FinFET contributes to the increase in the threshold voltage dispersion. In the MP FinFET, the RDD induced dispersion is approximately 7 mV, whereas in LP FinFET the dispersion increases to approximately 24 mV.

Figure 5-11 shows the dispersion of the threshold voltage for the MP FinFET (left) and LP FinFET (right) simulated using a statistical sample of 1,000 transistors, where only the RDD are taken into account. The threshold voltage for the MP and LP FinFET was measured at $1.48 \times 10^{-8} \text{ A}/\mu\text{m}$ and $6.5 \times 10^{-7} \text{ A}/\mu\text{m}$ respectively. The significant increment in channel doping concentration when transforming the MP FinFET into the LP FinFET, results in the RDD playing a major role in the statistical variability of the LP FinFET.

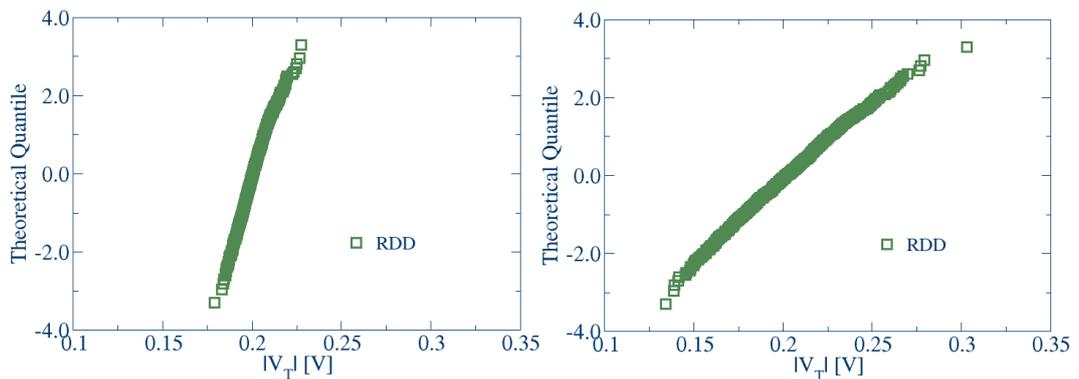


Figure 5-11: Distribution of threshold voltage dispersion for the MP FinFET (left) and LP FinFET (right) due to RDD parameters over 1,000 device simulations.

5.2.2 Gate Edge Roughness

GER is one of the important statistical variability sources for the Intel FinFETs. The impact of the GER is similar to the impact of LER in planar MOSFET, as discussed in the previous chapter. The LER is affected by the molecular resist granularity and uncertainties during the lithography process. The GER in this simulation is modelled using a Fourier synthesis based approach (Asenov, Kaya, et al., 2003b). GER is defined by two important parameters, the root mean square (RMS) magnitude of LER, Δ and the correlation length as Λ . Previous analysis shows that for a well-tuned CMOS technology, the rms magnitude Δ of 0.66 resulting in LER of 2 nm and typical correlation length Λ is 25 nm (Xingsheng, Brown, Binjie, et al., 2011). These parameters are used to define the GER in this analysis.

The implementation of GER in the atomistic TCAD simulation results in local fluctuations in the channel length resulting in the variations of threshold voltage shown in Figure 5-12. The threshold voltage is measured again at 1.48×10^{-8} A/ μm and 6.5×10^{-7} A/ μm for the MP and LP FinFETs respectively. The MP FinFET has a V_T dispersion of 6.5 mV, while the LP device has a V_T dispersion of 7 mV. The impact of GER for the MP transistor is compatible to the impact of RDD. For the LP transistor however the impact is much smaller compared to the impact of RDD.

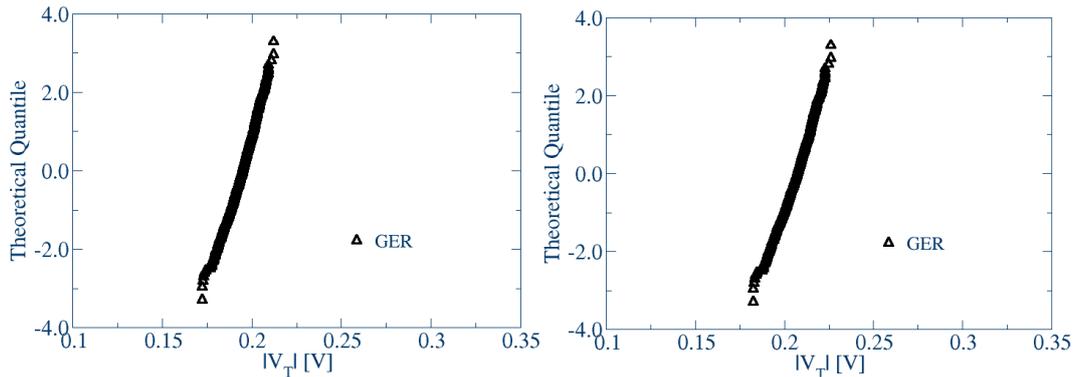


Figure 5-12: Distribution of threshold voltage dispersion for the MP FinFET (left) and LP FinFET (right) due to GER over 1,000 device simulations.

5.2.3 Metal Gate Granularity

In this section, MGG is introduced into the SV analysis. The impact of this SV source is compared to the impact of GER and RDD. The MGG simulation is based on two important parameters. The first parameter is the average grain size which was assumed to have a diameter of 5 nm. The second parameter is the WF difference due to the two major grain orientations, $\langle 200 \rangle$ and $\langle 111 \rangle$, which is assumed to be a 0.2 V WF span. The first orientation $\langle 200 \rangle$ appears with a probability of 60% which results in the higher WF (Dadgour, Endo, De, & Banerjee, 2008).

Figure 5-13 illustrates the impact of MGG on both the MP and LP FinFETs over 1,000 device simulations. The result shows that the MP FinFET has a threshold voltage dispersion of 14 mV, while the LP FinFET has an average threshold voltage dispersion of 13.6 mV.

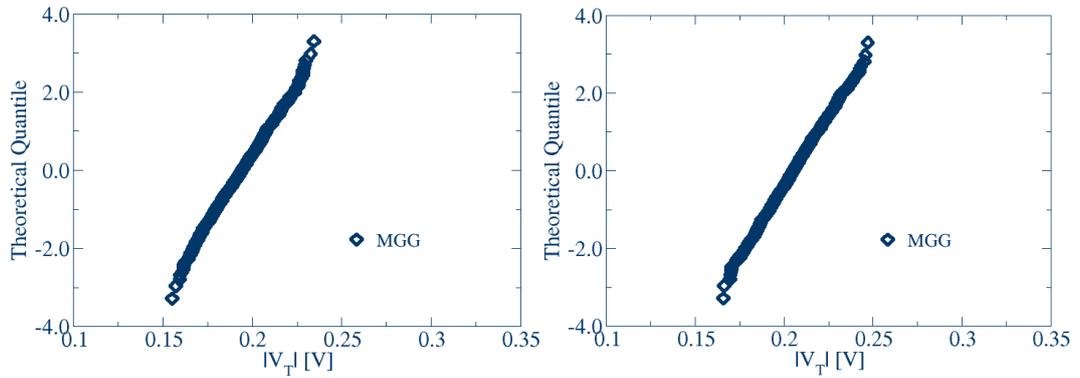


Figure 5-13: The distribution of threshold voltage dispersion for the MP FinFET (left) and LP FinFET (right) as a result of the MGG parameters over 1,000 device simulations.

5.3 Statistical Reliability (BTI)

In this section, the FinFET is subjected to a statistical BTI simulation analysis by using ensembles of 1,000 microscopically different transistors including SV sources and with average trap density corresponding to three levels of degradation. The degradation of the FinFET performance is monitored in respect to the fresh transistor (at t_0) and includes average trapped charge densities of $3.2 \times 10^{11} \text{ cm}^{-2}$ and $7.2 \times 10^{11} \text{ cm}^{-2}$ for a degraded transistor at t_1 and t_2 respectively for the MP FinFETs. For the degraded LP FinFETs, the average trapped charge density is assumed to be $4.6 \times 10^{11} \text{ cm}^{-2}$ and $1.2 \times 10^{12} \text{ cm}^{-2}$ at t_1 and t_2 respectively. The average trapped charge density is based on the corresponding average threshold voltage shift in the simulated transistors. The trapped charge numbers in the individual transistors follow a Poisson distribution. For each level of trapped charge induced in the FinFET, the IV characteristics are simulated for a gate voltage ramping from 0 up to 1.5 V. At each ageing level, the device performance of both MP and LP FinFETs is evaluated in terms of threshold voltage and ON current dispersion.

The Intel MP transistor is evaluated in terms of averages and the dispersion of V_T . For the MP FinFETs as a result of the ageing process, the average V_T increased from 200 mV to 212 mV and 227 mV at t_1 and t_2 respectively. Simultaneously, the standard deviation of V_T , increases from 17.3 mV to 18.2 mV and 19.5 mV at t_1 and t_2 respectively. Figure 5-14 illustrates the V_T distribution of the MP FinFET at different levels of degradation. The trend of the mean and standard deviation of V_T for the MP device is shown in Figure 5-15. The increase in the dispersion of V_T , is related to the interaction between the SV sources and the increase in the average number of traps at the interface.

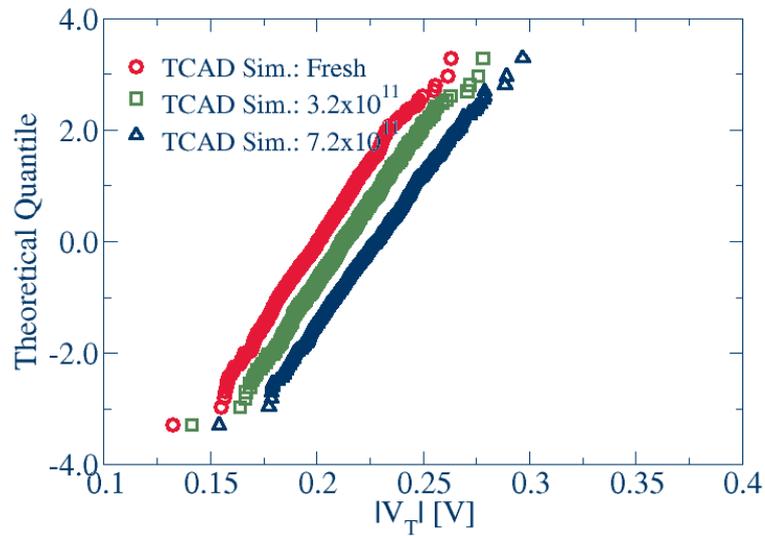


Figure 5-14: The distribution of the threshold voltage of the MP FinFET for a TCAD simulation at several levels of degradation [RH-3].

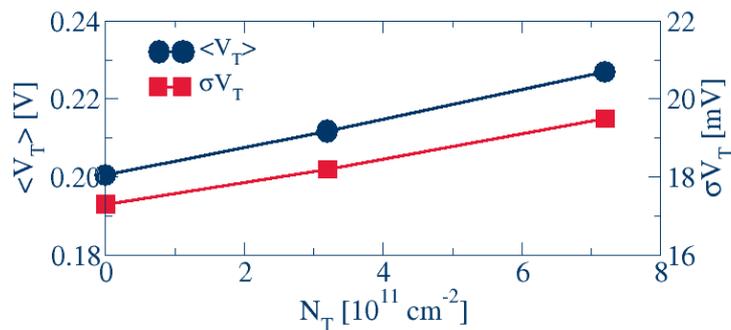


Figure 5-15: Summary of the ageing of the MP FinFET at different levels of degradation

An investigation of the BTI degradation was also performed on the LP device. The average threshold voltage increases from 201 mV in the fresh transistor to 216 mV and finally to 243 mV at t_1 and t_2 respectively. Simultaneously, in the standard deviation increases from 29.6 mV in the fresh transistor, 30.8 mV and 32.2 mV at t_1 and t_2 respectively. Figure 5-16 illustrates the V_T distribution of LP FinFETs at different levels of degradation.

The trend of the mean and standard deviation of V_T for the LP device is shown in Figure 5-15. The increase in the dispersion as a result of the degradation stems from the interaction between the initial SV sources and the increase in the average number of traps at the interface. For both mean, V_T and the standard deviation of V_T both MP and LP FinFETs show similar trends.

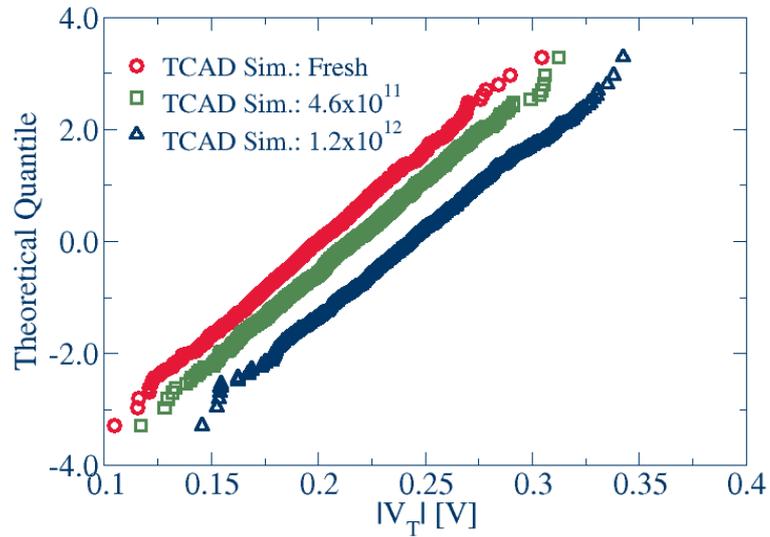


Figure 5-16: The distribution of the threshold voltage of the LP FinFET for a TCAD simulation at several levels of degradation [RH-3].

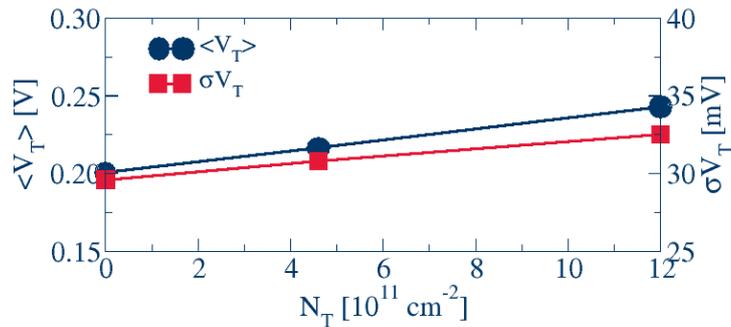


Figure 5-17: Summary of the ageing of the LP FinFET at different levels of degradation

The BTI phenomenon is further analysed in terms of drive current, which is important in relation to the timing variation in a circuit simulation. Figure 5-18 presents the distribution of I_{ON} for the MP device, having a dispersion of 3.44×10^{-7} A for a fresh device, which is associated only with the impact of SV sources present in the simulations. As the degradation progress to t_1 and t_2 , the dispersion of I_{ON} increased up to 3.5×10^{-7} A and 3.6×10^{-7} A respectively. The I_{ON} average decreases as the trap density increases as expected. For a fresh device, the average of I_{ON} was 9.0×10^{-6} A. After the degradation to t_1 and t_2 , the I_{ON} average reduces to 8.9×10^{-6} A and 8.6×10^{-6} A respectively. The trend of the mean and standard deviation of I_{ON} for the MP device is shown in Figure 5-19.

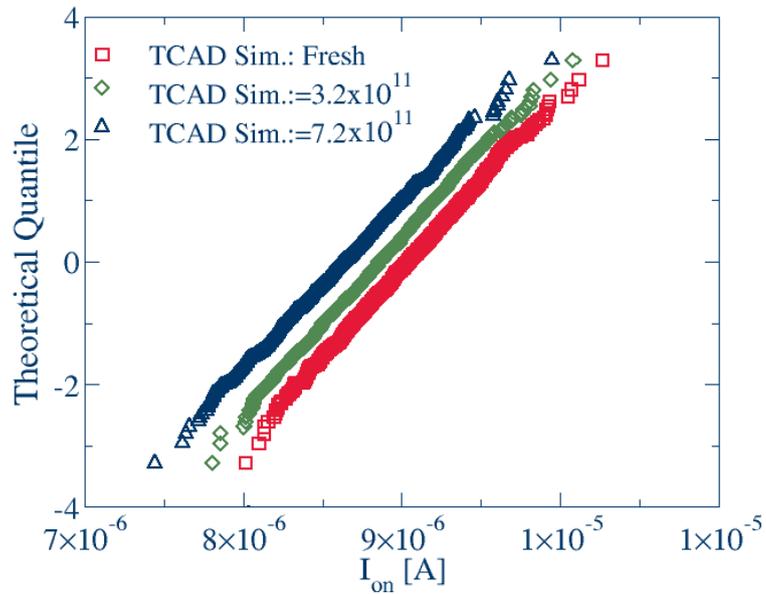


Figure 5-18: The distribution of the I_{ON} of the MP FinFET for a TCAD simulation at several levels of degradation. The drive current is measured at a gate voltage of 0.8 V.

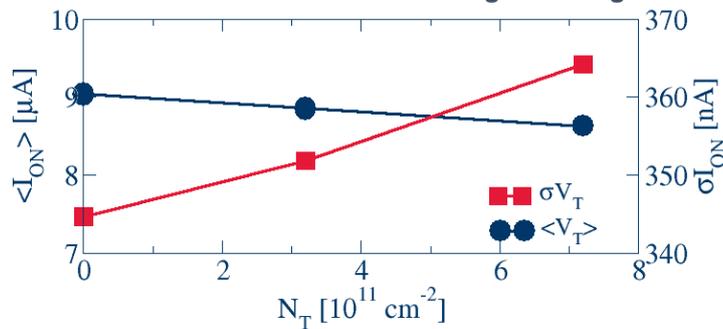


Figure 5-19: Summary of the ageing MP FinFET at different levels of degradation.

Figure 5-20 shows the distribution of I_{ON} for the LP device having a dispersion of 2.8×10^{-8} A for a fresh device, which is only associated with the impact of the initial SV sources. As the device is aged to t_1 and t_2 , the dispersion of I_{ON} increased up to 2.9×10^{-8} A and 3.0×10^{-8} A respectively. Simultaneously, the I_{ON} average decreased from 3.1×10^{-7} A in the fresh device to 2.9×10^{-7} A and 2.7×10^{-7} A at t_1 and t_2 respectively. The trend of the mean and standard deviation of the I_{ON} for the LP FinFET is shown in Figure 5-19.

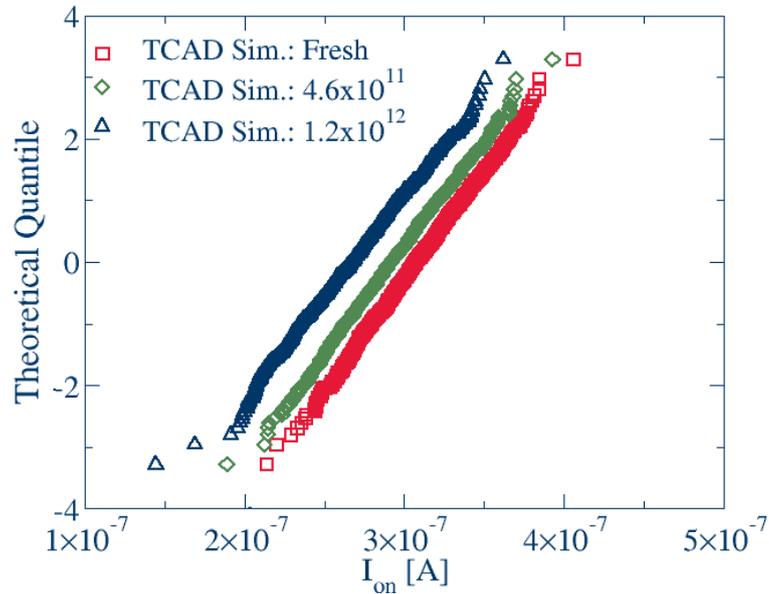


Figure 5-20: The distribution of the I_{ON} of the LP FinFET for a TCAD simulation at several levels of degradation. The drive current is measured at a gate voltage of 0.8 V.

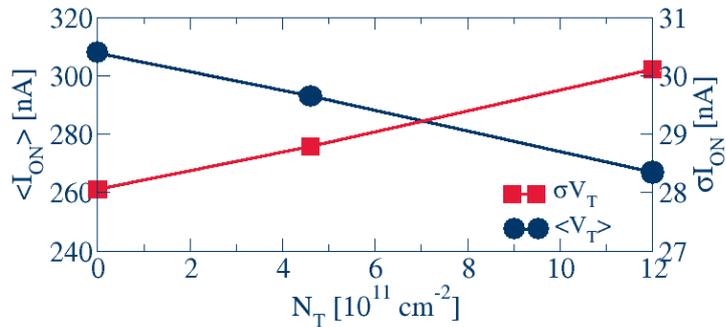


Figure 5-21: Summary of the ageing LP FinFET at different levels of degradation.

5.4 Summary

In this chapter, the calibration of the 22 nm Intel FinFET CMOS technology using the GSS 3D simulator, and GARAND was described to allow the prediction of the device degradation associated with the interaction between statistical variability and statistical reliability. The MP and LP FinFETs have been analysed in terms of V_T and I_{ON} distributions at several different degradation levels. Qualitatively the threshold voltage trends in respect of mean and dispersion are similar to the trends in the 70 nm bulk IMEC MOSFET.

From the statistical variability perspective, the impact of the individual and combined statistical variability source, for both the MP and LP FinFETs have been analysed in detail. It was assumed in this study that the LP device was realised by increasing the channel doping concentration only. The simulation reveals that, the statistical variability in the MP FinFET

is dominated by MGG, due to the relatively low channel doping concentration, whereas in the LP FinFET, RDD is the dominant source of statistical variability.

The impact of the statistical reliability was evaluated at two different levels of degradation. It is expected that the average and the standard deviation of the threshold voltage increase with the increase of the degradation time. The simulations for the first time provide quantitative values for the magnitude of the BTI degradation in the 22 nm Intel technology FinFETs.

Chapter 6: 6T SRAM Ageing Simulation

Background

With the progression of CMOS scaling, the stability of the static random access memory (SRAM) cell has become a critically important issue and a concern among design and test engineers (Kuo et al., 1990; Kwai, Chang, Liao, Chiao, & Chou, 2000; Meixner & Banik, 1997). The impact of statistical variability (SV) due to the granularity of charge and discreteness of matter on the SRAM yield has become increasingly challenging for the semiconductor industry (Asenov, Brown, et al., 2003). Thus, the accurate modeling of SV has become essential for circuit design engineers to handle variability aware design and simulation for an accurate prediction of product performance and yield (Aadithya et al., 2011). Additionally, the reliability phenomenon related to existing and build in an increase of SV with time and has to be properly considered in the design process (Kaczer et al., 2012).

This chapter outlines the compact model (CM) library extraction and the circuit simulation methodology based on the calibrated TCAD simulations performed in the previous two chapters. The 70 nm bulk imec MOSFET and the 22 nm Intel FinFET technology have been used in the CM extraction ("GSS simulator, "). Two levels of CM extraction, namely uniform and statistical CM extractions are involved in this process. The accuracy of the CM extraction is evaluated at each level of the extraction process. Once the CM library is produced, the performance of the two technologies at circuit level is evaluated using 6T-SRAM cells in terms of static noise margin (SNM) based on several scenarios of the SRAM operation. Finally, the comparisons between these technologies is summarised in the final section.

6.1 Compact Model Extraction

The process of CM extraction involves two stages. The first stage is a uniform CM extraction followed by statistical CM extraction. The BSIM4 CM is used for 70 nm bulk imec MOSFET while BSIM-CMG CM is used for 22 nm Intel FinFET. The following sections discuss details of each step of the extraction process.

6.1.1 Uniform Compact Model

The initial process of CM extraction uses a uniform continuously doped transistor to produce a full basic CM model library without introducing any variability effects. The extraction results for both technologies under investigation transistors are presented in the next subsections.

6.1.1.1 70 nm bulk imec MOSFET

In order to perform the uniform CM extraction, sets of the transfer characteristic ($I_D V_G$) and output characteristic ($I_D V_D$) are required. The CM extraction process utilised the $I_D V_G$ characteristic is performed at different substrate bias voltages of $V_B = -0.4$ V, $V_B = 0.0$ V and $V_B = 0.4$ V. While the utilised output $I_D V_D$ characteristics are simulated with gate bias of $V_G = 0.6$ V, $V_G = 0.8$ V and $V_G = 1.0$ V.

The extraction process methodology using Mystic is described in Section 3.3.1. This approach aims to achieve a specified extraction error with respect to the targeted IV characteristics of the simulated transistor. The average percentage relative error is described in Equation 6.1:

$$E_{\mu} = \frac{1}{n} \sum_{1 \rightarrow n} E_n \quad (6.1)$$

where E_{μ} is the average percentage relative error and E_n represents the n^{th} individual percentage error for each target IV characteristic of the p-channel 70 nm IMEC technology transistor having an error of 5.271%, while the n-channel transistor has an error of 2.952% as illustrated in Figure 6-2 (right). The extraction process based on the IV characteristic produces an error of 3.124% for a p-channel transistor and 1.84% for n-channel transistor. The comparison of IV characteristics between TCAD simulation and the extracted CM is presented in Figure 6-2 and Figure 6-3. As a result, the average percentage relative error for

a p-channel transistor and n-channel transistor is 4.198% and 2.408% respectively. Details of these errors are summarised in Table 6.1.

Table 6-1: Summary the average percentage relative error in the extraction CM process. The minimum percentage error indicates the closeness of CM extraction in preserving the TCAD transistor characteristic.

	$I_D V_D$ characteristic	$I_D V_G$ characteristic	Average percentage relative error
p-channel transistor	5.271%	3.124%	4.198%
n-channel transistor	2.952%	1.864%	2.408%

The average percentage relative error of 2.4% shows that the uniform CM extraction process captures well the drain bias dependence and the substrate bias dependences. Once the process of uniform CM extraction is completed, the uniform CM library is generated and used in the statistical CM extraction process.

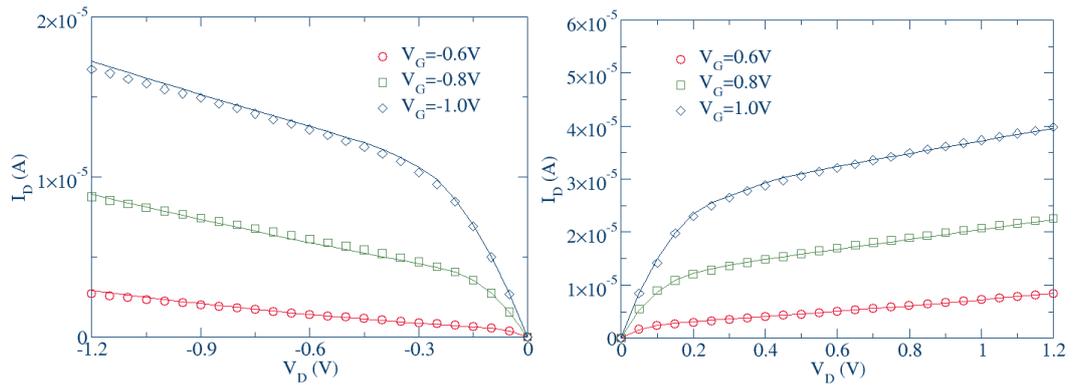


Figure 6-1: The comparison of output characteristic for p-channel transistor (left) and in n-channel transistor (right). Solid lines illustrate TCAD simulation results while CM simulation results are shown by symbols.

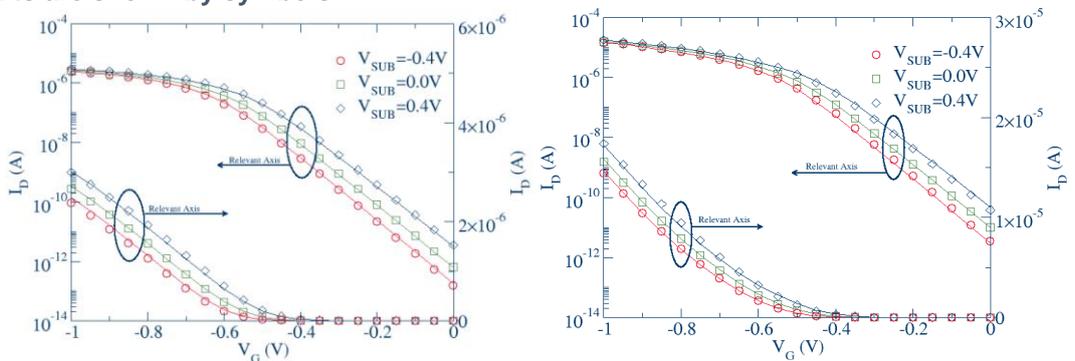


Figure 6-2: The comparison of the transfer characteristic of the p - channel transistor by using drain bias at $V_D=50$ mV (left) and using drain bias at $V_D=1.0$ V (right). TCAD simulation results are illustrated by solid lines while CM simulation results are shown by symbols.

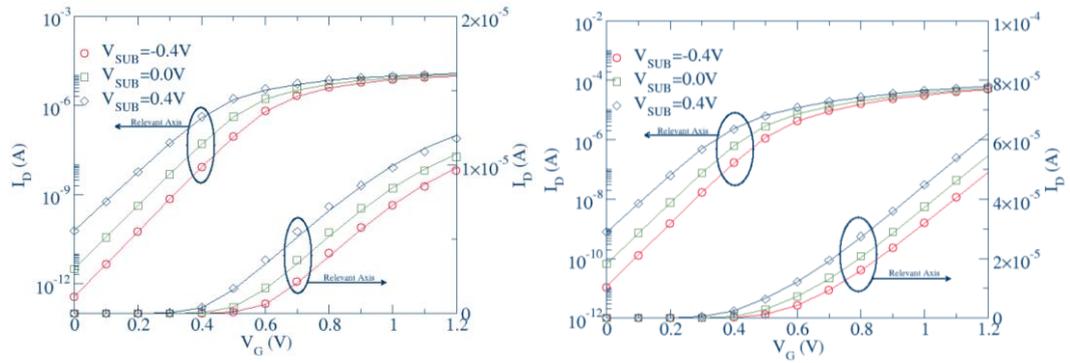


Figure 6-3: The comparison of the transfer characteristic of an n - channel transistor by using drain bias at $V_D=50$ mV (left) and using drain bias at $V_D=1.0$ V (right). Solid lines illustrate 0 V. TCAD simulation results while CM simulation results are shown by symbols.

6.1.1.2 22 nm Intel FinFET

In this section the extraction results of the 22 nm Intel FinFET are presented and discussed. The uniform CM extraction is based on a set of $I_D V_G$ and $I_D V_D$ characteristics. Several gate biases of $V_G=0.5$ V, $V_G=0.6$ V and $V_G=0.7$ V are used for the simulation of the IV characteristic. Substrate bias of $V_B=0.0$ V at low drain and high drain of $V_D=0.05$ V and $V_D=0.8$ V respectively are used in the simulation of the $I_D V_D$ characteristics.

The extraction process for the FinFETs is similar to the extraction process used for the 70 nm bulk imec MOSFETs discussed earlier. The iteration in the extraction process continues until the average percentage relative error reaches the desired value.

The percentage errors in the extraction process for $I_D V_D$ characteristic of a p-channel and n-channel FinFETs are 5.712% and 6.253% respectively. The accuracy in the extraction process for this output characteristic is illustrated in Figure 6-4. For the transfer characteristic, the percentage error of a p-channel transistor is 2.281% and for the n-channel transistor is 2.324%. The comparison of IV characteristic between TCAD simulation and the extracted CM is illustrated in Figure 6.5. The total relative percentage error calculated for a p-channel transistor and n-channel transistor is 3.997% and 4.289% respectively. Details of the errors related to the CM extraction of the transistors are given in Table 6.2.

Table 6-2: summarise the average percentage relative error in the extraction CM process. The minimum percentage error indicates the closeness of CM extraction in preserving the TCAD transistor characteristic.

	$I_D V_D$ characteristic	$I_D V_G$ characteristic	Average percentage relative error
p-channel transistor	5.712%	2.281%	3.997%
n-channel transistor	6.253%	2.324%	4.289%

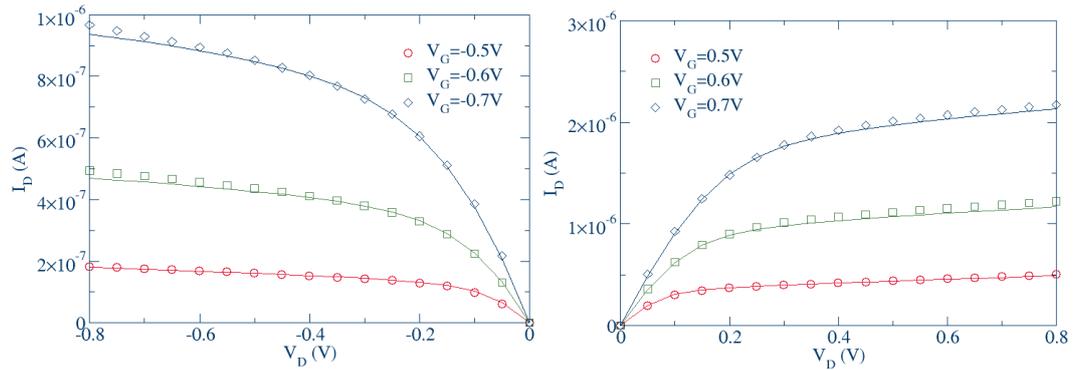


Figure 6-4: The comparison of output characteristic for p-channel transistor (left) and in n-channel transistor (right). TCAD simulation results are illustrated by solid lines while CM simulation results are shown by symbols.

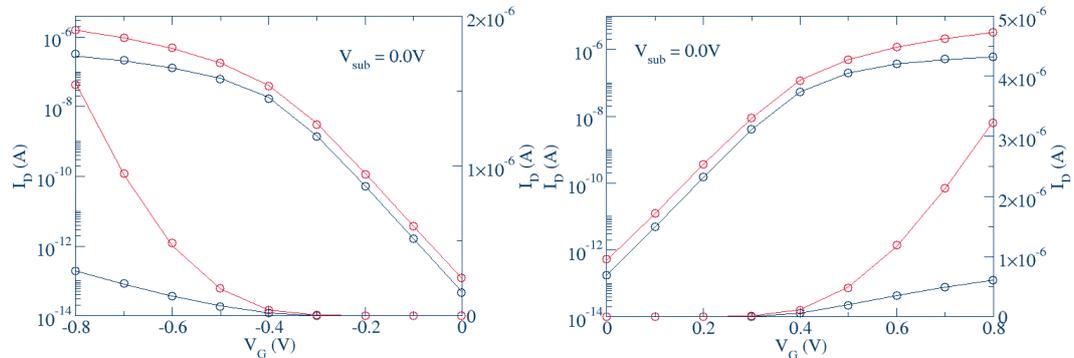


Figure 6-5: The comparison of transfer characteristic for p-channel transistor (left) and in n-channel transistor (right). TCAD simulation results are illustrated by solid lines while CM simulation results are shown by symbols.

6.1.2 Statistical Compact Model

The second stage of the CM extraction process of producing a complete CM library is the statistical CM. At this stage, the extraction process includes the simulated $I_D V_G$ characteristic of an ensemble of ‘atomistic’ TCAD transistors. The SV sources depend on the gate material used in the transistors of interest. For example in the simulations of the 70 nm bulk imec MOSFET, poly-silicon is used as a gate material leading to random discrete dopants (RDD),

line edge roughness (LER) and poly-silicon granularity (PSG) as SV sources (Asenov, Brown, et al., 2003; Reid et al., 2010). While for a 22 nm FinFET, metal gate material is used leading to RDD, gate edge roughness (GER) and metal gate granularity (MGG) considered as the SV sources in the TCAD simulations (X. Wang et al., 2011).

Moreover, the time dependent variability has also been introduced in the atomistic TCAD simulations. This will enable investigation of the impact of the bias temperature instability (BTI) degradation process (Muhammad Ashraful Alam & Mahapatra, 2005; Tibor Grassler, Kaczer, et al., 2011; Kaczer et al., 2010; Rauch III, 2007; Schroder, 2007; Stathis & Zafar, 2006) on the SRAM circuit behaviour. For the purposes of this study, several levels of degradation have been considered. Results for both technologies considered in this study are presented in the next section.

6.1.2.1 70 nm bulk imec MOSFET

The extraction of statistical CM is based on the atomistic TCAD simulation of an ensemble of 1000 transistors with a uniform CM library presented in the Section 6.1.1.1 as a reference.

Apart for the variability in the fresh transistors, three levels of degradation have been considered corresponding to average charge sheet density of $1 \times 10^{11} \text{ cm}^{-2}$, $5 \times 10^{11} \text{ cm}^{-2}$ and $1 \times 10^{12} \text{ cm}^{-2}$. These degradation levels are chosen based on the experimental data published in (Toledano-Luque et al.). For each level of degradation, ensemble of 1000 $I_D V_G$ characteristic are simulated at both low and high drain biases.

After a careful sensitivity analysis the following parameters have been selected for the statistical CM extraction; d_{sub} , $nfactor$, V_{OFF} , V_{SAT} , U_a and V_{TH0} to capture the statistical variability in the fresh and degraded transistors. The selected parameter set is based on their physical importance in capturing specific aspect of the transistor behaviour. Moreover, the combination of selected parameters can capture accurately the correlation between the key transistor figures of merit. For example the d_{sub} parameter accounts for the drain-induced barrier lowering (DIBL). The complete description of the selected parameter sets is summarised in Table 6.3.

Table 6-3: selected parameter set used in the extraction process

Parameter	Description
dsub	DIBL coefficient
nfactor	Sub-threshold swing factor
V_{OFF}	Offset voltage in sub-threshold region
V_{SAT}	Saturation velocity of the carrier
V_{TH0}	Threshold voltage
Ua	Mobility coefficient

The distribution of extracted parameters is expected to be unimodal and often needs to be characterised by four distribution moments (mean, standard deviation (STD), skew and kurtosis) (Ramberg, Dudewicz, Tadikamalla, & Mykytka, 1979). If this unimodal distribution is represented by higher order moments which have complex correlation, the parameter generation process becomes more complicated and requires a larger sample set of data.

The distributions of the selected parameter set can be analysed in the form of QQ-plots with a dashed line indicating the Gaussian distribution. Unimodal distribution of each parameter at each level of degradation is observed. If this condition is not met, then the extraction process is repeated by improving the extraction strategy. Most of the distribution parameters set illustrated in Figure 6-6 to Figure 6-11 have non-Gaussian distribution. For example V_{TH0} for the n-channel fresh transistor in Figure 6-6 shows a skewed distribution. V_{SAT} for the n-channel transistor degraded at $1 \times 10^{12} \text{ cm}^{-2}$ in Figure 6-11 has a distribution with a significant kurtosis. The impact of skew and kurtosis in this distribution are determined by the physical meaning in each particular transistor.

In the statistical extraction process, the average percentage error is an important measurement for the quality of the extraction. In the case of the p-channel transistor, the fresh transistor has an average error of 3.194% with a standard deviation (STD) of 0.504%, the degraded transistor at t_1 has an average error at 3.272% and STD of 0.543%, the degraded transistor at t_2 has an average error at 3.801% and STD of 0.665% and finally the degraded transistor at t_3 has an average error at 4.093% and STD of 0.943%. For an n-channel transistor, the fresh transistor has an average error at 2.633% with STD of 0.867%, the degraded transistor at t_1 has an average error at 2.675% and STD of 0.895%, the degraded transistor at t_2 has an average error at 2.963% and STD of 1.061% and finally the degraded transistor at t_3 has an average error at 3.4813% and STD of 1.263%. It is also important to

note that the higher error is related to the rare combination of physical effect related to the degradation. The information about the extraction error is summarised in Table 6.4.

Table 6-4: summarised the percentage average error in statistical CM extraction process.

	p-channel transistor				n-channel transistor			
	fresh	t_1	t_2	t_3	fresh	t_1	t_2	t_3
Average	3.194%	3.272%	3.801%	4.093%	2.633%	2.675%	2.963%	3.481%
STD	0.504%	0.543%	0.665%	0.943%	0.867%	0.895%	1.061%	1.263%

After achieving low average error, the accuracy of the extraction process is examined based on the key transistor figures of merit (FoM) including the threshold voltage (V_T), DIBL, OFF current (I_{OFF}), ON current (I_{ON}) and sub-threshold slope (SS). V_T is extracted using a current criterion at $0.16\mu\text{A}$. DIBL is calculated using the definition 6.1 below:

$$DIBL = -\frac{V_T^{DD} - V_T^{low}}{V_{DD} - V_D^{low}} \quad (6.1)$$

V_T^{DD} is the threshold voltage extracted at high drain bias, and V_T^{low} is the threshold voltage extracted at low drain bias, V_{DD} is the supply voltage and V_D^{low} is the low drain bias. I_{OFF} and I_{ON} are the current at $V_G=0\text{V}$ and $V_G=V_{DD}$ respectively. SS is defined by a gate voltage required to change the subthreshold drain current by one order of magnitude.

The degree of difference in the distributions of the FoM and their correlations obtained from the TCAD simulations and from the extracted CM illustrate the accuracy of the extraction process. The distribution of FoM is plotted using scatter plots for both p-channel and n-channel transistors for all degradation levels as illustrated from Figure 6-12 to Figure 6-19 listing also the correlation coefficient. For example for the fresh p-channel transistor, the correlation coefficient between V_T and I_{OFF} is 0.98 and 0.98 for CM and TCAD simulation respectively. Another way of visualising the accuracy is by overlapping the scatter plot distributions of the TCAD and CM FoMs.

Once the extraction process achieves unimodal distribution of the selected parameter set and low extraction error, the CM library is ready for use in the circuit simulation.

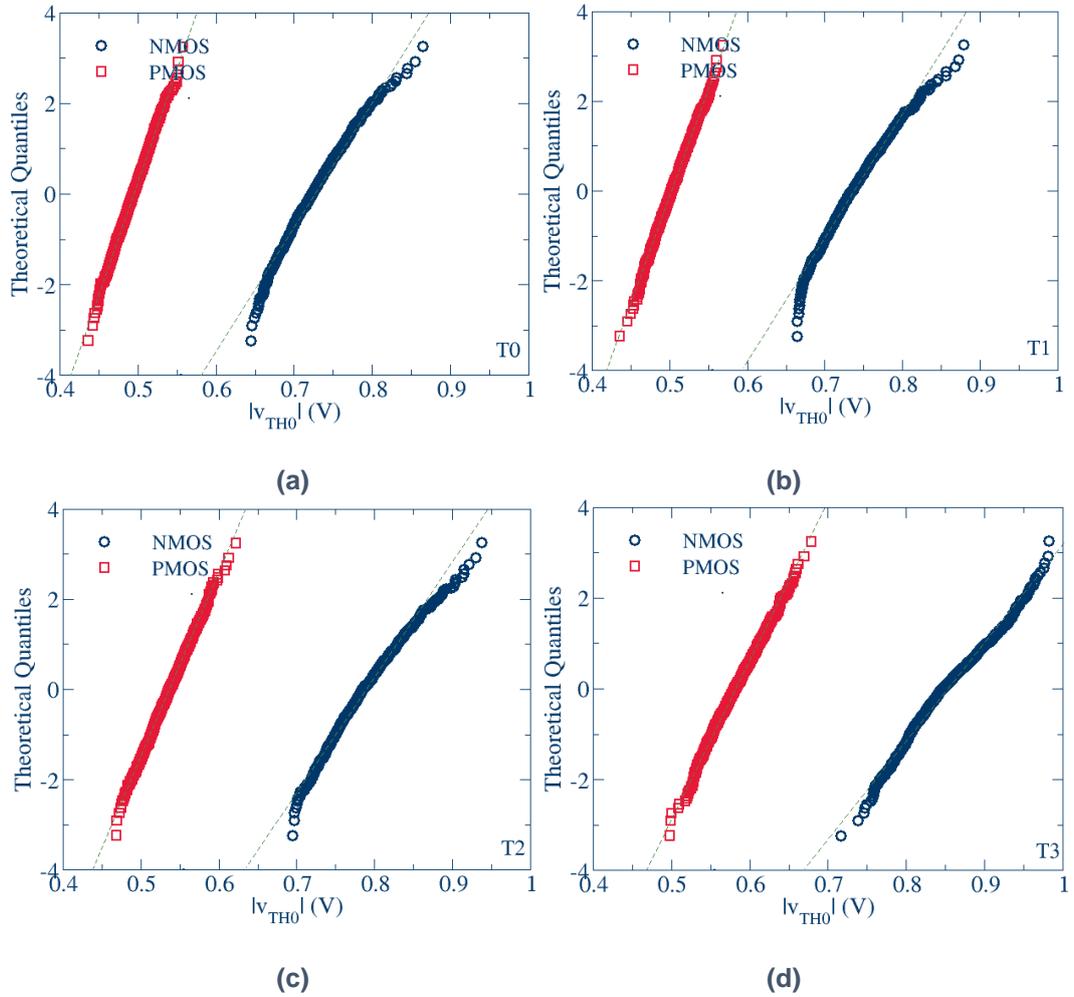
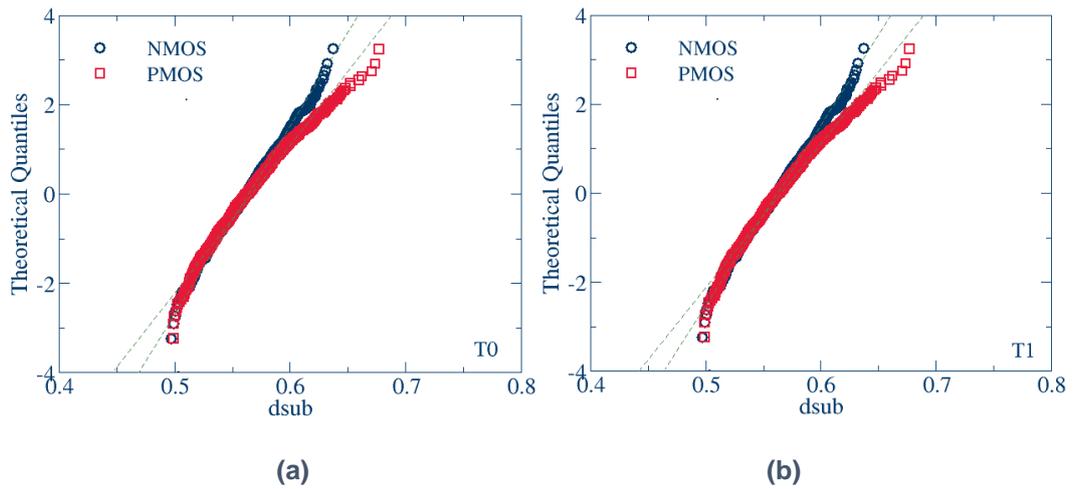


Figure 6-6: Extracted V_{th0} parameter distribution (a) in fresh transistor, and a degraded transistor at (b) $1 \times 10^{11} \text{ cm}^{-2}$ (c) $5 \times 10^{11} \text{ cm}^{-2}$ and (d) $1 \times 10^{12} \text{ cm}^{-2}$.



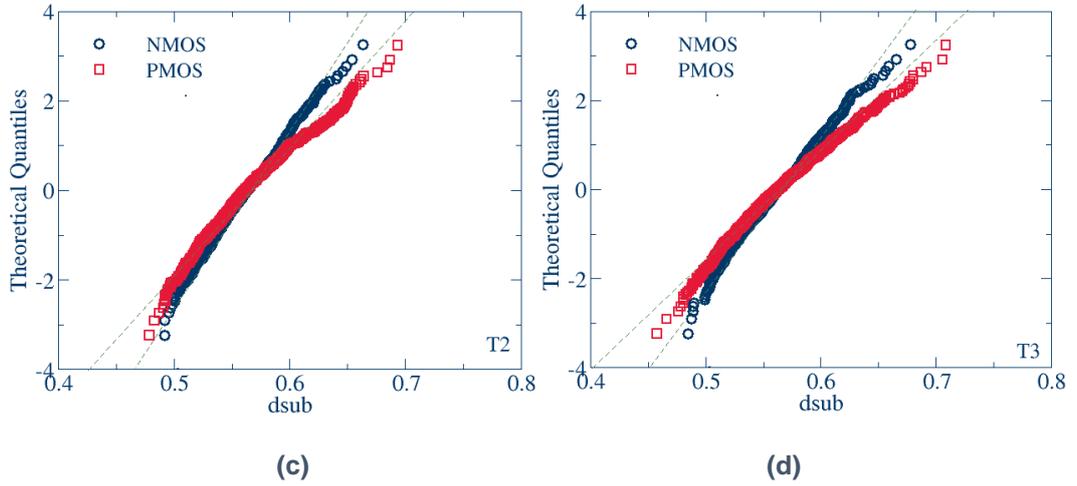


Figure 6-7: Extracted d_{sub} parameter distribution in (a) fresh transistor, and a degraded transistor at (b) $1 \times 10^{11} \text{ cm}^{-2}$ (c) $5 \times 10^{11} \text{ cm}^{-2}$ and (d) $1 \times 10^{12} \text{ cm}^{-2}$.

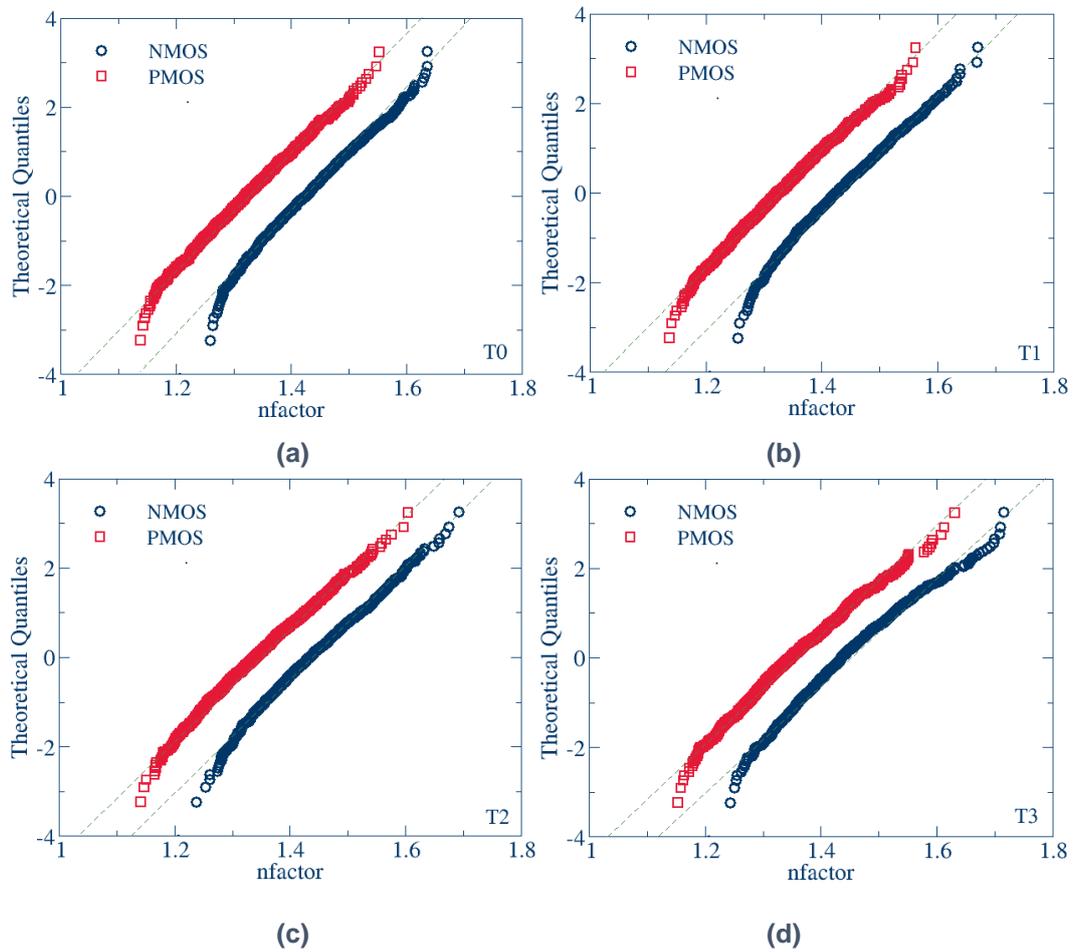


Figure 6-8: Extracted n_{factor} parameter distribution in (a) fresh transistor, and a degraded transistor at (b) $1 \times 10^{11} \text{ cm}^{-2}$ (c) $5 \times 10^{11} \text{ cm}^{-2}$ and (d) $1 \times 10^{12} \text{ cm}^{-2}$.

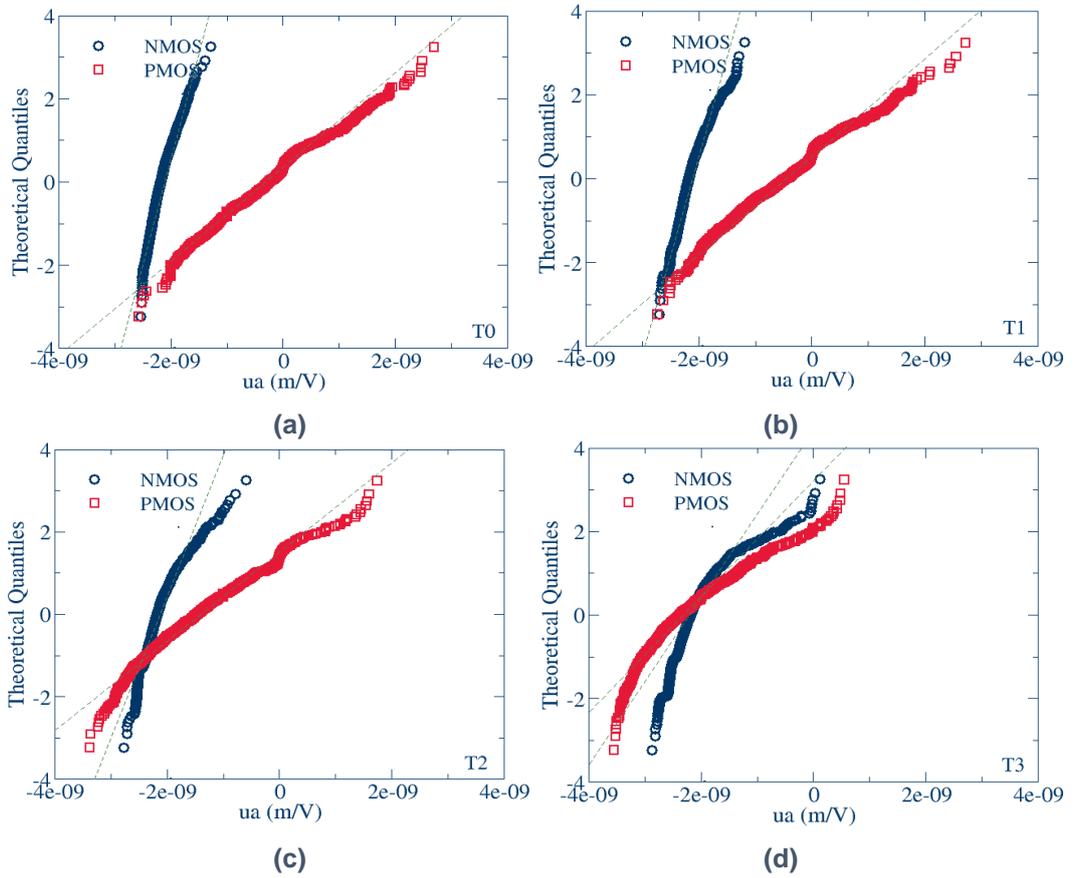


Figure 6-9: Extracted u_a parameter distribution (a) in fresh transistor, and a degraded transistor at (b) $1 \times 10^{11} \text{ cm}^{-2}$ (c) $5 \times 10^{11} \text{ cm}^{-2}$ and (d) $1 \times 10^{12} \text{ cm}^{-2}$.

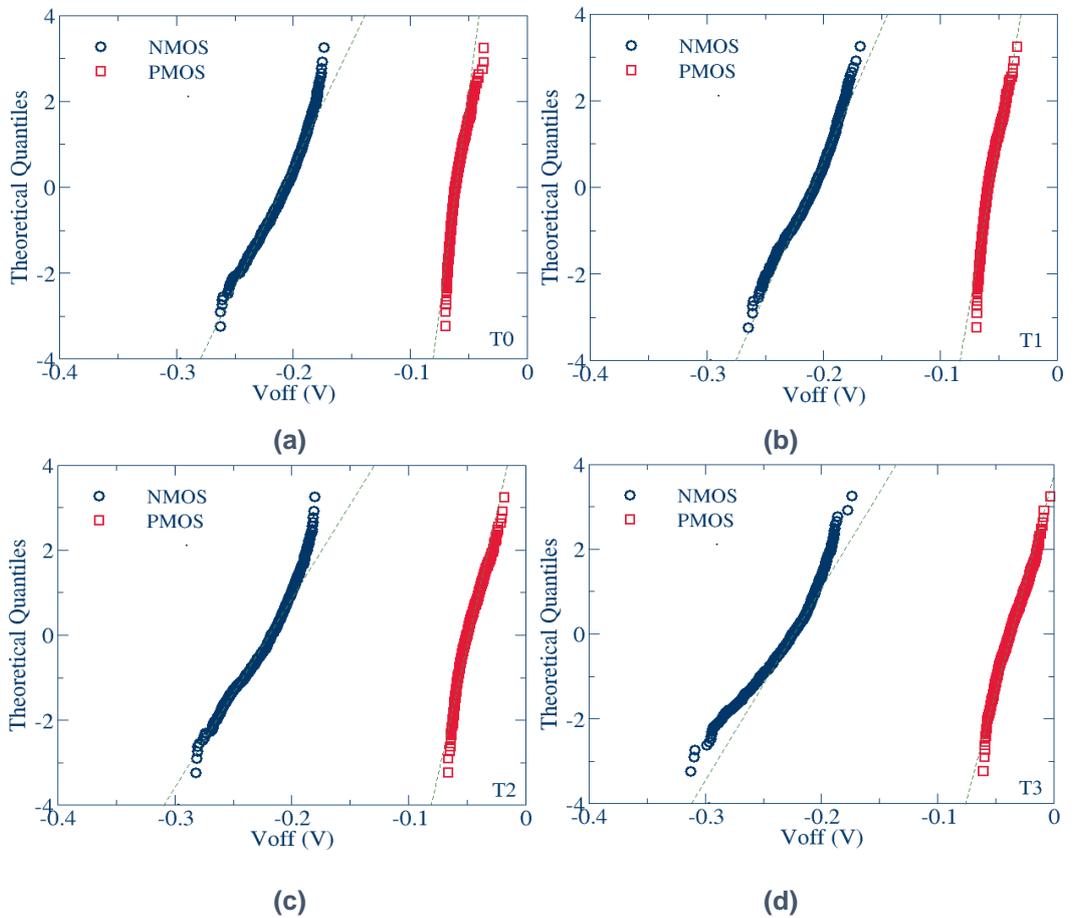


Figure 6-10: Extracted V_{off} parameter distribution (a) in fresh transistor, and a degraded transistor at (b) $1 \times 10^{11} \text{ cm}^{-2}$ (c) $5 \times 10^{11} \text{ cm}^{-2}$ and (d) $1 \times 10^{12} \text{ cm}^{-2}$.

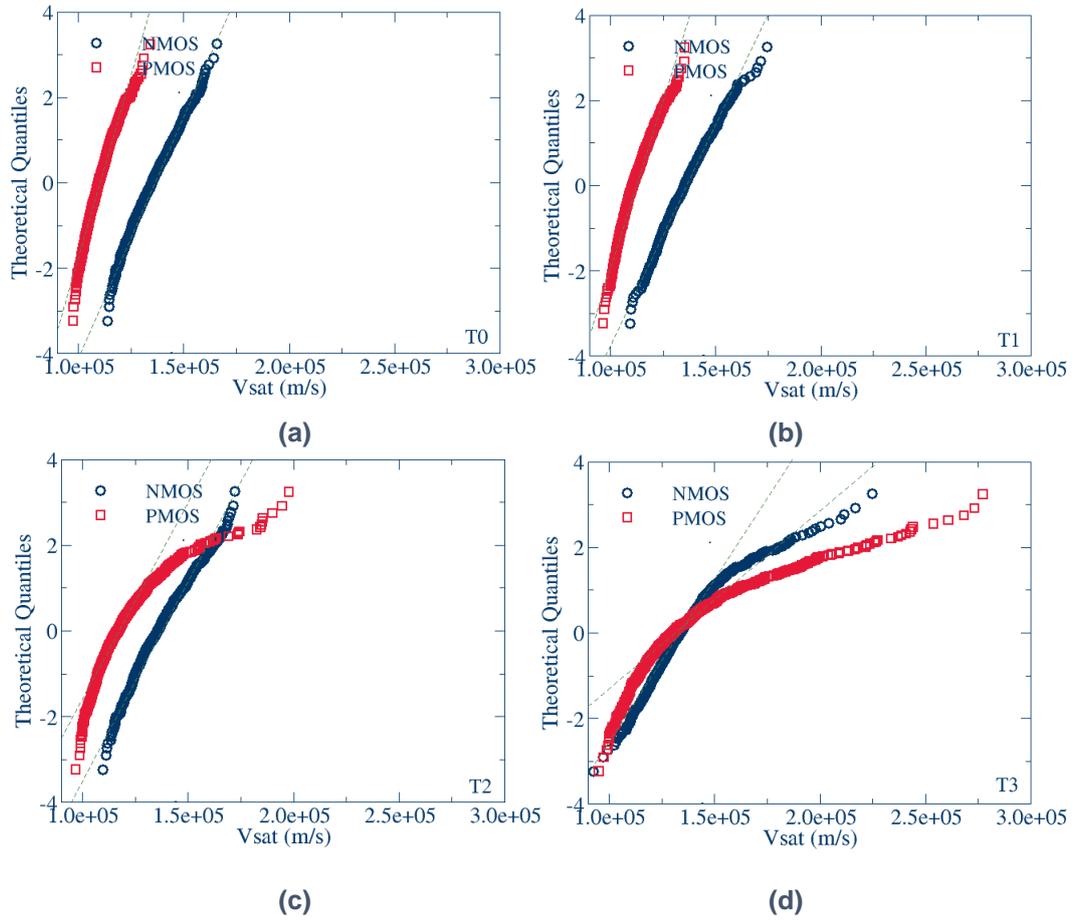


Figure 6-11: Extracted Vsat parameter distribution (a) in fresh transistor, and a degraded transistor at (b) $1 \times 10^{11} \text{ cm}^{-2}$ (c) $5 \times 10^{11} \text{ cm}^{-2}$ and (d) $1 \times 10^{12} \text{ cm}^{-2}$.

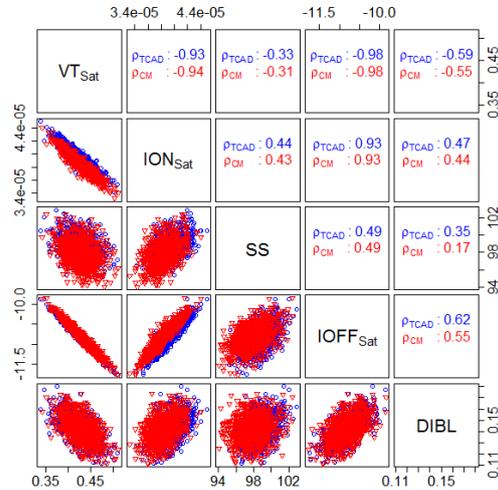


Figure 6-12: Distribution and correlation between TCAD simulation results and extracted CM for a fresh p-channel transistor. Blue colour represents the TCAD simulation results and extracted CM represent by red colour.

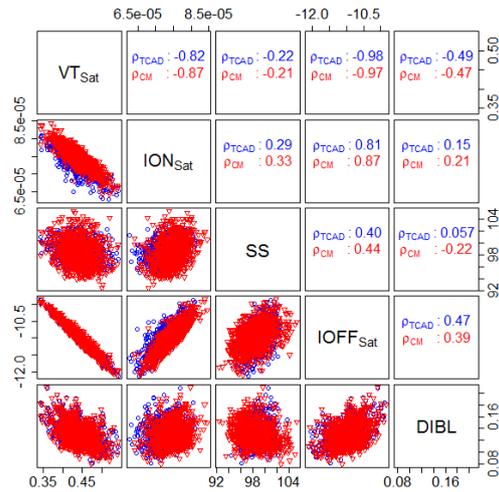


Figure 6-13: Distribution and correlation between TCAD simulation results and extracted CM for a fresh n-channel transistor. Blue colour represents the TCAD simulation results and extracted CM represent by red colour.

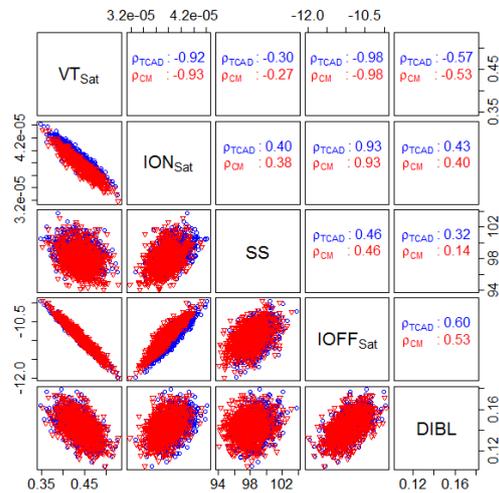


Figure 6-14: Distribution and correlation between TCAD simulation results and extracted CM for a degraded transistor having a trap density at $1 \times 10^{11} \text{ cm}^{-2}$ in p-channel transistor. Blue colour represents the TCAD simulation results and extracted CM represent by red colour.

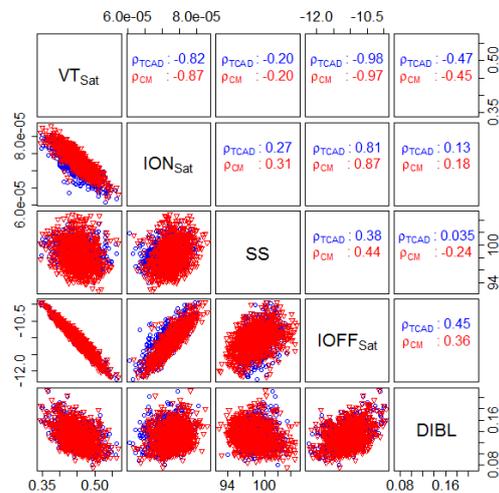


Figure 6-15: Distribution and correlation between TCAD simulation results and extracted CM for a degraded transistor having a trap density at $1 \times 10^{11} \text{ cm}^{-2}$ in n-channel transistor. Blue colour represents the TCAD simulation results and extracted CM represent by red colour.

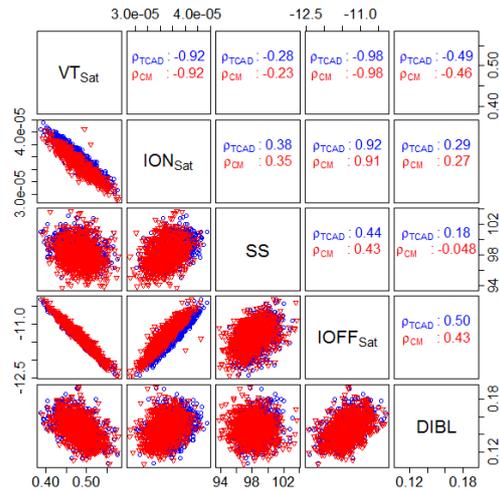


Figure 6-16: Distribution and correlation between TCAD simulation results and extracted CM for a degraded transistor having a trap density at $5 \times 10^{11} \text{ cm}^{-2}$ in p-channel transistor. Blue colour represents the TCAD simulation results and extracted CM represent by red colour.

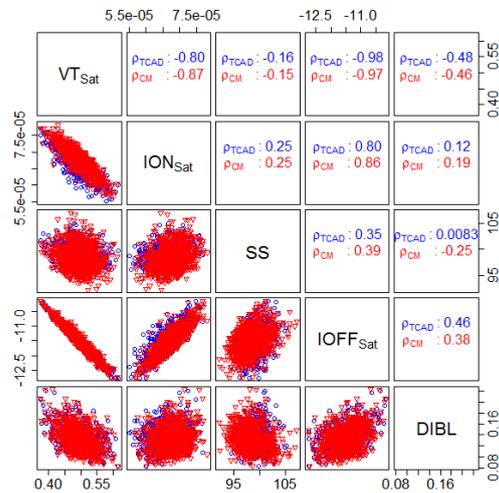


Figure 6-17: Distribution and correlation between TCAD simulation results and extracted CM for a degraded transistor having a trap density at $5 \times 10^{11} \text{ cm}^{-2}$ in n-channel transistor. Blue colour represents the TCAD simulation results and extracted CM represent by red colour.

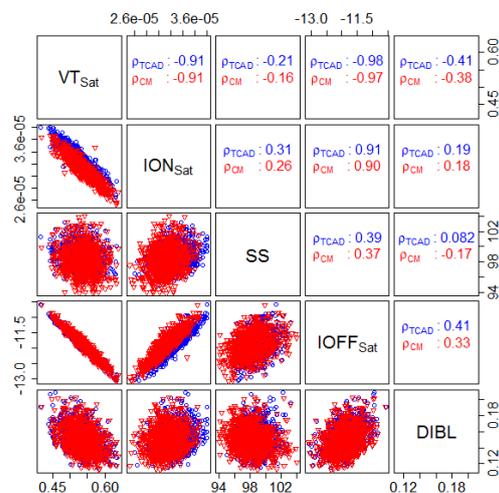


Figure 6-18: Distribution and correlation between TCAD simulation results and extracted CM for a degraded transistor having a trap density at $1 \times 10^{12} \text{ cm}^{-2}$ in p-channel transistor. Blue colour represents the TCAD simulation results and extracted CM represent by red colour.

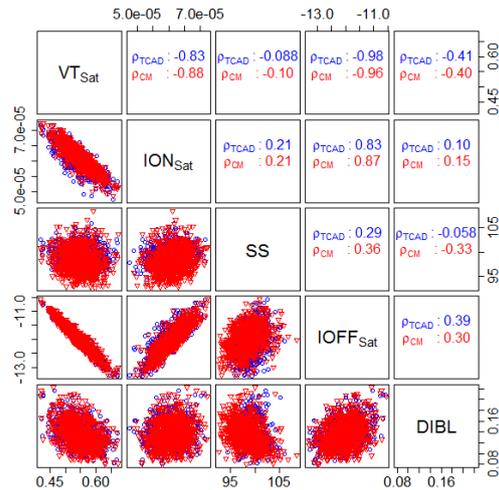


Figure 6-19: Distribution and correlation between TCAD simulation results and extracted CM for a degraded transistor having a trap density at $1 \times 10^{12} \text{ cm}^{-2}$ in n-channel transistor. Blue colour represents the TCAD simulation results and extracted CM represent by red colour.

6.1.2.2 22 nm Intel FinFET

In this section, results from statistical CM extraction for a 22 nm FinFET are presented. The procedure used in the extraction process is similar to that used for the 70 nm imec bulk transistor. The first stage was the full CM extraction, as discussed in 6.1.1.2. As in the case of the bulk transistor, the extraction of the statistical CM was performed on a fresh transistor and degraded transistors with average trap density of $4.6 \times 10^{11} \text{ cm}^{-2}$ and $1.2 \times 10^{12} \text{ cm}^{-2}$. The extraction process is carried out using charge sheet density mentioned above because of the TCAD simulation results presented in Section 5.1 and guided by the Intel experimental data.

As mentioned before, the selection of the parameter set used in the extraction process is very important. There is no universal solution of which parameter should be used in the extraction process. If too many parameters are used, the statistical generation process becomes more complicated. However, when selecting the parameter, it is important that for each segment of IV characteristic (subthreshold region, linear region, saturation region) suitable parameter are selected based on the effect of the physical behavior of the corresponding region. For the purpose of this study, the $CDSC$, $ETA0$, $PHIG$, $U0$ and Ua parameters of BSIM-CMG are used in the extraction process. This is based on several iterations in the extraction process to attain the unimodal distribution of the selected parameters. Table 6.5 summarises the statistical CM parameters.

Table 6-5: selected parameter set used in the extraction process

Parameter	Description
<i>CDSC</i>	Coupling capacitance between S/D and channel
<i>ETA0</i>	DIBL coefficient
<i>PHIG</i>	Work function of gate
<i>U0</i>	Low field mobility
<i>Ua</i>	Mobility coefficient

The statistical distributions of the extracted parameters are presented in the form of a QQ-plot as shown from Figure 6-20 to Figure 6-24. The *CDSC* and *ETA0* parameters in Figure 6-20 and Figure 6-21 exhibit minor skew in the distribution, while the *PHIG* parameter in Figure 6-22 is close to a Gaussian distribution. And for *U0* and *Ua* parameters shown in Figure 6-23 and Figure 6-24, have a significant kurtosis. However, the distribution in all selected parameter sets is still fulfilled the Mystic requirement where the distribution of parameter needs to be unimodal distribution.

In addition to fulfilling the unimodal requirement, the average percentage error of the extraction process is also important in determining the accuracy of the variability behaviour of each transistor. For the p-channel, the fresh transistor the average error is 4.337% with a STD of 1.343%, a degraded transistor at t_1 has an average error of 4.676% with a STD of 1.369% and finally a degraded transistor at t_2 has an average error of 5.089% with a STD of 1.736%. For an n-channel transistor, the fresh transistor has an average of 3.623% with a STD of 1.329%, a degraded transistor at t_1 has an average error of 3.950% with a STD of 1.503% and finally a degraded transistor at t_2 has an average error of 4.393% with a STD of 1.716%. It is also important to note that the higher error is related to the rare combination of physical effects. Error percentages are summarised in Table 6.6.

Table 6-6: Summarised the percentage average error in statistical CM extraction process.

	p-channel transistor			n-channel transistor		
	fresh	t_1	t_2	fresh	t_1	t_2
Average	4.337%	4.676%	5.089%	3.623%	3.950%	4.393%
STD	1.343%	1.369%	1.736%	1.329%	1.503%	1.716%

The degree of average error in the extraction process indicates the level of accuracy in preserving the variability. The accuracy of the extraction process is also examined in terms the distributions and the correlations of important transistor figures of merit (FOM)s. The distributions of these important FOMs are presented in a correlation matrix using scatter

plots and correlation coefficient of both p-channel and n-channel transistors in all degradation levels in Figure 6-25 to Figure 6-30. The correctness of preserving the variability in each transistor can be easily visualized using a scatter plot of each selected parameter distribution. The overlapped scatter plot of selected parameter distributions for CM simulation and TCAD simulation shows that the CM library has successfully captured the TCAD simulated variability for this transistor. The correlation coefficient between each two FOM are also very close. For example, in Figure 6-25, the correlation coefficient for V_{Tsat} and I_{OFFsat} is 0.92 for both CM and TCAD.

Once the extraction process fulfills the unimodal distribution of the selected parameter set and has acceptable error, the CM library is ready for used in the circuit simulation.

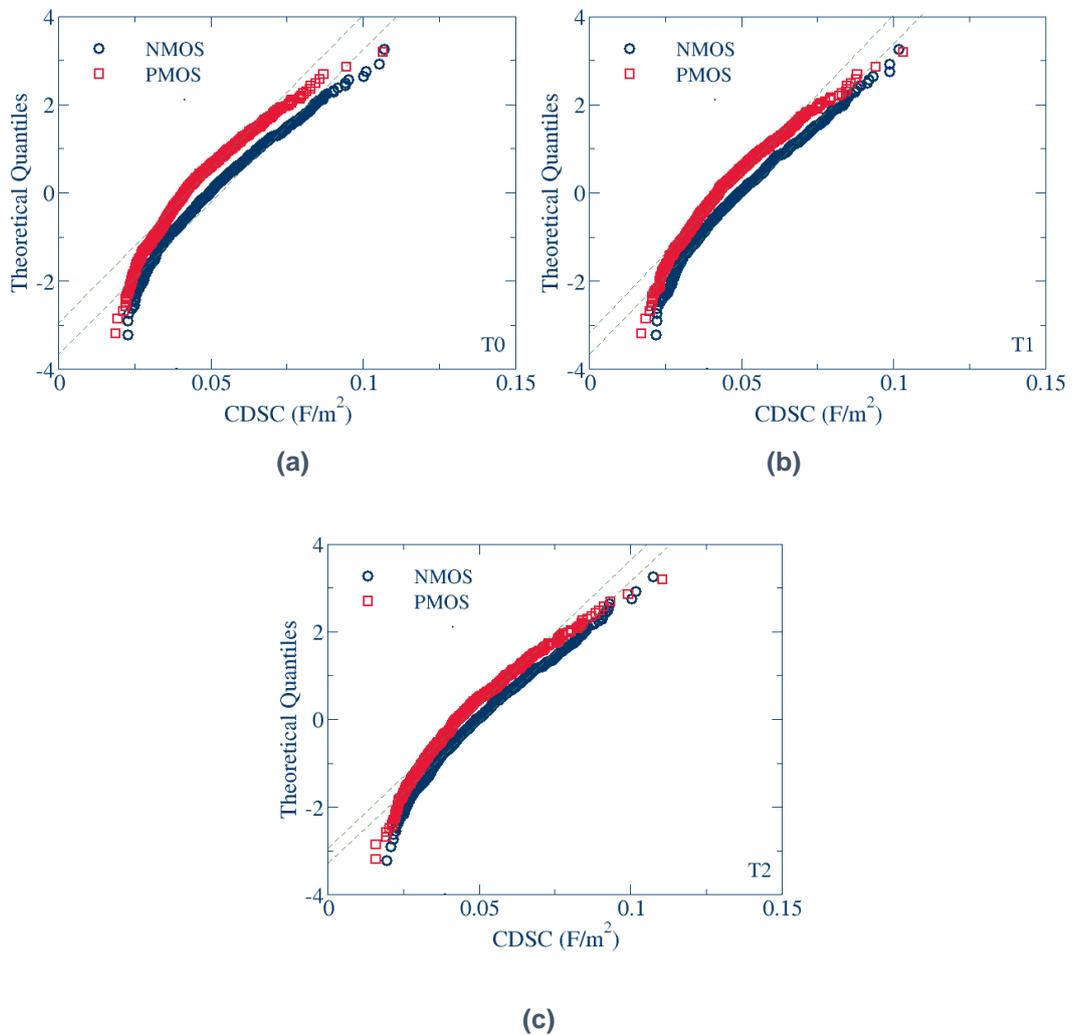


Figure 6-20: Extracted CDSC parameter distribution in (a) fresh transistor, and a degraded transistor at (b) $4.6 \times 10^{11} \text{ cm}^{-2}$ and (c) $1.2 \times 10^{12} \text{ cm}^{-2}$.

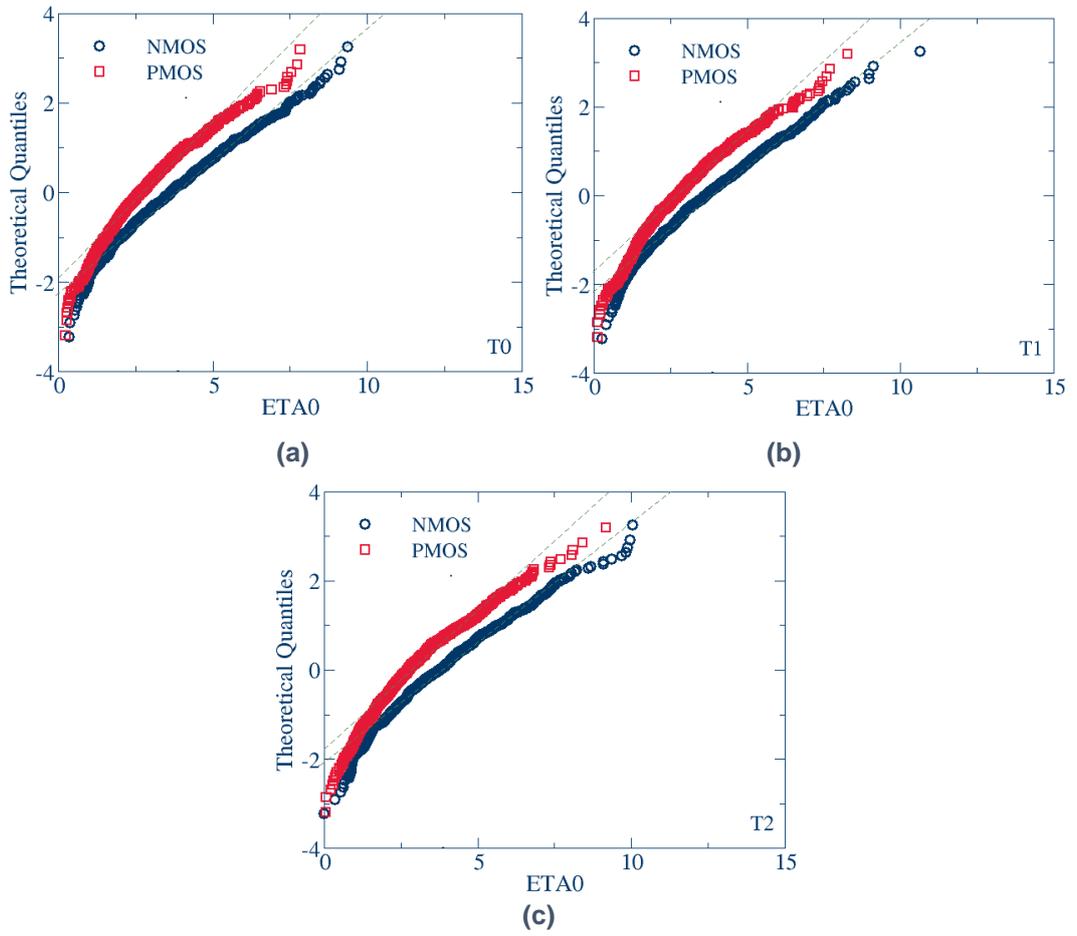


Figure 6-21: Extracted ETA_0 parameter distribution in (a) fresh transistor, and a degraded transistor at (b) $4.6 \times 10^{11} \text{ cm}^{-2}$ and (c) $1.2 \times 10^{12} \text{ cm}^{-2}$.

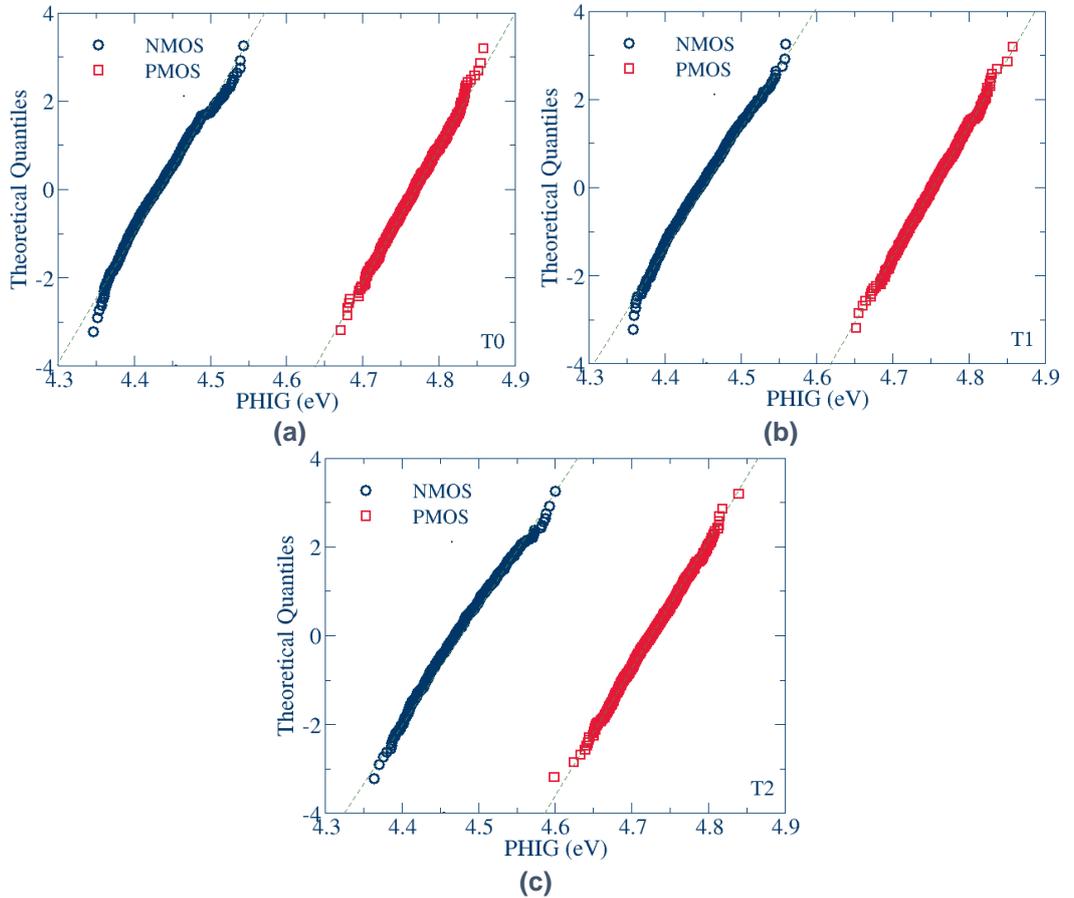


Figure 6-22: Extracted PHIG parameter distribution in (a) fresh transistor, and a degraded transistor at (b) $4.6 \times 10^{11} \text{ cm}^{-2}$ and (c) $1.2 \times 10^{12} \text{ cm}^{-2}$.

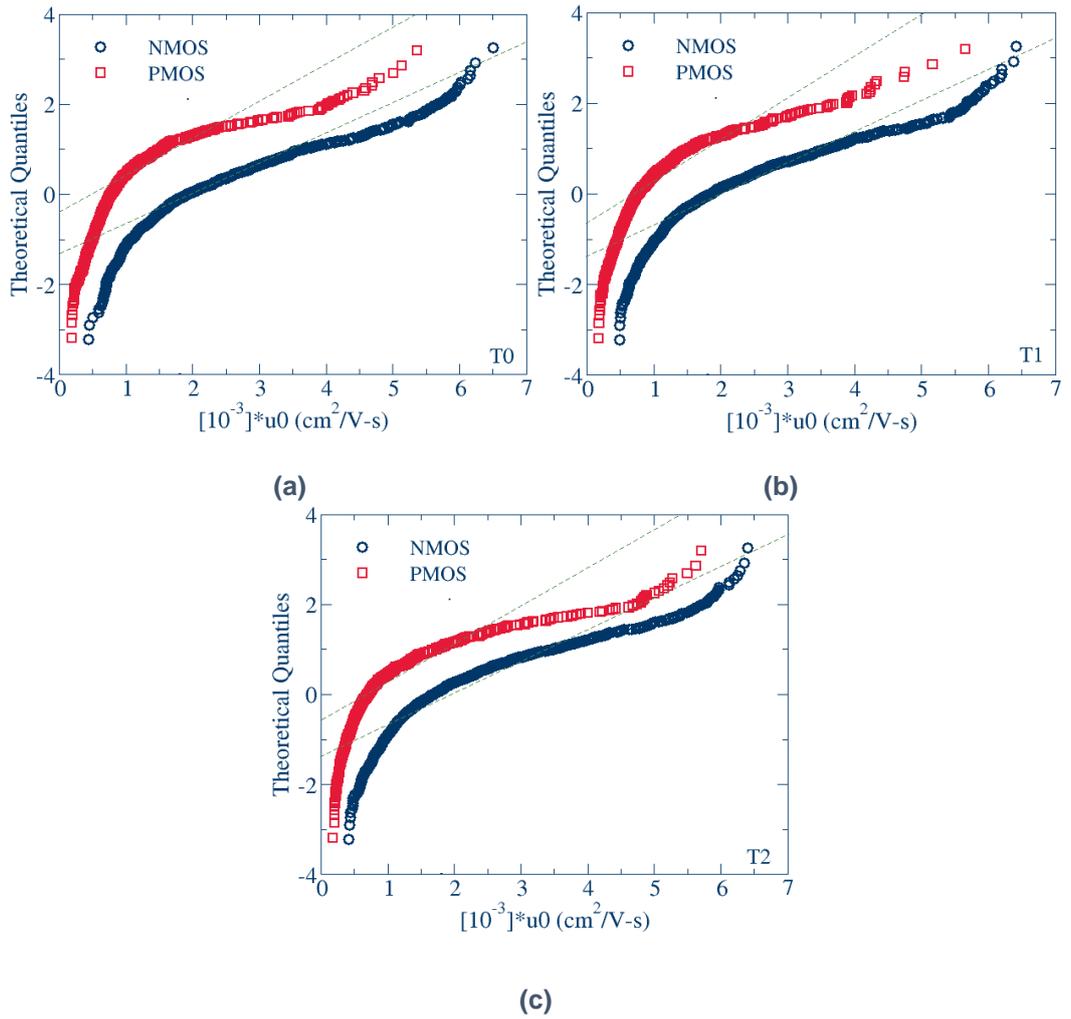
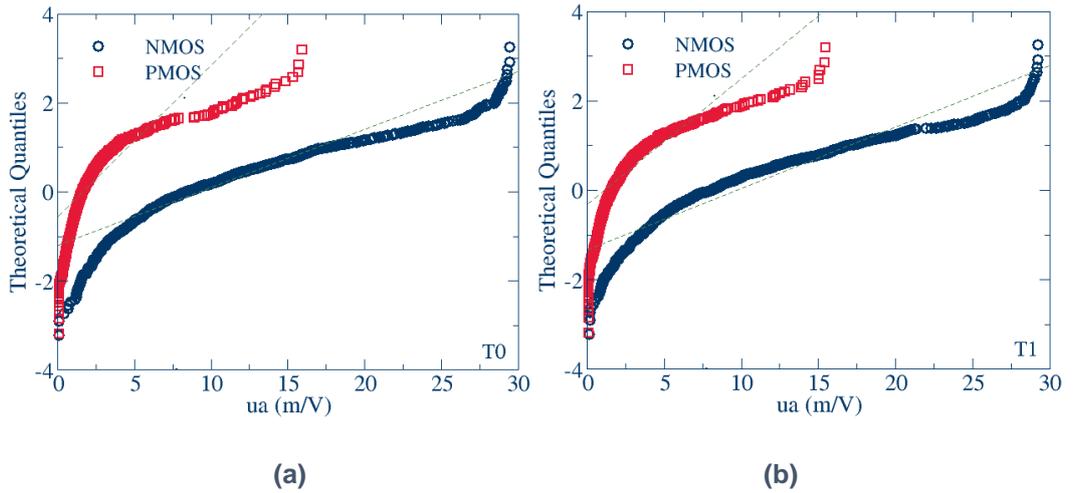
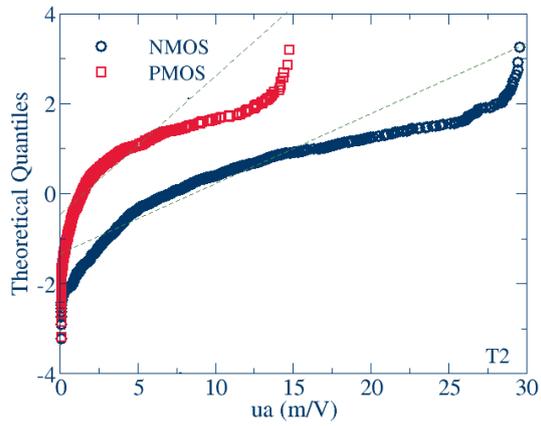


Figure 6-23: Extracted U0 parameter distribution in (a) fresh transistor, and a degraded transistor at (b) $4.6 \times 10^{11} \text{ cm}^{-2}$ and (c) $1.2 \times 10^{12} \text{ cm}^{-2}$.





(c)

Figure 6-24: Extracted U_a parameter distribution in (a) fresh transistor, and a degraded transistor at (b) $4.6 \times 10^{11} \text{ cm}^{-2}$ and (c) $1.2 \times 10^{12} \text{ cm}^{-2}$.

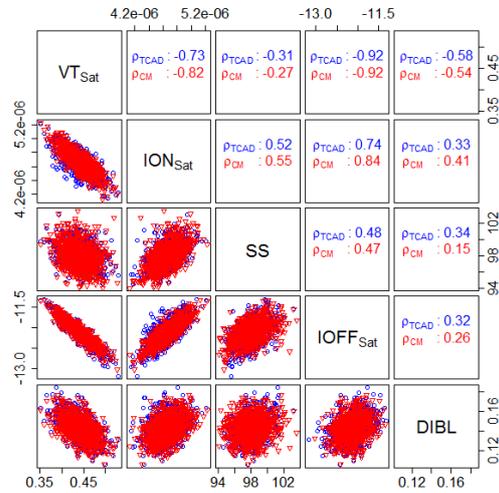


Figure 6-25: Distribution and correlation between TCAD simulation results and extracted CM for a fresh p-channel transistor. Blue colour represents the TCAD simulation results and extracted CM represent by red colour.

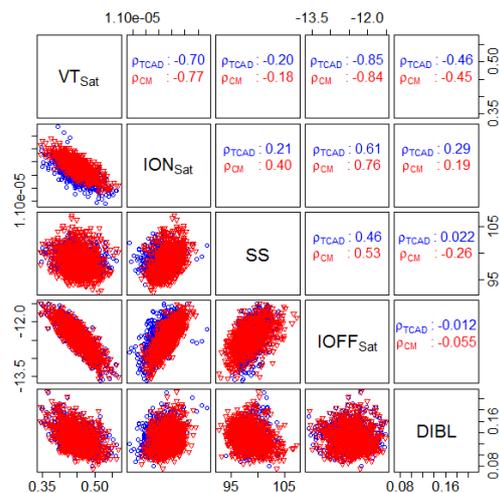


Figure 6-26: Distribution and correlation between TCAD simulation results and extracted CM for a fresh n-channel transistor. Blue colour represents the TCAD simulation results and extracted CM represent by red colour.

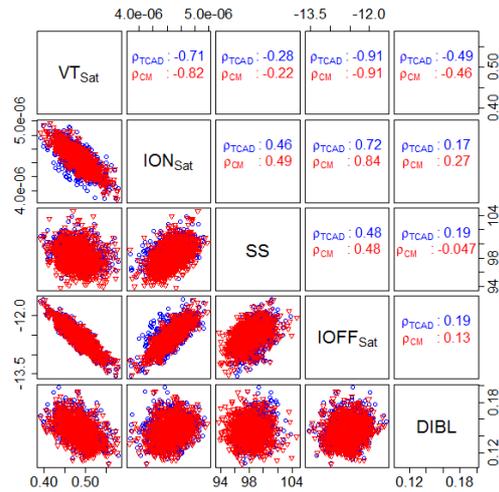


Figure 6-27: Distribution and correlation between TCAD simulation results and extracted CM for a degraded transistor having a trap density at $4.6 \times 10^{11} \text{ cm}^{-2}$ in p-channel transistor. Blue colour represents the TCAD simulation results and extracted CM represent by red colour.

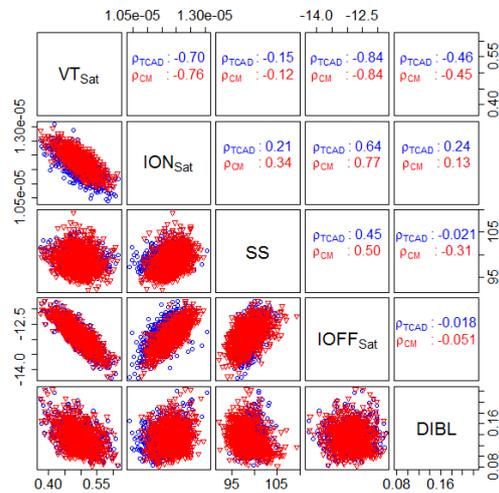


Figure 6-28: Distribution and correlation between TCAD simulation results and extracted CM for a degraded transistor having a trap density at $4.6 \times 10^{11} \text{ cm}^{-2}$ in n-channel transistor. Blue colour represents the TCAD simulation results and extracted CM represent by red colour.

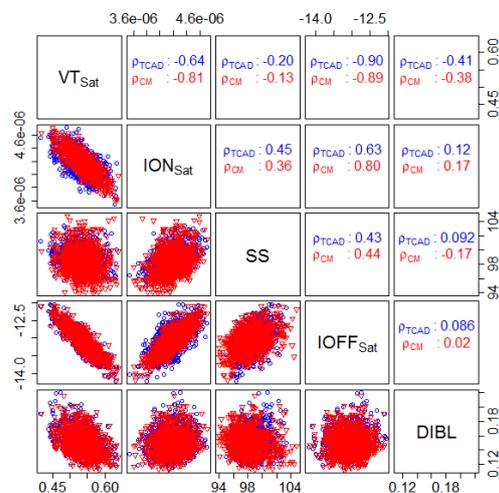


Figure 6-29: Distribution and correlation between TCAD simulation results and extracted CM for a degraded transistor having a trap density at $1.2 \times 10^{12} \text{ cm}^{-2}$ in p-channel transistor. Blue colour represents the TCAD simulation results and extracted CM represent by red colour.

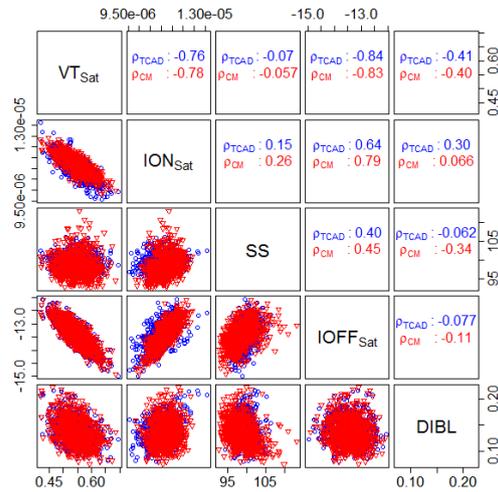


Figure 6-30: Distribution and correlation between TCAD simulation results and extracted CM for a degraded transistor having a trap density at $1.2 \times 10^{12} \text{ cm}^{-2}$ in n-channel transistor. Blue colour represents the TCAD simulation results and extracted CM represent by red colour.

6.2 6T-SRAM cell ageing

In this section, the generated CM libraries will be used in circuit level simulation. The degradation behaviour of a 6T-SRAM, based on both 70 nm bulk IMEC MOSFET and 22 nm FinFET has been studied. The schematic of the 6T-SRAM is illustrated in Figure 6-31. It consists of two inverter pairs, in a feedback configuration. The 6T-SRAM holds ‘data’ inside due to the feedback between input signal from one inverter and the output of the other. A part of these two pairs of transistors, the 6T-SRAM contains Pass Gate (PG) transistors, which are controlled by a Word Line (WL), with sources connected to the Bit line (BL).

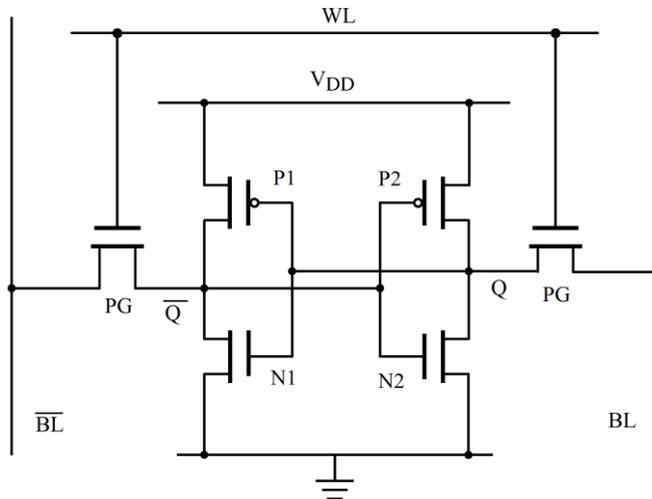


Figure 6-31: 6T-SRAM circuit used in this study.

The pull-up (PU) transistors in the inverted part are often p-channel transistors (P1 and P2), whereas pull-down (PD) transistors are n-channel transistors (N1 and N2). Since the extraction of CM is based on a L/W ratio of one for both transistors, the 6T-SRAM is configured as 1:1:1 for PU: PD: PG which have 70 nm width in the case of the bulk imec MOSFET and single fin for the Intel FinFET.

Several scenarios have been identified to investigate the 6T-SRAM performances under degradation. These scenarios are summarised in Table 6.7. They are based on the operation of the 6T-SRAM itself, the storing, writing and reading of information inside the 6T-SRAM. Scenario A is related to the operation of 6T-SRAM holding information. In this case, the 6T-SRAM is assumed to perform a hold '0' for a long period. In order to perform this operation, the gates of the N1 and P2 transistors are set to high (V_{DD}) or in other words having a BTI stress condition. The long period of degradation in this case means the total degradation has both permanent and recoverable components since the stress for this transistor is never released.

In Scenario B, the 6T-SRAM is assumed to operate in fast reading and writing modes. In this case, the N1 and P2 transistors are alternately frequently and alternately stressed with the N2 and P1 transistors respectively. This means that both N1, N2, P1 and P2 are under a BTI stress condition. The terms of fast operation mean that 6T-SRAM operates at higher frequency compared to the degradation recovery times. As a result, the total degradation in these transistors is based on permanent and recoverable degradation since the stress for this transistor increases with time. Finally, in Scenario C, the 6T-SRAM operates based on Scenario B, but this time the degradation in the PG transistor is taken into account as well.

Table 6-7: Scenario used in to investigate the 6T-SRAM performances

Scenario	A	B	C
Degraded transistor			
N1	X	X	X
P1	-	X	X
N2	-	X	X
P2	X	X	X
PG	-	-	X

In different CMOS technologies, the p-channel and n-channel transistors are degraded at a different rate as reported in (Kerber & Cartier, 2009). In the poly-silicon gate technology, the degradation in the p-channel transistor, which is affected by NBTI, is triggered earlier compared to the n-channel transistor under PBTI. This is because both of these transistors

have a different charge injection mechanism for the trapped charge. Based on (Kerber & Cartier, 2009), the PBTI degradation is considered to be a factor of three less than NBTI degradation. To reflect these differences, in this study, degradation level ratios between p-channel and n-channel transistors are considered. In Type 1, trapped charge density in the p-channel transistor is equal to the trapped charge density in the n-channel transistor. In Type 2, trapped charge density in the p-channel transistor is to be half of the of the trapped charge density in the n-channel transistor. Finally in Type 3, the trapped charge density in the p-channel transistor is only a quarter compared trapped charge density in the n-channel transistor. However, in Scenario C when the 6T-SRAM operates in fast reading and writing mode, with the PG transistors will also suffer from BTI stress degradation. Therefore, the ratio of degradation level is slightly modified and another two more degradation ratios have been introduced. In Type 4, the degradation level of the PG transistor is at half of the trapped charge density in the inverter pairs. Finally in Type 5, the degradation level of the PG transistors is half for the n-channel degradation and a quarter for the p-channel degradation. Table 6.8 summarises all simulation scenarios used to investigate the 6T-SRAM performances under degradation.

Table 6-8: Complete simulation setup with a degradation level ratio.

Scenario A	Scenario B	Scenario C
$N_{T_NMOS} = N_{T_PMOS}$	$N_{T_NMOS} = N_{T_PMOS}$	$N_{T_NMOS} = N_{T_PMOS}$
$N_{T_NMOS} = \frac{1}{2}N_{T_PMOS}$	$N_{T_NMOS} = \frac{1}{2}N_{T_PMOS}$	$N_{T_NMOS} = \frac{1}{2}N_{T_PMOS}$
$N_{T_NMOS} = \frac{1}{4}N_{T_PMOS}$	$N_{T_NMOS} = \frac{1}{4}N_{T_PMOS}$	$N_{T_NMOS} = \frac{1}{4}N_{T_PMOS}$
Additional scenario focused on a realistic degradation in SRAM circuit		$PG = \frac{1}{2}N_{T_NMOS} = \frac{1}{2}N_{T_PMOS}$
		$PG = \frac{1}{2}N_{T_NMOS} = \frac{1}{4}N_{T_PMOS}$

SNM can be defined as the maximum input voltage that can be tolerated during the read operation without changing data inside the cell (Seevinck, List, & Lohstroh, 1987) as illustrated in Figure 6.32 for one atomistically different transistor. The SNM can be measured by applying a sweep signal at the SL (or SR) node and measuring the output at the opposite node. This procedure is repeated with the other node to obtain two sets of simulations. The IV characteristic for both results is plotted as in Figure 6-32. A largest square box is fitted in the eye of each butterfly curve and based on these the SNM is defined the diagonal of the larger square. Since the 6T-SRAM has 1:1:1 ratio, it is not optimally sized in terms of the SNM of the uniform transistors without variability.

Figure 6-33 (b) illustrates the butterfly curves degraded transistors in Scenario A compared to fresh transistor illustrated in Figure 6-33 (a). In Scenario A, only N1 and P2 are degraded. Thus, the imbalance between both pairs of inverters increases the unsymmetrical of the butterfly curve. This is because for the inverter consisting of N1 and P1, it is easier to charge output \bar{Q} while for the inverter consisting of N2 and P2 it is easier to discharge the output Q. While in Scenario B, both pairs of transistors are equally degraded, and as a result the asymmetry of the butterfly curve is smaller as shown in Figure 6.33 (c). Finally, in Scenario C, the influence of PG degradation is taken into account. Due to the trade-off between V_T shift and driveability ratio in PG and PD transistors this leads to an imbalance in the butterfly curve as illustrated in Figure 6.33 (d).

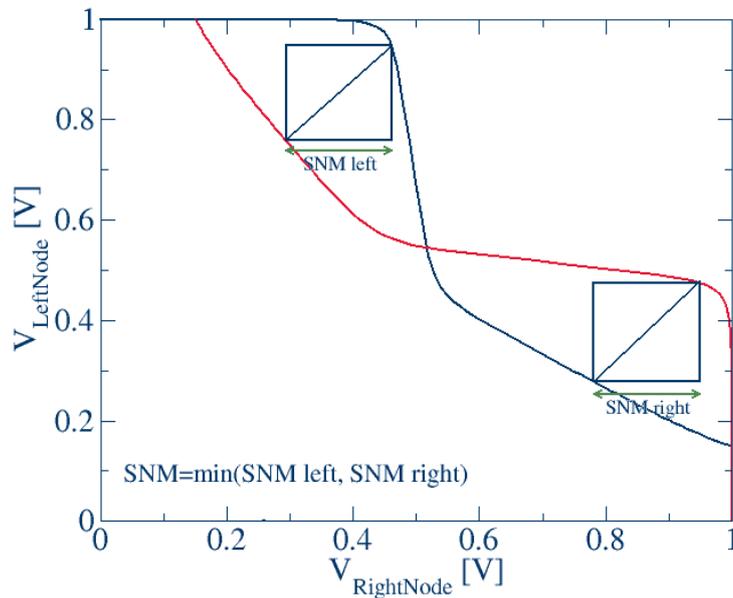
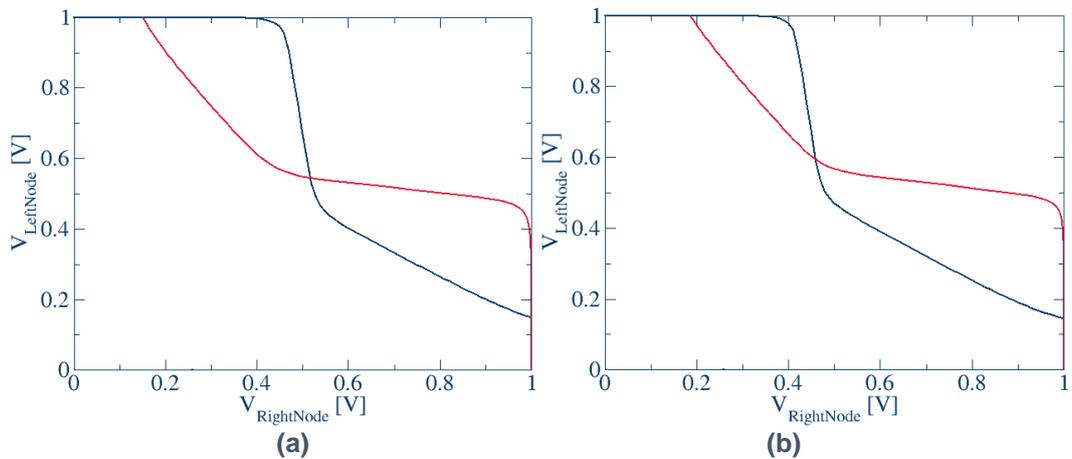


Figure 6-32: Definition of SNM based on the simulated at node Q and \bar{Q} .



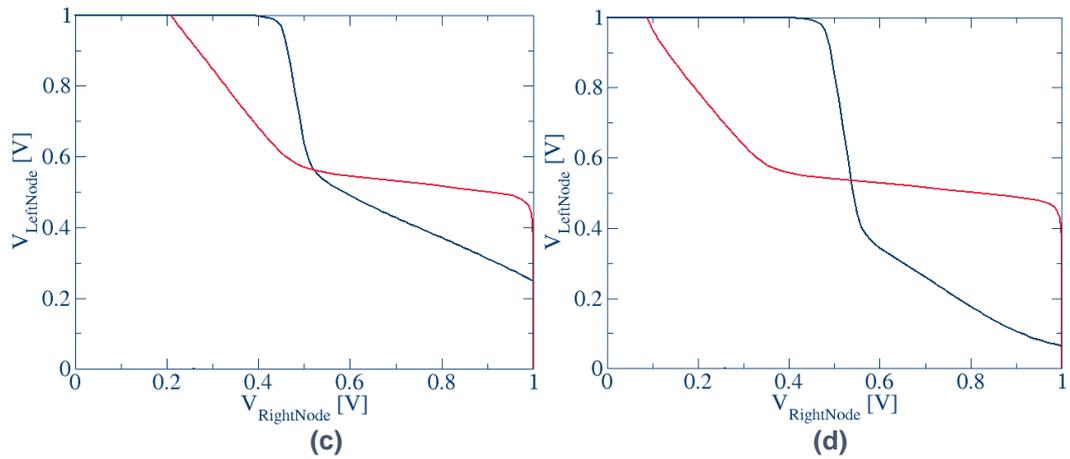


Figure 6-33: Simulation result of butterfly curve for a) fresh transistor, b) Scenario A, c) Scenario B and d) Scenario C.

According to the analytical expression for SNM summarised in (Pavlov & Sachdev, 2008) the SNM performance depends on V_{DD} , V_T and cell ratio. Since this section is mainly focused on investigating the degradation in 6T-SRAM with a fixed cell ratio and at fixed drain bias, the V_T shift induced by the ageing process is considered as a major factor that affects the SNM performance. In the next section, the results of SNM degradation for both 70 nm bulk imec MOSFET and 22 nm FinFET are presented.

6.2.1 70 nm bulk imec MOSFET

Simulation results for 70 nm bulk imec MOSFET are presented in this section. In order to evaluate the 6T-SRAM performance the circuit has been simulated based on the scenarios described in Section 6.2. The degradation ratio in this circuit is taken into account due to the different impact of ageing between the p-channel and the n-channel transistors.

Scenario A is evaluated based on the hold phase operation. During this operation, only transistor N1 and P2 have been subject to degradation. Due to the unbalanced degradation in the SRAM cell, the left eye of the butterfly curve is closing faster than the right eye. As a result, the lower tail of the distribution is more affected in comparison to the upper tail as shown in Figure 6-34. The ageing process in the transistor subject to BTI leads to a V_T shift, which has a direct impact on the mean of the SNM with the mean of the distribution decreasing relative to the fresh cell.

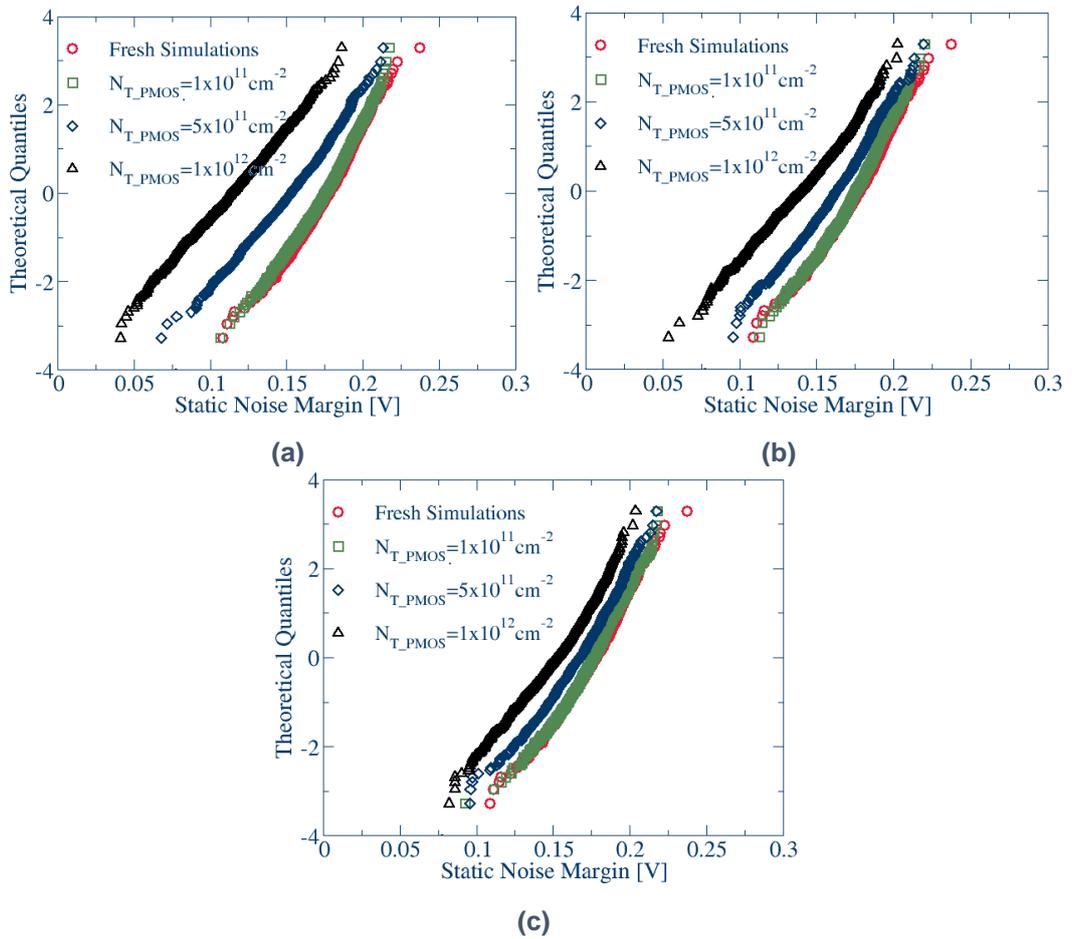
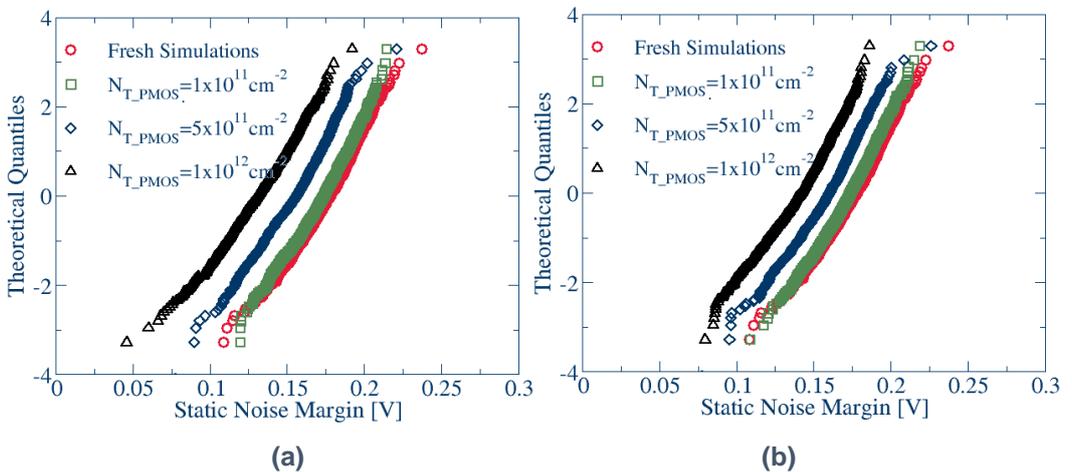


Figure 6-34: QQ-plot for snm distribution in Scenario A with a) Type 1 simulation, b) Type 2 simulation and c) Type 3 simulation.

In Scenario B, both pairs of inverter transistors are equally degraded. In this scenario the output signals from Q and \bar{Q} are balanced and the resulting butterfly eye remains symmetrical. The V_T shift due to the ageing process shifts the SNM distributions to the rigid distribution. Based on Figure 6-35, the degraded SNM distribution has a smaller dispersion together with the right shift.



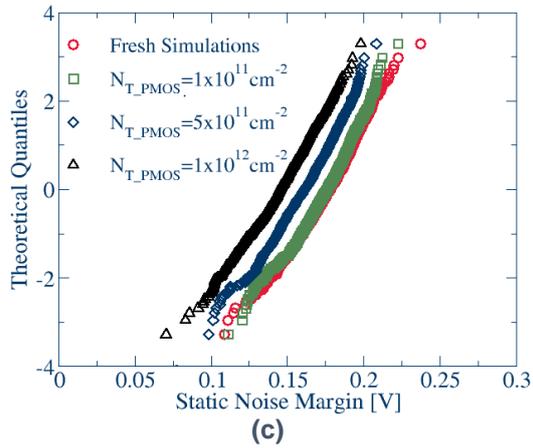
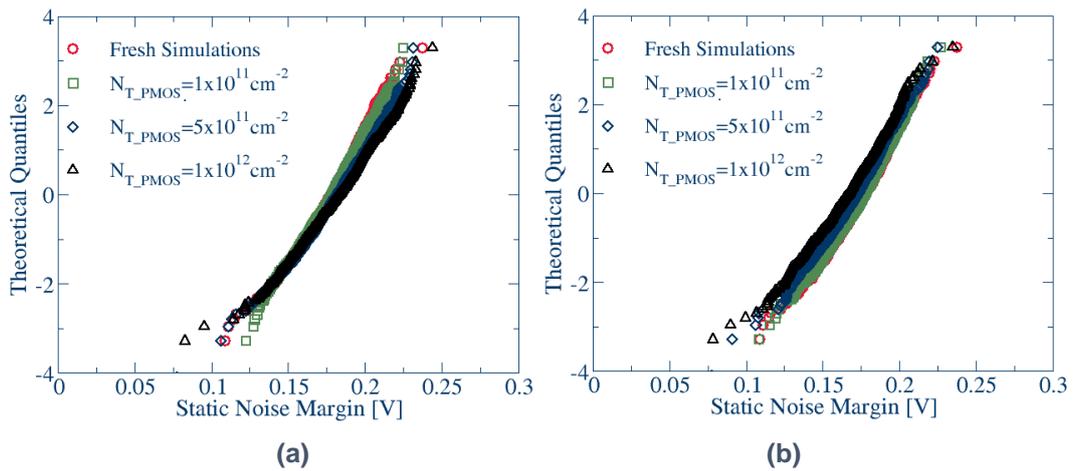


Figure 6-35: QQ-plot for snm distribution in Scenario B with a) Type 1 simulation, b) Type 2 simulation and c) Type 3 simulation.

Finally, in Scenario C, the influence of the PG transistor in the case of fast read and write operation is taken into account. As observed in Scenario B, the uniform degradation of the inverter transistors leads to a decrease in SNM dispersion. However, if the PG degradation is taken into account, the SNM dispersion no longer decreases with the degradation. For example, in Type 1 case, where all transistors have similar degradation, the mean SNM and STD SNM increase compared with the fresh transistor case. This is because of the trade-off impact between the V_T shifts and the driveability in the cell affected by the relative degradation of the PG and PD transistors. Figure 6-36 illustrates the SNM distribution in Scenario C.



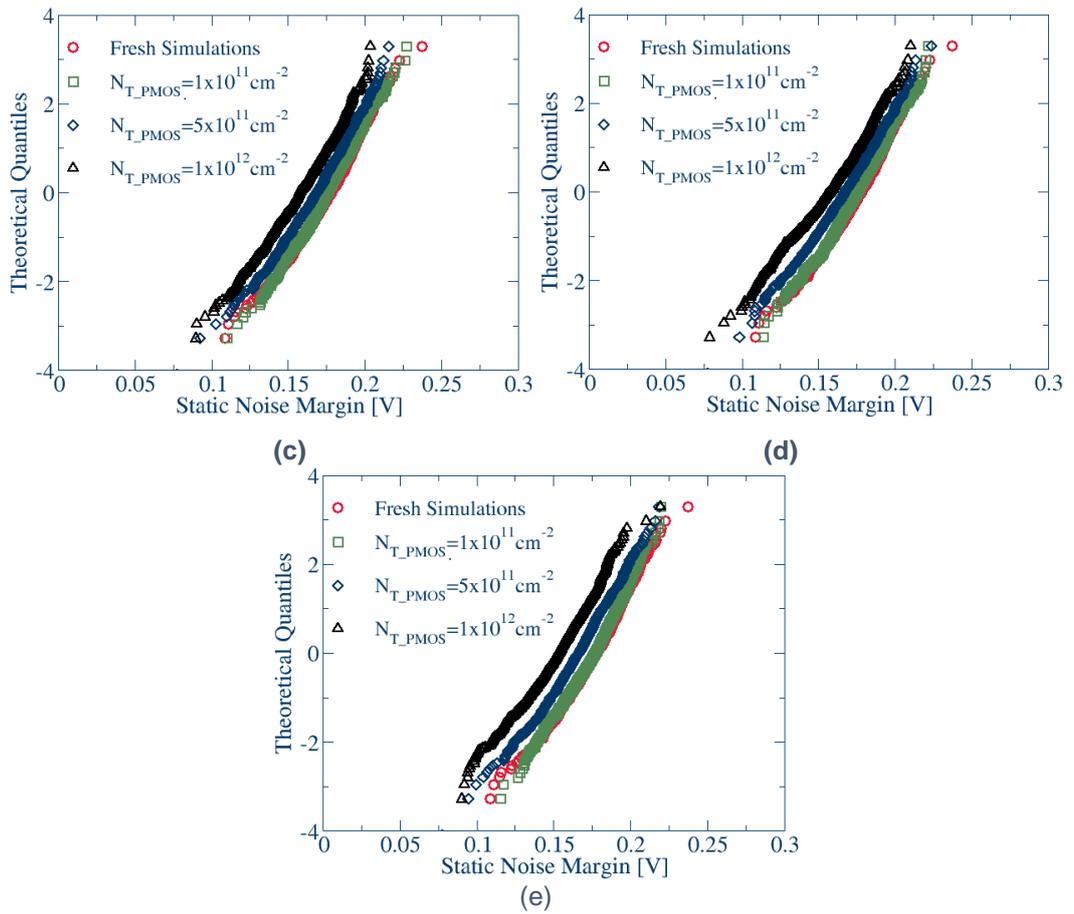


Figure 6-36: QQ-plot for SNM distribution in Scenario C with a) Type 1 simulation, b) Type 2 simulation c) Type 3 simulation d) Type 4 simulation and e) Type 5 simulation.

Figure 6-37 summarises the trends in standard deviation of the SNM distribution for each scenario. It shows that the dispersion of SNM increases as transistor degradation levels increase. Figure 6-38 shows that the general trend is that the mean of SNM distribution reduces with the increase in transistor degradation. However, in Scenario C where all transistors have similar degradation conditions, the mean of SNM distribution can also increase compared to the fresh transistor. This shows that the cell stability improves in certain degradation conditions.

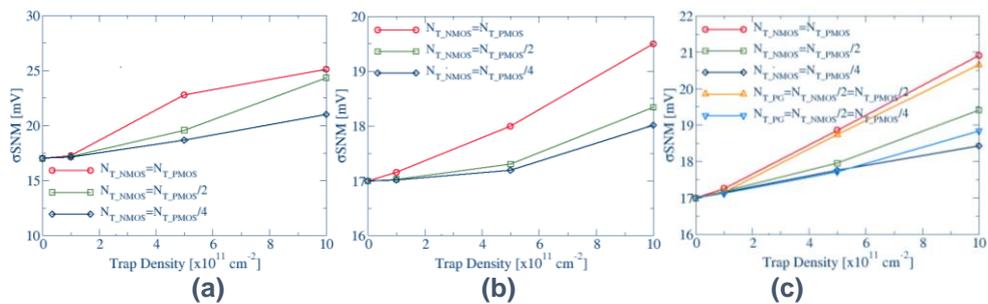


Figure 6-37: standard deviation of SNM distribution in (a) Scenario A, (b) Scenario B and (c) Scenario C.

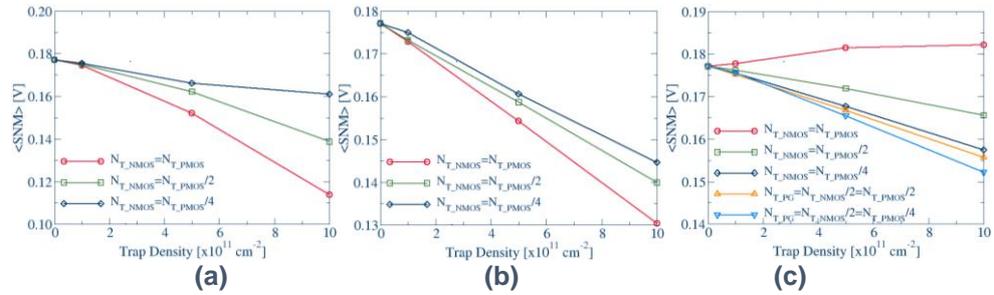
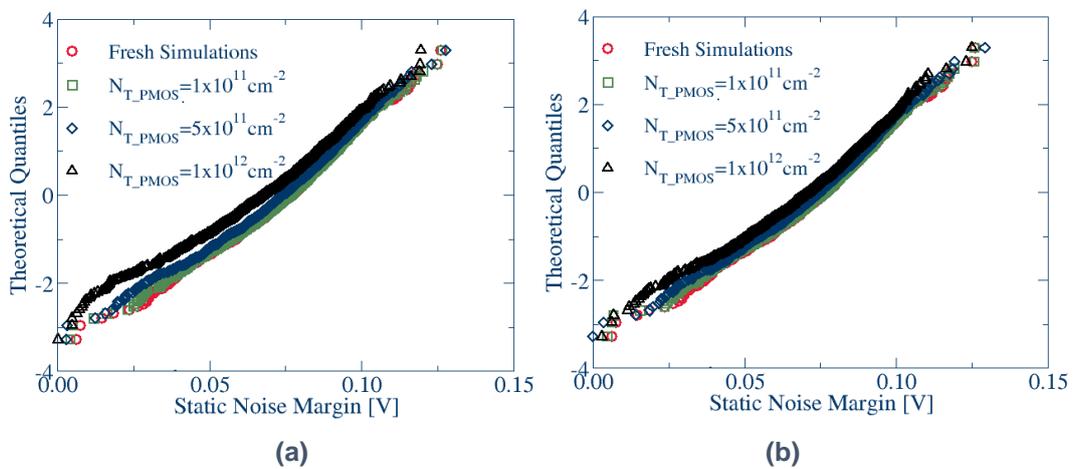


Figure 6-38: mean of SNM distribution in (a) Scenario A, (b) Scenario B and (c) Scenario C.

6.2.2 22 nm Intel FinFET

This section presents the simulation results of SNM of an SRAM degradation based on the 22 nm FinFET. The SRAM degradation is simulated subject to all scenarios described in Section 6.2. Due to the different impact of degradation in the p-channel and the n-channel transistors, several types of degradation ratio between the different transistors are also considered in the simulations.

As in the case of the bulk transistor, described in the previous section, in Scenario A the FinFET SRAM is evaluated based on the hold phase operation. In this operation only N1 and P2 transistors are considered to be subject to BTI degradation. As discussed in the previous sections, the unbalanced degradation in these transistors leads to a similar trend in the FinFET SRAM compared to the bulk transistor case. The lower tail of the SNM distribution is more affected by the degradation compared to the upper tail. The increase in V_T results in a progression reduction of the mean SNM with the degradation. Figure 6-39 illustrates the SNM distribution for Scenario A.



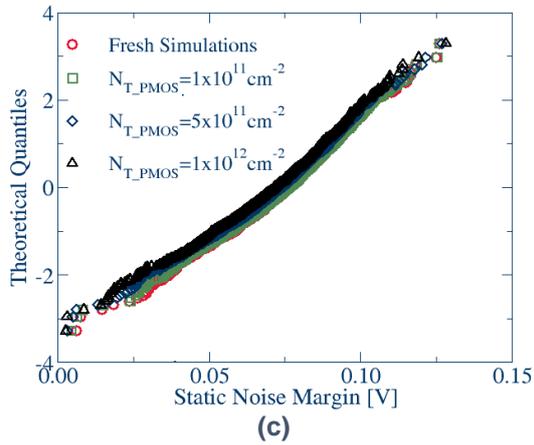


Figure 6-39: QQ-plot for snm distribution in Scenario A with a) Type 1 simulation, b) Type 2 simulation and c) Type 3 simulation.

Scenario B is related to the fast read and write operation; in this operation, all transistors in the inverter pair are degraded simultaneously. Therefore, the butterfly curve produced in this scenario has a balanced symmetrical shape. The trend in SNM distribution is similar to the trend in the conventional MOSFET case. The rigid shift in SNM distribution in the degraded cell decreases when compared to the fresh transistor as illustrated in Figure 6-40.

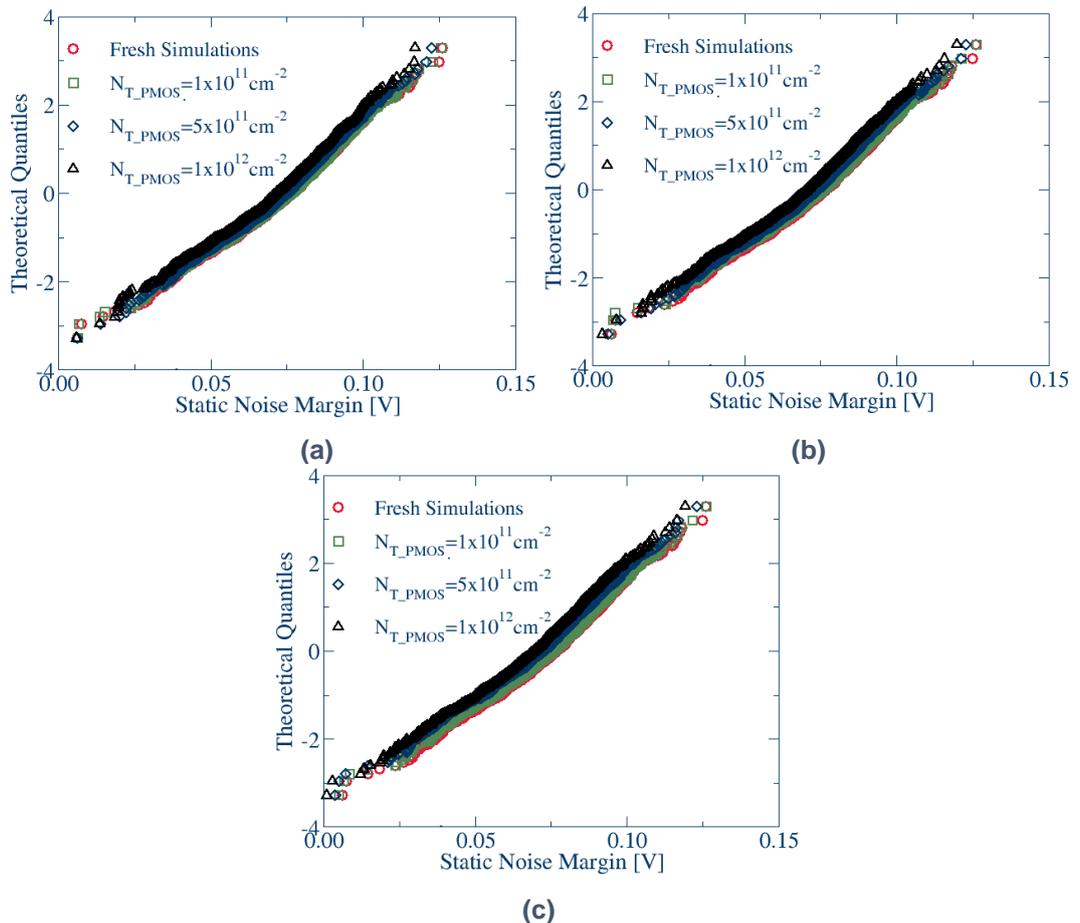


Figure 6-40: QQ-plot for snm distribution in Scenario B with a) Type 1 simulation, b) Type 2 simulation and c) Type 3 simulation.

Finally, in Scenario C, the influence of the PG transistor on the SNM distribution in a fast read and write operation scenario is simulated. As described in the bulk transistors, the trend in the SNM distribution for Scenario C does not have the rigid shift as observed in Scenario B.

In the case of the degradation ratio of types 1, 2 and 4, the mean SNM increases in respect to the fresh transistor. This is because of the trade-off in the impact due to an ageing of the PG and PD transistors and the corresponding cell driveability. Figure 6-41 illustrates the SNM distribution for this scenario.

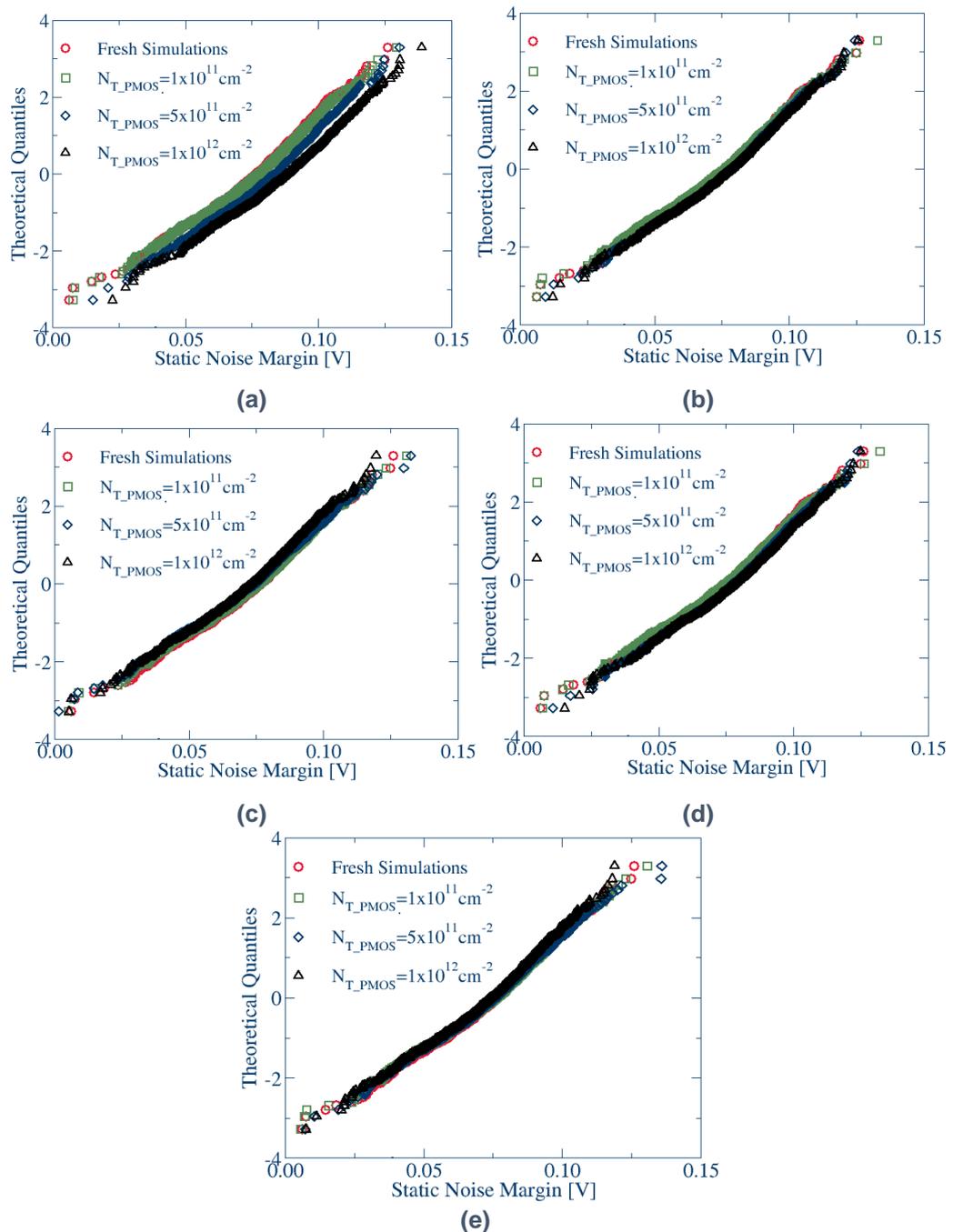


Figure 6-41: QQ-plot for snm distribution in Scenario C with a) Type 1 simulation, b) Type 2 simulation c) Type 3 simulation, d) Type 4 simulation and e) Type 5 simulation.

Figure 6-42 summarises the trends in the STD SNM distribution in each scenario. It shows that the dispersion of the SNM is increasing with the transistor degradation level. Figure 6-43 illustrated, the trend for the mean SNM. Generally the mean of the SNM decreases as the transistor is ageing. But in Scenario C, some of the setup simulation assumptions lead on increase in the mean of SNM with the degradation of the transistor.

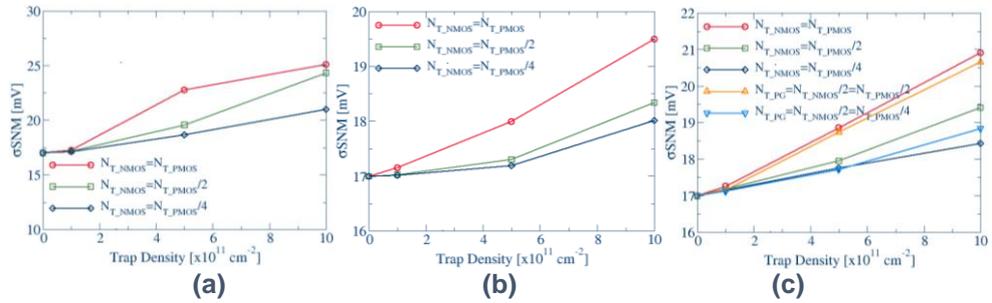


Figure 6-42: standard deviation of SNM distribution in (a) Scenario A, (b) Scenario B and (c) Scenario C.

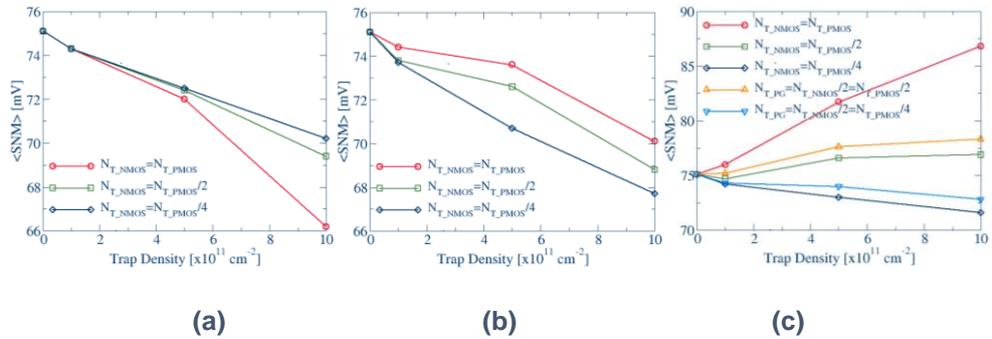


Figure 6-43: mean of SNM distribution in (a) Scenario A, (b) Scenario B and (c) Scenario C.

6.3 Summary

In this chapter, compact model extraction of a 70 nm bulk imec MOSFET and 22 nm Intel FinFET were performed using GSS tools. The CM models of both transistors were extracted over a range of substrate and drain biases. Statistical compact models were also extracted in the case of the 70 nm bulk imec MOSFET. There levels of degradation were considered corresponding to average trapped charge densities of $1 \times 10^{11} \text{ cm}^{-2}$, $5 \times 10^{11} \text{ cm}^{-2}$ and $1 \times 10^{12} \text{ cm}^{-2}$. For the 22 nm Intel FinFET, two degradation levels at $4.6 \times 10^{11} \text{ cm}^{-2}$ and $1.2 \times 10^{12} \text{ cm}^{-2}$. Although the parameter extraction for the imec and the Intel transistors was carried out at different levels of degradation, the capability of Mystic to interpolate in between the extraction levels was used in the analysis. Excellent agreement between the compact models and the TCAD simulation results has been achieved.

The CM libraries generated were then used in the SRAM cell degradation simulations. The impact of the degradation performance of each transistor on the SNM distribution is studied

in detail. Several scenarios have been identified based on the 6T-SRAM operations. Different scenarios for the ratio of degradation of each transistor have also been considered since the degradation levels in the n-channel and p channel transistors are dissimilar. If the SRAM cell is operated according to Scenario A, the degradation increases the SNM variability. This is due to the imbalance in degradation of the inverter pair transistors. Another important finding is the influence of the PG transistor on the SNM distribution due to the change in the driveability between PG and PD transistors.

Chapter 7: Conclusions and Future Works

7.1 Conclusions

The aim of this work was to investigate the impact of statistical variability (SV) and time dependent variability (TDV), related to random telegraph noise (RTN) and bias temperature instability (BTI), on transistors and circuit performance in complementary metal oxide semiconductor (CMOS) technology. As transistors reach the sub-micron regime, the discreteness of charge and matter become major issues in the semiconductor industry. The interaction of TDV with SV was taken into account in TCAD simulations in order to predict accurately their impact of SV and TDV on the transistor characteristics. In this study a 70 nm bulk imec metal oxide semiconductor field effect transistor (MOSFET) and 22 nm Intel fin-shaped field effect transistor (FinFET) have been used. The corresponding TCAD simulations were calibrated using the methodology described in details in Chapter 3. The technology computer-aided design (TCAD) model is developed with the aid of Transmission Electron Microscopy (TEM) image and Scanning Spreading Resistance Microscopy (SSRM) measurements. The substrate sensitivity was used to refine the vertical doping profile by modulating the depletion region, while for the lateral doping profile, V_T roll-off analysis was used to validate the 2D doping distribution. The doping profile was further optimised using atomistic simulations, in comparison with the distribution obtained from the statistical measurements. Finally, comprehensive TCAD simulations of the RTN and BTI phenomena were carried out, based on the calibrated TCAD model.

The investigation of the impact of BTI was extended to the circuit level using the calibrated TCAD simulation results. The aim of the circuit simulations is to predict the static noise

margin (SNM) behaviour in 6T-SRAM cell. In order to evaluate the impact of the ageing on SNM, the calibrated TCAD variability simulations were used to extract statistical compact models. The compact models were extracted from a large statistical ensembles at a different level of degradation, preserving the correlation between the key figures of merit of the transistor. The extracted compact models were then utilised to evaluate the degradation trends in SNM distribution in 6T-SRAM cell.

In Chapter 2, the issues related to CMOS scaling including variability and reliability were presented. The stochastic nature of the ‘atomistic’ transistors where the statistical variability (SV) plays an important role was discussed. The impact of SV becomes more severe with the progressive of transistor scaling. Another crucial issue in determining the transistor performances is oxide reliability which has become critical with the transistor scaling. The simulation of the oxide reliability phenomena is not accurate without taking into account the impact of SV on the transistor performance. This chapter also discusses the importance of the accurate statistical simulation technology in the TCAD and circuit simulation domains, and the need for bridging the gap between these domains by utilising advanced compact model extraction and generation methodology.

In Chapter 3, a comprehensive methodology for TCAD calibration in the presence of statistical variability and reliability was presented. The TCAD transistor structure is calibrated and validated against the measured average of transistor characteristics. The transistor dimensions were extracted from a TEM image and the doping profile deduced from SSRM measurements. The doping profile was refined in the vertical and lateral directions by using the V_T back bias and roll-off dependence respectively. The Masetti and the Caughey-Thomas mobility parameters were adjusted in the calibration process to match the current-voltage characteristics. Finally, the statistical transistor behaviour was taken into account in the calibration. The doping profile near the interface was further refined to match the measured dispersion of the threshold voltage. The link from the TCAD simulation to the circuit simulation by the necessary compact models was also described. The advanced compact model extraction tool Mystic and the statistical ModelGen technology generation tools were used in the circuit simulations. The compact model extraction process captures accurately the variability in each transistor at any degradation level. The ModelGen technology implemented in RandomSpice is capable of generating any arbitrary level of degradation using the interpolating method based on the extraction samples of data. Apart from the methodology, the choice of the DD simulations with Density Gradient correction in GARAND is justified in terms of efficiency and accuracy. The large scale statistical circuit

simulations were enabled by RandomSpice running in a parallel on a large computer cluster to deliver statistically reliable results.

In Chapter 4, the comprehensive calibration of the 70 nm bulk imec MOSFET in respect of experimental data was presented. Initially the calibration was performed on uniform transistor simulations. The transistor dimension were deduced from a TEM image and SSRM measurement to help describe the doping distribution introduced by Anadope. The doping profile was refined further in the lateral direction by using V_T roll-off dependence and refined in the vertical direction by modulating the depth of the depletion region. The $I-V$ characteristic were calibrated using the mobility parameters. Each of these calibration stages delivered a good agreement in compared to of the measurement data. The calibration of the statistical simulation delivers good agreement between simulated and the measured dispersion of the V_T as well. The fine calibration of the doping near the interface improved the simulated dispersion of the threshold voltage associated with RDD, while LER and PSG parameters remain close to the parameters used in previous research. In the reliability analysis, single charge trapping at the interface and the corresponding distribution of the RTN amplitudes was validated in comparison with experimental data measured at imec. Based on this calibrated TCAD model, comprehensive analyses of the RTN and BTI phenomena were carried out and guidelines for the improvement of the transistor variability and reliability were provided.

In Chapter 5, the comprehensive results of the calibration of 22 nm Intel FinFET with respect to published data were presented. Since the published data are limited for this study, three assumptions have been adopted for the purpose of calibration. First, the threshold voltage of the medium power (MP) FinFET was calibrated by Work Function (WF) engineering in order to have a low channel doping concentration. Secondly, the threshold voltage and the leakage current in the SP and LP FinFETs was reduced by increasing the channel doping concentration. This chapter also presents the statistical variability simulation result of this FinFET. At the time this study was performed, the only published data available were the $I_{ON}-I_{OFF}$ ratio in several types of transistor. As for the SV sources in this FinFET (RDD, Gate Edge Roughness (GER) and Metal Gate Granularity (MGG)), the parameters reflect the current state of well-tuned CMOS technology. After the calibration, the simulated $I_{ON}-I_{OFF}$ ratios for the MP, SP and LP FinFETs are located centered in the cloud of the $I_{ON}-I_{OFF}$ ratio of the published results. Following the assumptions made earlier, where the LP FinFET has higher channel doping concentration, the SV simulations shows that the dominant impact of the SV of MP FinFET is from MGG, while for the LP transistor, the impact of the RDD

is more dominant. This is attributed to the increased the doping concentration in the channel of the LP transistor. The impact simulation for the statistical reliability in both MP and LP FinFETs was also presented. For the MP FinFET, the distribution of V_T for fresh transistors and those having trap densities of $3.2 \times 10^{11} \text{ cm}^{-2}$ and $7.2 \times 10^{11} \text{ cm}^{-2}$ has been simulated, while in the LP transistor, the distribution of V_T was simulated for fresh transistors and one having trap densities of $4.6 \times 10^{11} \text{ cm}^{-2}$ and $1.2 \times 10^{12} \text{ cm}^{-2}$. The simulations showed that the average and the standard deviation of the threshold voltage increased with increase of the degradation time. The simulations for the first time provide quantitative values for the magnitude of the NBTI degradation in 22 nm Intel technology FinFETs.

The development of compact models for the 70 nm bulk imec MOSFET and 22 nm Intel FinFET is presented in Chapter 6. The compact model was extracted using Mystic. For the uniform compact model, the extraction process is based on the back bias dependence and drain bias dependence of the continuous current voltage characteristic obtain from xxx TCAD simulations. At the SV compact model extraction stage, the aim of the extraction process was to accurately preserve the variability in each transistor using small sub-set of statistical compact model parameters. The ModelGen technology implemented in RandimSpice allows the interpolation the statistical ensemble at arbitrary levels of degradation based on the extraction domain data. This chapter also presents the circuit simulation of a 6T-SRAM cell to evaluate the impact of the degradation on its performance. The 6T-SRAM performance is evaluated based on the SNM distribution. Several scenarios were considered based on the 6T-SRAM operation. Due to the different levels of degradation in the p-channel and n-channel transistors, the ratio of degradation transistor is also identified, resulting in 3 simulation scenarios A, B and C. If the 6T-SRAM operates in Scenario A, the time dependent variability has a significantly higher impact on SNM compared to Scenarios B and C. The significant variability in Scenario A is due to the imbalance in the inverter pair. Another important highlight in the study of the SNM performance due to ageing is the influence of the pass gate (PG) transistor in the trend of SNM performance degradation. The trade-off between driveability and V_T shift due to the ageing process results in a distinct trend in the mean SNM distribution.

7.2 Future Works

Several research areas are now identified that could be followed to expand the impact of this work. Firstly, in the methodology, the calibration processes in this work is performed manually. The calibration process at each stage is needed to align the simulations with the experimental data. It is important to have a good automated strategy for the calibration process in order to reduce the duration of that process. For the proof of concept in the methodology flow, the calibration of the transistor is successfully done manually. However, it is better if the calibration process is optimised and automated, as this can save a lot of time which can be used to focus on more important and interesting aspects of the research.

The main purpose of this work was to study the impact of the interplay between reliability and variability in TCAD simulation. The simulation of a thousand transistors in each ensemble is adequate for analysing the V_T shift trend in reliability projection. The simulation results are used to extract a statistical compact model which can be used in the circuit simulation. The simulation in 6T-SRAM cell is based on a somewhat restricted transistor sample set to evaluate the SNM performance. This size is adequate for analysing the trend in SNM distribution. However, in the industry environment, engineers are more concerned about the tail of the distribution. Thus the sample size has to increase to support 5σ or beyond. This 5σ represents the probability of design failure in 1 simulation out of 3.5M simulations.

Currently the description of the reliability phenomenon is based on a framework considering bistable BTI defects, featuring quite complicated trapping dynamics, including two states: capture and emission processes. This defect also allows for different transition paths, which can explain the dual trap behaviour seen in Time Dependent Defect Spectroscopy (TDDS). However, a comprehensive charge trapping multi-states model is in the development process and will be implemented in the 3D 'atomistic' simulator GARAND at a latter stage. This model will be used to obtain the transition rates necessary to feed an ad-hoc developed Kinetic Monte Carlo (KMC) engine that ultimately will provide the stochastic dynamic BTI traces that will be compared to the experimental data. By having this new framework, it will be useful if the reliability part is re-simulated and compared with the mismatch between each framework.

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