On-detector electronics for high speed data transport, control and power distribution for the LHCb VELO and ATLAS Pixel Upgrades.

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Abstract

The Large Hadron Collider (LHC) will see an upgrade to higher luminosity to widen the scope of study of particle physics and this will be a major upgrade of the LHC. The LHC collides protons at an energy of 13 TeV in order to study the fundamental components of matter and the forces that bind them together. The High-Luminosity Large Hadron Collider (HL-LHC) will enter service after 2025, increasing the volume of the data for analysis by a factor of 10. The phenomena that physicists are looking for have a very low probability of occurring and this is why a very large amount of data is needed to detect them. Vertexing and tracking sub-detectors for these High Energy Physics (HEP) experiments deliver very high data rates that require multi-gigabit transmission links. Commercial solutions such as optical transmission or wire cabling are investigated, however, due to high radiation environments and low radiation length requirements, electrical transmission with low mass custom designs have to be considered. Designing transmission lines with this requirement does pose a challenge and optical data transmission is used when space and radiation limits allow.

The increase in luminosity will produce more data making it possible to study the phenomena in more detail by increasing the number of collisions by a factor of between five and seven. The increase in data will require an enhanced readout system and related electronics to be able to transmit and read out the data for further processing. At the same time powering systems need to be looked at to understand cost efficient and reliable techniques to be able to power such electronics. The thesis focuses on the readout electronics of the LHCb Vertex Locator (known as the 'VELO') Upgrade and the ATLAS Inner Tracker (known as the 'ITk') Upgrade including design of some components of the sub-systems, testing for high-speed data signaling, powering schemes and analysis of PCB designs and scope for improvements.

An introduction to the LHC and the four experiments that use its beam - ATLAS, CMS, ALICE and LHCb is outlined. The thesis work is focused on two of these detectors namely ATLAS (A Toroidal LHC ApparatuS) and LHCb (Large Hadron Collider beauty) and these are further explained and details of the sub-systems that make up these detectors are elaborated. Major differences to the upgrade of the experiments is explained highlighting the changes and the main challenges that would need to be addressed.

The work on the On-detector electronics of the LHCb VELO Upgrade with details of the design requirements and implementations for the different components is described and test

results are presented. Data tapes for carrying high speed data signals and control signals from the front-end chip to the Vacuum Feedthoough (VF) were designed and successfully tested to have a loss of $<$ 10 dB at the Nyquist frequency of 2.5 GHz and a characteristic impedance of approximately 94 Ω which is within the 10% tolerance of 100 Ω for differential signals. Sensitivity to radiation damage as well as additional mass in the detector acceptance were some factors that motivated the design of the Opto Power board (OPB). In addition, there was a need to power the front-end ASICs but from outside the vacuum tank. The OPB was designed to meet these requirements in addition to be more easily accessible for repair and maintenance. The OPB is realised in an 8-layer stackup, with custom designed radiation hard ICs, and was designed for optical to electrical conversion of 20 high-speed data links at 5.12 Gb/s per link to be read by the Off-detector electronics. The board comprises 13 DC-DC converters for powering 12 ASICs, two front-end hybrids and the OPB itself with a total current supply of 26 A.

The ATLAS experiment will implement the Inner Tracker (ITk) which is a new tracker to be installed during the major ATLAS Upgrade during Long Shutdown 3. The work on the ATLAS ITK addresses two topics; a novel pixel powering scheme adopting layout techniques for high-speed design. A serial powering scheme was evaluated to be an optimal option and this scheme was tested to understand its scope and implementation in the pixel endcap design and results are presented. A study to understand the existing Crescent Tape PCB layout and techniques to improve the design for high-speed data transmission was evaluated.

Methods for analysing high-speed data using S-parameters and eye diagrams, sources of signal degradation and mitigation techniques, are detailed. The laboratory test setup for high-speed measurements with the equipments used is also explained.

Acknowledgements

This thesis has become a reality with the blessings of the Almighty for giving me the strength, patience and keeping me focused though this journey. There are many people who have directly or indirectly contributed towards the completion of my thesis and I would like to express my deepest gratitude to all of them.

Firstly, I would like to thank my mentors, Prof. Lars Eklund and Dr. Richard Bates for helping and guiding me more than I could ever give credit for here. This accomplishment would not have been possible without their guidance and involvement, their support and encouragement at every stage of the thesis. They both were always there whenever I ran into a trouble spot or had any question related to my work or thesis writing. I would like to thank Dr. Kenneth Wraight, Dr. Cameron Dean, Dr. Manuel Schiller and Ms. Leyre Flores with whom I closely worked to complete some part of my thesis results. They have been extremely supportive and helpful colleagues and their extensive knowledge in physics and electronics has helped me a lot in meeting the objectives.

I am grateful to all of those with whom I have had the pleasure to work on both the ATLAS Upgrade and LHCb VELO Upgrade projects during this time. Each of the members I have worked with has provided me with professional guidance and support whenever needed.

I would like to express my thanks to the University of Glasgow for all the infrastructure made available that was much needed to carry out my research work. The atmosphere at the University, especially within the Detector Development Group, is incredibly collaborative and a wonderful learning environment. Not forgetting the Beans on Roast club for the lively environment in the office next door.

Finally, my thanks to my family for all of the love, support, encouragement and prayers they have sent my way along this journey. I must express my very profound gratitude to my parents who have been my ultimate role models and for always being with me in whatever I pursue. I am in debt to the unconditional love and care and the sacrifices they have done to help me be where I am today. I would like to thank my sister, Shradha, for always being there for me as a friend. Thanks to my parents-in-law who have believed in me and supported me in my goals.

From the thought of pursuing the Masters degree to its completion would not have been possible without the help of my husband, Amogh, who has provided me with unfailing love

and continuous support throughout my years of study and through the process of writing the thesis. Thanks for being patient with me when I was frustrated and for encouraging me to be focused to complete my thesis. I wish to thank my beautiful daughters, Anika and Aahana, who have tried to understand me and have helped me in their own way to complete this thesis. You both are my endless inspiration and have made me stronger and more fulfilled than I could have imagined.

Declaration

This report is a product of my own work for the Masters degree and has not previously been presented for another degree in any other department or University.
Chapter 1 is a description of the LHC and specifically about the ATLAS and LHCb experiments and environments and doesn't contain any of my work.
Chapter 2 describes the methods and techniques used for design and testing and does not contain any of my work, apart from Section 2.5 where my contribution to the design of the CTLE is described. I have consolidated the information related to design guidelines and techniques which has been used in the work covered in the thesis.
Chapter 3 is a description of the LHCb Velo Upgrade where I have contributed to the systems design of the VELO electronics and my work on design is detailed.
Chapter 4 is a description of the LHCb VELO On-detector electronics testing. I designed all the PCBs that are described in the measurements except for the Vacuum Feedthrough Board where I was closely involved in the design and review. The Data tape measurements was a joint effort by Dr. Cameron Dean and myself. The high-speed links and Opto Power Board characterisation was a joint effort by Prof. Lars Eklund, Dr. Manuel Schiller, Dr. Cameron Dean along with me. The full link testing was mainly done by Dr. Cameron Dean with my help on the setup and testing, wherever needed. The testing of test coupons for high-speed performance before and after radiation was done by me.
Chapter 5 describes the systems design of the ATLAS ITk which does not involve my contribution. I have specifically worked on two topics described in this Chapter. I have collaborated with others to build a test system for testing serial powering scheme and I have designed all the test PCBs described in this section. Dr. Kenneth Wraight and myself together worked on debugging the hardware along with testing the different powering schemes. I was focused more on the electronics work while the the scans/plots for noise measurements were done by Dr. Wraight. For the high-speed measurements on the Crescent tape, all the test boards and measurements described were performed by me.
Wherever contribution of others is involved, every effort is made to indicate this clearly, with relevant reference to the literature and acknowledgment of collaborative research and discussions.

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Chapter 1

Introduction

1.1 The Large Hadron Collider

The Large Hadron Collider [1] (LHC) is the world's largest and most powerful particle accelerator. It first started up on 10 September 2008, and remains the flagship of the CERN's (The European Organization for Nuclear Research) accelerator complex located in Geneva. The LHC consists of a 27-kilometre ring of superconducting magnets with a number of accelerating structures to boost the energy of the particles along the way. A view of the inside of the LHC tunnel is shown in Figure 1.1. Inside the accelerator, two high-energy particle

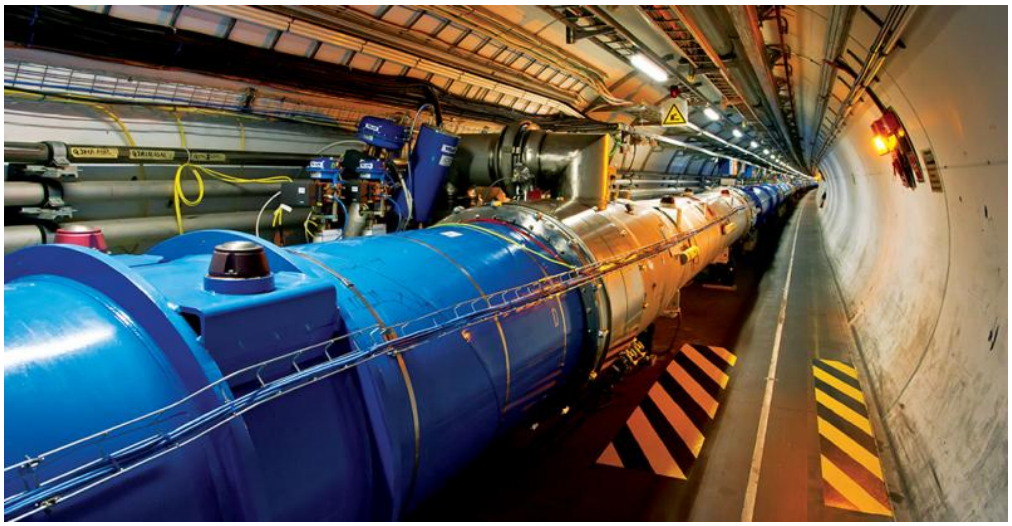


Figure 1.1: A view inside the Large Hadron Collider (LHC) Tunnel [2].

beams travel at close to the speed of light before they are made to collide. The beams travel in opposite directions in separate beam pipes, in two tubes kept at ultrahigh vacuum. They are guided around the accelerator ring by a strong magnetic field maintained by superconducting electromagnets. The electromagnets are built from coils of special electric cable that operates in a superconducting state, efficiently conducting electricity without resistance or loss of energy. This requires chilling the magnets to -271.3°C, a temperature colder than

outer space. For this reason, much of the accelerator is connected to a distribution system of liquid helium, which cools the magnets, as well as to other services.

The LHC has thousands of magnets of different varieties and sizes that are used to direct the beams around the accelerator. These include; 1232 dipole magnets 15 metres in length which bend the beams, and 392 quadrupole magnets, each 5-7 metres long, which focus the beams. Just prior to collision, another type of magnet is used to focus the particles closer together to increase the chances of collisions. The particles are approximately of radius of 10^{-15} m and the task of making them collide is analogous to firing two needles 10 kilometres apart with such precision that they meet halfway. All the controls for the accelerator, its

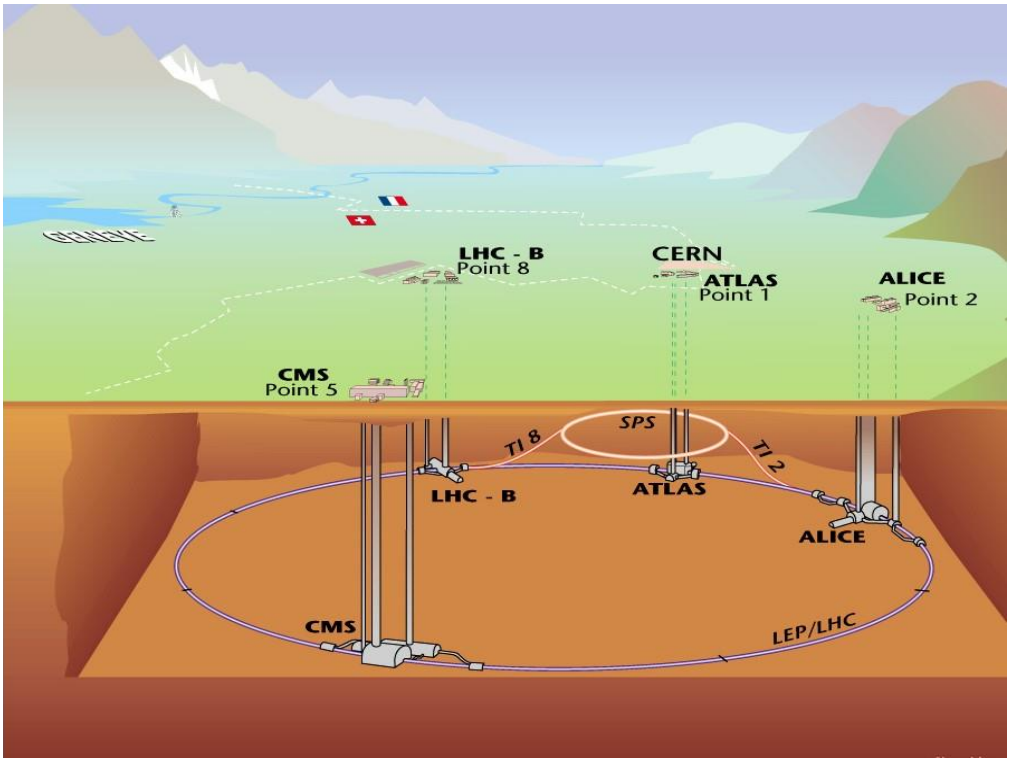


Figure 1.2: Sketch of the LHC ring and the four experiments. The beams are injected in the LHC from the Super Proton Synchrotron (SPS) at an energy of 450 GeV [7].

services and technical infrastructure are housed under one roof at the CERN Control Centre. From here, the beams inside the LHC are made to collide at four locations around the accelerator ring, corresponding to the positions of four physics experiments - ATLAS [3], CMS [4], ALICE [5] and LHCb [6] as shown in Figure 1.2. The LHC represents for the experiments both an unprecedented possibility to study physics at the TeV scale, as well as an extreme experimental environment. To satisfy the requirements for precision measurements, as well as to cope with high interaction rates, radiation doses, particle multiplicities and energies, these experiments have to be carefully designed.

After the consolidation of the electrical splices between the superconducting magnets in the Long Shutdown 1 (LS1), the LHC has operated in Run 2 at 13 TeV centre-of-mass

energy from 2015 and has progressively increased the luminosity attaining the nominal design luminosity of 1 x 10^{34} $cm^{-2}s^{-1}$ in 2016. Despite a reduced number of bunches (about 2200 cf. 2800 nominal) a peak luminosity up to 1.2 x 10^{34} $cm^{-2}s^{-1}$ has been routinely obtained in 2016. This peak is largely thanks to reduced emittance from the injectors and a beta [8] value of 40 cm (cf. 55 cm nominal value) at the high luminosity interaction points. In the period 2017-2023 the LHC will hopefully further increase the peak luminosity and margins in the design of the nominal LHC are expected to allow about two times the nominal design performance. After Run 3 the statistical gain in running the accelerator without a significant luminosity increase beyond its design and ultimate values will become marginal. The running time necessary to halve the statistical error of a given measurement after 2020 will be more than ten years. Therefore, to maintain scientific progress and to exploit its full capacity, the LHC will need to have a decisive increase of its luminosity after 2020. A subsequent major luminosity upgrade to High Luminosity (HL-LHC) will make it possible to study the data produced in more detail by increasing the number of collisions by a factor of between five and seven. This upgrade together with focused research and development activities would boost the potential for physics discoveries after 2025. The LHC schedule and timelines are as shown in Figure 1.3.

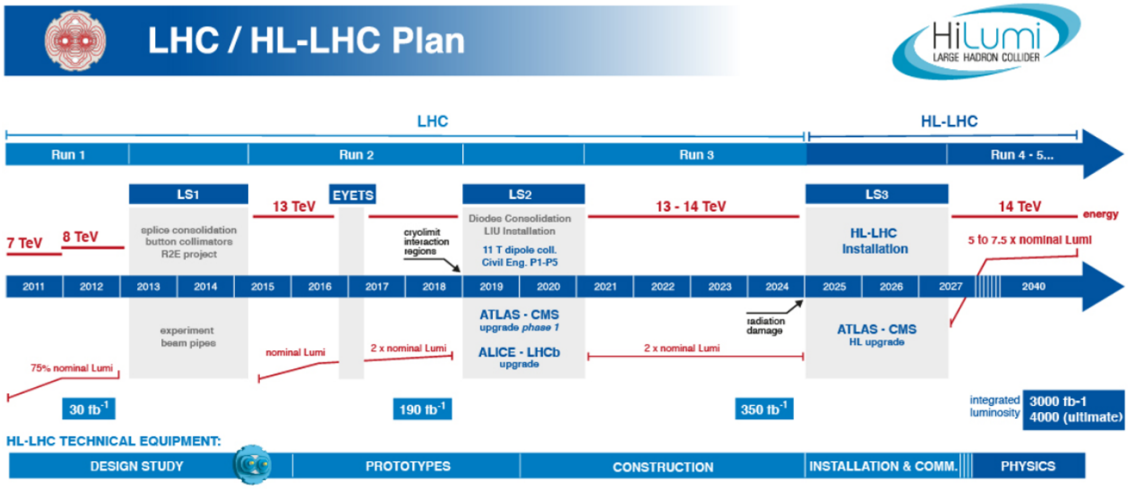


Figure 1.3: The LHC Schedule overview [9].

1.2 The LHCb Detector - The first version

The Large Hadron Collider beauty (LHCb) experiment [10] is a single arm spectrometer aimed at measuring CP[1] [11] violation and rare decays of beauty (b) and charm (c) quarks,

[1] CP violation, in particle physics, is a violation of the combined conservation laws associated with charge conjugation (C) and parity (P) by the weak force, which is responsible for reactions such as the radioactive decay of atomic nuclei.

collectively known as heavy flavour hadrons (to include both the b and c physics programme, and baryons). The experiment's 5,600 tonne detector is specifically designed to reconstruct these particles and the products of their decay. The detector is 21 metres long, 10 metres high and 13 metres wide, and sits 100 metres below ground near the village of Ferney-Voltaire, France. About 27% of the $b\bar{b}$ quark pairs produced are in the LHCb acceptance and predominantly close to the beam axis which is reflected in the design of the detector. Other LHC experiments surround the entire collision point with layers of sub-detectors, but the LHCb detector stretches for 20 metres along the beam pipe, with its sub-detectors stacked behind each other. Each one of LHCb's sub-detectors specializes in measuring a different characteristic of the particles produced from the proton collisions. The system is designed to detect all the particle types produced except for neutrinos as they are so weakly interacting and their presence is inferred if the energy of the detected particles is less than the colliding ones. Collectively, the detector's components gather information about the identity, trajectory, momentum and energy of each particle generated, and can single out individual particles from the billions per second that spray out from the collision point. Figure 1.4 shows the schematic view of the LHCb detector showing the different sub-systems that are explained here.

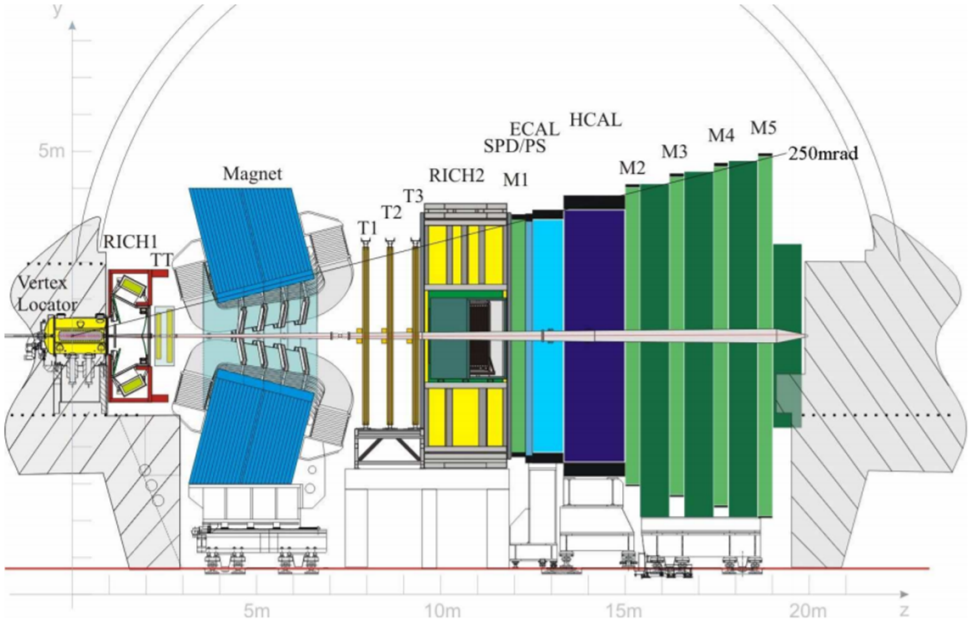


Figure 1.4: Schematic view of the LHCb Present detector. VELO = Vertex Locator; RICH1,2 = Ring Imaging Cherenkov detectors; TT= Tracker Turicensis; T1, T2, T3 = Tracking stations; SPD/PS = Scintillating Pad Detector/Preshower; ECAL = Electromagnetic Calorimeter; HCAL = Hadron Calorimeter; M1, M2, M3, M4, M5 = Muon stations 1 to 5. [6].

The (High Rapidity Shower Counters) HeRSCheL detector : This detector is located not in the LHCb cavern but in the LHC tunnel itself, on both sides of the LHCb

interaction point. The HeRSCheL system comprises three stations at negative z, known as backward or 'B' stations, and two stations at positive z, known as forward or 'F' stations. The station closest to the interaction point, named 'B0', is located at $z \sim 7.5$ m and the most distant stations, 'B2' and 'F2', are located at $\sim \pm 114$ m, close to the point at which the beam pipe splits into two, one for each beam. The detector was built during 2014 and installed at the beginning of 2015 with the goal of enhancing studies of diffractive physics at LHCb. It consists of twenty square plastic scintillators, about 30 cm wide, in which tiny flashes of light are produced when a charged particle passes through. The scintillators are placed at a distance of only centimeters from the LHC beam, just outside the vacuum pipe, and can therefore be used to detect activity corresponding to particles produced by a particle collision in the main LHCb detector but whose deviation from the beam direction is so small that they escape down the beam-pipe and only emerge further along the tunnel, near the HeRSCheL detectors. This ability to detect particles at such small angles is crucial for a particular set of measurements made by physicists enhancing LHCb's capabilities in diffractive physics -in particular Central Exclusive Production (CEP) analyses [12] . These measurements revolve around the study of proton-proton interactions where rather than colliding head-on, the interacting protons merely glance off each other and, in doing so, produce a very small number of particles that can be detected using the standard LHCb detectors and should not lead to activity in HeRSCheL.

The Vertex Locator : The LHC proton beams pass through the full length of the detector, safely encased within a beryllium pipe. The only point where the beams collide, and particles containing b and anti-b quarks are produced, is inside the Vertex Locator (VELO) sub-detector [13, 14]. The VELO reconstructs the production and decay vertices of the particles produced in the collisions. The first version of the VELO detector is manufactured with 84 single-sided radial (R) and azimuthal-angle (ϕ) measuring strip sensors operated in a secondary vacuum inside the LHC beam pipe. The R and ϕ sensors are mounted on either side of a highly thermally conductive spine which also supports the readout hybrid, and the resulting double sided module is supported on a carbon fibre paddle stand. The modules are arranged perpendicularly to the beam along a length of about 1 m. Module cooling is provided by evaporative CO_2 circulating in stainless steel pipes embedded within aluminum pads which are clamped to the base of the module. The detector is divided into two moveable halves, allowing it to retract during LHC injection. The cabling between the modules and detector hood must be flexible enough to absorb these movements, which occur for every LHC fill. LHCb differs from the other experiments in that a VELO is inserted inside a vacuum tank [15] around the interaction point, separated from the beam vacuum by a 300 μm thin aluminum foil (RF foil). In the beam pipe region the material is corrugated in such a manner as to reduce as much as possible the material traversed by particles before their first measured

point. Additional corrugations are provided in order to allow the two sides of the VELO to close completely, ensuring full geometrical coverage with a small overlap added for alignment purposes.

The arrangement of the array of VELO modules within the vacuum tank is shown in Figure 1.5.

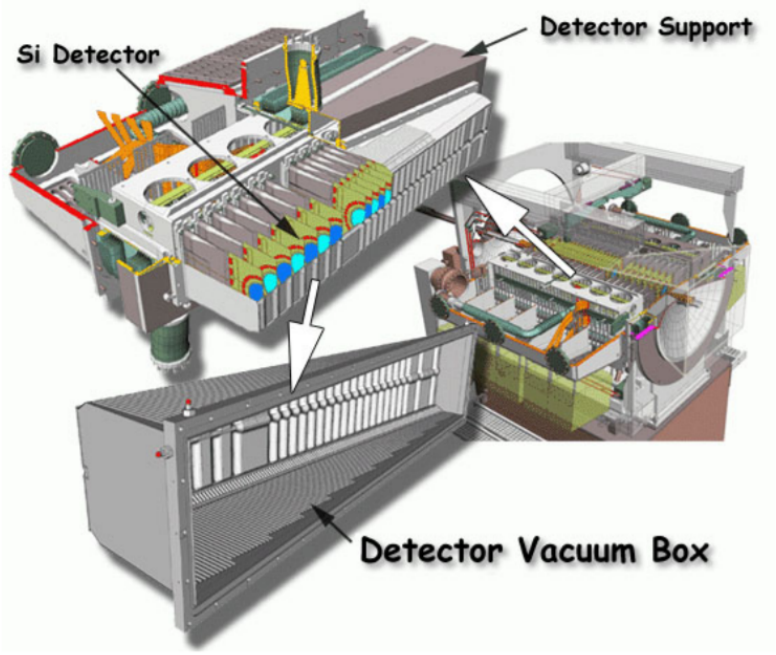


Figure 1.5: Layout overview of the first version of the VELO detector, illustrating the vacuum tank, module positioning and RF foil. For the upgrade it will be necessary to change the modules, foil, module bases, and detector hoods, in addition to major refurbishment of the motion, vacuum and cooling system [16].

The vacuum tank and stand, which together represent a significant fraction of effort and investment in the construction of the current VELO, can be reused for the upgrade, along with the rectangular bellows which allow the movement of the two halves. The concept of the mixed phase CO_2 cooling system will be re-used for the design of the new cooling system for the upgrade.

Ring Imaging Cherenkov (RICH) Detectors : The two detectors (RICH-1 and RICH-2) [17] positioned on either side of LHCb's powerful magnet, are positioned for particle identification in different ranges of momenta. The RICH detectors work by measuring emissions of Cherenkov radiation. This phenomenon, often compared to the sonic boom produced by an aircraft breaking the sound barrier, occurs when a charged particle passes through a certain medium (in this case, a dense gas) faster than light does in that medium. As it travels, the particle emits a cone of light, which the RICH detectors reflect onto an array of sensors using mirrors. The opening angle of the cone of light depends on the particle's

velocity, enabling the detector to determine its speed. This information is then combined with a record of its trajectory (collected using the tracking system and a magnetic field) to test and see which of the possible mass hypothesis (for kaons, pions, protons, etc) best match the observed Cherenkov rings.

Tracking system : The principal task of the tracking system is to provide efficient reconstruction of the charged particle tracks. The main tracking system comprises four tracking stations: one station (TT) is located between RICH-1 and the LHCb dipole magnet, while the other three stations (T1-T3) are located between the magnet and RICH-2. Two different detector technologies are employed in each tracker station. The silicon tracker [18], which is placed close to the beam pipe, uses silicon microstrip detectors to detect passing particles. Charged particles collide with silicon atoms, liberating charge carriers and creating an electric current, which indicates the passage of the original particle. It comprises the entire TT station and a cross-shaped area (the Inner Tracker) around the beam pipe in stations T1-T3. The outer tracker [19] is situated further from the beam pipe and is made up of thousands of gas-filled straw tubes. Whenever a charged particle passes through, it ionizes the gas molecules, producing electron-ion pairs. The position of the track is found by timing how long the electrons take to reach an anode wire situated in the centre of each tube. The outer tracker covers the largest fraction of the detector sensitive area in stations T1-T3.
Silicon is more expensive per unit area but gives a better position resolution than the gas-filled straw tubes. The gas straw tube technology has a coarser resolution than the silicon detectors but is much cheaper and therefore very well suited to cover the large areas of the tracking system where particle densities are not as high. As the best resolution is required closer to the beam pipe the optimal performance-to-cost is obtained with the described arrangement of the tracker technologies.

Magnets : To help identify the explosion of particles produced when protons are smashed together, particle detectors typically include a powerful magnet. The charged particles experience a Lorentz force from the magnetic field and their trajectory is therefore bent. Particles with opposite charge polarity are bent in opposite directions and the amount of the deflection is determined by the particle's momentum and charge. This gives valuable information about the particle to allow it to be identified in combination with the sub-detectors. The experiment's enormous magnet consists of two coils, both weighing 27 tonnes, mounted inside a 1,450 tonne steel frame. Each coil comprises 15 individual monolayer 'pancakes' of trapezoidal racetrack shape, and bent at 45 degrees on the two traverse sides. Each pancake consists of 15 turns of conductor, wound from 300 m length of extruded aluminium.

Calorimeters : The calorimeters measure the energy a particle loses as it passes through the detector. It is usually designed to stop entirely or 'absorb' most of the particles coming

from a collision, forcing them to deposit all of their energy within the detector. Calorimeters typically consist of layers of 'passive' or 'absorbing' high-density material, for example, lead, interleaved with layers of an 'active' medium such as solid lead-glass or liquid argon. The Calorimeter is composed of an electromagnetic calorimeter (ECAL), followed by a hadron calorimeter (HCAL), and before both of them there is a double detector made of three layers, the Scintillator Pad Detector (SPD), a 2.5 radiation lengths lead wall, and the Preshower (PS). The SPD/PS system helps the calorimeter to achieve good background rejection and reasonable efficiency on the detection of photons with reasonable precision. Electromagnetic calorimeters measure the energy of electrons and photons as they interact with matter. Hadronic calorimeters sample the energy of hadrons (particles that contain quarks, such as protons and neutrons) as they interact with atomic nuclei. Calorimeters can stop most known particles except muons and neutrinos.
LHCb uses both types of Calorimeter [20] with the ECAL followed by the HCAL. Both calorimeters have a sandwich-like structure, with alternating layers of metal and plastic scintillator plates. When particles hit the metal, they produce showers of secondary particles. These, in turn, excite polystyrene molecules within the plastic plates, which emit ultraviolet light. The amount of ultraviolet light produced is proportional to the energy of the particles entering the calorimeter.

Muon system : Muons are particles that usually pass through the Inner Detector and Calorimeter undetected. They are tiny, electron-like particles that are present in the final stages of many heavy flavour hadron decays, and so muon detection is important for the LHCb experiment. Muons are weakly interacting and as such are not stopped by the calorimeter system unlike the majority of the other particles produced (except for neutrinos). Located at the far end of the detector, the muon system [21] comprises five rectangular 'stations', gradually increasing in size and covering a combined area of 435 m^2. Each station contains chambers filled with a combination of three gases: carbon dioxide, argon, and tetrafluoromethane. The passing muons deposit energy in the gas,ionising it and wire electrodes detect the results. In total, the muon system contains around 1,400 chambers and some 2.5 million wires.

1.3 LHCb Upgrade and the Vertex Locator (VELO)

The development towards an upgrade of the LHCb detector are ongoing and installation will be completed in 2020. All LHCb sub-detectors at the upgrade will face increased occupancies and rates due to the increase in luminosity. Some of the sub-systems will see a change or upgrade to work with this increase in luminosity. The Tracker Turicensis (TT) will be replaced with a silicon strip tracker called the Upstream Tracker (UT) while the tracker T1-

T3 will be replaced with Scintillating Fibre (Sci-Fi) trackers. The RICH detectors will have new photodetectors and front-end electronics and RICH1 optics and mechanics will also see changes. The Calorimeter system will have an updated front-end electronics with the removal of the Scintillating Pad Detector/Preshower (SPD/PS). Finally, the Muon system will as well see an upgrade to the front-end electronics and M1 will be removed. The schematic side-view of the Upgrade I detector highlighting the changes that will be implemented is shown in Figure 1.6.

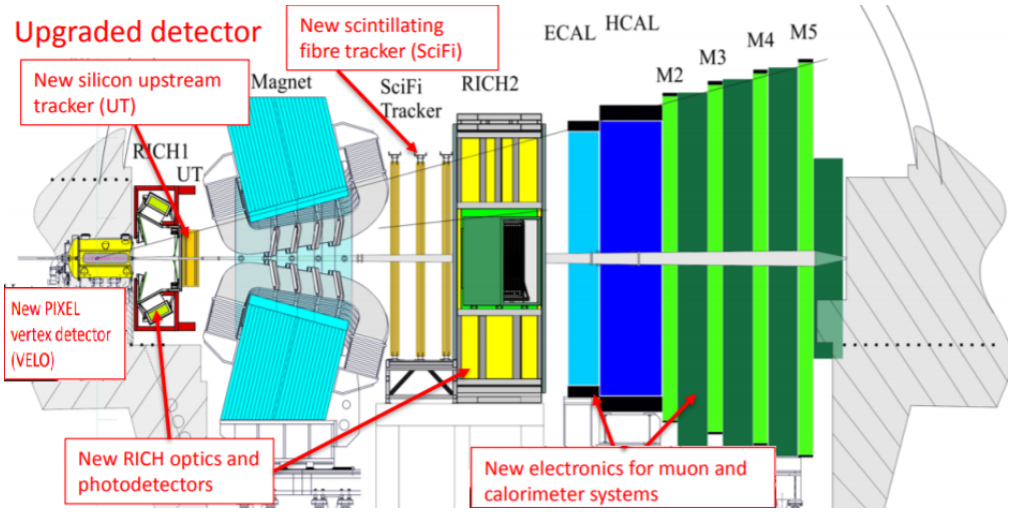


Figure 1.6: The schematic side-view of the Upgrade I detector. The figure highlights the changes that will be seen in the different sub-systems [22].

The upgraded VELO will comprise of a lightweight hybrid pixel detector with a trigger-less system reading out the full detector at 40 MHz. The luminosity will increase to 2 x 10^{33} cm^{-2}s^{-1}, which is a factor of five larger than at present. The comparison of the beam conditions for the current and the best estimates at the upgrade, which have been used in the simulation studies, are given in Table 1.1.

	LHCb	LHCb Upgrade
Beam Energy	7 TeV, 8 TeV, 13 TeV	14 TeV
Number of bunches colliding at LHCb	2200	2400
Luminosity	4 x 10^{32} cm^{-2}s^{-1}	2 x 10^{33} cm^{-2}s^{-1}
# visible interactions per crossing	1.7	5.2
z RMS luminous region σ_{tot}	55 mm	63 mm

Table 1.1: Overview of global LHCb and LHCb Upgrade settings for simulations.

Of particular relevance to the VELO are the z RMS of the beam and the crossing angle, which together determine the extent of the luminous region in z in LHCb to be around $\sigma_{\text{lumi}} =$ 63 mm. This affects the number of stations which must be distributed around the interaction region, and also has an influence on the minimum aperture available at LHCb. Another important parameter is the number of bunches colliding at the LHCb location (IP8), which has

been put at a conservative 2400 bunches, but the expectations are to achieve the maximum possible 2622 bunches, which will slightly ease the occupancy situation at LHCb. The VELO upgrade performance has been evaluated for these conditions, corresponding to μ (number of visible interactions per crossing) = 5.2. However, in order to understand the robustness of the system and to take into account the possibility of less favourable filling schemes, larger multiplicities than expected and increased numbers of secondaries the behaviour has been explored for higher data rates and number of primary vertices. The evolution of the interaction rates as the luminosity increases is shown on the left hand side of Figure 1.7.

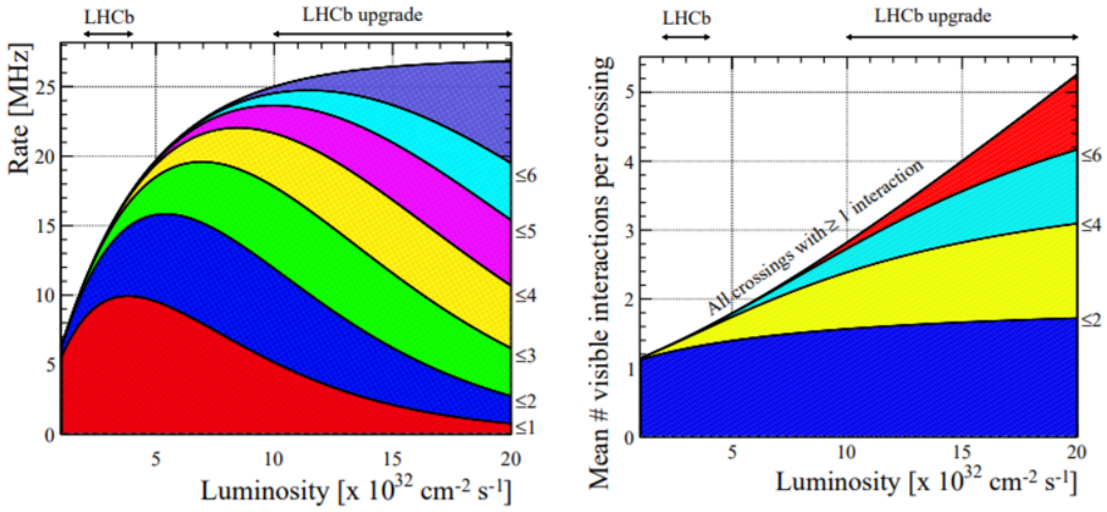


Figure 1.7: Left - Evolution of interaction rates in LHCb (assuming 25 ns spacing) as a function of luminosity, split into categories of number of interactions per event shown on the right axis and colour coded as: red<=1, blue<=2, green<=3, yellow<=4, magenta<=5, cyan<=6, indigo>6. A significant increase in pile-up is visible when going from 1 to 2 x 10^{33} cm^{-2}s^{-1}. Right - Average number of pp (proton-proton) interactions per bunch crossing visible in LHCb as a function of luminosity, for events with at least one visible interaction. [16].

The right hand side of the figure shows the mean number of interactions per bunch crossing in LHCb. The collision rate is 40 MHz with a 25 ns spacing. However the bunches are not evenly spread but come in trains and there are gaps between them. In total there are 3564 'buckets', 25 ns apart in one full turn of the machine (which takes 89 μs). The plan is for a filling scheme where 2400 of these are filled, which gives an interaction rate of 2400/3564 * 40 MHz = 26.9 MHz which is the maximum seen in Figure 1.7 (left). Hence during the bunch trains, it is 40 MHz, but averaged over time it is less depending on the filling scheme. The instantaneous and average collision rates are both relevant for the readout and hence justifies the need of buffers to average out the rates. The displayed average rate being different from the instantaneous rate which can be as high as 40 MHz, which is the peak value used in the estimation of data rates. The expected distribution of the number of vertices per event visible in LHCb is shown in Figure 1.8. At the upgrade ($\mu \sim 5.2$) the number of empty events is almost eliminated, in contrast to the situation in current running ($\mu \sim 1.7$).

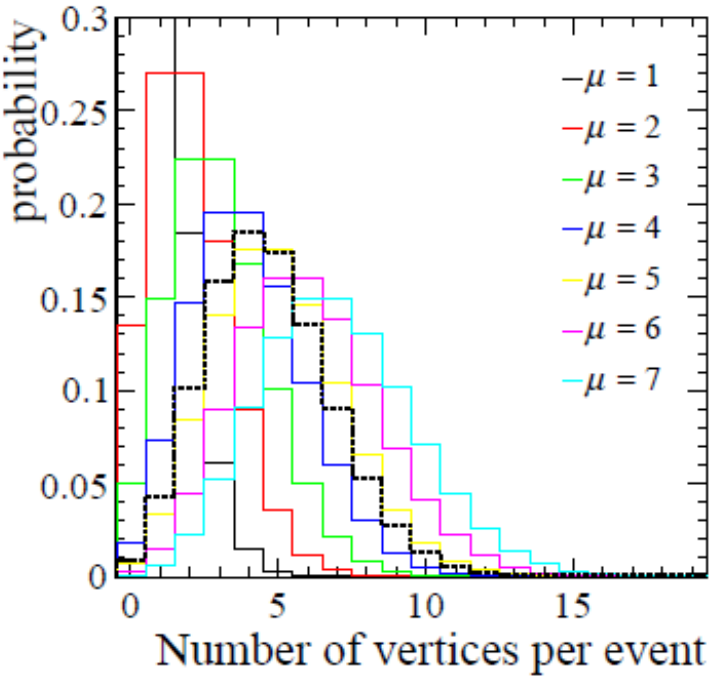


Figure 1.8: Number of vertices per event for running at various values of μ (# of visible interactions per bunch crossing). The default value used in the simulation, corresponding to 2 x 10^{33} $cm^{-2}s^{-1}$, is indicated by the dotted line. [16].

As explained above, the upgraded VELO must maintain or improve its physics performance while delivering readout at 40 MHz in the operating conditions of the upgrade. This can only be achieved by a complete replacement of the silicon sensors and electronics. Following an externally refereed review, the collaboration has chosen to install a detector based on hybrid pixel sensors [13]. A new radiation hard ASIC called the VeloPix [23] capable of coping with the data rates is developed and is being tested. The module cooling system is being designed to protect the tip of the sensor from thermal runaway effects after significant irradiation, and to cope with the high-speed pixel ASIC power dissipation and for this reason, the upgrade cooling is integrated within the module, in contrast to the currently installed detector. The cooling is provided by CO_2 circulating within miniature channels etched into thin silicon substrates which form the backbone of the modules [24]. The upgraded VELO reuses large parts of the current mechanical infrastructure, in particular the vacuum tank, and elements of the very successful mixed phase CO_2 cooling system.

The conceptual layout of the VELO Upgrade detector within the LHCb coordinate system is shown in Figure 1.9. It is very similar to the current VELO layout, however the z positions of the modules have been changed in order to reach similar acceptance given the smaller module size and smaller distance from the beam line to the first measured point. The positions of the modules in the closed (LHC stable beam operation) position along with the

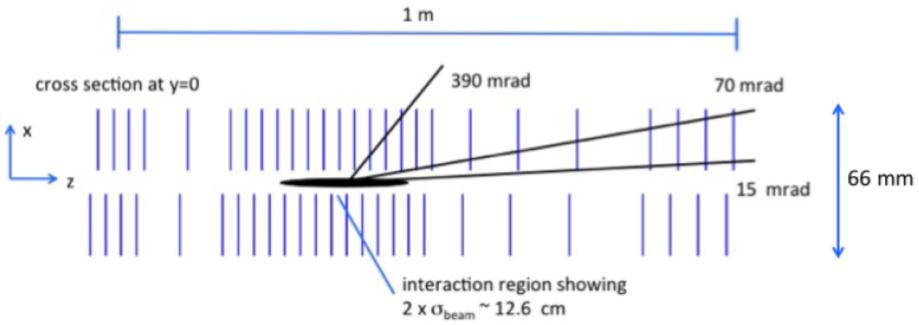


Figure 1.9: The conceptual layout of the VELO Upgrade detector within the LHCb coordinate system [16].

other components of the On-detector electronics is shown in Figure 1.10. In contrast to the current VELO no additional overlap is needed as due to the non projective L-shape geometry of the modules approximately 10% of tracks traverse both the left and right side, and can be used to align the sides. The reconstruction speed and precision of the detector is enhanced by this L-shaped pixel geometry and the distance from the beam to the first sensitive pixel is decreased from 8 mm to 5.1 mm.

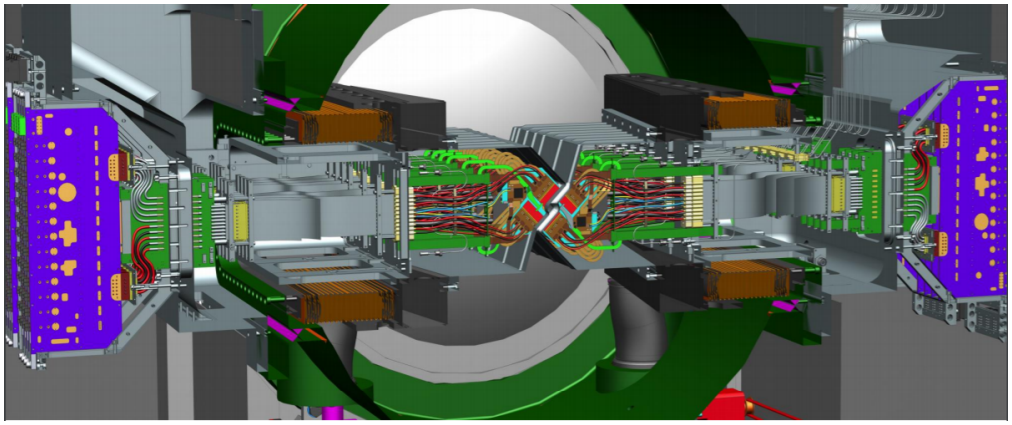


Figure 1.10: View of the Upgrade VELO system in closed position showing the 2 modules with L-shaped geometry at the centre, close to the beam. Also seen are the data tapes, Vacuum Feedthrough Board (VFB) and the Opto Power Board (OPB) that make up the On-detector electronics [25].

1.4 ATLAS - The present System

The ATLAS (A Toroidal LHC ApparatuS) [26] experiment at the LHC is designed with the primary goal of probing pp collisions at high luminosity and in order to maximize the potential for the discovery of physics beyond the standard model. Large acceptance in pseudo rapidity with almost full azimuthal angular coverage is required along with high detector granularity needed to handle the particle fluxes and to reduce the influence of overlapping events. Detector elements, such as electronics and sensors, should be fast and radiation-hard to survive in the LHC environment during the entire experiment lifetime. Different detector sub-systems should then assure a good charged particle momentum resolution and track reconstruction efficiency, as well as electron identification, and measurement of secondary vertices for identification of τ-leptons and heavy quarks. In addition, a highly efficient trigger for particles at low-pT (low-transverse momentum) thresholds, with sufficient background rejection is needed to achieve an acceptable trigger rate for most physics processes of interest. These specifications have been used in the design of the ATLAS experiment resulting in the layout shown in Figure 1.11.

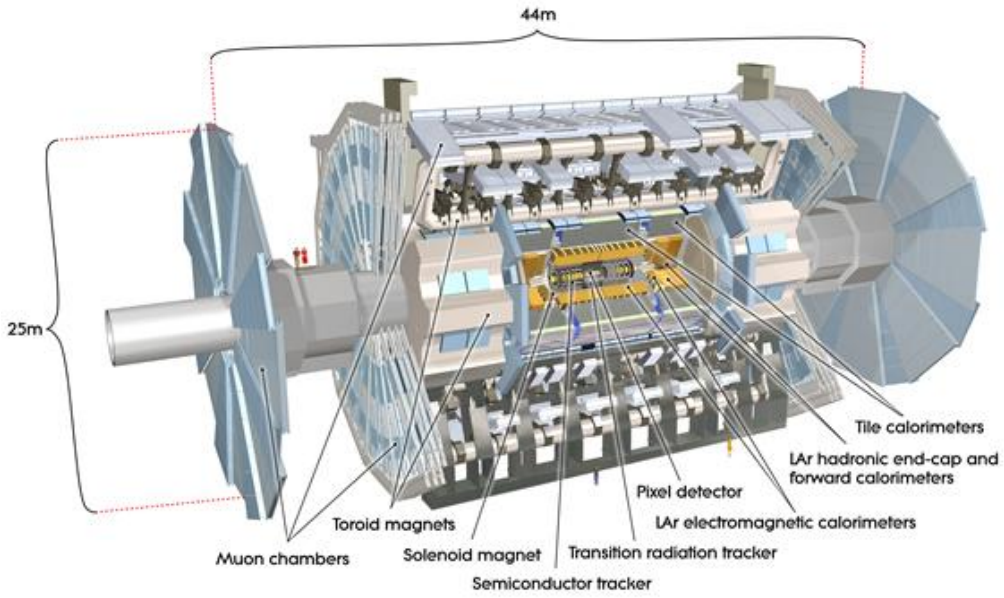


Figure 1.11: Cut-away of the overall ATLAS experiment showing the various sub-detectors and the two magnet systems [3].

The ATLAS experiment is a 4π detector, forward backward symmetric with respect to the interaction point. The detector has a height of 25 m and it is 44 m long, with a total weight of 7000 tonne. The detector is the largest volume particle detector ever constructed and sits in a cavern 100 m below ground near the main CERN site, close to the village of Meyrin in Switzerland. The central detector region is called the barrel, and the two sides are the endcaps. In the ATLAS coordinate system the z-direction is set along the beam axis, while

x and y coordinates are in the transverse plane. Polar coordinates are used in the transverse plane, where the R coordinate describes the radial position from the beam axis, and the ϕ coordinate describes the azimuthal angle. The pseudorapidity describes the angular position with respect to the beam axis, and it is defined as η = -ln(tan(θ/2)), where θ is the angle with the beam axis. The detector sub-systems can be seen as concentric cylinders, centered around the beam pipe. Pattern recognition, momentum and vertex measurements, and electron identification are achieved with tracking detectors, that make up the inner detector system, which is immersed in a solenoidal magnetic field of 2 T. The beams of the LHC consist of trains of particle bunches with the minimum time interval between passage of successive bunches within a train being 25 ns. Thus collisions can take place every 25 ns within a time interval determined by the lengths of the bunches, i.e. typically shorter than 1 ns. At an instantaneous luminosity of 10^{34} cm^{-2}s^{-1} and bunch spacing of 25 ns the average number of interactions is about 23 per bunch-crossing, corresponding to about 10^9 interactions per second. A 3-level trigger system [27] is used to convert the 1 GHz interaction rate at design luminosity, to a final data taking rate of approximately 200 Hz. This system provides an overall rejection factor of 5 x 10^6 against minimum-bias processes, while maintaining maximum efficiency. The physical event rate from which events must be selected is 40 MHz: the rate at which the beam bunches are delivered to the LHC experiments. The three-level trigger system selects interesting events and cuts down the initial bunch crossing rate of 40 MHz to about 75 kHz at Level-1, to about 3 kHz at Level-2, and to about 200 Hz at the final stage. The different sub-detectors for ATLAS are described here.

Inner Detector : The Inner Detector [28] is the first part of ATLAS to see the decay products of the collisions, so it is very compact and highly sensitive. It is the most important detector used in the identification and reconstruction of secondary vertices from the decay of, for example, particles containing a b-quark or for b-tagging of jets. In addition, it provides excellent spatial resolution for reconstructing primary vertices coming from the pp interaction region within ATLAS even in the presence of the multiple interactions at the LHC design luminosity. The Inner Detector measures the direction, momentum, and charge of electrically-charged particles produced in each proton-proton collision. It consists of three different systems of sensors all immersed in a magnetic field parallel to the beam axis. The main components of the Inner Detector are: Pixel Detector, Semiconductor Tracker (SCT), and Transition Radiation Tracker (TRT). The Pixel Detector system [29, 30] is the innermost element of the Inner Detector that comprises the barrel (low-$|z|$ region) in the central area and the endcaps (high-$|z|$ regions) which are, at either ends of the barrel. There are 3 barrel layers (1456 modules) and 3 pixel discs (288 modules) on each side. There are in all 80 million pixels (80 million channels) covering an area 1.7 m^2 and 15 kW of power consumption. The Semiconductor Tracker (SCT) comprises a silicon microstrip tracker consisting of 4088 two-

sided modules and over 6 million implanted readout strips. 60 m^2 of silicon is distributed over 4 cylindrical barrel layers and 18 planar endcap discs. The Transition Radiation Tracker (TRT) consists of 350000 read-out channels with a volume of 12 m^3. It provides additional information on the particle type that fly through the detector i.e. if it is an electron or pion.

Calorimeter : The components of the ATLAS calorimetry system are: the Liquid Argon (LAr) Calorimeter and the Tile Hadronic Calorimeter [31,32]. Both the electromagnetic and hadronic calorimeters in ATLAS are at larger radius to the solenoidal magnet that surrounds the Inner Detector.

Solenoid : A superconducting solenoid is used to provide the B-field to deflect the charged tracks in the Inner Detector to aid particle identification [33].

Muon Spectrometer : The muon spectrometer [34], made up of 4000 individual muon chambers using four different technologies produced by 48 institutions in 23 production sites around the world, identifies and measures the momenta of muons. Subsections of the Muon System comprise Thin Gap Chambers, Resistive Plate Chambers, Monitored Drift Tubes, and Cathode Strip Chambers.

Magnet system : The magnet system bends the path of particles as they traverse the various layers of detector systems, making it easier to contain the tracks of particles. The magnet system bends the charged particles due to Lorentz force and from the direction of bend the sign of the charge can be determined while the amount of bend determines the momentum. The main sections of the magnet system are Central Solenoid Magnet, Barrel Toroid and 2 Endcap Toroids [35].

1.5 ATLAS - Upgrade and Inner Tracker (ITk)

The ATLAS detector has been assembled over a period of three years. Commissioning started in the second half of 2007, and data taking in 2009 with the first stable beams from the LHC. The detector performed remarkably during the first three years of operation, proving that the chosen design allows to investigate a wide spectrum of physical phenomena at the TeV energy scale in the harsh LHC environment. With the integrated luminosity recorded by the experiment, the ATLAS collaboration discovered a new boson whose properties confirm the hypothesis of a Standard Model (SM) Higgs boson [36]. The detector capability has to be consolidated and improved to maintain the capability of the experiment. This would enhance precision measurements and potential for the discovery of physics beyond the standard model, while meeting the new challenges of operating in a high luminosity environment. No major interventions were made to the detector system during LS1, as during Phase-0 the machine

operated at design parameter, only the pixel detector underwent the first upgrade project. In order to preserve performance strength and efficiency at higher than design luminosity, a new pixel layer, the Insertable B-Layer (IBL) [37], was added at a smaller radius inside the present detector. Insertion of the IBL was done during the first LHC shutdown 1 (LS1), and operation started during run 2 of the LHC, but is still considered Phase-0 of the ATLAS experiment. The Phase-I [38] upgrade of ATLAS concerned mostly an improvement of the trigger system to cope with luminosities higher than the LHC nominal value that will take place in LHC Run 3 from 2021 onwards. In particular the Level-1 trigger upgrade allows the maintaining of low-p_τ thresholds for isolated leptons, as required for precision measurements of the Higgs boson couplings in the low mass region, as well as for searches for supersymmetric (SUSY) particles in a large region of the SUSY parameter space. Improvement of the high-level trigger leads to more efficient identification of events with isolated τ leptons and B-hadrons, improving the selection of Higgs boson decays and the sensitivity to many other physics channels. The detector sub-systems involved in this upgrade are the calorimeters and the muon spectrometer. Phase-II [39] will see a major upgrade of the detector systems. In particular, the increased luminosity requires a new Inner Detector able to cope with the higher rates, higher pile-up, and higher radiation levels. A new all-silicon tracker and a new tracker readout will include the implementation of a track trigger to improve the ATLAS trigger capabilities. New readout systems are also required to maintain the performance of the calorimeters and of the muon spectrometer. Finally, a new trigger architecture will be implemented to exploit the upgrades of the detector readout systems, improving the event selection.

In order to maintain tracking and b-tagging performances in such a track-dense environment, a tracking detector with improved resolution, efficiency, and material budget will be required. Such a tracking detector will also have to cope with the increased radiation damage expected from the integrated luminosity of the High luminosity (HL)-LHC, compared to that of the LHC. The current ATLAS Inner Detector will be heavily radiation-damaged by the time the LHC reaches the end of its intended data-production period thereby requiring replacement. The layout shown in Figure 1.12 is based on one of the candidate layouts described in the Strip TDR called 'Inclined Layout' taken from reference [40]. The Inclined Layout represents a significant evolution compared to the layouts discussed in the ATLAS Phase-II Upgrade Letter of Intent [39] and in the Phase-II Upgrade Scoping document [41]. Like the reference detector layout from the Phase-II Upgrade Scoping document, the detector design presented in the Strip TDR combines precision central tracking in the presence of an average of 200 pile-up events with the ability to extend the tracking coverage to a pseudorapidity of 4 while maintaining excellent tracking efficiency and performance. The ITk comprises two subsystems: A Strip Detector surrounding a Pixel Detector. The Strip Detector has four barrel layers and six endcap petal-design disks, having modules on both sides of each layer

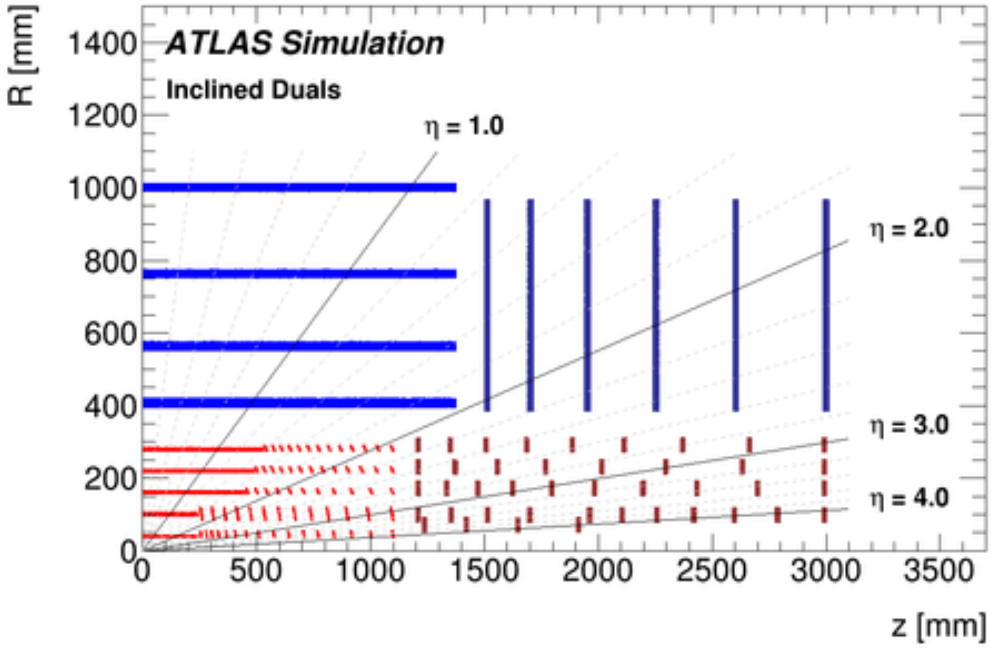


Figure 1.12: Schematic layout of the ITk for the HL (High luminosity)-LHC phase of ATLAS as presented in the Strip TDR [40]. The active elements of the barrel and endcap Strip Detector are shown in blue, for the Pixel Detector the sensors are shown in red for the barrel layers and in dark red for the endcap rings. Here only one quadrant and only active detector elements are shown. The horizontal axis is the axis along the beam line with zero being the interaction point. The vertical axis is the radius measured from the interaction region. The outer radius is set by the inner radius of the barrel cryostat that houses the solenoid and the electromagnetic calorimeter.

with a small stereo angle between the strip orientation to add z (R) resolution in the barrel (endcaps), respectively. The Strip Detector, covering $|\eta| < 2.7$, is complemented by a 5 layer Pixel Detector extending the coverage to $|\eta| < 4$. The Pixel Detector comprises 5 barrel layers and multiple forward disks. The Pixel and Strip Detector volumes are separated by a Pixel Support Tube (PST). In addition, and because of the harsh radiation environment expected for the HL-LHC, the inner two layers of the Pixel Detector are replaceable. The inner two pixel layers are separated from the outer three layers by an Inner Support Tube (IST), that facilitates a replacement of the inner layers. The combined Strip plus Pixel Detectors provide a total of 13 hits for $|\eta| < 2.7$, with the exception of the barrel/endcap transition of the Strip Detector, where the hit count is 11 hits. The Pixel Detector presented in the Strip TDR was designed to supply a minimum of at least 13 hits from the end of the strip coverage in pseudorapidity to $|\eta|$ of 4. While the Strip Detector remains unchanged and is described in detail in reference [40], the Pixel Detector layout has evolved to further improve the performance, reduce cost and incorporate engineering constraints. With the increase in the instantaneous luminosity to 7 x 10^{34} $\mathrm{cm}^{-2}\mathrm{s}^{-1}$, 2.5-3.5 times larger compared to the end of Phase-1, the pile-up also increases at the same rate and hence pile-up mitigation becomes

important to maintain detector performance. Pile-up results in mis-association of the tracks from other collisions making it worse for the jet energy measurement [42]. Pile-up could also occur due to low or uncorrected detector response from particles of the previous bunch crossings. Some of the techniques that are looked into to mitigate the pile up issue [43] are high granularity and thin sensor active region, increase in the number of the tracking layers, removing hits coming from low-pT particles by using the hit pattern in the silicon tracker, and precise timing information to reject out-of-time pile-up.

Chapter 2

Methods and Techniques

This chapter covers the methods and techniques that were used for the characterisation and testing of the designs for both ATLAS and the LHCb upgrades that are in the scope of the report. With the requirement to readout data at a faster rate of the order of Gb/s, high speed data transmission is required which in turn calls for signal integrity. Signal Integrity (SI) is a set of measures of the quality of an electrical signal. In digital electronics, a stream of binary values is represented by a voltage (or current) waveform. However, digital signals are fundamentally analogue in nature, and all signals are subject to effects such as noise, distortion, and loss. Over short distances and at low bit rates, a simple conductor can transmit a signal with sufficient quality but high bit rates and over longer distances or through different mediums, various factors can degrade the electrical signal to the point where errors occur and the system or device fails. Characterising the high-speed transmission properties of the lines such as the signal losses over the length of transmission, the crosstalk between adjacent lines, the impedance over length, eye diagram and the bit error rate are required to understand the signal performance. It is essential to address the factors that contribute toward signal interference or degradation because their cumulative effect significantly decreases the stability and reliability of high-speed design. Steps to mitigate signal interference or degradation like impedance matching, reducing electromagnetic interference, minimising the effect of propagation delay, reducing crosstalk etc., are discussed in Section 2.1. Considering design techniques that ease the manufacturability and testability of the boards is also equally important and is described in Section 2.3. Analysing data by reading S-parameters (discussed in Section 2.2) and eye diagrams (discussed in Section 2.6) and a Continuous Time Linear Equalisation (CTLE) filter for improving signal quality at high frequencies is covered in Section 2.5. Section 2.4 describes the laboratory setup along with the equipment used for carrying out the high-speed link measurements.

2.1 Sources of Signal Degradation and Mitigation techniques

Signal integrity is important at high speed as, with an increase in the frequency, the signal is more prone to degradation due to various factors like the Printed Circuit Board (PCB) material, the design techniques or the environment in which the electronics operates. This section addresses some of the main sources of signal degradation and mitigation techniques that can be followed to reduce or avoid the degradation of the signal quality. Some of these factors and techniques are explained in detail and are ones that were studied and measures applied in most of the PCBs designed.

Impedance Mismatch : Changes in the impedance of a signal path cause reflections, ringing and distortion. The extent of the interference is more pronounced with the higher frequencies associated with digital circuits. Every trace on a PCB has its characteristic impedance that is influenced by its geometry and dielectric surroundings. Any change in this impedance causes impedance mismatch and reflection. Changes in PCB trace widths, PCB trace branches, line stubs, connector pins and vias that connect a signal to different layers all create impedance discontinuities. Due to impedance mismatch, part of the signal is reflected back to the source and could build up constructively/destructively causing overshoot/undershoot and the resulting ringing.

Impedance matching : This is a technique of trying to match the load impedance to the source impedance to ensure that maximum power is delivered to the load. In order to avoid mismatch, termination schemes [44] such as series termination, parallel termination, AC termination etc. can be used at the source or the load. Impedance mismatch can also be reduced by choosing of the right PCB material. The dielectric constant of the PCB material plays an important role in the signal integrity and impedance of signals on the PCB. For high frequency applications, material with a stable dielectric constant over a broad range of frequencies is ideal. Using material with a lower dielectric constant between layers that need to be tightly coupling like a signal layer to its related reference plane will help in minimising noise and improving signal quality. Loss tangent or dissipation factor is a measure of the signal loss as the signal propagates down the transmission line on the PCB. Hence material with lower loss tangent is a better choice for higher frequencies. PCB techniques like maintaining uniform trace widths and keeping the trace lengths short, continuous reference planes for high speed signals, avoiding stubs etc. can be followed to avoid impedance mismatch.
A discontinuity is a feature that causes a change in impedance of the traveling signal. If the trace width reduces, its surface area on the PCB will reduce and the impedance will increase and vice versa. Keeping trace lengths short exposes the signal to less noise and interference

from nearby signals and is one of the general layout guidelines for traces on a PCB.
The return path of a signal travels the path of least impedance and hence high speed signals have to be coupled to the reference plane adjacent to the signal layer so there is a shortest path for the return current. Adding a ground return path also keep unwanted currents from forming in parts of the circuit where they are undesirable. Providing ground return vias and ground return paths for all of the signals especially high-speed switching signals near to the signal traces aids a short return current path. Routing signals over its assigned reference and avoiding signals switching between planes is a good design practice to avoid impedance mismatch.
In a multilayer PCB, a signal traveling from one layer to another, could give rise to a discontinuity. This discontinuity could arise when a signal travels between layers through a via [1] that in turn can result in impedance variation. The via structure on a PCB is as shown in Figure 2.1. In the via structure, the current flows from one conductor to another on the two

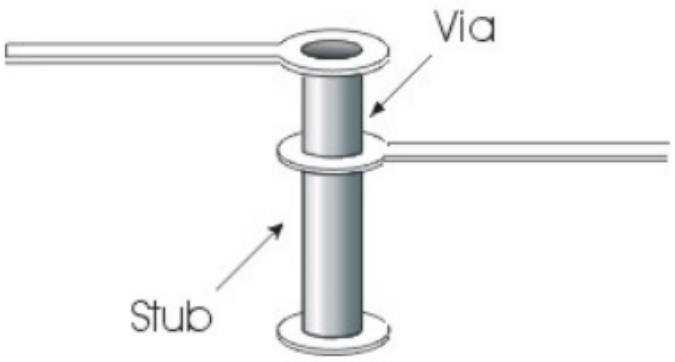


Figure 2.1: Structure of a via showing the stub feature in via. Image reproduced from [45].

layers where the signal has to travel. The conductor below this path, acts like an unterminated transmission line (antenna) and is called a 'stub'. The stub is a cause of discontinuities and degrades the signal quality more then the via itself. If the via length is small then the effect of the discontinuity is less prominent. Stubs are unwanted features on the PCB and can be removed by using a technique called 'back drilling'. The via hole is drilled slightly larger than the finished via hole to take away the unwanted copper plating as shown in Figure 2.2. Back-drilling also reduces resonance which in turn reduces signal attenuation and also reduces crosstalk between vias.

Crosstalk : This is the effect of a signal on its neighbouring signal. The rapid changes in voltage and current induce voltages in adjacent traces due to inductive and capacitive coupling. The closer the signal paths are laid out the greater the effect of crosstalk seen on

[1] A via consists of two pads in corresponding positions on different layers of the board, that are electrically connected by a plated hole through the PCB.

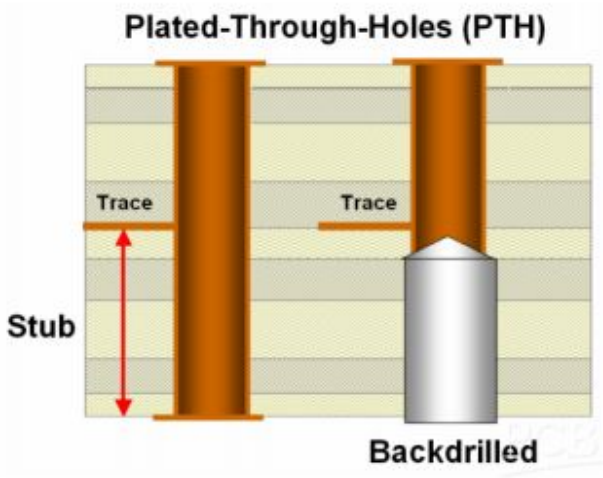


Figure 2.2: Back drilling of a via. It is a technique in fabrication that is used to improve impedance matching by reducing reflections due to stubs that act as unterminated transmission lines. Image reproduced from [46].

the neighbouring signal. There are two types of crosstalk, Near-end crosstalk (NEXT) and Far-end crosstalk (FEXT). NEXT is the effect a signal might experience from a nearby signal on the same end of the circuit. FEXT is effect from a neighboring signal, but on the opposite end of the circuit.

Avoiding Crosstalk : Using a differential signalling scheme helps avoid crosstalk. PCB design rules such as separating traces that are likely to interfere by using ground traces in between them or adding continuous ground planes between signal layers that will also provide the required return path for the signals, have to be implemented to control the crosstalk between signals. For designs with multiple signal layers adjacent to each other, alternate horizontal and vertical routing schemes should be followed. This reduces the chance of broadside coupling by not allowing the traces to run in parallel, one above the other.

Propagation delays : Signals that travel different distances or through different mediums do not arrive at their destination at the same time. These discrepancies, called signal skew, cause signal sampling errors, particularly at high clock frequencies. Differential signals skew could arise if the traces are not matched in length on the PCB. The mismatch in lengths results in electric fields that no longer cancel from equal and opposite currents and gives rise to common-mode noise.

Length matching : Length matching of traces is important to ensure that the signals arrive at the same time at the destination so issues like signal skew are kept to a minimum. The speed at which the signal travels depends on the medium and therefore on the dielectric

constant in case of a PCB. Switching signals between stripline[2] and microstrip[3] would mean a change in the dielectric environment and hence in the speed of the signals. For differential signals, since the output signal is the difference of the signal on the two lines, any noise tends to affect both lines identically. The output noise is negligible only if the two lines are coupled together and are matched in length. The signal speed and the propagation delay time are important factors in differential and high-speed signals where factors like timing and skew are critical.

Attenuation : The amplitude of a signal is attenuated by the resistance of PCB traces (conductor loss) and the dielectric properties (dielectric loss) [47] in the signal transmission. For typical PCB materials, conductor losses increase as the square root of frequency, while dielectric losses increase linearly, making dielectric loss more prominent at high frequencies. At low frequencies, conductor loss exceeds dielectric loss; dielectric loss increases at a higher rate than conductor loss and predominate above 1.1 GHz for a stripline environment as shown in Figure 2.3. The frequency at which the dielectric loss starts to dominate the conductor loss depends on the material type and the dielectric environment.

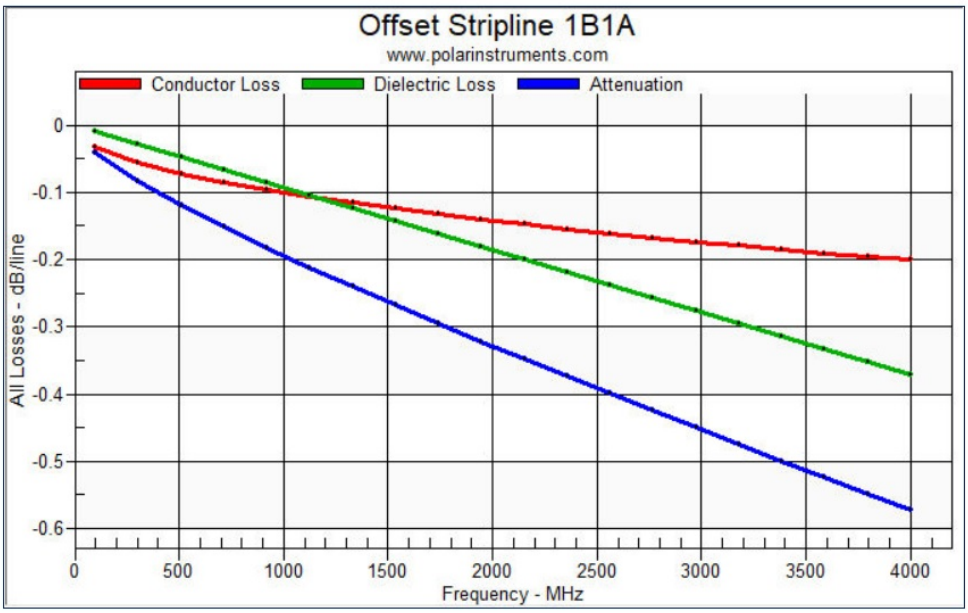


Figure 2.3: Plot showing the effect of conductor and dielectric loss as a factor of frequencies. Image reproduced from [48].

Conductor loss: This is the loss in a conductor due to a flow of current through it. At high frequencies, the skin effect is prominent due to the skin depth being less than the conductor thickness. Skin effect losses occur when current is concentrated at the surface of the

[2]Stripline is a transmission line trace surrounded by dielectric material constructed between two ground planes on internal layers of a PCB.

[3]Microstrip is a transmission line trace routed on an external layer of the board thus it is separated from a single ground plane by a dielectric material.

conductor, thereby reducing the overall area and increasing resistance. One solution is to increase the width of the traces to give more surface area but this is not always possible due to density of the PCB layout and controlled impedance requirements. The PCB material has a structure wherein the dielectric core material is bonded to the copper foil and in order to achieve a good bond the copper is intentionally roughened. The challenge is to improve the conductor loss and hence better electrical performance while ensuring good dielectric adhesion. This is addressed by using materials that have a smoother copper finish, that are 'weave-free' all-polyimide profile that provide a smoother surface and homogeneous medium for improved signal quality.

Dielectric loss: This is the loss in the signal quality due to the properties of the dielectric material [49]. Dielectric constant is the measure of the ability of a material to store electrostatic energy. It is also a measure of the degree to which an electromagnetic wave is slowed down as it travels through the material; the higher the dielectric constant, the slower a signal travels along a transmission line. For most PCB materials the value ranges from 2.5 to 4.5. The dielectric constant varies with frequency and generally decreases as frequency increases. At high frequencies, choosing materials with a flat frequency response helps in better signal propagation.

Loss Tangent: This is also an important parameter to be considered in the material selection process and it is a measure of losses when a material releases the stored energy. A lower loss tangent means less of the signal is absorbed by the material composition. Most PCB materials range from 0.02for most commonly used materials to 0.001 for very low-loss high-end materials. Loss tangent also varies with frequency and increases as the frequency increases. Using isotropic (properties of a material are the same in all directions) material over woven fiberglass is a good option when choosing material for high frequency signal transmission. Isotropic PCB materials help reduce signal integrity issues like signal distortion and attenuation.

Attenuation is also important when there are interconnecting PCBs made of different material. Interconnects cause the signal to move to different mediums thereby causing signal distortion.

Reducing attenuation : Attenuation can be reduced on PCBs by selecting materials with low dielectric loss and low profile copper. These materials also have a smooth copper surface that reduces the skin effect and allows a signal to flow through the thickness of the trace and not only on the surface thereby reducing the resistance to the signal. Materials with thick copper-clad laminates can also be used that allow to use wider traces on the PCB for the same required characteristic.

Electromagnetic Interference (EMI) : EMI is an electromagnetic emission that causes a disturbance in another electrical device. EMI can be caused by direct physical contact

with a conductor, called conducted EMI, or by induction, called radiated EMI. This effect increases with high frequencies and can induce noise and degrade signal quality.

Electromagnetic Compatibility (EMC) : EMC [50] implies following techniques in PCB design to reduce electromagnetic interference. Keeping the clock frequencies as low as possible and rising edges as slow as possible, spacing sensitive signals at a distance from the clock and avoiding loops in the clock are some of the rules to follow for the high-speed clock signals. In addition, routing high-speed signals in stripline (on an inner layer) with continuous ground reference is preferred. Good grounding and shielding techniques help to keep the EMI low and maintain signal quality.

Understanding the sources of signal degradation and ways to mitigate the same is an important step in high-speed designs before starting the PCB layout. Once the design is done and the hardware is ready, measurements have to be performed to test the signal quality in order to perform post-layout simulations. As we approach high frequencies in electrical systems it is helpful to describe signals in terms of waves rather than voltage or current via S-parameters to describe such networks using power waves.

2.2 S-parameters

S-parameter [51, 52] or Scattering parameters (part of a S-matrix or Scattering-matrix) are used to describe the electrical behavior of linear electrical networks when undergoing various steady state stimuli by electrical signals. At high-speed a transmission line is not an ideal one but would see discontinuities and attenuation along its path. The voltage or current in a electrical network would see these factors affecting it as it traverses along the transmission line thereby in some way scattering the signal and affecting the ports around it. S-matrix gives an understanding of the effect on a signal on a incident port as it propagates to the receiving port and also the effect of the signal on the neighbouring ports in terms of crosstalk induced. The S-parameters are a mathematical construction that quantifies how RF energy propagates through a multi-port network. These measurements are made as a function of frequency hence the S-matrix is a frequency dependent quantity. There are a few terms that need to be defined to get a better understanding of what each of the S-parameters means. The S-matrix for an N-port circuit contains N^2 coefficients (S-parameters), each one representing a possible input-output path.

S-parameters are usually displayed in a matrix format, with the number of rows and columns equal to the number of ports. A two port network can be depicted as shown in Figure 2.4. The variable a_i represents a wave incident to port i and the variable b_j represents a wave reflected from port j. If we assume that each port is terminated in the reference

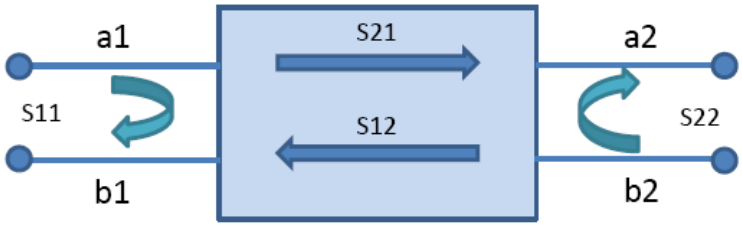


Figure 2.4: S-parameter for a two port network.

impedance Z0, we can define the four S-parameters of the 2-port as

$$\begin{aligned} S_{11} &= b_1/a_1 \\ S_{12} &= b_1/a_2 \\ S_{21} &= b_2/a_1 \\ S_{22} &= b_2/a_2 \end{aligned} \tag{2.1}$$

Parameters along the diagonal of the S-matrix are referred to as reflection coefficients because they only refer to what happens at a single port, while off-diagonal S-parameters are referred to as transmission coefficients, because they refer to what happens at one port when it is excited by a signal incident at another port. The S-matrices for a two and a four port network can be expressed as

$$\begin{pmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{pmatrix} \quad \begin{pmatrix} S_{11} & S_{12} & S_{13} & S_{14} \\ S_{21} & S_{22} & S_{23} & S_{24} \\ S_{31} & S_{32} & S_{33} & S_{34} \\ S_{41} & S_{42} & S_{43} & S_{44} \end{pmatrix}.$$

For measuring S_{11}, we inject a signal at port one (a_1) and measure its reflected signal (b_1). In this case, no signal is injected into port 2, so $a_2 = 0$; for almost all laboratory S-parameter measurements, we only inject one signal at a time. To measure S_{21}, we inject a signal at port one (a_1), and measure the signal power exiting port two (b_2) and so on for the other ports. The losses of the system are described in terms of their decibel loss (dB) which can be expressed as

$$Loss[\text{dB}] = -10 \cdot log10(P_{out}/P_{in}) \tag{2.2}$$

where P_{out} and P_{in} are the output and input power respectively. The input and output voltage, are measured to get this power. As power is proportional to voltage squared, we can

write equation 2.2 as

$$Loss[\text{dB}] = -20 \cdot log10(\text{V}_{\text{out}}/\text{V}_{\text{in}}). \tag{2.3}$$

The S-parameter matrix and the equations described above are used to evaluate the network under test and quantify the losses. We then need to understand these losses in detail, the causes and the corrective measures to be taken to reduce them if they are beyond the acceptable range at the frequency of interest.

The S-matrix can be transformed into a pseudo-TDR (Time Domain Reflectometer) measurement to get a more physical representation of the losses. A variant of the inverse Fast Fourier Transform (FFT) provides a method for transforming frequency domain data from the Vector Network Analyser (VNA) into the time domain. A TDR analysis involves propagating a signal into a system and observing the reflected signal by the system. By analyzing the magnitude, duration and shape of the reflected waveform, the nature of the impedance variation in the transmission system can be determined. The time domain results help to determine the location of impedance discontinuities in the network so corrective measures can be applied.

2.3 Design for Manufacturing (DFM) / Design for Testing (DFT)

DFM/DFT are engineering practices that are followed during product design in order to ease the manufacturing or testing process. Implementing these processes in the design phase of the projects can help optimise the design and also reduce the cost. This has to be done in close interaction with the manufacturing industry to explain the design requirement and understand their capabilities. DFM helps address factors that may affect the manufacturability such as the type and quality of raw material, dimensional tolerances and feature sizes as well as finish of the material. Addressing these factors at the design phase helps reduce the manufacturing cost that is a major cost in the product design. In the case of the PCB industry, DFM also comprises set of design rules to be followed that creates a design that eases manufacturability. As the industries are constantly evolving and new technologies for manufacturability are being developed, the DFM guidelines update accordingly and are more focused to fabricate complex and high density designs.
DFT defines techniques to be followed to ease the testability of the product designed. These need to be implemented at the design phase based on the testing requirements for the product. In case of PCBs, this implies adding testpoint on the PCB for automatic In Circuit

Test (ICT) fixtures, JTAG[4]-boundary scan or visual inspection (manual or machine). Test coupons on the same panel as the design can be made with test features to check Cu thickness, via plating, high voltage tolerances, current tolerance etc.

Various PCBs were designed as described in the thesis for both the ATLAS Upgrade and the LHCb VELO Upgrade projects. These were new designs that were taken from prototype to production and test boards to test functionality of the Device Under Test (DUT). DFM/ DFT techniques were discussed and evaluated at early stages and implemented considering the scope and requirements of the design.

2.4 Laboratory setup for S-parameter measurements.

High-speed signal transmission tests were carried out on PCBs based on the requirements and these are described in different sections of the report. The bench top laboratory setup for testing consists of a 13.5 GHz Keysight N5231A PNA-L Network Analyser[5] to measure the S-parameters. The network analyser data can be read out on Keysight's 2015 Physical Test Layer Software (PLTS)[6] for further analysis. A 13.5 GHz Keysight DSA91304A Digital Signal Analyser[7] for measuring the eye parameters and a Keysight N4903B J-BERT[8] is used that is capable of producing the required high-speed patterns and measuring the Bit Error Rate (BER). The network analyser comes with a Keysight N4431B Electronic Calibration Kit that is used to calibrate the device to remove the effects of the analyser and cables attached to the device under test (DUT). Cables built with air dielectric adapters, 3.5 mm in diameter, are used in order to reduce measurement errors from thermal expansion of the insulating material. The calibration kit is able to remove the effect of the network analyser and the cables which are 1 m in length. In addition there were test PCBs designed to interface the cables to the DUT. These test PCBs were identical or different depending on the interface of the DUT at the port under test. The PLTS has a feature called Automatic Fixture Removal (AFR). The process involves measuring the full link with the fixture. Then the DUT is disconnected from the fixtures and the AFR is run that corrects the measurement by removing the effect of the fixtures. This feature does a set of open and through measurements to remove the effect of the fixtures thereby allowing to analyse the measurement only of the DUT. Once a measurement is carried out and the raw file is saved, the PLTS allows the analysis of this data as single ended or differential mode in both frequency and time domain. The S-parameters can be exported in touchstone files or ASCII text file, which is a format that many programs can read for further analysis.

[4]named after the Joint Test Action Group formed in the 80's to develop a method of verifying designs and testing PCBs after manufacture.

[5]`https://literature.cdn.keysight.com/litweb/pdf/N5235-90004.pdf?id=2755232`

[6]`https://literature.cdn.keysight.com/litweb/pdf/5992-3233EN.pdf?id=3005532`

[7]`https://literature.cdn.keysight.com/litweb/pdf/5989-7819EN.pdf?id=1364807`

[8]`https://literature.cdn.keysight.com/litweb/pdf/5990-3217EN.pdf?id=1876866`

2.5 Continuous Time Linear Equalisation (CTLE)

At high-speed signal transmissions, signal distortion becomes an important factor as the signal travels from the source to the receiver due to various factors in the transmission path. The material in which the signal travels, crosstalk with nearby noisy signals, material change due to interconnects, reflections etc. are some of the factors causing signal distortion. These factors are addressed using PCB layout techniques, some of which are described in section 2.1. One of the important effects that needs to be addressed for high-speed serial transmission links is Inter Symbol Interference (ISI). One or more symbols interfere with the adjacent ones resulting in signal distortion. The main cause of this is the bandwidth limitation [53] and the inherent frequency response of the channel. The bandwidth limitation basically filters the signal beyond the cutoff frequency[9]. Passing the signal through such a channel, changes the shape of the signal in comparison to the signal sent over the time period and also causes it to spread and interfere with the next symbols. This results in distorted signals at the receiver that degrades the performance of the system depicted by a closed eye diagram[10] and a higher BER.

A possible solution is to use an equaliser (active or passive) designed to suppress the low frequencies and pass the high frequencies of the channel. The principle of the Continuous Time Linear Equaliser (CTLE) [54] is explained in Figure 2.5. CTLE can be purely passive or can be active with an amplifier to provide gain. Passive structures offer excellent linearity, but no gain at the Nyquist[11] frequency. It opens up the eye but reduces the overall voltage swing and is also susceptible to component-to-component variation and stray capacitances on the PCB. Active CTLE has an input amplifier that have a gain response peaking at Nyquist frequency. This is a powered circuit with transistors that needs to be built as a separate circuit block to be added on the existing PCB or as a separate daughter card to the channel under consideration.

A decision on using a passive CTLE for the LHCb VELO with discrete components was made as it was considered to be an effective solution that involved changes in the layout to add the circuit for each link but with low implications on the overall project timeliness. The values obtained in designing the circuit are used to aid the general description of the process of designing a CTLE system. The schematic of the passive CTLE built with discrete components is as shown in Figure 2.6.

[9] Cutoff frequency is a boundary in a system's frequency response at which energy flowing through the system begins to be reduced (attenuated or reflected) rather than passing through.

[10] An eye diagram is an oscilloscope display where a digital signal from a receiver is repetitively sampled and applied to the vertical input while the data rate is used to trigger the horizontal scale.

[11] The Nyquist frequency is half of the sampling rate of a discrete signal processing system.

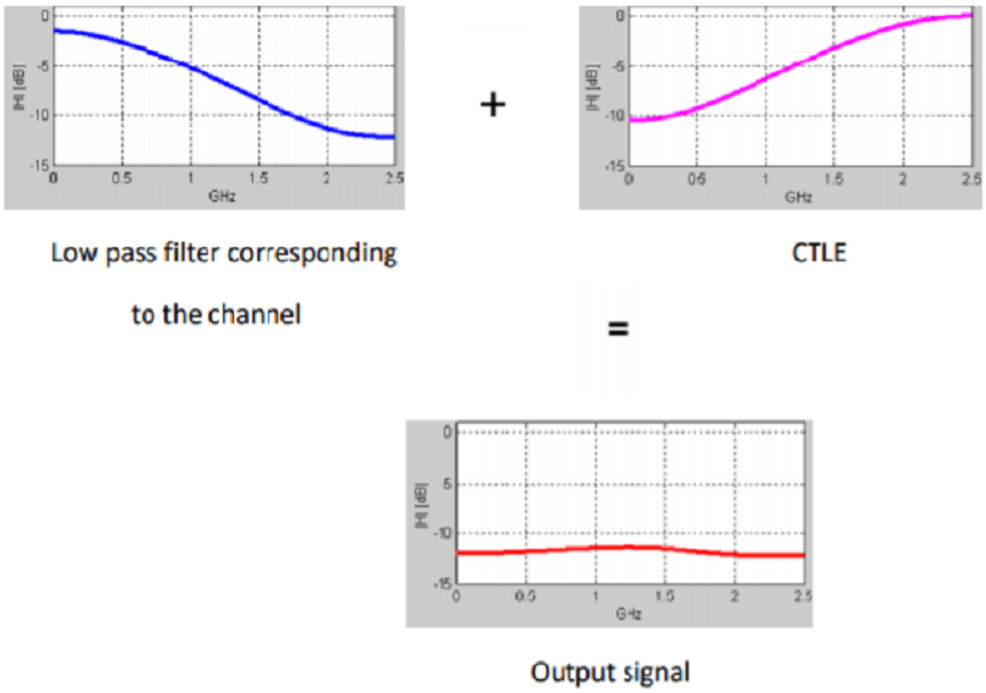


Figure 2.5: Top left - Low pass channel response. Top Right - Continuous Time Linear Equaliser (CTLE) response. Bottom - Combined response of the low pass channel and the CTLE. Image reproduced from [55].

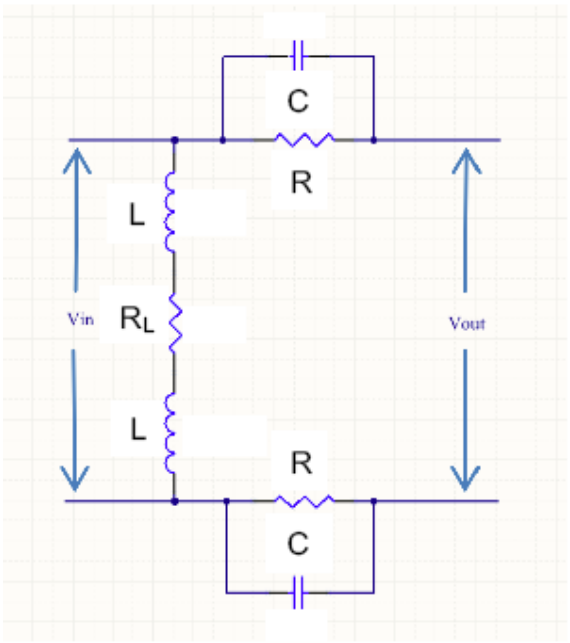


Figure 2.6: Schematic of the passive CTLE with discrete components. Image reproduced from [56].

The transfer function for the passive CTLE for the differential signals is given as

$$H(j\omega, R, C) = \frac{1 + j\omega RC}{1 + \frac{2R}{R_T} + j\omega RC} \tag{2.4}$$

where R and C are the resistance and capacitance values of the CTLE circuit, R_T is the line termination resistor (typically 100 Ω) and ω is the angular frequency. The component values for resistors (R) and capacitors (C) of the CTLE network are tuned to compensate for the frequency response of the link. The inverse of the transfer function is fitted to the S-parameter for transmission (S_{12} or S_{21}) using an analysis software to get the values for the components as shown in Figure 2.7.

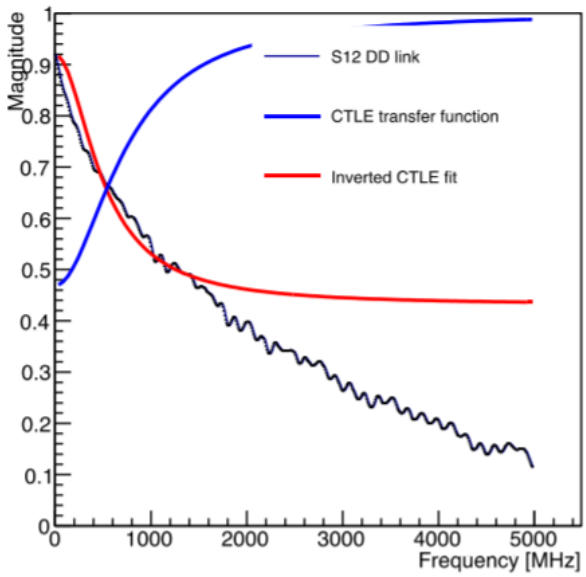


Figure 2.7: The inverse of the transfer function $H(j\omega, R, C)$ fitted to the S_{12} response to attain the values of the passive CTLE components. The plot fit is up to 2 GHz. Credit to Prof. Lars Eklund, University of Glasgow.

The input impedance of the CTLE circuit Z_C without the L-R-L network can be expressed as

$$Z_C = \frac{2R + R_T + j\omega R_T RC}{1 + j\omega RC} \tag{2.5}$$

where R_T is the input impedance of the GigaBit Laser Driver (GBLD). The values for R_L and L are chosen to give a matched impedance for all values of ω and are given by

$$\begin{aligned} R_L &= R_T + \frac{{R_T}^2}{2R} \\ L &= \frac{R_T^2 C}{2} \end{aligned} \tag{2.6}$$

The values for these components, together with the parameters of the CTLE are given in Table 2.1.

On the OPB, this CTLE is implemented at the receiving end of the data signals at the input of the VTTx's. For the control signals, the same passive network is implemented at

Component	Data link	Control link
R	100 Ω	88 Ω
C	2.2 pF	2.7 pF
R_L	150 Ω	161 Ω
2 X L	11 nH	13.5 nH
Zero f_z	0.719 GHz	0.724 GHz
Pole f_p	1.9 GHz	2.17 GHz
DC Gain	0.38 (-8.4 dB)	0.33 (-9.5 dB)
Gain @ 2.5 GHz	0.83 (-1.6 dB)	0.79 (-2.1 dB)

Table 2.1: Values for the passive CTLE components and the parameters of the filter.f_p and f_z are the pole and zero of the transfer function. Table reproduced from [56].

the sending end for the downlink (to the front-end hybrid) at the output of the GBLD chip. For the uplink the same circuit is on the hybrid side. Since the CTLE for the control links is located on the sending end of the link, the L-R-L circuit to adjust the input impedance is not needed. However, a series capacitance is required to AC couple the control links. There are already series capacitors on the VTTx modules hence no further AC coupling is needed for the data links. The layout for the same is shown in Figure 2.8.

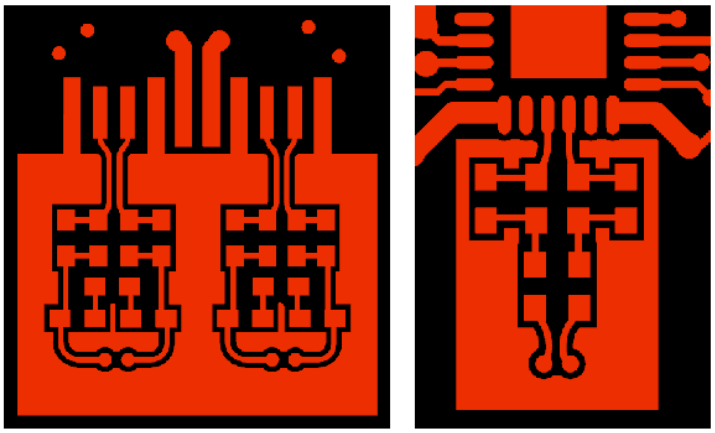


Figure 2.8: Layout of the passive CTLE as implemented on the OPB. Left - CTLE for data links and Right - CTLE for control links. Image reproduced from [56].

2.6 High-speed digital signalling and eye diagram

As described in earlier sections, high-speed signals get degraded both in amplitude and in time as they travel from the transmitting to the receiving end. Low Voltage Differential Signalling (LVDS) is used as an interface standard for high-speed digital signals as these signals travel on two lines and with tight electric and magnetic field coupling between them thereby significantly reducing the amount of electromagnetic noise. This noise reduction is

due to the equal and opposite current flow in the two wires creating equal and opposite electromagnetic fields that tend to cancel each other. As described in earlier sections, high-speed signals get degraded both in amplitude and in time as they travel from the transmitting to the receiving end. Low Voltage Differential Signalling (LVDS) is used as an interface standard for high-speed digital signals as these signals travel on two lines and with tight electric and magnetic field coupling between them thereby significantly reducing the amount of electromagnetic noise. This noise reduction is due to the equal and opposite current flow in the two wires creating equal and opposite electromagnetic fields that tend to cancel each other. At the receiver end, it is essential that the receiver clock is synchronised with the transmitter clock. Otherwise, the rising and falling slopes of the signal will gradually shift their position in the eye diagram and finally blur it. One way to avoid this is to provide the clock from the transmitter directly. This is however highly inefficient, as it requires an additional channel. The other option is to recover the clock from the data signal using some clock recovery algorithm. To recover the sampling clock, the receiver needs a reference clock of approximately same frequency as the transmitted data stream. To generate the recovered clock, the receiver needs to phase align the reference clock to the transitions on the incoming data stream. This is called clock recovery. Sampling of that incoming data signal with the recovered clock to generate a bit stream is called Data recovery. Together, they are called Clock Data Recovery (CDR). To analyse the recovered output signal in a pictorial format for ease of understanding, an eye diagram is used. It is an oscilloscope output that is a representation of the digital signal at the receiver that is repetitively sampled and applied to the vertical input, while the bit period defines the horizontal eye opening. It is called an eye diagram as for several types of data coding schemes, the pattern looks like a series of eyes between the voltage rails. Figure 2.9 shows an eye diagram highlighting the key electrical parameters of the signal to be visualized and studies to take corrective measures.

In an ideal case, digital signals in the form of '1' and '0' are expected to arrive at the receiver at a certain time and for a predetermined time period. At high-speed, various factors result these bits to be displaced in time and can be misinterpreted (a '0' for a '1' or vice versa) causing an erroneous output. One such error that arises due to timing issues is jitter. Jitter [58] occurs when rising or falling edges occur at times that differ from the ideal time. As the bit rate increases, the timing errors increase thereby reducing the size of the eye opening. There are different forms of jitter and Inter Symbol Interference (ISI) is one of the most common forms of data dependent jitter when there is bandwidth limitation on transmission lines.

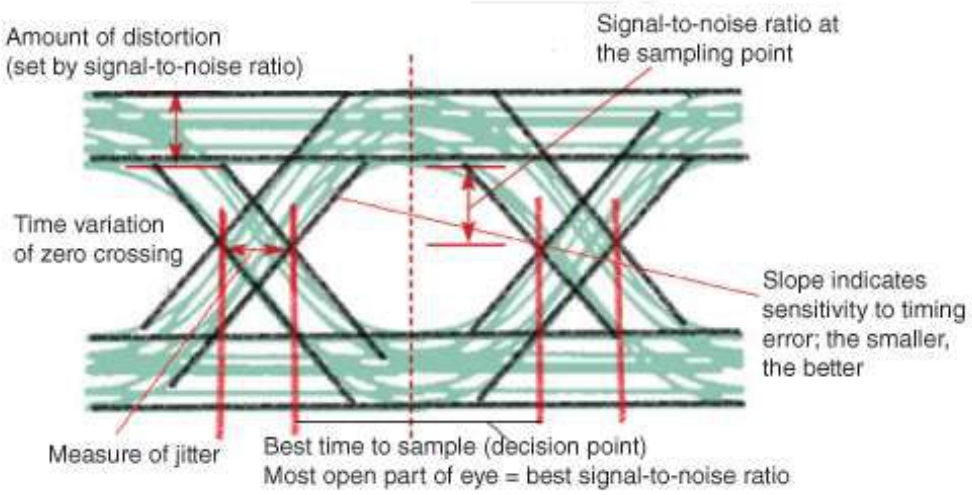


Figure 2.9: Eye diagram showing a visual representation of the key electrical parameters. Dotted red line shows the best time to sample a signal. Jitter and amplitude distortion are also highlighted. Image reproduced from [57].

Chapter 3

LHCb VELO Design

This chapter covers details of the LHCb Vertex Locator (VELO) Upgrade including the design and functionality of the various components that make up the VELO. The motivation behind the design of the On-detector electronics, the design cycle from prototype to production of the Data tapes and OPB and an overview of the off-detector readout system will be covered in this chapter.

3.1 Introduction

The VELO surrounding the interaction region of the LHCb detector is used to reconstruct primary and secondary decay vertices and measure the flight distance of long-lived particles. The upgraded LHCb VELO [16] will be installed together with the rest of the upgraded LHCb experiment during the LHC long shutdown (LS2) in 2019 - 2020. An illustration of the upgraded VELO highlighting the main components of the On-detector electronics is shown in Figure 3.1. The VELO will operate in vacuum and is designed to absorb the VELO motion. Each VELO half is retracted in the horizontal plane and is only closed once stable beam conditions are declared in order to ensure detector safety during beam injection and adjustments. The VELO is operated in secondary vacuum, separated from the beam by a thin foil in order to minimise the material traversed by the particles before their first measured point. The thermal management of the system will be provided by evaporative CO_2 cooling [24] circulating in microchannels embedded within the silicon plates. The upgraded VELO will use the custom developed VeloPix [23] front-end ASIC to read out 41 million pixels. The hit information will traverse through the On-detector components and will be read out by the PCIe40 readout system for processing.

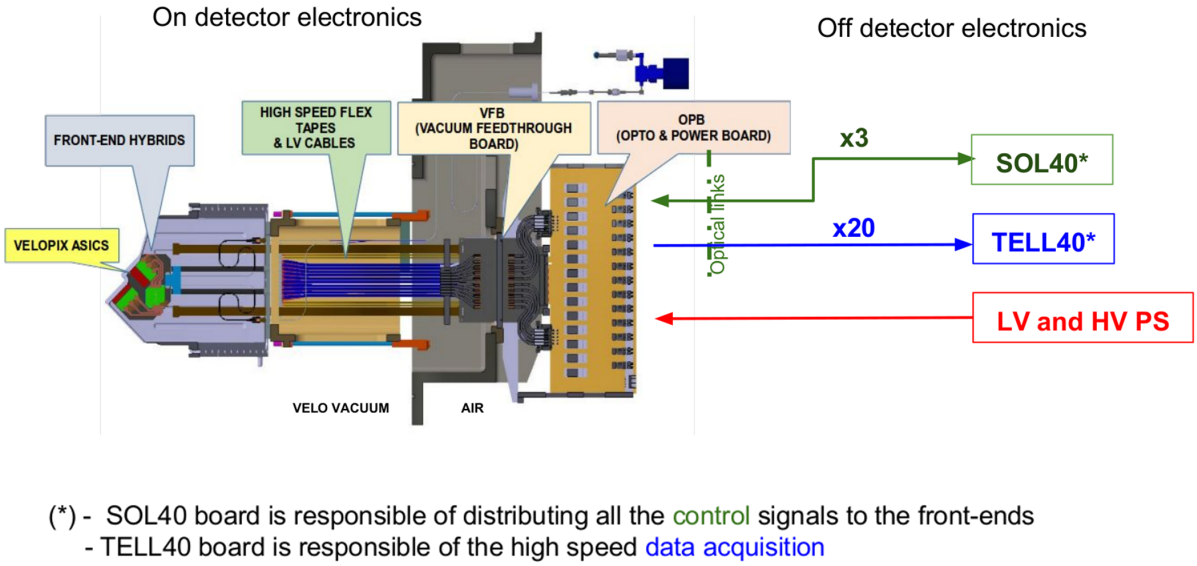


Figure 3.1: An illustration of the Upgraded VELO highlighting the module comprising VeloPix ASIC-sensor assembly and front-end hybrid mounted on the micro-channel cooling substrate, High-speed data tapes and Low voltage (LV) cables, Vacuum Feedthrough Board (VFB) and Opto and Power Board (OPB). The Off-detector electronics comprising of the SOL40, TELL40 and the Low Voltage (LV) and High Voltage (HV) Power Supply (PS) is shown. Image reproduced from [59].

3.2 On-detector electronics for the LHCb VELO Upgrade

This section will cover the various components that make up the On-detector electronics for the VELO Upgrade [60]. The designs of front-end hybrid and kapton tapes (covered in subsection 3.2.1), high-speed Data tapes (covered in subsection 3.2.2), Vacuum Feedthrough Board (covered in subsection 3.2.3) and the Opto Power Board (covered in subsection 3.2.4) will be elaborated.

3.2.1 Front-end Hybrid and Kapton Tapes

The front-end Hybrid is mounted on the VELO detector module. There are in all 52 modules, 26 on each side of the beam. Each silicon sensor is bump-bonded to a row of three VeloPix ASICs, the assembly of which forms a 'tile'. Each module is made up of 4 such tiles, 2 on each side of the micro-channel cooling substrate. The Hybrid will provide power and control signal distribution and readout signal routing to the tiles. The High Voltage (HV) goes through a separate HV kapton that is glued on directly to the back of the sensor. The VeloPix ASIC [13] is based on the TimePix3 ASIC [61] and is designed in the TSMC 130 nm CMOS process. The ASIC has data driven readout with on chip zero suppression. It has four serial outputs, each transmitting data at 5.12 Gb/s. The highest occupancy ASICs will have pixel hit rates of 900 Mhit/s and produce an output data rate of over 15 Gbit/s,

Feature	**TimePix3**	**VeloPix**
Readout	ToT	Binary
Max.Power	1W/cm^2	1.5W/cm^2
Pixel Matrix/size	256 x 256 / 55 μm x 55 μm	256 x 256 / 55 μm x 55 μm
Hit Rate	80 Mhit/s	900 Mhit/s
Data Rate	5.12 Gbit/s	20.4 Gbit/s (4 x 5.12)
Technology	130 nm CMOS	130 nm CMOS

Table 3.1: Comparison of the key features and differences between TimePix3 and VeloPix.

adding up to 1.6 Tbit/s of data for the full VELO. The VeloPix has a 256 x 256 pixel array with each pixel grouped in smaller 4 x 2 pixel arrays known as SuperPixels. Each pixel uses Time over Threshold (ToT) to register a hit with the threshold being programmable for a SuperPixel [62]. Each SuperPixel writes a data packet if any of the 8 associated pixels register a hit. The data packet consists of an 8 bit hit map, a 9 bit time stamp and a 13 bit address. The data packets are sent in groups of four with a header (of 1010 in binary or 0xA in hexadecimal) for frame alignments and a four bit parity check resulting in a total frame size of 128 bits. These frames are sent at 40 MHz, thus the data rate of each serial data output is 5.12 Gb/s. The VeloPix has been delivered and initial tests have shown that the ASIC works to the required specifications. A comparison of the key features and difference between the TimePix3 and VeloPix chips is presented in Table 3.1 while the internal chip architecture explaining the pixels, SuperPixel packets and frames is shown in Figure 3.2.

The production front-end Hybrid assembly is made up of 3 parts; the front-end Hybrid for 3 VeloPix ASICs, the Gigabit Transceiver (GBTx) Board and the Kapton tapes. A front-end Hybrid PCB serves one tile of 3 ASICs, hence there are 4 such PCBs per module. The ASICs are bump-bonded to the sensors are wirebonded to the front-end Hybrid PCB. This PCB has a slimstack connectors that interface to the Kapton tapes that carry data signals to the long Data tapes (detailed in Section 3.2.2) and control signals to the GBTx Board. The Kapton tapes are of two types; one type carries the data from each front-end Hybrid to the long data tapes and the second type interfaces with the GBTx PCB to the front-end Hybrid. The 3 PCBs that make up the front-end Hybrid assembly are shown in Figure 3.3. The 3 parts of front-end Hybrid assembly comprises different layer stackup and material that is chosen based on the requirements of the design and manufacturing capabilities. The front-end assembly aims at having minimum copper to keep the mass as low as possible. Nevertheless, issues such as reliability of plated holes with less copper or bowing due to non uniform copper leads to a compromise on the overall copper on these PCBs. All the PCBs are made with Dupont All-Polyamide (AP)[1] laminate, flexible material rated for advanced material performance, temperature resistance, and high reliability. The front-end Hybrid

[1] `https://www.dupont.com/content/dam/dupont/products-and-services/electronic-and-electrical-materials/flexible-rigid-flex-circuit-materials/documents/PyraluxAPclad_DataSheet.pdf`

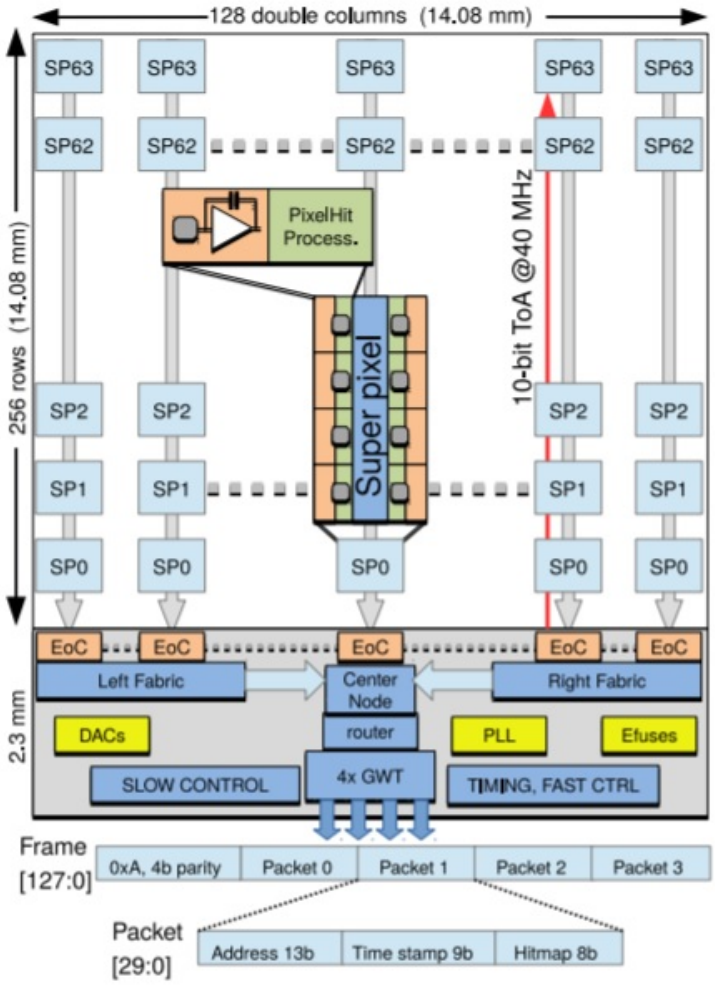


Figure 3.2: Chip architecture of the VeloPix ASIC [23].

is a 4-layer PCB built with AP8535R (Copper-clad laminate with 75 μm core and 18 μm of copper) combined with LF bondply[2] to glue on the two laminates. The GBTx board is a 4-layer PCB built with two AP8515R and a AP8545R laminate along with LF bondply combined together to optimise the requirements of the design. The 2 types of Kapton tapes are made with AP8545R, a 2-layer design with 100 μm dielectric and 18 μm of copper on each side. These tapes are designed to achieve a 100 Ω differential impedance to match to the long Data tapes to keep the signal reflection to a minimum. The front hybrid PCBs are designed by Tony Smith, University of Liverpool, fabricated in industry and are undergoing the final production run tests.

[2] https://www.dupont.com/content/dam/dupont/amer/us/en/products/ei-transformation/documents/PyraluxLFbondply_DataSheet.pdf

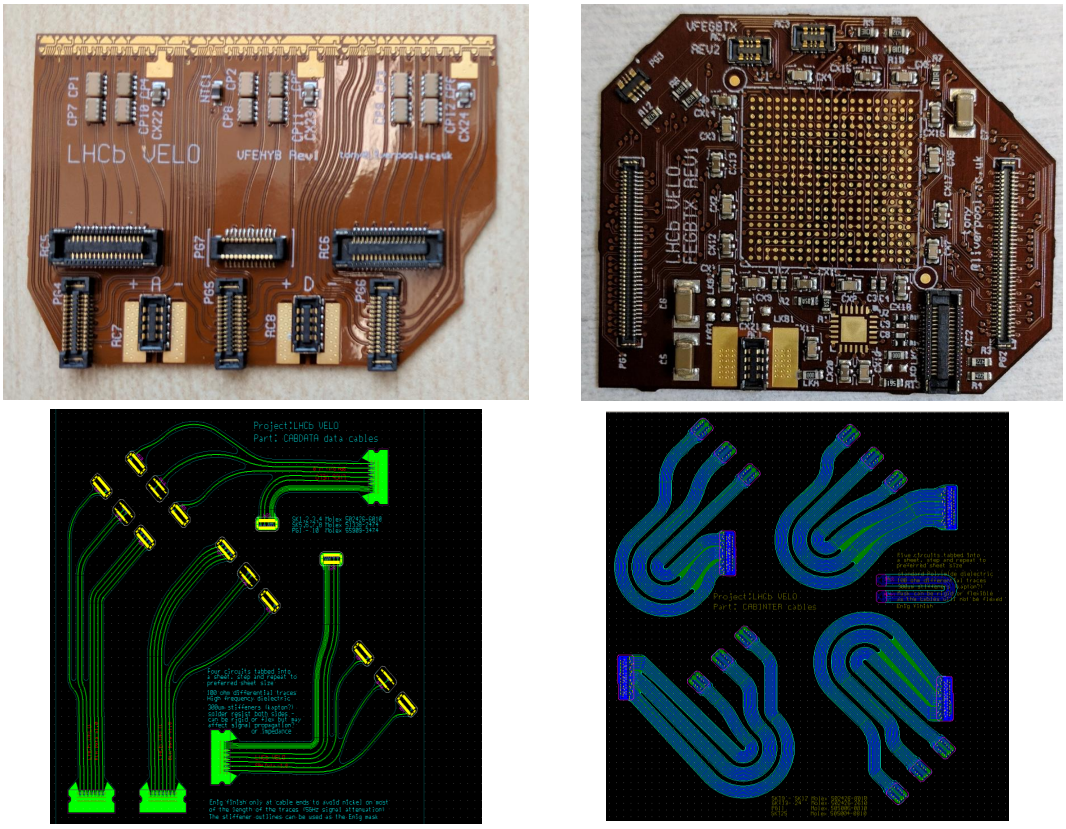


Figure 3.3: Components of the front-end Hybrid assembly. Top left - Front-end Hybrid. Top right - GBTx Board. Bottom left - Kapton tapes for the high-speed data signals to the Data tape links. Bottom right - Kapton tapes to interface the GBTx PCB to the front-end Hybrid. Credit to Tony Smith, University of Liverpool.

3.2.2 High-speed Data tapes

The front-end VeloPix ASIC gathers data from the pixels, column wise, in the End-of-Column (EoC) logic and this data from the EoC blocks are routed to the 4 output serialisers, each running at a speed of 5.12 Gbit/s. The decision not to have any optical component (lasers, diodes, fibres and optical connectors) inside the secondary vacuum has a significant impact on the architecture (detailed in 3.2.4) of the On-detector electronics. As a consequence, high-speed signals for data and control must be routed on low mass electrical cables from the modules through the vacuum wall to the Opto Power Board (OPB) located on the periphery of the vacuum tank.

The data links are implemented as low mass flex PCBs, upto 575 mm long electrical tapes carrying data at 5.12 Gb/s per link. The tapes route control and data signals between the modules to the Vacuum Feedthrough Board (VFB). The VELO has 208 tapes for 52 modules with 20 data links and 4 control links per module. In addition, the tape also carries the reset, voltage monitoring and temperature readout for the module.

The tapes have to be flexible to absorb the motion of the VELO and should be vacuum

compatible. This led to an intense investigation on the types of flexible materials available on the market that would be suitable for high-speed signal transmission in addition to the above requirements. Fabricating prototypes with a special laminate by Dupont called Pyralux AP PLUS[3] was chosen based on the study. Unlike typical PCBs that are constructed from various woven fiberglass, AP PLUS is a 'weave-free' All-Polyimide (AP) profile that provides a smoother surface and homogeneous medium for improved Signal Integrity (SI). The homogeneous dielectric core provides a consistent dielectric constant (dielectric constant (1 MHz-10 GHz) - 3.4) for controlled impedance circuit requirements. The material also provides excellent thickness stability with tolerances of $\pm$ 10%, which minimizes impedance variations on the signal lines. The copper foil is rolled-annealed, that provides a smooth surface finish and minimizes the skin effect loss (described in Section 2.1).

The longest of the tapes had to be 575 mm (the other two lengths were 561 mm and 550 mm) between the module and the VFB. The length of the tapes was critical for the fabrication as the maximum length had to be within the size of the standard sheets of the Dupont material after considering the tolerances for the tooling in the fabrication process. The assembly of the tapes was a very important consideration as the tapes had to be assembled as per standard IPC[4] specifications for assembly. The tape has two low profile connectors on each end so fitting this tape on the assembly line was the key consideration. Proper assembly using industrial standards is required for reliability for the long time the tapes would we installed in the VELO.

The four VeloPix ASICs that are surrounding the beam hole see the highest track rates and will require all four serial output links to transfer the data. The other eight ASICs that are further away from the beam need only two or one links. The detector tile closest to the beam will have 4 + 2 + 1= 7 data readout links, whereas the outermost 3 tiles will have only one link each. Each side of the module will have 10 data readout links with a total number of data links being 1040 for 52 modules. The Gigabit Transceiver (GBTx) [63] on either side of the module will have two high-speed signals each, for control signals to and from the ASIC. The GBTx uses the Giga Bit Laser Driver (GBLD) [64] as a standalone line driver on the OPB and on the front end hybrid to drive signals from VTRx's on the OPB and the GBTx ASICs on the front-end Hybrid. The GBLD, GBTx and the Slow control Adapter (SCA) [65] target High Energy Physics (HEP) applications for which radiation tolerance is mandatory. The GBLD is composed of two drivers capable of sinking up to 12 mA each from the load at a maximum data rate of 5 Gb/s, and of a current sink for the laser bias current. The laser driver also includes pre-emphasis and duty-cycle control capabilities. To improve the quality of the signal going down to the front-end Hybrid, a passive Continuous Time Linear Equalizer (CTLE) made with discrete components was implemented, for the downlink, at the output of

[3] `https://www.cirexx.com/wp-content/uploads/Pyralux_AP-Plus_DataSheet1.pdf`

[4] Institute for Interconnecting and Packaging Electronic Circuits(IPC) standards are the electronics industry adopted standards for design, PCB manufacturing, and electronic assembly.

the GBLD on the OPB. The same circuit was placed on the front-end Hybrid for the uplink to the OPB. The data links have been tested with output patterns like Pseudo-Random Binary Sequence[5](PRBS15, PRBS31) and scrambled data. The observed excess jitter on the clock in the VeloPix ASIC in combination with the frequency dependent attenuation of the flex cables causes the eye diagrams to close, thereby giving rise to a too high Bit Error Rate (BER). By introducing a Continuous Time Linear Equalizer (CTLE) circuit, similar to the control links, the BER could be improved from order 10^{-7} to 10^{-15}. The performance of the high-speed links have been studied in detail and the results are presented in Section 4.1.

The design of the tapes was focused on the signal integrity of the signals running from the module to the OPB. The signals on the tape have a data rate close to 5 Gbit/s and are differential signal pairs with Current Mode Logic (CML) electrical levels. To minimize electromagnetic interference, the traces are implemented as edge-coupled stripline, with characteristic impedance close to 100 Ω and intermediate ground guard traces between the pairs to reduce crosstalk, as shown in Figure 3.4.

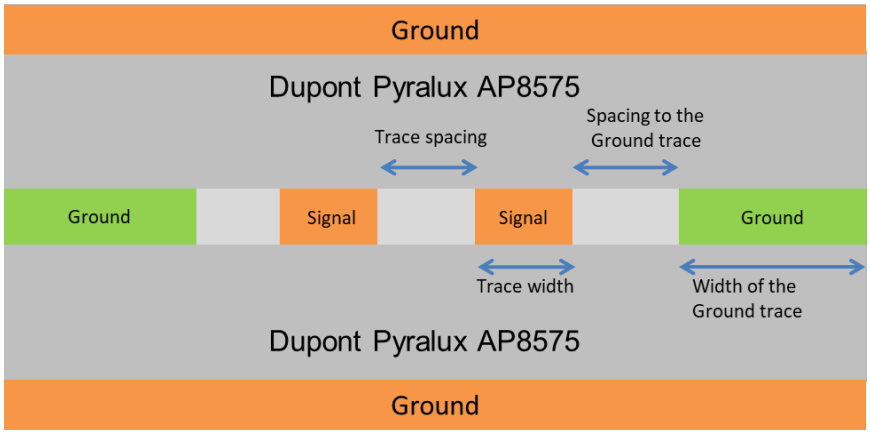


Figure 3.4: Cross-section of the Data tape design showing the 3 layers and the edge-coupled stripline traces for high-speed signals.

The layout of the prototype tapes comprised of a 3-layers flexible laminate build using Dupont Pyralux AP Plus 8575 which is an all polyamide flexible copper-clad laminate with 175 μm of kapton core and 18 μm of copper. Molex Slimstack connectors with a 400 μm pitch were used at two ends of the tape to connect to the front-end Hybrid and VFB respectively. This connector is mounted on the inner layer (of the 3-layer stackup) by removing the top layer dielectric in this region. This is not an industrial standard technique but feasible for fabrication and avoids vias on the high-speed signal traces. This was incorporated in order to test the high-speed links and to keep the signal losses to a minimum. The tape connects to the front-end Hybrid with plug 502430-6010 and to the VFB with socket 502426-6010 from

[5]A Pseudorandom Binary Sequence (PRBS) is one of the most important sequences generated which is a binary pattern that is commonly generated by a special pulse pattern generator called the PRBS generator. This finds applications in telecommunication, correlation technique and encryption, etc.

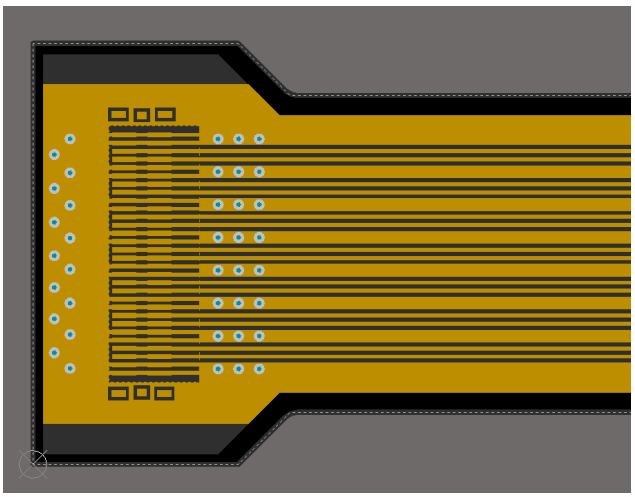


Figure 3.5: PCB layout of the data tape with trace width/trace spacing of 0.2 mm/0.2 mm. The vias around the connector are stitching vias to connect the ground planes on all the three layers together.

the Molex SlimStack range of connectors[6].

A section of the first prototype tape highlighting the high-speed layer (embedded between two ground planes) is shown in Figure 3.5. Three variants of the data tapes were designed to identify the best layout for high-speed transmission rate of 5.12 Gb/s. The inner layer is sandwiched between the top and bottom (continuous ground references) layers and carries the high-speed signals. These prototypes were fabricated at the PCB workshop at CERN. The variants were called TapeVar1, TapeVar2 and TapeVar3 and the details of the design differences is shown in Table 3.2.

Data tape variant	**Trace width**	**Trace spacing**	**Spacing of pair to adjacent ground trace**	**Width of the Ground trace between differential pair**
TapeVar1	0.2 mm	0.2 mm	0.2 mm	0.6 mm
TapeVar2	0.15 mm	0.25 mm	0.225 mm	0.6 mm
TapeVar3	0.1 mm	0.1 mm	0.35 mm	0.6 mm

Table 3.2: The intial three variants of the Data tapes with different trace width and trace spacings to determine optimal parameters for high-speed signal performance.

A Test Board was designed to interface the tape to the network analyser for measuring S-parameters. The Test Board has a molex connector (to mate to the tape) and a Samtec BAR-J-22[7] (to connect to the network analyser). The Samtec connector is a small sized 22 positions SMA connector thereby allowing to route the 7 differential pairs on a single connector. This connector is a high-density, high-performance test point array rated for

[6] https://www.molex.com/molex/products/family/slimstack_fine_pitch_smt_board_to_board_connectors

[7] https://www.samtec.com/products/bar-j-22

high-speed up to 20 GHz/40 Gbps. The layout inner layer of the test board is as shown in Figure 3.6.

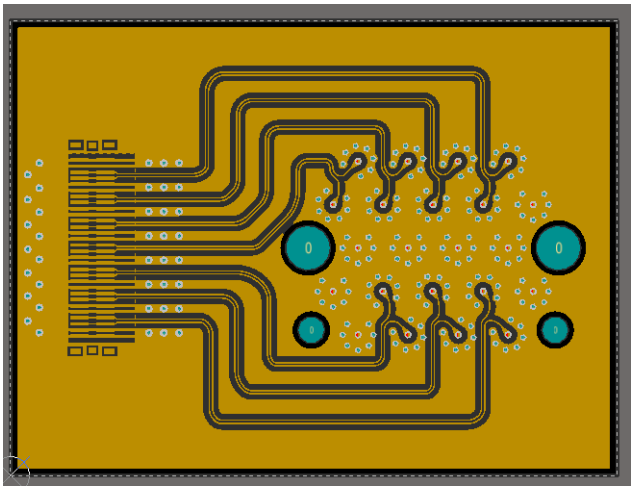


Figure 3.6: Layout of the Test Board - variant 1 highlighting the inner layer carrying the high-speed signals.

The test board was designed with a trace width/spacing of 0.1 mm/0.1 mm same as TapeVar3. The board had the same build as the tapes with an additional stiffener at the bottom side for ease of handling.

TapeVar1 showed the best performance of the three tape designed and hence the next prototype was designed using these layout specifications as the reference. Further, detailed layer stackup was built by industry (Polar calculator[8]) and by institute (Ansys Simulation[9]) to tweak the trace width/trace spacing to attain 100 Ω differential impedance.

TapeVar1.1 was built by industry with the same material and specifications as that of TapeVar1, to start the process of interacting with industry and understanding the manufacturability of the design. The connector footprint was made a dual footprint in the first prototype (TapeVar1). This was in order to be able to mount either a plug or the socket of the Molex connector. The dual footprint was not ideal for solderability and hence it was changed to individual plug and socket footprints drawn as per specified in the datasheet. It was observed that since the connector was 'embedded' on the inner layer, the assembly was not as per industrial standard and caused issues with soldering and handling the connected for multiple mating cycles.

In order to incorporate a standard design while maintaining signal quality over the length,

[8]Polar Impedance calculator does enhanced modeling to predict the finished impedance of multiple dielectric PCB builds and also takes into account the local variations in dielectric constant on close spaced differential structures. The details of the impedance calculator can be found at `https://www.polarinstruments.com/products/cits/Si8000.html`

[9]Ansys Q3D Extractor efficiently performs 3D and 2D quasi-static electromagnetic field simulations and automatically generates an equivalent SPICE sub circuit model. These highly accurate models can be used to perform signal integrity analysis. The details of the simulator can be found at `https://www.ansys.com/products/electronics/ansys-q3d-extractor`

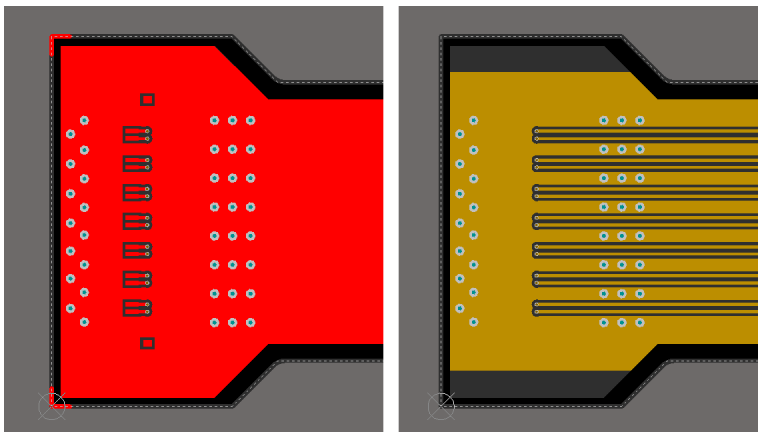


Figure 3.7: PCB Layout of TapeVar1.2. Left - Top layer and Right - Inner signal layer.

the connector was moved to the top layer and high-speed signals were routed in stripline environment using vias for connectivity. The trace width/trace spacing was modified to 0.18 mm/0.22 mm as the simulation results for impedance were similar to that with 0.2 mm/0.2 mm. This was done in order to understand the effect of this modification on the impedance and to finalise the trace width/trace spacing for the final layout. A new pinout for the connector was developed for it to be placed on top layer and also to reduces the inter pin capacitance when adjacent pins are connected to the same net. This prototype was called TapeVar1.2 and its layout is shown in Figure 3.7 showing the connector moved to the top layer and the new pinout.

The change in the layout of the connector led to a new test board for testing the tapes. Test Board-variant 2 that was in line with earlier designed test board with the difference that the BAR-J-22 connector was replaced by a CCH-J-02 connector of the same series but with 2 pins. This connector was chosen as it was identified to be easy to mount/unmount cables on it in comparison to the BAR-J-22. The ease in handling of the new connector helped in testing and hence was used in the final Test Board-variant 3. The test board variant 3 was the same as variant 2 with minor tweak in the footprint of the CCH-J-02[10] for ease of connectivity. The test board has 7 such connectors each for one high-speed data pair. The layout of this test board is shown in Figure 3.8.

High-speed link tests were conducted on the data tapes to understand the frequency response as well as to study the impedance performance over the length. The results were analysed and the final production tapes were made with trace width/trace spacing of 0.2 mm/0.2 mm. Minor changes in the ground vias, via pad size and via spacing were made to optimise the final design.

Based on the design of the overall VELO Upgrade, there were two types of tapes designed; one that carried 7 data pairs (Left Hand Side (LHS) tape) and the other that carried 3 data pairs in addition to control, reset, voltage monitoring and reset (Right Hand Side (RHS)

[10] https://www.samtec.com/products/cch-j-02

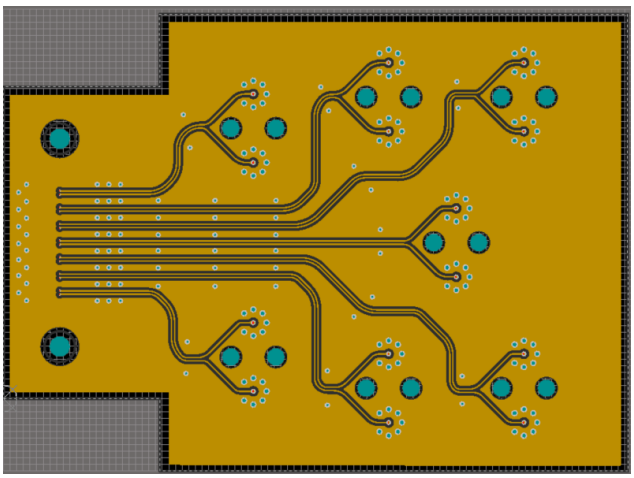


Figure 3.8: Layout of the Test board-variant 3 highlighting the inner layer carrying the high-speed signals.

tape) signals. In addition, 3 tapes lengths (575 mm, 561 mm and 550 mm) were converged upon based on the mechanics of the full system and these were designed for the production version of the tapes. The results of testing the different tape variants from prototype to production version are shown in Section 4.1.

3.2.3 Vacuum Feedthrough Board (VFB)

The Vacuum Feedthrough Board (VFB) is the interface between the high-speed data link tape and the OPB and brings the signals through the vacuum wall of the VELO. The final VFB design is integrated with the vacuum wall but the first prototype was made as a purely electrical object. The prototype VFB was interfaced to the OPB with PCIe connectors that carry the data and the low voltages. The low voltages were provided on a separate connector from that of the data (that run over Data tapes) on the front-end Hybrid side. These low voltages were distributed on the hybrid by separate cables. The component placement and the design of the prototype VFB is shown in Figure 3.9. This prototype was designed to interface with the prototype OPB to read out one tile of the front-end hybrid. It was an 8-layer PCB design with the high-speed signals routed in stripline environment. A dedicated ground layer was assigned below the high speed signal layers to provide a continuous ground return path. The layer stackup for the design is shown in Table 3.3. There were a few changes with respect to the connectors and signalling scheme of this PCB for the production board. All the modifications were done to achieve optimum mechanical stability while maintaining signal integrity for the high-speed signals.

The production VFB was designed to be a 12-layer PCB. The increase in layers was required to maintain signal integrity, proper ground referencing and accommodating all signals with minimum crossovers. Figure 3.10 shows the component placement and the design of the production VFB and the layer stackup is shown in Table 3.4.

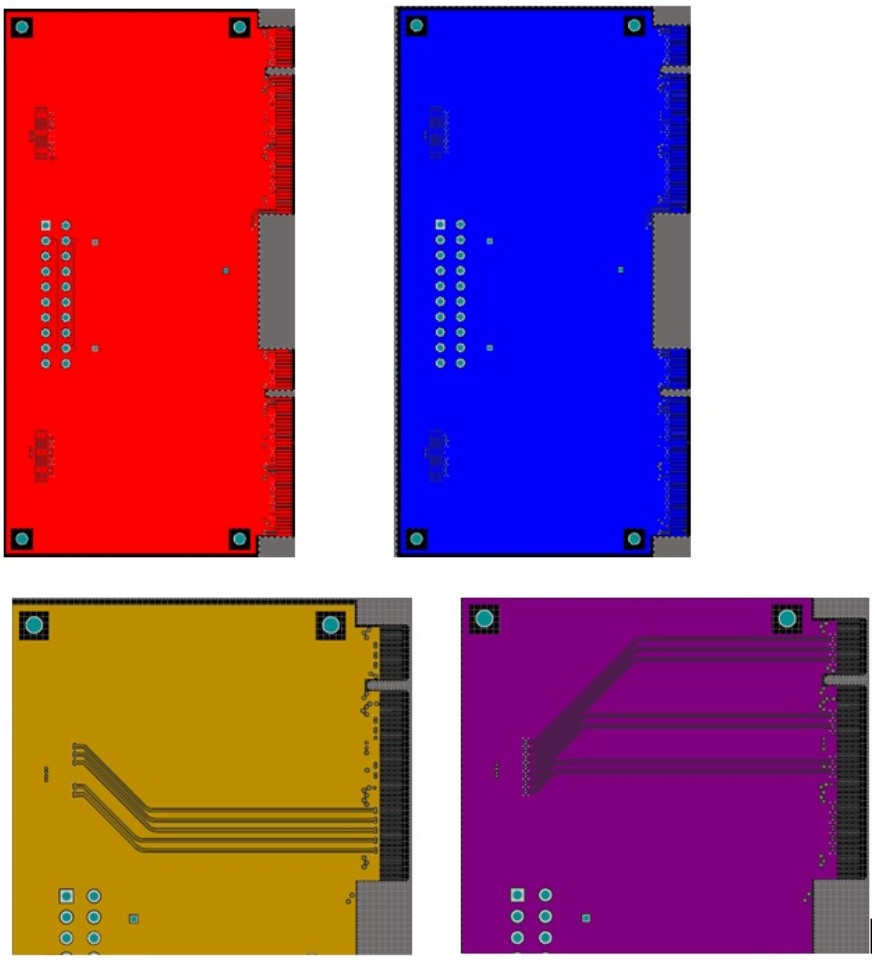


Figure 3.9: PCB layout of the prototype of the Vacuum Feedthrough Board (VFB). Top left - Top layer and Top right - Bottom layer showing the component placement. Bottom left and bottom right - High-speed signal layer in stripline environment. Credit to Leyre Flores, University of Glasgow.

Layer	Layer Assignment	Purpose
1	Top Layer	Connectors for data tapes and PCIe
2	Signal_BH	5.12 Gb/s signals for back hybrid
3	Dgnd_BH	Ground reference for back hybrid signals
4	Power_BH	Split plane for power on the back hybrid
5	Power_FH	Split plane for power on the front hybrid
6	Signal_FH	5.12 Gb/s signals for front hybrid
7	Dgnd_FH	Ground reference for back hybrid signals
8	Bottom Layer	Connectors for data tapes and PCIe

Table 3.3: PCB layer stackup for the prototype Vacuum Feedthrough Board (VFB).

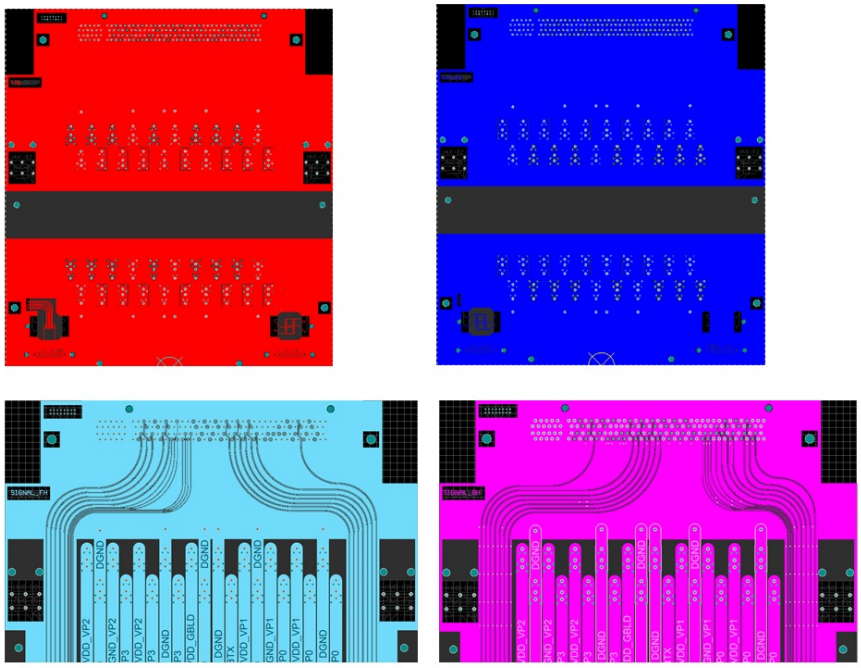


Figure 3.10: PCB layout of the production Vacuum Feedthrough Board (VFB). Top left - Top layer and Top right - Bottom layer showing the component placement. Bottom left and bottom right - High-speed signal layer in stripline environment for front and back hybrid. Credit to Jan Buytaert and Alexander Leflat, CERN.

Layer	**Layer Assignment**	**Purpose**
1	Top Layer	Connectors for data, HV and PT100
2	Dgnd_FHT	Ground reference for front hybrid signals
3	Signal_FH	5.12 Gb/s signals for back hybrid
4	Dgnd_FHB	Ground reference for front hybrid signals
5	PT100	PT100 temperature sensor signals
6	HV_SUP_F	High voltage supply front hybrid
7	HV_SUP_B	High voltage supply back hybrid
8	HV_RET	High voltage return
9	Dgnd_BHT	Ground reference for back hybrid signals
10	Signal_BH	5.12 Gb/s signals for back hybrid
11	Dgnd_BHB	Ground reference for back hybrid signals
12	Bottom Layer	Connectors for data and HV connector

Table 3.4: PCB layer stackup for the production Vacuum Feedthrough Board (VFB).

3.2.4 Opto and Power Board (OPB)

The optical components in the VELO system such as lasers, diodes, fibres and optical connectors cannot be placed inside the secondary vacuum mainly because of the difficulty of cooling these high power dissipating optical components in vacuum. Sensitivity to radiation and added overall mass in the detector acceptance are also important parameters to be considered. The electronics should also be easily accessible to allow maintenance and repair during operation. For similar reasons stated above, the DC/DC converters powering the front-end ASICs have to be moved into an accessible area outside the vacuum tank. This motivated the design of the OPB [56] that comprises all the parts that need to be outside the vacuum to operate. All the ICs have to be radiation tolerant in addition to its functionality. The radiation numbers for the VELO Upgrade are estimated at the full integrated luminosity of 50 fb^{-1} and the OPBs will receive a dose of up to 2.5 kGy. The local clock for the front-end Hybrid as well as the timing, clock and command for the ASICs is handled by the GBTx (Gigabit Tranceiver) on the Hybrid itself. The serial data and control links are carried over the flexible Data tapes that extend upto the vacuum wall where they interface to the VFB. The design of the On-detector electronics is based on the GBT chip-set and the versatile link developed for the LHC Upgrades.

The OPB connects between the VFB and the Off-detector electronics and its main functions are optical to electrical conversion for the data and control signals, control and monitoring of the components on the OPB as well as DC/DC conversion of the supply voltages for the front-end Hybrids and OPB itself. Each OPB will service two front-end Hybrids that are attached on opposite sides of a detector module.

Prototype OPB

The prototype OPB was designed in line with the prototype front-end Hybrid capable of reading 3 VeloPix ASICs on one tile. The prototype OPB has full functionality of the production board but with reduced number of channels. This was implemented in order to save prototype components and reduce complexity. The prototype OPB was designed to test the electrical functionality of the link from the Hybrid to the Off-detector electronics. The overview of the prototype system is shown in Figure 3.11. The OPB uses the GBTx [63], the serialiser/deserialiser IC that also provides a clock and control interface. It is a radiation hard chip that can be used to implement multipurpose high-speed (3.2-4.48 Gb/s user bandwidth) bidirectional optical links to be used simultaneously for data readout, trigger data, timing control distribution and slow control and monitoring. In case of the OPB, the GBTx is used for local control of the OPB using the control links on the Versatile Transceiver (VTRx). The GBTx communicates with the Slow Control Adaptor (SCA) [66] that provides the I2C link to configure the GBLD laser driver ASICs and logical I/O signals for the DC-DC converters. The ADC inputs of the SCA ASIC are used for voltage monitoring and monitoring the

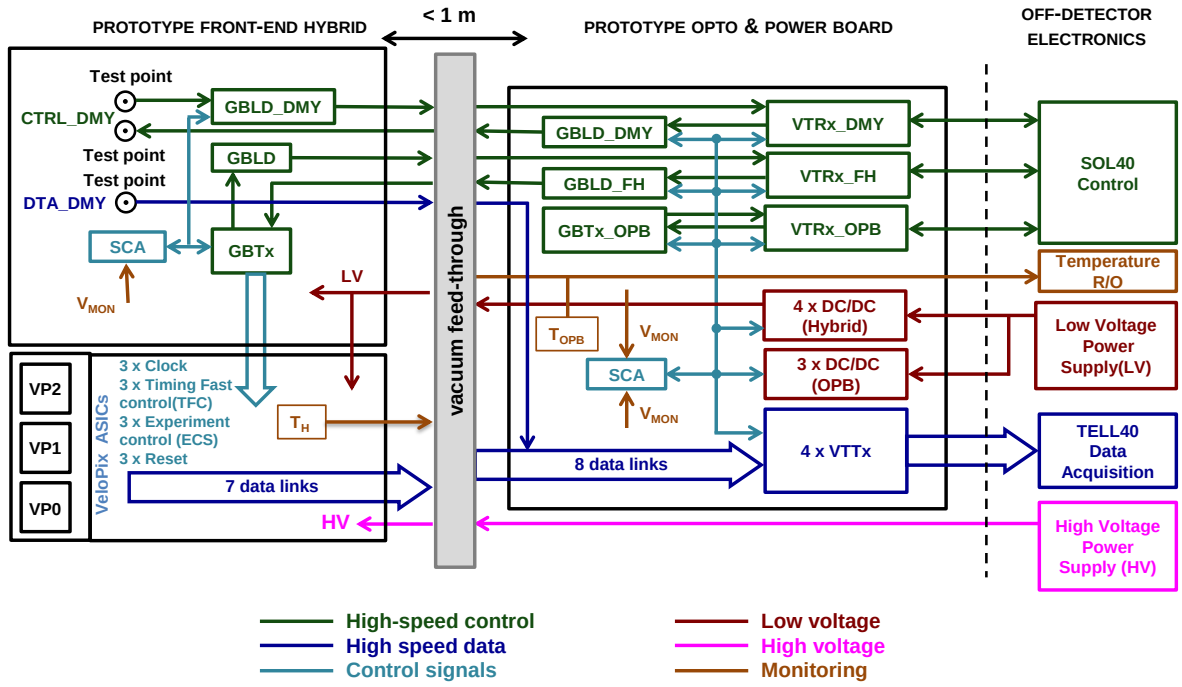


Figure 3.11: Overview of the prototype system showing the role of the prototype OPB. The main components of the prototype front-end Hybrid and OPB are shown. The colours indicate the type of signals involved. Image reproduced from [56].

received optical power. The VTRx [67] and the VTTx (Versatile twin transmitters) [68] are optical modules, which provide an optical interface to the system. The VTRx is used for the bidirectional control signals between the front-end Hybrid and Off-detector electronics. The VTTx are optical twin transmitters that comprise Laser Driver Diodes (LDD) that drive the received electrical signals to optical signals to be carried by optical cables to the readout system. The DC-DC converters [69] are radiation and magnetic field tolerant modules that supply the voltages required for the front-end Hybrids and the OPB. A temperature readout system is used to read the temperature of the Hybrid and the OPB by reading the NTCs mounted at appropriate positions on the PCBs.

The prototype is a multilayer board with hybrid construction of FR4[11] and Isola Itera[12] laminate similar to that of the prototype VFB. High-speed data signals are routed as edge-coupled stripline with continuous ground planes on either side of this signal layer. Design rules for controlled impedance and matched trace length are followed to maintain signal

[11] http://www.ventec-group.com/products/lead-free-assembly/vt-47/datasheet/
[12] http://www.isola-group.com/wp-content/uploads/data-sheets/i-tera-mt40.pdf

integrity of the high-speed differential signals. In order to achieve 100 Ω impedance on the high-speed differential signals, calculations are performed using online calculators / POLAR calculator and simulations using the ANSYS simulation tool. Details of the high-speed signal routing are covered in subsection 3.2.2. The prototypes feature a dummy control link down to the front-end Hybrid where the signals are routed to a test-point connector so that the control link driven by the GBLD ASIC can be evaluated. Moreover, a dummy data link is implemented to make it possible to inject a signal on a test-point connector on the hybrid to characterise the data uplink. The GBLD ASIC is routed with two different powering options. It can be supplied with 2.5 V through the standard power pads where the internal voltage regulator converts the 2.5 V to 1.5 V . The other option is to supply 1.5 V through the standard power pads and the decoupling pads after the internal voltage regulator. This is done to validate the powering schemes for the final system and to try to avoid using a separate 2.5 supply just for the GBLD ASICs. The input supply to the board is in the range of 6 V-8 V. This is the input voltage to the DC-DC convertors for the front-end Hybrids and to the ones powering the electronics on the OPB. The digital grounds on the hybrid and the OPB are firmly tied together since the ground planes on the high-speed links have to be connected to digital grounds of both the sender and receiver. The analogue VeloPix ASIC voltages are supplies through separate LV channels for the Hybrid with no ground reference on the OPB. This ensures that the analogue return current from the hybrid are separate and not mixed with the digital return current.

Full size OPB

The full size OPB is designed to control and read out 2 hybrids each comprising 2 tiles. The overview of the VELO electronics system and the role of the OPB is shown in Figure 3.12. The block diagram showing the placement of the main components on the PCB is shown in Figure 3.13.

The full sized OPB comprises 14 DC-DC convertors required for both the front-end Hybrids and the OPB itself, 8 of which are for analogue and digital power for the front-end ASIC's and 2 for powering the GBTx and GBLD on the hybrid. Four of the DC-DC convertors are for powering the VTTx/VTRx modules and OPB itself. The components being powered and their DC-DC convertors are shown in the Figure 3.14. The full sized OPB will have 20 pairs of data to VTTx modules. There are in all three VTRxs, two VTRxs are used for control signals to and from the 2 front-end Hybrids and one VTRx is used for control signals for the OPB. Each of these DC-DC convertors will use I2C connections to the SCA for communication. The addresses on the VTTx/VTRx are hardwired and hence dedicated I2C lines are required. The SCA supports only 16 I2C channels hence two SCAs are used to get the extra I2C channels required. The pairs are consistently and identically distributed between the two SCAs to have symmetric routing and ease of software programming. Based

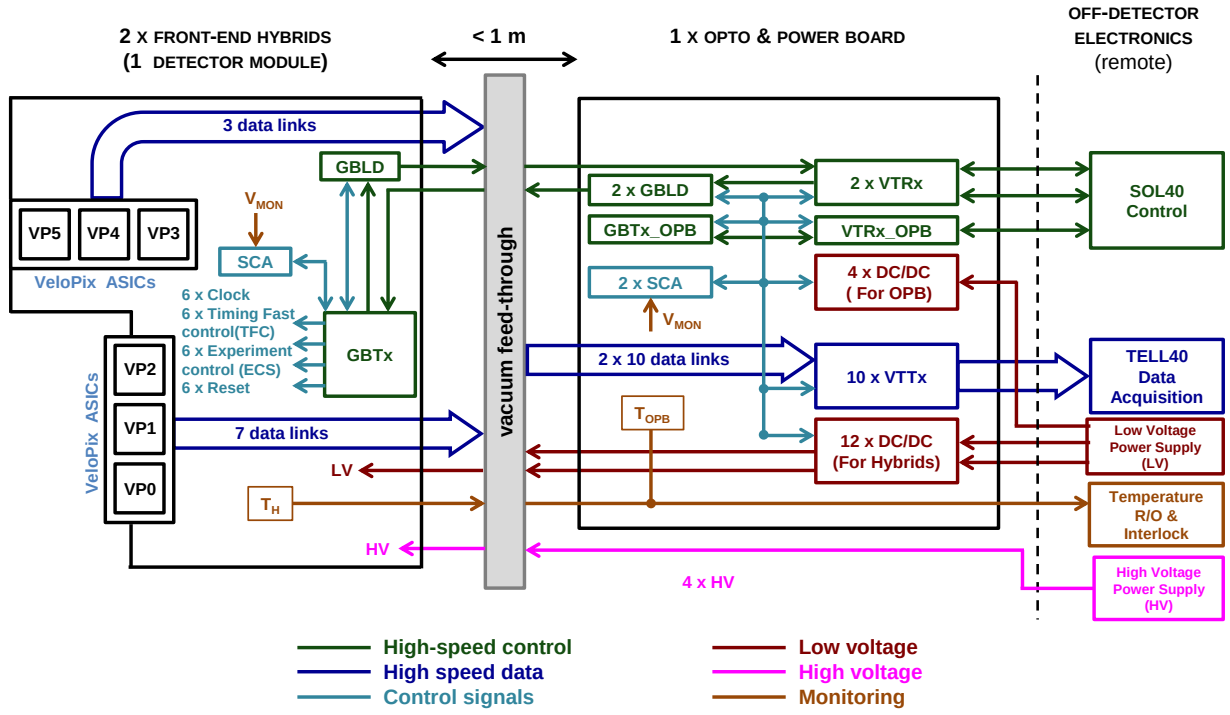


Figure 3.12: Overview of the VELO Upgrade electronics showing the role and functionality of each block in the system. The colours indicate the type of signals involved. Image reproduced from [56].

on the testing of the prototype boards for high-speed links, it was decided that a technique to improve the signal quality was required. A passive Continuous Time Linear Equalization (CTLE) circuit is implemented at the receiver end just before the VTTx modules for the data signals. For the downlink (control signals going to the front-end Hybrid), the CTLE is implemented at the sending end at the output of the GBLD on the OPB. A similar circuit is added on the Hybrid for the uplink (control signal to the Off-detector electronics) and the CTLE is described in detailed in Section 2.5. The GBLD was tested with both 1.5 V and 2.5 V supply and the results were found to be better with 2.5 V. The MOS (Metal oxide semiconductor) transistor used in the GBLD chip use 1.5 V supply. There are 2.5 V compatible transistors available in the selected process, however their performances do not match their 1.5 V counterparts. The GBLD has been therefore designed to work at 1.5 V except for the modulator and bias output stages, which are made 2.5 V compatible. In the bias current stage, which does not have special requirements in terms of speed, a 2.5 V compatible transistor has been used. It was observed that supplying the GBLD with 2.5 V and using the internal voltage regulator to generate the 1.5 V gave better results and hence a separate

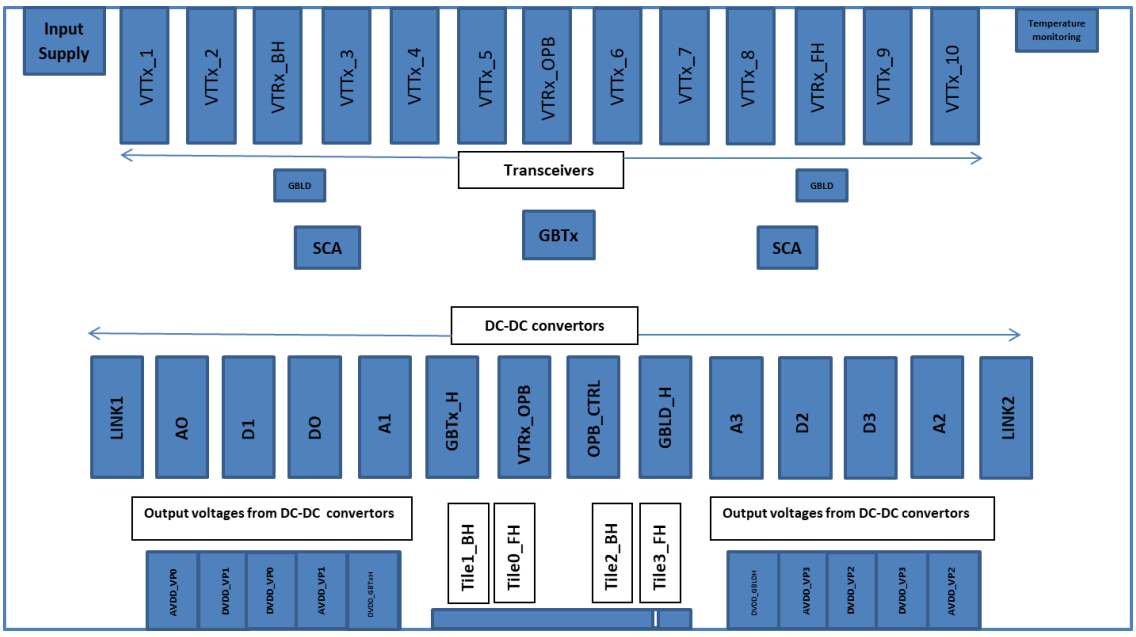


Figure 3.13: Block diagram showing the placement of main components on full size OPB.

Powering components	Supply	V [V]	I [A]	DC/DC converter
VTRx_OPB	OPB common	2.5	0.3	DCDC_OPB_VTRx
GBTx_OPB, SCA_OPB_1, SCA_OPB_2		1.5	1 + 2 x 0.3	DCDC_OPB_CTRL
VTTx (5),VTRx_BH, GBLD_OPB_BH	DIG front hybrid	2.5	5 x 0.4 + 0.3 + 0.1	DCDC_OPB_LINK_1
GBTx_FH		1.5	1	DCDC_FH_GBTx
GBLD_FH		2.5	0.1	DCDC_FH_GBLD
Tile 0 front hybrid digital		1.3	3 x 1	DCDC_FH_VPD0
Tile 3 front hybrid digital		1.3	3 x 1	DCDC_FH_VPD3
VTTx(5), VTRx_FH, GBLD_OPB_FH	DIG back hybrid	2.5	5 x 0.4 + 0.3 + 0.1	DCDC_OPB_LINK_2
GBTx_BH		1.5	1	DCDC_BH_GBTx
GBLD_BH		2.5	0.1	DCDC_BH_GBLD
Tile 2 back hybrid digital		1.3	3 x 1	DCDC_BH_VPD2
Tile 1 back hybrid digital		1.3	3 x 1	DCDC_BH_VPD1
Tile 0 front hybrid analogue	ANA front hybrid	1.3	3 x 1	DCDC_FH_VPA0
Tile 3 front hybrid analogue		1.3	3 x 1	DCDC_FH_VPA3
Tile 2 back hybrid analogue	ANA back hybrid	1.3	3 x 1	DCDC_BH_VPA2
Tile 1 back hybrid analogue		1.3	3 x 1	DCDC_BH_VPA1

Figure 3.14: DC-DC powering scheme on the OPB. Image reproduced from [56].

2.5 V DC-DC module was used for the GBLDs in the production version. A measurement performed to evaluate the supply voltage for the GBLD is shown in Figure reffig:gbldresult.

The Low Voltages (LV) on the prototype board were routed onto the two PCIe connector that also carries the data. In the production version, the low voltages are routed on two Positronic connectors[13], one for each hybrid. The GBTx and the GBLD voltages for the front-end Hybrids are also routed one on each of these connectors. The LV connectors are rated for high contact current of 80 A, very low contact resistance of 0.5 mΩ and 1000 mating cycles. The PCIe connector was changed from two 98-pin to one 164-pin connector.

[13] https://12109o3xn5ljytlkf36jl30f-wpengine.netdna-ssl.com/wp-content/uploads/2016/09/M015_RevA_1910_Scorpion.pdf

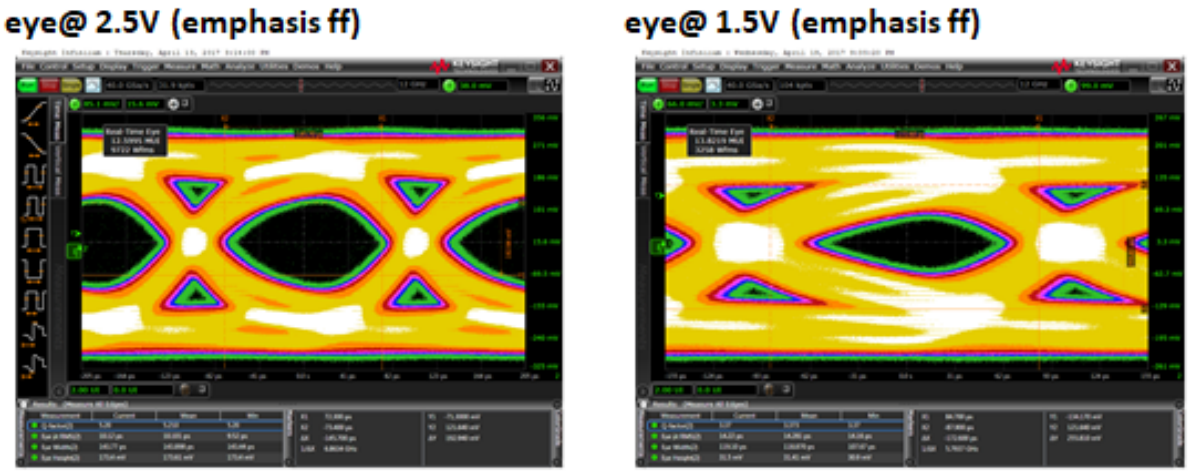


Figure 3.15: Measurement of the link from the front-end hybrid to the VTRx on the OPB. The GBLD is used as a line driver and can perform emphasis to compensate for signal distortion due the long data tape. The emphasis does improve the eye but the 2.5 V gives better results in comparison to 1.5 V supply. Credit to Jan Buytaert, CERN

Layer	Layer Assignment	Purpose
1	Top Layer	Components, non-critial signals and power traces/planes
2	Signal 1	80 MHz signals, low speed signals and some power traces.
3	Ground	Split ground plane for analogue and digital grounds
4	Power	Split power plane for the generated output voltages of the DC-DC convertors .
5	Ground	Continuous digital ground reference
6	Signal 2	5.12 Gb/s signals
7	Ground	Continuous digital ground reference
8	Bottom Layer	Components, non-critial signals and power traces/planes

Table 3.5: Layer stackup of the production version of the OPB.

For mechanical reasons and ease of assembly the PCIe connector was moved on the VFB and the edge fingers to mate to the connector, were moved to the OPB. There are components like LEDs, terminal blocks and jumpers that are used at various points in the design to ease testability. Some of these components used as a part of 'design for testing' are not radiation hard and hence are kept in the design but will not be mounted for the final boards. The grounding and powering scheme remains the same as the prototype board with just additional low voltage references for both the front and back hybrids. It was observed that the prototype PCB bowed and one of the cause could have been the non-symmetric build due to the hybrid construction of the PCB with FR4 and Isola I-tera material. A more balanced build of the PCB was investigated and the same 8-layer stackup, as that of the prototype, but with a full Isola I-tera build. The individual layer assignments and their purpose is shown in Table 3.5. The boards fabricated with this build were found to be flatter, as expected.

3.3 Off-Detector Electronics

The LHCb Upgrade uses a common readout board for all off-detector electronics. The board is called PCIe40 [70] and is based on the Altera Arria 10 FPGA and the role of this board in the experiment (SOL40, TELL40) is determined by its firmware only. For testing purposes, the different functionalities are combined into a single system called MiniDaq [71]. The first version of MiniDaq was used to test prototypes of the On-detector electronics.
The SOL40 boards distribute the control signals to all the front-end chips and keep the whole experiment synchronous. As a single SOL40 provides 48 control links, a total of four SOL40 boards are needed for controlling the 156 links of the whole VELO. The LHCb SOL40 common firmware was modified matching with VELO requirements in order to control the front-end VeloPix ASICs directly from the GBTx e-ports.
The TELL40 boards are responsible for high-speed data acquisition with a maximum data rate of 100 Gbit/s, making it possible to read out the complete VELO module with 20 data links. Therefore a total of 52 boards will be needed for VELO Upgrade.

Chapter 4

Electronics Characterisation for the LHCb VELO Upgrade

The chapter covers the performance of the electronics designed for the LHCb VELO Upgrade and the results of the measurements are shown and described. Some prototype runs were carried out to evaluate the designs and test results were studied to understand the scope for improvement. Section 4.1 covers the Data tape characterisation; the different variants of tape, the design changes and the motivation for the changes, and the results of transmission performance from these variants. Section 4.2 covers the results from measurements of the prototype Opto Power Board (OPB) with High-speed links and the Vacuum Feedthrough Board (VFB). Section 4.3 shows the measurement results from the full link test and the conclusion of the measurements.

The laboratory test setup has the front-end Hybrid connected to the network analyser using Bulls-eye[1] high-density, high-performance test points rated to 20 GHz/40 Gbps. The hybrid is connected to the 560 mm long data tape followed by the VFB and then the OPB. The OPB further connects to the network analyser using off-the-shelf SFP+ to SMA interface card. The aim for the electronics is to have a loss of < 10 dB at the Nyquist frequency of 2.5 GHz for the full system, a characteristic impedance of 100 Ω to avoid impedance mismatch and reflections to the system, and a minimal rate of errors in the transmission of the bits, set to be $<10^{-13}$. Section 4.4 covers the radiation tests performed on test coupons for the OPB and the Data tapes to evaluate that the material used in the fabrication of the PCBs can withstand the specified radiation dose without any visible damage and with acceptable electrical performance.

[1] `https://www.samtec.com/cables/high-speed/test/bulls-eye`

4.1 Data Tape characterisation

The Data tapes are flex tapes designed to connect between the front-end Hybrid and the Vacuum Feedthrough Board (VFB). Some variants were designed and produced namely TapeVar1, TapeVar2 and TapeVar 3 for the Data tape with layout specifications as shown in Table 3.2. These were made with different trace widths and trace spacing to identify the one best matched to 100 Ω characteristic impedance with minimal loss in transmission. The comparison of the three variants with and without the connectors mounted at either end of the tapes is given in Figure 4.1. These tapes were 560 mm long and the same ones were made in a very short length of approximately 50 mm. The purpose of the short tapes was to disentangle the effect of the connectors on the tape by a process of Automatic Fixture Removal (AFR) on the PLTS interface of the network analyser (described in Section 2.4).

The characteristic impedance of the traces can be calculated from electrostatics. This is done with a commercial software provided by Polar Instruments [2] where the build is defined in two dimensions with copper and dielectric layers. The simulation from the calculations for impedance with trace width/trace spacing of 0.2 mm/0.2 mm are as shown in Figure 4.2. This tool gives an approximation of the impedance with a variation of ± 10%, that could arise due to the fabrication process.

The performance with trace width/trace spacing of 0.2 mm/0.2 mm (TapeVar1) was measured to be the best with connectors and with fixture removal method.

The next generation prototype was made with the same build as that of TapeVar1 but fabricated in industry. A few changes in the layout were implemented to improve the overall performance. This variant was called TapeVar1.1 and the results of the testing are shown in Figure 4.3.

Variant TapeVar1.2 was produced with a small modification in the trace width and trace spacing and the pinout of the connector was changed to reduced inter-pin capacitance. Another run of tapes namely TapeVar1.3 and TapeVar1.4 were produced with 0.18 mm/0.22 mm and 0.2 mm/0.2 mm respectively as the results with these two trace widths and trace spacings were close and the idea was to keep the other PCB parameters constant while only changing the trace width and trace spacing and study the results. The simulation from the calculations for impedance with trace width/trace spacing of 0.18 mm/0.22 mm is shown in Figure 4.4. The results of the S-parameter comparison of the different tape designs that were produced to converge on the final design are shown in Figure 4.5. TapeVar1.2 and TapeVar1.4 differed only in the length of the tape and hence TapeVar1.4 is shown in the comparison. The plot showing the impedance comparison is shown in Figure 4.6.

The results from the measurement were analysed and compared and the conclusion was to go ahead with the trace width/trace spacing of 0.2 mm/0.2 mm.
The mechanics of the VELO required two variants namely the Left Hand Side (LHS) and

[2] https://www.polarinstruments.com/products/cits/Si8000.html

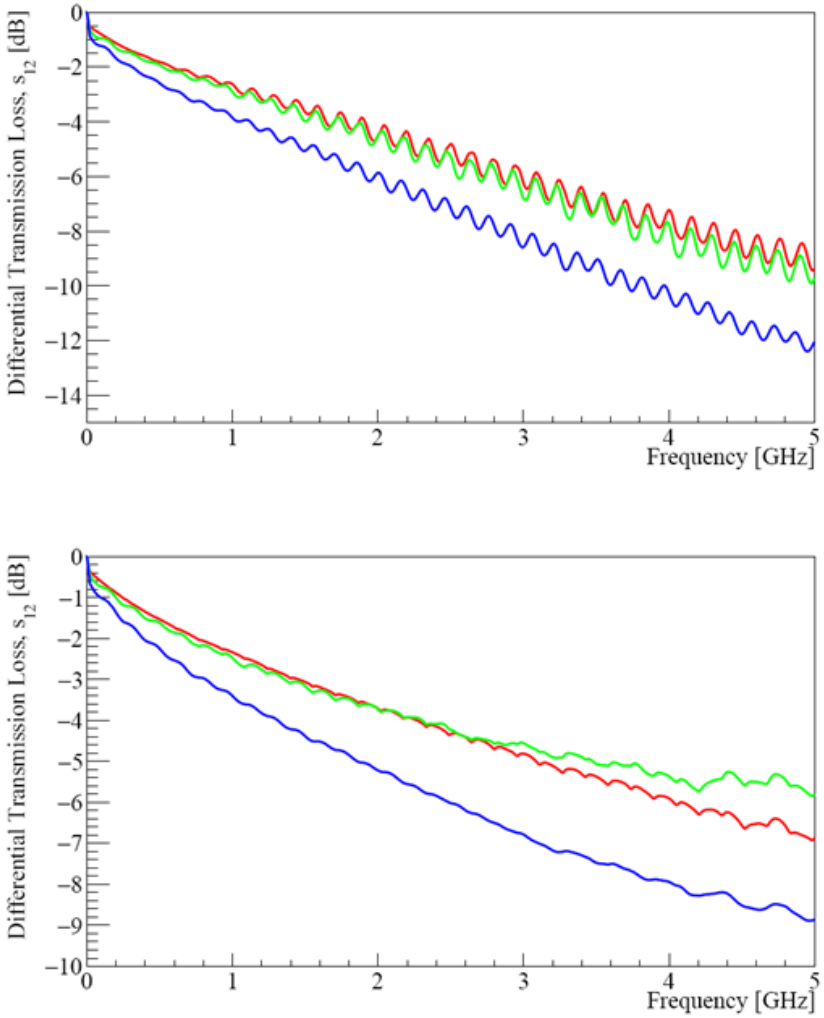


Figure 4.1: Transmission results (S-parameters) comparing the three prototype tapes (fabricated at CERN) along a channel. Top - The losses due to the full cable. Bottom - The losses due to the traces on the PCB. The red distribution shows the losses with a trace width/trace spacing of 0.2 mm/0.2 mm . The green distribution shows the looses with a trace width/trace spacing of 0.15 mm/0.25 mm. The blue distribution shows the losses with a trace width/trace spacing of 0.1 mm/0.1 mm. Plots reproduced from [72].

Right Hand Side (RHS) tape and with three different lengths. The pre-production boards were measured for loss and impedance on the 2 types of tapes, Left Hand Side (LHS) and Right Hand Side (RHS) tape with a mean loss of approximately 9.29 dB at 2.5 GHz without fixture removal which would further reduce the loss. The results of the measurement on a LHS for each of the 7 data pairs is shown in Figure 4.7. Thanks to Phil Collins for measuring some of the pre-production tapes. The results of the measurement on a RHS for each of the data 3 data pairs and 2 control pairs is shown in Figure 4.8.

The impedance plot for the above measurements for the LHS and RHS tapes measure an impedance of 94 Ω which is within the 10% fabrication tolerance. The plot for impedance is shown in Figure 4.9.

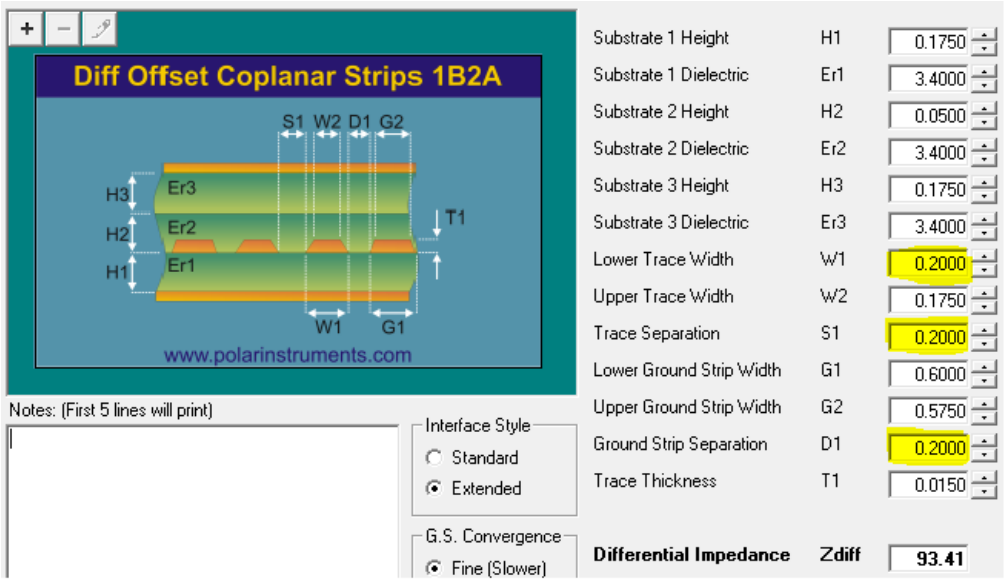


Figure 4.2: Calculations of the trace width/trace spacing of 0.2 mm/0.2 mm for the data tape using Polar calculator.

A few of the final production tapes were measured to ensure that the signal quality and impedance measurements were within the acceptable limits. The signal losses improved with minor tweaks in the layout. A tape from each production panel was measured for loss and impedance and the results are shown in Figure 4.10. The design of the different variants of the tapes describes in this section and the changes implemented between the variants as well as the reason for the changes is described in Section 3.2.2. All the measurement results and the touchstone files were saved in a database to record the results and help trace back if required. This process was followed for all the panels of the production batch produced.

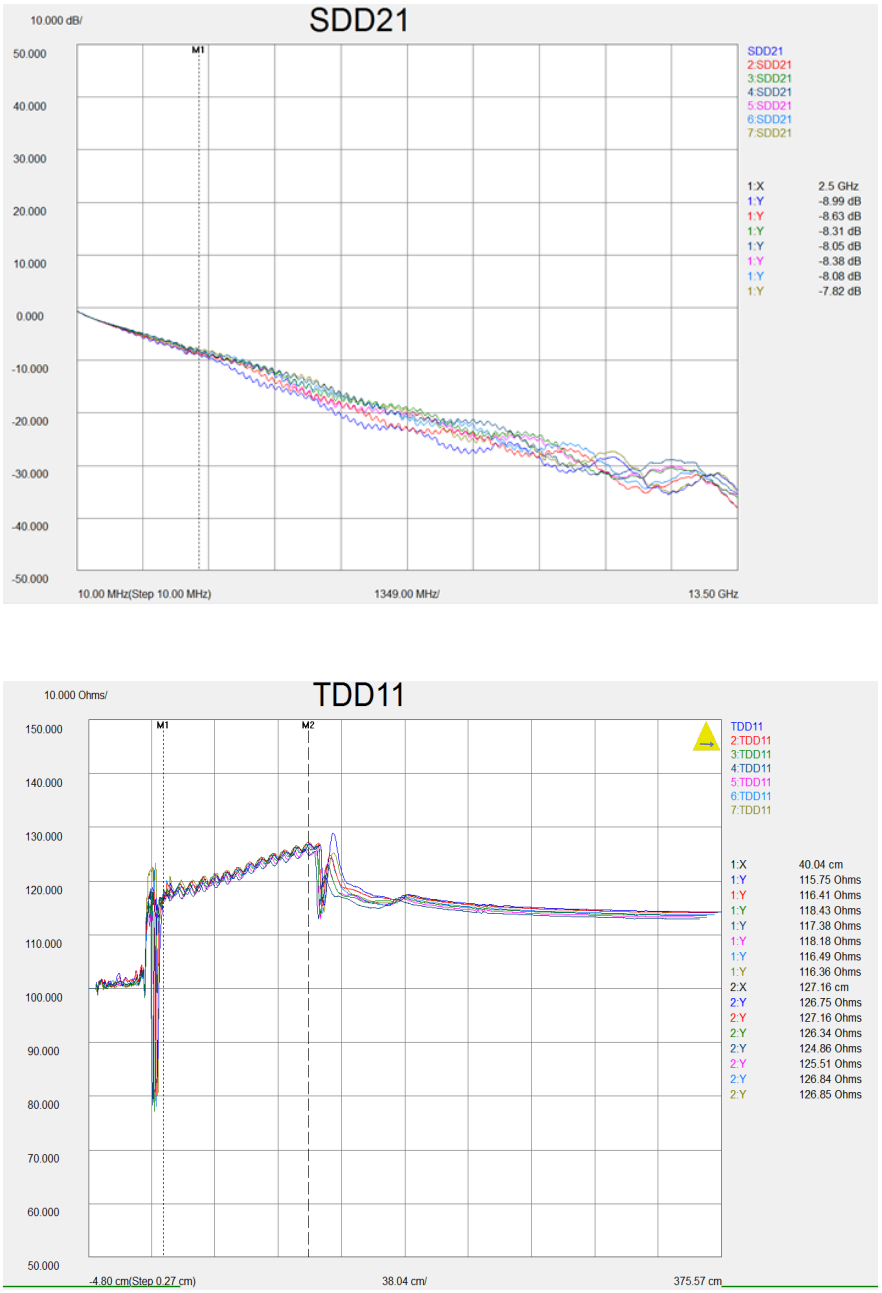


Figure 4.3: Top - Transmission results (S-parameters) for TapeVar1.1 measuring a mean loss of 8.32 dB at 2.5 GHz. The results are without fixture removal. Bottom - Impedance measured to be 120 Ω on (pseudo) TDR on the network analyser.

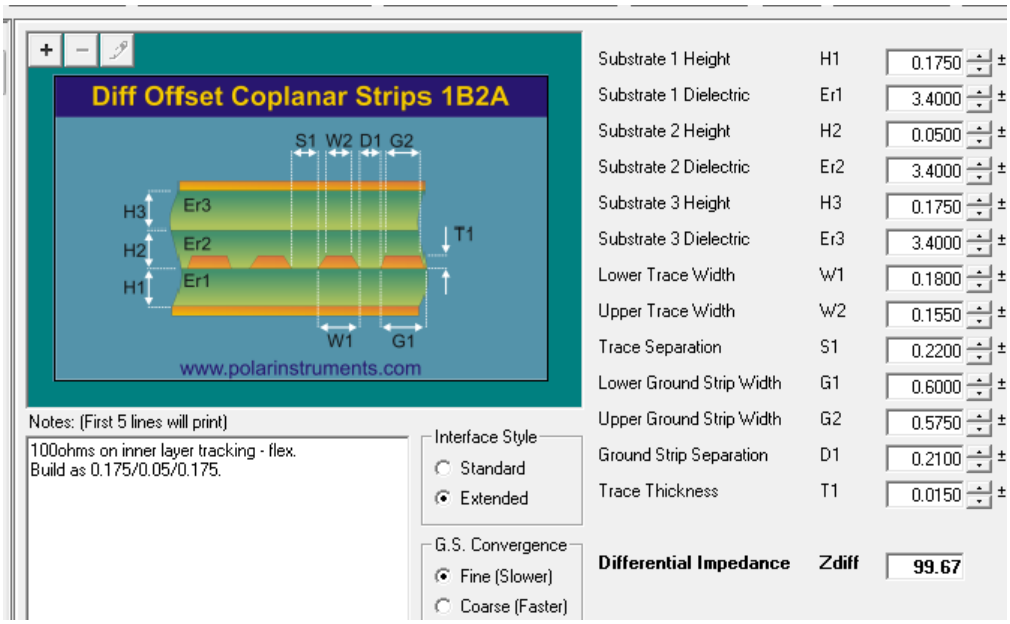


Figure 4.4: Calculations of the trace width/trace spacing of 0.18 mm/0.22 mm for the data tape using Polar calculator.

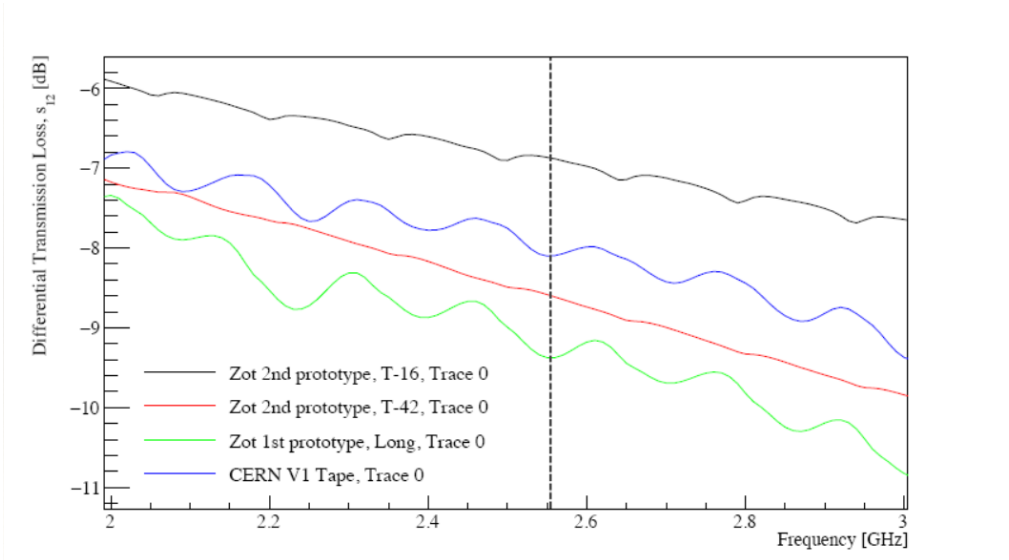


Figure 4.5: Transmission results (S-parameters) comparing the losses from the different tape designs (zoomed between 2 and 3 GHz). (Black) - 0.2 mm / 0.2 mm (TapeVar1.4), (red) - 0.18 mm/0.22 mm (TapeVar1.3), (green)- 0.18 mm/0.22 mm (TapeVar1.1), (blue) - 0.2 mm/0.2 mm (TapeVar1). The results are without fixture removal.

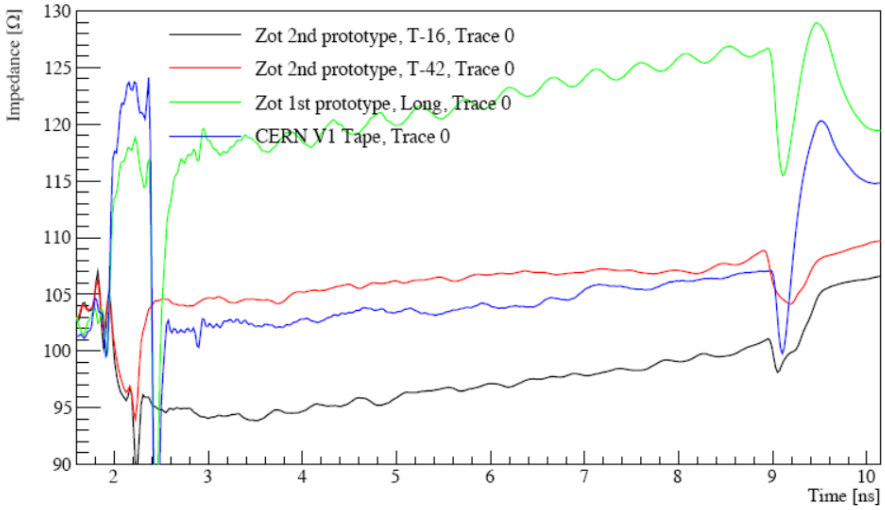
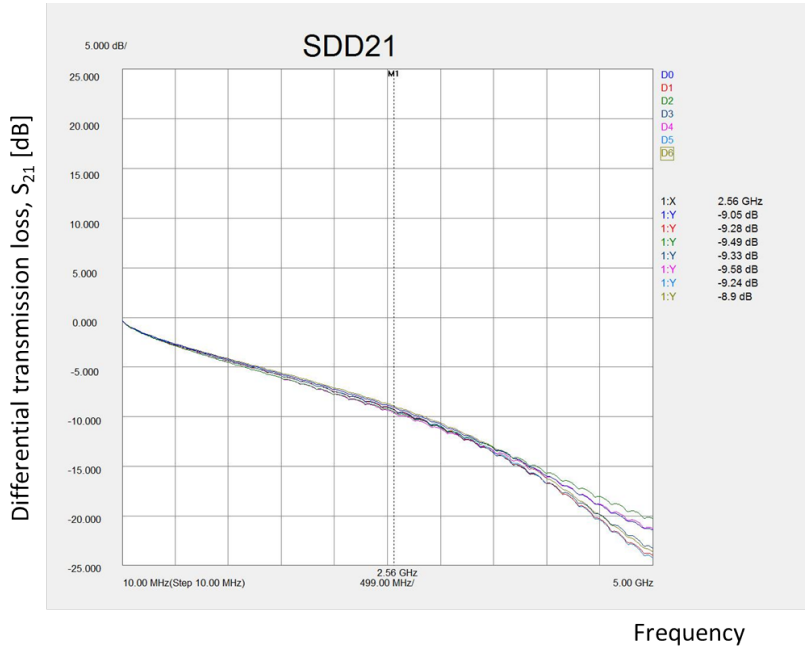


Figure 4.6: Comparison of the impedance of different tape designs. (Black) - 0.2 mm/0.2 mm (TapeVar1.4), (red) - 0.18 mm/0.22 mm (TapeVar1.3), (green)- 0.18 mm/0.22 mm (TapeVar1.1), (blue) - 0.2 mm/0.2 mm (TapeVar1). The aim is to get closest to 100 Ω with minimum loss in transmission.

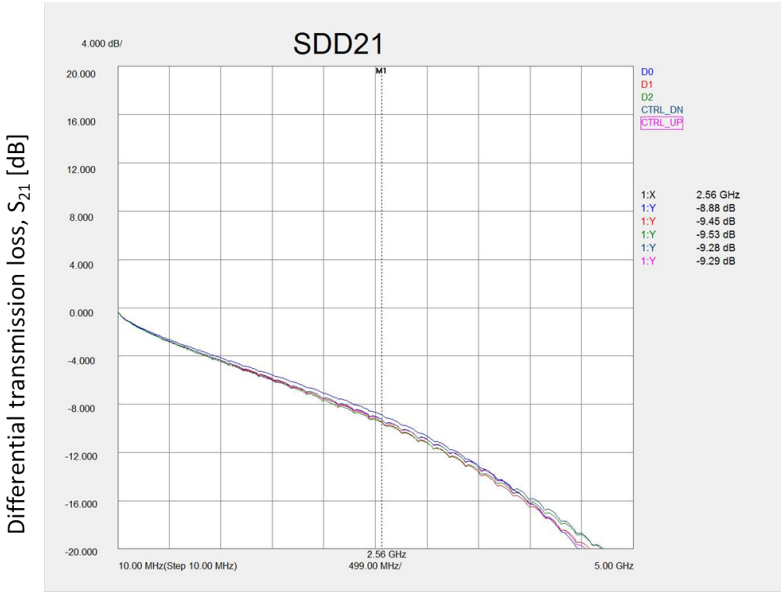
Channel	Loss @ 2.56 GHz [dB]
D0	9.05
D1	9.28
D2	9.49
D3	9.33
D4	9.58
D5	9.24
D6	8.90



Mean attenuation @ 2.56 GHz = 9.28 dB

Figure 4.7: Results of a Left Hand Side (LHS) tape for each of the 7 data pairs measuring a mean loss of 9.28 dB at 2.5 GHz. The results are without fixture removal.

Channel	Loss @ 2.56 GHz [dB]
D0	8.88
D1	9.45
D2	9.53
CTRL_DN	9.28
CTRL_UP	9.29



Mean attenuation @ 2.56 GHz = 9.29 dB

Figure 4.8: Results of a Right Hand Side (RHS) tape for each of the 3 data pairs and 2 control pairs measuring a mean loss of 9.29 dB at 2.5 GHz. The results are without fixture removal.

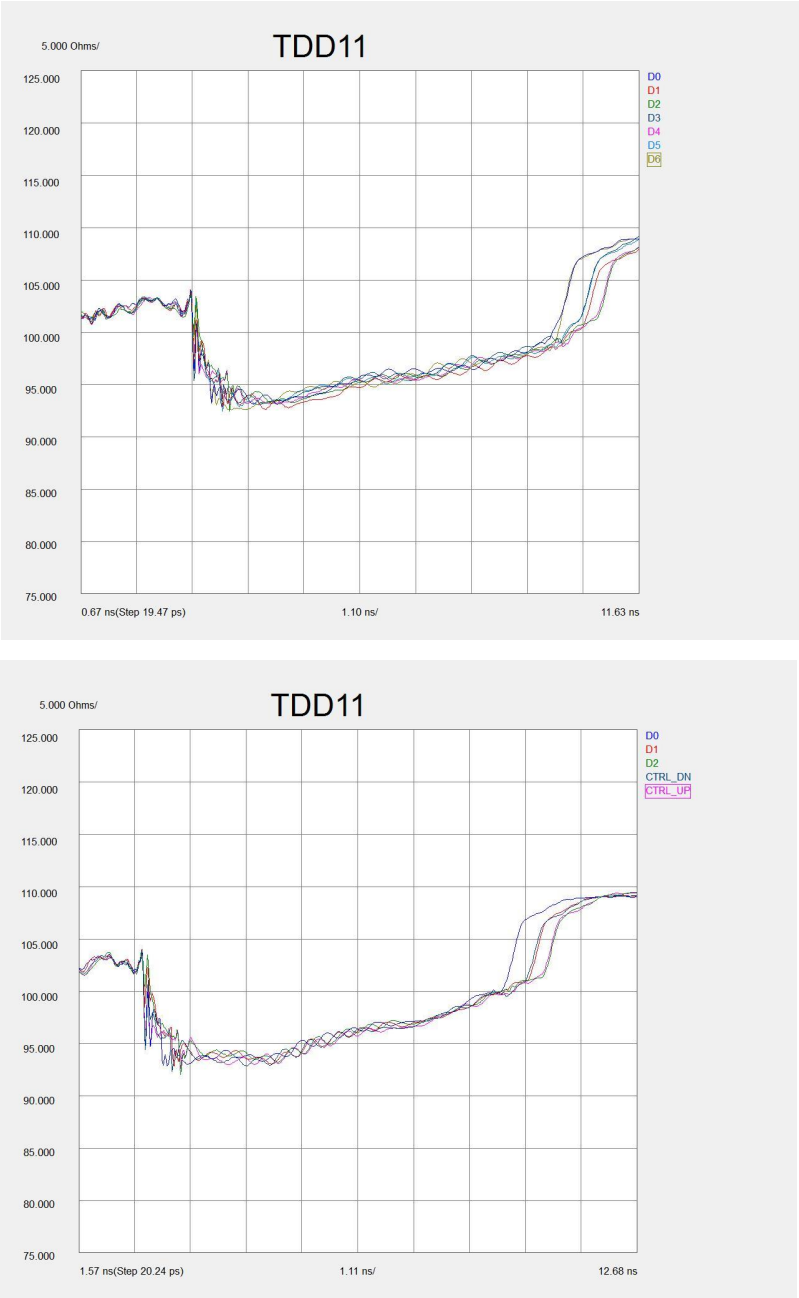


Figure 4.9: Differential impedance profile for Tapes. Top - Left Hand Side (LHS) tape and Bottom - Right Hand Side (RHS) tape measuring an impedance of 94 Ω on (pseudo) TDR on the network analyser.

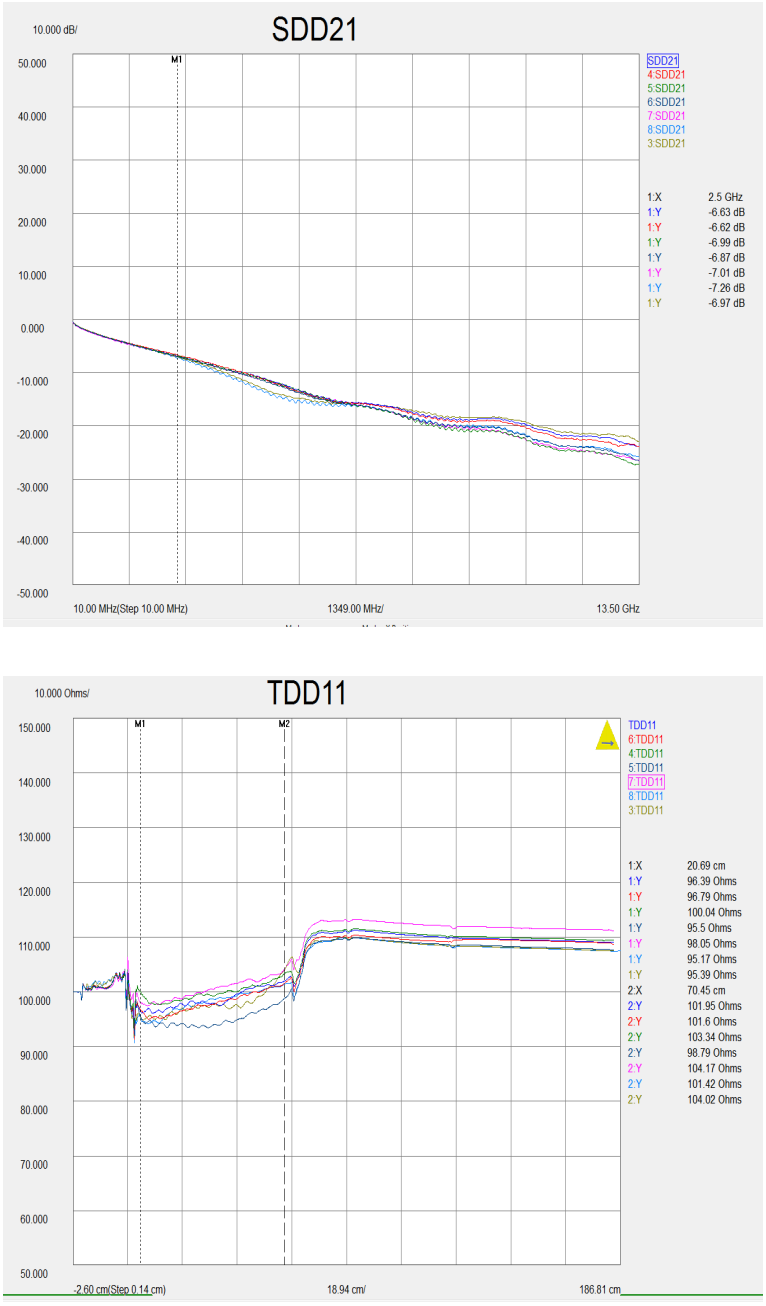


Figure 4.10: Results of tapes from different production panels. Top - Measurements with a mean loss of 6.9 dB at 2.5 GHz. The results are without fixture removal. Bottom - Impedance measured to be of 96 Ω on (pseudo)TDR on the network analyser.

4.2 High-speed links and Opto Power Board (OPB) characterisation

For the prototype OPB (described in Section 3.2.4), High-speed links were measured with the Data tapes and the prototype Vacuum Feedthrough Board (VFB) and the eye diagram is shown in Figure 4.11.

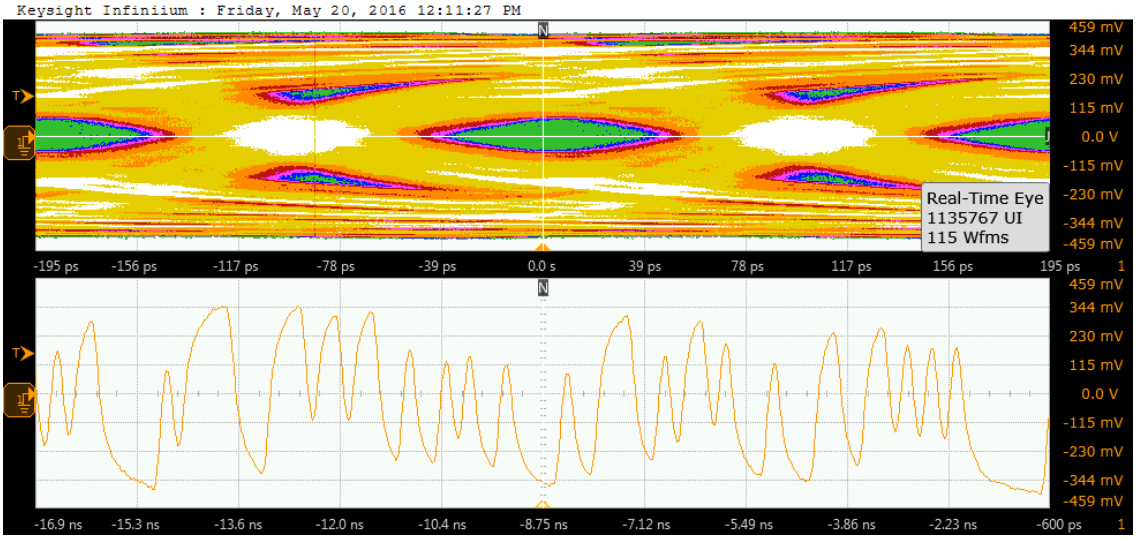


Figure 4.11: Top - Eye diagram produced by the prototypes for the full setup produced using a PRBS $2^7 - 1$ signal at 5.12 Gb/s. It can be seen that the eye has just closed (green is the lowest valued colour scale) which resulted in a large bit error rate. Bottom - The bit pattern measured at the output of the setup [72].

It was observed that the eye just closed (green is the lowest valued colour scale) which resulted in a large bit error rate. Efforts towards improving the quality of the signal transmission lead to adding a passive CTLE network on the OPB for each of the high-speed differential pairs. The details of the passive CTLE network are explained in Section 2.5. The CTLE is implemented at the receiving end of the data signals at the input of the VTTx's (Versatile twin transmitters) module. For the control signals, the same passive network is implemented at the sending end for the downlink (to the front-end Hybrid) at the output of the GBLD (GigaBit Laser Driver) chip. For the uplink (to the Off-detector electronics) the same circuit is implemented at the GBLD output on the front-end Hybrid. The transfer function for the passive CTLE is plotted and the inverse of the transfer function is fitted to the S-parameter for the link using an analysis software and the fit was made to determine the optimal component values. The output of this analysis is shown in Figure 4.12.

The plot in Figure 4.13 shows the theoretical CTLE plot and the one measured with L-R-L (on the data links) and without L-R-L (on the control links) circuit. The circuit was evaluated for impedance results with and without the L-R-L circuit and the performance plots are shown in Figure 4.14. The laboratory setup and the instruments used are described

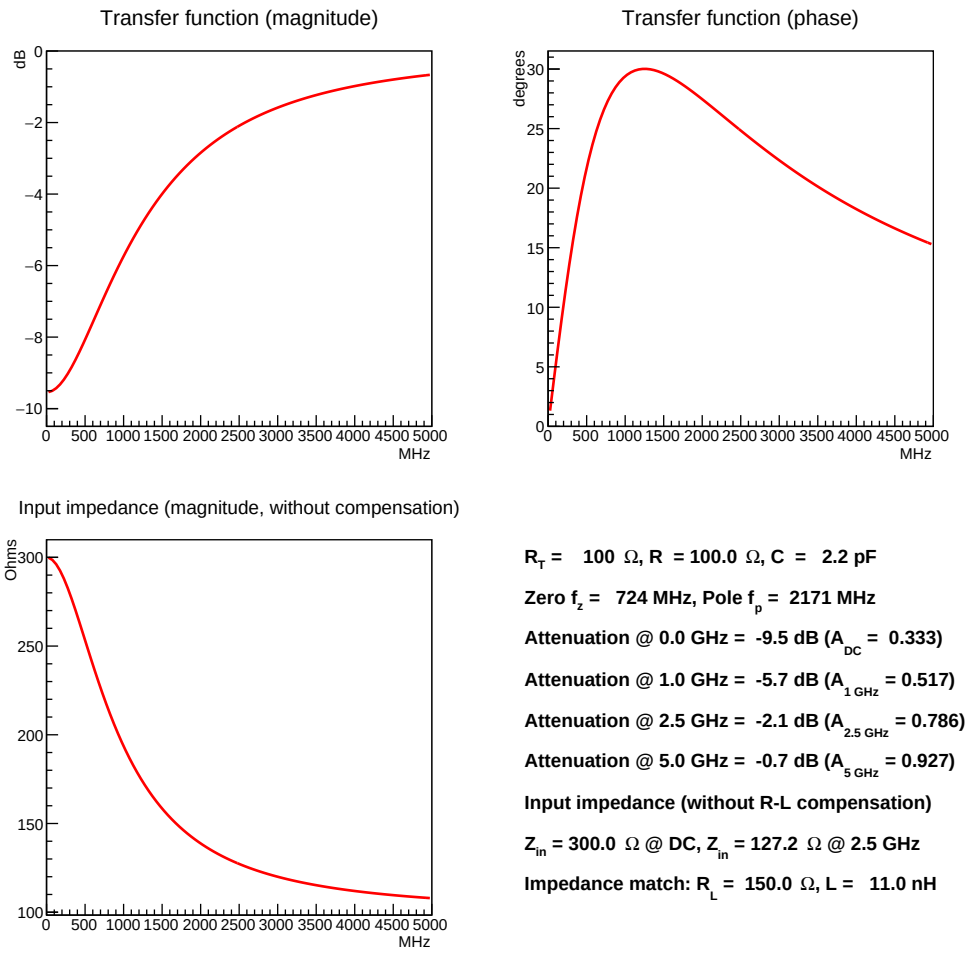


Figure 4.12: The transfer function magnitude and phase plots and the impedance plot for the passive CTLE network.The optimal component values are derived by fitting plots using an analysis software. Credit to Prof. Lars Eklund, University of Glasgow

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in Section 2.4. The J-BERT source with ± 600 mV swing that matches the output swing from the VeloPix chip, 5.12 Gbit/s and PRBS $2^7 - 1$ is applied as the input signal. The J-BERT is connected via SMA cable to the SMA-SFP + adaptor, OPB, Vacuum Feethrough, 56 cms tape, SMA adaptor, (optional CTLE) and SMA cable to the oscilloscope. The eye diagram before and after CTLE and with and without the L-R-L is shown in Figure 4.15.

It is observed that the reflection and impedance plots are better with L-R-L with a small effect of non-ideal components and parasitics seen as a small resonance at 3.5 GHz. A solution for this was to use capacitors for the CTLE circuit that are rated for high-speed signal transmission. The eye diagram looked similar with and without the L-R-L network but the impedance and reflection plots were better with L-R-L and hence the CTLE circuit (described in detail in 2.5) was implemented at the input of the VTTxs on the OPB.

For the control links from the OPB to the front-end Hybrid and vice versa, it was decided to place the CTLE network on the sender side. The CTLE was implemented on the OPB for

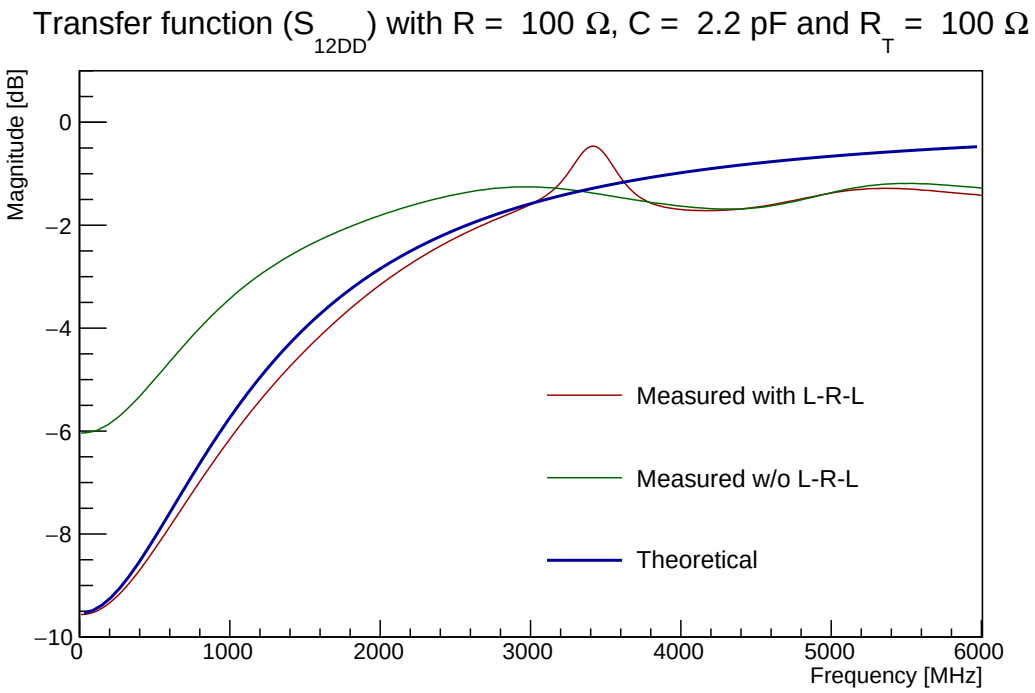

Figure 4.13: Comparision of the CTLE transfer function, (blue) theoretical, (red) measured with L-R-L and (green) measured without L-R-L.

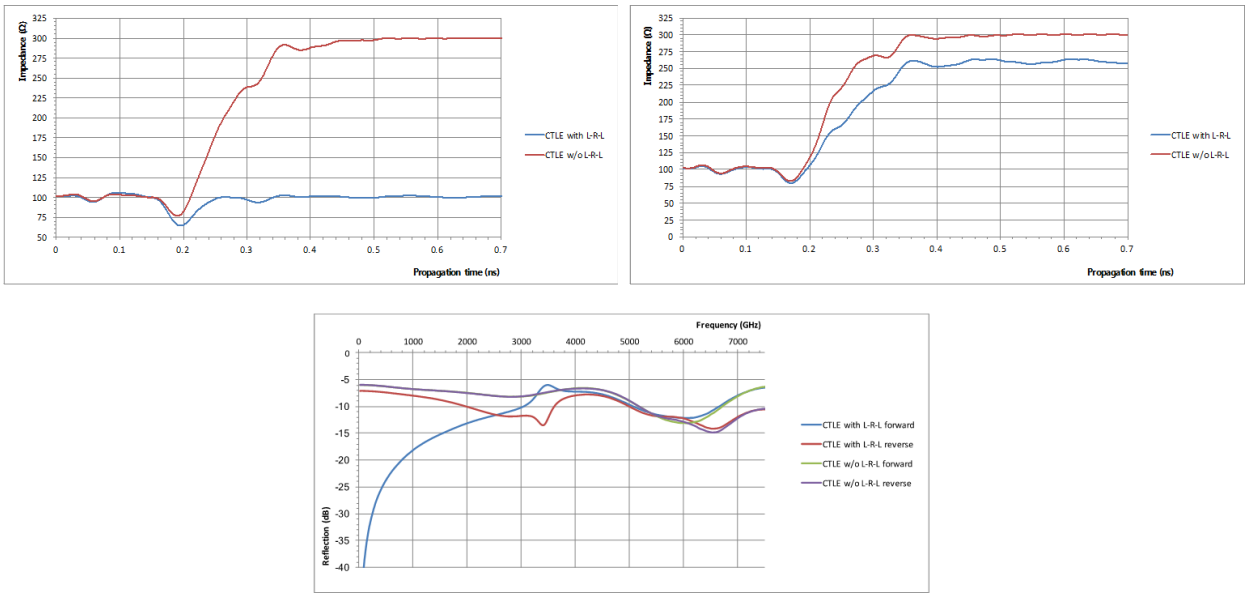

Figure 4.14: Comparing impedance with and without the L-R-L circuit. Top left - Measuring in forward direction, from L-R-L circuit side. Top right - Measuring in reverse direction. (Bottom) Measuring reflection of CTLE circuit with and without L-R-L in forward (from L-R-L side) and reverse direction. The impedance plot and the reflection is seen to be better with the L-R-L circuit and hence implemented in the design.

the downlink and on the front-end hybrid for the uplink. Since the circuit was implemented on the sender side the L-R-L network for impedance matching mattered less in this configuration. AC coupling capacitors were implemented in series after the CTLE to lump all impedance

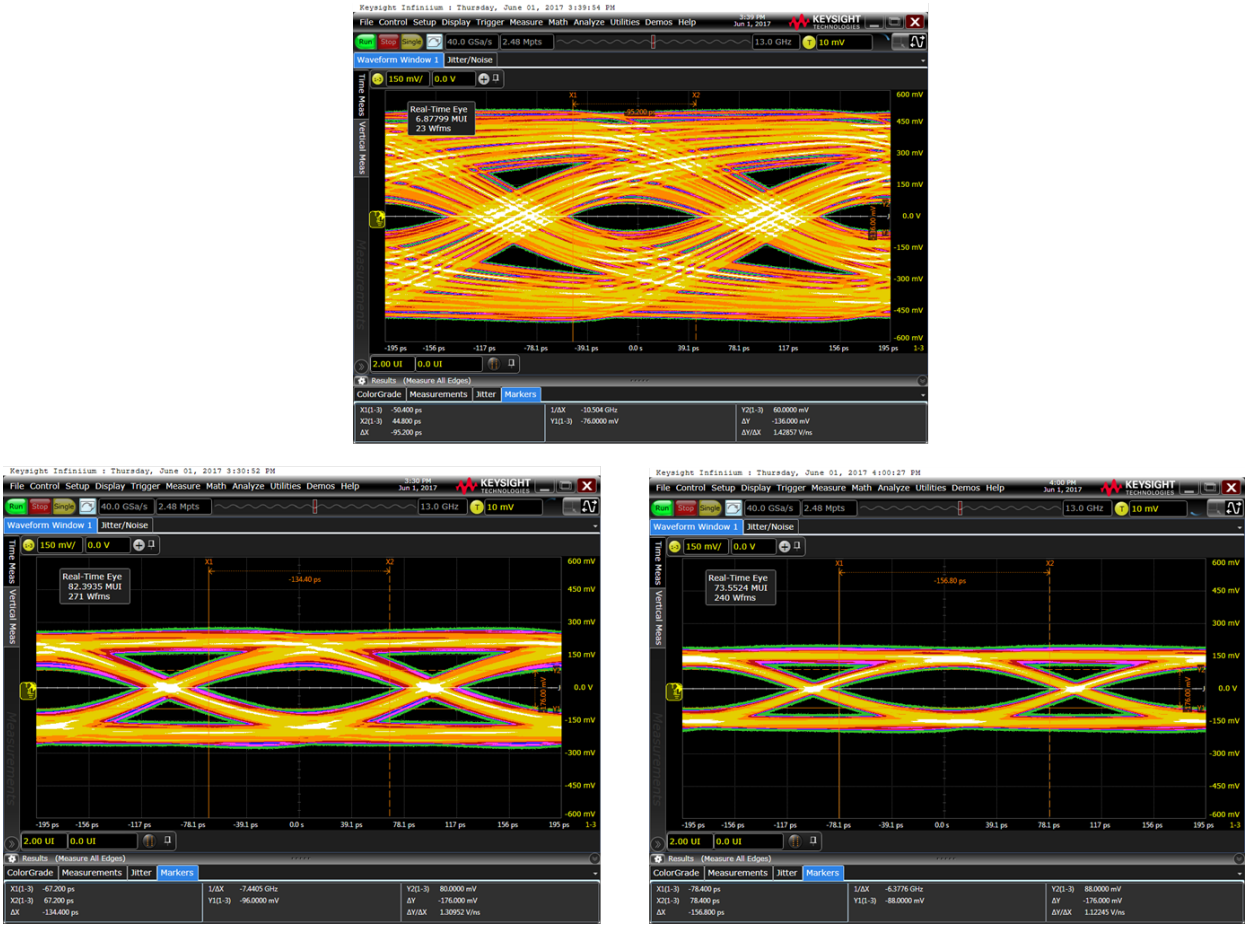

Figure 4.15: Top - Eye diagram with no CTLE applied. Bottom left - Eye diagram with CTLE circuit without L-R-L network and Bottom right - CTLE circuit with L-R-L network.

mismatches in one place. For the uplink, the CTLE was implemented on the front-end Hybrid with no AC coupling capacitor as there were already capacitors present in the VTRx modules. The CTLE with the modification to the L-R-L network is shown in Figure 4.16.

The CTLE circuit with the derived values was implemented on the OPB and the 10 VTTx pairs were measured and the results are shown in Figure 4.17. The VTRx control uplink pair is also measured that shows the difference with and without CTLE in the plots. This link has the CTLE on the front-end hybrid while the control downlink has the CTLE components at the output of the GBLD on the OPB. The laser driver chip (GBLD) is targeted at driving VCSELs (type of semiconductor laser diodes), however, the range of selectable modulation and laser bias currents allow it to be used a line driver as used in this design. The modulation current, the laser diode bias current and the pre-emphasis settings for the GBLD are programmable either through hard wired signals or through an I2C serial port. By tuning the GBLD settings, an eye opening that exceeds the requirements of 200 mV x 40 ps (eye window) was aimed to be produced.

For the control link, the CTLE values were further tweaked to get the optimal performance and values of R = 82 Ω and C = 2.7 pF were used as these values matched the S-parameter

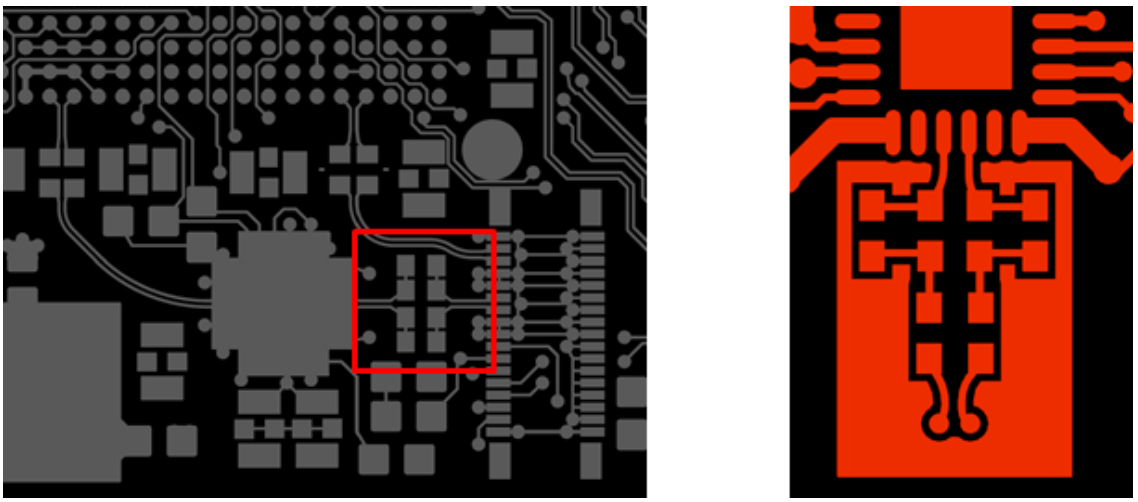

Figure 4.16: Left - CTLE circuit on the front-end Hybrid for the uplink. Right - CTLE circuit on the OPB for the downlink.

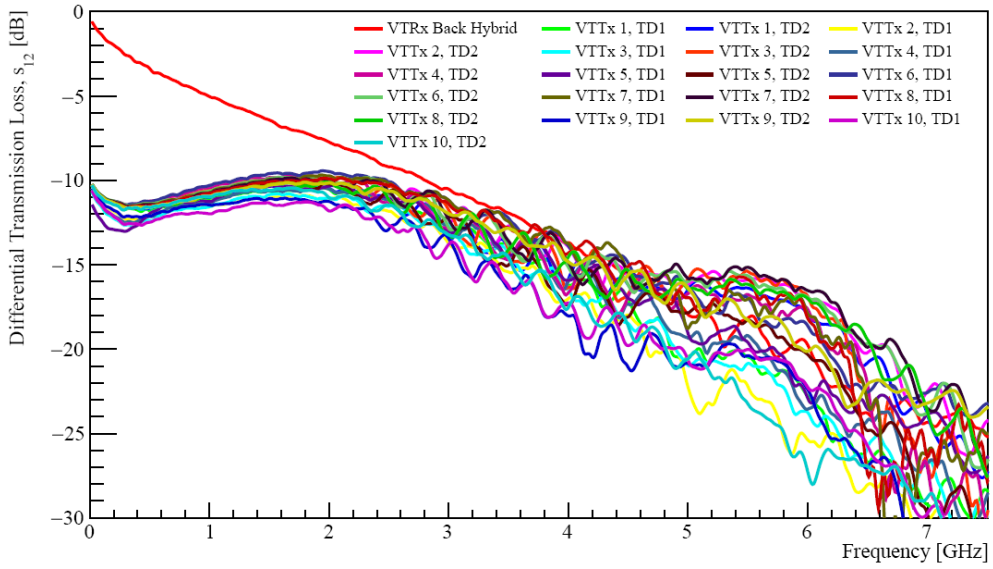

Figure 4.17: Measurements for differential transmission losses for the full sized pre-production prototype across 20 traces. The red trace does not have a CTLE circuit as this is a control downlink that has the CTLE on the receiving end on the front-end Hybrid. Plot reproduced from [72].

plot closely than the data link values (R = 100 Ω and C = 2.2 pF). The plot in Figure 4.18 shows the more moderate CTLE with the changed values of R and C.

The setup is the same as the Data links with the J-BERT source (with ± 500 mV swing, 4.8 Gbit/s), SMA cable, SMA-SFP+ adaptor, GBLD on the OPB, VFB, 56 cm tape, SMA cable, CTLE, SMA cable connected to the oscilloscope. With the power-on GBLD setting, modulation current of 6 mA with no pre-emphasis and with PRBS $2^7 - 1$, the eye diagram is as shown in Figure 4.19.

The link was further evaluated with pre-emphasis (amplitude = 7.6 mA & width = 70ps)

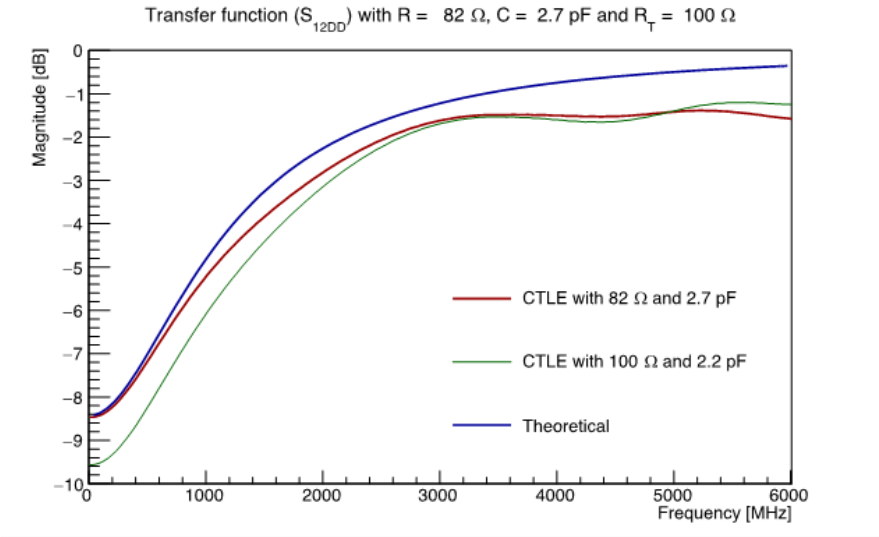

Figure 4.18: (Blue) Theoretical CTLE transfer function, (green) Transfer function with R and C values for Data link, (red) Transfer function with R and C values for a more moderate CTLE.

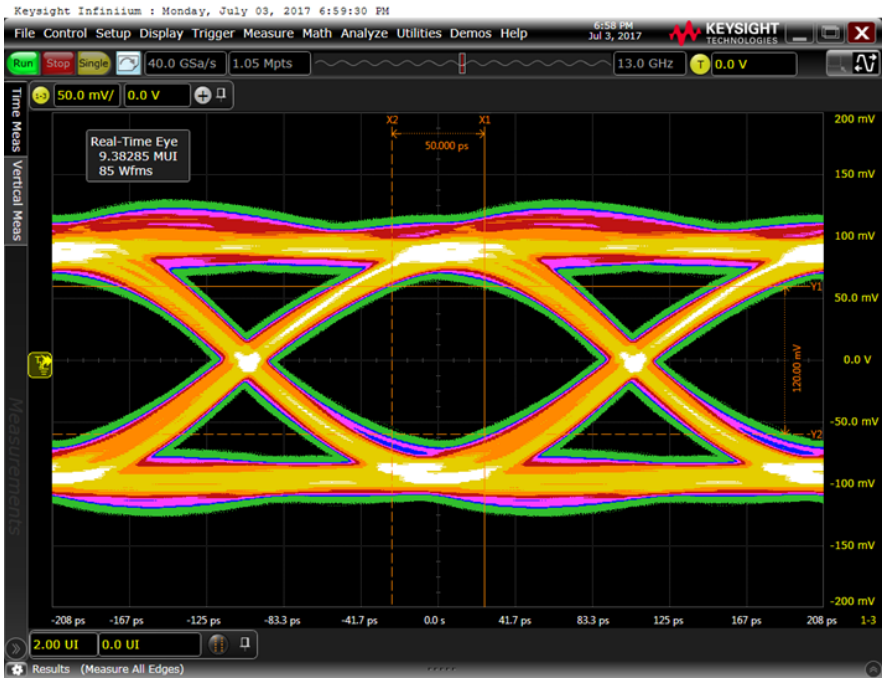

Figure 4.19: Eye diagram for the control link with power-on GBLD settings: modulation current of 6 mA with no pre-emphasis and PRBS $2^7 - 1$: 120 mV opening over 50 ps.

and without pre-emphasis and modulation current set to 7 mA to see the effect on the eye opening. The JBERT source with ± 500 mV swing, 5.12 Gbit/s and PRBS 2^7-1, comparision of the two eye diagrams is shown in Figure 4.20. The eye window was observed to be better with pre-emphasis.

Based on the same settings as in the previous measurement, a few more measurements were performed to understand the effect of the values of the passive components of the CTLE

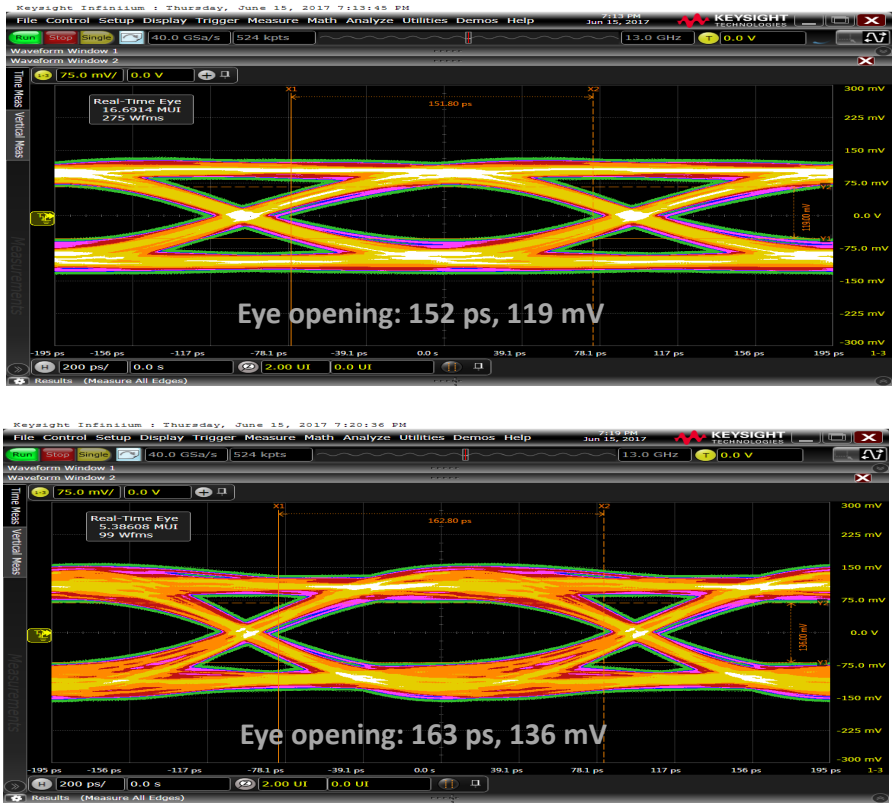

Figure 4.20: Eye diagram with modulation current of the GBLD set to 7 mA. Top - without pre-emphasis and Bottom - with pre-emphasis (amplitude = 7.6 mA and width = 70ps).

(R and C), with and without pre-emphasis and variation to the modulation current on the eye opening. This is summarised in the plot in Figure 4.21.

Based on the measurements and study of the plots and eye diagrams, GBLD setting of modulation current of 12 mA and pre-emphasis amplitude 6.7 mA with 50 ps was tweaked and resulted in an eye as shown in Figure 4.22.

The eye window observed with these settings was within the electro-optical specifications of the VTTX/VTRx modules and hence these settings were considered to be used for the final production testing.

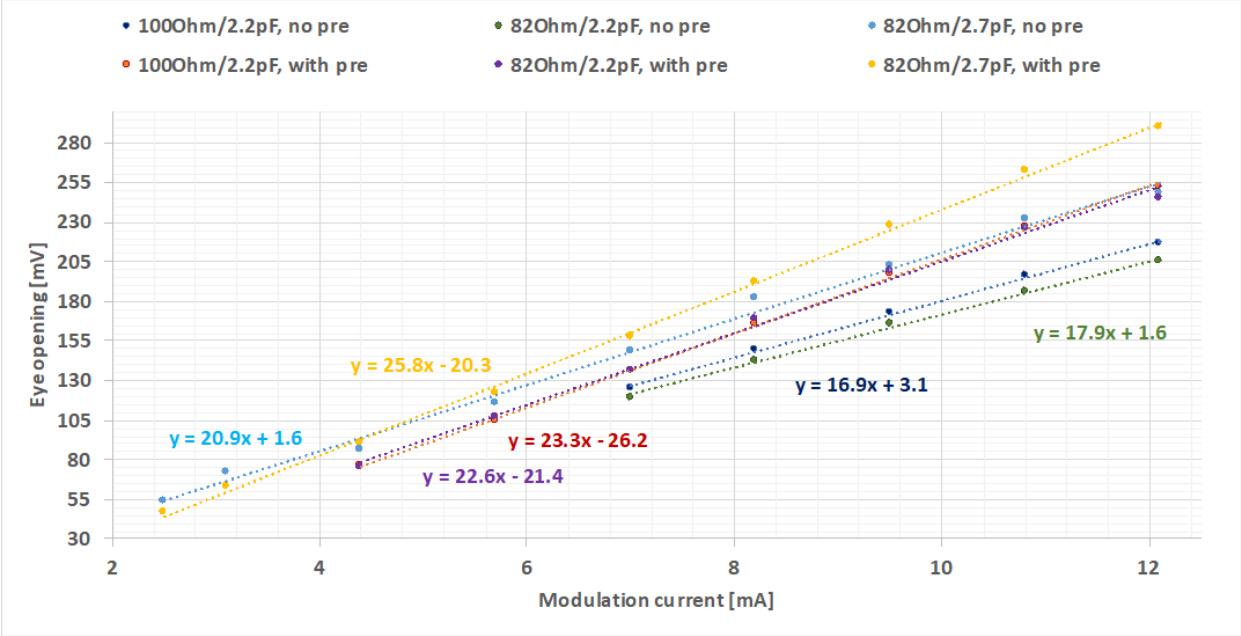

Figure 4.21: Effect of the CTLE passive components (R and C) and the GBLD parameters (modulation current and pre-emphasis) on the eye opening.Credit to Prof. Lars Eklund, University of Glasgow.

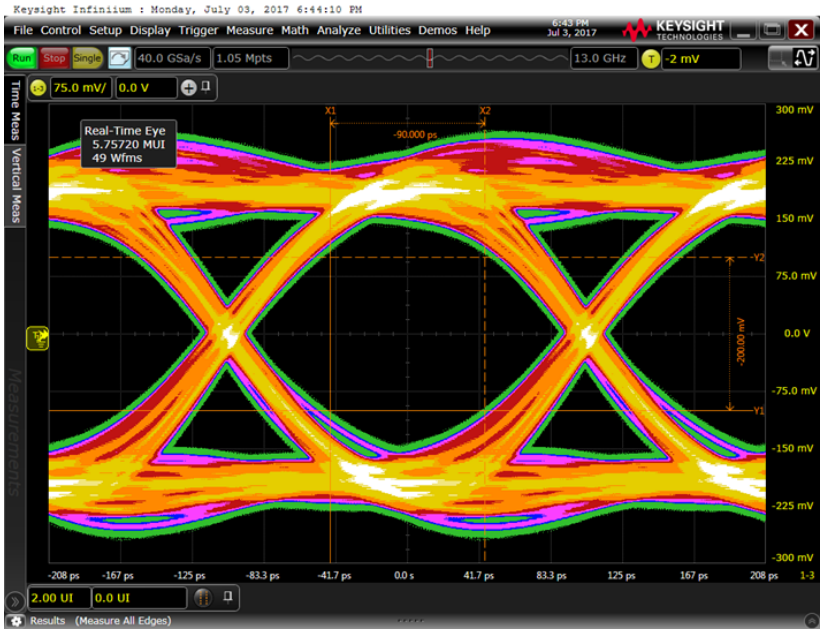

Figure 4.22: Eye diagram for the control link with tweaked GBLD settings: modulation current of 12 mA and pre-emphasis amplitude 6.7 mA with 50 ps. Eye opening with PRBS $2^7 - 1$: 200 mV opening over 90 ps (expected input of the VTTX/VTRx modules is 200 mV x 40 ps).

4.3 Full link characterisation

A full link setup for testing comprised the front-end Hybrid, Data tape, VFB and the OPB connected to a four port 13 GHz network analyser. The details of the tools and its features are described in Section 2.4. The project requires the production of 52 detector modules (2 front-end Hybrids per module), 208 data cables, 52 OPBs and 52 VFBs for installation in the final detector plus spares of each component. The full scale prototype designs can be seen in Figure 4.23.

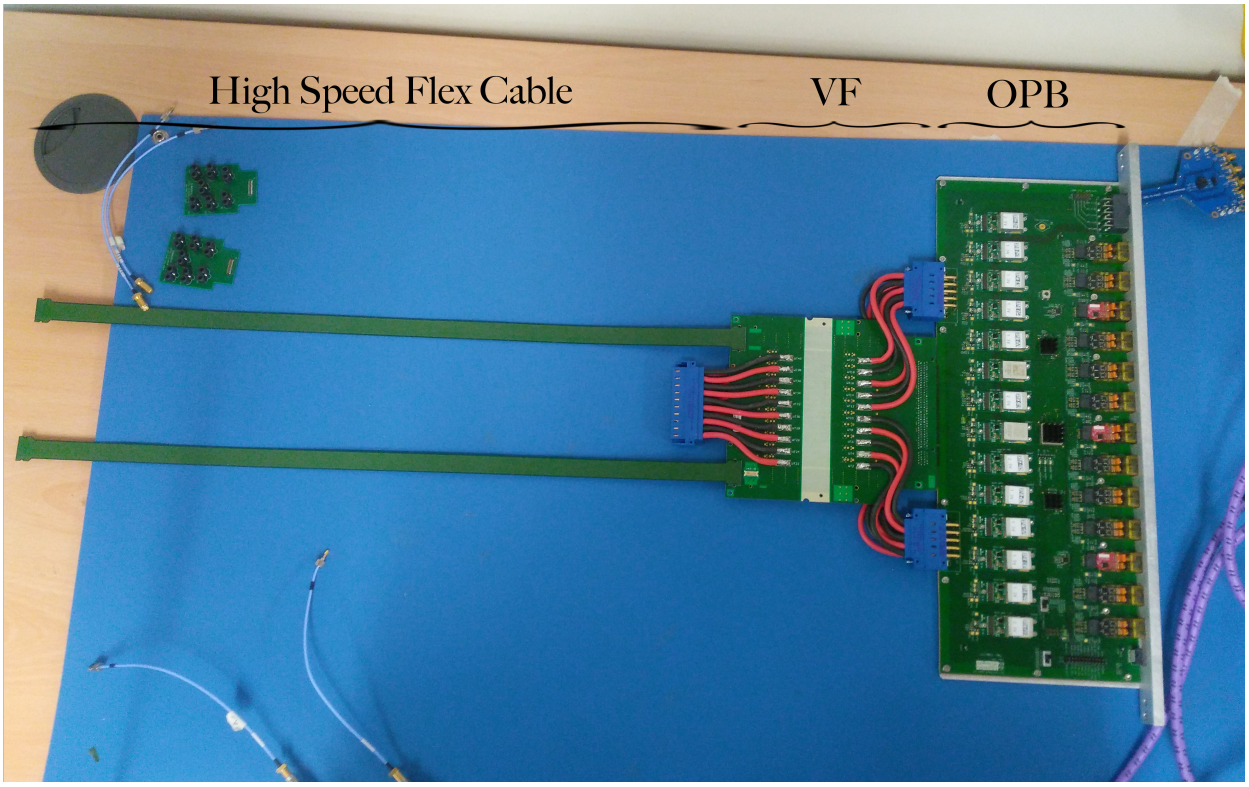

Figure 4.23: Setup showing the prototype desgins the full sized Opto Power board (OPB), Vacuum Feedthrough Board (VFB) and two Data tapes. The red and black cables connected to the blue connectors are the low voltage lines. The column of 14 DC/DC converters can be seen near the left hand side of the OPB. The GBTx is visible as the central black ASIC with its two SCAs located above and below. (Dark green) The ten VTTx modules can be seen on the far right of the OPB along with (red) the three VTRx modules. Image reproduced from [72].

The front-end Hybrid and the Data tapes could be measured individually but the VFB and OPB were measured together. This was done mainly because the test boards to extract the signals to the network analyser could not be connected to each board separately. The S-parameters of individual components and full link were measured. A plot of transmission loss S_{12} (dB) versus frequency (GHz) of each component on the link and the complete link is shown in Figure 4.24. The Data tape was found to have a loss of 3.9 dB, the Hybrid was found to have a loss of 2.3 dB while the VFB and OPB were found to have a combined loss

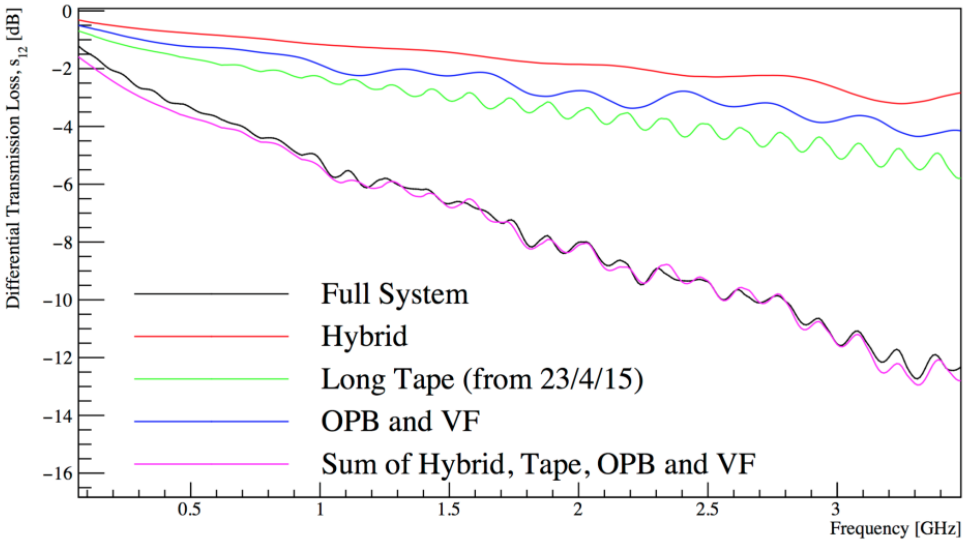

Figure 4.24: Signal loss as a function of frequency losses for (red) the hybrid, (green) data tape, and (blue) combined VFB and OPB and (magenta) the sum of all the component. This closely overlaps to the full system test (black). Plot reproduced from [72].

of 3.1 dB at the Nyquist frequency of 2.5 GHz with a combined transmission loss of 9.4 dB. The full system measures a loss of around 9.4 dB at base harmonic of 2.5 GHz. The eye diagram that was measured using a 5.12 Gb/s pseudo-random 7 bit pattern (PRBS $2^7 - 1$) for the full link showing an open eye as shown in Figure 4.25.

The results of the hardware testing was satisfactory and the work towards final stages of production for the On-detector electronics is ongoing. The Data tape production run is finished and the measurements for most of the data tapes are completed and results recorded. Credit to University of Santiago de Compostela, Spain for testing a considerable percentage of the production tapes. Relevant data for the same that includes S-parameters and impedance values are stored in a custom made database for future reference. The production version of the OPB is produced in a small batch and tested for its functionality using the most recent readout software. The testing is found satisfactory and meets the requirements with minor changes identified in the PCB layout. These were implemented and the design has been released for the final production.

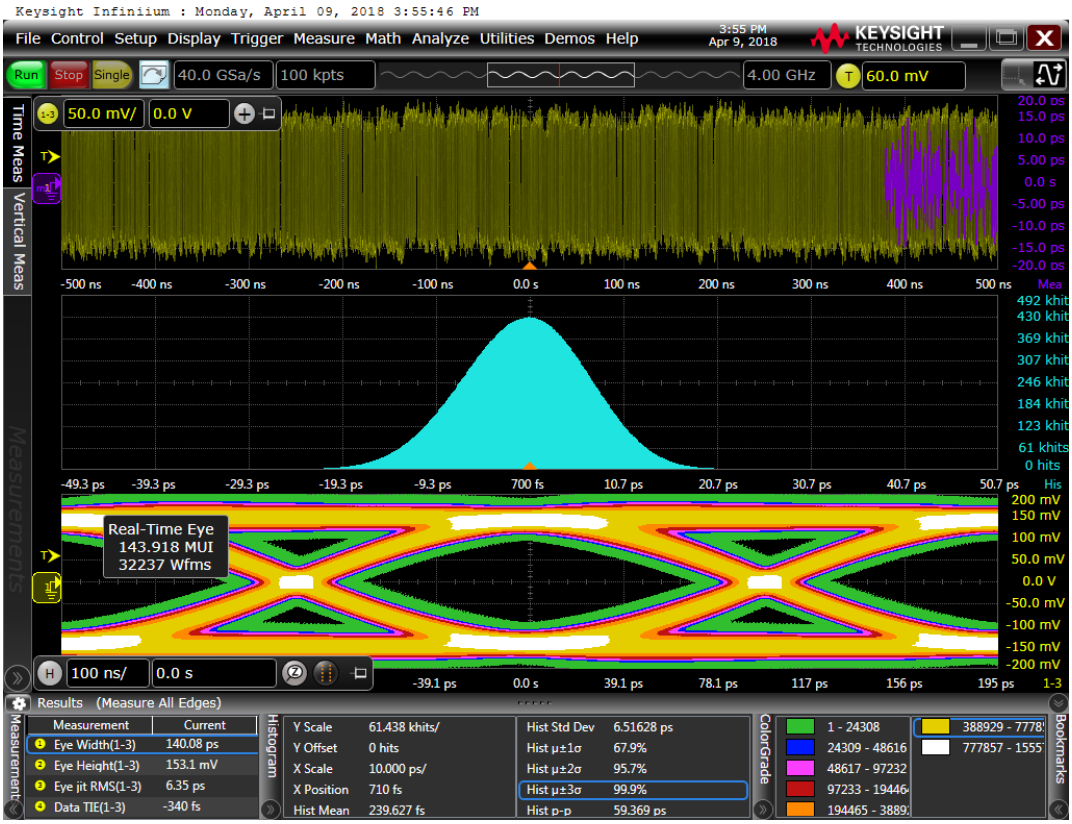

Figure 4.25: A screenshot of a typical trace under test from the pre-propoduction prototype using a PRBS $2^{31} - 1$ signal at 5.12 Gb/s. The top distribution shows the incoming data pattern in yellow and the offset of the signal from the difference between the measured and predicted arrival time of the signal in purple. The middle plot shows the timing distribution of the signal with respect to the threshold. The bottom plot shows the eye produced by the prototypes. The bottom left box shows the measured parameters for the eye diagram, the middle box shows the measured parameters of the signal offset and the bottom right box shows the numbers of signals corresponding to each colour scale in the eye diagram. Plots reproduced from [72].

2*Tape	Fluence (n_{eq}/cm^2))	
	Target	**Delivered**
1	2×10^{13}	4.43×10^{13}
2	2×10^{13}	4.61×10^{13}
3	2×10^{13}	3.67×10^{13}
4	2×10^{13}	1.97×10^{13}

Table 4.1: The test coupon irradiation measurements at the facility at Birmingham. The four measurements are from different areas in the box where the coupons were placed.

4.4 Radiation tests on Test coupons

The radiation numbers for the LHCb Velo Upgrade are estimated for an integrated luminosity of 50 fb^{-1}. Sensors and VeloPix ASICs will receive 8 x 10^{15} (1 MeV) neutron equivalent fluence or 4 MGray ionising dose. The hottest part of the data tape will receive 2 x 10^{13} (1 MeV) neutron equivalent fluence or 30 kGray ionising dose while the OPB will receive an ionising dose of 2.5 kGray. To study the effect of irradiation on the PCBs for both the data tapes and the OPB, test coupons were designed. These were 20 cm test PCBs with a pair of differential traces routed to Samtec CCH-J-02 test point connectors for measuring with the network analyser. The test coupons were added to the same panels as the Data tape and OPB during fabrication and the PCB layout is shown in Figure 4.26.

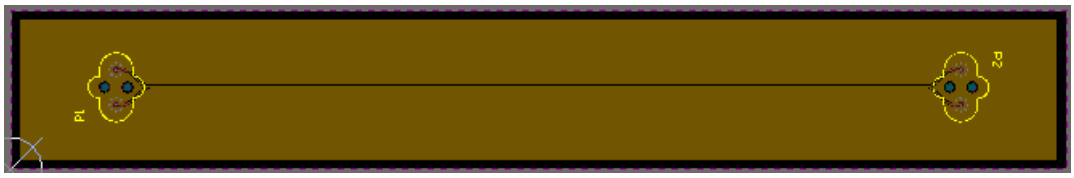

Figure 4.26: PCB layout showing the inner layer of the 3-layer stackup of the test coupon for radiation tests. The top and the bottom layer are continuous ground planes. P1 and P2 in the layout are high-speed test point Samtec connectors CCH-J-02 to interface to the network analyser for S-parameter measurements.

This activity was carried out at the irradiation facility in Birmingham [73] and co-ordinated by Dr. Laura Gonella, University of Birmingham and Dr. Kenneth Wraight, University of Glasgow. The details of the irradiation dose for the test coupons is shown in Table 4.1. The test coupons for both the OPB and the data tapes were measured before and after radiation to compare the difference in performance. The results of the OPB measurements are shown in Figure 4.27. The results of the Data tape measurements are shown in Figure 4.28. The discontinuities on the plots are due to the interconnection of the 100 Ω cables of the network analyser to the test-point connectors on the test coupon. The irradiation dose used for these coupon measurements is the dose which one end of the Data tape (closer to the beam) would receive and the remaining length of the tape and the OPB would receive

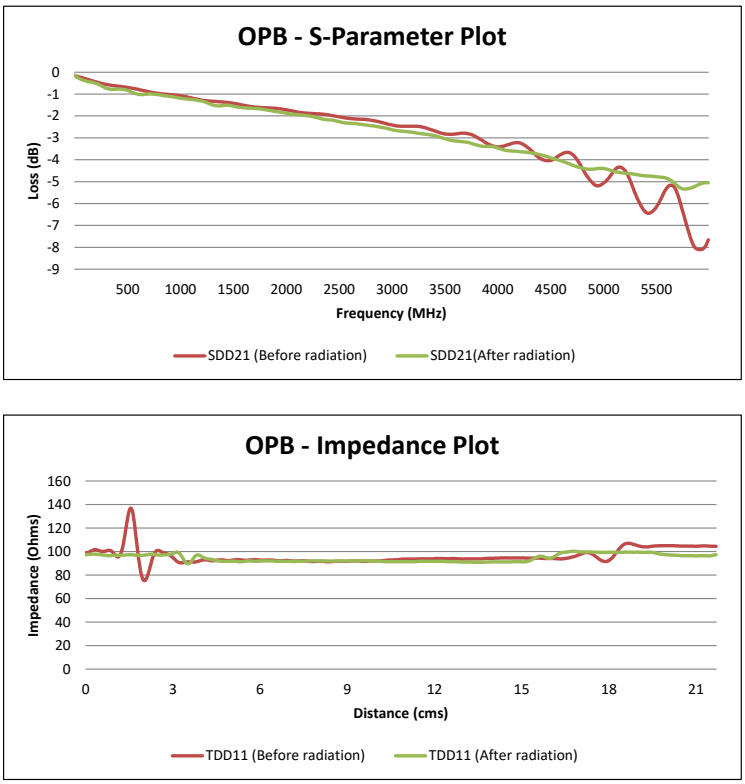

Figure 4.27: The measurement results of the OPB test coupon before and after radiation. Top - S-parameter plot with loss of approximately 2.2 dB and showing a marginal variation at Nyquist frequency of 2.5 GHz. Bottom - Pseudo-TDR measurement with impedance of 91 Ω.

a much lower ionising dose. As such, the variation in the S-parameter values are within the acceptable range specifications.

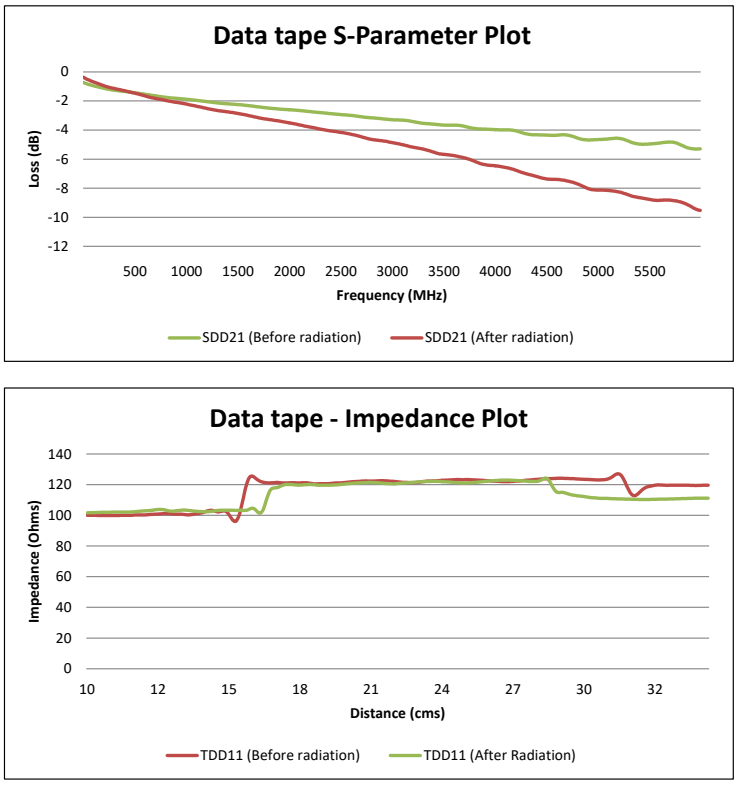

Figure 4.28: The measurement results of the data tape test coupon before and after radiation. Top - S-parameter plot with loss of 2.9 dB (before radiation) 4.1 dB (after radiation) and showing a 1.2 dB variation at Nyquist frequency of 2.5 GHz. Bottom - Pseudo-TDR measurement with impedance of approximately 120 Ω.

Chapter 5

ATLAS ITk (Inner Tracker) Pixel Designs

This chapter covers some of the components worked on to address issues with the material budget and high-speed data transmission for the ATLAS ITk Pixel On-detector electronics. With the increase in luminosity, data readout has to be done at much higher speeds and as such emphasis on the electronics readout system becomes important. Evaluation of the existing pixel outer endcap Crescent tape (detailed in Section 5.3) for high-speed transmission is covered. Methods and practices to improve the design to address high-speed transmission are discussed and measurement results are presented. With the increase in the number of readout channels on modules, the number of data cables increases. Investigation of low mass cables to reduce the material budget is ongoing. In detector systems, the powering scheme is point to point with individual power cables per module that gives rise to a large number of power cables as there are a large number of modules. A work around for this was to investigate the serial powering scheme [74] as a way of reducing the number of cables. More over using serial powering increases the voltage in the feed wire and therefore reduces the power loss due to joule heating in the system. The setup for implementing the serial powering scheme is explained and the results are shown.

For evaluating both the material budget and the powering scheme, the assembly of the FE-I4B [75] ASIC with Si-sensor is used in a single chip card (SSC) and PixFlex module. The SSC is a rigid PCB that hosts one FEI4 ASIC which has one serial differential readout channel while the PixFlex consists of 4 FE-I4 ASICs bump-bonded to a single monolithic Si-sensor, reading out 4 differential data pairs in parallel. The FE-I4 integrated circuit contains readout circuitry for 26880 hybrid pixels arranged in 80 columns on 250 μm pitch by 336 rows on 50 μm pitch. It is designed in a 130 nm feature size bulk CMOS process. The letter 'B' in FE-I4B refers to the design revision intended for production of the Insertable B-Layer [37] detector. Sensors must be DC coupled to the FE-I4 with negative charge collection. Each FE-I4 pixel contains an independent amplification stage with adjustable shaping, followed

by a discriminator with independently adjustable threshold. The ASIC registers the firing time of each discriminator as well as the Time over Threshold (ToT) with 4-bit resolution, in counts of an externally supplied clock, nominally 40 MHz. Information from all discriminator firings is kept in the chip for a latency interval, programmable up to 255 cycles of the external clock. Within this latency interval, the information can be retrieved by supplying a trigger. The data output is serial over a current-balanced pair (similar to LVDS). The primary output mode is 8b/10b encoded with 160 Mb/s rate. The FE-I4 is controlled by a serial LVDS input synchronized by the external clock. No further input/output (I/O) connections are required for regular operation, but several others are supported for testing.

5.1 Signal generation and Time over Threshold (ToT) in the FE-I4 pixel chip

The pixel sensor is an array of readout channels connected to a sensitive doped p-n junction. The sensor collects the charge freed in the bulk by energy deposition via ionization when an ionizing particle interacts with the sensor. The high voltage (-100 V) bias applied to the detector depletes the silicon to create a high field region throughout the silicon detector. This high voltage value was because the silicon was unirradiated and will be higher (-600 V) post irradiation. The freed charge carriers drift in this electric field towards the collecting electrode and this is read by the FE-I4 as an analogue signal. A threshold is used to limit the noise measured and the collected charge is proportional to the time over this threshold. A diagram summarising the ToT measurement is shown in Figure 5.1.

The ToT value recorded by each pixel gives information about how much energy the particle has deposited in the pixel volume while the hit pixel location and ToT value together give the approximate location the particle has travelled through the detector. The collected charge may be shared between multiple pixels in the array. To get a better precision a weighted average of pixels using the ToT value can be used. The ToT is calibrated with a known injected charge and not from an ionizing particle. S-curves [76] were obtained and the ToT for a given injected charge was extracted and added to a histogram. The histogram is expected to be Gaussian, a smaller standard deviation (sigma) shows a more uniform ToT throughout the pixel array. The mean of the ToT scan should be as close to the predetermined value as possible and a significant deviation from the expected ToT suggests that the pixel may not be functioning correctly: grounding, shorting or open. The plot produced is a histogram of the ToT values obtained for a given injection charge and a set of thresholds for an FE-I4 chip (thus the large number of entries). The ToT is a measure of how long a given signal pulse stays above a digitally set threshold which is given in units of the LHC's bunch crossing time (25 ns), meaning that a measured ToT of 8 implies that the signal stayed above threshold for 8 x 25 ns = 200 ns. The Figure 5.2 shows the ToT histograms for 7 different

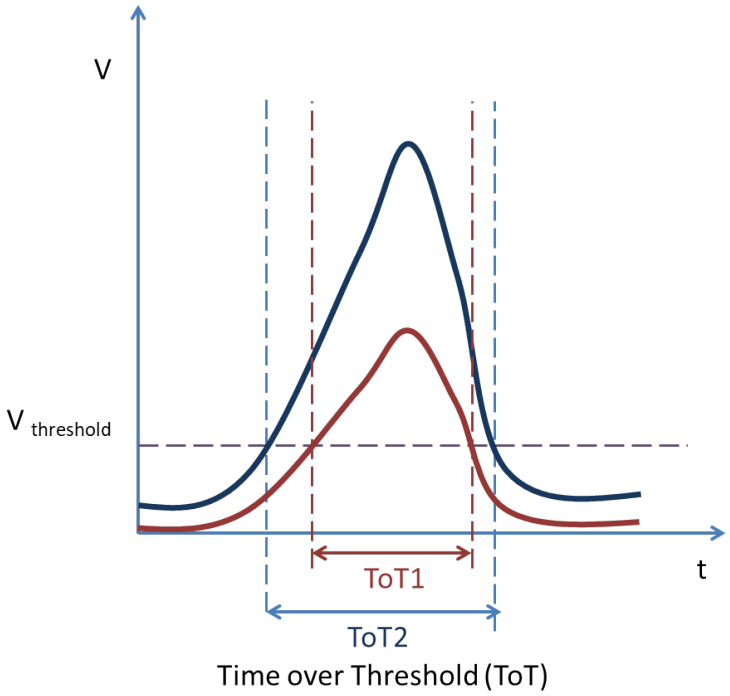

Figure 5.1: Time over threshold (ToT) digitizing scheme wherein a clock measures the amount of time the signal spends over the predetermined threshold value $V_{\text{threshold}}$. ToT1 would have a lower ToT value than ToT2, suggesting more energy was deposited into the pixel by the ToT2 interaction.

modules on the same graph. The FE-I4 is tuned using the various DACs in the chip that

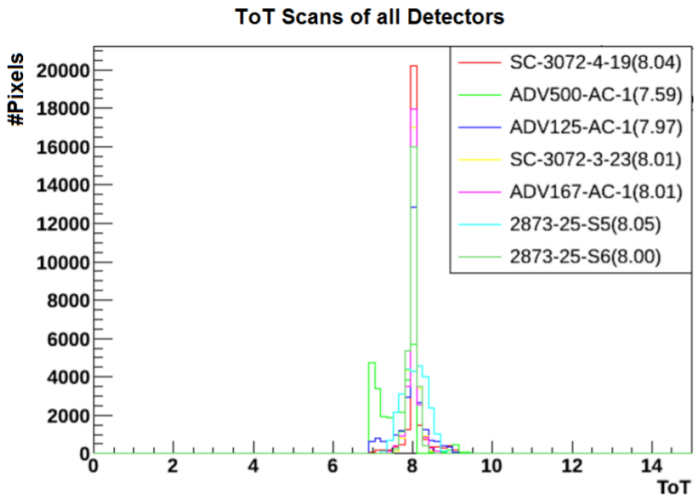

Figure 5.2: Time over threshold (ToT) scans of some operational detectors. The mean value of each detector was within an acceptable range of the pre-determined ToT value of 8 thereby indicating that all detectors were tuned properly.

control different settings; global and local threshold adjustment (TDAC) and global and local feedback current adjustment (FDAC)) in the chip to allow pixel variations to be removed.

5.2 Serial powering testing using Single Chip Card (SCC)

The Single Chip Card (SCC) is designed to readout an FE-I4 chip. The bond pads for the top row of pads are removed as these are typically not used by module developers. Removing these allows a cut out to be placed behind the chip to enable easier attachment of a cooling finger. The assembly is mounted to a Carbon Fiber Reinforced Polymer (CFRP) board. The edge of the board is covered with kapton tape to avoid any splinters. The PCB of a SSC is shown in Figure 5.3. The PCB design for the SSC was an update to the older version

Figure 5.3: Single Chip Card (SCC) with ASIC-Sensor assembly mounted on a Carbon Fiber Reinforced Polymer (CFRP) base board.

with a few changes in the schematic/layout as well as the fabrication techniques to optimise the design. This included changing some capacitor values based on testing results, moving traces and mounting holes on board to accommodate a new mounting assembly structure, improving fabrication process to achieve flatter wire bonding pads etc. The SCC design has wirebond pads for bonding the FE-I4 chip onto the PCB. A Molex connector was used to supply the power to the chip and an RJ-45 connector was used for carrying the LVDS control and data signals to and from the chip. In addition, a KEL[1] connector is mounted on the PCB that is used to interface to a PC for externally controlling the FE-I4 features. A LEMO[2] connector was used to provide the high voltage for biasing the sensor. Additional test pads and connectors were added to ease the testing process. Provisions were added on the PCB for implementing and testing features like shunt LDO, setting chip ids, etc.

The ATLAS trackers use parallel powering schemes that results in massive cable cross

[1] https://www.kel.jp/files/topics/490_ext_19_en_0.pdf
[2] https://www.lemo.com/pdf/EPL.00.250.NTN.pdf

sections and low efficiency due to voltage drop over cables. In this scheme, the chips in a module are powered in parallel and the drop over cables further increases with the number of modules added in parallel and hence a serial powering scheme was investigated. In the setup to test the serial powering scheme, a stand alone bench-top readout setup comprising the High-Speed In Out (HSIO)-II interfaced with Reconfigurable Cluster Element (RCE) [77] that is suitable for medium scaled lab and testbeam operations, was used. The HSIO-II is interfaced to the IBL adapter Board that hosts the mezzanine cards.
In order to be able to connect multiple SCCs for serial powering, an RJ45 breakout Board was designed. This board mapped the high-speed cable coming from the IBL adaptor Board to 4 individual connectors that further connected to sixteen RJ45s. These connectors could interface to 16 SCCs for serial powering. The apparatus for serial powering is as shown in Figure 5.4. The SCC had to be adapted to work in the serial powering mode and the changes

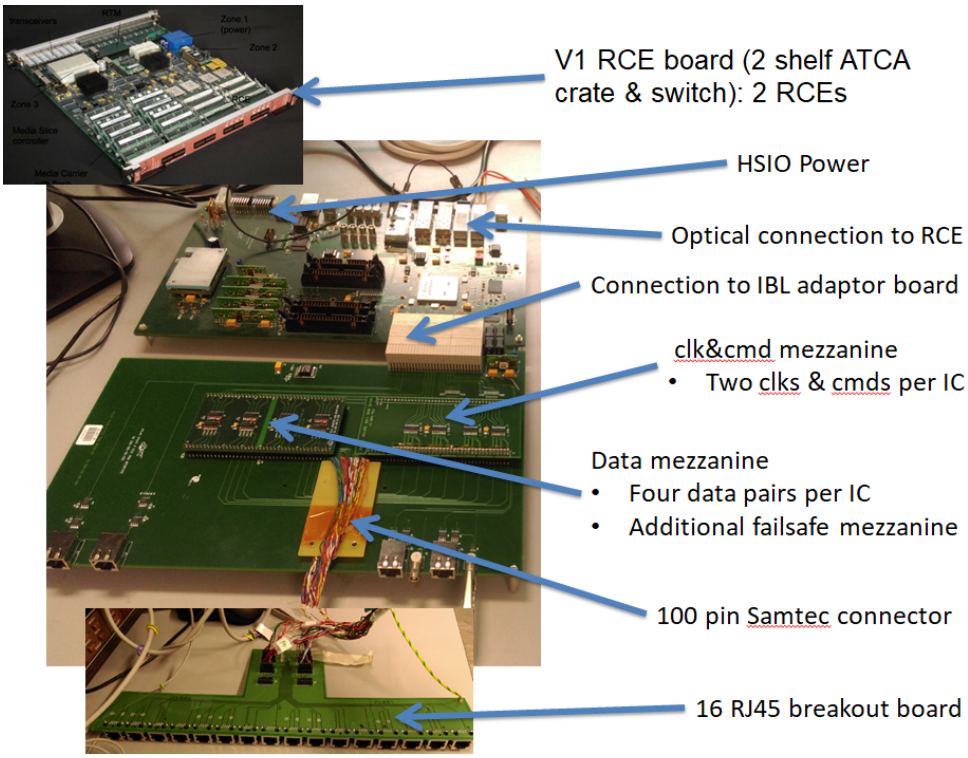

Figure 5.4: Serial powering apparatus with RCE, HSIO-II, IBL adaptor Board, RJ45 breakout Board that interfaces to Single Chip Card (SCC).

needed to be done were as follows-

- Enable the Shunt Low Dropout (SLDO) feature on the FE-I4 chip and connect jumpers on the SCC to connect the voltage reference to the bandgap reference voltage for analogue and digital supply.
- Add Rext in parallel to the internal resistor (R3) to reduce the effective resistance and increase the reference current definition at analogue and digital regulator for the serial powering application. This is detailed in 5.2.

- Add capacitors for AC coupling of clock (clk)/command (cmd) and data.

The Shunt-LDO regulator is a combination of a low-drop linear voltage regulator and a shunt regulator. The Shunt-LDO regulator can be configured as a pure linear voltage regulator for usage in a conventional voltage based supply scheme. In addition, the regulator provides dedicated shunt circuitry which can be enabled for application in a current based serially powered supply scheme. In a serial powered scheme, modules are placed in series and powered by a constant current source. Shunt regulators are used at module level to generate the supply voltage out of the current supply. The Shunt-LDO regulator scheme combines the capability of Low drop-out regulators to generate a constant supply voltage with the feature of shunt regulators to assure a constant current flow through the device. When modules are powered serially, a potential hazard that has to be avoided is the break of the supply chain. Dedicated circuitry is therefore needed to bypass a broken module. A regulation scheme is required where the devices are capable to operate in parallel at module level and to shunt additional current in case of a device failure. Furthermore, a lower supply voltage is very often applied to the digital part of the readout ASIC with respect to the analogue part, to reduce the current consumption of the digital circuitry. Hence parallel operating regulators that generate different supply voltages out of the single current supply are very beneficial for this powering scheme and reduce the implementation effort. There are two Shunt-LDO regulators in FE-I4B, one on the far left (back row of bond pads, intended to supply the analogue voltage) and the other on the far right (intended to supply the digital voltage). A simplified circuit of the Shunt-LDO regulator is shown in Figure 5.5. and the Shunt LDO

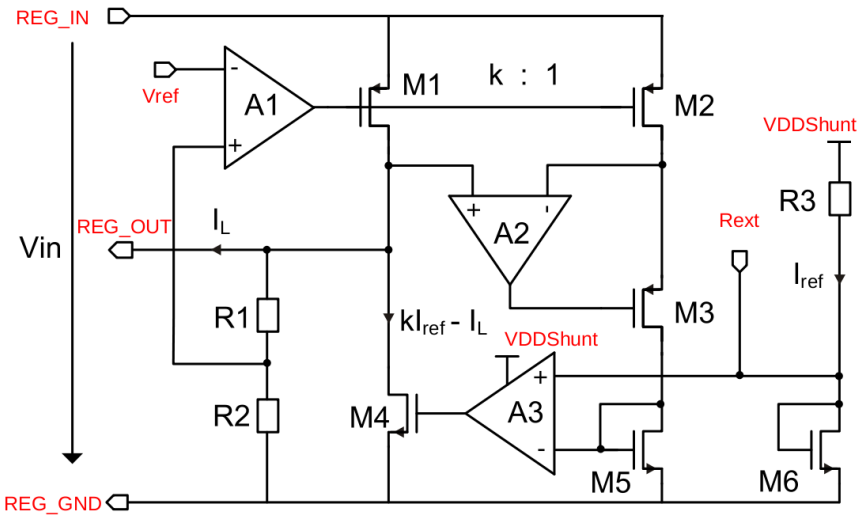

Figure 5.5: Low Dropout (LDO) regulator with Shunt capability (Shunt-LDO) as implemented in FE-I4B. Image reproduced from [78].

pin specifications are listed in Table 5.1. The LDO regulator part is formed by the error amplifier A1, the PMOS pass transistor M1 and the voltage divider formed by the resistors R1 and R2. In a voltage based supply scheme, the unregulated input voltage is applied to the

Ports	Type	Nominated value	Description
REG_IN	Power	1.4 - 2.5 V/500 - 600 mA	regulator voltage/current input
VDDShunt	Power	1.4 - 2.5 V	supply voltage of shunt circuitry
REG_GND	Ground		local ground / shunt current output
REG_OUT	Power	1.2 - 1.5 V	regulator voltage output
Vref	Analogue	600 - 750 mV	reference Voltage (REG_OUT=2Vref)
Vbp	Analogue		bias voltage for PMOS transistor
R_ext	Analogue		port for external reference resistor

Table 5.1: Shunt-LDO circuit pins as implemented in the FE-I4B. Table reproduced from [78].

REG_IN port which is referenced to the local ground. The regulator generates an output voltage REG_OUT = 2Vref, where Vref is the reference voltage which is provided to the inverting input of the error amplifier A1. In a current based supply scheme the supply current is flowing into the REG_IN port. The bypass transistor M1 is biased to create a voltage drop VDS between regulator input REG_IN and the output voltage terminal REG_OUT such that the wanted output voltage is generated with respect to local ground. For shunt operation, the transistor M4 is added to provide an additional current path to REG_OUT. Transistor M4 is controlled to drain all current which is not drawn by the load connected to REG_OUT. For this purpose the current flow through transistor M1 is compared with a reference current which is defined by resistor R3. A fraction of the current flowing through transistor M1 given by the aspect ratio k of the current mirror formed by transistor M1 and M2, is drained into the gate-drain connected transistor M5. The amplifier A2 and the cascode transistor M3 are added to improve the mirroring accuracy. The reference current which depends on the input potential REG_IN is drained into the gate-drain connected transistor M6. The reference current is compared to the fraction of current flowing through transistor M1 by use of the differential amplifier A3. If the current drained to transistor M6 is smaller than the reference current, the shunt transistor M4 is steered to draw more current and vice versa. By this means, a constant current independent of the regulator load is flowing through transistor M1 with a value defined by

$$I\mathrm{in} = (\mathrm{kV_{in}} - \mathrm{V_{thM6}})/\mathrm{R3}$$

where V_{thM6} is the threshold voltage of transistor M6. The resistor R3 is integrated internally and has a resistance of 8 K (16 K) for the analogue (digital) regulator of FE-I4B. These values have been chosen to reduce current draw fluctuations in the IBL implementation, but are too large (too little current) for a serial power application. Resistor R3 is used for the reference current definition if the VDDShunt port is connected externally to REG_IN. However the reference current can be increased to any desired value by adding an external resistor in parallel to R3, between Rext and REG_IN (note that VDDShunt must still be powered for the shunt circuitry to work). Alternatively, a resistor from Rext to REG_GND will

Resistor	Analogue	Digital
R3 (internal resistor)	8 K	16 K
Rext	5.1 K	20 K
Reff	3.11 K	8.89 K

Table 5.2: External resistor (Rext) and effective resistance (Reff) for analogue and digital regulator for FE-I4B.

steal current from R3 and will therefore reduce the shunt current (a short to REG_GND will zero the shunt current). With 2 K resistance (parallel sum of external resistor plus R3), a maximum shunt current of 500 mA can be reached. Shunt operation is disabled by shorting the Rext and VDDShunt ports to the local ground port REG_GND. Since the Shunt-LDO regulator has no integrated voltage reference circuit, the reference voltage which defines the REG_OUT voltage has to be provided externally (the FE-I4B has 4 reference voltage outputs to choose from for this purpose). However biasing currents are generated by an internal biasing circuit. The generated biasing voltage can be measured on the Vbp port. The Shunt-LDO regulator requires an external capacitor of 2.2 nF connected to the REG_OUT port for stable operation. In simulation, capacitors with an Equivalent Series Resistance (ESR) of about 1 Ω are recommended for stable regulation, but on the PCB, low ESR ceramic capacitors can be used without problems. The simulated output resistance of the regulators is significantly lower than measurements of actual devices. The Shunt-LDO has an external jumper for both analogue and digital side called Shunt1 and Shunt2 on the SCC. A jumper head had to be connected between the 2 pins that connect the Rext to the VDDShunt voltage. The Rext in the setup is set to the value shown in Table 5.2.

AC coupling of the SCC is required for the serial powering scheme. The data, clk and cmd have to be AC coupled so each module does not see the voltage shift as compared to the previous module in the chain. The AC coupling for clk and cmd was implemented on the SSC while that for the data was on the receiving end on the HSIO side. This was done by using the interface card designed to AC couple the data and was mounted on the IBL adapter board as a mezzanine card.

5.2.1 Requirements for running multiple SSC in serial powering scheme

As summarised in the above section, in addition to setting up the FE-I4B to be configured for serial powering, some mezzanine cards were designed to test the serial powering scheme and are described below-

RJ-45 breakout Board : This board is an interface between the readout HSIO board and the SCC. The design of this board and the assembled PCB is shown in Figure 5.6. This

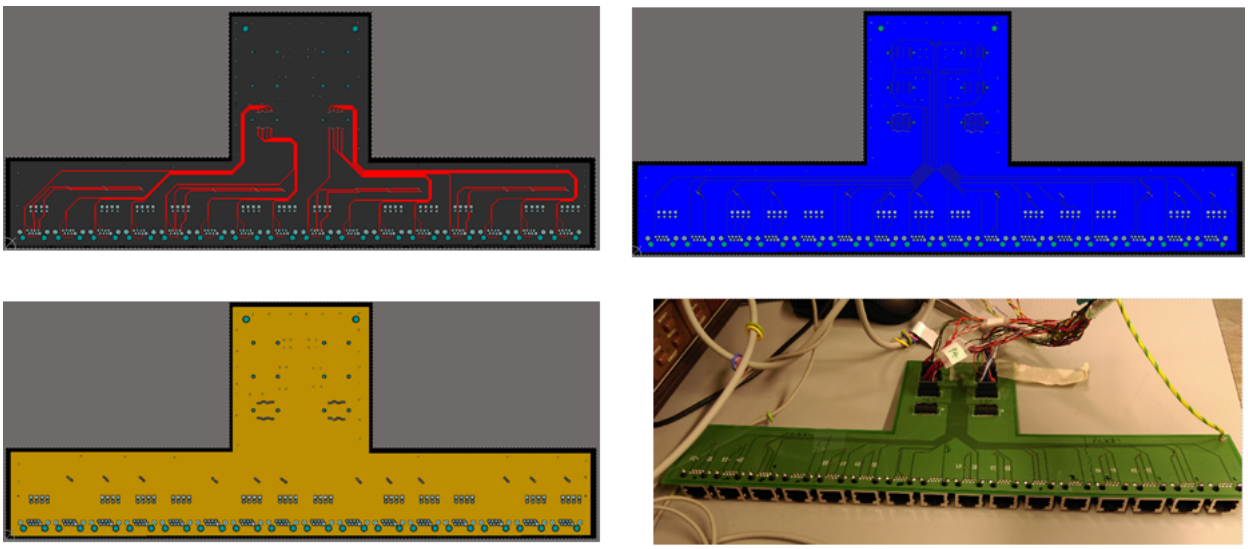

Figure 5.6: RJ45 breakout board for multi-module testing showing the PCB layout and the assembled PCB. Top left - Top Layer, Top right - Bottom layer, Bottom left - Inner ground plane and Bottom right - Assembled PCB.

PCB was designed as a 3-layer build with FR4 material. The data and control signals were routed following high-speed design guidelines such as length matching, grounding between differential pairs and dedicated ground reference to achieve a characteristic impedance of 100 Ω differential for each pair of traces. A continuous ground plane on the inner layer was used as a ground reference for the signals that run on both top and bottom layer.

AC Coupling board : This board was designed as a mezzanine card that connects on the IBL adaptor Board. This is a board that has AC coupling capacitors, to AC couple the data that is read out from the ASIC on the SCC. The board sits between the IBL adaptor Board and the test card driver-receiver board. The test card comprises high-speed differential line drivers to carry LVDS signals to the HSIO readout board. The PCB for this board is a 2-layer build with FR4 material. The CMOS output of the LVDS receiver might be in an undefined state and may reach an intermediate state of increased current consumption or even start oscillating. This condition can arise if the LVDS receiver inputs are left open and are unused, if the LVDS driver is powered off, if the transmission line is broken or if the LVDS receiver inputs are shorted. The circuit for mitigating this issue is called a fail safe circuit and is present on the LVDS receiver at the FE-I4 chip. This circuit was implemented as a provision for the data lines after the AC coupling capacitors on the PCB. Figure 5.7 shows the schematic for one of the data pairs. The design of the AC coupling board and the assembled PCB is shown in Figure 5.8.

The bench setup is shown in Figure 5.9 showing the connections between different components to test the serial powering scheme.

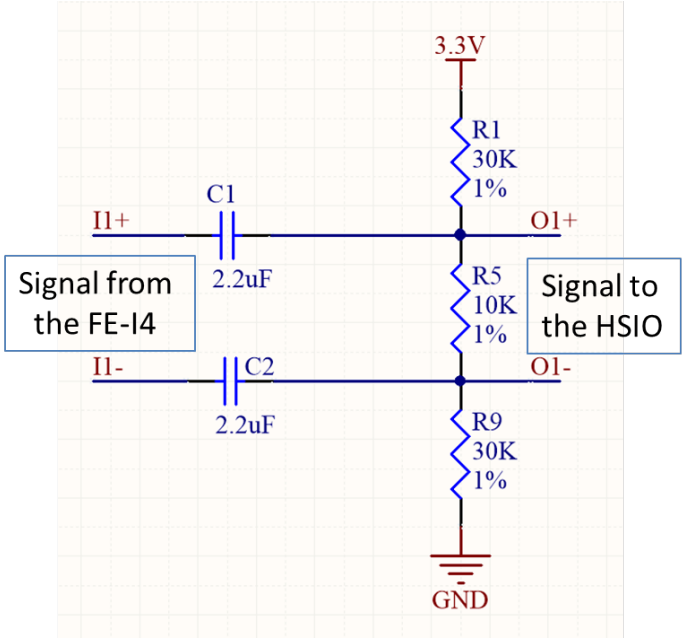

Figure 5.7: AC coupling capacitors and the fail safe circuit implemented on one of the data pair. This circuit is identical for all the 16 data pairs.

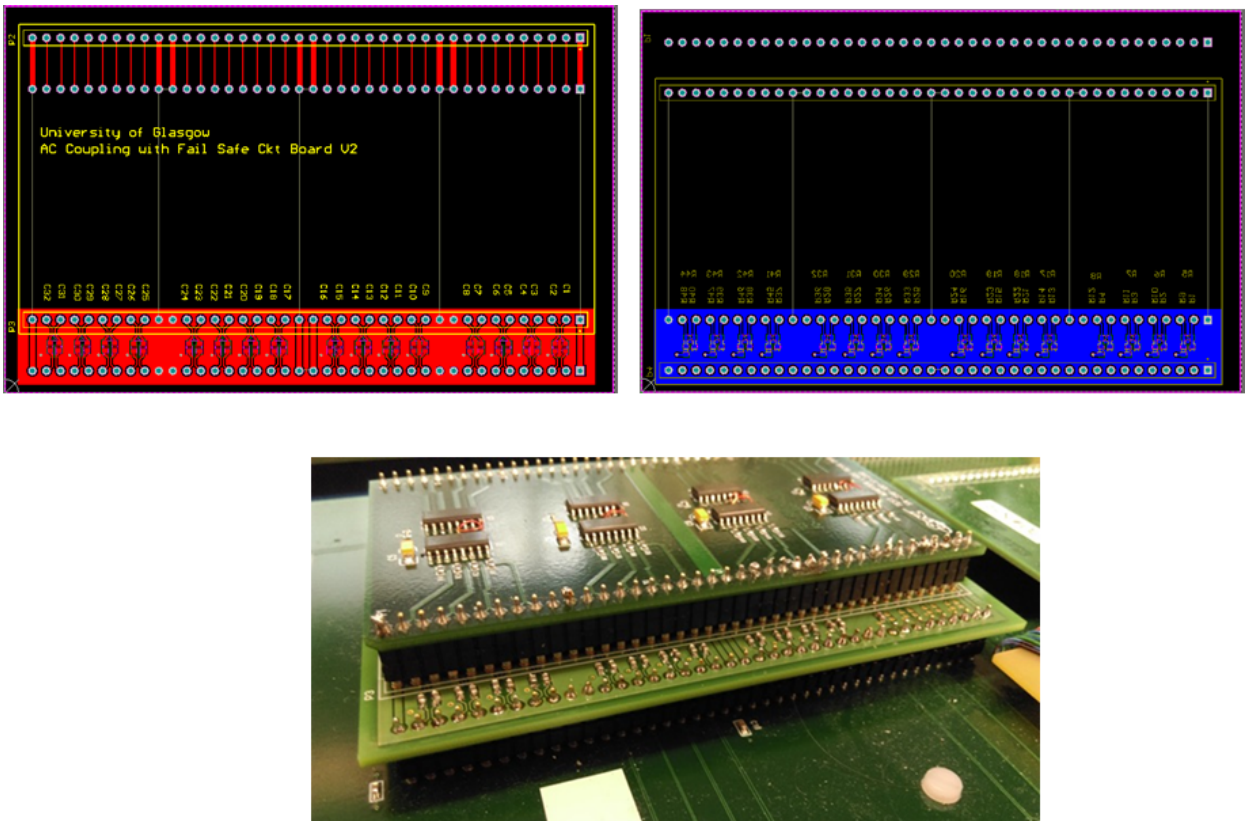

Figure 5.8: AC coupling Board. Top left - Top layer, Top right - Bottom layer, Bottom - Assembled PCB as a mezzanine card between the HSIO and the driver-receiver board.

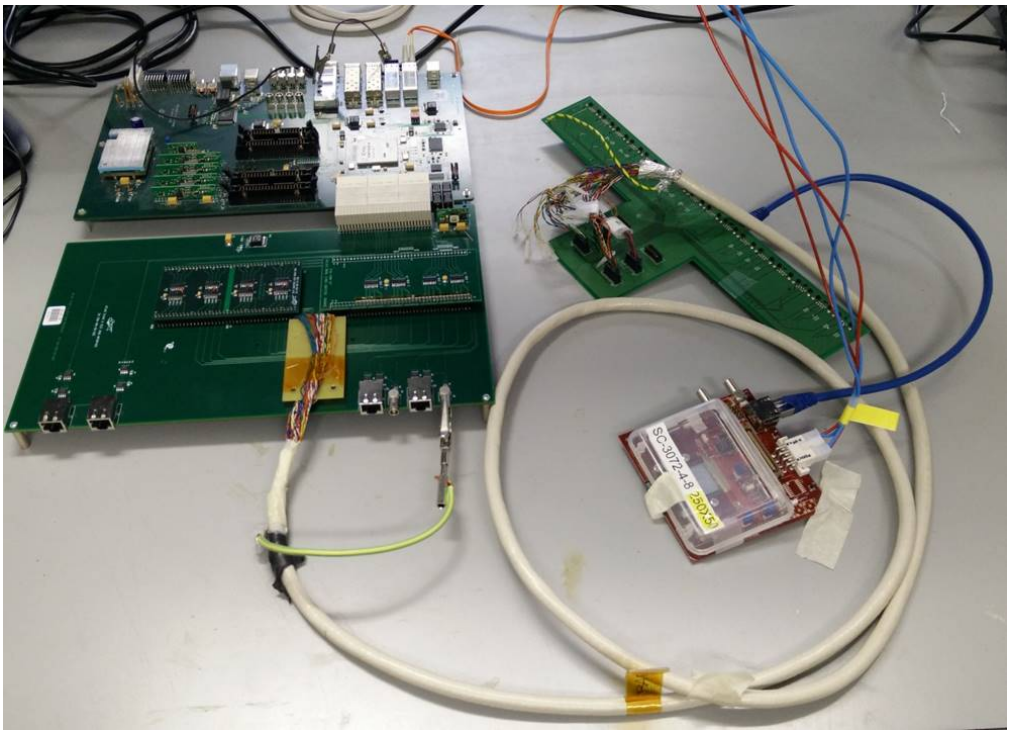

Figure 5.9: Serial powering setup with HSIO and RCE, RJ45 breakout board and Single Chip Card (SCC).

5.2.2 Connection of High Voltage (HV) return to the Low Voltage (LV) return

In the serial power chain the ground of a module becomes the input supply to the next module in the chain. Each silicon detector must have a HV supply. This can be achieved using a floating HV supply for each detector, referenced to the current return path of the serial powering loop. The schematic of the serial powering chain and connections of the HV and LV returns is shown in Figure 5.10. This was implemented on the SCC on vertical header

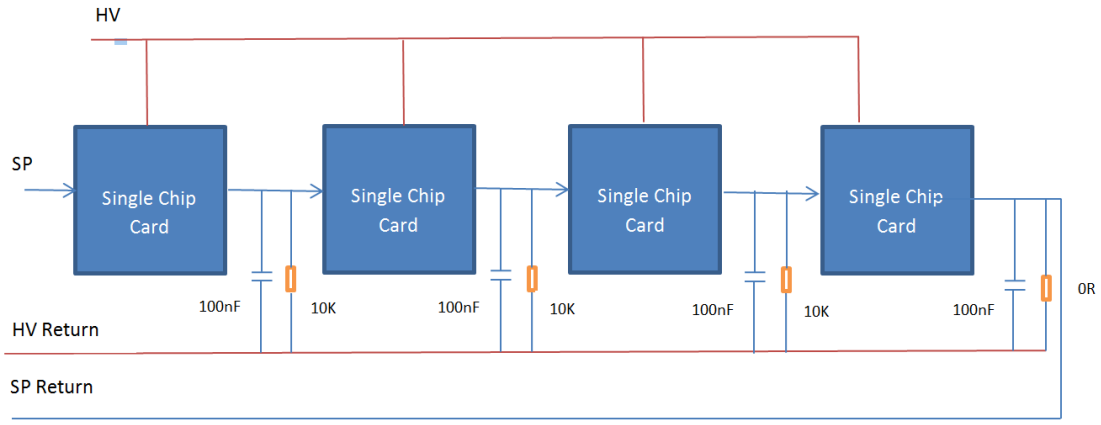

Figure 5.10: Schematic showing High Voltage (HV) and Low Voltage (LV) connection in the system for multi-module testing in serial powering scheme.

(HV_RTRN) pins as highlighted in Figure 5.11.

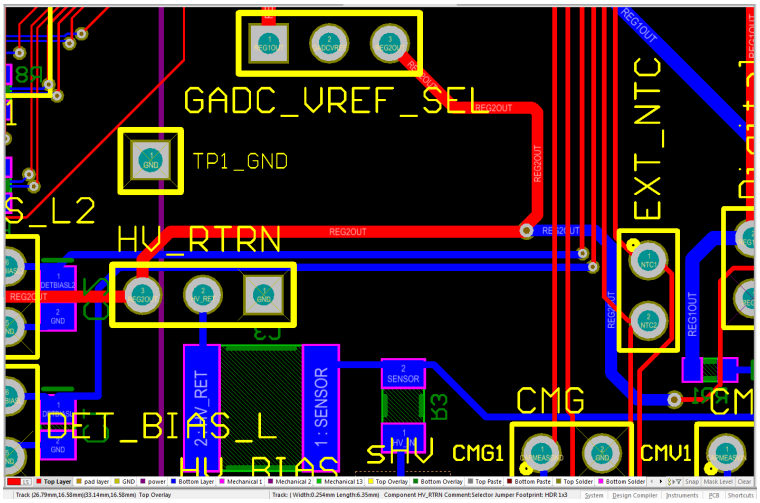

Figure 5.11: Implementation of HV and LV connection on Single Chip Card (SCC).

5.2.3 Measurements of Single Chip Card (SCC) with Serial powering

For taking measurements, a clock and command signals were sent by the computer into one of several RCEs. An optical cable was used between the RCE and the HSIO to avoid grounding issues that could arise. This further connected to the HSIOs FPGA and via the cmd/clk mezzanine, the high-speed cable, the RJ45 breakout Board and onto the SCC. The data signal was then returned through the HSIO's FPGA and sent through the optical connection to the RCE board. The RCE board used its own FPGAs to create histograms from the device data. Calibration Graphical User Interface (CalibGUI) [79] was the application used to control the experimental apparatus from a computer. CalibGUI allows the user to manually set the in and out ports of the RJ45 breakout Board that connects to the modules, the choice of RCE as well as the configuration file to be used. For a detector to measure any useful data the threshold of the pixel array must be as uniform as possible, as any significant aberrations in the array would display false data. In order to test the FE-I4 modules a pre-defined list of commands to the chip (primlist) tunes the threshold of each individual pixel to a selected value, then a threshold scan measures the actual threshold response from each pixel. Each pixel was injected with a known charge and the ToT for each pixel was measured. In order to fully calibrate the pixel front-end chips, a series of calibration scans were run by amending the configuration files until the chip becomes optimally tuned as the user desires. The primlist feature of the calibGUI does this automatically by way of loading in a file with the desired calibration scans and their parameters. Individual scans performed on the module could also be selected using the CalibGUI. The setup is first powered with the LDO mode with one SCC. The ToT and the threshold scan results are shown in Figure 5.12. It was observed

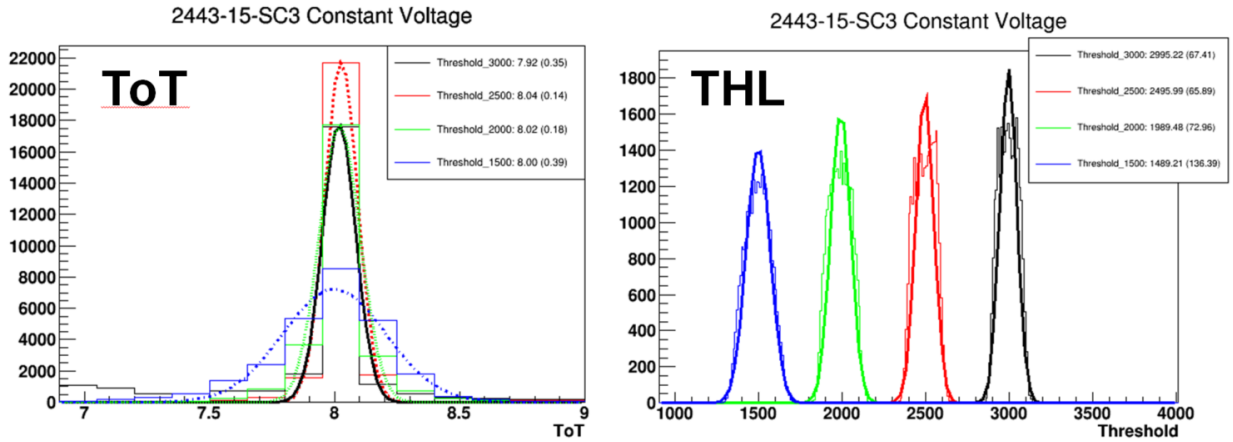

Figure 5.12: Left - Fitted Gaussian scans for Time over Threshold (ToT). Legend: predetermined threshold (mean ToT (sigma)). Right - Histogram of the $V_{\text{threshold}}$ value from the S-curve obtained from threshold scans for different values of the set global threshold value. Legend: predetermined threshold (mean threshold (Sigma)), for a detector in LDO mode.

that the width of the distributions reduce with increasing threshold values. A ToT of 8 and a threshold (equivalently units of electrons) of 3000 e gave best results. For testing in Shunt-LDO mode, the LV power source was changed to constant current and the observed results are as shown in Figure 5.13. The Rext were set to 5.1 K (analogue) and 20 K (digital)

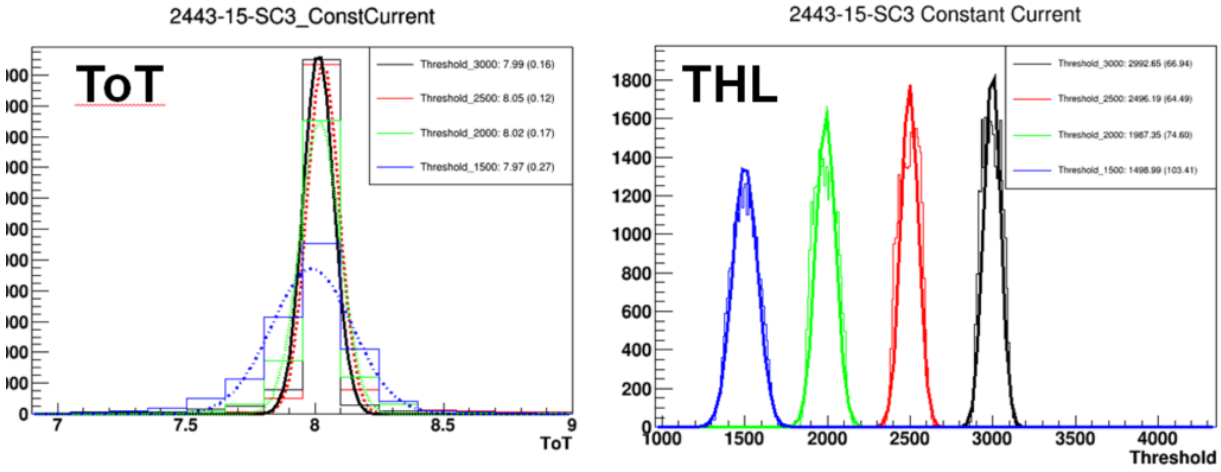

Figure 5.13: Left - Fitted Gaussian scans for Time over Threshold (ToT). Legend: predetermined threshold (mean ToT (sigma)). Right - Histogram of the $V_{\text{threshold}}$ value from the S-curve obtained from threshold scans for different values of the set global threshold value. Legend: predetermined threshold (mean threshold (sigma)), for a detector in Shunt LDO mode.

and the current supply the range of 350 mA-500 mA. The results were consistent with the constant voltage scan and the scans improved with an increase in threshold value.

The same setup was then used to serially power devices; there were three modules in series and the output observed on one detector was as shown in Figure 5.14. The results were consistent with that of separately powering each module. The summary plot comparing the scans for the three powering schemes described above are shown in Figure 5.15.

While the results obtained showed that the serial power chain results were consistent with individually powered modules, the apparatus was limited to 3 modules that could be tested due to issues in the apparatus. There were some grounding issues observed when simultaneously tuning chips in serial powering mode. The issues were not consistent and efforts were made to improve this by trying to ground and shield the various boards in the setup to improve results. Out of the few techniques tried, it was observed that the position of the module on the RJ45 board influenced the results. The RJ45 board received 4 pairs of clk and cmd signals from the HSIO board and these 4 pairs were routed to 4 quadrants in order to be able to connect 16 SSCs. The 4 RJ45s that shared one pair of clk and cmd made up one quadrant. Figure 5.16 shows the position of the modules on the RJ45 board.

When modules were placed in position as shown in the Case 1 or Case 4, where they were connected in the same quadrant, there were issues seen with the scans. When modules were connected as in Case 2 or Case 3 , the scans were good. Good scan results were seen when the

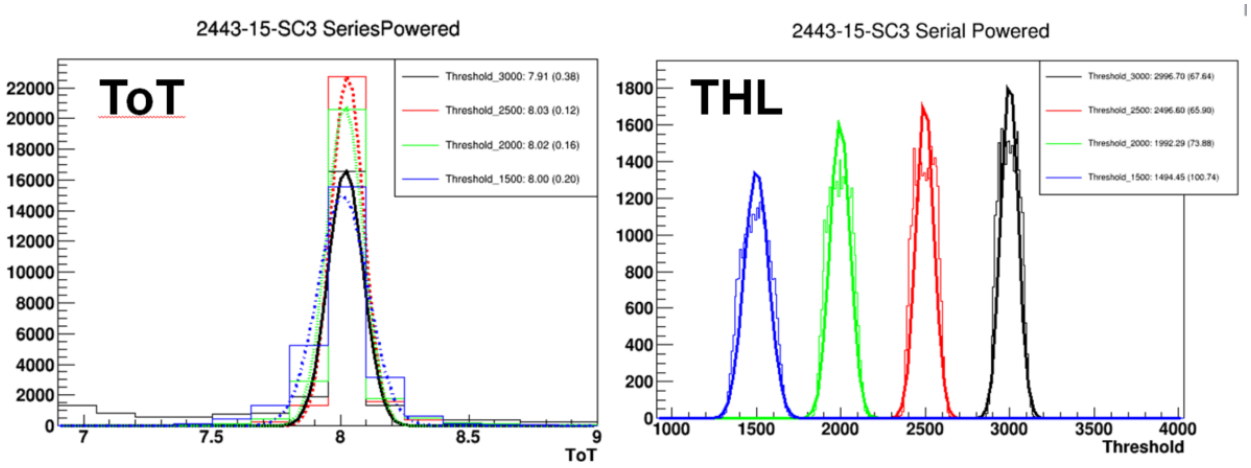

Figure 5.14: Left - Fitted Gaussian scans for Time over Threshold (ToT). Legend: predetermined threshold (mean ToT (sigma)). Right - Histogram of the $V_{\text{threshold}}$ value from the S-curve obtained from threshold scans for different values of the set global threshold value. Legend: predetermined threshold (mean threshold (sigma)), for a detector in serial powering mode.

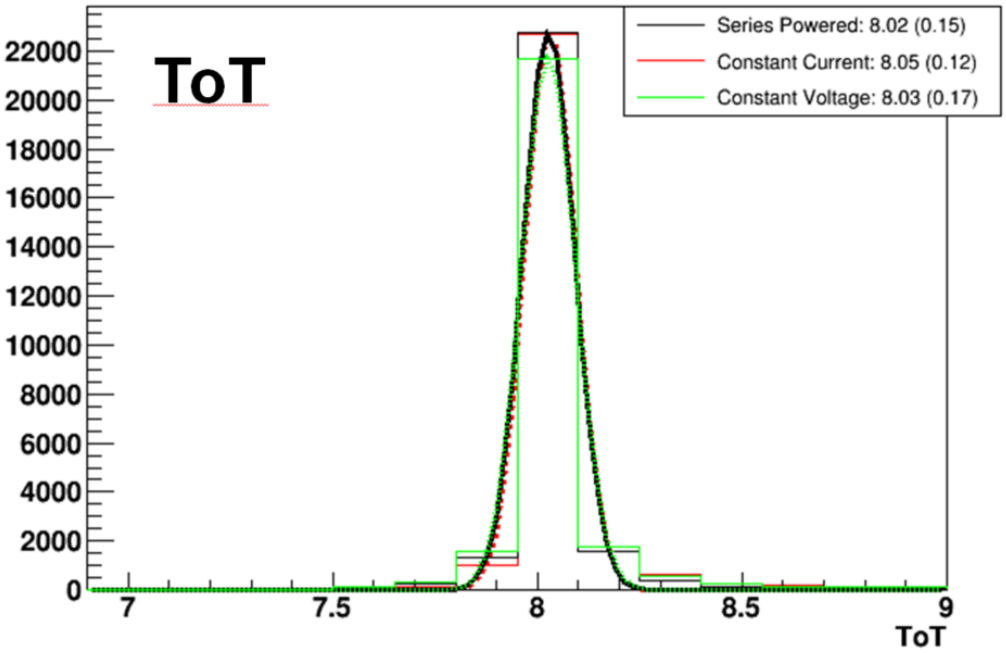

Figure 5.15: Overlap of a single tune scan for the constant voltage, constant current and serial powering and all the 3 overlap for 8 ToT@20k and threshold value=2500. Legend: powering modes (mean ToT (sigma)).

modules were placed adjacent to each other but between different quadrants (Case 3). There was no clear conclusion on what caused this effect as it was not always consistent but it could have been related to the clk and cmd sharing between 4 modules in each quadrant. This issue was avoidable by placing modules as Case 2 or Case 3. Due to this limitation, 3 module could be connected in serial powering chain in the existing setup but the serial powering scheme

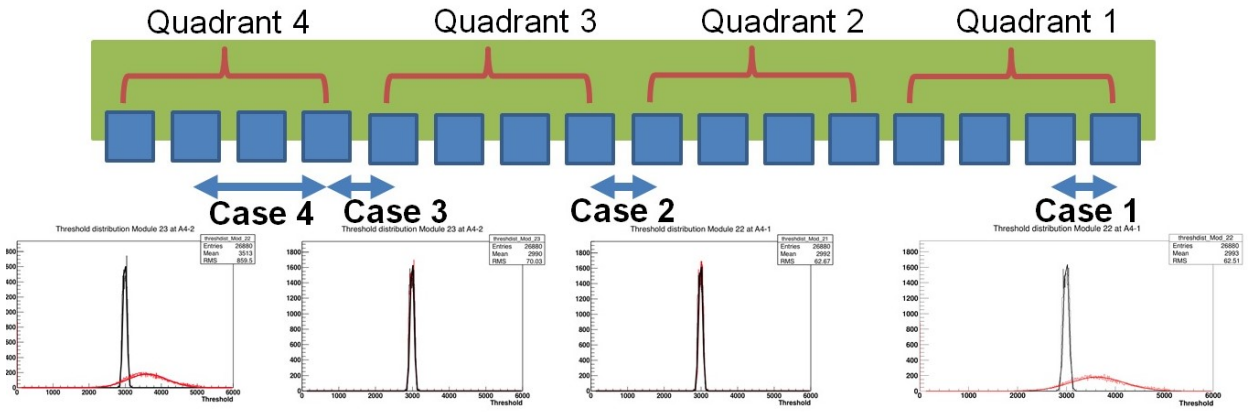

Figure 5.16: Position of the modules on the RJ45 breakout Board and the influence on the scans.

worked with the 3 modules connected nnd the results were found satisfactory. The Gaussian histograms produced showed a smaller sigma and a more uniform ToT throughout the pixel array. The mean of the ToT scan was also close to the predetermined value and consistent for the constant voltage, constant current and serial powering chain. The measured output noise did not show a significant noise increase and this was used as an essential parameter to determine if the serial powering scheme worked as expected.

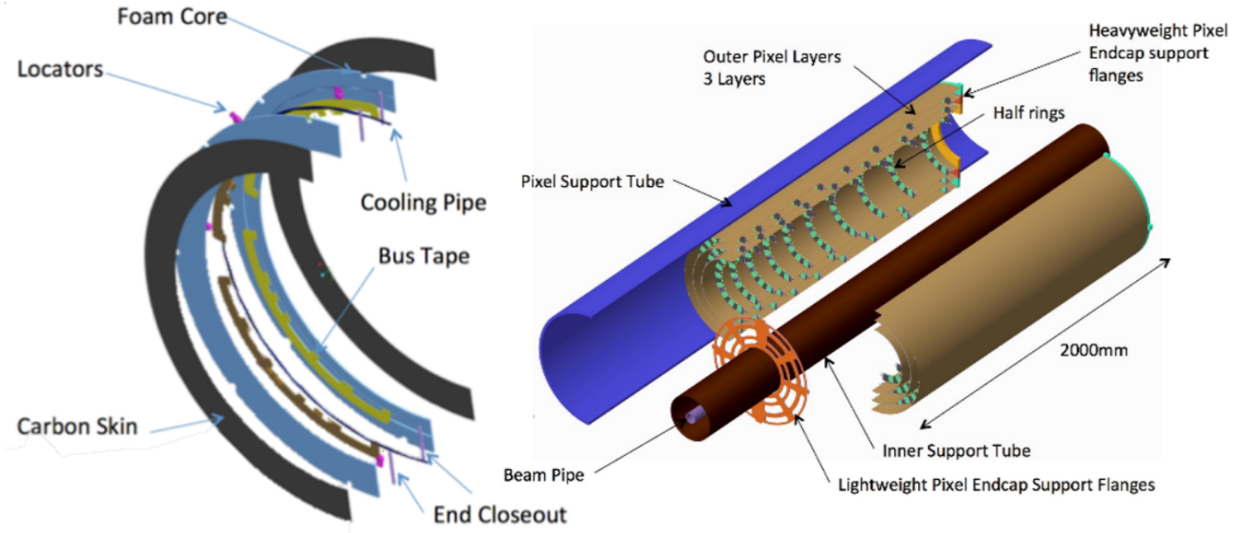

Figure 5.17: ITk Pixel Endcap system showing the different components including the half rings for mounting modules [80].

5.3 High-speed Tape Testing

The pixel endcaps will consist of rings, grouped together in layers, each layer at a different radius. As there are radial gaps between layers, η-hermeticity is achieved by adjusting the z-positions of the individual rings in each layer. The number of rings per layer is still under optimisation. Each ring will consist of a carbon foam and carbon fibre core containing cooling and electrical services. Each ring will be built out of two half-rings, for ease of construction. Quad modules will be mounted on both sides of each ring to allow overlap for hermeticity. The innermost pixel endcap layer will need to be more robust than the outer three layers, due to the higher radiation dosages it will be subject to. The ITk pixel endcap is illustrated in Figure 5.17, showing the half rings with mechanical support structure as well as the position of the Bus (Crescent) tape and the cooling structure.

The ATLAS Crescent Tape described here is the middle ring tape that was used as the device under test (DUT) with the quad modules (PixFlex) mounted with FEI4 chips. The flex tape has 5 tabs for connections to the quad modules and tabs for EoS (End of Structure) cards that connect to the outside services. The tape was designed to receive the low voltage, high voltage, and monitor the temperature for each of the quad modules on the EoS PWR TAB and the data, clock and command signals were routed out through the EoS DATA TAB to the outside services. The outline of the flex tape is shown in Figure 5.18.

The tape was a 4-layer flex PCB built with Dupont All-Polyamide (AP) material. The build of the tape is shown in Figure 5.19. ‘

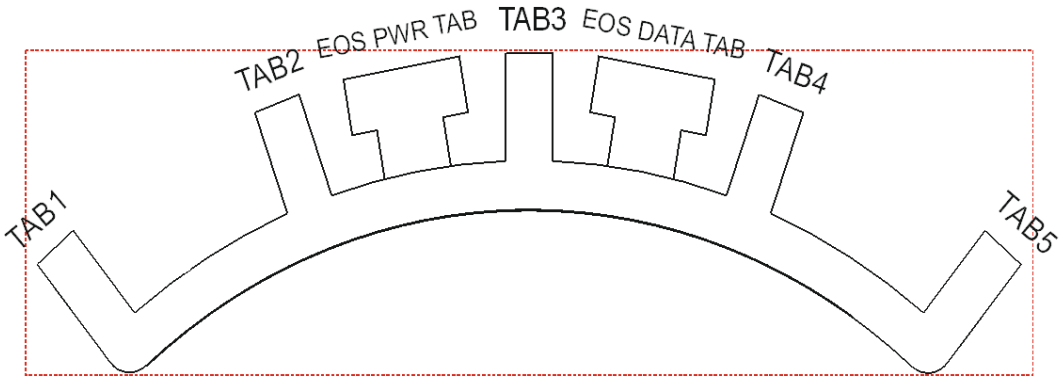

Figure 5.18: Crescent Tape showing TAB1-TAB5 (5 tabs to connect quad modules), (EOS PWR) TAB for Low Voltage (LV), High Voltage (HV) and NTCs (for temperature monitoring of the modules), (EOS DATA) TAB to readout data from the quad modules.

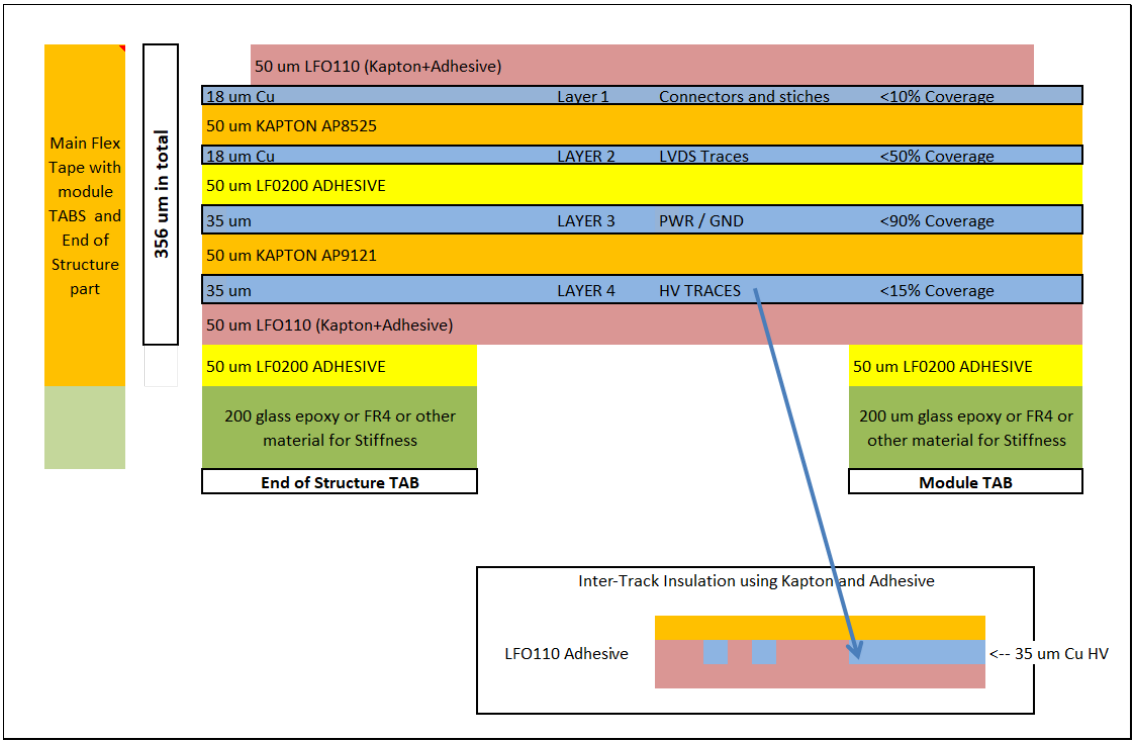

Figure 5.19: Crescent tape build showing the layer assignments and the material build. The design of this tape was done by the University of Edinburgh.

5.3.1 Requirements for testing the Crescent Tape

With the increase in luminosity, the data rate increases and a faster readout system had to be designed to read out the data. In addition to reading out the data at high-speed, the design has to be of low mass so as to not interfere with the particles that are produced. The PCB is also located in close proximity to the beam and hence susceptible to high doses of radiation. The Crescent tape was evaluated to understand the existing design and test if it was suitable for high-speed data transmission of 1.28 Gb/s. The setup for the measurement

of the tape is shown in Figure 5.20.

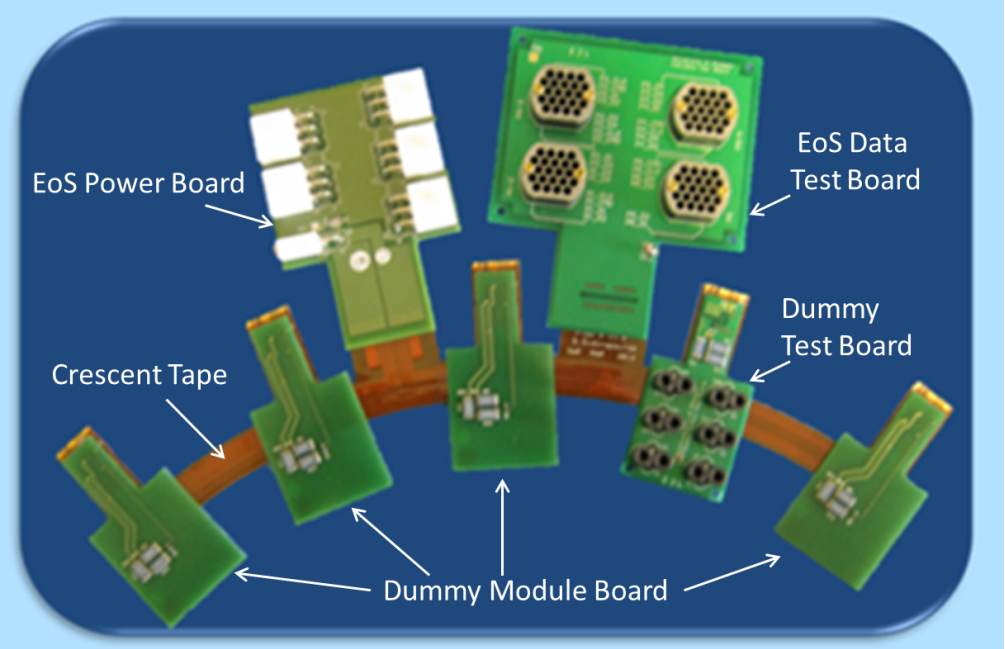

Figure 5.20: Apparatus for measuring the Crescent tape comprising the Tape with Dummy Module Test Board, EoS Data Board and the EoS Power Board.

Test boards for testing the Crescent Tape

For testing the Crescent Tape, there were four PCBs designed to be able to analyse the S-parameters and time domain results using the network analyser. The test boards were designed to have high performance test points that interface to the network analyser. These are connected to a RF25S[3] Samtec cable assembly which on one end connects to a test point connectors (CCH-J-02/ BAR-J-22) and the other side to a bulkhead jack that connects to the low loss cables of the network analyser. Details of the setup for the measurements are described in Section 2.4. The PCB layout of the 4 test boards is shown in Figure 5.21.

Dummy Module Board : This board was designed as a dummy for testing in place of a quad PixFlex board. The PixFlex board is the flex design that reads out 4 FE-I4s in parallel. This dummy board was designed for the purpose of testing without the need to use real assembled quad flexes. The pinout and mating connector to the tape was kept the same and a resistor network was connected on the PCB between supply and ground to draw current equivalent to that of a real quad module which is approximately 2 A.

Dummy Module Test Board : This board is similar to the Dummy Module Board but the four data pairs, clk and cmd traces that are routed onto high performance test points,

[3] https://www.samtec.com/products/rf25s

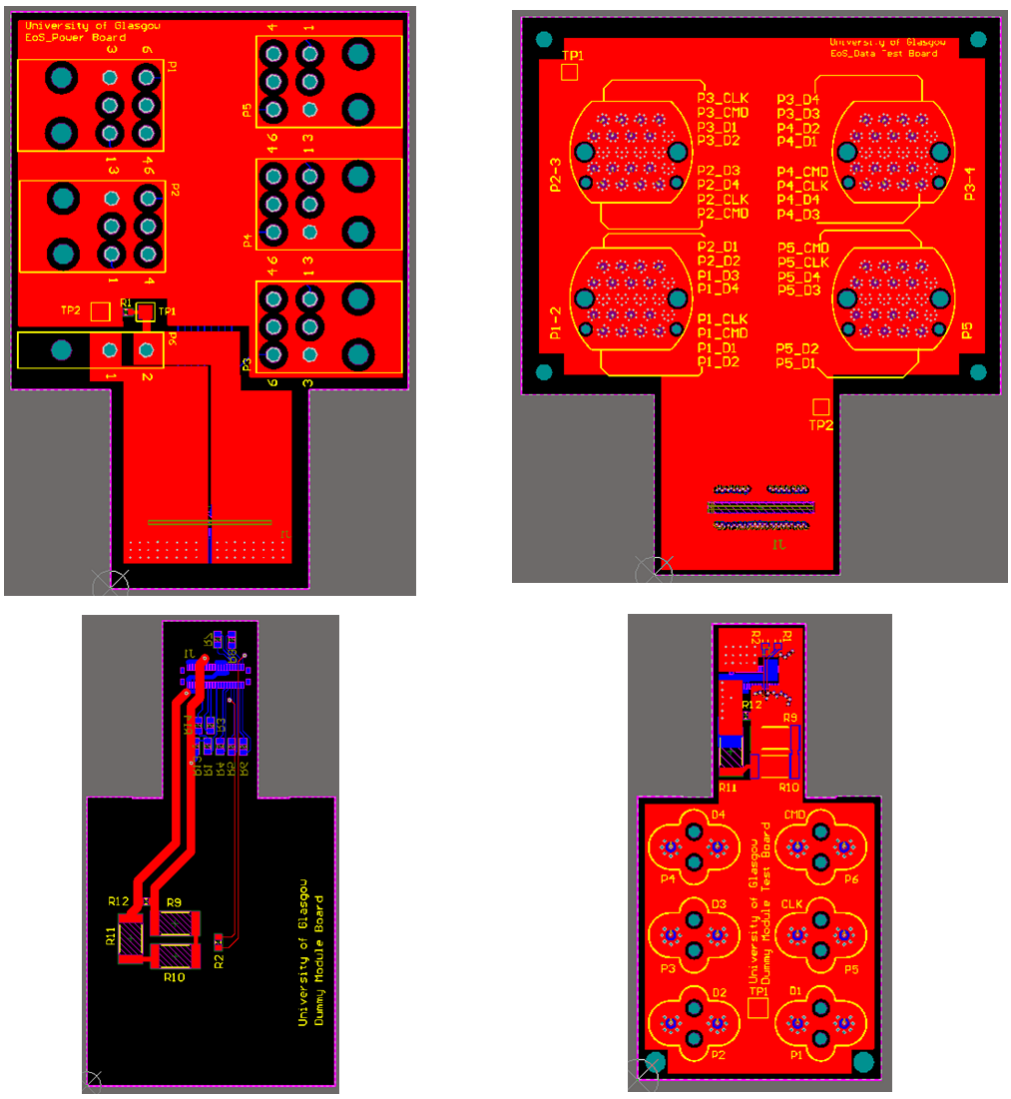

Figure 5.21: Test PCBs for testing the Crescent Tape. Top left - EoS Power Board. Top right - EoS Data Test Board. Bottom left - Dummy Module Board. Bottom right - Dummy Module Test Board.

Samtec CCH-J-02[4], rated up to 20 GHz / 40 Gbps.

EoS Data Test Board : This board was designed to mate with the EoS data tab on the tape. The board routes out the data, clk and cmd onto a high performance test point array, Samtec BAR-J-22[5] connector rated up to 20 GHz / 40 Gbps.

EoS Power Board : This board was designed to supply the Low Voltage (LV) and High Voltage (HV) to the modules on the tape. It has 5 connectors to give HV in parallel to all 5 modules while the LV connector would provide the input voltage to the first module in the chain (for serial powering). The output of this module will be the input supply to the next

[4] https://www.samtec.com/products/cch-j-02
[5] https://www.samtec.com/products/bar-j-22

module in chain and so on. The board also has its own shield ground that can be connected to the shield of the system. This is important to avoid noise injection in the system due to poor grounding and shielding. The block diagram and the bench setup for the tape testing are shown in Figure 5.22 and Figure 5.23 respectively.

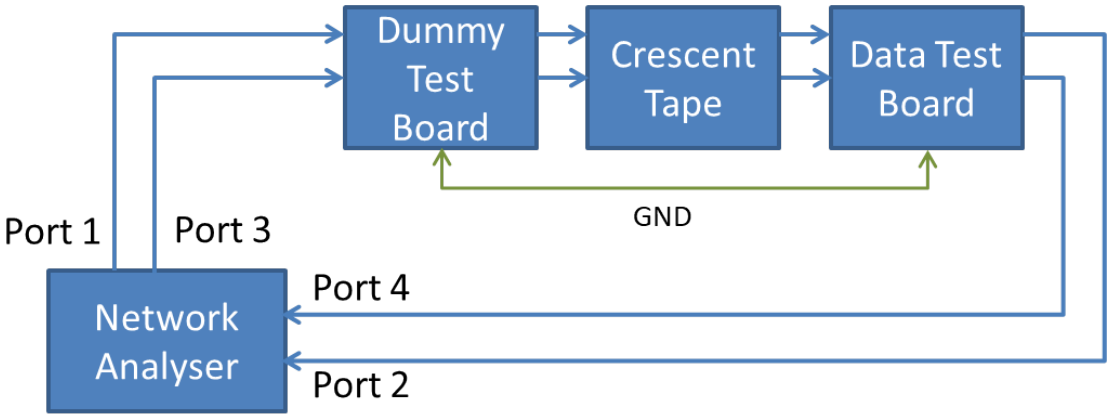

Figure 5.22: Block diagram showing the connections between the network analyser, Crescent Tape and the different test boards.

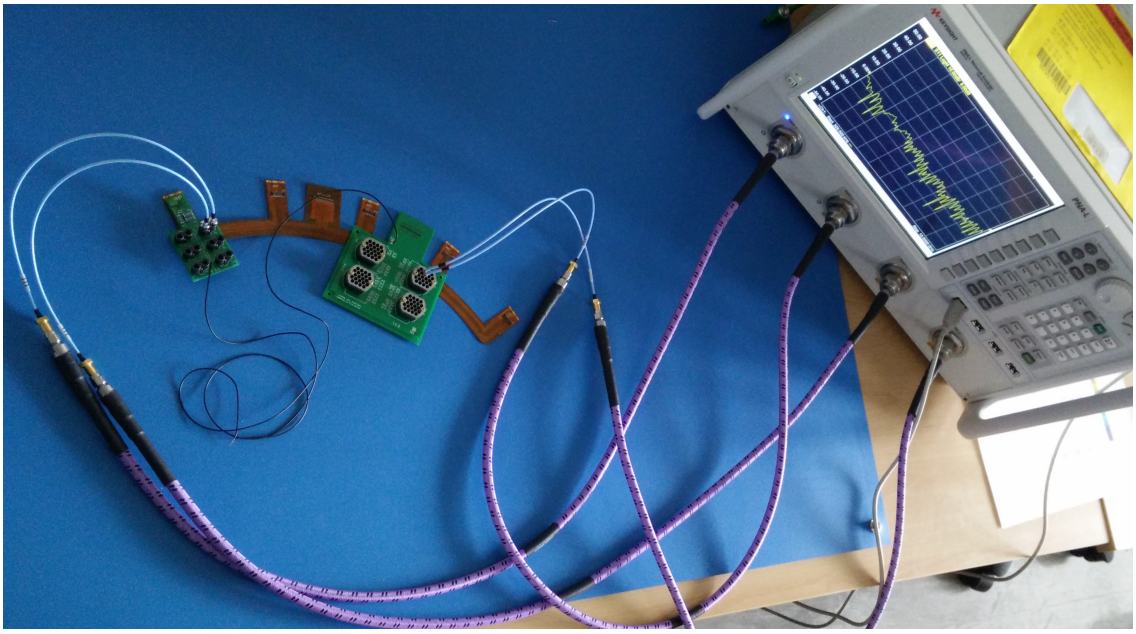

Figure 5.23: Bench setup for characterising the Crescent Tape.

5.3.2 Results of Crescent tape testing

The design of the Crescent tape was first evaluated to understand the build and stackup chosen. It was found that the data and control signals are routed on a inner layer of the four layer stackup with the serial powering plane as its reference. The serial powering reference

is made up of multiple copper plane areas and it was noted that the high-speed signals cross these planes while traveling from the module tab to the EoS Data tab and is shown in Figure 5.24. It was also seen that the data tab does not have a reference and as such the signals do not have a reference ground plane to calculate the 100Ω differential impedance. The network

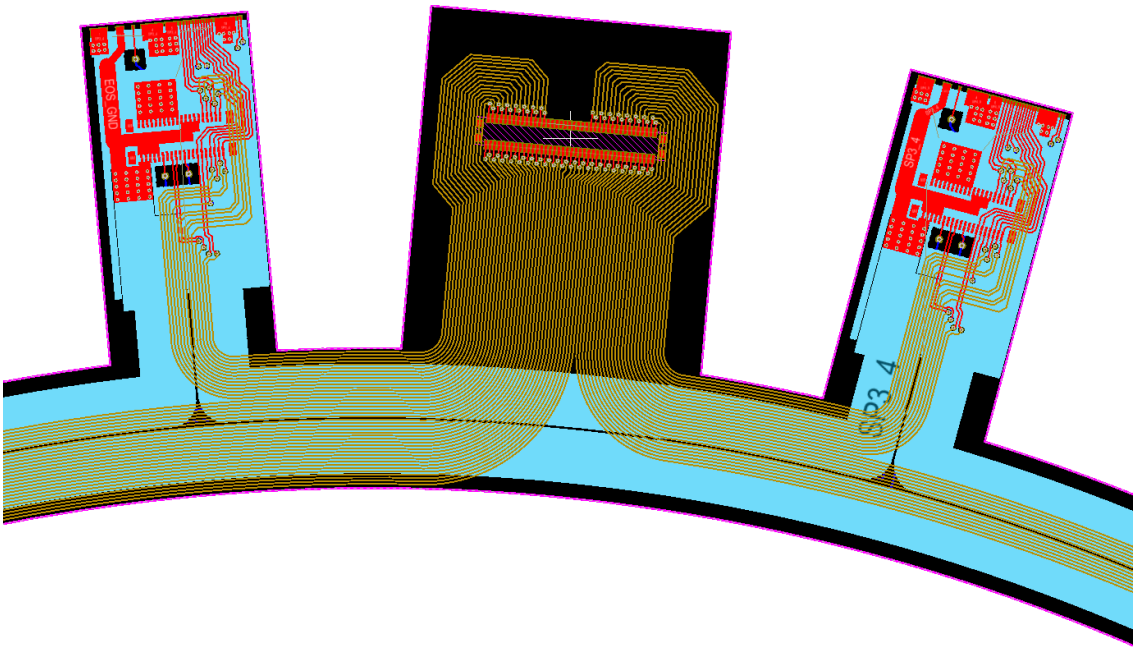

Figure 5.24: Layout of part of the Crescent Tape showing (brown) high-speed data signals, (cyan) split low voltage plane layer, (red) top layer and (navy blue) high voltage.

analyser was used to performed S-parameter measurements on each of the data and control pairs to study the effect of discontinuities on the signal performance. Both the test PCBs had the signal names labelled in silkscreen to identify the signals as shown in Figure 5.25 and to make it easy to connect the signal under test.

The PLTS (Physical layer test system) (detailed in Section 2.4) is used for analysing data post measurements. It allows data to be analysed in the time and frequency domains and for both single ended and differential signalling. It also has a feature to generate eye diagrams (see section 2.6). If the Bit Error Rate (BER) is to be calculated then the files have to be exported from PLTS and analysed on the Bit Error Rate Tester (BERT).

There are a few factors that introduce inaccuracy in the measurements and their interpretation. Firstly, The test boards are built in FR4 and the tape in flexible material. While analysing the time domain plots we had to specify the dielectric constant and this is not accurate as different constants could not be added for each board but had to be added for the setup in general. Secondly, the test boards in this case were made with data traces in

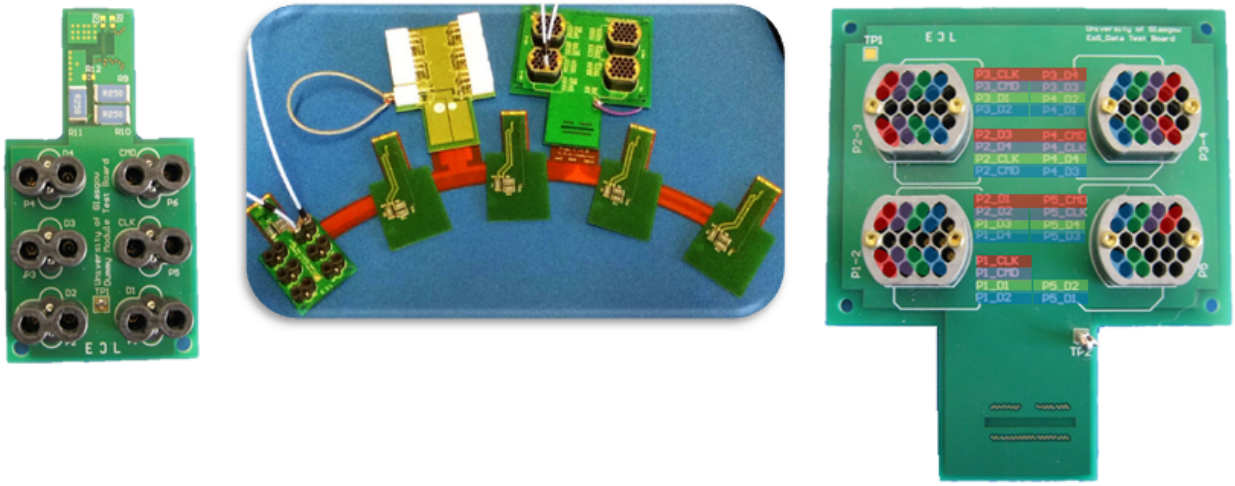

Figure 5.25: Setup for connecting an example signal under test. In this case TAB1-CMD signal.

stripline environment with ground references on both sides. There was a fabrication error where the signal layer was duplicated to have a symmetry in the stackup and hence a 60 Ω instead of 100 Ω was measured (seen in Figure 5.27 and Figure 5.29). Nevertheless, the results did help understand the possible causes of loss in the signal transmission and ways to mitigate them were also identified.

The two examples below illustrate the measurements performed to study the Crescent Tape design. The schematic reference is shown in Figure 5.18. The markers on the time domain plot are to distinguish between the three PCBs in the system. The part between M2 and M3 was the device under test, the Crescent tape in this case. The part between M1 and M2 and that between M3 and M4 were the two test boards. It was observed that the path the traces traverse on the PCB and the number of crossovers on the reference planes affected the impedance of the signal.

The S-parameter and time domain plots for cmd trace on TAB1 (P1-cmd) and clk trace on TAB3 (P3-clk) are shown in Figure 5.26 and Figure 5.27.

The loss on the shorter (P3-clk) signal trace was less compared to the longer signal (P1-cmd) trace on the PCB. The P1-cmd trace switched reference on the adjacent plane more than the P3-clk and this was reflected in the time domain plot with more variations in the impedance value.

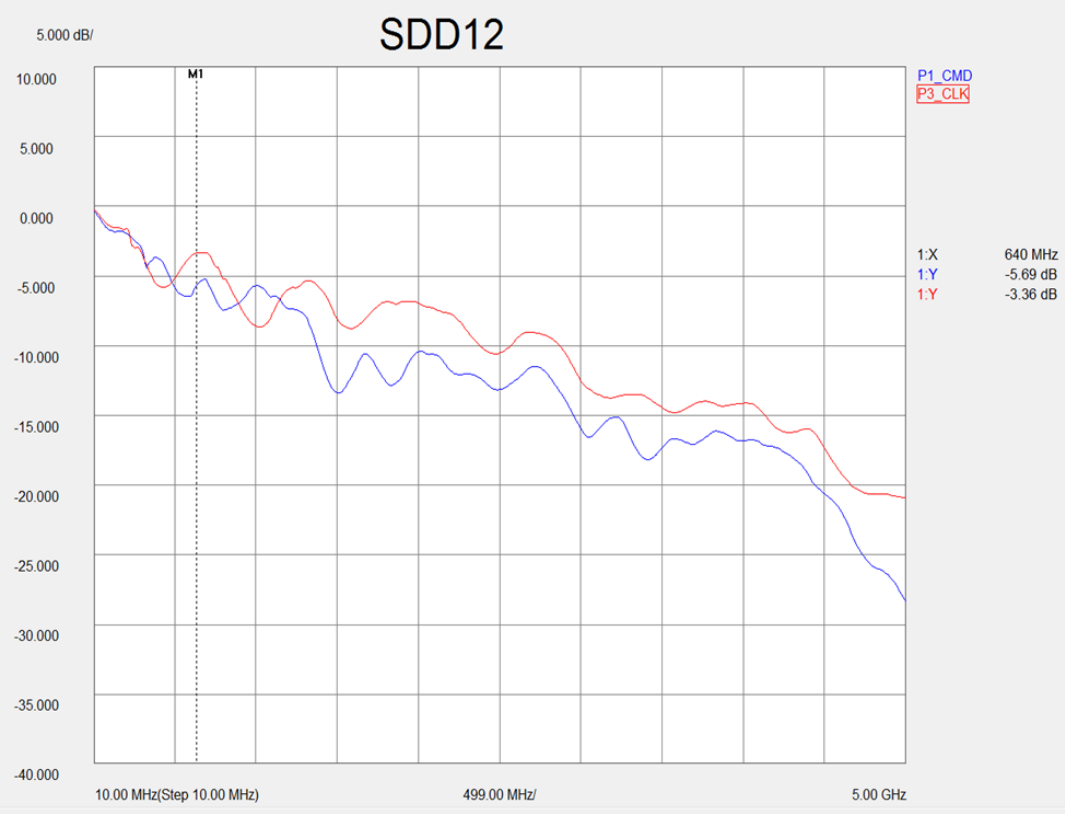

Figure 5.26: Plot showing the S-parameter comparison for the for P1-cmd and P3-clk signals at Nyquist frequency of 640 MHz: Loss (P1-cmd)= 5.69 dB and Loss (P3-clk)= 3.36 dB.

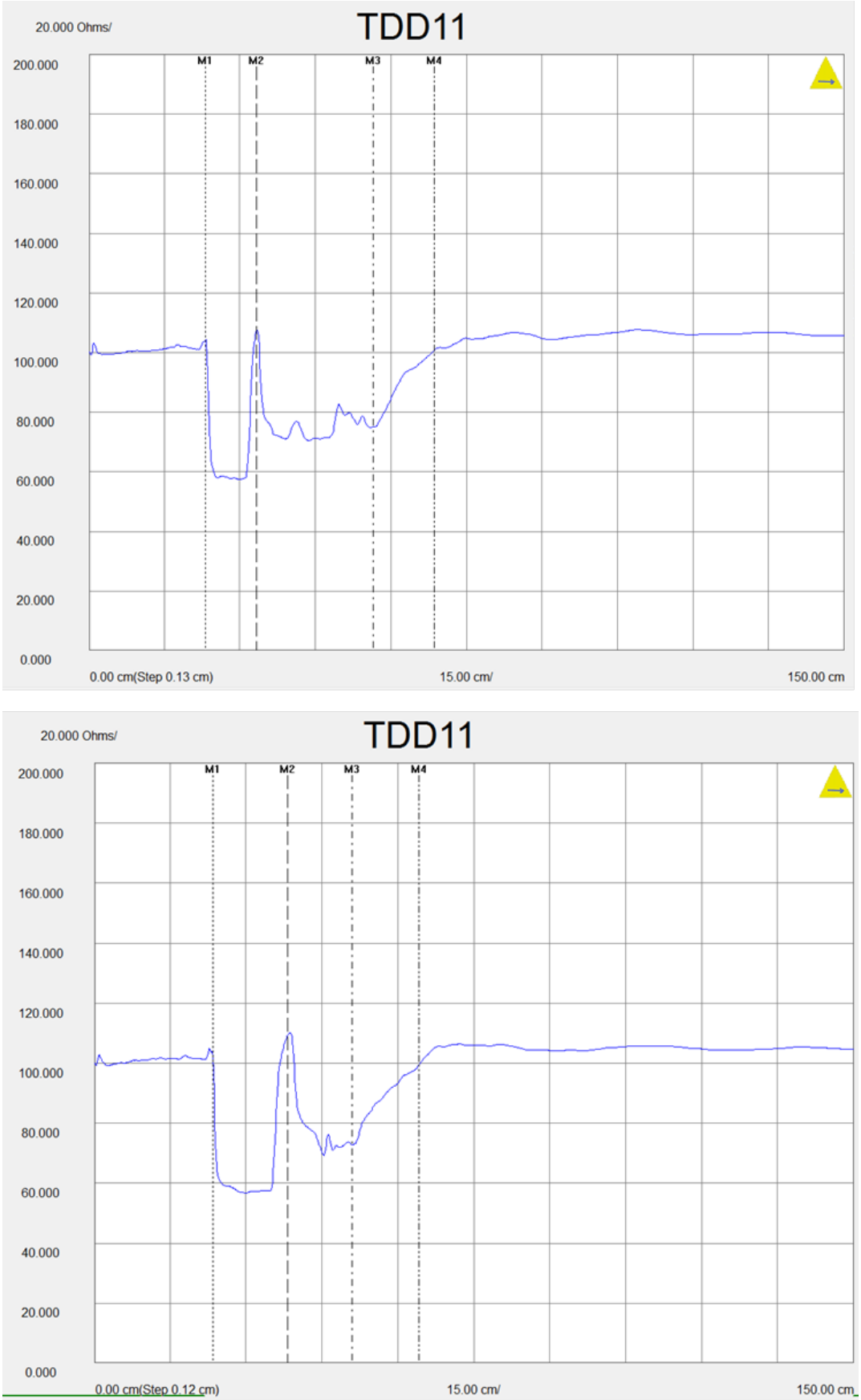

Figure 5.27: Top - Impedance plot for P1-cmd signal and Bottom - Impedance plot for P3-clk signal on (pseudo) TDR on the network analyser. The markers on time domain plot are to distinguish between the three PCBs in the system. The part between M2 and M3 was the device under test, the Crescent Tape in this case. The part between M1 and M2 and that between M3 and M4 were the two test boards.

Another example of the S-parameter and time domain plot for the data trace on TAB 2 (P2-D2) and the data trace on TAB 5 (P5-D2) is shown in Figure 5.28 and Figure 5.29. In this case, data pair 2 (there are 4 data pairs per module, one for each ASIC) on two different tabs.

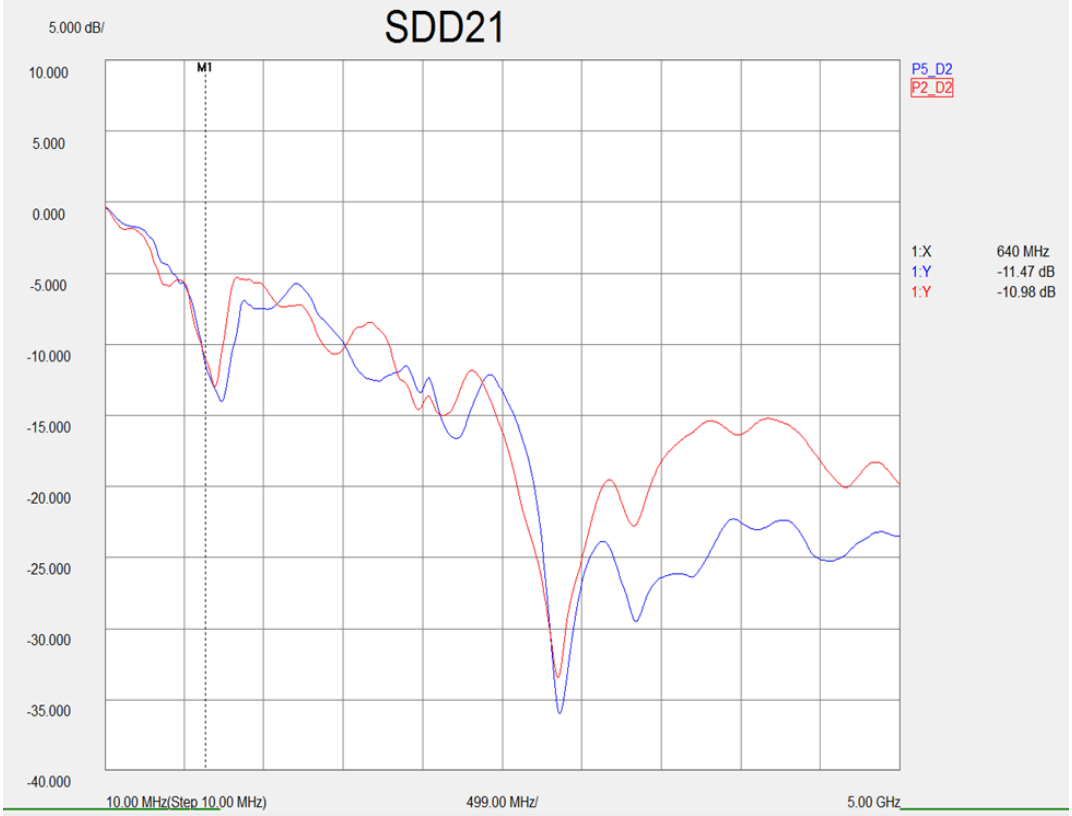

Figure 5.28: Plot showing the S-parameter comparison for the for P2-D2 and P5-D2 signals at the Nyquist frequency of 640 MHz: Loss (P2-D2)= 10.98 dB and Loss (P5-D2)= 11.47 dB.

It was observed that even when the P5-D2 signal traverses a longer path than P2-D2. The difference in the loss was less then 1 dB but the loss was close to 10 dB for both the signals. The P2-D2 signal crossed 2 reference planes while P5-D2 crossed just one but the time domain plot did not seem to be much different in this case.

Multiple measurement like this were made and compared, but a clear correlation between the length of traces or break in ground reference, to the signal degradation, was not deduced. Nevertheless, some points layout improvements were clear and were summarised and implemented in the next iteration of the tape design. It was clear that the high-speed data signal had to have a good ground reference and as far as possible a continuous reference. The references needs to be extended up to the connectors as they are one of the main causes of impedance discontinuities in the signal path. The length the signal travelled didn't really mean it was more lossy but having a reference plane running parallel to it would definitely help in maintaining the signal integrity. Eye diagrams and BER on the BERT were also studied to see if a correlation between the BER and the S-parameters could be concluded.

There were a few signals where the transmission (SDD_{21}) were similar but the reflections (SDD_{11}) were higher and caused a poor bit error rate and hence a closed eye diagram was seen. It was concluded that the PCB design was not suitable for high-speed data transmission of 1.28 Gbps as the losses on the tape were much larger than the accepted loss $<$ 1 dB on the PCB and the characteristic impedance for the signals was also not within the $100 \pm 10\Omega$ range. The overall length of the data links from the front-end chips to the optobox for readout to the Off-detector electronics would be approximately 7 m and considering this length every effort to keep the loss on the tape to a minimum was imperative. Techniques and guidelines for a good layout of the tape were identified, some of these are described in Section 2.1 and the same were given as input specifications for the design of the next variant of the tape.

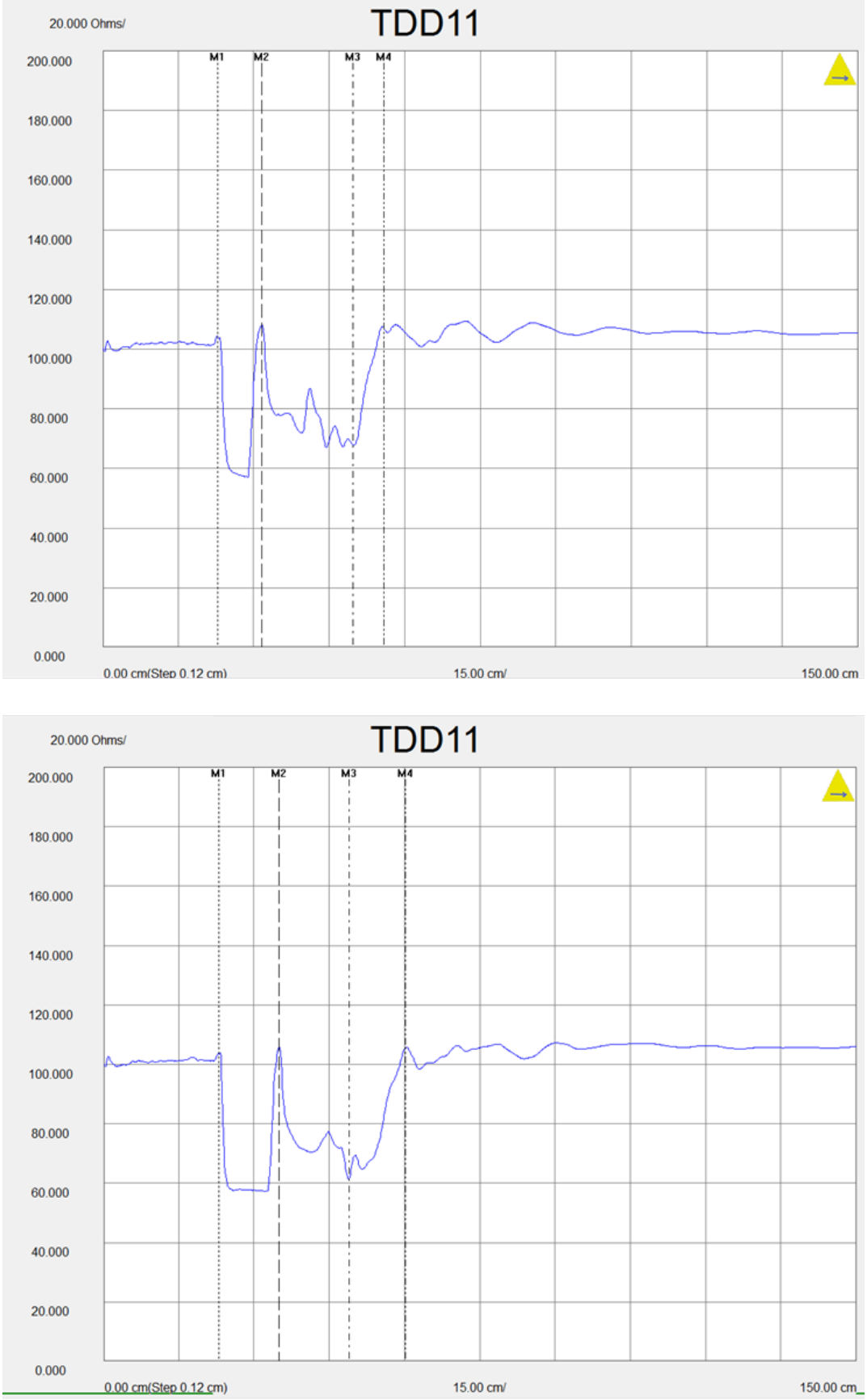

Figure 5.29: Top - Impedance plot for P2-D2 signal and Bottom - Impedance plot for P5-D2 signal on (pseudo) TDR on the network analyser. The markers on time domain plot are to distinguish between the three PCBs in the system. The part between M2 and M3 was the device under test, the Crescent Tape in this case. The part between M1 and M2 and that between M3 and M4 were the two test boards.

Chapter 6

Conclusions

The Large Hadron Collider (LHC) with its four experiments - ATLAS, CMS, ALICE and LHCb aims to make precision studies and searches for physics beyond the Standard Model (SM). The four experiments generate enormous amount data that needs storage and processing to be able to undergo analysis and help High Energy Physics (HEP) experiments. This thesis focuses on the electronics design of parts of the sub-systems of the LHCb VELO and ATLAS ITK Upgrades. Two main topics that outline the scope of the thesis are the powering schemes and data transmission system. With the increase in luminosity, more data and at higher data rate needs to be processed. Factors like the radiation environment and the need to minimize the mass in the overall system, pose challenges and result in stringent design requirements. Work towards addressing these issues and developing and designing electronics to efficiently read out data for the study of these physics experiments is performed and results are presented.

Chapter 1 is an introduction to the LHC and its experiments, the focus being the ATLAS and LHCb. The experiments have been performing extremely well but new developments aiming at further physics study has resulted in upgrades to the said experiments. Details of the present systems for both the experiments are described followed by the specific ATLAS ITK Upgrade and LHCb VELO Upgrade where the work of this thesis is focused.

Chapter 2 covers the methods and techniques used while doing the overall work covered in the scope of the thesis. Sources of signal degradation and ways to mitigate these are explained and these have been considered in all the design work from schematic design, PCB layout to material selection to make the PCBs. Techniques used like S-parameters to evaluate high-speed transmission and eye diagrams to study the output, CTLE scheme for improving signal quality and its implementation on the OPB are elaborated. The high-speed measurements are done using advanced tools and the setup detailing the tools used for the said measurements is explained.

Chapters 3 and 4 covers the LHCb VELO Upgrade experiment, the need for the upgrade and the details of the On-detector electronics. The LHCb collaboration has historically

performed very well and has managed to achieve remarkable results. Run II of the LHC ended in December 2018 and at this point the detector will undergo a full upgrade to improve the physics capabilities of the experiment. One of the major projects is the upgrade of the VELO detector, moving from a silicon strip detector with a readout of 1 MHz to a pixel detector with a trigger-less system to readout data at 40 MHz. In order to be able to read out the data at high-speed, electronics circuits and the On-detector electronics as a whole had to be designed to meet this change in requirement. The Data tapes to carry data from the VeloPix ASICs to the Vacuum Feedthough was thoroughly investigated and a significant research effort was invested. In addition, significant effort was spent closely working with the mechanics team to understand a broader picture of the sub-system, placements of cables, alignment and orientation. Multiple iterations were made to conclude on the best solution in terms of electronics design as well as overall mechanics.

The work on the LHCb VELO Upgrade is split into two chapters, the first chapter covers the theory and requirements for the designs of the On-detector electronics. This includes the scope of the designs, schematic requirements, PCB layout, layer stackup and the various iterations designed and the need for the same is highlighted. Some of the components designed by other members are shown in this chapter to ensure completeness of the sub-system design. The complete design cycle from prototype to production for the OPB and the Data tapes has been shown, highlighting the issues faced and lessons learnt to the stage of achieving a satisfactory production version of the designs. Substantial effort was spent in effectively communicating the requirements for fabrication of these PCBs to the external vendors. This was important as the designs had strict requirements when it came to total mass, high speed controlled impedance requirements, non standard material needs as well as the radiation environment.

The second chapter is in sync with the theory chapter and shows the results from the designs developed. The aim for the electronics is to have a loss of < 10 dB at the Nyquist frequency of 2.5 GHz for the full system, a characteristic impedance of 100 Ω to avoid impedance mismatch and reflections to the system and a minimal error rate in the transmission of the bits, set to be 10^{-13}. The data tapes were fabricated in-house at CERN with 3 variants to study the performance and converge on the best layout specifications and optimal performance. A few iterations followed in order to improve transmission performance by modifying connector pinout, trace width/ trace spacing as well as fabrication changes to make the design more in line with industrial standards and ease the manufacturing process. Results from the prototype to the production tapes highlighting the performance of the tapes is presented. A detailed understanding of the attenuation at high speed, conductor and dielectric losses was required to decide on the material to be used to fabricate the tapes as well as the trace width/trace spacing to be used on the layout to achieve the best results. Measurements on the full sized OPB specifically on the high speed links for the signal transmission parameters,

impedance, jitter and BER were performed to evaluate the links. There was considerable jitter and the eye diagram appeared closed and not ideal for the link. CTLE with passive components was implemented on the OPB for the data and control links and the results were found very satisfactory. Detailed measurements to tweak values of the GBLD laser driver, used as a line driver in this application, were carried out to find the optimal values for the pre-emphasis and modulation current. This together with the CTLE improved the signal quality and transmission parameters considerably. Finally, results of the full link test for the On-detector electronics from the front-end Hybrid to the OPB is shown and the results were well within the set requirement and hence satisfactory.

Chapter 4 covers the ATLAS ITK electronics which will also see an Upgrade and is a much larger experiment and hence more issues to tackle. The Upgrade will see a new inner detector to be able to cope with the higher rates, pile-up, and radiation levels. A new all silicon tracker and a new tracker readout will include the implementation of a track trigger to improve the ATLAS trigger capabilities. There are two specific topics addressed related to this Upgrade in the thesis, the evaluation of an effective powering scheme and design improvement for high speed requirements.

The increase in the readout data will lead to an increase in the number of overall cables to the Off-detector. Serial powering is evaluated as this scheme would mean less cables and hence less material in the overall mass of the detector sub-system. The FEI4 single chip and quad design along with the RCE and HSIO readout system is used to evaluate this scheme. Changes to the FEI4 SSC and design of new interface boards to perform these measurements were implemented and are explained in detail. The schematic requirements, PCB layout and layer stackup of the boards are shown. The measurement setup and the ToT scans showing the noise performance of the single chip cards in serial powering chain were measured and presented. There were some issues seen when sharing quadrants on the interface board but these issues were avoidable by changing positions of the modules. The system still worked satisfactorily and was tested successfully for the serial powering scheme.

The other topic looked upon was the high-speed layout of the Crescent Tape for the FEI4 modules. With the requirement of high-speed the existing design needed an iteration to be able to carry data with minimum losses in transmission. The existing design was tested for high-speed link tests and appropriate dummy boards were designed to help with these measurements. The goal of these measurements was to identify the layout techniques including layout specifications, layer stackup and PCB material selection to achieve best results for high-speed links while considering the serial powering scheme and high voltage distribution on the Crescent Tape. Significant measurements were performed and results obtained were used to give inputs to the design team for the next variant of the tape to be produced. The results of the new design were found to be more promising and capable of handling the high-speed transmission.

The thesis addresses a few of the topics from designing electronics from the start to modifying designs to make them compatible with testing requirements, testing for high-speed transmission and evaluating designs with highlighting scope for improvement. The process of requirement gathering to going through the stages of electronic design has been competitive yet challenging. Some results were a clear win while others had to be a compromise between requirements and results, but all in all the results have been satisfactory.

The precision measurements and searches for physics beyond the Standard Model will continue and the results obtained in this thesis constitute a significant contribution towards these studies. Some of the work is complete and while some were results based on studies that would be used as inputs for development in the future for both the LHCb and the ATLAS experiments.

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