Advanced GaN HEMTs for High Performance Microwave Power Amplifiers

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Abstract

The ever increasing demand for high power levels at higher frequencies from the industry has stimulated extensive research in gallium nitride (GaN) transistor technology over the past two decades. This has led to significant advances of the technology, but the degradation in the device performance due to device self-heating and trap generation in the device epilayers during device operation is still a major challenge with the current GaN high electron mobility transistor (HEMT) technology.

This thesis focuses on minimising device self-heating effects by means of efficient heat distribution within the device. Two approaches are analysed in this work. Firstly, the impact on the device DC performance of improved wafer growth conditions by using method called hot-wall MOCVD (metal organic chemical vapour deposition) are investigated. It was found that 2 µm × 100 µm devices on this wafer exhibit only 4% degradation in the saturated output current density at 20 V compared with 13% for devices fabricated on a wafer grown by standard MOCVD growth. This improved performance was attributed to lower thermal boundary resistance achieved by improved growth quality of the epitaxial material layers. In the second approach, the impact on self-heating was investigated through the use of a distributed device channel, i.e. introducing inactive regions along the device channel to distribute the hot spots in the device. Here a planar isolation method was used to achieve planar distributed gate devices that led to low leakage currents below 200 nA/mm at gate voltage of -20 V. A decrease in the peak channel temperature of 30°C was found through thermal simulations over a single 100 µm wide gate finger. Moreover, these distributed channel devices with gate periphery of 10 ×100 µm showed 13 % higher saturated current density than standard devices with the same active device area.

The other major issue addressed in this thesis is the so-called current collapse which is a degradation in the output current caused by electron trapping in the device structure. An alternative solution to the conventionally used dielectric passivation is proposed and it entails the use of a thick undoped GaN cap layer to reduce the surface effects by moving the surface further away from the device channel. Drain lag measurements show 15% and 35% decrease in the current at quiescent bias decrease points of [-7 V; 10 V] and [-7 V; 20 V] respectively for the proposed structure compared with 80% decrease and complete current collapse at these quiescent bias points in the same geometry devices on a standard wafer with 2 nm GaN cap layer and a thin 10 nm thin SiN_x passivation, respectively. The 10 nm

thin passivation layer does not minimise the surface effects, but it protects the devices from oxidation.

Finally, a single stage class A amplifier was demonstrated using the developed technology exhibiting peak output power of 30 dBm at 10 GHz and associated power added efficiency of 44% and gain of 10 dB. Also, gain of at least 9.4 dB was shown over 8-13 GHz bandwidth.

Associated publications

M. Elksne, A. Al-Khalidi, E. Wasige 'Thick GaN capped AlGaN/GaN HEMTs for reduced surface effects', *UK Nitrides Consortium*, online, January 2021.

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M. Vasilevska, A. Al-Khalidi, E. Wasige 'Thermal Performance of AlGaN/GaN HEMTs on SiC substrates', *UK Nitrides Consortium*, Sheffield, UK, July 2017.

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Author's declaration

Statement of Originality to Accompany Thesis Submission

Name: Maira Elksne
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I certify that the thesis presented here for examination for a PhD degree of the University of Glasgow is solely my own work other than where I have clearly indicated that it is the work of others (in which case the extent of any work carried out jointly by me and any other person is clearly identified in it) and that the thesis has not been edited by a third party beyond what is permitted by the University's PGR Code of Practice.

I declare that the thesis does not include work forming part of a thesis presented successfully for another degree.

I declare that this thesis has been produced in accordance with the University of Glasgow's Code of Good Practice in Research.

I acknowledge that if any issues are raised regarding good research practice based on review of the thesis, the examination may be postponed pending the outcome of any investigation of the issues.

Signature :… …..

Date :……03/09/2020……...

Definitions

2DEG	2-Dimensional electron gas
Al	Aluminium
Au	Gold
AlGaN	Aluminium gallium nitride
AlN	Aluminium nitride
Ar	Argon
BCl_3	Boron trichloride
Cl_2	chlorine
CPW	Coplanar waveguide
CV	Continuous wave
CVD	Chemical vapour deposition
DC	Direct current
e-beam	Electron beam
f_{MAX}	Maximum oscillation frequency
f_T	Current gain cut-off frequency
GaN	Gallium nitride
GHz	Gigahertz
g_m	transconductance
HEMT	High electron mobility transistor
IV	Current voltage
ICP	Inductively coupled plasma
JWNC	James Watt Nanofabrication Centre
L_G	Gate length
MIBK	methyl isobutyl ketone
MIS-…	MIS-HEMT
MMIC	Monolithic microwave integrated circuit
MBE	Molecular beam epitaxy
MOCVD	Metal organic chemical vapour deposition
N_2	Nitrogen
Ni	Nickel
P_{PE}	Piezoelectric polarisation
P_{SP}	Spontaneous polarization
PAE	Power added efficiency

PECVD	Plasma enhanced chemical vapour deposition
PMMA	Poly methyl methacrylate
q	Electron charge
RO	Reverse osmosis
RIE	Reactive ion etching
R_c	Ohmic contact resistance
R_{sh}	Sheet resistance
RF	Radio frequency
RTA	Rapid thermal annealing
SEM	Scanning electron microscope
SiC	Silicon carbide
$SiCl_4$	Silicon tetrachloride
Si	Silicon
SiN_x	Silicon nitride
TiN	Titanium nitride
Ti	Titanium
TBR	Thermal boundary resistance
V_{BR}	Breakdown voltage
V_{DS}	Drain-source voltage
v_{eff}	Effective electron velocity
v_{sat}	Saturated electron velocity
V_{GS}	Gate-source velocity
V_P	Pinch off voltage
V_T	Threshold voltage
W_g	Gate width
ε_0	Vacuum permittivity
ε_r	Relative permittivity
Γ	Reflection coefficient

1. Introduction

1.1. Overview

Since the invention of semiconductors, silicon (Si) has dominated the semiconductor industry [1]. This is mainly due to the low cost and availability of Si worldwide. However, the demand for higher power and higher frequencies has always increased. Therefore, in order to go beyond the limits of silicon electronics an alternative technology is necessary. Transistors made from direct bandgap materials particularly III-V compounds such as gallium arsenide (GaAs), indium phosphide (InP) and gallium nitride (GaN) offer higher electron mobilities, sustain greater voltage levels and can operate at higher frequencies and temperatures compared with Si devices.

One of the transistor types made from III-V materials that is of great interest recently is the high electron mobility transistor (HEMT). The first HEMT was made using GaAs by T. Mimura in 1980 [2]. Today GaN is the preferred choice for HEMTs over GaAs for many applications up to 100 GHz since GaN offers better performance for high power HEMTs due to higher carrier density and higher electron mobility in the channel, higher breakdown strength and higher operating temperature due to its larger bandgap [3]. These properties make GaN HEMTs the most promising high power amplifier technology today for a lot of applications ranging from mobile/wireless base stations [4], radar systems [5] to satellite communication and power systems [6], [7]. The first GaN HEMTs were reported in 1993 [8] and have been steadily developed over the last 27 years. In the last decade, they have also been actively researched for power electronics applications [9].

Material properties of common semiconductors in comparison to GaN are shown in Table 1.1 [10]. Besides Si, GaAs and InP, these include silicon carbide (SiC) as well. Parameters in the Table 1.1 are evaluated at 300K. Energy band gaps, relative dielectric constants (static), thermal conductivities, breakdown fields are given for unintentionally doped (UID) bulk materials.

Table 1.1. Properties of common semiconductor materials used in HEMTs at 300K [10].

Parameter (units)	Si	GaAs	InP	4H-SiC	GaN	SiC
Energy bandgap (eV)	1.12	1.43	1.34	3.2	3.44	3.26
Relative dielectric constant, ε_r	11.9	12.5	12.4	10.0	9.5	9.7
Thermal conductivity, k (W/Km)	150	54	67	400	130	400
Breakdown electric field (MV/cm)	0.3	0.4	0.45	3.5	3.3	3
Saturated electron velocity (10^7 cm/s)	1	1	1	2	2.5	2
Electron mobility (cm^2/Vs)	1500	8500	5400	700	900	700

One of the biggest advantages of GaN is that it can easily form heterojunctions to wider band gap materials such as aluminium gallium nitride (AlGaN) and aluminium nitride (AlN). This creates a quantum well also known as 2-dimensional electron gas (2DEG) channel which consists of high electron density (>10^{13}/cm^2) with electron mobilities of up to 2000 cm^2/Vs. Even though GaAs and InP has higher electron mobilities, the much higher 2DEG density in GaN results in lower sheet resistance, which is crucial for high power applications at high frequencies. Moreover, GaN exhibits much higher band gap energy of 3.4eV and breakdown field of 3.3 MV/cm compared to InP (1.34 eV, 0.45 MV/cm) and Si (1.12 eV, 0.3 MV/cm), which allows high voltage operation of GaN HEMTs. GaN HEMTs have been shown to attain breakdown voltages of 500 V at gate to drain distance of 10 µm with ultralow on-resistance (0.75 mΩ·cm^2) [11] which is way beyond the capability of Si [12]. High voltage operation of GaN devices makes them suitable for high line power converters and photovoltaic power converters. GaN also has higher thermal conductivity of 130 W/Km compared to GaAs (54 W/Km) and InP (67 W/Km) which combined with its wide bandgap makes GaN power devices suitable for high temperature applications such as oil industry, automotive and aircraft engine applications. Some of the applications of GaN mentioned above are illustrated in Figure 1.1 [13].

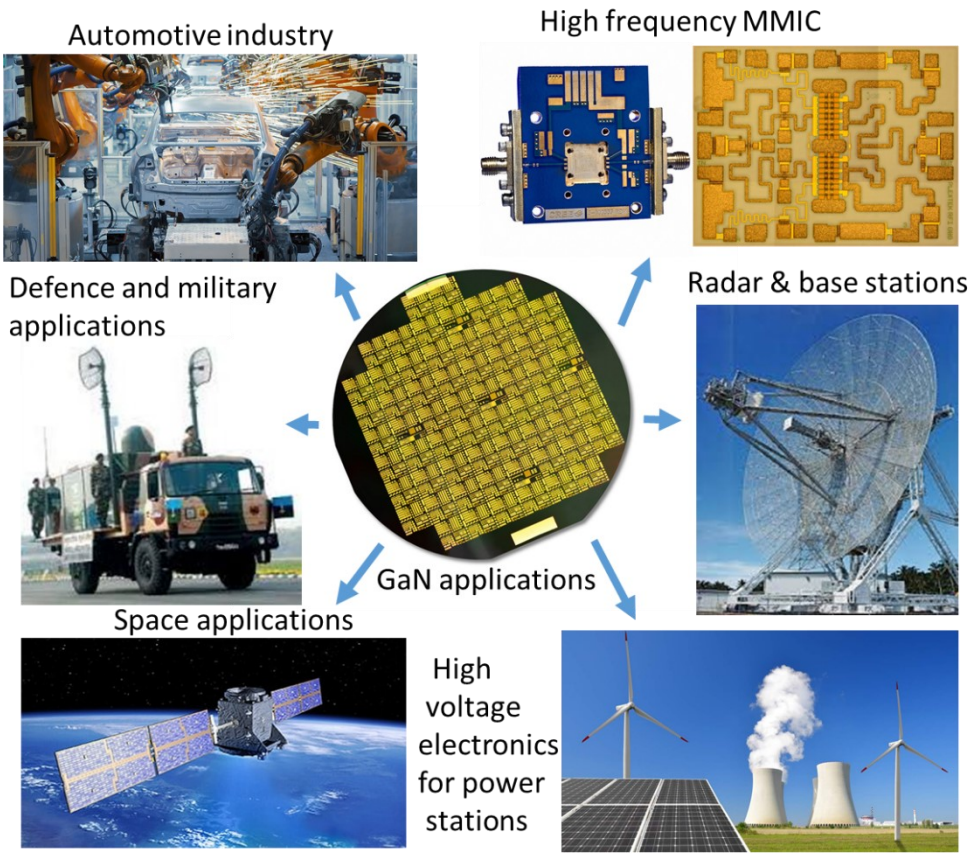


Figure 1.1 Illustrations of some of the applications for GaN HEMTs [13].

1.2. Research challenges

Even though there has been significant progress in GaN HEMT technology, the performance of the state of the art devices with RF power densities achieved as high as 9.4 W/mm at 10 GHz [14] and typical breakdown voltage in the range of 80-100 V for devices with gate lengths of 0.14 - 0.7 µm with source drain spacings between 3 -7 µm [15],[16] but it is still far from theoretical limits of 3.3 MV/cm, and so improvements in various aspects of the device technology are needed. Also, GaN devices working at high voltage and high current conditions suffer from enhanced heat generation in the device channel. This self-heating phenomenon is one of the major limitations of the current technology. The other major and long-standing challenge for this technology is the so-called current collapse, details of which are provide in the next section.

Industry also suffers from the lack of native GaN substrate in reasonable sizes and required purity to be competitive which leads to necessity of employing other substrates, such as Si, sapphire and silicon carbide (SiC) substrates. There is also a lot of research in diamond as a substrate for GaN HEMTs due to its excellent thermal dissipation properties, however the large lattice mismatch and coefficient of thermal expansion (CTE) between GaN and diamond is making the realisation of these devices a challenge [17].

A further challenge for GaN HEMTs is related to the realisation of devices operating at higher frequencies and high voltages that are demanded by the growing wireless communication industry especially in the Ka band (26-40 GHz) and above. Higher frequency operation can be achieved by reducing device size, such as gate to channel distance, gate-length and gate to drain distances. However, device downscaling is achieved in trade-off with breakdown voltage as compared to larger devices [18]. Breakdown voltages are reduced in scaled devices mainly due to increased leakage currents. Typical breakdown voltages for highly scaled GaN HEMTs is 10 V [19] (20 nm gate-length, Lsd = 120nm, Lgd = 50 nm) to 12 V [20] (55 nm gate-length, Lsd = 175 nm) compared to around 100 V in larger devices with sub-micron gate lengths (0.7µm gate length, Lsd =7 µm) [16]. Nevertheless, GaN HEMTs have been successfully scaled and fabricated for high frequency applications. For example at W-band, GaN devices used in monolithic microwave integrated circuit (MMIC) power amplifiers have been demonstrated to outperform one of the best competing technologies (InP devices) in power by a factor of 7 even though their cut-off frequencies were a factor of 2 lower compared with InP HEMTs for a 94 GHz power amplifier [21].

There is room for improvements for both RF GaN devices and also power GaN devices. Besides self-heating and current collapse there are other challenges faced by power GaN technology such as AlGaN/GaN based device's inherently depletion mode or normally-On behaviour. However, this is an issue only for power devices, since for radio frequency (RF) applications normally-On device operation is preferable. Normally-Off behaviour of device which also known as enhancement or e-mode device is desirable in power devices since they are employed as power switches. It is a necessity in power applications for both safety reasons (the circuit are fail-safe, i.e. the high voltage supply is cut off unless enabled by the gate control voltage) and high performance by reducing leakage current, simplifying circuit layout, improving device stability and efficiency since e-mode devices don't require to supply any additional power to turn them off. There have been various approaches to achieve e-mode devices as illustrated in Figure 1.2 from the first so called 'fluoride gate' HEMTs [22], where fluoride ions are implanted below the gate to several variations of p-type layers on top of the GaN HEMT, deep recessing the gate and variations of devices with gate oxide also known as MIS-HEMTs [23]. E-mode devices could also be made by using TiN gate structures, which are shown to produce very low leakage currents [24].

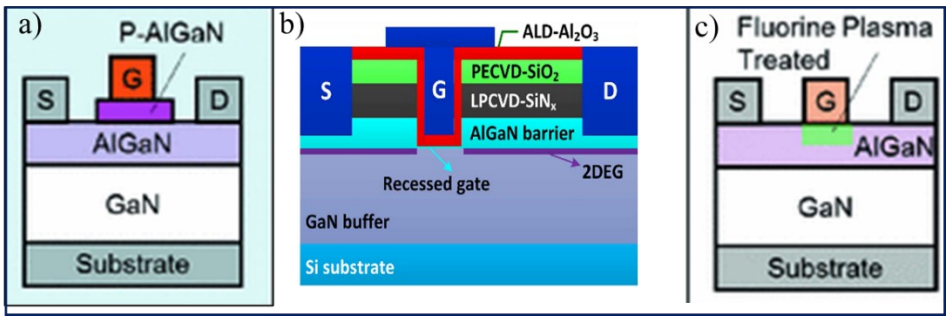


Figure 1.2. Illustration of the three types of e-mode GaN HEMTs a) with p doped layer under the gate, b) deep recessed gate with insulator under the gate and c) fluoride treated region under the gate [25].

A further challenge for GaN devices for high power applications is the requirement for high breakdown voltages, 100's of volts to kV. In this regard, vertical GaN devices have shown potential of achieving higher breakdown compared with lateral devices without enlarging the chip size. The highest reported breakdown voltage was close to 2kV for a GaN fabricated device [26]. Even though high breakdown was demonstrated for these devices, this is still much lower than the avalanche breakdown voltage of 5 kV in vertical GaN pn diodes and therefore improvements in the device design and processing technology are needed [23]. Further improvements in lowering the on-resistance (R_{ON}) and device capacitances are still required. Figure 1.3 shows theoretical limits of on-resistance as a function of the breakdown

voltage of Si, 4H-SiC and GaN with characteristics of the state-of-the-art reported GaN devices [27].

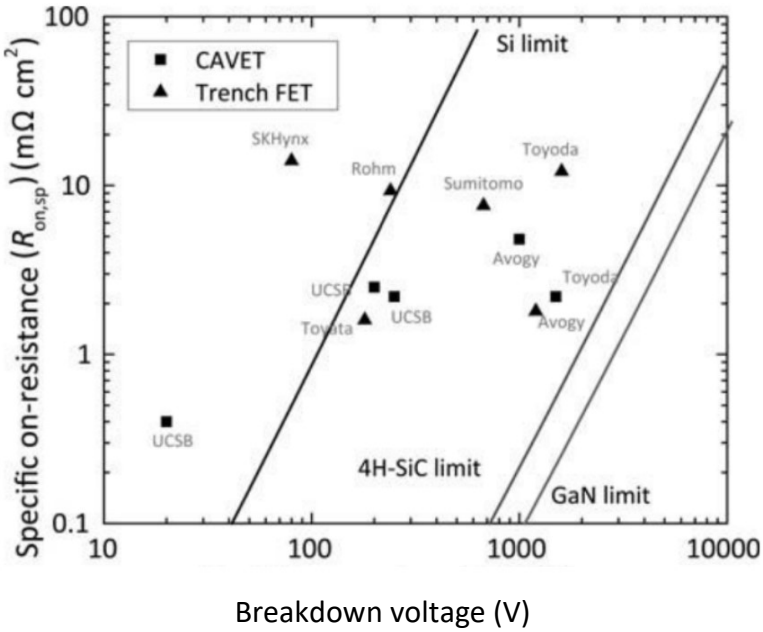


Figure 1.3 Theoretical limits of on-resistance as a function of the breakdown voltage of Si, 4H-SiC and GaN with characteristics of the state-of-the-art reported GaN devices [27].

1.2.1. Current collapse

GaN HEMTs suffer from an undesirable phenomenon known as current collapse or dc-RF dispersion, i.e. the current level during device operation is reduced compared to the actual current capability of the device. This is related to electron trapping at the surface or in the bulk of epitaxial layers [28], [29]. Trap levels within a certain heterostructure are believed to be generated at the crystal growth stage and during device processing [30]. Current collapse increases the device on-resistance and is one of the most critical issues that needs to be solved for GaN devices to be used in actual power switching applications [31]. It also causes reduced transconductance for RF devices.

One of the methods of reducing the density of electron traps on the AlGaN surface is by employing surface passivation. Different dielectric materials have been studied for this purpose such as silicon nitride (SiN_X) [32] [33], silicon dioxide (SiO_2) [30], SiON [34], zirconia dioxide (ZrO_2 [35], alumina oxide (Al_2O_3) [36], hafnia dioxide (HfO_2) [37] and others. Even though surface passivation with dielectric films has been demonstrated to improve the levels of current collapse it does not eliminate this problem. Also, although the importance of surface passivation is widely recognized, the physics of trapping associated with it is not very well understood.

Another common method of current collapse suppression is the use of field plates. A field plate is essentially a metal plate elevated by using dielectric passivation films above the device's gate-drain region where the electric field is the highest. An example of a field plated device is illustrated in Figure 1.4 a). Simulations show that the electric field can be reduced up to 50% using field plates as illustrated in Figure 1.4 b) [38], which allows to achieve higher device breakdown voltage, higher efficiency and also reduces high field trapping effects [39]. However, adding field plates to HEMT leads to higher drain-to-source (C_{ds}) and gate-to-drain (C_{gd}) capacitances resulting in a lower current gain frequency (f_T) so there is a trade-off between high breakdown voltages and high operating frequencies. In addition, the additional passivation layer required for field plate fabrication impacts the strain in the barrier and, thus, reduces the power performance. There are various configurations of the fields plates such as source connected field plates, gate connected field plates, field plates that are not connected to any device electrodes and combinations of these. If multiple field plates are used, they are usually separated by a dielectric film typically SiN_X or SiO_2 of chosen thickness. It has been reported by Saito *et al* that by using field plates one can enhance the breakdown voltage and also supress the increase of the dynamic on-resistance (R_{ON}) and the current collapse due to the relaxation of the electric field crowding at the gate edge on the drain side [40]. Improvement in breakdown voltage makes higher drain bias possible leading to higher output power performance with good reliability. As an example, an output power density of 17 W/mm with power added efficiency (PAE) of 50 % was achieved at a drain bias voltage of 80 V (when using field plates) compared to 5.5 W/mm power at 4 GHz with 30V drain bias (without field plates) [41]. Field plates have also been shown to be an effective way to reduce electron trapping by limiting tunnelling injection of electrons into surface traps located at the gate- drain region [42]. However, for gate field plates, since these are essentially an extension of the gate, with dielectric layer underneath, this creates a larger effective gate length causing degradation in the saturated drain currents and transconductance [43]. This also increases the drain to gate capacitance acting as drain to gate feedback capacitor providing an additional modulation on the signals at the input and output of the device which negatively impacts the RF performance, e.g. decrease in cut-off frequency.

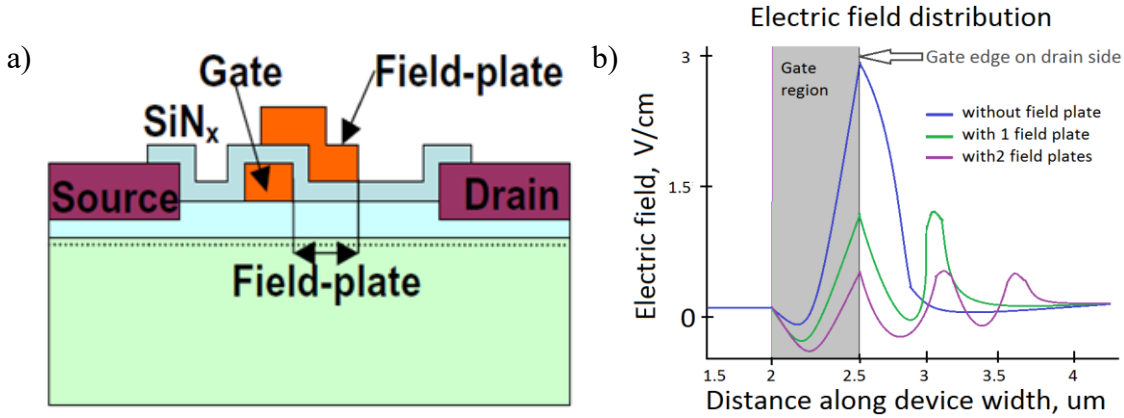


Figure 1.4 Schematic illustration of a) HEMT with 1 field plate above the gate [44] and b) the electric field distribution with 1 , 2 (the second field would be above the first with passivation layer in between the two field plates) or no field plates (adapted from [184]**).**

In this thesis a novel approach chosen to supress the current collapse will be described. In order to limit electron trapping at the surface an undoped thick GaN cap of 70 nm on an undoped GaN HEMT epistructure will be employed. In this device configuration all of the device electrodes are deeply recessed as shown in Figure 1.5 and due to the increased distance from the 2DEG channel to the surface of the device the electron trapping levels are expected to decrease. This approach also minimises any trap generation that may occur in the process of dielectric film deposition as demonstrated in unpassivated doped structures with thick GaN and AlGaN cap layers [44], [45]. The devices fabricated on this project do not deteriorate over time even without passivation, as opposed to conventional GaN HEMT epitaxial wafers (with thin 1-5 nm think GaN cap layer) in which the 2DEG concentration reduces over time due to the surface oxidation. This leads to reduction in polarization effects thus severely degrading the device to the extent that it becomes dysfunctional within 3 months if it is not passivated. Fabrication, measurements and analysis of devices with this wafer structure will be discussed in more detail in chapter 5.

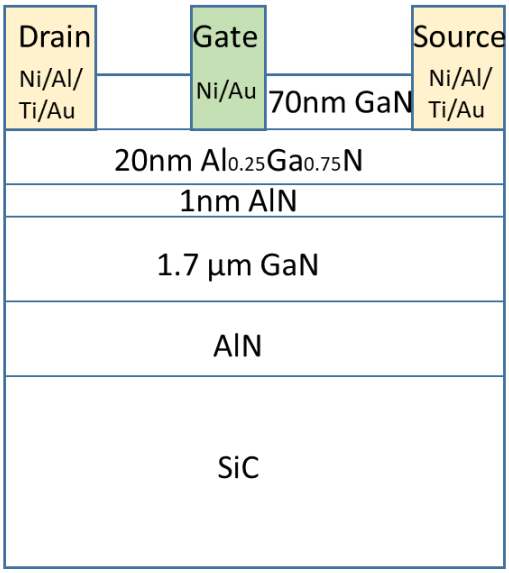


Figure 1.5 Proposed unpassivated device structure with deeply recessed Ohmic contacts (into 70 nm GaN cap layer) indicated as Drain and Source contacts (using Ti/Al/Ni/Au metal scheme) and the Schottky gate contact in the middle indicated as Gate (formed using Ni/Au metal scheme).

1.2.2. Self-heating

With the rapid development of GaN HEMT technologies power densities as high as 40 W/mm for GaN on SiC [46] and 56 W/mm of dissipated DC power have been demonstrated for GaN-on-diamond devices [47]. Cut-off frequencies (f_T) exceeding 450 GHz [48], RF power levels reaching 800 W in the S-band (2-4 GHz) [49] and power densities up to 5.8 W/mm at 30 GHz have been shown [50]. Highest RF power density of 8.84 W/mm with total power of 663 mW with associated power added efficiency of 27 % at 23 V drain bias have been reported for N-polar GaN on SiC HEMTs W-band frequency range (75-110 GHz) [51]. These results clearly demonstrate the potential for GaN HEMTs for various RF applications. However commercially available devices are typically operated conservatively, in most cases well below 7 W/mm to limit the channel temperature under 200 °C to ensure reliable operation [52]. Therefore, improvements in heat dissipation for GaN devices are necessary to enable the use of high-power density devices commercially.

Thermal management of GaN RF devices is commonly provided through high thermal conductivity substrates mainly silicon carbide (SiC) which has a thermal conductivity, k, of ~400 W/mK. Recent GaN research has focused on replacing the SiC substrate with nano-crystalline diamond (NCD) which has 5 times higher thermal conductivity of 2000 W/mK [53] [54]. First demonstrations of this approach have been recently reported, with an expected 3× enhancement in power handling capability compared to the best published GaN-on-SiC device results, but this is an expensive and specialized approach [53]. However, GaN

growth on any chosen substrate requires some transition layers to mitigate the stress at the interface due to the lattice mismatch between GaN and the substrate. Typically AlN is chosen as transition layer however it can have a thermal conductivity as low as 10 W/mK [55], and has been found to limit heat flow from the active device layers to the substrate and increases the channel temperature by up to 50% [56], [57]. Other thermal management approaches include thermally efficient packaging [58], [59], liquid cooling [60], [61] and the use of heatsinks [62]. To date, however, all of the techniques mentioned above are still limited by the thermal boundary resistance resulting from the AlN nucleation layer which limits heat flow to the substrate and subsequent packaging.

In this thesis, two approaches to reduce self-heating in GaN-based HEMTs devices are investigated.

- In one approach, a comparative study is carried out on the performance of devices fabricated on two GaN-on-SiC wafers, one grown conventionally using cold-wall metal-organic chemical vapor deposition (MOCVD) and the other by a new growth technique, the so-called hot-wall MOCVD. Using the latter technique, optimization of the nucleation layer growth has been demonstrated to significantly improve the quality of grown epitaxial layers leading to lower thermal boundary resistance associated with it which should result in more thermally efficient GaN HEMTs [50]. The fabrication, measurements and analysis of device performance with these wafer structures will be discussed in more detail in chapter 6.

- In the second approach, a novel approach of using a distributed device channel with a planar isolation method is assessed as a way to reduce the self-heating effect. The results of this approach are described and discussed in more detail in chapter 7.

Thus, in this thesis, two approaches to thermal management is to use GaN HEMTs have been investigated: one use devices grown on SiC substrate using the hot-wall MOCVD technique (for with low thermal boundary resistance) and, the other approach is to incorporate distributed gate/channel designs [63],[64].

1.3. Research aim

This project seeks to develop thermally enhanced GaN HEMT radio frequency (RF) electronic devices grown on the high thermal conductivity SiC substrates. The new devices

should enable uncompromised amplifier design that can reduce component count and reduce the amplifier footprint by leveraging the high power density into smaller more broadband circuitry. The project therefore has the following objectives:

- Design, fabrication and characterization of small gate periphery GaN-based HEMT devices with new epilayers structure incorporating 70 nm thick GaN cap layer to investigate improvements in current collapse.
- Design, fabrication, characterization and comparison of GaN HEMTs with the epi-structure grown by standard and hot-wall MOCVD processes;
- Design, fabrication and characterization of small gate periphery 200µm wide GaN-based HEMT devices with distributed gates for thermal performance.
- Design, fabrication and characterization of large gate periphery 1 mm wide GaN-based HEMT devices with integrated distributed gate design.
- Design, fabrication and characterization of small and large gate periphery GaN-based HEMT devices with distributed gates and with unity current gain and power gain current cut-off frequencies in excess of 40 GHz;
- Design and fabricate a monolithic microwave integrated circuit (MMIC) power amplifier (PA) in the 6 – 16 GHz range.

1.4. Thesis structure

This thesis is divided into 9 chapters. This chapter (Chapter 1) gives an overview of the AlGaN/GaN technology, its applications and highlights the material advantages over competing technologies. The research challenges and objectives including a summary of achievement are also described here.

Chapter 2 describes the theory of the GaN HEMT device starting from basic transistor structure, piezoelectric and spontaneous polarization, Ohmic contact formation to its operation principle.

Chapter 3 describes basic theory of transistor-based microwave and RF power amplifiers. Scattering parameter measurements and amplifier design principles are also discussed.

Chapter 4 describes standard fabrication techniques used for GaN HEMTs available at the James Watt Nanofabrication Centre (JWNC), University of Glasgow. It starts with device layout design followed by descriptions of material growth, different metallisation techniques and plasma processing involved in GaN HEMT fabrication.

Chapter 5 describes an experimental study of devices fabricated on a GaN epitaxial layer structure employing a thick cap layer or buried channel. The literature review on this type of epilayer structure and its impact to the device performance is presented. Results and benefits of fabricated devices on this wafer are described.

Chapter 6 describes an experimental comparative study of cold-wall and hot-wall MOCVD growth of GaN-on-SiC wafers and their impact on device performance. Two commercially sourced wafers are compared. Results of fabricated devices on each wafer and detailed analysis of device performance are presented.

Chapter 7 describes an experimental study of a developed new thermal management technique based on a planar distributed gate/channel. Development process and fabricated device measurement results are presented. Both small area and large area devices are presented to illustrate the benefits of this technique.

Chapter 8 presents measurement results and discussion of a fabricated class A single stage power amplifier with multi-finger GaN HEMT in the frequency range 6 to 16 GHz.

Chapter 9 provides a summary of the work done during this project and suggestions for future work.

2. Basic theory of GaN HEMTs

2.1. HEMT layer structure

The typical GaN HEMT epitaxial structure consists of 4 layers of materials as shown in Figure 2.1. Due to the limited availability of native GaN substrates, GaN HEMT layers are usually grown epitaxially on a non-native substrate such as sapphire (Al_2O_3) [65], silicon (Si) [66]or silicon carbide (SiC) [67]. The first layer grown on the substrate is the nucleation layer. This is usually a thin (20 – 200 nm) aluminium nitride (AlN) which is required to initiate the growth of the actual transistor layers and also to reduce stress from the lattice mismatch between GaN and the non-native substrate.

After the nucleation layer, an undoped GaN channel layer is grown, typically 1-3 µm thick. Since this layer is undoped, it is of high resistivity and so can act as a low loss substrate at high frequencies. Above the GaN channel is the barrier layer consisting of a material with a higher bandgap compared to GaN. This layer is commonly realized as aluminium gallium nitride (AlGaN or more precisely $Al_xGa_{1-x}N$, where x is the mole fraction or percentage of Al in the alloy), and is typically 20-25 nm thick, with 20-25% Al-content. As the AlGaN and GaN layers have different energy bandgaps, a low energy potential region known as a quantum well forms at the interface between the two layers in the lower bandgap GaN layer. Other less commonly used barrier layers include aluminium nitride (AlN) and indium aluminium nitride (InAlN).

The wurtzite physical structure of both the GaN and AlGaN layers results in a polarized crystal, i.e. there are net positively charged and net negatively charged regions within the structure, and so an intrinsic electric field known as spontaneous polarization exists in crystal. Also, because of the lattice mismatch between GaN and AlGaN, there is physical stress at the interface which enhances the polarization (called piezoelectric polarization). As a consequence of the spontaneous and piezoelectric polarization, electrons from the higher bandgap AlGaN accumulate in the quantum well, forming the so-called two (2) dimensional electron gas (DEG) or 2DEG. Electrons in the 2DEG are not bound to any of the layers and therefore are free to move. The Al mole fraction of AlGaN determines electron density and electron mobility in 2DEG [68]. The higher the mole fraction, the higher the energy bandgap of the barrier layer, and the higher the electron density in the 2DEG.

The top epitaxial layer is the GaN cap and is typically 2-3 nm thick. It prevents oxidation of the AlGaN surface, lowers the surface electric field (since it introduces a negative

polarization charge at the upper heterointerface causing increase of electric fields in AlGaN[69]) , reduces transistor gate leakage current (since the barrier height is increased) and enables the formation of low resistance drain (D) and source (S) Ohmic contacts [70]. The fabrication process of these electrodes are explained in the chapter 4.

To make a transistor, two Ohmic contacts, the source and drain contacts and one Schottky contact, the gate between them are realized as illustrated in Figure 2.1. The Ohmic contacts are metal-semiconductor junctions (heterointerface) which allow roughly equal current to flow both ways within normal device operation range. The voltage-current relationship of this junction is similar to a resistor, therefore they are known as Ohmic contacts. Typically, a positive bias is applied to the drain while the source is grounded, which forces electrons to flow from source to drain in the channel. The gate (G) contact, on the other hand, is made so that it is a Schottky barrier contact, i.e. a metal-semiconductor rectifying contact, so that current can only flow in one direction. The Schottky gate can control the potential distribution of heterostructures below the contact - by applying a negative bias the carrier concentration in the channel is reduced. If a large negative bias is applied, the channel becomes depleted of carriers, therefore no current can flow between the drain and source – device is then in the OFF state.

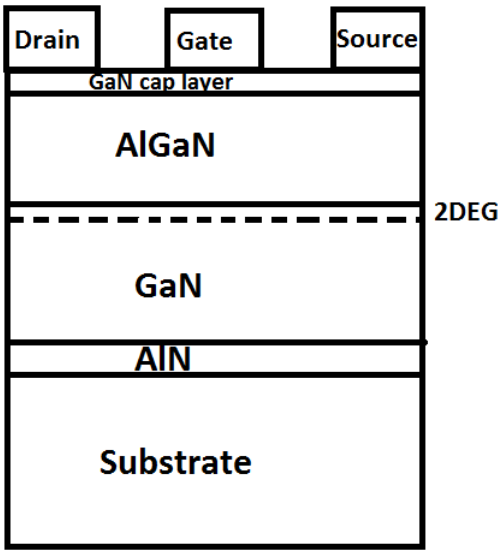


Figure 2.1 Schematic illustration of a conventional AlGaN/GaN HEMT structure.

2.2. 2DEG formation

GaN is a wurtzite group III nitride that forms a hexagonal structure in which the bilayers consist of two closely packed hexagonal layers: one formed by nitrogen (N_2) atoms and other by gallium (Ga) atoms as shown in Figure 2.2. (a). When GaN is grown along the c-plane there appears spontaneous polarization P_{SP} (since there is no applied external field), due to

intrinsic asymmetry of the bonding in the wurtzite crystal structure, which gives a rise to strong electric fields of around 3 MV/cm [71]. Spontaneous polarization P_{SP} of an AlN/GaN and AlGaN/GaN structure can be obtained by the following equation [71]:

$$P_{SP,Al_xGa_{1-x}N/GaN_x}(x) = (-0.052 * x - 0.029)Cm^{-2} \quad (2.1)$$

If a thin AlGaN barrier layer is grown on top of GaN buffer layer, due to the lattice mismatch AlGaN layer experience strain (mechanical stress) that leads to piezoelectric polarization, P_{PE}. If the Al content in the strained AlGaN is increased the piezoelectric polarization is also increased. If AlGaN barrier is grown on top of GaN layer an additional electric field of about 2 MV/cm is added to the structure due to the piezoelectric polarization. Figure 2.2 a) shows the crystal structure of GaN/AlGaN interface, while Figure 2.2 b) the polarization in the layer structure, with P_{SP} being spontaneous polarization and P_{PE} the piezoelectric polarization. Without the external electric field, the total polarization in the AlGaN layer is the sum of P_{SP} and P_{PE} creating a fixed polarization charge density σ at the AlGaN/GaN interface. When σ is positive ($+\sigma$), free electrons try to compensate for the induced charge leading to the formation of a 2DEG. Similarly, when σ is negative ($-\sigma$) holes accumulate at the interface, which can happen at the AlGaN/GaN cap interface creating a 2-dimensional hole gas, if the GaN cap layer is sufficiently thick. As usually GaN cap layer is 2-3nm this is not a problem.

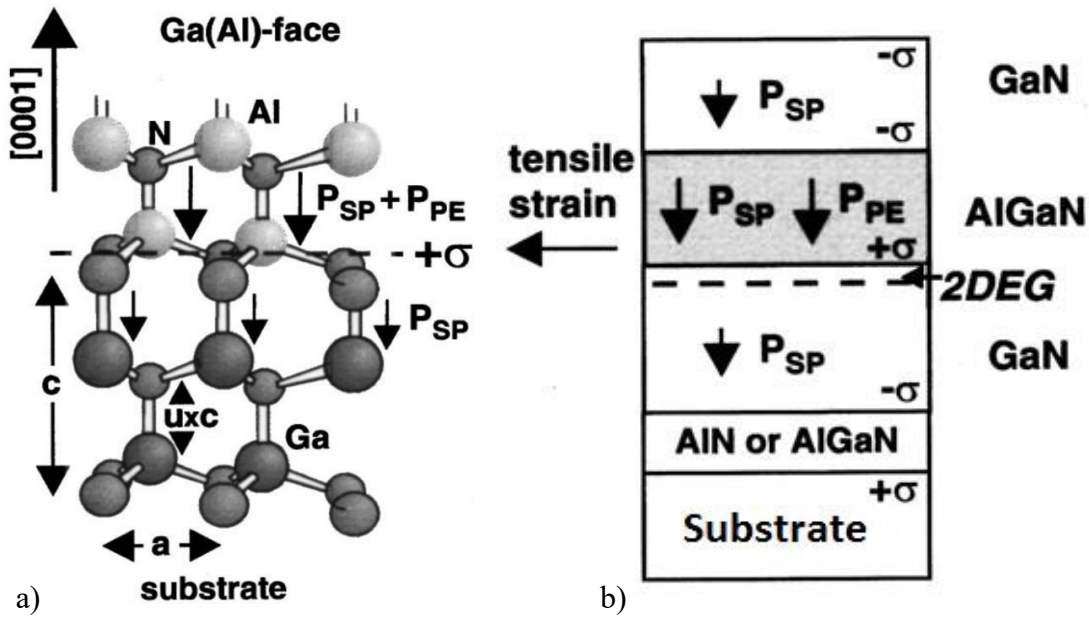


Figure 2.2 a) Crystal structure of wrutzite Ga (Al) face GaN b) polarization induced sheet charge and direction of the spontaneous and piezoelectric polarization in Ga-face strained AlGaN/GaN heterostructures [6].

The polarization effect is important here since it leads to 2DEG formation. With increasing Al composition in the AlGaN layer, the sheet carrier concentration of the 2DEG increases

[68]. However, if the Al concentration is higher than 35% lattice mismatch at GaN/AlGaN interface is too large, leading to large tensile stress that causes severe degradation in 2DEG properties and possible micro crack formation in the AlGaN layer [16]. Therefore, most commercial AlGaN/GaN HEMT structures have Al composition in the range of 20 - 30 %.

2.3. Metal semiconductor contacts

Figure 2.3 shows the energy bands at the metal and n-type semiconductor contact. Here $Ø_m$ is the metal work function, $Ø_{Bn}$ is the barrier height (difference between $Ø_m$ and the electron affinity of the semiconductor χ) and qV_{bi} is the built-in potential. E_C, E_F and E_V are the conduction band, Fermi and valence band energy levels, respectively.

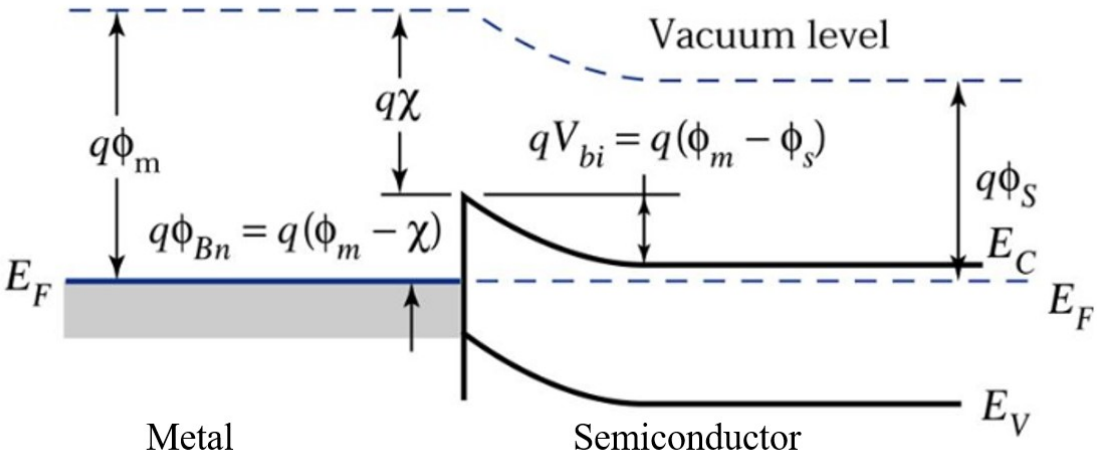


Figure 2.3 Energy band diagram for a metal (n-type) semiconductor contact in thermal equilibrium [72].

There are 3 main mechanisms of how electrons transit through the metal-semiconductor interface: thermionic emission, field emission and thermionic field emission as shown in Figure 2.4. Thermionic emission relies on the thermal energy given to the electron to cross the energy barrier. Field emission relies on the barrier quantum thickness thus happening in highly doped contacts. Thermionic field emission is a combination of field and thermionic emissions.

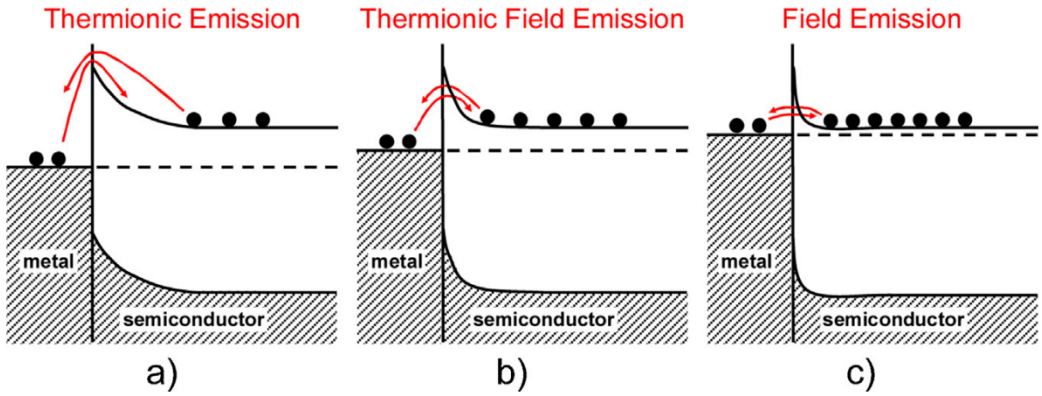


Figure 2.4 Schematic of electron transport at metal semiconductor interface a) thermionic emission b) thermionic field emission and c) field emission [73].

The contact between metal and a semiconductor can be either Schottky or Ohmic. Schottky contacts appear naturally at metal semiconductor interface and these contacts behave non-linearly to current flow, relying mainly on thermionic emission and are used in GaN HEMTs as gate contacts. Schottky barrier height at metal semiconductor interface is highly dependent on metal work function [74]. For Schottky contacts, a high barrier is needed therefore in GaN devices typically Ni/Au [75] or Pt/Au [76] Schottky contacts are used for gate formation. Nickel is a popular choice for gate metallisation and is used in this project as gate metal because of the good adhesive properties [76] and it gives barrier height of 1.27 eV [74].

In the GaN material system, the Schottky contact transforms in Ohmic contact after contact annealing at high temperature due to the metal alloying. Metals with low Schottky barrier height, in the range of 0.4-0.5 eV such as titanium and aluminium are recommended to obtain Ohmic contacts on GaN [73]. Typically used metal schemes for Ohmic contacts on GaN are Ti/Al/Ni/Au [77], Ti/Al/Mo/Au [78] and Ti/Al/Ti/Au[79].

2.4. Ohmic contact formation

Ohmic contacts behave linearly due to the field emission of electrons from the metal into the semiconductor, which is controlled by the width and magnitude of the barrier (difference between the E_C at the interface and E_F). The smaller the barrier height the easier it is for the electrons to cross it resulting in a low Ohmic contact resistance. The barrier height depends on the bandgap (difference between E_C and E_V), the lower the bandgap the lower $Ø_{Bn}$ while the width of the barrier depends on the semiconductor doping level.

For a GaN HEMT to have optimal performance a low-resistance, thermally stable Ohmic contacts are required. This ensures that

- A maximum drain current is achieved
- On-resistance is reduced
- Power dissipation in the Ohmic contacts due to high current density is minimized
- Extrinsic transconductance is maximized – enabling higher current gain cut-off frequency f_T and maximum frequency of oscillation f_{MAX} of the device

Typically, Ohmic contacts are formed on the AlGaN/GaN wafer surface and annealed at high temperatures in the range of 750 - 850 °C. Often, GaN can be heavily doped with silicon using doping densities up to $1*10^{20}$ cm^{-3} in order to achieve (non-anneled) low Ohmic contact resistances [80]. Ohmic contacts on n-GaN material were made using the Ti/Al (titanium/aluminium) where the N atoms are extracted (during the high temperature annealing) from the GaN by Ti to form TiN interface layer [81]. The N vacancies generated in the GaN became the electrically active donors, which reduces the barrier width and make the tunnelling of electrons easier. However, this technique doesn't work that well on AlGaN due to the amount of energy released at the contact creation process (known as enthalpy of formation) of GaN (-110.9 KJ/mol), TiN (-265.5 KJ/mol) and AlN (-318.1 KJ/mol). Bonding in AlN is stronger than bonding in TiN which results in to Al_3Ti formation that leaves AlGaN intact. This leads to high Ohmic contact resistance and therefore the same metallization method cannot be used for both GaN and AlGaN [82]. A metal stack of Ti/Al/Ni/Au was shown to achieve better Ohmic behaviour for AlGaN/GaN devices resulting in a typical good Ohmic contact resistances about 0.5-1.0 Ω-mm [83].

Non-annealed Ohmic contacts are currently being researched where Ohmic contact behaviour is achieved using highly doping the GaN contact layer to reduce the barrier height, e.g. this has been done by re-growing n-doped GaN in the contact regions [84]. Mostly, molecular beam epitaxy (MBE) is used for re-growing Ohmic contacts on HEMTs [85], especially selective area growth based on plasma assisted molecular beam epitaxy (PAMBE) is shown to be successful for growing the recessed n+ GaN layer for the drain and source contacts [86]. Non alloyed Ohmic contacts with regrown n+GaN can provide higher breakdown voltages and reduction of up to 10^6 in leakage current [87], [86] and low Ohmic contact resistances of 0.2 Ω-mm [84],[88], 0.16 Ω-mm [89] and 0.11 Ω-mm [90].

At the moment non-alloyed Ohmic contacts are the most effective method to produce low resistance Ohmic contacts typically giving contact resistance in the range of 0.1-0.2 Ω/mm. Theoretically the resistance of the regrown interface could be brought down to less than 0.02 Ω-mm due to quantum contact resistance theory if the regrowth is improved [85]. According to quantum theory, the limit of the minimum interface resistance between 2DEG and a large

contact depends on a 2DEG concentration near the interface; therefore, a fabrication process with minimized damage is necessary to achieve such low resistances [85]. Non annealed Ohmic contacts have better reproducibility. However, they are more challenging and much more expensive to fabricate, due to the required complicated high-temperature (above 1100°C) and high-pressure (15 kbar) regrowth process of GaN since it (GaN) decomposes at atmospheric pressure in temperatures below 1000°C. Therefore non-alloyed Ohmic contacts are not used in commercial devices yet [91], [92].

2.5. Ohmic contact characterisation

The quality of Ohmic contacts can be evaluated using the transmission line model (TLM) test patterns as shown in Figure 2.5 [93]. The interface of two dissimilar materials such as a stack Ohmic metals and a semiconductor can be characterised by a contact resistance *Rc*.. Thin film materials or doped semiconductor layers are usually characterized by a resistance, the sheet resistance, *Rsh* measured in ohms per square (Ω/□). In a TLM pattern current flows from one contact to the other through the semiconductor underneath and then into another metal contact encountering *Rc*, *Rsh* and *Rc* again (following the path of least resistance). The total resistance R_T of a metal semiconductor contact is the sum of the encountered resistances given by:

$$R_T = 2R_C + \frac{R_{sh}d}{W} \tag{2.2}$$

with W the contact width, d the gap spacing between the contacts.

Figure 2.5 a) show the geometry of transmission line model (TLM) that allows us to obtain the total resistance by applying constant current between the contact pads and measuring voltage drop between the gap spacing d as illustrated in Figure 2.5 b). Here four probe measurement is necessary for high measurement accuracy, because when the unknown resistance is very low (which usually is the case with Ohmic contacts for GaN HEMTs) the lead wire/probe resistance is comparable to the unknown resistance and these resistances themselves will drop considerable voltage. So the voltage being measured across the unknown resistance cannot be measured properly. To overcome this, two sets of probes are used, one pair to supply current to the unknown resistance and the second pair to measure voltage across it. The voltage probes do not draw appreciable current as voltmeter resistance is high so current probe drop is not a problem. TLM patterns are surrounded by mesa isolation such that the only path for current to flow is directly from one contact pad to another.

The measured total resistance can then be plotted against the gap spacing *d* to obtain a linear fit as illustrated in Figure 2.6 from which the Ohmic contact resistance and semiconductor sheet resistance can be extracted. Sheet resistance *Rsh* is obtained from the slope of the linear fit. Contact resistance *Rc*, is obtained from the intersect of the linear fit and y axis. Intersect between the linear fit and x axis gives information about transfer length L_T, which is the average distance that electrons (or holes) travel in the semiconductor beneath the contact before it flows up into the contact.

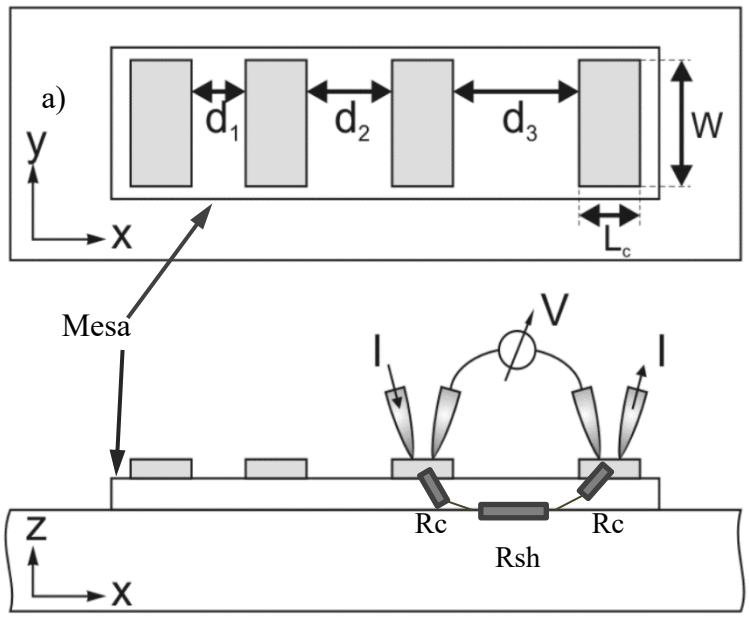


Figure 2.5 Schematic illustration of a TLM structure in a a) top view and b) side view.

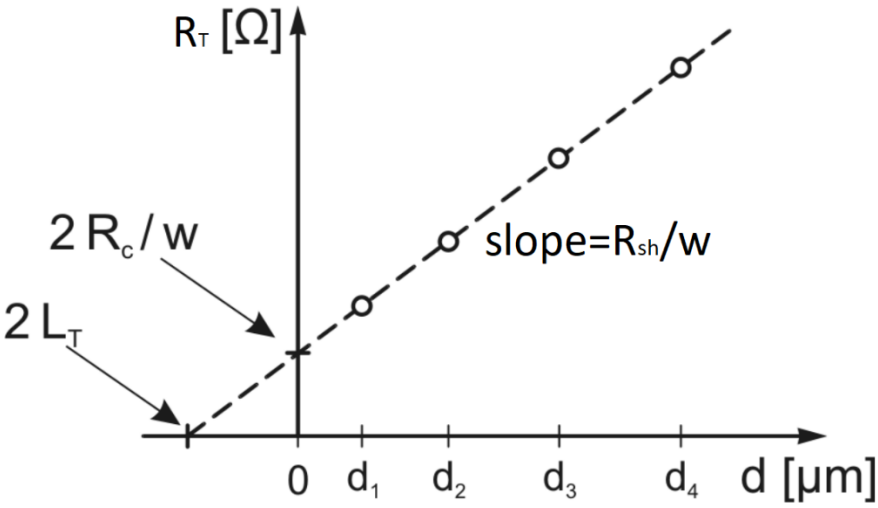


Figure 2.6 An example of a plot of total resistance measurements as a function of different gap spacings *d*.

2.6. HEMT operational principles

In a HEMT current flows between the two Ohmic contacts, the source and the drain. This current or rate at which 2DEG charge move across the gate can be represented by the following expression [94]:

$$I_D = qn_s v_{eff} W_G \tag{2.2}$$

where q is the electron charge, v_{eff} is the effective velocity of the electrons in the channel, n_s is the 2DEG charge density and W_G is the gate width. The velocity of electrons in the channel is the product of their mobility μ_n and the applied electric field, E and therefore can be expressed as:

$$v_{eff} = \mu_n E = \mu_n \frac{V_{DS}}{L_{DS}} \tag{2.3}$$

where V_{DS} is the voltage applied between drain and source Ohmic contacts, L_{DS} is the distance between drain and source Ohmic contacts.

The current flow is controlled by the Schottky gate contact. In the GaN HEMT structure, the 2DEG channel exists without an external bias being applied due to the polarization effect, and so it is a depletion mode or normally-on transistor. If a negative bias is applied on the gate the 2DEG channel depletes (in proportion to the applied voltage). The (gate) threshold voltage, V_T, is the bias that just depletes the channel of electrons and so no current flows between the source and drain contacts, i.e. the device is turned off. For increasing gate bias above V_T, the electron density in the 2DEG also increases and current can flow between the source and the drain if a bias voltage is applied between them. For a Schottky gate there is a limitation of +1 V after which it turns on, starts conducting, and so no longer controls the 2DEG concentration or the drain source current. Depending on the gate bias, the sheet carrier density can vary from a maximum value n_{s0} to a minimum value of zero when the channel is fully depleted. The gate metal and 2DEG channel can be modelled as a capacitor and therefore n_s can be expressed as:

$$n_S = \frac{\epsilon_{AlGaN}}{q(d_{AlGaN} + \Delta d)}(V_G - V_T) \tag{2.4}$$

where d_{AlGaN} is the thickness of the AlGaN barrier layer, V_G is the gate bias voltage and Δd is the effective distance of the 2DEG from the heterointerface, since due to the polarization effects sharp potential well leads to electrons being confined in a 2D plane just below the AlGaN/GaN interface. The typical current voltage (I-V) characteristic of a GaN HEMT is

illustrated in Figure 2.7. Here one can see that at each given gate voltage above the threshold voltage the drain current first increases linearly and then saturates with increasing drain bias voltage. Increasing gate voltage leads to more electrons accumulating in the 2DEG channel leading to increasing drain current.

The transconductance of the device can be defined as follows:

$$g_m = \frac{\delta I_{DS}}{\delta V_G} \tag{2.5}$$

where δI_{DS} is change in current and δV_G is change in voltage.

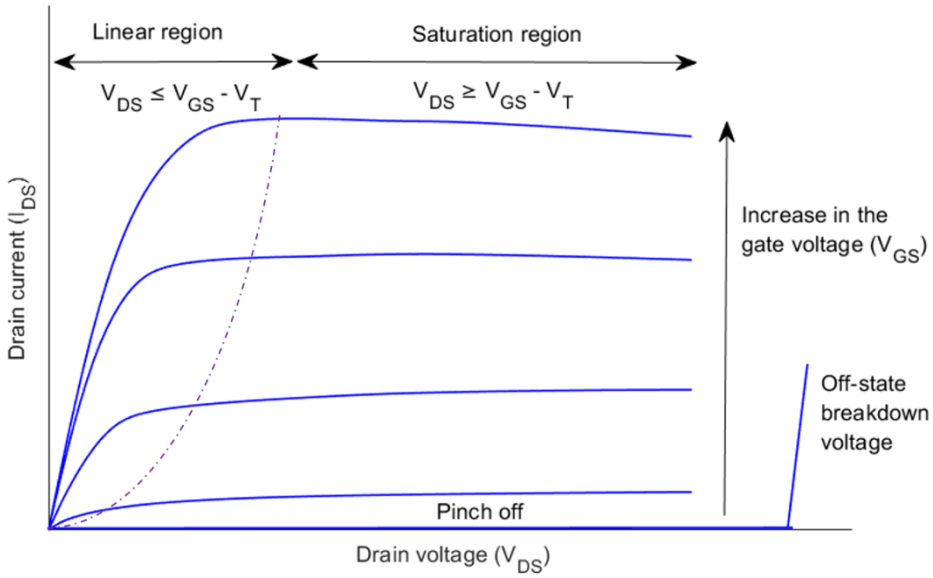


Figure 2.7 Output DC-IV characteristics of a typical GaN HEMT.

Another way of understanding how HEMTs operate is to consider their response to small/weak AC or radio frequency (RF) signals for a given set of bias conditions. In this case, the HEMT can be represented by a small-signal equivalent circuit model which is derived from the physical structure of the device. Figure 2.8 shows a small signal model of a HEMT device superimposed on the device cross-section with the elements located in the actual locations within the device. This model uses a representation of HEMT physical properties in terms of circuit elements; for example, the depletion region under the gate contact can be represented by a capacitance. The small signal model or equivalent circuit shown in Figure 2.8 corresponds to a device biased in the saturation region.

In the model, R_g, R_d R_s are contact and access resistances of the gate, drain and source electrodes, respectively. R_{in} models the region between the gate and source, while R_{ds} is the output resistance. C_{gd}, C_{gs}, and C_{ds} are gate-drain feedback, gate-source and drain-source capacitances, respectively, while g_m is the transconductance, defined as the ratio of the output current to the voltage across the device input.

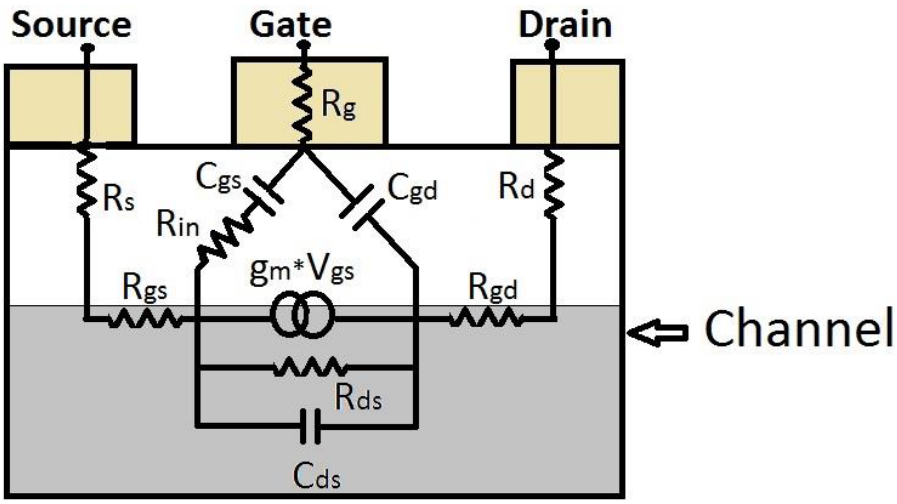


Figure 2.8 Small signal equivalent circuit of a HEMT.

The device small signal model (which can be extracted by following the procedure described in this reference [95]) is very useful representation of the device because it allows evaluating the device performance based on the extracted parameters from a fabricated device and determine which areas need improvement. For example, if a lower gate resistance is needed a T-gate can be used, which is a gate in a shape of the letter "T" instead of standard planar gate, and if the gate length is reduced the capacitances C_{gs} and C_{gd} are also reduced improving the device performance. Small signal parameters also allow calculate the device current and power gain cut-off frequencies f_T and f_{MAX}, respectively, and hence the frequency range over which the device could operate in a circuit. All the small signal model parameters can be calculated from S-parameter measurements which are discussed in the next chapter.

2.7. Transistor cut-off frequencies

A HEMT has 2 ports : input and output port, between the gate and source for the input and between the drain and the source for the output. This is marked on the micrograph of the fabricated device in Figure 2.9. At any given bias point, the transistor can be characterised by measuring its scattering or S-parameters by using a vector network analyser (VNA). S-parameters can be used to describe 2 port networks such as transistors or transistor amplifiers by measuring transmission and reflection of a travelling wave. Using the S-parameters, one can determine the input and output impedance of a transistor under any loading conditions. Specifically, they are used in the design of input and output matching networks. The reference impdance for these measurements is usually 50 Ω. The VNA is first calibrated so that the reference measurement points are at the probe tips which make contact with the transistor pads (see Figure 2.9.).

S-parameters are represented in a matrix $S = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix}$, where S_{11} is the input reflection coefficient, S_{12} is the reverse transmission coefficent, S_{21} is the forward transmission coefficient and S_{22} is output reflection coefficient.

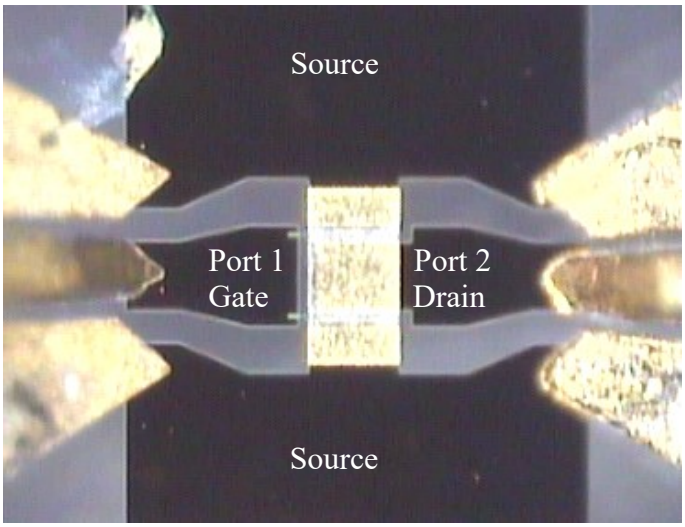


Figure 2.9 Micrograph of a fabricated GaN HEMT with landed RF ground-signal-ground probes on device RF ports.

Measured S-parameters can be transformed to hybrid parameters (h-parameters) to obtain the current gain cut-off frequency f_T. h_{21} is forward-transmission hybrid or h-parameter that represents the current gain of the network with the output port short circuited and can be found from the S-parameters using equation [96]:

$$h_{21} = \frac{I_{out}}{I_{in}} = \frac{-2S_{21}}{(1 - S_{11}) * (1 + S_{22}) + S_{12}S_{21}} \tag{2.5}$$

Maximum oscillation frequency can be found using Masons unilateral power gain (U), which is defined by S-parameters as:

$$U = \frac{P_{out}}{P_{in}} = \frac{\left|\frac{S_{21}}{S_{12}} - 1\right|^2}{2\left[K\left|\frac{S_{21}}{S_{12}}\right| - Re\left(\frac{S_{21}}{S_{12}}\right)\right]} \tag{2.6}$$

where *Re* is the real part of the value and K is the Rollet stability factor , which is defined by S-parameters as:

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\triangle|^2}{2|S_{12}S_{21}|} \tag{2.7}$$

where $\triangle = S_{11}S_{22} - S_{12}S_{21}$. K indicates if the device is uncondtionally stable or conditionally stable (likely to oscillate without a stabilising network). If K>1 and $|\triangle| < 1$ the device is unconditionally stable, which means that it won't oscillate regardless of the

passive source/load network around it. If $K<1$ it means that the device is conditionally stable, i.e. stability depends on source and load terminations.

Another way of determining device stability is through geometric stability factor μ, defined as:

$$\mu = \frac{1 - |S_{22}|^2}{|S_{22} - \triangle S_{11}^*| + |S_{12}S_{21}|} \tag{2.8}$$

Geometric stability factor measures the distance from the centre of the Smith Chart to the nearest unstable region. The larger the value of μ, the more stable the device. The device is unconditionally stable if $\mu > 1$.

The maximum gain a transistor is capable of delivering at certain drain voltage is at the peak of transconductance for each drain voltage, therefore S-parameters of a given transistor are usually measured at these bias points. From the measured S-parameters one can then determine f_T and f_{MAX}, which then determines the frequency range over which a transistor can be used in a circuit. The unit gain current cut-off frequency f_T is defined as the ferquency at which $h_{21} = 1$ and can be derived from small signal parameters. In the saturation region, the small signal transistor model from Figure 2.8 can be reduced to the model in Figure 2.10, with a voltage source connected at the input and the output short-circuited:

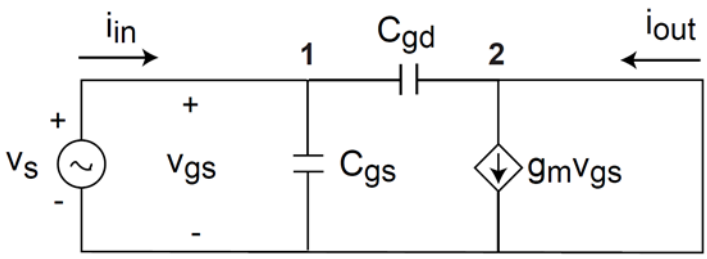


Figure 2.10. Intrinsic part of HEMT small signal model at the saturation with the output short-circuited and a voltage source connected at the input.

From this model i_{in} and at node 1 and i_{out} at node 2 can be defined as:

node 1: $$i_{in} - v_{gs}j\omega C_{gs} - v_{gs}j\omega C_{gd} = 0 \tag{2.9}$$

$$=\gg \quad i_{in} = v_{gs}j\omega(C_{gs} + C_{gd})$$

node 2: $$i_{out} - v_{gs}g_m + v_{gs}j\omega C_{gd} = 0 \tag{2.10}$$

$$=\gg \quad i_{out} = v_{gs}(g_m + j\omega C_{gd})$$

Then h_{21} can be rewritten as:

$$h_{21} = \frac{i_{out}}{i_{in}} = \frac{g_m - j\omega C_{gd}}{j\omega(C_{gs} + C_{gd})} \tag{2.11}$$

giving magnitude of h_{21} as:

$$|h_{21}| = \frac{\sqrt{g_m^2 - j\omega^2 C_{gd}^2}}{\omega(C_{gs} + C_{gd})} \tag{2.12}$$

which then can be approximated at low frequencies, when $\omega \ll \frac{g_m}{C_{gd}}$ giving:

$$|h_{21}| = \frac{g_m}{\omega(C_{gs} + C_{gd})} \tag{2.13}$$

and at high frequencies, when $\omega \gg \frac{g_m}{C_{gd}}$:

$$|h_{21}| = \frac{g_m}{\omega(C_{gs} + C_{gd})} < 1 \tag{2.14}$$

h_{21} can then be plotted against ω in logarithimic scale as showed in Figure 2.11:

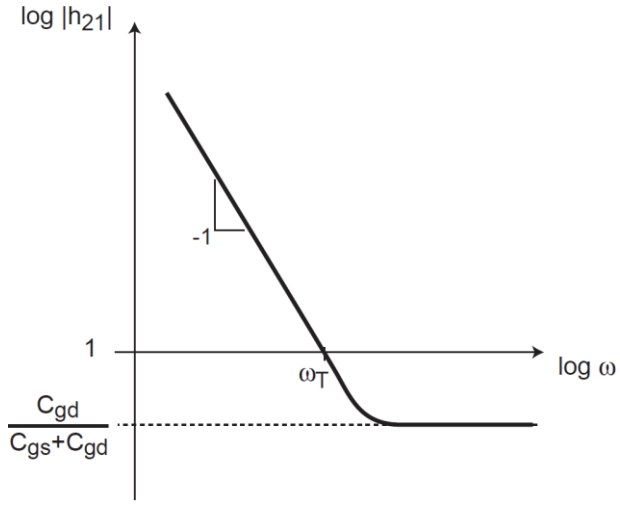


Figure 2.11 Logarithmic magnitude of h_{21} against ω_T.

it can be seen that $|h_{21}|$ becomes unity at ω_T :

$$\omega_T = 2\pi f_T = \frac{g_m}{C_{gs}+C_{gd}} \tag{2.15}$$

So f_T can be defined as:

$$f_T \approx \frac{g_m}{2\pi(C_{gs} + C_{gd})} \tag{2.16}$$

The maximum oscillating frequency f_{MAX} is defined as the frequency at which Masons unilateral power gain U = 1. Similarly to f_T , f_{MAX} can also be estimated using intrinsic device parameters the by following equation [97]:

$$f_{MAX} \approx \frac{f_T}{2\sqrt{(R_i + R_S + R_g)g_{ds} + (2\pi f_T)R_g C_{gd}}} \tag{2.17}$$

Typically transistors are used in a circuit up to one fourth of the obtained f_{MAX}. Transistor bonding pads add parasitics to the measured S-parameters which decrease the frequency performance by around 10%, and therefore these parasitics should be excluded when calculating the operational frequency of the circuit with a given transistor.

2.8. Summary

This chapter described the basic theory of GaN HEMTs from the epi-layer structure to the physics behind the 2-DEG formation, Ohmic contact formation and the operational principles of the HEMTs. The role of the spontaneous and piezoelectric polarization in the creation of the 2DEG channel was also discussed. A description of the small signal equivalent circuit model and its importance was also provided. In addition, the procedure of determining transistor cut-off frequencies is briefly described in this chapter.

3. GaN HEMT device fabrication methods

3.1. Introduction

This chapter describes fabrication processes used during this project for AlGaN/GaN HEMT fabrication on commercially grown GaN on SiC substrates. These processes include lithography, metallisation, etching and dielectric film deposition. As material growth is done outside of the University of Glasgow, growth methods are discussed only briefly. All fabrication processes are done at the James Watt Nanofabrication Centre (JWNC).

3.2. Epitaxial material growth

Epitaxial material growth involves the transporting of atoms of required species from high purity sources to the surface of a substrate wafer. The quality and uniformity of the grown layered epitaxial structures highly depend on the growth parameters such as temperature, pressure and gas flow rates, therefore these parameters must be optimised for the application. The two main growth techniques employed for growing GaN based heterostructures are metal organic vapour deposition (MOCVD) [98] and molecular beam epitaxy (MBE) [99]. Wafers grown in this project were commercially grown using, mostly using MOCVD, except the wafer structure with a thicker GaN cap (details in Chapter 4) which was grown using the MBE growth technique.

3.2.1. MOCVD

The most popular growth method in GaN industry is metal organic chemical vapour deposition (MOCVD) due to its low cost compared to other available techniques [100]. Typical growth rates in MOCVD are 1-2 µm/hr [101] which is around twice as faster compared to MBE growth. The growth temperature of MOCVD growth is typically above 1000°C. MOCVD chambers can grow GaN based materials for 36×2 inch wafers simultaneously with GaN on SiC being produced on up to 6 inch wafer sizes[102].

The basic MOCVD system consists of the following parts:

• Load lock: used to transfer wafers in and out of the reaction chamber. Load lock is maintained at high vacuum with a turbo molecular pump.

• Gas handling unit: this system has the precursors and all of the valves and instruments necessary to control the gas flow to the reaction chamber.

• A reaction chamber: all the reactions required for creating the epilayers for wafers take place in this chamber.

• Heating and temperature system: this controls the temperatures in the reaction chamber required for various MOCVD reactions.

• Exhaust, pumping, and pressure control system: this consists of a vacuum pump for low pressure operation and an exhaust part to remove waste products.

Typical gas reaction of GaN growth are given by this equation of chemical reaction:

$$TMG+NH_3 \rightarrow TMG:NH_3 \rightarrow GaN+3CH_4 \quad (3.1)$$

Where is TMG is Trimethyl gallium, NH_3 is ammonia and CH_4 is methane.

A schematic of an MOCVD growth chamber is shown inFigure 3.1.

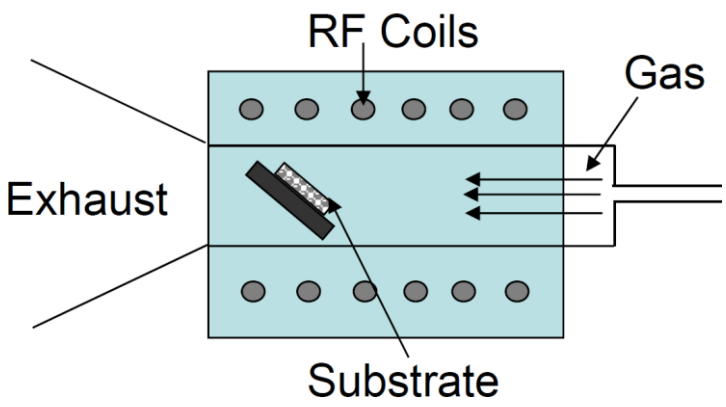


Figure 3.1. Schematic illustration of an MOCVD chamber

3.2.2. MBE

Molecular beam epitaxy (MBE) is a growth technique with a very precise definition and increased flexibility of the polarity of interface. These are the main advantages of this technology. Typical growth temperature is around 700 °C which is lower than MOCVD. However, the typical growth rates for GaN material in an MBE system is around 0.5-1 µm/hr which is slower than MOCVD growth, making it a more expensive technique. MBE is therefore mainly used for research purposes, since this high-quality material can be used for proof of concept experiments. Basic MBE system consists of the following parts:

• Load lock: used to transfer wafers in and out of the reaction chamber. Load lock is maintained at high vacuum (10^{-8} Torr) with a mechanical pump and ion pump.

• Reaction chamber: where all the reactions required for creating the epilayers for wafers take place. It consists of a sample manipulator, growth cells (effusion cells), reflection high-energy electron diffraction (RHEED) transmission mode monitoring system for process control, cryo-shrouds and pumps [103].

• Effusion cells are place where a solid or liquid source material is held in an inert crucible which is heated by radiation from a resistance-heated source. Usually a thermocouple is used to provide temperature control.

A schematic of a typical MBE chamber is shown in Figure 3.2**Error! Reference source not found.**.

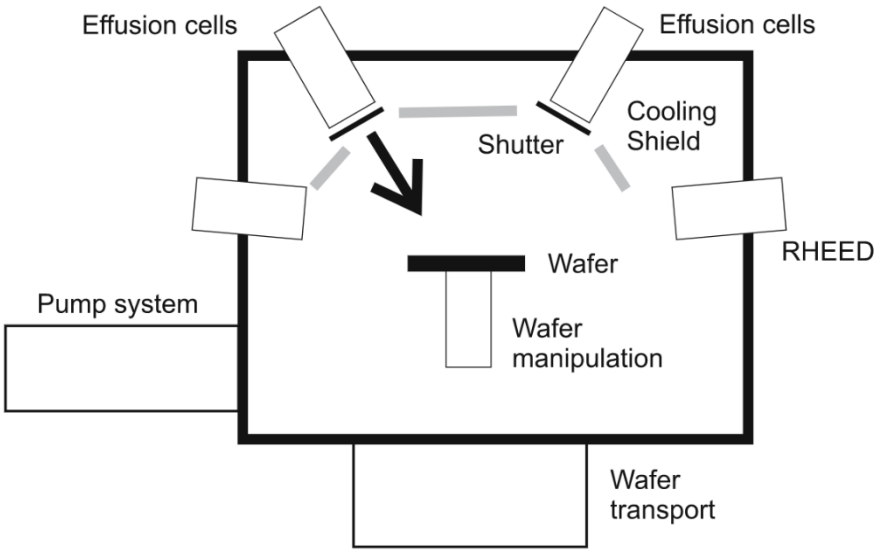


Figure 3.2. Schematic illustration of an MBE growth chamber.

3.3. Lithography

Lithography is the transferring of patterns onto substrates, which is an integral step in the manufacturing of devices. It is the fundamental process for nano- and micro-fabrication of semiconductor devices. The two main types of lithography are optical lithography known as photolithography and electron beam or e-beam lithography. Photolithography is a relatively fast process with an alignment accuracy of 1 μm and can be used to fabricate features down to 1 μm. E-beam lithography, on the other hand, has an alignment accuracy of 0.5 nm and so can be used to fabricate submicron features down to 3 nm, but it is a relatively slow, expensive process and has complex processing steps.

3.3.1. Photolithography

Photolithography is the process of transferring patterns onto the substrate by applying ultraviolet (UV) radiation through a mask plate to radiation sensitive compound, usually a polymer, known as photoresist. There are two types of photoresists: positive and negative tone resists. The difference between them is in how they react with UV light. When a positive resist is exposed by UV light it breaks the chains in the polymer at the exposed areas which become soluble to developer solutions. When developed positive tone resists result in the same pattern as on the mask plate. In contrast, negative tone resists are soluble when not

exposed and become non-soluble when exposed to UV light. Therefore the developed pattern with negative resists results in reverse image of the mask plate.

In this project various Shipley S1800 series positive photoresists and AZ series photoresists were used. Depending on the resist thickness, the exposure time necessary for the UV light to penetrate through the resist is different. In this project UV exposure is generated by Suss Mask Aligner (MA6) shown in Figure 3.3 which uses wavelength of 365nm. This tool offers 6 different contact types between the mask and the sample: proximity contact, soft contact, hard contact, low vacuum contact , vacuum contact and flood exposure. In proximity contact mode a preselected gap is programmed between mask and substrate. The damage of mask is reduced, but resolution is reduced too. This contact mode gives a resolution of 2.5 µm. Soft contact mode uses a slight mechanical pressure to produce contact between mask and substrate giving resolution of 2 µm. Hard contact similarly to soft contact has additional force applied to substrate, thus improving the resolution to 1 µm. In low vacuum and vacuum contact mode the contact between mask and substrate is optimized by evacuating the gap. This mode performs the highest resolution level giving resolution of 0.7 µm. Flood exposure mode is typically used for blanked exposing the resist on the substrate with no mask plate. In this project for all the photolithography steps a hard contact mode is selected. For resist development, the following developing solutions were used: Microdeposit developer concentrate, Microdeposit MF319 and AZ400K developers.

Figure 3.3. Photo of the Suss Mask Aligner (MA6).

In this project photomasks for device fabrication were designed using a software Tanner EDA L-edit by Mentor Graphics[104]. This software has CAD drawing tools for drawing 2D geometries. The design was then exported as a GDSII (Graphic Data System – Version

II) datatype file and sent to company Compugraphics International Ltd for mask plate production.

3.3.2. Electron beam lithography

Electron beam lithography is the process for transferring of patterns onto the substrate by electron radiation onto the e-beam resists, which are also polymers. Electron beam lithography offers submicron pattern transfer directly to the wafer without using a mask plate, i.e. the pattern is directly transferred to the e-beam lithography tool and the electron gun moves across the wafer and exposes the pattern. Another advantage of the e-beam lithography is that different doses of exposure can be selected within one exposure. This means that different doses can be selected for different regions of the sample, e.g. towards the edges of a sample where the resist films are usually thicker. Moreover, this technique also allows for precisely controlled operation, ultra-high resolution and excellent alignment accuracy of 0.5 nm.

The main part of an e-beam tool is the column. It is the part of the tool where electron beam for pattern exposing/writing is created and is shown in Figure 3.4. Electron beam is generated by electron gun which usually is a thermionic field emission gun purpose-built for an e-beam tool. Electron gun is at the top of the column. Then the electron beam is guided through magnetic condenser lenses that focus the electron beam. These lenses can have varying strength of the magnetic field which then lets to vary the beam current depending on the desired exposure parameters. Typically, electron beam currents are in the range of 1 nA to 100 nA. The beam then goes through deflection coils that are used to steer the beam. The deflection system usually can defer the beam by about 1 mm and the maximum deflection is limited by aberration errors. To write patterns over larger areas the stage where the sample is positioned is being moved. Therefore larger patterns are typically divided in to fields and each field is written separately. Stage also has an interferometer with precision below 1nm which then allows to calibrate the whole system to sub-nanometre precision.

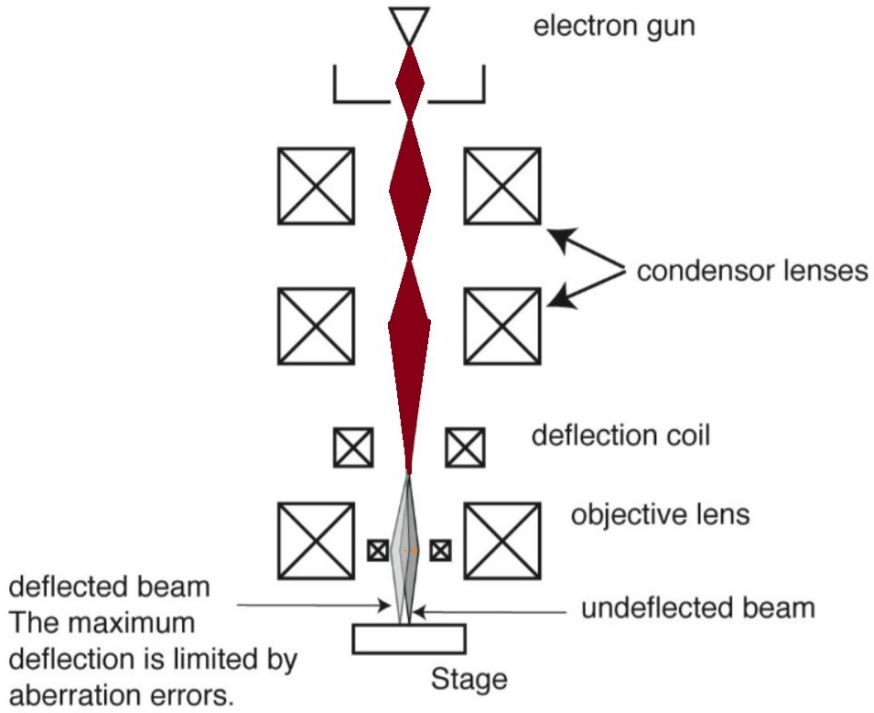


Figure 3.4. Schematic illustration of the column of an electron beam lithography tool.

In this work the Vistec VB6 UHR EWF shown in Figure 3. 5 was used.

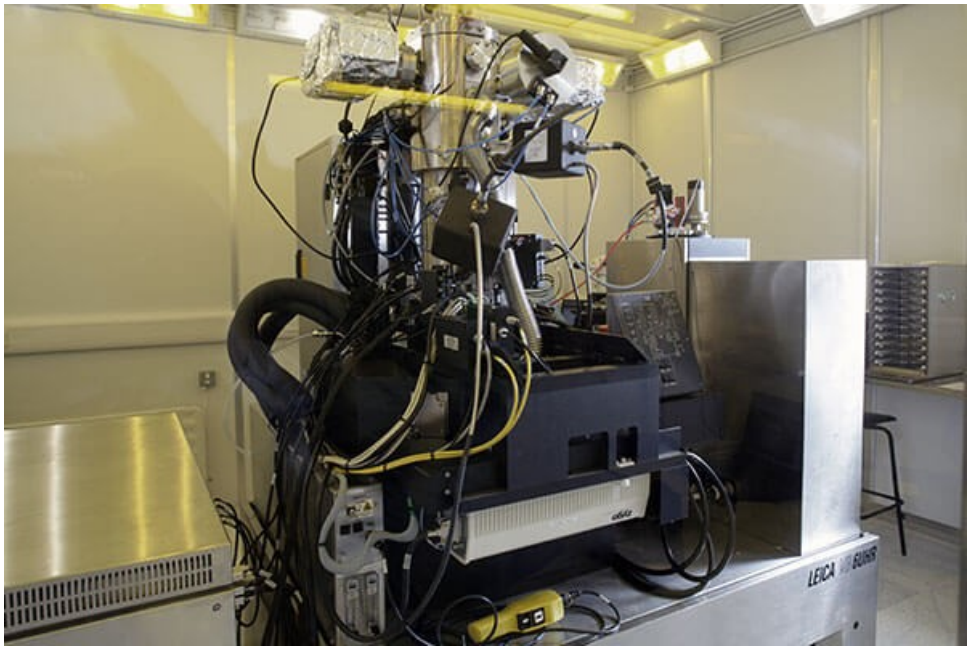


Figure 3. 5 Photo of the electron beam lithography tool Vistec VB6 UHR EWF.

3.3.3. Alignment

Most micro and nano-scale electron devices require more than one lithography step in order to make a functional device therefore each fabrication level must be aligned with the

previous one. For instance, to fabricate GaN HEMT gate electrodes of a device must be aligned with Ohmic contacts in the same device. Thus, usually the first lithography pattern transferred onto a wafer has a set of alignment markers which are used as a reference when aligning the rest of the patterns. An example of transistor layout in L-edit is shown in Figure 3.6. Here each lithography pattern is in a different colour. The bottom right of Figure 3.6 shows alignment markers for photolithography which are used to align layers manually under the microscope. Illustration of all the fabrication steps are given later in this chapter in Figure 3.19. The bottom left of Figure 3.6 shows e-beam alignment markers which are designed to be found by the e-beam tool. These markers need to be designed as big crosses with thin arms so that rough alignment can be easily done by the technical staff that loads the sample/wafer into the e-beam machine. The tool uses these crosses for defining the correct placement of the pattern to be written and for defining the contrast between the substrate and marker material (often metal, like gold) to find the square markers indicated in the illustration. At least 2 square markers are necessary to correct any rotational errors.

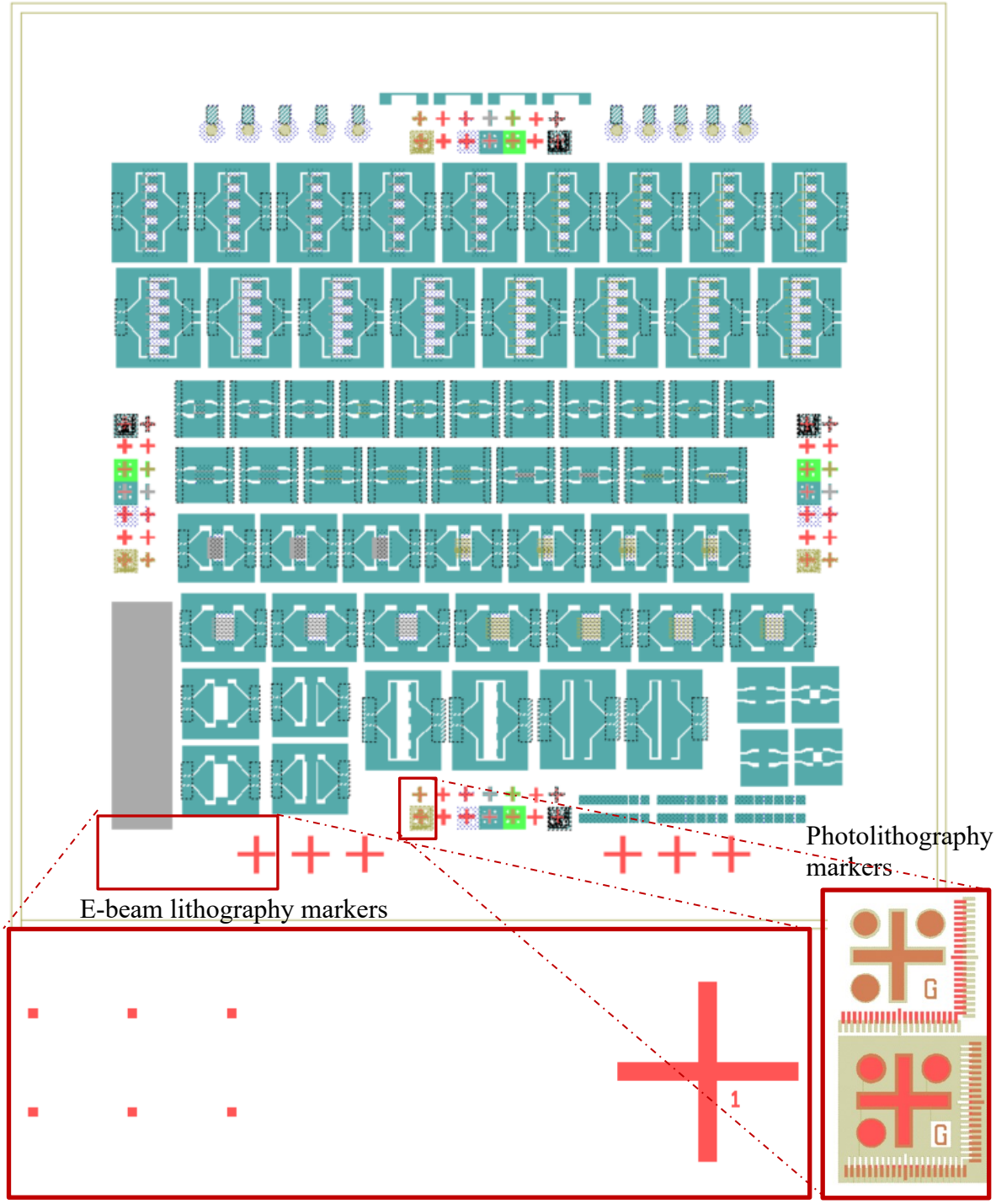


Figure 3.6 Mask file for GaN HEMT devices designed for combining photolithography and e-beam lithography processes indicating photolithography markers (bottom left) and e-beam lithography markers (bottom right).

3.4. Metallisation

One of the most important steps in semiconductor device fabrication is a metal-semiconductor contact formation. There are several ways how to deposit metal onto semiconductor surfaces. In this project electron beam evaporation, sputtering and electroplating were used.

3.4.1. Electron beam metal evaporation

When an electron beam is focused directly towards a solid metal target it causes the metal to evaporate under certain conditions. This metal crucible is water-cooled such that only the surface where the electron beam is focused evaporates, therefore evaporated metals using electron beam are high purity films without any contamination. In this project the tools used for metal evaporation is Plassys MEB 550S (further referred as Plassys II) and Plassys MEB 450 (further referred as Plassys IV). Photo of the Plassys IV is shown in Figure 3.7. These tools provide very precise metal film evaporation through the control system that first pumps and establishes the vacuum in the chamber is in the range of 10^{-6} to 10^{-8} Torr. Then the electron gun is switched on and a stable deposition rate is established. The sample is protected by a shutter from any metal being deposited during this initial stage. Only after a stable deposition rate is established, does the shutter open and metal gets deposited on the sample. During the deposition, metal thickness is monitored using feedback of the oscillation frequency from a quartz crystal, which is inside the chamber. As this is very precise metal deposition with typical rates of 0.3-0.5 nm/s, this is usually used for metal layers of up to 1 µm. The process of metallisation by electron beam evaporation is illustrated in Figure 3. 8. Plassys IV has an additional feature, an argon (Ar) source inside the chamber behind an additional shutter which lets one to have an in-situ Ar surface treatment before metallisation. In this project Ar surface pre-treatment was used before Ohmic metal deposition since it removes the native oxides leaving the surface essentially free from oxides which naturally appear within nano-seconds when the GaN surface is exposed to the atmosphere. In-situ Ar pre-treatment before Ohmic contact metallisation also roughens the surface leading to better metal adhesion.

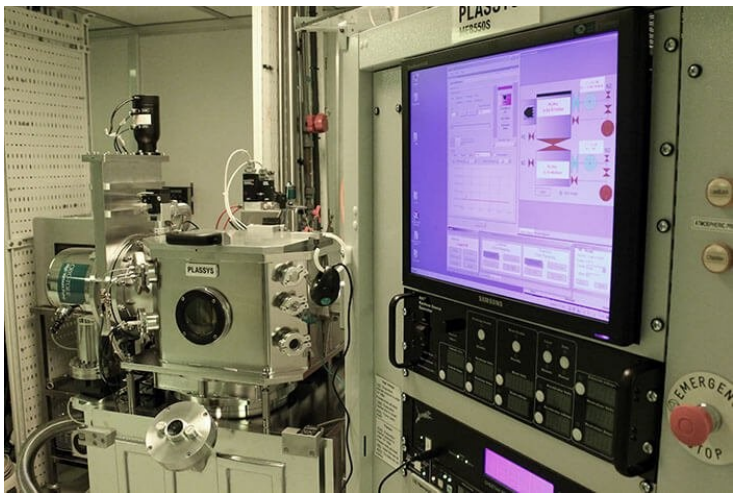


Figure 3.7 Photo of the metal evaporation tool Plassys IV.

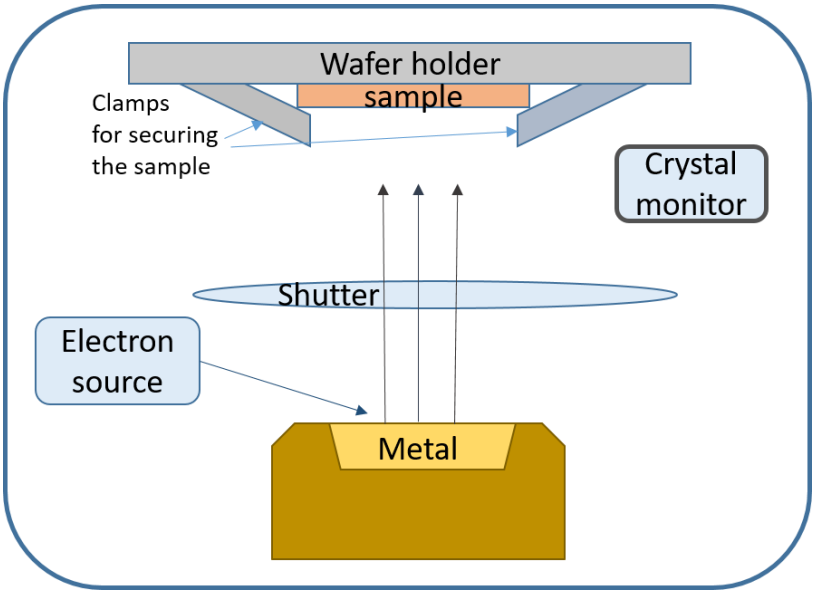


Figure 3. 8. Illustration of the mechanism of metallisation by electron beam evaporation.

3.4.2. Metal lift-off technique

As evaporated metal is directional, it evaporates on the whole exposed surface vertically and a lift-off process can be used to define metal features on the semiconductors. The lift-off process used in this project consists of a bilayer of resists that create an undercut profile. The undercut profile is necessary for the resist remover to access the resist under the metal in the region where it needs to be lifted off. This is achieved with LOR10 and S1805 resists when using photolithography and is illustrated in Figure 3.9. In the case of e-beam lithography this can be achieved by using e-beam resists with different molecular weights, since the resists with smaller molecular weights develops faster so it can be used as the lower layer of the bilayer structure.

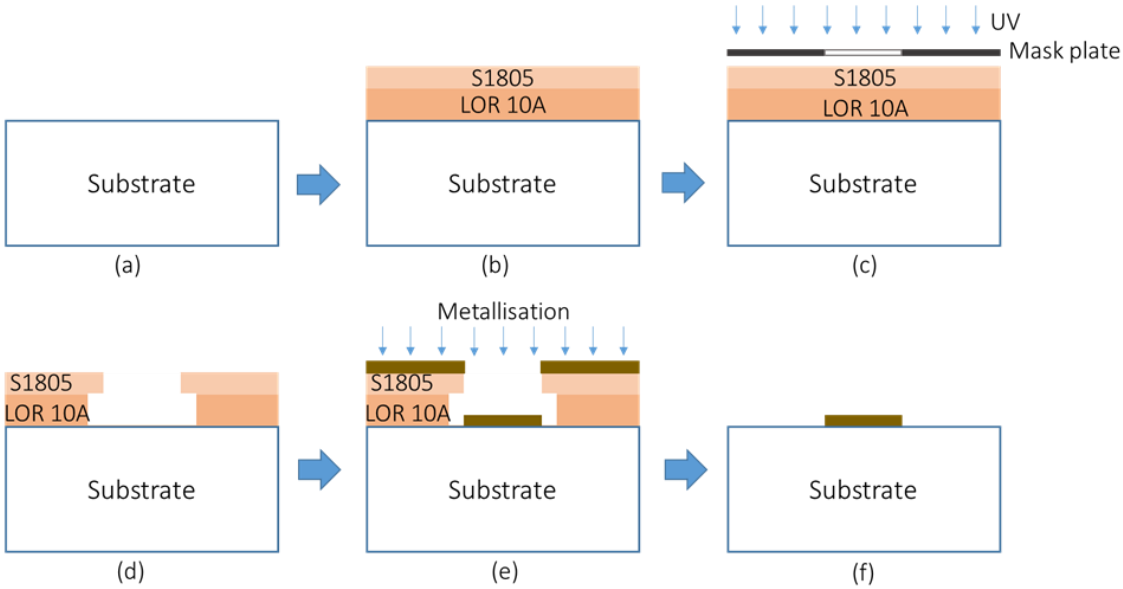


Figure 3.9. Metal lift-off process for photolithography.

3.4.3. Electroplating

Electroplating is a process widely used in industry because it allows the metallisation of up to a few tens on micrometres of the required metal at a time and has less metal waste compared to sputtering and evaporation since metal can be deposited only at the required areas instead of the whole wafer. In this process, an electric current is passed through a solution called an electrolyte that contains the required metal ions. This is done by submerging two electrodes into the solution as illustrated in Figure 3.10 and connected in a circuit with a power supply. When the current flows through this circuit the electrolyte splits up and metal atoms from the solution are deposited onto one of the electrodes. To electroplate metal onto a semiconductor, typically a thin layer of evaporated or sputtered metal (called the seed layer) is used to make an electrical connection between cathode and the surface that requires electroplating. To plate metal only on specific areas, the wafer is patterned above the seed layer with resist and as current flows the metal is electroplated only on the resist openings above the seed layer. This process is typically used for large features with high tolerance in metal thickness as the electroplated metal is non uniform.

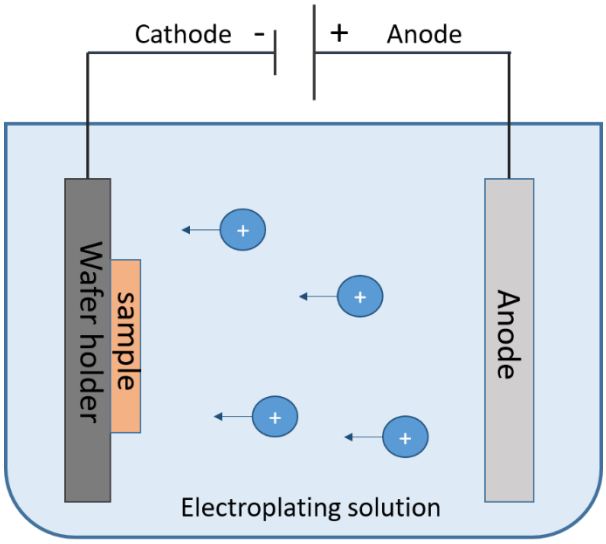


Figure 3.10 Illustration of metal electroplating process.

3.5. Annealing

Rapid thermal annealing is a process widely used in semiconductor fabrication where a single wafer is heated up in order to affect its electrical properties. This can be done is a chamber filled with a gas such as nitrogen (N_2) or forming gas. Convectional Ohmic contacts for GaN HEMTs with Ti/Al/Ni/Au metal stack requires a 30-45 second annealing step at 750°C-950°C in N_2 ambient in order to create the TiN alloy underneath the contact to ensure

electron flow from the contact into the 2DEG. For this step Jipelec JetFirst 200 rapid thermal annealing (RTA) machine shown in Figure 3.11 is used.

Figure 3.11 Photo of the Jipelec JetFirst 200 rapid thermal annealing (RTA) machine.

3.6. Etching

Etching is a process to remove material, such as metal, semiconductor or dielectric material from the wafer. Some of the etching applications are device mesa isolation, selective material removal for device patterning, and (through-wafer) vias. Figure 3.12 shows the etching process using photolithography. As the etching solution or gas attacks not only the wafer but also the resists, one needs to make sure that the photoresist mask is sufficiently thick and can withstand the etching conditions. E-beam resits, metal and other materials such as dielectrics, polyimide etc. can also be used as etch masks. There are two etching methods; dry etching where the etchant is gaseous and wet etching where the etchant is in liquid form.

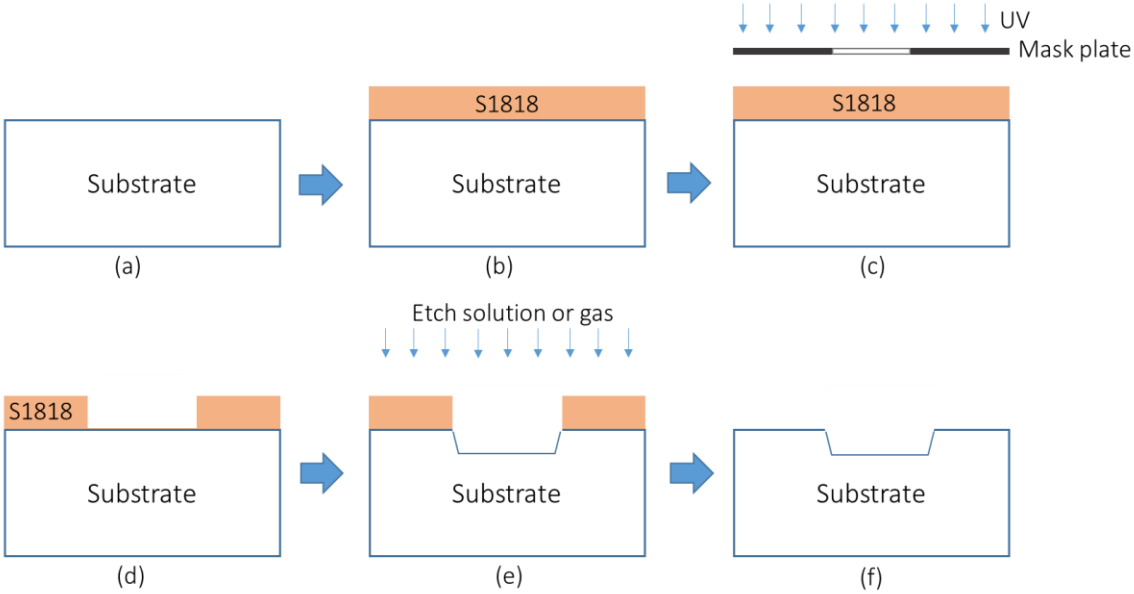


Figure 3.12 Illustration of an etch process using S1818 photoresist.

3.6.1. Wet etching

Wet etching is a process that relies on the chemistry between the reagents in the liquid etchant and the wafer surface to be etched. One of the main advantages of wet etch is that it does not cause damage to the deeper layers of the material that could degrade device performance. However, the wet etch process occurs in both vertical and lateral direction, therefore there is very limited control of the lateral etching and sidewall profiles are strongly dependent on the crystallographic directions within the crystal. Moreover, wet etching has limited uniformity. GaN has, however, high chemical stability which makes it highly resistant to conventional wet-etching. Therefore, dry etching is used for GaN.

3.6.2. Dry etching

Dry etching, also known as plasma or reactive ion etching is a process that relies on chemical effects between plasma generated species and the surface of the material to be etched. These species react with the surface atoms to produce volatile products which are then removed. The higher the volatility of these products the less redeposition takes place, resulting in a clean etched surface. The etch process is either entirely chemical resulting in an isotropic etch profile or may be partly physical from the kinetic energy of the accelerated plasma ions which enables and enhances the etch process leading to directional (more vertical) etch profiles. Since dry etching is a chemical process reactant gasses can be chosen so that they react only with certain materials introducing an important etching feature called selectivity. Thus layers of materials can be etched completely by dry etch stopping on underlying layers of different material composition.

In this project two dry ecth techniques were employed: reactive ion etching (RIE) with fluorine based chemistry such as SF_6/N_2 and chlorine based chemistries such as $SiCl_4$ and BCl_3/Cl_2 chemistries and inductively coupled plasma (ICP) etching with $BCl_3/Cl_2/Ar$ chemistry (complete list of the used etch parameters listed in the Appendix A). The main difference between them is that RIE has only one RF generator while ICP has DC and RF generators. GaN device isolation is typically obtained by dry etching the epilayers down to the semi-insulating buffer layer leading to a typical etch depth around 200 nm.

3.7. Deposition of dielectric materials

Etching is not the only way that plasma processing is used in semiconductor device fabrication. Similarly to GaN material growth, dielectric materials can also be deposited on a wafer. In this project silicon nitride (SiN_x) deposition is used as a passivation layer to

protect the GaN surface after device fabrication. In the JWNC, there is an inductively coupled plasma (ICP) deposition tool (PlasmaFab System 100) which is used for SiN_x deposition. Other options include plasma enhanced chemical vapour deposition (PECVD), which generally operates at 300 °C and can deposit up to microns of SiN_x films. PECVD deposited films are more thermally stable than ICP deposited films, however they often have relatively high concentration of hydrogen leading to low density [105]. This issue is often addressed by thermal annealing in different gas atmospheres [106][107], but PECVD deposition process is still advantageous due to high process reproducibility, highly flexible operation method and good step coverage. The advantage of using the ICP tool is that the deposition can be done at room temperature and flow rate of the typically used gases N_2/SiH_4 can be adjusted leading to low mechanical stress (-50 to +200MPa) and low refractive index (<2) of the deposited SiNx film [105].

3.8. Oxygen plasma treatment for mesa isolation

There are two main ways of achieving mesa isolation of GaN HEMT devices: by mesa etching, where the active layers around the device are physically removed by etching or by changing the material properties in such a way that the conducting (active) device layers are converted into non-conductive or non-active device layers leaving the device planar. This can be done by ion implantation[108], surface treatments [109] or by selective material growth [86]. Ion implantation and selective material growth are very complicated, expensive technologies that require high temperature processing. In this project an oxygen plasma surface treatment approach is chosen due to relatively easy implementation and low cost [13]

Oxygen plasma ashing is used routinely in semiconductor processing to remove photoresist residues after patterning. It is also used as such in our GaN processing but we noticed a drop in current levels between contact pads used to evaluate contact resistances whenever the exposure to the plasma was extended. This was investigated and developed into an isolation technique based on selective oxygen plasma treatment at room temperature [13]. In the literature, it is known that O_2 plasma can oxidize GaN layers [110] and this has been used to minimize gate leakage currents in AlGaN/GaN HEMTs through oxidation of the barrier layer surface underneath the gate electrode [111]. In this case, it is thought that the oxygen plasma treatment completely neutralizes the polarization at the interface between AlGaN barrier layer and GaN channel layer in the exposed desired areas as illustrated in Figure 3.13.

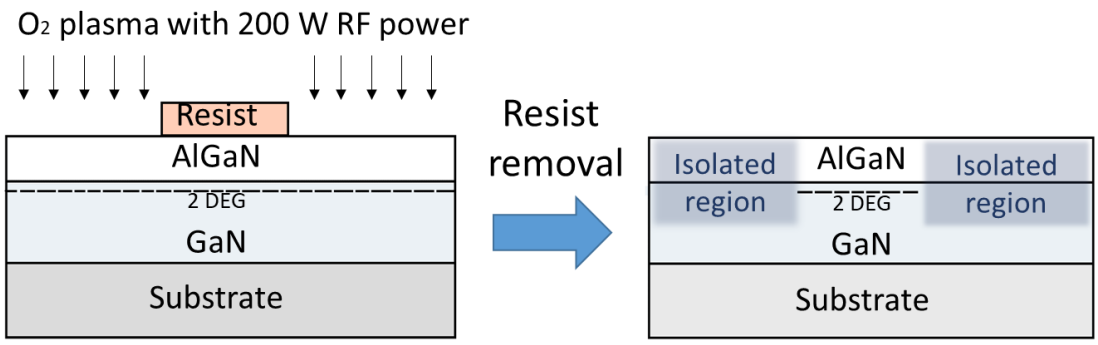


Figure 3.13 Illustration of the oxygen plasma treatment process

Using this approach, we obtain planar devices similar to ion implanted devices, but it is a simpler and lower cost process. For GaN HEMT heterostructures used in this project, O_2 plasma treatment at 200 W for 7 minutes can completely deplete the 2DEG underneath making it non-conducting, however the process parameters must be adjusted for each specific wafer depending of the barrier layer thickness and its Al mole fraction Gate leakage currents measured for different oxidisation process lengths of 0, 1, 4 and 7 minutes are given in Figure 3. 14. Here 7-minute isolation process is achieving low value of 180 nA/mm gate leakage currents at – 20V of gate voltage for 200nm gate length device presented in chapter 6. It was also observed that low RF power ashing (PlasmaFab RF Barrel Asher 505) of up to 80 W from 1 to 2 minutes does not have a degrading effect of the 2DEG properties, therefore this process used for resist residue removal after the photoresist development step.

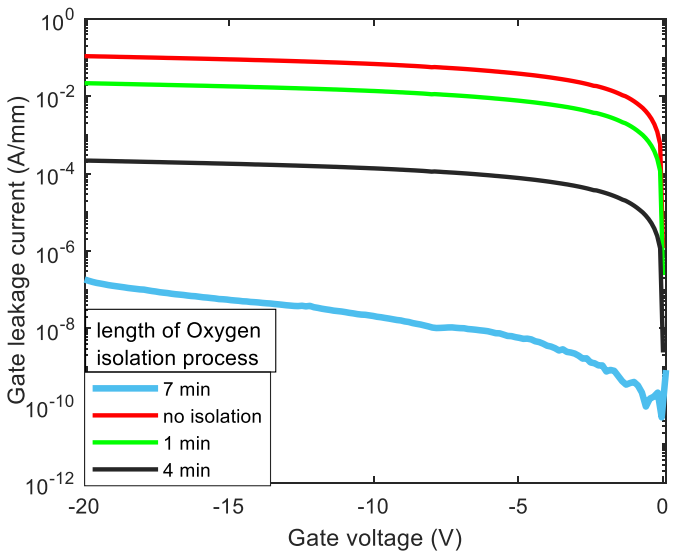


Figure 3. 14. Leakage currents of the samples with no isolation, and oxygen plasma treatment for 1 , 4 and 7 minutes.

To test the effectiveness of the O_2 plasma isolation method for RF applications, scattering parameter (S-parameter) measurements were performed on two 2000 µm long coplanar

waveguide (CPW) transmission lines with signal line width of 50 µm gap spacing of 25 µm and thickness of 2 µm of gold (Au), characteristic impedance of 50 Ω fabricated on AlGaN/GaN samples used for device fabrication. One sample was exposed to O_2 plasma prior CPW metallization and the other was not. Forward transmission coefficients (S21) of these two transmission lines are compared to a third CPW transmission line of identical length on a low-loss alumina substrate that is used for vector network analyser (VNA) system calibration. S21 measurement shows how much power that is delivered to port 1 is leaving the two port network (CPW line in this case) at port 2, thus an ideal CPW would have S21 as 0 dB, which is the case for the calibration substrate. The measurements are shown in Figure 3. 15. Here, one can see that non-isolated CPW line exhibits high losses across the entire measurement frequency range, reaching -50 dB at 67 GHz whereas the O_2 plasma isolated CPW has a loss of only -2 dB (which is attributed to characteristic impedance mismatch from the different substrate material, since the three lines had the same geometry) which is comparable to the measurement on the calibration substrate. This result shows that O_2 plasma treatment is an effective way of achieving isolated or non-conducting regions in AlGaN/GaN material.

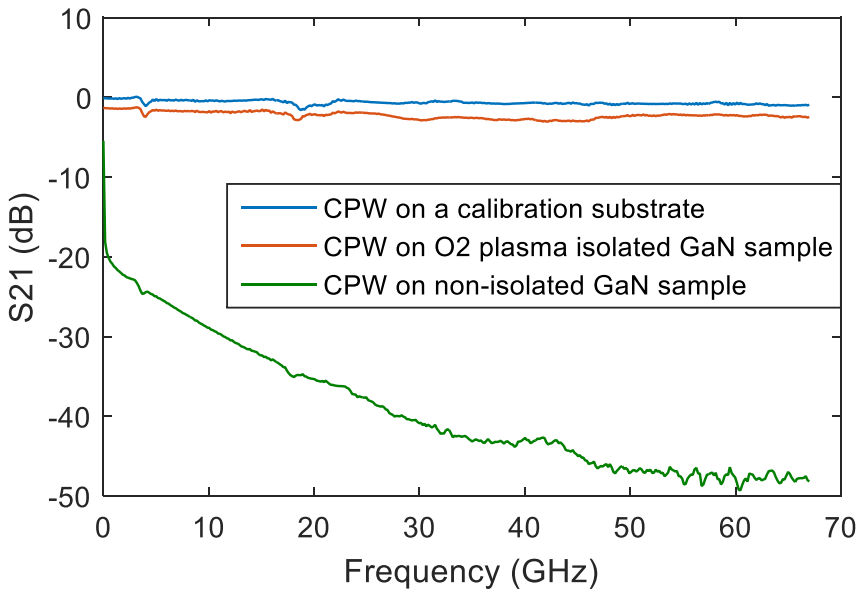


Figure 3. 15 S-parameter S21 measurements of three CPW transmission lines: CPW on a calibration substrate, CPW on an isolated AlGaN/GaN sample by O_2 plasma treatment and non-isolated AlGaN/GaN sample.

3.9. Air-bridge fabrication

Multifinger devices require all the source contacts to be connected. This can be done either above the device using air-bridges or through the substrate using vias and metallisation of the bottom of the device chip. In this work air-bridge approach was chosen since long CPW

transmission lines and T-junctions also require airbridges that connect the ground planes so that there is no potential difference at any given point on the ground plane. In this project air-bridges were made using photolithography. The fabrication process starts with applying the bottom resist Shipley S1828 which is then exposed and developed. This step defines the location for the posts of the air-bridges. After development to achieve the sloped sidewalls of the resist it is baked at 115 °C for 10 minutes in which the resist starts to reflow, and forms sloped sidewalls as shown in Figure 3.16. Then a thin metal layer of Ti/Au 20nm/20nm is deposited using metal evaporation in Plassys evaporation tool. This metal layer will serve as a seed layer for electroplating process. After that a second layer of S1828 is applied on top, which is then exposed and developed in a pattern of the air-bridges. This second UV exposure does not affect the bottom photoresist since barely any UV light gets through the metal seed layer. Then the sample is electroplated with 2 µm of gold (Au). Afterwards, the top resist layer is removed with acetone. Then the metal seed layer around the bridges is wet etched with Au etch and Ti etch solutions. Finally, the bottom resist is removed with acetone. Figure 3.16 shows an illustration of the full developed air-bridge fabrication process and the details of each of the processing steps can be found in Appendix A.

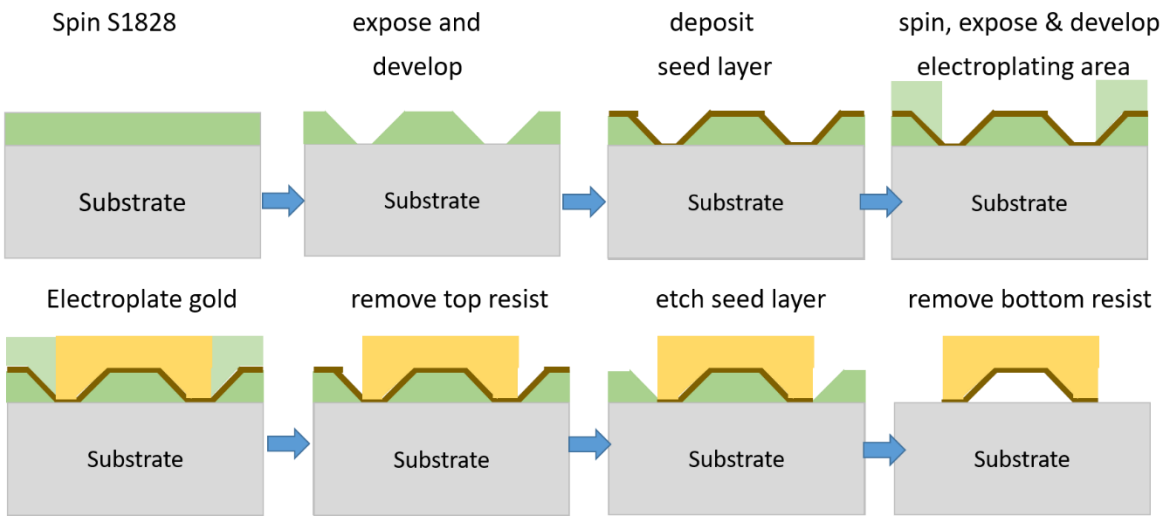


Figure 3.16 Schematic illustration of the air-bridge fabrication process.

This air-bridge fabrication process was then integrated into multifinger device fabrication flow. Examples of fabricated air-bridges connecting the source electrodes in a multifinger device and an air-bridge at a coplanar waveguide (CPW) T-junction are shown in Figure 3.17 and Figure 3.18respectively.

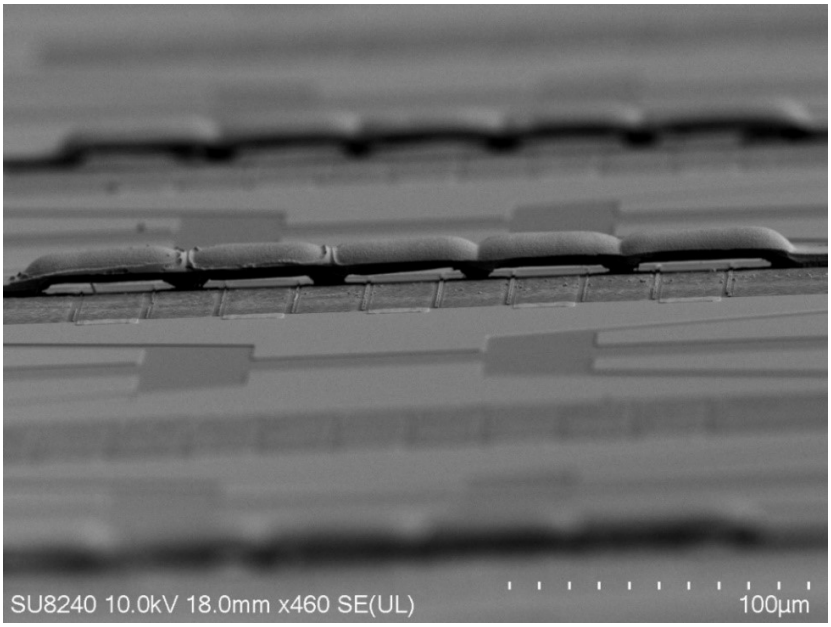


Figure 3.17 SEM image of an air-bridge connecting the source electrodes of a multifinger device with 10 fingers.

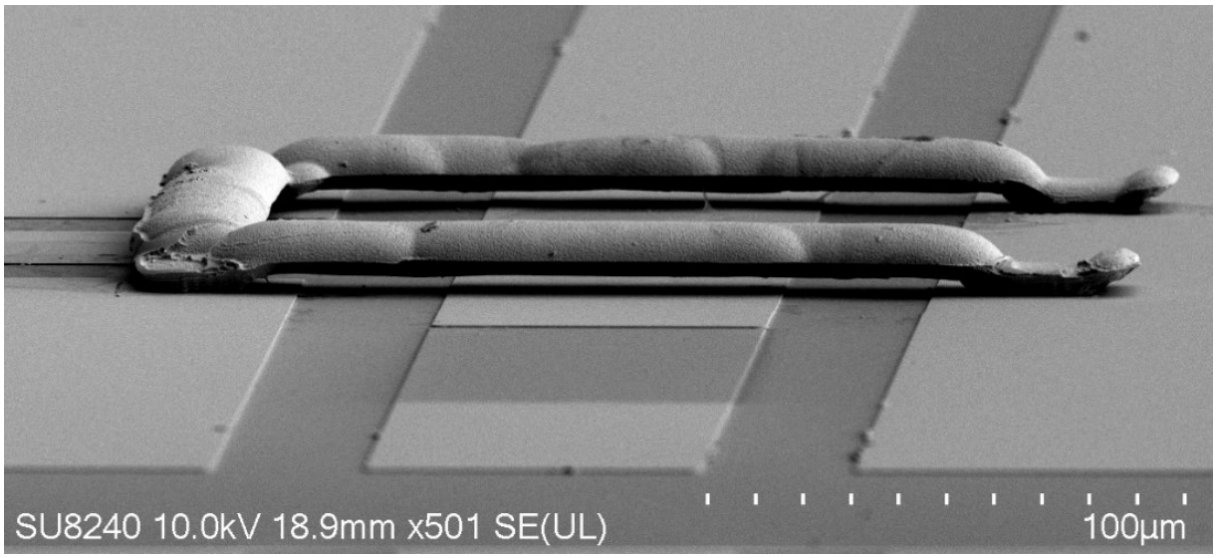


Figure 3.18 SEM image of a fabricated air-bridge over a CPW T-junction connecting ground planes.

3.10. HEMT fabrication flow

All the fabrication techniques described above such as etching, metal deposition and lift-off techniques can then be used to fabricate GaN HEMTs. Figure 3.19 shows the main steps in GaN HEMT fabrication. Details of each step can be found in the Appendix A.

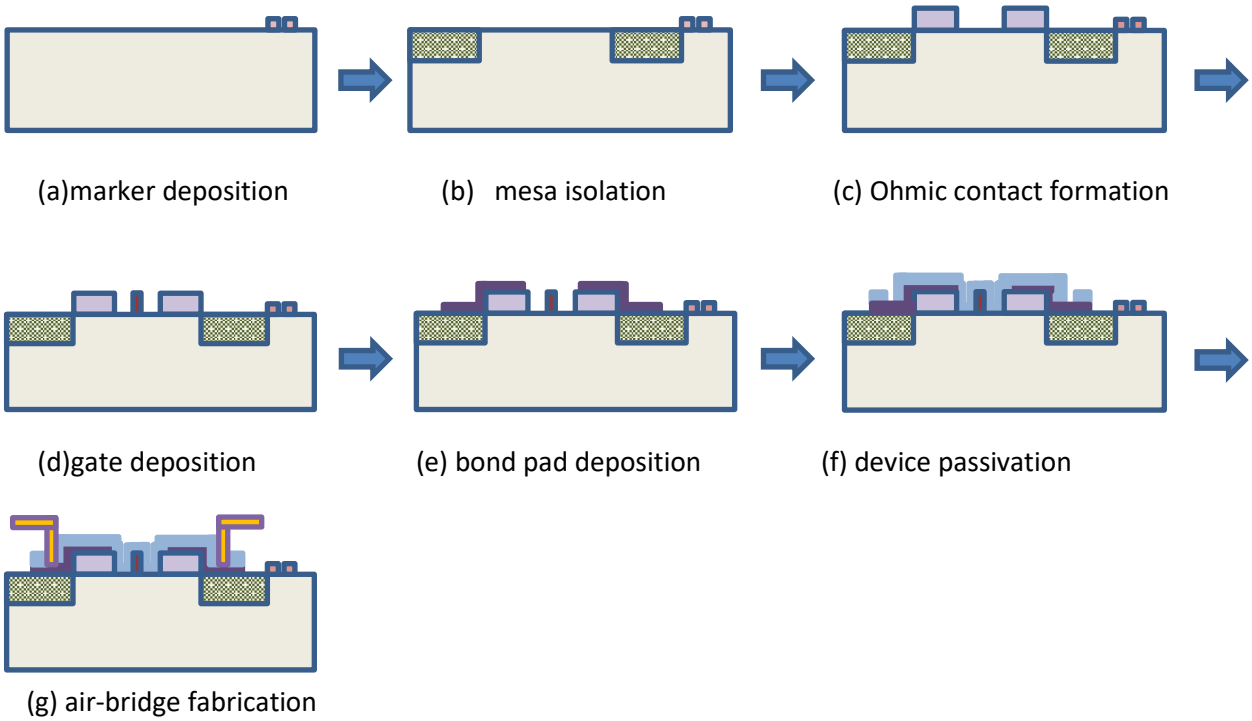


Figure 3.19 HEMT fabrication process, starting with alignment marker metallisation (a),isolation step (b), Ohmic contact metallisation and annealing (c), then gate metallisation (d), then bondpad metallisation (e), then passivation (f) and finished with source connecting bridges (g), which are required only for multi-finger devices

3.11.Summary

This chapter described details of different processing methods and steps involved in GaN HEMT fabrication starting from epitaxial growth to lithography, etching and different metallisation methods. Planar mesa isolation method by oxygen plasma have also been discussed. Full device fabrication flow involving mentioned techniques was described. Details of all the individual fabrication steps are listed in Appendix A.

4. Deep channel GaN HEMT devices

4.1. Introduction

AlGaN/GaN high electron mobility transistors (HEMTs) have a great potential for high-power and high-frequency applications due to the combination of high breakdown field, high sheet charge density and high electron velocity. Output-power densities of more than 30 W/mm at 4 GHz [39], 10.5 W/mm[112] at 40 GHz and 8.84 W/mm at 94 GHz [51] have been reported. However, one of the limitations of the today's technology is DC-RF dispersion or current collapse. DC-RF dispersion can be effectively reduced utilising SiN_x passivation in conjunction with field modulating plates (schematic image of a field plated device given in Figure 1.4). However, for some applications such as millimetre wave amplifiers, the filed plate structure is not desirable because of the added additional gate capacitance introduced by the field plate which degrades the high frequency performance. Device passivation with SiN_x layer without the field plates is the most used method to reduce the current collapse due to its effectiveness and simplicity. However, passivation with SiNx films does not remove the current collapse completely and is largely dependent on the deposition conditions making the reproducibility of gate leakage, breakdown voltages and effectiveness of dispersion removal is not always the same [113]. The use of SiNx as a surface passivant can cause issues with increased off- state drain and gate leakage currents which degrade the device DC and RF performance[114]Moreover, the coverage of the passivation film over three dimensional structures is not always achievable due to the physical process of the film deposition, which can result in voids in the fabricated structures as can be seen in an example in Figure 4.1 of a highly scaled GaN HEMT [115]. In this example there is a void created at the gate edge which it can negatively impact the device performance.

Other solutions to minimise the DC-RF dispersion that don't require passivation have been demonstrated using thick cap layers on the HEMT structure such as graded 250nm thick AlGaN cap layer [45], 260nm GaN Cap layer with Si delta-doping at the interface between AlGaN barrier and GaN cap layer [116] and N-polar GaN MIS-HEMTs with 120nm of GaN cap [117]. These epitaxial solutions offer high RF power densities up to 17 W/mm at 4 GHz [45], but either require doping, which then leads to a trade-off between high breakdown voltage and dispersion or have high off-state leakage currents of 0.27 mA/mm at V_{DS} = 20 V like in the case of N-polar epitaxial structure [117].

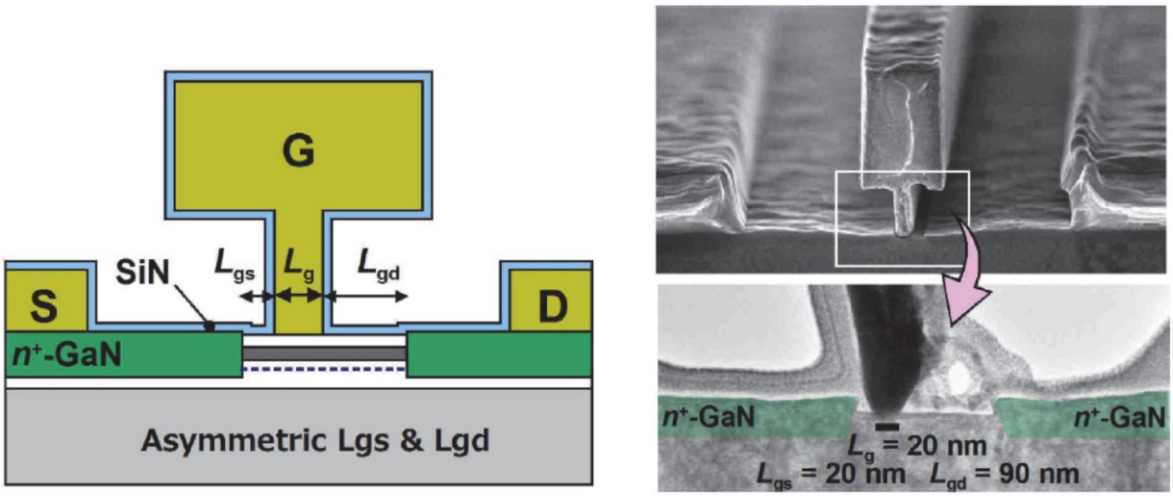


Figure 4.1 Schematic illustration and cross-sectional image of state-of-the-art GaN HEMT aggressively scaled for high frequency applications [115].

In this chapter an unpassivated GaN HEMT with 70 nm thick undoped GaN cap is discussed. This structure mitigates the surface effects without requiring passivation because the channel is buried deeper into the device and does not require any doping. The introduction of a thick undoped GaN cap layer significantly reduces the current collapse in the device and increases the off-state breakdown voltage to over 200 V for 2×200 µm wide devices. A gate annealing process was required and so was introduced to the fabrication process and led to reducing observed gate leakage currents by half. Fabricated devices show good DC-IV performance up to 100 V. The proposed device is also compared to conventional, AlGaN/GaN HEMTs passivated with thin 10nm SiN layer that are fabricated at the same time i.e. both devices have exactly the same processing conditions and the same device geometry, so the only difference between the wafers is the epilayer structure. The achieved results demonstrate great potential of this novel epitaxial approach for passivation-free GaN-based HEMTs for high-power applications.

4.2. Current collapse in unpassivated GaN HEMTs

4.2.1. Reported GaN HEMTs with thick cap layers

Current collapse also known as DC-RF dispersion is the reduction in current swing for RF as compared with the measured DC current due to the electron trapping within the structure, both in bulk layers and surface and are believed to be caused during the device epilayer growth and fabrication processes [28]. DC-RF dispersion and the gate leakage are strongly affected by surface charging, therefore thicker cap layers have been proposed to mitigate the DC-RF dispersion [118]. For thin GaN cap layer, electrons easily get in the gate-to-drain

region surface depleting the channel underneath thus leading to a significant extension of the gate depletion region towards the drain side. The extension of the depletion region then relaxes the field crowing at the edge of the gate resulting in lower gate leakage. However, the extended depletion region caused by surface charging is highly resistive and limits the RF current swing resulting in a DC-RF dispersion. By having the surface far away from the device channel, the impact of surface charging on device operation can be minimised since a minimal extension of the gate depletion region towards the drain side occurs thus minimising the DC-RF dispersion.

Moreover, using charge control analysis, it can be shown that the ability of the surface potential to modulate the charge in the channel is inversely proportional to the distance between the channel and surface. It can be evaluated by considering the threshold voltage, V_T (value of the surface potential at which the 2DEG in the channel is completely depleted also known as pinch-off voltage). The larger the threshold voltage is, the weaker the ability to modulate the channel from surface, thus the lower is the dispersion. The first-order approximation of the pinch-off voltage of the a thick capped AlGaN/GaN HEMT structure can be written as[119]:

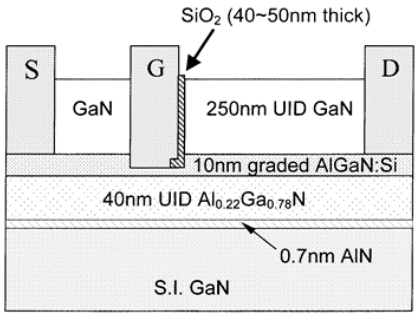
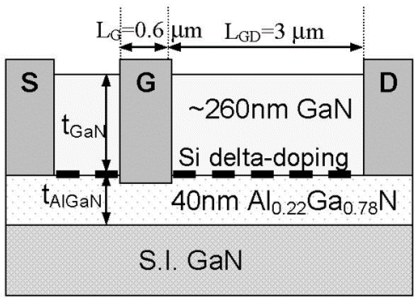
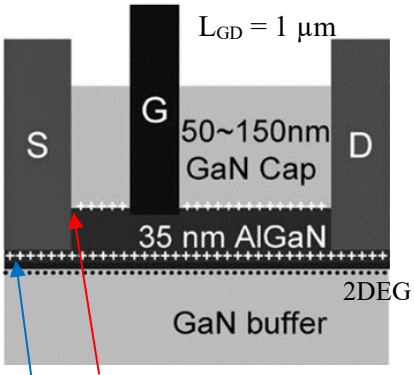
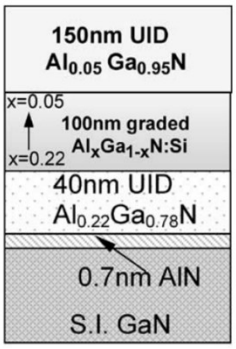
$$V_T = -\frac{q}{\varepsilon \cdot \varepsilon_0}(t_{GaN} \cdot \sigma_{Si} + t_{AlGAN} \cdot \sigma_1) \tag{4.1}$$

where t_{AlGaN} is the thickness of the AlGaN layer t_{GaN} is the thickness of GaN cap layer, σ is the polarization sheet charge density of AlGaN/GaN interface and σ_{Si} is the sheet charge density of Si delta-doping. Clearly threshold voltage is proportional to t_{GaN}, the thickness of the GaN cap layer, provided other parameters are fixed. The threshold voltage in the unetched drain access region of the deep-recessed HEMT can be as large as -40 V for a device with 200nm thick GaN cap layer, which is almost one order of magnitude higher than that of standard AlGaN/GaN HEMTs[116]. Dispersion is reduced or eliminated in deep-recessed devices since the surface effects to the channel are largely weakened.Several MOCVD grown GaN HEMT epilayer designs with thick GaN or thick graded AlGaN cap layers that have been reported in literature are summarised in Table 4.1with the following performance parameters: breakdown voltage V_{BR}, gate leakage currents and RF power densities with associated power added efficiency (PAE) and drain bias voltage measured at either 4 GHz or 10 GHz. The different designs are denoted as device A, B, C and D. All 4 compared designs have devices with 150 µm gate periphery (2x75 µm) showing breakdown voltages in the range of 90 to 200 V for gate lengths of 0.7 µm (design A and C) and 0.6 µm (design B and D). However, all the structures exhibited quite high gate leakage currents

above the industry requirement of 1 μA/mm. A Si delta-doped layer in all 4 of these structures is incorporated at the upper GaN/AlGaN interface to provide electrons to the channel and prevent positive charge accumulation which would lead to formation of a 2 dimensional hole gas or a parasitic channel. Each of the studies have indicated a parameter or method to reduce the gate leakage currents and increase the breakdown voltage as listed below.

- In design A covering the side wall of the gate at the drain side with 40-50nm of SiO_2 layer as illustrated in Table 4.1 leads to improvement in gate leakage currents from 10 to 0.3 mA/mm and increase in breakdown voltage from 35V to 90 V, however authors have mentioned that the introduction of SiO_2 negatively affects the device long term stability.
- Design B studied 3 different Si-doping densities at the GaN/AlGaN interface of 10, 7.5 and $5 \cdot 10^{12}$ and it was found that the lower doping density led to improvement in breakdown voltage from 50 V to 160 V and reduction in gate leakage currents from 2.17 mA/mm to 12 μA/mm.
- Design C studied 3 different undoped GaN cap thicknesses of 50 nm 100nm and 150 nm and it was found that the gate leakage currents were proportional to the GaN cap thickness. 150 nm cap layer had gate leakage currents of 1 mA/mm, 100 nm cap layer 10 μA/mm and 50 nm cap layer had 0.5 μA/mm for the structure with two layers of Si-doping as illustrated in Table 4.1.
- For design D it was found that fluorine treatment under the gate improved two terminal breakdown voltage from 35 to 120 V reaching a destructive breakdown of 200V.

Table 4.1 Published unpassivated AlGaN/GaN HEMT structures with their breakdown voltages V_{BR}, gate leakage currents and RF power densities with corresponding associated power added efficiency (PAE) and bias voltages V_D.

Device design	V_{BR} (V)	Gate leakage current (µA/mm)	RF power density with associated PAE at 4GHz	RF power density with associated PAE at 10 GHz	Ref.
A 	90	300		12W/mm PAE 40% V_D = 45 V	[120]
B 	160	12	6 W/mm PAE = 72% V_D =30 11.6 W/mm PAE = 63 % V_D = 50V	10,5 W/mm PAE 53% V_D = 48 V	[116]
C 		1000 (150nm) 10 (100nm) 0.5 (50nm)	5.6 W/mm PAE = 72 % V_D = 28 V		[118]
D  LGD = 3 µm	200		17 W/mm PAE = 50% V_D = 80V		[45]

From these 4 experimental studies it can be concluded that excellent RF power densities can be achieved from unpassivated GaN HEMTs with thick cap layers due to minimised DC-RF dispersion by increasing the distance between the channel and the device surface. However increasing the cap layer thickness decreases the 2DEG density [69] thus doping is introduced in the reported structures to achieve higher currents in the reported structures.

Higher doping densities at the channel are shown to increase the gate leakage currents and decrease the breakdown voltage. Since increasing the thickness of the GaN cap layer is shown to increase the gate leakage currents, it can be concluded that there is a trade-off between the minimising current collapse and having high breakdown voltages and low gate leakage in the reported structures with thick cap layers.

Another unpassivated device structure is shown in Figure 4.2[117]. This epilayer design is also grown by MOCVD growth but it is made using N-polar GaN instead of the conventional Ga-polar GaN material structure. In N-polar GaN structures the polarization fields are reversed compared to Ga-polar materials. N-polar devices are advantageous due to better electron confinement in the channel and better scalability since the charge inducing AlGaN layer is in the back barrier decoupling charge density and aspect ratio [121]. However growth process of N-polar GaN HEMT structures is more challenging due to the higher incorporation of oxygen then Ga-polar GaN growth process [122]. This unpassivated device design led to good RF performance with power density of 5.5 W/mm at 4 GHz with PAE of 74 % and a small signal gain of 14.5 dB at drain voltage of 24 V for 0.7 µm gate length device with total gate periphery of 100 µm (2 x50 µm). This was a successful demonstration of an unpassivated N-polar GaN HEMT with thick undoped GaN cap layer, however the breakdown voltage of this device was only 45 V.

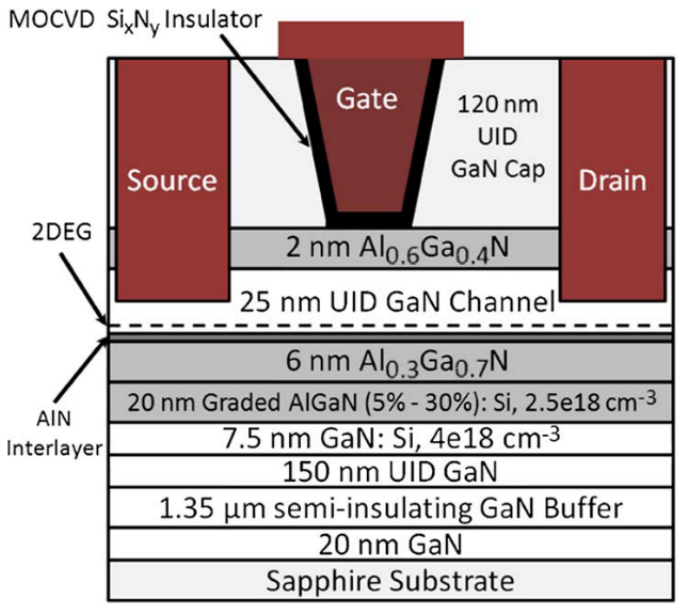


Figure 4.2. Unpassivated N-polar AlGaN/GaN HEMT [117].

Figure 4.3shows experimental results of drain current RF/DC ratio at drain bias voltage of 5 V for deeply recessed GaN HEMTs with thick cap layers of 0, 20, 50, 100 and 200nm of GaN cap layer. From the DC-RF dispersion point of view, for surface charging to be eliminated a thicker cap layer of 200 nm and above would be the most beneficial [123].

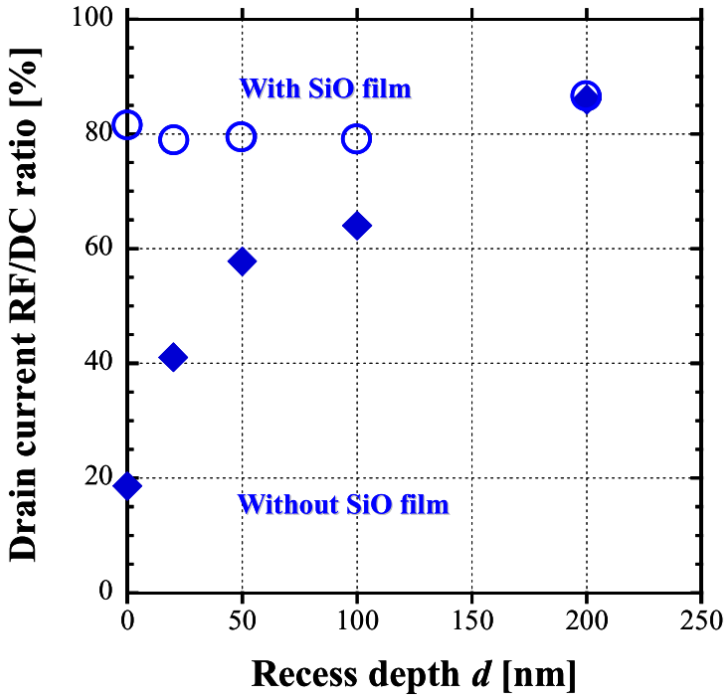


Figure 4.3. Experimental results of drain current RF/DC ratio at drain bias voltage of 5 V for deeply recessed GaN HEMTs with thick cap layers of 0, 20, 50, 100 and 200nm of GaN cap layer with (indicated as empty circles) and without SiO passivation layer (indicated as filled diamonds) [123].

4.2.2. Effects of increasing GaN cap thickness

With increasing GaN cap layer thickness there is positive charge accumulation at the GaN/AlGaN interface which leads to formation of a 2 dimensional hole gas or parasitic channel. It has been reported that 2 DEG density decreases and then saturates but Hall mobility increases and then saturates in AlGaN/GaN HEMT structures with 20nm $Al_{0.32}Ga_{0.68}N$ barrier layer with increasing GaN cap layer thickness as shown in Figure 4.4 [69].

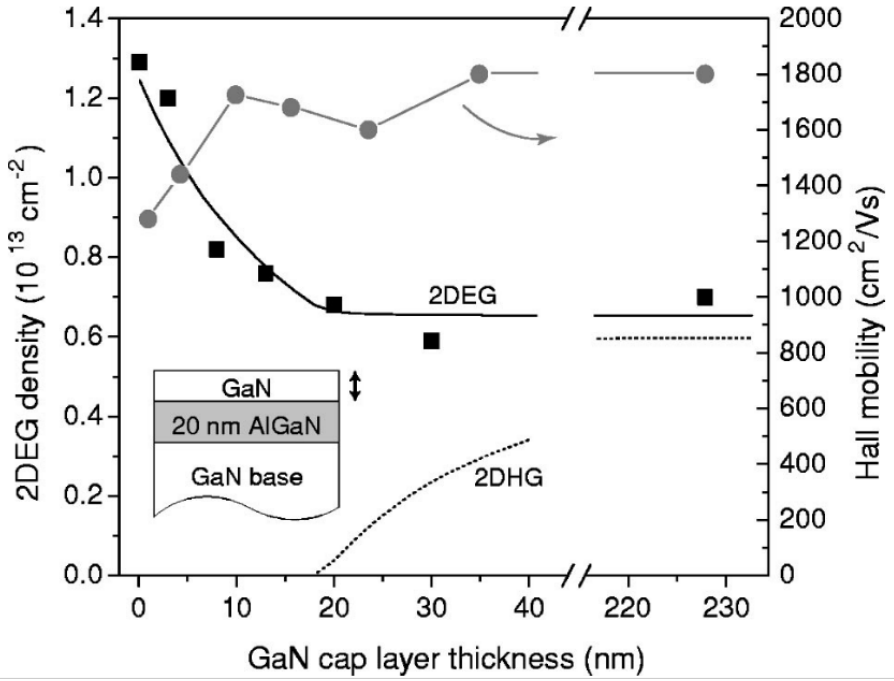


Figure 4.4. The effect of GaN cap layer thickness on sheet carrier density and Hall mobility, for a GaN/AlGaN/GaN heterostructure with a fixed AlGaN layer thickness of 20 nm, Al concentration of 32 %. The black solid line is a fit to simulations, and the gray line connecting the Hall mobility points is a guide for the eyes **[69]**.When a 2DHG is formed next to the 2DEG, one would think that both the 2DEG and the 2DHG would be probed when performing Hall effect measurements. However, an experimental study has shown that due to a much superior mobility and conductance of the 2DEG compared to the 2DHG, nearly all of the probing current flows through the 2DEG, with the effect that the measured sheet carrier density and mobility are completely dominated by the 2DEG [69]. Therefore, it is assumed that 2DEG dominates the electron transport in this kind of device and the IV performance of an undoped AlGaN/GaN HEMT with thick undoped GaN cap layer will be investigated in this chapter.

Form the gate leakage point of view some amount of surface charging helps to minimise the peak electric field and therefore gate leakage thus a thinner cap layer is beneficial. From the

devices reported in the literature leakage currents below 1 µA/mm have been reported only for structure with 50 nm cap layer [118]. A compromise on the choice of the GaN cap layer thickness must thus be reached at a specific drain voltage so that surface charging is not significant enough to cause noticeable DC-RF dispersion but very effective in supressing the gate to drain leakage currents. For structure C mentioned earlier that has 2 sets of doping at the AlGaN/GaN interfaces at drain bias voltage of 28 V the optimum GaN cap thickness was found experimentally to be 100 nm [118]. Moreover, it has also been reported that reduction in Si-delta doping from 10 x 10^{12} to 5 x 10^{12} in the thick capped devices lead to 180 times lower leakage currents [116]. Therefore, based on the device results published in the literature a cap layer between 50 and 100 nm would provide sufficient DC-RF dispersion and have leakage currents below 1µA/mm leading to high breakdown voltage. A structure with 70 nm of UID GaN cap layer with no doping within the structure was chosen for investigation and results are reported in the next sections of this thesis.

4.3. Experimental results

4.3.1. Device fabrication

In this thesis a different unpassivated device design without any doping is proposed to mitigate DC-RF dispersion. AlGaN/GaN HEMTs with deeply recessed contacts were fabricated on the structure with 70 nm thick undoped GaN cap shown in Figure 4.5 a). This wafer was a commercially sourced GaN epistructure with high thermal conductivity 4H-SiC substrate grown by molecular beam epitaxy (MBE). Using Hall measurements, it was determined that this structure had a 2DEG sheet carrier concentration of 2.7x10^{12} cm^{-2} and electron mobility of 780 $cm^2/V{\cdot}s$. The source and drain Ohmic contacts were obtained by recess etching of 70 nm using $SiCl_4$ followed by 1 minute 37% HCl 3:1 RO water dip followed by 45 second in-situ Ar treatment and Ti/Al/Ni/Au (30 nm /180 nm/40 nm/100 nm) metal evaporation followed by annealing in a nitrogen atmosphere at 800 °C for 30s. Ohmic contact resistances of 1 Ω·mm was obtained from TLM measurements. Sheet resistance measured by manufacturer at the surface was 3000 Ω/□ but from TLM measurements with the recessed Ohmic contacts it was calculated to be 2590 Ω/□. The Schottky gate contact was formed by recess etching 70 nm of the cap layer using SF_6/N_2 chemistry followed deoxidation using 1 minute 37% HCl 3:1 RO water dip and evaporation of Ni/Au (20 nm/400 nm) metals. Mesa isolation was achieved by dry etching the epilayers down to the buffer layer using $SiCl_4$ chemistry. Devices with width of 200 µm, gate length of 2 µm and drain to source distance of 7 µm were realised using photolithography are shown inFigure 4.6. Similarly, without recessing the Ohmic and gate contacts, same geometry devices were made

on a standard MOCVD grown GaN wafer with 2 nm GaN cap layer with epilayer structure shown in Figure 4.5 b). It is believed that during the deoxidation step prior the gate metal deposition on the standard wafer the 2nm GaN cap layer is removed. Ohmic contact resistance for the standard wafer was determined to be 0.5 Ω·mm.

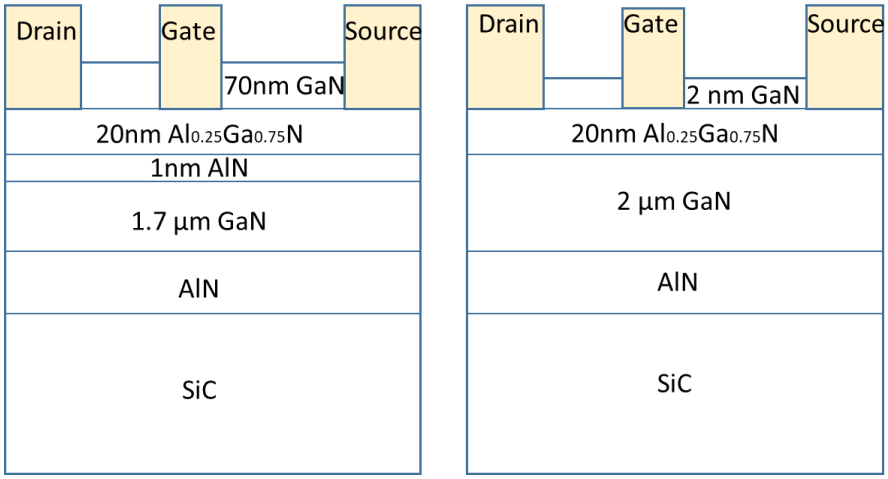


Figure 4.5. Wafer structure of the compared devices with a) 70 nm thick GaN cap (MBE grown structure) and b) 2 nm thick GaN cap layers (MOCVD grown structure).

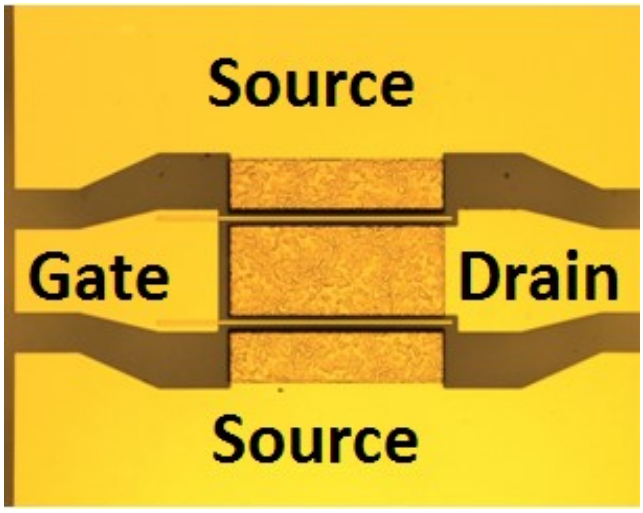


Figure 4.6. Micrograph of the fabricated 200 µm wide device with gate-length of 2 µm.

4.3.2. Device measurements

DC-IV measurements were performed on the device with 70 nm GaN cap layer and are shown in Figure 4.7(left) with gate voltages from -5V to 0 V with increments of 1 V. High gate leakage currents of 218 µA/mm at V_D = -20 V were measured on these devices and are attributed to the etch damage introduced during the gate recess process. During process optimisation steps it was found that a post gate deposition annealing process in rapid thermal annealing (RTA) tool at 400 °C at N_2 ambient for 10 minutes is effective to reduce the gate-source leakage currents down to 3.74 µA/mm at V_D = -20 V as shown in gate leakage measurements in Figure 4.7 (right). The leakage currents in the proposed device are lower

than in the doped structures with 100 nm and 150nm cap layers that were reported to have gate leakage currents of 10 and 1000 μA/mm respectively [118]. Note, as can be seen in Figure 4.5 the gate is recessed in the proposed device structure, i.e. the cap layer is removed under the gate, the gate metal sits directly onto the AlGaN barrier layer, so there is no 2D hole gas under the gate, so the gate only controls the 2DEG channel.

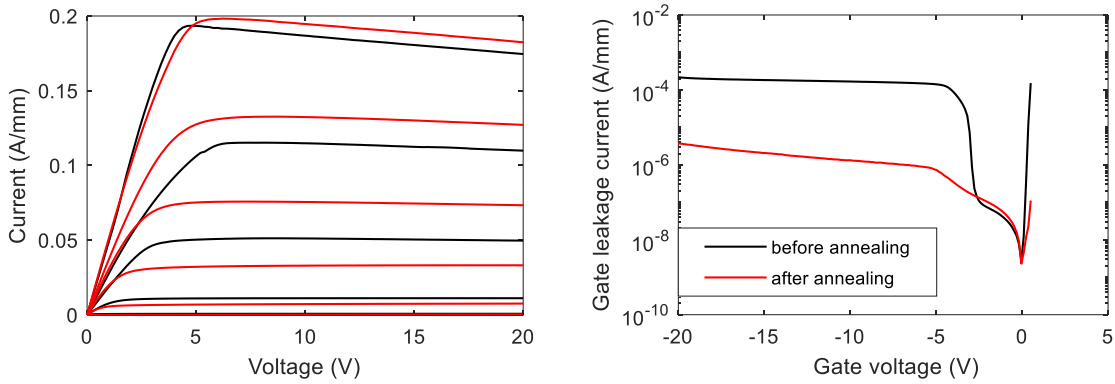


Figure 4.7. Measured drain current with gate voltages from -5 V to 0 V with increments of 1 V (on the left) and gate leakage currents (on theright) for devices before (black lines) and after post gate annealing (blue lines).

Transfer characteristics and transconductance measured at drain voltages V_D from 2 V to 6 V shown in Figure 4.8 illustrate that post gate annealing process improve the transconductance from 25 mS to 40 mS and threshold voltage V_T from -4.7 V to -5.5 V for the devices with 70nm GaN cap layer.

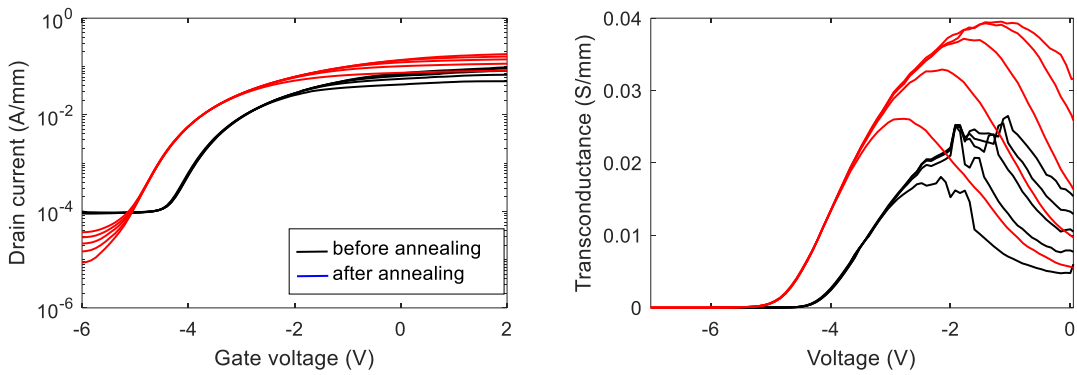


Figure 4.8. Measured transfer characteristics (on the right) and transconductance (on the left) at drain voltage V_D from 2V to 6V.

Devices with 70nm thick GaN cap layer show good DC performance up to 100 V drain voltage as shown in Figure 4.9 on (on the left). The improved fabrication process showed improvement in destructive breakdown voltages from 192 V to over 200 V as illustrated in Figure 4.9 (on the right).

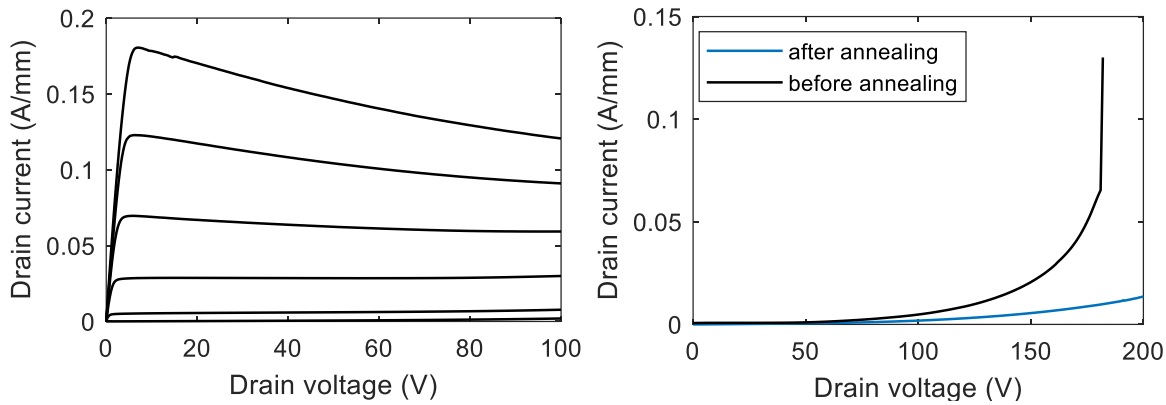


Figure 4.9. DC-IV characteristics with gate voltages from -6 V to 0 V with increments of 1 V (on the left) and off state destructive breakdown measurement with V_G = -6 V(on the right).

Same measurements were performed to the devices with 2nm GaN cap layer and key parameters are summarised in the Table 4.2. Increasing the cap layer to 70nm has lead to decrease in the 2 DEG density from 1 x10^{13} cm^{-2} to 2.7x10^{12} cm^{-2} which is expected. However measured Hall mobility has also decreased for wafer with 70nm thick GaN cap from 1400 cm^2/V·s to 780 cm^2/V·s compared to wafer with 2nm GaN cap, which does not agree with previously reported results where mobility increases for increasing GaN cap thickness up to about 10nm and then saturates. This is believed to be a result of complications reported by manufacturer in the growth process. The decreased mobility is attributed to the higher fabricated Ohmic contact resistance of 1 Ω·mm for the 70nm GaN capped devices compared to 0.5 Ω·mm on standard wafer. Peak current and transconductance is 3 times lower in the thick GAN capped device which is attributed to reduced 2DEG mobility and density. Thicker GaN capped wafer is showing much higher breakdown voltage over 200V and higher threshold voltage of -5.5V compared to -3.7 V on the standard wafer which indicates that surface effects are decreased in this structure.

Table 4.2 Key parameters of the compared devices on wafers with 2 and 70 nm thick GaN cap layers.

	Wafer with 70nm cap	Wafer with 2nm cap
2DEG mobility μ_e	780 cm^2/V·s	1400 cm^2/V·s
2DEG density n_s	2.7x10^{12} cm^{-2}	1 x10^{13} cm^{-2}
Average sheet resistance	2590 Ω/□.	406 Ω/□
Breakdown voltage	over 200 V	80 V
Gate-source leakage current at -20V, I_{Gl}	3.74 µA/mm	1 µA/mm
Threshold voltage, V_T	-5.5 V	-3.7 V
Peak transconductance at 6V, g_m	40 mS/mm	150 mS/mm
Saturated Current, I_{DMAX}	190 mA/mm	570 mA/mm
Ohmic contact resistance, R_C	1 Ω·mm	0.5 Ω·mm

4.3.3. Pulsed IV measurements

In pulsed IV measurements the drain and gate terminals are pulsed and the drain current is measured during the on-period of the pulse instead of applying continuous voltage as its done in DC-IV measurements. First the drain pulse is applied and then the gate pulse is applied to prevent the flow of excessive current. The width of the drain pulse is chosen to be smaller than the width of the gate pulse. The ratio between the pulse width and period of the pulse is known as duty cycle. The pulses are originated from a static quiescent bias point chosen from the IV plane and the set of IV curves are generated by pulsing voltages away from the chosen quiescent bias point. The gate and drain voltages of quiescent bias point determine the type of the electric field state that is present in the HEMT in between the pulses.

Pulsed IV measurements with quiescent bias point with zero electric field between the pulsed has gate and drain voltages of V_G = 0 V and V_D= 0 V with low duty cycle (<1%) and are known as cold state measurements since the device has enough time to recover from temperature transients and self-heating effects are excluded from this measurement. Measurements with quiescent point with drain voltage V_D = 0 V and the gate voltage V_G well into the off state of the transistor are known as gate lag measurements, while measurements with V_G well into off state voltage but with V_D above zero depending on the desired stress level chosen for the test are known as drain lag measurements.

To evaluate DC-RF dispersion in these devices pulsed IV-measurements of drain lag and gate lag were performed and are compared to devices on a standard wafer with 2 nm GaN Cap grown by MOCVD and 10 nm thin ICP SiN passivation layer. Note, industry standard passivation layer is around 100 - 200nm of SiN_x , but 10 nm SiN_x passivation is enough to prevent the surface oxidation, but not thick enough to eliminate the current collapse so this device can be treated as unpassivated device. This way the device with 10nm SiN can be sent and measured in the facilities at the university of Lille and the device doesn't oxidise on the way but it can also be treated as an unpassivated device. Epilayer structures of both compared wafers are shown in Figure 4.5. Figure 4.10 shows DC and pulsed IV measurements for both wafers with following quiescent bias points of the pulsed measurements [V_G (V),V_D (V)] of [0, 0],[-7, 0],[-7, 10],[-7, 20] and [-7, 25]. Pulse width of 500 ns with duty cycle of 1 % and edge time of 100ns was used for pulsed measurements. Generally, when the gate terminal is in strong reverse bias there is induced high electric field at the gate edge on the drain side which leads to electrons tunnelling from the gate to the

surface of the device. These electrons fill ionised surface donors depleting the 2DEG channel. Therefore, when transient gate bias is changed the trapped electrons cannot respond immediately and drain current degradation also known as current collapse occurs. In Figure 4.10 the current collapse with strongly reversed gate voltage and increasing drain voltage is indicated with arrows following saturated current levels in both measurement graphs. Decreased trapping effects leading to reduced current collapse can be seen as a smaller decrease in the current for thick GaN cap device where the saturated current at V_D = 10 V drops from 93 mA to 82 mA and 78 mA at quiescent voltages of [-7 V,0 V] and [-7 V, 10 V] as illustrated in Figure 4.10 a) whereas in the standard device the drop in the current is from 210 mA down to 51 mA and 20 mA for the same quiescent bias points as illustrated in Figure 4.10 b). Moreover, at quiescent point of [-7 V, 25 V] the drain current of thick GaN cap structure drops down to 46 mA but for a standard device the device drain current collapses completely, which is typical for a device with very thin passivation layer or no passivation. Drain lag measurements show the current collapse primarily due to the electrons getting trapped in the bulk epilayers however at high V_D self-heating of the device also contributes to the current degradation. Gate lag measurements, on the other hand, are known to degrade current due to the electrons trapped in both surface and bulk epilayers [124]. Even though the total current in the thick GaN capped device is 3 times smaller than in standard device when the device is measured with quiescent points with strongly reversed gate voltage of -7V with drain voltage from 0 to 25V the total drain currents is higher for thick GaN capped. For the presented new structure the surface is further away from the surface therefore electron leakage through the surface is minimised even without the passivation layer. In Figure 4.10 it can also be seen that both of these devices suffer from self-heating effects and/or trapping effects as there is 20% and 18% decrease in the saturated drain current from the cold point measurement to the DC-IV measurement for thick GaN capped device and standard device respectively.

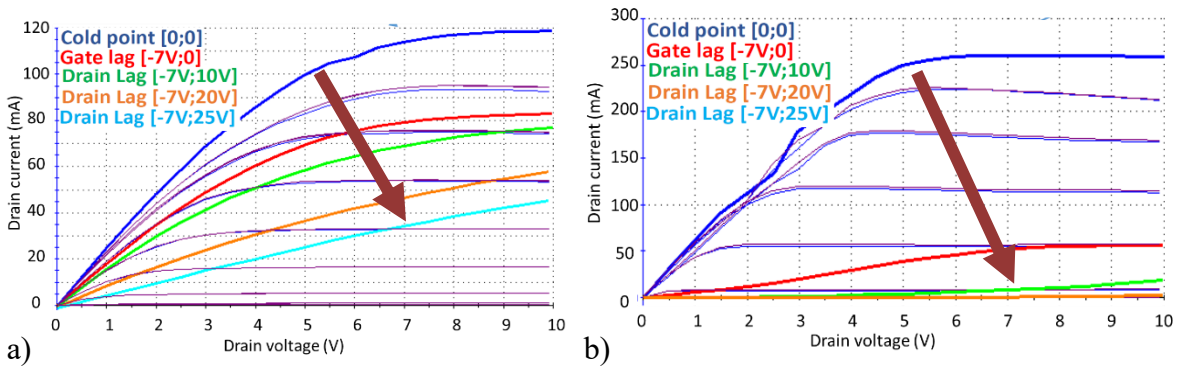


Figure 4.10. Pulsed IV measurements with bias conditions [V_G (V), V_D (V)] of [0, 0],[-7, 0],[-7, 10],[-7, 20] and [-7, 25] with DC-IV characteristics for devices on a) wafer with 70nm thick GaN cap and b) standard wafer with 2 nm GaN cap and 10 nm SiN passivation. Here current

collapse in indicated with the arrows following the current saturation levels at different quiescent bias points.

4.4. Conclusion

The introduction of a thick undoped GaN cap layer described in this chapter significantly reduces the current collapse in the device and increases the off-state breakdown voltage to over 200 V for 2×200 μm wide devices. Adding a gate annealing process after gate metallisation lead to reduce the gate leakage currents by half. Even though the total current density is smaller for the proposed device structure than compared to conventional devices (with thin (2nm) GaN cap layer) fabricated thick GaN cap devices show good DC-IV performance up to 100 V indicating that they could be operated at much higher drain voltages to achieve the same output power. These results demonstrate a great potential of this novel undoped epitaxial approach for passivation-free GaN-based HEMTs for high-power applications.

5. Comparative study of cold-wall and hot-wall MOCVD GaN HEMTs

5.1. Introduction

GaN HEMTs are a high-power density technology, therefore the heat generated due to dissipated power in the device must be extracted efficiently. Without efficient heat extraction techniques, key device performance parameters such as saturated drain currents, transconductance, gain and power output are severely degraded due to the increased junction temperature. Thermal management, i.e. heat extraction or minimisation of heat generation in the device, is one of the main challenges for current GaN HEMT technology. This project is focused on investigating novel methods for thermal management of GaN devices. In this chapter, a review of the importance of the choice of the substrate material will be given, then the role and impact of the nucleation layers between the substrate and GaN will be discussed, and finally results of an experimental comparative study of two commercially sourced GaN on SiC wafers with different nucleation layer thicknesses and growth methods will be presented.

5.2. SiC Substrate for the thermal management of GaN HEMTs

It has been demonstrated that device heating is mainly determined by the DC biasing point so that neither changes in temperature nor its distribution is dependent on the RF signal [125]. Saturation current, electron mobility, bandgap, breakdown and pinch-off voltages, transconductance, noise performance, device lifetime and output power - all of these parameters are directly affected by the channel temperature [126]. Furthermore, for high power operation, high voltages are required, and as output power levels increase the heat waste also increases. Also when these transistors are used in power amplifiers (PA), transistor heating also causes memory effects which then degrade the linearity of these PAs [127]. For these reasons, minimisation of heat generation within the device and maximisation of heat removal from GaN devices is important.

High thermal conductivity substrates such as diamond or silicon carbide (SiC) can be used to dissipate some of the heat. Even though nanocrystalline diamond (NCD) has the highest thermal conductivity k ~ 2000 W/mK [53],[54] lattice mismatch of 11.8 % between GaN and diamond makes it extremely difficult to integrate diamond in the GaN devices. This

would require thicker or more complicated transition layers to mitigate the stress between the materials. These transition layers then limit the heat transfer into the diamond acting as a thermal resistor. It is also more challenging to grow good quality GaN HEMT epilayers on top of the diamond due to the difference in the thermal coefficient of expansion α (α_{GaN}= $5.59\text{x}10^{-6}$ K^{-1} and $\alpha_{diamond}$ =$1\text{x}10^{-6}K^{-1}$) [128]. Diamond does not expand as much as GaN and once it is removed from the growth chamber GaN might crack. Even though GaN on diamond devices have been shown to exhibit three times larger power handling capability than those on SiC [129], the methods to realise GaN on diamond devices are complicated and expensive [59]. Recent developments have shown that GaN on diamond wafers can be made by transferring GaN epilayers to CVD diamond for up to 3 and 4 inch wafer sizes [130], [131]. Moreover, the feasibility of directly growing GaN on diamond was demonstrated, but this technology has not yet matured to deliver the required material quality for GaN HEMT device fabrication [132],[128]. However, devices biased at 28 V under class AB operation delivering power of 5.5 W/mm with power added efficiency of 50.5% at 10 GHz have been demonstrated on the bonded GaN on diamond wafers [130], but any backside processing remains a challenge for this technology.

SiC is one of the most used substrates for GaN device fabrication with thermal conductivity of 400 W/mK at room temperature, but at 200 °C this decreases to approximately 120 W/mK [133]. There are many reasons for using SiC as a substrate for GaN devices such as : it offers good electrical isolation (>10^9 Ω·cm), low lattice mismatch to GaN of only 3.1% which can be mitigated with very thin nucleation layers resulting in low defect densities and the ability to grow good quality GaN epilayers on SiC. There are also developed technologies for backside processing of SiC devices such as wafer thinning (by grinding) and backside via fabrication techniques to integrate these devices into monolithic microwave integrated circuits (MMICs)[134], [135].

5.3. Thermal boundary resistance of the AlN nucleation layer

5.3.1. Heat flow within the GaN HEMT epistructure

Even high thermal conductivity substrates such as diamond and SiC substrates require transition layers in order to grow GaN on these substrates, the thermal boundary resistance (TBR) associated with this nucleation layer is intrinsic to the material and therefore cannot be impacted/reduced with common thermal management approaches such as liquid cooling

[60][61], thermally efficient packaging [58],[59], distributed gate designs [63],[64] or the use of heatsinks [62]. Examples of these approaches are illustrated in Figure 5.1.

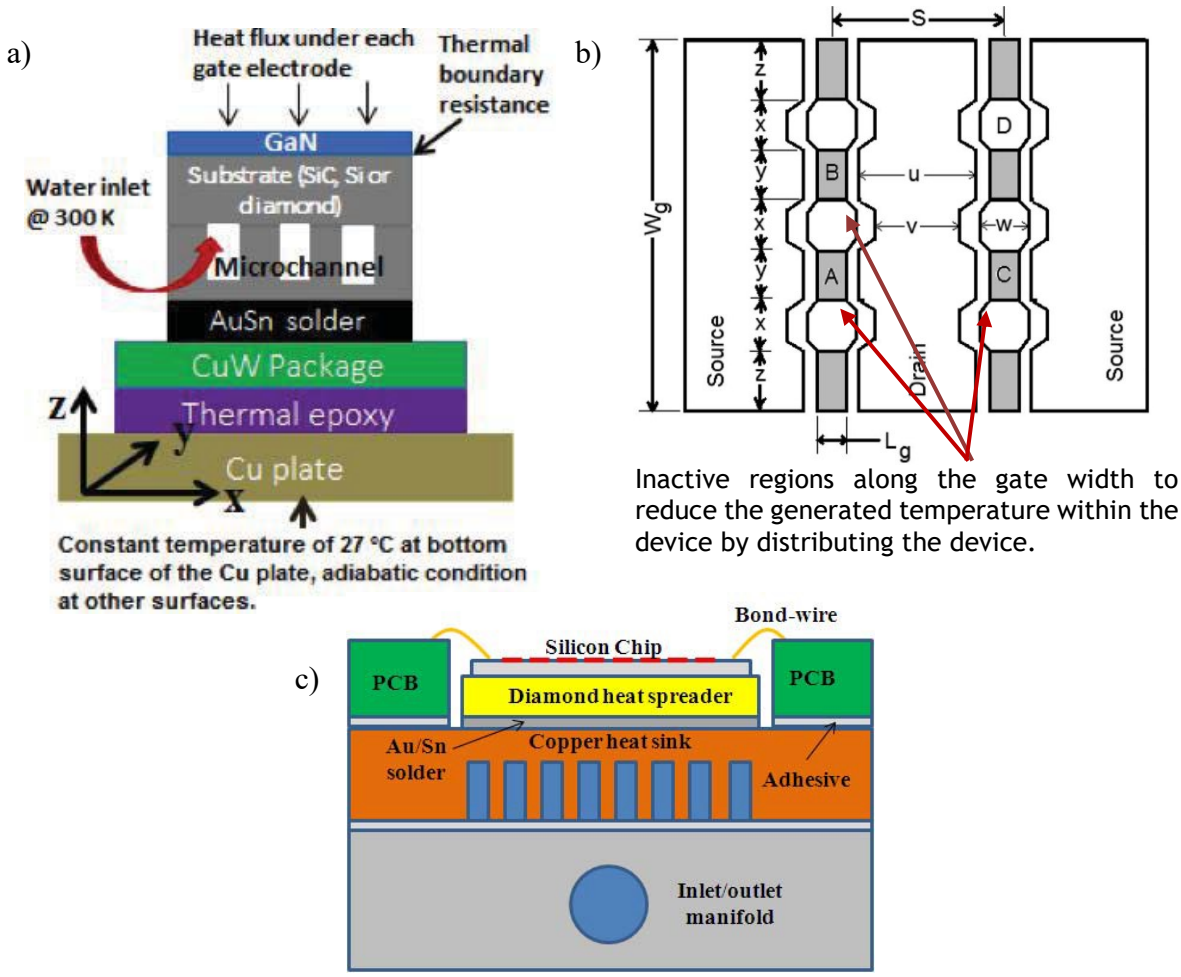


Figure 5.1. Schematic illustrations of thermal management approaches using a) liquid cooling, cold plate with thermally efficient packaging [136] **b) distributed gate design**[63] **and c) thermally efficient packaging with copper and diamond heat sinks** [137].

The effects of TBR associated with the nucleation layer should be considered separately. Figure 5.2 illustrates the current flow through a typical AlGaN/GaN HEMT device (maroon arrows from drain to source). Device heating occurs along this path, with the highest temperature occurring on the drain side of the gate since the electric field is highest at this point. The upper two layers (AlGaN/GaN) are the active layers that create the channel due to the polarization effects. When the device is in operation, electrons move through the channel, gaining high kinetic energy thus generating heat in the process. This heat distributes through diffusion to the colder areas over the whole chip. However, since the GaN HEMT consists of several layers of different materials, with each material having a different thermal conductivity as indicated in Figure 5.2, the thermal flow is also limited accordingly. At each interface, such as the GaN/AlN interface, the associated thermal resistance restricts the heat flow. Ideally, we would want to put high thermal conductivity substrate straight under the

channel layers, but as most popular substrates such as sapphire, silicon and SiC have some lattice mismatch as well as a CTE (coefficient of thermal expansion) mismatch and so there is a need for an interlayer (conventionally called nucleation layer) to reduce the mechanical stress that would appear at the interface which would otherwise limit the device performance, reliability and lifespan. In the case of SiC, the nucleation layer is usually aluminium nitride (AlN), which is also necessary to stimulate GaN buffer growth. Unlike bulk AlN which exhibits thermal conductivity of 237 W/mK [138], thin AlN has structural defects like voids and dislocations at the GaN/AlN/SiC interface [50] leading to a low thermal conductivity of 1.5-23 W/mK. Having a layer with low thermal conductivity in the epistructure slows down the heat flow into the substrate and this layer acts as a thermal boundary resistance (TBR) [19]. TBR is used to describe heat transport across an interface and it is defined as the inverse of thermal boundary conductivity given by this equation[139]

$$R_{Bd} = \left[\frac{\dot{Q}}{A \cdot \Delta T}\right]^{-1} \tag{5.1}$$

where $\dot{Q}$ is the heat flow across an interface, A is the area and ΔT is the temperature difference between the two side of the interface. Other researchers have found that this TBR can cause up to 50% increase in the channel temperature [56], [57], [140]. If the TBR is reduced by 25% it results in 10% decrease in the channel temperature, hence improving the device performance [141].

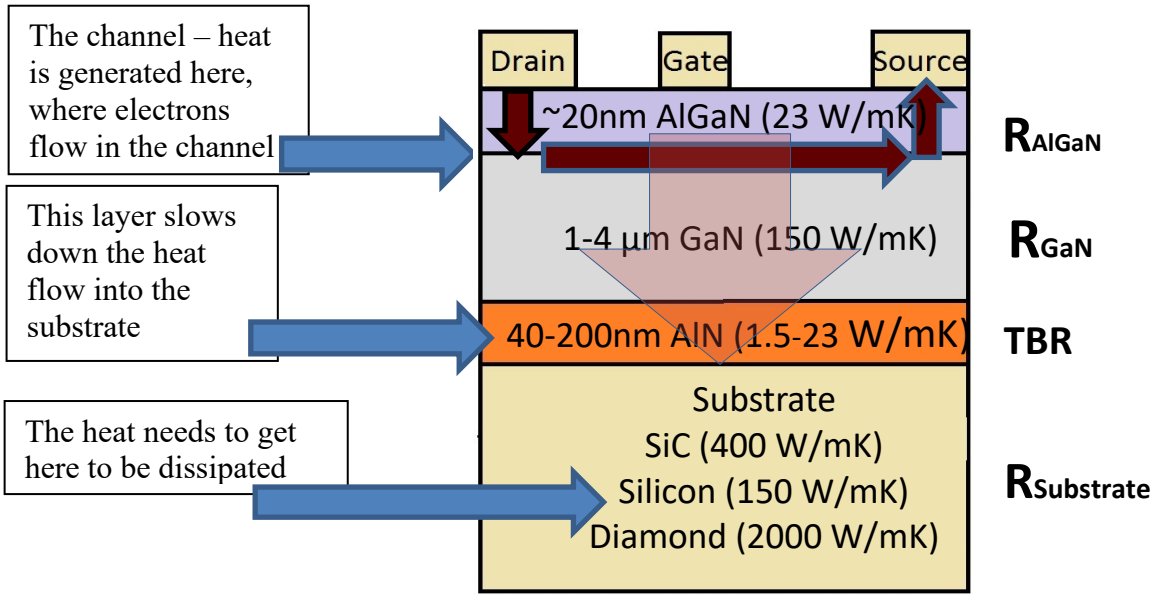


Figure 5.2 Illustration of the standard AlGaN/GaN HEMT with heat flow indicated as a big arrow from the channel to the substrate. The thermal conductivities of the typical layers and substrates are also provided.

5.3.2. MOCVD growth methods

Improving the nucleation layer growth conditions can lead to better quality GaN epitaxial layers. Higher quality epitaxial layers would lead to better electrical and thermal properties [41]. During conventional cold-wall MOCVD growth process only the wafer carrier, known as a susceptor, is heated up to the necessary growth temperature, so no gas reaction takes place before reaching the hot wafer surface. As a consequence, there are large temperature gradients across the growth chamber primarily in the vertical direction but also in the horizontal direction. These temperature gradients influence the uniformity of the growth rate, doping and composition. However, in a hot-wall MOCVD growth process the whole chamber is heated up leading to better uniformity of the growth process due to the low temperature gradients in the chamber. The gasses (H_2/N_2) and precursors (TMAl/TMGa+NH_3) are mixed before entering the hot zone. The processing gases are forced through a hollow shaped, RF-induction heated graphite susceptor surrounded by insulator as shown in the schematic view of the hot-wall MOCVD setup is shown in Figure 5.3. This setup has been shown to have by an order of magnitude smaller vertical temperature gradient in the hot-wall MOCVD SiC growth chamber than conventional cold-wall MOCVD chamber [142].

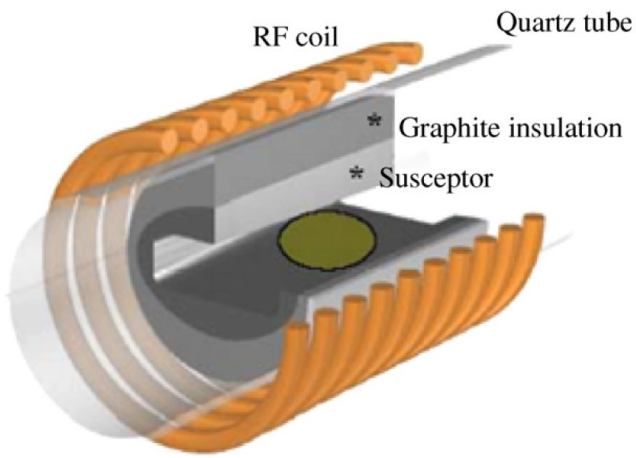


Figure 5.3 Schematic view of the hot-wall MOCVD growth chamber setup, showing the substrate in the hot zone. All precursors TMAl/TMGa+NH_3) and carrier gases (H_2/N_2) are mixed before entering the growth chamber [143].

The use of hot-wall MOCVD technique was first proposed by G. J. Riedel *et al* and resulted in improved epitaxial quality and hence reduced TBR [56]. Conventionally grown AlN nucleation layers exhibit grain like morphology and so the interface between AlN and GaN crystallites is not smooth, an effect that is also known as a grain boundary. However, using hot-wall MOCVD leads to a grain boundary free AlN nucleation layer with low TBR which

also allows for high quality GaN to be grown on top. The difference in the structural integrity of the epilayers can be clearly seen in a cross sectional TEM images showed inFigure 5.4. Moreover, the heated chamber also reduces wafer bow improving the growth quality and therefore benefiting the device performance [144], [145].

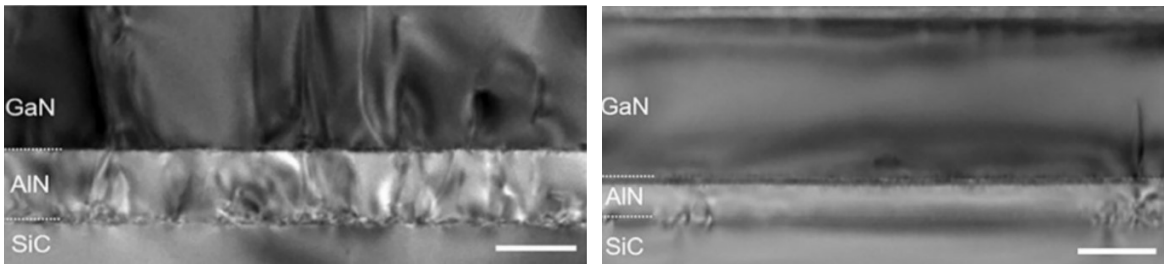


Figure 5.4 Cross-sectional TEM at the GaN/AlN/SiC interface using a) conventional AlN nucleation MOCVD growth and b) hot wall MOCVD growth [50]**.**

Using calculations from diffuse mismatch model (DMM) the TBR across the GaN–substrate interface of AlGaN/GaN HEMTs has been reported to be $\sim 1 \times 10^{-9}$ $m^2 \cdot K/W$ at room temperature [139]. However DMM only considers true interfacial phonon scattering and other forms of disorder-induced phonon scattering near to the interface are neglected and therefore it is known to underestimate experimentally measured TBR values [146]. Reported experimental values of the TBR in the GaN/substrate interface are by 1-2 orders of magnitude higher than predicted by DMM [57][56]. Experimental values of TBR for GaN/SiC devices grown by standard cold-wall MOCVD growth methods from commercial suppliers are 3.3 - 6×10^{-8} $m^2 \cdot K/W$ using Raman spectroscopy [57], 1.2×10^{-7} $m^2 \cdot K/W$ using a 2-D laser interferometry. However published data for measured TBR on a wafer grown by commercial supplier SweGaN AB who uses hot-wall MOCVD growth show lower TBR values between 0.8 - 1.8×10^{-8} $m^2 \cdot K/W$, demonstrating that improved growth conditions lead to lower TBR [141].

Wafers grown with hot wall MOCVD can then be used in device fabrication to quantify the improvements in device electrical performance.

5.4. Experimental results

5.4.1 Hot-wall and cold-wall MOCVD GaN HEMTs

A comparative study was performed on two GaN HEMT epitaxial structures on high thermal conductivity 4H-SiC wafers grown by metal organic chemical vapour deposition (MOCVD) growth technique sourced from two different commercial wafer suppliers, supplier A who employ the conventional cold wall MOCVD (wafer 1), and SweGaN AB who use hot wall

MOCVD (wafer 2). The main difference between the wafers is the AlN layer growth conditions, i.e. using hot and cold wall MOCVD growth methods, which lead to different nucleation layer quality and required thicknesses. Wafer 1 had a 2 nm GaN cap layer, 20 nm thick AlGaN barrier with 25% Al content and 2 µm GaN buffer or channel layer, while wafer 2 had a 1 nm GaN cap, a thinner 16 nm AlGaN barrier with 31% Al content, a 1 nm AlN spacer layer, and also a thinner 1.6 μm GaN channel layer. The epitaxial layer structures of both wafers are shown in Figure 5.5. The manufacturer of wafer 2 claimed to have extremely low thermal boundary resistance due to the optimised wafer growth process using hot-wall MOCVD growth technique, that lead to the use of only only 35 nm AlN thin nucleation layer while wafer 1 was grown using conventional growth process and has 200 nm thick AlN nucleation layer. Table 5. 1 shows average sheet resistivity, 2DEG mobility and density provided by the manufacturers. Wafer 2 exhibits lower average sheet resistance and higher 2DEG mobility and density due to the higher Al concentration in the AlGaN barrier layer and due to the AlN spacer layer which increase the polarization effects at the quantum well.

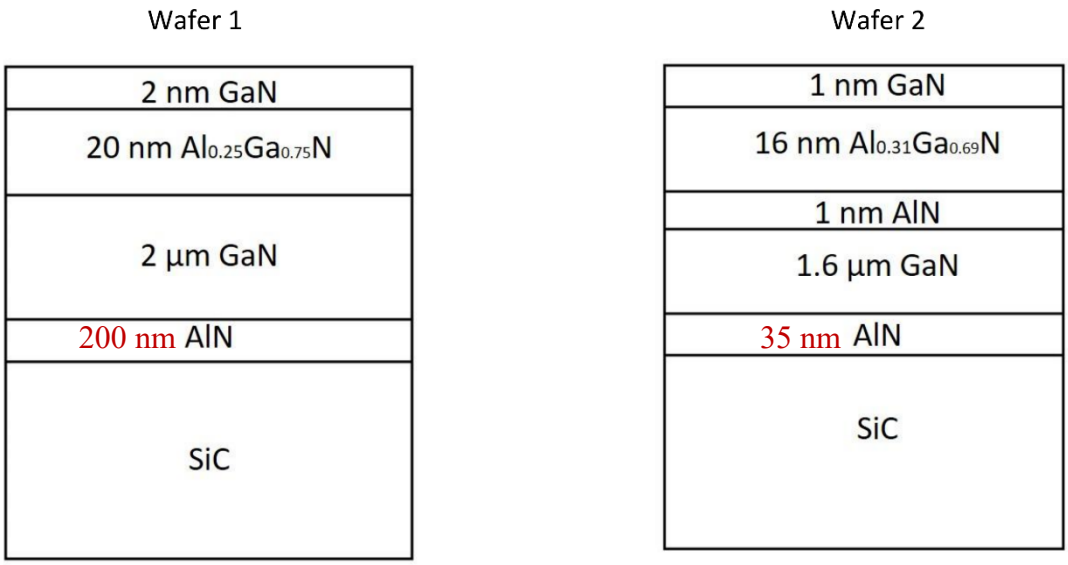


Figure 5.5 Epitaxial wafer structure of the compared wafers.

Table 5. 1 2DEG mobility, density and average sheet resistances for both wafers measured by manufacturers.

	Wafer 1	Wafer 2
2DEG mobility μ_e	1400 cm^2/Vs	1900 cm^2/Vs
2DEG density n_s	1 x10^{13} cm^{-2}	1.2 x10^{13} cm^{-2}
Average sheet resistance	406 Ω/□	270 Ω/□

Both wafers were also tested at the University of Glasgow using capacitance-voltage (CV) measurements on Schottky diodes fabricated in the James Watt Nanofabrication Centre (JWNC). An optical image of the fabricated diode is showed in Figure 5.6. The Schottky

contact diameter had a of 100 µm and a gap of 5 µm between Schottky contact and surrounding Ohmic contact. The Ohmic and Schottky contact fabrication process for the diodes was the same as used for the transistors and can be found in Appendix A. These diodes were then characterised using CV measurements at 1 kHz, 200 kHz, 500 kHz and 1 MHz. The results are showed in Figure 5.7 a) and b) for wafers 1 and 2, respectively. Here, one can also see that wafer 1 has a higher threshold voltage of -3.6 V whereas wafer 2 has a threshold voltage of -4 V which can be attributed to higher 2DEG density (due to the higher Al content in the barrier) and better electron confinement in the channel (due to the presence of the AlN spacer layer).

Figure 5.6 Optical microscope image of a fabricated diode structure with centre Schottky contact diameter of 100 µm and spacing between surrounding Ohmic contact and Schottky contact of 5 µm.

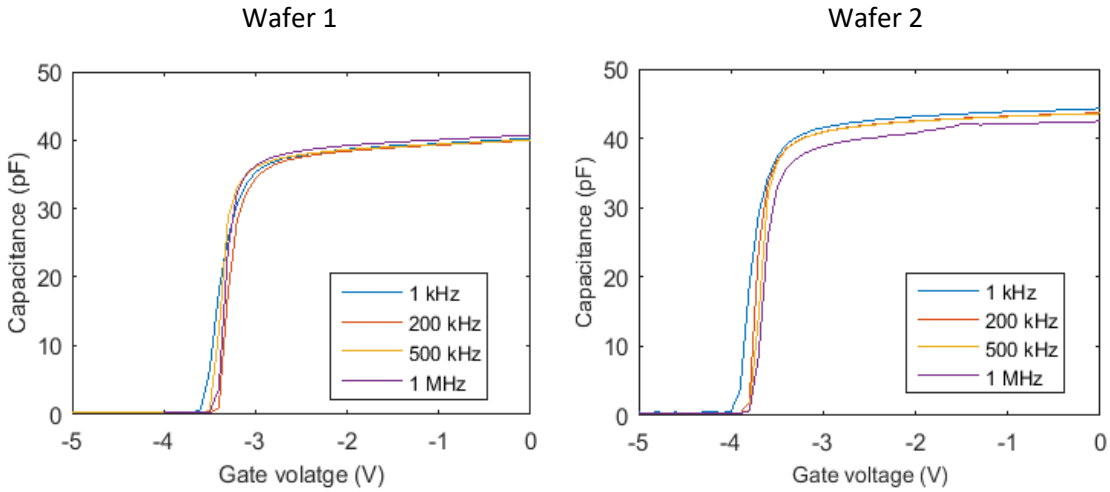


Figure 5.7 Capacitance -voltage (CV) measurements of the fabricated diodes on wafer 1 and wafer 2.

Using equation B.2. the apparent carrier concentration extracted from the C-V measurements at 1 MHz for both samples are showed in Figure 5.8 (more details on the CVmeasurments can be found in Appendix B). As the barrier thickness is smaller and AlGaN concentration higher in wafer 2, the extracted peak apparent carrier concentration is $3.75 \cdot 10^{20}$ cm^{-3} compared to $1.32 \cdot 10^{20}$ cm^{-3} in wafer 1. The peak of carriers appears at 20 nm and 16 nm depth from the Schottky contact on wafer 1 and 2 respectively. In both cases the peak is 2 nm above the GaN/AlGaN and GaN/AlN interfaces. However, it must be noted, that this is just an approximation of the carrier concentration due to the depletion assumption.

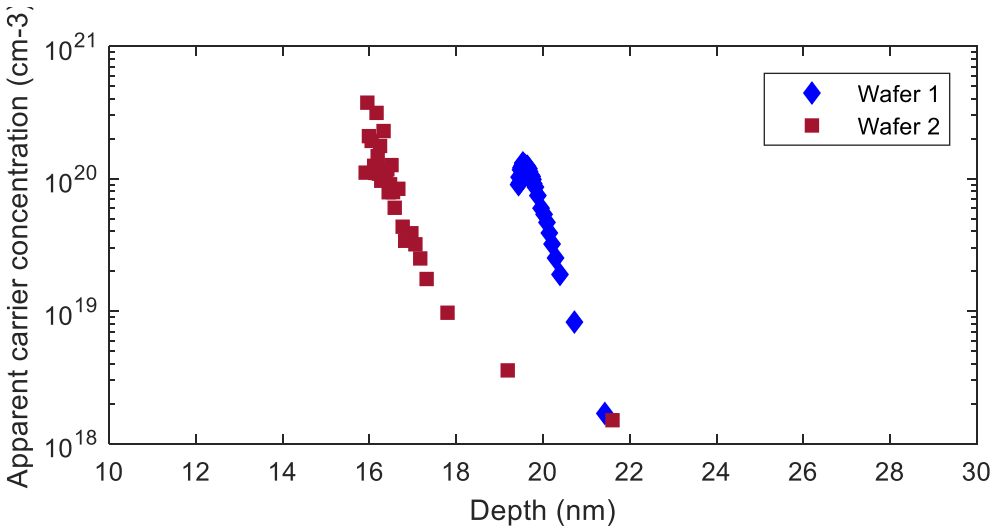


Figure 5.8 Apparent carrier concentration versus estimated depletion depth from the CV measurements for wafer 1 and wafer 2.

From the CV measurements one can also estimate electron sheet concertation σ_{2DEG} using the following expression [147]:

$$\sigma_{2DEG} = \frac{\int_{V_T}^{V_{bi}} C dV}{qA} \tag{5.2}$$

Using this extraction method, the 2DEG sheet concentration was estimated to be 1 x10^{13} and 1.1 x10^{13} cm^{-2} for wafer 1 and 2 respectively, which agrees with the manufacturer's measurements.

5.4.2 Device results

Two finger devices with 2 µm gate length and gate widths of 50 and 200 µm were fabricated simultaneously on each wafer using photolithography to examine the effects of thermal boundary resistance. A micrograph of the fabricated 50 µm and 200 µm wide device are shown in Figure 5.9 and Figure 4.6 respectively. Ohmic contact resistances were extracted from transmission line method (TLM) measurements to be 0.58 Ω·mm and 0.55 Ω·mm for wafers 1 and 2, respectively. Similarly, sheet resistances were obtained to be 400 Ω/sq and 300 Ω/sq for wafers 1 and 2, respectively.

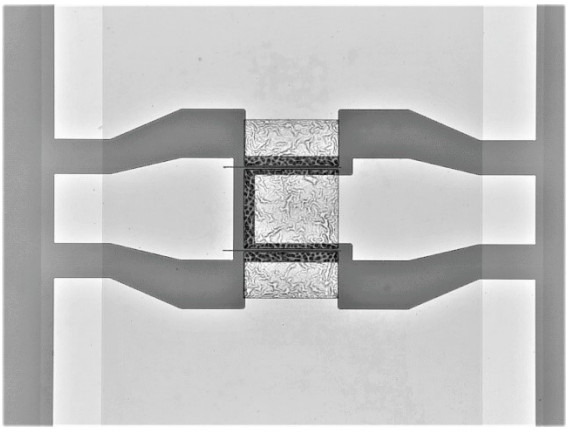


Figure 5.9 Micrograph of a fabricated 50 µm wide device.

DC-IV measurements were done on a 200 µm wide device on wafer 1 using only single finger and measuring both fingers at the same time. It can be seen in Figure 5.10. that the saturated output currents have decreased from 0.35 A/mm to 0.31 A/mm which corresponds to dissipated DC powers levels of 7.2 W/mm and 6.4 W at 20 V drain voltage for 1 and 2 finger devices respectively. This can be attributed to thermal crosstalk between the device fingers. With decreasing gate voltage device channel gets slowly depleted leading to less current flowing in the channel and the difference in the saturated current levels for 1 and 2 finger devices also reduces. As both of the compared IV characteristics are done on the same device trapping levels are assumed to be the same, so reduction in the current is assumed to be associated mainly with self-heating here.

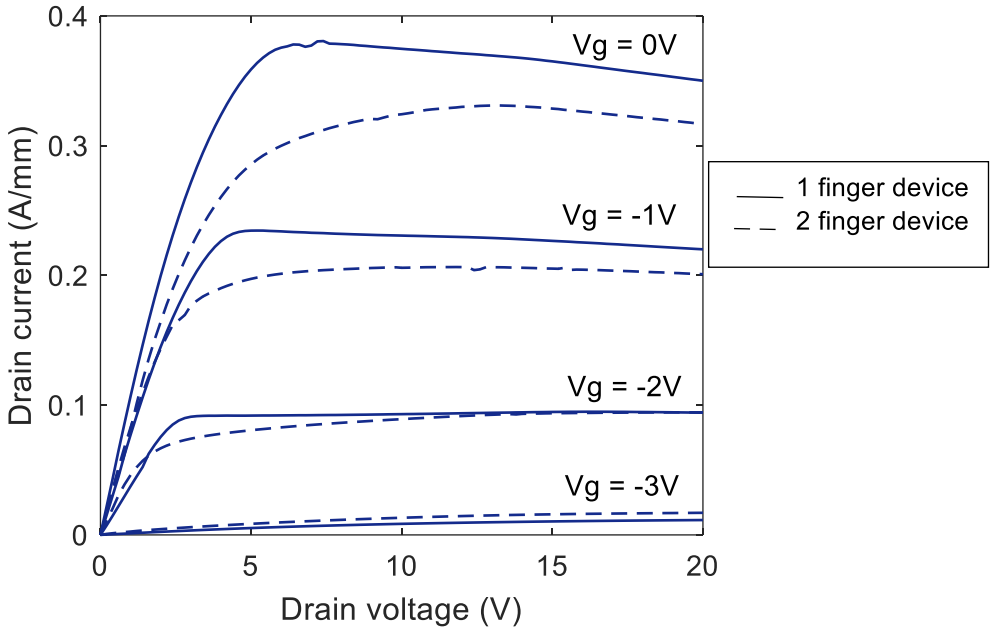


Figure 5.10 DC-IV characteristics of 200 µm wide device with 1 device finger and 2 device fingers fabricated on wafer 1.

The same trend can be seen in differently sized devices, i.e. comparing devices with different gate widths. Wider devices generate more heat than smaller devices due to difference in total active area. This can be seen in DC-IV characteristics for 50 and 200 µm wide devices fabricated on each wafer illustrated in Figure 5.11. As one can see, there is a decrease in drain current density for larger devices on both wafers and the compared devices in each graph are fabricated on the same wafer so the trapping effects that can cause current degradation can be assumed to be the same, therefore the drop in the current density is attributed to the self-heating. This is what one would expect since the substrate is relatively far away from the channel i.e. hotspot (more than 2 µm), so it is impossible to extract all the heat via the substrate. However, the decrease in the dissipated DC power is 12% between differently sized devices on wafer 2, compared to a 20% decrease on wafer 1 at 20 V drain voltage, which indicates that the heat dissipation is better on wafer 2.

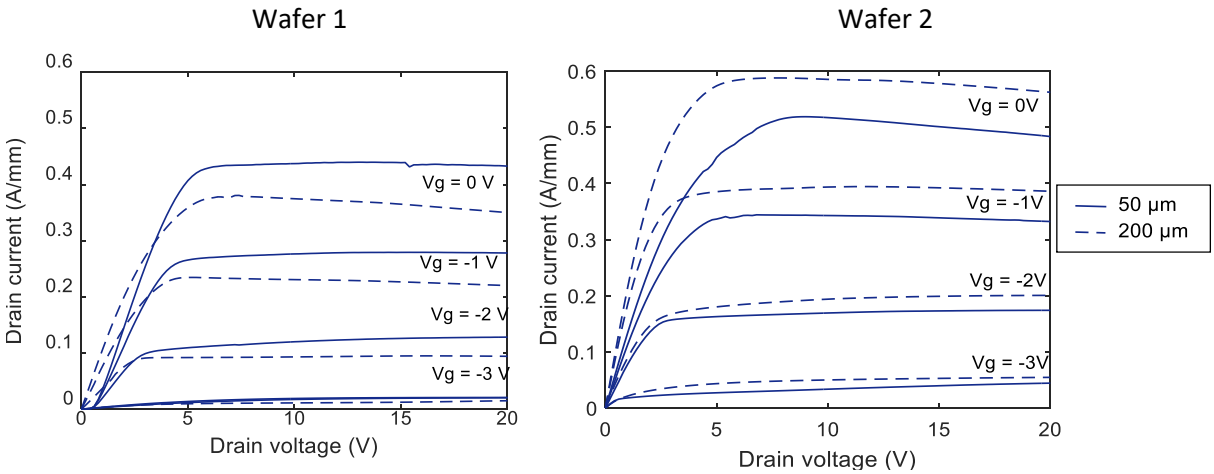


Figure 5.11 I_{DS}-V_{DS} characteristics for 50 and 200 µm wide devices on wafer 1 and 2.

To better understand the device performance, device IV characteristics for devices with 50 µm width on both wafers are plotted in the same graph, see Figure 5.12. Devices on wafers 1 and 2 exhibit maximum drain currents I_{DSS} of 530 mA/mm and 600 mA/mm, respectively, so there is by 13% higher drain current for wafer 2 as expected. To investigate device self-heating, the reduction in the saturated drain current with bias between knee voltage at V_{DS} = 5 V and a voltage well into saturation region of V_{DS} = 30 V was observed. The measurements show that devices on wafer 1 suffer a larger reduction in I_{DSS} and thus dissipated DC power levels, i.e. the effect of self-heating is larger, of 19% compared to 15% for wafer 2, even though devices on wafer 2 exhibit 13% higher I_{DSS} compared to devices on wafer 1. Here it is attributed to the reduced TBR associated with the improved AlN nucleation layer growth method using hot-wall MOCVD. However, it must be noted that these devices are on different wafers and it is known that trapping within devices leads to decrease in the saturated current levels, so different trapping levels among these wafers could contribute to the current

collapse. Both devices have been passivated at the same time and therfore have experienced the same processing conditions so it is assumed that the surface effects should be minimised or made similar on both wafers. However, it is possible that devices on wafer 2 experience less degradation in the saturated current partially due to the improved material quality that could lead to less impurities/defects in the materials and therefore less trapping in the device epilayers, especially in the buffer region. The device on-resistances measured in the linear region of the I-V characteristics for wafers 1 and 2 were 8.6 Ω·mm and 5.9 Ω·mm, respectively, with wafer 2 showing lower resistance as expected. It is known that buffer thickness does affect the thermal dissipation [148] as the distance between the channel and the high thermal conductivity substrate is different but it is assumed here that the difference in buffer thicknesses is not the main factor affecting thermal dissipation.

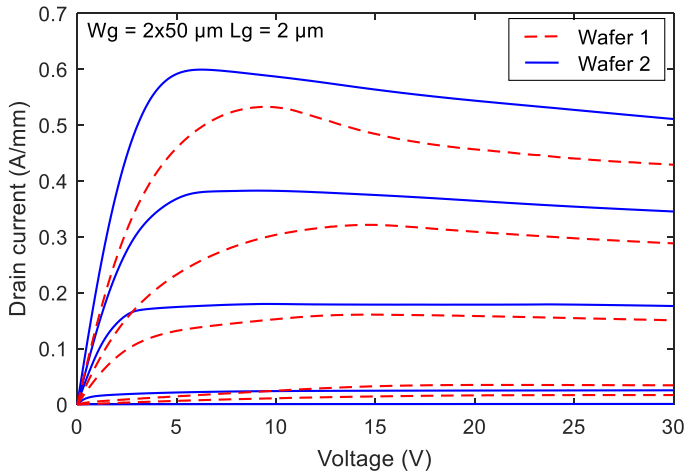


Figure 5.12 I_{DS}-V_{DS} characteristics for 50 µm wide devices on wafer 1 and 2.

The transconductance of the two 50 µm wide devices on both wafers is shown inFigure 5.13. The devices exhibit maximum transconductances of 150 mS/mm and 210 mS/mm on wafers 1 and 2, respectively. It can also be seen in Figure 5.13 that wafer 2 has one order of magnitude better device on-off ratio compared to wafer 1 which leads to higher transconductance. We attribute this to the lower drain leakage current due to the improved wafer growth.

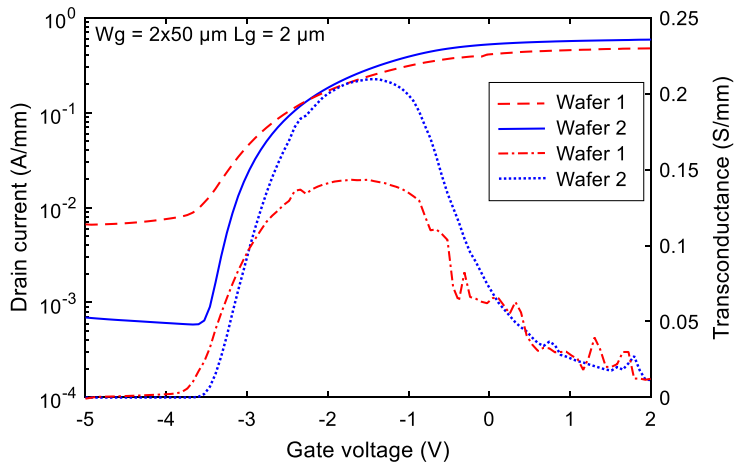


Figure 5.13 Transfer characteristics and transconductance of 2×50 µm wide devices on wafers 1 and 2 at V_{DS} = 4V.

The gate leakage currents of the two devices are shown in Figure 5.14. Devices on wafers 1 and 2 exhibit gate leakage currents of 140 nA/mm and 600 µA/mm at a gate voltage of -20 V, respectively. The higher gate leakage current for devices on wafer 2 is attributed to the thinner barrier layer and higher current density in the channel. Other than gate leakage currents, all other measured device parameters are better for wafer 2, so it is concluded that the hot-wall MOCVD growth process is beneficial for improving the device performance. Note that gate leakage of devices on wafer 2 could be reduced also by improving the mesa isolation process and/or adding a gate dielectric.

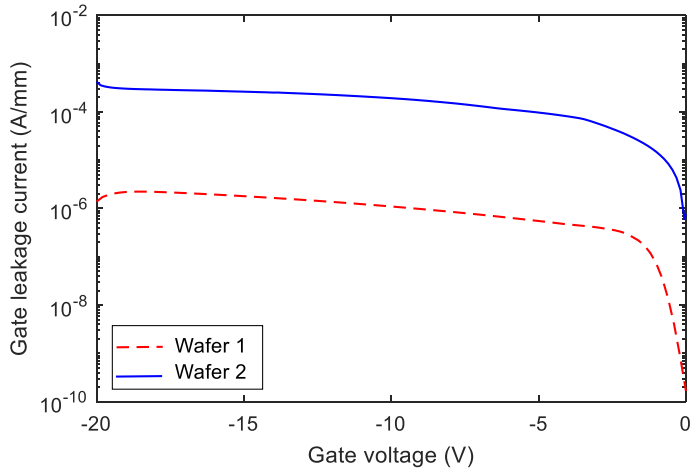


Figure 5.14 Gate leakage currents of 2×50 µm wide devices on wafers 1 and 2.

5.4.3 Large gate periphery devices

Large area devices with smaller source to drain distance are more prone to self-heating and this severely affects DC characteristics. 10 x100 µm wide device with gate-length of 0.5 µm were fabricated on both wafers. To achieve higher accuracy both the Schottky gate and Ohmic contacts were fabricated using e-beam lithography and the rest of the fabrication

steps were done using photolithography. The drain to source separation was 3.5 µm and source contacts were connected by metal bridges with polyimide (PI2454) for support. Both devices had the same geometry as shown in Figure 5.15.

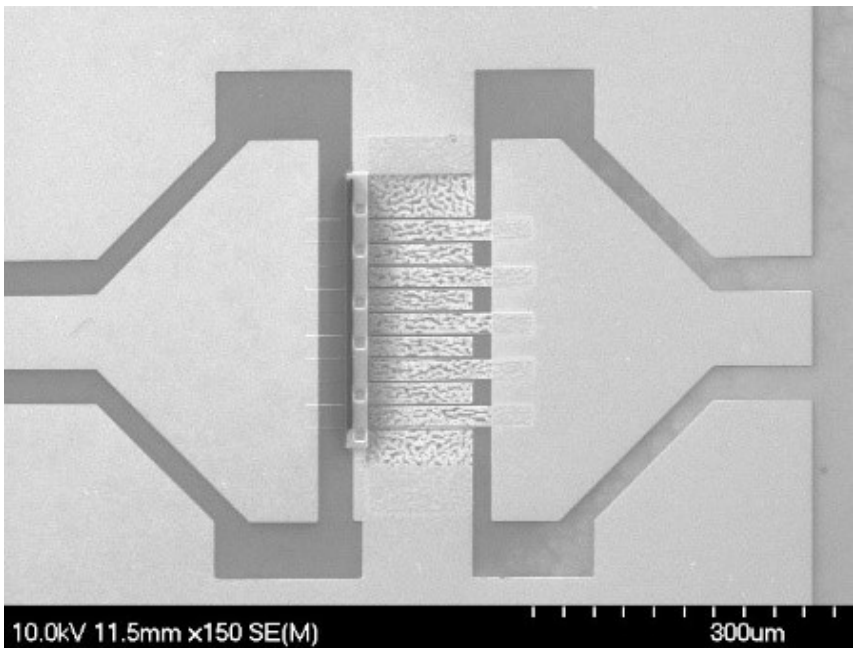


Figure 5.15 SEM image of fabricated 10 finger devices.

As discussed above wafer 2 has higher Al concentration and AlN spacer layer which leads to higher 2DEG mobility/density and lower sheet resistance resulting in higher saturated drain currents. However, the contact resistance (R_C) of wafer 1 was determined to be 0.48 Ω·mm but on wafer 2 R_C = 0.68 Ω·mm. Here the contact resistance was higher compared with in the 2 finger device (0.55 Ω·mm reported in section 6.4.2) due to variations between fabrication runs. This higher contact resistance led to lower saturated currents and higher on-resistance for device on wafer 2 than expected from previous results. DC- IV characteristics of devices on both samples are shown in Figure 5.16. Here one can see that for V_{GS} = 0 V both devices have the same saturation point but the decrease in the current with increasing drain voltage is much smaller on wafer 2, showing dissipated DC power levels of 10.4 W/mm and 9 W/mm at 20 V drain voltage for wafer 2 and 1 respectively. Here, similarly as above it is assumed that the difference in the dissipated current levels mainly comes from better head distribution excluding the possibility of different trapping levels and is attributed to the improved TBR.

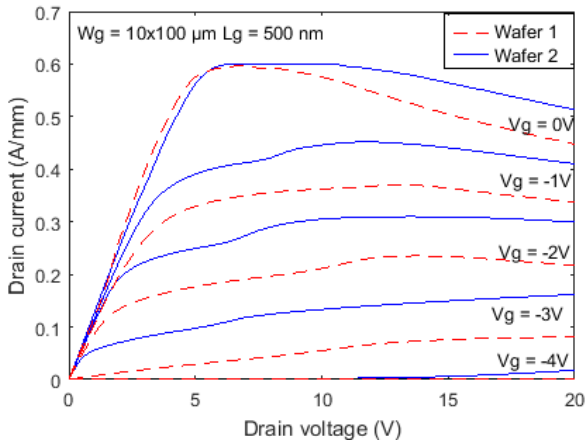


Figure 5.16 I_{DS}-V_{DS} characteristics for 10x100 µm wide devices on wafer 1 and 2.

Similar to the 2 finger devices, the threshold voltages were found to be -3.6 V and -4.1 V for wafers 1 and 2 respectively (as can be seen in transconductance characteristics inFigure 5.17). The maximum transconductance for wafer 1 was 177 mS/mm while for wafer 2 it was 183 mS/mm. Wafer 2 exhibits relatively lower transconductance because of the lower quality Ohmic contacts, but is still higher than wafer 1 due to improved heat dissipation within the epi-structure.

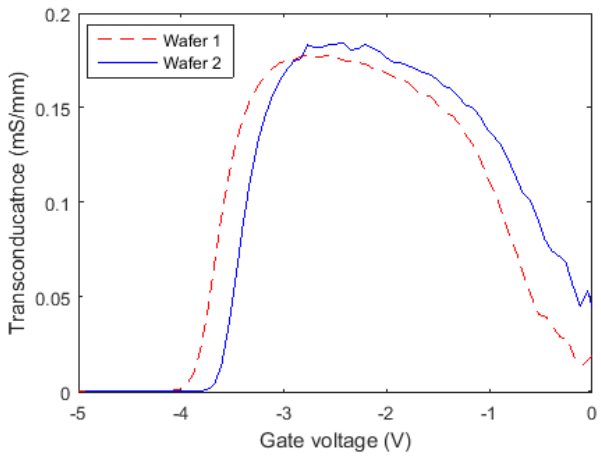


Figure 5.17 Transconductance for 10 x100 µm wide devices on wafer 1 and 2 at V_{DS} = 4 V.

5.5. Summary

As thermal boundary resistance acts as a thermal resistor, having thinner higher quality nucleation layer helps improve the device thermal performance. The AlN nucleation layer creates a thermal boundary resistance (TBR) which limits the heat transfer into the high thermal conductivity SiC substrate. This leads to higher device self-heating and therefore degraded device performance. Therefore, the lowering of TBR as attempted in wafer 2 is beneficial to improved device performance. We have attributed difference in AlN nucleation layer quality as the main factor for differences in the performance of the 2 wafers.

It should, however, be noted that wafer 2 also has lower sheet resistance and higher 2 DEG mobility due to the 1 nm of AlN spacer layer which increases the current density and reduces alloy scattering, and this wafer is associated with higher leakage currents within devices. Therefore to definitely say that the thin AlN nucleation layer is the main factor in the heat transfer a study, 2 wafers of identical layer structures have to be grown where the only difference in wafer are the nucleation layer and the growth method. In addition, as the high thermal conductivity substrate is still quite far from the channel (over 1 µm distance) other heat removal techniques or approaches to minimise heat generation such as heat sinks and/or distributed gates are required to further improve device performance Moreover measurements of the channel temperature and TBR are required to confirm that hot-wall MOCVD growth method leads to devices with better performance.

6. Distributed channel GaN HEMTs

6.1. Introduction

The use of high thermal conductivity substrates such as SiC or diamond improves the thermal performance of GaN devices, but the substrate alone is not enough to unlock the full potential of this technology [55]. In this chapter investigations of a device geometry/architecture for improved thermal performance will be described. A device layout with active and inactive regions along the width of the gate or channel has been shown to lead to channel temperature reduction. Darwish *et al.* used this distributed gate (DG) approach by forming inactive regions along the gate through etching the active layers [63]. And in [149], 330 nm wide etched trenches along the channel were shown to improve the DC characteristics (increased saturation current levels, etc.). A similar approach was taken by Lin *et al.* where the GaN layers were grown on a Si substrate patterned with stripes of SiO_2 to realise inactive and active regions along the device [150]. Using this approach, a good improvement in the thermal performance of the devices was demonstrated, but due to the etched mesa isolation the devices exhibited high gate leakage current.

In this thesis, a novel method of obtaining a distributed gate GaN HEMT with planar isolation using oxygen plasma treatment was investigated. The use of oxygen plasma treatment for mesa isolation and for realising a distributed gate/channel device as well as the device performance will be described. Thermal simulation presented here shows 30 °C improvement in the peak channel temperature across 100 µm wide gate finger with distributed gate/channel.

6.2. Principle of heat flow in distributed gate devices

Distributed gates efficiently improve the heat dissipation along the devices because they comprise an active device region next to an inactive region as illustrated in Figure 6.1. Active device areas generate heat (indicated as ''hot'' region), but inactive device areas do not. These regions (indicated as ''colder'' region) only absorb the heat leading to a reduced channel heating. In comparison with a conventional device geometry with a continuous active device where each segment would generate heat and therefore also contribute some heat to the segment next to it leading to much higher overall channel temperature, the distributed gate/channel architecture promises reduced channel temperature.

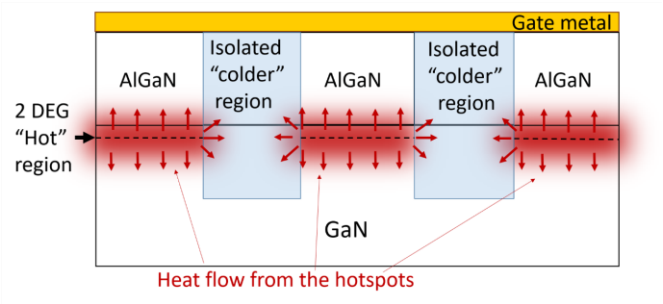


Figure 6.1 Illustration of the principle of heat flow in a distributed channel device.

Since heat diffusion is isotropic, to minimize the thermal crosstalk between the device fingers it is favourable to make an inactive region next to each active region along each finger and also in the neighbouring finger. Figure 6.2 illustrates a layout of distributed gates where each active region (indicated with "A") is surrounded by inactive regions from all sides (indicated with "I") further increasing the benefit of heat distribution. Figure 6.3 is a scanning electron microscope (SEM) image of a fabricated HEMT device with a distributed gate/channel realised using selective O_2 plasma treatment.

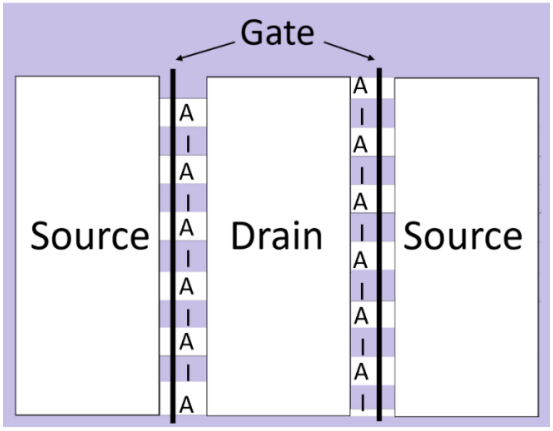


Figure 6.2 Illustration of a distributed region geometry in a device.

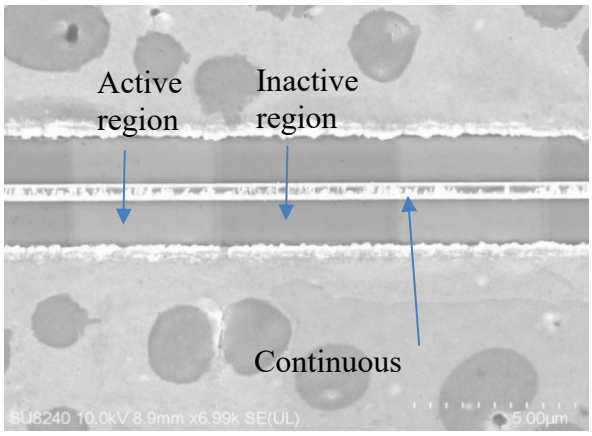


Figure 6.3 SEM image of the distributed gate region within a HEMT device.

6.3. Devices

6.3.1. Device geometry optimisation

In a HEMT, self-heating can be most clearly seen at high drain currents, e.g. at $V_{GS} = 0$ V, after current saturation. Since a TLM (transmission line method) structure on HEMT epilayers is essentially a HEMT without a gate, initial experiments on the distributed channel concept used this to test the concept. In order to find the optimum active and inactive region sizes and ratio tests on a 100, 200 and 500 µm wide TLM structures with 5 µm spacing between the Ohmic contacts were performed. Figure 6.4 shows results from a 200 µm wide TLM structure with 4 isolated gaps along the channel of width of 3, 5 7, 10 and 20 µm. These

show that larger gaps lead to larger current density, but at the same time the total active area is smaller, and they indicate that at least 40-50% of the device area should be made inactive in order to make significant improvement in heat reduction. These results are however inconclusive because the active area is not the same. In Figure 6.4 and for devices in the rest of this chapter the current densities are calculated by taking into account only the active device areas i.e. adding all the active gate periphery fragments along the device channel together to obtain the total active gate periphery of the device. Note that only the two larger structures (200 and 500 µm wide) showed significant changes in current density.

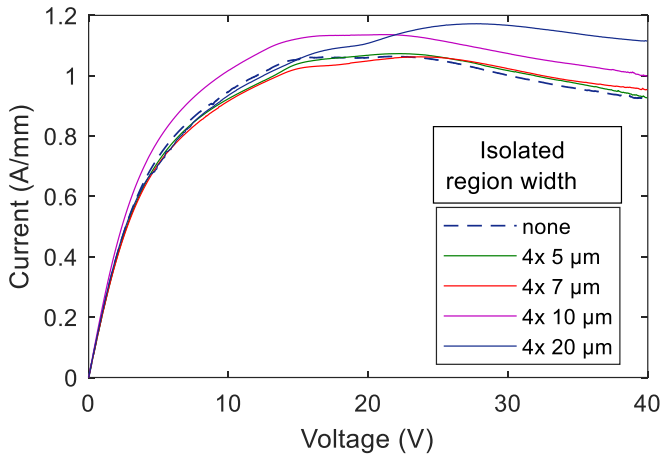


Figure 6.4 Currents across the 200 µm wide TLM structures with inactive region across the TLM width.

For the next test, all the TLM structures were chosen to have the same total active area. Figure 6.5 shows the current density between 500 µm wide TLM structures with different ratios of active (ON) and inactive (OFF) regions. The standard TLM structure exhibits a large decrease in the current after the saturation from 0.89 A/mm to 0.64 A/mm as the voltage increases up to 40 V, which is attributed to a higher channel temperature. The ratio of 5 µm active/ 5 µm inactive regions seemed to be the best and show steady saturated current with increasing applied voltage.

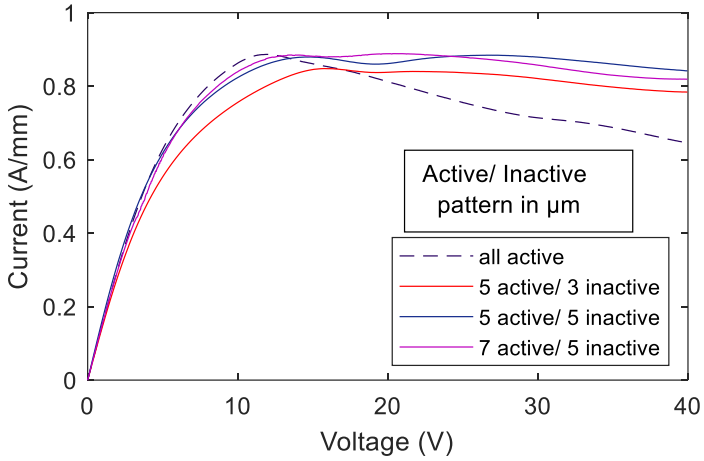


Figure 6.5 Currents across the 500 µm wide TLM structure with different ON/OFF region ratios.

For further insight, the channel temperature of device with a distributed gate (DG) architecture dissipating 2 W was simulated using finite element analysis software COMSOL Multiphysics [151]. The device epilayer structure used for simulation was the same as that used for the fabricated devices and consisted of a 350 µm SiC substrate, a 200 nm AlN nucleation layer, 2 µm GaN channel layer and 20 nm AlGaN barrier layer. The assigned thermal conductivities were 150 W/mK and 30 W/mK for GaN and AlN layers, respectively. Channel was inserted as a heater between AlGaN barrier layer and GaN buffer layer. Source and drain contacts are set up as a Gold layers with separation of 5 µm. Channel was represented as a heater with power dissipation of 2 W located at the AlGaN/GaN interface. Schematic illustration of the setup used for this simulation is shown in Figure 6.6.

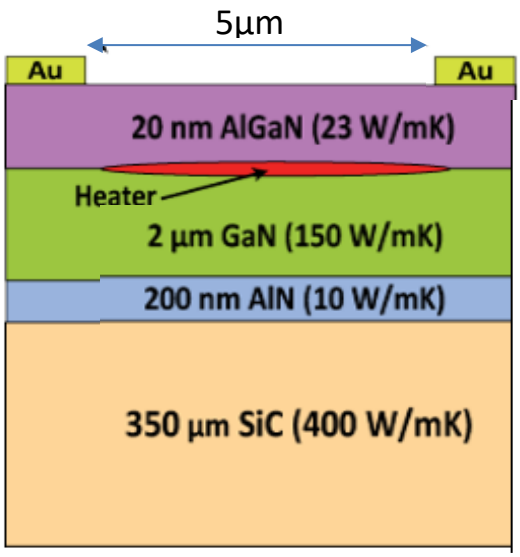


Figure 6.6 Schematic illustration of the device setup used for COMSOL temperature simulation.

A cross-section of the temperature profile vertically through the simulated device on a 1mm wide sample is shown in Figure 6. 7.

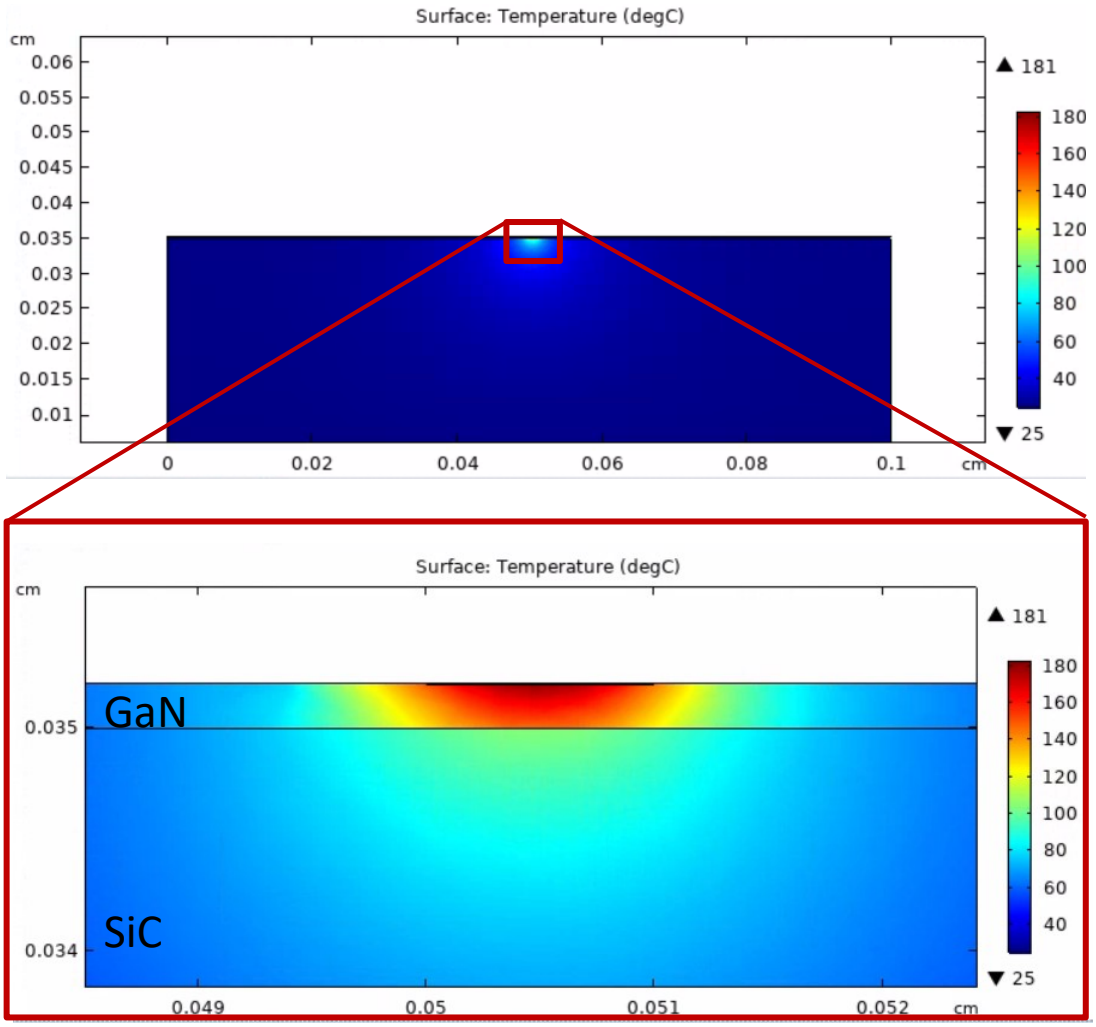
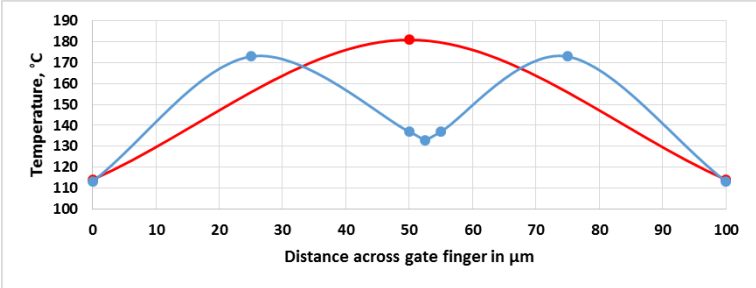


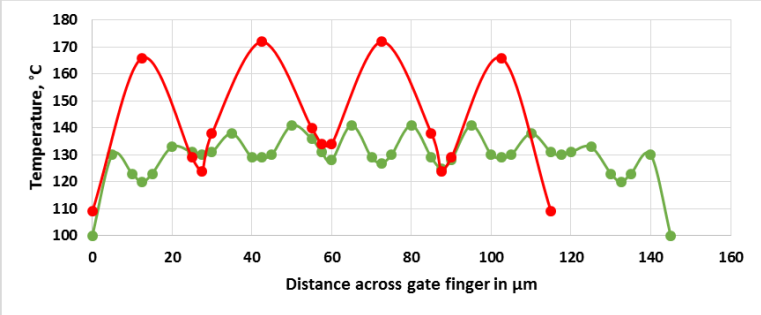
Figure 6. 7 Cross-section of the simulated device showing temperature distribution vertically through the device with zoomed in image of the channel area.

Four distributed gate structures with 1, 2, 4 and 10 active sections (or 0, 1, 3 & 9 inactive sections), with respective active areas of 1 × 100 µm, 1 × (2×50) µm, 1 × (4×25) µm, and 1 × (10×10) µm, respectively, were simulated. The heat source was located in the 2DEG channel at the GaN and AlGaN interface. The total active gate width in each case was 100 µm wide, while each inactive section was 5 µm wide. Figure 6.8 shows a comparison of the temperature profile across the 1×100 µm and 1× (2×50) µm gate geometries. The gate design with one inactive region in the middle of the device width results in a lower maximum channel temperature by 10 °C. Also, a low temperature zone in the middle of the active channel is introduced by the inactive region. Further sectioning of the gate finger, e.g. into four 25 µm or and ten 10 µm wide active gate sections Figure 6.8, reduces the maximum channel temperature even further, by over 30 °C. Clearly, one can see here that the relative

sizing and number of active/inactive sections along the width of the gate determines the device operating temperature.



(a)



(b)

Figure 6.8 COMSOL simulation of the temperature profile for a 100 µm wide active finger with one and without any 5 µm wide inactive section in the middle (a); and with three and nine 5 µm wide inactive sections (b). Power dissipation within device was 2 W.

This simulation was used only as in indication that this device design lowers the device channel temperature. The impact of the distributed gate geometry on device performance was then investigated experimentally.

6.3.2. Small gate periphery devices

As the 5/5 µm active/inactive area ratio seemed to have a steady saturated current in the TLM tests, this design was implemented into devices. Since it is known that the main heat generating spot within a device is the gate edge on the drain side [152], a device geometry with the isolated regions only under the gate was first implemented to test whether the isolated regions should be implemented along the whole channel or only under the gate. Both geometries are shown in Figure 6. 9.

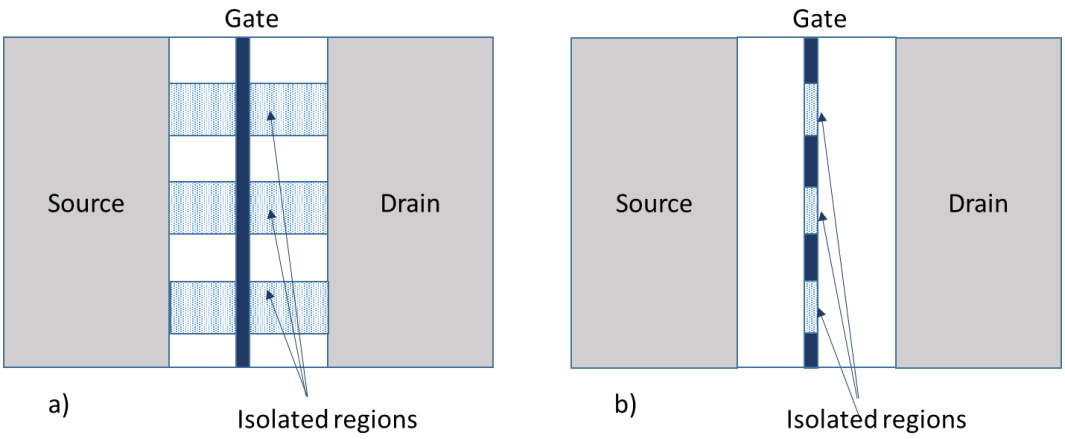


Figure 6. 9 Schematic illustration of the two distributed gate approaches a) under the whole channel and b) only under the gate.

Figure 6.10 shows a comparison of DC-IV curves among devices with total area of 2×100 µm as illustrated in Figure 6. 12 d) (denoted as Device C2) with active regions in 5µm/5µm inactive/active regions implemented only under the gate (denoted DG*-HEMT), along the whole channel (DG-HEMT) and a standard device without any inactive regions along the device width (C-HEMT). Here, one can see that distributing regions along the whole channel improves the saturated currents from 0.56 A/mm to 0.59 A/mm, having a 5% increase in the dissipated DC power at 20V drain-source voltage compared to isolating regions only under the gate. This result also suggests that the heat within the device comes not only from the heat-spot at the gate edge but also from the access regions and/or the metal semiconductor junction at Ohmic contact as was shown in TLM structures previously [153]. Therefore further work employed devices with distributed gate/channel regions.

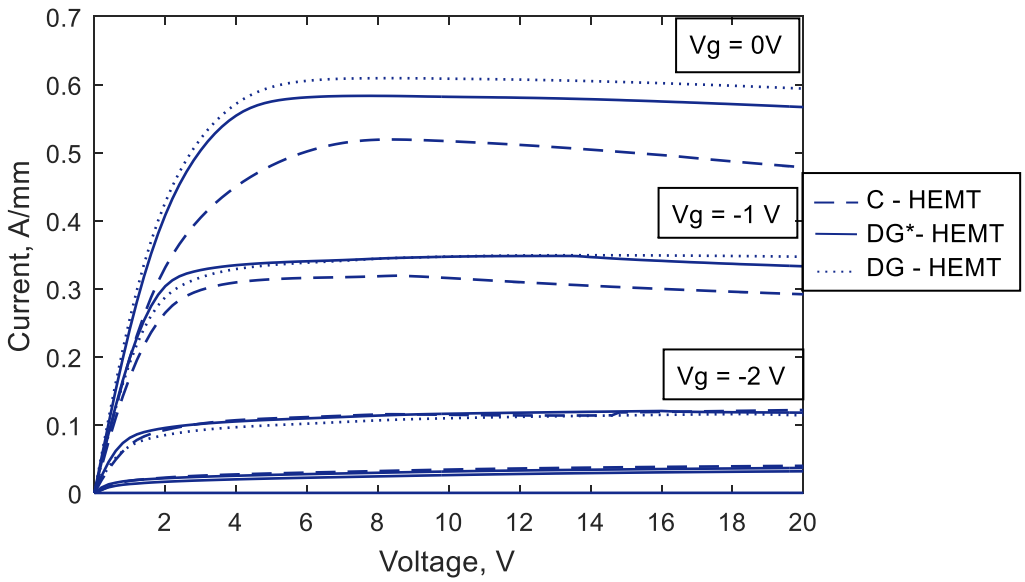


Figure 6.10 DC I-V Characteristics of standard device (indicated as (C-HEMT)), distributed gate (indicated as (DG*-HEMT)), and distributed gate and channel devices (indicated as (DG-HEMT).

Two different ways of how to implement distributed gates by isolation regions of the channel were investigated. The first method used isolated stripes only in the channel region as illustrated in Figure 6. 11 a). The second method used isolated stripes across the whole device, including the Ohmic contacts as illustrated in Figure 6. 11 b). It was found that the device behaviour was the same for both methods, which was expected as the active area of the device between the Ohmic contacts was the same. Therefore, for further distributed device designs a geometry with isolated regions along the device channel was implemented.

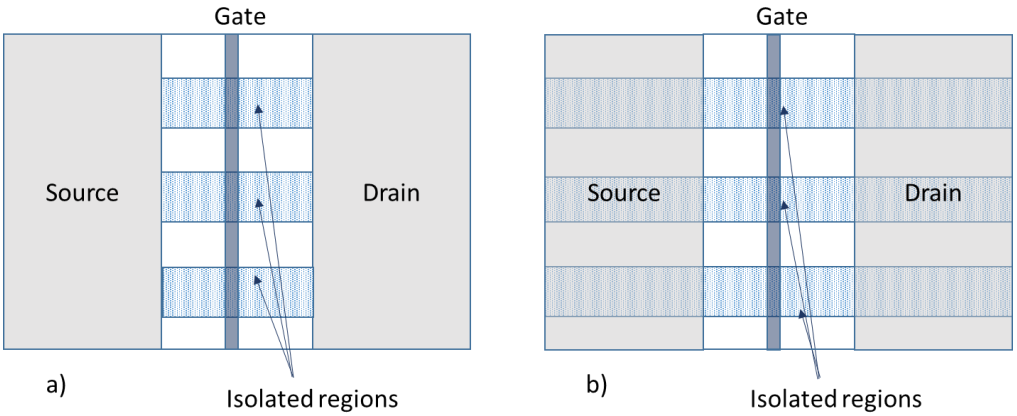


Figure 6. 11Schematic illustration of the two distributed gate approaches a) under the whole channel and b) under the whole device including Ohmic contacts.

The 5 µm ON/5 µm OFF ratio with isolation across the channel was first implemented into small gate periphery devices and standard DC measurements were performed on the fabricated distributed gate (DG-HEMT) and conventional devices (C-HEMT) with active area of 200 µm. Four devices (A, B, C and C2) were fabricated on the same wafer simultaneously all having 2×100 µm active area. Devices A and B had a gate pitch of 23.5 µm, with A is a standard device and B a distributed channel device, while devices C and C2 had a gate pitch of 83.5 µm, with C is a standard device and C2 is a distributed gate device. An SEM picture of each device is shown in Figure 6. 12.

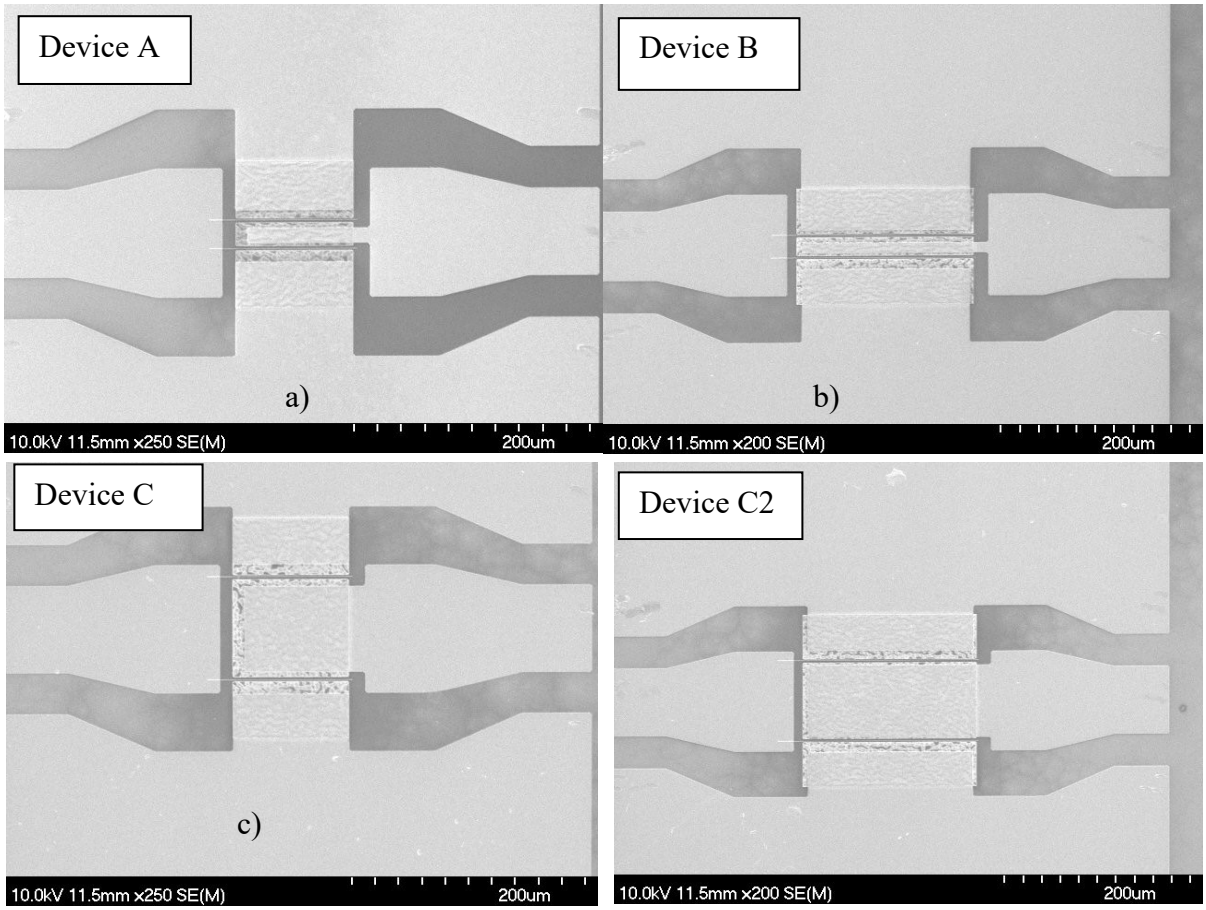


Figure 6. 12 Fabricated 2 finger devices with 200 µm active area a) device A (gate pitch of 23.5 µm standard device) b) device B (gate pitch of 23.5 µm distributed channel device) c) device C (gate pitch of 83.5 µm standard device) and d) device D (gate pitch of 83.5 µm distributed gate device).

The device output characteristics are shown in Figure 6.13 for all 4 devices A, B, C and C2. It can be seen that at $V_G = 0$ V and $V_G = -1$ V, where self-heating can be most clearly seen, saturated output currents are higher for the distributed gate/channel HEMTs B and C2 when compared to standard devices A and C. However there is almost no difference between saturated current at 40 V for devices C2 and B. The transfer characteristics of devices A, B and C at $V_{DS} = 5$ V are shown in Figure 6.14. Here one can see that all three devices have the same peak of transconductance. The 9% higher currents are attributed to the reduced channel temperature due to the inactive regions along the device channel.

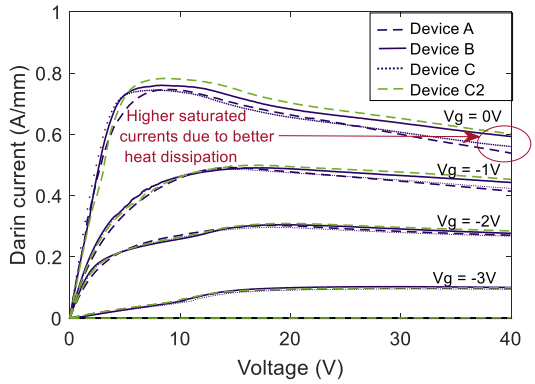


Figure 6.13 I_{DS}- V_{DS} characteristics of 2×200µm DG- and C- HEMTs.

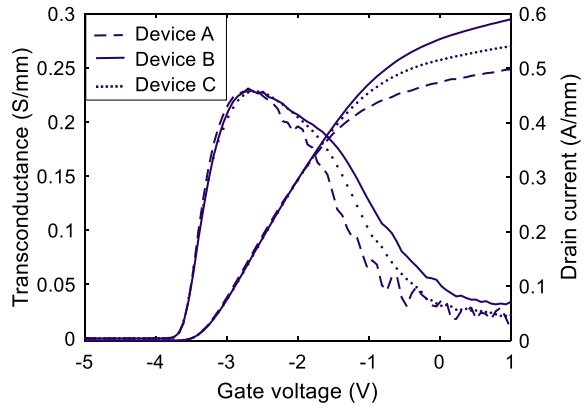


Figure 6.14 Transfer characteristics of devices A, B and C at V_{DS} = 5 V.

The transfer (I_{DS}-V_{GS}) characteristics at V_{DS} = 4 V shown in Figure 6. 15 illustrate that both distributed gate/channel devices and standard HEMTs have the same threshold voltage of -3.8 V and have current levels under 1 µA/mm in the pinch-off region for V_{DS} = 4V. Figure 6. 16 shows the gate leakage currents which were less than 1.8 µA/mm for both types of devices. The difference in the leakage currents was negligible for the compared devices. There was no visible degradation in the leakage currents for distributed gate/channel device compared to standard devices due to the planar surface under the gate. This is the main advantage of the proposed technique described here over the etched distributed gates, since it also reduces the possibility of damaging the substrate during the etching process. This approach not only improves the heat dissipation within the device but also shows lower leakage currents than any of the previous DG device fabrication attempts made by other groups, where for instance implementing distributed gates led to an increase in the gate leakage currents from 2.1 µA/mm to 8.2 µA/mm [150].

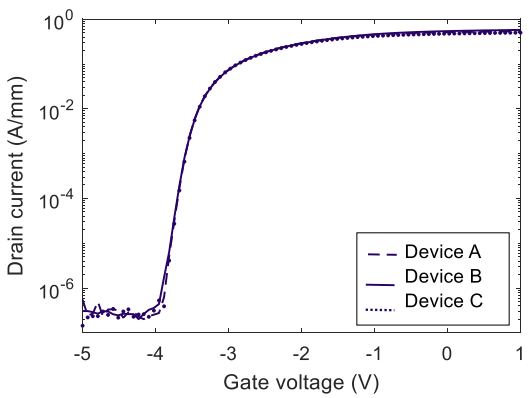


Figure 6. 15 I_{DS}-V_{GS} characteristics of DG- and C-HEMTs with 200 µm gate periphery at V_{DS} = 4V.

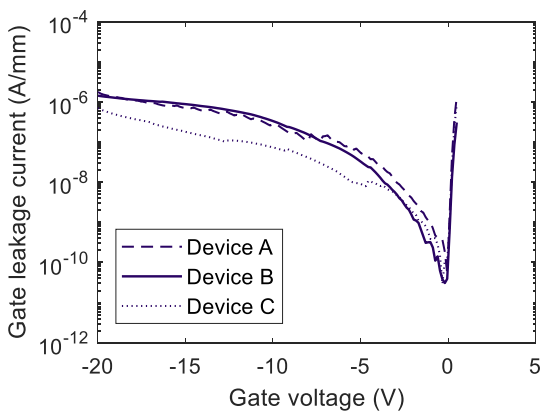


Figure 6. 16 Gate leakage currents of DG- and C-HEMTs with 200 µm gate periphery.

S-parameter measurements were done on all four devices biased at two drain voltages of V_D = 15 V and V_D = 25 V corresponding to peak transconductance. Extrapolated cut off frequencies (f_T) and maximum oscillating frequencies (f_{MAX}) are provided inTable 6.1. Devices A and C have the same cut-off frequencies of 45 GHz and 35 GHz at 15V and 25V, respectively. One can see that there is almost negligible decrease of 3 GHz for f_T at V_D =15 V and just 1 GHz decrease for f_T V_D = 25 V for distributed gate/channel device B when compared to standard devices A and C. However device C2 exhibits much lower cut-off frequencies f_T /f_{MAX} and therefore is considered as not successful design.

Table 6.1 Extrapolated f_T and f_{MAX} values from S-parameter measurements of devices A, B, C and C2 a VD of 15 V and 25 V.

Device	Gate pitch (µm)	F_T (GHz)		F_{MAX} (GHz)	
		V_D = 15 V	V_D =25 V	V_D =15 V	V_D =25 V
A	23.5	45	35	78	60
B **(DG)**	23.5	42	34	56	47
C	83.5	45	35	77	64
C2 **(DG)**	83.5	36	30	48	44

As these devices are small, i.e. have only 2 gate fingers, the gate pitch does not have a huge impact on the cut of frequencies f_T /f_{MAX}. However, for larger devices the gate pitch will determine how many gate fingers can be made in a certain transistor before it starts to have phase discrepancies due to the time difference of how long the signal has to travel to reach each gate finger.

6.3.3. Device I-V measurements at various ambient temperatures

DC-IV measurements were performed on standard HEMT and DG-HEMT with active area of 1×100 µm in ambient temperatures from 9 K to 300 K. DC-IV measurements at 9 K show the full potential of the device since the heating effects are minimized. At the ambient temperature of 9 K both devices exhibit the same amount of saturated output current as expected since they both have the same active area. In Figure 6.17 one can see that as the ambient temperature increases the saturated output current at 10 V drain voltage decreases due to heating effects. The decrease in the current is still insignificant up to 150K, but as the temperature increases the saturated current severely drops due to the self-heating effects. However, it is noted that the decrease in the saturated output currents is not linear.

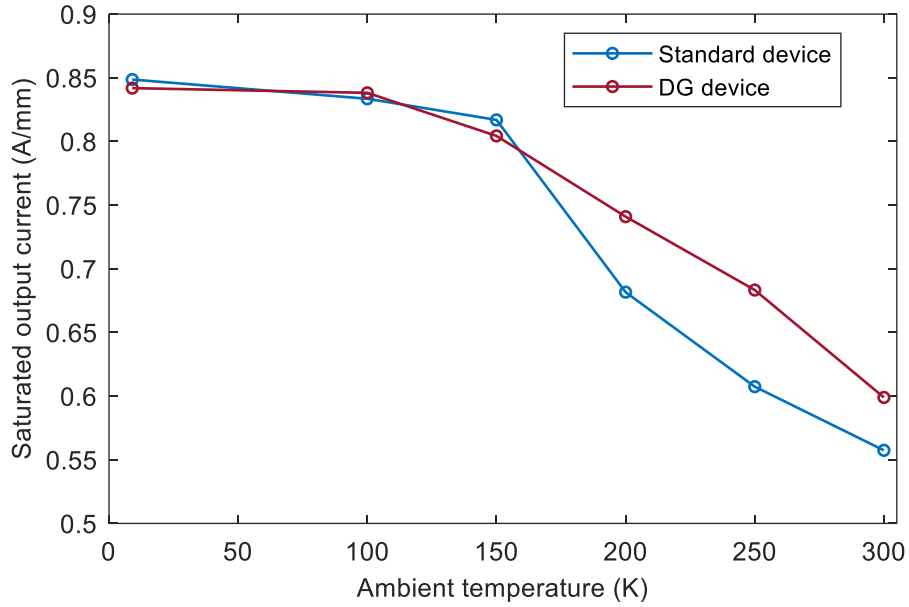


Figure 6.17 Saturated output currents at V_D = 10V and V_G = 0V with varying ambient temperature for devices with active area of 1x100µm.

Both types of devices exhibit knee walkout as the ambient temperature increases as can be seen in Figure 6.18. Knee walk out is generally associated with self-heating and electron trapping in the buffer layer and surface [16]. The devices compared here are made on the same wafer simultaneously, therefore have the same epilayer characteristics, Ohmic and gate contact properties, passivation, isolation. Moreover, these devices have been through the same processing steps thus it is assumed that the electron trapping levels in both devices are the same or at least the difference in trapping levels are negligible. However, there is a significant difference in the knee voltages between DG and standard devices as illustrated in Figure 6.18. DG devices exhibit significantly smaller knee walkout, reducing the knee voltage by a factor of two. We attribute this to the improved heat dissipation in the channel demonstrating how crucial the reduction of the channel temperature is in the device in order to improve device performance. It is also suspected that due to the thin (30 nm) SiN passivation there is a slight virtual gate formation on the surfaces of both devices but in the DG device it is reduced since the peak of electric field at the gate edge on the drain side is distributed due to the inactive regions along the device, but still the main improvement in knee voltage comes from the efficient heat distribution.

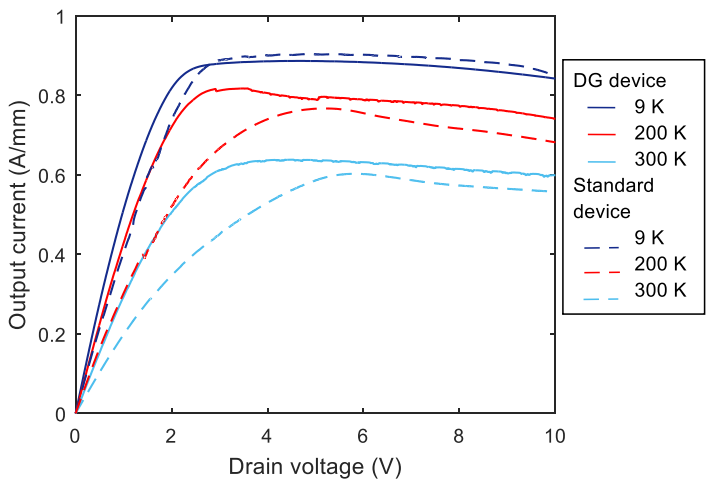


Figure 6.18 Saturated output currents at V_G = 0V with varying ambient temperature for devices with active area of 1×100µm.

6.3.4. Large gate periphery devices

Three different device designs with a gate periphery of 1 mm were fabricated on the same sample; two standard geometry devices with gate pitch of 23.5 (device D) and 83.5 µm (Device F) and a distributed gate device with gate pitch of 23.5 (Device E). All devices had source-drain separation of 3.5 µm, gate length of 200 nm, total active device area of 10 × 100 µm. Distributed gate/channel device had a stripe pattern of 5 µm wide isolated lines and 5 µm active regions along the device width. Scanning electron microscope (SEM) images of fabricated 10 finger standard and distributed gate/channel HEMTs with gate pitch of 23.5 µm are shown in Figure 6.19 & Figure 6.20, respectively. To have a 1 mm wide active region when isolated regions of 5 µm are introduced after each 5µm active region the total contact area of the device becomes almost 2 times larger. To compare the effects on self-heating of distributed gate/channel devices with other means of reducing self-heating such as increasing gate pitch, a standard device with gate pitch of 83.5 µm were also fabricated. An SEM micrograph of this shown in Figure 6.21. The source contacts on all devices were connected through metal bridges with 2 µm thick polyimide (PI-2545) layer underneath them for support as shown in Figure 6.22. Bond pads were fabricated in CPW (coplanar waveguide) technology with pitch of 100 µm.

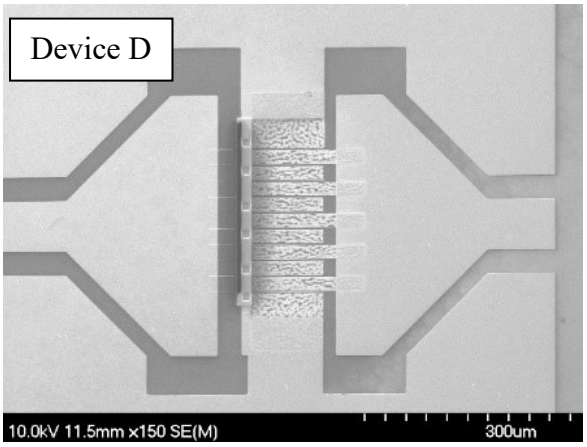


Figure 6.22 SEM image of a fabricated distributed gate device D.

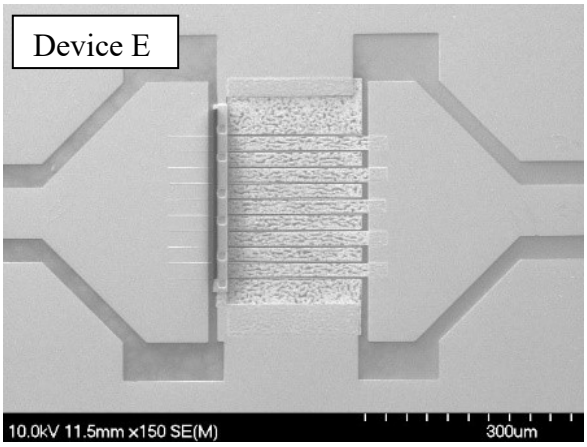


Figure 6.22 SEM image of a fabricated distributed gate device E.

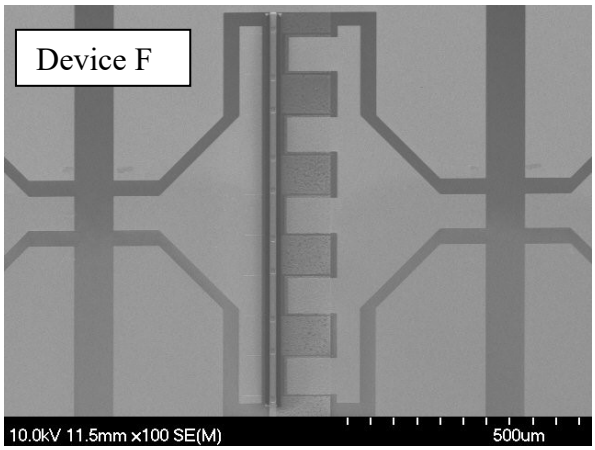


Figure 6.22 SEM image of a fabricated distributed gate device F.

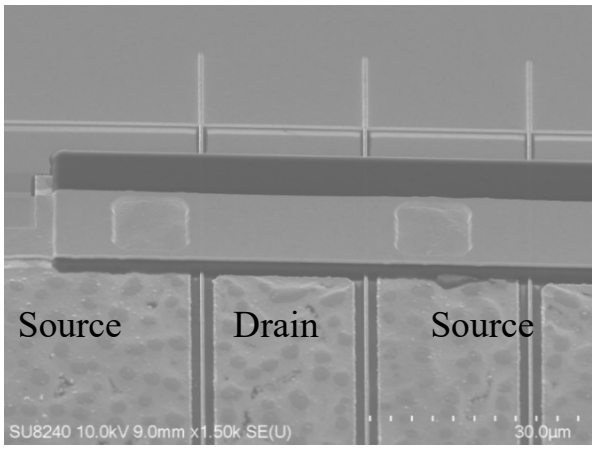


Figure 6.22 SEM image of a metal bridge connecting source contacts with the supporting polyamide layer.

Standard DC current-voltage (IV) measurements at room temperature were performed on all three fabricated 10 finger devices D, E and F. Figure 6. 23 shows IV characteristics for distributed gate/channel (device E) and standard devices (devices D and F) measured continuously from V_{GS} = 0 V to V_{GS} = -5 V with 1 V decrements. In the large gate periphery devices there is a tradeoff between increasing the total device area and reducing the channel temperature and consequently improving performance. It can be seen from Figure 6.23 that both devices E and F perform better than device D, i.e. have higher saturated current. Here, one can also see that increasing the device width for the 10×100 µm device 2 times by introducing the inactive regions along the channel (device E) reduces the channel temperature more efficiently compared to increasing gate pitch by increasing the length of Ohmic contacts 4 times (device F), which can be seen as increased saturated current.

All three fabricated devices exhibited extremely low gate leakage currents of <0.2 µA/mm at V_{DS} = 0 V and V_{GS} = -20 V as shown in Figure 6. 24 . This is attributed to the use of oxygen plasma treatment for creation of the non-conducting regions including device

isolation. The planar geometry eliminates electrons tunneling into the channel from the gate through the mesa sidewall, for instance. As seen with small gate periphery devices there is no degradation in the leakage currents for the DG device compared to the standard devices showing the advantage of this planar device geometry over previous attempts to fabricate distributed gate HEMTs using etched isolation [150].

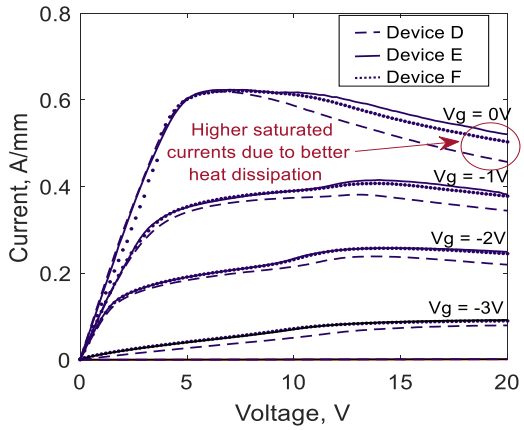


Figure 6. 23 I_{DS}- V_{DS} characteristics of DG- and C- HEMTs with 10x100μm gate periphery.

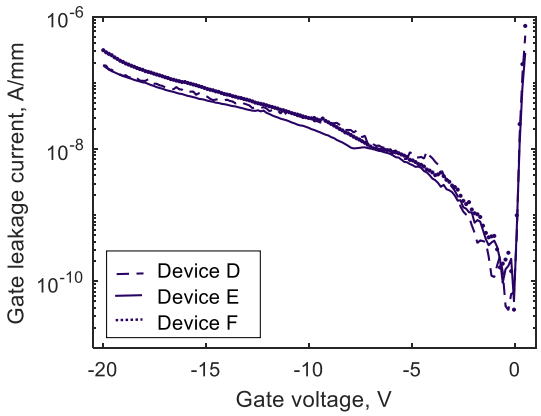


Figure 6. 24 Gate leakage currents of DG- and C- HEMTs with 10x100μm gate periphery.

As each gate finger is a heat source in multiple finger devices there are multiple heat sources and therefore gate pitch plays an important part in the channel temperature due to the thermal crosstalk between the gate fingers. This can be seen in measured DC-IV characteristics.

The device pitch also has an impact on RF performance and total achievable device size for given frequencies. S-parameter measurements were performed on devices D, E and F using Network Analyzer E8361A PNA. The measured data was converted into hybrid parameters to obtain the current gain, h21, while Mason's unilateral power gain was directly calculated and both quantities are shown in Figure 6.25. Extrapolated f_T and f_{MAX} values (pad parasitics included) are given inTable 6.2. At V_D of 15 V we see a 5 GHz decrease in the f_T for DG device (device E) compared to standard devices D and F due to the longer total gate width. However, increasing the bias point to V_D = 25 V there is no change in f_T, which suggests that with higher power dissipation within the device there is less degradation in cut-off frequency than there is for standard devices. It also suggests that with even higher bias voltages f_T might be higher for distributed gate device than it is for standard devices, which agrees with the previous work [63]. Extrapolated f_{MAX} values are higher for device D and the same for devices E and F, which lets one conclude that increasing device size by introducing distributed regions to increase the device width by 2 times gives more advantage than reducing the Ohmic contact length by 4 times. This is so because it allows one to design

a larger device with the same active area. Here f_{MAX} is still significantly lower compared to 2 finger devices for all three devices D, E and F due to parasitic capacitance that comes from the polyimide used for source connecting bridges. This can be improved by using air-bridge structures since air has the lowest dielectric constant of 1 compared to 2.6 for polyimide (PI2645). Cut off frequencies also depend on the contact resistance R_C which here is 0.47 Ω·mm for all devices described in this chapter. Improving contact resistance would increase the saturated currents and device gain therefore also cut off frequencies.

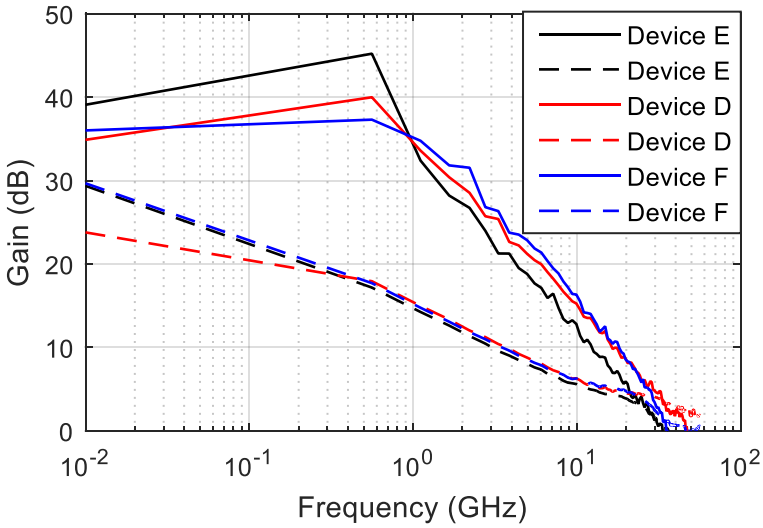


Figure 6.25 Measured H21 and Maximum signal gain for devices D, E and F at V_D = 15V.

Table 6.2 Extrapolated f_T and f_{MAX} values from S-parameter measurements of devices D, E (distributes gate device) and F at V_D of 15 V and 25 V.

Device	Gate pitch (µm)	F_T (GHz)		F_{MAX} (GHz)	
		V_D = 15 V	V_D = 25V	V_D = 15V	V_D = 25 V
D	23.5	40	33	46.7	45
E **(DG)**	23.5	35	33	35	35
F	83.5	40	33	35.4	35

The achieved results demonstrate that increasing the gate pitch and width is not advantageous for RF performance because

- the phase discrepancies between the centre gate and gates toward the end of the device since the signal path lengths are different
- larger drain pads lead to increased drain-source capacitance which reduces gain, bandwidth and is also harder to design an output match circuit
- larger source pads lead to increased source inductance Ls which gives lower gain because of its negative feedback effect

Therefore, in conclusion, we can say that there is a trade-off between decreasing the channel temperature and keeping the same frequency performance using this method at V_D of 15 V.

However, when these devices are driven at higher drain voltage of 25 V there is no cut off frequency f_T degradation. Improved DC-IV performance and no degradation in f_T also lets one suspect that the device lifetime of distributed gate devices would be longer than the lifetime of standard devices. Therefore distributed gate devices can be very useful in applications where the operational temperature of the chip is limited since the device can be biased at much higher drain voltage while maintaining operational temperature below the required temperature limit [154]. Based on these results it can be concluded that the method of distributed gate/channel does improve both the thermal and electrical performance of AlGaN/GaN HEMTs.

6.5. Summary

In this chapter a novel approach of obtaining planar distributed gates by using oxygen plasma treatment has been described and discussed. Small gate periphery devices with two fingers and large gate periphery devices with ten gate fingers were studied. The proposed method allowed the realisation of distributed gate devices with no degradation in gate and drain leakage currents as compared to previously reported distributed gate devices [150]. The devices exhibited decreased the channel temperature as could be deduced from the measured device output characteristics and simulated data. Simulated data showed peak temperature decrease by 30 °C across a single 100 µm wide gate finger. The distributed gate/channel device geometry is therefore expected to provide longer device lifetimes and less memory effects that usually come from device self-heating. These devices seem suited for use in power amplifier circuits at high operating voltages (above 25 V) where the advantage of the improved thermal dissipation outweighs the reduced gain/cut off frequencies from the added parasitics from increasing the gate width as also shown in previously reported designs [63].

7. GaN-based microwave power amplifiers

7.1 Introduction

With the constant development of GaN HEMT technology and demand for higher power levels and high frequencies there have been major developments in this area. HEMTs can be used in circuits that operate up to a quarter of the device f_{MAX}, therefore to realise X-band amplifiers the desired transistor cut-off frequencies for this project is around 50 GHz. In the previous chapter reported 200nm gate length devices exhibit f_T and f_{MAX} of 45 GHz and 79 GHz with pad parasitics included and so will be used for the amplifier design. In this chapter class A single stage amplifier (with external bias tees) design, fabrication and measurement results will be described and discussed. The amplifier design was done at the University of Liverpool and was fabricated and characterised at the University of Glasgow.

7.2 Microwave amplifier basics

An amplifier is a device/component that turns small input electric current/voltage into a larger output electric current/voltage. In a power amplifier (PA), the input power (voltage × current) is turned into a larger output power. A transistor amplifies a signal at its input terminals, usually applied between the gate and source, with the output between the drain and source electrodes. As the source electrode is common to both the input and output, this is called a common source configuration. From the maximum power transfer theorem [155], we know that for a (voltage) source of internal impedance (Z_S) driving a load of impedance (Z_L), $Z_L = Z_S^*$ is necessary to maximize power transfer from the source to the load, this is also known as conjugate matching. Since in microwave and radio frequency (RF) electronic systems the reference impedance is 50 Ω, to amplify the signals using transistors requires that the input and output impedances of the transistor are transformed to 50 Ω. This is done using input and output impedance matching networks as illustrated in Figure 7.1. Matching networks can be designed from combinations of circuit elements (capacitors, inductors, transmission line sections), that are not sources of energy and do not have gain, known as passive elements. In a power amplifier, the energy that is added to the input signal has to be supplied externally from the DC supply, since due to the conservation laws, energy cannot be created from nothing. In a HEMT PA, external power supply (DC) is provided through the drain and gate contacts of the transistor and chosen to bias the transistor at an appropriate bias point. The schematic/block diagram of PA with one transistor shown in Figure 7.1. is called a single stage amplifier.

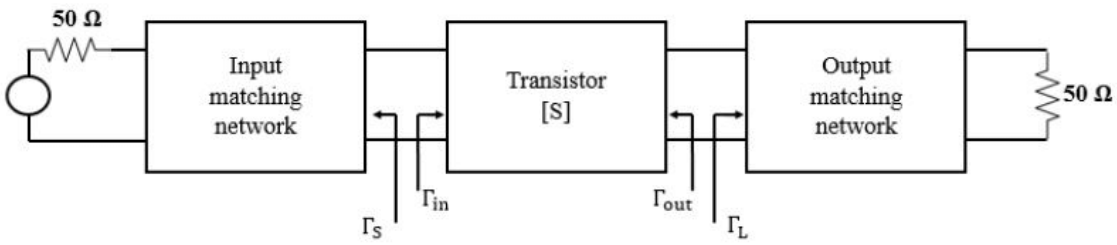


Figure 7.1 Schematic of single stage power amplifier.

Here Γ_S, Γ_{in}, Γ_{out} and Γ_L are source, input, output and load reflection coefficients respectively.

7.3 Matching network design

Using equation (3.14) the power capability of a transistor can be estimated [156]:

$$P = 0.25 * \left(V_{DSQ} - V_K\right) * I_{MAX} \tag{7.1}$$

where V_{DSQ} is the drain voltage applied to the HEMT, V_K is the transistor knee voltage (gate voltage at which the transistor enters the saturation region), I_{MAX} is the maximum drain current defined at the knee/saturation region.

From the measured DC-IV characteristics and S-parameters one can design the matching circuit for a transistor.

The operating power gain, G_P, provides a graphical matching network design method that can be used for Class A amplifiers (amplifier classes defined in section 7.5). Constant operating power gain can be represented as a contour of a circle on the Smith Chart. Smith Chart is based on a polar plot of the voltage reflection coefficient Γ which can be defined in terms of impedance Z_L. If a lossless transmission line with characteristic impedance Z_0 is terminated with a load with impedance Z_L then Γ_L can be written as:

$$\Gamma_L = |\Gamma_L| e^{j\theta} = \frac{Z_L - Z_0}{Z_L + Z_0} \tag{7.2}$$

Then Γ_L forms the load of the amplifier (as it can be used to define G_P which is independent of the source impedance and given by equation (3.16) [157]:

$$G_p = \frac{|S_{21}|^2 (1 - |\Gamma_L|^2)}{\left(1 - \left|\frac{S_{11} - \Delta\Gamma_L}{1 - S_{22}\Gamma_L}\right|^2\right)|1 - S_{22}\Gamma_L|^2} = |S_{21}|^2 g_P \tag{7.3}$$

where g_P is a circle on the Γ_L plane, the radius R_L and centre C_L are given by

$$R_L = \frac{\sqrt{1 - 2K|S_{12}S_{21}|g_{P+}|S_{12}S_{21}|^2 g_P^2}}{|-1 - |S_{22}|^2 g_P + |\Delta|^2 g_P|^2} \tag{7.4}$$

$$C_L = \frac{g_P(S_{22}^* - \Delta^* S_{11})}{1 + g_P(|S_{22}|^2 - |\Delta|^2)} \tag{7.5}$$

Maximum gain occurs when $R_L = 0$, so g_P can be rewritten as:

$$g_{P,MAX} = \frac{1}{|S_{12}S_{21}|}\left(K - \sqrt{K^2 - 1}\right) \tag{7.6}$$

In general, the matching procedure is as follows:

1) Find g_P
2) Draw operating gain circle on the Smith Chart
3) Draw load stability circle, select Γ_L that is in the stable region and not too close to the stability circle
4) Draw source stability circle
5) To maximise amplifier gain, calculate Γ_{IN} and check if $\Gamma_S = \Gamma^*_{IN}$ is in the stable region if it is not, iterate on Γ_L or compromise the gain

For simplicity in this project only unconditionally stable transistors at the design frequency (with geometric stability factor μ > 1) will be considered. The above procedure is shown in Figure 7.2 for a selected transistor with S-parameter S_{11} and S_{22} measurements at 10 GHz using software called Advanced Design System (ADS). As this transistor is unconditionally stable the source and load stability circles lie outside of the normalised Smith chart with radius of 1. That means that Γ_L can be selected from $g_{P,MAX}$ for the output match, which happens when $\Gamma_S = \Gamma^*_{OUT}$ and can be also calculated by:

$$\Gamma_L = \frac{S_{22}^* - \Delta \cdot \Gamma_S^*}{1 - S_{11}^* \Gamma_S^*} = \Gamma_{OUT}^* \tag{7.7}$$

Γ_S can be selected such that $\Gamma_S = \Gamma^*_{IN}$. Source reflection coefficient Γ_S can be calculated by:

$$\Gamma_S = \frac{S_{11}^* - \Delta \cdot \Gamma_L^*}{1 - S_{22}^* \Gamma_L^*} = \Gamma_{IN}^* \tag{7.8}$$

Then selected Γ_L and Γ_S are used to transform the corresponding impedances Z_S and Z_L to 50 Ohms. At microwave frequencies, transmission line components are used for impedance transformation. Transmission line sections in series transform the impedance inductively and transmission line stubs, i.e. short sections terminated in an open or short circuit, are usually connected in parallel and transform the impedance capacitively and inductively. Stubs work by means of standing waves of RF waves along their length and are used for matching network design in this thesis.

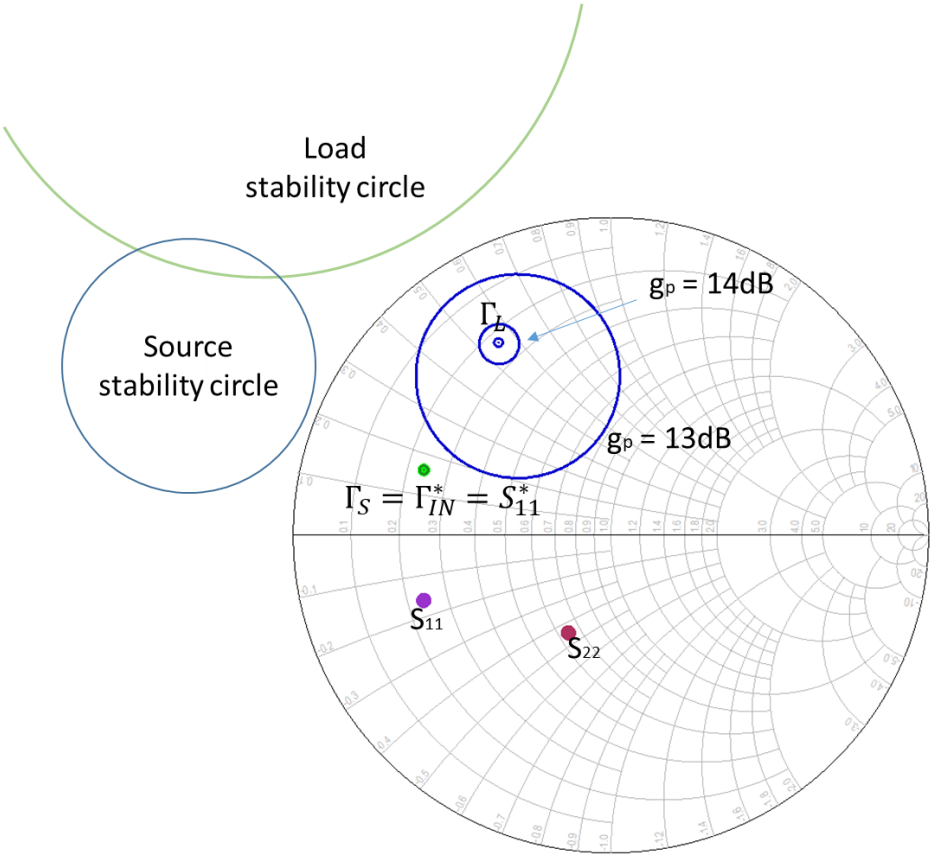


Figure 7.2 Smith chart with constant gain circles g_p for 13 dB and 14 dB, load and source stability circles, measured S_{11}, S_{22} at 10 GHz and selected Γ_L and Γ_S.

Maximum gain is achieved on a single point source/load impedance on the Smith chart however the gain can be traded for other properties such as bandwidth, noise, gain flatness or linearity by choosing different source/load impedances. For example, if a larger bandwidth is required gain can be compromised by selecting Γ_S as a point near the origin on constant gain circle for the source while keeping the real impedance as large as possible.

In a single stage amplifier, there are only 2 matching networks required, the input and output matching networks. However more than one transistor can be used in a single stage amplifier, in fact there can be two or more transistors in parallel. In that case the input matching network has to match all of the input transistor impedances to one 50 Ω input impedance and similarly all the output impedances have to be matched into a single output port with 50 Ω impedance. Amplifiers can also have multiple amplifying stages. In that case there is an inter-stage matching network that transforms the output impedance of the transistors in the first amplifying stage to the input impedance of the transistors in the next amplifying stages.

To ensure the functionality of the entire power amplifier including passive matching networks and the active transistors, small signal simulation needs to be done to verify the

stability of the circuit across the required frequency bandwidth. It is an important criteria because an unstable circuit can oscillate and appropriate control of the circuit is no longer possible. If necessary, a stabilising circuit must be included in the amplifier design.

7.4 Amplifier bias networks

A transistor with matching networks is essentially an amplifier however it also has to be biased. This requires the use of a bias tee, a T-shaped circuit junction which enables the separation or combining of both DC and RF signals. A bias tee usually consists of an inductor and a capacitor as shown in Figure 7.3. There are two main components of a bias tee – a part that blocks RF signal (usually an inductor) and lets through a DC signal called RF choke and a part that blocks DC signal (usually a capacitor) and lets RF signal through called DC block.

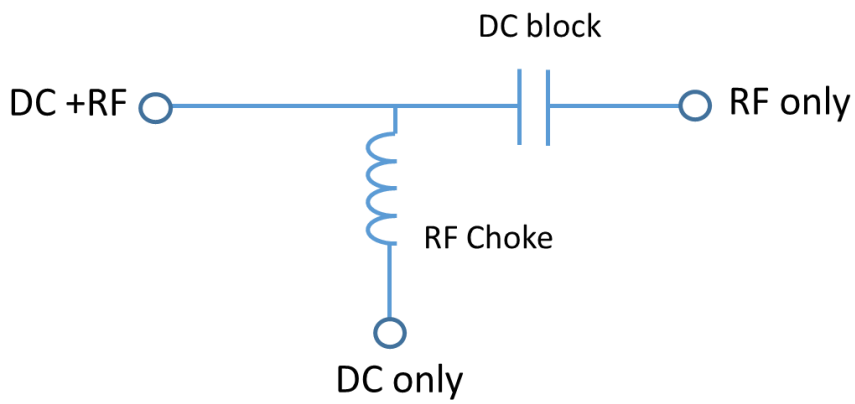


Figure 7.3 Equivalent circuit of a bias tee.

The RF choke is typically a large inductor placed in series with a conductor such as a wire or a circuit board trace, so it blocks changes in current thus acting as a low pass filter. So, having an inductor as RF choke in line with the DC bias of the amplifier blocks high frequencies while allowing the DC current to pass through, therefore effectively isolating the DC signal form RF signal. However, this inductor must be chosen with a self-resonance frequency (SRF) above the intended working frequency.

The bias network has to be "invisible" to the RF signal, i.e. be as close to open circuit as possible. On a MMIC, a short-circuited quarter wavelength (λ) transmission line stubs are often used to apply DC bias on active devices due to difficulty of finding bias choke inductors with sufficient SRF. The short-circuited end is usually grounded by a decoupling capacitor as shown in Figure 7.4. A quarter wavelength ($\lambda/4$) transmission line transforms the impedance from short circuit to a open circuit therefore the travelling RF signal 'doesn't see' this extra transmission line that is parallel to the path where the RF signal is travelling. In practice, this is usually not an ideal lumped element but a parallel plate component whose phase length becomes significant at high frequencies. Therefore, the short circuit plane does

not exist exactly at the end of the stub, which means the bias network is not fully decoupled from the RF signal line. So, there is a trade-off between large capacitor to provide better RF short circuit at the expense of poorer DC/RF decoupling and more ideal DC/RF decoupling at the expense of poorer short circuit due to reduced capacitance. This can be solved by adding an inductor which decouples the low frequencies if needed as shown in Figure 7.4. Another consideration is that SRF of high-value capacitor is low, in practice this decoupling capacitor is therefore often backed up by larger values further away with additional inductors and resistors to help the DC/RF separation and to take out any chance of feedback coming from the power supply and bias circuit.

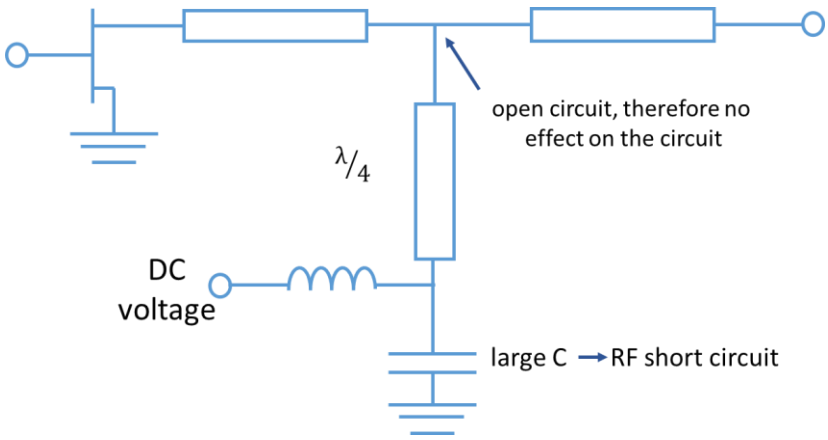


Figure 7.4 HEMT biasing using a short-circuited stub in parallel.

Another effective method is to use a radial microstrip stub as shown in Figure 7.5, which provides a low-impedance as illustrated in Figure 7.5. The "shorted" λ/4 line is a good solution for narrow bandwidth. The radial stub provides a wider bandwidth and can be further increased by adding a second radial stub symmetrically but still gives narrower bandwidth than an inductor can offer. Therefore, the choice of the design will depend on the target design parameters and target frequency.

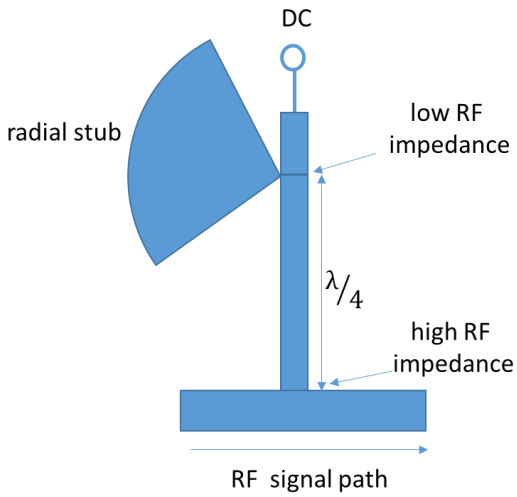


Figure 7.5 RF choke using radial stub.

On a MMIC, a DC block usually consists of a capacitor in series which doesn't let the DC signal to pass through but only the RF signal can travel through this capacitor. Usually the reactance of the DC blocking capacitor should be less than 0.1 Ω at the working frequency. A DC block capacitor must be used both at the RF signal input and output to keep the applied DC voltages only within the device/MMIC for which they are indented for, i.e.also keep it away from the RF signal source, receiver or measurement system which may malfunction with the unwanted dc bias.

7.5 Amplifier classes

Amplifiers can be divided into classes of operation from linear low efficiency operation to non-linear high efficiency operation. There is always a trade-off between efficiency and linearity. These classes consist of two main groups: PAs defined by the conduction angle (class A, AB, B &C) and ''switching'' amplifiers (class D, E, F, G, S, T). Conduction angle is the proportion of the input cycle (one period of signal for a sinusoidal signal) that the amplifier gives an output. Switching amplifiers use transistors to function as electronic switches that can be either on or off. These amplifiers use a technique called pulse width modulation to convert the signal into a stream of pulses where the time average power of the pulses is proportional to the original analog signal. The frequency of the pulses is many times higher than the highest frequency of the input signal so that passive low-pass filter can be used to smooth the pulses and convert them back to an analog signal.

Class A PA is a linear amplifier with low efficiency, theoretically only up to 50% [157]. It is biased in the middle region of the output characteristics as shown in Figure 7.6 such that the output current flows at all times. The input current is small enough to avoid the transistor being driven into cut-off so the device is always on, i.e. it has a conduction angle of 360°. Class A amplifiers are most commonly used in small-signal applications where linearity is more important that power efficiency. They are also used in large signal applications that require high linearity and high gain that outweighs the disadvantage of the poor power efficiency. Very high gain Class A amplifiers and higher amplifier classes (class B, C and above) cannot be designed using small signal (S-parameter) approach, and so other conventional design techniques such as load pull [158], active load-pull[159] and two port large signal characterisation[160] are used. The load line approach for choosing the bias points for different amplifier classes illustrated in Figure 7.6 and is used in large signal designs.

The DC bias point of a class B amplifier is set so that the conduction angle of each RF cycle is half sine waveform or 180°, i.e. the transistor conducts during either the positive or the negative half of the input signal cycle. Class B PA has higher efficiency than Class A amplifier- around 75%. Class AB PA are a compromise between Class A and Class B amplifier operation, it has conduction angle between 180 and 360 and efficiency between 50% and 75%, and it is not linear. Class C amplifiers have conduction angles significantly less than 180 improving the efficiency but causing distortion. They use additional tuned circuits to minimize distortion at the output and are used for narrowband applications [161]. DC bias points of class A, B, AB and C amplifiers are shown in Figure 7.6.

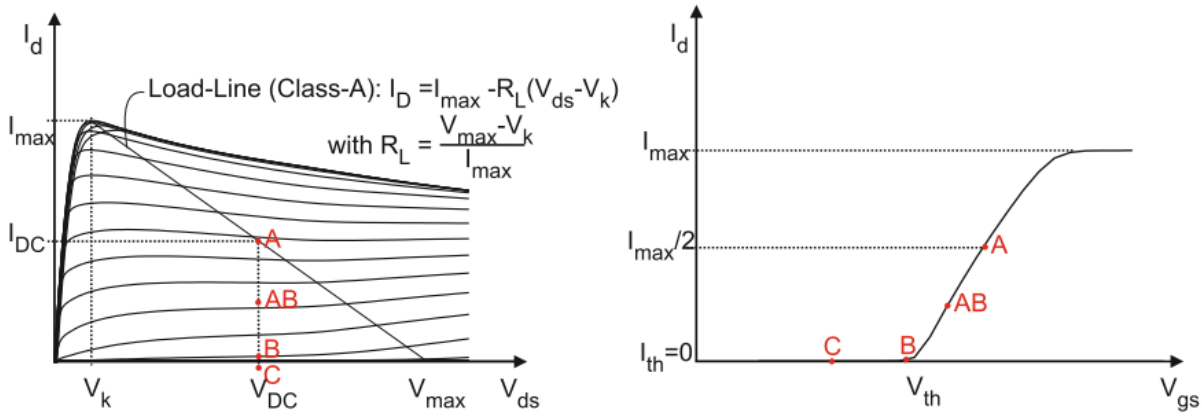


Figure 7.6 Transistor bias points for different class amplifiers on output characteristics (left) and on transfer characteristics (right).

Power amplifier classes D to T employ nonlinear switching between on and off states of the transistor, minimizing power loss and achieving high efficiencies by avoiding having high voltage across output transistor terminals and high current going through it simultaneously [162]. These classes differ from each other in the way the transistor output is tuned at various harmonic frequencies. Switching PA classes with high efficiency are the least understood from power amplifier types and therefore are currently being researched by various research groups [163]–[165].

7.6 X-band GaN power amplifiers

GaN HEMT power amplifiers are becoming more and more capable to deliver higher powers entering the kilowatt power range (at lower frequencies), which show their potential to replace travelling-wave tube amplifiers in the future. Kwack *et al*. have shown a design and manufactured multistage S-band 1-kW pallets working at 2.9 -3.3 GHz range [166]. Power added efficiency (PAE) values as high as 72% with the absolute power of 3.5 W have been reached for 10 GHz frequency operation [167].

X-band radar applications require output power levels greater than 20 W from a MMIC. For a typical X-band MMIC unit cell device with gate periphery between 1-1.5 mm, the continuous wave (CW) mode output power density drops to 5 W/mm due to strong device heating. Large GaN devices produce heat fluxes of more than 1 kW/cm^2, which are very challenging to dissipate with existing cooling technologies [168]. Therefore, state of art X-band GaN power amplifiers (PA) have to be operated in a low duty cycle (<10%) pulsed mode to prevent overheating , i.e. keeping the junction temperature below 200 °C and to maintain power density of over 3 W/mm [52]. Typical GaN HEMT sizes and performance parameters are showed in Table 7. 1 and typical power amplifier parameters with these transistors are shown in Table 7. 2. Most X-band amplifiers employ 8 to 10 finger HEMTs with gate lengths between 140-300 nm. Typical 250 nm gate length devices used in power amplifier have at least 1 A/mm of maximum drain current I_{DMAX} with contact resistance R_C of 0.4 ± 0.2 Ω·mm delivering around 35 dBm amplifier output power at 10 GHz.

In this thesis, the PA target frequencies were 6-16 GHz which spans over the X band (8-12 GHz) and Ku band (12-18 GHz) frequency range. A novel structure with 70 nm thick GaN cap layer, i.e. with a buried channel layer, was be investigated to minimise current collapse which causes significant device gain reduction and is one of the major issues with current GaN HEMT technology. In addition, different thermal management approaches were considered for integration in the device fabrication process to improve the output power and efficiency of the GaN devices so that amplifiers with higher output powers could be realised. Proposed thermal management solutions are described in chapters 6 and 7.

Table 7. 1 State of the art AlGaN/GaN transistor sizes used in power amplifiers for X-band applications compared to 2 and 10 finger devices from Chapter 6.

Gate length (nm)	No. of device fingers	AlGaN (%)	AlGaN thickness (nm)	Rc (Ω·mm)	I_{DMAX} at V_G = 1V (A/mm)	V_{DS} (V)	f_T (GHz)	f_{MAX} (GHz)	Ref
140	8 × 100	25	Double hetero-junction	0.2	1.2	10	97	230	[167]
140	8 × 130	-	-	-	1.2	10	58	150	[15]
180 (recessed gate)	2 × 100	25	20	0.35	0.55	10	48	130	[169]
250	8 ×100	25	28	0.6	1.17	30	36	51	[170]
250	16 ×100	-	-	0.2	-	20	18	35	[171]
250	8 × 100	25	28	0.6	1.17	30	36	51	[172]
250	2 ×125	-	-	0.4	1.05	28	23	65	[173]
300 (recessed gate)	10 ×100	26	22	-	1	30	28.2	>50	[174]
300 (recessed gate)	10 × 125	26	22	-	1	25	21.7	>60	[175]
200	10x100	25	20	0.48	0.63	25	33	45	This work
200	2x100	25	20	0.48	0.78	15	45	78	This work

Table 7. 2 State of the art parameters of AlGaN/GaN power amplifier MMICs on SiC used for X-band applications compared to the amplifier presented in this Chapter.

No. of GaN HEMTs	No. of amp. stages	Gate length (nm)	HEMT size (µm)	V_{DS} (V)	Small signal gain (dB)	Power density (W/mm)	Output power (dBm)	PAE (%)	Frequency (GHz)	Ref.
1	1	250	8 × 100	40	-	4.6	35.7	26	10	[170]
1	1	150	10 × 100	20	-	-	35.1	67	10.1	[176]
1	1	250	8 × 100	25	-	3.3	34.2	32	10	[170]
1	1	140	8 100	21	8	5.5	36.4	57	10	[167]
1	1	140	8 × 100	15	9	3.2	34	72	10	[167]
2	1	300	8 × 125	30	10	-	36.5	40	8-8.4	[177]
2	1	250	8 × 125	20	11.5	-	36.7	45	8.8	[178]
2	1	250	8 × 100	39	8	5	39	33.8	10	[172]
2	1	150	10 × 100	20	-	-	35	56.4	10.1	[176]
4	1	300	10 × 150	35	7	3.73	41.6	-	10	[179]
4	2	300	8 × 150	40	18	4.16	43	-	10	[179]
6	2	250	6 × 100	25	16.3	6.7	46.3	52	10.5	[171]
6	2	300	10 × 100	28	15	4.8	39	20	9-11.2	[174]
1	1	200	10x100	20	9.8	1	30	44	10	This work

7.7 Impedance matching network design for a single stage power amplifier

For the first-generation amplifier, a 10-finger device with gate length of 200 nm was chosen. To improve the thermal efficiency a wafer grown by hot-wall MOCVD growth described in chapter 6 was chosen. S-parameter measurements were performed for the chosen transistor and this transistor was found to be unconditionally stable above 7.5 GHz following equation 2.8. F_T and f_{MAX} of 200 nm gate length device was found to be 45 GHz /79 GHz, respectively, therefore these transistors are suitable for an amplifier circuit in the X band. The software used to design matching circuits here was Microwave Office by National Instruments [180]. To design a matching network for the chosen transistor input and output impedances at the frequencies of interest must be matched to 50 Ohms. Load and source impedance Γ_L and Γ_S are selected following procedure explained in Section 7.3. Output impedance in chosen by calculating optimum load impedance Γ_L by calculating maximum operating gain $g_{p,MAX}$ using equation 3.16 giving the centre of Gp at 0.615 ∠ 117.45° for 14 dB gain, which corresponds to $Z_L = Z_0(0.32 + j0.561) = 16 + j28.05\ \Omega$ with characteristic impedance $Z_0 = 50\ \Omega$. Input matching is set for maximum gain by introducing a conjugate match at 15 GHz calculated by equation 3.20 giving a source impedance $Z_S = Z_0(0.238 + j0.09) = 12.9 + j4.5\ \Omega$. These input and output impedances were then matched using coplanar waveguides as transmission lines in two designs, one with double stub matching denoted as amplifier A and one with single stub matching denoted as amplifier B. The schematic of the input and output matching networks are given in Figure 7.7 and Figure 7.8 for amplifiers a and b respectively. Here coplanar waveguides in series and stub configurations are chosen to transform the input and output impedances. Design parameters of the coplanar waveguide transmission lines were set as follows:

- Signal line width W was set to 75 µm
- Gap between the ground and signal S was set to 40 µm
- Dielectric constant of SiC was set to 9.6
- Substrate thickness H was set to 500 µm
- Metal thickness T on CPW was set to 1 µm
- Loss tangent Tanδ set to 0.0005

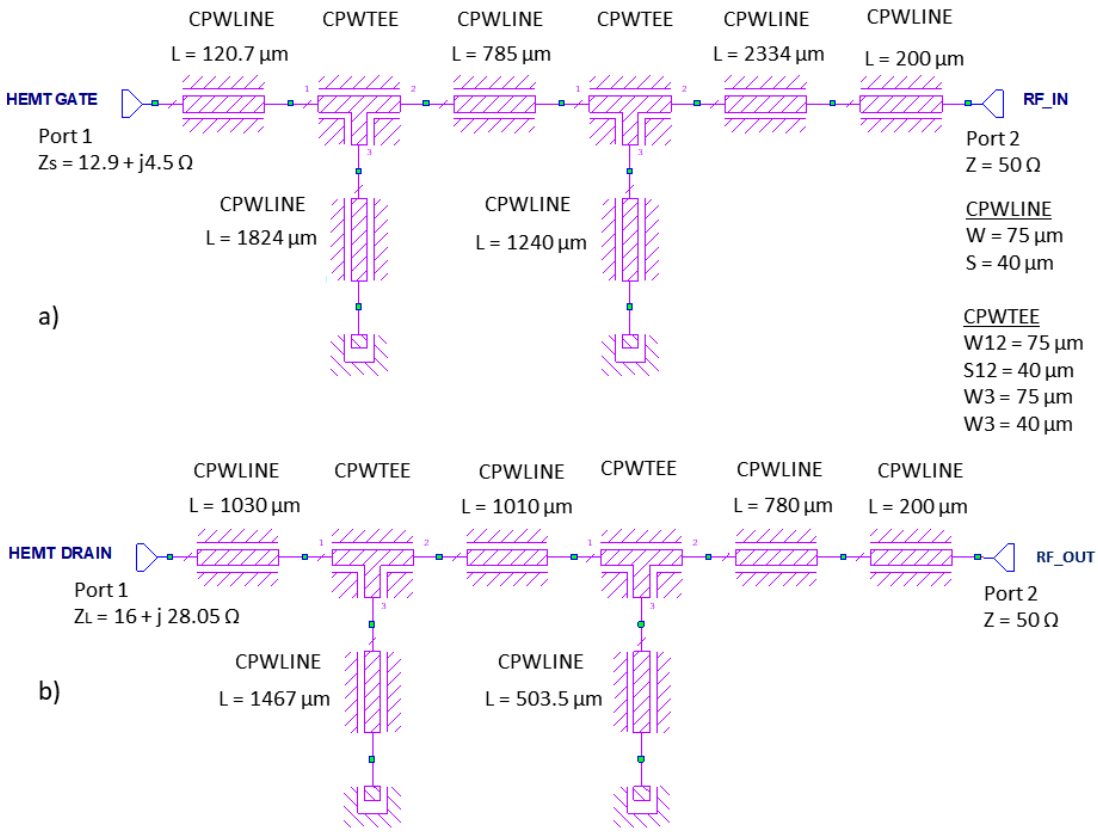


Figure 7.7 Schematic of the designed a) input and b) output matching networks for amplifier A.

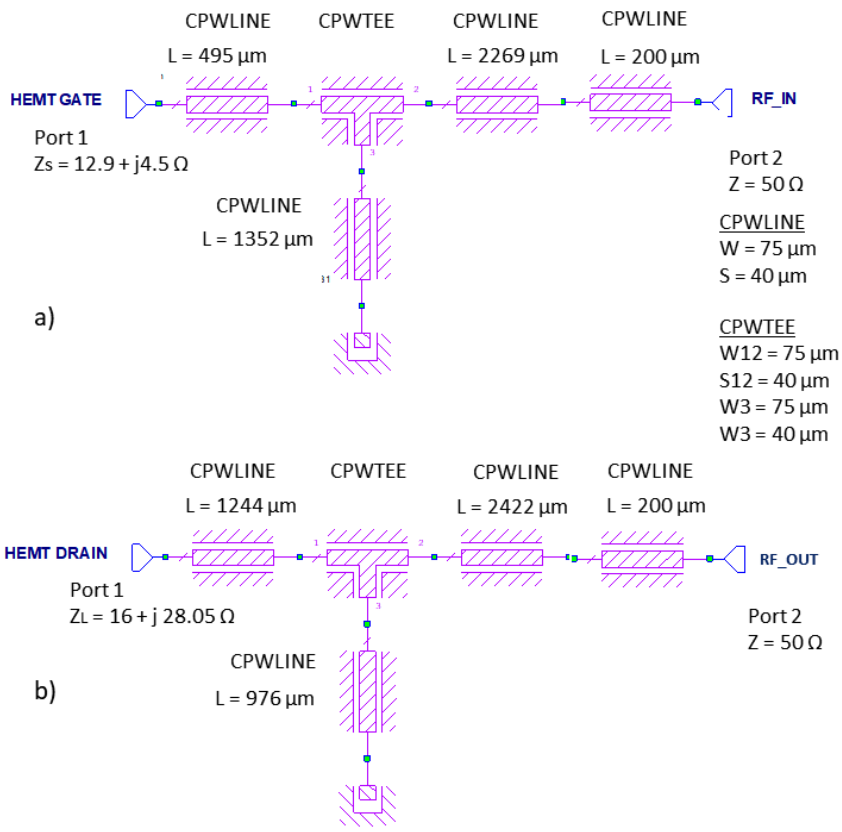


Figure 7.8 Schematic of the designed a) input and b) output matching networks for amplifier B.

Here the T-junctions of the transmission lines require air-bridges so that the ground planes at any given point have no potential difference. Therefore the matching network design has to include the air-bridges. Fabrication of these air-bridges is discussed in the chapter 4. The design parameters of the T-juncions were set as follows

- Signal line width at all three sides W12 and W3 was set to 75 µm
- Gap between the ground and signal line at all 3 sides S12 was set to 40 µm
- Airbridge height was set to 3 µm
- Airbridge width Wab was set to 40 µm

Detailed CPW T-junction simulation setup and a shematic illustration of it is shown in Figure 7.9.

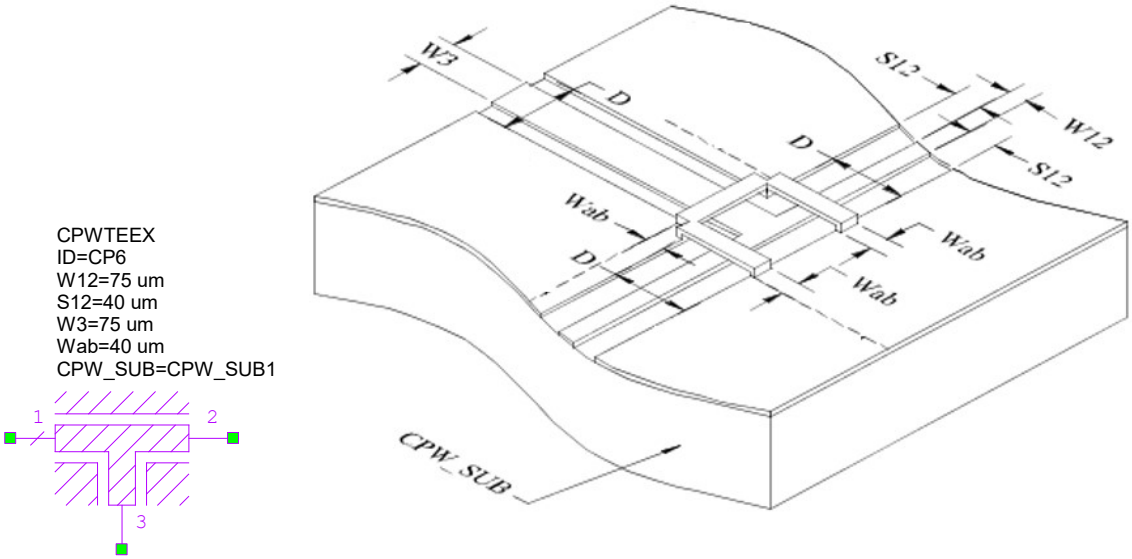


Figure 7.9 Schematic of CPW T-junction setup used in the matching network design.

Once the design has been finished, both matching networks can be transformed into a GDS file that represents the layout of these networks that is transferred onto a photomask for fabrication. The finalised layouts for amplifier A is shown in Figure 7.10. Simulated S-parameter data is plotted together with measurment results and is described in section7.8.

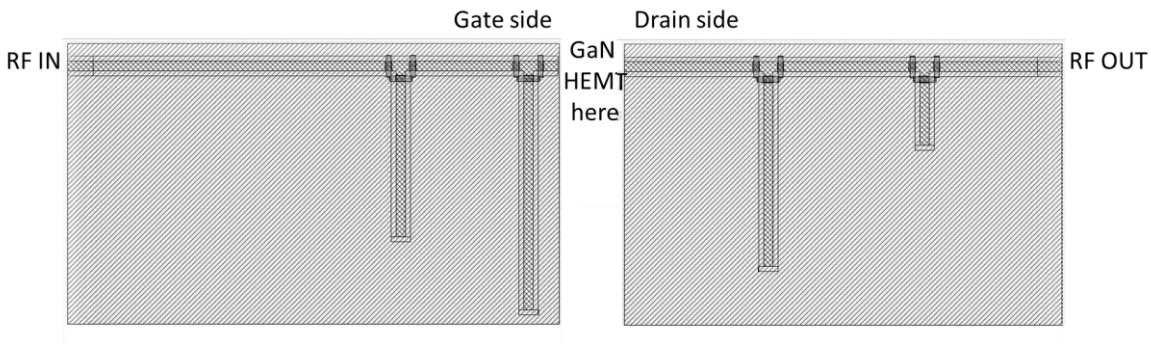


Figure 7.10 Layout of the design matching networks.

7.8 Experimental results

The designed amplifier MMICs were fabricated using the fabrication processes detailed in Appendix A. Two different matching circuits were employed: amplifier A and B. Both circuits employed only transmission lines for matching and were fabricated simultaneously on the same sample. Here coplanar waveguides were chosen due to the fact that they do not require any backside processing. An Optical image of the fabricated amplifier A with matching circuit design form Figure 7. 11 is shown in Figure 7. 12.

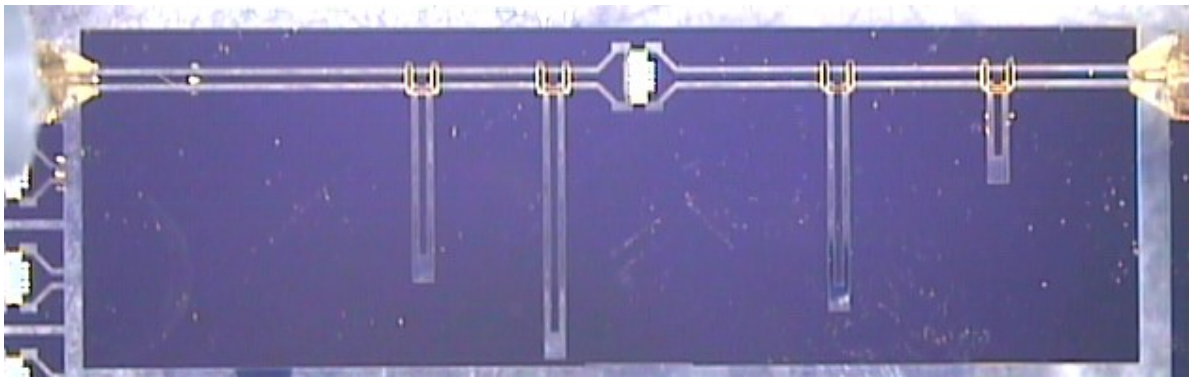


Figure 7. 11 Optical image of a fabricated amplifier A.

In a similar way to the design in Figure 7.10, a design with just one stub on each matching network side the amplifier B was designed, fabricated and is shown in Figure 7. 12.

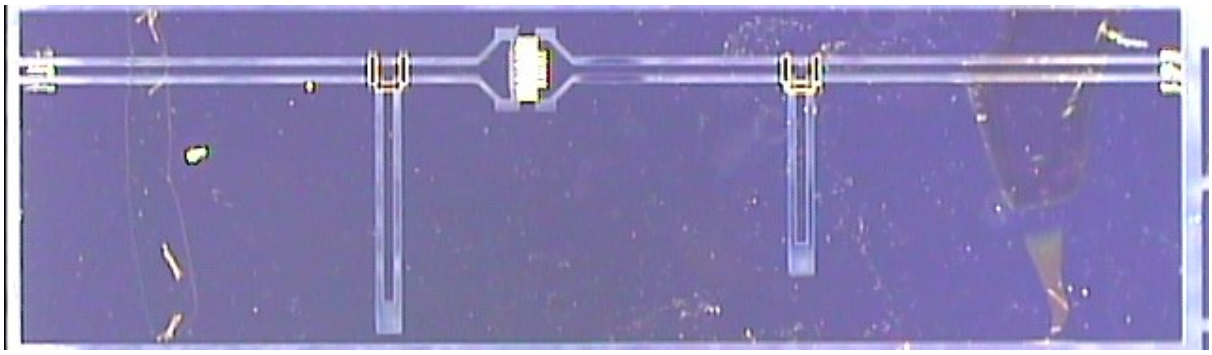


Figure 7. 12 Optical image of a fabricated amplifier B.

The simulated and measured S-parameter data shown in Figure 7.13 and Figure 7.14 for amplifiers A and B, respectively. Amplifier A shows measured gain of at least 8 dB with input and output return losses better than 5 dB over 4 GHz bandwidth from 9 to 13 GHz. Amplifier B shows measured gain of at least 8 dB with input and output return losses better than 5 dB over 3 GHz bandwidth from 12 to 15 GHz. Peak small signal performance with gain of 10 dB with input and output return losses below 10 dB is measured at 10 GHz for Amplifier A. Peak small signal performance for amplifier B is measured at 13 GHz with gain of 9 dB and input and out return losses below 15 dB. The results show that having one stub in input/output matching network leads to narrower bandwidth but lower input and

output return losses compared with having two stubs on each matching network. Note though that the designed amplifier small signal performance doesn't exactly match the fabricated and measured results. This discrepancy comes from the variations between different fabrication runs, for example, poorer isolation on the second sample of 214 nA/mm compared to 31 nA/mm at V_D = -10 V on the devices used for the design, which leads to higher losses. These losses cause a reduction in the peak of transconductance g_m, for example at V_D = 5 V it reduces from 215 mS/mm to 200 mS/mm between the two samples and this then translates to amplifiers as well. The measured small signal gain (S_{21}) in both amplifier designs is also lower than designed values, see Figure 7.13 and Figure 7.14 for amplifier A and B, respectively. Ohmic contact resistances on both fabricated samples are the same of 0.45±0.04 Ω·mm, therefore it is assumed that there is no variation of device performance that could be caused by variation in the Ohmic contacts. Figure 7. 15 shows the input and output reflection coefficients S_{11} and S_{22} of the measured results from transistors on the two samples. There is no significant difference in the S_{11} parameter (input reflection coefficient) between the two samples and therefore the measured input reflection coefficient for amplifiers A and B are close to the modelled data. However, there is a significant difference in the S_{22} parameters between these transistors on the two samples, which lead to shift in the output reflection coefficients in the measured S-parameter data on amplifiers A and B.

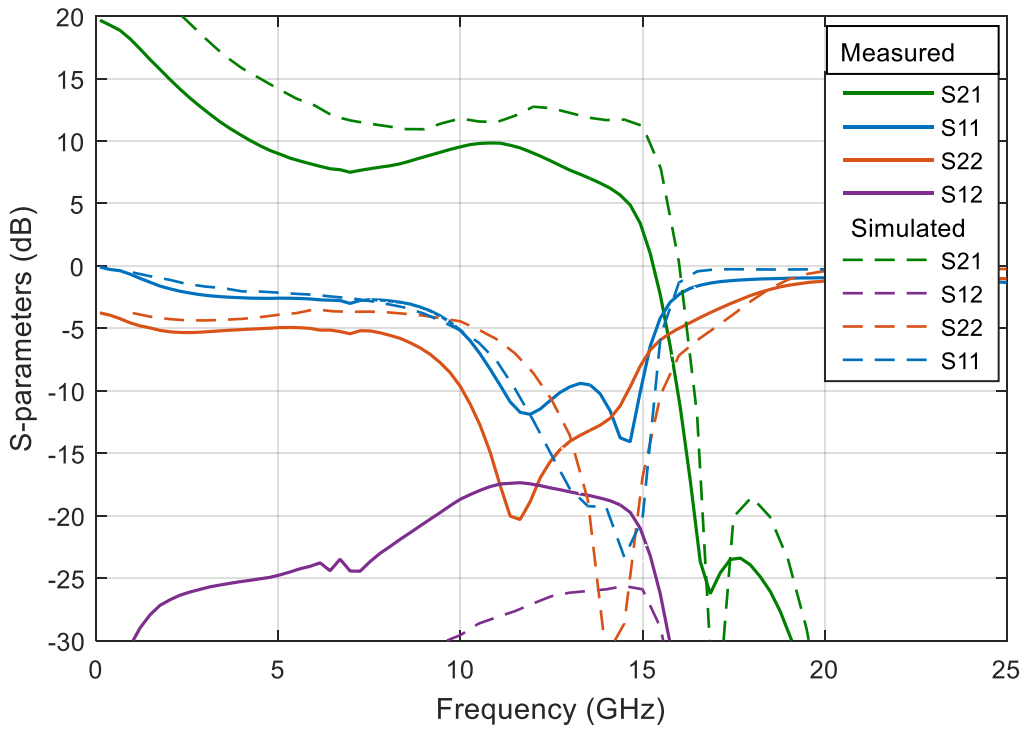


Figure 7.13 S-parameter measurement results and simulated data of the fabricated amplifier A at V_G = -3 V and V_D = 25 V.

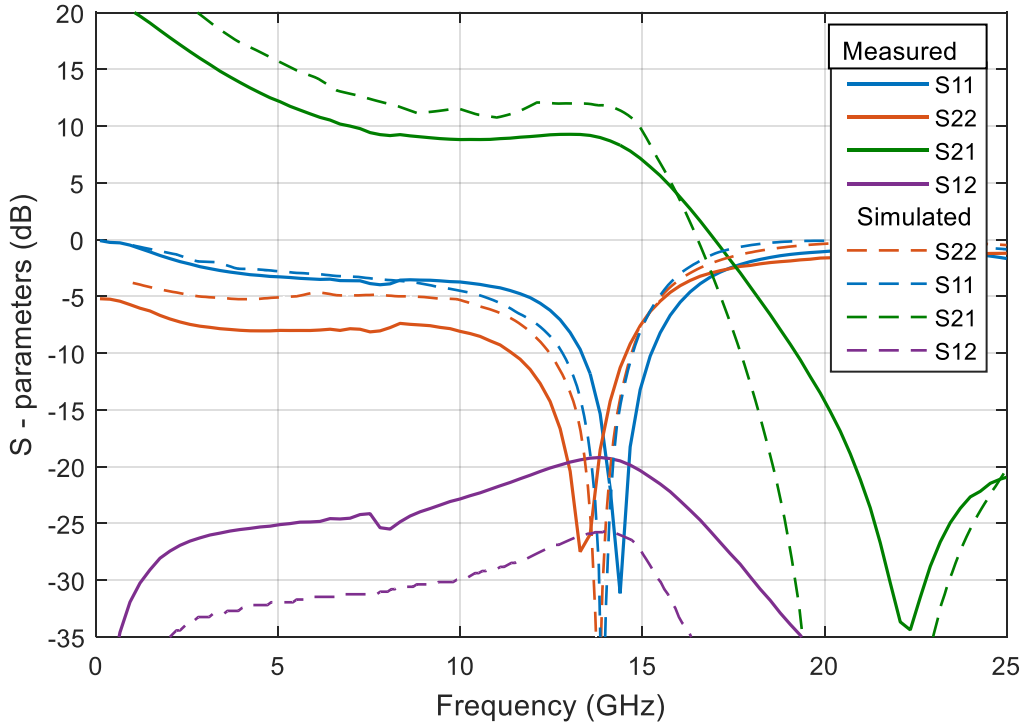


Figure 7.14 S-parameter measurement results and simulated data of a fabricated amplifier B at V_G = -3 V and V_D = 25 V.

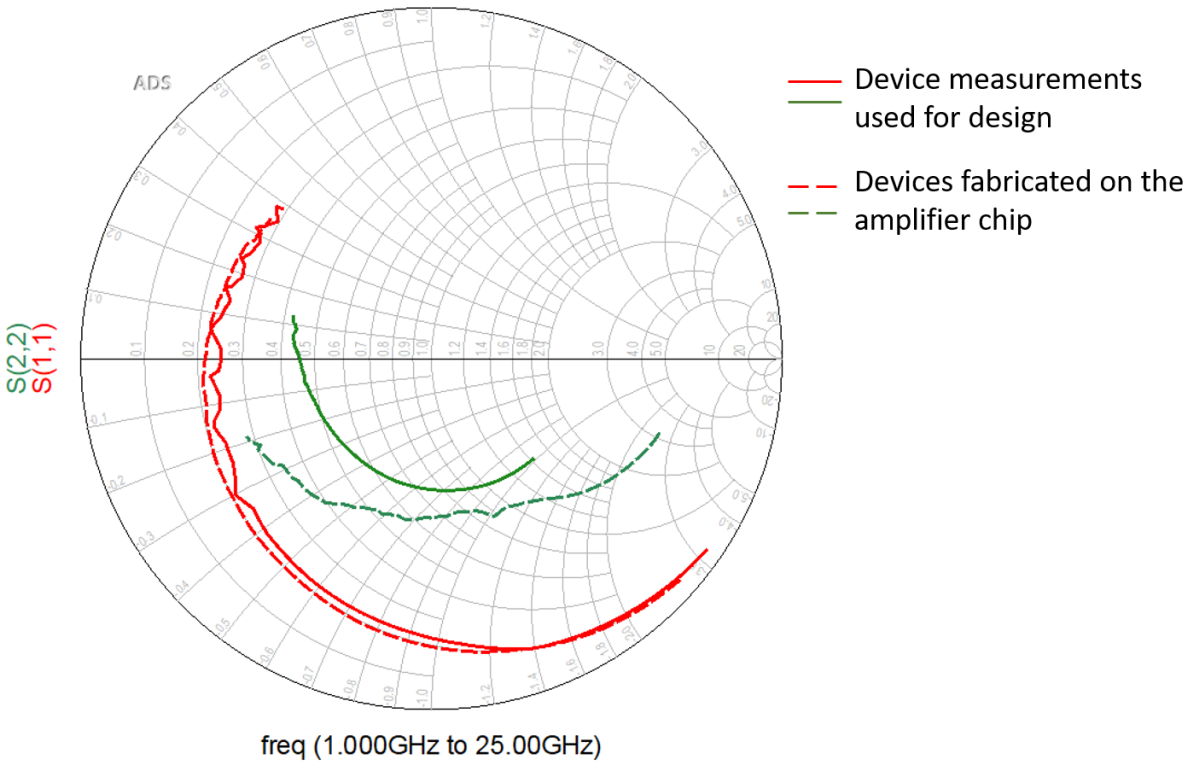


Figure 7. 15 Input and output reflection coefficients of the transistors used for matching network design and the transistors in the fabricated amplifiers A and B.

Both amplifiers were then measured with a synthesized sweep signal generator Wiltron 6818B which can generate RF signals up 20 dBm and the output power was measured with Agilent PSA Series Spectrum Analyzer E4448A. Amplifiers were biased with Agilent

B2902A Precision Source/Measure unit. Schematic illustration of the measurement setup is given in Figure 7. 16 . Any losses in the cabling/measurement setup are taken into account by adding the measured the output power for each input power/frequency combination substituting device under test (DUT) with a 2 µm long CPW line (THRU line of a calibration kit on alumina substrate also used in Chapter 3).

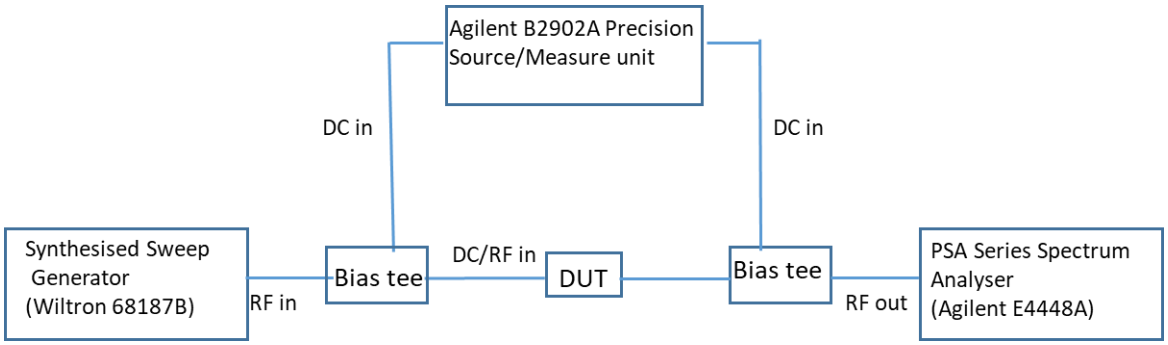


Figure 7. 16 Schematic illustration of the measurement setup.

The measured output power with associated power added efficiency and gain at a drain voltage V_D = 20V , gate voltage V_G = -3V over 8 to15 GHz frequency range with input RF power of 12 dBm are shown in Figure 7.17 and Figure 7.18 for amplifier A and B respectively. Amplifier A exhibited peak power of 30 dBm at 10 GHz with associated PAE of 45%. It has gain of at least 9.4 dB from 8 to 13 GHz. Amplifier B exhibits peak power of 29.6 dBm, gain of 9.6 dB at 13 GHz with PAE of 27%. Amplifier A exhibits higher PAE of over 36% over the 9-12 GHz frequencies while amplifier B has PAE below 27.5% over the same frequencies. Power added efficiency was calculated using equation 8.1.

$$PAE = \frac{P_{RFout} - P_{RFin}}{P_{DC}} \tag{7.9}$$

where P_{RFout} is the output RF power, P_{RFin} is the input RF power and P_{DC} is the dissipated DC power.

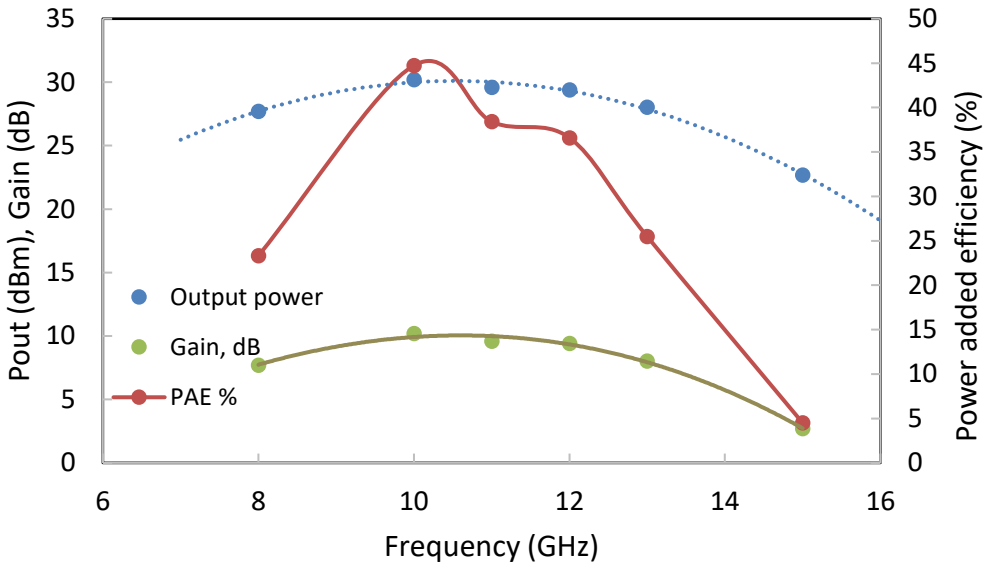


Figure 7.17 Measured output power versus frequency of Amplifier A at drain voltage of 20V, gate voltage of -3 V and RF input power of 12 dBm.

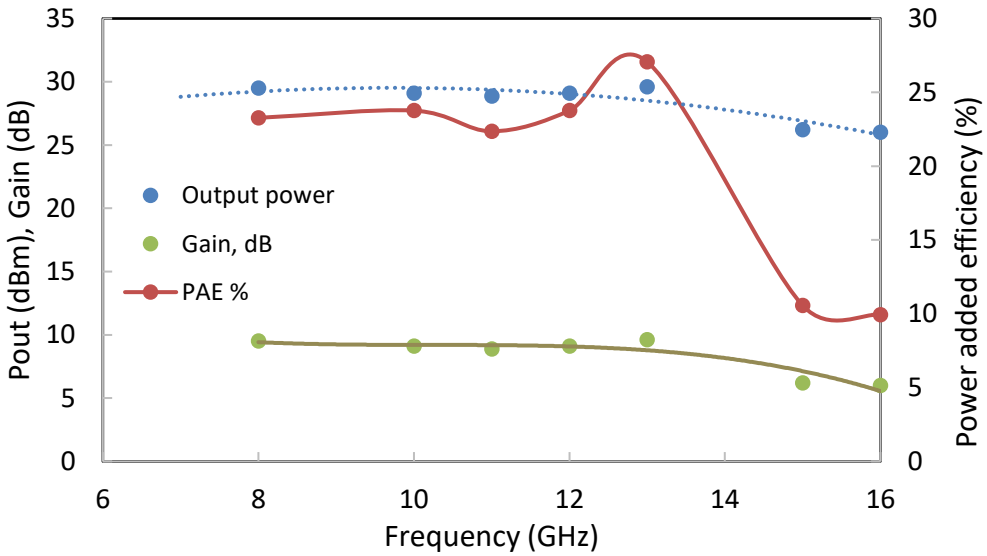


Figure 7.18 Measured output power versus frequency of Amplifier B at drain voltage of 20 V, gate voltage of -3 V and RF input power of 12 dBm.

Same characteristics are measured versus input power from -8 dBm to 12 dBm are shown in Figure 7. 19 and Figure 7. 20 for Amplifiers A and B at 10 and 13 GHz respectively. Frequencies of 10 and 13 GHz are chosen since amplifier A exhibits peak power at 10 GHz and Amplifier B exhibits peak power at 13 GHz. It is observed that a constant gain of at least 9.4 dB at 10 GHz and 8 dB at 13 GHz at is maintained over input powers of -8 to 12 dBm for Amplifier A. Similarly constant gain of at least 7 dB at 10 GHz and 9 dB at 13 GHz is maintained from -8 dBm to 12 dBm input power for amplifier B. Gain compression is not

observed up to 12 dBm for both amplifiers at neither 10 GHz nor 13 GHz but is expected to happen above 12 dBm input power, but cannot be experimentally measured duo to the limitation of 20 dBm of the generated signal power of the used signal generator with measured cabling losses of 8 dBm and 9dBm at 10 and 13 GHs respectively. At 10 GHz amplifier A has by 2-3 dB higher gain across the measured input power levels with significantly higher associated PAE but at 13 GHz amplifier B exhibits by 2 dB higher gain across the measured input power levels however there is no significant difference in the associated PAE between the two amplifiers.

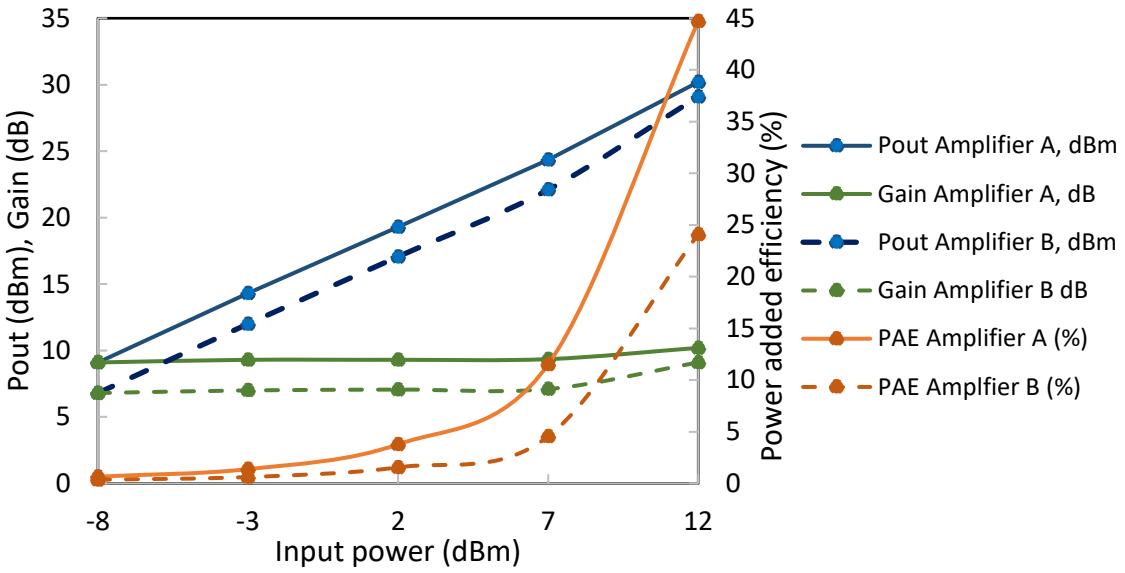


Figure 7. 19 Measured output power, gain and obtained power added efficiency for amplifier A (solid lines) and B (dashed lines) at 10 GHz.

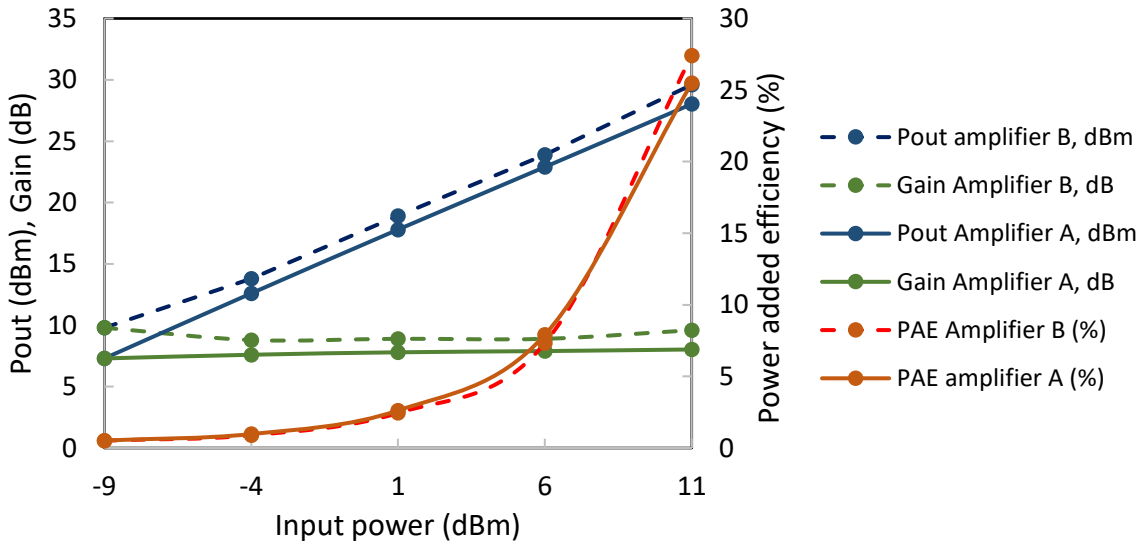


Figure 7. 20 Measured output power, gain and obtained power added efficiency for amplifier A (solid lines) and B (dashed lines) at 13 GHz.

7.9 Summary

The process of a single stage class A amplifier design, realisation and measurements were described in this chapter. Two different amplifier designs using coplanar waveguide transmission lines were successfully fabricated and characterised showing small signal gain of at least 5 dB up to 15 GHz. It is seen that employing double stub design in input and output matching networks leads higher amplifier bandwidth but also higher input and output reflection coefficients than matching networks with just one stub. Double stub amplifier was measured to have peak output power of 30 dBm with gain of 10 dB at 10 GHz with associated PAE of 45% measured with 12 dBm input power. Double stub design is found to have higher gain of at least 9.4 dB and PAE of at least 25% over 8 to 13 GHz bandwidth than single stub design.

This chapter has outlined the design procedure for a typical GaN HEMT class-A amplifier circuit, both using S-parameters and/or using the device output characteristics. The basic building blocks of a single stage amplifier design such as input and output matching network design and bias network design have also been discussed. A table representing the state-of-the-art parameters of discrete GaN HEMTs and MMICs used for X-band applications was presented with a discussion of the underpinning device technology. The main limitation with the current GaN HEMT MMIC amplifiers is thermal management which comes from the device self-heating. Possible solutions to the device self-heating that could lead to better amplifier performance once these devices are integrated into circuits are discussed in Chapters 5 and 6.

8. Conclusions and Future work

The superior properties of GaN HEMTs such as high 2DEG sheet carrier density and mobility, and high breakdown fields make them very promising for future RF and power applications. However, as demands for higher frequencies and power densities combined with smaller and smaller chip sizes are higher than before device self-heating becomes an important challenge. The work done in this thesis has contributed to the two main challenges with the current GaN HEMT technology: thermal management and current collapse.

8.1. Key results

The main results of this thesis are summarised below.

1) Reduction in current collapse was demonstrated for unpassivated devices by using 70 nm thick GaN cap layer. Surface effects that because significant current collapse were reduced using this approach, and thereby demonstrating an alternative route to device passivation. Unpassivated buried channel devices presented in this thesis showed high off-state breakdown voltages over 200 V for 2 µm gate-length devices compared to around 100 V for conventional devices. From pulsed IV measurements, the results also showed that unpassivated buried channel devices exhibited significantly lower current collapse compared with conventional devices. However, it was observed that the use of 70 nm GaN cap increased the gate leakage currents, but through a post gate annealing process the gate leakage currents were reduced from 218 µA/mm down to 3.74 µA/mm at -20 V gate bias.
2) The impact of material growth on device DC characteristics was studied by comparing devices fabricated from a GaN epitaxial structure grown by hot wall MOCVD growth and standard MOCVD. It was observed that hot wall MOCVD growth leads to better quality GaN HEMT epitaxial layers with less associated thermal boundary resistance which then lead to better thermal dissipation to the substrate and better device performance. Devices from two commercially supplied wafers were compared and the degradation in current with increasing drain voltage up of 20 V of hot wall MOCVD grown wafer was found to be 15% with $I_{DMAX} = 0.6$ A/mm whereas on the standard wafer it is found to be 19% with $I_{DMAX} = 0.52$ A/mm for 2µm gate length devices. The hot-wall MOCVD grown structure which has higher Al composition exhibited much larger leakage currents ~100 µA/mm compared to 7µA/mm for the standard wafer, and an order of 2 higher on-off ratio than standard structure. We note, though, that since the wafers used in this study did not have exactly the same epilayer structure the obtained

results are only indicative and more work would need to be done to obtain definitive results.

3) From simulation work, it was observed that the peak channel temperature can be reduced by 30 °C by using a distributed device channel. In Chapter 6 a planar distributed device technology realised using using oxygen plasma treatment was presented and led to low leakage currents of under 200nA/mm. Moreover no degradation in the leakage currents was observed for distributed channel devices which is an improvement compared to the previously reported distributed gate designs. Even though the distributed channel devices have almost double the device width due to the inactive regions introduced in the device, the measured device DC output characteristics showed higher saturated drain currents compared to a standard device. Fabricated devices exhibited no degradation in the current gain cut off frequency f_T at 25V and are expected to have longer lifetime compared to standard devices due to the lower operational temperature.
4) Two different small signal class A amplifier designs were studied and showed small signal gain of at least 8 dB up to 14 GHz. Amplifiers employing the double stub impedance matching design exhibited peak power of 30 dBm at 10 GHz with associated PAE of 44% and gain of 10 dB, while the single stub design exhibited peak power of 29.6 dBm at 13 GHz with PAE of 27% and gain of 9.6 dB. Also, the double sub design led to a wider bandwidth of 6 GHz with gain of at least 6 dB compared to 4 GHz with gain of at least 6 dB for single stub design.

8.2. Future work

Each of the separate aspects studied in this thesis brings an improvement to GaN HEMT device performance and therefore a combination of some of the proposed device concepts could significantly improve device performance. Nonetheless, further investigations are needed for some of the device concepts studied in this thesis.

First, deep channel and distributed gate/channel devices realised on wafers grown by hot-wall MOCVD growth could significantly advance the state of the art GaN HEMT technology by exploiting the both the advantages of the device architectures and this growth method. However, the impact of the 2-dimensional hole gas or a secondary channel between the AlGaN barrier layer and thick GaN cap in a deeply buried channel HEMT device was not studied in this thesis. Analysis of the effects of this secondary channel on device performance such as RF characteristics and trapping effects is required. Even though it has been shown that employment of 70nm undoped GaN cap decreases the current collapse in an unpassivated GaN HEMT, current collapse was not removed completely so effects of adding

passivation layer to this structure and its impacts should be studied for further insight. In addition, significant self-heating effects were observed in this structure, therefore thermal management solutions also need to be applied to the proposed thick capped device structure. This could, for instance, involve the use of this epitaxial layer structure with a GaN-on-diamond substrate [47].

Secondly, deeper analysis of the thermal characteristics of both distributed gate/channel design and device epitaxial layer structure grown by hot-wall MOCVD material growth are required. Channel temperature measurements of these devices are needed to quantify the improvements towards with regards to device self-heating effects. As there is no direct temperature measurement within a device channel, a common approach is to measure the device surface temperature and then to use simulations to estimate the channel temperature [180]. Other approaches to obtain channel temperature of GaN devices include using infra-red (IR) microscopy [181], micro-Raman microscopy [182] or thermoreflectance measurements [183]. In addition to channel temperature measurements, measurement of the thermal boundary resistance for the structure grown by hot-wall MOCVD growth method is needed to quantify improvements in channel temperature attributed to enhanced heat dissipation within the wafer epilayers.

Thirdly, reliability testing of the proposed technology is needed to establish whether it could be used in commercial devices. Such testing would include constant device operation at CW/pulsed conditions to evaluate device lifetime and whether or not there is any performance degrading over time. As alluded to in the thesis, a higher voltage design and current collapse-free GaN HEMT technology could be developed. Further, device fabrication processes could be improved to reduce the gate leakage currents and Ohmic contact resistances. For instance, improved processing steps can be executed on a wafer with 70 nm thick GaN cap layer to mitigate the current collapse further and increase the breakdown voltage above 200 V which will allow for high operating voltage above 100 V. Further, Ohmic contact resistances can be brought down by using re-grown Ohmic technology [84].

Finally, the proposed device technology can be used for the realisation of high-performance microwave amplifiers. Moreover, amplifier efficiency can be improved by improving the circuit design, incorporating multiple amplification stages and optimising all the passive components used for the design.

In summary, this project has delivered basic transistor design and fabrication processes that can enable the implementation of highly efficient practical amplifiers for applications in communications systems.

Appendix A

GaN HEMT fabrication processes using photolithography

1) Sample cleaning

- Dip in acetone for 3minutes using ultrasonic bath
- Dip in methanol for 3minutes using ultrasonic bath
- Dip in Isopropyl Alcohol (IPA) for 3minutes using ultrasonic bath
- Blow dry using N_2

2) Ohmic contact deposition

- Spin LOR 10A at 6000rpm for 30seconds
- Bake at 150ºC for 2 minutes
- Spin S1805 at 4000 rpm for 30seconds
- Bake at 115ºC 3 for minutes
- Expose in the MA6 mask aligner using hard contact for 2.3 seconds
- Develop using MF319 for 2 minutes
- Rinse in reverse osmosis (RO) water
- Blow dry with N_2
- Ash at 110W for 1 minute
- Use Ar gun for 30 seconds in the Plassys IV
- Metalize Ti/Al/Ni/Au 30/180/40/100nm
- Liftoff using 1165 resist stripper in the hot water bath for 15 minutes, pipette clean
- Rinse with water
- Blow dry with N_2
- Anneal in N_2 at 800C for 30 seconds

3) Mesa isolation

- Spin S1818 at 4000rpm for 30 seconds
- Bake at 115ºC for 2 minutes
- Expose in the MA6 using hard contact for 3.8 seconds
- Develop using MF319 for 75 seconds
- Rinse with RO water
- Blow dry with N_2

- Use BP80 with O_2 with 20sccm and power of 200W at 20mT for 5minutes
- Remove resist using Acetone
- Dip in IPA
- Blow dry with N_2

4) Gate contact deposition

- Spin LOR 10A at 6000rpm for 30seconds
- Bake at 150ºC for 2 minutes
- Spin S1805 at 4000 rpm for 30seconds
- Bake at 115ºC 3 for minutes
- Expose in the MA6 mask aligner using hard contact for 2.3 seconds
- Develop using MF319 for 2 minutes
- Rinse in RO water
- Blow dry with N2
- Ash at 110W for 1 minute
- Metalize Ni/Au 20/200nm
- Liftoff using 1165 resist stripper in the hot water bath for 15 minutes, pipette clean
- Rinse with RO water
- Blow dry with N_2

5) Bond pad deposition

- Spin LOR 10A at 6000rpm for 30seconds
- Bake at 150ºC for 2 minutes
- Spin S1805 at 4000 rpm for 30seconds
- Bake at 115ºC for 3 minutes
- Expose in the MA6 mask aligner using hard contact for 2.3 seconds
- Develop using MF319 for 2 minutes
- Rinse in RO water
- Blow dry with N_2
- Ash at 110W for 1 minute
- Metalize Ni/Au 20/200nm
- Liftoff using 1165 resist stripper in the hot water bath for 15 minutes, pipette clean
- Rinse with RO water

- Blow dry with N_2

6) Surface passivation

- Deposit 10nm of Si_3N_4 using ICP 180 Deposition tool

7) Air-bridge fabrication

- Spin S1828 at 3000rpm for 30 seconds
- Bake at 115ºC for 3 minutes
- Expose in the MA6 using hard contact for 12 seconds
- Develop using Microdeposit developer concentrate 1:1 water for 75 seconds
- Rinse with RO water
- Blow dry with N_2
- Ash 3 min at 110 W
- Bake at 115ºC for 10 minutes
- Deposit seed layer Ti/Au 20/20 nm
- Spin S1828 at 4000 rpm for 30 seconds
- Bake at 115ºC for 3 minutes
- Expose in the MA6 using hard contact for 12 seconds (whole bridge area)
- Expose in the MA6 using hard contact for 12 seconds (bridge post area)
- Develop using Microdeposit developer concentrate 1:1 water for 75 seconds
- Rinse with RO water
- Blow dry with N_2
- Ash 3 min at 110 W
- Electroplate 2 µm of Au
- Remove top resist using Acetone
- Dip in IPA
- Blow dry with N_2
- Use gold etch solution for 30 seconds
- Rinse with RO water
- Blow dry with N_2
- Remove bottom resist using Acetone
- Dip in IPA
- Blow dry with N_2

Fabrication using E-Beam lithography

8) Sample cleaning

- Dip in acetone for 3minutes using ultrasonic bath
- Dip in methanol for 3minutes using ultrasonic bath
- Dip in Isopropyl Alcohol (IPA) for 3minutes using ultrasonic bath
- Blow dry using N_2

9) E-beam markers

- Spin 12% 2010 PMMA at 5000rpm for 60 seconds
- Bake at 155ºC for 2 minutes
- Spin 4% 2041 at 5000 rpm for 60 seconds
- Bake at 155ºC for 2 minutes
- Expose at VB6 with dose of 700, with current 32 nA, resolution of 25
- Develop in MIBK:IPA 2.5:1 for 60 seconds at 23C
- Dip in IPA
- Rinse with RO water
- Blow dry with N_2
- Metalize Ti/Pl 20/80nm
- Liftoff in warm acetone for 15min, pipette clean
- Dip in IPA
- Blow dry wih N_2

10) Ohmic contact formation

- Spin 12% 2010 PMMA at 5000rpm for 60 seconds
- Bake at 155ºC for 2 minutes
- Spin 4% 2041 at 5000 rpm for 60 seconds
- Bake at 155ºC for 2 minutes
- Expose in VB6 tool with dose of 700, with current 32 nA, resolution of 25
- Develop in MIBK:IPA 2.5:1 for 60 seconds at 23C
- Dip in IPA
- Rinse with RO water
- Blow dry with N_2
- Use Ar gun in Plassys IV for 30 seconds
- Metalize Ti/Al/Ni/Au 30/180/40/100nm

- Liftoff in warm acetone for 30 minutes, pipette clean
- Dip in IPA
- Blow dry wih N_2
- Anneal at 800C for 30 seconds

11) Mesa isolation

- Spin 15% 2010 PMMA at 4000rpm for 60 seconds
- Bake at 155ºC for 2 minutes
- Expose in VB6 tool with dose of 800, beam current of 64nA and resolution of 25
- Use dry etch machine System 100RIE T-gate with 25sccm of $SiCl_4$ at power 75W at 8mT for 5min
- Remove resist in warm acetone for 30 minutes, pipette clean
- Dip in IPA
- Blow dry with N_2

12) T-gate fabrication

- Spin 4% 2041 PMMA at 5000rpm for 60 seconds
- Bake at 155ºC for 90 seconds
- Spin 4% 2041 PMMA at 5000rpm for 60 seconds
- Bake at 155ºC for 90 seconds
- Evaporate 10nm of Al discharge layer
- Spin 8% 2010 PMMA at 5000rpm for 60 seconds
- Bake at 155ºC for 90 seconds
- Spin 8% 2010 PMMA at 5000rpm for 60 seconds
- Bake at 155ºC for 90 seconds
- Spin 2.5% 2041 PMMA at 5000rpm for 60 seconds
- Bake at 155ºC for 90 seconds
- Evaporate 10nm of Al discharge layer
- Expose in VB6 tool with:

  Gate foot exposed with dose of 800, beam current of 4nA, resolution of 4

  Gate head exposed with dose of 430, beam current of 8nA, resolution of 10
- Dip in CD-26 for 2 minutes
- Rinse with RO water for 60 seconds
- Blow dry with N_2

- Develop in MIBK:IPA for 40 seconds at 23 ºC
- Dip in IPA
- Blow dry with N_2
- Dip in CD-26 for 90 seconds
- Rinse with RO water for 60 seconds
- Blow dry with N_2
- Develop with MIBK:IPA for 40 seconds at 23ºC
- Dip in IPA
- Blow dry with N_2
- Metalize Ni/Au 20/400 nm
- Liftoff in warm acetone for 2 hours, pipette clean
- Dip in IPA
- Blow dry with N_2

13) Si_3N_4 patterning

- Spin 15% 2010 PMMA at 5000 rpm for 60s
- Bake in the 180ºC oven for 2 hours
- Spin 15% 2010 PMMA at 5000 rpm for 60s
- Bake in the 180ºC oven for 2 hours
- Expose in VB6 tool with dose of 1000, beam current of 64nAm, resolution of 25
- Develop in MIBK:IPA 2.5:1 for 60 seconds at 23ºC
- Dip in IPA
- Blow dry with N_2
- Use dry etch tool System RIE T-gate with 25/50 sccm of SF_6/N_2 with power of 18W at 15mT pressure for 15 minutes
- Remove resist using warm acetone for 1 hour, pipette clean
- Dip in IPA
- Blow dry with N_2

14) Bond pad metallisation

- Spin 12% 2010 PMMA at 5000rpm for 60 seconds
- Bake at 155ºC for 2 minutes
- Spin 4% 2041 at 5000 rpm for 60 seconds
- Bake at 155ºC for 2 minutes

- Expose in VB6 tool with dose of 700, with current 64 nA, resolution of 25
- Develop in MIBK:IPA 2.5:1 for 60 seconds at 23ºC
- Dip in IPA
- Rinse with RO water
- Blow dry with N_2
- Metalize Ti /Au 20/400 nm
- Liftoff in warm acetone for 15 min, pipette clean
- Dip in IPA
- Blow dry with N_2

Appendix B

Capacitance-voltage measurements

Capacitance-voltage measurements can be used to evaluate fabrication processes and determine semiconductor material properties such as apparent carrier density and sheet carrier concentration.

Capacitance-voltage measurements rely on the principle that the width of the depleted space-charge region w in the semiconductor depends on the applied voltage. Capacitance can be defined as change in the semiconductor charge by change in the applied voltage, where voltage is the superposition of a small ac voltage v_{ac} and the reverse DC voltage V. The amplitude of the ac voltage at 1MHz is typically 10 to 20 mV which is used for further data analysis in chapter 6 [181]. If 2DEG is considered as a conductive plane that is connected to the Ohmic contact and there is zero external bias applied, we can regard the depletion region as being in touch with the 2DEG due to built-in voltage V_{bi}. Then the capacitance across the depletion space charge is given by [181]:

$$C = A \cdot \frac{dQ}{dV} = A\frac{\varepsilon_0 \varepsilon_s}{w} \tag{B.1}$$

where Q is the semiconductor charge, A, ε_s, ε_0, w are the area of Schottky barrier, relative dielectric constant, vacuum permittivity and depletion width respectively.

Assuming that the depletion approximation is valid, i.e. the 2DEG density is negligible in the depleted space-charge region and all carriers are fully ionised in the buffer one can express the apparent carrier concentration as [182].

$$N_D = -\frac{C^3}{q\varepsilon_s\varepsilon_0 A^2 \frac{dC}{dV}} = \frac{2}{q\varepsilon_s\varepsilon_0 A^2 \frac{d\left(\frac{1}{C^2}\right)}{dV}} \tag{B.2}$$

where q is the elementary electron charge. The depletion width is further given by:

$$w = \sqrt{\frac{2\varepsilon_s\varepsilon_0}{qN_D}(V_{bi} - V)} \tag{B.3}$$

where V_{bi} is the built-in voltage of the Schottky contact and V is the external voltage applied to the contact. An example of the capacitance-voltage measurement plot of a Schottky diode is shown in Figure B.1. Here for V = 0 V, the 2DEG with its high sheet carrier concentration acts as an equipotential plane. With this condition, the device capacitance reduces to the capacitance of a parallel plate capacitor of area, a, delimited by the Schottky contact and the underlying 2DEG This capacitance is given by equation B.1 If

increasing negative voltage is applied to this diode, the 2DEG below the Schottky contact gradually depletes from mobile carriers and the capacitance remains nearly constant, until the 2DEG underneath the contact fully depletes. This last condition causes the sharp decrease of the capacitance observed at the pinch off voltage. For V below the pinch off voltage, the depletion zone extends laterally, in between the electrodes, giving rise to a fringe capacitance, which is much smaller than the initial Schottky capacitance.

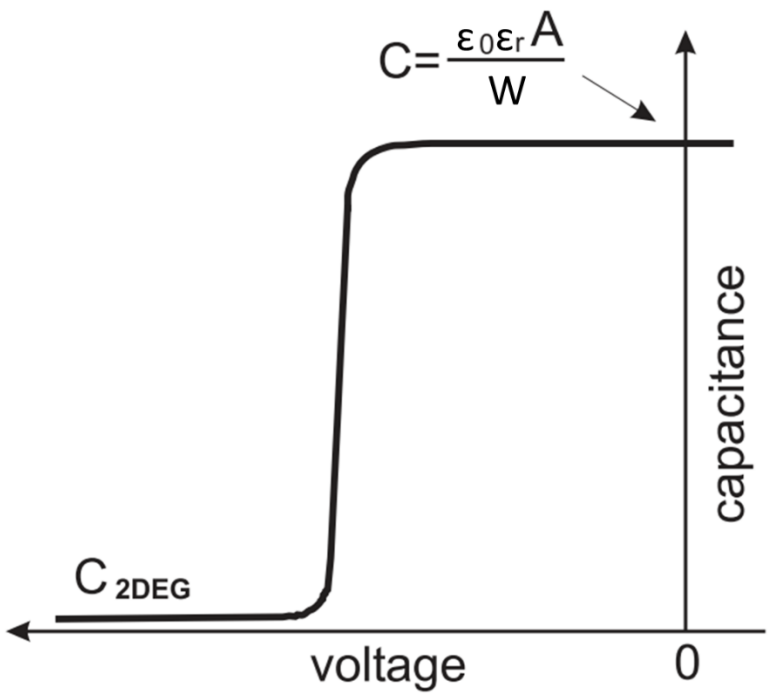


Figure B.1 Example capacitance voltage characteristics for a Schottky diode with 2DEG.

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