Power Management Systems based on Switched-Capacitor DC-DC Converter for Low-Power Wearable applications

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Declaration of Originality

I hereby declare that this thesis was composed and originated entirely by myself, that the work contained herein is my own except where explicitly stated otherwise in the text, and that this work has not been submitted for any other degree or professional qualifications.

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April 2021

Minor correction at July 2021

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ABSTRACT

The highly efficient ultra-low-power management unit is essential in powering low-power wearable electronics. Such devices are powered by a single input source, either by a battery or with the help of a renewable energy source. Thus, there is a demand for an energy conversion unit, in this case, a DC-DC converter, which can perform either step-up or step-down conversions to provide the required voltage at the load. Energy scavenging with a boost converter is an intriguing choice since it removes the necessity of bulky batteries and considerably extends the battery life.

Wearable devices are typically powered by a monolithic battery. The commonly available battery such as Alkaline or Lithium-ion, degrade over time due to their life spans as it is limited by the number of charge cycles- which depend highly on the environmental and loading condition. Thus, once it reaches the maximum number of life cycles, the battery needs to be replaced. The operation of the wearable devices is limited by usable duration, which depends on the energy density of the battery. Once the stored energy is depleted, the operation of wearable devices is also affected, and hence it needs to be recharged. The energy harvesters- which gather the available energy from the surroundings, however, have no limitation on operating life. The application can become battery-less given that harvestable energy is sufficiently powering the low-power devices. Although the energy harvester may not completely replace the battery source, it ensures the maximum duration of use and assists to become autonomous and self-sustain devices.

The photovoltaic (*PV*) cell is a promising candidate as a hypothetical input supply source among the energy harvesters due to its smaller area and high power density over other harvesters. Solar energy use *PV* harvester can convert ambient light energy into electrical energy and keep it in the storage device. The harvested output of *PV* cannot directly connect to wearable loads for two main reasons. Depending on the incoming light, the harvested current result in varying open-circuit voltage. It requires the power management circuit to deal with unregulated input variation. Second, depending on the *PV* cell's material type and an effective area, the I-V characteristic's performance varies, resulting in a variation of the output power. There are several works of maximum power point tracking (MPPT) methods that allow the solar energy harvester to achieve optimal harvested power. Therefore, the harvested power depends on the size and usually small area cell is sufficient for micro-watt loads low-powered applications. The available harvested voltage, however, is generally very low-voltage range between 0.4-0.6 V. The voltage ratings of electronics in standard wearable applications operate in 1.8-3 V voltages as described in introduction's application example section. It is higher than the supply source can offer. The overcome the mismatch voltage between source and supply circuit, a DC-DC boost converter is necessary.

The switch-mode converters are favoured over the linear converters due to their highly efficient and small area overhead. The inductive converter in the switch-mode converter is common due to its high-efficiency performance. However, the integration of the inductor in the miniaturised integrated on-chip design tends to be bulky. Therefore, the switched-capacitor approach DC-DC converters will be explored in this research. In the switched-capacitor converter universe, there is plenty of work for single-output designs for various topologies. Most converters are reconfigurable to the different DC voltage levels apart from Dickson and cross-coupled charge pump topologies due to their boosting power stage architecture through a number of stages. However, existing multi-output converters are limited to the fixed gain ratio. This work explores the reconfigurable dual-output converter with adjustable gain to compromise the research gap.

The thesis's primary focus is to present the inductor-less, switched-capacitor-based DC-DC converter power management system (PMS) supplied by a varying input of *PV* energy harvester input source. The PMS should deliver highly efficient regulated voltage conversion ratio (VCR) outputs to low-power wearable electronic devices that constitute multi-function building blocks.

Contribution 1: Wearable devices comprise different building blocks, e.g. sensors, analogue front-ends, processors, etc. which each block operates at different power ratings. The available conventional DC-DC converter is a single-input-single-output (SISO) charge pump that can configure a wide range of DC gains. However, supplying multi-blocks with various power ratings with a single output converter will drive the converter with the highest gain. It takes away the use of a reconfigurable converter. The lowest voltage rating load was received from the SISO charge pump's highest VCR via some drop-down circuits. Hence additional considerable power loss has occurred. Therefore, single-input-multi-output (SIMO) charge pumps that can configure different DC gains at outputs have become attractive solutions. However, the existing SIMO charge pumps come with a fixed gain VCR. **This work** explores the highly efficient single-input-dual output (SIDO) charge pump design, which can configure into different DC gains (reconfigurable). The series-parallel topology is used due to its ability to configure fractional gains as well as integer gains. The proposed charge pump is designed in a 4-phase clock scheme and produce two simultaneous DC gain. It can also reconfigure into step-up (boost) or step-down (buck) diverse VCRs. The programmable Verilog-A control unit selects which transistors turn on or turn off to configure certain VCR at a series-parallel reconfigurable power stage network. Finally, two final outputs are internally self-regulated through an interleaving scheme using identical internal networks of the power stage. Therefore, the SIDO charge pump does not require a big filter capacitor for a stable DC supply. It is designed in a 180-nm AMS technology Cadence virtuoso environment and has achieved a maximum power efficiency of 85.26%.

Contribution 2: **This work** investigates the system-on-chip charge pump and improves the previous SIDO charge pump in Contribution-1 and fabricated on-chip in 180-nm TSMC technology. It features integrated on-chip a new transistor-based gain control unit (GCU) to configure various VCR in a series-parallel power stage network to configure SISO and SIDO integer step up gains. The proposed charge pump operates in two-steps adiabatic 2-phase clock signals designed in the tri-state driver. It provides the slow transient charging/discharging characteristic and avoids drastic voltage amplitude swing intake from the input source during the charge sharing process. Moreover, this work introduces reconfigurable SISO VCR gains in the SIDO charge pump. One of the SISO gain modes, namely 'Low-powered (*LP*)' gain mode, which produce ($\times 2$), is dedicated to the low load and idle condition. The charge pump consumes a low power of 4-μW in *LP* mode. Hence it benefits applications with idle mode conditions and demands the energy constrain power management system.

Likewise, the 4-phase topology charge pump, this design is also self-regulated due to the interleaving scheme and applies to all available gain modes except for the 'High conversion (*HC*)' mode. *HC* mode is another SISO design to produce VCR of ($\times 3.5$) and follow Dickson's ladder topology whilst the rest of the available gain modes are configured by the series-parallel configuration. These are all done in the same reconfigurable power stage network designated mainly by the series-parallel configuration. The performance analysis of this work is done as (1) stand-alone converter design (without feed-in), in which GCU and clock generator circuits are powered by input source and additional power supply, and (2) system-level (feed-in), in which the converter output self-suppled to the GCU. Then rest of the circuit is self-powered by the input source. This work has achieved power efficiencies of 90.43% and 80.28% at stand-alone and system-level, respectively.

Contribution 3: This work presents the proposed PMS comprising a start-up charge pump and the main charge pump. The various start-up charge pump designs have been explored to accommodate the ultra-low input from the *PV* cell energy harvester. Among which an appropriate start-up charge pump is integrated with SISO and SIDO main charge pump proposed in Contribution 2. It is required because, in Contribution-2, the assumption has been made that two *PV* cells are connected in series and have a stable input source that provides around 1 V to sufficiently supply the proposed work. Contribution 2 work is not designed to operate in low voltage input and does not include line regulation to sustain varying input voltage. Thus, the start-up charge pump is introduced and enhanced the envisioned PMS. It can operate in ultra-low varying inputs from the *PV* cell energy harvester and produce highly efficient regulated reconfigurable (SISO and SIDO) wide VCRs outputs. **This work** presents a system-on-chip PMS design and fabricated in 180 nm TSMC technology. As a result, this work has yielded a power efficiency of 85.92%.

Publications

Journal Articles:

J. Zhao, **K. O. Htet**, Yuchi, R.Ghannam and H. Heidari, "Photovoltaic Energy Harvesting for Implantable Medical Devices," in J. of Advanced Healthcare Materials , vol.9,pp.1000779, 2020.

K. O. Htet, R. Ghannam, Q. H. Abbasi and H. Heidari, "Power Management Using Photovoltaic Cells for Implantable Devices," in IEEE Access, vol. 6, pp. 42156-42164, 2018.

K. O. Htet, R. Ghannam, M.A. Imran and H. Heidari, "Reconfigurable Switched Capcitor DC-DC Converter for Energy Efficient Wearable devices," in IEEE Trans. on Circ. and Sys. II (TCASII)-brief, 2021. [Under review minor revision]

K. O. Htet, A. Rashidi, F. Moradi, R. Ghannam and H. Heidari, "A 85% Efficient Switched-Capacitor Power Mangement for Photovoltaic-powered werable devices," in IEEE Open access Journal Circuit and System, 2021. [Under review]

K. O. Htet, H. Heidari, F. Moradi and R. Ghannan, "Energy-Efficient Start-up Dickson Charge pump with clock booster cirucit for Batteryless Biomedical Implant Devices," in IEEE Open acess Journal Circuit and System, 2021 [In Prepearation]

Conference Papers:

K. O. Htet, H. Heidari, F. Moradi and R. Ghannan, "Energy-Efficient Start-up Dickson Charge pump for Batteryless Biomedical Implant Devices," in IEEE International Conference on Electronics, Circuits and Systems (ICECS) Conference, Glasgow, , pp.1-4, 2020.

K. O. Htet, H. Fan and H. Heidari, "Switched Capacitor DC-DC Converter for Miniaturised Wearable Systems," IEEE International Symposium on Circuits and Systems (ISCAS), Florence, Italy, 2018, pp. 1-5.

K. O. Htet, J. Zhao, R. Ghannam and H. Heidari, "Energy-Efficient Start-up Power Management for Batteryless Biomedical Implant Devices," 25th IEEE International Conference on Electronics, Circuits and Systems (ICECS), Bordeaux, 2018, pp. 597-600.

H. Fan, **K.O. Htet**, W. Cheng, Y. Li, Q. Feng, H. Che, X. Zeng, H. Wang, H. Wang, D.Li, K. Zhang, Y. Cen and H. Heidari, "High-Precision Adaptive Slope Compensation Circuit for System-on-Chip Power Management," IEEE 38th International Performance Computing and Communications Conference (IPCCC), London, 2019, pp. 1-2.

J. Zhao, **K. O. Htet**, R. Ghannam, M. Imran and H. Heidari, "Modelling of Implantable Photo-voltaic Cells Based on Human Skin Types," 15th Conference on Ph.D Research in Microelectronics and Electronics (PRIME), Lausanne, Switzerland, 2019, pp. 253-256.

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Chapter 1 – *INTRODUCTION*

1.1. Power Mangement System in Low-powered weareable devices

There is a growth of applications in wearable technology to enhance the quality of life through incorporated into healthcare, education, security and, many more [1-7], as illustrated in Fig. 1.1. Advances in CMOS fabrication processes are further miniaturising these devices [8-10]. These devices will be integrated on soft contact lenses [11-15] or wrist-worn smart bracelets [16-20], as an example, and will transform our day-to-day lives. Such devices can be divided into several building blocks, as shown in Fig 1.2, such as sensors, actuators, analogue front-end devices, and so on to serve the purpose of recording, stimulation, and communication. Given the example in Fig.1.2 (a), energy harvesting was received from the photovoltaic and thermal means, power management is done in converter and the provide it to sensings and transmission via Bluetooth module. Similarly, in Fig. 1.2. (b), sensing and processing was done by the electrochemical sensor and microcontroller. Meanwhile, energy harvesting was performed and stored in the capacitor. Each of these not only has different functionalities as well as operates in different voltage ratings. An increase in the specification and functionality of the device means more electronics modules are needed to integrate.

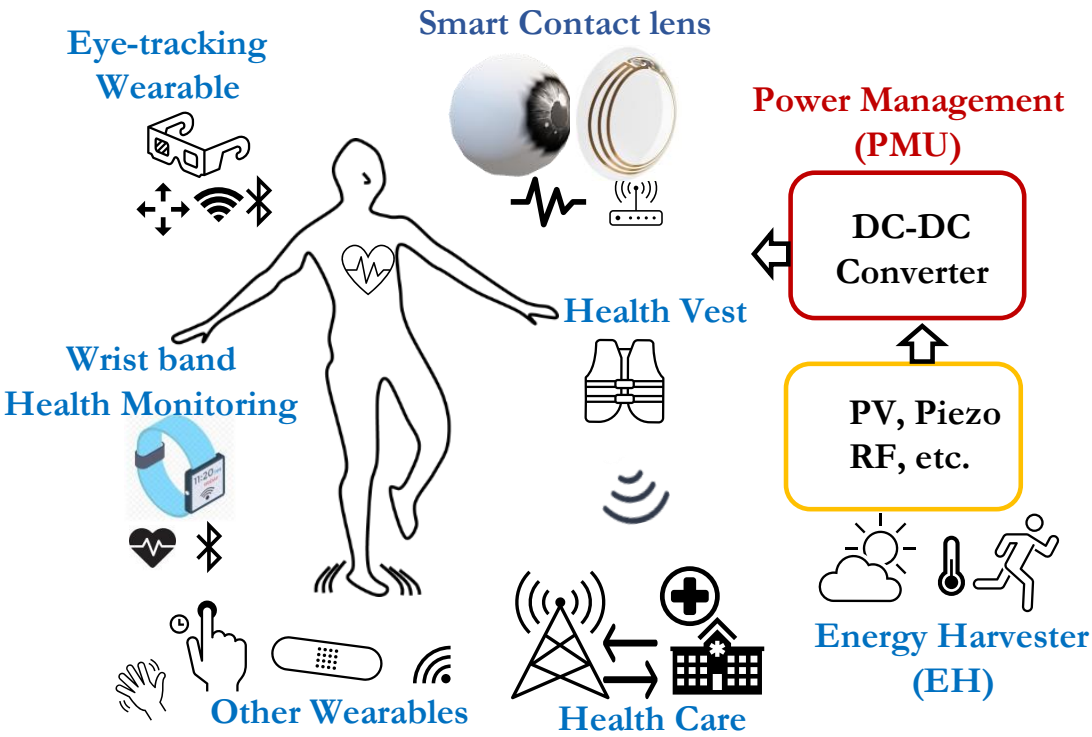


Figure 1- 1. Overview of Power Management System in the wearable application.

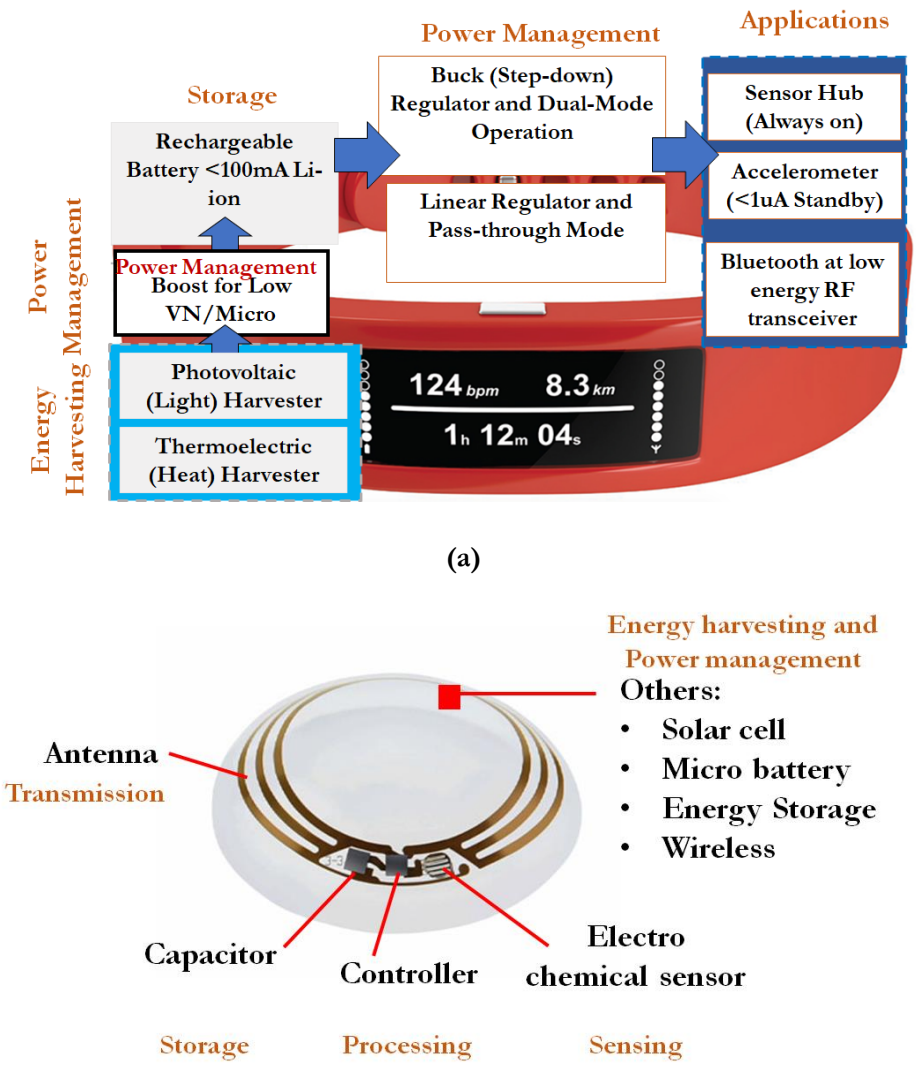


Figure 1- 2. (a) Wearable wrist-worm bracelets or (b) Smart Contact lens comprise multiple electronic modules which operate in different power ratings.

While wearable designs are growing fast, battery life is the central discomfort point in wearables devices due to the size and the fixed amount of capacity [21]. Once a battery reaches the maximum charge cycle, it needs to be taken out to recharge it. Instead, the autonomous (self-powered) wearable system can be achieved by integrating the energy harvesters with a battery. As a result, it extends the battery life and reduces the size of the storage device [22].

As illustrated in Fig. 1.3, energy can be extracted either from the surroundings or from the body [23]. However, the power extracted from these sources is usually unreliable. For instance, Photo-Voltic (*PV*) cell is the location, and incoming irradiation depends [24, 25]. Any *PV* cells shading leads to unstable output power [26]. Other similar factors that affect output power include the high motion dependency of the piezoelectric system in [26], the temperature dependency of the thermoelectric system in [27], the electrostatic discharge phenomenon of the electrostatic system in [28], and the relative motion between a conductor and a magnetic flux dependency of an electromagnetic system in [29]. Therefore, several degradation factors, such as temperature, light, movement, etc., dedicated the harvester's output. Thus, self-powering devices need efficient and reliable power management or DC-DC converter. The most important features can be distinguished into type of conversions, performance, reliability, and flexibility.

The DC-DC power **conversion circuit** is necessary for wearable applications. The desire circuit supply and the source voltages are usually mismatched[30], especially for a system with multi-block electronics. The step-up (Boost) converter [31-33] can be used when the source voltage is lower than the desired supply circuit. Alternatively, if the input source is much larger than a load voltage rating, a step-down (Buck) converter [34-36] can be implemented.

Moreover, the **performance** of the converter heavily relies on power efficiency. It is mainly influenced by the losses [37] that occur during the conversion process. The important converter outcome such as power densities and voltage conversion ratio (VCR) is determined by how losses are minimised through several optimisation techniques [38-40].

The **reliability** of the converter is usually defined by regulation at the output side (load regulation) [41, 42] and regulation at the input side (line regulations)[43, 44]. For an application that contains multi-blocks of electronics, load regulation is essential to keep up with the load conditions changes. Similarly, self-powering devices that use the unreliable input source line regulation of the converter set overall efficiency and performance.

Furthermore, the VCR of a converter with a fixed ratio gain [45, 46] will decrease over time since the gain ratio relative to the input value changes. This phenomenon is usually influenced by the critical factor of the input source- degrading a battery life span over time. To continue relevant over time, many converter designs that enable the wide range of VCR have been proposed [47, 48]. Thus, self-powered devices need efficient and reconfigurable power converters to provide a wide range of broad DC gains to maintain the high (VCR) and power efficiency. Moreover, accessibility to the wide range of DC gains benefits the applications that require dynamic loading conditions like many essential building blocks or electronic modules in wearable devices with different operations, functionality, and voltage ratings. Hence, design **flexibility** is crucial for the PMS of wearable devices.

This research focuses on a miniaturised integrated Power Management system that can fulfil the discussed requirements, as highlighted in Fig. 1.3.

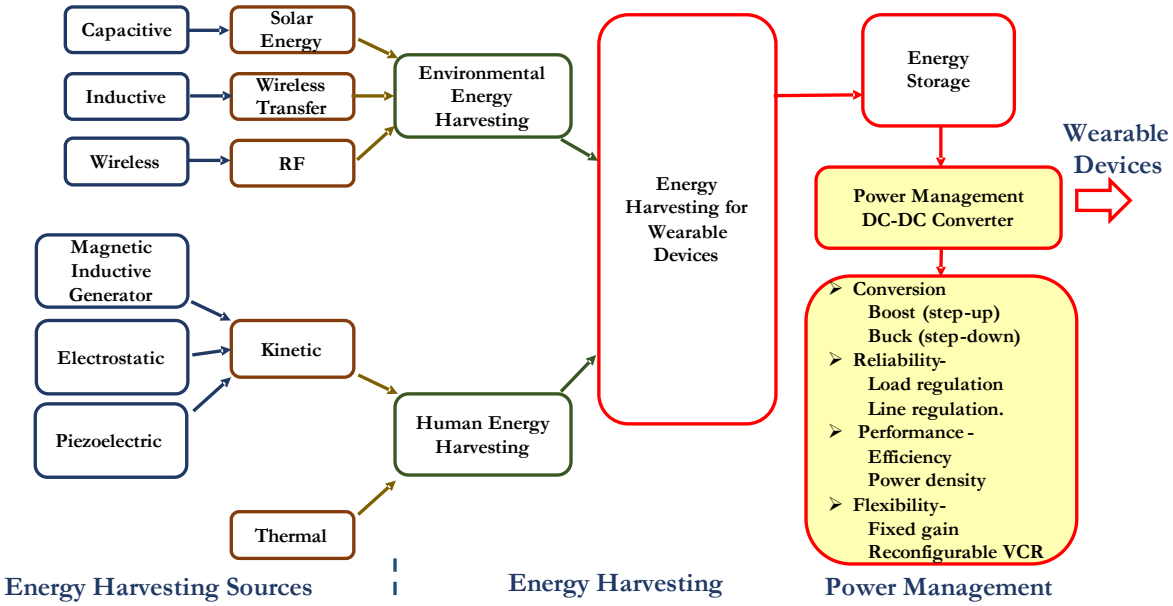


Figure 1- 3. The different types of energy harvesters harvest energy from the various energy harvesting sources and the essence of power management in wearable devices.

In selecting energy harvesting mechanisms for miniaturised power systems in wearable devices, size and power density are primary factors. Comparing different energy harvesters in terms of size and power is presented in Fig. 1.4 and summarised in TABLE 1.1. The power densities are defined by the output power over the available area of the solar cell. Fig. 1.4 was constructed from the literatures information of TABLE 1.1, in which different types of energy harvesters are compared in terms of size, power density and the type of materials. Due to the smaller size (comparable to biofuel) and wide range of power density, Solar cells have been widely used in wearable electronic devices. Among which, Silicon (Si) materials solar cells had high power densities of up to 104 μW/mm² over 10 mm² area. For instance, the artificial iris demonstrated in [49] and [50]. However, energy harvesting systems that rely on solar energy need to have rectifying circuits to maintain high energy efficiency because of the intermittency and variability of incoming solar radiation [51].

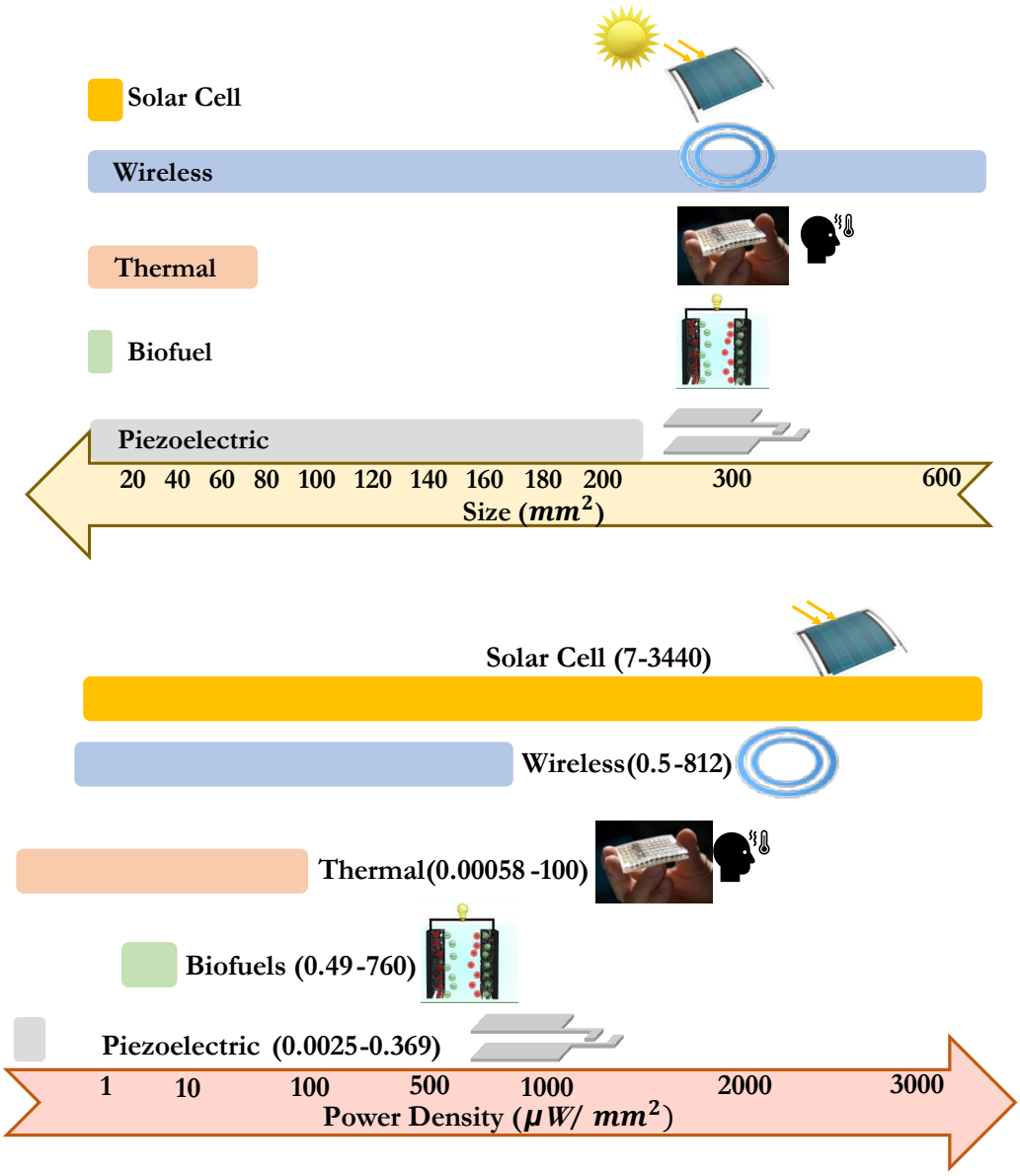


Figure 1- 4. The comparison of energy harvesters in Size and power density.

Photovoltaic cells convert light into electricity. These cells range from expensive, high-efficiency multi-junction devices to lower-cost non-crystalline devices. The performance of a solar cell can be determined by the current density I-V curve, which has the relation of the open-circuit voltage (V_{oc}) and the short circuit current (I_{sc}) [52]. Depending on the sunlight or indoor illumination, the output characteristic of I-V curve varies over the given parameter settings.

TABLE 1- 1. VARIOUS OUTPUT POWER DENSITIES OF POWER HARVESTERS.

Power Harvester	Area (mm^2)	Material	Power harvested ($\mu W/mm^2$)	Reference
Piezoelectric	100	PVDF	0.0033	Sohn, J. W., et al. (2005) [53].
	100	PVDF	0.0025	Sohn, J. W., et al. (2005) [53].
	36	PVDF	< 0.369	Yu, Y., et al. (2016) [54].
	226.98	PVDF	0.01	Cheng, X., et al. (2016) [55].
	0.0255	ZnO	0.01	Khan, A., et al. (2016) [56].
	25	PZT	0.055	Shi, Q., et al. (2016)[57].
Biofuel	7.069	OMCs	0.491	Zhou, M., et al. (2009) [58].
	Nil	SWNTs	760	Lee, J. Y., et al. (2011) [59].
	2.3	Nil	12.6	Katic, J., et al. (2018) [60].
	6.28e-8	CNT	0.096	Tan, Y., et al. (2009) [61].
Thermal	7.92	Bi-Te	18.939	Yoon, E.-J., et al. (2018) [62].
	67.92	Bi-Te	0.442	Yoon, E.-J., et al. (2018).
	Nil	Poly-Si	100	Yoon, E.-J., et al. (2018).
	nm scale	PZT	0.00058	Zhang, G., et al. (2018) [63].
Wireless power	615.75	Litz wire	812	Borton, D. A., et al. (2013) [64].
	452.38	Copper ceramic	22.10	Stingl, K., et al. (2013) [65].
	176.71	PZT	565.9	Ozeri, S., et al. (2010) [66].
	91.60	Copper polyimide	10.91	Kim, T.-i., et al. (2013) [67].
	0.5	Copper polyimide	400	Wentz, C. T., et al. (2011) [68].
PV cell	1.512	Si	39.68	Lu, L., et al. (2018) [69].
	8.91	Si	3440	Hung, Y., Jr., et al. (2018) [70].
	0.5776	GaAs	90.5	Song, K., et al. (2017) [71].
	10	Si	104.96	Moon, E., et al. (2017) [72].
	1	a-Si	102.42	Moon, E., et al. (2017).
	1.23	Si	7.75	Moon, E., et al. (2017).
	1.23	GaAs	12.24	Moon, E., et al. (2017) [73].
	Nil	Si	100	Gong, S. and W. Cheng (2017) [74].
	1.3	Si	322	Chen, Z., et al. (2017) [75].
	1.67	Si	159	Hung, Y., Jr., et al. (2014) [76].
	0.12	Si	11	Ayazian, S., et al. (2012) [77].

This research presents an innovative solution to convert the unregulated output voltage of *PV* cells to a regulated DC voltage, namely the start-up charge pump. Ultimately, the reliable and efficient DC-DC conversion offers steady and regulated DC output voltage from an unregulated source to attain more prolonged and more efficient system run-time. Then can be stored in the storage device, such as the capacitor, which will act as the secondary power source to the main DC-DC conversion charge pump.

In exploring the different types of converter, the pros and cons of each converter should be analysed. As depicted in Fig. 1.5, linear regulators such as low dropout regulator (LDO) and voltage regulator are also common choices. Due to the linear control capability and achieve (1) easy down conversion, (2) cost-effective, (3) low ripples characteristic and low noise (no switching involve), and (4) high efficiency. Due to the discussed advantages, the linear regulator stands out over switching power converters. However, there is a high power dissipation across passive elements, such as Darlington transistors [78], and the fixed-gain configuration is still a major challenging issue regarding noise immunity and low complexity. If a different voltage level is necessary, multiple LDO needs to stack together [78]. Lastly, linear regulators require tuning over time due to degrading input sources and their fixed-gain ratio nature. Therefore, switching type converter is more attractive for application requiring (1) a high-power efficiency, (2) an area-efficient, (3) reconfigurability of VCR suitable for a varying input from energy harvester source, (4) and benefits application comprises with different voltage ratings.

When switching mode DC-DC converter is applied, commonly use traditional type inductive based boost [79, 80] or buck converters [81, 82]are undeniably a popular choice. The inductive converter displays high energy efficiency [82, 83]. However, in search of a miniaturised on-chip power supply, the integrated inverter is bulky and unattractive.

On the other hand, another switching converter type - the switched capacitor approach compromises the desirable miniaturised on-chip converter design for wearable devices. The comparison of different kinds of conversion units is presented in TABLE 1.2. In this research, the switch-capacitor DC-DC converter is selected for a potential miniaturised power system for a low power wearable application due to high efficiency and small area overhead.

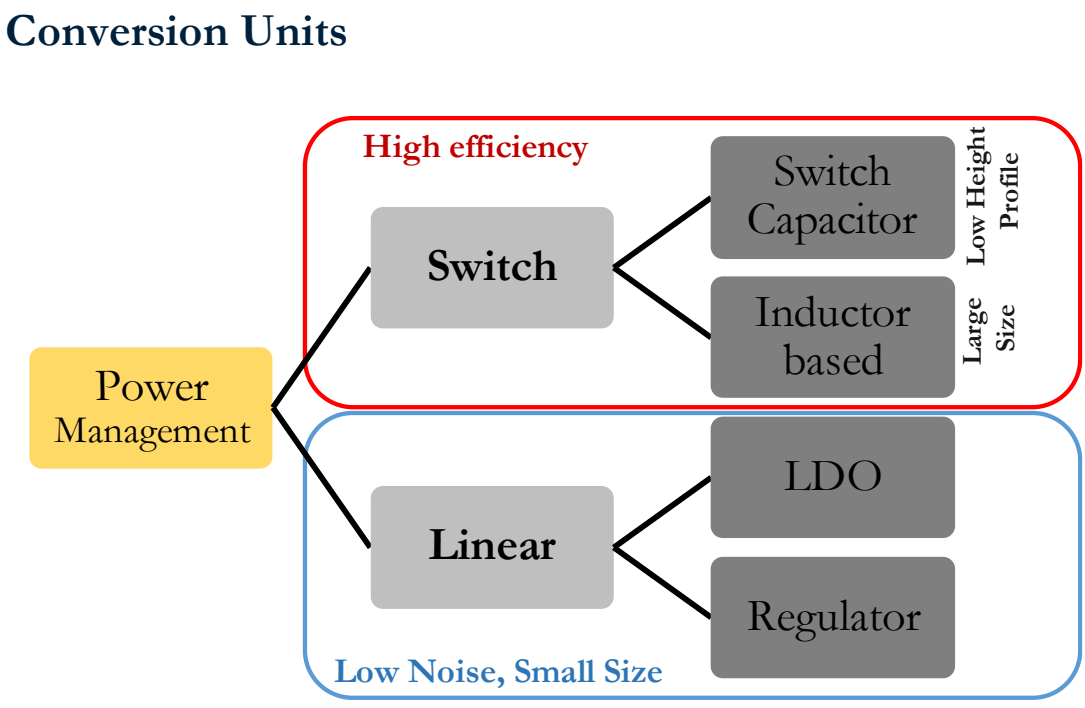


Figure 1- 5. The advantage and disadvantages of linear and switching mode power management units in comparison.

TABLE 1- 2. ADVANTAGES AND DISADVANTAGES OF DIFFERENT CONVERSION UNITS.

Type	Advantage	Disadvantage
Linear Drop-Out (LDO) Regulator	• Can manifest on-chip with little area coverage. • Fast transient and small ripple characteristics [84, 85] • Low cost	• Linear Lost effect since voltage dropped is controlled by the resistance of the transistor. • Require tuning over time due to decay of battery life. • Fixed voltage ratio set up
Inductor based DC-DC converter	• 100% theoretically efficient independent of load voltage, providing that passive device is ideal. • Display high efficiency [82] • It can be controlled digitally with little overhead power [86].	• Require significant off-chip filter components. • The inductor is bulky[87] • [88] suggests integrating an on-chip inductor to minimise area will need to be run at >1000MHz high switching frequencies. • Consequently, an increase in switching losses and conduction losses due to low Q factors on-chip inductor type installation
Switched Capacitor (SC)	• Can achieve high VCR and power efficiency. But not comparable to the Inductive-Capacitive converter. • The use of a passive component capacitor has a relatively tiny size than the bulky inductor. • Highly area-efficient • Suitable for on-chip power supply design	• Switching loss is significant and can potentially induce crosstalk. • High output impedance loss and high output ripple limit practical applications. [89]. • The voltage conversion ratio has also been limited by the flexibility of gain configuration. • Other losses, such as bottom plate parasitic loss, conduction loss, is dominant. Due to the lack of a protective diode, clock control's poor design can trigger reversion loss in step-up conversions. • Above losses directly towards power efficiency.

1.2. *Brief history of the charge pump topologies*

The first-ever design of the switched-capacitor (SC) converter voltage doubler was presented in 1914 by Greinacher [90], as depicted in Fig. 1.6.. Later in 1923, Marex [91] has proposed the pulse power generator for research of the lightening and later use in eye surgery applications [92, 93].

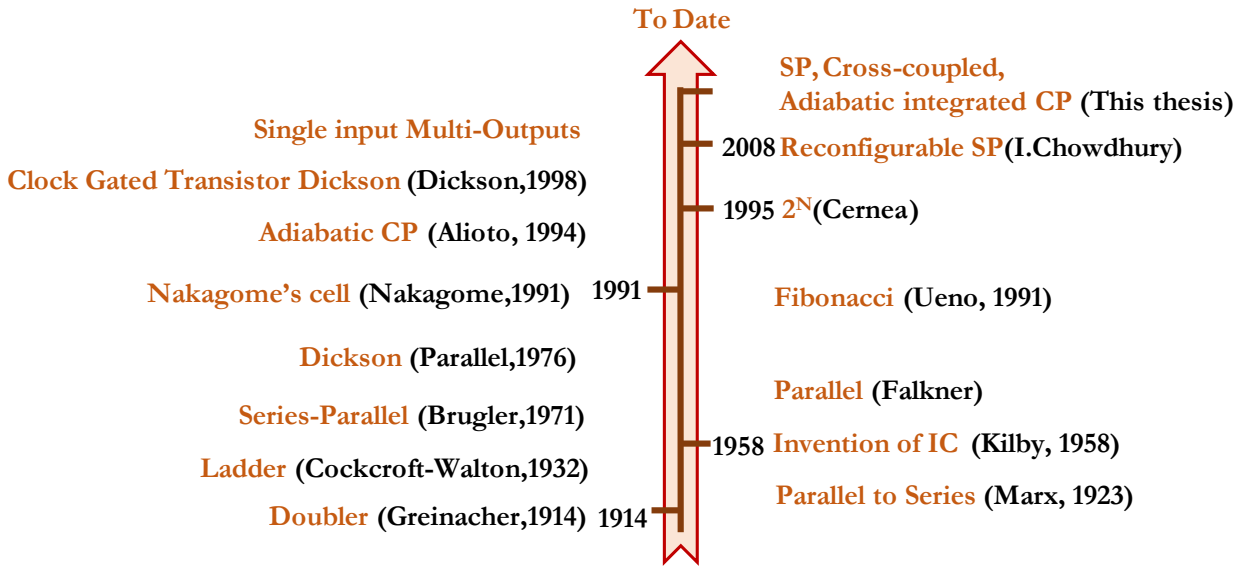


Figure 1- 6. The brief history and the evolution of the charge pump topologies.

Cockcroft [94] in 1932 presented two time DC voltage gain for generating high-velocity positive ions in a particle accelerator, and it produces a very high voltage of up to 1 MV [94]. Later, it became popular in generating a pulse for X-Ray medical equipment [95]. The invention of the integrated circuit (IC) began in 1958 by Kilby [96]. Since then, the integration of SC converters in IC has become popular. Brugler proposed series-parallel topology in 1971 [97], and Falker in 1973[98]demonstrated three clock-controlled parallel topologies that use SC converters for ICs. Later in 1976, the first commercial SC converter was introduced by J.F. Dickson [99] for non-volatile memory and later used for EEPROM [100-102]. Since then, innovative topologies of SC charge pumps have become increasingly popular in integrated circuit applications due to their small area and high efficiency. The evolution of widely use Dickson's charge pump topologies [103-108] has been collectively reviewed in [109]. To achieve high voltage gain with fewer stages, topologies such as Fibonacci in 1990 [110] and 2^N design in 1995 [111] have also been reported. Both topologies require high-voltage devices (capacitors and diodes) to operate.

Another significant milestone in charge pump history is the invention of the cross-coupled charge pump. It was first invented as the 2-stage charge pump Doubler by Nakagome et al. [112] for a DRAM word-line driver. It has further advanced into a dual branch charge pump- Gariboldi and Pulvirenti present the cross-coupled charge pump for quad monolithic line driver[113, 114]. The advantage of cross-coupled charge pump enables the ripple management at the output side due to their 180 degree out of phase complementary MOS structure enhance reliable DC supply at the load and improve charge transfer. The various improvements [115-119] have been proposed to date to achieve better efficiency, drivability, low voltage input operation and minimise reversion loss. Similarly, the composite charge pump that reaches the low ripple output is also presented in [109, 120]. The time-interleaved [47, 121]between two or more identical networks eliminate the need for a large filter capacitor. It is done by splitting a single charge pump into smaller identical ones with half the value for each network expansion and operate in complementary charge-discharge action. As a trade-off, the complexity of the multi-phase clock-phase generator and its power consumption increase. One example of high efficient multistep split-merge charge pump which uses a solar energy harvester can be found in [121].

To lower the power consumption of the charge pump, many researchers have proposed the adiabatic charge pump [122, 123], which charging-discharging action was operated in a two-time step charge sharing clock waveform [124, 125]. Such a strategy in energy harvesting application can be found in [126]. In recent times, a similar concept of soft-charging technique [35, 127, 128] charge pumps are increasingly popular. Lastly, an Adaptive converter or reconfigurable charge pump to provide the flexibility of charge pump gain configuration has been proposed [129, 130]. It allows a number of power stages to freely configure [116, 131] to closely supply the various voltage rating of the different loads with the highest voltage conversion ratio [132-134] from the varying input voltage source [135]. Therefore, a reconfigurable charge pump enhances the need for a drop-out circuit and its power dissipations. It is suitable for energy-efficient devices [136] and microscale energy harvesting electronics [137]. It is beneficial for low power applications such as Flash memory [138]. The only downside of this design approach is the flexibility of the charge pump that come with circuit complexity in configuring different gain modes.

J. S. Burglar [Brugler1971] has reported that voltage multiplier circuits in series connection suffer worse bottom-plate parasitic than the parallel connection. The non-ideal condition analysis of the area, number of stages, the optimal number of discrete capacitors, the current efficiency of each topology have been described in comparison [139, 140]. The noteworthy equations of each topology are extracted from [93, 139] and demonstrated in TABLE 1.3.

The design strategy and power stages vary upon the application requirements. But the selection of SC topology and its power stage design can be categorised into two groups with the output power requirement [141] – monolithic SC converter by using integrated both capacitors and switches [142], and one integrated and one discrete of capacitors and switches [143, 144]. The first category falls into low power applications such as an operational amplifier, sensors, memories, etc. The second category is for high voltage RF application [145], LED driver [146] and so on.

TABLE 1- 3. IMPORTANT EQUATIONS OF CHARGE PUMP TOPOLOGIES.

Topologies	V_{MAX}	R_{PMP} Uniform Cap	Each Cap		Current Eff	V_{CAP} Max	V_{SWITCH} Max	Parasitic Cap Impact
Ladder	N+1	$\frac{N^2(N+1)(N+2)}{12C_{Total}}$	C2i-1 (odd)	C2i (even)	1/Gain	1	1	+
			$(\frac{N}{2}-i+1)$					
		$\frac{N^2(N+1)(N^2+2N+3)}{12C_{Total}}$	$(\frac{N+1}{2}-i+1)$	$(\frac{N-1}{2}-i+1)$				
SP	N+1	$\frac{N^2}{C_{Total}}$	$\frac{C_{Total}}{N}$		1/Gain	1	N	+++
Dickson	N+1	$\frac{N^2}{C_{Total}}$	$\frac{C_{Total}}{N}$		1/Gain	N	1	-
Fibonacci	F(N+1)	$\frac{N}{C_{Total}}\sum_{i=0}^{N-1}F(i)^2$	F(N-i)		1/Gain	F(N-1)		++
2^N	2^N	$\frac{N}{C_{Total}}(\frac{2}{3}N(N-1)(2N-1)+1)$	$C_{Total}\frac{2N-i}{2N-1}$		1/Gain	2^{N-1}		+++

Effective Output Impedance (RPMP)

Number of stages (N)

Fibonacci number (F)

i^{th} number of stage (i)

1.3. Standard Conversion Losses

In search of a suitable low power design charge pump, the following losses depicted in Fig. 1.7 dictate the charge pump's final efficiency [47]. Hence require significant attention during the design.

1.3.1. Redistribution loss

The following factors contribute to the redistribution loss [147] -

- Usually, at least node in Dickson (C_{out} discharge all charge to load and next cycle in contact again to resupply the charge) [39].
- The cross-coupled charge pump is better performance at redistribution loss due to low ripple output [116]from two interleaved networks of the cross-coupled circuit. Operating in two opposite phases ensures that the charge is continuously delivered at the load, unlike the Dickson charge pump.
- The standard series-parallel method also suffers from redistribution loss due to requiring a one clock cycle to recharge the empty charge pump capacitor.
-

1.3.2. Conduction loss

The following factor contributes towards the conduction loss [148]-

- Since conduction loss depend on equivalent resistance of transistor [147]-

$$R_{eq} = \frac{L}{\mu Cox(V_{GS}-V_{th})W} \quad (1.1),$$

  either setting low threshold voltage, bigger width (can increase in device threshold) or smaller length (result in poor leakage current). These trade-offs are to consider ensuring the high efficiency of the charge pump.

1.3.3. Reverse charge sharing

The following factors contribute towards the reverse charge sharing [149] and its challenges-

- Short small channel length can cause reverse charge sharing or leakage, whilst a longer channel length can generate redistribution of Mosfet's charge channel and consequently affect the poor charge pump efficiency.
- PMOS can replace with NMOS because of the low mobility charge carrier.
- The complementary MOS structure of a cross-coupled charged pump controlled by a 2-stage transistor between each stage prevents revere charge sharing [40].
- Having a stronger gate voltage also help. But consume more power.

1.3.4. Body effect

The following factors contribute to the body effect [150] in the charge pump-

- The last stage of standard Dickson's charge pump suffers from body effect because of charge transfer switches being NMOSs, and its bias is connected to the ground. Therefore, it has gotten worse as the number of stages increases.
- NMOS transistor can be used to improve forward charge sharing but have a strong body effect.
- PMOS have improved body effects and are immune to reverse charge sharing because hole mobility is slower than electrons.
- PMOS (highest potential of source or drain should connect to the bulk); therefore, the bulk's usual connection to the source is not viable. It depends on the operation of charge sharing between the source and drain of the switch's transistor suffer body effect.

1.3.5. Threshold loss

The following factors contribute to the threshold effect in the charge pump-

- Last stage or first stage (if the input voltage is very low)
- PMOS (has less absolute threshold) than NMOS
- Cross-coupled has advantages– due to complementary two pumping bunch there is no large device involve in it and maintain small threshold and a strong charge transfer [151]-

$$Vth = V_{TO} + r(\sqrt{2|\phi_F|} + V_{SB} - \sqrt{2|\phi_F|}) \quad (1.2)$$

- Gate voltage (V_{TO}) Body Effect (r) Strong Inversion (ϕ_F) Voltage diff between Source-Bulk(V_{SB}).

1.3.6. Switching loss

- The charge-discharge mechanisms of a gate-source parasitic capacitance of MOSFET transistors (C_{gs}), the frequency of switching (f_s) and the gate-source voltages (V_{gs}) of individual switches along the path (i) dominate the switching power losses [152] -

$$P_{sw\_Mode(boost,buck)} = f_s \sum_i C_{gsi} V_{gsi}^2 \cong f_s C_{OX} \sum_i W_i L_i V_{gsi}^2 \quad (1.3)$$

- where (W_i, L_i) are the width and length of individual transistors along the charge transfer path.

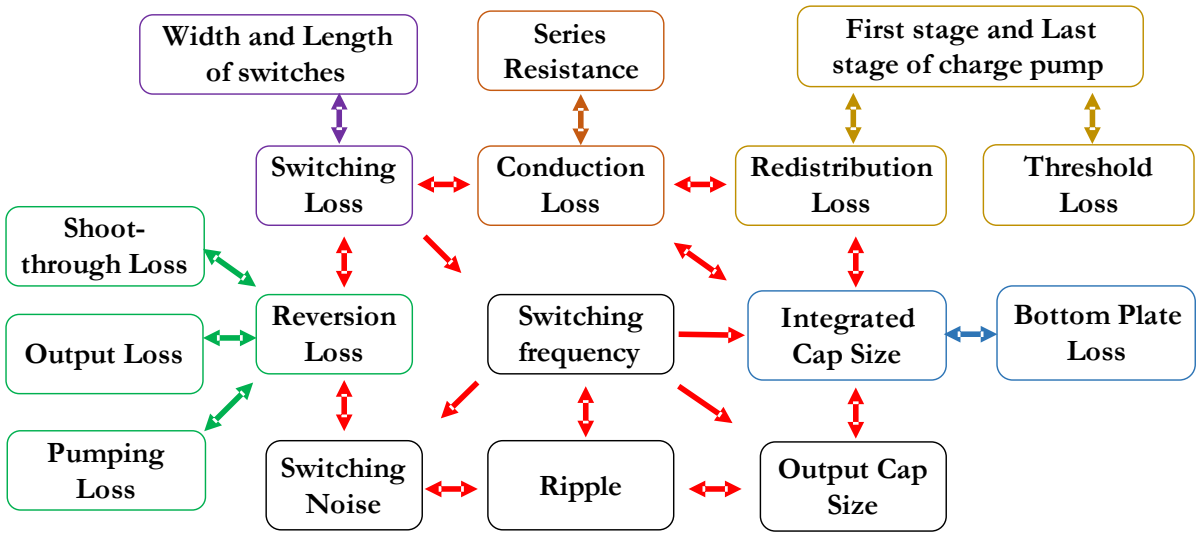


Figure 1- 7. The trade-off diagram of the losses contributes towards the power efficiency of the charge pump.

1.4. State-of-the-art power management units by using the PV cells as the input source.

Henceforth, various literature on converters that uses the *PV* cell as an input source shall be discussed. All in one system-on-chip with a power management system (PMS) operates under solar energy harvester is presented in [26]. Best to my knowledge, this is the first paper to combine *PV* cell and on-chip DC-DC converter. The following works are based on a system-on-chip DC-DC converter with a switched capacitor (inductor-less) approach using the *PV* cell as the primary energy source. The summary of all the power management units presented in this Chapter-2 to Chapter-5 is generalised and depicted in Fig. 1.8.

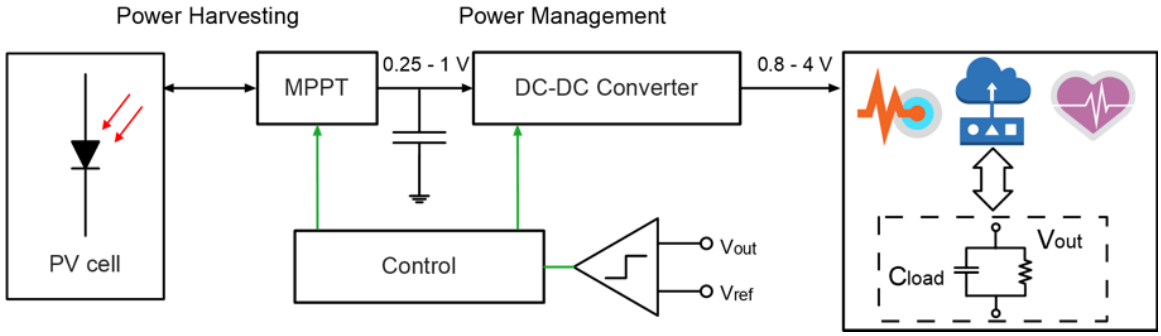


Figure 1- 8. The generalise state-of-the-art Power management units integrated with *PV* cells.

1.4.1. Power Management Systems with optimised end-to-end efficiency

Contrary to the conventional converters, in step-up voltage conversion at the load end, instead of continuously gathering charge from the energy source, the proposed (DHA) converter accumulates slow charging at an input capacitor and rapidly fire the load capacitors. The charge pump (CP) minimises the efficiency loss for a wide input range, especially true for two conditions that contribute to poor efficiencies-

(1) In low ambient conditions, a low input power P_{in} is harvested from the energy source. The charge pump's operating frequency should slow down for slow energy delivery and incur leakages during this condition.
(2) Secondly, the increase in P_{in}, where the charge pump needs to run fast to correspond to the input power surge trigger constant overhead of clock power consumption and charge pump efficiency, is bound to transistors driving strength. DHA is applicable during the condition (1).

In two phases, DHA's operation thrives through trade-offs in Maximum power point tracking (MPPT) and CP efficiencies to achieve optimal end-to-end efficiency. The harvested voltage V_{sol} has deviated from $V_{MPPT,}$ resulting in a slight reduction in harvesting source efficiency. Yet CP efficiency is improved by duty cycle through transistor switches to enable through Mode Controller (MC). During the first phase, V_{sol} increases until it reaches above the reference V_{MPPT} and isolates the CP by disconnecting transistor switches connecting the source and output. The sacrifices of MPPT efficiency and power gating of the charge pump reduce the leakage below 15 pW and improve the overall end-to-end efficiency. However, in conventional CP, it will hold V_{sol} at fixed V_{MPPT} and enhance constant high leakage and CP's low efficiency in poor ambient conditions. When V_{sol} is adequate, a burst mode or quick charge transfer phase of start-up mode or phase-2 is operated in its peak efficiency at a steady state. After a short period, V_{sol} decreases rapidly and returns to harvesting mode [153]. However, the leakage can be minimised by reducing the power transistors size, limiting maximum harvestable energy. The end-to-end efficiency of power management is defined by the multiplication of charge pump efficiencies, which has many limitations over leakages and other losses [149, 154], and MPPT efficiency, which efficiency can be easily maintained for a high input range. Their paper, a moving sum, a hybrid structure energy harvester, automatically modulates different duty cycles independently from charge pump operating frequency.

1.4.2. Power Management Systems with optimised voltage conversion ratio (VCR) efficiency

X. Liu et al. [155] in 2016 has proposed a reconfigurable converter design that configures fractional VCR from the harvested voltage from energy sources. The proposed design minimises the inducing of a charge redistribution loss. Moreover, this design benefits the variation of harvested voltages because the environmental change affects the drastic loss in voltage conversion efficiency (V_{CE}) with fixed CR. The capacitive dc-dc topology is inherent to its structure, and several stages depending on the type of topology applied [155]. Similarly to this work, my previous work is also based on the reconfigurability of series-parallel charge pump topology, which can configure dual outputs with wide VCRs [156]. Recently in 2019, an algebraic series-parallel (ASP) topology for switched-capacitor charge pump, which is known to be able to configure flexible fractional voltage conversions (VCRs) is proposed by Y.Jiang and co-workers [157]. In conventional two-dimensional series-parallel CP (2DSP) [158, 159], it often has sizeable bottom-plate voltage swings induced by circuit configuration structure contributing towards parasitic loss despite the flexible rational gain nature of VCRs. This paper's improvement contributes more gain flexibility over fractional gain ratios, which will improve operational output ranges and help the system with an extensive input variation range.

1.4.3. Power Management Systems which address the issues of input source, varies with ambient changes and other factors.

S. Modal and group in 2016 [160] have presented another innovative PMS for solar energy harvesting. The novelty of the power conditioning design involves the simplicity of hardware, and variation of the ambient conditions are considered. Power managing topology is categorised into three different states-
(1) A single DC-DC converter is usually employed to regulate the desired output power load and stored excess energy in a super-capacitor when there is sufficient ambient condition that incurs high harvestable energy to supply the load. It has been achieved by comparing V_{DIV} and V_{REF1} – the charge transfer phase ($V_{DIV}<V_{REF1}$) is performed and stored charge from last stage integrated capacitor C_3 deliver to C_{load} and the store energy phase ($V_{DIV}>V_{REF1}$) from C_3 to back up capacitor C_{STO} through switches M_8-M_{10}. This stored energy is reused with the switching regulator when there is a second condition (2) when there is low harvestable energy at poor ambient conditions. A comparison of V_{DIV} and V_{REF2} governs this operation. The charge transfer from C_{STO} to C_{load} occurs when $V_{DIV}>V_{REF2}$ through transistor M_{11} as the increase in drain potential of M_{11} is more significant than its source and turns the transistor on. (3) The like of varying ambient conditions are also considered to maintain a higher efficiency of LDO regulator (LDR), secondary means of linear DC-DC converter between output capacitor of switching converter and output load, by introducing proper regulation at an intermediate voltage between switching regulator and LDR [160]. Moreover, the same group in 2017 has presented architecture with measurement results of fabricated chip design [161] and analytical modelling in [162]. Moreover, our previous work in 2019, which has intended for implantable applications, has demonstrated the varying input power rating in implantable solar energy harvesters over the penetration of different ethnic group skin types. The variable input voltages are regulated through the reconfigurable DC gains. This Single-Input-Dual-Output (SIDO) power management design produces simultaneous reconfigurable gain pairs and achieves wide VCRs outputs [156, 163]. In 2017, the switched capacitor DC-DC converter reported a discontinuous harvesting approach (DHA) with enabling ultralow-power energy harvesting system. The potential poor ambient conditions resulting in the poor harvestable energy delivery from *PV* cells are considered and sustain the minimum of 40% efficiency illustrated in [153].

1.4.4. Other Harvesters type power management and ultra-low voltage input converters

In conclusion, other literature works proposed ultra-low-power charge pumps worth exploring for a potential candidate for the power management of solar energy harvesting. For a start, the reconfigurable capacitor charge pump powered by thermal energy harvester for IoT applications presented by S. Yoon et al. [164] can operate ultra-low input voltage range of 0.27-1 V with 64% efficiency and regulate towards 1V output. Similarly, the proposed literature from H. Peng and the group in 2014 presented multiple start-up charge pumps that can be used for low input voltages [119]. Finally, the high energy-efficient Dickson charge pump with a clock blocker circuit with high efficiency of 89% was achieved by B. Mohammadi et al. in 2015 [165]. In summary, state-of-the-arts literature of power management units using *PV* solar energy harvesters are all presented and compared in TABLE. 1.4.

TABLE 1- 4. SOLAR ENERGY HARVESTER USE POWER MANAGEMENT UNITS STATE-OF-THE-ART.

	TBioCAS17 [26]	Access18 [156]	JSSCC16 [155]	JSSCC15 [159]	VLSID16 [160]	Prime19 [163]
Vin (V)	0.25	1	0.25-0.65	0.45-3	0.33-0.405	0.25-1
Vout (V)	852m	1.49-2.825	3.8-4	3.3	1.01	1
Pin (W)	0.6m	-	113p-1.5µ	-	1.188m	
Pout (W)	1.65 µ	0.23m	-	<50 µ	1.01m	1.2-20.4m
Integrated Cap (F)	-	1n	1.5n	62.7p	500p	3n
Conversion ratio	×3.5	0.5-3	NA	4/3, 5/3,…8	x2.49-3	1.25-5
Efficiency (%)	67@0.31V	85.26	60@0.5V	81	82.4	80
Topology	AQP+LC+ Dickson	SP&SIDO	Moving-sum CP	Reconf. CP	Tree-top CP	ASP-based
Technology (nm)	180	180		180	180	650
Area (mm^2)	0.24	-	2.72	4	994.5	0.54
Frequency (Hz)	800k	5.8823k-1.1M	NA	140.6k - 1M	100k	4.4-57 M
No of Stage	3	1	3	4	1	NA

1.5. Proposed Power Management System (PMS) comprises with proposed control clock, novel start-up charge pump, and novel main DC-DC converter

I aim to achieve a power management system (PMS) with low input power from the *PV* cell in this design. The harvested energy from the *PV* cell is first power managed through an ultra-low powered boost start-up charge pump. It performs step-up DC-DC conversion to convert low input voltage to meaningful voltage. It can be implemented together with on-chip self-oscillating clock generators [166] and a non-overlapped clock to control the charge sharing clock (CSC) and charge transfer switches (CTS) of the start-up converter. Two CSC and CTS control operate well with charge pump and clock disabler to prevent constant power drawing from *PV* cells.

Secondly, the start-up charge up can store the energy output in the storage unit, in this case, a capacitor that can be external if it is for wearable devices or an integrated capacitor for implantable applications. It then acts as the second input source to our proposed main converter to consume minimum power across the main charge pump with high conversion efficiency. This reconfigurable main charge pump will provide the required voltage with sufficient current to the wearable application. Internal modules operate at different voltages depending on their operational functions, i.e., sensing, processing, recording, etc. The proposed system architecture is described in Fig. 1.9.

Reliable and efficient DC-DC conversion provides steady, regulated DC output voltage with a wide range of voltage conversion ratios (VCR) to maintain the highest conversion efficiency and power efficiency. It is especially true for applications requiring dynamic loading conditions. Moreover, low-power implantable and wearable biomedical devices require either batteries or novel energy harvesting techniques that extract energy from the surroundings or the body. However, the power extracted from these sources is the location and time-dependent [167]. Thus, self-powered devices need efficient and reconfigurable power converters to provide a wide range of dynamic output voltages.

This proposed main charge pump presents a novel 2-phase reconfigurable switched-capacitor (SC) DC-DC power converter that can provide different DC gains. The configured DC gains can simultaneously produce two different levels of VCRs and a single reconfigurable output. Compared to our previously proposed 4-phase design [156, 168], this 2-phase converter operates in 2-phase clock logic, which minimises multi-phase clock generator complexity. Moreover, a low-power mode is added, which means that our design is ideal for applications requiring an energy-saving scheme. Moreover, due to the dual output capability with different VCR, my proposed design is beneficial in a system with operating blocks requiring different operating voltages at the same time. Most importantly, the converter is self-powered, which means that an additional power supply is not necessary. It helps reduce complexity, chip size, and cost.

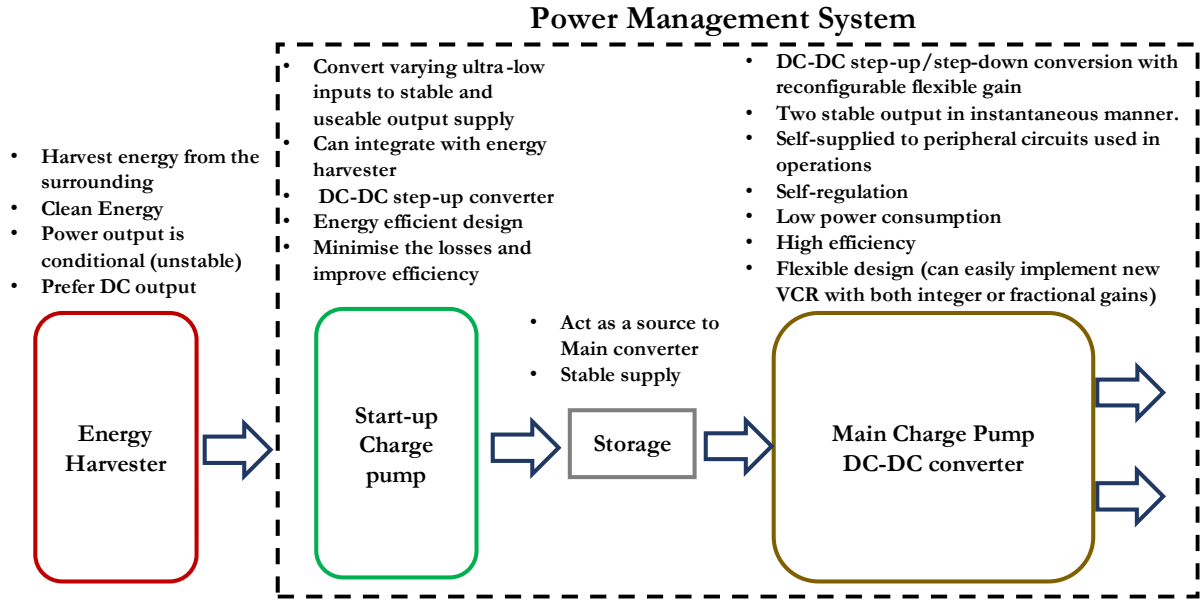


Figure 1- 9. A high-level diagram of the proposed power management system.

1.6. Research Objective

This research presents a novel reconfigurable switched-capacitor (SC) DC-DC power converter. The main charge pump can provide different gain modes capable of simultaneously producing two VCRs levels and a single reconfigurable output. Due to the dual output capability with various VCRs, this research contribution is beneficial in a system with operating blocks requiring different operating voltages at the same time. Most importantly, the converter is self-powered, which means that an additional power supply is not necessary. It has been achieved through a start-up converter which converter ultra-low input from energy harvester source to an operational standard transistor threshold to further power management in the main converter.

1.7. Application Example

One application example of the low-powered multiload smart contact lens micro system presented in [169, 170]. In this work, the intraocular pressure sensing microsystem (IOPM) for the smart contact lens is powered by the 0.07 mm^2 integrated solar cell harvester and stored in the 1 mm^2 thin-film battery. The thin-film 1 μA-hr Li battery was made by Cymbet Corporation [171] and yields 10 μA at 3 V. At the peak current battery can produce up to 35-45 μW, and the battery can last 28 days with no energy harvesting. Energy autonomy was achieved by 0.07 mm^2 solar energy harvester with a power consumption of 10 nW and recharge the battery to achieve a longer run time.

IOPM circuitry consists of sigma-delta capacitance to digital converter (CDC), static random-access memory (SRAM), microprocessor (μP), and wake up comparators (WUC) as shown in Fig. 1.10(a). In this literature, SRAM and CDC were directly supplied from the solar cell, which produces an open-circuit voltage of 0.45 V. The output of the solar cell (V_{Solar}) was connected to the 0.45 V power rail line of the 75% efficiency 8:1 Ladder topology switched-capacitor voltage regulator (SCVR). When V_{solar} goes beyond 0.45 V, the SCVR perform up conversion and recharge the battery. However, when the open circuit voltage drops below 0.45 V due to the incoming light condition, light irradiance of 100 mW/cm^2 [172] in outdoor sunlight yields 500 mV, it was then disconnected and become the load. Then the down conversion was made from a battery by SCVR and powered it for energy harvesting as well as to the rest of the circuits in the system. Note that V_{Solar} tends to drop to 460 mV in indoor lighting with an irradiance of 15 μA W/cm^2. The various harvested open-circuit voltage over charge power was illustrated and achieved up to 80 nW

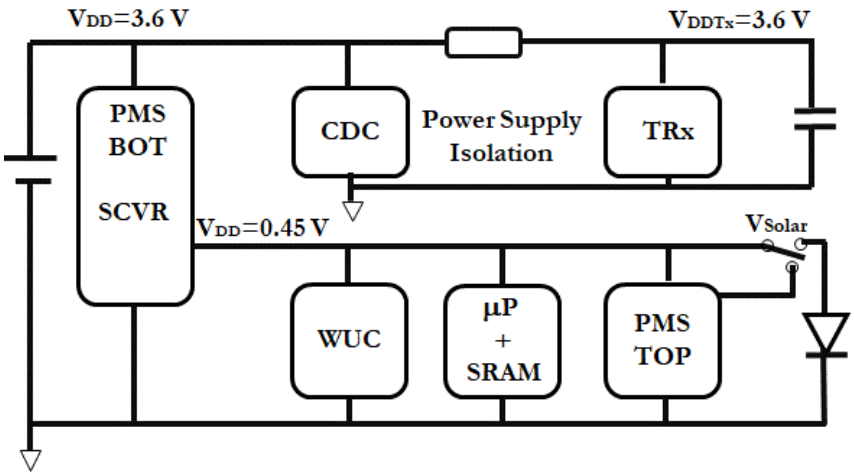
charging power. The achieved 0.08 μW on a sunny day for 0.07 mm² *PV* cell corresponded to a power of 1.14 μW/mm². Hence was suggested that either 1.5 hours of sunlight or 10 hours of indoor lighting harvesting time per day was required to supply the desire IOP sufficiently.

The high intermediate voltages (2.7 V, 1.8 V, 0.9 V and 0 V) are required for the power switches of SCVR during the operation. It was generated through the Level-connector (*LC*) from the battery. The transceiver (TRx) during the data transmission consumes 47-mW power, which was more than the battery can supply. Therefore, it was provided by an off-chip 1.6-nF capacitor instead.

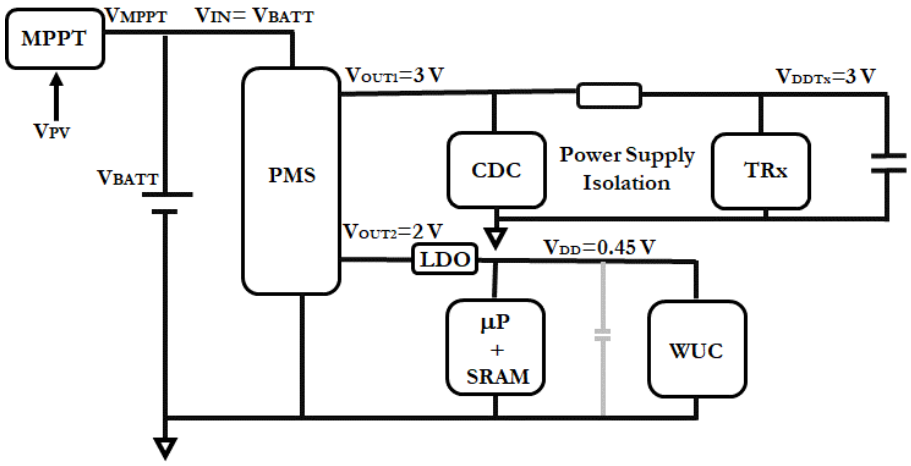
TABLE 1- 5. POWER BUDGET OF SMART CONTACT LENS IN [169, 170]

Active mode	Voltage	Current	Power	Time/Day	Energy/Day
CDC	3.6V	1.94μA	7μW	19.2s	134. 8μJ
μP + SRAM	0.45V	20nA	90nW	19.2s	1.7μJ
TRx	3.6V	13mA	47mW	134.4us	6.3μJ
Standby mode	**Voltage**	**Current**	**Power**	**Time/Day**	**Energy/Day**
CDC	3.6V	48pA	172.8pW	24hr	14.9μJ
μP + SRAM	0.45V	21.8pA	9.8pW	24hr	846.7nJ
WUC	0.45V	137.7pA	62pW	24hr	5.2μJ
TRx	0.36	9.16nA	3.3nW	24hr	285.1μJ

According to the power budget provided in the table, assuming the CDC can operate at 3 V, my proposed power management converter can be employed for this smart contact lens' loads as shown in Fig. 1.10(b).



(a)



(b)

Figure 1- 10. Example application of (a) Power management system in [169, 170] and (b) proposed power system in this thesis for a wearable smart contact lens.

The output of the energy harvester system can be stored in the battery (V_{BATT}). It is then used as the input supply (V_{IN}) to the proposed power management system (PMS) in Chapter 4. The PMS start-up charge pump will convert the low voltage of V_{IN} closer to 1 V. Consequently, the main charge pump in Chapter 3 Super Boost (*SB*) mode (×3, ×2) will generate (3 V, 2 V) and use 3 V power rail to supply CDC and the dropped down with either linear dropped out regulator circuit (LDO) [173] or the divider circuit with two series resistors.

IOP measurement was done every 15 min using CDC and measurement interval was controlled by the WUC, and then the measured data is processed by using µP & SRAM. Providing that supply towards CDC is independent to µP & SRAM, the PMS can operate in high conversion (*HC*) mode (×3.5) and supply 3.6 V to CDC (satisfy the original specification) and then after the switch to Low power (*LP*) mode (×2) to supply 2 V to µP & SRAM via the voltage drop-down medium. In switching *HC* and *LP* modes, the smaller capacitor can be charged in *LC* mode to power the WUC in *HC* mode. A similar smart contact lens for diabetic diagnosis and therapy can be seen in [174], whereas the IOP sensor and the sensor readout consumes 0-30 µW and 34.4 µW, respectively. However wireless module consumes about 2.3 mW.

In both cases, just as in the original literature, transmission exceeds the power capability due to the high current consumption and thus required to power from the external capacitor. The total current consumption, excluding the transmission module, consume less than 2 µA. The simulated result show PMS at 1 µA load in *HC* mode consume 49.3162 µW and 2.33 µW in *LP* mode. Similarly, *SB* mode at 1 µA load on both outputs consume 30.99 µW. Hence it is essential that the input supply can provide approximately 50 µW. The energy delivery requirement for PMS with active load will consume approximately (50 µW × 19.2s) 960 µJ. The high voltages required for the proposed PMS can be fed in from its output and do not require additional *LC* as described in the original literature.

Finally, low-powered electronics such as microprocessor [175, 176], accelerometer [177], EEPROM memory [178], temperature sensor [179], optical sensor [180], Photoplethysmogram (PPG) [181], pressure sensors [182], temperature and pressure sensor[182], heart rate monitor[183], analog front end [184]and so on, were commonly integrated in wearables applications; for instance, smart waist band [185, 186]. Finally, Fig .1.11 illustrates the power budget of each component.

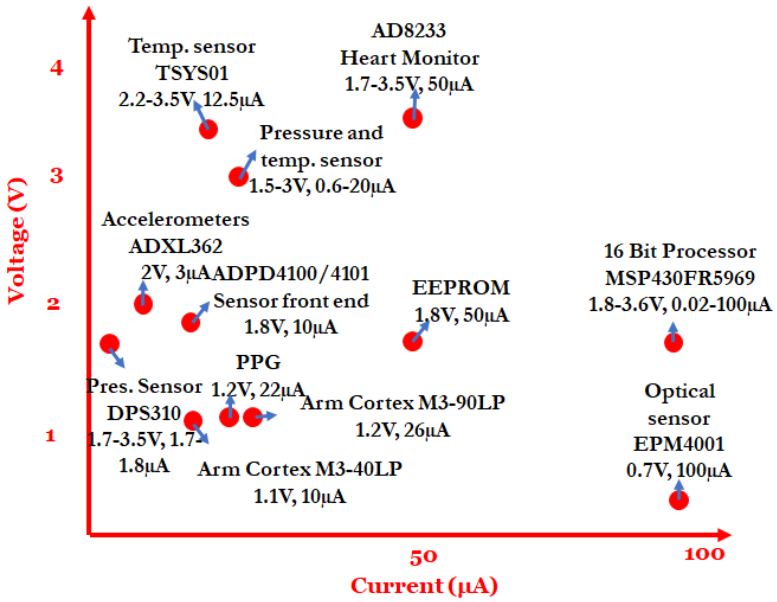


Figure 1- 11. Power budget of commonly used electronics in wearable technologies.

Choice of sufficient input source by using solar energy harvester:

The entire power management design to charge NiMH micro-battery with a series connection of four nano wire solar cells with area 1 mm² was presented in [187]. The power density of 4.5 µW/mm² was harvested for 0.8 V at 10% light intensity at *AM 1.5* [188]. It was reported that typical outdoor and indoor irradiance levels in cloudy wintertime were 25 µW/mm² [189] and 1 µW/mm² [190], respectively. In outdoor conditions, the maximum power point for the reported maximum efficiency of 1% at 0.32 V and total area of 1 mm² *PV* cell [188] is

$$P_m{}^{Outdoor} = Efficiency \times G \times A = 1\% \times 1\ mW/mm^2 = 10\ \mu W/mm^2 \quad (1.4)$$

$$P_m{}^{Indoor} = Efficiency \times G \times A = 1\% \times 1\ \mu W/mm^2 = 0.01\ \mu W/mm^2 \quad (1.5)$$

Whereas input light irradiance is G (W/m²) and the A(mm²) represents the surface area of the solar cell.

The report in [191] discussed that among the different energy harvesting techniques, a solar cell could produce 100-1000 µW/mm² to sufficiently power micro and nano system. The survey of operating characteristics of other solar cells in [192] suggested that the efficiency of different solar cells is typically 5-16%. Hence-

$$P_m{}^{Outdoor(max)} = Efficiency \times G * A = 5\% \times 1\ mW/mm^2 = 50\ \mu W/mm^2 \quad (1.6)$$

$$P_m{}^{Outdoor(min)} = Efficiency \times G \times A = 16\% \times 1\ mW/mm^2 = 160\ \mu W/mm^2 \quad (1.7)$$

$$P_m{}^{Indoo(max)r} = Efficiency \times G \times A = 5\% \times 1\ \mu W/mm^2 = 0.05\ \mu W/mm^2 \quad (1.8)$$

$$P_m{}^{Indoor(min)} = Efficiency \times G \times A = 16\% \times 1\ \mu W/mm^2 = 0.16\ \mu W/mm^2 \quad (1.9)$$

On the other hand, for the flexible silicon solar cell typically range between 6-8 % efficiencies [193].

$$P_{m\ Outdoor(max)} = Efficiency \times G \times A = 6\% \times 1\ mW/mm^2 = 60\ \mu W/mm^2 \quad (1.10)$$

$$P_{m\ Outdoor(min)} = Efficiency \times G \times A = 8\% \times 1\ mW/mm^2 = 80\ \mu W/mm^2 \quad (1.11)$$

$$P_{m\ Indoo(max)r} = Efficiency \times G \times A = 6\% \times 1\ \mu W/mm^2 = 0.06\ \mu W/mm^2 \quad (1.12)$$

$$P_{m\ Indoor(min)} = Efficiency \times G \times A = 8\% \times 1\ \mu W/mm^2 = 0.08\ \mu W/mm^2 \quad (1.13)$$

Therefore, the harvested power range can vary between 60-80 μW/mm² for outdoor conditions and 0.06-0.08 μW/mm² for indoor lighting can be expected. In summary, the available energy of the solar cell in the worst-case scenario 1.8 mJ per day (0.05 μW/mm² × 10 hr), is well within the power budget of PMS 960 μJ to supply the required loads. In [185, 186] reported using eight amorphous silicon solar cells in parallel to power the wearable bracelet and smart watch. The Sanyo energy solar cells *AM 1471CA* reportedly yields 1.6 V at 15 mA in sunlight and 1.9 V at 100 μA in indoor condition.

Single solar cells produce low output voltages. In [26, 194] CMOS structure, single-junction diode provide 0.3-0.4 V. With the varying thickness (0.5-1.5 μm) of GaAs nanostructured solar cell under 1 sun illumination had reportedly produce an open-circuit voltage (V_{oc}) of 0.417-0.851 and current density of 11.4 mA/cm². However, the higher voltage output can yield depending on the materials and configurations of *PV* cells [195]. The reported V_{oc} in comparison varies from 0.49-5.462 V.

Moreover, Organic *PV* (OPV) cells were used for retinal applications due to their sensitivity to NIR light [196]. The reported V_{oc} under simulated sunlight (AM1.5G, 100 mW cm²)for single-junction *PV* cells was 0.67 V, and tandem OPV cells based on a bulky heterojunction was 1.31 V.

1.8. Thesis Outline

This research presents a novel reconfigurable switched-capacitor (SC) DC-DC power converter. The main charge pump can provide different gain modes capable of simultaneously producing two VCRs levels and a single reconfigurable output. Due to the dual output capability with various VCRs, this research contribution is beneficial in a system with operating blocks requiring different operating voltages at the same time. Most importantly, the converter is self-powered, which means that an additional power supply is not necessary. It has been achieved through a start-up converter which converter ultra-low input from energy harvester source to an operational standard transistor threshold to further power management in the main DC-DC converter.

This Thesis is organised as follow-

Chapter 2: Presents the charge pump DC-DC converter based on single input dual outputs by using the 4-phase topology. The statement of why a multi-output charge pump is suitable for the multi-load system has been discussed. Followed by a brief literature review of the existing multi-output design and its research gap. Then proposed methodology, the circuit design and the performance analysis of the novel single-input dual out-put SIDO charge pump are presented.

Chapter 3: Demonstrates the charge-pump DC-DC converter based on single-input dual-outputs and single-output by using a 2-phase topology. This chapter proposed the novel SISO and SIDO reconfigurable converter design in one charge pump.

Chapter 4: Full switched-capacitor-based power management system comprises start-up charge up and main DC-DC converter from Chapter-3. The implementation and the proposed system results were analysed and compared with the state-of-the-art.

Chapter 5: Summary of the thesis and direction of the future plan is going to discuss in this section. Finally, my vision and recommendation of necessary development in future charge pump technologies are discussed in the conclusion remark.

CHAPTER 2: CHARGE-PUMP DC-DC CONVERTER BASED ON SINGLE INPUT DUAL OUTPUTS

2.1. Motivation

2.1.1. Research gap for Single input single-output (SISO) state-of-the-art

The integrated monolithic chip converter or power management system is based on the charge pump designs described in TABLE 2.1. Examples include the Dickson charge pump [27, 197] and cross-coupled design [198] for step-up conversion purposes or the use of the hybrid charge pump together with an energy harvester [199]. However, only the integer gains can be configured in charge pump design, making them inconvenient for applications with varying inputs. Whenever there is a change in input voltage, the circuit may need to be readjusted to keep up with the high conversion ratios. Therefore, series-parallel converters [200] that can configure non-integer gain values and reconfigure DC gains [133, 201]are becoming more popular.

TABLE 2- 1. INTEGRATED POWER MANAGEMENT DESIGNS.

Ref	Configuration	C_{fly} (F)	Mode	Input (V)	Output (V)	Gain	Max-Efficiency (%)	Power (W)
[27]	Dickson	40p×4	Boost	0.55-0.7	1.1-3.4	4-stage	66	0.1-32µ
[198]	Cross-coupled	630p×6	Boost	1.2	4.8	3-stage	80.2	479µ
[199]	Dickson+Cross	20p×9	Boost	0.45-0.60	4	6-stage	51.7	-
[200]	Series-parallel	1µ×4	Buck	1.6-3.3	0.5-3	Multiple	91	250m
[201]	Series-Parallel	1µ×3	Boost	1.4-3	4.8	Multiple	82	2.4-48m

Present series-parallel converters are reconfigurable. Sometimes, a specific load operating at the highest voltage requires maximum power from the converter for an extended period. Thus, the converter ends up driving at its optimum gain almost all the time to provide sufficient voltage to all the present loads connected to a single output line. Moreover, since all the loads are connected to a single output line, small loads with low operating voltages require further drop down using additional Linear Drop Out (LDO) circuits. It leads to power losses across different components.

Single input single output converter designs are conventional as well as popular. Even the reconfigurable converter aims to drive to the optimal voltage to adapt to the dynamic change of load. It is then branched out to supply different voltages across the LDO since wearable and implantable devices consist of other functional operational electronic modules which operate at different voltages. For example, if the converter provides 3 V and system-on-chip loads require 1V for the sensors and 3 V for LEDs, then the converter output voltage is compactable for the LEDs, but not so much for sensors and digital modules. Moreover, since power loss is $\frac{V^2}{R}$, having a multi-output converter can greatly benefit applications consisting of electronic modules with different operational voltages, as shown in Fig. 2.1.

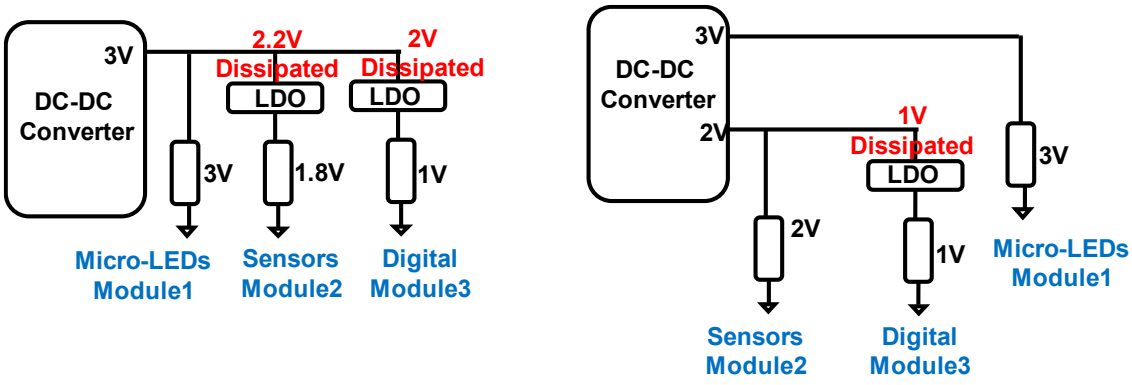


Figure 2- 1. Example of the energy-efficient delivering method in comparison of (a) SISO design (b) SIDO design.

2.1.2. Research gap for Single input dual output (SIDO) state-of-the-art

To overcome these issues, researchers have presented SIMO converter designs. The advantage of having a multioutput converter is discussed in [202, 203]. The existing SIMO converter's underlying requirement [45, 159, 167, 204-206] is their gain configuration restricted to either fixed or limited to step-down conversions. The capability of a 4-phase converter in comparison with dual output sand single output state-of-the-art is presented in TABLE 2.2.

TABLE 2- 2. NOVELTY AND FUNCTIONALITY COMPARISON WITH STATE-OF-THE-ART.

	[202]	[45]	[206]	[204]	[207]	[208]	This work
No. of Output	2	2	2	2	1	1	2
Conversion type	SD	SD	SU	SD	SU, SD	SD	SU
Self-power	External	External	External	External	External	Yes	Yes
Regulation	Internal	Internal	External	Internal	-	-	Internal
Regulation method	PFM	Interleave	External Cap	Hysteretic	-	-	Interleave
Reconfig	No	No	No	No	Yes	Yes	Yes

The implementation of a two-rung SC ladder circuit topology for several discrete power modes for a power-aware application is presented in [45, 205]. Three different voltages regions are generated spontaneously by uneven 3-flying capacitors in each cell sharing charge with identical sub-cell, which operates in anti-phase, across odd number switches in two-phases mode. The ripple performance of all three sub voltages outputs, super-threshold (V_{dd}), near-threshold ($2V_{dd}/3$), and sub-threshold ($V_{dd}/3$), are further enhanced by N times interleaving. It increases the sub-cells to N times to reduce the output ripples and compensates for the increase in the chip area by reducing each network's capacitors' size by 1/N factors. Further optimisation is done by using unequal flying capacitors instead of conventional equal capacitances across the network. The large capacitor is used for those at the large load region (V_{dd}) twice much of the bottom region ($V_{dd}/3$).

However, although the total area remains the same, the complexity of design for **multiple interleaving growth as the number of sub-cells increases**, the demand for considerable change in physical mechanics rather than optimising through system design is not ideal for implant power management design. Secondly, a change in the charge pump capacitor's size due to expanding the sub-cells will require a system to readjust the operating frequencies to discharge/charge and fully install an additional phase controller. Thirdly, due to the **fixed ratio**, the voltage conversion ratio dropped once the input voltage change. It is because the way the charge pump is configured depending on the intermediate note voltage. Discussed [45, 205] uses the two-to-Nth symmetric interleaving method. The converter is not reconfigurable, and gain configurations are limited to step down (SD) conversions only. Moreover, **additional powering is required for peripheral circuits,** which are necessary for circuit operation.

Other converter designs that use interleaving regulation schemes, such as two symmetric paths interleaving of two crossed-coupled converters [18, 19], are **limited to integer gain; fixed DC gain** output is bond to the total number of stages. Similarly, the switched-capacitor approach step-up converters such as Dickson's converters [209-214] and Cross-coupled converters [109, 215-218] produce fixed integer gain ratios. Step-up gain conversions are directly proportional to the number of stages. Therefore, increasing the step-up gains mean an increase in power switches and capacitors in the power stage network.

Moreover, A dual output converter integrated design producing ($2V_{in}$ and $-V_{in}$) for liquid crystal display (LCD) application is presented in [206]. Their proposed design was fabricated in 0.13 μm technology. This work uses dual-side-dual-output (DSDO), which enables simultaneous step-up and step-down conversions possible. A total number of 4 capacitors with two on-chip and two off-chips were used. During the operation, the phase 1 and 3 are the charging phase of the charge pump. Then, the charged capacitor C1 from phase 1,3 is discharged to C7 in series with input source voltage to produce the output voltage ($2V_{in}$).

Meanwhile, the voltage generated at C8 in phase 2 by charged capacitor C2 from phase 1,3. Since at phase 3 it goes back to charging again, the charged capacitor C1 is delivered to C8 and C2 to C7 at phase 4. Therefore, there are always two phases of charging and the other two phases for energy produced to the output. The downside of this design is **the fixed-gain dual outputs**, two independent voltage inverters, and voltage doublers with the same number of charge pump capacitors with switches can be replaced. On the other hand, single-output designs [207, 208] are usually reconfigurable. Furthermore, discussed [206] had to rely on the **external capacitor to regulate** the output and the operational process. Integrating passive devices such as capacitor contribute directly to a **chip area and cost**.

Similarly, the capacitive DC-DC step-down converter governs by a traditional hysteretic controller used simultaneous dual output design is fabricated in 90 nm CMOS technology and presented in [204]. From the 1.2 V input battery, by using the four charge pump capacitors and switches, two spontaneous dual outputs of 0.755 V and 0.32 V are gathered and have displayed efficiencies between 68.6-75.3%. However, whenever the input voltages change due to the battery life spans degrade, the conversion efficiency will drop from the fixed gain ratio design.

The following objectives are desirable and should be comparable in the state-of-the-art in result section –

- To achieve a high power efficiency of at least 68% compared to state-of-the-art in result sections.
- To achieve output closer to the target voltage conversion ratio (VCR) relative to the input voltage and conversion gain.
- To achieve reconfigurability and adjustable gain, this converter is designed to configure up to 6 gains which can perform both step-up and step-down conversions simultaneously.
- To achieve stable Load regulation/Line regulation-i.e., the relative change of output voltage relative to input and the gain ratio (Line regulation) and being able to maintain minimum output variation when the load changes (Load regulation). In the result section, a linear output change graph can be observed.
- To be able to Self-regulate-i.e., being able to internally regulate instead of using the large filter capacitor to enhance ripple immunity- shown up to 95 mV ripple in state-of-the-art comparison in result sections.
- A self-powered converter that is integrable with an energy harvester is desirable. Small scale (few millimetres) energy harvesters can harvest around few micro-watts (up to 4 V, 100 μA electronics has been summarised in Fig. 1.11). Hence power conversion of converter for low-powered applications should be able to operate within a micro-watt power scale.
- Converter must be area-efficient as fabricated chip area contributes directly to the cost. The state-of-the-art converters are usually millimetre scales.
- Targeted output power of few micro-watts for low-powered electronics should be able to produce micro watt over millimetre scale charge pump chip area.

2.1.3. Contribution of 4-phase converter design

This work introduces a miniaturised power management DC-DC converter design, an integrated on-chip power system for wearable devices. An inductor-less, switched-capacitor, DC-DC converter design is proposed to remove the involvement of bulky inductors. Moreover, power management is obtained using series-parallel connections of flying capacitors via MOSFET power switches. These are all digitally controlled using digital modules, as shown in Fig. 2.2. The *PV* cell and its energy storage device are used as primary energy inputs. Depending on the power conversion unit's load requirements, the proposed system performs both step-up and step-down voltage conversions simultaneously using the novel 4-phases rotation scheme with four flying capacitors. The appropriate gain pairs are chosen accordingly to produce a different gain of step-up conversion simultaneously. These various VCR gain pairs can be categorised into four different modes (Normal, High, Double Boost, and Super Boost). This novel topology, which uses a single-input-dual- output (SIDO) design, is inspired by the single-input-single-output (SISO) 3-phase rotation topology presented in [129], whereby one idle capacitor in every charging phase is always present. Two outputs need to be produced independently to achieve the same objective. It will require either doubling the SISO converters [219], which can only generate one gain at a time or stacking the capacitors as a capacitor bank [220].

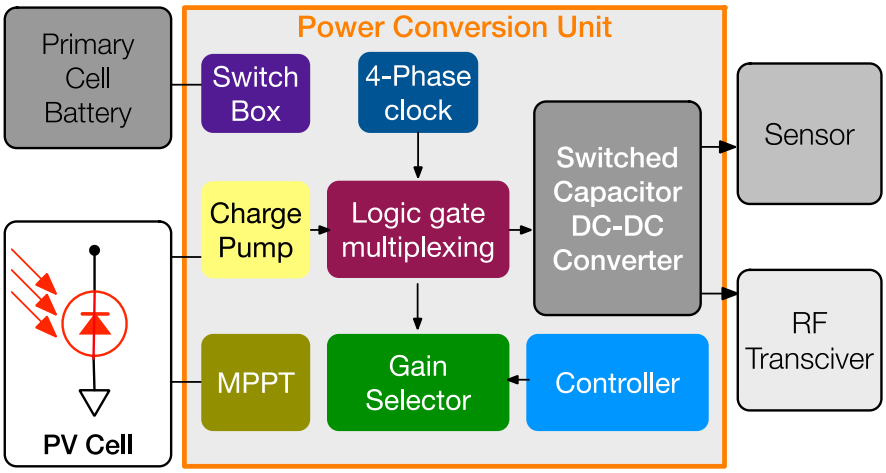


Figure 2- 2. Block Diagram of power conversion for energy harvesting using photovoltaic cells in Implantable applications.

The following objectives this chapter aims to contribute:

- Single Input Dual Output (SIDO) converter design.
- The converter can produce a dual output with a different set of gain pairs spontaneously.
- Simultaneous dual output can configure both step-up (boost) and step-down (buck) conversion simultaneously.
- The gain configuration is both integer and non-integer (fractional) gains.
- This dual output converter is reconfigurable.
- In every configuration, there is no idle operational capacitor.
- Aim to achieve a high power efficiency of 80-90% for simulation results. At least 10% less efficiency can be expected in the measurement result.
- Produce various voltage conversion ratios (VCR).
- Outputs are regulated by using the interleaving scheme.
- Only four capacitors are needed in total in the power stage network and agree with the number of integrated capacitors used in state-of-the-art.

2.2. *System Description*

Using a switch-mode regulation, this converter illustrated in Fig. 2.3(a-b) has achieved the reconfigurable dual outputs (V_{out1}, V_{out2}), which can produce regulated voltage pairs of both boosting or boost and buck at the same time. There are four different gain modes, each representing a set of voltage gains generated from two internal conceptual networks (*Net0, Net1*). Various DC gains are configured in each network by constructing series-parallel configurations of capacitors and switches, as suggested by methodology. Since its operation changes follow each capacitor's positions in every phase, the corresponding internal outputs (O_{ut1}-O_{ut4}) also change accordingly. Henceforth, these internal outputs shall be referred to as "discontinuous" outputs (O_{ut1}-O_{ut4}), whereas "continuous" output refers to two-outputs (V_{out1}, V_{out2}) connected to external loads. Four DC gain modes can be configured in (V_{out1} and V_{out2}), each consisting of two different voltages. Therefore, discontinuous-to-continuous switches or rectifier circuits (peak detector) can be employed to correspond to the connection of internal outputs (O_{ut1}-O_{ut4}) to external loads (V_{out1} and V_{out2}) at different phases.

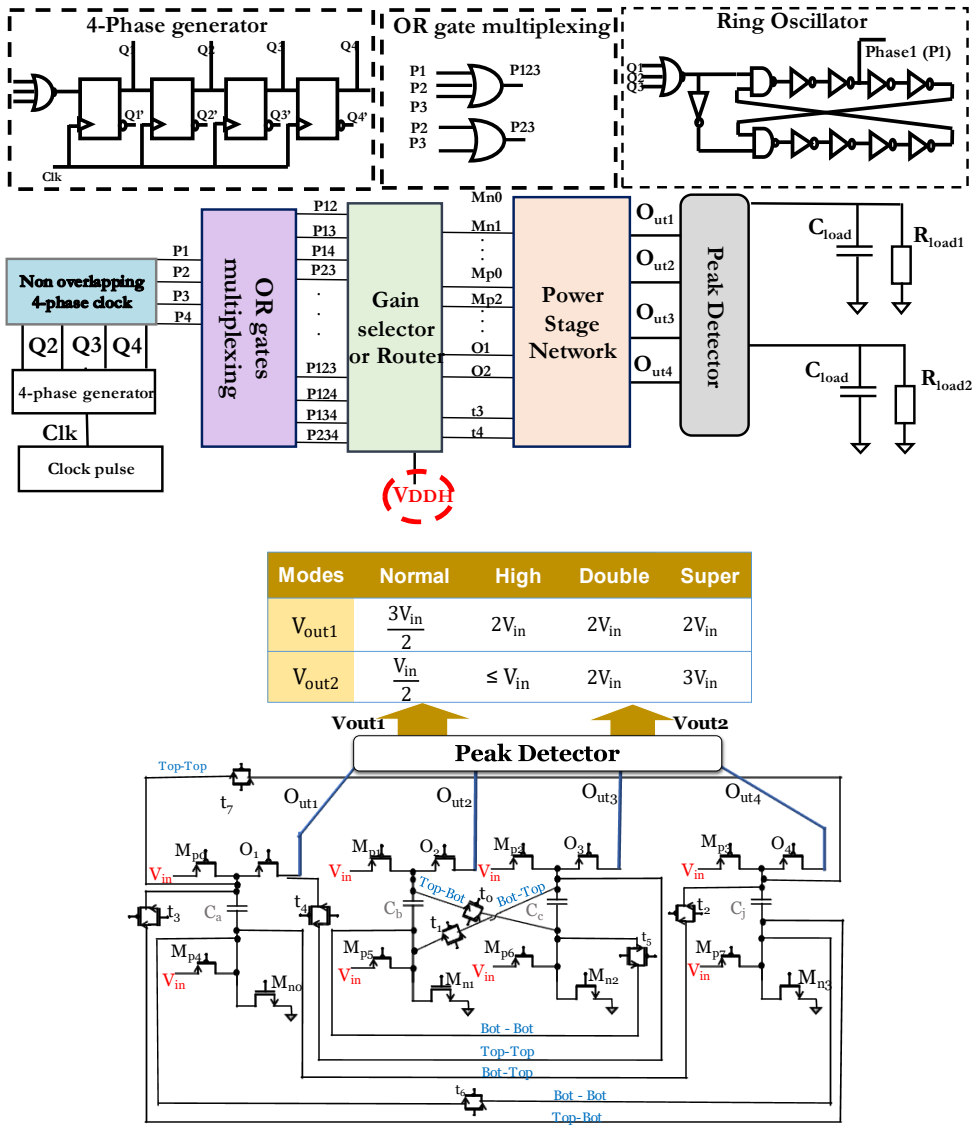


Figure 2- 3. (a) Overall schematic diagram of the proposed converter and the crucial blocks are highlighted in colours. (b) Circuit level diagram of the power stage network in which a non-overlapping 4-phases clock digitally controls the operation.

The four D-flip flops are constructed to produce a 90-degree phase shift for four different phases at every rising edge of the input clock signal and are further enhanced by passing it through ring oscillators. Thereby, the power stage's transistor switches benefit from non-overlapping 0.1-ns dead time intervals between the consecutive clock phases by eliminating the signal leakage during the switching and full charge settling of the SC network clock cycle.

The outputs of non-overlapping clocks are OR-gate multiplexed to ensure that all the possible 4-phases pairs are accessible for the next block router module. In the proposed methodology, the selected transistors are active for the present clock logic. Some switches can be reused for successive clock logic or the one after next for all 4-phases logics. Thereby even the new gain configuration addition in the future can benefit from it. The model's selection or a pair of gains changes when the load demands higher voltages at the output. All the transistor addresses for four different phases logics are registered and reconfigure the power stage network under the proposed methodology when selecting gain modes to change.

The configuration of four integrated 1-nF capacitors in the power stage is controlled through 20 switches (4-Transmission gates, 4-NMOS, 12-PMOS). The power switch protocols are carefully designed to ensure that all the power stage (O_{ut1}-O_{ut4}) internal outputs are regulated at all 4-phases for all gain modes. It is due to multiple ways to route for the same logic. Each offers a different resistance path along with the switches—the various resistances across the path leading to slight variations in ΔV at outputs. The obtained design ensures the optimum route with minimum on-resistance and maintains the symmetric R_{on} values for all 4-phases are accessible for consistency of outputs level through simulations.

Finally, all available gain pairs for Normal mode, High mode, Double Boost, and Super Boost mode of our proposed converter can be summarised in TABLE 2.3-

TABLE 2- 3. RECONFIGURABLE GAIN PAIRS OF THE PROPOSED CONVERTER.

Modes	Normal	High	Double	Super
V_{out1}	$\frac{3V_{in}}{2}$	$2V_{in}$	$2V_{in}$	$3V_{in}$
V_{out2}	$\frac{V_{in}}{2}$	$\leq V_{in}$	$2V_{in}$	$2V_{in}$

2.3. System Methodology

The proposed converter is designed to configure into four different gain modes when using a switch-mode regulation, each with two different simultaneous regulated stable dual outputs (V_{out1}, V_{out2}). The power stage network is divided into two internal conceptual networks (*Net0, Net1*), and boost operation will perform in *Net0* while buck or boost output produces at *Net1*. Therefore, in every clock cycle, there will be two active corresponding internal outputs at (O_{ut1}-O_{ut4}), as illustrated in Fig. 2.4. These internal outputs will then connect to High and Low/High loads through a peak detector. As a result, two loads connected to the main charge pump will receive steady current flow, regulated output, a low ripple from four phases interleave, and lower redistribution losses since the output condition remain the same at all 4-phases.

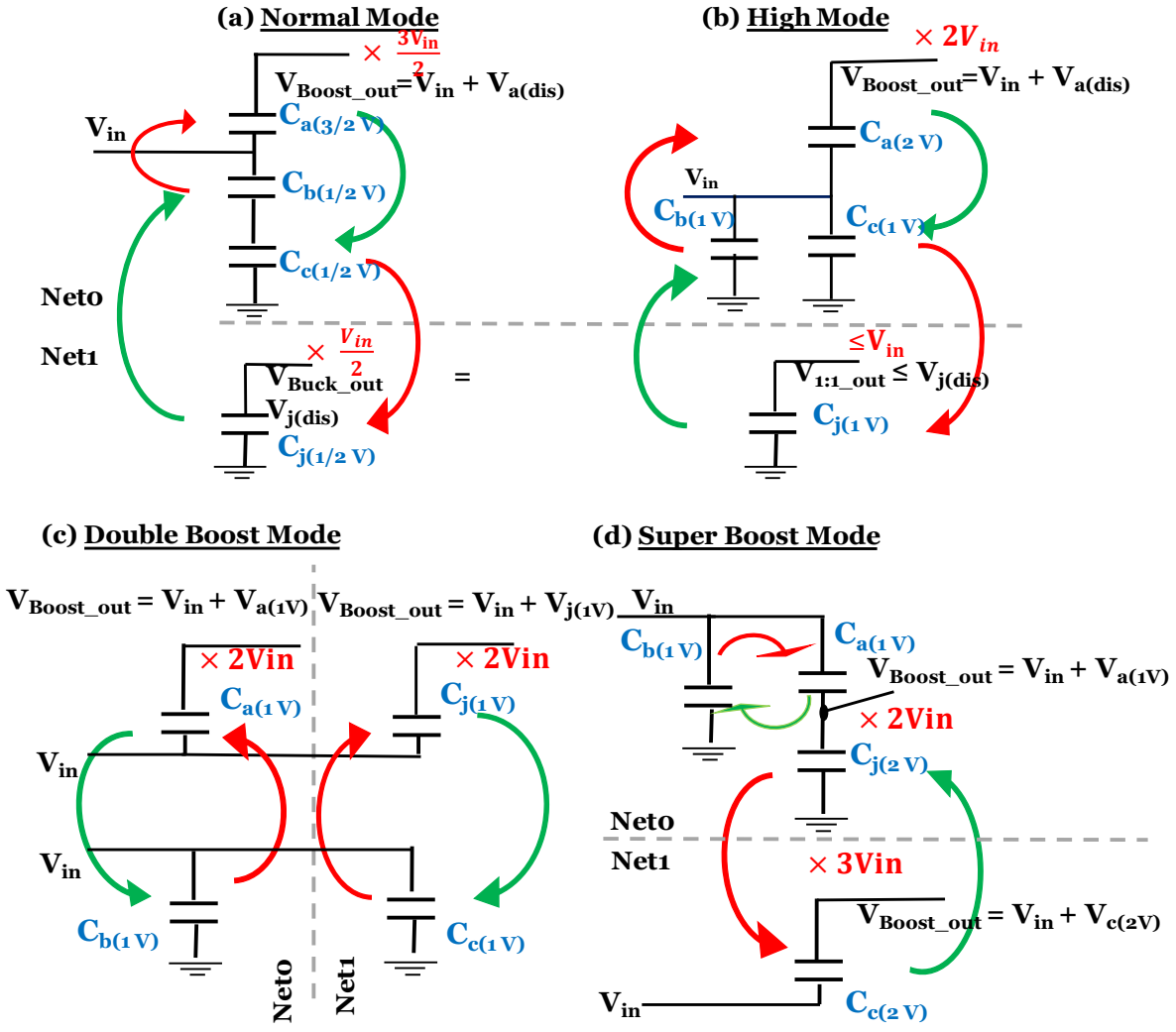


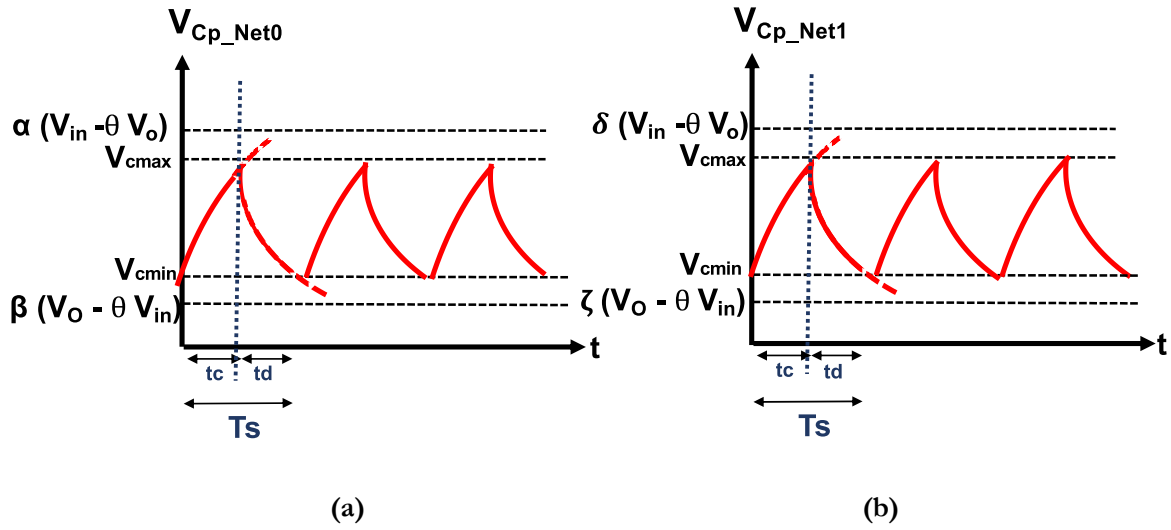
Figure 2- 4. The methodology of (a)Normal Mode, (b)High Mode, (c)Double Boost Mode, and (d)Super Boost Mode configurations.

2.3.1. Summary of Output Voltages and Output Power losses

The first-order differential equation of charging and discharging part of the R-C circuit in Laplace and convert it back to the time domain in Inverse Laplace, a final voltage $V_c(t)$ is the sum of the initial charging voltage $V_c(0)$ and the input voltage V_{in}. The total switching time (t) with R-C time characteristic in Equation. (2.1).

$$V_c(t) = V_c(0)e^{-\frac{t}{RC}} + V_{in}(1 - e^{-\frac{t}{RC}}) \tag{2.1}$$

According to the four modes' circuit configuration, the coefficient of voltage values for each charged pump capacitor tends to charge-discharge to, and actual voltages of capacitors (V_{max}, V_{min}) in Fig. 2.5 varies and are defined in TABLE 2.4.



(a) (b)

Figure 2- 5. Charging discharging characteristic graph of flying capacitors in two internal networks (a) Net0 and (b) Net1.

TABLE 2- 4. VARIABLE VALUES FOR FIGURE. 2.5.

Normal mode	High mode	Double Mode	Super Mode
α=1/2, β=1, δ=1/2, ζ=1, θ=0	α=1, β=1, δ=1, ζ=1, θ=1	α=2, β=1, δ=1, ζ=1, θ=1	α=1, β=1/2, δ=1, ζ=1, θ=1

The derivation of output voltages for all modes is described in Appendix 1. By taking the total amount of charge for steady-state charging and discharging voltage-time ΔQ_{Mode} for Normal mode, High mode, Double Boost, and Super Boost are $\frac{I_0}{2\,f_s}$, $\frac{I_0}{3\,f_s}$, $\frac{I_0}{4\,f_s}$ and $\frac{I_0}{2\,f_s}$, respectively. The gain ratio multiplier (k) represents the desire voltage gain ratio relative to the input voltage. The output voltage for individual modes can be generalised as:

$$V_{boost,buck\_Mode} = kV_{in} - \frac{\Delta Q_{Mode}}{\alpha\, f_s C_p}\left(\frac{1}{1-e^{-\frac{t_d}{T_d}}} + \frac{1}{1-e^{-\frac{t_c}{T_c}}} - 1\right) \tag{2.2}$$

where t_d represents discharging time and t_c represents the charging time. R-C time constant (T_d and T_c) are subjected to on-resistance along the path of charging-discharging R_{on}, α is the charge multiplier that varies over different modes and flying capacitor C_p which has the most dominant capacitance in the power stage. The conduction power loss can be expressed from the second term of Equation (2.2). Multiplying by the output current I_o gives Equation (2.3):

$$P_{conduct\_Mode} = \frac{I^2_{o\_boost,buck}}{\alpha\, f_s C_p}\left(\frac{1}{1-e^{-\frac{t_d}{T_d}}} + \frac{1}{1-e^{-\frac{t_c}{T_c}}} - 1\right) \tag{2.3}$$

$$P_{sw\_Mode} = f_s \sum_i C_{gsi} V^2_{gsi} \cong f_s C_{OX} \sum_i W_i L_i V^2_{gsi} \tag{2.4}$$

Equation (2.4) represents switching power loss (P_{sw}), which is influenced by charge-discharge mechanisms of a gate-source parasitic capacitance of MOSFET transistors (C_{gs}), the frequency of switching (f_s), and the gate-source voltages (V_{gs}) of individual switches along the path [152]. The other variables are the width (W_i) and length (L_i) of individual transistors along the route and the transistor gate-oxide capacitor (C_{ox}), which has the approximate value of 8.31 fF/μm^2 for 0.18 μm technology. For a steady-state, due to the symmetric nature of output waveforms in every mode, redistribution loss is considered by taking KQL of one phase operation. Whereas present phase discharge capacitor (Cd), switching time (T_s), and the number of parallel connections (n) with Cd are described in Equation (2.5):

$$P_{redis\_Mode} = \frac{I^2_{o\_boost,buck}\, T_s}{4\, C_d} + \frac{I^2_{o\_boost,buck}\, T_s}{8(nC_d + C_{load1,2})} \tag{2.5}$$

2.4. Circuit Implementation

The circuit design is implemented in a standard 0.18 μm AMS CMOS technology, and the overall system diagram is depicted in Fig. 2.6.

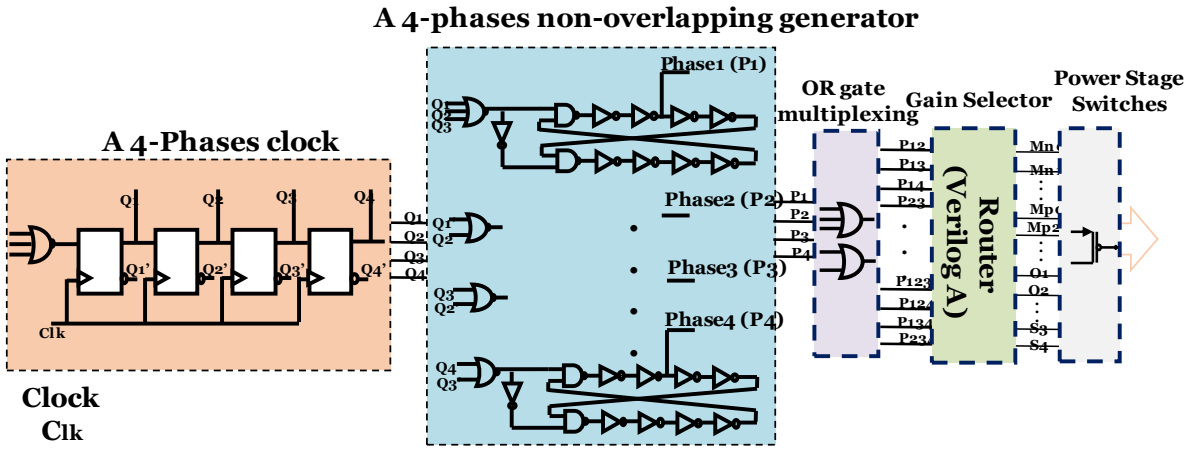


Figure 2- 6. The system overview of the 4-phase charge pump's digital controller.

2.4.1. Implementation of Power stage network

The power circuit network comprises 20 switches to configure four integrated 1-nF capacitors from the analogue library in series-parallel positions. The operating frequencies for different modes are chosen to certify that 1-nF charge pump capacitors are fully charged/discharged over MOSFET switches. However, only a few power switches are required to configure the gain mode selection, as shown in Fig. 2.7(a-d). To charge-discharge the capacitors, the power switches have been implemented by PMOS and NMOS transistors. The transmission gates are employed due to their bi-directional charge transfer, switching fast on-off transitions, small turn-on resistance to minimise conduction power loss, and avoiding charge injection or clock feedthrough on both capacitors connected in the series arrangement. By keeping the minimum length for all transistors, the width of PMOSs is 60 μm, and 20 μm for NMOSs is used.

There are 20 switches in total (4 Transmission gates, 4 NMOS, 12 PMOS). However, only 7-power switches for Normal mode and 8-power switches are required for High mode. For instance, they are used in every clock phase. The circuit-level configurations of the charge pump for all four gain modes are illustrated in the following sections. The power switch protocols are designed to have all internal outputs of the power stage (O_{ut1}-O_{ut4}) produce output consistency results at all 4-phases at all time resulting in minor variations in ΔV at outputs. It is chosen through minimal and maintains the symmetric on-resistance R_{on} values path through simulation.

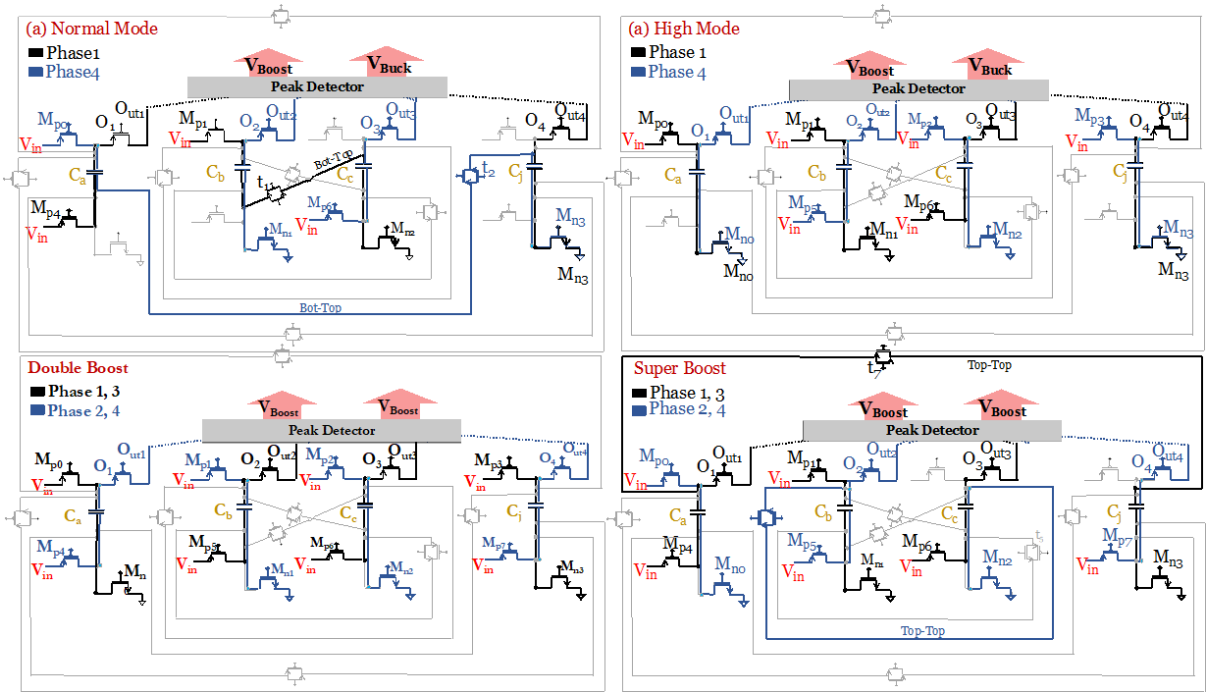


Figure 2- 7. The operation phases of the power stage network at 4-different modes: (a) Normal Mode, (b) High Mode, (c) Double Boost and (d) Super Boost.

2.4.2. Implementation of 4-phase clock

The four D flip-flops are constructed in Fig. 2.8(a) to produce a 90-degree phase shift for four different phases at every rising edge of the input clock signal and is further enhanced by passing it through ring oscillators Fig. 2.8(b). Thereby, the power stage's transistor switches benefit from non-overlapping of approximately 0.1 ns dead time intervals between the consecutive clock phases by eliminating the signal leakage during the switching and full charge settling of the SC network in every clock cycle. It is shown in Fig. 3.9(a-b). Moreover, note that the clock signal is generally at 'high', and hence overlapping two consecutive low clock signal inputs at the same transistor should be avoided to eliminate leakage current.

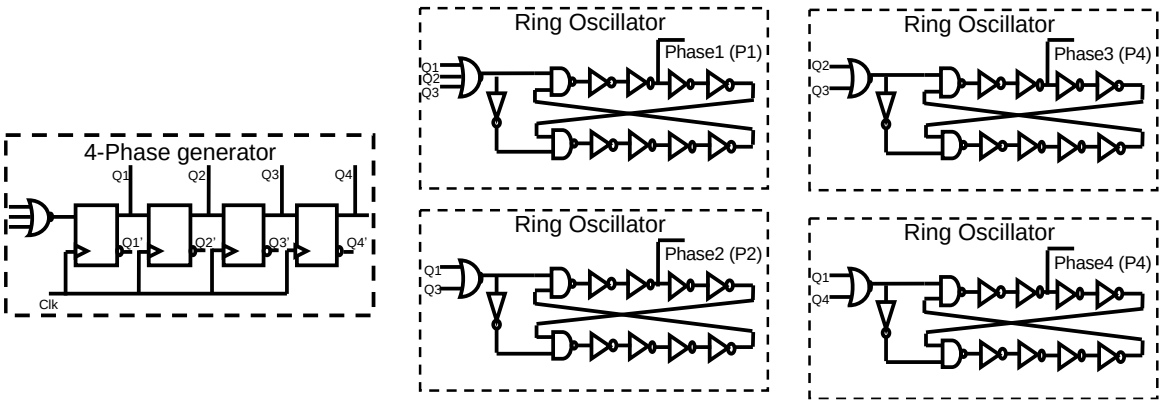
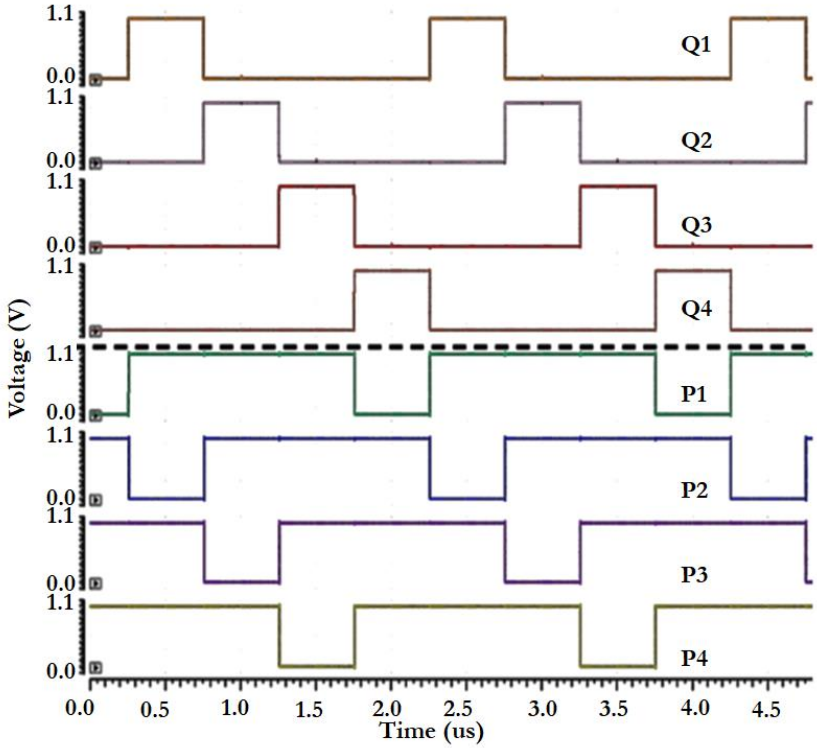
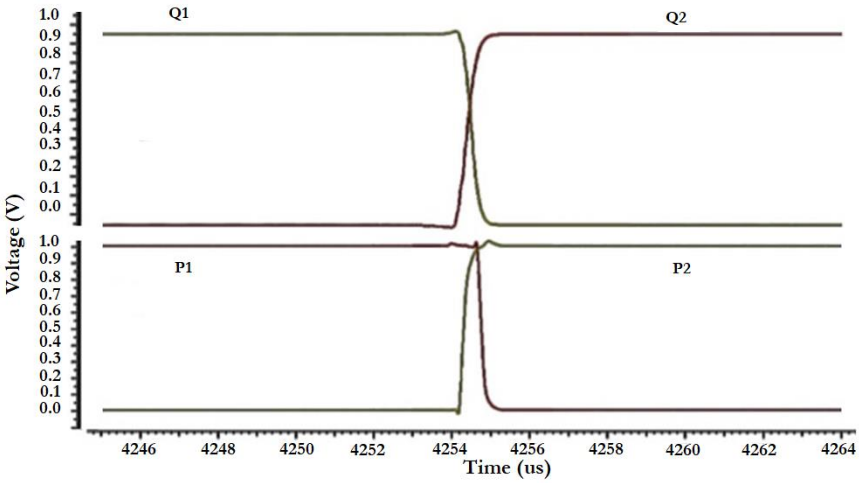


Figure 2- 8. (a) The 4-phase clock generators and (b) ring oscillator circuits for non-overlapping clocks.



(a)

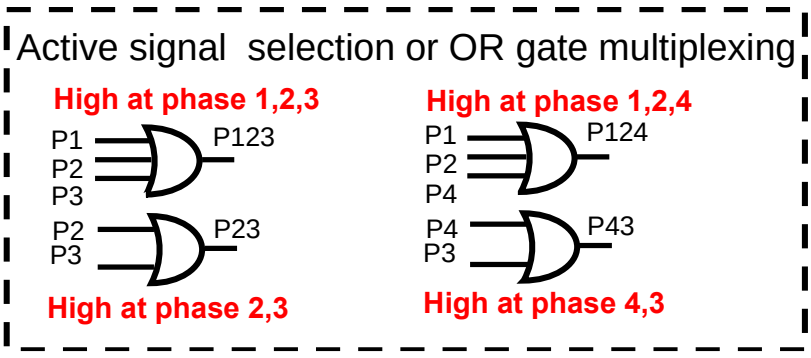


(b)

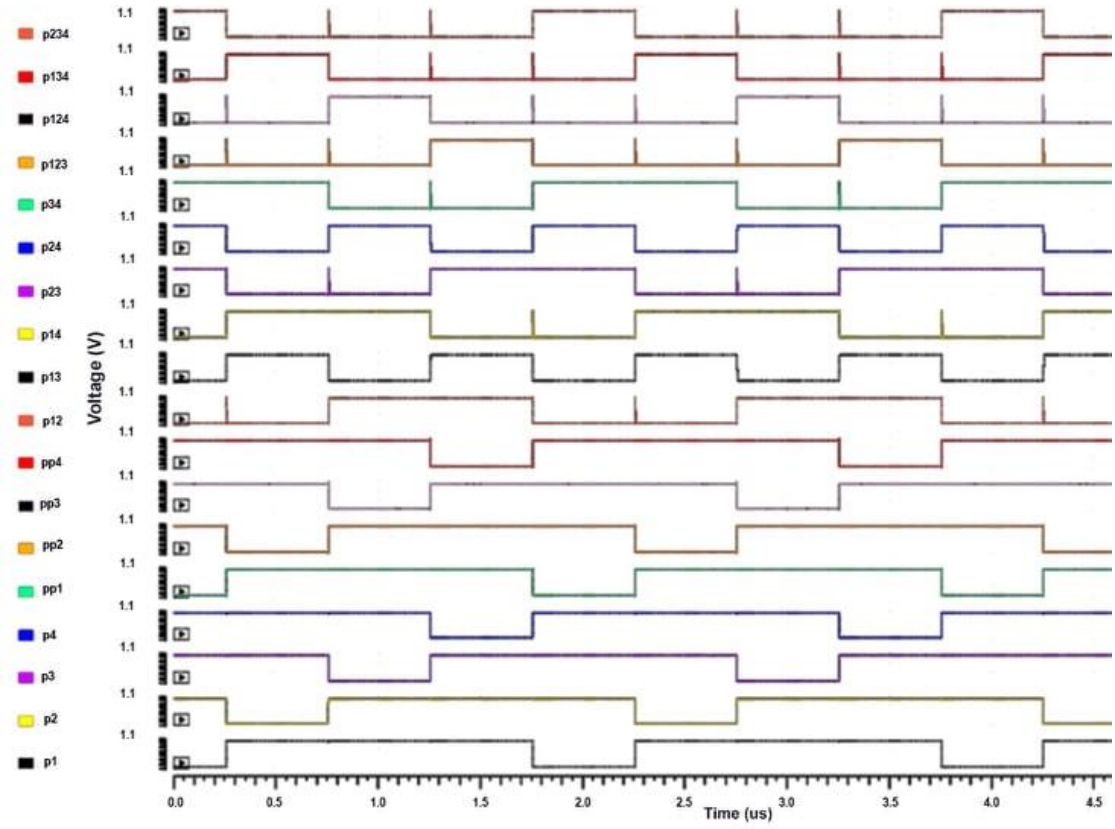
Figure 2- 9. (a)Waveform diagram of a 4-phases output and (b)non-overlapping signals in comparison.

2.4.3. Implementation of OR gate multiplexing

The outputs of non-overlapping clocks are OR-gate multiplexed, as shown in Fig. 2.10(a-b), to ensure that all the possible 4-phases pairs are accessible for the next block router module. In the proposed methodology, the selected transistors are active for the proposed clock logic. The switches can be reused for successive clock logic or the one after next for all 4-phases logics. Thereby even the new topology addition in the future can benefit from it. The selection of DC gain pairs should change when the load demands higher voltages at the output. All the transistor addresses for four different phases of logic are registered in Verilog-A programming.



(a)



(b)

Figure 2- 10. (a) Implementation and (b) Waveform diagram of OR gate multiplexing.

Implementation of Verilog-A router: TABLE 2.5 illustrates what transistors to turn on at different phases depending on the user's choice gain mode. Verilog-A will choose registered transistor addresses to send out turn-on signals to the power stage network by selecting an appropriate gain mode.

TABLE 2- 5. TRANSISTOR ADDRESS FOR ALL MODES.

Phase	Net0						Net1			
Normal Mode										
P1		Mp1	t1	Mn2	Mp4	O1			Mn3	O4
P2		Mp3	t3	Mn0	Mp5	O2			Mn2	O3
P3		Mp2	t0	Mn1	Mp7	O4			Mn0	O1
P4		Mp0	t2	Mn3	Mp6	O3			Mn1	O2
High Mode										
P1	Mp0	Mn0	Mp1	Mn1	Mp6	O3			Mn3	O4
P2	Mp2	Mn2	Mp3	Mn3	Mp4	O1			Mn1	O2
P3	Mp0	Mn0	Mp1	Mn1	Mp7	O4			Mn2	O3
P4	Mp2	Mn2	Mp3	Mn3	Mp5	O2			Mn0	O1
Double Boost Mode										
P1		Mp0	Mn0		Mp5	O2	Mp3	Mn3	Mp6	O3
P2		Mp1	Mn1		Mp4	O1	Mp2	Mn2	Mp7	O4
P3		Mp0	Mn0		Mp5	O2	Mp3	Mn3	Mp6	O3
P4		Mp1	Mn1		Mp4	O1	Mp2	Mn2	Mp7	O4
Super Boost Mode										
P1	Mp1	Mn1	t7	Mn3	Mp4	O1			Mp6	O3
P2	Mp0	Mn0	t4	Mn2	Mp5	O2			Mp7	O4
P3	Mp0	Mn0	t4	Mn2	Mp5	O2			Mp7	O4
P4	Mp1	Mn1	t7	Mn3	Mp4	O1			Mp6	O3

2.4.4. Design Summary

This work is implemented in a standard 0.18 μm AMS CMOS technology, and the overall system diagram is depicted in Fig. 2.11. The operating frequency of 1.1 MHz is used to certify that 1- nF charge pump capacitors are fully charged/discharged over MOSFET switches. The four D-flip flops are constructed to produce a 90-degree phase shift for four different phases at every rising edge of the input clock signal and are further enhanced by passing it through ring oscillators. Thereby, the power stage's transistor switches benefit from non-overlapping 0.1-ns dead time intervals between the consecutive clock phases by eliminating the signal leakage during the switching and full charge settling of the SC network clock cycle.

The limitation of this proposed design in Fig. 2.11 is external power source is required to supply V_{DDH} value. It is needed to strongly switch off the gates which are not involved in the operation. Depending on the dual-mode configurations, left-hand side and right-hand side networks require different high gate voltages. However, since it is only V_{DDH} connection to the gain configuration unit, which is also known as a router, the highest value is chosen suitable for both networks' transistors across the power stage. This limitation shall address in the next chapter charge pump design.

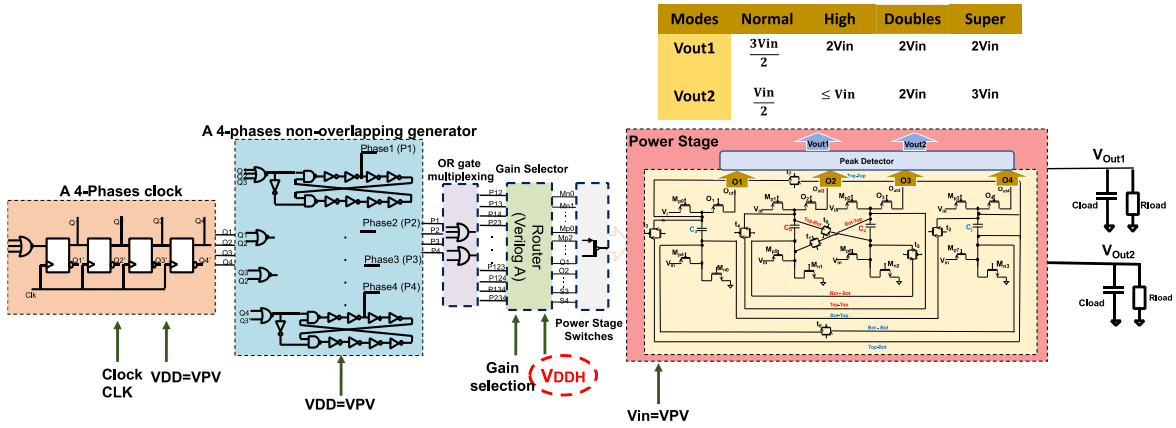


Figure 2- 11. The System Diagram of a proposed converter that operates in a non-overlapping 4-phases clock.

The circuit diagram can be collectively depicted, as shown in Fig. 2.12. The next plan is to replace the programming Verilog-A with a transistor circuit design. The complexity of the 4-phase can be simplified into the 2-phase control clock. It is essential to do so because integrating multiple clocks in on-chip can potentially trigger cross-talk interferences.

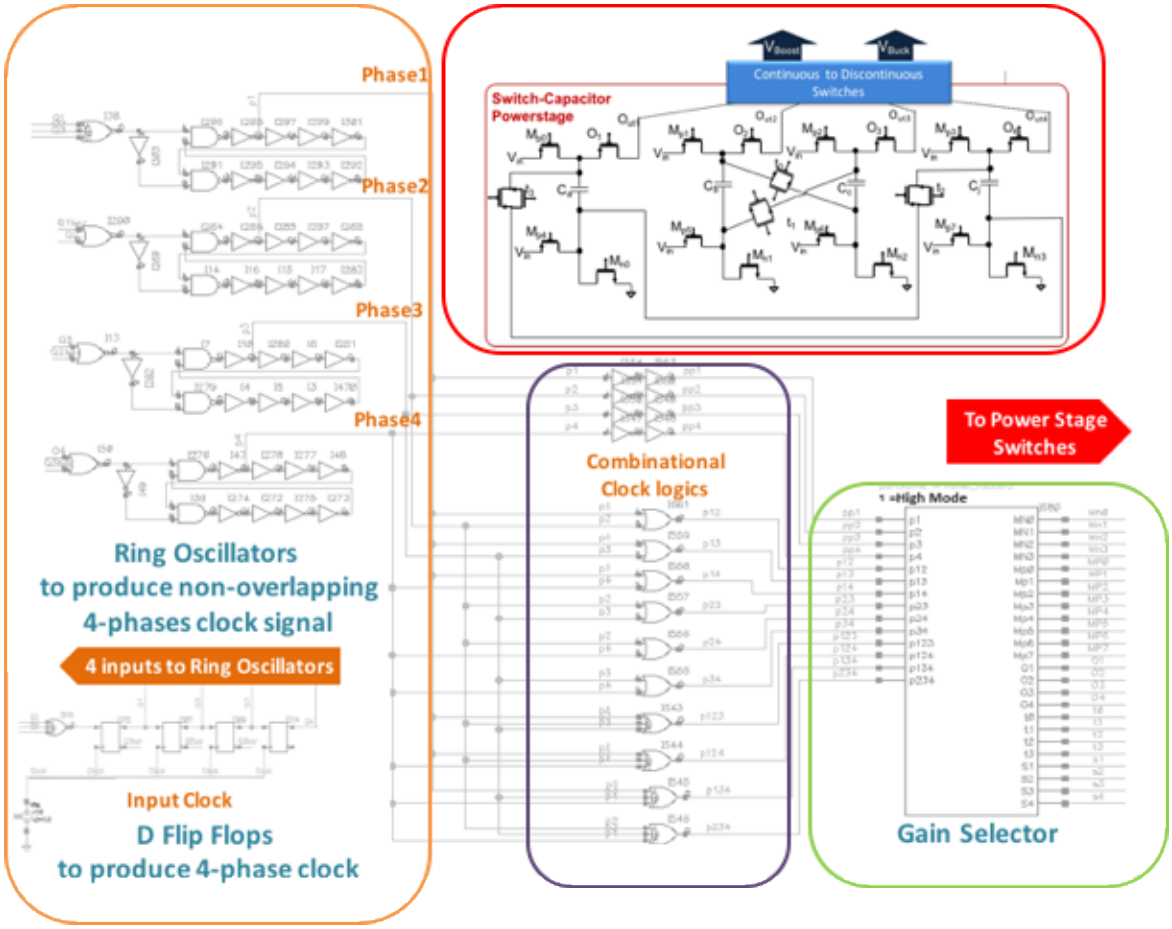


Figure 2- 12. The overall circuit diagram of the 4-phase converter system.

2.5. Methodology, Circuit design and Implementation: Normal mode, High mode, Double mode, and Super mode.

2.5.1. The methodology of Normal Mode

Fig. 2.13 demonstrates the construction of 3/2 gain configuration at *Net0* and 1/2 gain at *Net1*. Assuming this is a continuous sequence of rotation and all the capacitors have equal capacitances, capacitors *Cb* and *Cc* are charged in series to $V_{in}/2$. Previously charged *Ca* is now discharged to *Net0* boost output in a series with V_{in}. Therefore, *Net0* produces to load at

$$V_{boost\_out1} = V_{in} + V_{Ca} = \frac{3V_{in}}{2} \tag{2.6}$$

Meanwhile, *Net1* capacitor *Cj,* which was involved in the previous charging clock cycle of *Net0* and held the value of $V_{in}/2$, is now discharged to buck output -

$$V_{buck\_out2} = V_{Cj} = \frac{V_{in}}{2} \tag{2.7}$$

This rotation sequence is repeated until it is reconfigured into different gain modes. The advantage of this rotation technique can ensure there are always two capacitors charging and outputs of two networks continuously receive simultaneous discharge to loads from two charge pump capacitors and produce two different V_{DD}.

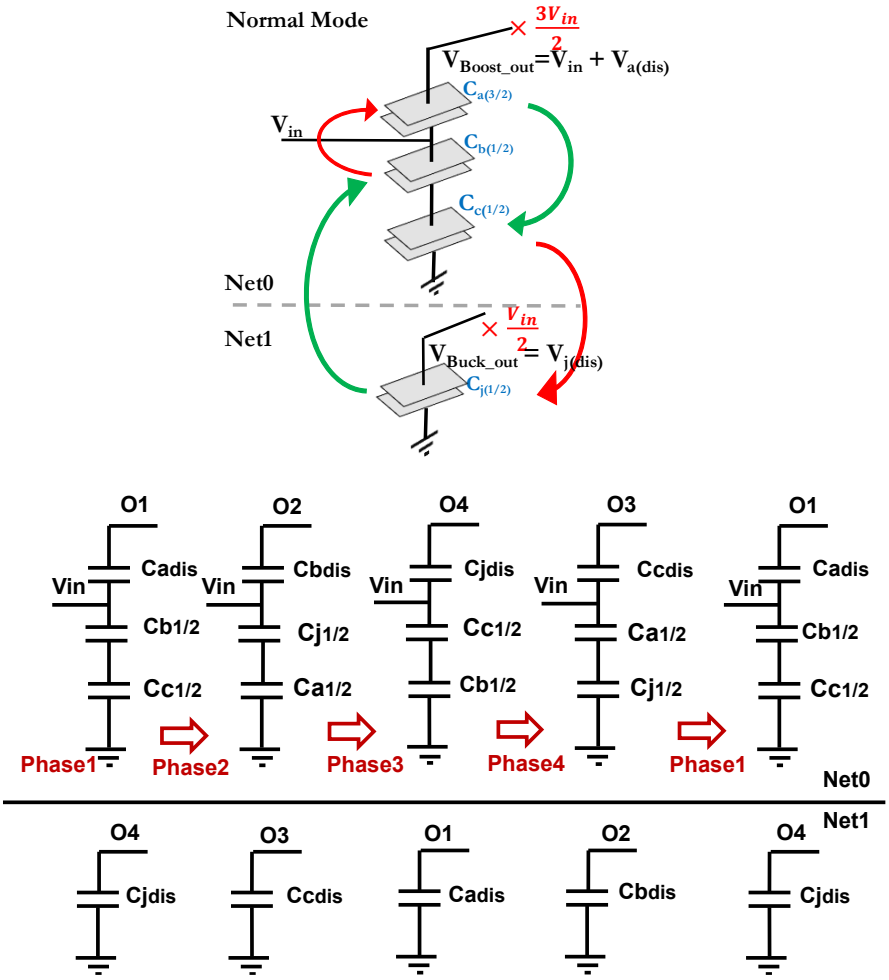


Figure 2- 13. Proposed Methodology of Normal mode with arrows indicating charging(green) and discharging(red) directions.

2.5.2. *Circuit Implementation of Normal mode*

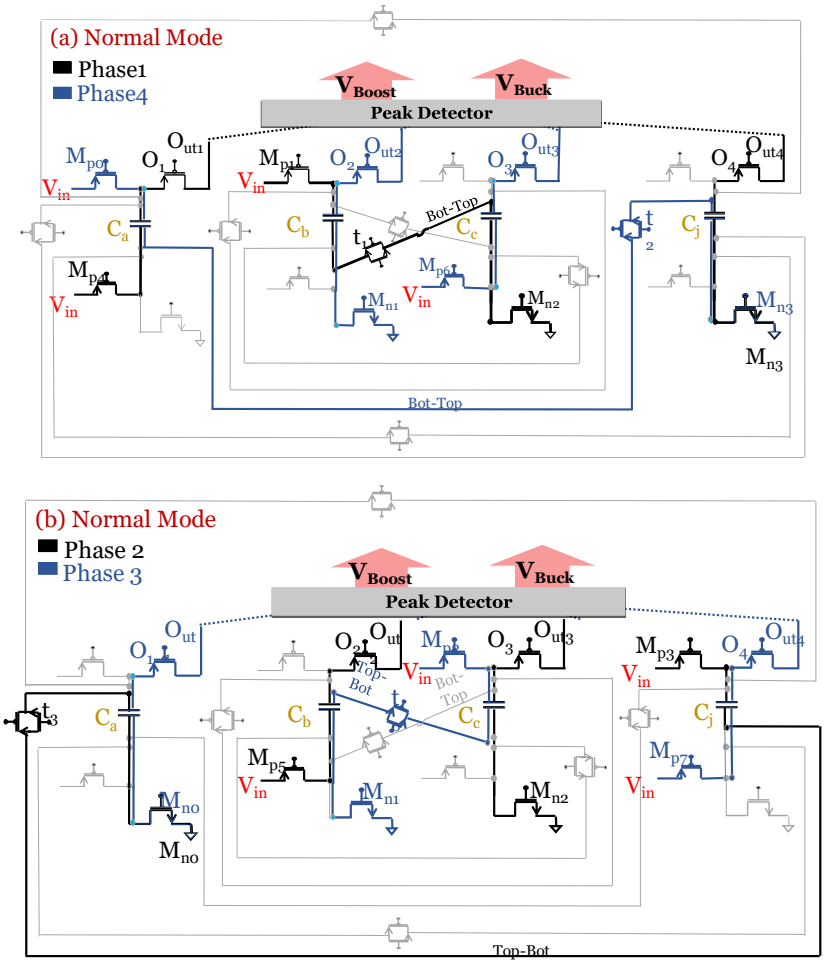


Figure 2- 14. Normal mode operation in circuit-level diagram (a) Phase 1, 4 (b) Phase 2, 3.

The circuit is implemented at the transistor level, as suggested in Fig. 2.14(a). In phase1 charging phase, the two capacitors (*Cb, Cc*) are charged in series by $V_{in}/2$ via transistors (*Mp1, t1, Mn2*) and capacitors (*Cc, Cj*), which are being charged in the phase4 uses (*Mp0, t2, Mn3*). For phase1, the capacitor *Ca* in series with the V_{in} has discharged the gain of $3V_{in}/2$ to Out1 through the switches (*Mn4, O1*). While the capacitor *Cj* is discharged $V_{in}/2$ to the *Out4* via (*Mn3, O4*). Similarly, phase-4 uses (*Mp0, t2, Mn3*) for the charging of capacitors (*Ca, Cj*) and *Net0* outputs are received from *Out3* through the switches (*Mp6, O3*), and *Net1* output is powered by (*Mn1, O2*). Due to the design's symmetry, the same can be said for phase-2 and phase-3 in Fig. 2.14(b), and the active power switches employed for these operations are also recorded in TABLE 2.6. In the construction of Normal mode operation, two capacitors of (*Ca, Cj*) and (*Cb, Cc*) communicate in both charging and discharging for all 4 phases.

TABLE 2- 6. ACTIVE TRANSISTORS FOR NORMAL MODE OPERATION.

	Net0					Net1		
	Normal Mode							
P1	Mp1	t1	Mn2	Mp4	O1		Mn3	O4
P2	Mp3	t3	Mn0	Mp5	O2		Mn2	O3
P3	Mp2	t0	Mn1	Mp7	O4		Mn0	O1
P4	Mp0	t2	Mn3	Mp6	O3		Mn1	O2

2.5.3. The methodology of High Mode

The proposed converter can reconfigure into relatively even higher gain ratios for both boost and buck outputs than Normal mode. Therefore, the power stage of the switched-capacitor (SC) converter benefits from reconfigurable DC gains flexibility for single-input dual-outputs (SIDO). As suggested by Fig. 2.15, the following derivation is achieved for High mode operation:

$$V_{boost\_High} = V_{in} + V_{Cc} = 2\,V_{in} \tag{2.8}$$

The voltage of equal or less than source voltage can be achieved by controlling the switching frequency of capacitor discharge at buck conversion:

$$V_{buck\_High} \leq V_{in} \tag{2.9}$$

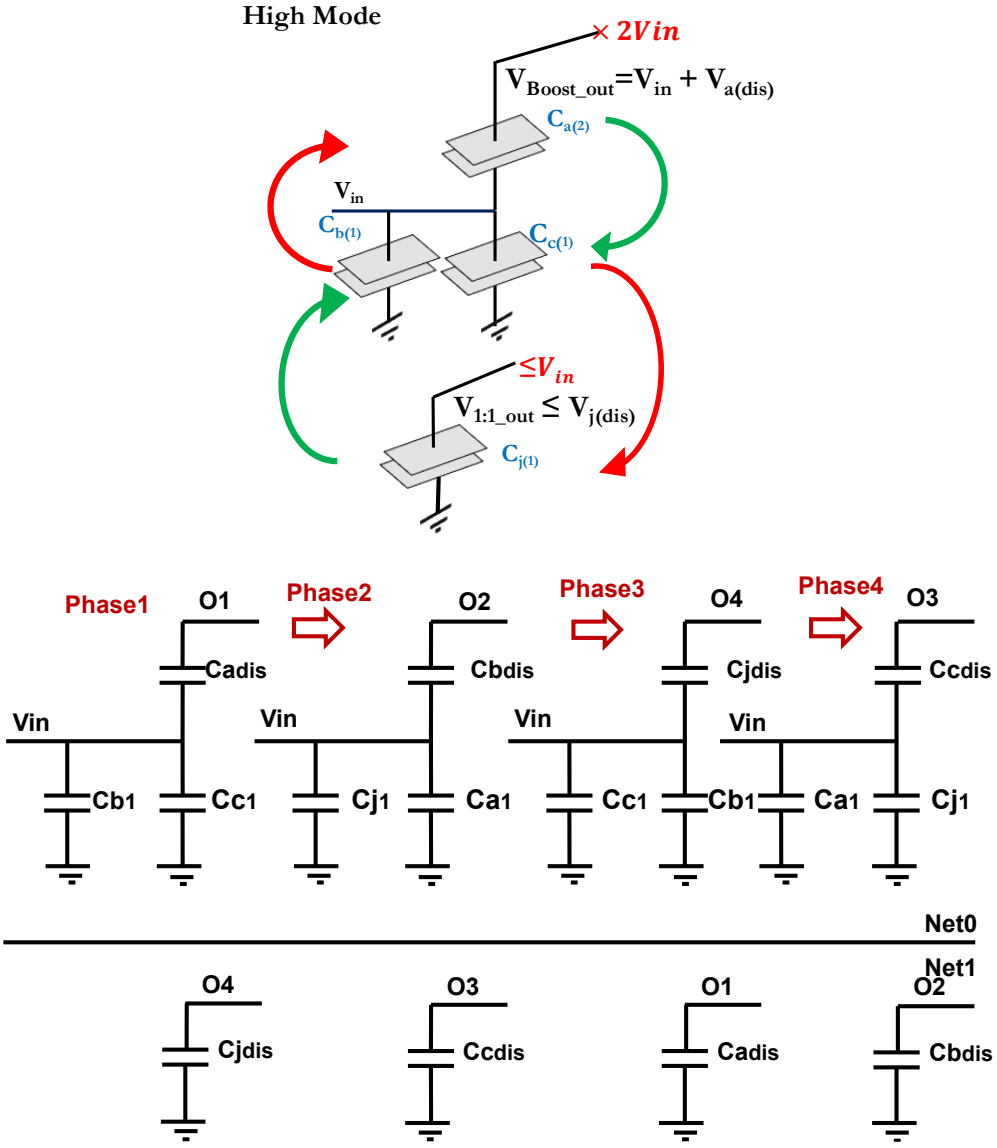


Figure 2- 15.Proposed Methodology of High mode with arrows indicating charging(green) and discharging(red) directions.

2.5.4. Circuit Implementation of High mode

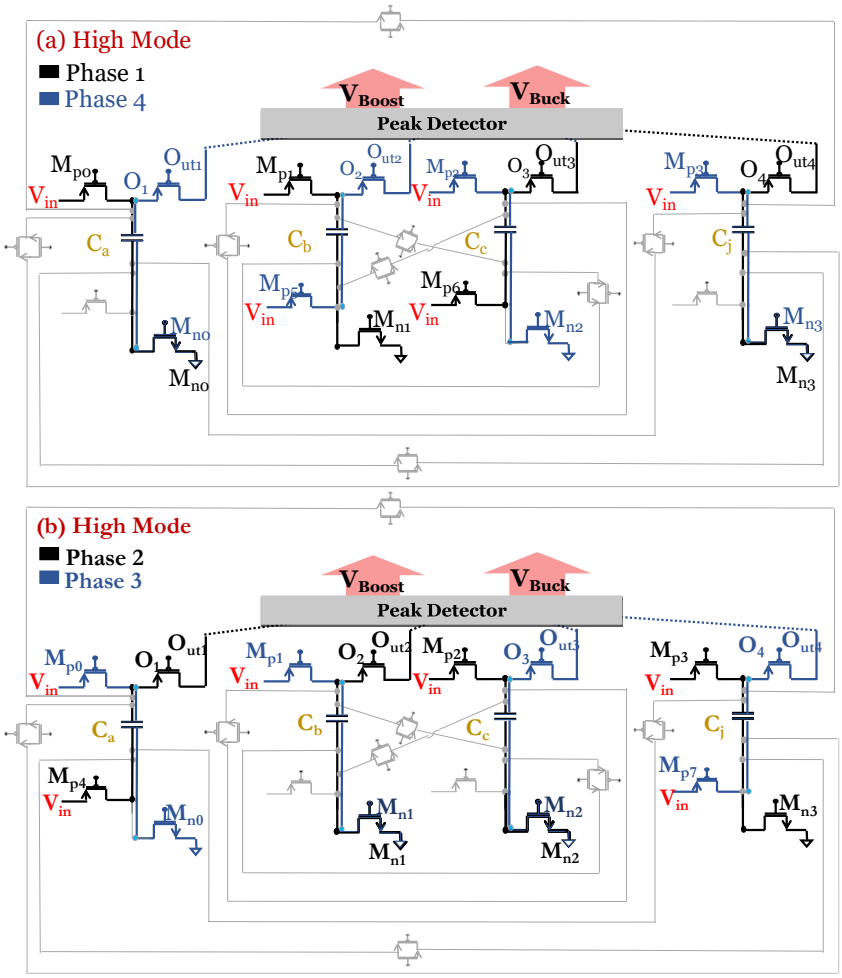


Figure 2- 16. High mode operation in circuit-level diagram (a) Phase 1, 4 (b) Phase 2, 3.

In Fig. 2.16(a), the two capacitors are charged in parallel to V_{in} to capacitors (*Ca, Cb*) through (*Mp0, Mn0, Mp1, Mn1*) in the phase1. Then (*Mp2, Mn2, Mp3, Mn3*) are employed to charge capacitors (*Cc, Cj*) in phase4. Meanwhile, in phase1 of *Net0*, the capacitor *Cc* is discharged in-series with input voltage to get $2V_{in}$ at O_{ut3} through (*Mp6, O3*), and capacitor *Cj* is independently discharged at *Net1* to the gain of V_{in} at O_{ut4} through (*Mn3, O4*). Likewise, in phase4, the *Net0* output with the gain $2V_{in}$ is received at O_{ut2} via (*Mp5, O2*), and *Net1* output yields V_{in} DC gain level at O_{ut1} via (*Mn0, O1*). Due to the design's symmetry, phase-2 and phase-3 can be described similarly as phase1 and phase3. All the active switches involved in Fig.2.16 (b) phase2 and phase3 are described in TABLE 2.7.

TABLE 2- 7. ACTIVE TRANSISTORS FOR HIGH MODE OPERATION.

	Net0						Net1	
	High Mode							
P1	Mp0	Mn0	Mp1	Mn1	Mp6	O3	Mn3	O4
P2	Mp2	Mn2	Mp3	Mn3	Mp4	O1	Mn1	O2
P3	Mp0	Mn0	Mp1	Mn1	Mp7	O4	Mn2	O3
P4	Mp2	Mn2	Mp3	Mn3	Mp5	O2	Mn0	O1

2.5.5. The methodology of Double Boost Mode

In the Double Boost methodology, both the output at *Net0* and *Net1* are step-up gains of $2V_{in}$. It is achieved by charging capacitor *Cb* to V_{in} while discharging *Ca*, which was previously charged to V_{in}, is connected in series with the input source to reach $2V_{in}$ DC voltage gain. During the phase of the illustrated diagram Fig. 2.17, the output voltages are-

$$V_{boost_{Double}(out1,out2)} = V_{in} + V_{Ca} = V_{in} + V_{Cj} = 2\,V_{in} \tag{2.10}$$

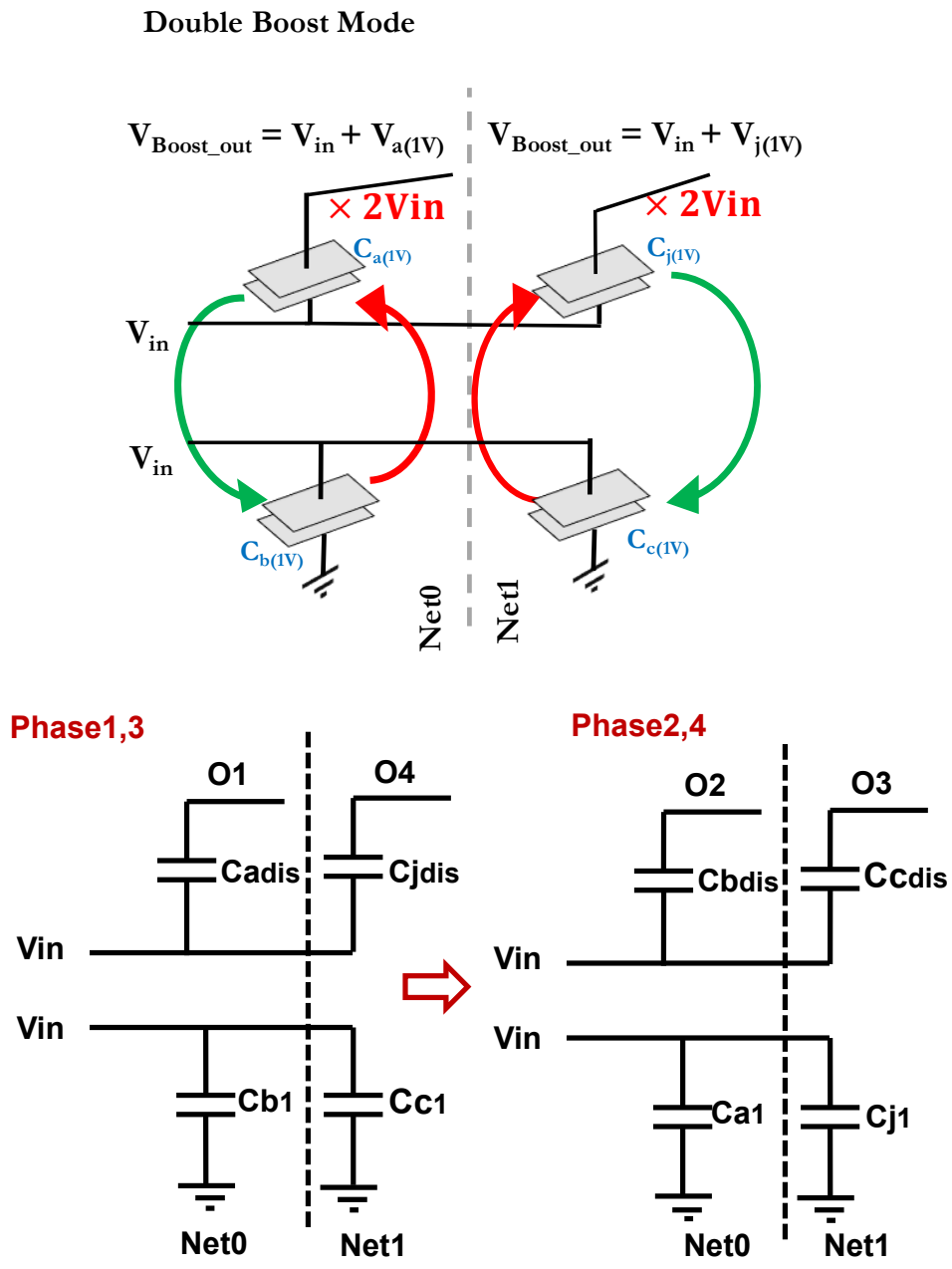


Figure 2- 17. Proposed Methodology of Double Boost with arrows indicating charging(green) and discharging(red) directions.

2.5.6. Circuit Implementation of Double Boost Mode

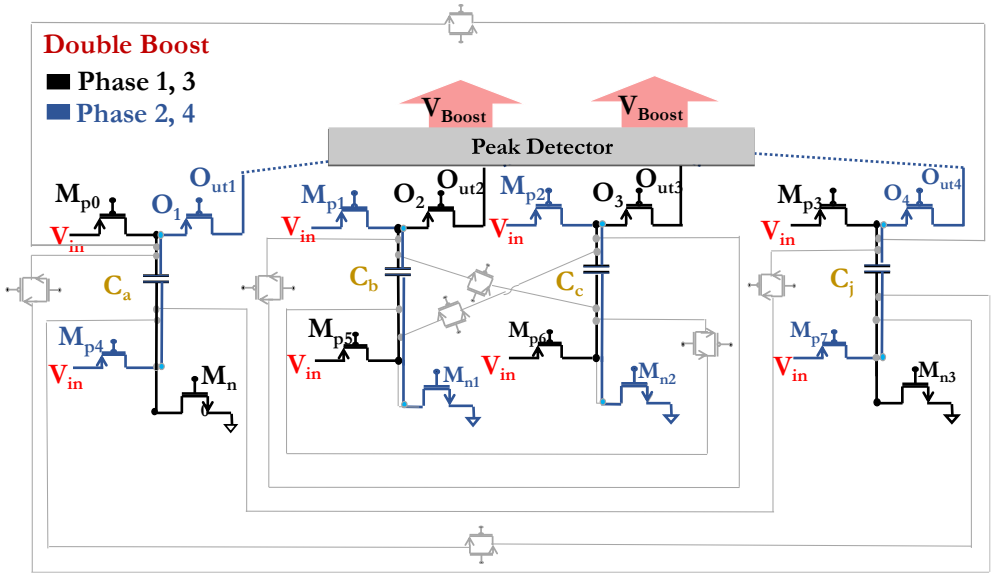


Figure 2- 18. Double Boost operation in the circuit-level diagram (a) Phase 1, 3 (b) Phase 2, 4.

The circuit configuration of Double Boost mode in phase1 and phase3 is shown in Fig. 2.18- by charging capacitor *Ca* to V_{in} via switches (*Mp0, Mn0*) and discharging previously charged capacitor *Cb* in the series with input source via (*Mp5, O2*) to the O_{ut2} at the *Net0*. For Net1, the exact process is repeated to charge *Cc* compared to *Ca* through switches (*Mp3, Mn3*) and likewise *Cb*, capacitor Cc uses (*Mp3, O3*) to discharge at O_{ut3}. A similar explanation can be given to phase-2 and phase-4 due to the design's symmetry, and all transistor's construction is recorded in TABLE 2.8.

TABLE 2- 8. ACTIVE TRANSISTORS FOR DOUBLE BOOST OPERATION.

	Net0				Net1			
	Double Boost Mode							
P1	Mp0	Mn0	Mp5	O2	Mp3	Mn3	Mp6	O3
P2	Mp1	Mn1	Mp4	O1	Mp2	Mn2	Mp7	O4
P3	Mp0	Mn0	Mp5	O2	Mp3	Mn3	Mp6	O3
P4	Mp1	Mn1	Mp4	O1	Mp2	Mn2	Mp7	O4

2.5.7. *The methodology of Super Boost Mode*

The step-up gain of $3V_{in}$ and $2V_{in}$ dual outputs are simultaneously achieved in Super Boost operation. As illustrated in Fig. 2.19, first *Cb* is charged to V_{in} and, second, *Ca* is discharged in series with V_{in} to V_{out} and charge the capacitor *Cj*. Thus, both V_{Cj} and the output of *Net0* receive a voltage of $2V_{in}$. It is described in the Equation-

$$V_{Boost_{Super}(out1)} = V_{in} + V_{Ca} = 2\,V_{in} \tag{2.11}$$

Meanwhile, in *Net1*, capacitor *Cc* discharge in series with V_{in} to achieve $3V_{in}$ at the output.

$$V_{Boost_{Super}(out2)} = V_{in} + V_{Cc} = 3\,V_{in} \tag{2.12}$$

In the next phase, all the discharge capacitors (*Ca, Cc*) are swapped with charged capacitors (*Cb, Cc*) accordingly, as suggested in Fig. 2.19.

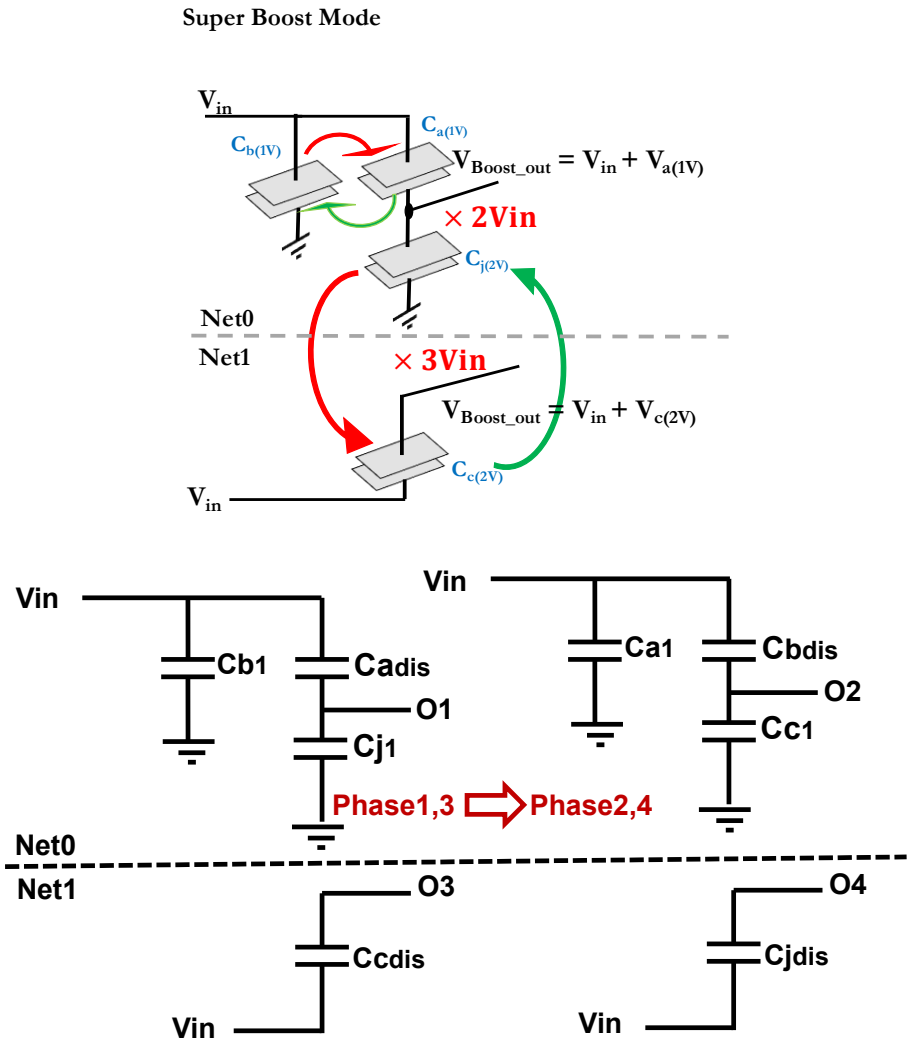


Figure 2- 19. Proposed Methodology of High mode with arrows indicating charging(green) and discharging(red) directions.

2.5.8. *Circuit Implementation of Super Boost mode*

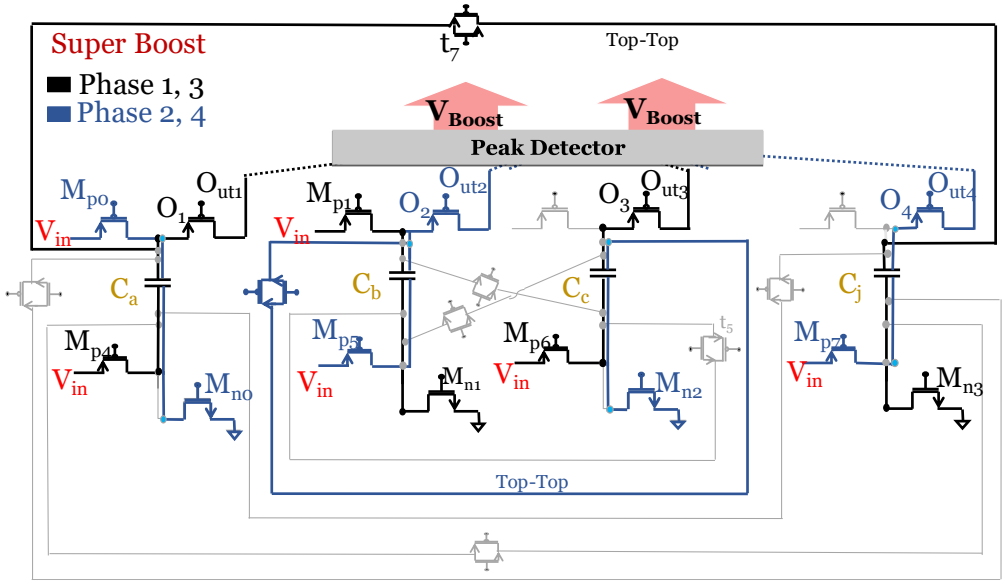


Figure 2- 20. Super mode operations in circuit-level diagram Phase 1,4 and Phase 2,3.

As proposed in Fig 2.20, in phase 1 and 4, capacitor *Cj* is charged to $2V_{in}$ through (t_7, M_{n3}), in parallel with the delivered output with the gain of $2V_{in}$ step-up voltage by discharge capacitor *Ca* connect in series with input source via (M_{p4}) parallel to O_{ut1} through (O_1). In the meantime, the capacitor *Cc*, which has the $2V_{in}$ voltage, discharge in-series with input source to O_{ut3} via (O_3 *and* M_{p6}). Correspondingly, phase 2 and phase 3 can be understood by following the same procedure with transistors provided in TABLE. 2.9.

Observed that M_{p4} in phase-1,3 or M_{p5} in phase-2,4 can assume to belong to both charging and discharging as these switches connect in parallel to output connection and capacitor charging at the same time.

TABLE 2- 9. ACTIVE TRANSISTORS FOR SUPER BOOST OPERATION.

	Net0							Net0	
	Single Boost Mode								
P1	Mp1	Mn1	t7	Mn3	Mp4	O1		Mp6	O3
P2	Mp0	Mn0	t4	Mn2	Mp5	O2		Mp7	O4
P3	Mp0	Mn0	t4	Mn2	Mp5	O2		Mp7	O4
P4	Mp1	Mn1	t7	Mn3	Mp4	O1		Mp6	O3

2.6. *Result and discussion*

2.6.1. *Performance Analysis of Output Voltages Load regulations*

The converter takes approximately 3.2 µs to get the first signal. Hence the line transient and 5.1 µs load transient time to reach the Normal mode saturation, Fig. 2.21. Ideally, from 1 V input multiply with (2/3 and 1/2) gains should achieve 1.5 V and 0.5 V. In practice, the first output managed to reach the expected value at peak 1.5 V and 487.487 mV for second output. The load regulation test was also carried out by changing the output resistances (50-100 kΩ) and demonstrated that the converter maintains the optimum stability with only slight variations. The highest performance is at 50 kΩ load for every phase duration, and this is due to the higher the loaded sink with the fast discharge time.

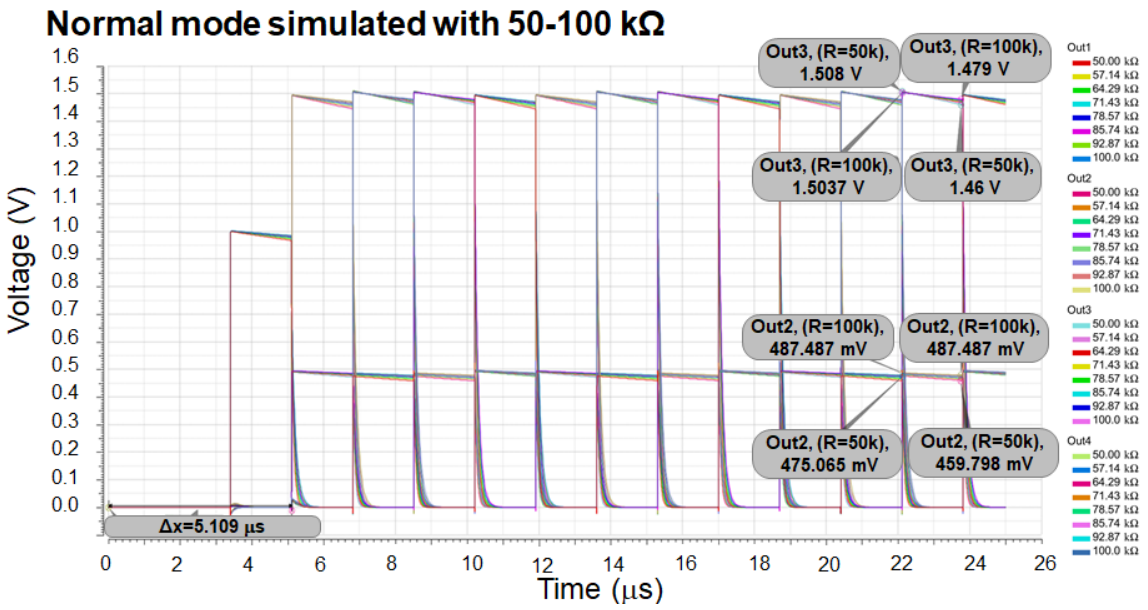


Figure 2- 21. Simulation of Normal mode tested with 1pF and 50-100 kΩ loads.

The converter takes approximately 3.1-µs to get the first signal. Hence the line transient and 4.49-µs load transient time to reach saturation of the High mode. The outputs are expected to achieve 2-V and 1-V in theory, but rather 1.9937-V and 997.4-mV are obtained at peak. The simulated output result is demonstrated in Fig. 2.22.

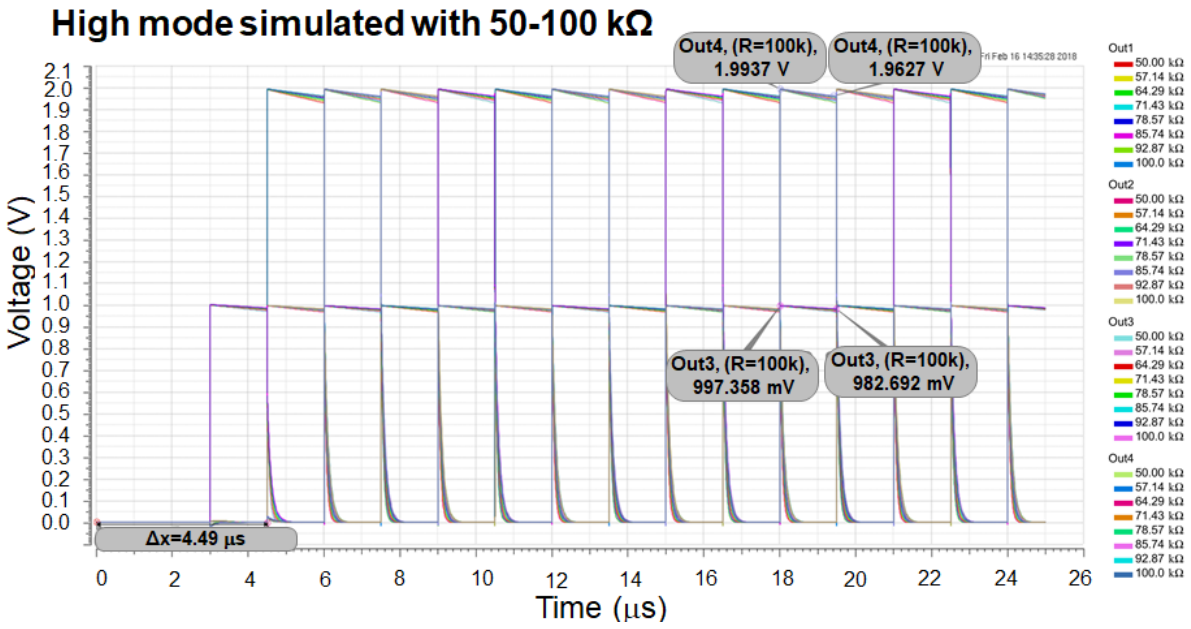


Figure 2- 22. Simulation of High mode tested with 1 pF and 50-100 kΩ loads.

The outputs for Double Boost mode are expected to yield 2 V for both outputs, and Fig. 2.23 demonstrated that 1.994 V is obtained for both outputs. Moreover, the converter takes about approximately 1.8 µs line transient and 2.65 µs load transient time to reach the Double Boost mode saturation.

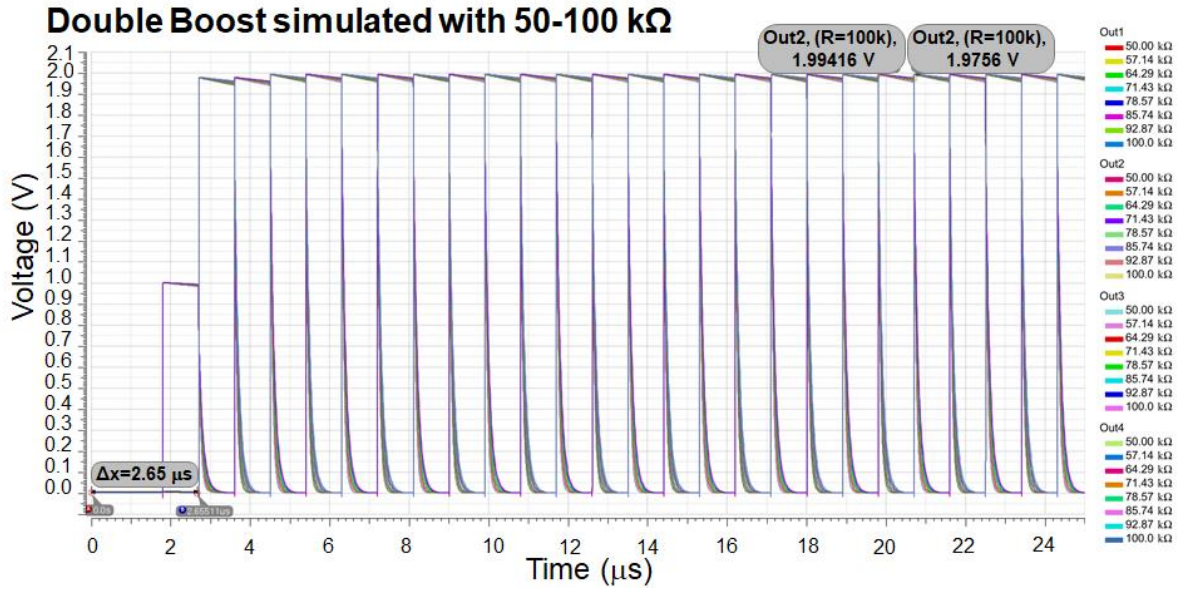


Figure 2- 23. Simulation of High mode tested with 1pF and 50-100 kΩ loads.

Super Boost mode outputs take approximately 1 µs line transient time, and 15 µs load transient time to reach saturation. The converter is expected to achieve 3-V and 2-V at the outputs, but rather 2.917-V and 1.92-V are attained in practice. It is shown in Fig. 2.24.

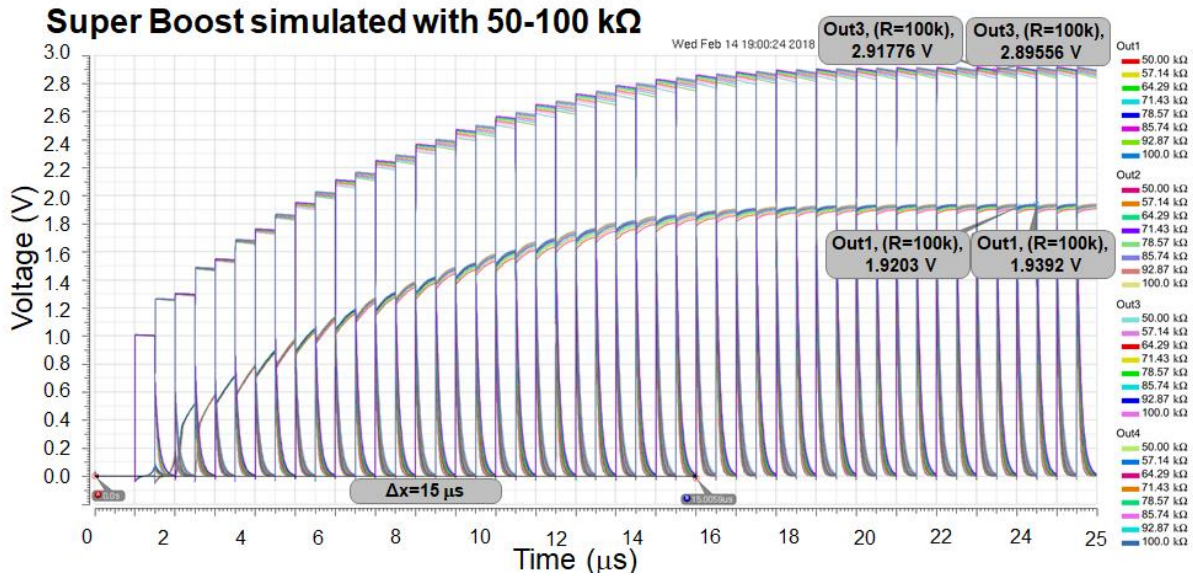


Figure 2- 24. Simulation of Super Boost mode tested with 1 pF and 50-100 kΩ loads.

2.6.2. Current-Voltage (I-V) Characteristics.

The proposed system's output power is acquired by recording the output voltages, and the output currents of all DC gain modes are simulated with various resistance loads 50-100 kΩ. These values are then plotted in Fig. 2.25. When the loads increase, the voltage at the output increases and the current dropped as expected from Ohms law. Each mode has a different gradient change due to its difference in internal Ron resistance of the current paths. Although High mode's Out_1, Double Boost mode's $Out_{1,2}$, and Super Boost mode's Out_2 share the same gain of ($2V_{in}$), each is configured differently with different switches. Coincidently, the High mode's Out_1 and Double Boost mode's $Out_{1,2}$ displays the same I-V characteristic since they overlapped and closely matched with Super Boost's Out_1 line.

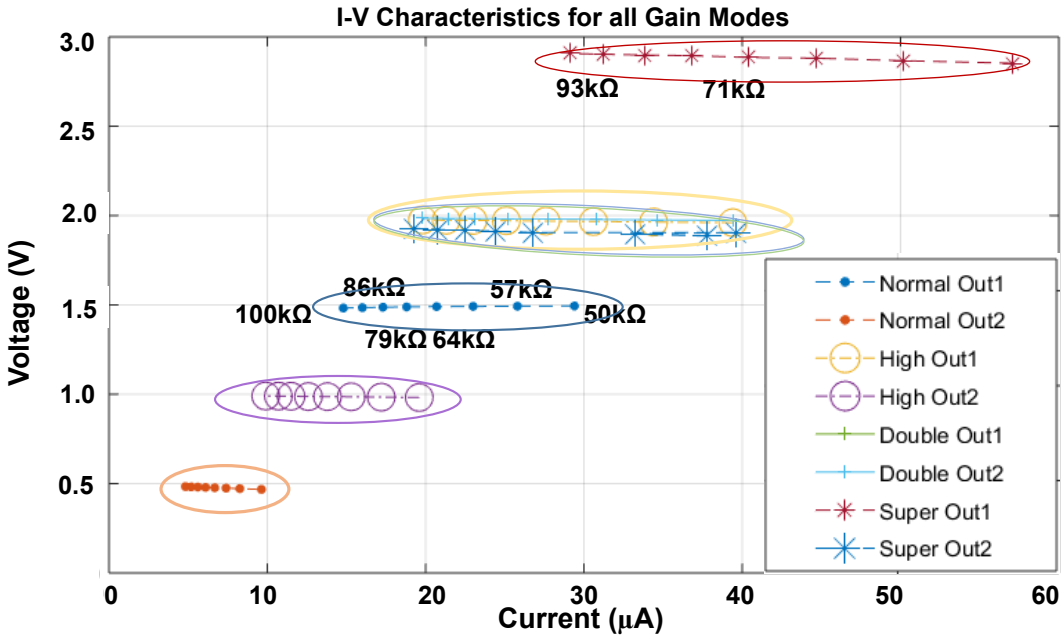


Figure 2- 25. Current-Voltage Characteristics for all Gain Modes.

2.6.3. Average Output Power.

Consequently, from the simulated I-V curve values, the converter's average output power varies across the different loads of 50-100 kΩ is demonstrated in Fig. 2.26. The average low power output ranges from 0.0023-0.23 mW. The Super boost mode produces the highest power output, and the Normal mode output yields the lowest average power as expected. It was also observed that the average power of two Double Boost outputs and out1 of High mode share the overlapped lines and closely match the out2 of the Super Boost mode since all of them aim the same targeted gain value. It demonstrated that the voltage conversion could perform up to 98%. At best, the average boost output mode produces 1.49 V (at 29.45 μA), and the buck being 0.467 V (at 9.36 μA) Normal mode. Likewise, for the High mode, the average boost output produces 1.905 V (at 39.2 μA) and 0.98 V (at 19.6 μA) for the buck output. Similarly, Double Boost has 1.97 V (at 39.4 μA), and Super Boost yields 2.85 V (at 57.1 μA) and 1.89V (at 37.8 μA) average outputs. The output ripples are recorded between 14-59 mV.

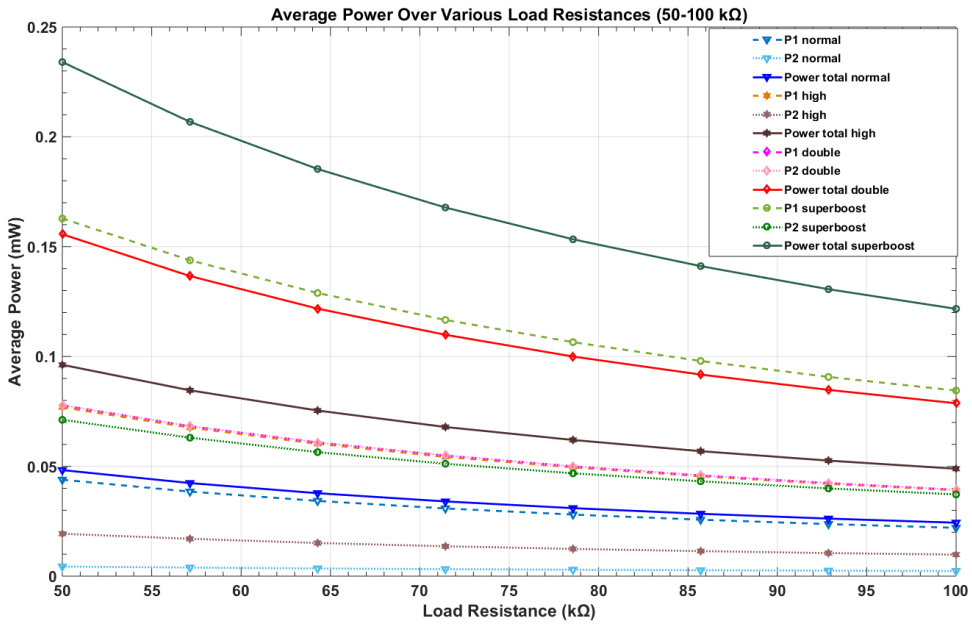


Figure 2- 26. The average Power output of various 50-100 kΩ loads.

2.6.4. Line Regulation

Assuming input integrated battery degrades over time or supplied *PV* cell power degrades at low light such as a night-time, line regulation with varying inputs of 1-0.8 V, simulated with a fixed load of 100 kΩ and the results are shown in Fig. 2.27. Though the output voltages reduce from targeted values due to input changes, the linear line indicates that the converter still maintains correct gain operation relative to a given input. The target output values are the same (×2 gain) for P1 Double, P2 Double, and P1 High. Therefore, some performance lines appear overlapped.

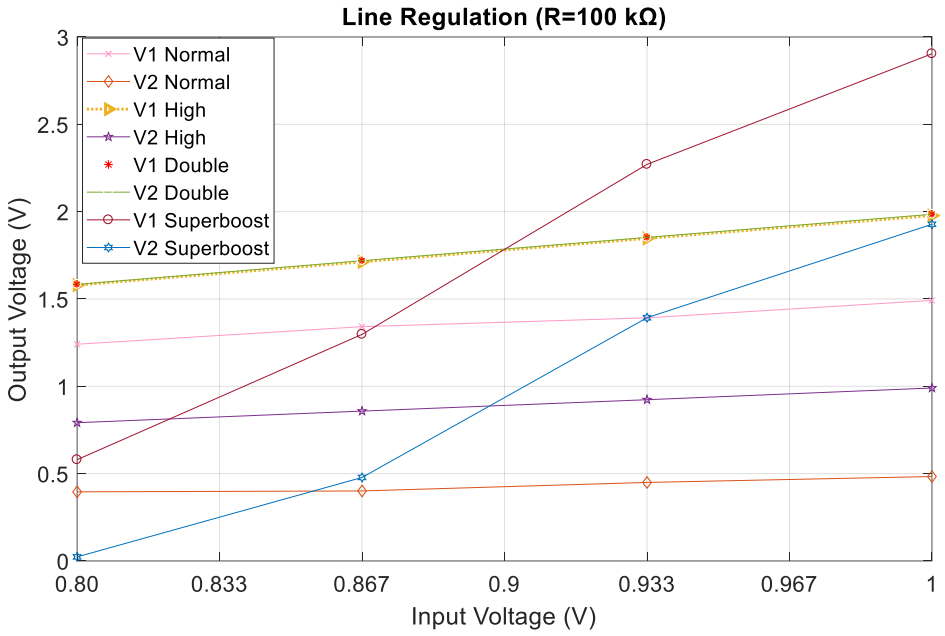


Figure 2- 27. Line Regulation Tested with Input Voltages varies from 1-0.8 V and 100 kΩ load.

Finally, the performance summary of the design is described in TABLE 2.10.

TABLE 2- 10. PERFORMANCE SUMMARY OF A PROPOSED 4-PHASE CONVERTER.

Input (V)	**0.8-1**
Output (V)	**1.49, 0.47 or 1.91, 0.98 or 1.97, 1.97 or 2.85, 1.88**
Load current (mA)	**0.04, 0.06, 0.08, 0.1**
Conversion ratios	**(3/2, 1/2) or (2, 1) or (2, 2) or (3, 2)**
Max Power Out (mW)	**0.23**
Ripple (mV)	**20-60**
Efficiency max (%)	**85.257, 72.884, 53.6, 47.85**
Frequency (Hz)	**5.8823 k, 666.66k. 1.1 M, 2 M**
Load transient (µs)	**5.1, 4.49, 2.65. 15**
Line transient (µs)	**3.2, 3, 1.8, 1**
Flying Cap (F)	**1n ×4**
Filter Capacitor (F)	**1p**
Load Resistance (kΩ)	**50-100**

2.6.5. Comparison of State-of-the-art

TABLE 2- 11. SIMULATED RESULTS AND COMPARISON WITH STATE-OF-THE-ART.

Specification	**This work 180nm Simulated**	**[167] 40nm Measured**	**[220] 45nm Simulated**	**[204] 90nm Measured**	**[206] 130nm Measured**	**[159] 350nm Measured**
Input (V)	**1**	**3.7**	**1**	**1.2**	**2.5**	**1.1-1.8**
Vout (V)	**1.49, 0.47 1.91, 0.98**	**1.8, 0.8**	**0.66, 0.33,1**	**0.76, 0.32**	**4.81, -2.31**	**2, 3**
	1.97, 1.97	**-**	**-**	**-**	**-**	**-**
	2.85, 1.88	**-**	**-**	**-**	**-**	**-**
I_{load} (mA)	**0.04, 0.06, 0.08, 0.1**	**0.4, - 1**	**-**	**0.4, 0.9**	**2, 2**	**12**
Conversion Ratios	**3/2, 1/2 or 2, 1 or 2, 2 or 3, 2**	**1/2, 1/4**	**2/3, 1/3, 1**	**1/2, 2/3**	**2, -1**	**3, 2 or 2, 2**
P_{out_max}(mW)	**0.23**	**1.3**	**1.3**	**1**	**9.62**	**60**
Ripple (mV)	**14-59**	**60**	**9.6**	**19.5-40.6**	**95, 85**	
Efficiency (%)	**85.26**	**70**	**90**	**68**	**92**	**90**
Capacitor (F)	**1n ×4**	**2.24n × (≥2)**	**3.7n × (≥4)**	**5n×2 6n×2**	**1µ ×4**	**4.7µ ×2**

The recent state-of-the-art single-input-multi-output converters, which were previously discussed, are summarised TABLE. 2.11. Apart from [220], which produces three simultaneous outputs, the rest of the SC converters presented in the above table are SIDO designs. Depending on the application and required output power and availability of chip area, most of the methods use Nano Farad size capacitors and typically employ four flying capacitors for dual output designs. Contrary to state-of-the-art, the only two designs- this work and [159] can reconfigure into different gain values. The rest of the SIMO converter designs have relatively fixed gain ratios. However, the topology of [159] has some idle time for every 180-degree phase shift due to it going back to the charging phase, and our proposed topology can simultaneously output the different VCR at the same time. Moreover, this proposed work has the highest reconfigurability since it can configure four various DC gain pairs.

Furthermore, only the [159, 206] designs are accessible for step-up conversion, while other SIDO converters only enable simultaneous down conversions. Although this proposed design has the lowest maximum power output compared, it is to note that the 1-nF charge pump capacitor is utilised. It is still the open-loop, and the maximum efficiency this converter is capable of producing is comparable to most of the existing technologies. The efficiency value of this converter is described in TABLE.2.11. is in consideration of digital circuitry and input power losses. If only charge pump power losses are considered, it can go as high as 98% efficiency.

2.7. Summery

In summary, the following statements are contributing to knowledge-

- **A novel** topological approach of switched-capacitor for **4-phase** rotation designed in 180 nm AMS CMOS technology
- The proposed converter yields **simultaneous dual output** conversions for multi-functional implantable applications with internally integrated electronic modules.
- This technique **optimizes the use of integrated capacitors with no idle capacitors.**
- **Simultaneous Boost and Buck conversions are accessible**, and the system is **reconfigurable.**
- This topology has **fulfilled the gap of reconfigurability in SIDO converters**, **fast response** time. It offers the ability to **reconfigure** the converter into **step-up or step-down gain ratios** for simultaneous outputs.
- It **prevents efficiency degradation in a wide input range since the extensive** range of **gain pairs** is **accessible**.
- The simulated result of the converter has a **high power efficiency** of up to 85.26%.
- Converter displays **stable load regulation** over various simulated loads of 50-100 kΩ and produces 0.0023-0.23 mW output power at different gain modes.
- **Line regulations** was also simulated by varying input voltage from 0.8-1 V. The output display linear response to all modes except for the super boost mode.
- Converter displays **VCR outputs** –(1.49 V, 0.47 V), (1.91 V, 0.98 V), (1.97 V, 1.97 V) and (2.85 V, 1.88 V) close enough to the ideal target value (3/2 V, 1/2 V), (2 V, 1 V) , (2 V, 2 V) and (3 V, 2 V).

The following statement need for future work-

- The efficiency degradation in higher conversions (such as double boost and super boost modes) is due to leakage currents between the phase-changes transitions, which are governed by the higher frequency switching, which are yet to be improved.
- Furthermore, this dual output converter design has the potential to become a self-powering system.
- The converter's outputs can be used to supply the peripheral circuits or digital controller instead of having a separate power source for $V_{DD\text{-}Digital}$ (V_{DDH} in Fig. 2.11.) It requires higher voltages than the input supply voltage. Therefore, the output can be used to supply the load as well as the peripheral circuit.
- A peak detector (discontinuous to continuous) is needed to achieve clean DC output. The further approach needs to consider eliminating the need for these peak detectors.
- Nano farad size capacitor can consume a considerable chip area.

CHAPTER 3: CHARGE-PUMP DC-DC CONVERTER BASED ON SINGLE-INPUT DUAL-OUTPUTS AND SINGLE-OUTPUT

3.1. Motivation

Future medical devices will be integrated into a variety of body-worn applications that can sense, diagnose and treat chronically ill patients [3-7], as shown in Fig. 3.1(a). These devices will be integrated into soft contact lenses [11-15] or wrist-worn smart bracelets [16-20] and will transform our day-to-day lives. Such devices consist of several building blocks that require different operational voltages, as shown in Fig. 3.1(b).

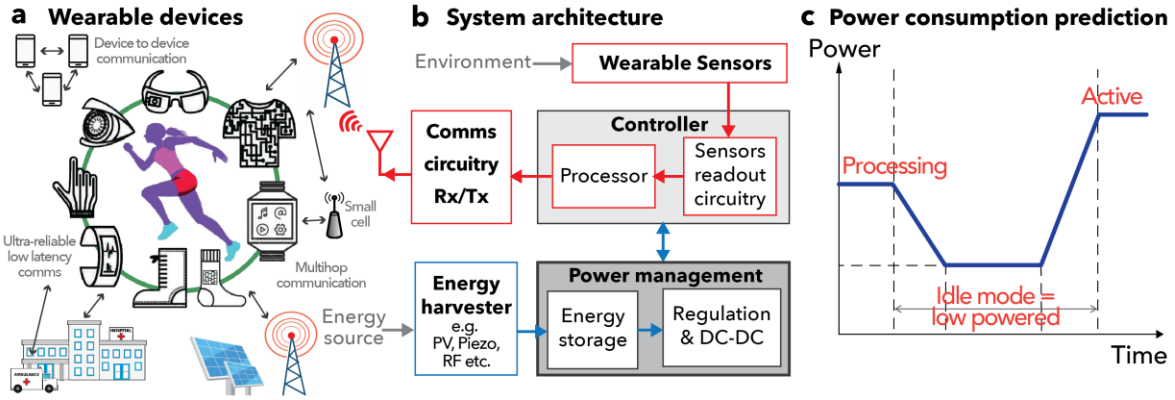


Figure 3- 1. (a) Concept of wearable medical devices, (b) wearable sensing system architecture, and (c) predicted power consumption graph.

Reliable and efficient DC-DC conversion provides a steady and regulated DC output voltage with a wide range of voltage conversion ratios (VCR), affecting overall power efficiency [157]. It is especially true for applications requiring dynamic loading conditions, as demonstrated in Fig. 3.1(c). Moreover, efficient and reconfigurable power converters that provide a wide range of dynamic output voltages are required since low-power wearable biomedical devices now rely on power harvested from these energy harvesting sources that are location and time-dependent [25, 221]. In this chapter, the assumption has been made that a fixed input voltage of 1 V is supplied to the power management system (PMS). Although a single-junction *PV* cell produces V_{oc} of 0.53 V, stacking two *PV* cells in series can achieve around the required 1 V [163]. In [195] also stated depending on the materials and configurations of *PV* cells, higher voltages can be achieved. Later in next Chapter-4, I will address the discussed and design the PMS, which can also handle the input variation due to the nature of energy harvesters. The focus of this chapter is to develop the PMS that generates reconfigurable output voltage to supply different system-on-chip electronic devices.

This chapter presents a novel 2-phase reconfigurable switched-capacitor (SC) DC-DC power converter that provides different DC gain modes. The output of the proposed converter simultaneously produces two different levels of VCRs and a single reconfigurable output. Compared to our previously proposed 4-phase designs [156, 163, 168], this 2-phase converter has other modes and presents a new gain configuration unit (GCU). If desired, both integer/non-integer additional gains can be added via a change to GCU with a small area trade-off without changing the power stage network and still providing output regulation to those added gain outputs. Most importantly, the converter is self-powered, which means that an additional power supply is not necessary and self-supplied, for which peripheral circuits are fed in by converter outputs. This reconfigurable converter offers dual outputs with a choice of multiple output voltage ranges, which will be beneficial for multi-functional wearable devices operating at different voltages. Moreover, single-output modes make it ideal for energy-constrained devices. This proposed design is helpful for the plethora of wearable devices comprising electronic modules requiring different operational voltages.

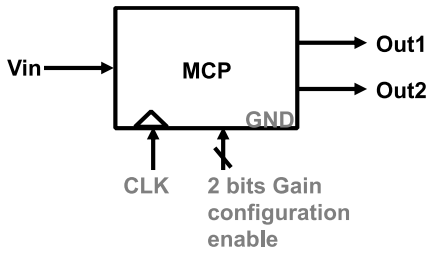
Therefore, the proposed novel 2-phase design will be implemented with the objective -

- To **minimise the chip area**, the charge pump capacitor size will reduce to the Pico-Farad region (1nF in the 4-phase design) for a smaller chip area size, contributing directly to the cost.
- To reduce the **complexity** of the control clock generator over the previously proposed novel 4-phase charge pump design. As the design complexity reduces, the use of components to generate the desired clock also **decreases, and** consequently, the **power consumption** of the sub-circuit is minimized.
- To replace the programmed Verilog-A **GCU with a transistor design**.
- To eliminate the need for output peak detector (discontinuous to continuous).
- To produce stable output performances and high efficiencies.
- To achieve VCR close enough to targeted gain value- i.e., input voltage times conversion gain.
- To produce **reconfigurable single-output DC gain** for idle mode conditions and **reconfigurable dual-output** for a wide range of applications.
- To be able to **self-regulate** without needing the large filter capacitor.
- To be able to **self-supplied** from its power stage output to peripheral circuits.

3.1. Overview of Single-input-dual-outputs (SIDO) and Single-input-Single-output (SISO)with a Proposed 2-Phase Charge Pump.

The proposed power management DC-DC converter produces a reconfigurable gain single-input-single-output (SISO). It generates single-input simultaneous dual-outputs (SIDO), with each output line comprises reconfigurable gain modes, as shown in Fig. 3.2. The charge pump network is designed to have symmetric nature by interleaving regulation scheme in each side of the loads R_{load1}(at O_{ut1}) and R_{load2} (at O_{ut2}) at SIDO, or a single load if the configuration is SISO. Therefore, the output voltages are achieved with a low ripple, and there is a constant current supplied to the loads, which minimizes redistribution loss.

The integrated four capacitors connections can be reconfigured to achieve four different voltage and power modes; namely- (1) Low-power mode (*LP*) produces (×2) gain at the O_{ut1} and regulated, (2) Double-boost mode (*DB*) achieves two simultaneous VCR of (×2, ×2) at O_{ut1} and O_{ut2} respectively and regulated with interleaving the symmetric path in both outputs, (3) Super Boost mode (*SB*) yields a step-up gain of (×3, ×2) dual outputs are achieved simultaneously [159] and regulated with the symmetric paths interleaved in both outputs, and lastly (4) High-conversion mode (*HC*) achieve (×3.5) VCR by employing Dickson ladder topology inspired series-parallel network. In *HC* mode, there is no identical interleaved network to perform the regulation scheme.



	LC	DB	SB	HC
Out1	×2	×2	×2	-
Out2	-	×2	×3	×3.5

Figure 3- 2. Proposed 2-phase main charge pump (MCP) and its reconfigurable gains.

3.2. Methodology and Circuits Design Implementation

3.2.1. The methodology of the 2-phase charge pump

Low-power mode (LP): Produces (×2) gain at the O_{ut1}. As depicted in Fig. 3.3(a), only *Ca* and *Cb* of the power network is used for gain conversion and the regulation purpose, conserving the use of the rest of the transistor power gates.

$$V_{boost_{LP}(out1)} = V_{in} + V_{Ca} = 2\,V_{in} \tag{3.1}$$

Double-boost mode (DB): The two simultaneous voltage gain ratios of (×2, ×2) outputs are achieved at O_{ut1} and O_{ut2}, respectively. According to the topology shown in Fig. 3.3(b), the output voltage of phase 1 is equal to phase 2:

$$V_{boost_{Double}(out1,out2)} = V_{in} + V_{Cb} = V_{in} + V_{Cc} = 2\,V_{in} \tag{3.2}$$

Super-boost mode (SB): The step-up gain of ($3V_{in}$, $2V_{in}$) dual outputs are achieved simultaneously in this operation. As illustrated in Fig. 3.3(c), C_b is charged to V_{in}, and *Ca* is discharged in series with V_{in} to O_{ut1}, and capacitor *Cd* is charged. Thus, both V_{Cd} and the O_{ut1} achieve a voltage of $2V_{in}$. The output of phase 1, which is mirrored in phase 2, is:

$$V_{Boost_{Super}(out1)\_phase1} = V_{in} + V_{Ca} = 2\,V_{in} \tag{3.3}$$

Meanwhile, the capacitor *Cd* discharge in-series with V_{in} to achieve $3V_{in}$ at the output O_{ut2}, while *Cc* is charged to $2V_{in}$. In the next phase, *Cc* and *Cd* swapped the operation.

$$V_{Boost_{Super}(out2)\_phase1} = V_{in} + V_{Cd(2Vin)} = 3\,V_{in} \tag{3.4}$$

High-conversion mode (HC): to achieve high VCR, both power network is used. Although this topology follows the series-parallel configuration, it is inspired by Dickson's charge pump topology. As depicted in Fig. 3.3(d), the output at O_{ut2} can be determined using:

$$V_{boost_{HC}(out2)} = V_{in} + V_{Cc(3Vin)} = 4\,V_{in} \tag{3.5}$$

Power Efficiency (*PE*): The power efficiency of the charge pump in Equation. (3.6) is calculated as:

$$PE = \frac{Pout}{Pin} \times 100\% = \frac{Vout \times Iout}{Vin \times Iin} \times 100\% \tag{3.6}$$

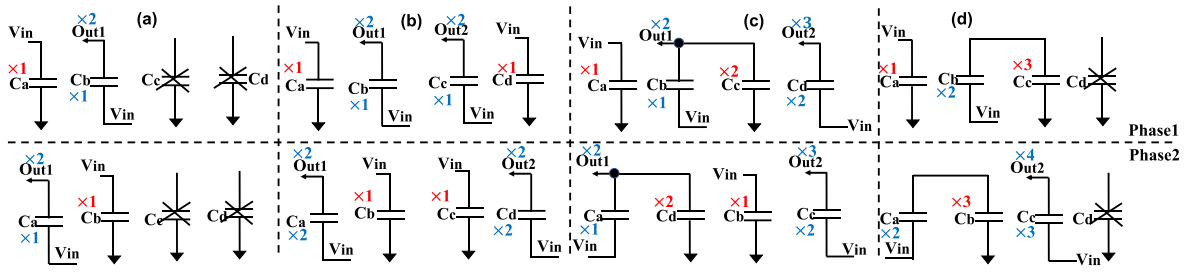


Figure 3- 3. The topology of the proposed gain modes: (a) *LP,* (b) *DB*, (c) *SB*, and (d) *HC*.

3.2.2. Proposed gain configuration unit (GCU)

The communications medium between the control clock and the transistor switches in the power converter network is essential to enable flexible and reconfigurable outputs. To ensure that only operational transistors are 'on' in intended gain configuration and 'off' switches that are not involved are entirely off and eliminate the potential leakages. Fig. 3.4(a) shows there are three input signal amplitudes in controlling the individual transistors. The two-phase clocks with an amplitude of V_{DD} of the converter are denoted by (P_1, P_2). High amplitude clocks equal to the voltage at $O_{ut1}(P_1^*, P_2^*)$ and clock amplitude being the same as O_{ut2} $(P_{1,2}^{**})$ to ensure some PMOS transistors have the high source voltage during operation are entirely off at the cut-off region with a sufficient gate voltage.

Fig. 3.4(b) proposes a control by using the two-bits control multiplexer circuit (MUX) in configuring the desire gain mode. Two high amplitude clocks are achieved through the level shifter proposed in [222]. Taking two-phase clock signals $(P_{1,2})$, level shift to higher clock amplitude from two different V_{DDH}- V_{out1} and V_{out2}. However, the challenge arises when connecting to the MUX. Regardless of the input amplitudes, the amplitude of MUX output is bounded by the V_{DDH} of the MUX. Another challenge arises as the propagation delay is triggered by different voltage amplitude from either four inputs (A-D) or two control bits (*a, b*) or the upper limit of the MUX (V_{DDH}). A long transition for input racing from 1-V to V_{DDH} level is too long due to the internal of MUX having many gate operations with individual delays in between.

As a result, there will be a delay mismatch between the input signal, V_{DDH}, and the control bits. Therefore, by the time input is at 1 V, the output is still at 0 V, racing towards 2 V at a slow pace. In this proposed design, to avoid such challenges, multiplexing is only done with three signal inputs (P_1, P_2, and V_{DD}) which keep the same amplitude level with control signal bit and V_{DDH} as depicted in Fig. 3.4(c). Therefore, any potential delay mismatch can be eliminated. After multiplexing, transistors that require high amplitude gate voltage in operation are now supplied by the level shifter. The amplitude shift of the level shifter V_{DDH} is self-powered from O_{ut1} and O_{ut2} of the proposed converter, as illustrated in Fig. 3.4(d).

(a)

Trans	LP	DB	SB	HC
Mp0	P1*	P1*	P1*	P1*
Mp1	P2*	P2*	P2*	VDD*
Mp2	VDD**	P2**	VDD**	VDD**
Mp3	VDD**	P1**	VDD**	VDD**
Mp4	P2	P2	P2	P2
Mp5	P1	P1	P1	P1
Mp6	VDD**	P1**	P2**	P2**
Mp7	VDD**	P2**	P1**	VDD**
O1	P2*	P2*	P2*	P2*
O2	P1*	P1*	P1*	P2*
O3	VDD**	P1**	P2**	P2**
O4	VDD**	P2**	P1**	VDD**
Mn0	P1	P1	P1	P1
Mn1	P2	P2	P2	P2
Mn2	VDD	P2	P1	P1
Mn3	VDD	P1	P2	VDD
t1	VDD**	VDD**	P2**	P1**
t2	VDD**	VDD**	P1**	VDD**

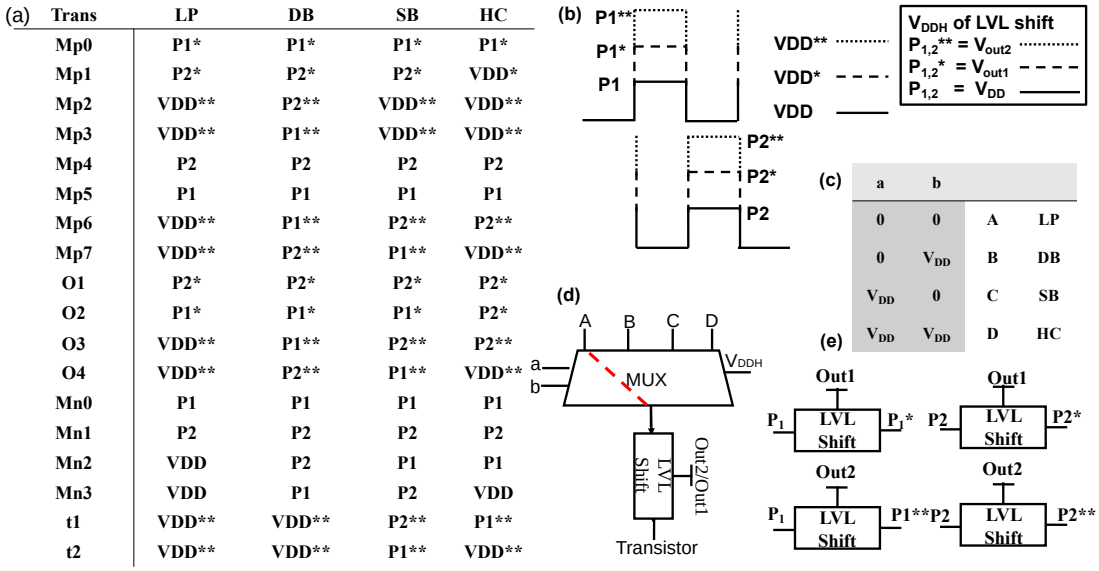


Figure 3- 4. The proposed gain configuration unit (GCU).

3.2.3. Implementation of the power stage network

The 3-V thick gate PMOS transistors are accommodated for output switches O_1-O_4. The dynamic switches are implemented to adapt between the voltage swing at the top of the capacitor and the V_{in} to ensure that the highest voltage to bulk connection is available for maximum charge sharing capability in the capacitor charging phase. These dynamic switches are implemented for (M_{p0}-M_{p3}) and (t_1, t_2), as shown in Fig. 3.5. However, the other charge transfer transistors (M_{p4}-M_{p7}) can be implemented simply with standard transistors in the 180 nm technology library without needing to use the dynamic switches.

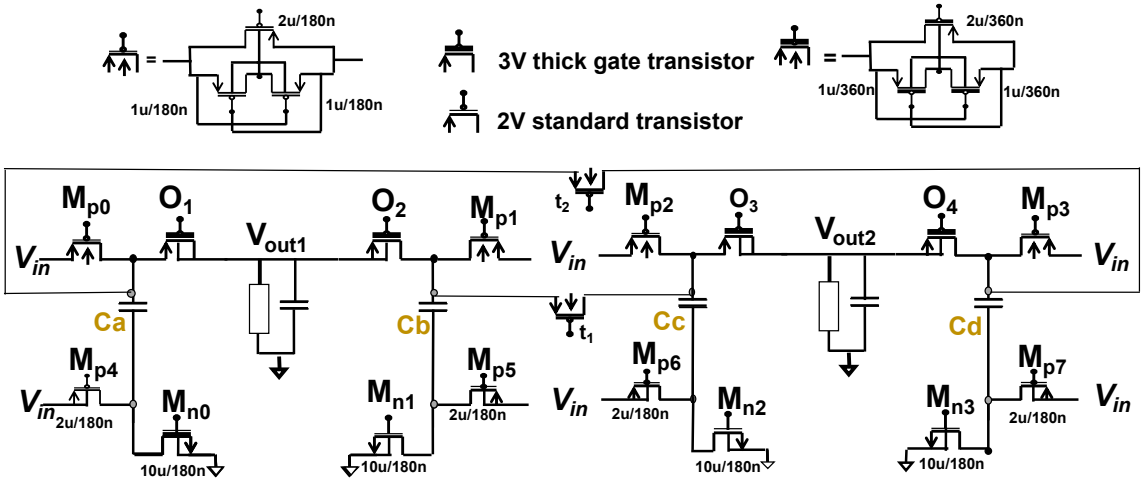


Figure 3- 5. Circuit implementation of the proposed 2-phase charge pump.

3.2.4. Circuit Configuration of Low-power (LP), Double-Boost (DB), Super-Boost (SB), and High conversion (HC) modes

The configuration of different gain modes is better understood through Fig. 3.6(a-d), where the red and blue lines represent operation at two different phases (P_1, P_2) controlled by GCU.

LP mode: As observed in Fig. 3.6(a), the capacitor *Ca* in phase-1 is charged to V_{in} through (M_{p0}, M_{n0}) while *Cb* discharges $2V_{DD}$ to the O_{ut1} in-series with V_{in} through transistors (M_{p5}, O_2). To regulated output V_{out1}, in phase 2, *Ca* is now at discharge towards O_{ut1}, similar to phase 1 operation. It is done by transistors (M_{p4}, O_1). Meanwhile, *Cb* goes back to charging.

DB mode: In this mode, both outputs have a step-up gain of $2V_{in}$, as depicted in Fig. 3.6(b). It is achieved by charging capacitor *Ca* to V_{in} via (M_{p0}, M_{n0}) while discharging *Cb*, previously charged to V_{in}. It is connected in series with the input source via (O_2, M_{p5}) to achieve $2V_{in}$ gain. Similarly, the second half of the network performs the same operation with (*Cc*, *Cd*). In phase 2, the charging/discharging action of previous capacitors is swapped. It is done by charging capacitor *Cc* to V_{in} via switches (M_{p2}, M_{n2}) and discharging previously charged capacitor *Cd* in the series with input source via (M_{p7}, O_4) to O_{ut2}.

SB mode: As proposed in Fig. 3.6(c), in phase1, capacitor *Cb* connects in series with input source to deliver $2V_{in}$ at the O_{ut1} via (M_{p5}, O_2) and parallel charging to capacitor *Cc* through (t_1, M_{p5}, M_{n2}) at the same time. In the meantime, the capacitor *Cd*, which has $2V_{in}$, is discharged via (O_4, M_{p7}) to O_{ut2} in-series with the input source and gather $3V_{in}$. Due to the design symmetry, the same amplitude as the previous phase yield at O_{ut1} and O_{ut2} delivered by *Ca* and *Cc*.

HC Mode: In this conversion mode, the circuit operation is done as described in Fig. 3.6(d). The capacitor *Cc* is charged to $3V_{in}$ from capacitor *Cb* in series with V_{in} through (M_{p5}, t_1, M_{n2}). Meanwhile, capacitor *Ca* is charged to V_{in} through (M_{p0}, M_{n0}). In phase 2, capacitor *Cb* is now discharged in-series in V_{in} to achieve $4V_{in}$ at the O_{ut2}. During this phase, *Cb* is now charged from *Ca* in series with V_{in} via (M_{p4}, O_1, O_2, M_{n1}).

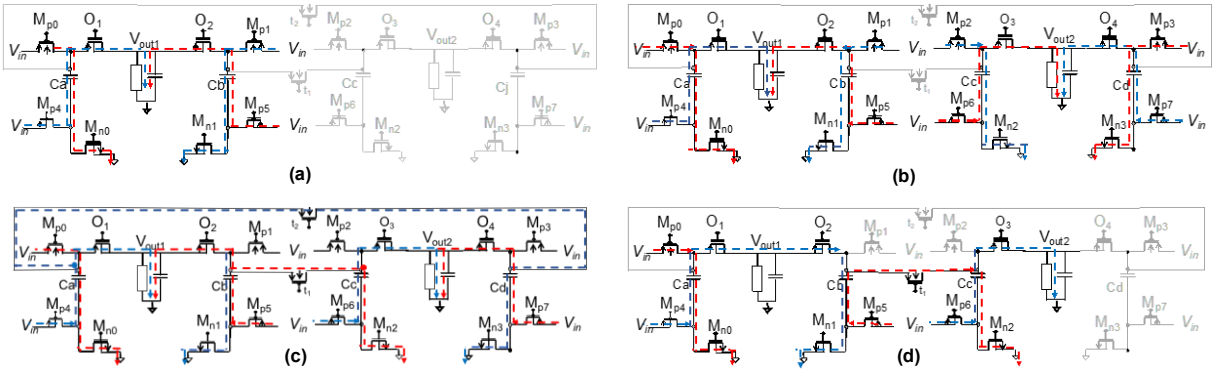


Figure 3- 6. Configuration of proposed converter for (a) *LP*, (b) *DB*, (c) *SB*, and (d) *HC* modes.

3.2.5. Implementation of gain configuration unit (GCU)

As previously discussed, controlling the non-overlapping two clock signal to configure the desired gain configuration in the power stage network is achieved by the multiplexer circuit. During the operation of the four gain modes discussed in section B, one may notice the top plate of the transistor to have a high voltage of around 2-3V_{dd}. Therefore, adjacent transistors next to that high voltage, which should be turned off to co-operate the successful desired configuration, now have high source voltage for PMOS transistors. Thus, high gate voltage equivalent to source voltage must be in the strong cut-off region and needs to be entirely off to avoid leakages. Moreover, to prevent delay mismatch due to having different amplitude inputs, the GCU or router is constructed as demonstrated in Fig. 3.7.

Consequently, the output of the multiplexer can directly connect to the level-shifter in [222]. In which case, the V_{DDH} of the level-shifter is feed-in (self-supplied) by connecting to either O_{ut1}, to produce $P_{1,2}^{*}$ or O_{ut2}, to make $P_{1,2}^{**}$, and generate desired clock amplitude depending on the gate voltage requirement of transistors in the power network. The enable gate signal V_{DD}, located next to P_1 and P_2, is implemented to switch on/off (depending on MOS type) to those unutilised switches during gain configuration. It is later denoted as V_{DDD}.

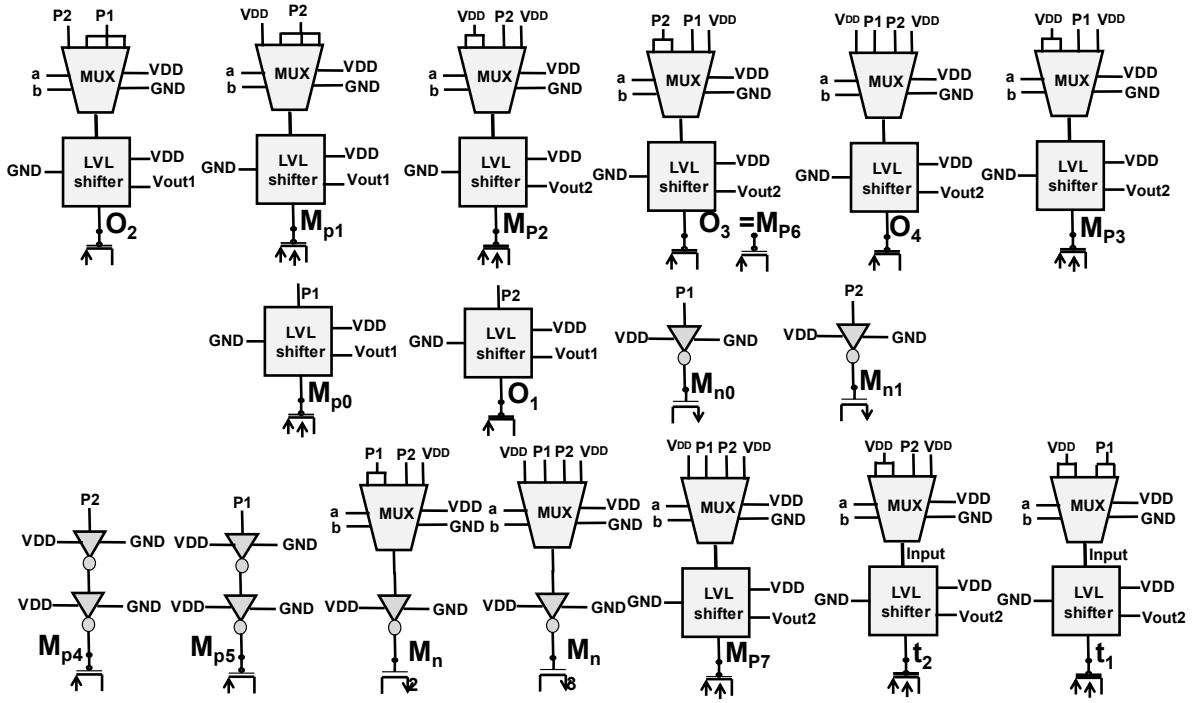


Figure 3- 7. GCU addresses the individual transistors in the charge pump network with adequate clock amplitude for optimal charge sharing.

3.3. The Simulation Set-up

The proposed design is implemented in standard 0.18 μm TSMC RF CMOS technology. The operating frequency of 3-4 MHz is chosen to certify that four 30-pF charge pump capacitors are fully charged/discharged over MOSFET switches. The output filter capacitor of 10-pF is selected for both O_{ut1} and O_{ut2}. The reason for choosing ×3 smaller capacitors than the integrated capacitors is to show that the proposed converter can regulate and reconfigure itself.

The testing approach is depicted in Fig. 3.8(a-b), whereas testing is divided into self-supplied in Fig. 3.8(a) and the stand-alone configuration in Fig. 3.8 (b). As illustrated, numerous input sources are attached to the schematic symbol to analyse each block's power consumption. According to Fig. 3.8(a-b), the power stage network's input voltage source is denoted as 'V_{in}'. Similarly, the voltage source to GCU is indicated as '$V_{DDDIGITAL}$', and the V_{DD} of the clock being 'V_{DDCLK}'. The '*Clockin*' is a square wave clock input signal and two control input bits to the multiplexer, which is used for the selection of gain modes configuration, are regarded as 'A_{small}' and 'B_{small}'. The analytical power sources use for simulation can be replaced with harvested *PV* cell output later, except for clock input and $V_{DDHDIGITAL}$ (O_{1D}/O_{2D}).

The purpose of having $V_{DDHDIGITAL}$ (O_{1D}/O_{2D}) is to analyse the power stage network's performance and power consumption by separating it from the overall power management unit. This form of testing shall be addressed as 'stand-alone' performance or without feed-in (*W/O feed-in*) mode. However, in self-supplied mode, known as feed-in (*W/feed-in*) mode, converter output is self-supplied towards the $V_{DDHDIGITAL}$ (O_{1D}/O_{2D}). Thereby, successfully simulation will achieve the desire self-supplied and self-powered power management system.

Although most of the V_{DD} rail can be combined and connect to the one input V_{DD} source, the reason for separating is to identify each power consumption of each power rail.

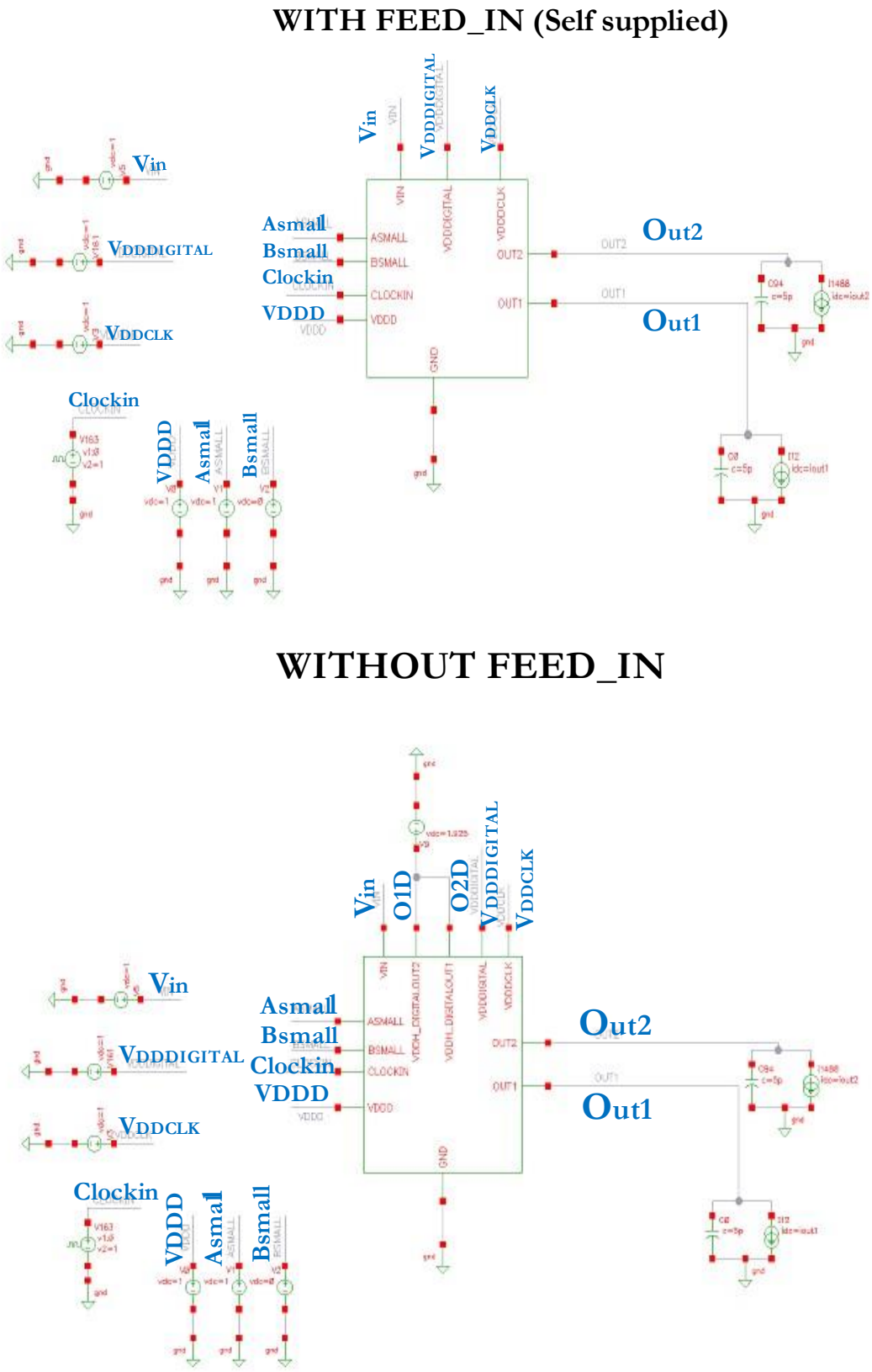


Figure 3- 8. The top-level test set up of (a) 'self-supplied (b) 'stand-alone' modes.

The feed-in block's inherent view in Fig. 3.8 (b) is depicted in Fig. 3.9. It is a block diagram constructed during the implementation of the proposed PMS. Assuming all the power sources to PMS will later replace by the energy harvester unit, input to the power stage network is protected by a single buffer. It is later removed and single out to V_{in} only due to adding more leakage current into the performance. The breakdown power consumption analysis of each of the modules is discussed in Section 3.4.1.

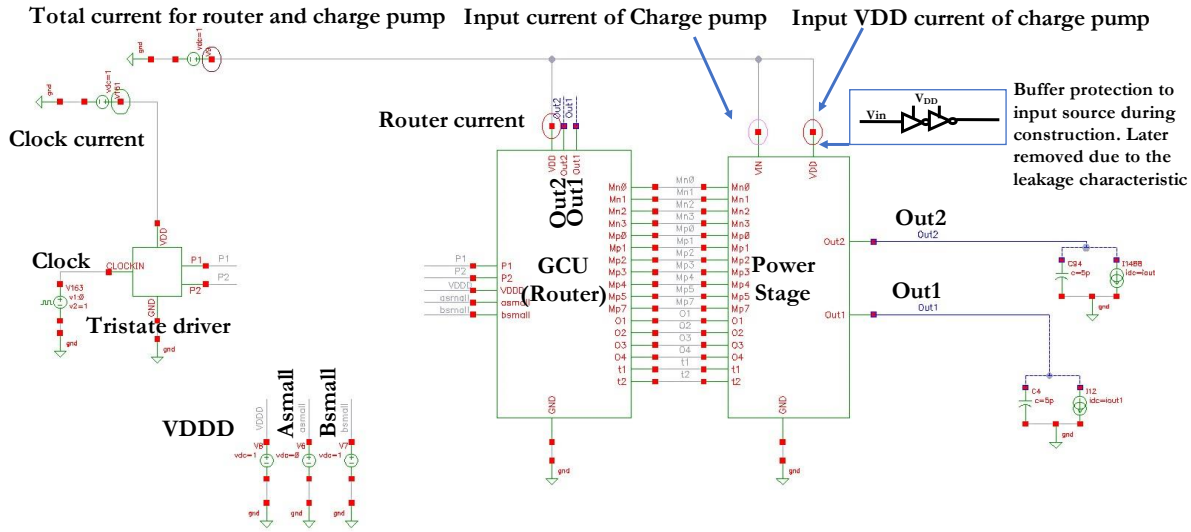


Figure 3- 9. The low-level test set up a view of self-supplied mode.

Moreover, the chip micrograph of the fabricated chip is illustrated in Fig. 3.10. The effective area is the same for both *feed-in* and *stand-alone* converters with an effective chip area (180 µm x 558 µm).

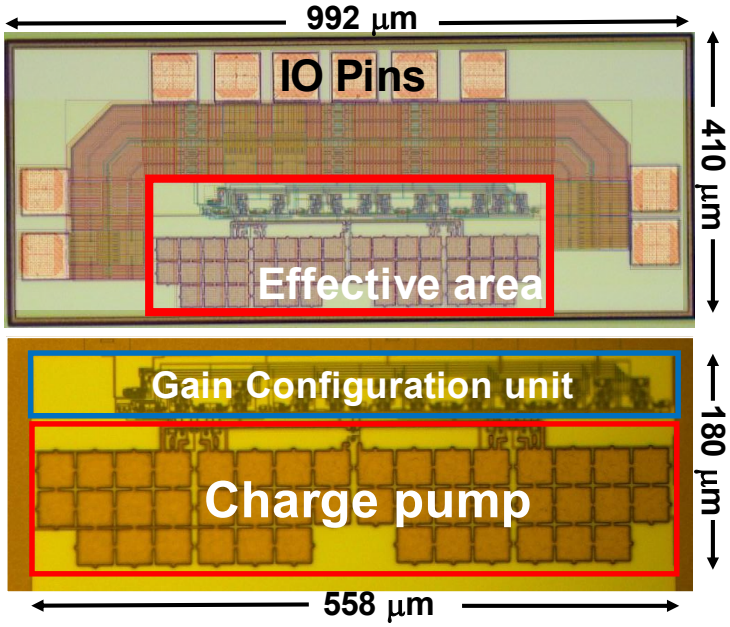


Figure 3- 10. Chip microphotograph (top) includes pins (with the back-annotated layout) and (bottom) effective chip area.

3.4. Result and discussion of the main charge pump, novel 2-phase converter.

3.4.1. Simulation Current consumption analysis of individual I/O signals in the feed-in mode of 2-phase converter

In this section, the simulation is carried out to observe the individual components' break-down power consumption in the proposed power management system. It is done by varying the output load current and keeping the identical 10-pF output capacitors. Assuming most of the voltage source are set 1 V, the measuring the current sink or current consumption from individual source supplied towards different modules define power consumption itself, since power is the multiplication of voltage-time current. No-load condition *(i1=i2*=0 A) is considered to illustrate the dynamic power consumption of each module.

The simulation results of two single output configuration modes, *LP* and *HC*, are presented in Fig. 3.11 and Fig. 3.12. Similarly, dual output modes *DB* and *SB* are simulated with varying current loads, as shown in Fig. 3.13 and Fig. 3.14. In all cases, the power stage network and GCU consume primary power consumption as expected.

The total current consumption for the router and charge pump is the sum of the current consumption of GCU or router current. Therefore, the input current of the charge pump (I_{in}) and input V_{DD} current of the charge pump (I_{VDD}) which altogether considered as total current consumption of the power stage network. The rest being the current consumption of the clock driver and the enable input (V_{DDD}), are all added together to get the system's total current consumption.

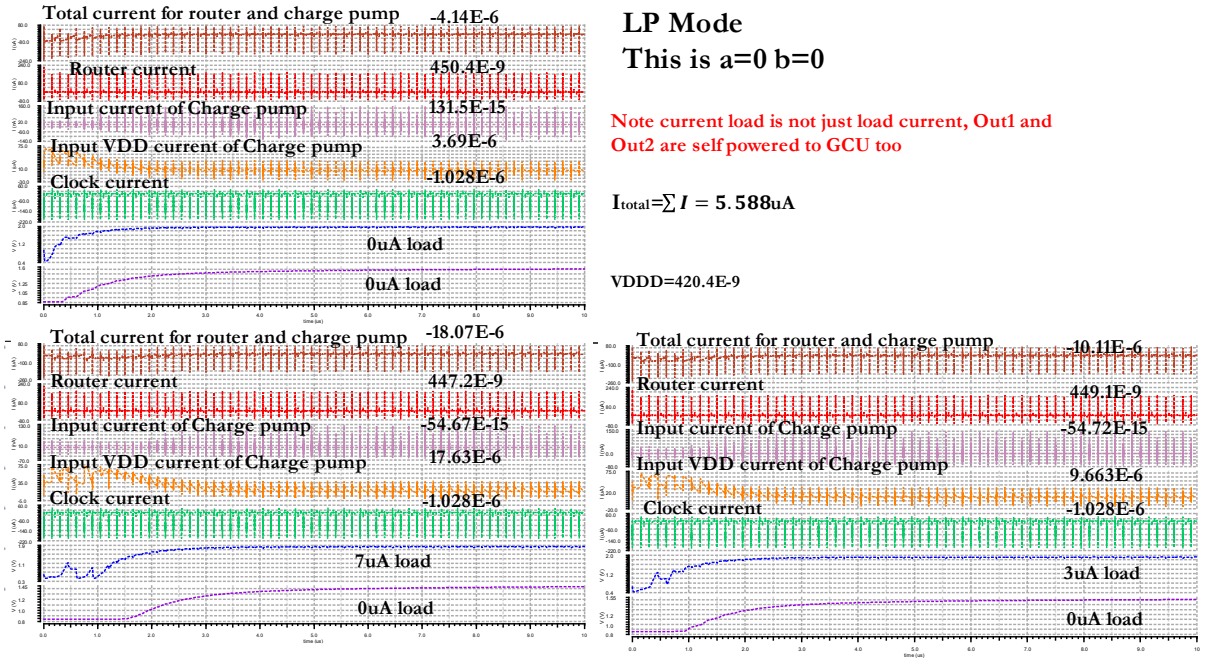


Figure 3- 11. Current consumption break-down analysis of *LP* mode.

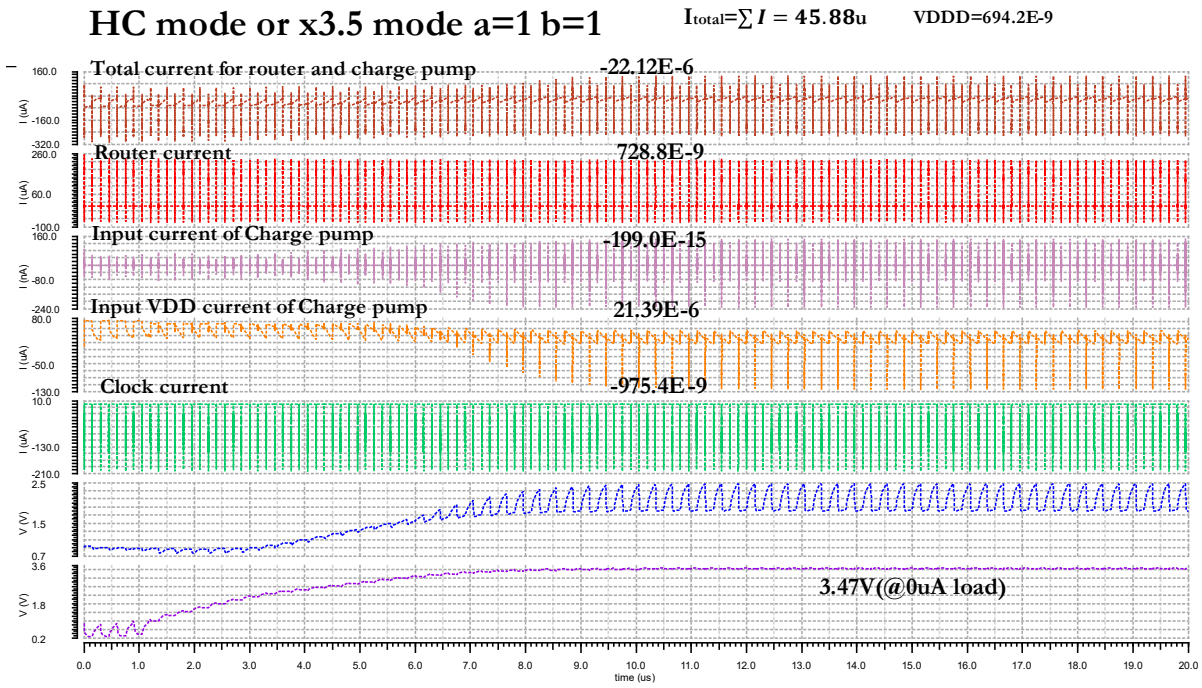
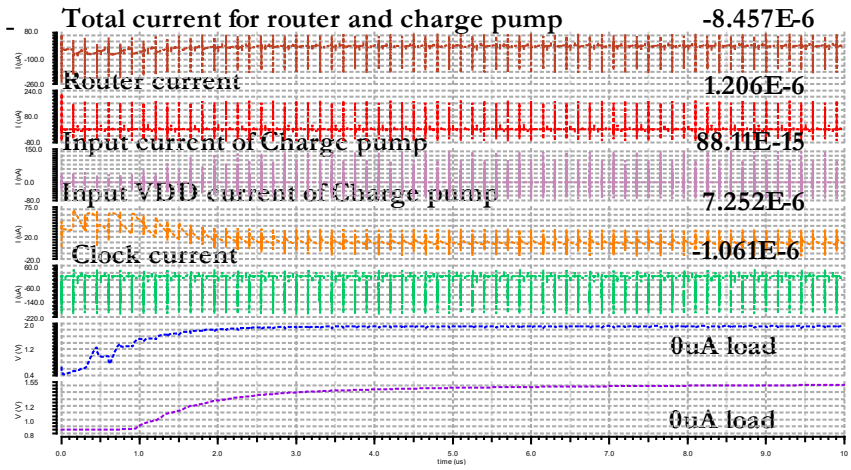


Figure 3- 12. Current consumption break-down analysis of *HC* mode.



Double Mode (x2, x2) a=1 b=0

$I_{total}=\sum I = 10.642uA$

VDDD=1.124E-6

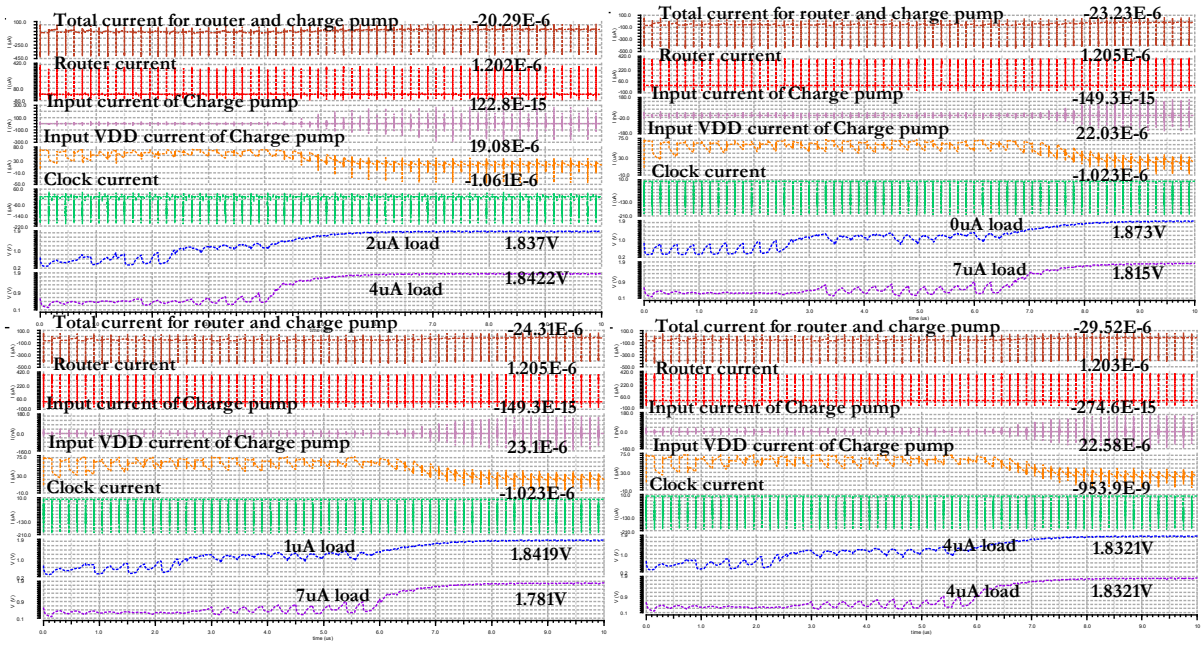
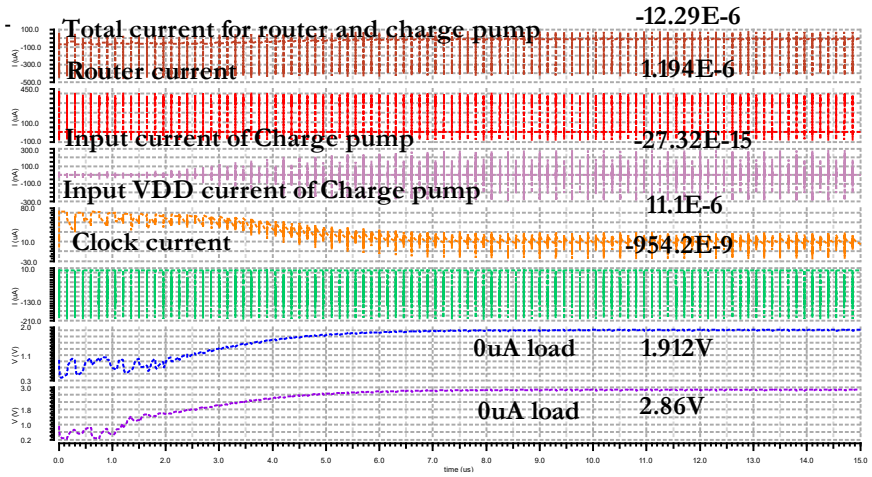


Figure 3- 13. Current consumption break-down analysis of *DB* mode.



Super Mode (x3, x2) a=0 b=1

$I_{total}=\sum I = 13.22uA$

VDDD is 25.41E-15

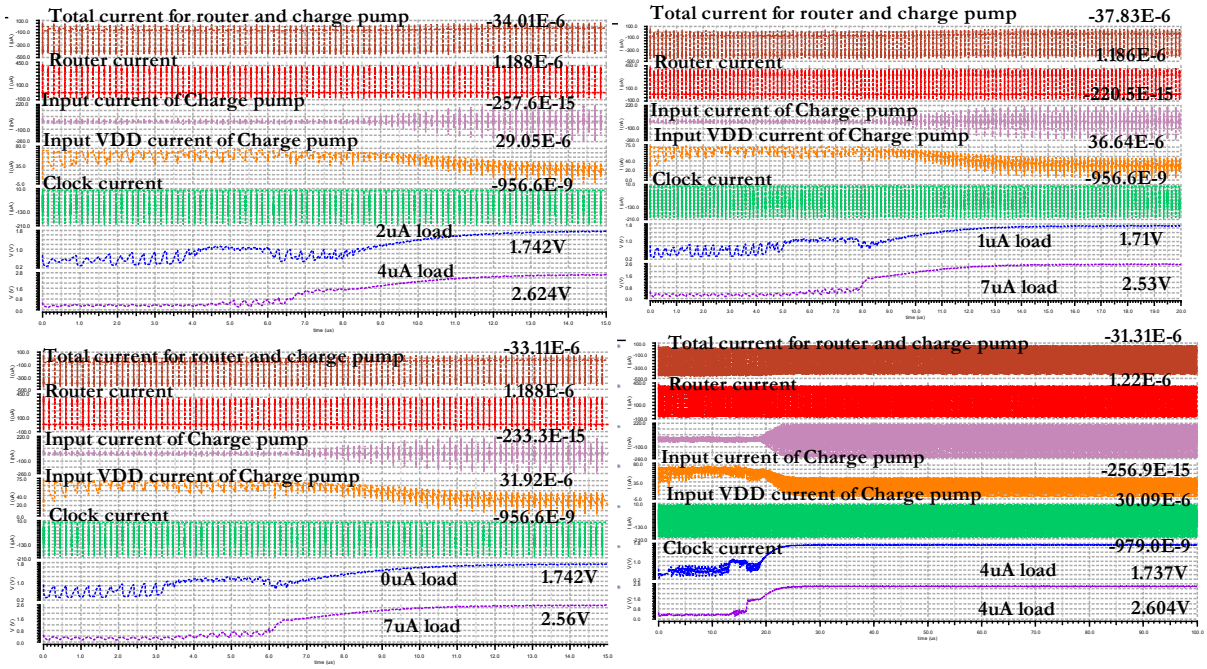


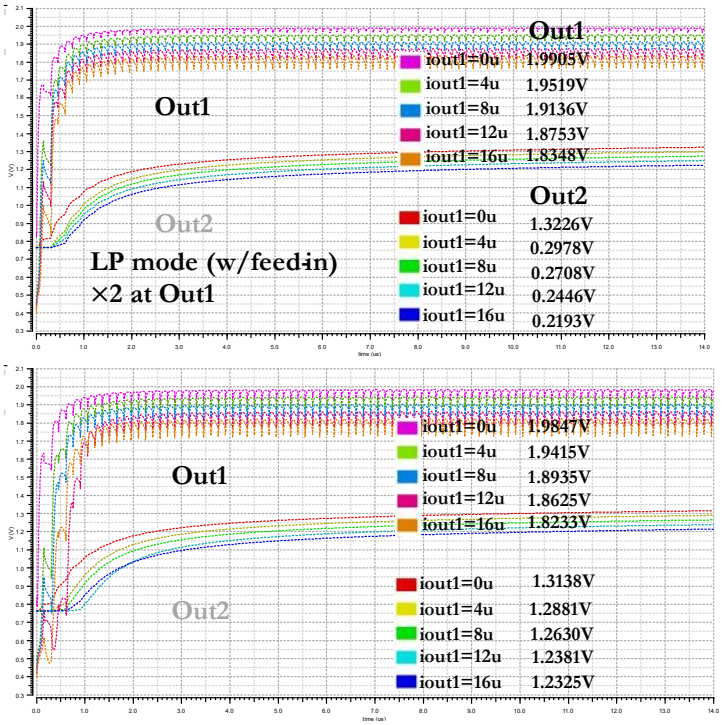
Figure 3- 14. Current consumption break-down analysis of *SB* mode.

In summary, the simulation results in Fig. 3.11 to Fig. 3.14 indicate that power consumption of power management systems at self-supplied mode consume 5.588 µW, 10.642 µW, 13.22 µW, and 23.789 µW for *LP, DB, SB*, and *HC* modes, respectively.

3.4.2. Comparison of Simulation and Post-layout simulation of self-supplied (Feed-in) 2-phase converter

Comparing schematic simulation and post-layout simulations of self-supplied (feed-in) mode is compared for parametric sweep different loading conditions for all four gain modes. They were resulting in a linear I-V characteristic response which agrees with Ohm's law, as the current load increases voltage amplitude of the decrease of the output and hence the trade-off. The following results demonstrate that well-designed symmetric charge sharing networks produce almost identical voltage outputs as expected thanks to the equivalent on-resistance R_{on} optimal paths in all four modes.

The *LP* mode's power consumption as shown in Fig. 3.15 varies from 4 µW (@i_1=0A, ~1 MΩ, V_{out1}=1.987 V) up to 36.98 µW (@i_1=16 µA, ~1 kΩ V_{out1}=1.814 V). It was achieved up to the highest efficiency of 85.89% (@V_{out1}=1.902 V, $i1$=8 µA, $Pout$=22.3 µW). This mode is ideal for operation running idle conditions (sleep mode) and low power loading.



	I1=0 I2=x	I1=4u I2=x	I1=8u I2=x	I1=12u I2=x	I1=16u I2=x
Iinavg	-2.029u	-10.01u	17.99u	-25.97u	33.96u
Vout1	1.987	1.945	1.902	1.859	1.814
Vout2	1.323	1.298	1.273	1.248	1.223
Pin	2.029u	10.01u	17.99u	25.97u	33.96u
Pout	0	7.78u	15.22u	22.3u	29.02u
Eff	0	77.7	84.59	85.89	85.47

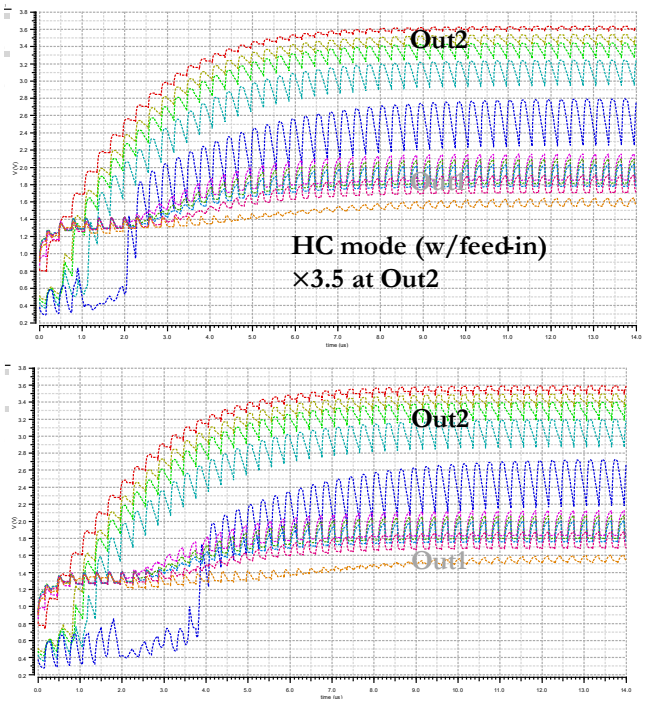
Simulation result

Post layout Simulation result

	I1=0 I2=x	I1=4u I2=x	I1=8u I2=x	I1=12u I2=x	I1=16u I2=x
Iinavg	-4.088u	-12.03u	-19.97u	-27.92u	-35.86u
Vout1	1.975	1.933	1.889	1.845	1.8
Vout2	1.314	1.288	1.263	1.237	1.212
Pin	4.088u	12.03u	19.97u	27.92u	35.86u
Pout	0	7.731u	15.12u	22.14u	28.79u
Eff	0	64.26	75.7	79.29	80.28

Figure 3- 15. The comparison of schematic simulation and post-layout simulation of feed-in *LP* mode.

Likewise, another single output *HC* mode has the highest efficiency at 53.19 % (@V_{out2}=2.517 V, i_2=16 µA, P_{out}=28.79 µW). The voltage conversion ratio (VCR) is highest at 3.558 V (@$i2$=0), as illustrated in Fig. 3.16.



	I1=x I2=x	I1=x I2=2u	I1=x I2=4u	I1=x I2=8u	I1=x I2=16u
Iinavg	-19.16u	-25.89u	-32.59u	-45.96u	-72.56u
Vout1	1.985	1.938	1.891	1.795	1.594
Vout2	3.615	3.499	3.38	3.136	2.592
Pin	19.16u	25.89u	32.59u	45.96u	72.56u
Pout	0	6.997u	13.52u	25.09u	41.47u
Eff	0	27.03	41.49	54.58	57.15

Simulation result

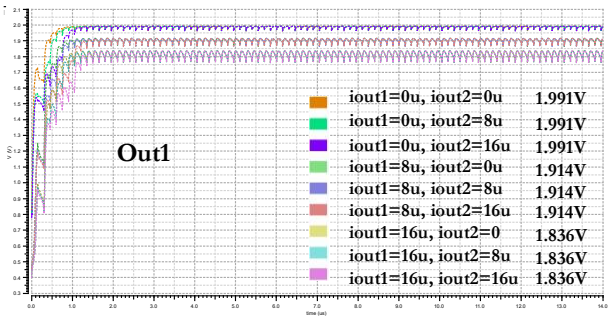
Post layout Simulation result

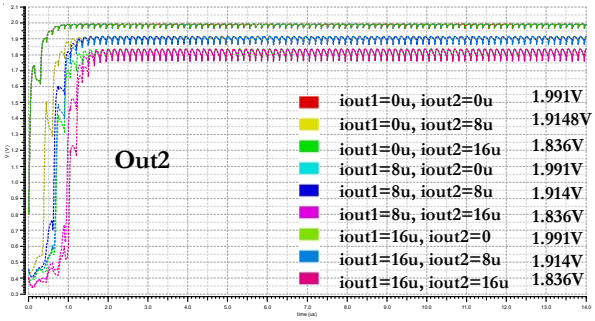
	I1=x I2=x	I1=x I2=2u	I1=x I2=4u	I1=x I2=8u	I1=x I2=16u
Iinavg	-23.05u	-29.62u	-36.19u	-49.31u	-75.7u
Vout1	1.959	1.912	1.865	1.768	1.559
Vout2	3.558	3.443	3.324	3.078	2.517
Pin	23.05u	29.62u	36.19	49.31u	75.7u
Pout	0	6.885u	13.3u	24.62u	40.27u
Eff	0	23.34	36.74	49.94	53.19

Figure 3- 16. The comparison of schematic simulation and post-layout simulation of *HC* feed-in mode.

As shown in Fig 3.17, the dual outputs *DB* mode suggests the schematic simulation produces the highest efficiency at 86.67 %(@V_{out1}=1.815 V, V_{out2}=1.814 V, i_1=16 µA, i_2=8 µA, P_{out}=43.89 µW, and P_{in}=56.07 µW). On the other hand, post-layout simulation achieved the highest efficiency at 78.28 %(@V_{out1}=1.8 V, V_{out2}=1.887 V, i_1=16 µA, i_2=8 µA, P_{out}=43.89 µW, and P_{in}=56.07 µW). Moreover, the floating outputs of post-layout simulation in *DB* mode at (i_1= i_2=16 µA) are due to the long transient time of post-layout simulation within 14-µs runtime. They can be expected to be different in experimental results with longer run time.

However, the maximum VCR for *DB* mode is achieved at the no-load condition for both simulations; V_{out1}=1.987 V and V_{out2}=1.987 V. In the post-layout simulation, V_{out1}=1.976 V and V_{out2}=1.974 V is achieved. As observed, although simulation two voltage outputs are identical, there is a slight variation in post-layout results. It is due to the non-ideal (R-C-CC) parasitic of the layout design.

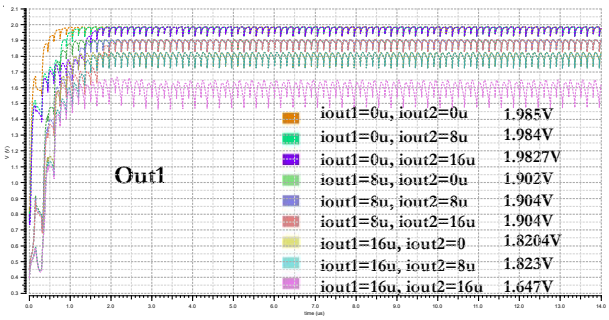


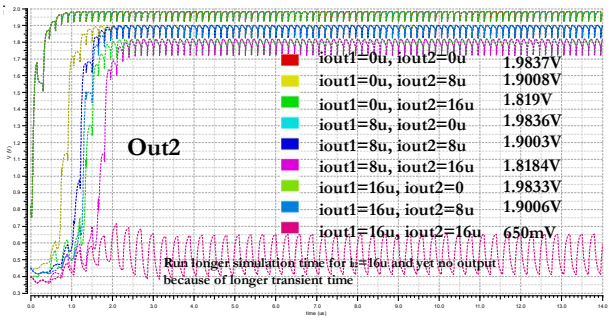


Double Boost mode (w/feed-in) ×2, ×2

Simulation result

	I1=0 I2=0	I1=0 I2=8u	I1=0 I2=16u	I1=8u I2=0	I1=8u I2=8u	I1=8u I2=16u	I1=16u I2=0	I1=16u I2=8u	I1=16u I2=16u
Iinavg	-3.98u	-19.96u	-35.92u	-19.96u	-35.93u	-51.9u	-35.92u	-51.89u	-67.86u
Vout1	1.987	1.987	1.987	1.903	1.903	1.903	1.815	1.815	1.815
Vout2	1.987	1.903	1.814	1.987	1.903	1.814	1.987	1.903	1.814
Pin	3.988u	19.96u	35.92u	19.96u	35.93u	51.9u	35.92u	51.89u	67.86u
Pout	0	15.22u	29.03u	15.22u	30.44u	44.25u	29.04u	44.26u	58.07u
Eff	0	76.27	80.82	76.26	84.73	85.27	80.83	85.29	85.57





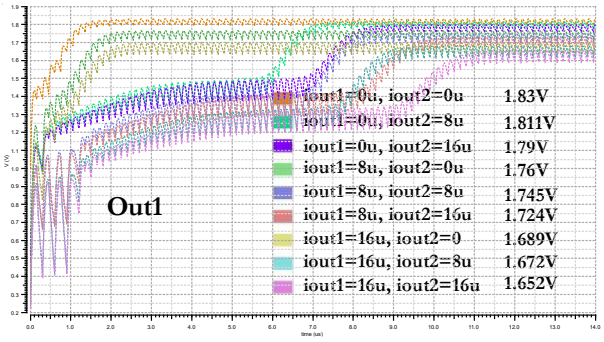
Double Boost mode (w/feed-in) ×2, ×2

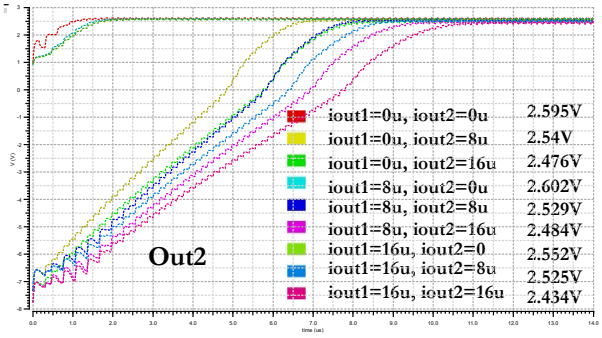
Post Layout Simulation result

	I1=0 I2=0	I1=0 I2=8u	I1=0 I2=16u	I1=8u I2=0	I1=8u I2=8u	I1=8u I2=16u	I1=16u I2=0	I1=16u I2=8u	I1=16u I2=16u
Iinavg	-8.42u	-26.31u	-40.21u	-24.3u	-40.2u	-56.09u	-40.18u	-56.07u	-122.3u
Vout1	1.976	1.976	1.975	1.89	1.89	1.89	1.8	1.8	1.593
Vout2	1.974	1.887	1.796	1.974	1.887	1.796	1.973	1.887	529.3m
Pin	8.42u	26.31u	40.21u	24.3u	40.2u	56.09u	40.18u	56.07u	122.3u
Pout	0	15.09u	28.74u	15.12u	30.21u	43.85u	28.8u	43.89u	33.99u
Eff	0	62.09	71.47	62.2	75.15	78.18	71.68	78.28	27.8

Figure 3- 17. The comparison of schematic simulation and post-layout simulation of feed-in *DB* mode.

Similarly, the dual output *SB* mode, as illustrated in Fig. 3.18, has yielded the highest efficiency at 69.61% (@V_{out1}=1.624 V, V_{out2}=2.422 V, i_1=16 µA, i_2=16 µA, P_{out}=64.75 µW, and P_{in}=93.02 µW). Meanwhile, the voltage conversion ratio (VCR) is highest with V_{out1}=1.815 V, V_{out2}=2.514 V at no-load conditions. The schematic simulation agrees with post-layout results with a bit of variation in all load conditions.

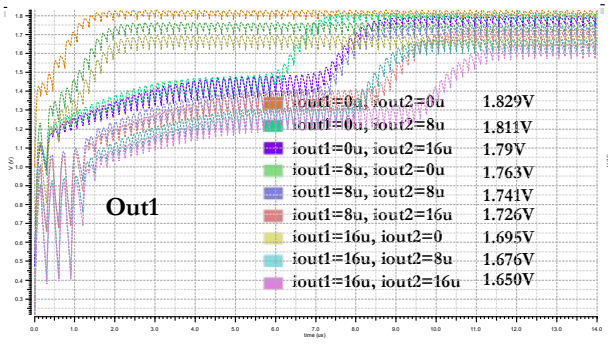


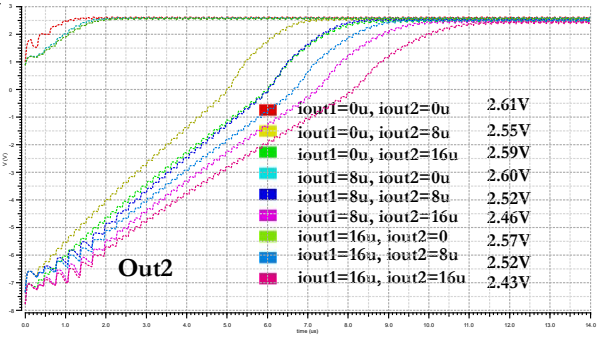


Super Boost mode (wo/feedin) ×3, ×2

Simulation result

	I1=0 I2=0	I1=0 I2=8u	I1=0 I2=16u	I1=8u I2=0	I1=8u I2=8u	I1=8u I2=16u	I1=16u I2=0	I1=16u I2=8u	I1=16u I2=16u
Iinavg	-46.52u	-58.18u	-70.59u	-56.61u	-68.53u	-81.37u	-66.82u	-79.06u	-92.48u
Vout1	1.816	1.8	1.782	1.746	1.729	1.708	1.673	1.654	1.63
Vout2	2.594	2.539	2.477	2.579	2.522	2.455	2.563	2.502	2.429
Pin	46.52u	58.18u	70.59u	56.61u	68.53u	81.37u	66.82u	79.06u	92.48u
Pout	0	20.31u	39.63u	13.97u	34u	52.94u	26.77u	46.48u	64.95u
Eff	0	34.92	56.14	24.68	49.62	65.06	40.06	58.79	70.23





Super Boost mode (wo/feedback) ×3, ×2

Post Layout Simulation result

Efficiency calculation can improve with i1=1u, i2=8u
Because i1=0 produces= P1= V1 . I1= 0 W.

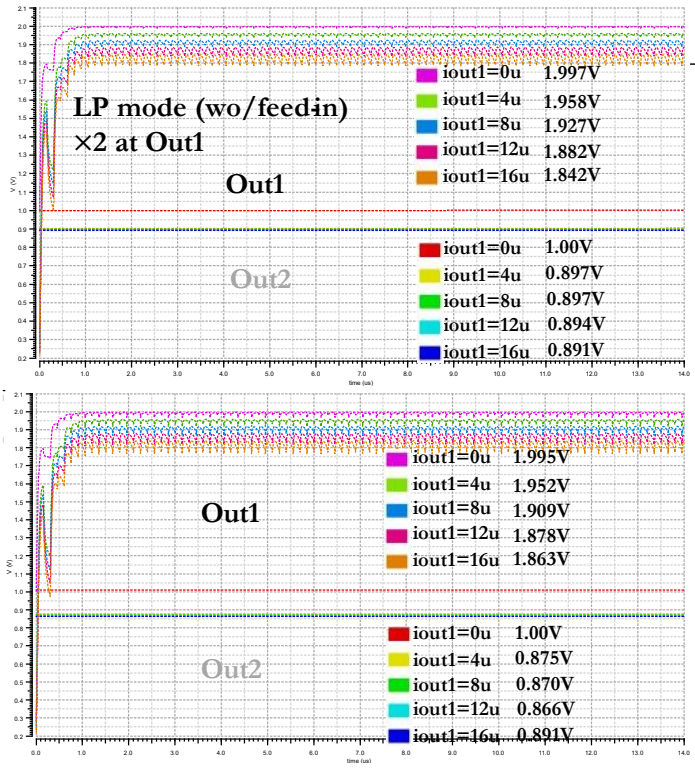
	I1=0 I2=0	I1=0 I2=8u	I1=0 I2=16u	I1=8u I2=0	I1=8u I2=8u	I1=8u I2=16u	I1=16u I2=0	I1=16u I2=8u	I1=16u I2=16u
Iinavg	-46.94u	-58.59u	71.03u	56.99u	56.99u	-81.84u	-67.18u	-79.45u	-93.02u
Vout1	1.815	1.799	1.78	1.744	1.744	1.705	1.67	1.65	1.624
Vout2	2.594	2.538	2.474	2.578	2.578	2.45	2.562	2.499	2.422
Pin	46.94u	58.59u	71.03u	56.99u	56.99u	81.84u	67.18u	79.45u	93.02u
Pout	0	20.3u	39.58u	13.95u	33.97u	52.84u	39.78u	46.39u	64.75u
Eff	0	34.65	55.72	24.48	49.28	64.56	59.21	58.39	69.61

Figure 3- 18. The comparison of schematic simulation and post-layout simulation of *SB* feed-in mode.

3.4.3. Comparison of Simulation and Post-layout simulation of stand-alone (without Feed-in) 2-phase converter

In this section, the analysis is only deduced to the power stage network's performance or converter only without considering power dropped across the other peripherical operation modules. The comparison of schematic simulation and post-layout simulation is made for stand-alone converter performance.

In Fig. 3.19, the stand-alone *LP*'s power consumption varies from 1.59 µW (@i_1=0 A, ~1 MΩ, V_{out1}=1.997 V) up to 33.48 µW (@i_1=16 µA, ~1 kΩ V_{out1}=1.814 V). It is achieved up to the highest efficiency of 86.89 % (@V_{out1}=1.905 V, i_1=8 µA, P_{out}=15.25 µW, and P_{in}=17.54 µW).



	I1=0 I2=x	I1=4u I2=x	I1=8u I2=x	I1=12u I2=x	I1=16u I2=x
Iinavg	-434.5n	-8.435u	-16.43u	24.43u	-32.43u
Vout1	1.997	1.955	1.912	1.869	1.824
Vout2	1.003	904m	898.4m	894.6m	891.6m
Pin	434.5n	8.435u	16.43u	24.43u	32.43u
Pout	0	7.819u	15.3u	22.42u	29.19u
Eff	0	92.7	93.11	91.79	89.99

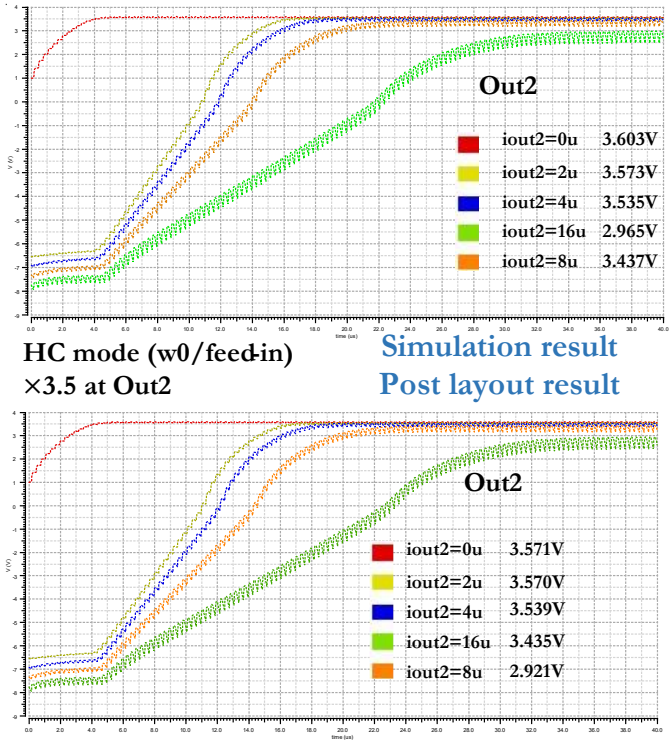
Simulation result

Post layout Simulation result

	I1=0 I2=x	I1=4u I2=x	I1=8u I2=x	I1=12u I2=x	I1=16u I2=x
Iinavg	-1.599u	-9.573u	-17.54u	-25.51u	-33.48u
Vout1	1.991	1.949	1.905	1.861	1.816
Vout2	1.009	875.4m	870.2m	866.5m	863.5
Pin	1.599u	9.573u	17.54u	25.51u	33.48
Pout	0	7.794u	15.24u	22.33u	29.06u
Eff	0	81.42	86.89	87.55	86.78

Figure 3- 19. The comparison of schematic simulation and post-layout simulation of *SB* stand-alone mode.

Similar single output *HC* mode has yielded the highest efficiency at 68.58 % (@V_{out2}=3.342 V, i_2=8 µA, P_{out}=26.73 µW) instead of system efficiency (feed-in), from the previous section, 53.19%. The voltage conversion ratio (VCR) is highest at 3.574 V (@i_2=0), as illustrated in Fig. 3.20.



	I1=x I2=x	I1=x I2=2u	I1=x I2=4u	I1=x I2=8u	I1=x I2=16u
Iinavg	-23.88u	-26.85u	-30u	-37.97u	-66.84u
Vout1	1.937	1.925	1.911	1.867	1.645
Vout2	3.577	3.533	3.486	3.357	2.812
Pin	23.88u	26.85u	30u	37.97u	66.84u
Pout	0	7.067u	13.94u	26.86u	44.u
Eff	0	26.32	45.47	70.75	67.3

Simulation result

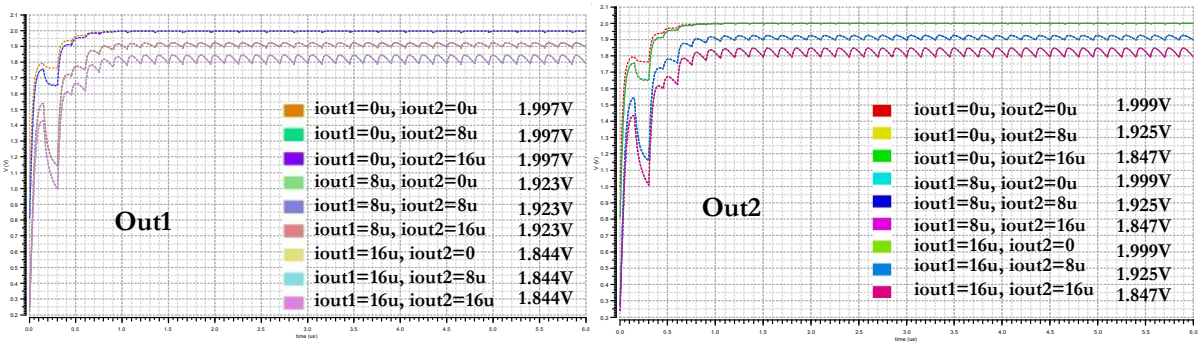
Post layout Simulation result

	I1=x I2=x	I1=x I2=2u	I1=x I2=4u	I1=x I2=8u	I1=x I2=16u
Iinavg	-24.41u	-27.4u	-30.61u	-38.98u	-68.34u
Vout1	1.938	1.925	1.911	1.86	1.627
Vout2	3.574	3.529	3.48	3.342	2.772
Pin	24.41u	-27.4u	30.61u	38.98u	68.34u
Pout	0	7.058u	13.92u	26.73u	44.34u
Eff	0	25.76	45.47	68.58	64.89

Figure 3- 20. The comparison of schematic simulation and post-layout simulation of *HC* stand-alone mode.

As illustrated in Fig. 3.21, the dual outputs *DB* mode in simulation produces 96.91 % (@V_{out1}=1.912 V, V_{out2}=1.912 V, i_1=8 µA, i_2=8 µA, P_{out}=30.61 µW, and P_{in}=31.59 µW). In comparison, the post-layout simulation achieved the highest efficiency at 91.09% (@V_{out1}=1.905 V, V_{out2}=1.995 V, i_1=8 µA, i_2=8 µA, P_{out}=30.51 µW, and P_{in}=33.49 µW). Moreover, the previous (*feed-in*) post-layout simulation in *DB* mode ($i1$= $i2$=16 µA) no longer produces the floating output, and efficiency is improved.

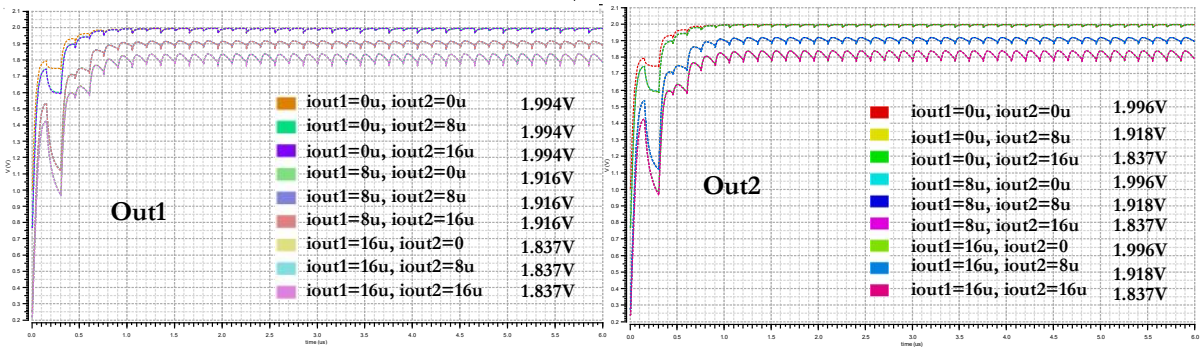
Furthermore, the maximum VCR for *DB* mode in simulation has achieved V_{out1}=1.997 V and V_{out2}=1.999 V. Similarly, the post-layout simulation's VCR has yield V_{out1}=1.991 V and V_{out2}=1.995 V.



Double Boost mode (wo/feedin) ×2, ×2

Simulation result

	I1=0 I2=0	I1=0 I2=8u	I1=0 I2=16u	I1=8u I2=0	I1=8u I2=8u	I1=8u I2=16u	I1=16u I2=0	I1=16u I2=8u	I1=16u I2=16u
Iinavg	-558.3n	-16.08u	-31.64u	-16.07u	-31.59u	-47.15u	-31.61u	-47.13u	-62.69u
Vout1	1.997	1.997	1.997	1.912	1.912	1.912	1.824	1.824	1.824
Vout2	1.999	1.915	1.827	1.999	1.912	1.827	1.999	1.915	1.827
Pin	558.3n	16.06u	31.64u	16.07u	31.59u	47.15u	31.61u	47.13u	62.69u
Pout	0	15.32u	29.23u	15.3u	30.61u	44.52u	29.19u	44.51u	58.41u
Eff	0	95.24	92.37	95.21	96.91	94.44	92.34	94.42	93.19



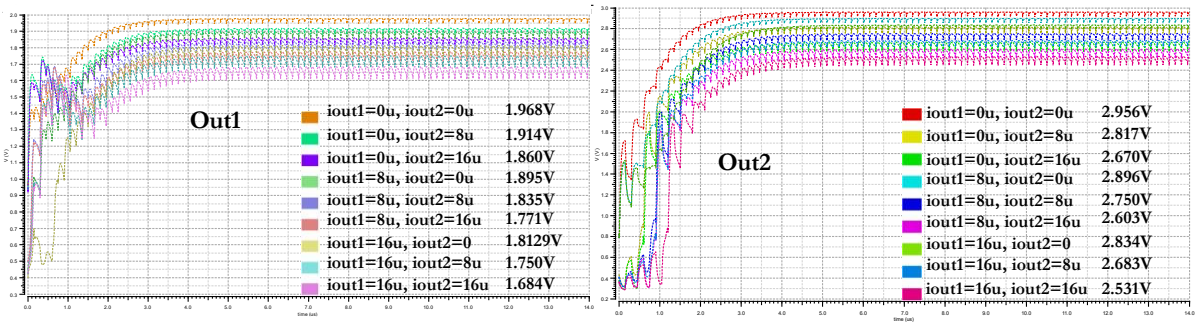
Double Boost mode (wo/feedin) ×2, ×2

Post Layout Simulation result

	I1=0 I2=0	I1=0 I2=8u	I1=0 I2=16u	I1=8u I2=0	I1=8u I2=8u	I1=8u I2=16u	I1=16u I2=0	I1=16u I2=8u	I1=16u I2=16u
Iinavg	-2.492u	-18.01u	-33.57u	-17.97u	-33.49u	-49.05u	-33.49u	-49.01u	-64.57u
Vout1	1.991	1.991	1.991	1.905	1.905	1.905	1.816	1.816	1.816
Vout2	1.995	1.908	1.818	1.995	1.908	1.818	1.994	1.908	1.818
Pin	2.492u	18.01u	33.57u	17.97u	33.49	49.05u	33.49u	49.01u	64.57u
Pout	0	15.27u	29.09u	15.24u	30.51u	44.33u	29.06u	44.32u	58.14u
Eff	0	84.75	86.65	84.82	91.09	90.37	86.77	90.43	90.03

Figure 3- 21. The comparison of schematic simulation and post-layout simulation of *DB* stand-alone mode.

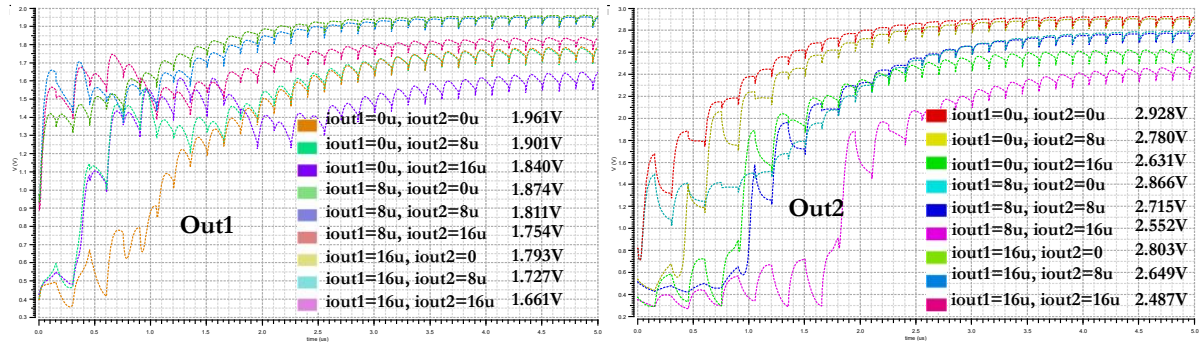
Lastly, the dual output *SB* mode in Fig. 3.22 has yield the highest efficiency at 72.17 % (@V_{out1}=1.735 V, V_{out2}=2.535 V, i_1=8 µA, i_2=16 µA, P_{out}=54.44 µW, and P_{in}=75.43 µW). Meanwhile, the voltage conversion ratio (VCR) is maximum with V_{out1}=1.954 V, V_{out2}=2.916 V at no-load conditions. Simulation results also agree with post-layout results with slight variation apart from the transient time to reach saturation takes a few more microseconds.



Super Boost mode (wo/feedin) ×2, ×3

Simulation result

	I1=0 I2=0	I1=0 I2=8u	I1=0 I2=16u	I1=8u I2=0	I1=8u I2=8u	I1=8u I2=16u	I1=16u I2=0	I1=16u I2=8u	I1=16u I2=16u
Iinavg	-6.924u	-30.54u	-54.18u	-22.72u	-46.33u	-69.98u	-38.52u	62.11u	85.76u
Vout1	1.973	1.912	1.849	1.886	1.822	1.757	1.795	1.729	1.66
Vout2	2.954	2.804	2.647	2.892	2.74	2.579	2.829	2.674	2.509
Pin	6.924u	30.54u	54.18u	22.72u	46.33u	69.98u	38.52u	62.11u	85.76u
Pout	0	22.43u	42.35u	15.09u	36.49u	55.32u	28.72u	49.05u	66.72u
Eff	0	73.46	78.17	66.4	78.77	79.05	74.58	78.97	77.8



Super Boost mode (wo/feedin) ×2, ×3

Post Layout Simulation result

	I1=0 I2=0	I1=0 I2=8u	I1=0 I2=16u	I1=8u I2=0	I1=8u I2=8u	I1=8u I2=16u	I1=16u I2=0	I1=16u I2=8u	I1=16u I2=16u
Iinavg	-13.15u	-36.47u	-59.82u	-28.78u	-52.09u	75.43u	-44.4u	67.7u	91.04u
Vout1	1.954	1.892	1.828	1.865	1.801	1.735	1.773	1.705	1.636
Vout2	2.916	2.764	2.604	2.854	2.699	2.535	2.791	2.633	2.464
Pin	13.15u	36.47u	59.82u	28.78u	52.09u	75.43u	44.4u	67.7u	91.04u
Pout	0	22.11u	41.67u	14.92u	36u	54.44u	28.36u	48.34u	65.6u
Eff	0	60.62	69.65	51.85	69.1	72.17	63.88	71.41	72.05

Figure 3- 22. The comparison of schematic simulation and post-layout simulation of *SB* stand-alone mode.

In summary, the power consumption is the lowest in *LP* mode as intended. The converter displays the fast transient response in all modes with ultra-low power consumption, such as 1.599 µW, 2.492 µW, 13.15 µW, and 24.41 µW for *LP, DB, SB*, and *HC* modes.

3.4.4. The summary of Output Voltage and Power efficiencies of the proposed converter

As illustrated in Fig. 3.23 the from the minimum of 1 V as input supply, the VCR of the self-powered converter has achieved 1.975 V in *LP*, 3.558 V in *HC*, 1.954 V in SB_{Out1}, 2.916 V in SB_{Out2}, 1.976 V in DB_{Out1}, and 1.974 V in DB_{Out2}. The voltage conversion efficiency of the four modes has been achieved from 88.95% up to 98.75%. Moreover, the load regulation for the converter is also tested with R_{load} range from 1M-24 kΩ . Its output power over power efficiencies (*PE*) is depicted in Fig. 3.24, and results are based on Appendix 2.4. The *LP* mode has the highest efficiency of 80.28% and produces up to 29 µW. It is noteworthy to mention a trade-off between VCR and *PE*.

Furthermore, to investigate the charge pump's *PE* alone in the proposed system, the result is compared with no feed-in powered back to the subsystem, meaning the charge pump only supplies the loads. The no feed-in system's *PE* achieved up to 90.43% in *DB* mode and generated the highest power output of 64.75 µW (@69.61% PE) in SB mode. The steady-state output is achieved within 4-µs for all modes except HC mode, which takes about 6 µs to settle. The ripple output(ΔV) is highest in *HC* with 50 mV, but 16 mV has been achieved for the rest of the modes.

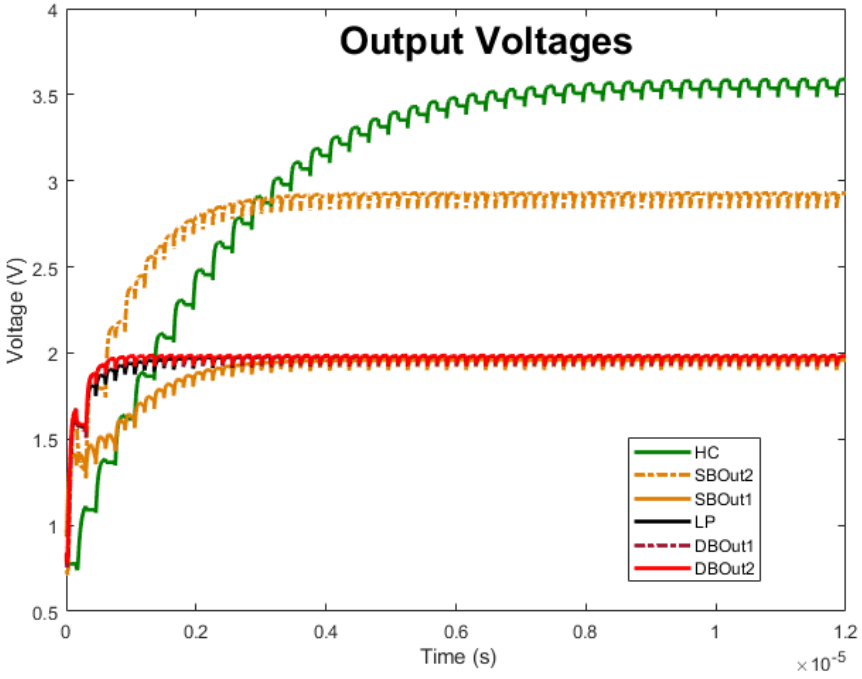


Figure 3- 23. Output voltages of (a) *LP*, (b) *HC*, (c) *DB* and (d) *SB* at 1 MΩ and 10 pF.

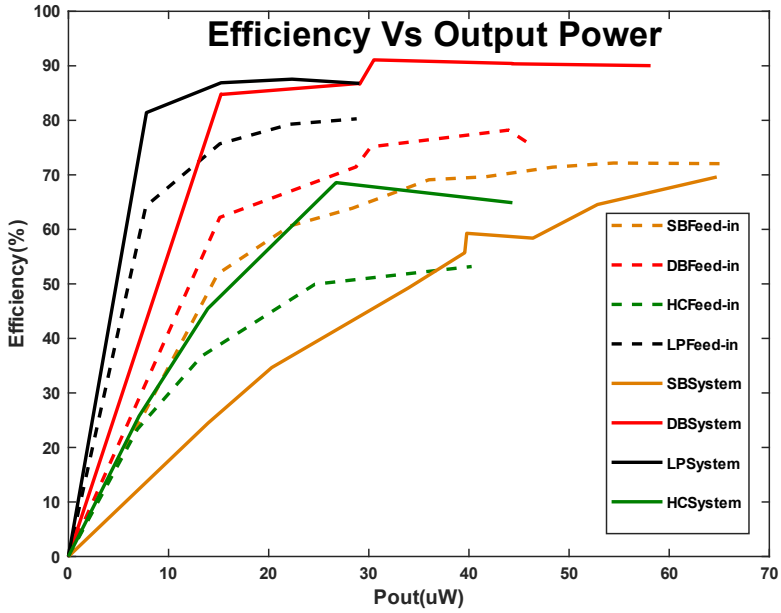


Figure 3- 24. The efficiency vs the output power compared with feed-in (*W/F*) and without feed-in (*Wo/F*) designs.

3.4.5. The process variation and mismatch corner

The measurement output voltage can expect to be less than the post-layout simulation result. In this charge pump design, L parasitic is not a big concern; R-C-CC extraction in the post-simulation is considered. The only parasitic parameter is not enough to guarantee my circuit's operation after manufacturing due to process variation. Therefore, robust post-layout simulations are depicted in Fig. 3-25(a-c). Not only the flying capacitors variations but all the transistors are also considered in this Monte Carlo simulation. The Monte Carlo simulation demonstrates the potential process variation in rigid corners and mismatch are described in Fig. 8(a-b). DB mode is chosen because it produces the same VCR (×2) at both outputs, and hence symmetry performance of the power stage for each output side can be easily compared and levelled with this mode. The DB mode in standard room temperature of 27°C with 8 µA loads at both outputs yields 1.884 V at 79% PE. Taking 50 sample point of Monte Carlo post-layout simulation, the variation in output voltages (Out1, Out2) in Fig. 3-25(a) suggests that even in the worst corner output voltage with same set up remain at 1.87 V. The standard deviation of 0.004 and mean value of 1.883 V is achieved. Similarly, Fig. 3-25 (b) *PE* results in a mean value of 79.2 % and a standard deviation of 0.426. All VCRs at dynamic load change from 0-16 µA current loads are compared. As seen Fig. 3-25 (c), although approximately 4us transient time is required for the initial stage, the drastic load changes. Moreover, the high ripple in HC mode at a high load can be controlled by a fast switching process.

Furthermore, the potential temperature variation had also been considered since the power converter is intended for a wearable device. The assumption had made that in cold region room temperature of 15°C to the body temperature up to 35-45°C were considered, shown in Fig below. In both extreme cases, there was a little as 1% change in power efficiency and the milli-volt change to the output voltages. It is shown in Fig. 3.26.

As observed, even in a worse corner, the efficiencies remain relatively stable for both Monte Carlo post-layout simulation in Fig. 3.25 and Fig. 3.26. The results justified that the presented simulations results were reliable and can be expected to have a close approximation to the experimental result.

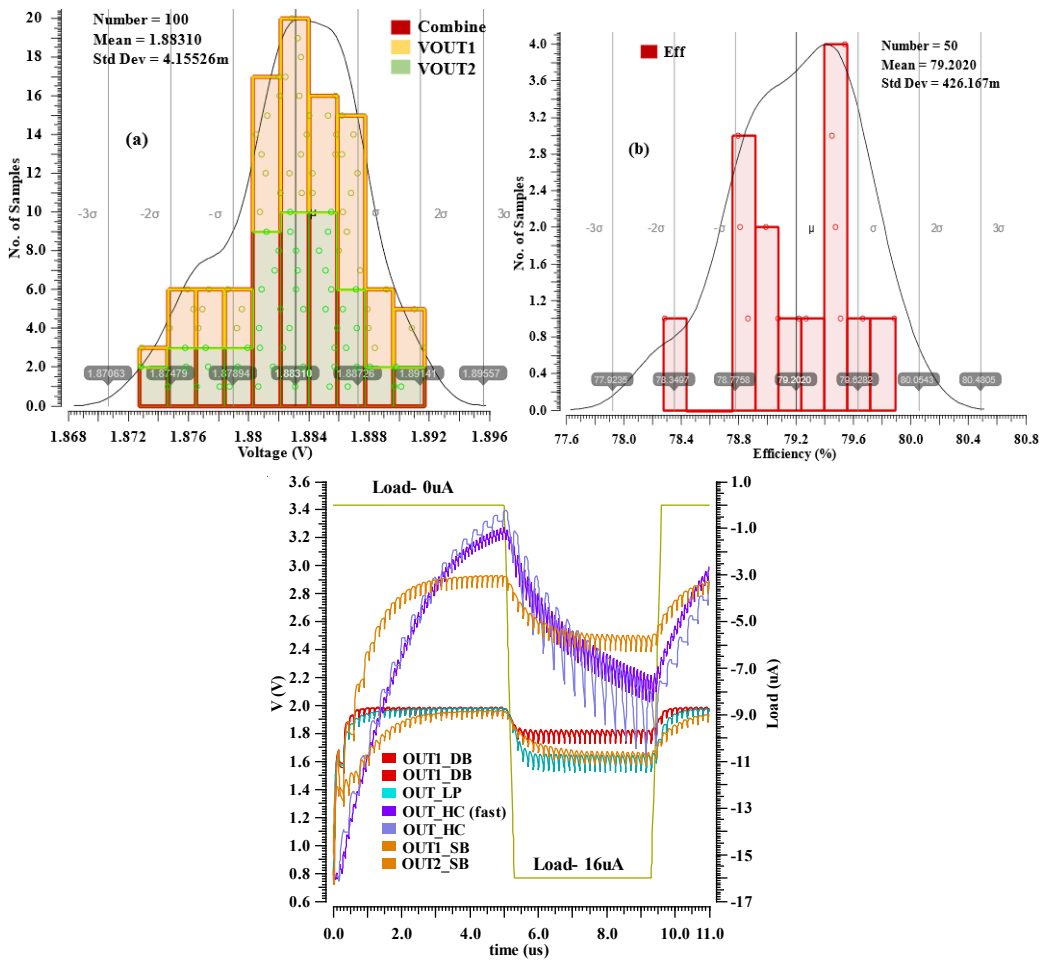


Figure 3- 25. The process variation in rigid corners and mismatch of Montecarlo simulation for (a) Output Voltages and (b) Efficiency are illustrated. It is depicted in *DB* mode with 8-µA load at Out1 and Out2. (c) All modes at dynamic load 0-16-0 µA.

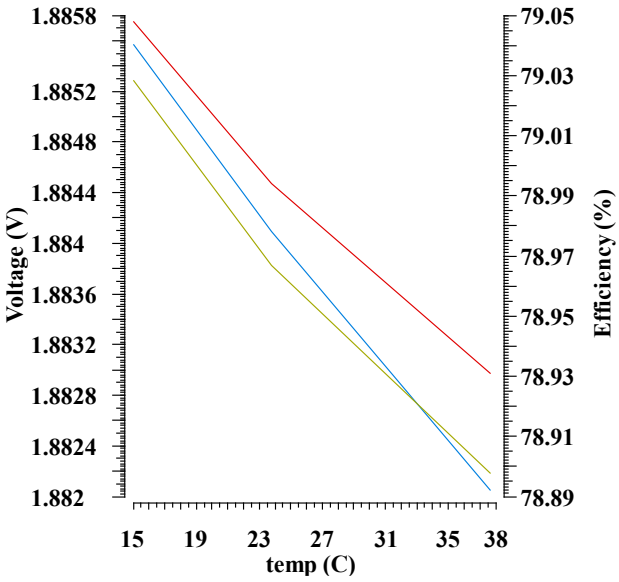


Figure 3- 26. The variation in voltage and efficiency over temperature change.

3.4.6. Comparison with state-of-the-art and conclusion

A comparison between this proposed design and the literature is shown in TABLE 3.1. Assuming that each *PV* cell provides approximately 0.5 V, a 1 V input can be achieved by stacking two *PV* cells in parallel [163, 223]. Feed-in (self-powered) converters have acquired 1.975 V in *LP*, 3.558 V in *HC*, 1.954 V in SB_{Out1}, 2.916 V in SB_{Out2}, 1.976 V in $DB_{Out1,}$ and 1.974 V in DB_{Out2}. Moreover, to demonstrate the proposed converter's performance stability in varying load conditions, the load regulation was tested with a R_{load} range from 1MΩ - 24 kΩ. Its output power over power efficiencies (*PE*) is depicted in Fig. 3.24. The *LP* mode has the highest power efficiency of 80.28% and produces up to 29 μW. It is noteworthy to mention a trade-off between VCR and power efficiency.

Furthermore, to investigate the stand-alone charge pump's *PE*, converter output only supplies towards the loads in the proposed system. The result is compared with the converter with feed-in; outputs of the converter provided to the subsystem, and the loads. The overall system's *PE* reached 90.43% in *DB* mode and generated the highest power output of 64.75 μW (@69.61% *PE*) in *SB* mode. The steady-state output was achieved within 4 μs for all modes except the *HC* mode, which required 6 μs to settle. The ripple output (ΔV) is highest in HC with (50 mV) but is lowest (16 mV) has achieved for the remaining modes.

Moreover, this proposed design maintains a high-power efficiency even in the feed-in system (self-powered). Apart from [203], other works require an external power source for both the converter and its peripherical circuits. Moreover, our converter offers a flexible range of gain (similar to [207, 224]) and step-up gains (similar to that in [159]). Unlike SISO converters [129, 207] which are highly reconfigurable, most SIDO converters such as [159, 225] are designed with fixed gain multi outputs. Although this converter does not have the step-down option or the non-integer gains in [156], the proposed design is highly flexible. It can be easily implemented with additional step-up or step-down gains at the expense of making some changes in GCU. In [226], a similar converter uses MUX in gain configuration, but [129, 207] uses programming, and [203] uses the state machine. Furthermore, [203] discusses the benefit of using dual output designs and proposed the dual output converter. In comparison to our design, their system has poor voltage ripple regulation, low efficiency, and fixed gain configuration. Lastly, in contrast with literatures [159, 207, 226], this design uses small integrated capacitors, which minimises the effective chip area and cost, while still producing a high-power density.

TABLE 3- 1. PERFORMANCE SUMMARY OF NOVEL 2-PHASE CONVERTER AND COMPARISON WITH STATE-OF-THE-ART.

Specification	This work	[159] JSSC'15	[207] TCASI'19	[225] VLSI'19	[203] Springer'20	[224] ISSCC'17	[129] T Ind Elec'09	[226] TCASI'20	[156] Access'19
Technology	180nm	35nm	130nm	130nm	65nm	28nm	35nm	180nm	180nm
Result	Post-Simu	Measured	Simulation	Measured	Measured	Measured	Simulation	Measured	Simulation
Input (V)	1	1.1	0.7-3.5	1.5	1.05-1.4	1.3-1.6	1.5-3.3	0.64-1.4	1
Output (V)	1.98 - 3.6	2,3	0.2-3.5	0.44,0.88	0.55,1	04.-0.9	0.9-3.3	3-4.2	0.47-2.85
I_{load} (mA)	0.032	24	0.1	12	0.35,0.01	100	90		0.04-0.1
VCRs(×)	2, 3, 4	2,3	11 CRs (SD/SU)	1/3,2/3	1/2,1	-	11CRs (SD/SU)	2.14-6.56	3/2,1/2.1,2,3
No. of outputs	2,1	2	1	2	2	2	1	1	2
$P_{out\ max}$(mW)	0.0656	2.5	-	-	-		-	<2.1m	0.23
P_{Den}(mW/mm^2)	0.653	-	-	-	1.32	150	-	0.359	-
Ripple(mV)	16, 50(@HC)	16-210	-	20-60	50-80	-	-	-	14-59
Efficiency (%)	80.28 W/F 90.43 Wo/F	89.5	83.41 (SD) 74.69 (SU)	78	78	83.8	88	88.9 @1.4V Vin,3.4V Vout	85.26
Int. Passive Device	30pF ×4 (MIM)	9.4μF	1.2nF	0.98nF	450pF (MIM)	8.1nF(MOM +MIM)	0.33uF	19.8nF	1nF ×4 (MIM)

3.5. Summery

This chapter demonstrated a new switched-capacitor approach consisting of a 2-phase scheme.

- **Minimize the chip area;** the charge pump capacitor size will reduce to the Pico Farad region (1-nF in the 4-phase design) for smaller chip area size, contributing directly to the cost.
- **The control clock generator and power stage network's complexity** over the previously proposed 4-phase charge pump design **has been reduced**. As the design complexity reduces, the use of components to generate the desired clock also **decreases, and** consequently, the **power consumption** of the sub-circuit is minimized.
- Results verify that this converter is **low-powered** and only consumes a few microwatts (1.59-24.41 μW for *stand-alone* and 4-46.94 μW for *feed-in* systems) to operate**.**
- **Functional GCU with the transistor-based analogue design** is proposed over the programmed Verilog-A.
- Thanks to differential load connection, I have **eliminated** the need for an output peak detector (internal discontinuous intermediate output voltages to continuous stable DC output).
- Output performances and efficiencies of the proposed converter is comparable to the state-of-the-art designs as described in TABLE 3.1.
- This converter is **reconfigurable** as the two outputs with four capacitor connections to achieve four different voltage/power modes.
- The converter has produced **single output reconfigurable** for idle mode conditions and **dual output reconfigurable** for a wide range of applications as described in the application example in section 1.7.
- Using two symmetric paths (*O1, O2*), the interleaving scheme enhances the output ripples **(self-regulate)** without needing the large filter capacitor. It has been demonstrated that the filter capacitor (10-pF) one third smaller than the integrated capacitor (30-pF). Due to the smaller capacitor size, the chip area is minimised.

- **The converter is self-supplied** from its power stage output to peripheral circuits.
- Thus, a self-powered, self-regulated, self-supplied proposed charge pump has been achieved through post-layout simulation.
- Moreover, the converter **can produce reconfigurable SISO and reconfigurable SIDO** conversions in the same design.
- This converter displays **high power efficiency** up to 90.43% with *Wo/F* and 80.23 with *W/F* configurations.
- The **power density** of 0.653 mW/mm^2 and comparable to state-of-the-art.
- Converter displays **a stable load regulation** over varying loads and Monte Carlo post-layout simulations.
- Converter displays **VCRs** close enough to the ideal target value- the output voltage equal to input voltage relative to conversion gain. However, there is a trade-off between the output voltage and current depending on the load.
- Lastly, this converter has a **flexible design** and is adjustable to design changes in gain configuration, such as adding more step-up/down configurations for both rational and integer DC gains. For such changes, only MUX in GCU needs to transform with the expense of slight chip area expansion.

CHAPTER 4: FULL SWITCHED-CAPACITOR-BASED POWER MANAGEMENT SYSTEM

4.1. Motivation

Nowadays, medical devices are integrated into various body-worn applications that can sense, diagnose, and treat chronically ill patients. These devices will be integrated into wearable devices such as soft contact lenses. In my research group, Microelectronic Lab (meLAB), the team develops wearable devices to assist people's day-to-day lives. Such devices can be divided into several building blocks, which require different operational voltages. The vision of such low power wearable biomedical devices requires energy harvesting assisted power sources that extract energy either from the surroundings or from the body.

As discussed in Chapter-1, the photovoltaic (*PV*) cell that uses solar energy is the best candidate due to its smaller size and harvestable power density, which is defined by output power over a solar cell area. However, all energy harvesters, by their nature, are location and environmental dependent. Similarly, the open-circuit voltage and short circuit current vary with incoming solar irradiation on the available *PV* cell area. As a result, the overall output harvested power also varies. To optimise the variability at the input side, several methods of maximum power point tracking (MPPT) had been reported in [221, 223, 227-229] to maximise the energy extraction from *PV* cells at all lighting conditions. However, *PV* cell usually provides ultra-low voltages; for instance, in [26, 194] CMOS structure single junction diode provide 0.3-0.4 V. Therefore it is not good enough to directly supply towards the loads as they demand higher operating voltages- at least 0.7 V as discussed in Chapter 1. Therefore, self-powered devices require a step-up converter to satisfy the low input voltages. Moreover, the converter should provide a wide range of regulated dynamic stable supply output voltages to loads of multiple electronic modules comprised of various operational voltages.

This chapter's focus is to develop a power management system comprised of two different DC-DC converters that serve different purposes. First, design of the cold-start converter or start-up charge pump (SCP), which operate in ultra-low voltage from an energy harvester source. Next, the main charge pump (MCP) produces the dual output capability with various DC gains configurations to accommodate multi-block electronics with different operating voltages. As a result, the power management system (PMS) containing both cold-start and reconfigurable converter is formed. The proposed PMS is ideal for energy-constrained devices and applications requiring wider operational voltages. Most importantly, the converter is self-powered as it is designed to operate with the solar energy harvester. Furthermore, the proposed charge pumps are designed to produce high power in the minimal area, which results in smaller chip sizes and lower costs.

In this section, the proposed SCP and the MCP are separately designed for a different purpose are interfaced together to observe whether these two can operate as intended. The connections are made, as shown in Fig. 4.1. From a single power source input V_{PV}, start-up charge pump output (PV_{OUTPUT}) is fed into the main charge pump input (V_{in}). It produces two simultaneous outputs (*Out1 and Out2*) or single-output (*Out1* or *Out2*) depending on the main charge pump's configuration from 2 bits gain configuration (A_{small} and B_{small}) discussed before. There is no storage unit between start-up and main charge pumps to test the main charge pump's stability at high ripple input conditions.

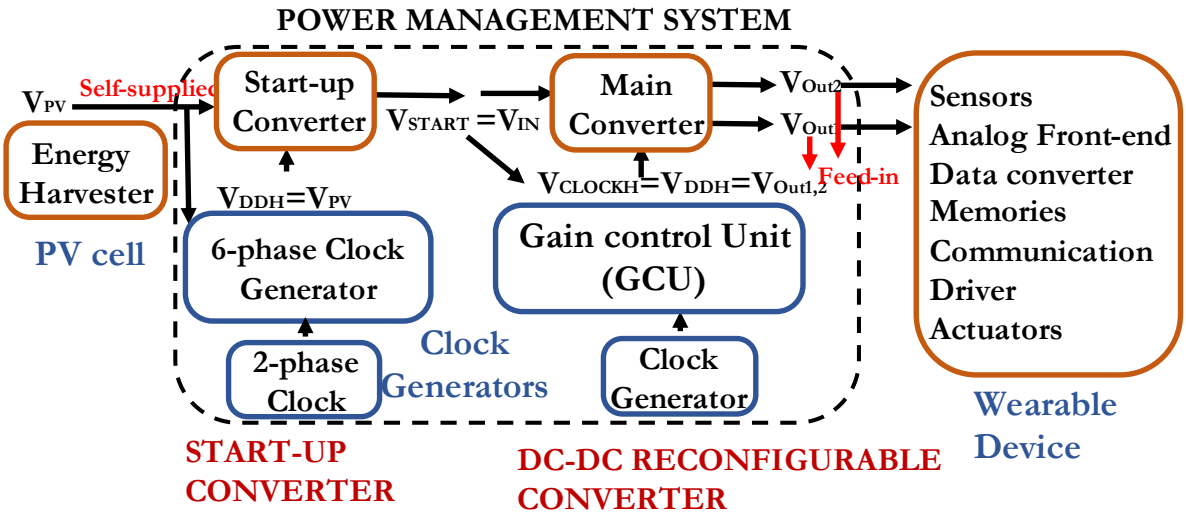


Figure 4- 1. The system architecture of the overall system; interaction of start-up and main charge pumps.

The conventional on-chip switched-capacitor (S.C.) converters are usually reconfigurable single-input single-output (SISO) designs. However, wearable devices comprise many electronic modules that operate in different voltages. If an SISO converter is implemented for such applications, high power loss can occur due to an imbalance of power rating at loads across the additional drop-down circuit. The best way to compromise is to provide a multi-output converter, weighing numerous advantages over SISO [203]. The converters in Chapter 2 [156, 168] and Chapter 3 introduce a novel reconfigurable DC-DC power converter. The proposed MCP can achieve different gain modes, which simultaneously produces two different voltage conversion ratios, VCRs, and a single reconfigurable output. It eliminates the existing fixed conversion problem at dual output designs and allows us to self-regulate internally. Second, to integrate with solar energy harvester, which usually produces ultra-low power output, energy-efficient start-up charge pump designs are examined and implemented. In search for a suitable start-up charge pump for this system, various start-up charge pump converters were explored and presented in Appendix-3. The challenges, such as reversion loss and parasitic loss, which contribute directly towards efficiency, were addressed. Finally, two types are converters are interfaced together and collectively established as the power management system (PMS).

Therefore, the proposed PMS overview in this work comprises a start-up charge pump to bridge the varying low output nature of the *PV* cell, followed by a self-sustain, reconfigurable main charge pump. The former is to provide high efficiency and stable outputs in line regulation, and the latter is to address a high efficiency and robustness for load regulation. The proposed converters are ideal for energy-constrained devices and self-sustain applications requiring wider operational voltages.

4.2. Description of Design

Ultra-low-power applications such as wearable biomedical devices need novel energy harvesting techniques that extract energy either from the surroundings or from the body. However, the power extracted from these sources is location and time-dependent. Thus, self-powered devices need efficient and reconfigurable power converters to provide a wide range of dynamic output voltages.

First, the various start-up charge pump designs have been presented in Appendix-3 to integrate with the energy harvester. Proposed Start-up designs have the objectives of (1) being able to operate in ultra-low voltage input the *PV* cell energy harvester can produce, (2) hence stable output performance in line regulation is prioritised. (3) Improve the efficiency by minimising the losses across the converter operation via CSC and CTC. (4) Moreover, I have investigated further optimisation of clock disabler energy-efficient design improvement from original literature to minimise the overall power consumption of proposed PMS, which work together with start-up and main converter.

Second, my work on main converter designs- 4-phase topology in Chapter-2 and 2-phase topology in Chapter-3. The improved 2-phase topology converter presented in Chapter-3 is selected as the final main charge pump for PMS. A novel switched-capacitor (inductor-less) DC-DC converter produces reconfigurable step-up dual outputs or a single output using 2-phase logic switch-mode regulation. With an input voltage of 1-V, the designed converter achieves 2-V in low-power mode, two simultaneous 2-V in double-boost gain mode, 3-V and 2-V in super-boost gain and 3.5-V high-conversion mode.

The proposed converter has been designed and fabricated using standard TSMC 0.18 μm CMOS technology. In this chapter, PMS will discuss a combined start-up charge pump and novel 2-phase topology converter as the main charge pump without using the storage in between intended in Chapter-1.

4.3. Implementation of Power management System (PMS)

The integrated photo-voltaic cell (*PV*) is chosen to convert ambient light energy into electrical energy [163]. Due to low output and varying output nature from the *PV* cells, the proposed inductor-less switched-capacitor approach DC-DC ultra-low-powered converter or power management unit (PMS) comprises with- start-up charge pump; high efficiency and stable performance in line regulation, and main charge pump; design to self-sustain, reconfigurable, highly efficient, and robust to load regulation.

Because of the low DC output and varying nature of the P.V. cell's output, typically, the harvested voltage level should be boosted using a start-up charge pump (SCP) [37, 119] which can operate in low-level input. One of the primary factors of efficiency loss in charge pump (CP) circuits is due to reversion loss [40, 215, 230, 231] triggered by the in-between transition of the two charge sharing clocks. Thus, proper design of the clock signals is of great importance for step-up CPs such as SCP. Switching loss by MHz-range pumping clocks is another factor that should be addressed in high-efficiency CP circuits. Previous work in [232] shows a 6-phase clock scheme to address the above efficiency-degrading factors for boosting a 1.8 V DC-level. In this proposed PMS, SCP is implemented with a mixture of standard and medium-threshold transistors to operate in varying low-voltage levels provided by the *PV* cell.

In the next step, the voltage level at the start-up's output needs to boost again to provide the required voltage level at the sensors and actuators' supply rails. Once the V_{START} is yielded at the start-up charge pump's output, the main charge pump uses it as an input (V_{IN}) without having a secondary storage source in between, such as a capacitor, to ensure the stable DC input. However, to minimise the area consumption and the line regulation of the proposed main charge pump is insensitive to voltage variation at the input side.

Even though there are high-efficiency CPs in the literature, most of them lack multiple reconfigurable outputs for multi-application devices. Previous work of the main charge pump (MCP) in [156] presents the reconfigurable CP with two different levels of simultaneous outputs Verilog-A programming controls its gain selection. In Chapter-4's recent MCP design, the CP's gain is configured by an analogue gain control unit (GCU).

The primary objective main converter is to (1) provide regulated voltage output from unregulated input from harvester converter by interleaving between symmetric network, (2) reconfigurable simultaneous outputs each with different voltage level and (3) provide a wide range of (VCR); which contribute the overall power efficiency. The presented work in Chapter-3 is the reconfigurable converter with two different simultaneous outputs. The energy conserves low power loading condition and high conversion mode, intended for the application that requires around 3-4 V DC voltage, are considered by employing the single reconfigurable output. The selection of gain modes VCRs is selected by the proposed gain control unit (GCU), designed by multiplexers and level-shifters. Moreover, the requirement of an additional power supply for the operation of GCU is eliminated, and self-supplied(feed-in) through the two outputs of the main converter is utilised.

4.4. Circuit Design

4.4.1. Power Management Unit (PMS)

The proposed inductor-less power management system (PMS) that harvests the power from a P.V. cell and generates the required supply voltages (V_{out1} and V_{out2}) for other blocks in the wearable system. As shown in Fig. 4.1, the PMS can be divided into (1) high-efficiency SCP, which operate in ultra-low voltage output yield from *PV* cell energy harvester. (2) The MCP reconfigurable DC-DC converter with different gain reconfigurability. The Unreliable and varying *PV* cell's output (V_{PV}) is first regulated and boosted into V_{START}. V_{PV} is used as the input of the SCP and power supply rail for the clock generators. V_{START} at the SCP output is used as an input to the MCP reconfigurable CP to provide different voltage conversion ratio (VCR) and regulate outputs at V_{out1} and V_{out2}. A Gain Control Unit (GCU) powered by the V_{START} is implemented for configuring the DC gain of the MCP. This proposed PMS is beneficial in a system with operating blocks with different concurrent operating voltages requirements due to dual-output capability. For a single-output CP, it will end up running in the maximum gain, and thus the high-power dissipation will occur across the low-voltage loads. Moreover, due to SCP implementation, the proposed PMS can operate in low-input voltages and integrate with energy harvesting sources. The proposed PMS, which contains both SCP and MCP, is beneficial for energy-constrained devices and applications requiring a wider range of operational voltages.

4.4.2. Start-up Charge Pump (SCP)

The circuit schematics and the timing diagrams of the proposed start-up charge pump are presented in Fig. 4.2. The basic 6-phase clock scheme is adopted from [232], while the proposed circuits in this work are designed to comply with the SCP's low-voltage requirements. Correspondingly, the circuit is designed with a combination of standard transistors and medium-threshold transistors. The switching transistors (M1-M3) sizing is designed based on a trade-off between the minimum conduction loss and the minimum switching loss and according to the target output load. A dynamic bulk biasing circuit is implemented for the PMOS devices to prevent latch-up.

Subsequently, three different sets of clock signals are used for driving the pumping capacitors (*CLK1* and *CLK2*), NMOS switches (*PQ1* and *PQ2*) and PMOS switches (*P1* and *P2*), all out of *PHI1* and *PHI2* clocks. To prevent reverse current from CP's output to its input while employing a charge recycling technique for reducing the switching loss. The *CLK1* and *CLK2* signals are being generated in a charge transfer clock generator (CTCG). This circuit is designed for recycling the stored energy at the parasitic bottom-layer capacitors of pumping capacitors to reduce the switching power loss. Moreover, the bottom plates of both capacitors are connected in parallel using the switch 'k1'. It is turned on during Δt when the two pumping capacitors remain idle and apply charge recycling to SCP.

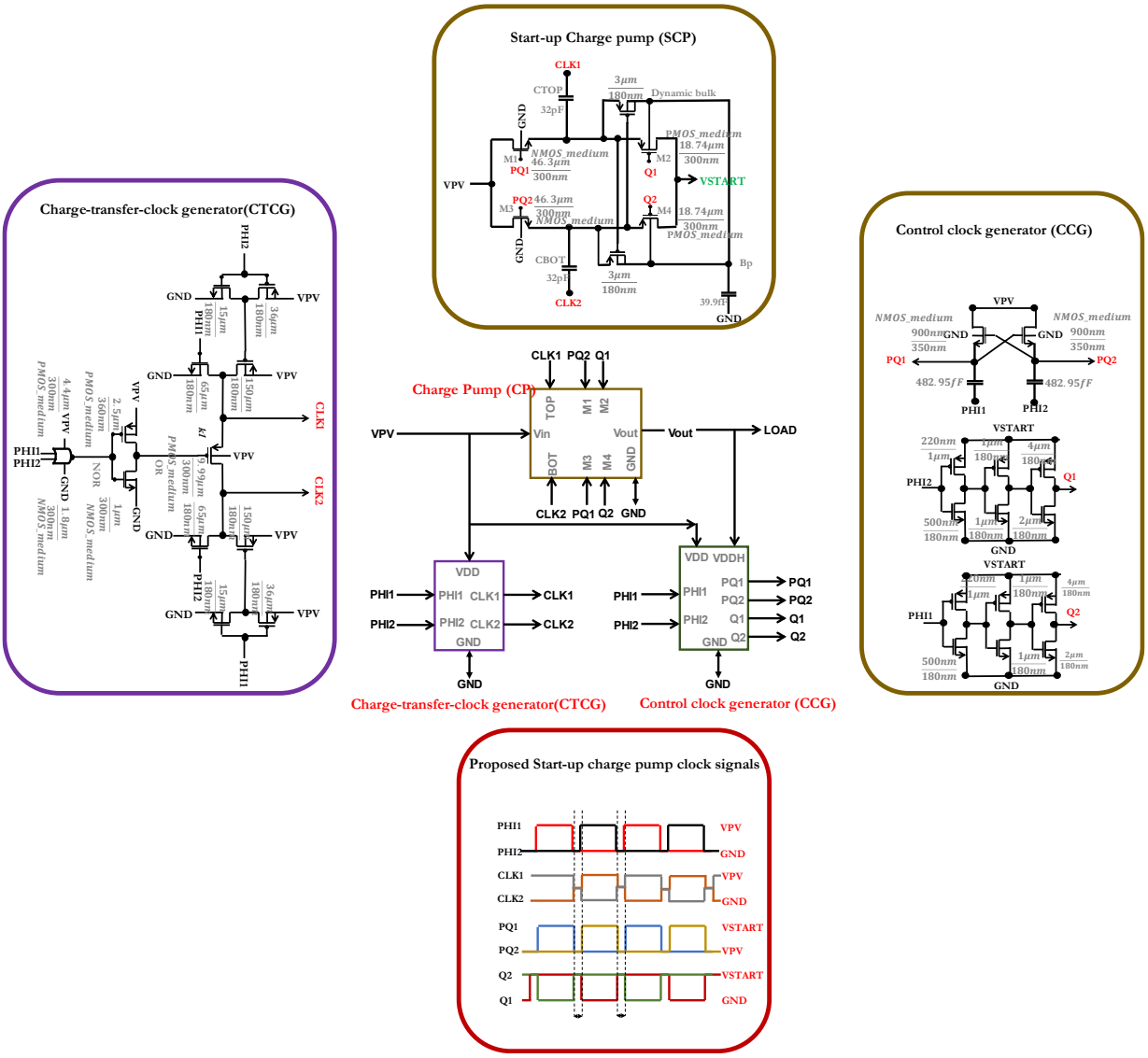


Figure 4- 2. Schematic diagram of start-up charge pump converter with proposed crossed-couple control clock diagram, charge sharing clock generator $CLK_{1,2}$ and charge transfer switches clock signals $PQ_{1,2}$ and $Q_{1,2}$.

4.4.3. Main Charge Pump (MCP)

Once the V_{START} is yielded at the start-up charge pump's output, the main charge pump uses it as an input (V_{IN}). A filter capacitor can be implemented between SCP and the MCP to ensure that MCP receives clean DC input. However, to compromise the chip area, the output of SCP is directly connected to MCP input in the layout. Line regulation of the MCP enables insensitive to voltage variation at the input side. The SCP is operating in approximately three times faster frequency (i.e., 8.8 MHz) than the MCP frequency (i.e., 3.3 MHz). These two frequencies were selected through the optimal results achieved from simulation.

The MCP is designed to provide regulated voltage output by using interleaving between symmetric networks. Simultaneous dual outputs and single outputs with a wide range of VCRs can be achieved through MCP. Moreover, CP is self-powered by a *PV* energy harvester, and its peripheral circuits are self-supplied by the outputs (V_{out1}, V_{out2}) of the MCP. The selection of gain modes VCRs is selected by the proposed gain control unit (GCU) in Fig. 4.3. It is designed by multiplexers and level-shifters. Moreover, the requirement of an additional power supply for the operation of GCU is eliminated and self-supplied (feed-in) through CP outputs.

The four different voltage and power modes are achieved by integrating four capacitors (C1-C4) connections through the power stage network depicted in Fig.6(a). These are (1) Low-power (*LP*) mode, (2) Double-boost (*DB*) mode, (3) Super Boost (*SB*) mode and (4) High-conversion (*HC*) modes. In comparison with MCP in Chapter III, low-powered (L.P.) single-output configurations and high-conversion (H.C.) modes are added in this work to achieve flexible CP. For applications that may require energy constrain conditions such as operation idle time, *LP* mode may find beneficial as step-up *LP* mode (×2) consume low power of 4-μW (*feed-in*) and 2-μW(*stand-alone*) at no load.

For regulation purposes, two symmetric networks in each side of output are implemented and operate in a 180° phase-shift interleaving regulation scheme. However, the *HC* mode uses Dickson's ladder topology in a single power stage network and thus interleaving scheme did not apply to this model. The main challenge is to make sure switches that are not involved in chosen gain modes require to operate at the cut-off region to avoid creating the unexpected leakage path within the network. It involves interface with GCU to provides the correct clock signal ($P_{1,2}$, V_{DD}) at adequate gate voltage amplitude ($P_{1,2}'$, $P_{1,2}''$, $P_{1,2}'''$, V_{DD}', V_{DD}'', V_{DD}''') to each of the PMOS and NMOS transistors within the network. The thick gate PMOS transistors *O1-O4* are used for output switches. The dynamic bulk biasing switches are implemented in input PMOS switches (M_{p0}-M_{p3}) and the network bridge switches (t_1, t_2) to guarantee the strong bulk connection between the voltage swing top plate, the capacitor and input voltage during interleaving operation. Hence maximum charge sharing is enabled in the charging phase. The standard transistor with its highest potential at source and bulk terminal is tired together used for (M_{p4}-M_{p7}).

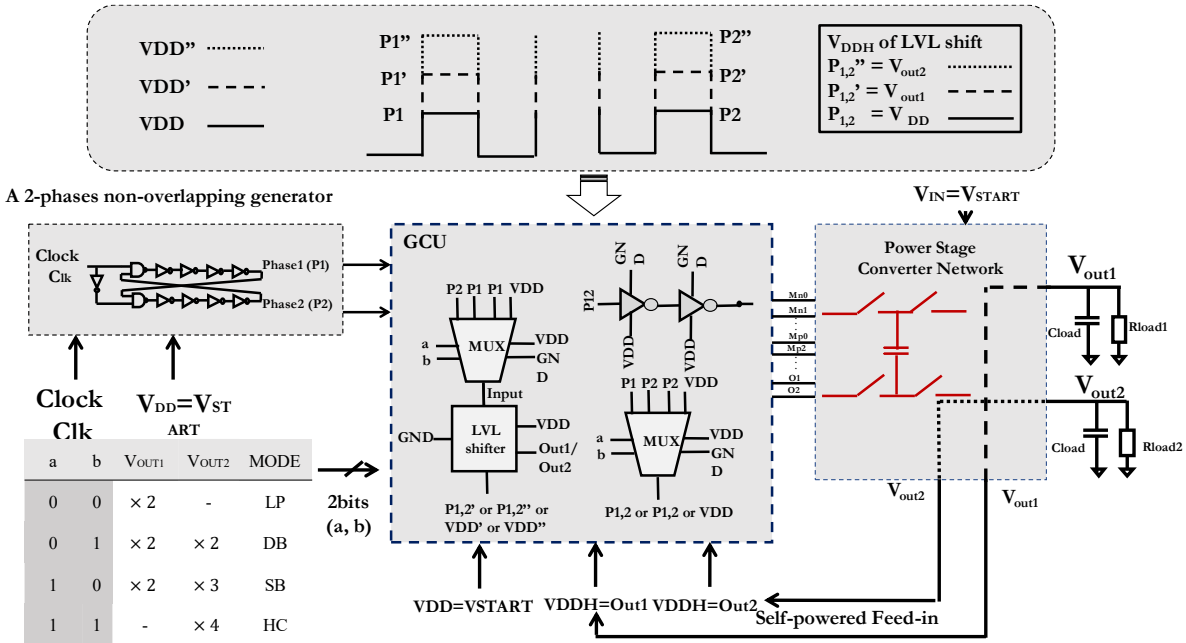


Figure 4- 3. System Architecture of the main charge pump DC-DC converter.

4.5. Simulation Set-up

A photo of the fabricated chip in TSMC 180 nm technology is illustrated in Fig. 4.4. The whole design occupies 1162 µm x 436 µm of silicon area, including the pads. To engage the better interface between two converters, the harvester charge pump has operated in approximately a three times faster frequency of 8.8 MHz and the main converter with 3.3 MHz operating frequency.

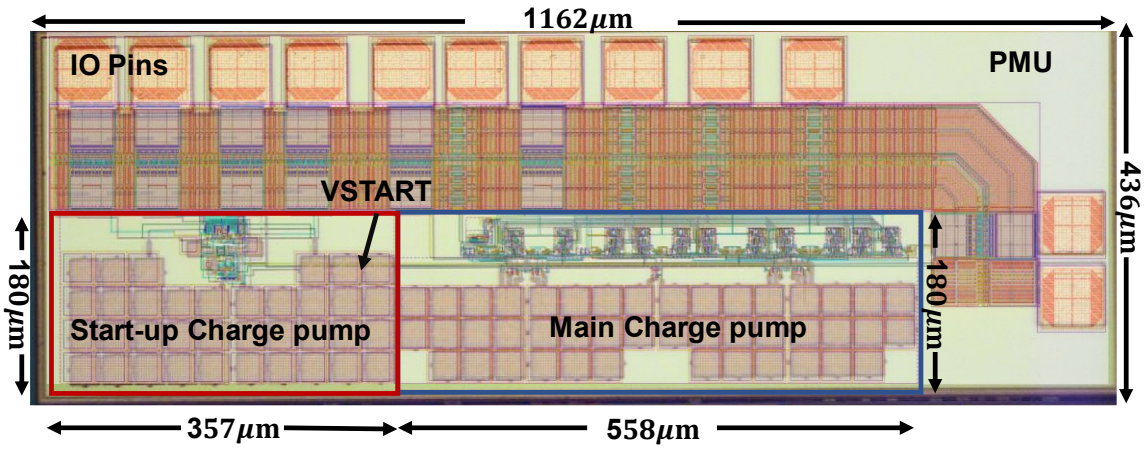


Figure 4- 4. Chip microphotographs include pins (with the back-annotated layout) of the proposed PMS.

The simulation set-up for the proposed PMS is as follow- The integrated MC in the proposed PMS uses the stand-alone configuration in Fig. 4.5, and feed-in configuration is used in Fig. 4.6. The difference is external Vdc is needed for stand-alone configuration to switch off power stage transistors that are not involved in the selected gain mode methodology. Instead, *Out1* and *Out2* of MCP are used for self-supplied feed-in mode. The internal V_{DD} rails such as V_{IN}, $V_{DDDIGITAL}$, $V_{DDCLOCK}$ and so on can be combined. However, the reason for separating them is to identify the power consumption of each node during the test. Similarly, the clock generator can be integrated, but to ensure fail-proof in later experiments, it is now supplied externally.

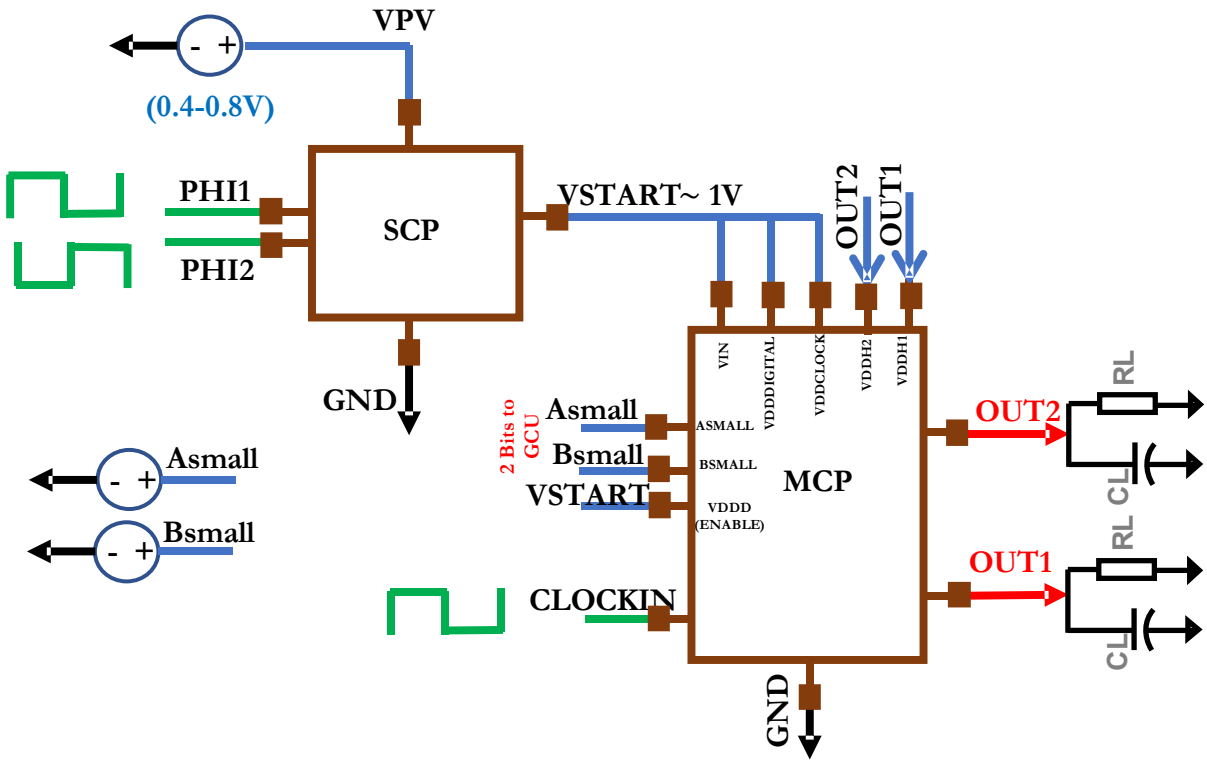


Figure 4- 5. Simulation Set-up for PMS with *without-feed-in* (*stand-alone*) MC.

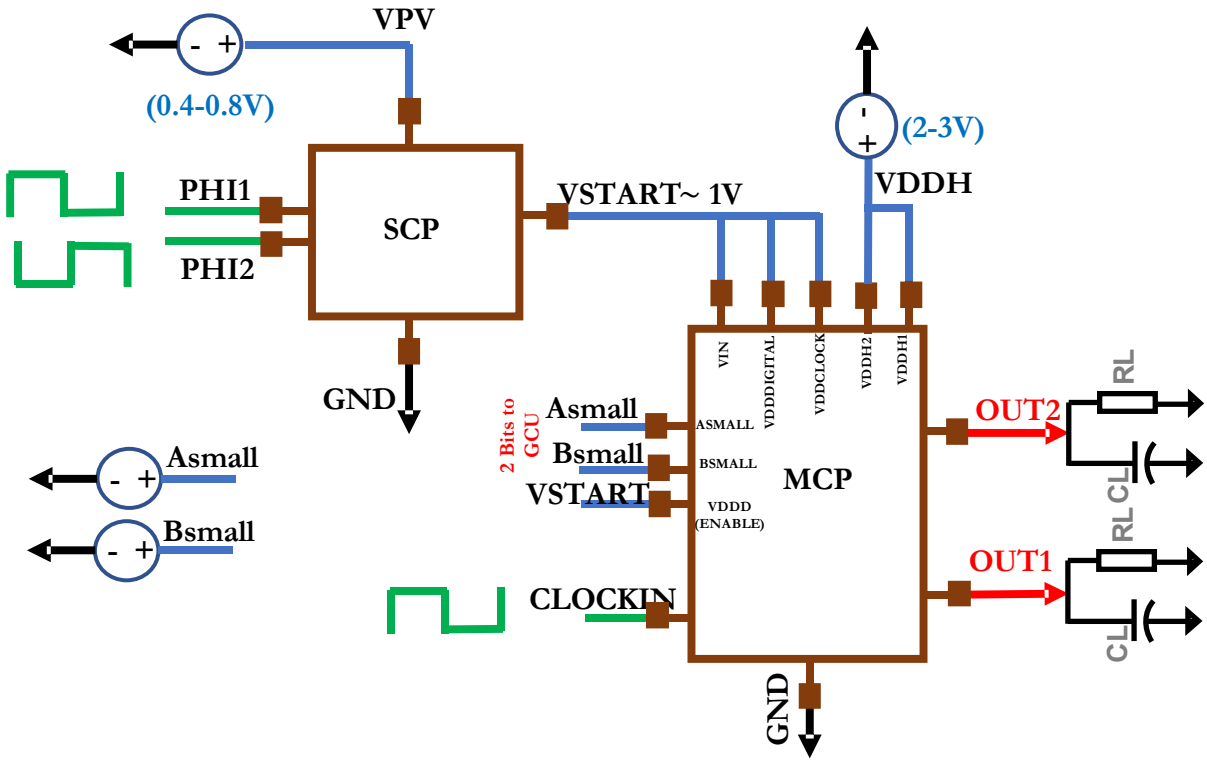


Figure 4- 6. Simulation Set-up for PMS with *with-feed-in* (System) MC.

4.6. Result and Discussion

4.6.1. Simulation of hypothetical Photo-Voltic (PV) cell.

The hypothetical tiny silicon Photo-Voltic (*PV*) cell with the use of the model proposed in [233] is simulated with the following parameters: series resistance (rs) of 0.001Ω, parallel resistance(rp) of 1 MΩ. The parameter used in AFORS-HET *PV* circuit model, a single cell (N_s) with diode ideality factor (n) of 1, short-circuit current density (jsc) of 11 mA/cm^2 and open-circuit voltage (V_{oc}) 0.6 V [234] is inserted in this simulation with a range of incoming solar irradiation 1000-600 W/m^2 at room temperatures.

The simulated I-V curve of the energy harvester *PV* cell is presented in Fig. 4-7. The variation in the generated current is due to a variation in the incoming solar irradiation. It results in the variation in the open circuit voltages, which intersect at a different point in the x-axis. However, this variation is slight. Regardless, when implementing the solar cell as an input source, the varying supply voltage is inevitable. Therefore, the desire power management system should be able to handle the input supply voltage variation. Fig. 4.8 demonstrated that the simulated solar cell has yields maximum output power of 62 mW, the harvested voltage of 450 mV and a current density of 14.4 mA/cm^2 at 35 ^{o}C. Similarly at 25^{o}C simulated *PV* model has achieved 0.54 mW, 0.528 V and 11 mA/cm^2 respectively. Similarly, other *PV* cell model example for wearable IoT applications, fabricated on the flexible substrate is demonstrated in [235].

The temperature related to the open circuit voltage wasn't mentioned in [233, 234]. However, it was derived in [236]. The *Voc* is temperature-dependent and has the relationship with Boltzman constant (k_B), elementary charge (e), Temperature (T), the concentration of ionised acceptor impurities (p_0), the excess carrier density (Δn) and laws of mass action (ni^2) which is the multiplication of electron (n) and hole (p) were derived in [236]-

$$V_{OC}(T) = \frac{k_B T}{e}.\, ln\left[(p_0 + \Delta n).\, \Delta n / n_i^2\right] \tag{4.1}$$

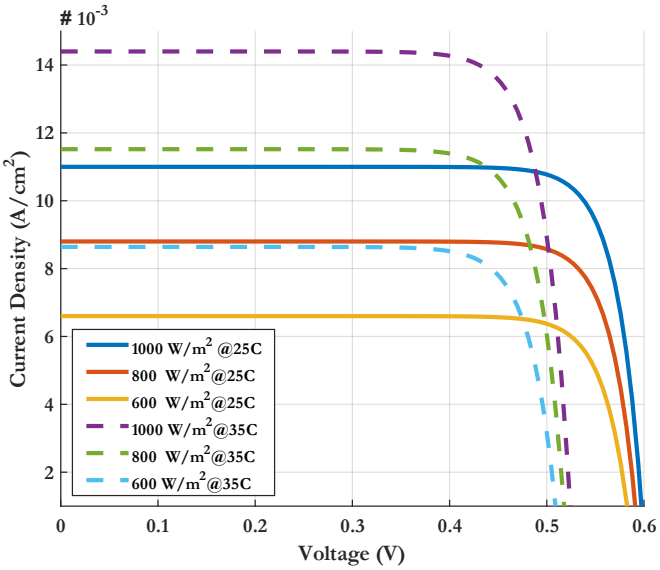


Figure 4- 7. I-V characteristic of the *PV* cell representing the current density and the output voltage.

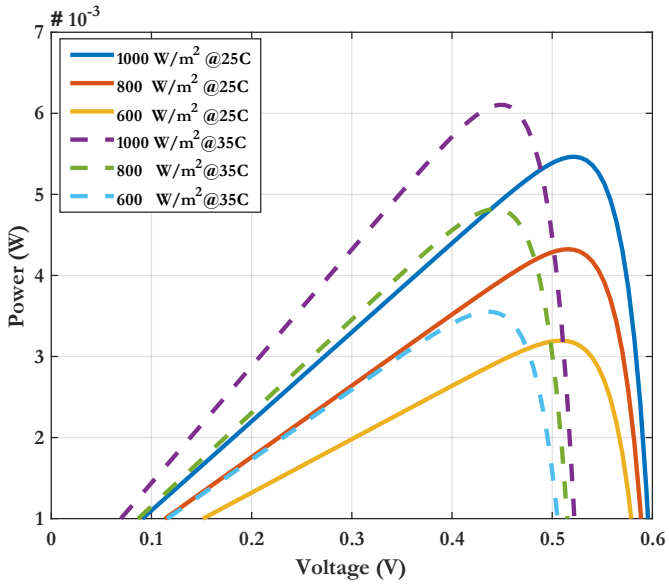


Figure 4- 8. Output Power over the output voltage of the simulated *PV* cell .

4.6.2. Result and discussion of Start-up charge pump SCP.

As demonstrated in Fig. 4.9, two non-overlapping control clocks *Phi*$_1$ and *Phi*$_2$, are modified into two-step charge sharing clock signals *CLK*$_1$ and *CLK*$_2$. It is done through the tristate driver CTCG to ensure that energy drawn from the power source is reduced as presented in [124] and charge recycling is accessible during the dead-time Δt. As expected from Fig. 4.9, the post layout three clock pairs (*CLK*$_1$, *CLK*$_2$), (*PQ*$_1$, *PQ*$_2$) and (*Q*$_1$, *Q*$_2$) have achieved the idle time Δt in line with each other and prevent potential reverse charging.

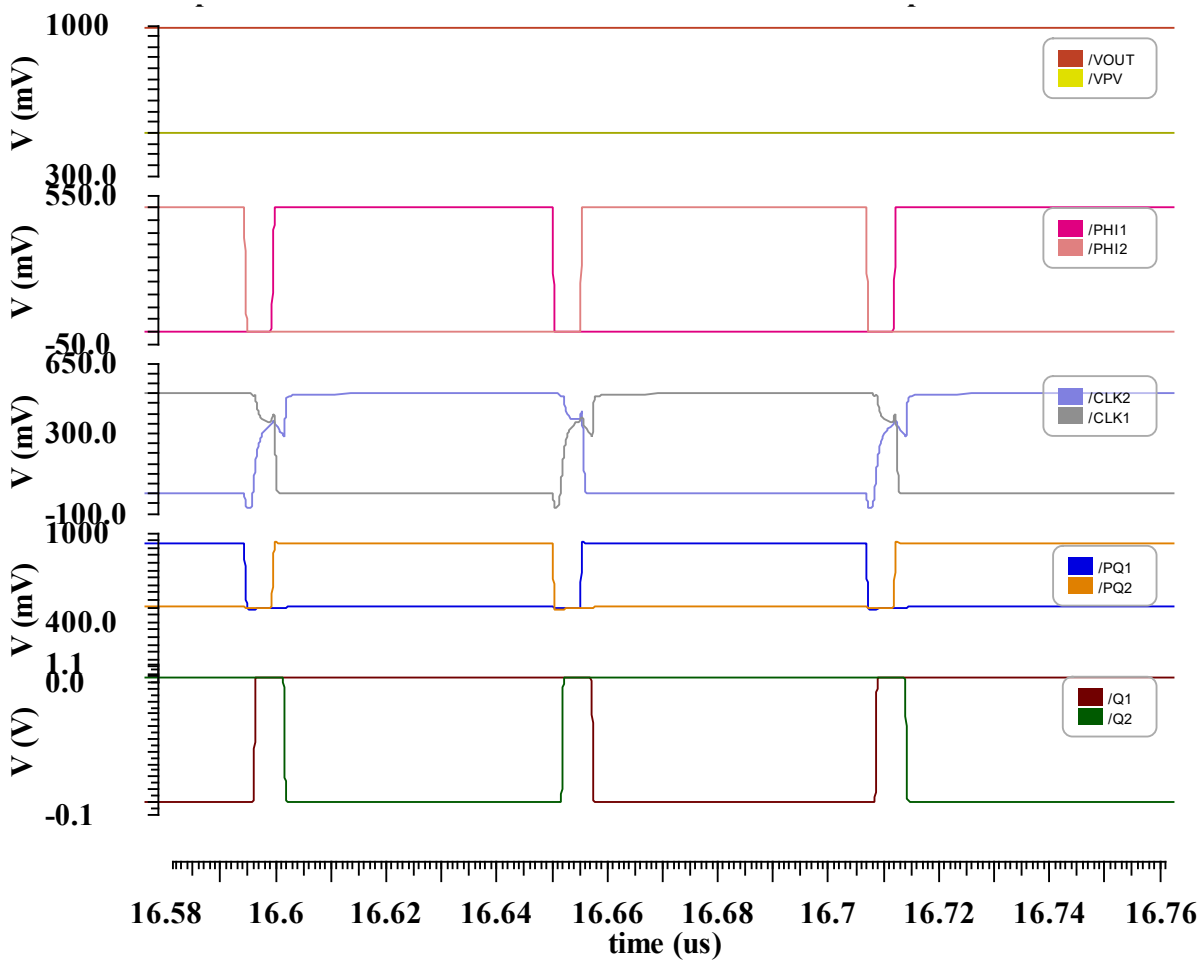
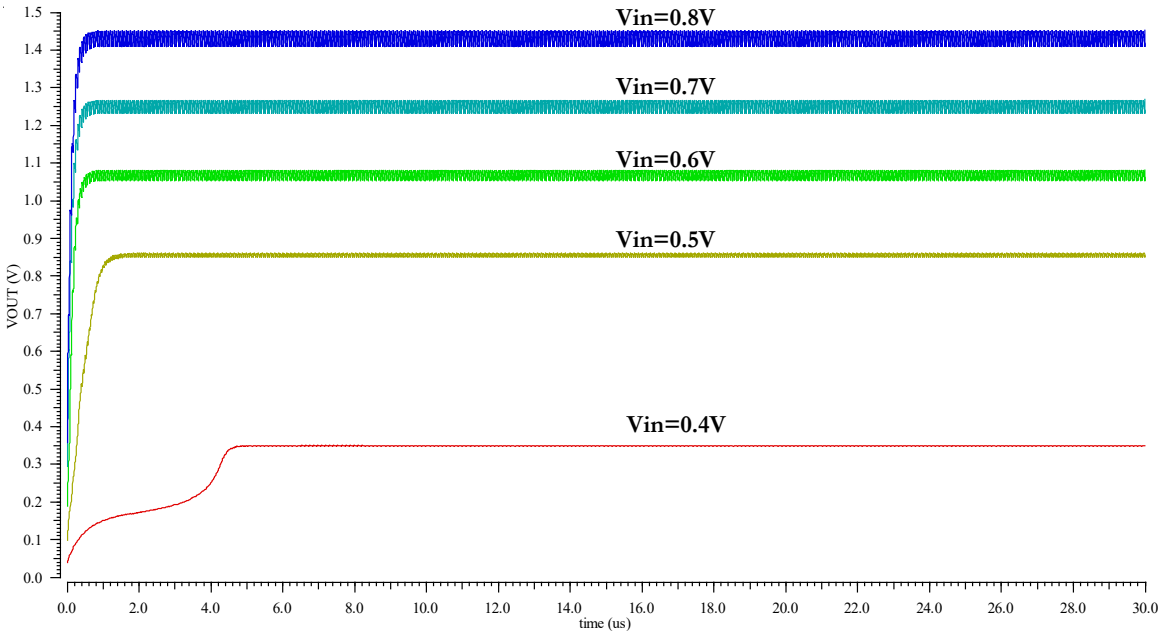


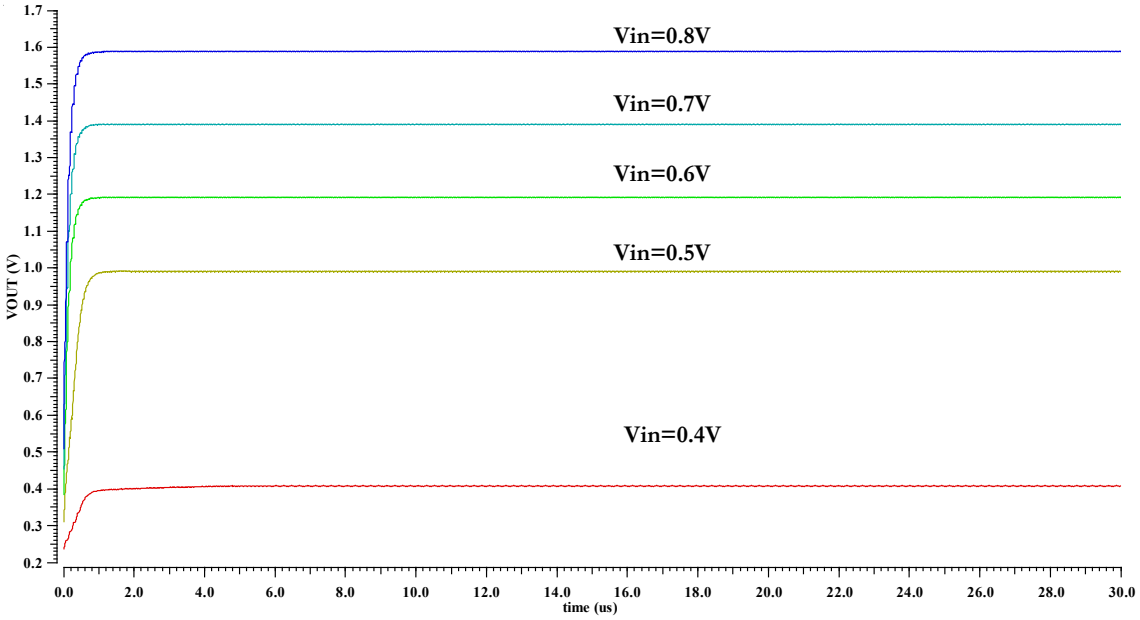
Figure 4- 9. Post layout simulated clock control signals for the proposed start-up charge pump.

The line regulation of the converter is demonstrated in Fig. 4.10 (a-b). It is tested with the fixed load to observe the change of output voltage according to the change of input voltage parametric sweep from 0.4-0.8 V to imitate the solar cell open-circuit voltages in different lighting conditions[25, 237]. In generating the desire 1-V required by the main charge pump, the proposed charge pump's line regulation has achieved up to 1.45 V within the input voltage range sweep from 0.4-0.8 V.

Moreover, no-current load (with a high resistance load of 1 MΩ) in Fig. 4.10(b) is simulated to see how much VCR can provide. Apart from the 0.4 V input voltage, which is slightly below the implemented medium transistor threshold, the rest has achieved up to 1.586 V, approximately two times the gain. As observed from Fig. 4.10(a-b), the output ripple is lessened at the higher resistive load.



(a)



(b)

Figure 4- 10. This voltage-time graph represents line regulation of the design-4 converter. The output voltage V_{OUT} changes when the input *Vin* changes. (a) at 15 kΩ and 60 pF load and (b) 1 MΩ and 60-pF.

The start-up charge pumps output voltages over different input voltages from 0.3-0.8V at line regulation test are also depicted in Fig. 4.11. It is tested for a fixed load of 20-kΩ, because the main charge pump (MCP) is likely to consume about 23 µW power at the no-load condition and 70 µW power at a maximum of 16-µA current load. Desire 1-V as input voltage-level to the main charge pump, the assumption has been made that the 70-µA sourcing current is needed to deliver from SCP. Not that the output voltage of SCP has achieved up to 1.469 V at 108 µW output power.

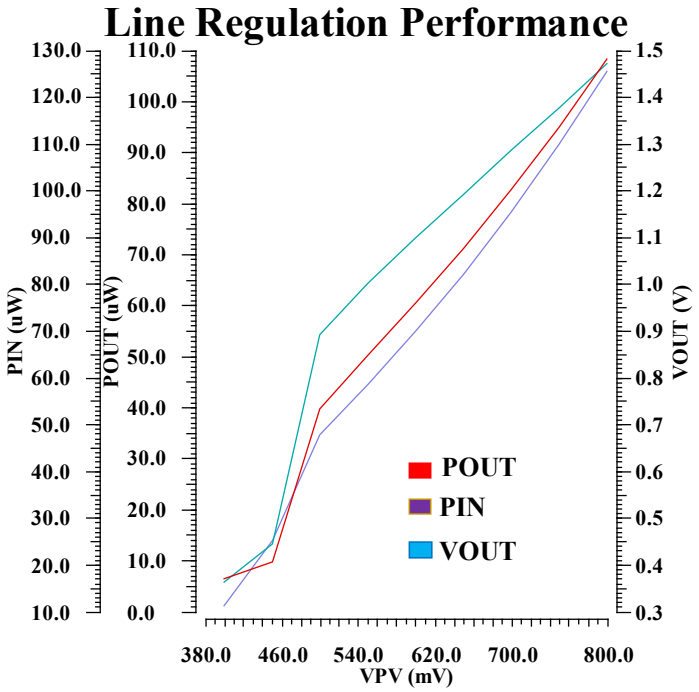


Figure 4- 11. The voltage-time graph represents the Line Regulation of the SCP when V_{PV} changes from 0.3-0.8 V at 20-kΩ. The other two axes represent the input power consumption P_{IN} (µW) and output power consumption P_{OUT}(µW).

Moreover, load regulation is tested with the resistive load changing from 10k-1M Ω at a fixed input voltage of 0.6 V. As depicted in Fig. 4.12, the output voltage has achieved 1-1.19 V and provide the relatively stable output. It demonstrates correct gain conversion capability at all load changes.

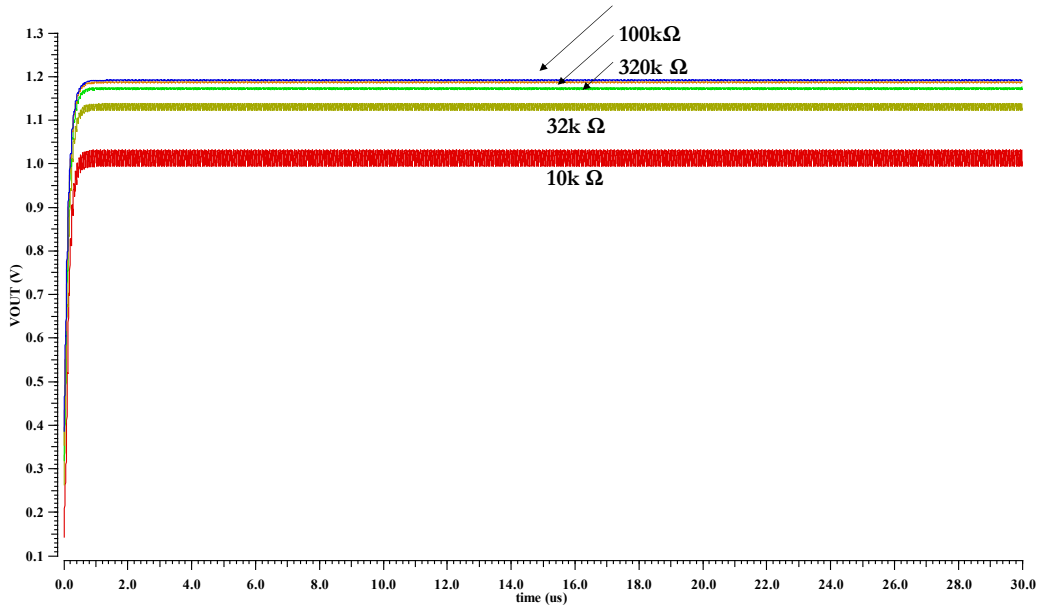


Figure 4- 12. Output voltage Load regulation ranging from 10 kΩ to 1 MΩ at an input voltage of 0.6 V.

Moreover, the load regulation is also tested with the range of resistive load ranging from 0-100 kΩ at a fixed input voltage of 0.6-V in Fig. 4.13. The output voltage has achieved from 1-1.18 V and provide relatively stable output and demonstrated correct gain conversion as the desire at all load changes. The

power consumption across the CP at 1-M Ω load is recorded 13.5 µW. Across the varying loads, the power consumption is noted as 126 µW and provide the output power of up to 105 µW.

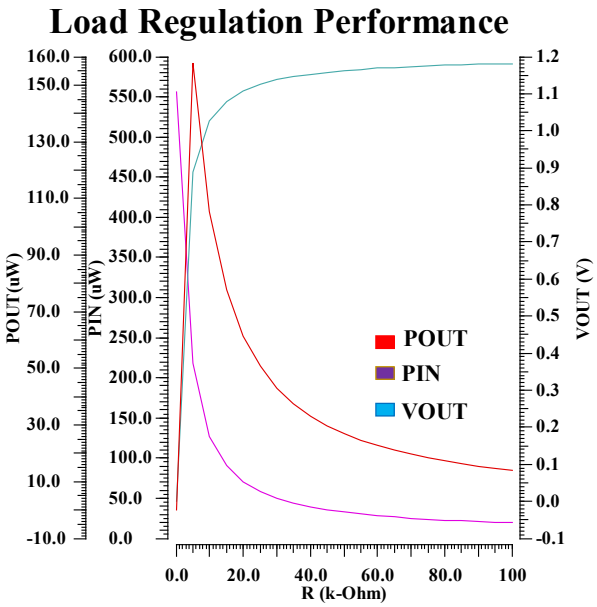


Figure 4- 13. The voltage-time graph represents the load regulation performance when the load resistor varies to 100-kΩ. The other two axes represent the input power consumption P_{IN} (µW) and output power consumption P_{OUT} (µW).

Furthermore, The post layout simulated efficiencies of both line regulation and load regulation is depicted in Fig. 4.14 (a-b). The maximum power efficiency of 86.2% is recorded for both various input voltages and different loads, respectively.

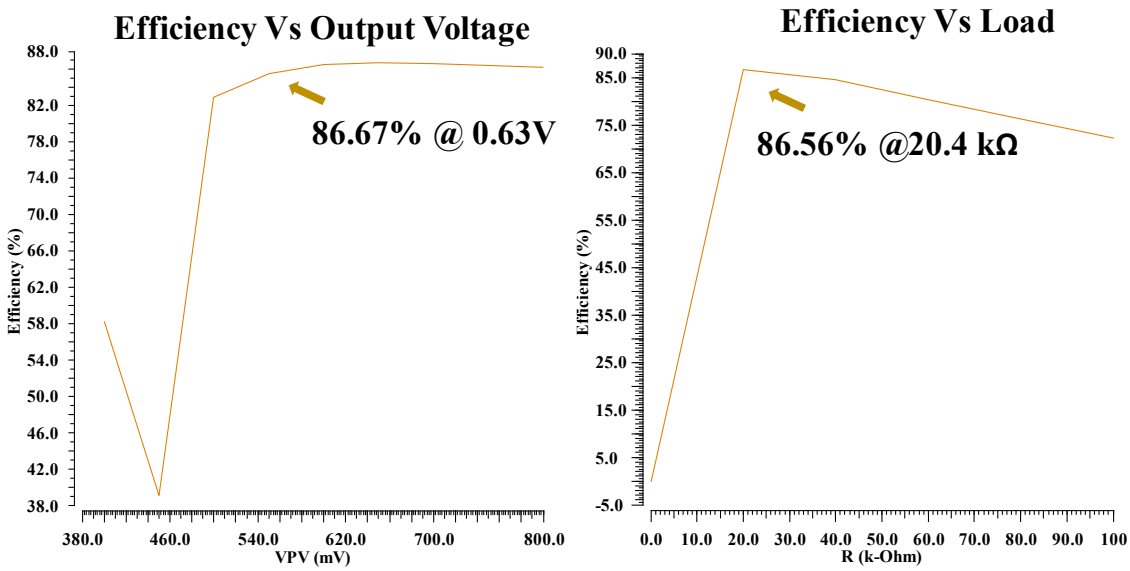


Figure 4- 14. Efficiency performance over (a) varying Input voltages and (d) Load changes.

4.6.3. Result and discussion of Main charge pump (PMS).

The design and discussion of SISO and SIDO design implemented as the main charge pump has been presented in detail in Chapter-3.

4.6.4. Result and discussion of Proposed PMS.

A. The comparison of schematic and post-layout simulation

Fig. 4.15 demonstrates the output voltages of both SCP and MCP in the proposed PMS, based on post-layout simulation. It shows the transients if a 0.5 V input voltage is fed to the SCP, and MCP is configured in *DB* mode. It has been tested with a small 5-pF capacitor at the load. The results in the output voltage ripple as low as 16 mV, thanks to the internal self-regulation scheme. Moreover, the MCP demonstrated that it could withstand the high input ripple at the SCP output. This high voltage ripple is because there is no smoothing capacitor at SCP's output for saving the silicon area. As observed, the MCP has achieved 2.26 V (i.e., VCR =96%) in *DB* mode while SCP generates V_{START}=1.17 V at *PV* cell input of 0.6 V.

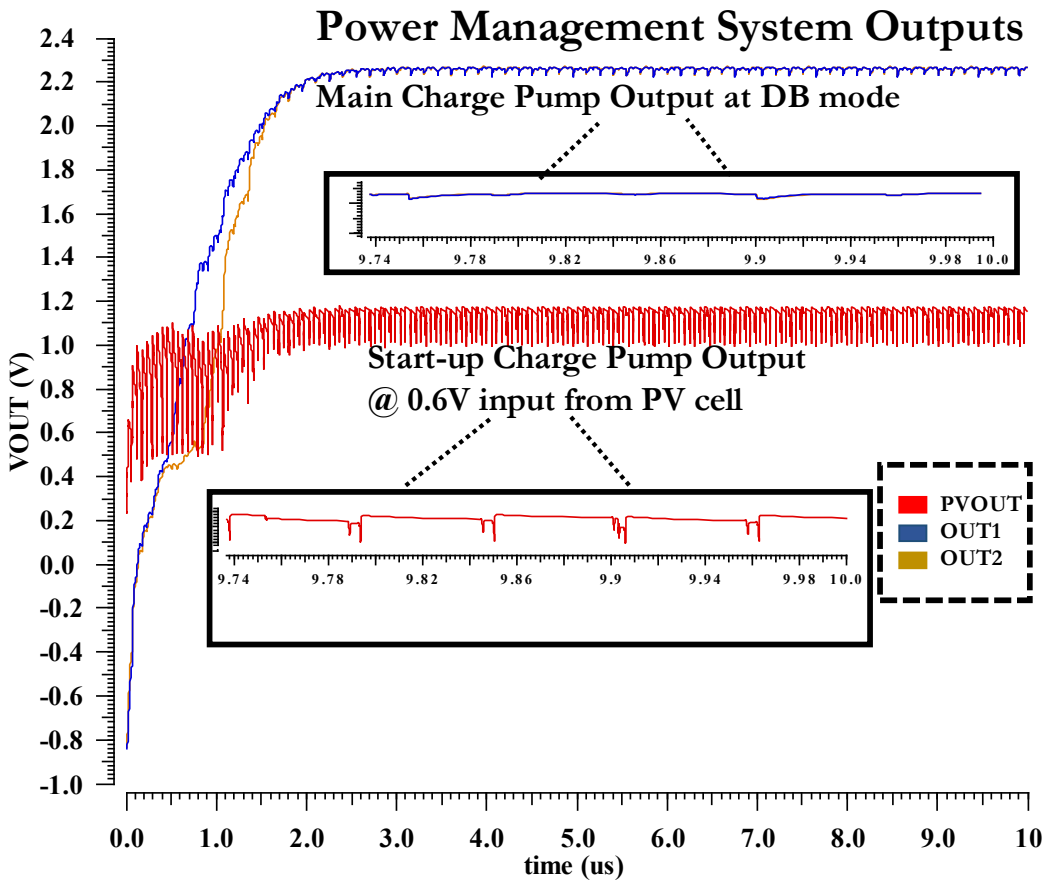


Figure 4- 15. The outputs of proposed power management system (a) in *DB.* mode at 0.5 V input.

The comparison of schematic simulation and post-layout simulations are compared in one graph to observe the variation. It is tested with both feed-in MCP (V_{DDH} of GCU is supplied from the Out1 and Out2 of MCP) and without feed-in MCP (V_{DDH} of the GCU is supplied from external supplied) integrated inside the proposed PMS. As demonstrated in Fig. 4.16, post-layout suffers from a slight voltage drop and a slightly longer short time to reach the steady-state. Apart from this minor setback, the fabricated layout design has only a slight output variation.

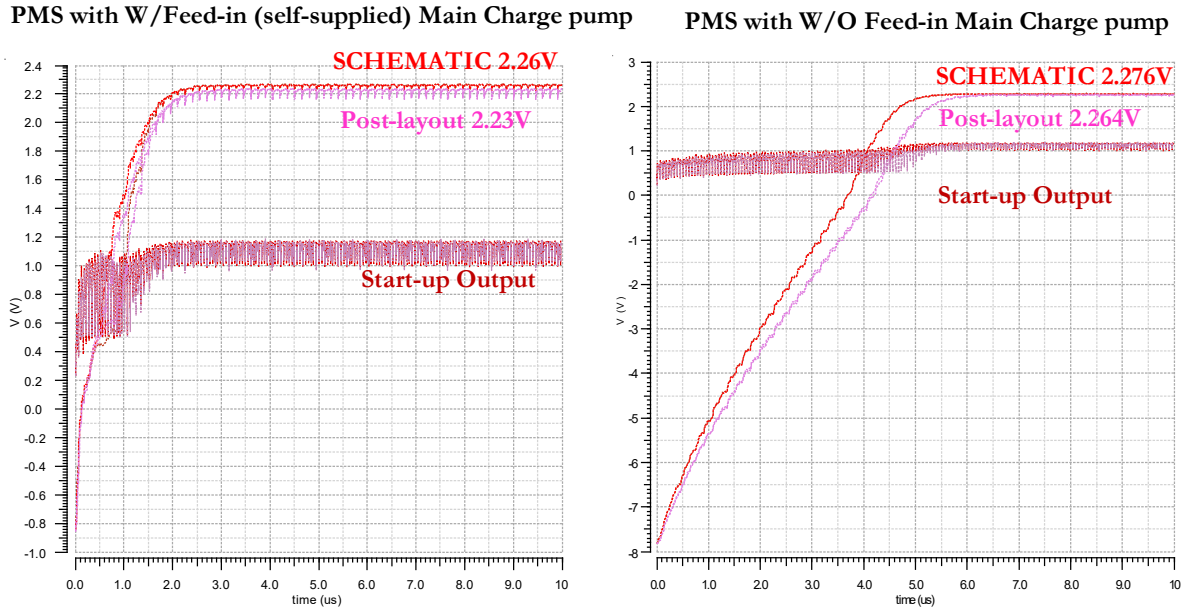


Figure 4- 16. Comparing schematic simulation and post-layout simulation outputs performance of proposed Power Management System in *DB* mode for both *W/feed-in* and *W/O feed-in* of MCP.

B. The result and discussion of PMS in Low-power (*LP*)mode

The comparison post-layout simulation of both *feed-in* and *W/O feed-in* for *LP* mode in PMS is presented in Fig. 4.17. By keeping the same input voltage of 0.6 V to PMS, various current load from 6-15 µA is tested. In *LP* mode, the output is only expected at the Out1, and thus Out2 can consider as the floating node. The comparison has suggested that, in every loading condition, the externally biased *W/O* feed-in has a longer transient time to reach the steady-state value. There is no DC output at *Out2* in *W/O* feed-in due to the switched-off transistors gate voltage are sufficiently applied from the external voltage source. Whilst in the feed-in system, some DC output in *Out2* can be observed. It is because bridge switches (*t1, t2*) between two power stage networks are not entirely off. These gates voltages are still in contact with *Vout1* and *Vout2* due to the reconfigurable network design. Therefore, this phenomenon can be considered one of the SISO configuration challenges in the SIDO power stage network. However, this is only an insignificant setback, and the feed-in system provides fast, transient response time with only a slight decrease in the final VCR DC voltage level compared with the *W/O* feed-in design. Note that the *feed-in* (self-supplied) system is the final goal that I am trying to achieve.

The total power consumption of PMS in *feed-in* at *LP* mode varies from 2.327 µW (@0.6-V input, 1-µA load) to 49.29 µW (@0.6-V input, 1-µA load). Achieved DC output voltage has the highest VCR in the lowest load (1-µA) and produce 2.327-V (@0.6-V input to SCP) and gathered lowest VCR of 2.09-V (@0.6-V input) at the highest load in simulation (16-µA). The efficiency has achieved up to 68.01% (@0.6 V input, 16 µA load) in the feed-in system and 73% (@0.6 V input, 16-µA load) in *W/O* feed-in system.

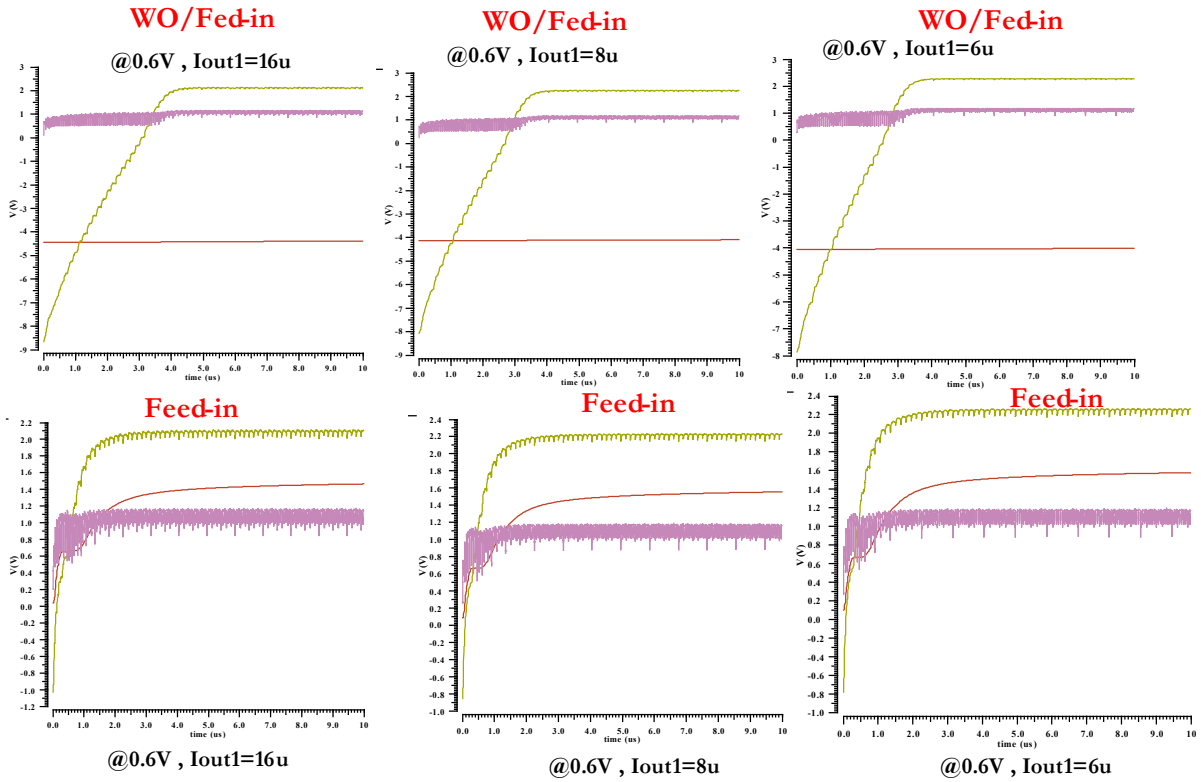


Figure 4- 17. Load Regulation of PMS in Low-Power (*LP*) mode with *with-feed-in* and *W/feed-in* systems.

Fig. 4.18 shows line regulation of PMS in *LP* mode feed-in system. It is tested in 16-µA current load with varying input from 0.5-0.8 V. The result has shown that converter is functional as expected, when the inputs are 0.8 V and 0.6 V. However, at 0.5 V input, the SCP output (V_{START}) only produce around 0.8 V. Hence, MCP cannot operate and there is no meaningful output at the Out1. It is further investigated in the next simulation.

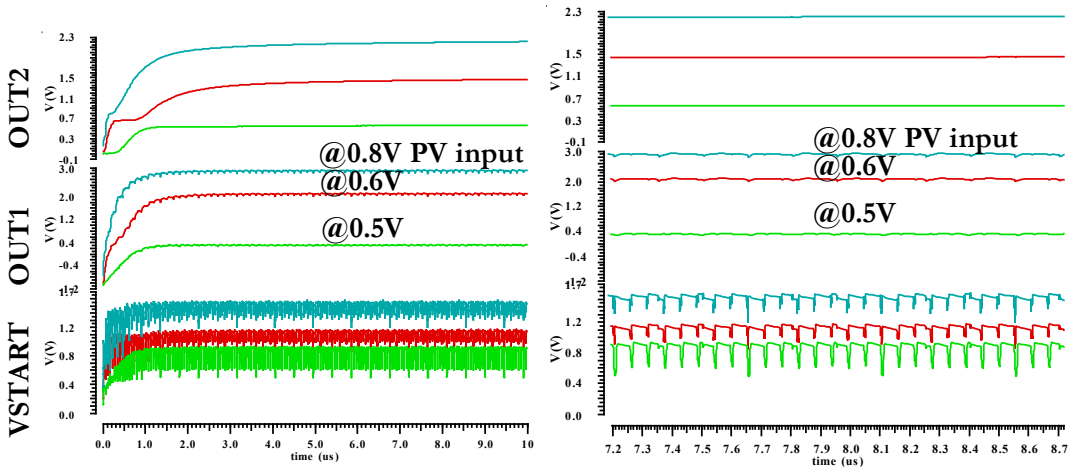


Figure 4- 18. (a) Line regulation of PMS in Low-Power (*LP*) with a *feed-in* system and (b) zoom-in view.

The results in Fig. 4.19 illustrates both line and load regulation of PMS in the *LP* mode feed-in system. According to the results of further investigation in Fig. 4.18, although Out1 cannot reach the desired output at 0.5-V input at 16-µA current load, at the lower current load of 2-µA, since V_{START} generate around 0.98 V and MCP is now functional. As seen in the zoom-in view of Fig. 4.19, the PMS has achieved the intended DC-outputs with high VCR across varying inputs and outputs and produce 16-mV low ripple outputs without needing a large filter capacitor. Low ripple is due to the interleaving regulation scheme of the proposed MCP.

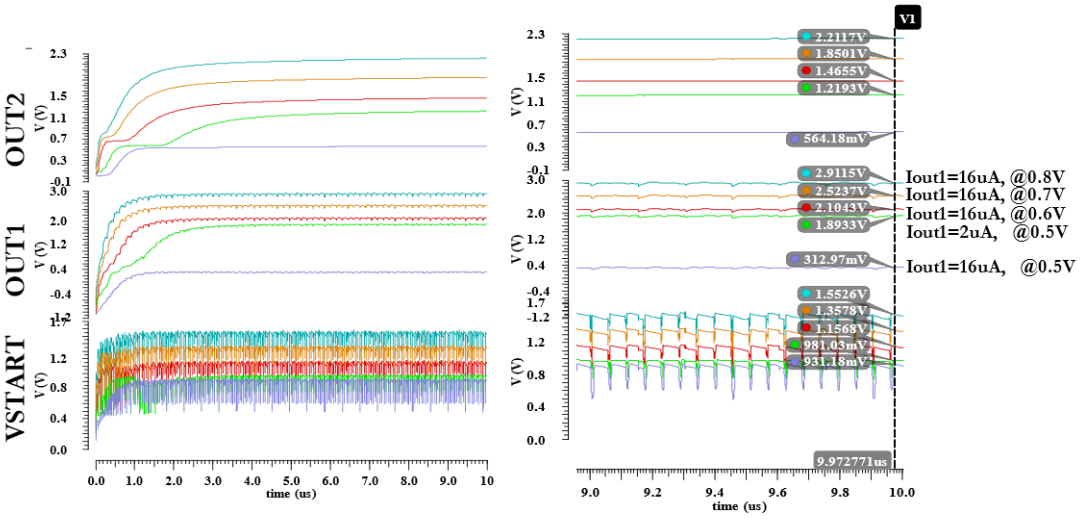
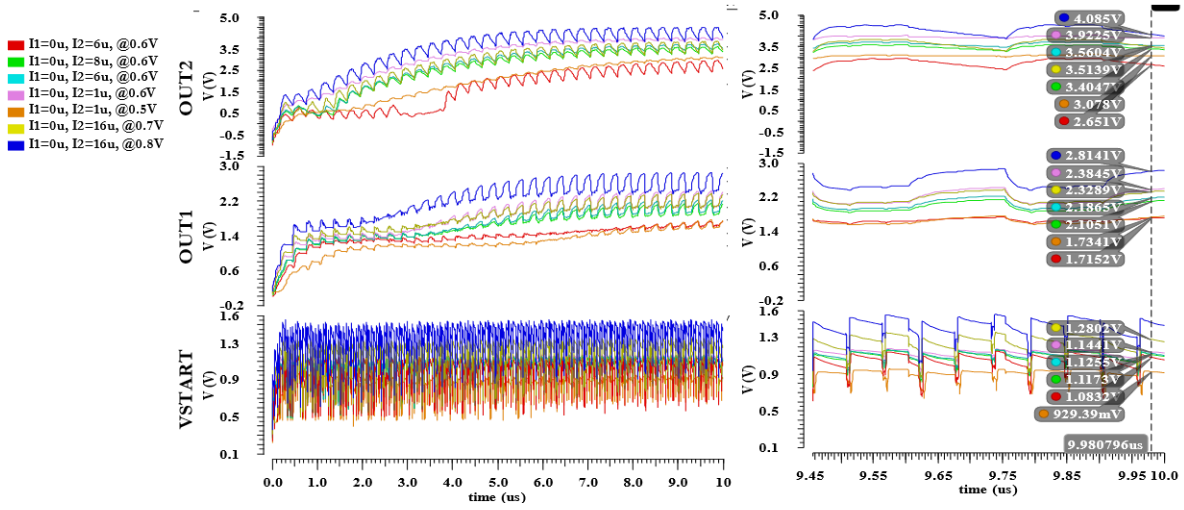


Figure 4- 19. Load and line regulation of PMS in Low-Power (*LP*) mode with a feed-in system and (b) zoom-in view.

C. The result and discussion of PMS in High Conversion (*HC*) mode

Similarly, post-layout simulation of PMS in *HC* mode with the feed-in system is investigated, as shown in Fig. 4.20. Load regulation is tested by keeping the same input voltage of 0.6V to the proposed PMS, and the current load varies from 1-µA to 16-µA. At 0.6V input, PMS has achieved highest VCR DC output of 3.946-V (*Pout*=3.942 µW and *Pin*=49.3162 µW, @ 1-µA load) and lowest DC output of 2.694-V (*Pout*=43.11 µW and *Pin*=107.27 µW, @ 16-µA load). In the *HC* mode, the highest efficiency has achieved up to 40.188%.

In *HC* mode, the output can be expected from *Out2* only. As expected, high output ripple (50-mV) is inherited due to Dickson's topology inspired configuration in a Series-parallel power stage network of MCP with no regulation scheme applied to this mode. Due to both left and right networks were needed to configure *HC* mode, and hence 180-degree matching network is not available for an interleaving scheme.



(a) **(b)**

Figure 4- 20. (a) Load and line regulations at High Conversion (*HC*) with a *feed-in* system and (b) its zoom-in view at saturation.

Again at 0.5-V input with 3.946-V (@16-µA load), no meaningful DC output is detected at *Out2*. However, when the load is lower to 2-µA, as shown in Fig. 4.21, the PMS starts to operate again because sufficient voltage is generated at V_{START} at a low load.

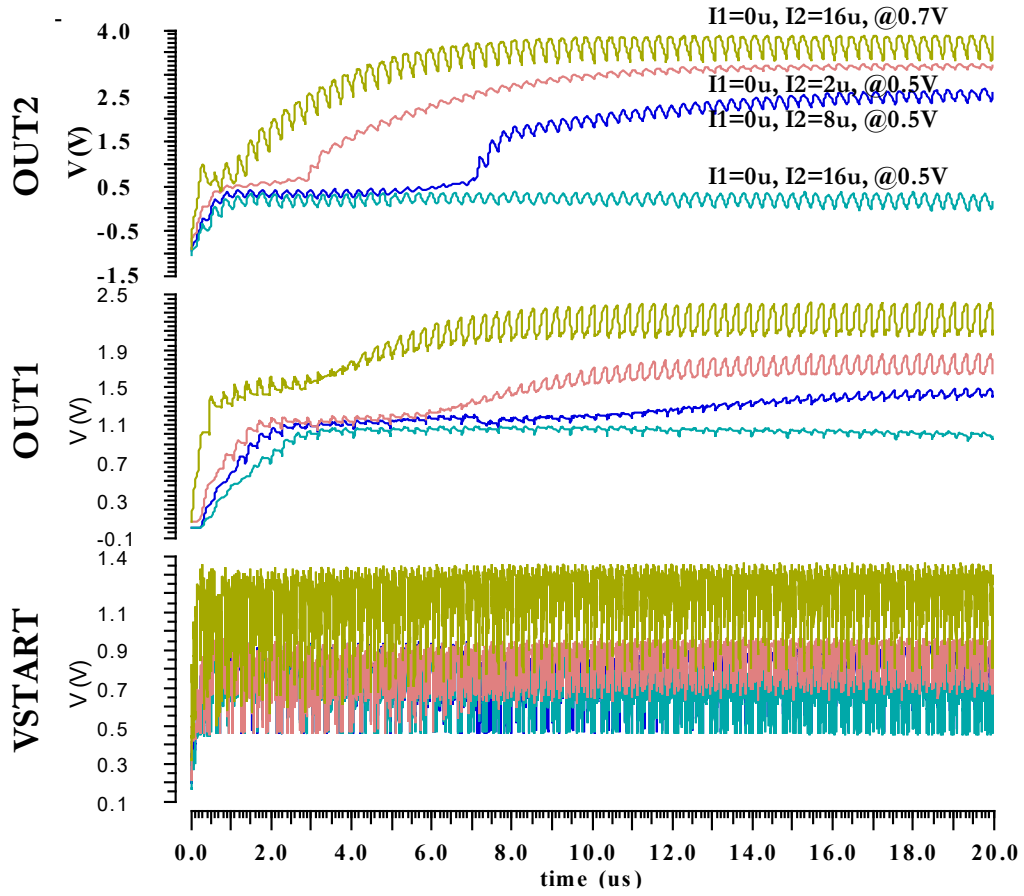


Figure 4- 21. Line regulations of PMS in High Conversion (*HC*) mode with a *feed-in* system.

D. The result and discussion of PMS in Double Boost (*DB*)mode

Once the SISO modes are considered, the SIDO modes are analysed through post-layout simulations. Starting with *DB* mode as depicted in Fig. 4.22, line regulation is simulated by keeping 0.6-V input and varying current loads (*I1, I2*) from 1-µA to 16-µA. The PMS has yields output voltages range from (1.978 V to 2.309 V) at *Out1* and (1.974 V to 2.309 V) at *Out2*. Total power output varies from 4.618 µW (@1-µA=*Out1*=*Out2, Pin*=22.518 µW) to 63.25µW (@16-µA=*Out1*=*Out2, Pin*=91.74 µW).

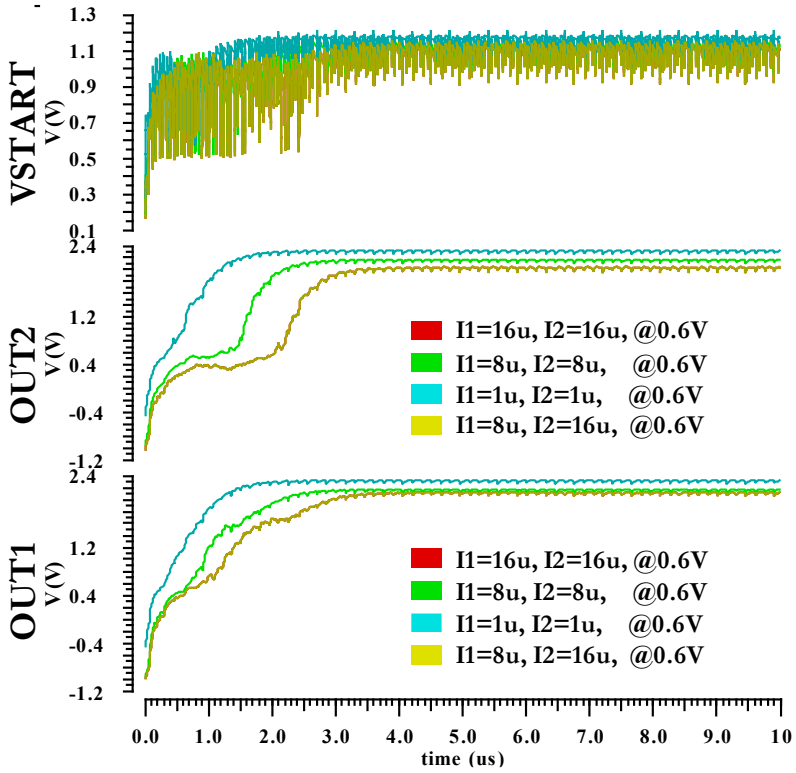
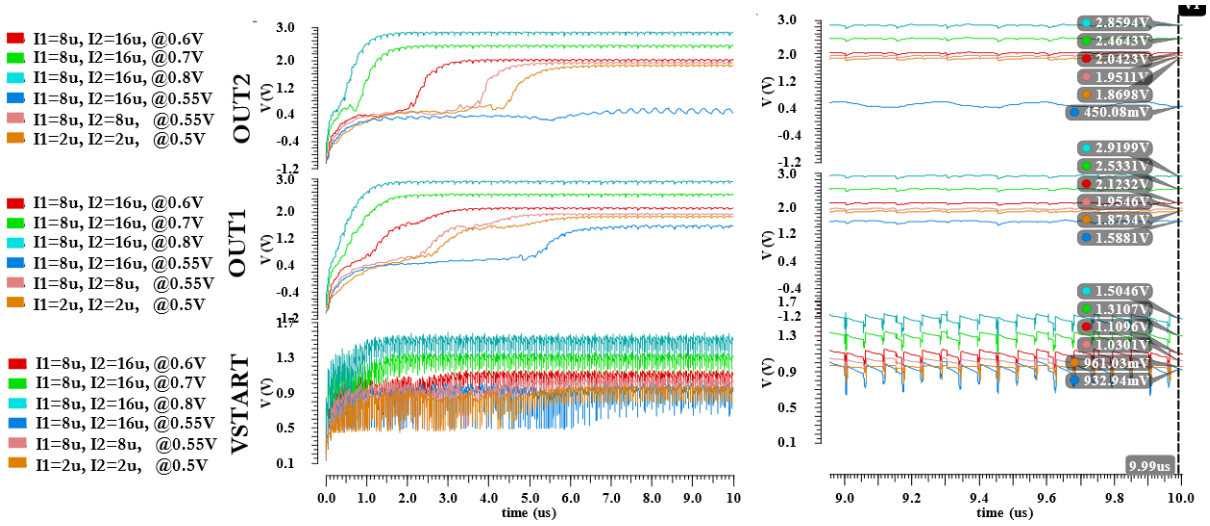


Figure 4- 22. Load regulations of PMS in Double Boost (*DB*) mode with a feed-in system.

Moreover, both load regulation, varying output from 2-µA to 16-µA, and line regulation, input voltages vary from 0.5-0.8 V, are simulated in Fig 4.23. Apart from (*I1*=8 µA, *I2*=16 µA, @0.55 V input), other conditions satisfy the expected outcome. This false state again reflects the same explanation discussed in *HC* and *LP* mode. In all situations, taking advantage of MCP's regulation scheme, the zoom-in results in Fig. 4.23 has confirmed the low ripple output of 16 mV has achieved. Finally, PMS in *DB* mode has reached the highest efficiency of up to 85.918 % (@0.5 V input, 2-µA load at each output).



(a) (b)

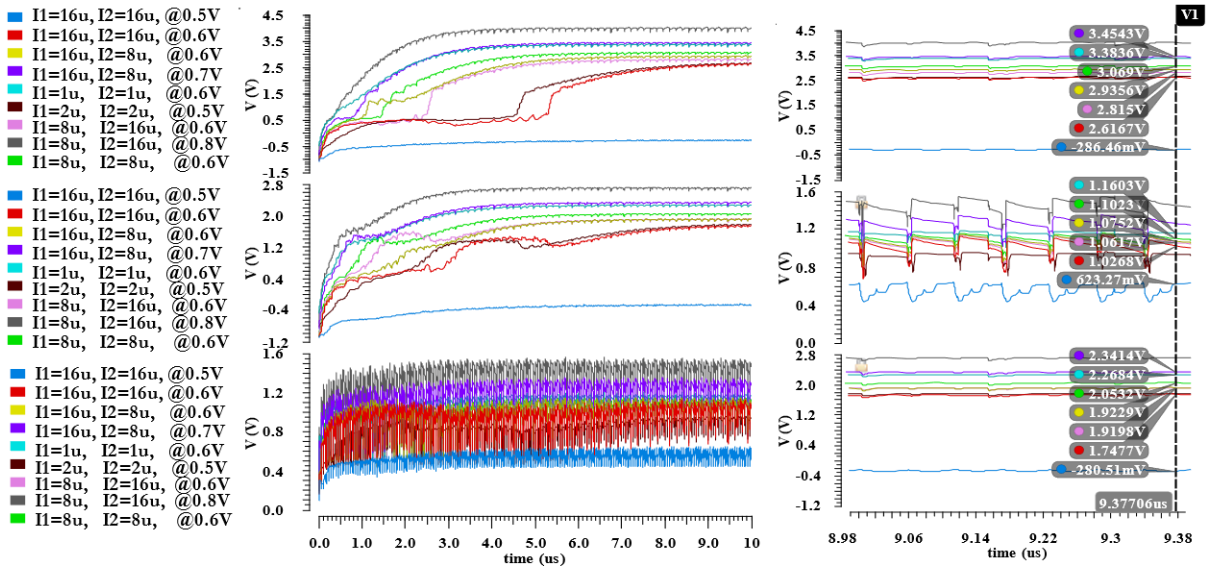
Figure 4- 23. (a) Load and line regulations of PMS in Double Boost (*DB*) mode with the feed-in system(b) and its zoom-in view at saturation.

E. The result and discussion of PMS in Super Boost (*SB*) mode

Finally, post-layout simulation of another SIDO *SB* mode with a feed-in system is analysed—Fig. 4.24 depicted load and line regulations of PMS in *SB* mode. In *SB* mode, higher DC outputs at *Out2* than *Out1* are expected at all load and line conditions. Simulated line regulation keeps 0.6-V input and varying current loads (*I1, I2*) from 1-µA to 16-µA. The output voltages of PMS range from (2.259 V to 1.71 V) at *Out1* and (3.37 V to 2.56 V) at *Out2*. Total power output varies from 5.629µW (@1-µA=*Out1*=*Out2, Pin*=30.99 µW) to 68.36 µW (@16-µA=*Out1*=*Out2, Pin*=122.7 µW).

Besides, load regulation in 0.5 V (*I1*=2 µA, *I2*= 2 µA) and 0.5 V (*I1*=16 µA, *I2*= 16 µA) is also simulated in Fig. 4.24. As expected, when 16–µA is connected to PMS at 0.5 V input, the V_{START} failed to reach the DC output to targeted around 1-V, which MCP can operate. The reason for being is because SCP can only provide the load current of 100–µA while generating the desired voltage of around 1 V. When PMS load is too high, the total power consumption of current load and MCP exceeds the supply limit of SCP. Therefore, the limitation is at SCP. This problem can be easily solved by scaling SCP to be able to handle a larger current load.

Furthermore, line regulation is simulated with the input of 0.6 V (*I1*=16 µA, *I2*= 8 µA), 0.7 V (*I1*=16 µA, *I2*= 8 µA), and 0.8 V (*I1*=16 µA, *I2*= 8 µA). Subsequently, PMS produces $V_{OUT1,@0.6V}$=1.90379 V and $V_{OUT2,@0.6V}$=2.92 V (*Pin*=53.78 µW, *Pout*= 88.21 µW), $V_{OUT1,@0.7V}$=2.371 V and $V_{OUT2,@0.7V}$=3.43 V (*Pin*=119.1 µW, *Pout*=65.38 µW), and $V_{OUT1,@0.8V}$=2.68 V and $V_{OUT2,@0.8V}$=4.05 V (*Pin*=144.2 µW, *Pout*= 75.46 µW) respectively. Lastly, PMS in *SB* mode has achieved an efficiency of up to 61.56 % (@0.6 V input, *I1*=8 µA, *I2*=16 µA).



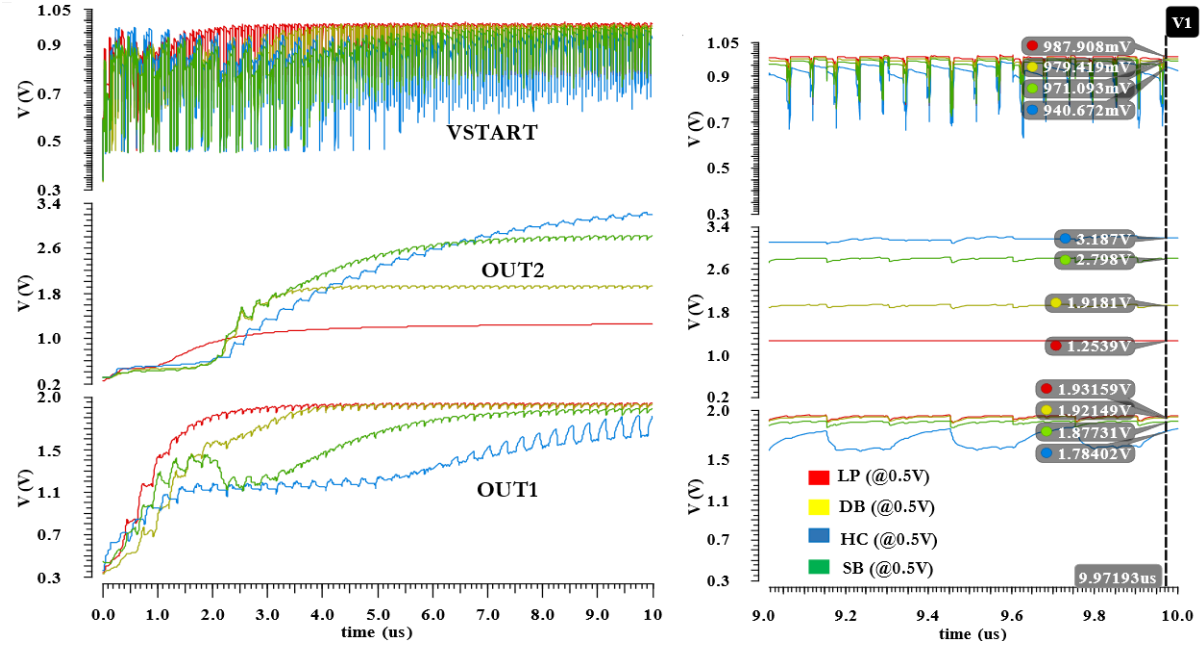
(a) (b)

Figure 4- 24. (a) Load and Line regulations of PMS in Super Boost (*SB*) mode with a *feed-in* system and (b) zoom-in view at saturation.

F. The result and discussion of PMS in *LP, HC, DB* and *SB* modes, in no resistive (zero current) load condition and current load change from 0-µA to 16-µA.

1.8.1.1.

Moreover, the PMS output transients for different MCP operational modes (i.e. *LP, HC, DB* and *SB* modes) are presented in Fig. 4.25(a), and their saturation region close-up view is illustrated in Fig. 4.25(b).



(a) **(b)**

Figure 4- 25. (a) The output results of PMS at an input voltage of 0.5 V to PMS in which the main converter operates in *LP, DB, HC* and *SB* modes. (b) The zoom-in view at saturation.

Further investigation is carried out by changing the current load of the PMS from zero to the 16-µA for a 10-µs period with 300-ns rising and fall time. Fig. 4.26 shows that PMS's output reciprocates with quick transient time within a few microseconds for an abrupt change at load. The adjustment was made by varying operation frequencies, mainly for the MCP and for the SCP. As observed, the output ripple tends to become more prominent at larger loading conditions. An increase in MCP's operating frequency enhances the stable output with smaller ripples, which eliminates the need to replace the bigger filter capacitor at the load. As seen in Fig. 4.26, the output voltage has dropped as expected since there is a significant change in the current sink at load. The MCP in *DB* mode achieves 2.309 V and 2.308 V at V_{out1} and V_{out2}, respectively, for 0.6 V input voltage and 1-µA current loads. They result in power efficiency of 71.9% and a VCR of 96%. However, at 16 µA current load, it yields V_{out1}=2.159 V, V_{out2}=2.157 V, the power efficiency of 77.9%, and VCR of 89%. An investigation from line regulation (0.5-0.8 V) and load regulation (1-16 µA) of proposed PMS suggest that the power efficiencies are highest for single output modes; in *LP* and *HC* modes achieve 73% (@*PV* input 0.6-V and 16-µA load) and 43.45% (@*PV* input 0.7-V and 16-µA load), respectively. Similarly, for dual output modes, in *DB* and *SB*, modes produce 85.91% (@PV input 0.5-V and 2-µA load at each output) and 61.56% (@*PV* input 0.6-V and 16-µA and 8-µA loads).

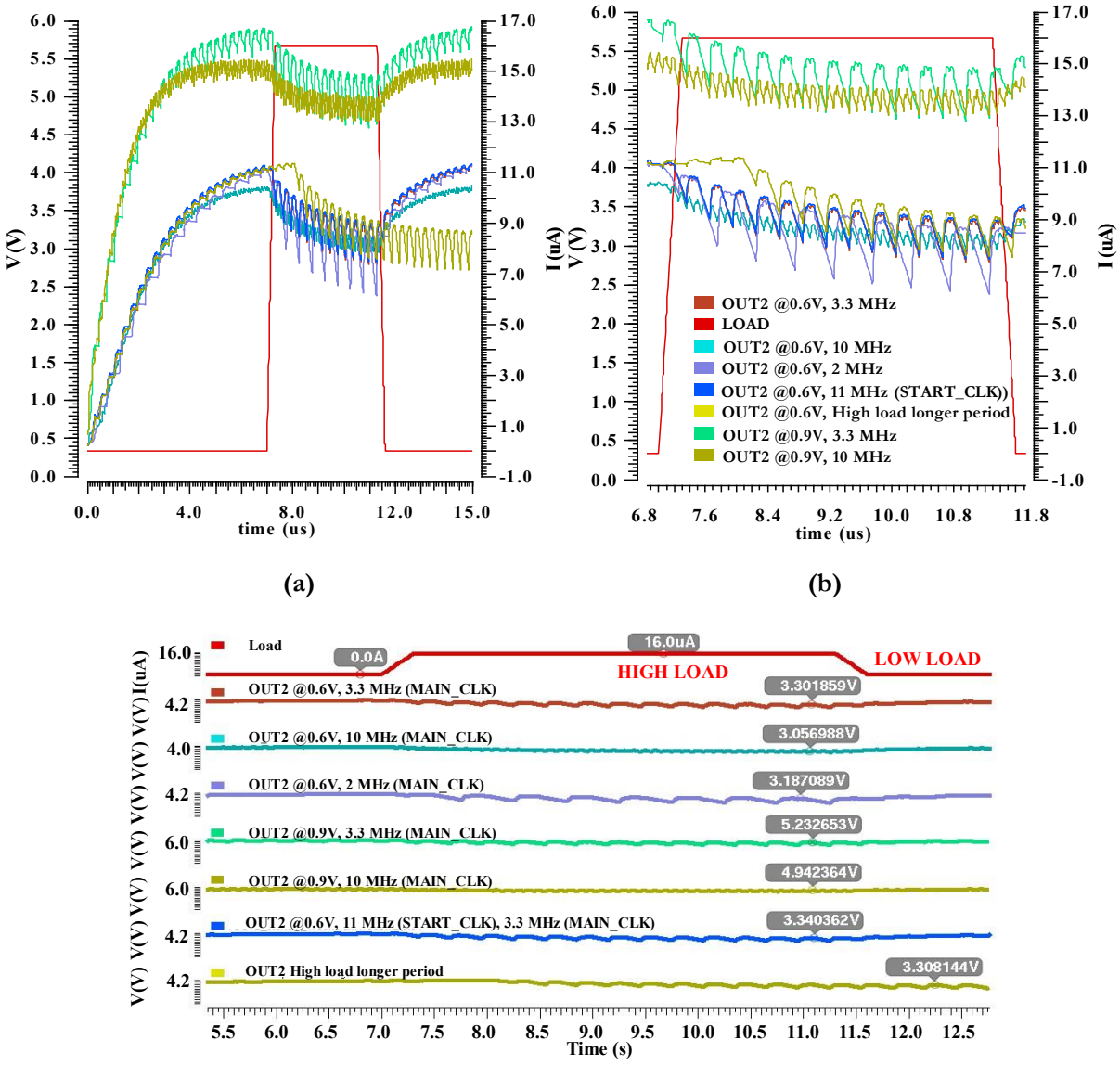


Figure 4- 26. The output performance of the proposed PMS when the current load varies from low (0-A) to high (16-µA) load. Its close-up view in (b) and in zoom-in view (c). The variation in operating frequencies of SCP and MCP clocks to observe ripple regulation.

G. Comparison with state-of-the-art

To validate this proposed work, the comparison has been made with state-of-the-art in TABLE 4.1. The presented work has a minimal area, the most miniature integrated capacitors, and comparable efficiencies for both individual CPs and overall PMS. Moreover, the PMS can produce both SIDO and SISO for step-up conversions of choices. Compared with fixed gain SIDO designs in [45, 128, 203], this CP is reconfigurable and can switch to SISO reconfigurable output. Contrary to designs such as [82, 128, 156, 238], presented work can only produce step-up conversions as well as integer gain. Notably, previous work of MCP [82, 238] has proven that this MCP network is flexible enough to get configured for fractional gains as well as step down conversions if desired. Simple resizing multiplexers can do this in GCU with a small layout area overhead.

Due to CP's interleaving regulation scheme, a small 5-pF external capacitor is sufficient to yield a low ripple of 16 mV for all modes except *HC* mode. Fig. 4.26 has proven that achieving the stable output in *HC* mode is feasible by compensating with a varying operating frequency for MCP. Therefore, it is fair to verdict CP produces the lowest output ripple performance, which is arguably closely matched to [239].

Finally, power density is driven by dividing the total effective die area of PMS (915 µm × 180 µm) over the maximum output power of 75.4 µW, resulting in a maximum CP power density of 0.457 mW/mm^2. Fig. 4.27 illustrates a comparison between this work and some other recent works from [82, 128, 203, 238-240]in terms of power density. As shown in this figure, the works in [45, 128, 238] have better efficiency, whereas multi-output CP in [45]with fixed gain ratio has the highest simulated efficiency of 90% and lowest measured efficiency of 74.5% is presented in [82]. The proposed PMS displays an efficiency of 85.92%, based on post-layout simulation. The proposed PMS produces a better result in comparison with [128, 240] and next-to-best work in comparison with [203]. However, this proposed CP is intended for a microwatt power range with a minimum area among state-of-the-arts, and it is suitable for wearable applications.

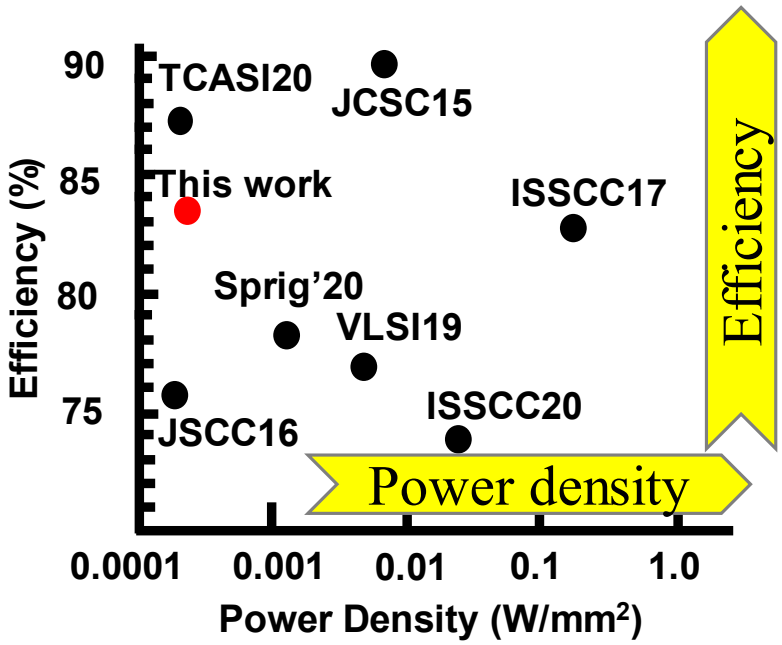


Figure 4- 27. Efficiency over Power Density in comparison with state-of-the-art in TABLE 4.1.

TABLE 4- 1. PERFORMANCE SUMMARY OF PMS AND COMPARISON WITH STATE-OF-THE-ART.

Specification	This work			ISSCC 20	ISSCC 17	VLSI 19	TCASI 20	Springer 20	JSSC 16
	Start-up	Main	System	[82]	[238]	[239]	[128]	[203]	[240]
Technology	180nm	180nm	180nm	180nm	28nm	130nm	180nm	65nm	180nm
Input(V)	0.5-0.8	1	0.5-0.8	2.4-44	1.3-1.6	1.5	0.64-1.4	1.05-1.4	0.35-0.60
Output(V)	0.7-1	1.98-3.6	1.98-3.5	1-2.2	0.4-0.9	0.44, 0.88	3-4.2	0.55, 1	0.86-1.8
I_{load} (mA)	0.018-0.103	0.032	0.032	2-50	100	12	-	0.35,0.01	-
VCR(x)	2.5	2,3,4	2.5,2,3,4	1/2	2/3. 1/2	1/3, 2/3	2.14-6.56	1/2, 1	3
No. of outputs	1	2,1	2,1	1	2	2	1	2	1
P_{out_max}(mW)	0.104	0.0656	0.0754	0.87	-	6	<2.1	-	<0.396
P_{Den}(mW/mm²)	-	0.653	0.457	53	150	8.3	0.359	1.32	0.226
Ripple(mV)	-	16,50 (@*HC*)	16,50 (@*HC*)	15-30	-	20-60	-	50-80	-
Efficiency (%)	86.67	80.28W/F 90.43Wo/F	85.92	74.5	83.8	78	88.9%@ 1.4V Vin, 3.4V Vout	78	75.8% @0.59V Vin 1.41V Vout
Int. Passive Device	3.58pF (MIM)	30pF ×4 (MIM)	3.58pF+ 120pF (MIM)	7nF	8.1nF (MOM+ MIM)	450pF (MOS)	1.2nF	450pF (MIM)	4.05nF
Area (mm2)	-	-	0.0001647	8.9	1.5	0.72	-	0.493	1.75

4.7. Summary and Remarks.

This proposed power management unit can be summarised as depicted in Fig. 4.28. The energy harvester has been discussed with survey approach in introduction section, and the power management system (startup charge pump in Appendix-3 section and main charge pump in this Chapter) had been analysed. I did not include a storage capacitor between the start-up charge pump and the main charge pump due to the large chip area consumption of a capacitor. This chapter demonstrated a power management system suitable for wearable devices with multiple DC voltage and small input DC levels. The PMS comprises SCP and MCP. The former withstands reliable line regulation and load regulation at high efficiency, and the latter produce SISO simultaneous dual output and SIDO with flexible gains of choice. The proposed PMS has achieved a high-power efficiency of 85.92% while occupying a silicon area of as small as 0.164 μm^2. The proposed ideas were validated with the post-layout simulation of the fabricated chip. Furthermore, the proposed PMS is compared with the state-of-the-art, reflecting competitive properties in terms of the silicon area and power efficiency and reconfigurability.

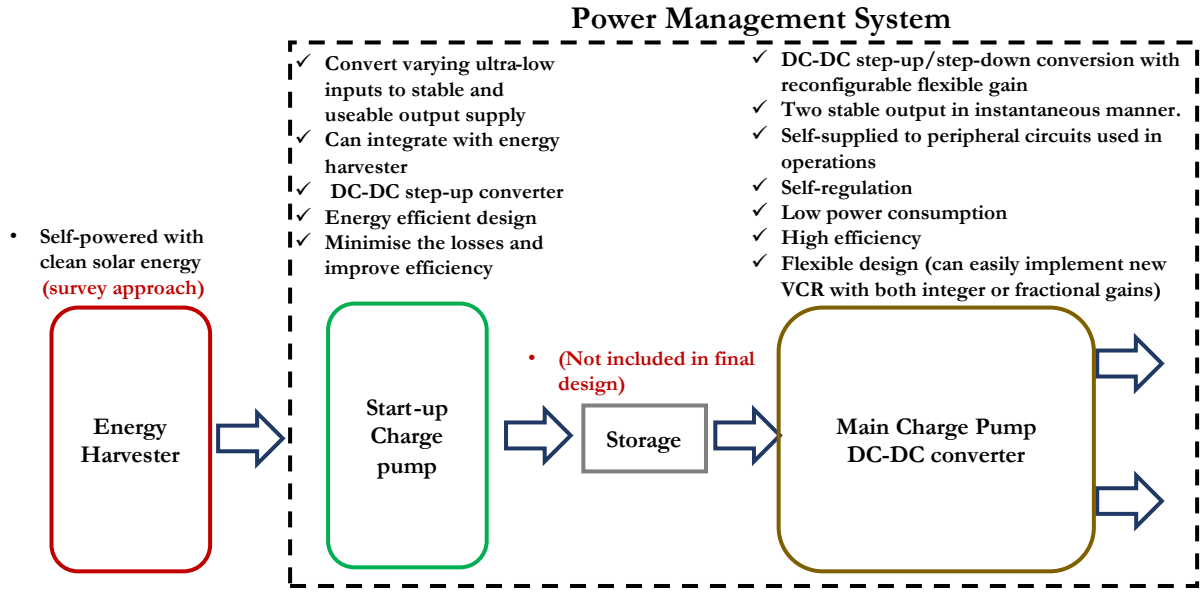


Figure 4- 28. The list of achievements is validated by the post-layout simulated results of a fabricated chip for the presented power management system.

CHAPTER 5: CONCLUSION AND FUTURE WORK

5.1. Thesis summary and conclusion

This Thesis demonstrated the novel power management system for low-powered wearable applications.

In Chapter-1, the project's motivation and the switched-capacitor approach converter was chosen to employ as the power management system (PMS) in wearable applications were introduced. Moreover, why the solar energy harvester type is a suitable candidate for wearable applications due to their harvestable power and size were discussed.

The discussion continues, where various topologies developed over the history of charge pumps have been demonstrated. Followed by the existing energy harvester used switched-capacitor approach DC-DC converter was widely reviewed. By taking inspiration from state-of-the-art literature, my step toward the proposed power management system comprises a start-up charge up that will later store in a secondary source – storage or capacitor, and then supply towards the main DC-DC converter to power manage were proposed.

In Chapter-2, the main charge pump converter's motivation and implementation, which was also the primary focus of this Thesis, was discussed. In the introduction the chapter-2, the discussion was made on why a single input multi-output converter (SIMO) provides an advantage over single input single output (SISO) for multi-load applications. It was due to wearable applications comprising multiple building blocks, each of which operates in different voltage ratings—starting with the novel 4-phase converter as the first step, the simultaneous dual output reconfigurable converter step-up and step-down conversion at the same time. Furthermore, the converter can configure in both integer and fraction gains- namely Normal mode (×3/2, ×1/2), High Mode (×2, ×1), Double Boost Mode (×2, ×2) and Super Boost Mode (×2, ×3). The analytical calculations of the novel 4-phase converter were extensively discussed. The converter achieved up to 85.26% power efficiency. The various load regulation varies from 50-100 kΩ has been presented for four different modes. At best, it produces (1.49 V, 1.905 V) for Normal mode, (1.905 V, 0.98 V) for High Mode, (1.97 V, 1.97 V) for Double Boost and (2.85 V, 1.89 V) for Super Boost mode. The output ripple varies between 14-59 mV. The line regulation was also simulated by varying inputs 0.8-1 V.

Subsequently, In Chapter-3, a newly improved proposed 2-phase converter which was evolved from the previous 4-phase design had presented. The novel 4-phase design converter's problem and challenges were discussed, and the analysis of how these challenges were overcome was described. In proposed 2-phase topology not only have properties of being able to gather simultaneous dual-output voltages offers step-up conversions with only 2-phases logic and reconfigurable scheme- namely Low Power Mode (×2), Double Boost Mode (×2, ×2), Super Boost Mode (×2, ×3), High Conversion Mode (×3.5). Normal mode was disregarded in this design because of the step-down VCR. However, if additional gains were required, the new gain control unit (GCU) was flexible, that with a bit of expense of chip area trade, new gains mode could be easily implemented. This process does not require a change in the power stage network.

Moreover, since the new converter design operates in 2-phase logic, the control circuit complexity and its power consumption in contrary to the 4-phase clock generator circuits had reduced. It can benefit the area consumption of the chip area, which contribute to the cost. Four integrated capacitors in the main charge pump had resized from 1-nF to 30-pF to present the miniaturised power converter. The passive device, such as a capacitor, consume a large area in the layout design. The discontinuous-continuous switches' requirement was also eliminated by simply connecting the two internal output pairs that share the different amplitudes at different phases that had interleaved each other in the differential load position. These were

regarded as O_{ut1} and O_{ut2}, and for simplicity, it was designed to have O_{ut2} higher than O_{ut1} in all gain modes. The operation frequency of 3-4 MHz was used in the simulations because it was in tune with the given integrated capacitor size and provided a few micro-seconds of the charge settling time in a saturation region. The operation frequency can vary according to the output ripple condition at the load. Converter performance was analysed in two parts- (1) stand-alone converter (without feed-in and self-supplied (with feed-in) system. In a stand-alone system, only the charge pump's power stage network was considered. However, the charge pump output self-supplied to the V_{DDH} of GCU in the feed-in system. Therefore, all the parts were integrated to function; the main charge pump was considered in the feed-in design. The converter provides high power efficiencies of up to 90.43% at (W/F) and 80.28% at (Wo/F)). Furthermore, the converter demonstrated power densities of 0.653 mW/mm^2. The process and mismatched Monte Carlo robust post-layout simulation suggest that only a slight variation can be expected in future experimental results. Hence conclude presented post-layout simulation was reliable in a small error margin.

This novel 2-phase main charge pump was self-powered, self-supplied and self-regulated. The charge pump can perform reconfigurable SISO and SIDO conversions to provide wide VCR and provide high power efficiencies of up to 90.43%. To the best of my knowledge, this proposed converter was the only converter that could configure SISO and SIDO in the same design and self-powered the control unit simultaneously. This reconfigurable converter offers SIDO a more extensive output voltage range, which can benefit multi-functional wearable devices operating at different voltages. This proposed design was beneficial for the plethora of low-powered wearable devices, and implantable devices operate in a micro-Watt scale.

In Chapter-4, the intended PMS system has achieved by combining the start-up and the main charge pump together. Moreover, Appendix-3 discussed many design ideas of the start-up charge pumps that have been designed and among which the Design-4 converter had chosen as PMS's start-up charge pump because of its ability to provide high load current as well as high power efficiency.

While combing two converters together, the storage unit- large capacitor was not included, as intended from Chapter-1. If the storage capacitor is integrated, it will consume a large chip area. However, the main charge pump can benefit from a clean DC input. This was because it can act as the filter capacitor to the start-up charge pump due to self-regulation. Nevertheless, cross-coupled topologies were immune to low ripple output because of interleaving between complementary MOS structures; this further helps with redistribution loss as the variation at the output is minimum. The results show that the main converter displayed excellent line regulation from the noisy output of the start-up converter and still provided reliable and stable intended voltage gains from selected modes. Thus, indicate the reliable line and load regulation performances of the main charge pump. Note that if the storage capacitor was integrated, it was worth considering the Design-3 charge pump type in Appendix-3 due to the energy-saving scheme offered by the clock disabler circuit. Therefore, when considering the end-to-end efficiency, the power losses across the start-up charge pump was no longer static.

Finally, Chapter-5 presented the summary of the thesis for each chapter as well as the conclusion remark for the switch-capacitor technology. Followed by the discussion of my future work where the fabrication process and experimental setup of the converters were mentioned. There was a total of 10 designs that came in different sizes and were fabricated in 5-mm^2 chip area. This was all implemented and fabricated in 180 nm RF CMOS technology. For the time being, there was a design defect in fabricated I.C.s due to a fatal error made while connecting to I.O. pads. The correction for the mistakes is being made, and I intend to refabricate again in the next taped-out run. Therefore, all the presented results were a post-layout simulation in this design.

In conclusion, the proposed PMS comprises a start-up converter, and the two designs of the main charge pump had successfully presented in this Thesis. The proposed PMS is suitable for low-power applications operate in micro-Watt regions.

5.2. Conclusion remarks

According to Inshad [141], integrating capacitors in monolithic SC converter imposes particular challenges. Restricted chip area constraint integrated capacitance and integrated capacitor suffers significant bottom plate parasitic capacitance, impacting efficiency. Moreover, the integrated switches suffer from process limitations. The thickness of the gate oxide influences how much gate voltage can be applied to the switches. In generating the step-up conversion in SC converter, high voltages were near to the output side. For high gain configurations (*SB, DB* and *HC*) in the power stage network, adequate over-drive gate voltages were needed for the power stage transistor switches. The maximum gate voltages reduce as the process technology gets smaller. Therefore, these restrictions collectively limit the use of monolithic SC converters to low power applications. The topologies such as the series-parallel and Fibonacci, which required high gate voltages during gain configurations and had high bottom plate parasitic loss suffer greatly in integrated design.

To overcome restrictions, either capacitors or switches can be discretely employed externally as a straightforward approach. For instance, using external capacitors, high-value capacitors can be now accessible to achieve diverse power stages and increase the suppliable load current. Therefore, it has become applicable for high power applications. Nevertheless, the following second category approach was not suitable for the area constraint system-on-chip intended applications.

To compromise, there is a need for more innovative solutions such as

- The charge recycling technique help reduces the bottom plate parasitic but not completely eliminate it.

- Ripple management techniques such as interleaving between two identical networks or adaptive pulse modulator to adjust the operating frequencies have been proposed to achieve a stable DC supply to the load. However, identical networks increase the chip area, and the frequency adjusting circuits can potentially induce noise and not be suitable for reading out circuits with high sensitivity.

- In SC converter, various losses contribute to the final efficiency. One of them being multiple reversion losses, for instance. It can be eliminated using a careful design clock control scheme. Depending on the topologies, the control clock scheme also varies. Thus, one solution may not apply to the other topologies.

- Since not all the topologies has the next power stage to borrowed require high voltage to supply the previous stages like Dickson design architecture. Therefore, to avoid the need for external supply in other topologies in which following stage gains are not readily accessible, the innovative approaches of *feed-in* (*self-supplied*) to overcome adequate over-drive gate voltages is necessary.

- As more and more applications use the assistance of the energy harvester for the long run time and to ease the battery size, the converter should be operatable accordingly to the output characteristic of desirable harvesters. Since their harvested outputs heavily rely on several factors, several techniques have been proposed and yet to be presented to further minimise the variations at the input side to the PMS.

- The multi-output converters provide optimal VCR to multi-loads application with different voltage ratings. More innovation work of the multi-output converter designs without doubling the integrated area is necessary. The use of the proposed 4-phase topology is one solution towards it. The following work- a proposed 2-phase design address the fixed gain configuration limitation of the multi-output converters. More gain configurations (fraction and integer gains) can still be added to get a wide range of VCR for single output and multi-project outputs. It can be achieved without increasing many areas overhead.

The future system-on-chip integrated power system can produce more power and improve area efficiency and be suitable for diverse applications by addressing challenges that arise from integrating both capacitors and switches through attractive solutions.

5.3. Future Work

5.3.1. Design process of fabrication and experimental setup

The proposed work comprises different reliable and efficient self-powered DC-DC converter designs, serving different purposes. The designs can be divided into three categories-

(1) four cold-start converters, which a solar energy harvester can power. Our energy-efficient converters are based on both Dickson and crossed-couple topologies.

(2) Four novel designs of dual outputs, highly efficient reconfigurable converters designed by series-parallel topology.

(3) The power management system contains both (1) and (2) is designed in Cadence software with its PDK provided by TSMC and to be fabricated in 180 nm TSMC RF technology to put the idea to the test. The design process flow is depicted in Fig. 5.1.

There are 10 designs, as shown in Fig. 5.2, which come in different sizes and performances. After fabrication, there will be 40 samples in total that should return. Each of the samples has a micrometre scale, and thus, to test it in our electronic lab environment, 10 samples are to send out to the external company to wire-bond on a printed circuit board (PCB). These 10 samples can be further divided into two categories: wire-bonded PCB_1 (5sample) and PCB_2 (5samples), as shown in Fig 5.3. Each wire-bonded $PCB_{1,2}$ allow us to test 5 chips at once. Ideally, I could dice 10 designs attached in one sample chip into 10 of them wire-bonded separately and achieve better performance in experimental results. However, dicing requires additional expenses as a trade-off. I only separate into two category PCB_1 and PCB_2, and plan to test 5 designs at once in each PCB. The manual reconfiguration of each testing can be done as suggested in Appendix 4- Fig. A4.2 and Fig. A4.3.

This is then fabricated in 180 nm TSMC RF technology to put our idea to the test. There are 10 designs, which come in different sizes and performances, in each chip, and I have fabricated 40 samples in total. Each of the samples has a micrometre scale, and thus, to test it in our electronic lab environment, 10 samples are sent out to the external company to wire-bond on the printed circuit board (PCB). These 10 samples can be further divided into two categories: wire-bonded PCB_1 (5 samples) and PCB_2 (5 samples). Each wire-bonded $PCB_{1,2}$ allow us to test 5 chips at once. Ideally, I could dice 10 designs attached in one sample chip into 10 of them wire-bonded separately and achieve better performance in experimental results. However, dicing requires additional expenses as a trade-off, can be divided into two categories PCB_1 and PCB_2 and test 5 designs at once in each PCB.

The experimental setup overview is illustrated in Fig. 5.4. Moreover, individual input-output signals from testing board PCB to transfer PCB are reassured, as shown in Fig. 5.5 via oscilloscope and the digital voltmeter available in the electronic lab, Glasgow University.

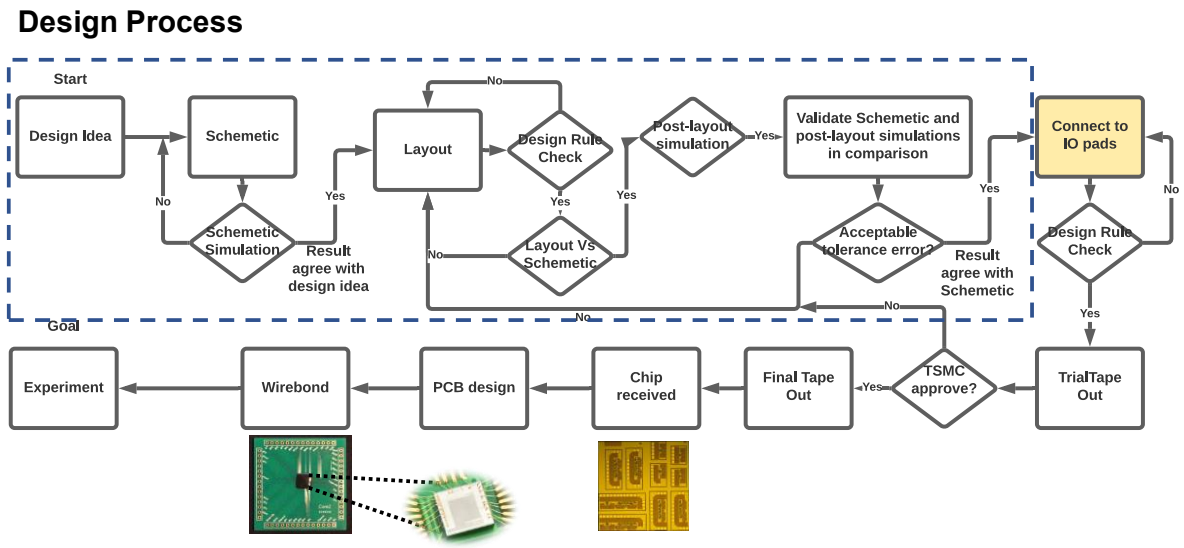


Figure 5- 1. The design process of the fabrication.

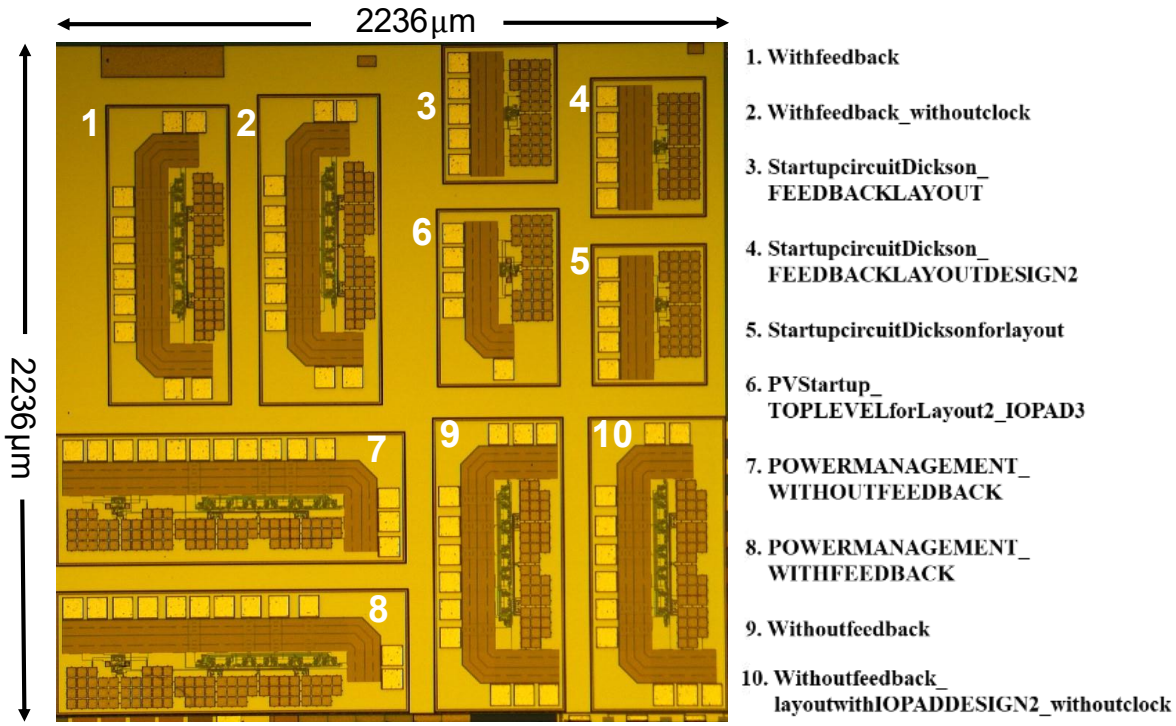


Figure 1. The fabricated chip microscopic photograph.

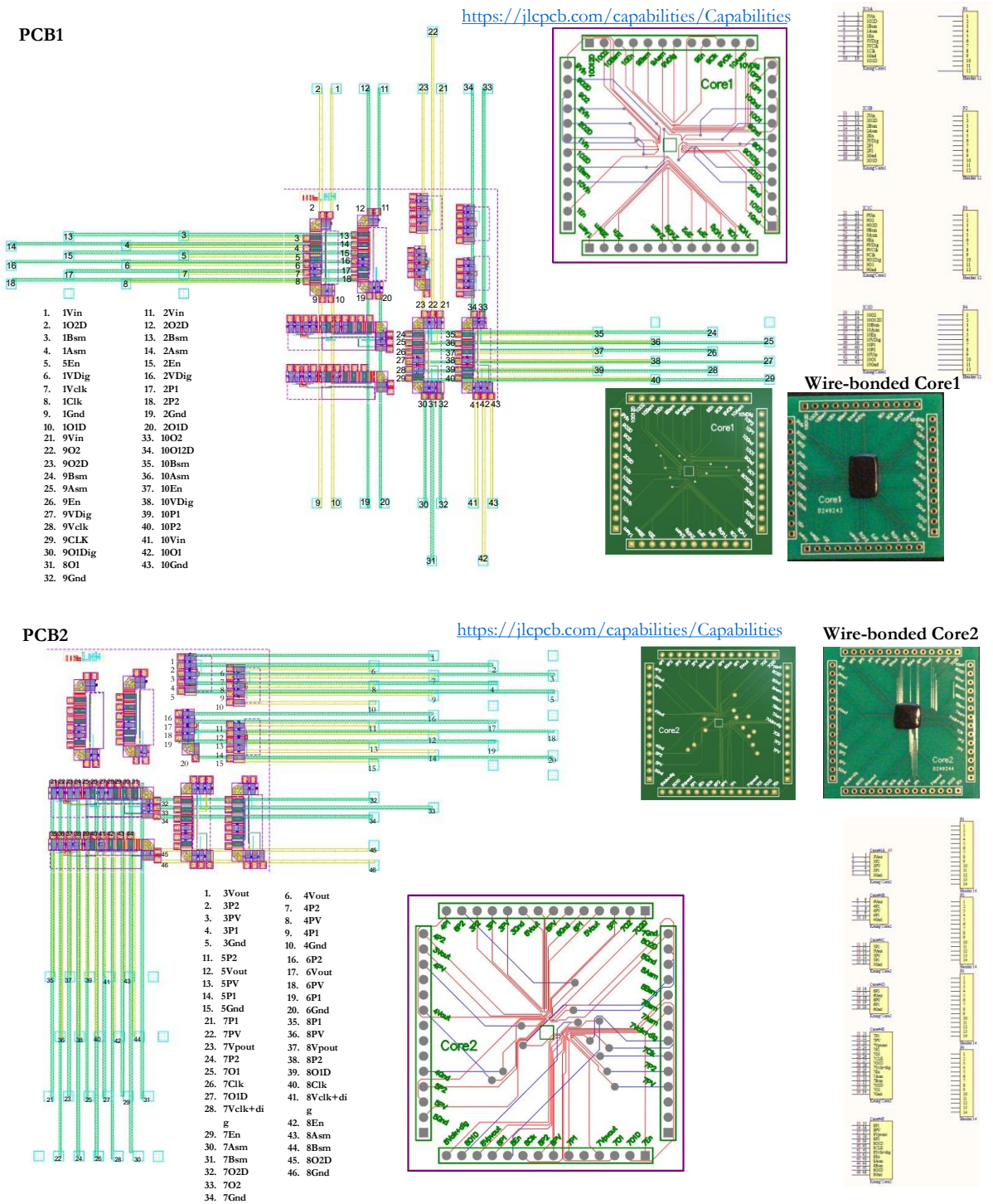


Figure 5- 2. Wire-bonded Core1 and Core2 on transferred PCBs.

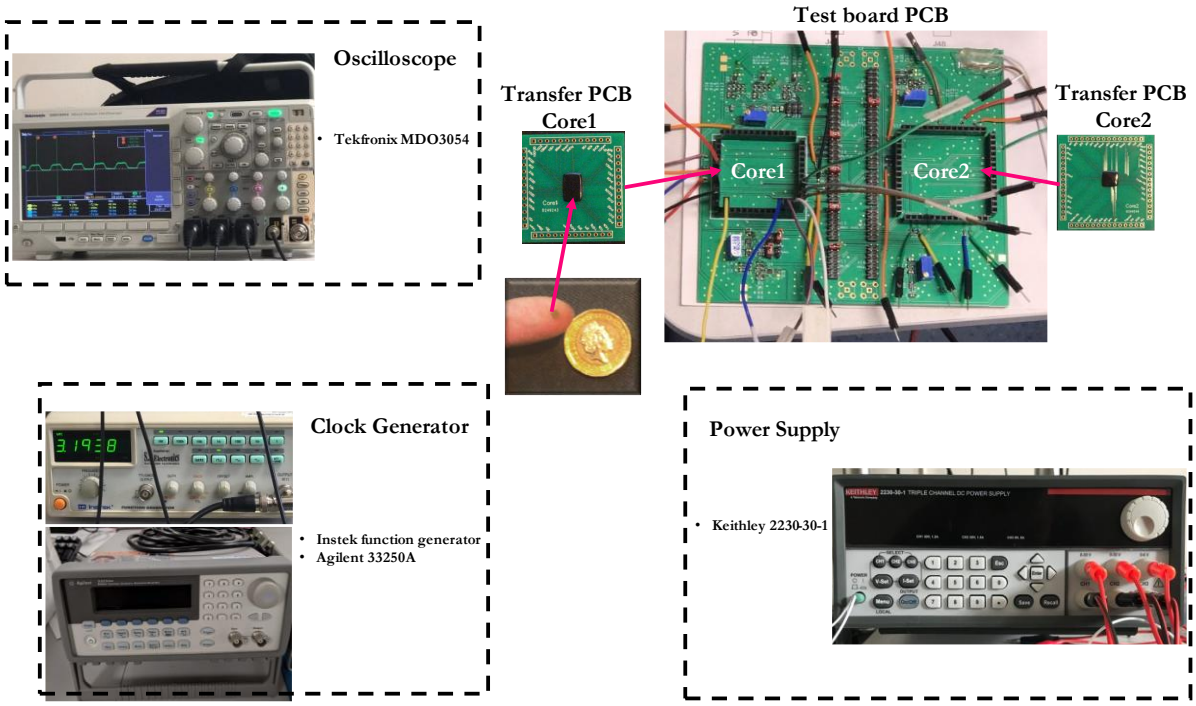


Figure 5- 3. Testing board and Equipment use.

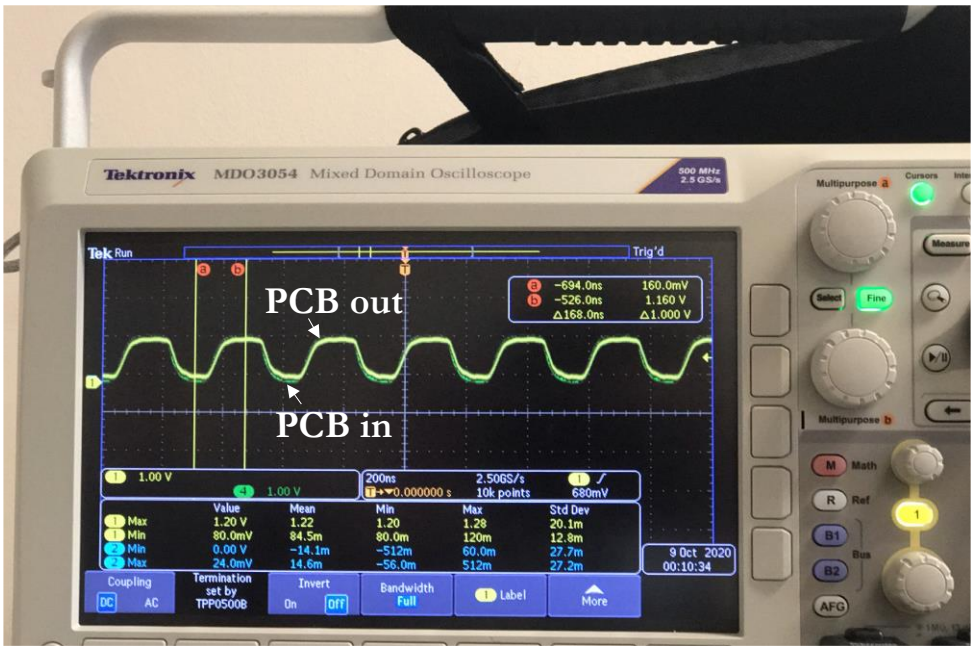


Figure 5- 4. Individual input-output signals of the testing board PCB have been tested and verified.

5.3.2. Main characteristic and challenges

The characteristic of proposed designs can be distinguished as-

(1) cold-start converters, which operate in ultra-low voltage output yield from energy harvester,

(2) the dual output capability with various DC gain configurations, which is beneficial in a system with operating blocks requiring different operating voltages at the same time.

(3) Lastly, the power management system contains both cold-start and reconfigurable converters altogether, making it ideal for energy-constrained devices and applications requiring wider operational voltages.

During our layout design process, the main challenge I have overcome is to minimise the non-ideal losses such as parasitic losses and maintain the highest optimum efficiency. My goal is to achieve a high-performance efficiency converter with minimum area consumption. I have made sure that R, C, and CC parasitic loss are minimum, and post-layout simulation produces 5% deviation within simulation results in constructing the layout. Achieving up to maximum efficiency of 83.5% for (1), converter (2) has 82.28% for the self-supplied system (SSS) and 90.43% for stand-alone (S.A.) converter. Also, PMU of (3), with (2) converter as the main converter, yields 67.5% with SSS and 70.79% with S.A., respectively. For example, to reduce the capacitive parasitic loss caused by two metal layers being too close to each other in a compact layout design, the width of the metal should increase. It has further cause resistive parasitic loss instead as a trade-off. I have tuned all the individual width and lengths of the track are optimum within the compact, effective area and still produce results closer to simulations results. In every change, DRC and LVS are validated. Thanks to carefully orchestrated steps and proven post-layout simulation results, the fabrication process's high success rate can be expected.

5.3.3. Troubleshooting the potential cause

Once we received back the wire-bonded sample, the experiment began, and we have discovered that most of the input-output ports (I.O.s) were unexpectedly shorted. I hypothesise that there are four potential causes - (1) during the wire-bond angle of wire accidentally cross each other, (2) wrong connection between sample chips I.O. to PCB ports, (3) top of the wire-bond is coated with protection after the wire-bond which could enhance the sealed polymer forcing wire to touch, (4) layout problem. Therefore, to trouble, each potential cause, here is how we analyse them.

Problem (1) – to avoid the wire bonding angle problem, I have placed the delta connection in PCB in the first place with adequate 100um space in between. Therefore, I am confident that it is not the issue. In addition, if it were an issue, the shorting would only occur for the neighbouring or adjacent wire. From our test, it is not the case.

Problem (2) – clear instruction has been provided on connections from sample chips I.O. pins to PCB ports. The clear label on PCB also helps intuitive understanding at the receiver end. During the double-check with the company technician, the suspicion was lifted as their understanding of our instruction was confirmed.

Problem (3) – One of the most likely causes. I could not visually confirm unless we get access through the X-ray machine due to black tape covering on wire-bonded PCB. I have tried to reach out to the university wire-bonding technician and had him confirm it too. However, the flaw in this suspicion would be-it should only affect only a few of the samples. But we have discovered that shorting occurs in all the sample chips.

Problem (4)- therefore, it has led to our last suspicion, the layout issue. Before introducing the layout and fabrication's potential issues, it is best understood to start off the introduction with the step-by-step establishment we have made during the layout design process, as depicted in Fig.1. According to the process, we can eliminate the steps taken highlighted in the dotted line because it has been validated by

both layouts versus schematic (LVS) and the design rule check (DRC). The issue come in the later stage when we connect the individual ports in layout design to predesign I.O. pads provided by TSMC company, as depicted in Fig. 5.6. These I.O. pads can be considered a doorway to the layout design to the outside world electronics. According to TSMC technicians, all the power lines should connect through the 'V_{DD}' pad which provides electronic system protection (ESP).

Moreover, all the ground signals should connect to 'V_{SS}' pad, and the rest of the signal lines should connect to the standard I.O. pad, which acts just like a wire without protection. Finally, each pad should connect through 'filler layers' or 'jumper layers' and 'conner cells' to position the location of I.O. pads from top to sideway and so on. I have chosen to connect the input power supply pins to the VDD pads by following the instruction, as it requires ESP protection. Similarly, the outputs of the converter are also connected to V_{DD} pads. This is because, in the DC-DC converter design, the output is considered the power line instead of the signal lines. Therefore, ESP protection is necessary to avoid unintended damage cause when the sensitive converter chip is used in a non-lab environment such as in medical devices.

As a result of choosing V_{DD} pads for both input and output lines, my experiment indicates that they ended up shorting together internally. Post discussion with the technicians and experience designers has pointed out that if we want to choose V_{DD} pads for both input and output, I require adding a 'Power Cut' pad in between or using the standard I.O. pad at own risk to the output pins. The only disadvantage of the 'Power cut' pad would be area will increase a few micrometres from our present design due to the additional pad size. But output pins are ESP-protected. The fundamental knowledge has not come to light during the layout design process because there were 100s of pads available in the I.O. pad library. It would not be possible to go through every pad in the datasheet. Therefore, I investigated selective few pads advised by technicians who do not have insight knowledge on my 10 different designs. Thus, a common beginner mistake has cost my first chip tape out and did not receive as expected results from my post-layout simulation. After gathering all the experiences, I have presented the correction plan as shown in Fig. 5.7.

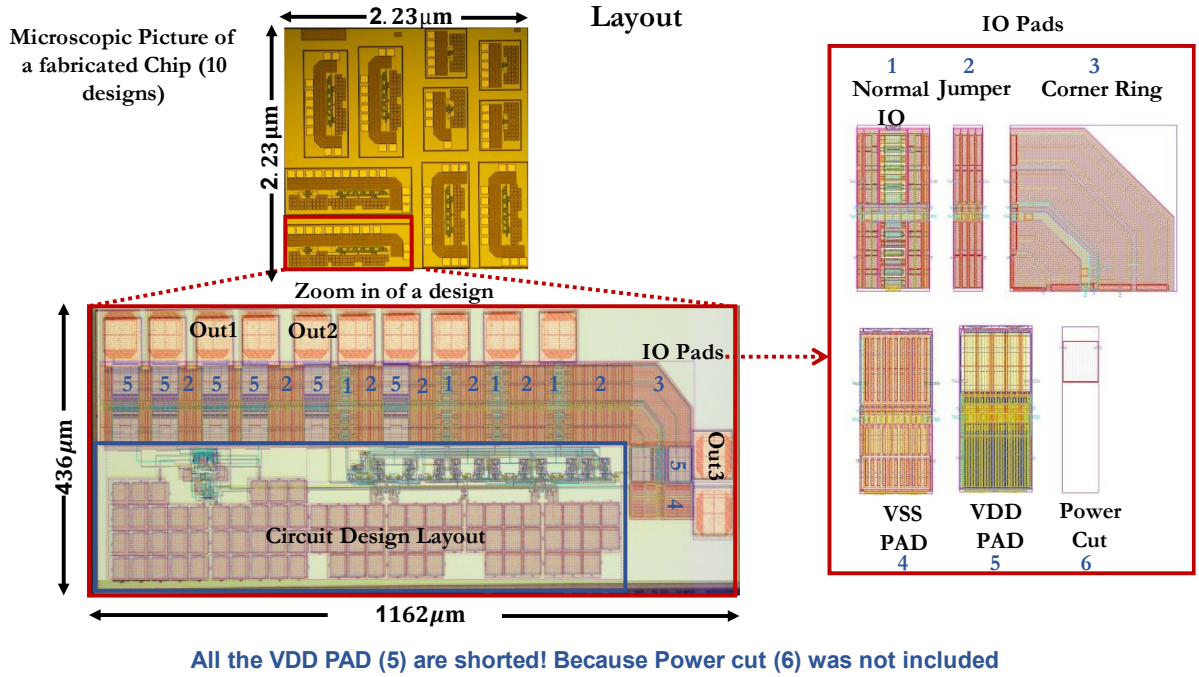


Figure 5- 5. Input/Output (I.O.) pads type used in fabrication.

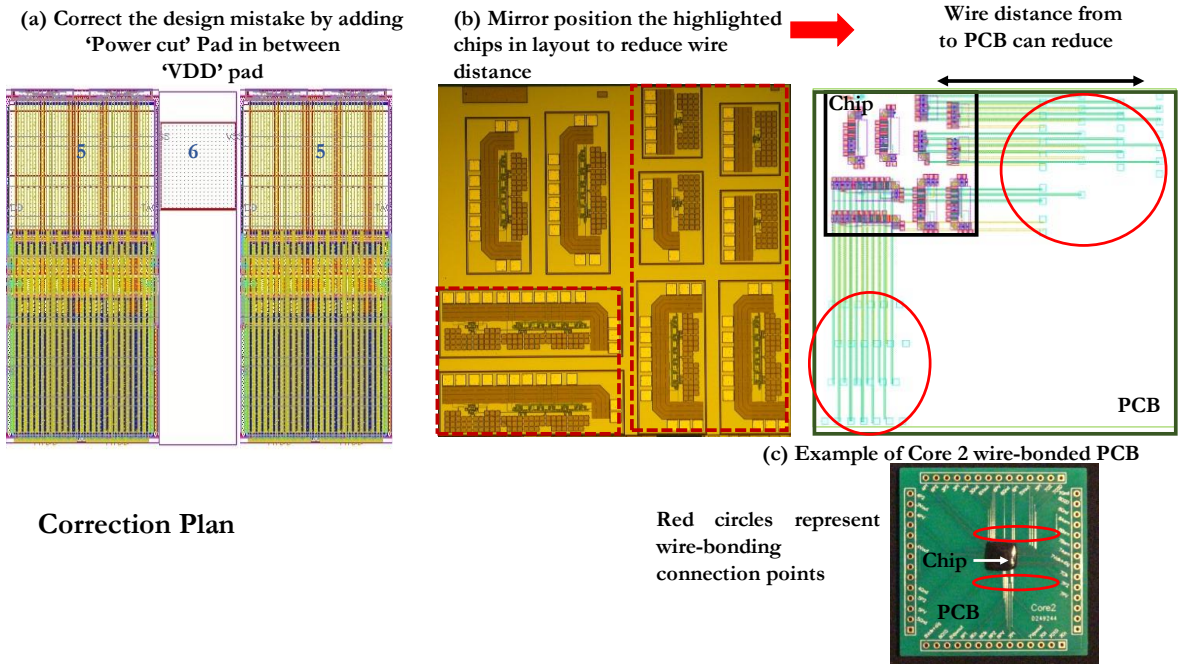


Figure 5- 6. Correction plan for next tape out.

APPENDIX

APPENDIX 1- CHARGE-PUMP DC-DC CONVERTER BASED ON SINGLE INPUT DUAL OUTPUTS (SIDO)

A1.1. Normal Mode analysis

A1.1.1. Output Voltages of Normal Mode

The first order differential equation of charging and discharging part of the RC circuit in Laplace and convert it back to time domain in Inverse Laplace, a final voltage $V_c(t)$ is the sum of the initial charging voltage $V_c(0)$ and the input voltage V_{in}. The total switching time (t) with RC time characteristic in Equation. (A1.1).

$$V_c(t) = V_c(0)e^{-\frac{t}{RC}} + V_{in}(1 - e^{-\frac{t}{RC}}) \quad \text{(A1.1)}$$

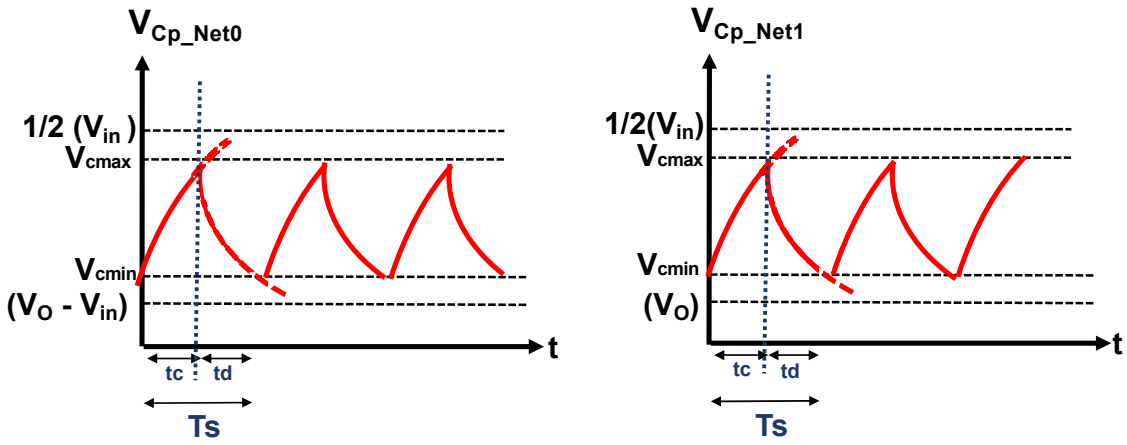


Figure A1. 1. Charging and discharging characteristic graph of capacitor in (a) Net0 boost conversion and (b) Net1 buck conversion in Normal Mode.

The coefficient of voltage values for each charged pump capacitors tends to charge-discharge to and actual voltages of capacitors (V_{cmax}, V_{cmin}). In the charging phase of Fig. A1.1 (a), a final voltage $V_c(t)$ is equal to V_{cmax} and the initial voltage $V_c(0)$ will be V_{cmin}. Since it is charged towards $\frac{1}{2}V_{in}$, produces the Equation. (A1.2). Likewise, a final voltage for a discharge phase is V_{cmin}, the initial voltage is V_{cmax} and V_{in} from Equation. (A1.1) can be replaced with $V_o - V_{in}$ to get Equation. (A1.3).

$$V_{cmax(net0)} = V_{cmin}e^{-\frac{t_c}{T_c}} + \left[\frac{1}{2}V_{in}\left(1 - e^{-\frac{t_c}{T_c}}\right)\right] \quad \text{(A1.2)},$$

$$V_{cmin(net0)} = V_{cmax}e^{-\frac{t_d}{T_d}} + [(V_o - V_{in})\left(1 - e^{-\frac{t_d}{T_d}}\right)] \quad \text{(A1.3)}.$$

Likewise for Net1 in Fig. A1.1 (b) can derive into-

$$V_{cmax(net1)} = V_{cmin}e^{-\frac{t_c}{T_c}} + \left[\frac{1}{2}V_{in}\left(1 - e^{-\frac{t_c}{T_c}}\right)\right] \quad \text{(A1.4)},$$

$$V_{cmin(net1)} = V_{cmax}e^{-\frac{t_d}{T_d}} + [(V_o)\left(1 - e^{-\frac{t_d}{T_d}}\right)] \quad \text{(A1.5).}$$

The output current is denoted as *Io*. The total amount of charge for steady state charging and discharging voltage-time for Normal mode ΔQ_{Normal} is $\frac{I_0}{2\,f_s}$ and solve together with; Equation. (A1.2) and Equation. (A1.3) give Equation. (A1.6, and solving Equation. (A1.4) and Equation. (A1.5) give Equation. (A1.7)

$$V_{boost\_Norm} = \frac{3}{2}V_{in} - \frac{Io\_boost}{2\,f_sC_p}\left(\frac{1}{1-e^{-\frac{t_d}{T_d}}} + \frac{1}{1-e^{-\frac{t_c}{T_c}}} - 1\right) \quad \text{(A1.6)}$$

$$V_{buck\_Norm} = \frac{1}{2}V_{in} - \frac{Io\_buck}{2\,f_sC_p}\left(\frac{1}{1-e^{-\frac{t_d}{T_d}}} + \frac{1}{1-e^{-\frac{t_c}{T_c}}} - 1\right) \quad \text{(A1.7)}$$

A1.1.2. Power losses and Efficiency of Normal Mode

The conduction power loss can deviate from the V_{out} and V_{in} relation of Equation. (A1.6) and Equation. (A1.7) are described as

$$P_{conduct\_Mode} = \frac{I^2_{o\_boost,buck}}{2\,f_sC_p}\left(\frac{1}{1-e^{-\frac{t_c}{T_c}}} + \frac{1}{1-e^{-\frac{t_d}{T_d}}} - 1\right) \quad \text{(A1.8)}$$

Where $T_d = \tau_d = R_{on\_discharge}C_p$ and $T_c = \tau_c = R_{on\_charge}C_p$. This is because R_{on} is turn on resistance along the path of charging and discharging, and C_p is much larger than capacitance of individual CMOS switches. Followed by R_{on} values for charging and discharging are recorded in from simulation for Normal mode operation.

Simulated result of output currents for Normal mode are $I_{out_boost} = 2.94 \times 10^{-5}$A and $I_{out_buck} = 9.36 \times 10^{-6}$A, f_s=588.23 kHz, $t_c = t_d = 1.7$ µs, and $T_c = T_d = R_{on\_charge}C_p = 331.2 \times 1 \times 10^{-9}$ and $R_{on\_discharge}C_p = 469.67 \times 1 \times 10^{-9}$ are inserted into Equation. (A1.8) resulted in-

$$P_{cond\_Norm\_boost} = \frac{\left(2.94 \times 10^{-5}\right)^2}{2\times588.23\times10^3\times1\times10^{-9}}\left(\frac{1}{1-e^{-\frac{1.7\times10^{-6}}{331.2\times1\times10^{-9}}}} + \frac{1}{1-e^{-\frac{1.7\times10^{-6}}{469.67\times1\times10^{-9}}}} - 1\right) = 0.759\times10^{-6}\text{W}$$

$$P_{cond\_Norm\_buck} = \frac{\left(9.36 \times 10^{-6}\right)^2}{2\times588.23\times10^3\times1\times10^{-9}}\left(\frac{1}{1-e^{-\frac{1.7\times10^{-6}}{331.2\times1\times10^{-9}}}} + \frac{1}{1-e^{-\frac{1.7\times10^{-6}}{469.67\times1\times10^{-9}}}} - 1\right) = 0.077\times10^{-6}\text{W}.$$

The total conduction power loss for Normal mode is $P_{cond\_Norm\_total} = 1.154 \times 10^{-6}$. Furthermore, charge-discharge mechanisms of a gate-source parasitic capacitance of MOSFET transistors (C_{gs}), the frequency of switching (f_s) and the gate-source voltages (V_{gs}) of individual switches along the path (i) dominate the switching power losses [152] and for this proposed methodology-

$$P_{sw\_Mode(boost,buck)} = f_s\sum_i C_{gsi}V^2_{gsi} \cong f_sC_{OX}\sum_i W_iL_iV^2_{gsi} \quad \text{(A1.9)}$$

where (W_i, L_i) are width and length of individual transistors along the path of operations and in this design length of transistor is kept to minimum value 180nm and width for PMOS being 60 µm and NMOS being 20 µm are used. The gate-oxide capacitor of the transistor (C_{ox}) in 0.18 um technology is approximately 8.31f F/µm². For PMOS V_{gs}=V_s=1V and NMOS V_{gs}= V_g=1.8V. Since the circuit is designed to have symmetric nature, taking phase1 as an example, the total switching power losses of boost and buck outputs for Normal mode give-

$$P_{sw_{Norm(boost)}} = f_sC_{OX}\left(W_{Mp4+Mp1}L_{Mp4+Mp1}V^2_{gsMp4+Mp1} + W_{t1}L_{t1}V^2_{gst1} + W_{Mn2}L_{Mn2}V^2_{gsMn2} + W_{O1+O4}L_{O1+O4}V^2_{gsO1+O4}\right) \quad \text{(A1.10)}$$

$$= f_sC_{OX}\left(\begin{matrix}2\,W_pL_pV^2_{gs} + W_pL_pV^2_{gs} + W_pL_pV^2_{gs} + W_nL_nV^2_{gs} + W_nL_nV^2_{gs} \\ +W_pL_p(\frac{3}{2})^2 + W_pL_p(\frac{1}{2})^2\end{matrix}\right)$$

$$= f_s C_{OX} \begin{pmatrix} 2 \times 60\mu \times 180\mu \times 1^2 + 60\mu \times 180\mu \times \left(\frac{1}{2}\right)^2 + 60\mu \times 180\mu \times 1.8^2 \\ +20\mu \times 180\mu \times 1.8^2 + 20\mu \times 180\mu \times 1.8^2 \\ +60\mu \times 180\mu \times (\frac{3}{2})^2 + 60\mu \times 180\mu \times (\frac{1}{2})^2 \end{pmatrix}$$

$$= 4.88 \times 10^{-9} \times 7.4628 \times 10^{-11} = 3.641 \times 10^{-19} \text{ W.}$$

$$P_{sw_{Norm(buck)}} = f_s C_{OX}\left(W_{O4} L_{O4} V_{gsO4}^2 + W_{Mn3} L_{Mn3} V_{gsMn3}^2\right) \quad \text{(A1.11)}$$

$$= f_s C_{OX}\left(W_p L_p V_{gs}^2 + W_n L_n V_{gs}^2\right)$$

$$= f_s C_{OX}\left(60\mu \times 180\mu \times (\tfrac{1}{2})^2 + 20\mu \times 180\mu \times 1.8^2\right)$$

$$= 4.88 \times 10^{-9} \times 1.1664 \times 10^{-11} = 7.011 \times 10^{-20} \text{ W.}$$

Therefore, the total switching power loss of normal mode $\mathrm{P_{sw_{Norm(total)}}} = 4.3411 \times 10^{-19}$ W. The redistribution power loss of Normal mode is derived as

$$P_{redis\_norm} = I_{out}^2 \frac{T_s}{4C_a} + I_{out}^2 \frac{T_s}{8(C_a + C_{out})} \quad \text{(A1.12).}$$

The $I_{out_boost} = 2.94 \times 10^{-5}$A and $I_{out_buck} = 9.36 \times 10^{-6}$A, $\frac{T_s}{4} = 1.7$ µs, $C_a = 1\,nF$ and $C_{out} = 1\,pF$. Insert these values into Equation. (A1.12)-

$P_{redis\_Norm\_boost} = 1.46 \times 10^{-6} + 7.339 \times 10^{-7} = 2.1939 \times 10^{-6}$ W and

$P_{redis\_Norm\_buck} = 1.489 \times 10^{-7} + 7.439 \times 10^{-8} = 2.2329 \times 10^{-7}$ W.

The total power loss for redistribution loss for Normal mode is $P_{redis\_Norm\_total} = 2.41 \times 10^{-6}\,W$.The average output power of for normal mode operation for boost and buck outputs are

$P_{out1avg_{Norm(boost)}} = V_{avg1} \times I_{avg1} = 1.494 \times 2.94 \times 10^{-5} = 4.39 \times 10^{-5}$ W and

$P_{out2avg_{Norm(buck)}} = V_{avg2} \times I_{avg2} = 0.467 \times 9.36 \times 10^{-6} = 4.37 \times 10^{-6}$ W respectively.

Therefore, total average power for Normal mode is $P_{outtotalavg_{Norm}} = 4.827 \times 10^{-5}\,W$. The other power losses influencing final outputs -the input power loss from source $P_{inlos_{Normal}} = 485.7 \times 10^{-6} W$, and the power loss from digital modules $P_{dig_{Normal}} = 80.82 \times 10^{-6}\,W$ are recorded from the simulation.

Lastly, the efficiencies of dual outputs for all modes can be calculated as such by taking the percentage of simulated output power divided by the sum of the input power.

$$\eta_{Mode_{boost,buck}} = \frac{P_{Mode_{boost,buck}} \times 100\%}{P_{inlos_{Mode}} + P_{dig_{Mode}}} \quad \text{(A1.13)}$$

Thus, the efficiency of normal mode can be calculated as-

$$\eta_{Normal_{total}} = \frac{4.39 \times 10^{-5} \times 100\%}{48.57 \times 10^{-5} + 8.082 \times 10^{-5}} = 85.257\%.$$

A1.2. High Mode Analysis

A.1.2.1. Output Voltages of High Mode

Correspondingly ΔQ_{High} for High mode is $\frac{I_0}{3\,f_s}$ for a charging phase, see Fig. A.1.2(a), final charging voltage $V_c(t)$ is equal to V_{cmax} and initial voltage $V_c(0)$ will be V_{cmin}. Since it is charging towards $(V_{in}\text{-}V_o)$, V_{in} from Equation. (A1.1) can be replaced and enhanced the Equation. (A1.14) is formed. The discharge phase, final voltage is V_{cmin}, initial voltage is V_{cmax} and hence V_{in} from Equation. (A1.1) can be replaced with $V_o - V_{in}$ produces Equation. (A1.15).

$$V_{cmax(net0)} = V_{cmin}e^{-\frac{t_c}{T_c}} + [(V_{in} - V_o)\left(1 - e^{-\frac{t_c}{T_c}}\right)] \quad \text{(A1.14)},$$

$$V_{cmin(net0)} = V_{cmax}e^{-\frac{t_d}{T_d}} + [(V_o - V_{in})\left(1 - e^{-\frac{t_d}{T_d}}\right)] \quad \text{(A1.15)}.$$

Same concept can be applied to Net1 in Fig. A1.2(b), derived Equation. (A1.6) and Equation. (A1.7).

$$V_{cmax(net1)} = V_{cmin}e^{-\frac{t_c}{T_c}} + [V_{in}\left(1 - e^{-\frac{t_c}{T_c}}\right)] \quad \text{(A1.6)},$$

$$V_{cmin(net1)} = V_{cmax}e^{-\frac{t_d}{T_d}} + [(V_o - V_{in})\left(1 - e^{-\frac{t_d}{T_d}}\right)] \quad \text{(A1.7)}.$$

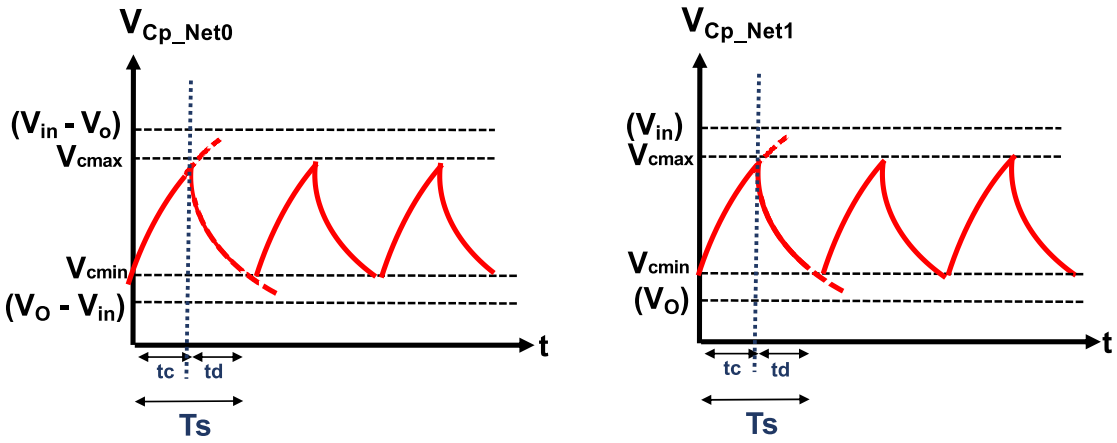


Figure A1. 2. Charging and discharging characteristic graph of capacitor in (a) Net0 boost conversion and (b) Net1 1:1 conversion in High Mode.

Inserting ΔQ_{High} value into Equation. (A1.14) and Equation (A1.15) together yields Equation. (A1.18). Similarly, ΔQ_{High} value into Equation. (A1.16) and Equation (A1.17) produces Equation. (A1.19).

$$V_{boost\_High} = 2V_{in} - \frac{Io\_boost}{3\,f_s C_p}\left(\frac{1}{1-e^{-\frac{t_d}{T_d}}} + \frac{1}{1-e^{-\frac{t_c}{T_c}}} - 1\right) \quad \text{(A1.18)}$$

$$V_{buck\_High} = V_{in} - \frac{Io\_buck}{3\,f_s C_p}\left(\frac{1}{1-e^{-\frac{t_d}{T_d}}} + \frac{1}{1-e^{-\frac{t_c}{T_c}}} - 1\right) \quad \text{(A1.19)}$$

A1.2.2. Power losses and Efficiency of Normal Mode

$$P_{conduct\_High} = \frac{I_{o\_boost,buck}^2}{3\, f_s C_p}\left(\frac{1}{1-e^{-\frac{t_d}{T_d}}} + \frac{1}{1-e^{-\frac{t_c}{T_c}}} - 1\right) \quad \text{(A1.20)}$$

Simulated result of output currents High mode are $I_{out_boost} = 3.92 \times 10^{-5}$A and $I_{out_buck} = 1.96 \times 10^{-5}$A, f_s=666.66 kHz, $t_c = t_d = 1.5$ µs, and $T_c = T_d = R_{on\_charge}C_p = 663.4 \times 1 \times 10^{-9}$ and $R_{on\_discharge}C_p = 593.29 \times 1 \times 10^{-9}$ are inserted into Equation. (A1.20) resulted in-

$$P_{cond\_High\_boost} = \frac{\left(3.92 \times 10^{-5}\right)^2}{3\times 666.66\times 10^3 \times 1\times 10^{-9}}\left(\frac{1}{1-e^{-\frac{1.5\times 10^{-6}}{663.4\times 1\times 10^{-9}}}} + \frac{1}{1-e^{-\frac{1.5\times 10^{-6}}{593.29\times 1\times 10^{-9}}}} - 1\right) = 0.9239 \times 10^{-6}\text{W}$$

$$P_{cond\_High\_buck} = \frac{\left(1.96 \times 10^{-5}\right)^2}{3\times 666.66\times 10^3 \times 1\times 10^{-9}}\left(\frac{1}{1-e^{-\frac{1.5\times 10^{-6}}{663.4\times 1\times 10^{-9}}}} + \frac{1}{1-e^{-\frac{1.5\times 10^{-6}}{593.29\times 1\times 10^{-9}}}} - 1\right) = 0.231 \times 10^{-6}\text{W}$$

The total conduction power loss for High mode is $P_{cond\_High\_total} = 1.154 \times 10^{-6}$.The charging time (*td* and *tc*) are the total switching time of charging and discharging. Moreover, R-C time constant (*Td* and *Tc*) are dominated by on-resistance along the path of charging-discharging Ron, and flying capacitor *Cp*, as it is larger than the capacitance of individual switches. Furthermore, charge-discharge mechanisms of a gate-source parasitic capacitance of MOSFET transistors (*Cgs*), the frequency of switching (*fs*) and the gate-source voltages (*Vgs*) of individual switches along the path dominate the switching power losses [152] and for this proposed methodology-

$$\begin{aligned} P_{sw_{High(boost)}} &= f_s C_{OX}\left(W_{Mp6+Mp0+Mp1}L_{Mp6+Mp0+Mp1}V_{gsMp6+Mp0+Mp1}^2 + W_{O3}L_{O3}V_{gsO3}^2 + W_{Mn0+Mn1}L_{Mn0+Mn1}V_{gsMn0+Mn1}^2\right) \quad \text{(A1.21)} \\ &= f_s C_{OX}\begin{pmatrix} 3\, W_p L_p V_{gs}^2 + W_p L_p (2)^2 \\ +2\, W_n L_n (1.8)^2 \end{pmatrix} \\ &= f_s C_{OX}\begin{pmatrix} 3\ \times 60\mu \times 180\mu \times 1^2 + \ 60\mu \times 180\mu \times (2)^2 \\ +2 \times 20\mu \times 180\mu \times 1.8^2 \end{pmatrix} \\ &= 5.539 \times 10^{-9} \times 9.88 \times 10^{-11} = 5.4 \times 10^{-19}\text{W} \end{aligned}$$

$$\begin{aligned} P_{sw_{High(buck)}} &= f_s C_{OX}\left(W_{O4}L_{O4}V_{gsO4}^2 + W_{Mn3}L_{Mn3}V_{gsMn3}^2\right) \quad \text{(A1.22)} \\ &= f_s C_{OX}\left(W_p L_p V_{gs}^2 + W_n L_n V_{gs}^2\right) \\ &= f_s C_{OX}\left(60\mu \times 180\mu \times (\tfrac{1}{2})^2 + 20\mu \times 180\mu \times 1.8^2\right) \\ &= 5.539 \times 10^{-9} \times 2.196 \times 10^{-11} = 1.244 \times 10^{-19}\text{W}. \end{aligned}$$

Therefore, the total switching power loss of normal mode $P_{sw_{High(total)}} = 6.714 \times 10^{-19}$ W.

The redistribution power loss of High mode is derived as

$$P_{redis\_high} = I_{out}^2 \frac{T_s}{4C_a} + I_{out}^2 \frac{T_s}{8(C_a + C_{out})} \quad \text{(A1.23)}$$

The $I_{out_boost} = 3.92 \times 10^{-5}$A, $I_{out_buck} = 1.96 \times 10^{-5}$A, $\frac{T_s}{4} = 1.5$ µs, $C_a = 1\,nF$ and $C_{out} = 1\,pF$. Insert these values into Equation. (A1.23)-

$P_{redis\_High\_boost} = 2.304 \times 10^{-6} + 1.151 \times 10^{-6} = 3.454 \times 10^{-6}$ W and

$P_{redis\_High\_buck} = 5.762 \times 10^{-7} + 2.878 \times 10^{-7} = 8.63 \times 10^{-7}$ W.

The total power loss for redistribution loss for High mode is $P_{redis\_High\_total} = 4.317 \times 10^{-6}\, W$. The average output power of for High mode operation for boost and buck outputs are

$P_{out1avg_{High(boost)}} = V_{avg1} \times I_{avg1} = 1.905 \times 3.92 \times 10^{-5} = 7.69 \times 10^{-5}$ W and

$P_{out2avg_{High(buck)}} = V_{avg2} \times I_{avg2} = 0.98 \times 1.96 \times 10^{-6} = 1.93 \times 10^{-5}$ W respectively.

The total average power for High mode is $P_{outtotalavg_{High}} = 9.62 \times 10^{-5}\, W$. The input power loss is simulated $P_{inlos_{High}} = 104 \times 10^{-6} W$, and the digital modules $P_{dig_{Normal}} = 27.99 \times 10^{-6}\, W$.

Thus, total efficiency of High mode can be calculated as-

$$\eta_{High_{total}} = \frac{9.62\times10^{-5} \times 100\%}{10.4\times10^{-6}+27.99\times10^{-6}} = 72.884\%.$$

Moreover, the efficiency of the charge pump alone without having considered the digital power loss is noted 68.38% and without both input power loss and the digital loss is observed 94.6%. The overall efficiency value including the power losses at the digital modules is 67.6% for High mode.

A1.3. Double Boost Analysis

A1.3.1. Output Voltages of Double Boost Mode

The total amount of charge for steady state charging and discharging voltage-time for Double Boost ΔQ_{Double} is $\frac{I_0}{4\, f_s}$. Following the same concept from previous modes and applied it into the Fig. A1.1, the Equation (A1.24) and Equation (A1.25) can be derived for both Net0 and Net1 respectively.

$$V_{cmax(net0)} = V_{cmin} e^{-\frac{t_c}{T_c}} + [(V_{in} - V_o)\left(1 - e^{-\frac{t_c}{T_c}}\right)] \quad \text{(A1.24)},$$

$$V_{cmin(net0)} = V_{cmax} e^{-\frac{t_d}{T_d}} + [(V_o - V_{in})\left(1 - e^{-\frac{t_d}{T_d}}\right)] \quad \text{(A1.25)}.$$

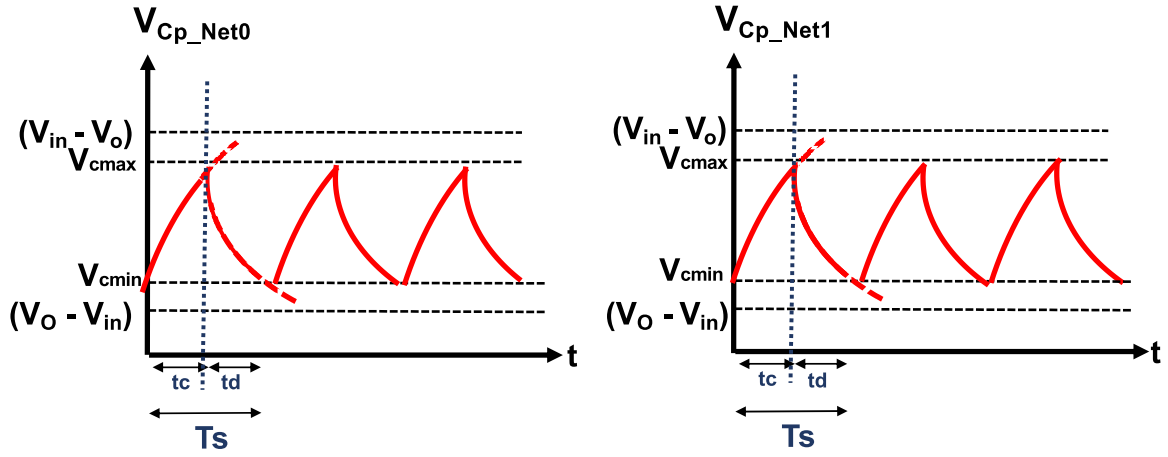


Figure A1. 3. Charging and discharging characteristic graph of capacitor in (a) Net0 boost conversion and (b) Net1 boost conversion in Double Boost Mode.

Thus, solving ΔQ_{Double} , Equation.(A1.24) and Equation.(A1.25) results in-

$$V_{boost_{Double}(out1,out2)} = 2\, V_{in} - \frac{Io\_boost}{3\, f_s C_p}\left(\frac{1}{1-e^{-\frac{t_d}{T_d}}} + \frac{1}{1-e^{-\frac{t_c}{T_c}}} - 1\right) \quad \text{(A1.26)}$$

A1.3.2 Power losses and Efficiency of Double Boost Mode

Hence Power loss for Double Boost mode can be derived as-

$$P_{conduct\_Double} = \frac{I_{o\_boost,buck}^2}{4\, f_s C_p} \left(\frac{1}{1-e^{-\frac{t_d}{T_d}}} + \frac{1}{1-e^{-\frac{t_c}{T_c}}} - 1\right) \quad \text{(A1.27)}$$

Simulated result of output current of Double Boost is $I_{out_double} = 3.94 \times 10^{-5}$A, f_s=1.1 MHz, $t_c = t_d = 900$ ns, and $\mathrm{T_c} = \mathrm{T_d} = \mathrm{R_{on\_charge}C_p} = 665.8 \times 1 \times 10^{-9}$ and $R_{on\_discharge}C_p = 693.22 \times 1 \times 10^{-9}$ are inserted into Equation. (A1.27) resulted in-

$$P_{conduction\_Double} = \frac{2\times(3.94\times10^{-5})^2}{4\times1.1\times10^6\times1\times10^{-9}} \left(\frac{1}{1-e^{-\frac{900\times10^{-9}}{665.8\times1\times10^{-9}}}} + \frac{1}{1-e^{-\frac{900\times10^{-9}}{693.22\times1\times10^{-9}}}} - 1\right) = 1.216\times10^{-6}\text{W}.$$

Furthermore, switching loss for Double Boost mode can be derived as -

$$P_{sw_{Double}} = 2\times f_s C_{OX}\left(W_{Mp0+Mp5}L_{Mp0+Mp5}V_{gsMp0+Mp5}^2 + W_{O2}L_{O2}V_{gsO2}^2 + W_{Mn0}L_{Mn0}V_{gsMn0}^2\right) \quad \text{(A1.28)}$$

$$= 2\times f_s C_{OX}\begin{pmatrix} 2\,W_pL_pV_{gs}^2 + W_pL_p(2)^2 \\ + W_nL_n(1.8)^2 \end{pmatrix}$$

$$= 2\times f_s C_{OX}\begin{pmatrix} 2\times 60\mu\times180\mu\times1^2 + 60\mu\times180\mu\times(2)^2 \\ +20\mu\times180\mu\times1.8^2 \end{pmatrix}$$

$$= 1.828\times10^{-8}\times7.6464\times10^{-11} = 1.3977\times10^{-18}\text{W}.$$

Therefore, the total switching power loss of Double Boost mode $\mathrm{P_{sw_{Double(total)}}} = 1.3977\times10^{-18}$ W.

Moreover, the redistribution power loss of High mode is derived as

$$\mathrm{P_{redis\_double}} = \mathrm{I_{out}^2}\frac{\mathrm{T_s}}{4\mathrm{C_a}} + \mathrm{I_{out}^2}\frac{\mathrm{T_s}}{8(\mathrm{C_a}+\mathrm{C_{out}})} \quad \text{(A1.29)}$$

The $I_{out_boost} = 3.92\times10^{-5}$A, $I_{out_buck} = 1.96\times10^{-5}$A, $\frac{T_s}{4} = 900$ ns, $C_a = 1\,nF$ and $C_{out} = 1\,pF$. Insert these values into Equation. (A1.29)-

$P_{redis\_double1,2} = 2\times(1.39\times10^{-6} + 6.97\times10^{-7}) = 4.188\times10^{-6}\,W$.

The total average output power of for Double mode is

$P_{outavg_{Double}} = 2\times V_{avg1}\times I_{avg1} = 2\times1.97\times3.94\times10^{-5} = 1.56\times10^{-4}$ W.

It was observed that since output1 and output2 are the same for the double mode due to symmetry of the circuit design and thus total power losses can be obtained by multiplying with 2 in the calculation. The input power loss is simulated $P_{inlos_{Double}} = 1.071\times10^{-4}W$, and the digital modules $P_{dig_{Double}} = 1.84\times10^{-4}\,W$. Finally, the efficiency of Double Boost mode output can be calculated as-

$$\eta_{Double_{1,2}} = \frac{1.56\times10^{-4}\times100\%}{1.84\times10^{-4}+1.071\times10^{-4}} = 53.6\%.$$

A1.4. Super Boost analysis

A1.4.1. Output Voltages of Super Boost

The total amount of charge for steady state charging and discharging voltage-time for Super Boost ΔQ_{Normal} is $\frac{I_0}{2\,f_s}$. According to the Fig. A1.1. V_{cmax} and V_{cmin} of both Net0 and Net1 can be derived into-

$$V_{cmax(net0)} = V_{cmin}e^{-\frac{t_c}{T_c}} + [(V_{in} - V_o)\left(1 - e^{-\frac{t_c}{T_c}}\right)] \quad \text{(A1.30)},$$

$$V_{cmin(net0)} = V_{cmax}e^{-\frac{t_d}{T_d}} + [(V_o - V_{in})\left(1 - e^{-\frac{t_d}{T_d}}\right)] \quad \text{(A1.31)}.$$

$$V_{cmax(net1)} = V_{cmin}e^{-\frac{t_c}{T_c}} + [V_{in}\left(1 - e^{-\frac{t_c}{T_c}}\right)] \quad \text{(A1.32)},$$

$$V_{cmin(net1)} = V_{cmax}e^{-\frac{t_d}{T_d}} + [(V_o - V_{in})\left(1 - e^{-\frac{t_d}{T_d}}\right)] \quad \text{(A1.33)}.$$

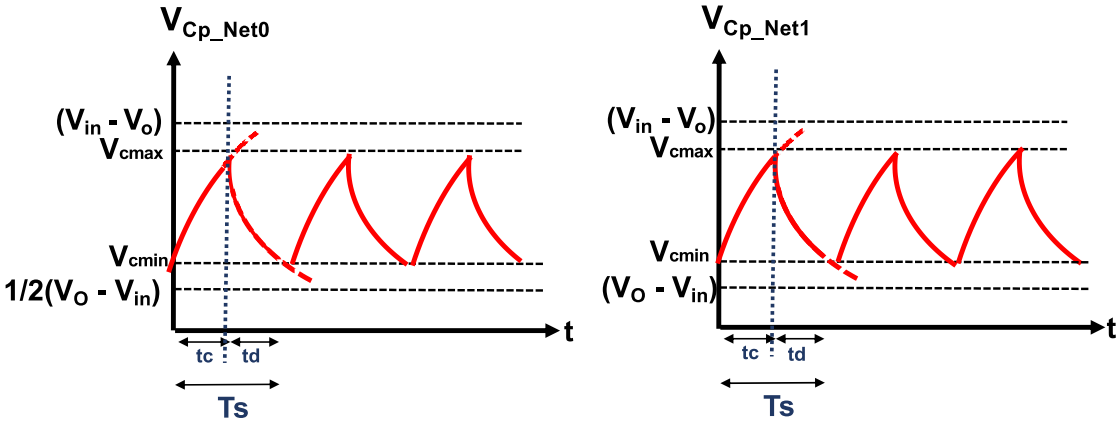


Figure A1.4. Charging and discharging characteristic graph of capacitor in (a) Net0 boost conversion and (b) Net1 boost conversion in Super Boost Mode.

Thus, Equation. (A1.34) and Equation.(A1.35) can be derived as-

$$V_{boost_{Super}(out1)} = 2\,V_{in} - \frac{Io\_boost1}{2\,f_s C_p}\left(\frac{1}{1-e^{-\frac{t_d}{T_d}}} + \frac{1}{1-e^{-\frac{t_c}{T_c}}} - 1\right) \quad \text{(A1.34)}$$

$$V_{boost_{Super}(out2)} = 3\,V_{in} - \frac{Io\_boost2}{2\,f_s C_p}\left(\frac{1}{1-e^{-\frac{t_d}{T_d}}} + \frac{1}{1-e^{-\frac{t_c}{T_c}}} - 1\right) \quad \text{(A1.35)}$$

A1.4.2. Power losses and Efficiency of Super Boost Mode

The conduction loss for Super boost mode is written as-

$$P_{conduct\_Super} = \frac{I_{o\_boost,buck}^2}{2\, f_s C_p} \left(\frac{1}{1-e^{-\frac{t_d}{T_d}}} + \frac{1}{1-e^{-\frac{t_c}{T_c}}} - 1\right) \quad \text{(A1.36)}$$

Simulated result of output currents Super boost mode are $I_{out\_boost1} = 5.71 \times 10^{-5}\text{A}$ and $I_{out\_boost2} = 3.78 \times 10^{-5}\text{A}$, f_s=2 MHz, $t_c = t_d = 500$ ns, and $T_c = T_d = R_{on\_charge}C_p = 364.97 \times 1 \times 10^{-9}$ and $R_{on\_discharge}C_p = 168.34 \times 1 \times 10^{-9}$ are inserted into Equation. (A1.36) resulted in-

$$P_{cond\_Super\_boost1} = \frac{(5.71 \times 10^{-5})^2}{2\times2\times10^6\times1\times10^{-9}} \left(\frac{1}{1-e^{-\frac{500\times10^{-9}}{364.97\times1\times10^{-9}}}} + \frac{1}{1-e^{-\frac{500\times10^{-9}}{168.34\times1\times10^{-9}}}} - 1\right) = 1.14 \times 10^{-6}\text{W}$$

$$P_{cond\_Super\_boost2} = \frac{(3.78 \times 10^{-5})^2}{2\times2\times10^6\times1\times10^{-9}} \left(\frac{1}{1-e^{-\frac{500\times10^{-9}}{364.97\times1\times10^{-9}}}} + \frac{1}{1-e^{-\frac{500\times10^{-9}}{168.34\times1\times10^{-9}}}} - 1\right) = 0.5013 \times 10^{-6}\text{W}.$$

The total conduction power loss for Super Boost mode is $\text{P}_{\text{cond\_Super\_total}} = 1.64 \times 10^{-6}$.

$$P_{sw_{Super(boost)}} = f_s C_{OX}\left(W_{Mp4+Mp1+Mp6}L_{Mp4+Mp1+Mp6}V_{gsMp4+Mp1+Mp6}^2 + W_{t1}L_{t1}V_{gst1}^2 + W_{Mn3+Mn1}L_{Mn3+Mn1}V_{gsMn3+Mn1}^2 + W_{O1+O3}L_{O1+O3}V_{gsO1+O3}^2\right) \quad \text{(A1.37)}$$

$$= f_s C_{OX}\begin{pmatrix} 3\, W_p L_p V_{gs}^2 + W_p L_p V_{gs}^2 + W_n L_n V_{gs}^2 + +2\, W_n L_n (1.8)^2 \\ +W_p L_p (2)^2 + W_p L_p (3)^2 \end{pmatrix}$$

$$= \text{f}_\text{s}\text{C}_\text{OX}\begin{pmatrix} 3 \times 60\mu \times 180\mu \times 1^2 + 60\mu \times 180\mu \times (2)^2 + 20\mu \times 180\mu \times 3.3^2 \\ +2 \times 20\mu \times 180\mu \times 3.3^2 + 60\mu \times 180\mu \times 2^2 + 60\mu \times 180\mu \times 3^2 \end{pmatrix}$$

$$= 1.662 \times 10^{-8} \times 3.336 \times 10^{-10} = 5.544 \times 10^{-18}\text{W}.$$

Therefore, the total switching power loss of Super boost mode is $\text{P}_{\text{sw}_{\text{Super(total)}}} = 5.544 \times 10^{-18}$ W.

The redistribution power loss of Super Boost mode is derived as

$$P_{redis\_Super} = I_{out}^2 \frac{T_s}{4C_a} + I_{out}^2 \frac{T_s}{8(C_a+C_j+C_{out})} \quad \text{(A1.38)}$$

The $I_{out\_boost1} = 5.71 \times 10^{-5}\text{A}$ and $I_{out\_boost2} = 3.78 \times 10^{-5}\text{A}$, $\frac{T_s}{4} = 500$ ns, $C_a = C_j = 1\,nF$ and $\text{C}_\text{out} = 1$ pF. Insert these values into Equation. (A1.38)-

$P_{redis\_Super\_out1} = 1.63 \times 10^{-6} + 4.073 \times 10^{-7} = 2.037 \times 10^{-6}\ W$ and

$P_{redis\_Super\_out2} = 7.1442 \times 10^{-7} + 1.785 \times 10^{-7} = 8.929 \times 10^{-7}\ W$.

The total power loss for redistribution loss for Super boost mode is $\text{P}_{\text{redis\_Super\_total}} = 2.929 \times 10^{-6}$ W. The average output power of for Super boost operation for boost1 and boost2 outputs are-

$P_{out1avg_{Super(boost1)}} = V_{avg1} \times I_{avg1} = 2.8525 \times 5.71 \times 10^{-5} = 1.63 \times 10^{-4}$ W and

$P_{out2avg_{Super(boost2)}} = V_{avg2} \times I_{avg2} = 1.8855 \times 3.78 \times 10^{-5} = 1.8855 \times 10^{-5}$ W respectively.

The total average power for High mode is $P_{outtotalavg_{Super}} = 2.34 \times 10^{-4}$ W. The input power loss is simulated $P_{inlos_{High}} = 3.34 \times 10^{-4} W$, and the digital modules $P_{dig_{Normal}} = 1.55 \times 10^{-4}$ W.

Finally, the efficiency of Double boost mode output can be calculated as-

$$\eta_{Super_{boost1}} = \frac{2.34\times10^{-4} \times 100\%}{3.34\times10^{-4}+1.55\times10^{-4}} = 47.85\%.$$

A1.5. Circuit Implantation and parameter sweeps

A1.5.1. Load Regulation (50k-1MΩ)of 4-phase converter

The analysis from the Fig.A1.5(a) can be deduced that- as the resistive load increase, the output voltage increases since increase in resistive value reduce the current sinking at load end. However, left network reaches to 1.92 V rather than intended 2V and thus there are some losses in the operation, see Fig.A1.5(b). This is tested with the W_p of output transistor=30 um, R_L=**50k-1M Ω**, F_{sw}=1/600n Hz, C_{load} =100 pF.

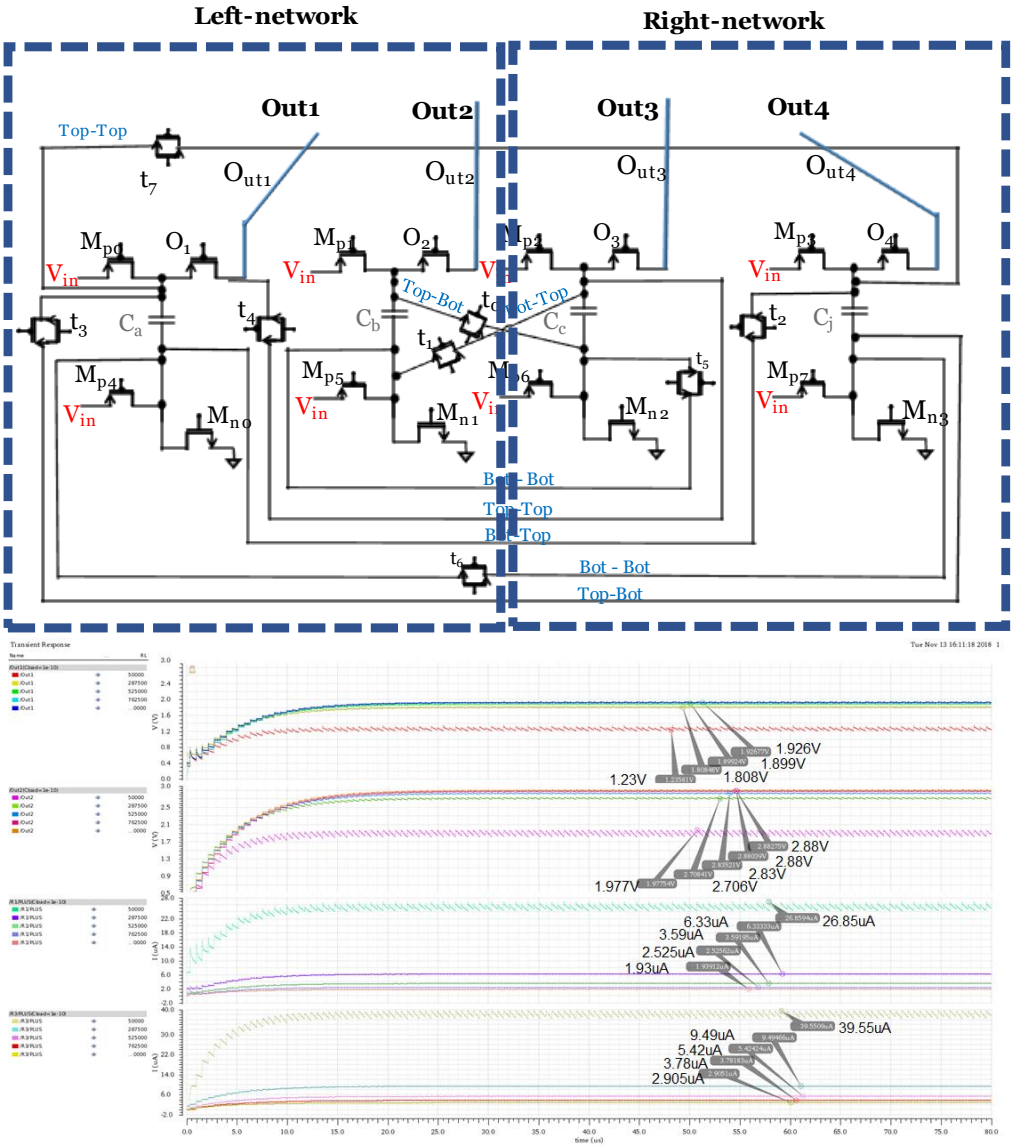


Figure A1.5. (a)Schematic of main charge pump and (b)Parametric Output voltage waveforms for varying load resistances in Super Boost mode.

A3.5.2. The Left network test only

To analyse the voltage losses in the previous observation, I have isolated the secondary capacitor changing in parallel to discharge at the load through Out1 in Fig.A1.6(a). The Wp=30 um, R_L=**500k-1M Ω**, Fsw=1/600n Hz, and Cload =100 pF.

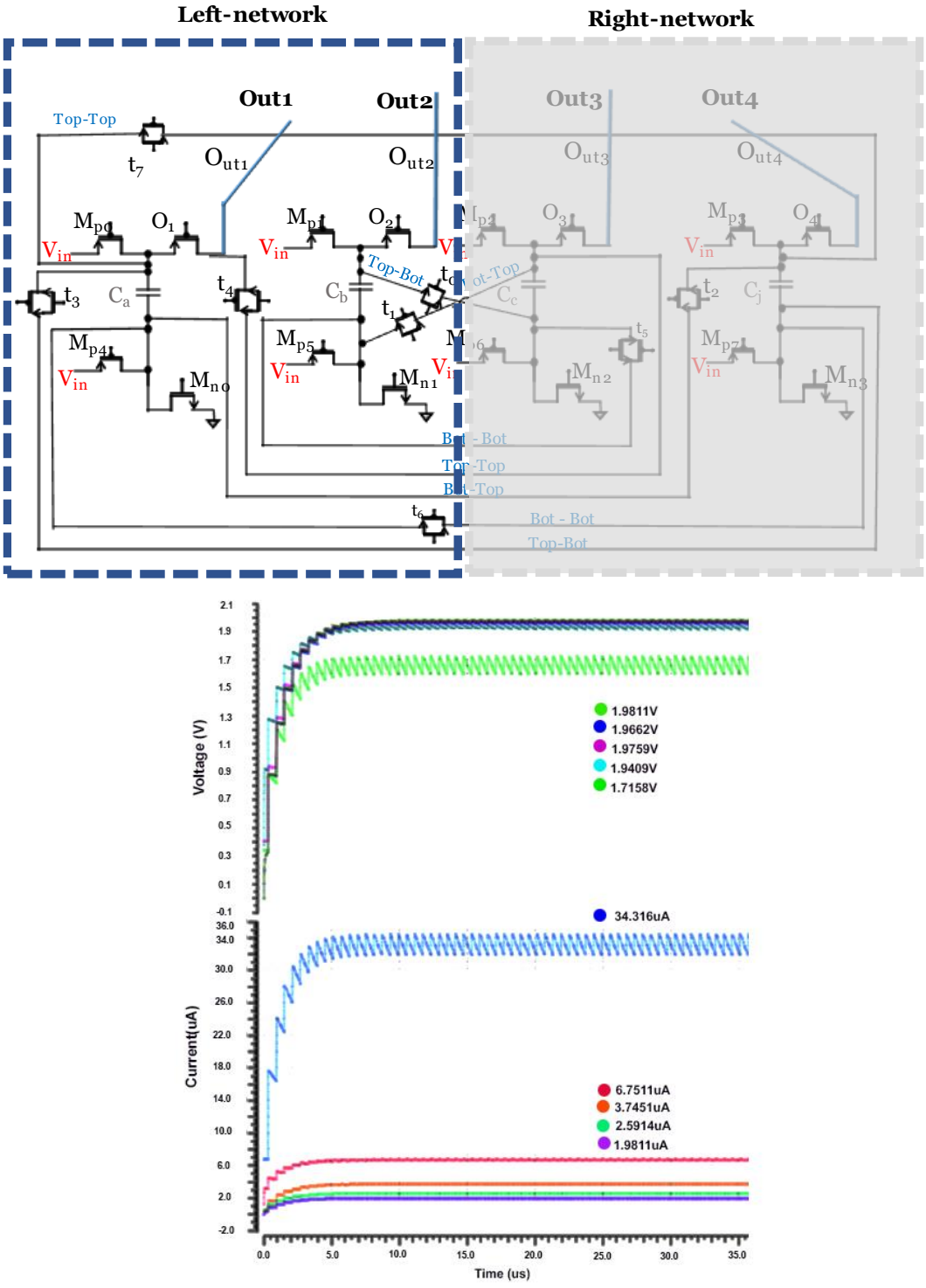


Figure A1.6. (a) Schematic of isolating first and second stage with no-connect device and (b) output waveforms for first stage output after isolating from second stage.

As the resistive load increase, the output voltage increases since current sinking at the load decreases. After isolating the first stage from the secondary charging stage, the output voltage is observed to become much closer to a target of 2V as shown in Fig A1.6(b).

A1.5.3. Varying width of size of the output transistor

The simulation is carried out to see whether conduction loss can be reduced by increasing the width of the output transistor. This is because to reduce current loss, I increase the width of the transistor on current paths and thus, the width changes from O1=30µm to 100µm. However, it has been observed that there is no significant change in the output. In addition, it has been discovered that there is a significant change, as depicted in Fig.A1.7. The W_p=**30µ-100µm**, R_L=500kΩ, F_{sw}=1/600nHz and C_{load} =100pF.

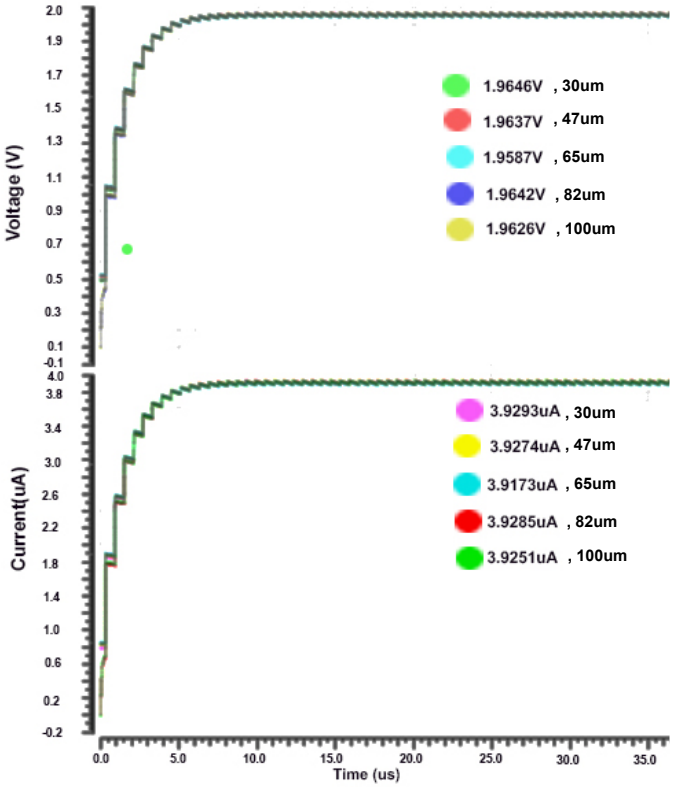


Figure A1.7.The parametric output voltage waveforms over the varying width of the transistor.

A1.5.4. Varying the operating frequency

The objective of this simulation is to observe the change of output voltage when there is a change in the operating frequencies. The frequency varies from **1/800ns – 1/90ns**, W_p=30µ, R_L=500k, F_{sw}=1/800n – 1/90ns and C_{load} =100p.

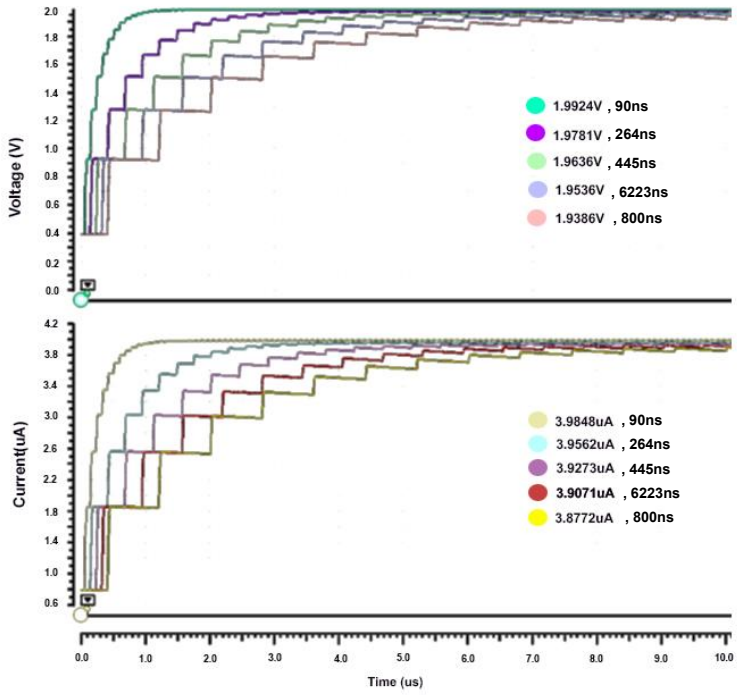


Figure A1.8. The parametric output voltage waveforms over the varying operating frequency.

As observed in Fig. A1.8, the increase in frequency help reach output voltage closer to the target voltage faster, in other word provides the faster transient response. This is beneficial for reducing the size of the charge pump and transient time. Now that all the variables in changing the output voltage are understood. Design parameters must adjust to fulfil the desire output specification around 2 V@10-20 µA.

A1.4.5. Illustrating performance of charge pump over variables

Change in parameter size of capacitor and frequency change is tested to observe the voltage and current characteristic. This simulation data is then recorded and plotted in Fig.A1.9(a-b). In order to reduce the chip area and I aim to achieve this proposed design suitable for low-power wearable applications. Therefore, as for the simulated sample data and for convenience of rescaling, if there are any changes require in the design process I-V characteristic when there is a change in important parameters is presented.

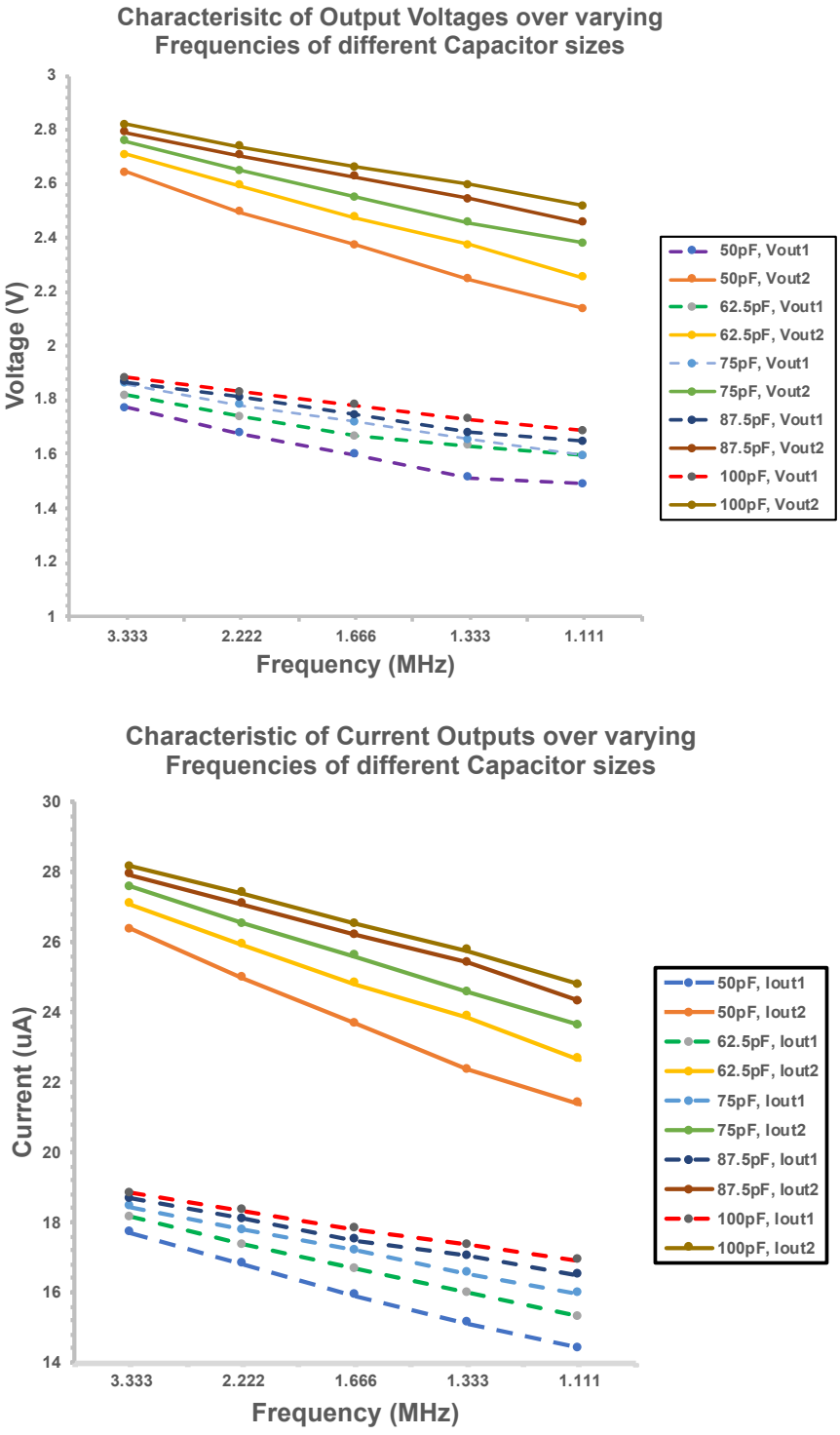


Figure A1.9. (a) ***Vout1, Vou2*** **(b)** ***Iout1, Iout2*** **at different capacitors values over varying frequencies.**

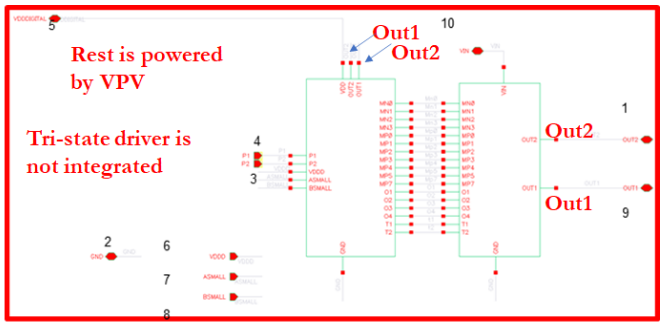
TABLE A1. 1. SIMULATED RESULT OF VARYING CAPACITOR, FREQUENCY AND OUTPUTS OF A 4-PHASE CONVERTER.

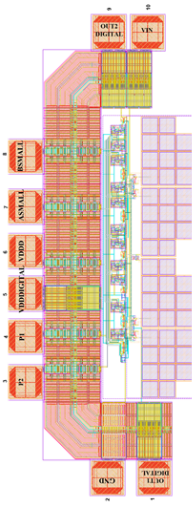
Cap (pF)	fsw (MHz)	Vout1 (V)	Iout1 (uA)	Vout2 (V)	Iout2 (uA)
50	3.333	1.7725	17.714	2.643	26.378
	2.222	1.6758	16.807	2.495	24.97
	1.666	1.5990	15.92	2.373	23.69
	1.333	1.5140	15.11	2.247	22.37
	1.111	1.4900	14.40	2.139	21.40
62.5	3.333	1.8166	18.15	2.707	27.07
	2.222	1.7385	17.37	2.592	25.92
	1.666	1.6679	16.67	2.476	24.81
	1.333	1.6315	15.98	2.374	23.87
	1.111	1.5957	15.31	2.253	22.64
75	3.333	1.8589	18.45	2.757	27.59
	2.222	1.7814	17.78	2.650	26.53
	1.666	1.7195	17.19	2.549	25.60
	1.333	1.6534	16.53	2.456	24.57
	1.111	1.5945	15.97	2.380	23.63
87.5	3.333	1.8660	18.67	2.790	27.91
	2.222	1.8114	18.09	2.704	27.07
	1.666	1.7447	17.49	2.624	26.21
	1.333	1.6783	17.03	2.544	25.42
	1.111	1.6467	16.48	2.456	24.31
100	3.333	1.8842	18.83	2.818	28.16
	2.222	1.8288	18.33	2.738	27.39
	1.666	1.7806	17.80	2.663	26.53
	1.333	1.7300	17.37	2.595	25.75
	1.111	1.6870	16.90	2.517	24.79

APPENDIX. 2: SINGLE-INPUT-DUAL-OUTPUTS (SIDO) AND SINGLE-INPUT-SINGLE-OUTPUT (SISO)WITH A PROPOSED 2-PHASE CHARGE PUMP.

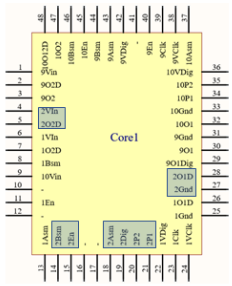
Appendix 2.1 : Experimental set up of 'feed-in' mode with external clock IC number 2 configuration from layout view to the lab environment.

2. Withfeedin_withoutclock





Layout



Wire-bonded PCB

1.	Out1DIGITAL	1.	2O1D
2.	GND	2.	2Gnd
3.	P2	3.	2P2
4.	P1	4.	2P1
5.	VDDDDIGITAL	5.	2Dig
6.	VDDD	6.	2En
7.	ASMALL	7.	2Asm
8.	BSMALL	8.	2Bsm
9.	OUT2	9.	2O1
10.	VIN	10.	2Vin
IC I/O name		Wire-bonded PCB name	

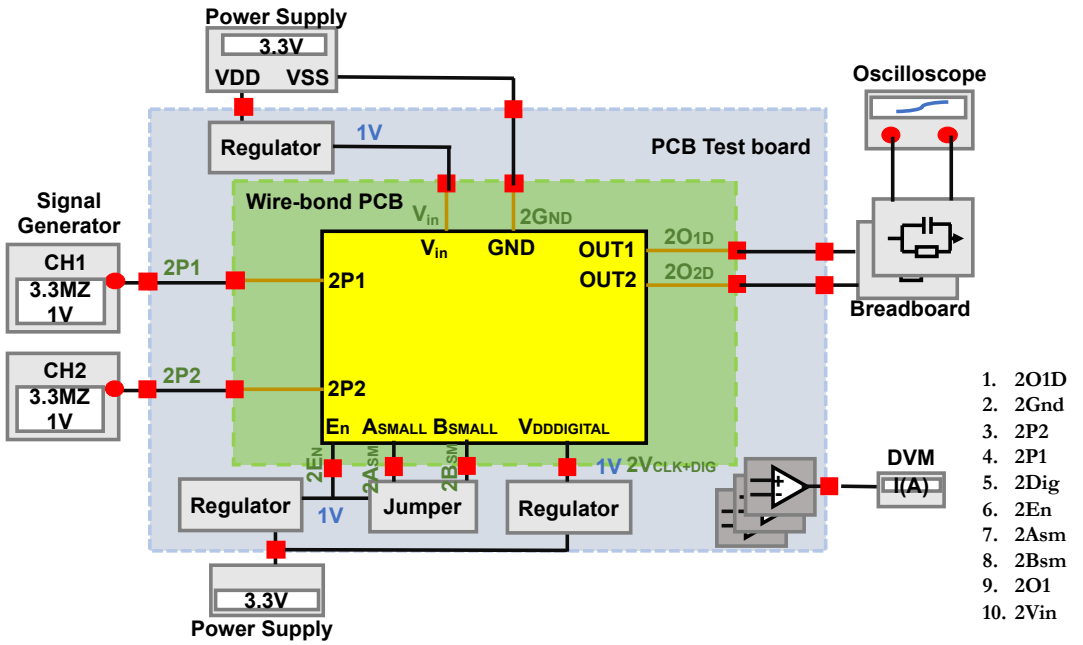
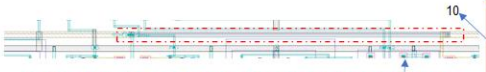


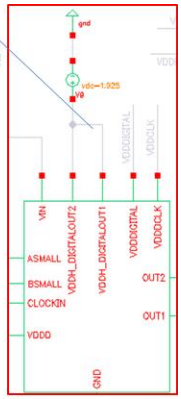
Figure A2. 1. Experimental set up of '*feed-in*' mode with external clock IC number 2 configuration from layout view to the lab environment.

Appendix 2.2 : Experimental set up of 'without feed-in (stand-alone)' mode with external clocks IC number 10 configuration from layout view to the lab environment.

10.Withoutfeedin_layoutwithIOPADDESIGN2_ withoutclock



Different from layoutwithIOPAD is Digital Out1 and Out2 is connected across M2-M5 via and M5 track and combine them as single IO –'OUT1AND2DIGITAL'

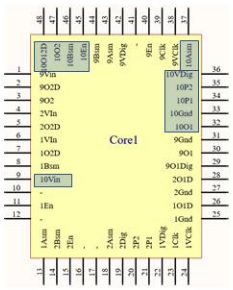


Same as chip no.9, without integrated tristate-driver

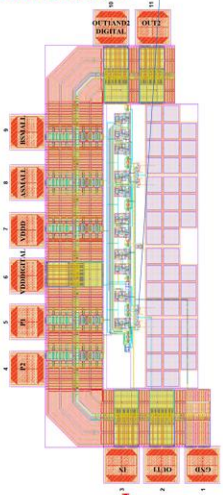
1. GND	1. 10Gnd (33)
2. OUT1	2. 10O1 (32)
3. IN	3. 10Vin (9)
4. P2	4. 10P2 (35)
5. P1	5. 10P1 (34)
6. VDDDDIGITAL	6. 10VDig (36)
7. VDDD	7. 10En (45)
8. ASMALL	8. 10Asm (37)
9. BSMALL	9. 10Bsm (46)
10. OUT1+OUT2Digital	10. 10O12D (48)
11. OUT2	11. 10O2 (47)

Wire-bonded PCB

IC I/O name



Wire-bonded PCB name



Layout

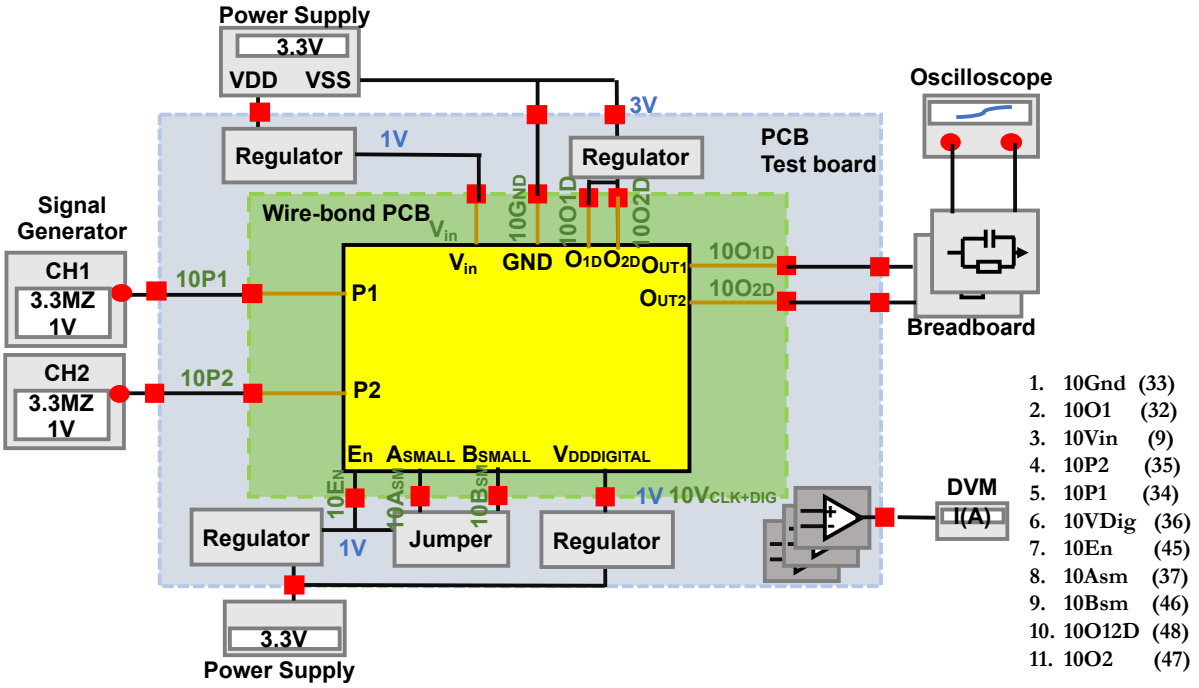


Figure A2. 2. Experimental set up of '*without feed-in (stand-alone)*' mode with external clock IC number 10 configuration from layout view to the lab environment.

Appendix 2.3 : Simulated output calculation in Cadence Virtuoso

The calculation of *Iin, Vin, Vout, Iout* and efficiency in cadence virtuoso.

Test	Name	Type	Details	EvalType	Plot	Save
PowerManagementContactlensLAYOUT:MainDCDCtopleveltest:1		signal	/I17/VDD	point	☑	☑
PowerManagementContactlensLAYOUT:MainDCDCtopleveltest:1		signal	/I0/VIN	point	☑	☑
PowerManagementContactlensLAYOUT:MainDCDCtopleveltest:1		signal	/I3/VDD	point	☑	☑
PowerManagementContactlensLAYOUT:MainDCDCtopleveltest:1		signal	/OUT2	point	☑	☑
PowerManagementContactlensLAYOUT:MainDCDCtopleveltest:1		signal	/OUT1	point	☑	☑
PowerManagementContactlensLAYOUT:MainDCDCtopleveltest:1	iinavg	expr	average(clip(IT("/I0/VIN") 9e-06 1e-05))	point	☑	☑
PowerManagementContactlensLAYOUT:MainDCDCtopleveltest:1	vout1	expr	average(clip(VT("/OUT1") 9e-06 1e-05))	point	☑	☑
PowerManagementContactlensLAYOUT:MainDCDCtopleveltest:1	vout2	expr	average(clip(VT("/OUT2") 9e-06 1e-05))	point	☑	☑
PowerManagementContactlensLAYOUT:MainDCDCtopleveltest:1	iout1	expr	VAR("iout1")	point	☑	☐
PowerManagementContactlensLAYOUT:MainDCDCtopleveltest:1	iout2	expr	VAR("iout2")	point	☑	☐
PowerManagementContactlensLAYOUT:MainDCDCtopleveltest:1	pin	expr	(iinavg * 1)	point	☑	☐
PowerManagementContactlensLAYOUT:MainDCDCtopleveltest:1	pout	expr	((vout1 * iout1) + (vout2 * iout2))	point	☑	☐
PowerManagementContactlensLAYOUT:MainDCDCtopleveltest:1	eff	expr	(pout / pin)	point	☑	☐

average(clip(IT("/I0/VIN") 9e-06 1e-05))
average(clip(VT("/OUT1") 9e-06 1e-05))
average(clip(VT("/OUT2") 9e-06 1e-05))
VAR("iout1")
VAR("iout2")
(iinavg * 1)
((vout1 * iout1) + (vout2 * iout2))
(pout / pin)

Appendix 2.4 : Post-layout simulation results

Feed-in				DB											SB								LP					HC			
Vin	1	1	1	1	1	1	1	1	1		1	1	1	1	1	1	1	1	1		1	1	1	1	1		1	1	1	1	1
Iinavg(u)	8.42	26.31	40.21	24.3	40.2	56.09	40.18	56.07	122.3		46.94	58.59	71.03	56.99	56.99	81.84	67.18	79.45	93.02		4.088	12.03	19.97	27.92	35.86		23.05	29.62	36.19	49.31	75.7
Vout1	1.976	1.976	1.975	1.89	1.89	1.89	1.8	1.8	1.593		1.815	1.799	1.78	1.744	1.744	1.705	1.67	1.65	1.624		1.975	1.933	1.889	1.845	1.8		-	-	-	-	-
Iout1(u)	0	0	0	8	8	8	16	16	16		0	0	0	8	8	8	16	16	16		0	4	8	12	16		-	-	-	-	-
Vout2	1.974	1.887	1.796	1.974	1.887	1.796	1.973	1.887	0.5293		2.594	2.538	2.474	2.578	2.578	2.45	2.562	2.499	2.422		-	-	-	-	-		3.558	3.443	3.324	3.078	2.517
Iout2(u)	0	8	16	0	8	16	0	8	16		0	8	16	0	8	16	0	8	16		-	-	-	-	-		0	2	4	8	16
Pout1(u)	0	0	0	15.12	15.12	15.12	28.8	28.8	25.488		0	0	0	13.952	13.952	13.64	26.72	26.4	25.984		0	7.732	15.112	22.14	28.8		-	-	-	-	-
Pout2(u)	0	15.096	28.736	0	15.096	28.736	0	15.096	8.4688		0	20.304	39.584	0	20.624	39.2	0	19.992	38.752		-	-	-	-	-		0	6.886	13.296	24.624	40.272
Pout_total(u)	0	15.096	28.736	15.12	30.216	43.856	28.8	43.896	33.9568		0	20.304	39.584	13.952	34.576	52.84	26.72	46.392	64.736		0	7.732	15.112	22.14	28.8		0	6.886	13.296	24.624	40.272
Pin	8.42	26.31	40.21	24.3	40.2	56.09	40.18	56.07	122.3		46.94	58.59	71.03	56.99	56.99	81.84	67.18	79.45	93.02		4.088	12.03	19.97	27.92	35.86		23.05	29.62	36.19	49.31	75.7
Eff	0	57.3774	71.4648	62.2222	75.1642	78.1886	71.6775	78.2879	27.7652		0	34.6544	55.7286	24.4815	60.6703	64.565	39.7737	58.3914	69.5936		0	64.2727	75.6735	79.298	80.3123		0	23.2478	36.7394	49.9371	53.1995

Stand-alone				DB											SB								LP					HC			
Vin	1	1	1	1	1	1	1	1	1		1	1	1	1	1	1	1	1	1		1	1	1	1	1		1	1	1	1	1
Iinavg(u)	2.492	18.01	33.57	17.97	33.49	49.05	33.49	49.01	64.57		13.15	36.47	59.82	28.78	52.09	75.43	44.4	67.7	91.04		1.599	9.573	17.54	25.51	33.48		24.41	27.4	30.61	38.98	68.34
Vout1	1.991	1.991	1.991	1.905	1.905	1.905	1.816	1.816	1.816		1.954	1.892	1.828	1.865	1.801	1.735	1.773	1.705	1.636		1.991	1.949	1.905	1.861	1.816		-	-	-	-	-
Iout1(u)	0	0	0	8	8	8	16	16	16		0	0	0	8	8	8	16	16	16		0	4	8	12	16		-	-	-	-	-
Vout2	1.995	1.908	1.818	1.995	1.908	1.818	1.994	1.908	1.818		2.916	2.764	2.604	2.854	2.699	2.535	2.791	2.633	2.464		-	-	-	-	-		3.574	3.529	3.48	3.342	2.772
Iout2(u)	0	8	16	0	8	16	0	8	16		0	8	16	0	8	16	0	8	16		-	-	-	-	-		0	2	4	8	16
Pout1(u)	0	0	0	15.24	15.24	15.24	29.056	29.056	29.056		0	0	0	14.92	14.408	13.88	28.368	27.28	26.176		0	7.796	15.24	22.332	29.056		-	-	-	-	-
Pout2(u)	0	15.264	29.088	0	15.264	29.088	0	15.264	29.088		0	22.112	41.664	0	21.592	40.56	0	21.064	39.424		-	-	-	-	-		0	7.058	13.92	26.736	44.352
Pout_total(u)	0	15.264	29.088	15.24	30.504	44.328	29.056	44.32	58.144		0	22.112	41.664	14.92	36	54.44	28.368	48.344	65.6		0	7.796	15.24	22.332	29.056		0	7.058	13.92	26.736	44.352
Pin	2.492	18.01	33.57	17.97	33.49	49.05	33.49	49.01	64.57		13.15	36.47	59.82	28.78	52.09	75.43	44.4	67.7	91.04		1.599	9.573	17.54	25.51	33.48		24.41	27.4	30.61	38.98	68.34
Eff	0	84.7529	86.6488	84.808	91.0839	90.3731	86.7602	90.4305	90.048		0	60.6307	69.6489	51.8416	69.1112	72.1729	63.8919	71.4092	72.0562		0	81.4374	86.8871	87.5421	86.7861		0	25.7591	45.4753	68.589	64.899

APPENDIX. 3: START-UP DC-DC CONVERTERS FOR POWER MANAGEMENT SYSTEM.

Appendix 3.1. The design of ultra-low input start-up charge pumps for energy harvesters.

Most biomedical devices are powered by a standard battery cell or renewable energy source to assist a battery. Implementing renewable energy as a power source to those devices is more attractive due to being clean energy, and energy can be harvested from day-to-day surroundings [22, 241]. Comparing with an alternative energy source, sunlight is omnipresent, reliable and renewable energy, which can also be harvested by the solar cell under the skin. To be specific, when implants with solar cell-powered are irradiated, the penetrated light, especially the invisible and Near-infrared region, will be converted into electricity and power the CMOS circuitry embedded in the same chip.

One example of power management circuits for a photovoltaic cell can be observed in [199]. The Dickson charge pump with the fast-transient response is compared with cross-coupled, which has high voltage conversion. However, a similar high voltage clock for the charge pump's partial stage has been presented in [103]. It modified Dickson charge pump NCP-3, which uses a high voltage clock generator and supply to the MOSFET controlled gate next to the output stage to eliminate threshold voltage losses. Assume such high voltage clocks are not external and consume primary energy sources rather than supply to the gate. Still, the capacitor would not have enough power to do so because the current gain is inversely proportional to the voltage gain in the Dickson Charge pump. Similarly, level shifting from output to control the gate of crossed couple switches has been presented in [40]. However, this is only to supply the neighbour transistor pairs' gate to eliminate reversion loss [149].

The output of the *PV* cell is too low to operate for the electronics module on chips. Hence mean of power management or power converter is necessary to supply the required power to the loads. The circuits presented in [24, 242] which power the peripheral part of the circuits such as the clock and digital circuits to make an operation of the converter possible by stacking additional *PV* cell. In all proposed designs, I aim to achieve the whole system to operate with just a photovoltaic energy source and less external input source as much as possible. This appendix focus on the start-up charge pumps design for the intended power management unit, as shown in Fig. A3.1.

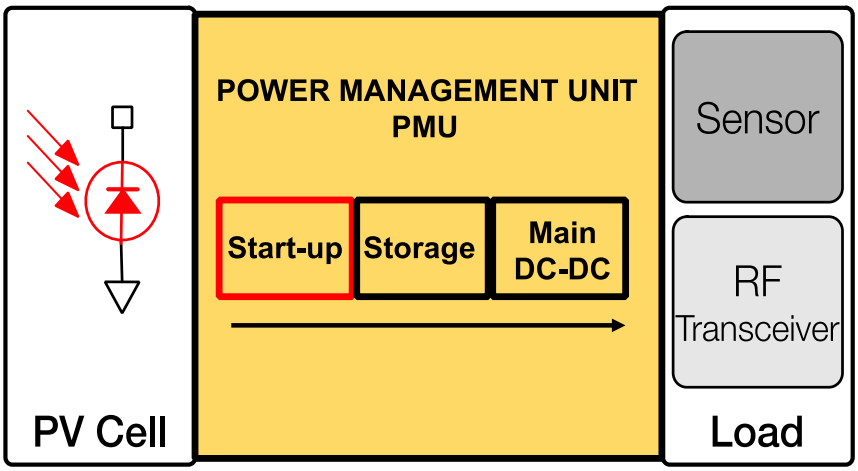


Figure A3. 1. The desire power management unit in which ultra-low input is harvested from the *PV* cell is a bridge towards the main DC-DC converter through start-up charge up.

In this Appendix, I will search for the start-up charge pump that can operate in ultra-low input from *PV* harvester and address the various potential losses to achieve the goal of 1V supply with voltage conversion efficiency close enough to targeted gain and provide high power efficiency to the main converter.

Appendix 3.3. Proposed design-1

Appendix 3.3.1. Background and motivation of design-1

The start-up charge pump proposed by B. Mohammadi in [165], with configurations suggested by the literature, is re-stimulated as depicted in Fig. A3.2. The central integral part of the start-up circuits are (1) the charge transfer switches (CTS) for transfer of charge between stage-0 to stage-2 controlled by the high voltage provided by the 'StartupOut', (2) two buffers switches which act as the level shifter by borrowing higher output voltage of the start-up charge pump to the gate of CTS PMOSs to eliminate reverse charge sharing, the output buffer (Outbuff) which is the consequence of clock blocker circuit enable same output as 'StartupOut' before external capacitor reach to desire threshold voltage, (3) two PMOS switches which give high impedance to CTS switches as the output get higher than VDD and (4) one NMOS switch which gate is controlled by 'Outbuff' to prevent leakage current at the ground path.

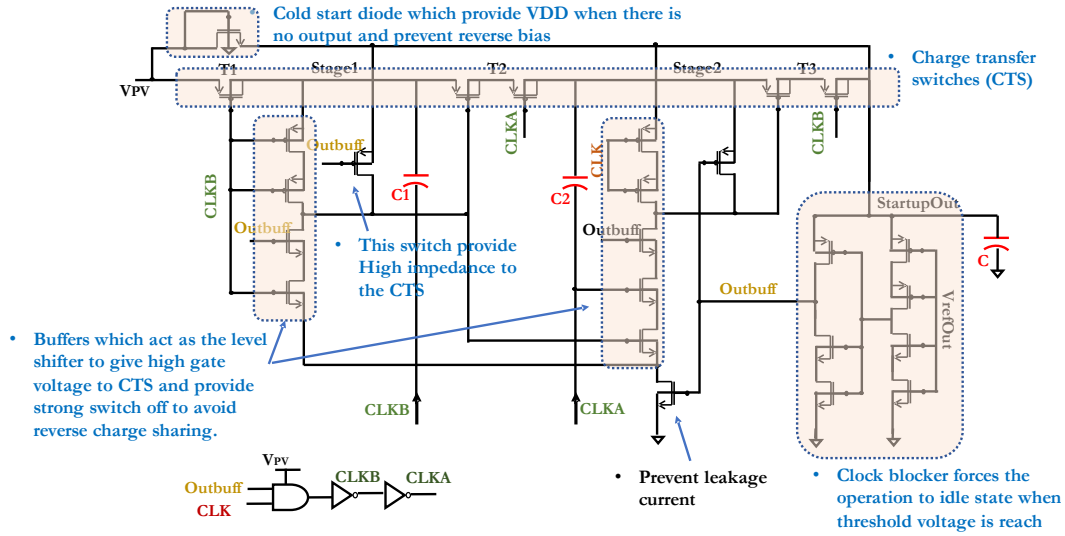


Figure A3. 2. the start-up charge pump suggested in Mohammadi(2015)[165].

As discussed previously, all the charge transfer switches (CTS) are entirely off due to their gate voltages are supplied by high voltage from the two buffer circuits, which act as the level shifter. However, due to the previous W/L ratio being (10 µm/180 µm), having low threshold voltages and transistors is always on since its gate-source voltage- gate voltages being VDD CLK_{Asmall} or CLK_{Bsmall}, and source terminal at the output voltage is smaller than the threshold voltage. Thus, the modification of W/L has changed to (220 nm/1 µm) and set it off to save power consumption when there are no signals at the CLK_{Asmall} or CLK_{Bsmall}. By doing so, the leakage current (I) of the few (µA) leaking towards the buffer circuits, which act as a resistive load, has been minimised.

Appendix 3.3.2. Contribution 1: First modified attempt

As noticed from [165], the original literature was designed with the external clock, and its opposite clock is separated only by the single inverter delay. Consequently, cause charge unsettling between charging and discharging operation since two operational clocks are overlapped. This design aims to achieve on-chip self-oscillating clock generators and non-overlapped clocks. Therefore, two charge transfer clocks CLK_A and CLK_B, need to control differently to operate well with the charge pump and clock disabler. The following diagram in Fig. A3.3 suggests the first attempt proposed solution.

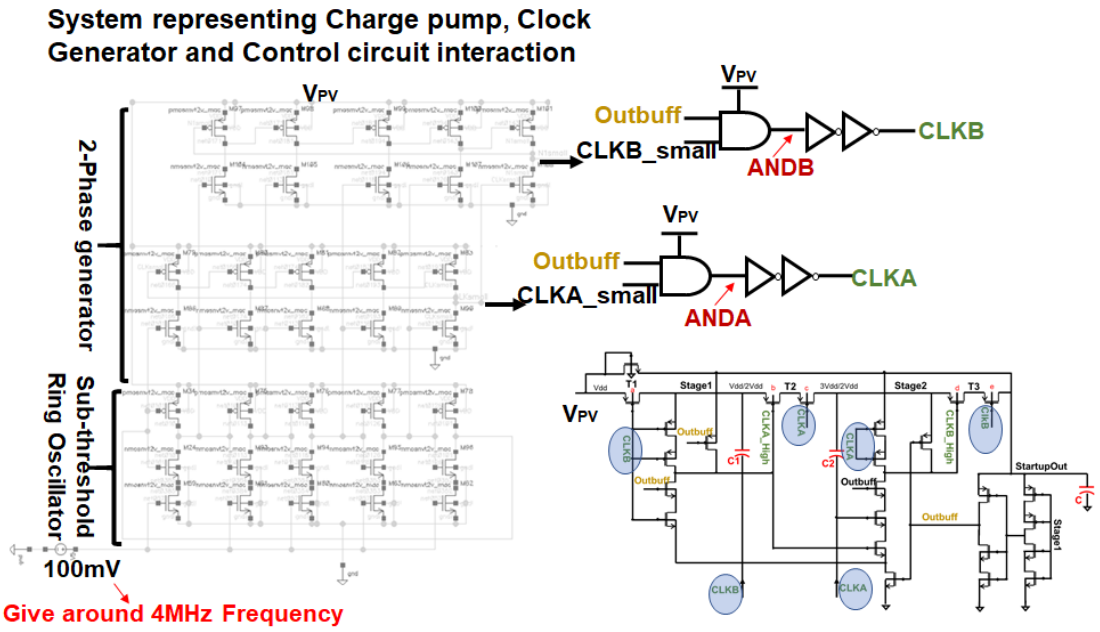


Figure A3. 3. The interaction of integrated clock, two-phase generator, control circuit and the charge pump implementation.

The generated two phases CLK_{A_small} and CLK_{B_small}, go through 'AND' operation with the clock's output disabler 'Outbuff'. The successful AND process produces two signals AND_A and AND_B, independently, then pass through the clock driver. By doing so, the power consumption across the large size clock driver is only static upon achieving the AND operation. It is because drivers' transistors need to be large enough (impedance matching) to eliminate the incoming distorted signal from capacitor charging-discharging actions. Moreover, the CTS switches and level shifter in the charge pump are also controlled by the charge transfer clocks CLK_A and CLK_B, as suggested by [165].

Having compared Fig. A3.3 and Fig. A3.4, the output of two-phase clocks is 'AND' together with 'Outbuff' to test whether the start-up charge pump has achieved the desired output voltage. Therefore 'Outbuff' can be regarded as enabling of 'AND' operation. The output voltage threshold is set by setting the buffer threshold that acts as the feedback connected to the start-up output. As a result, once the feedback buffer threshold, formerly known as 'Clock Blocker', aligned with the desire start-up output, the output buffer is low, and the whole 'And' operation is disabled. According to the Dickson charge pump principle, when the clock is disabled, the entire start-up operation is deactivated and saves energy consumption.

Appendix 3.3.3. Result and discussion of contribution 1

The output result of the operation of the start-up charge pump system is illustrated in Fig. A3.4. From the result, the oscillating waveform of 'Outbuff' is the consequence of disabling the clock disabler when the 'StartupOut' reach the desired output of 1 V. When the output falls slightly from the desired threshold, the operation is a resume and hence the entire operation restart again with the fast transient response.

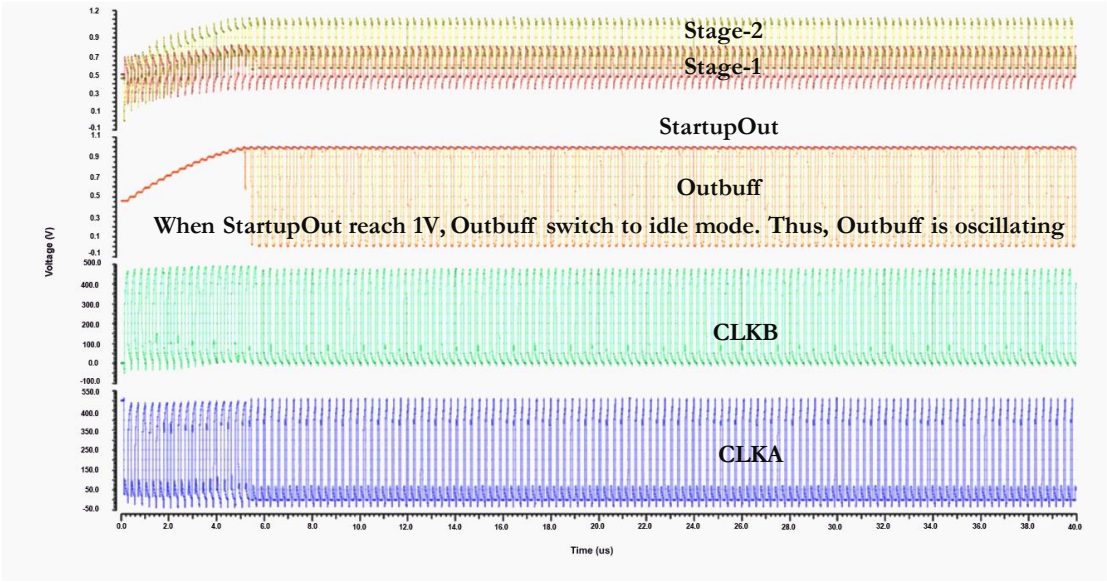


Figure A3. 4. Simulated result of the 'StartupOut' and 'Outbuff' demonstrating the clock control for the energy-saving scheme.

The result in Fig. A3.5 illustrates longer idle time occurs when the small load is connected to the start-up charge pump. Since there is no urgency in supplying the small load due to the clock disabler circuit, the converter operation has relaxed more and conserves more energy drawn from the source than the result in Fig. A3.6. This energy-saving condition with longer idle time also applies when the varying input voltage from the solar harvester is closer to the targeted output threshold voltage at 'StartupOut'. Since no charge sharing occurs during the idle mode, the power losses across the start-up charge pump have become dynamic power loss.

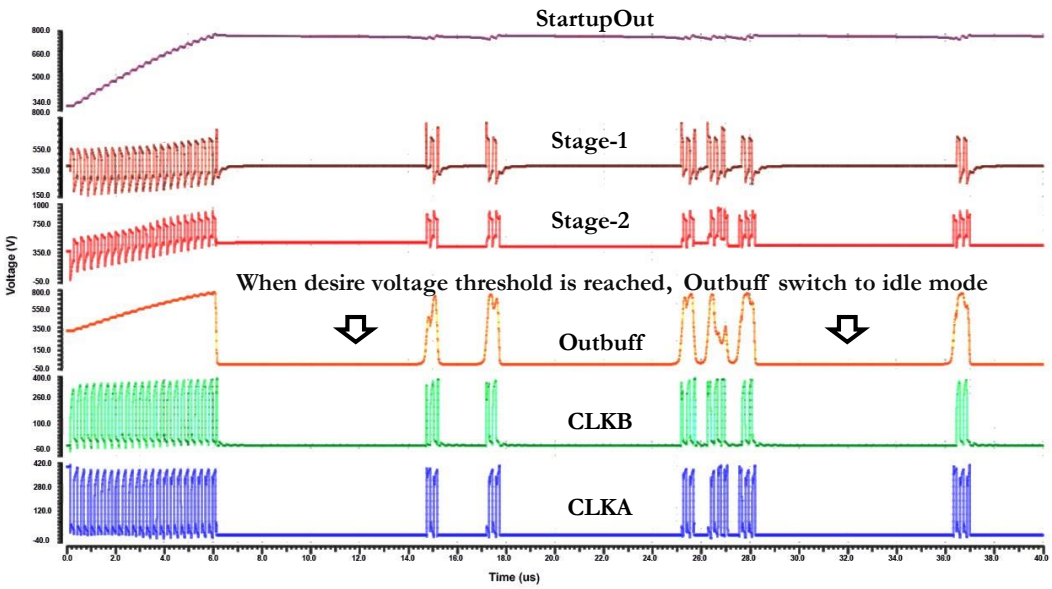


Figure A3. 5. Simulation result demonstrating the idle mode and operational mode of the start-up charge pump in the small load condition.

5.3.4. Appendix 3.3.4. Contribution 2: Second modification attempt

The circuit can be further modified into the design depicted in Fig. A3.6. The CTS switches' gate control signal now uses the undistorted 'CLK_{A_AND}' and 'CLK_{B_AND}', rather than the charge transfer clock 'CLK_A' and 'CLK_B'. These two clocks are initially generated by the two-phase generator and have directly connected with the capacitor's bottom plate. Thus, provide the undistorted clock waveform without needing to pass the clock driver.

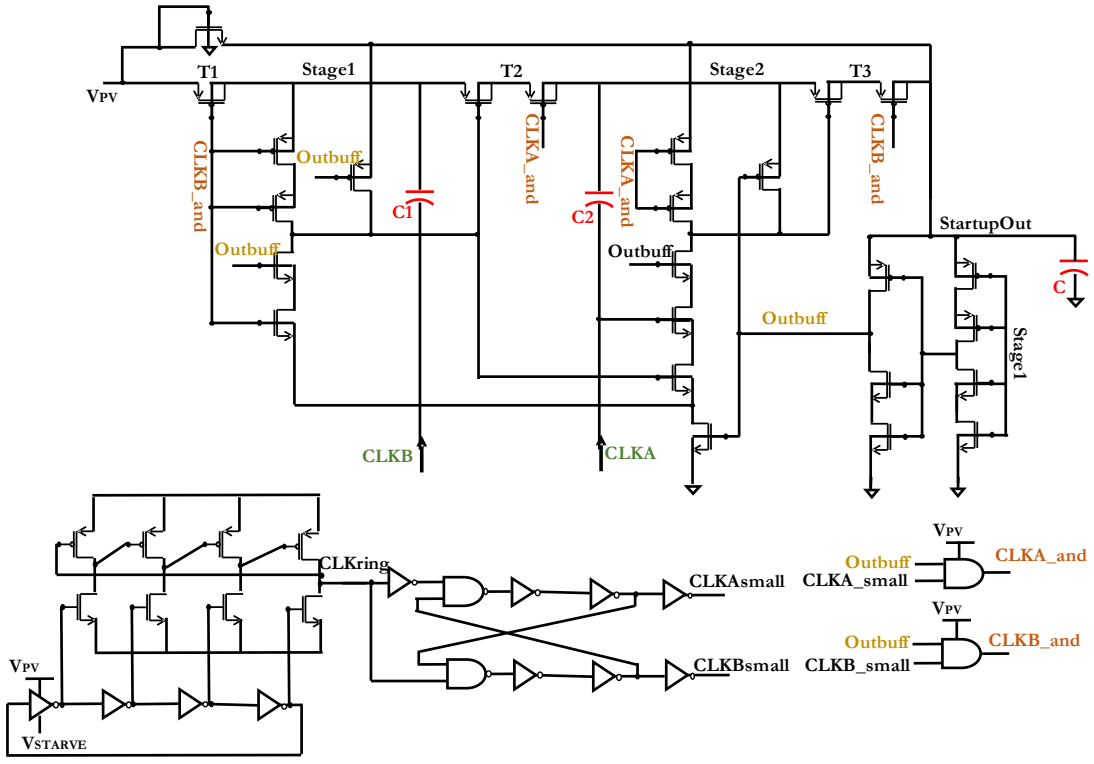


Figure A3. 6.The schematic diagram of Contribution-2 proposed clock scheme.

Due to the overlapping area between CLK_A and CLK_B, the standard two-phase non-overlapping clock generator[243] is used, and its output is regarded as CLK_{Asmall} and CLK_{Bsmall}. Then 'AND' operation with 'Outbuff'. As a result, the output of the clock disabler enables CLK_{Aand} and CLK_{Band}. It is later strengthened by using a buffer circuit, with the bigger width-length ratios transistors, as a clock driver to ensure there is no distortion at the bottom plate of the capacitor connections for charge transfer clocks. All the logic gates and inverter depicted in Fig. A3.6 are designed in a low voltage threshold to accommodate the *PV* cell's low input voltage.

5.3.5. Appendix 3.3.5. result and discussion of contribution 2

The results of the Contribution-2 circuit configuration is presented in this section. As illustrated in Fig. A3.7, charge transfer switches are now controlled by cleaner square wave CLK_{A/B_and} instead of distorted $CLK_{A/B}$ clock signals. Since input voltages (V_{PV}) vary, rather than using V_{PV} as the clock blocker circuit's input, the output of the clock disabler circuit 'Outbuff' is achieved by setting the relative ratio threshold ratio between the 'StartupOut' (as V_{DDH}) to the stage-1 (as input to the clock disabler) of the charge pump. It is depicted in Fig. A3.8(a-d). Thus the entire clock operations are forced to idle state as intended and save power consumption across the start-up charge pump system once the desired threshold voltage is realised.

The output voltages at a range of input voltages- 400 mV, 500 mV, 600 mV and 700 mV are 800 mV(ideal-*1.2 V), 980 mV(*1.5 V), 1.15 V(*1.8 V) and 1.3 V(*2.1 V) respectively. Therefore, the voltage conversion ratio (VCR) of the original design for different inputs are 66%(@400 mV), 65%(@500 mV), 63%(@600 mV) and 61%(@700 mV), respectively. However, the ideal values suggested in the literature is not in consideration of voltage drop across the clock disabler circuit. In [165] reported that the use of a clock blocker circuit comes with a trade-off between average power consumption and the drop of VCR ratio of the average output voltage.

Nevertheless, to achieve the targeted 1 V at the output, a minimum of 500 mV input voltage is required from the *PV* cell. It is because the boosting of 400-mV input has only achieved 800-mV. Therefore, the converter's VCR needs to be improved in the next contribution circuit design by eliminating potential leakage paths that create voltage losses within the charge pump.

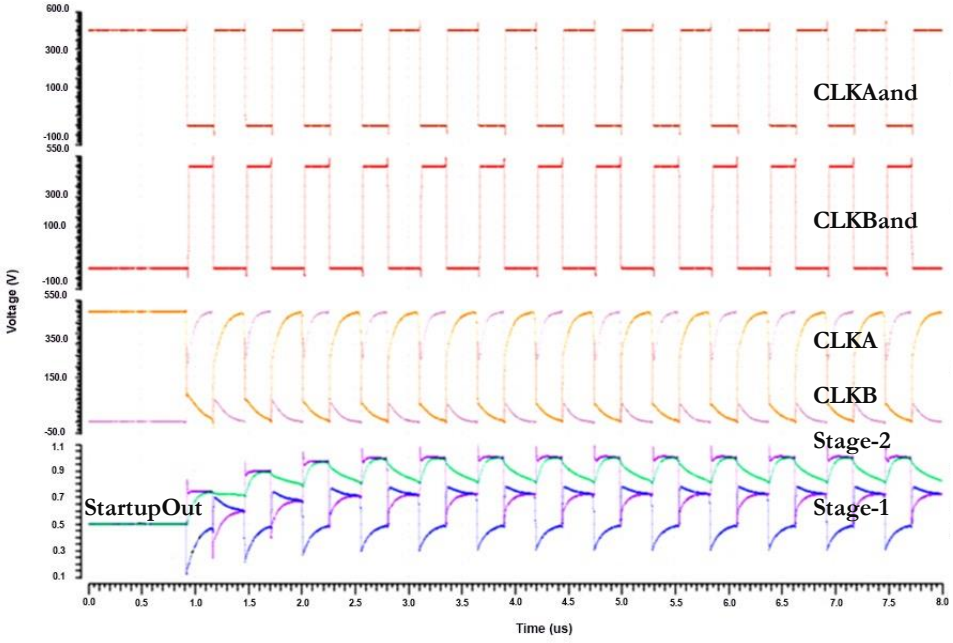


Figure A3. 7. Illustrates distorted CLKA and CLKB signals, and clean square wave CLKAand and CLKBand signals in comparison.

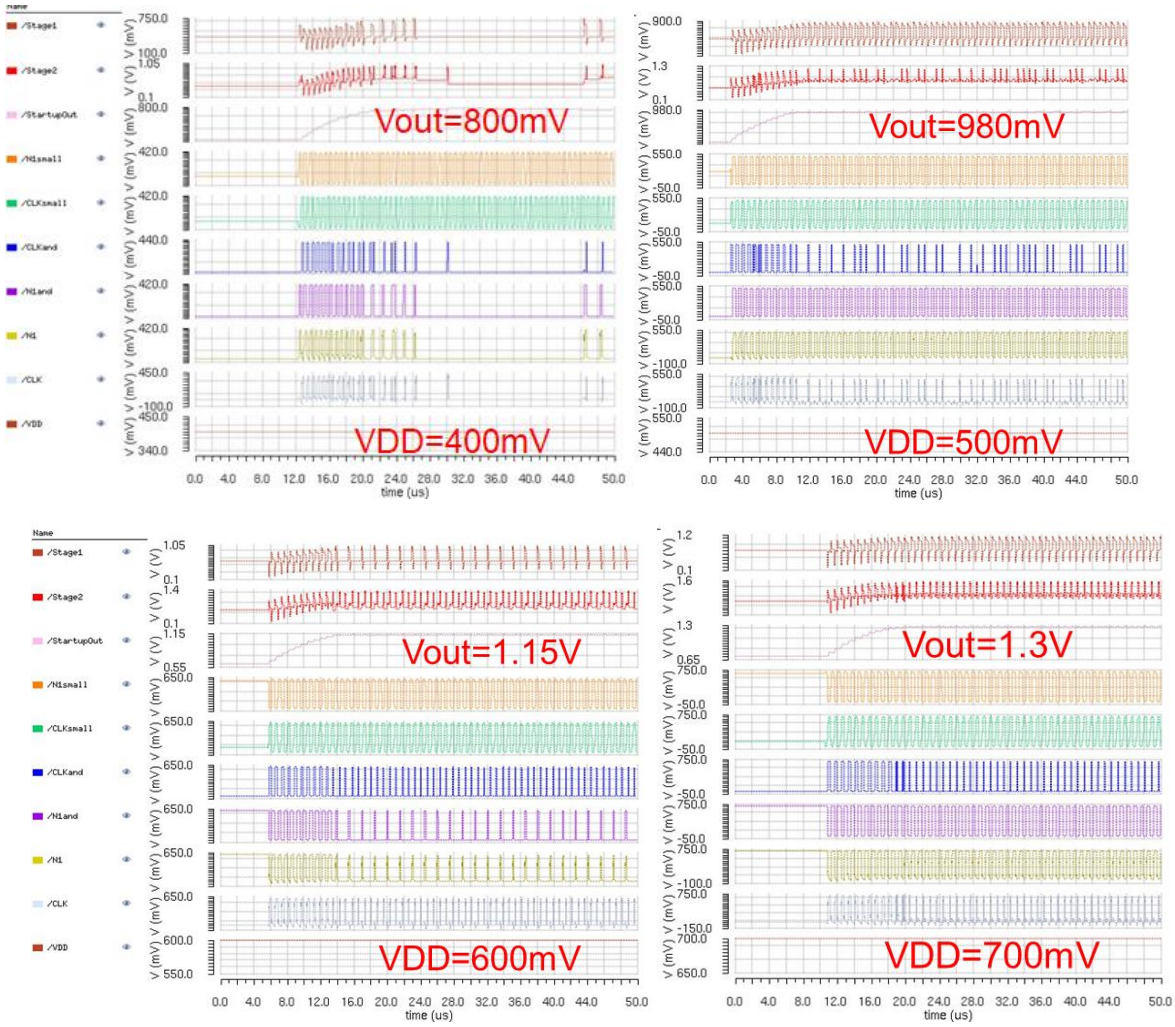


Figure A3. 8. The simulated result of Contribution 2 representing the output performance over the change of input voltages.

5.3.6. Appendix 3.3.6. Contribution 3: third modification attempt

To improve the voltage conversion ratio (VCR) of each stage-(1) all the leakage path across the level shifter design proposed in the [165] is removed. Then (2) was replaced with the level shifter presented in [222] and replaced with a mixture of native and medium threshold transistors to accommodate the low voltage operation. The proposed contribution-3 charge pump is shown in Fig. A3.9 (a), and its proposed clocking scheme is depicted in Fig. A3.9 (b).

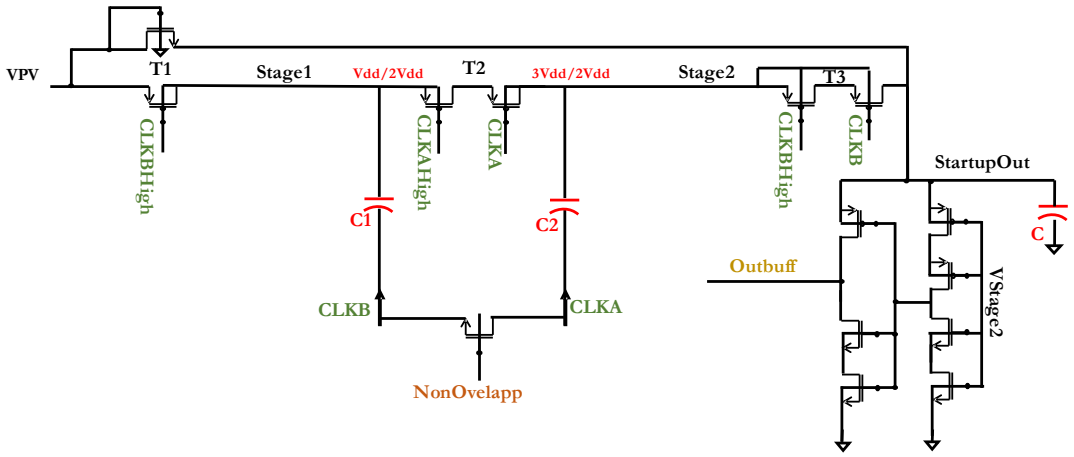
Moreover, (3) the novel clock scheme operating in the sub-threshold region is proposed to ensure enough dead time between two charge transfer clocks (CLK_A, CLK_B). (4) Implementation of the charge recycling technique as proposed in [124, 244, 245] to reduce the bottom plate parasitic loss. It is because energy deliver from the voltage source at charging charge pump capacitor to V_{DD} level in one step charging require [124]-

$$E_{source} = QV_{DD} \tag{A3.3}$$

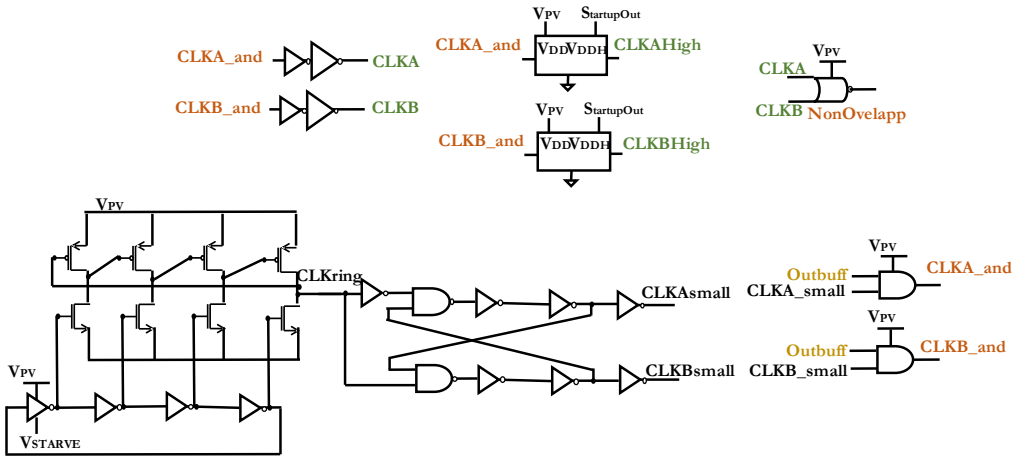
However, with the two-step slow charging from (G_{ND}-V_{DD}/2-V_{DD}) in the charging phase, the energy drawn from the voltage source is[124]-

$$E_{source} = \frac{1}{2}Q\frac{VDD}{2} + \frac{1}{2}QV_{DD} = \frac{3}{4}QV_{DD} \tag{A3.4}.$$

The implementation of the proposed clock scheme is depicted in Fig. A3.9 (b).



(a)



(b)

Figure A3. 9. (a) The schematic of the start-up charge pump and (b) proposed clock scheme of the Contribution-3.

5.3.7. Appendix 3.3.7. Result and discussion of contribution 3

The parametric analysis was carried out to illustrate each stage's conversion, leading to the final output over a varying input voltage range from 350-500 mV. As described in Fig. A3.10(a-d), the final output voltages (@given input voltages) are 875.35 mV(@350 mV), 993.98 mV(@400 mV), 1.08 V(@450 mV) and 1.157 V(@500 mV). Therefore, the conversion ratio efficiency of the design contribution-3 is 83%(@350 mV), 83%(@400 mV), 80%(@450 mV) and 77%(@500 mV).

It was observed in Fig. A3.10 that from 0.4 V input, the proposed Contribution-3 start-up charge pump has achieved 1.15 V . Therefore demonstrates that the proposed converter provides high VCR and achieved well within the targeted 1V voltage at no resistive load condition.

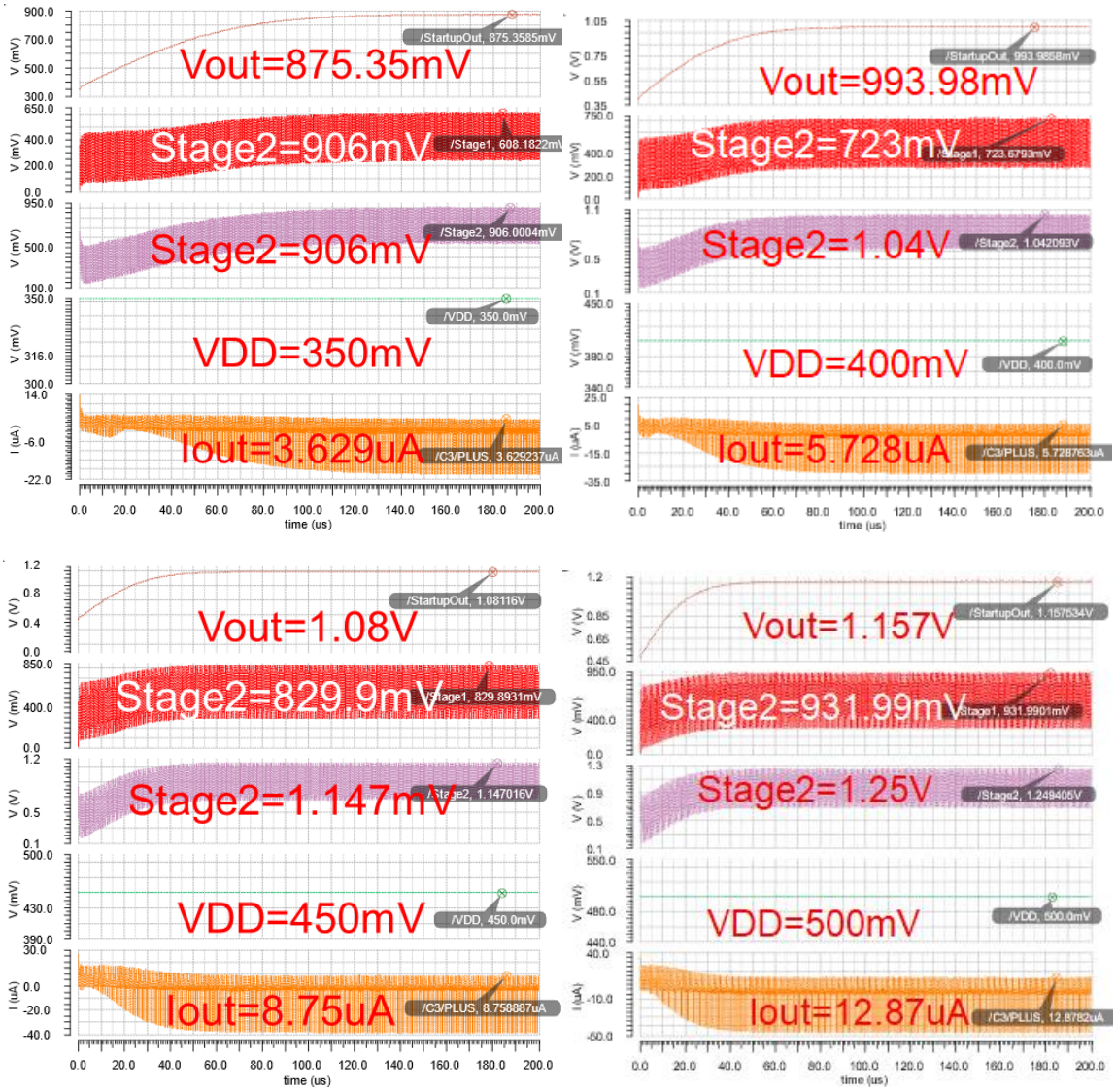


Figure A3. 10. The simulated output of the Design-1 Contribution-3 converter with inputs of (a) 350 mV (b) 400 mV (c) 450 mV and (d) 500 mV.

However, the delay problem arises when the amplitude shifted clock to implement the strong gate signal to avoid reverse charge sharing are slower than the charge transfer clocks CLK_A and CLK_B. The CLK_{AHigh} and CLK_{BHigh} are amplitude shifted clocks by using the level shifter proposed in [222]. It is illustrated in Fig. A3.11. Moreover, two high amplitude clocks are non-overlapped in zero-effective in contrary to charge transfer clocks. For the optimum charge transfer from one stage to another, control clock timing must be synchronised. In the next and final modification of the Contribution-4 design, the level-shifted clock and control clock signal's mismatched timing shall be addressed. It is essential because, during the slight microsecond of the delay mismatch between control clocks, the charge transfer switches can be potentially turn-on to incur unwanted reverse charge sharing action.

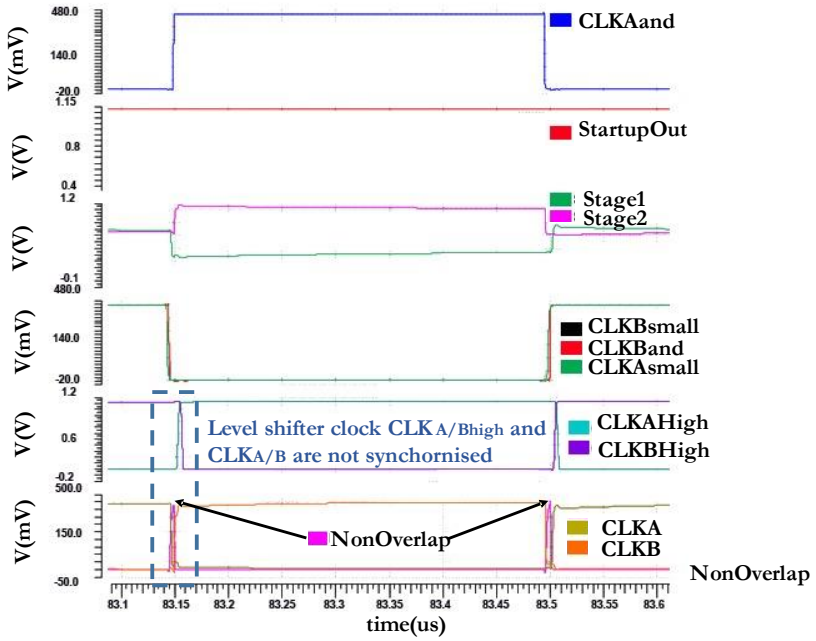


Figure A3. 11. The simulated output of the controlled clocks in Design-1 Contribution-3.

5.3.8. Appendix 3.3.8. contribution 4- final attempt and proposed design

Next, the simple buffer circuit (two inverters) is designed and implemented with a smaller size width transistor. The amplitude shifted signal will only control the gate of charge transfer transistors to switch off at off-period and eliminate reverse charge sharing effectively. Note that the buffer's V_{DDH} is connected to '*Outbuff*' instead of the charge pump in the second stage, as suggested in the literature. The voltage conversion ratio (VCR) of each stage has improved relative to the previous results. V_{DDH} of the peripheral circuit receives the low ripple supply since the 'Outbuff' signal is almost identical to the 'StartupOut', which again is connected to the external capacitor. It is demonstrated in Fig. A3.12.

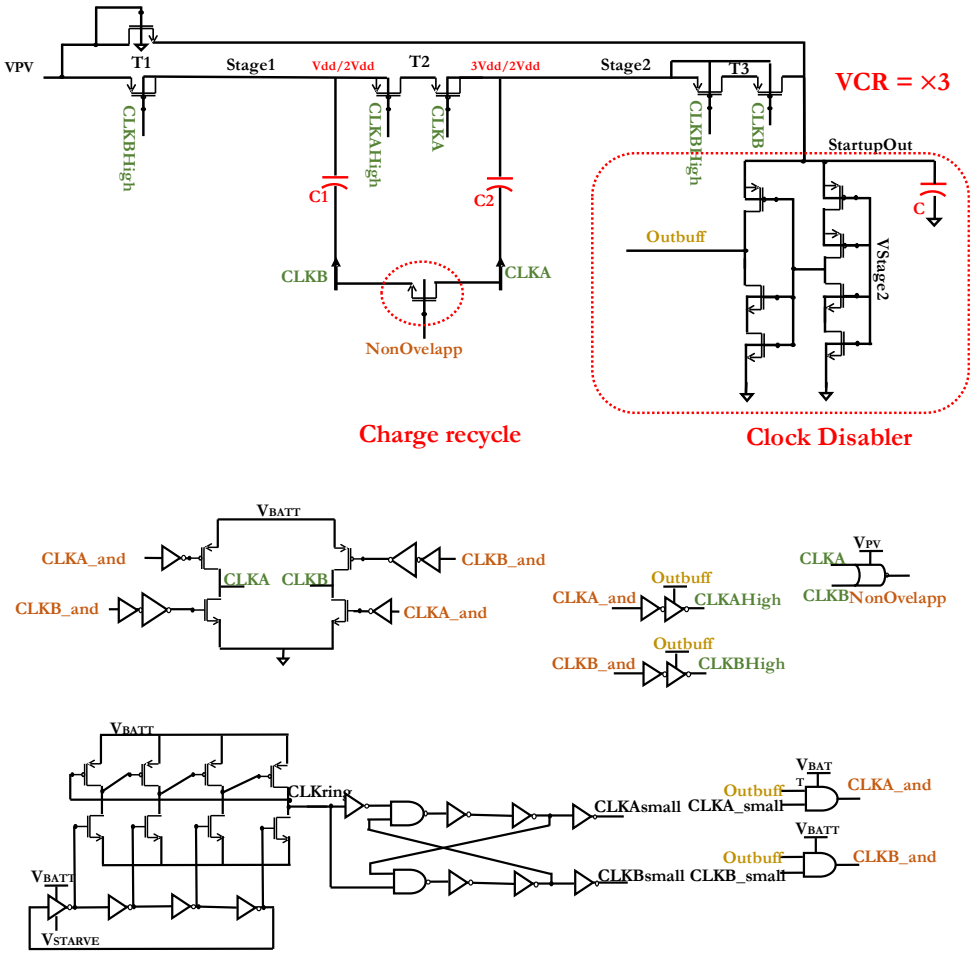


Figure A3. 12. The circuit implementation of the proposed Contribution-4.

This clock generator set up has managed to produce the non-overlapped two phases clock signals and maintain the synchronicity of higher amplitude timing with charge transfer clock signals. (CLK_A and CLK_B). However, the *CLKA* and *CLKB* slightly overlapped due to the charge recycling technique, which produces two adiabatic charge sharing steps; rather than rapid clock rise and fall amplitude between (0-V_{DD}), it is now (0- $V_{DD}/2$ -V_{DD}).

As suggested by [124], two charge sharing clocks, CLK_A and CLK_B, are generated by the tristate driver controlled by the signals CLK_{A_and} and CLK_{B_and}. These charge sharing clocks dictate the charging and discharging of capacitors C_1 and C_2 alternately. During the discharge phase, one of these two capacitors typically discharges to the ground. Instead, during the charging and discharging phase, also non as non-overlapping, the charge recycling transistor is a turn-on and pre-charge the next charging capacitor from next to the discharging capacitor $V_{DD}/2$. Then, the Equation's energy (5.4) ($E=3/4QV_{DD}$) is acquired via

charge sharing. Thus only (V_{DD}/2 to V_{DD}) is required from the source. The thereby first step of energy-conserving has been achieved.

By implementing the charge recycling switch in the bottom plate of two capacitors, the bottom-plate loss is minimised during the charge transfer operations [124, 246]. It is due to pre-charge action between two bottom parasitic capacitors connected across the switch, controlled by the non-overlapped signal.

5.3.9. Appendix 3.3.9. Result and discussion of contribution 4

The proposed Design-1 charge pump from Contribution1-4 are designed and simulated in 180 nm TSMC RF technology in a Cadence virtuoso environment. Fig. A3.13 demonstrates (1) the successful implementation of charge recycling, (2) the synchronise timing between amplitude shifted clocks and the charge transfer clocks, (3) and the simulated output at StartupOut, which is closely achieving to the target the ideal voltage conversion ratios. First, all the clock waveforms generated by the proposed clock generator evidence successfully implementing two-phase signals, non-overlapping with enough delay time and different amplitude clocks signals. The soft rising/falling characteristic of the charge transfer clocks ($CLK_{A/B}$) is also achieved, as suggested in [9]. Although there is a slight overlapping due to the slow rising/falling of the two clock transitions, the NMOS transistor between two bottom plate capacitors for charge recycling is designed to have enough threshold voltage with the amplitude of the non-overlapped signal. It is generated by the NOR operation of CLK_A and CLK_B.

Furthermore, the amplitude shifted clocks (CLK_{A/B_High}), generated by the buffer designed in low threshold transistors, are fast enough to synchronise with the charge transfer clocks ($CLK_{A/B}$). Consequently, it results in optimum charge sharing and prevents reserve charge sharing without any delay mismatch in the intended operation. Finally, we have discovered that for the input of 500 mV input, the output voltage has achieved 1.25 V, closer to the ideal target value (1.5 V).

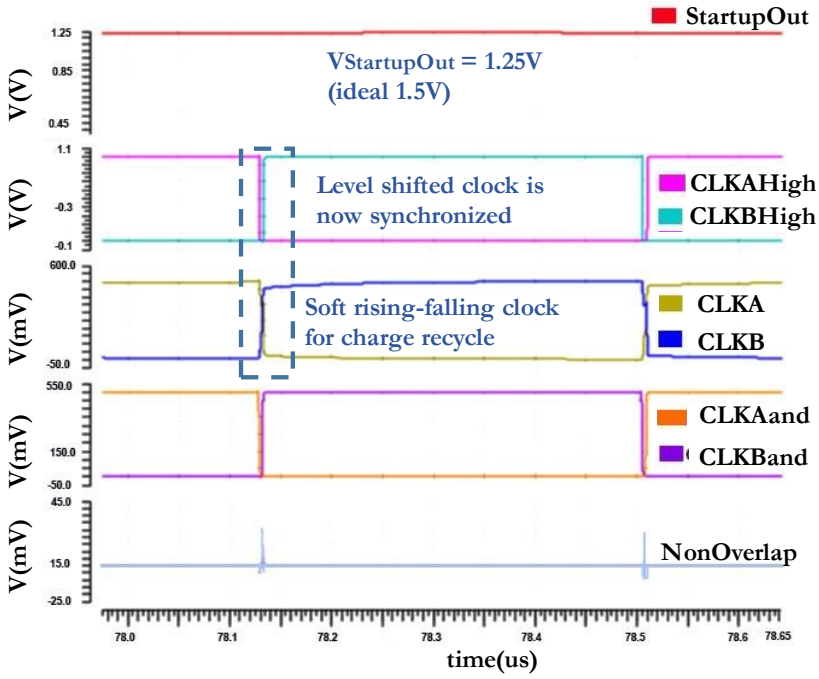


Figure A3. 13. The simulated output of the controlled clocks in the Contribution-4 system.

The comparison of output results from the varying input voltage in the line regulation test is presented in Fig. A3.14. It is important because this system's primary input is being a renewable energy source *PV* cell that can vary with the surrounding light condition. For the input voltages of 0.3 V, 0.375 V, 0.45 V, 0.525 V and 0.6 V, the output voltages are 554 mV(ideal-*0.9 V), 1.009 V(*1.125 V), 1.17 V(*1.35 V), 1.26 V(*1.575 V) and 1.332 V(*1.8 V) respectively.

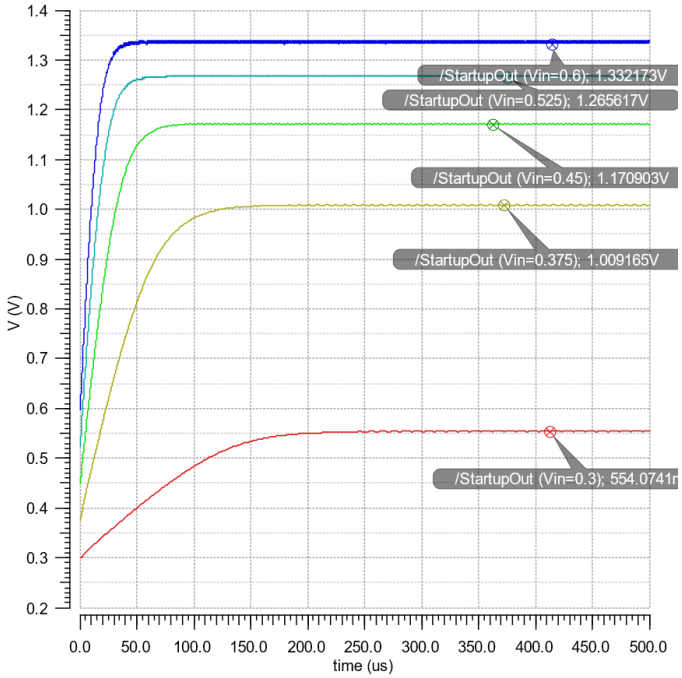


Figure A3. 14. The simulated outputs of the Design-1 Contribution-4 with the varying inputs from 0.3-0.6 V.

Appendix 3.4. Proposed Design-2

Appendix 3.4.1. background and motivation of design-2

The 2-stage cross-coupled design depicted in Fig. A3.15 is inspired by H. Peng's 6-stage body bias and backward control step-up charge pump [119]. Their work has promised low input voltage capability and is thus suitable for this intended application. The primary source is the *PV* energy harvester, which tends to provide a low output voltage with poor lighting conditions.

The original charge pump design was reported in [119]. It was reconstructed with transistors available in our 180 nm TSMC technology and modified into 2-stages crossed-coupled design than 6-stages suggested by the literature. Design-2 over Design-1 charge transfer switches are backwards controlled from the next stage to effectively switch on and off through the single inverter's output, high and low compared with the next stage's input voltage. The need for level-shifted buffers can eliminate by doing so. The complementary MOS structure of a cross-coupled charged pump controlled by a 2-stage transistor between each stage prevents revere charge sharing. On the contrary, Design-1 require adding additional charge transfer switches to serve the same purpose.

Furthermore, rather than setting the on-off threshold of charge transfer switches through the width-length ratio, manipulating the bulk terminal through symmetric crossed-couple interleaved voltages (1 and a, two and b). The CTS achieve the varying large threshold voltage at the switch-off condition and low threshold at the switch-on for better charge transfer capability. Moreover, the charge recycling technique [124, 245] at the bottom plate capacitor is also introduced to minimise the input source's energy.

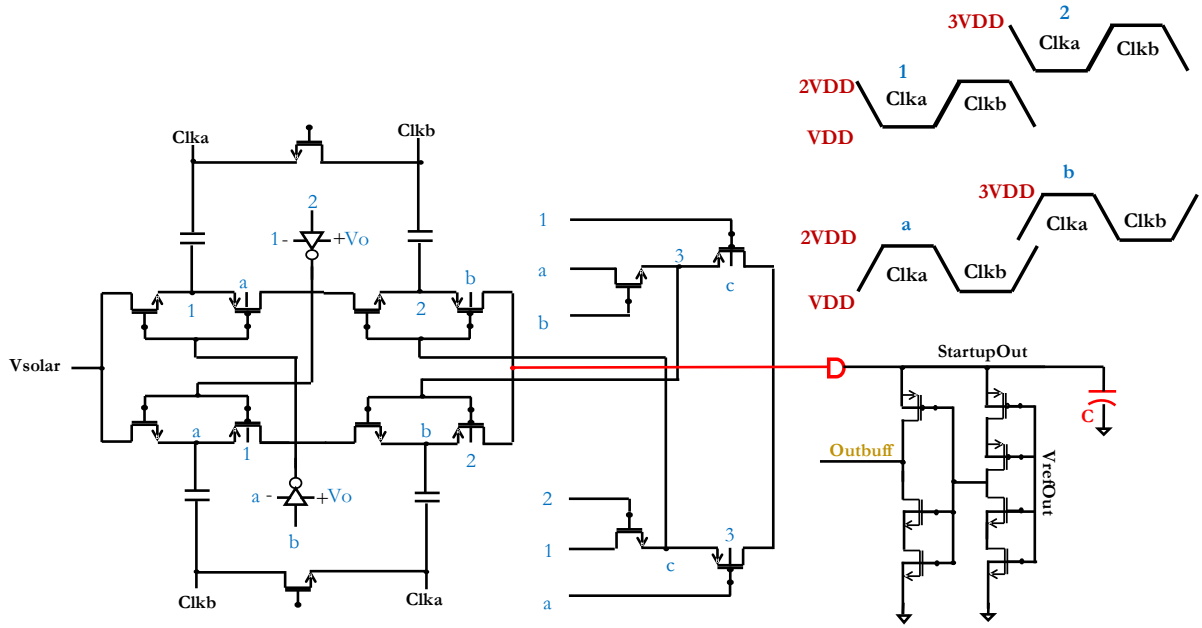
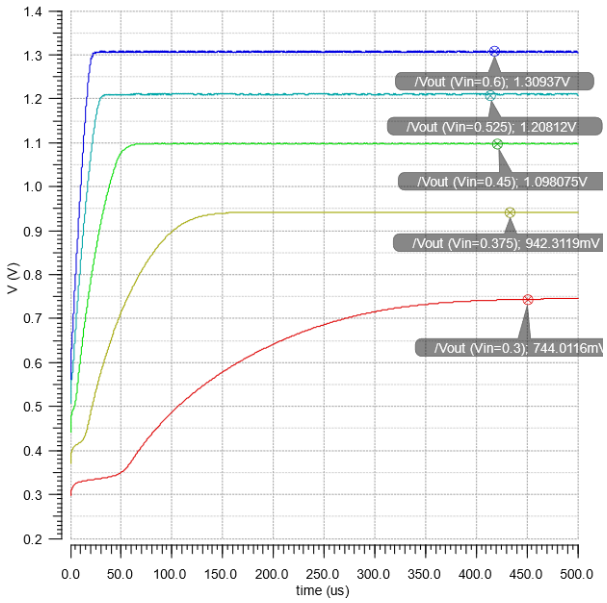


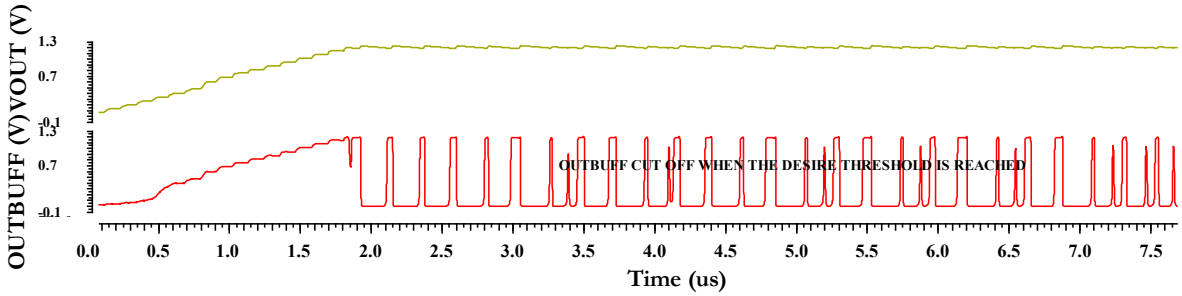
Figure A3. 15. Start-up Charge Pump-Design2: 6 stages charge pump in H. Peng (2014) is modified into 2-stage charge pump with charge recycling in Lauterbath (2000) and Lisboa (2016), and clock disabler circuit.

Appendix 3.4.2. result and discussion of design-2

The proposed Design-2 is implemented and simulated in 180 nm TSMC RF technology in a Cadence virtuoso environment. The line regulation for the varying input voltage in the line regulation test is presented in Fig. A3.16 (a). For the input voltages of 0.3 V, 0.375 V, 0.45 V, 0.525 V and 0.6 V, the output voltages are 744 mV(ideal-*0.9 V), 942.3 mV(*1.125 V), 1.098 V(*1.35 V), 1.2081 V(*1.575 V) and 1.309 V(*1.8 V) respectively. The converter can produce targeted 1 V output at the ultra-low voltage of 0.375-V input at no resistive load condition. It is also to note that this design allows the converter to operate at an ultra-low voltage minimum of 0.3-V. The demonstration of how energy is conserved by driving the converter into idle mode through the clock disabler circuit is presented in Fig. A3.16(b).



(a)



(b)

Figure A3. 16. The simulated result with line regulation test which input voltages vary from 0.3-0.6 V. (b) The converter output at 0.6 V and production of the clock disabler.

TABLE A3. 1. THE COMPARISON WITH ORIGINAL LITERATURES.

	Vin (V)	Design-1(V) 180 nm	[165] 180 nm	Deign-2 (V) 180 nm	[119] 650 nm
VCR		**×3**	**×3**	**×3**	**×9**
No. of stage		**2**	**2**	**2**	**6**
	0.30	**0.554**		**0.744**	**2V(@320mV)**
	0.375	**1.009**		**0.942**	**2.4V(@360mV)**
	0.45	**1.1709**		**1.098**	**2.6V(@400mV)**
	0.525	**1.265**	**1V(@500mV)**	**1.208**	**2.8V(@440mV)**
	0.6	**1.3321**		**1.3093**	

The VCR of Design-1 start-up system (@input voltage) provide- 61.5%(@0.3V), 89.6%(@0.375V), 86.6%(@0.45V), 80%(@0.525V), 74%(@0.6V). Similarly, for the Design-2, the VCR efficiencies (@input voltage) simulated provides- 82.36%(@0.3V), 83.76%(@0.375V), 81.33%(@0.45V), 76.7%(@0.525V), 72.7%(@0.6V). Therefore, Design-1 provide better VCR efficiency at the higher inputs, and Design-2 is suitable for poor performance (low voltage input) *PV* powered start-up charge pump design. It is to note that results from [119]in TABLE A3.1, which is also the based literature of Design-2, are for 6-stages converter design. In novel Design-2, however, only use 2-stages conversion for (×3) VCR. It is to note re-simulating the original design from literature with the same capacitors size and operation frequency as proposed Design-1 and Design-2 achieves less VCR, thanks to the charge recycling technique. Moreover, unlike [165], Design-1 will operate with an on-chip clock generator designed in a proposed novel clock generating scheme to provide robustly operate in subthreshold, self-oscillating, non-overlapping two-phase clock and fully function with control and charge pump circuits.

However, further investigations such as power efficiency and load regulation of this proposed Design-1 and Design-2 charge pumps are yet to be done. However, due to further improvement in ongoing research, these proposed two designs are to be fabricated.

Appendix 3.5. Proposed Design-3

Appendix 3.5.1. background and motivation

The first integrated switch-capacitor (SC) based DC-DC voltage step-up converter was proposed by Dickson [99]. Later, different versions of the Dickson charge pump were demonstrated [210, 212, 214, 247]. Although the Dickson charge pumps have fast transient responses compared to the other charge pumps, they suffer from poor current efficiency. However, there is a scope for improving Dickson's charge pump topology by mitigating different loss components such as shoot-through current loss, conduction loss and switching loss, which primarily contribute to power efficiency. The desired solar energy harvested start-up charge pump aims to bridge the low voltage *PV* harvested energy into the secondary storage source capacitor. It is then further power the main converter is shown in Fig. A3.17(a). Moreover, the SC converter's design trade-off discussed in [149]and this proposed design's contribution is depicted in Fig. A3.17(b).

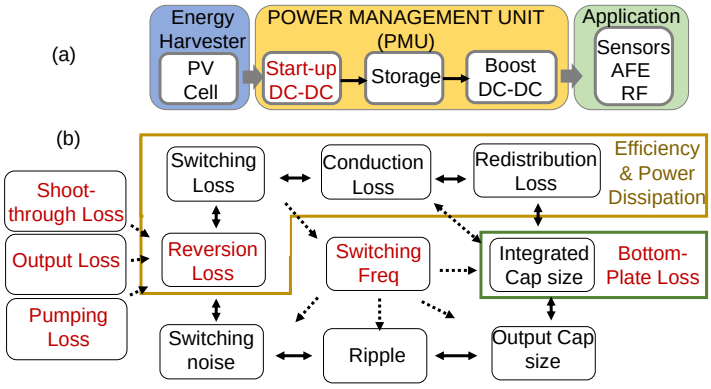


Figure A3. 17. Illustrating the use of (a) start-up charge pump in PMU. (b) SC design trade-off diagram and our contribution are highlighted in red.

This design aims to achieve a start-up charge pump for the power management system that operates with low input power supplied from a typical crystalline silicon *PV* cell. The *PV* cell's harvested energy is first power managed through an ultra-low-power step up start-up charge pump to convert low input voltage to meaningful voltage. It is operated with on-chip self-oscillating clock generators [166]and non-overlapped clocks to control the charge sharing clock (CSC) and the charge transfer switches (CTS) of the start-up converter. The proposed clocking scheme operates well with the charge pump and the clock disabler to prevent constant power drawing from the *PV* cell. Second, the start-up charge pump's energy output can be stored in a reservoir,i.e., a capacitor.

Appendix 3.5.2. Challenges and proposed contributions

In the Dickson charge pump's step-up conversion, the voltage boosting of voltage goes from left to right across the n-stage charge pumps and the voltage increases at each pumping node.

A. Challenge and contribution 1: Eliminate reverse charge sharing dynamic loss.

Reverse current paths from the output to the input direction results in output voltage loss and subsequently produce a negative contribution to overall power efficiency. Several reverse charge sharing path schemes are discussed in [40, 149]. Three types of reversion losses can occur, shown in Fig. A3.18(a). These are (1) Output loss that occurs when M2 is accidentally ON during the charging process of the charge pump capacitor C and current from load capacitor leaks towards the charge pump instead of sourcing to the load resistor, (2) pumping loss occurs when M_1 unexpectedly turns on and charge share backward from pumping

capacitor towards the supply source, and (3) shoot-through current loss or short circuit loss happen when both M_1 and M_2 are ON at the same time, and short circuit the output to input directly.

The two-phase clock-controlled method is typically used, provided that the gate control signals of the CTS are in the diode connection; the gate and the drain of the transistors are connected, or CTS is bootstrapped by the charge pump's next stage [248, 249]. Let's assume that the standard non-overlapping two-phase clocks are used for CSC (CLK_1, CLK_2) and CTS (Q_1, Q_2) as illustrated in Fig. A3.18(a, c). For simplicity, the example was given for a 2-stages charge pump with NMOS CTS, and three arbitrary clock periods (1/2/3) are taken to investigate the charge pump's operation. When the clock signal of Fig. A3.18(b) was applied to the CTC and boosting CSC, as shown in Fig. A3.18(a) in period-2(H-H-H), shoot-through current loss and in period-3(H-H-L), pumping loss occurs.

In the literature [250], a six-phase clock control scheme was proposed to control the crossed-coupled charge pump. In this proposed charge pump, the adaption of the original work [250] was utilised, and the four-phase clock scheme, shown in Fig. A3.18(c), was used to control the Dickson charge pump converter. Moreover, the charge pump design in [250] was designed to operate at a 1.8 V input source. In contrast, this proposed design is for a low-voltage solar harvested input source. The clock generators can work at ultra-low voltages.

A similar investigation can be repeated by employing the proposed clock scheme depicted in Fig. A3.18(c) into the simple Dickson charge pump circuit in Fig. A3.18(a). It was observed that the reversion loss was eliminated in all three periods.

B. Challenge and contribution 2: Charge recycling to reduce bottom plate parasitic loss

The dynamic power loss correlated to the bottom plate parasitic is another primary reason for low power efficiency. The charge recycling or charge sharing between the bottom layer and substrate parasitic has been studied in [244, 251]to minimise the loss.

As illustrated in Fig. A3.19(d), when any of the pumping capacitors are charged, the corresponding bottom parasitic capacitors are also charged to the same magnitude and stored some energy. This process can be considered as the bottom-plate loss during charge sharing. As suggested in Fig. A3.18(d), when the two parasitic capacitors are connected during the operation soft-charging/discharging time (Δt), before the next operation begins, the charged parasitic capacitor (CB_1) from the adjacent stage was pre-charged to the neighbour stage parasitic capacitor (CB_2) connected across the switch. Therefore, in the next operation when the second stage (C_2) was charged to $2V_{DD}$. Thanks to the pre-charged charge recycling action, the corresponding parasitic capacitance (CB_2) only varies between pre-charged voltage to $2V_{DD}$ instead of a whole amplitude from $2V_{DD}$ ground shown in Fig. A3.18(d).

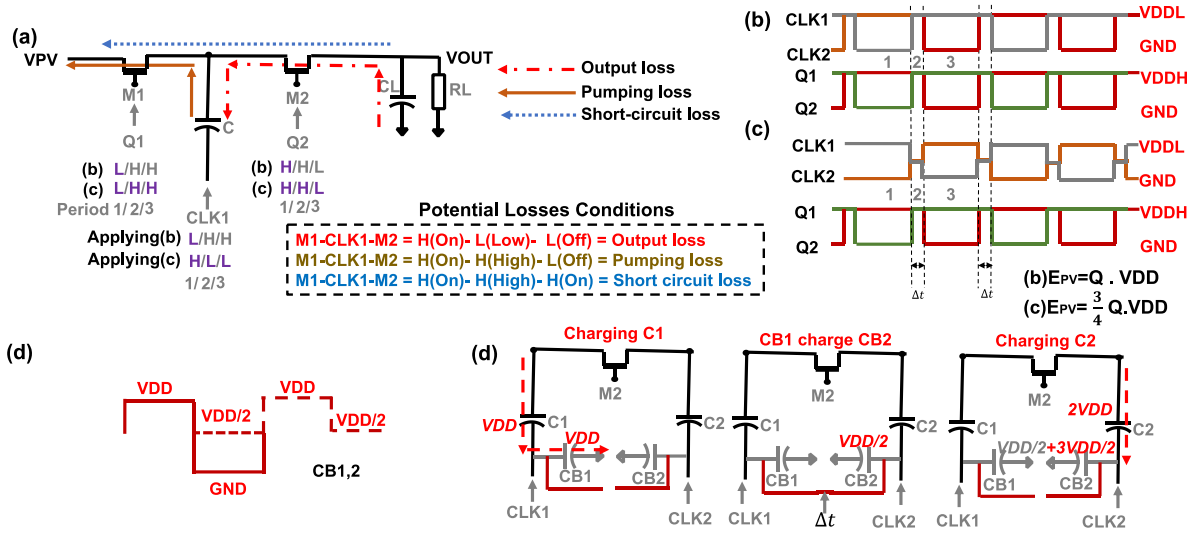


Figure A3. 18(a) Problem and challenges of potential reverse charge sharing losses in Dickson's charge pump. Designed with (b) standard non-overlapping control clocks, (c) proposed controlled signals and (d) explanation of why charge recycled technique can reduce the bottom plate loss.

C. Challenge and contribution 3: Two-step adiabatic CSC enable charge recycling as well as reduce power dissipation

A two-step adiabatic (CSC) high impedance capacitive driver was presented in [124, 250]. Thanks to the tristate driver, two-step charging-discharging was possible. It produces CSC non-overlapped period signal (Δt). According to [250], contrary to one-step charging, the source's energy dissipation has been reduced to three quarters. It has also been discussed in the previous section.

D. Challenge and contribution 4: Automatic clock disabler to reduces the energy dissipation

The constant power consumption across the start-up charge pump system can change into dynamic consumption if the start-up operation switches to idle mode once the desired voltage is achieved at the storage capacitor. The clock disabler buffer is implemented at the start-up charge pump's output to monitor and examine whether the output voltage threshold is reached to a pre-determined voltage required by the main converter. In previous studies, the charge pump design with clock disabler is proposed in [165] and integrated into this proposed charge pump design. The clock disabler's output was linked with the previously mentioned clock generators to enable the whole start-up operation and prevent constant energy dissipation from the source.

Appendix 3.5.2. Implementation of the proposed design-3 clock scheme and charge pump

In the 180 nm TSMC RF, a native threshold transistor is also available, but it is limited only to the NMOS. Upon availability of a native threshold transistor for both MOSFET pairs in other technologies, the ultra-low input voltage of lower than 450 mV can be configured. The proposed control clock scheme is inspired by [250]. The original work was designed to prevent any potential reverse charging for a crossed-couple charge pump circuit and operates at 1.8 V. The proposed design in Fig. A3.18 uses standard transistors. The mixture of native-threshold, medium-threshold and general-purpose transistors are appropriately used to ensure that the charge pump and the clock generators circuits are functional at low input voltage sources. The transistor seizes chosen through parametric sweep to ensure that their widths and lengths' optimal ratio guarantees the highest VCR and power efficiency.

Two charge transfer clocks CLK_1 and CLK_2, which are used primarily for the boosting process, are connected to the bottom plate of the top and bottom capacitors, respectively. It was implemented through the charge recycling technique to ensure that during the transition dead-time. Δt, when the two pumping capacitors remain idle, two bottom plates of both capacitors are connected in parallel by the switch. This switch ON signal was triggered by the OR gate signal configured from CLK_A and CLK_B. When pumping capacitors are charged, their correspondent bottom parasitic capacitors are also charged to the same magnitude and store some energy. This process can be considered as the bottom plate loss during charge sharing.

By introducing charge sharing in the process, this loss can be minimised. It is done by simply connecting two bottom plate capacitors across the switch and turning it on during the primary charge sharing process are in an idle state- i.e., Δt time. Therefore, during this period, since the two parasitic capacitors are also intertwined in two different phases, one charged parasitic capacitor share some stored energy with its counterpart capacitor. As a result, when the pumping capacitor charging action was resumed, due to its pre-charged action to the parasitic capacitor, charging the discharged parasitic capacitor in the following cycle was minimised energy consumption of the associated clock driver reduced to half.

To reduce the layout complexity and the area consumption, we did not use the deep n-well transistors, fully isolated NMOS does not suffer from the body effect when its bulk is connected to a different potential than the ground. As a trade-off, in generating the Q_1 and Q_2 clock signals, high/low amplitude varies between V_{DDH} to G_{ND} rather than V_{DDH} to V_{DD}. V_{DDH} being the same amplitude as the voltage at STAGE2, and the remaining annotation such as V_{DD}, V_{PV} and V_{DDL} are all tied to the input voltage. The circuit implementation is depicted in Fig. A3.19.

The output of two-phase clocks was *AND*ed together with '*Outbuff*' to test whether the start-up charge pump has reached the desired output voltage. Therefore '*Outbuff*' can be regarded as an enable of the '*AND*' operation. The output voltage threshold was set by setting the buffer threshold, which acts as the feedback connected to the output of the start-up's output. As a result, once the feedback buffer threshold was aligned with the desired start-up output, the output buffer was low, and the whole '*AND*' operation was disabled. When the clock is disabled, the entire start-up operation is deactivated to save energy consumption.

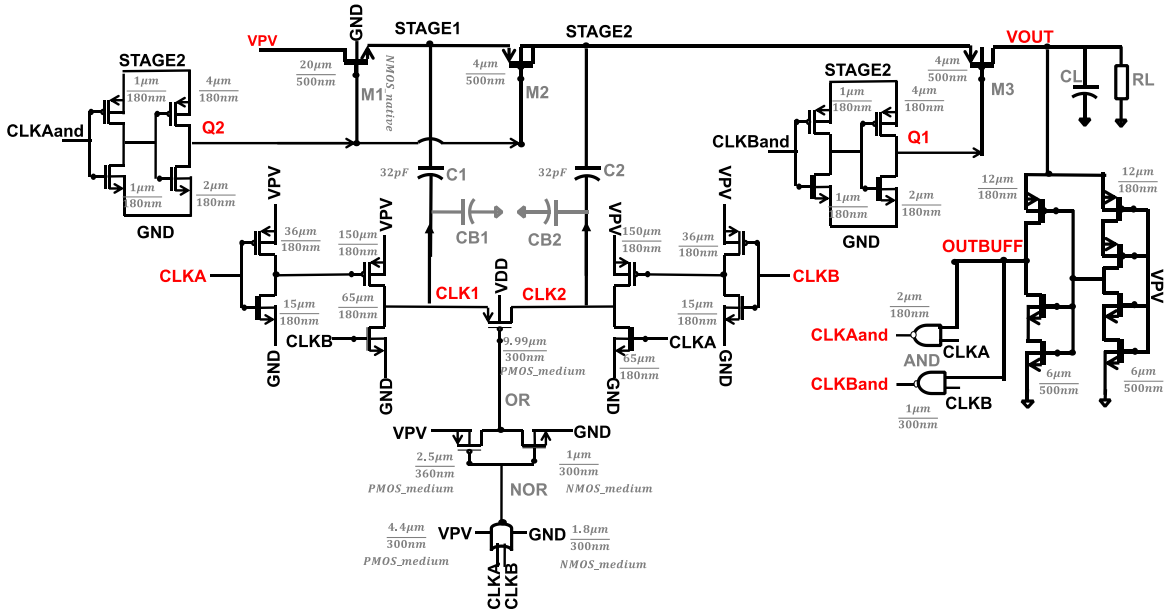


Figure A3. 19. Proposed circuit implementation of energy-saving clock disabler and charge recycled two-step adiabatic CSC controlled charge pump.

Appendix 3.5.3. test setup

This work was implemented in a standard 0.18 µm TSMC RF CMOS technology. The chip microphotograph of Design-3 is depicted in Fig. A3.20. The integrated capacitor of 2×20 pF and the output capacitor of 100 pF was used. The 8.8 MHz switching frequency was used for the operation, and each pulse was transformed into two-step adiabatic signals.

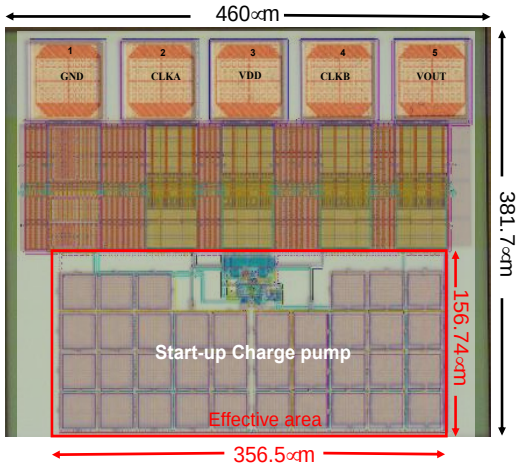


Figure A3.20. Chip microphotograph of Design-3 (bank annotated layout) with its effective area (356µm x 156.7µm).

Appendix 3.5.4. Result and discussion

Fig. A3.21 demonstrates the operation of the proposed charge pump with a clock disabler. Once the output voltage to the desire 1 V, the *Outbuff* goes to the idle, resulting in disabled control clock signals disable and, hence, stopped the charge pump.

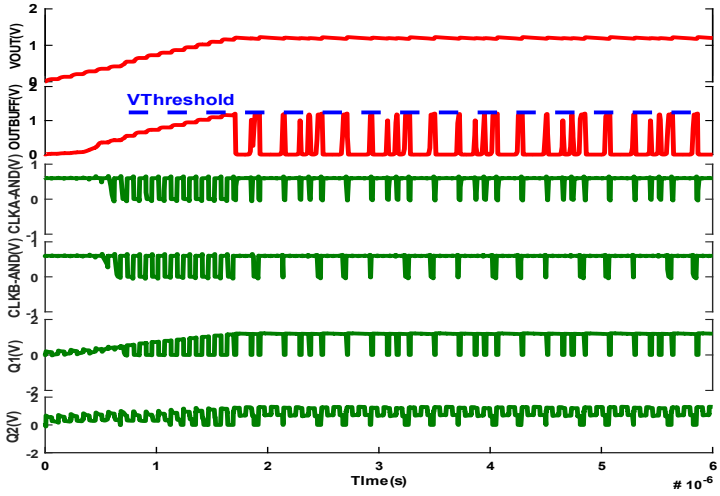


Figure A3.21. Demonstrate Output voltage remains stable even when the clock disabler's working operation is controlled by *Outbuff* signal.

As the input voltage increases, the Vout also increases. The output power has achieved up to 44.4-µW and 51% end-to-end maximum power efficiency. However, when the clock disabler was added, the efficiency has dropped significantly to 38.6%. The energy dissipation, squared of output voltage over the load resistance value ratio (V^2/R), was considered in Fig. A3.22. It demonstrates that the clock disabler design's proposed design has a 65% improvement in energy dissipation. Due to power loss being dynamic, the operation control clock disables the converter operation without interrupting the stable *Vout*, as shown in Fig. A3.23.

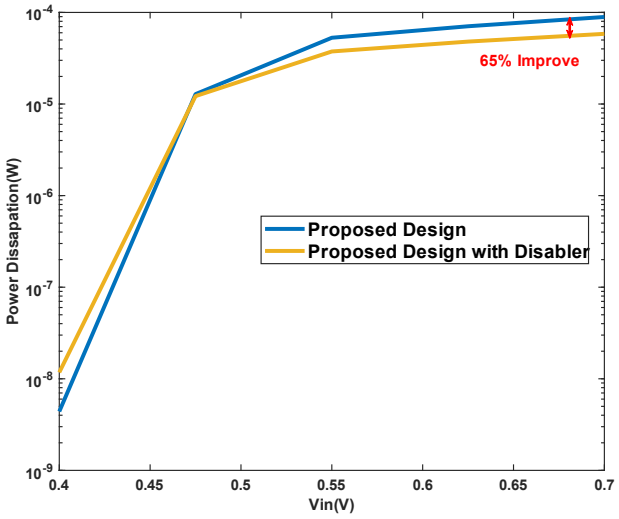


Figure A3. 22. Power dissipation in comparison with and without Disabler.

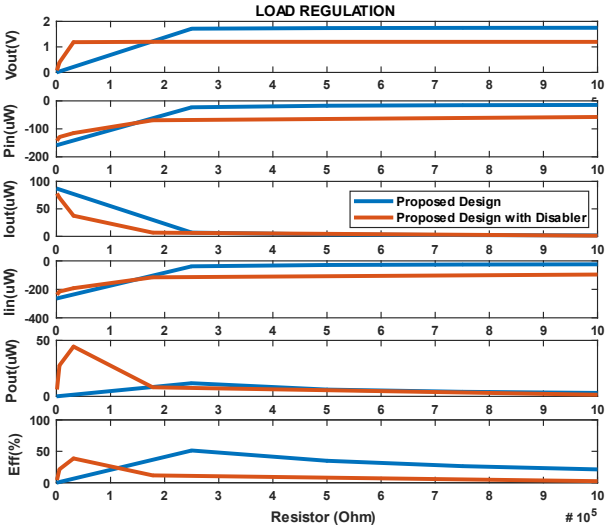


Figure A3. 23. Load regulation of the proposed charge pump sweeping from 1k-1MΩ.

The load regulation was tested with a wide range of 1 kΩ to 1 MΩ in Fig. A3.24. As the input voltage increases, the *Vout* also increases. The output power has achieved up to 44.4 mW and 51% end-to-end maximum power efficiency. The line regulation of the converter was demonstrated in Fig. A3.24. It is tested with the optimum load inherit from Fig. A3.23 to observe the change of the output voltage versus the change of input voltage (between 0.4-0.8 V) to imitate the solar cell open-circuit voltages different lighting conditions. It is noted that the output voltage has achieved up to 1.67 V at 0.7 V input voltage which is within the input voltage range sweep. The output power has achieved up to 89 μW at 73% efficiency. With a clock disabler, the efficiency has dropped to 46%, with the trade-off of improvement in power dissipation.

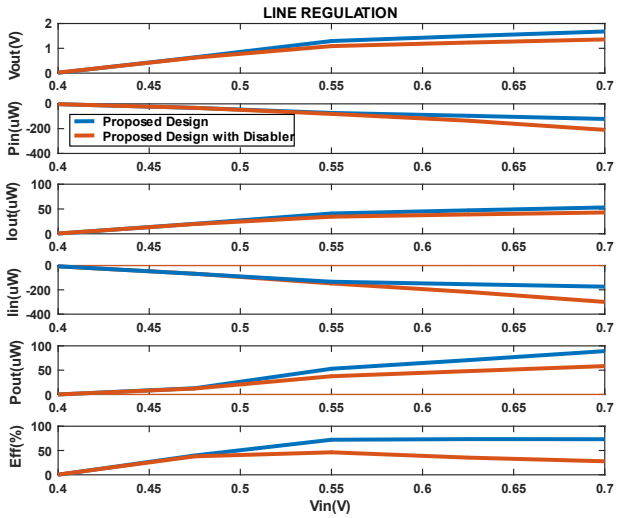


Figure A3. 24. Line regulation of the proposed charge pump (Blue) compares with the proposed charge pump with clock disabler (Red).

Appendix 3.6. Proposed Design-4

Appendix 3.6.1. background and motivation

The control clock signals are primarily crucial for step-up charge pumps, such as start-up converters. Because each of the factors presented in [149, 252] contributes to eliminating reverse charge sharing, which directly affects the power efficiencies. It has been widely accepted that crossed-couple charge pumps are better immune to reverse charge sharing than Dickson's charge pump topology due to their complementary MOS structure. However, if the control clock for both charging and discharging switches are not correctly designed as described in [149, 252], the potential reversion loss has not been eliminated. To address these issues, the proposed clock scheme for design4 based on [250] is presented in Fig. A3.25, and the desired clock scheme is proposed in Fig. A3.26(a). In this design, I and the original author co-design this together.

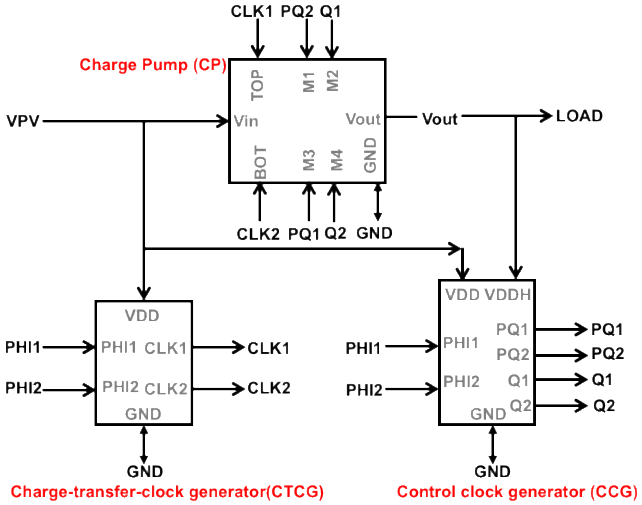


Figure A3. 25. The proposed architecture of start-up Design-4.

A. Challenge and contribution – potential reverse charge sharing in the cross-coupled converter.

Imagine a scenario top capacitor is in the charge-delivery phase to output whilst the bottom capacitor is being charged. Then, switches M_2 and M_3 should be at the active region and M_1 and M_4, on the other hand, should be at the cut-off area. There are three types of reverse charge sharing discussed in [252].

The output losses occur when the PMOS M_4 transistor should be off by strong 1 (V_{DD}). During the transition period, Δt gate voltage of M4 is less than the output voltage and, consequently, ends up being unexpectedly on. Similarly, pumping loss occurs when some charges flow back from the charge pump capacitor to the input source. In the same example, while M_2 is active, M_1 should be off. However, if there is a slow clock transition in the M1 transistor, boosting action through M_2 is already started before M1 is entirely switched off. As a result, the top capacitor discharge to the output as well as to the input source. Finally, short circuit loss happens during the transition of M1 and M2 or M3 and M4 simultaneously (see Fig. A3.26(b).

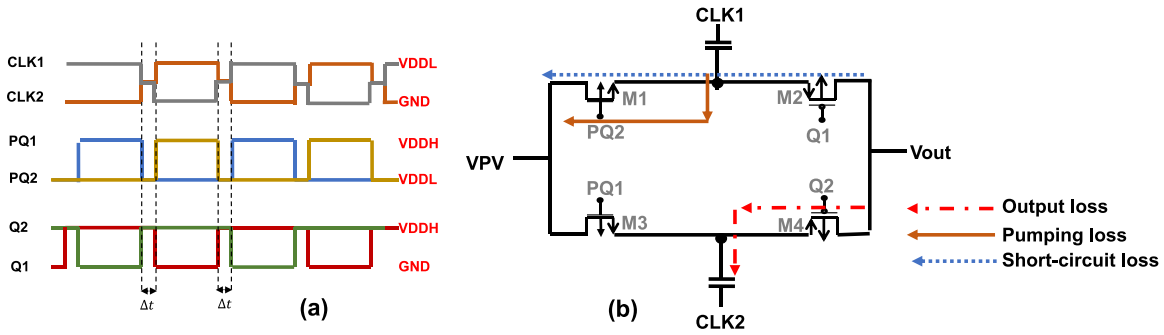


Figure A3.26. (a) Desire clock scheme minimised (b) the potential reverse charge sharing losses.

Appendix 3.6.2. Implementation of proposed Design-4

In the Design-3 charge pump [37], I have implemented a clock control scheme based on the literature [250] which was designed to prevent any potential reverse charging of Dickson's charge pump. However, this proposed design is for the cross-coupled converter and the original work adaption [250]. Design specification varies with the desired converter that will allow us to integrate into the energy harvester unit. Such an author was designed to operate in the 1.8 V input source, whereas this work's proposed circuits are intended to comply with the start-up charge pump's low-voltage requirements. Accordingly, the circuit is designed with a combination of standard transistors and medium-threshold transistors, as depicted in Fig. A3.27(a). In this figure, the switching transistors' sizing (M1-M3) is designed based on a trade-off between the minimum conduction loss and the minimum switching loss and according to the target output load. A dynamic bulk biasing circuit is implemented for the PMOS devices to prevent latch-up.

In the 180 nm TSMC RF, a native threshold transistor is also available but only limited to NMOS. Upon availability of a native threshold transistor for both MOSFET pairs in other technologies, the ultra-low input voltage of lower than 450 mV can be configured. The proposed start-up design depicted in Fig. A3.27 uses medium threshold MOSFET transistors for all charge transfer switches. The transistor seizes chosen through parametric sweep to ensure that the optimal ratio of width and length are set to guarantee the highest VCR and power efficiencies.

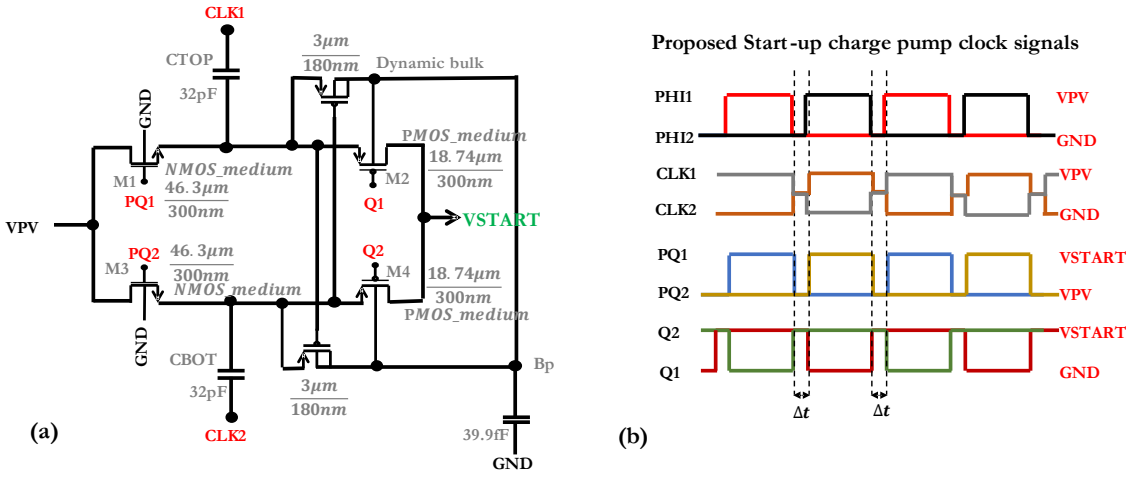
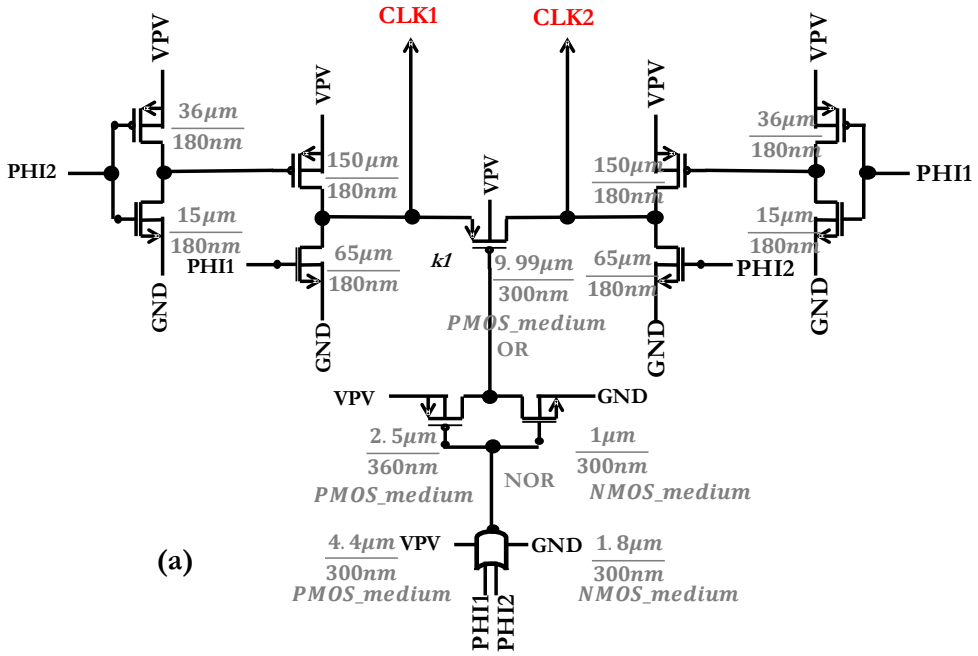
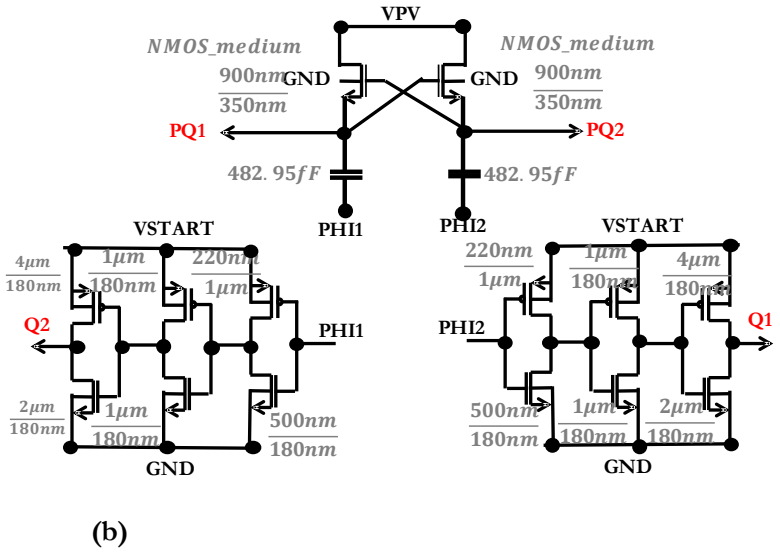


Figure A3.27. The circuit implementation of (a) the proposed charge pump and (b) timing diagram to control the switches and charge transfer clocks.

Fig. A3.27(b) shows the timing diagram of the clock signals. Three different sets of clock signals are used for driving the pumping capacitors (*CLK1* and *CLK2*), NMOS switches (*PQ1* and *PQ2*) and PMOS switches (*P1* and *P2*), all out of *PHI1* and *PHI2* clocks. It is to prevent reverse current from CP's output to its input while employing a charge recycling technique for reducing the switching loss. The circuit that generates *CLK1* and *CLK2* signals is depicted in Fig. A3.28(a). This circuit is designed for recycling the stored energy at the parasitic bottom-layer capacitors of pumping capacitors to reduce the switching power loss. Two bottom-plate of both capacitors are connected in parallel across the switch. It is turned on by the OR gate signal configured from Phi_1 and Phi_2. When either of the pumping capacitors is charged, the bottom parasitic capacitors that correspond to them are also charged to the same magnitude and stored some energy. This process can be considered as the bottom-plate loss during charge sharing. By introducing charge sharing in the process, this loss can be minimised. To this end, during Δt when the two pumping capacitors remain idle, the bottom plates of both capacitors are connected in parallel using the switch '*k1*'.

Therefore, since the two parasitic capacitors are intertwined in two different phases, charge recycling occurs between two counterpart parasitic capacitors during Δ*t*. Thus, during this period, since the two parasitic capacitors are also intertwined in two different phases, one charged parasitic capacitor share some stored energy with its counterpart capacitor. As a result, when the pumping capacitor charging action is resumed, due to its pre-charged action to the parasitic capacitor, charging the discharged parasitic capacitor in the following cycle is minimised the energy consumption of the associated clock driver is reduced. In other words, by using this charge recycling technique, less power is needed to drive the corresponding bottom-layer capacitor from $V_{PV}/2$ to V_{PV} rather than zero to V_{PV} in the next pumping phase. As shown in Fig. A3.28(b), the *Q1* and *Q2* clock signals' voltage levels are set to V_{START} and G_{ND} rather than V_{START} and V_{PV} to decrease the conducting resistance of PMOS switches (M_2 and M_4). Finally, the non-overlapping clock signals (*PQ1* and *PQ2*) for driving the NMOS switches (M_1 and M_3) are generated independently to *CLK1* and *CLK2* by a voltage doubler circuit (Fig. A3.28(b)). The deep n-well transistors are not utilised to simplify the layout complexity and minimise the area consumption, as the body effect does not affect this design crucially.





(b)

Figure A3.28. The circuit implementation of (a) charge sharing clock generator *CLK1,2* and (b) charge transfer switches clock signals *PQ1,2* and *Q1,2*.

Appendix 3.6.3. Simulation of Design-4

The proposed circuit is implemented and fabricated in 180 nm TSMC RF technologies, and the back annotated chip micrograph of Design-4 is presented in Fig. A3.29. The following section will discuss the post-layout simulation of Design-4.

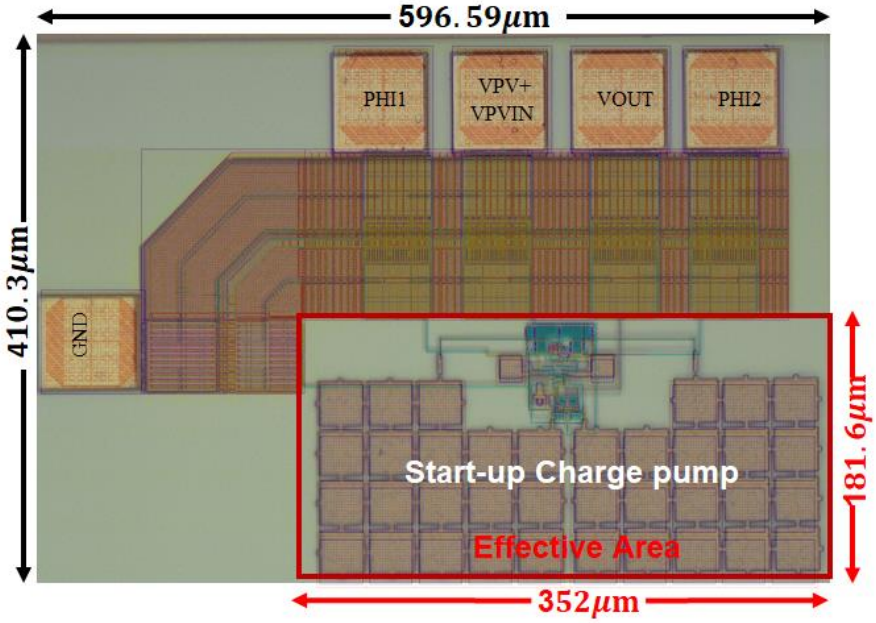


Figure A3.29. Chip microphotograph of Design-4 (bank annotated layout) with its effective area (352µm x 181.6µm).

Appendix 3.6.4. Result and discussion of design-4

Fig. A3.30 demonstrates the input/output signals from the proposed system. Further investigations were discussed in detail in Chapter 4's section 4.6.2.

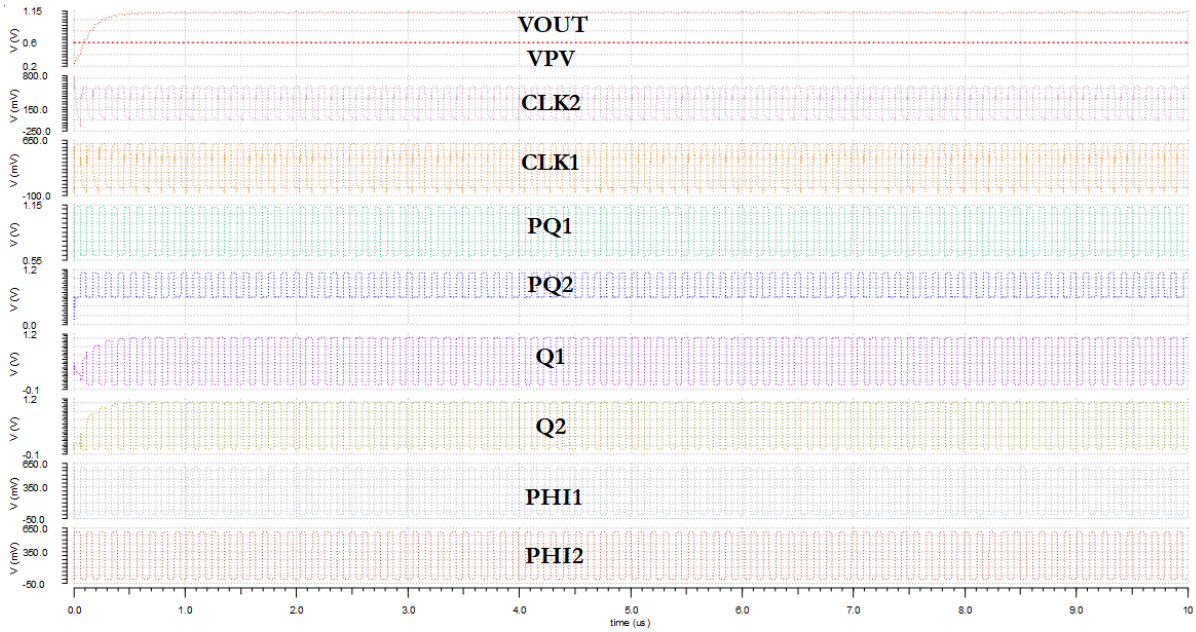


Figure A3.30. The overall outputs of the proposed design.

Finally, Design-4 is compared with the original work [250], which is designed to operate at 1.8 V input and other charge pumps supplied by solar energy sources. It is then tabulated in TABLE A3.2. As observed, the proposed Design-4 is in line with state-of-the-art and have comparable power efficiency and area efficiency.

TABLE A3. 2. COMPARISON OF DESIGN-4 WITH STATE-OF-THE-ART.

Specification	Design-4	[119] TCAS-I	[153] JSSCC17	[164] TCAS-II	[250] LSC18	[37] Design-3
Technology	180nm	180nm	180nm	130nm	65nm	180nm
Input (V)	0.48-1	0.32-0.5	0.25-0.65V	0.27-1	1.8	0.4-0.8
Output (V)	1	7	3.8-4V	1	3.38,-5.05	1
VCRs(×)	2	7	-	-	2	2
No. of Stage	1	6	-	6	1	1
Freq (MHz)	8.8	0.45	-	4.25	20	8.8
Int. Passive Device	32pF×2	48pF×6	1.5nF	1.5nF	350pF	20pF×2
Efficiency(%)	86	89	60	64	92.8	51

Appendix 3.7. Design summary of the Start-up charge pumps (Design 1-4)

The power management system's operation requires an integrated charge transfer clock for both start-up and main charge pumps. Due to low-powered input sources, such clock design can be challenging to operate in the ultra-low powered subthreshold region due to input voltage being smaller than the standard threshold transistors in most technologies. By using [166]sub-threshold body-biasing ring oscillator and two-phase generator is implemented. Moreover, due to the need for a non-overlapping charge transfer clock is then further modified.

Besides, to accommodate the charge recycling between stage-1 and stage-2 capacitors in a start-up charge pump, the 2-steps adiabatic charging and charge sharing charge transfer clock is implemented. It is presented in section 5.3.6 onwards by implementing the tri-state control clock driver [124], which work together with the output of generated self-oscillating clock and two phases of non-overlapping clock. Then further designed to complete the whole clock control scheme by taking the start-up converters' feedback signal. Consequently, these charge transfer clocks control the charge transfer switches and involve direct charge sharing between capacitors of each stage. Moreover, the energy-saving scheme clock blocker circuit, which followed the literature [165], work together with the proposed autonomous clock control circuits has also been discussed. It can be concluded the **Design-1** and the progress of work are projected through 'Contribution-1' to 'Contribution-4'.

Backward controlled topology used converter in [119], has taken the interest due to original work topology of carefully designed finals stage of the converter and ability to minimise reverse charge sharing, and the high voltage gate voltage of CTS are supplied via adjacent note potential difference without needing the additional level shifter circuit. It is further investigated through the proposed clocking scheme, which works together with charge recycle tri-state driver and clock disabler circuit. It has been presented in **Design-2,** and this work is re-implemented in 180 nm TSMC RF technology.

In Design-1, instead of using external clocks as suggested in the literature, an integrated proposed clock control scheme is proposed and ensure that non-overlapping between two charge transfer clocks for better charge settlings. Thus, the clock disabler for the energy-saving scheme is now operated appropriately with the integrated generated clock. The reference input to the clock disabler circuit is now the second stage of the charge pump. The width and length ratio of the clock disabler has been reconfigured to respond at the 1V threshold. The level shifter [222] used in the charge pump network is replaced with an appropriate low-powered buffer to avoid unnecessary leakages across the network during the 'off' period. This work is implemented in the 180 nm TSMC cadence technology. The Design-1 is integrated with two charge sharing capacitors with the (20-pF×2), the operation frequency of 4.4 MHz generated by providing 100mV to second NMOS stacked transistor of the ring oscillator and the external output capacitor is being 200pF. The VCR ratio of the (×3) 2- stage conversion has achieved up to 89.6%, which is the best at input voltage 0.375 V.

Similarly, the converter which can provide the highly efficient VCR in ultra-low power input is proposed in Design-2. Since it follows the crossed-couple topology, the integrated capacitor of (10-pF×4) for two stages are used and follow the same operating frequency and the external capacitor size as the Design-1. The Desing-2 converter provides the VCR of 82.36% at (@0.30V input), whereas the Design-1 converter is only managed to achieve 61.5% only. The trade-off between the Design-1 and Design-2 charge pumps are that Design-1 perform better at the higher input from 0.375 V onward, whereas Design-2 offer better VCR at the ultra-low voltages below the input voltage of 0.375 V. Moreover, the clock disabler scheme from Design-1 is also implemented in Design-2.

Two different topologies approach potential start-up charge pump designs, Design-1 and Design-2, which are implemented in 180 nm TSMC RF technology. The charge recycling between the integrated capacitors has been implemented to reduce parasitic loss at the capacitor's bottom plate and ease the energy drawn from the input voltage power source. The proposed designs demonstrate a better VCR than the original work. Further investigations and improvements of these two designs are yet to be done, and therefore, it can be noted as future work, and I plan to include these two designs in the next chip taped out. These two designs can be implemented as the potential start-up charge pump in my power management system upon successful results.

Next, the potential reversion loss, which contributes directly to the overall efficiency, was discussed. Instead of a two-phase control charge sharing clock, a multi-phase clock scheme tends to provide a better resolution to CTS and minimise the reversion losses. The proposed **Design-3** converter, which uses Dickson's topology, overcome, and contribute the followings- (1) reverse charge sharing dynamic losses are eliminated (2) bottom plate parasitic loss is reduced through charge recycling and (3) power dissipation of the charge pump has decreased by 65% due to the clock disabler circuit at the output. This charge pump shows stable load and line regulation. Although this Design-3 has achieved up to 73% power efficiency, it can only produce up to 51% efficiency with the clock blocker circuit. Therefore, further improvement is required.

Finally, **Design-4** presents a multi-phase control clocking scheme inspired by [250]and the original author and I co-design this together. Thanks to the careful design of the control clock scheme, the reversion loss is prevented. This work is implemented and fabricated the chip in the new 180 nm technology. In contrary to the original work, this work can operate in ultra-low input voltages. In contrast, the original literature is design to operate in standard 1.8 V. All the clock control circuits in this proposed work are redesigned to operate in the ultra-low input voltages. This work displays a high power efficiency of 86% efficiency and provides stable line and load regulations. As a result, a highly efficient low-powered charge pump Design-4 converter is accommodated as a start-up charge up to bridge between the solar energy source and the main converter.

Appendix 3.8. Conclusion remark of proposed Design 1-4

The potential start-up converter designs are discussed in this appendix. Design1 and Design2 have presented in the first part of Appendix-3. These proposed designs are suitable for *PV* powered on-chip power management. The proposed clock scheme enables low-powered input, charge recycled, and energy-saving start-up converter, converting the wide range of varying low input voltage to stable output voltage and stored in the secondary energy source. It is then supplied to the self-powered novel 2-phase converter to provide the required voltages sufficient to the load. The proposed start-up converter can operate at ultra-low input voltage as low as 0.3 V and achieve (×3) at 61.5% (@0.3V input) and 82.36% voltage conversion ratio in desgin1 output with 2-stage Dickson and in Design-2 2-stage Crossed-couple topologies, respectively. At maximum, Design-1 has achieved 89.6% (@0.375 V) and 83.75% (@0.375 V). The start-up circuit's power consumption is cut off to none when the desired output is reached, thanks to energy-saving scheme feedback control. The reduction in energy drawn from P.V. cell and bottom plate parasitic capacitance effect are considered with the charge recycling scheme.

In the second half of Appendix-3, the multi-phase control charge sharing clock (CSC) used Design-3 Dickson's charge pump novel converter and Design-4 Cross-coupled novel converter were introduced. Further investigation with clock blocker has also been made in Design-3 in search of energy-efficient charge pump design. The result demonstrated improved power dissipation by 63% with a clock blocker circuit, and there is a trade-off in efficiency significantly. According to my hypothesis, this could be due to the leakage path across the clock blocker circuit and additional circuit power consumption. Therefore, further work needs to be done to integrate the clock blocker perfectly with the desired start-up charge pump. By then, the start-up charge pump in PMU will only operate before reaching the desired input to the main

charge pump. As a result, the start-up charge pump's power consumption is dynamic only when it is being used. Bottom plate parasitic loss has been addressed by implementing a charge recycling technique with a tri-state clock driver that can also operate in the sub-threshold region.

In comparison to two-phase conventional controlled converters, the multi-phase approach has a better resolution to entirely turn on and turn off to charge transfer switches (CTS), or in the transition between charge, sharing to ensure that no reversion loss is possible. In comparison between the two designs, both converters can operate in ultra-low input voltages from a minimum of 0.4 V onwards and perform stable line regulation. However, due to the nature of the complementary MOS structure of the cross-coupled charge pump, Design-4 produce power efficiencies up to 84%. Therefore Design-4 has been chosen as the start-up converter to supply the main charge pump.

APPENDIX. 4: EXPERIMENTAL SET-UP.

Appendix 4.1. Fabricated IC Design.

The proposed work comprises different reliable and efficient self-powered DC-DC converter designs, serving different purposes. The designs can be divided into three categories-

(1) four cold-start converters, which a solar energy harvester can power. Our energy-efficient converters are based on both Dickson and crossed-couple topologies.

(2) Four novel designs of dual outputs, highly efficient reconfigurable converters designed by series-parallel topology.

(3) The power management system contains both (1) and (2) is designed in Cadence software with its PDK provided by TSMC and to be fabricated in 180 nm TSMC RF technology to put the idea to a test. The experimental set-ups are depicted as follow:

There is a total of 10 designs integrated into the 5-mm² chip area, as shown in Fig. A4.1. The experimental setup for future testing strategy is illustrated in Fig. A4.2 and Fig. A4.3. It is wire-bonded into Core1 and Core2 transfer PCBs without dicing the individual design. The design related to this chapter is integrated into Core1 PCB and demonstrates a matching simulation setup with wire-bonded PCB to the testing board. Core1 wire-bonded PCB port names with the internal connection to IO ports names are also illustrated next to each other. IC number 1 feed-in design in Fig. 3.12 and IC number 9 stand-alone design in Fig. 3.13, containing the integrated tristate driver.

As a foolproof plan, if the whole operation not working correctly in measurement due to the clock driver's accidental dysfunction, IC 2 and 10, the same designs as 1 and 9 but with two external clocks, are also fabricated. It has been illustrated in Fig. A2.1 and Fig. A2.2

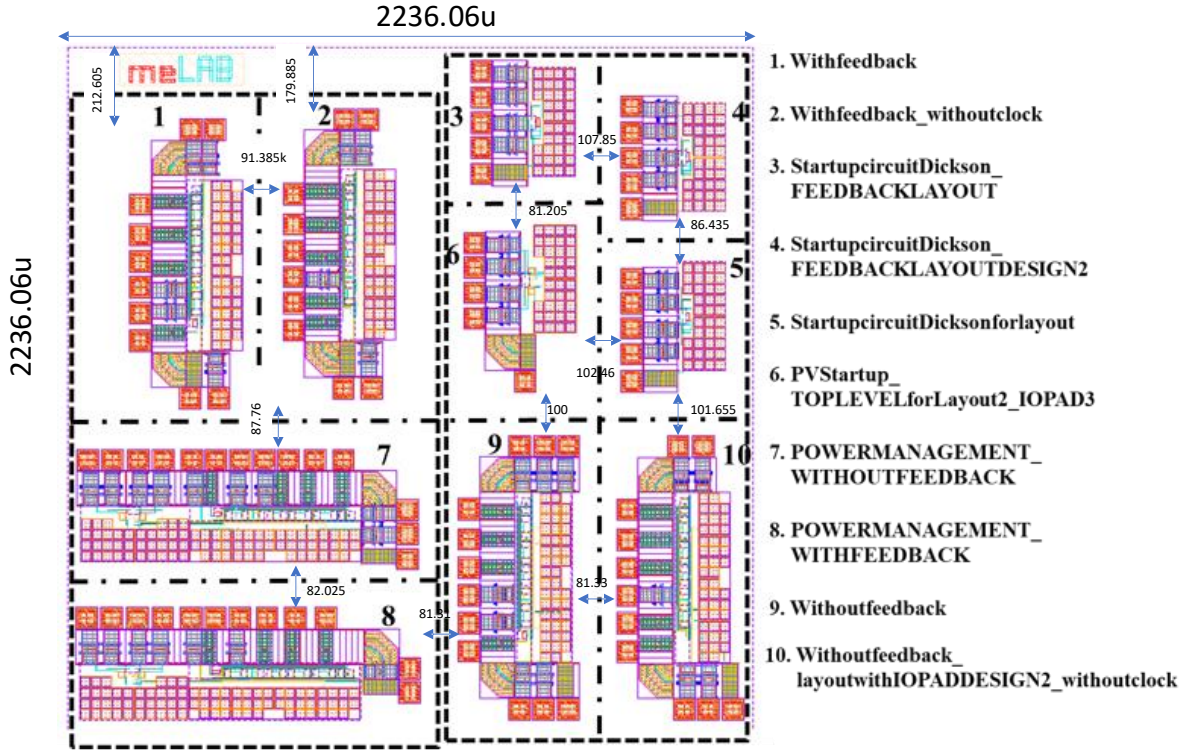


Figure A4. 1.The fabricated chip microscopic photograph.

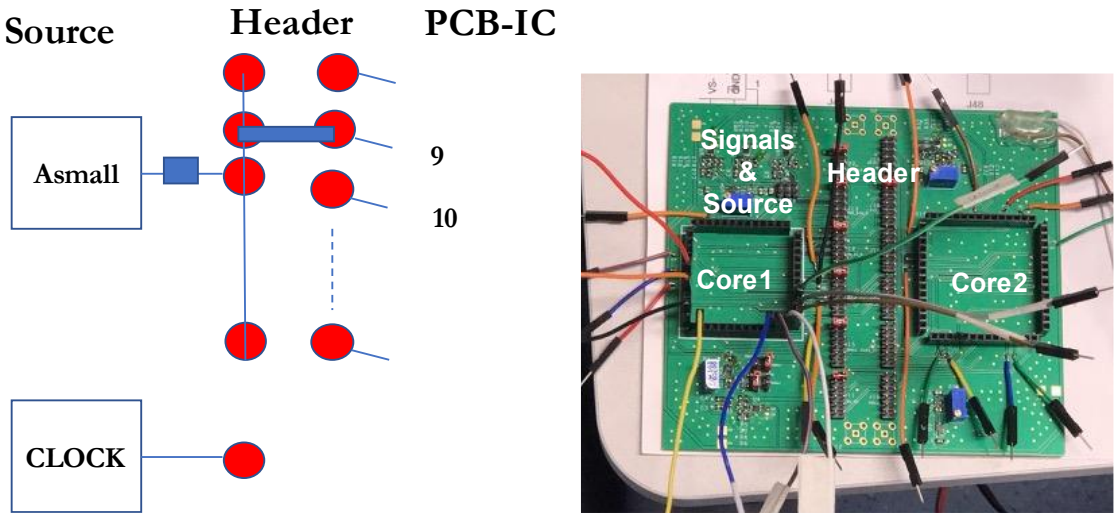


Figure A4. 2. Core 1 and Core 2 PCB manual configuration which allow testing to individual ICs.

J11 – VDD_EN		
Jp_l	Jp_r	net
1	12	1En
2	11	2En
3	10	9En
4	9	10En
5	8	7En
6	7	8En

J12 – VIN_IC_R		
Jp_l	Jp_r	net
1	12	1VIN
2	11	2VIN
3	10	9VIN
4	9	10VIN
5	8	
6	7	

J13 – VDD__DIG_R		
Jp_l	Jp_r	net
1	12	1VDIG
2	11	2DIG
3	10	9VDIG
4	9	10VDIG
5	8	
6	7	

J14 – ASMALL		
Jp_l	Jp_r	net
1	12	1Asm
2	11	2Asm
3	10	9Asm
4	9	10Asm
5	8	7Asm
6	7	8Asm

J15 – BSMALL		
Jp_l	Jp_r	net
1	12	1Bsm
2	11	2Bsm
3	10	9Bsm
4	9	10Bsm
5	8	7Bsm
6	7	8Asm

J16 – VDD3V		
Jp_l	Jp_r	net
1	12	9ODig
2	11	10O12D
3	10	7OD
4	9	
5	8	
6	7	

J17 – VPV0V6		
Jp_l	Jp_r	net
1	12	3PV
2	11	4PV
3	10	6PV
4	9	5PV
5	8	7PV
6	7	8PV

J18 – CLK1		
Jp_l	Jp_r	net
1	12	1CLK
2	11	2P1
3	10	10P1
4	9	7CLK
5	8	
6	7	

J19 – CLK2		
Jp_l	Jp_r	net
1	12	2P2
2	11	9CLK
3	10	10P2
4	9	8CLK
5	8	
6	7	

J20 – CLK1_0V6		
Jp_l	Jp_r	net
1	12	3P1
2	11	4P1
3	10	6P1
4	9	5P1
5	8	7P1
6	7	8P1

J21 – CLK2_0V6		
Jp_l	Jp_r	net
1	12	3P2
2	11	4P2
3	10	6P2
4	9	5P2
5	8	7P2
6	7	8P2

J22 – VIN_CLK_R		
Jp_l	Jp_r	net
1	8	1VCLK
2	7	9VCLK
3	6	7VCLK+DIG
4	5	8Vclk+dig

Figure A4. 3.Manual configuration table to test each ICs.

Appendix 4.2. Experimental set-up process

The experimental set up for main charge pump design – with feed-in and without feed-in are depicted in Fig. A4.4 and Fig. A4.5.

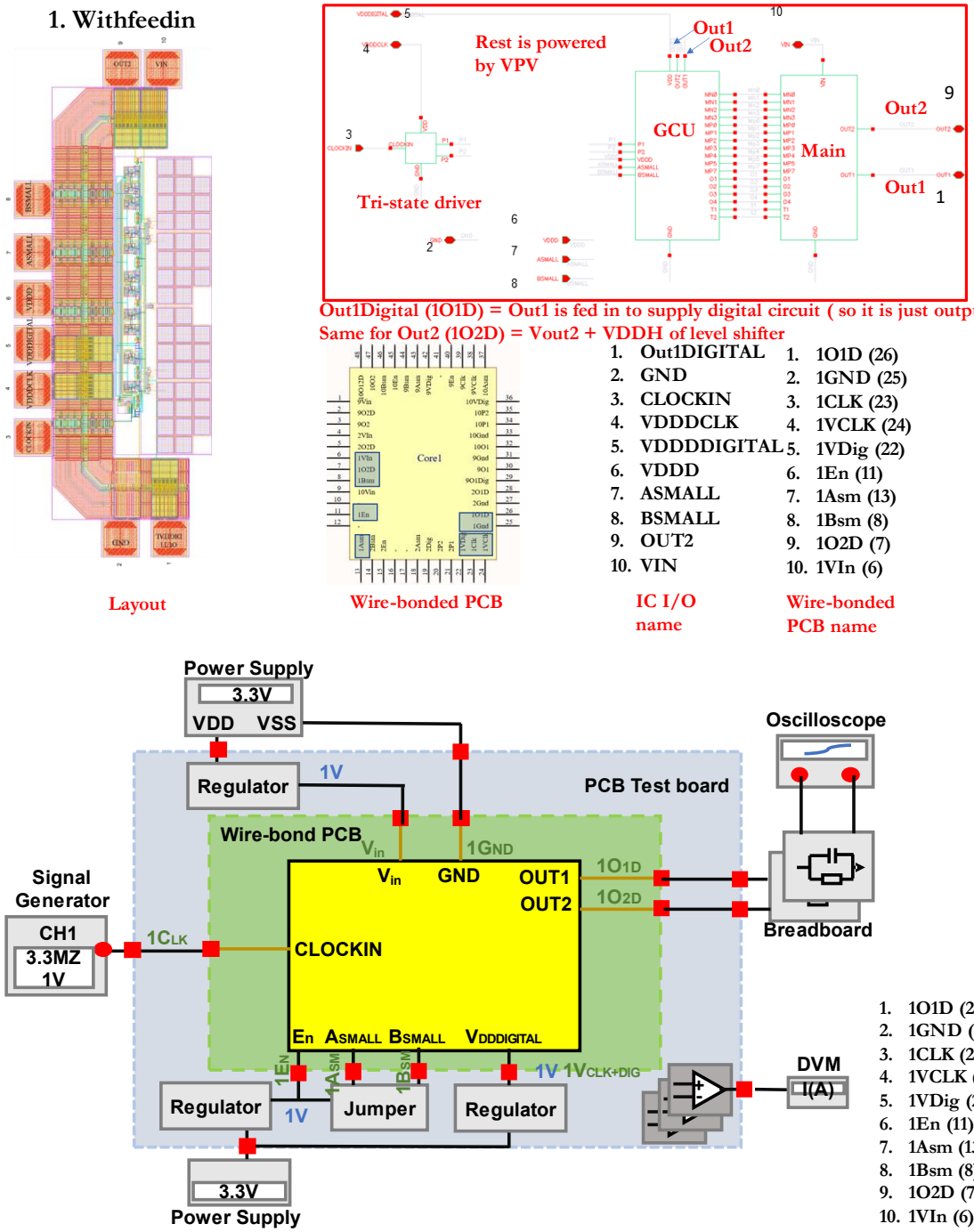
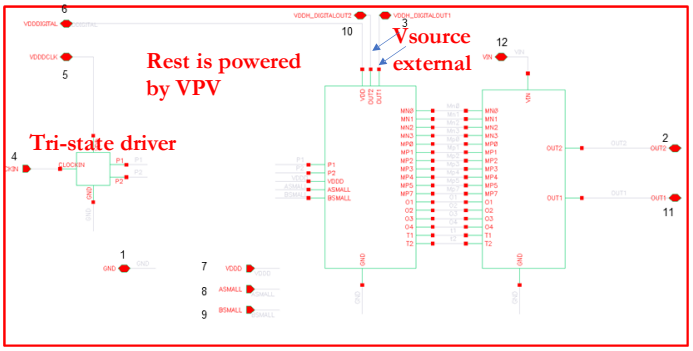
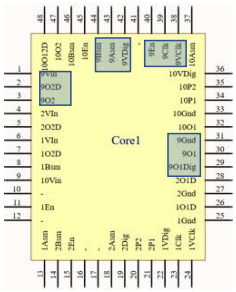


Figure A4. 4.Experimental set up of '*feed-in*' mode IC number 1 configuration from layout view to the lab environment.



9. Withoutfeedin- layoutwithIOPAD



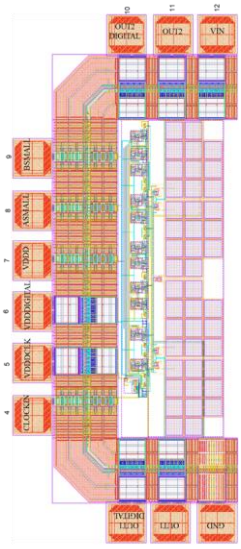
Wire-bonded PCB

1. GND
2. OUT1
3. OUT1DIGITAL
4. CLOCKIN
5. VDDCLK
6. VDDDIGITAL
7. VDDD
8. ASMALL
9. BSMALL
10. OUT2DIGITAL
11. OUT2
12. VIN

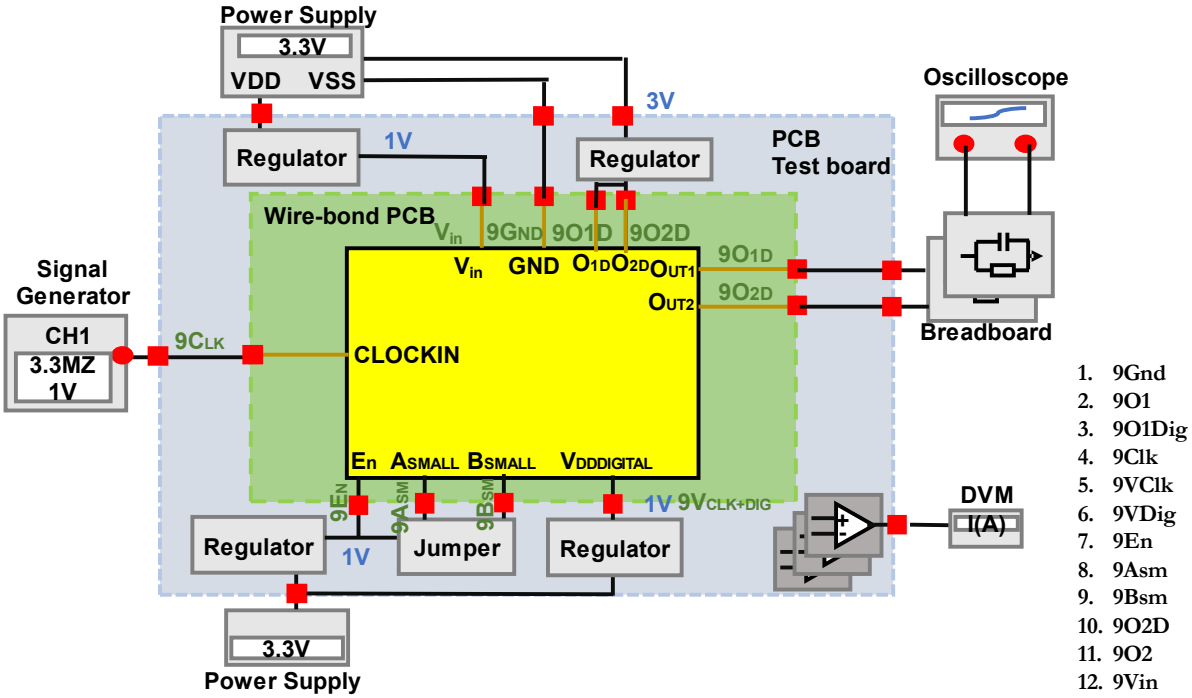
IC I/O name

1. 9Gnd
2. 9O1
3. 9O1Dig
4. 9Clk
5. 9VClk
6. 9VDig
7. 9En
8. 9Asm
9. 9Bsm
10. 9O2D
11. 9O2
12. 9Vin

Wire-bonded PCB name



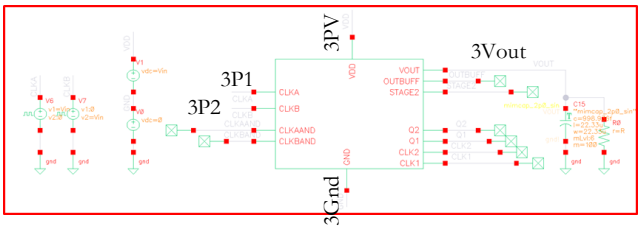
Layout



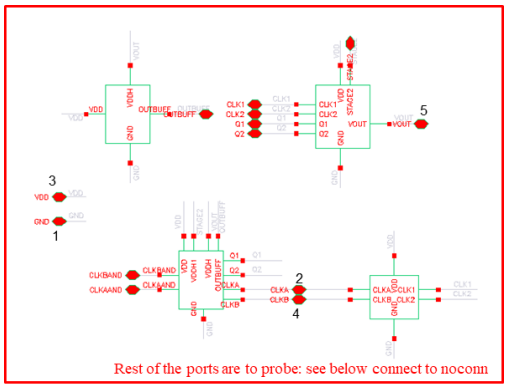
1. 9Gnd
2. 9O1
3. 9O1Dig
4. 9Clk
5. 9VClk
6. 9VDig
7. 9En
8. 9Asm
9. 9Bsm
10. 9O2D
11. 9O2
12. 9Vin

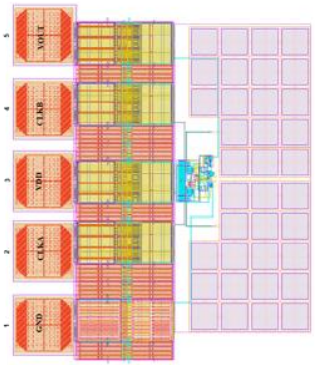
Figure A4. 5. Experimental set up of '*without feed-in/stand-alone*' mode IC number 9 configuration from layout view to the lab environment.

The microphotograph of the fabricated chip with the bank annotated Design-3 converter is depicted in Fig. A4.6. The future experimental set up for future testing strategy is illustrated in Fig. A4.6. Among 10-designs integrated into 5 mm² chip area, a fabricated chip of proposed energy saving Dickson's charge pump is wire-bonded to Core 2 transfer PCBs without dicing the individual design. IC number 3 in Fig. A4.6 and IC number 4 in Fig. A4.7 represent proposed Design-3 with different clock disabler thresholds. Meanwhile, IC number 5 in Fig A4.8 is the same circuit configuration without the clock disabler to compare with IC numbers 3 and 4.

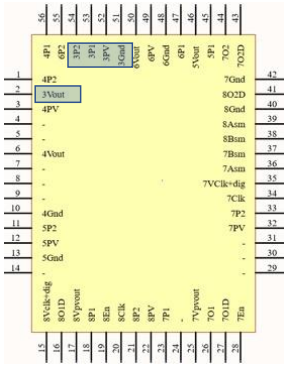


3.StartupcircuitDickson_FEEDBACKLAYOUT





Layout



Wire-bonded PCB

IC I/O name	Wire-bonded PCB name
1. GND	1. 3Gnd (51)
2. CLKA	2. 3P1 (53)
3. VDD	3. 3PV (52)
4. CLKB	4. 3P2 (54)
5. VOUT	5. 3Vout (2)

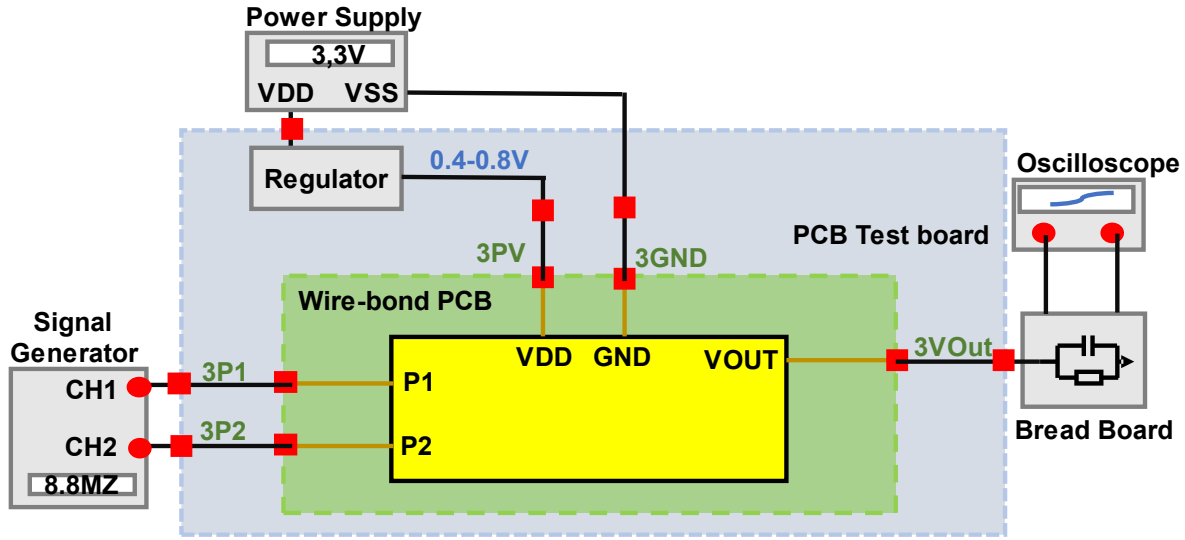
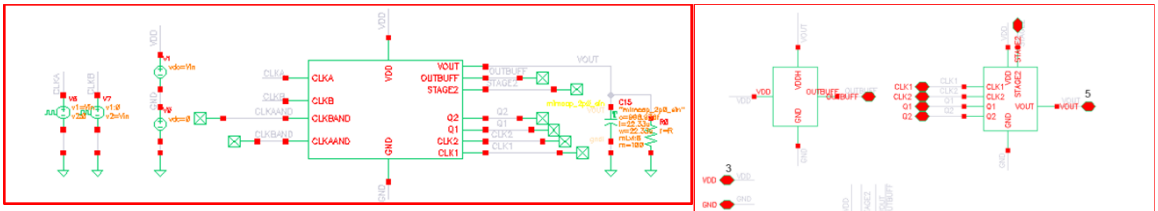
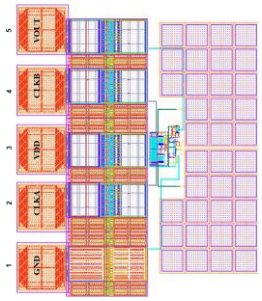
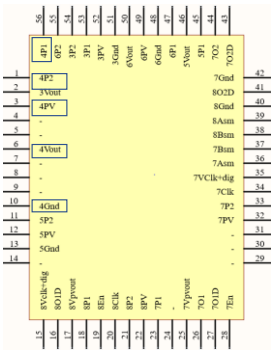


Figure A4. 6. Experimental set up of proposed Design 3 IC number 3 configuration from layout view to the lab environment.





Layout



Wire-bonded PCB

1. GND	1. 4Gnd	(10)
2. CLKA	2. 4P1	(56)
3. VDD	3. 4PV	(3)
4. CLKB	4. 4P2	(1)
5. VOUT	5. 4Vout	(6)

IC I/O name Wire-bonded PCB name

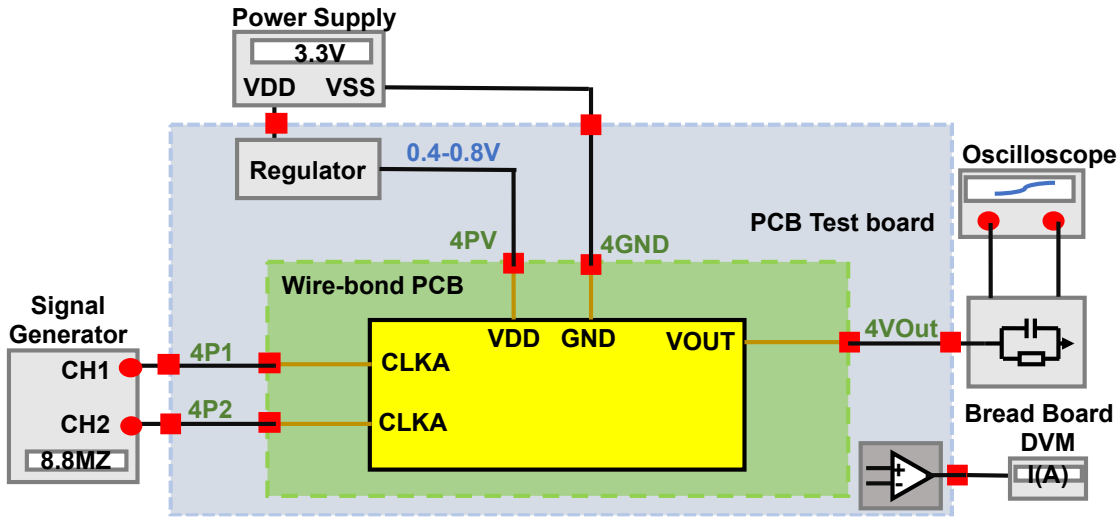
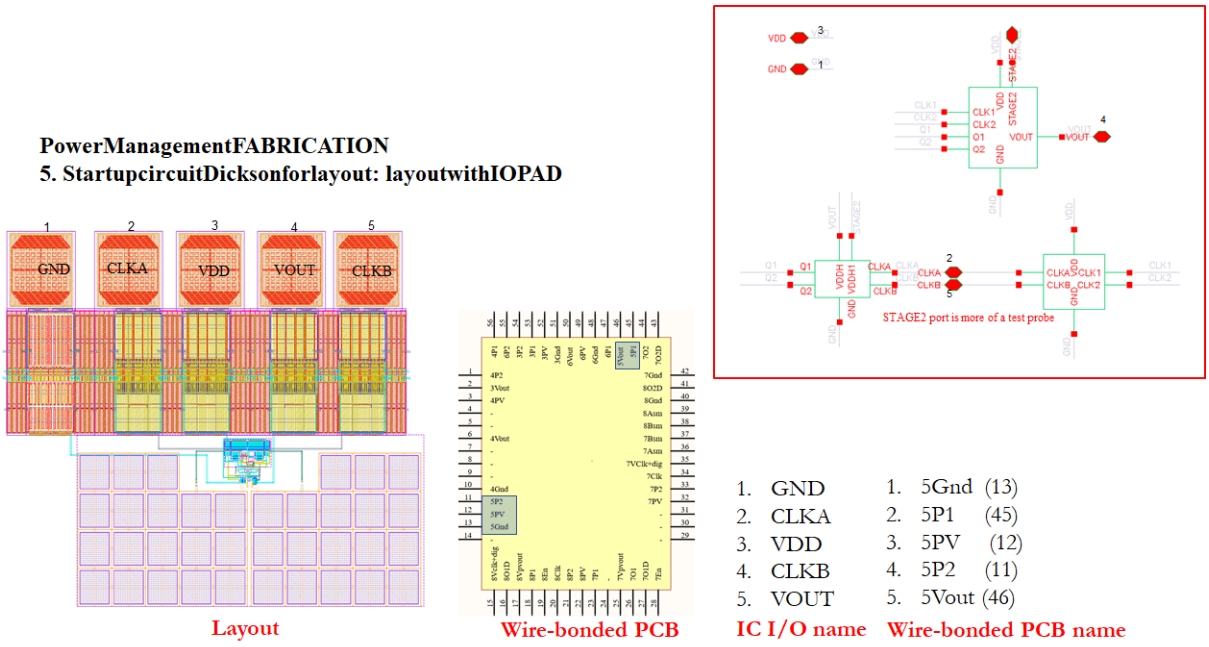


Figure A4. 7. Experimental set up of proposed Design 3 IC number 4 configuration from layout view to the lab environment.



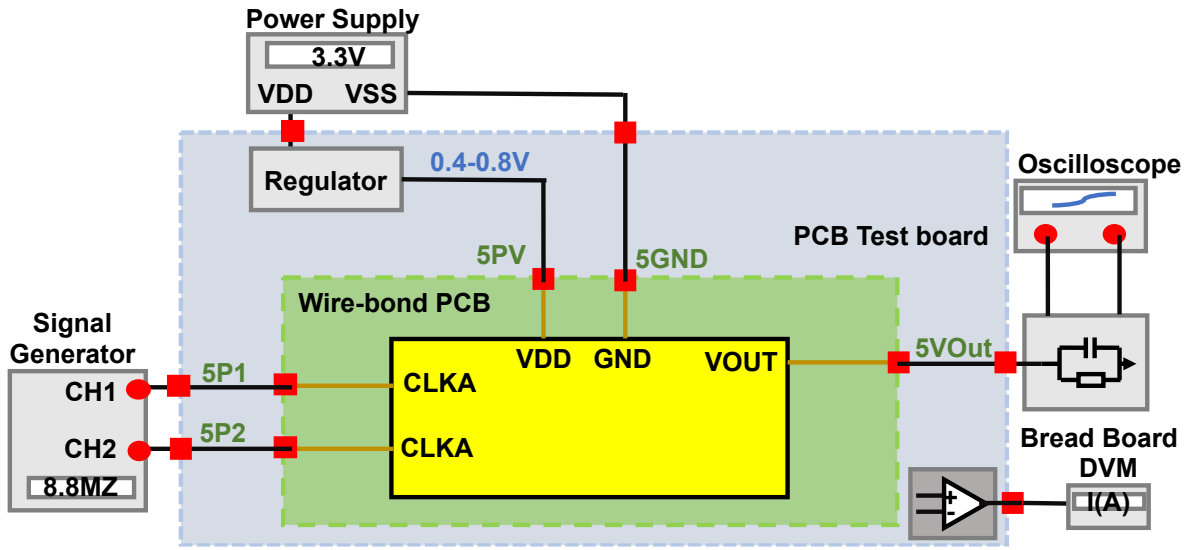
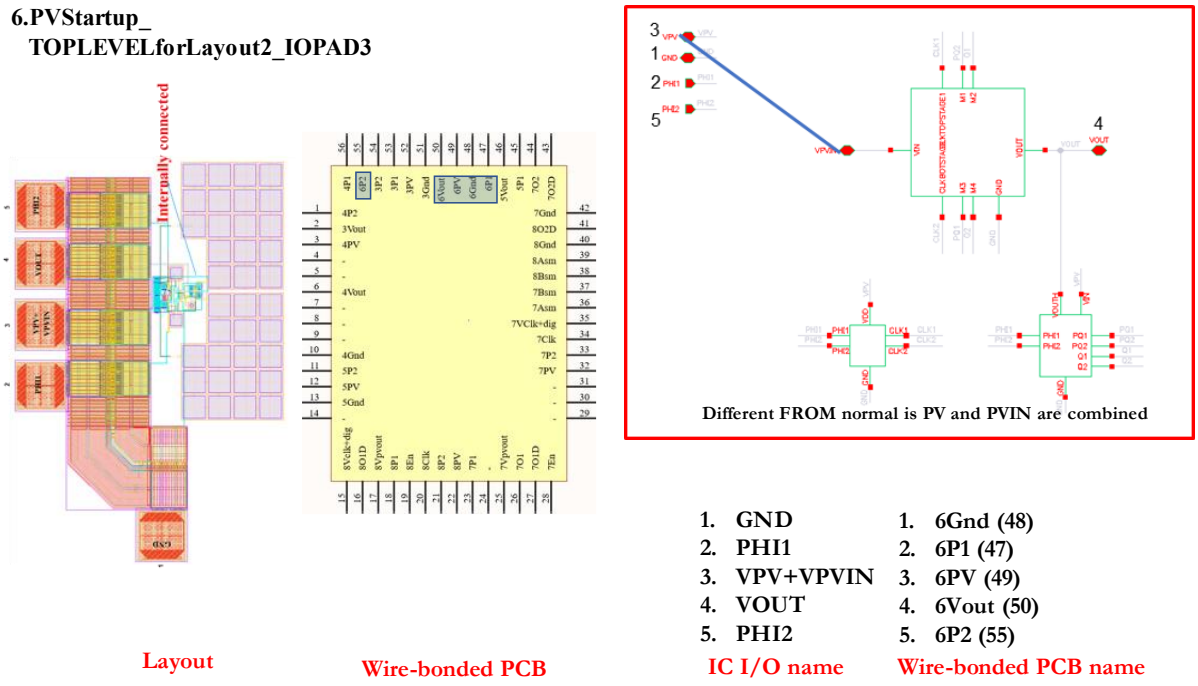


Figure A4. 8. Experimental set up of proposed Design-3 IC number 5 configuration from layout view to the lab environment.

The proposed circuit is implemented and fabricated in 180 nm TSMC RF technologies, and the back annotated chip micrograph of Design-4 is presented in Fig. A4.9. Out of 10 designs manufactured in the 5 mm2 chip area, a fabricated chip of the proposed Design-4 charge pump is wire-bonded to Core2 transfer PCBs without dicing the individual plan. The future experimental set up for IC number 5 is depicted in Fig. A4.9.



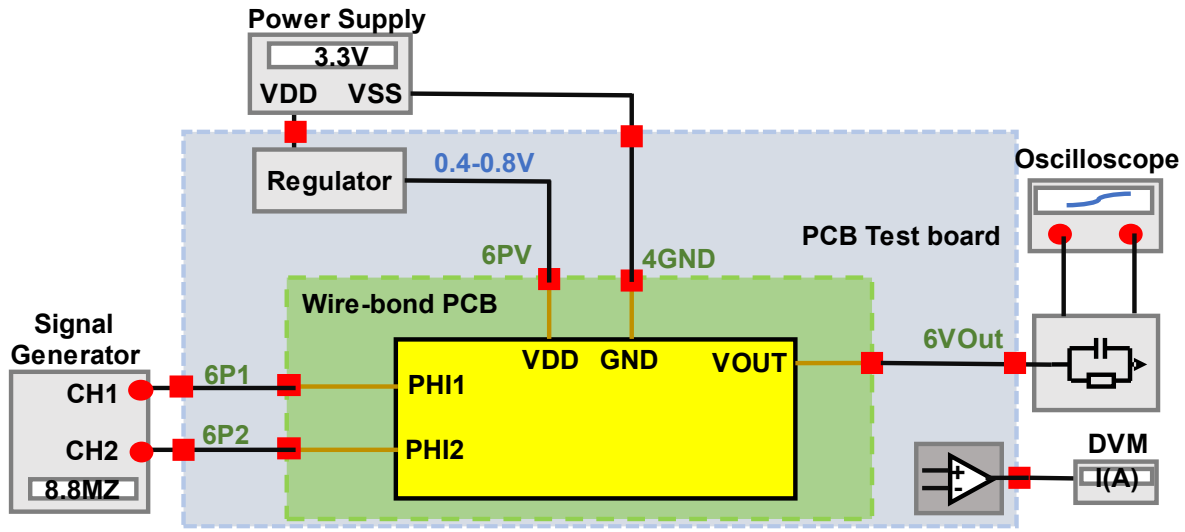
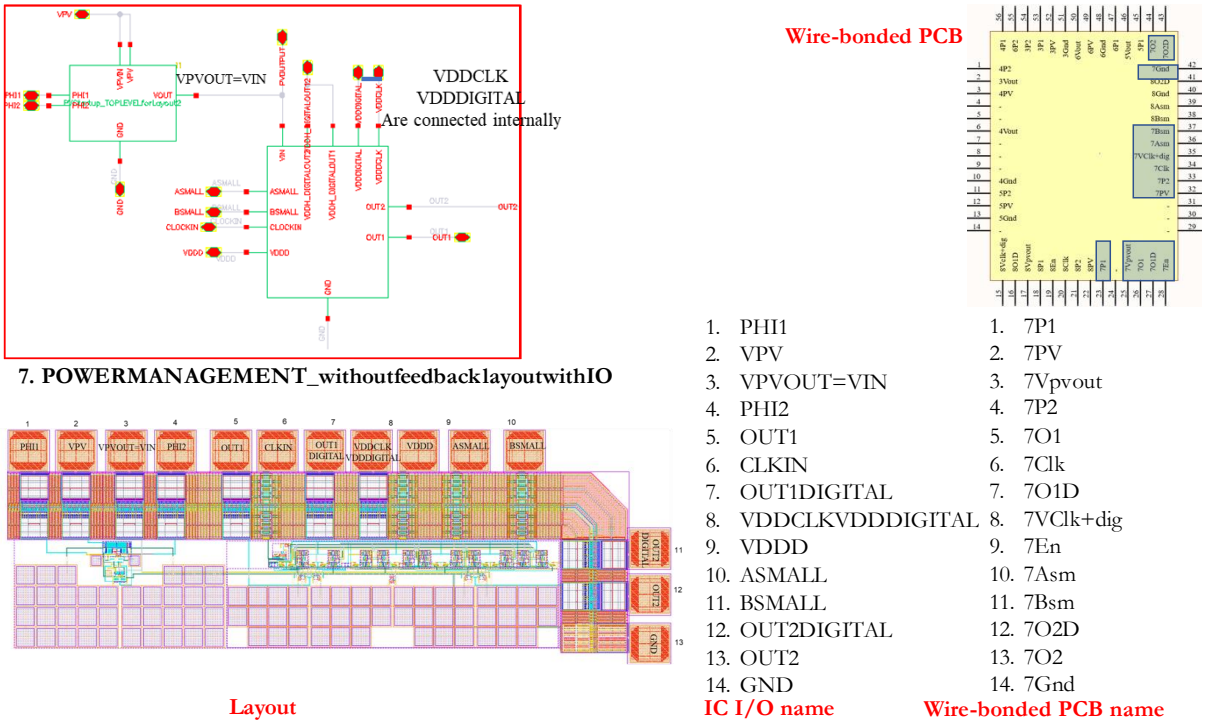


Figure A4. 9. Experimental set up of proposed Design 4 IC number 5 configuration from layout view to the lab environment.

The experimental set up for future testing strategy for the Power Management system presented in Chapter-4 is illustrated in Fig. A4.10 and Fig. A4.11. Out of 10 designs integrated into a 5-mm² chip area. PMS IC for both IC8- main charge pump with a feed-in converter (self-supplied) and IC-7 without feed-in are wire-bonded in Core-2 PCB. Similarly, the start-up converter used in this design is also implemented in Core-2. However, the individual designs of main charge pumps are wire-bonded in Core-1 PCB.



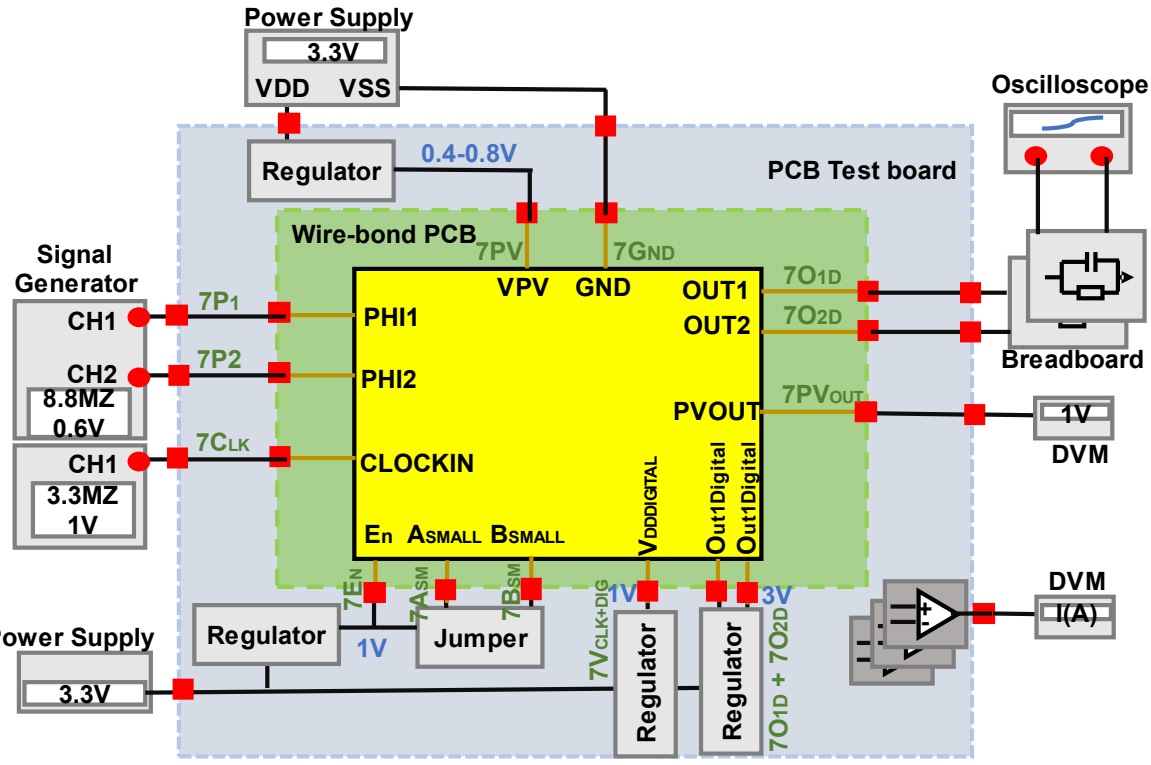
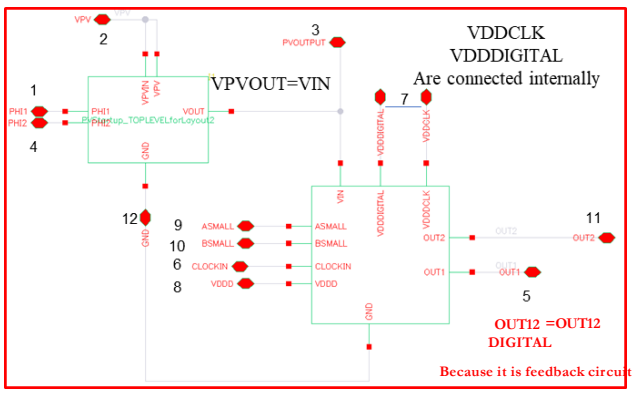
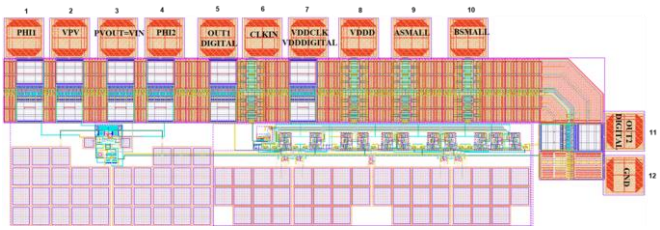


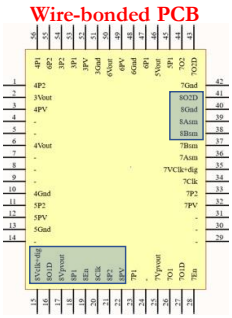
Figure A4. 10. Experimental set up of proposed I.C. number 7 configuration from layout view to the lab environment.





Layout

Wire-bonded PCB



1. PHI1	1. 8P1 (18)
2. VPV	2. 8PV (22)
3. PVOUT=VIN	3. 8PVOUT (17)
4. PHI2	4. 8P2 (21)
5. OUT1DIGITAL	5. 8O1 (16)
6. CLKIN	6. 8Clk (20)
7. VDDCLKVDDDIGITAL	7. 8Vclk+dig (15)
8. VDDD	8. 8En (19)
9. ASMALL	9. 8Asm (39)
10. BSMALL	10. 8Bsm (38)
11. OUT2DIGITAL	11. 8O2D (41)
12. GND	12. 8Gnd (40)
IC I/O name	Wire-bonded PCB name

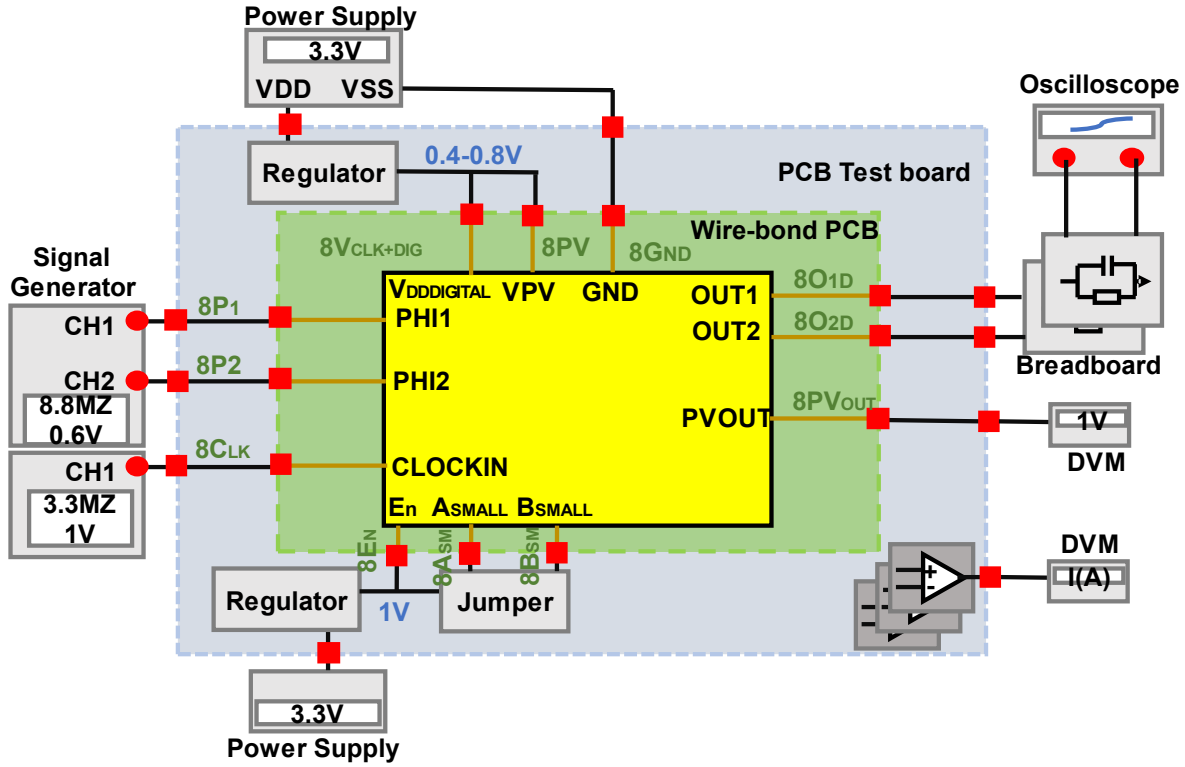
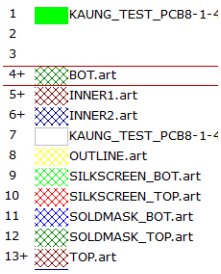
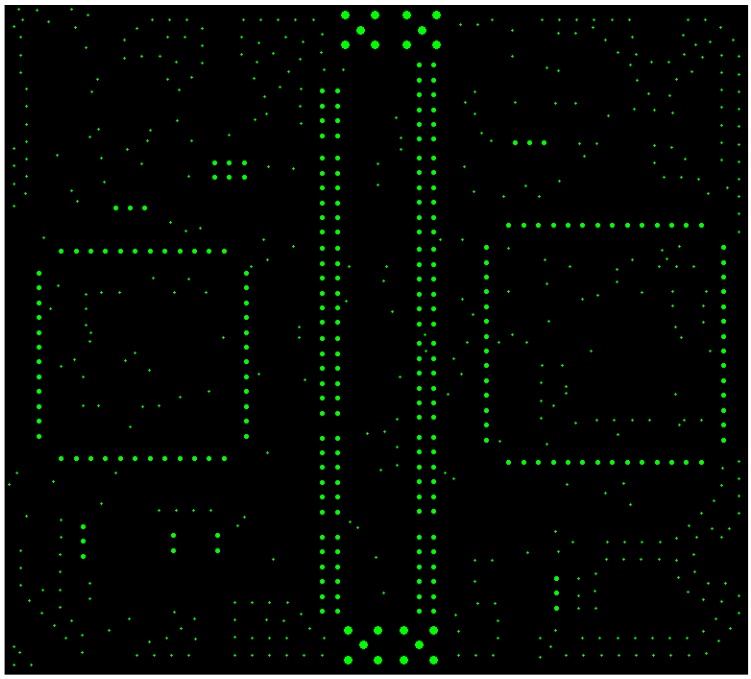


Figure A4. 11. Experimental set up of proposed I.C. number 8 configuration from layout view to the lab environment.

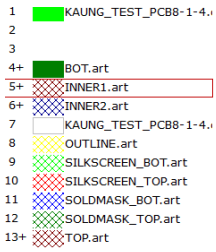
Appendix 4.4. 4-layer PCB design.

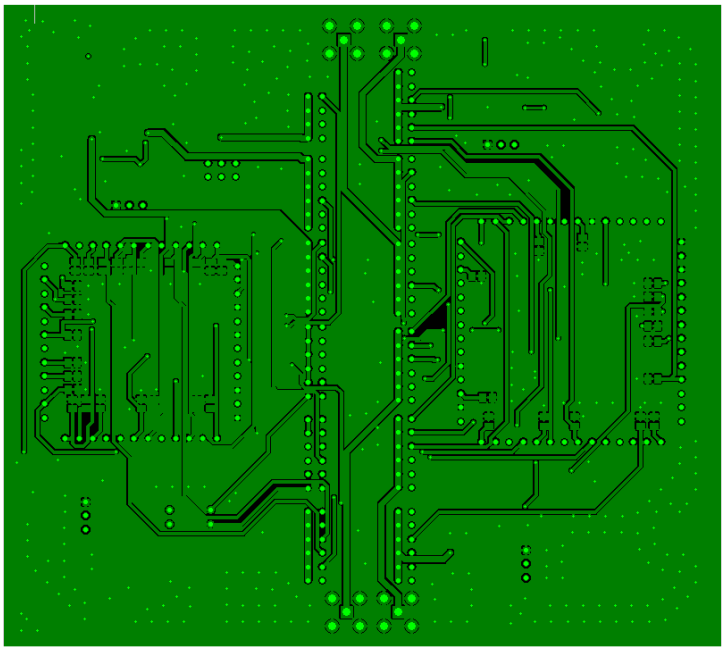
KAUNG_TEST_PCB8-1-4.drl



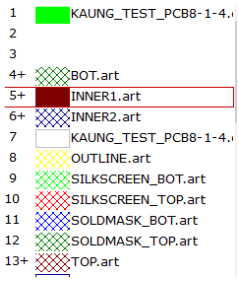


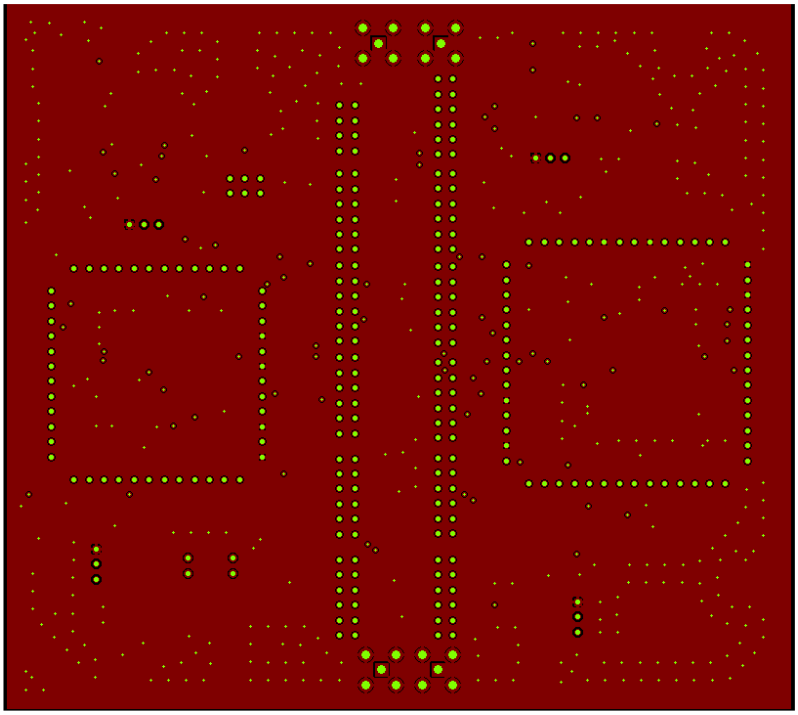
KAUNG_TEST_PCB8-1-4.drl
BOT.art





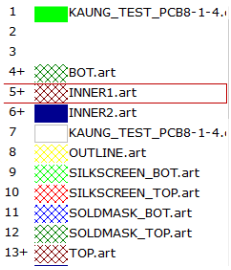
KAUNG_TEST_PCB8-1-4.drl
INNER1.art

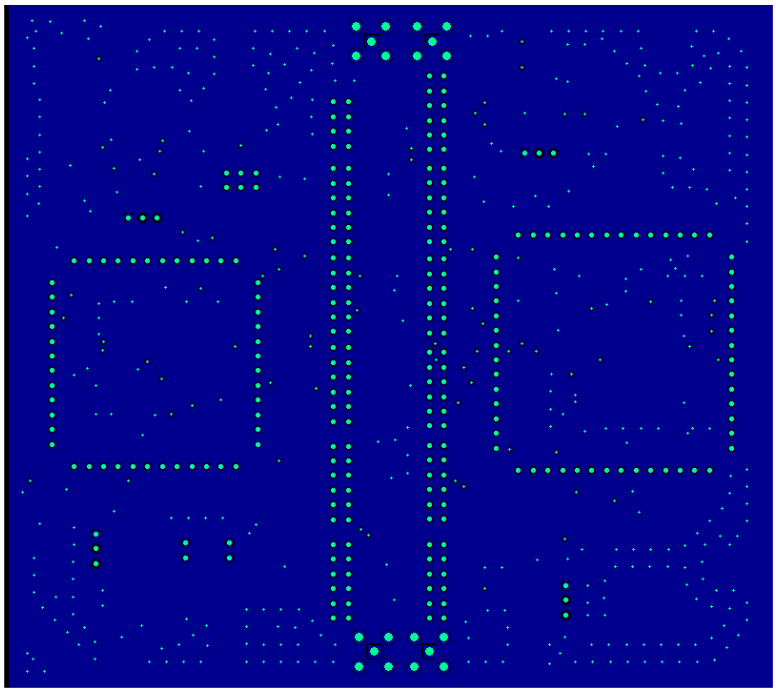




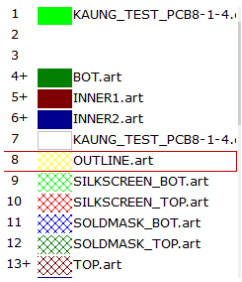
KAUNG_TEST_PCB8-1-4.drl
INNER2.art

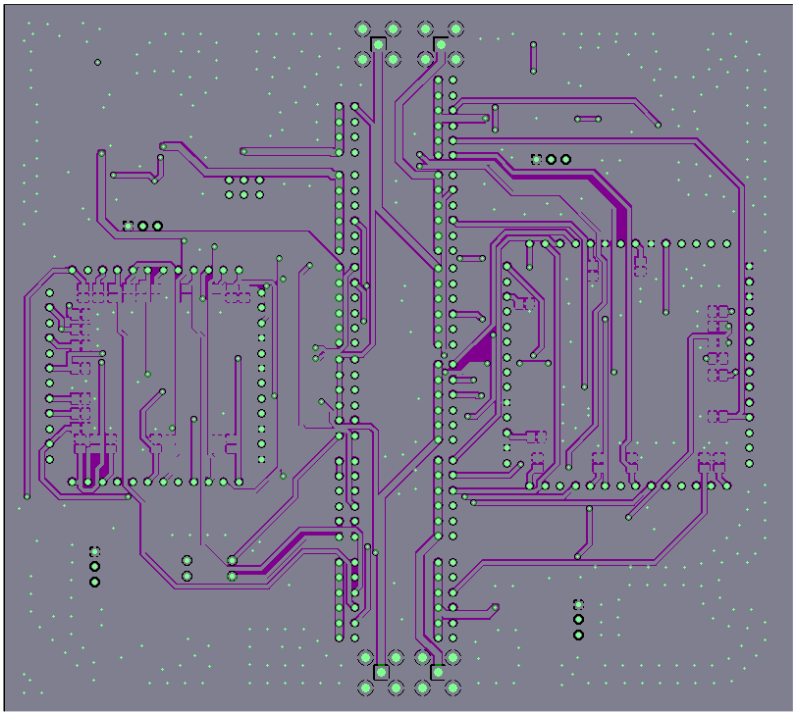
KAUNG_TEST_PCB8-1-4.drl



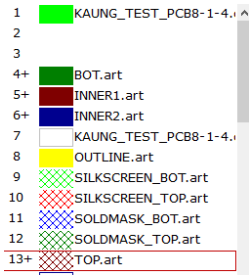


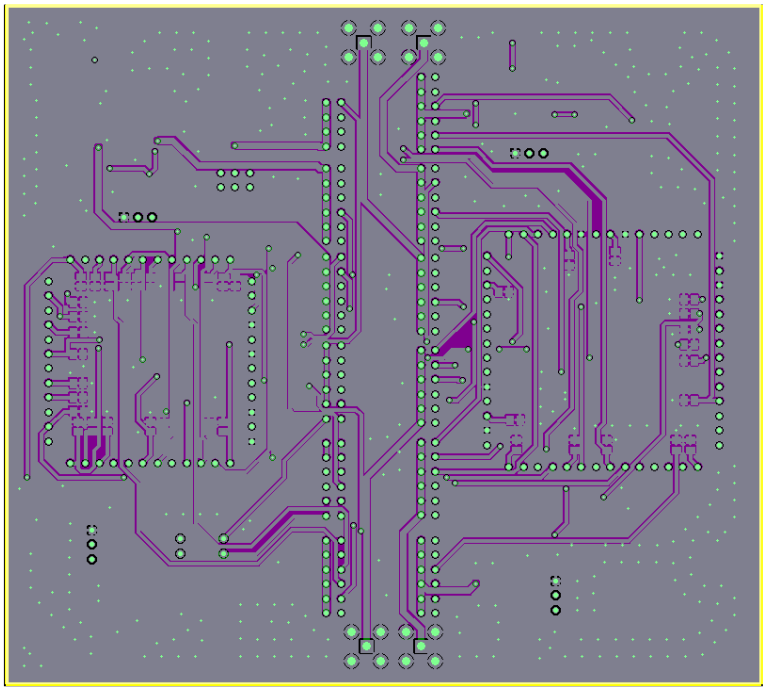
4 together



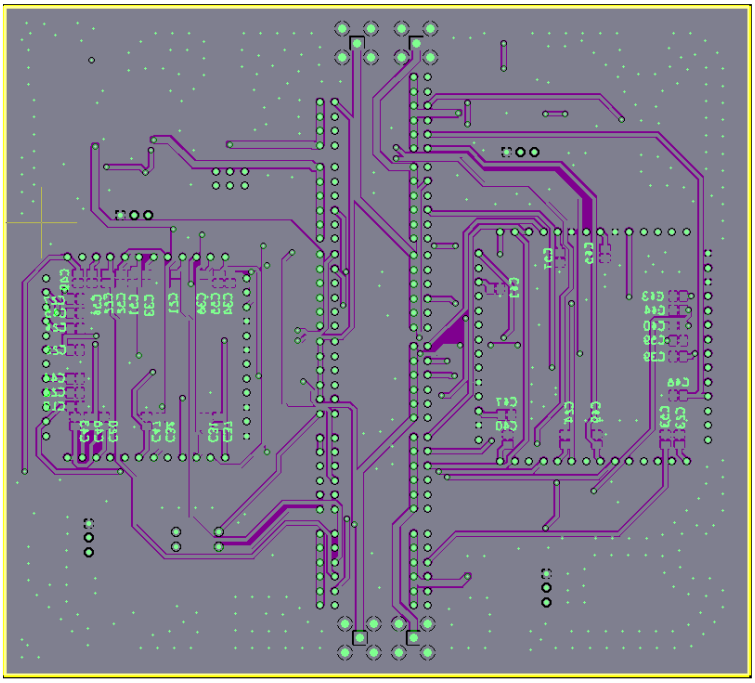


All 4+ OUTLINE.art

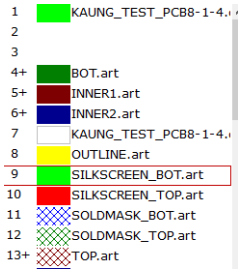


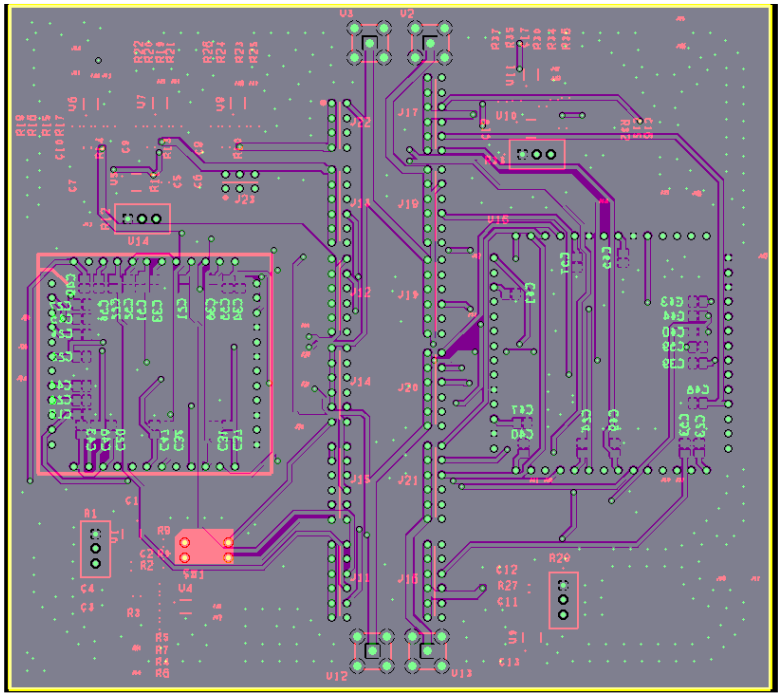


Above 5+
SILKSCREEN_BOT.art (cap names)



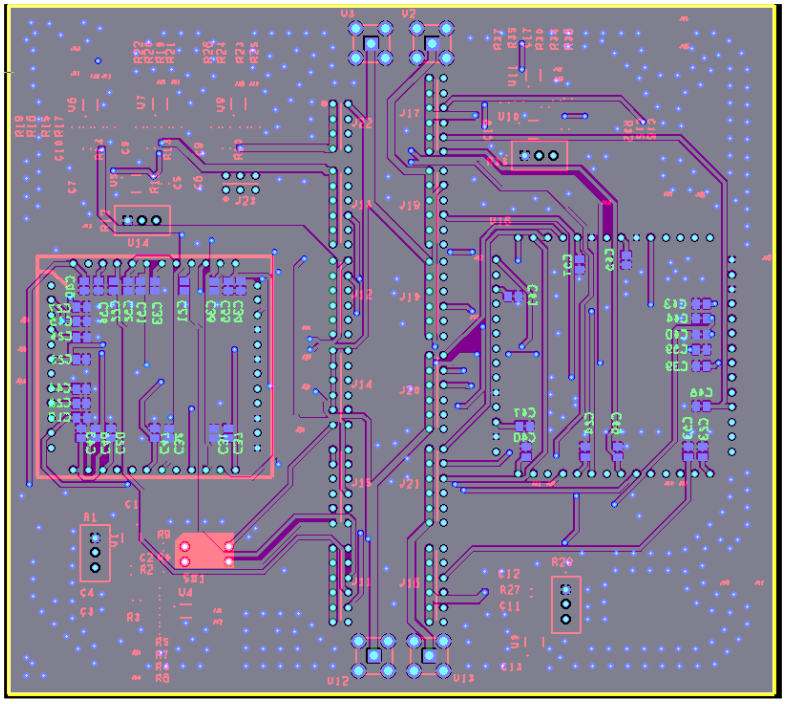
Above6+
SILKSCREEN_TOP.art (R, U paint etc)



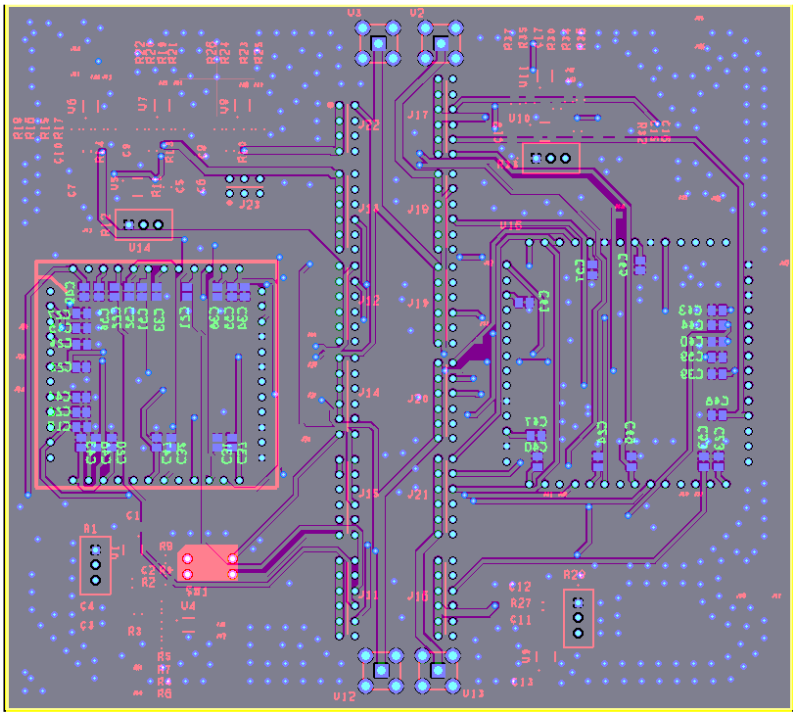


Above7+
SOLDERMASK_BOT.art

1	KAUNG_TEST_PCB8-1-4.(
2	
3	
4+	BOT.art
5+	INNER1.art
6+	INNER2.art
7	KAUNG_TEST_PCB8-1-4.(
8	OUTLINE.art
9	SILKSCREEN_BOT.art
10	SILKSCREEN_TOP.art
11	SOLDMASK_BOT.art
12	SOLDMASK_TOP.art
13+	TOP.art



Above8+
SOLDERMASK_TOP.art



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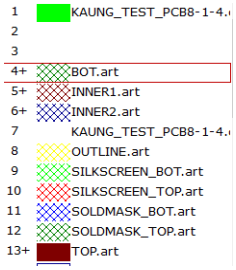

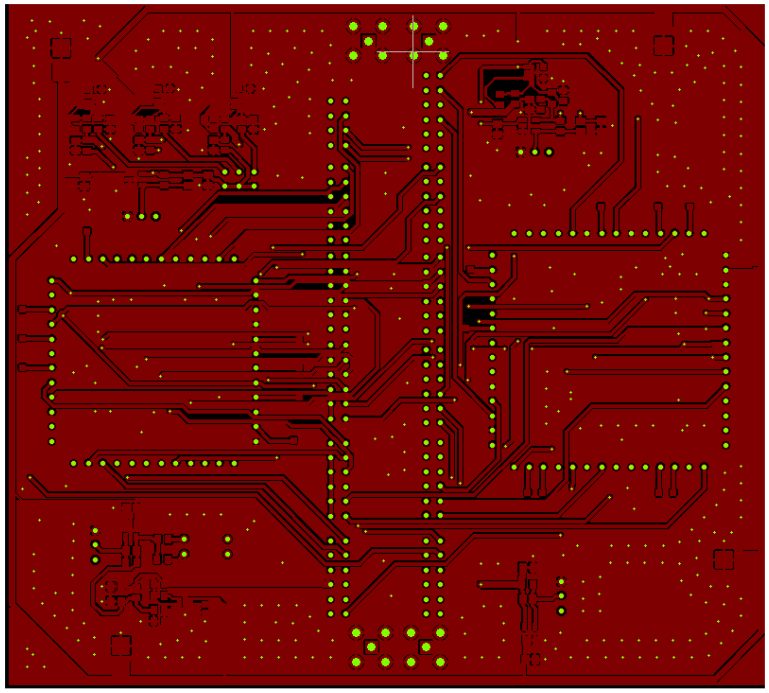

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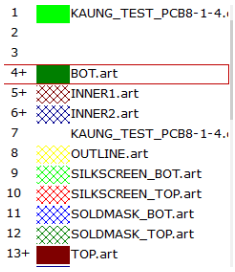
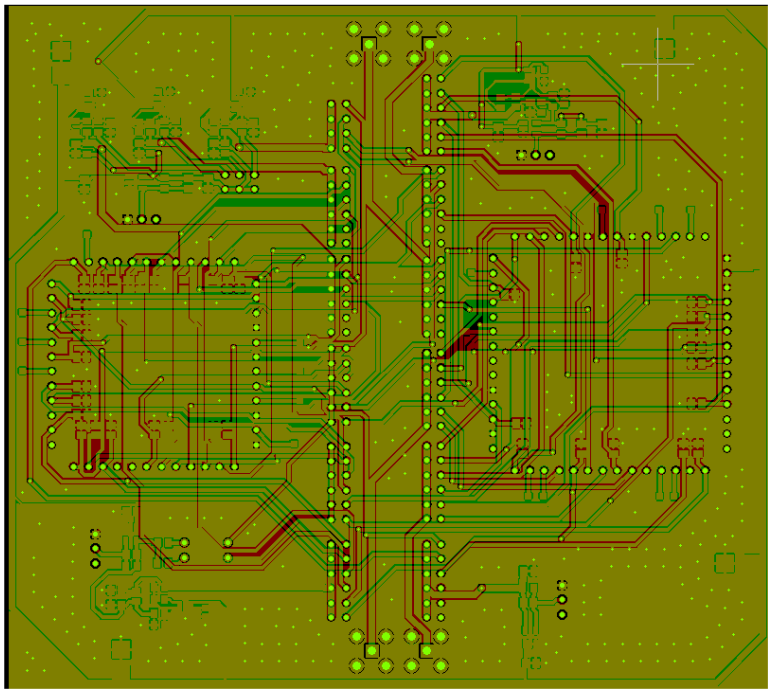
BOT.art





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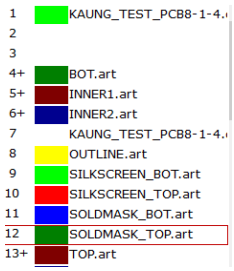
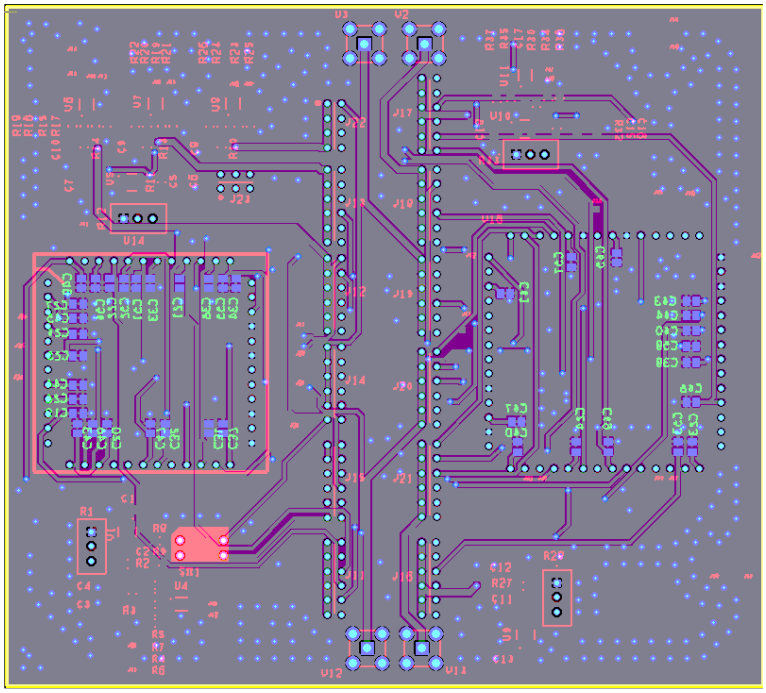
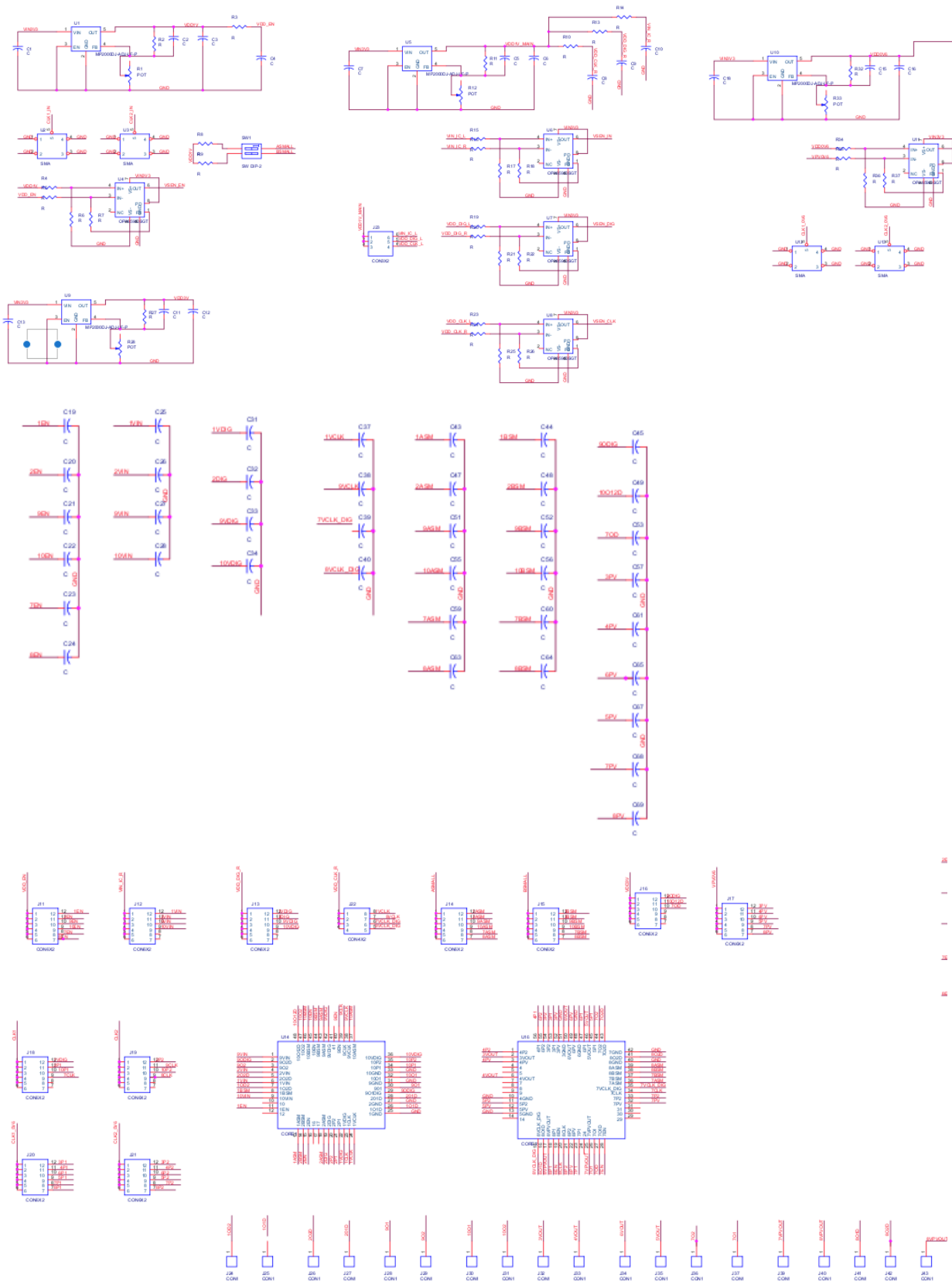




Appendix 4.5. Schematic of PCB



REFERENCES

[1] S. Vallurupalli, H. Paydak, S. Agarwal, M. Agrawal, and C. Assad-Kottner, "Wearable technology to improve education and patient outcomes in a cardiology fellowship program-a feasibility study," *Health and Technology,* vol. 3, no. 4, pp. 267-270, 2013.

[2] A. Pantelopoulos and N. G. Bourbakis, "A survey on wearable sensor-based systems for health monitoring and prognosis," *IEEE Transactions on Systems, Man, and Cybernetics, Part C (Applications and Reviews),* vol. 40, no. 1, pp. 1-12, 2009.

[3] S. Park and S. Jayaraman, "Enhancing the quality of life through wearable technology," *IEEE Engineering in medicine and biology magazine,* vol. 22, no. 3, pp. 41-48, 2003.

[4] R. Das, F. Moradi, and H. Heidari, "Biointegrated and Wirelessly Powered Implantable Brain Devices: A Review," *IEEE Transactions on Biomedical Circuits and Systems,* vol. 14, no. 2, pp. 343-358, 2020.

[5] N. Sultan, "Reflective thoughts on the potential and challenges of wearable technology for healthcare provision and medical education," *International Journal of Information Management,* vol. 35, no. 5, pp. 521-526, 2015.

[6] M. H. Iqbal, A. Aydin, O. Brunckhorst, P. Dasgupta, and K. Ahmed, "A review of wearable technology in medicine," *Journal of the Royal Society of Medicine,* vol. 109, no. 10, pp. 372-380, 2016.

[7] A. Rashidi, K. Laursen, S. Hosseini, H.-A. Huynh, and F. Moradi, "An implantable ultrasonically powered system for optogenetic stimulation with power-efficient active rectifier and charge-reuse capability," *Ieee Transactions on Biomedical Circuits and Systems,* vol. 13, no. 6, pp. 1362-1371, 2019.

[8] E. Covi *et al.*, "Adaptive Extreme Edge Computing for Wearable Devices," *arXiv preprint arXiv:2012.14937,* 2020.

[9] H. Heidari, E. Bonizzoni, U. Gatti, and F. Maloberti, "A CMOS current-mode magnetic Hall sensor with integrated front-end," *IEEE Transactions on Circuits and Systems I: Regular Papers,* vol. 62, no. 5, pp. 1270-1278, 2015.

[10] I. Williams and T. G. Constandinou, "An energy-efficient, dynamic voltage scaling neural stimulator for a proprioceptive prosthesis," *IEEE Transactions on Biomedical Circuits and Systems,* vol. 7, no. 2, pp. 129-139, 2013.

[11] A. Shtukater, "Smart contact lens," ed: Google Patents, 2020.

[12] A. V. Quintero, P. Pérez-Merino, and H. De Smet, "Artificial iris performance for smart contact lens vision correction applications," *Scientific reports,* vol. 10, no. 1, pp. 1-12, 2020.

[13] M. Nasreldin, R. Delattre, M. Ramuz, C. Lahuec, T. Djenizian, and J.-L. de Bougrenet de la Tocnaye, "Flexible micro-battery for powering smart contact lens," *Sensors,* vol. 19, no. 9, p. 2062, 2019.

[14] J. Park *et al.*, "Soft, smart contact lenses with integrations of wireless circuits, glucose sensors, and displays," *Science Advances,* vol. 4, no. 1, p. eaap9841, 2018.

[15] M. Yuan *et al.*, "Electronic Contact Lens: A Platform for Wireless Health Monitoring Applications," *Advanced Intelligent Systems,* vol. 2, no. 4, p. 1900190, 2020.

[16] R. M. Al-Eidan, H. Al-Khalifa, and A. M. Al-Salman, "A review of wrist-worn wearable: Sensors, models, and challenges," *Journal of Sensors*, 2018.

[17] J. Li, X. Hu, and Y. Wenjun, "Intelligent health wristband," ed: Google Patents, 2019.

[18] J. Sun and Y. Liu, "Using Smart Bracelets to Assess Heart Rate Among Students During Physical Education Lessons: Feasibility, Reliability, and Validity Study," *JMIR mHealth and uHealth,* vol. 8, no. 8, p. e17699, 2020.

[19] P. Shi, J. Du, F. Fang, H. Yu, and J. Liu, "Design and Implementation of an Intelligent Analgesic Bracelet Based on Wrist-ankle Acupuncture," *IEEE Transactions on Biomedical Circuits and Systems,* vol. 14, no. 6, pp. 1431-1440, 2020.

[20] X. Liang *et al.*, "Fusion of Wearable and Contactless Sensors for Intelligent Gesture Recognition," *Advanced Intelligent Systems,* vol. 1, no. 7, p. 1900088, 2019.

[21] I. H. Lee, "Power Management Circuits for Miniature Sensor Systems," Ph.D Dissertation and Thesis, 2014.

[22] M. N. Hasan, S. Sahlan, K. Osman, and M. S. Mohamed Ali, "Energy Harvesters for Wearable Electronics and Biomedical Devices," *Advanced Materials Technologies,* vol. 6, no. 3, p. 2000771, 2021.

[23] Y.-W. Chong, W. Ismail, K. Ko, and C.-Y. Lee, "Energy harvesting for wearable devices: A review," *IEEE Sensors Journal,* vol. 19, no. 20, pp. 9047-9062, 2019.
[24] J. Zhao *et al.*, "Simulation of crystalline silicon photovoltaic cells for wearable applications," *IEEE Access,* vol. 9, pp.20868-20877, 2020.
[25] J. Zhao, R. Ghannam, M. K. Law, M. A. Imran, and H. Heidari, "Photovoltaic Power Harvesting Technologies in Biomedical Implantable Devices Considering the Optimal Location," *IEEE Journal of Electromagnetics, RF and Microwaves in Medicine and Biology,* vol. 4.2, pp.148-155, 2019.
[26] Z. Chen, M.-K. Law, P.-I. Mak, and R. P. Martins, "A single-chip solar energy harvesting IC using integrated photodiodes for biomedical implant applications," *IEEE transactions on biomedical circuits and systems,* vol. 11, no. 1, pp. 44-53, 2016.
[27] A. Mahmoud, M. Alhawari, B. Mohammad, H. Saleh, and M. Ismail, "A charge pump based power management unit with 66%-efficiency in 65 nm CMOS," in *IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 1-4, 2018.
[28] M.-D. Ker and K.-C. Hsu, "Overview of on-chip electrostatic discharge protection design with SCR-based devices in CMOS integrated circuits," *IEEE Transactions on device and materials reliability,* vol. 5, no. 2, pp. 235-249, 2005.
[29] A. Khaligh, P. Zeng, and C. Zheng, "Kinetic energy harvesting using piezoelectric and electromagnetic technologies—state of the art," *IEEE transactions on industrial electronics,* vol. 57, no. 3, pp. 850-860, 2009.
[30] G. Chen, S. Hanson, D. Blaauw, and D. Sylvester, "Circuit design advances for wireless sensing applications," *Proceedings of the IEEE,* vol. 98, no. 11, pp. 1808-1827, 2010.
[31] K. Pietrzyk, J. Soares, B. Ohara, and H. Lee, "Power generation modeling for a wearable thermoelectric energy harvester with practical limitations," *Applied energy,* vol. 183, pp. 218-228, 2016.
[32] S.-W. Wang, Y.-W. Ke, P.-C. Huang, and P.-H. Hsieh, "Electromagnetic energy harvester interface design for wearable applications," *IEEE Transactions on Circuits and Systems II: Express Briefs,* vol. 65, no. 5, pp. 667-671, 2018.
[33] G. Singh and S. Kundu, "An efficient DC-DC boost converter for thermoelectric energy harvesting," *AEU-International Journal of Electronics and Communications,* vol. 118, p. 153132, 2020.
[34] Y.-J. Park *et al.*, "A design of a 92.4% efficiency triple mode control DC–DC buck converter with low power retention mode and adaptive zero current detector for IoT/wearable applications," *IEEE Transactions on Power Electronics,* vol. 32, no. 9, pp. 6946-6960, 2016.
[35] N. Butzen and M. S. Steyaert, "Design of soft-charging switched-capacitor DC–DC converters using stage outphasing and multiphase soft-charging," *IEEE Journal of Solid-State Circuits,* vol. 52, no. 12, pp. 3132-3141, 2017.
[36] M. Vasic, S. Round, J. Biela, and J. W. Kolar, "Mission profile based optimization of a synchronous-buck DC-DC converter for a wearable power system," in *IEEE 6th International Power Electronics and Motion Control Conference*, pp. 1384-1389, 2009.
[37] K. O. Htet, H. Heidari, F. Moradi, and R. Ghannam, "Energy-Efficient Start-up Dickson Charge Pump for Batteryless Biomedical Implant Devices," in *27th IEEE International Conference on Electronics, Circuits and Systems (ICECS)*, pp. 1-4, 2020.
[38] H.-P. Le, S. R. Sanders, and E. Alon, "Design techniques for fully integrated switched-capacitor DC-DC converters," *IEEE Journal of Solid-State Circuits,* vol. 46, no. 9, pp. 2120-2131, 2011.
[39] W.-H. Ki, F. Su, and C.-Y. Tsui, "Charge redistribution loss consideration in optimal charge pump design," in *IEEE International Symposium on Circuits and Systems*, pp. 1895-1898, 2005.
[40] F. Su, W.-H. Ki, and C.-Y. Tsui, "High efficiency cross-coupled doubler with no reversion loss," in *2006 IEEE International Symposium on Circuits and Systems*, pp. 4 pp.-2764, 2006.
[41] Y. Zhang, Y. Gao, J. Li, and M. Sumner, "Interleaved switched-capacitor bidirectional dc-dc converter with wide voltage-gain range for energy storage systems," *IEEE Transactions on Power Electronics,* vol. 33, no. 5, pp. 3852-3869, 2017.
[42] S. Li, Y. Zheng, and K. M. Smedley, "A family of step-up resonant switched-capacitor converter with a continuously adjustable conversion ratio," *IEEE Transactions on Power Electronics,* vol. 34, no. 1, pp. 378-390, 2018.
[43] W. Xie *et al.*, "A Step-up Series-parallel Resonant Switched-capacitor Converter with Extended Line Regulation Range," in *2019 IEEE Applied Power Electronics Conference and Exposition (APEC)*, pp. 2150-2154, 2019.

[44] S. Li, Y. Zheng, B. Wu, and K. M. Smedley, "A family of resonant two-switch boosting switched-capacitor converter with ZVS operation and a wide line regulation range," *IEEE Transactions on Power Electronics,* vol. 33, no. 1, pp. 448-459, 2017.

[45] Y. Yang, Y. Zhao, and G. Dong, "A multi-output on-chip switched-capacitor DC–DC converter with unequal flying capacitors for different power modes," *Journal of Circuits, Systems and Computers,* vol. 24, no. 04, p. 1550051, 2015.

[46] S. P. Lin and M. D. Ker, "Design of multiple-charge-pump system for implantable biomedical applications," in *IEEE Biomedical Circuits and Systems Conference (BioCAS)*, 2018: IEEE, pp. 1-4, 2018.

[47] D. Ma and R. Bondade, "Reconfigurable switched-capacitor power converters," in *Reconfigurable switched-capacitor power converters*: Springer, 2013, pp. 71-110.

[48] M. Krstic, S. Eren, and P. Jain, "Analysis and Design of Multiphase, Reconfigurable Switched-Capacitor Converters," *IEEE Journal of Emerging and Selected Topics in Power Electronics,* vol. 8, no. 4, pp. 4046-4059, 2019.

[49] J. De Smet, "The smart contact lens: From an artificial iris to a contact lens display," Ghent University, Ph.D Dissertation, 2014.

[50] F. De Roose *et al.*, "An active artificial iris controlled by a 25-μW flexible thin-film driver," in *2016 IEEE International Electron Devices Meeting (IEDM)*, pp. 32.1. 1-32.1. 4, 2016.

[51] J. A. Nelson, *The physics of solar cells*. World Scientific Publishing Company, 2003.

[52] J. Harper and X.-d. Wang, "I-V, CV and AC Impedance Techniques and Characterizations of Photovoltaic Cells," in *第七届中国功能材料及其应用学术会议论文集 (第 5 分册)*, 2010.

[53] J. Sohn, S. B. Choi, and D. Lee, "An investigation on piezoelectric energy harvesting for MEMS power sources," *Proceedings of the Institution of Mechanical Engineers, Part C: Journal of Mechanical Engineering Science,* vol. 219, no. 4, pp. 429-436, 2005.

[54] Y. Yan, J. E. Zhou, D. Maurya, Y. U. Wang, and S. Priya, "Giant piezoelectric voltage coefficient in grain-oriented modified PbTiO 3 material," *Nature communications,* vol. 7, no. 1, pp. 1-10, 2016.

[55] X.-Z. Chen *et al.*, "Magnetoelectric micromachines with wirelessly controlled navigation and functionality," *Materials Horizons,* vol. 3, no. 2, pp. 113-118, 2016.

[56] A. Khan, Z. Abas, H. S. Kim, and I.-K. Oh, "Piezoelectric thin films: an integrated review of transducers and energy harvesting," *Smart Materials and Structures,* vol. 25, no. 5, p. 053002, 2016.

[57] Q. Shi, T. Wang, and C. Lee, "MEMS based broadband piezoelectric ultrasonic energy harvester (PUEH) for enabling self-powered implantable biomedical devices," *Scientific reports,* vol. 6, p. 24946, 2016.

[58] M. Zhou, L. Deng, D. Wen, L. Shang, L. Jin, and S. Dong, "Highly ordered mesoporous carbons-based glucose/O2 biofuel cell," *Biosensors and Bioelectronics,* vol. 24, no. 9, pp. 2904-2908, 2009.

[59] J. Y. Lee, H. Y. Shin, S. W. Kang, C. Park, and S. W. Kim, "Application of an enzyme-based biofuel cell containing a bioelectrode modified with deoxyribonucleic acid-wrapped single-walled carbon nanotubes to serum," *Enzyme and microbial technology,* vol. 48, no. 1, pp. 80-84, 2011.

[60] J. Katic, S. Rodriguez, and A. Rusu, "A high-efficiency energy harvesting interface for implanted biofuel cell and thermal harvesters," *IEEE Transactions on Power Electronics,* vol. 33, no. 5, pp. 4125-4134, 2017.

[61] Y. Tan, W. Deng, B. Ge, Q. Xie, J. Huang, and S. Yao, "Biofuel cell and phenolic biosensor based on acid-resistant laccase–glutaraldehyde functionalized chitosan–multiwalled carbon nanotubes nanocomposite film," *Biosensors and Bioelectronics,* vol. 24, no. 7, pp. 2225-2231, 2009.

[62] E.-J. Yoon, J.-T. Park, and C.-G. Yu, "Thermal energy harvesting circuit with maximum power point tracking control for self-powered sensor node applications," *Frontiers of Information Technology & Electronic Engineering,* vol. 19, no. 2, pp. 285-296, 2018.

[63] G. Zhang, M. Li, H. Li, Q. Wang, and S. Jiang, "Harvesting energy from human activity: ferroelectric energy harvesters for portable, implantable, and biomedical electronics," *Energy Technology,* vol. 6, no. 5, pp. 791-812, 2018.

[64] D. A. Borton, M. Yin, J. Aceros, and A. Nurmikko, "An implantable wireless neural interface for recording cortical circuit dynamics in moving primates," *Journal of neural engineering,* vol. 10, no. 2, p. 026010, 2013.

[65] K. Stingl *et al.*, "Artificial vision with wirelessly powered subretinal electronic implant alpha-IMS," *Proceedings of the Royal Society B: Biological Sciences,* vol. 280, no. 1757, p. 20130077, 2013.

[66] S. Ozeri, D. Shmilovitz, S. Singer, and C.-C. Wang, "Ultrasonic transcutaneous energy transfer using a continuous wave 650 kHz Gaussian shaded transmitter," *Ultrasonics,* vol. 50, no. 7, pp. 666-674, 2010.
[67] T.-i. Kim *et al.*, "Injectable, cellular-scale optoelectronics with applications for wireless optogenetics," *Science,* vol. 340, no. 6129, pp. 211-216, 2013.
[68] C. T. Wentz, J. G. Bernstein, P. Monahan, A. Guerra, A. Rodriguez, and E. S. Boyden, "A wirelessly powered and controlled device for optical neural control of freely-behaving animals," *Journal of neural engineering,* vol. 8, no. 4, p. 046021, 2011.
[69] L. Lu *et al.*, "Biodegradable monocrystalline silicon photovoltaic microcells as power supplies for transient biomedical implants," *Advanced Energy Materials,* vol. 8, no. 16, p. 1703035, 2018.
[70] Y.-J. Hung, C.-H. Lu, J.-F. Liao, and M.-C. Hsieh, "Backside-Illuminated CMOS Photodiodes With Embedded Polysilicon Grating Reflectors," *IEEE Photonics Technology Letters,* vol. 31, no. 2, pp. 193-196, 2018.
[71] Y. Song, K. Choi, D.-H. Jun, and J. Oh, "Nanostructured GaAs solar cells via metal-assisted chemical etching of emitter layers," *Optics Express,* vol. 25, no. 20, pp. 23862-23872, 2017.
[72] E. Moon, D. Blaauw, and J. D. Phillips, "Subcutaneous photovoltaic infrared energy harvesting for bio-implantable devices," *IEEE transactions on electron devices,* vol. 64, no. 5, pp. 2432-2437, 2017.
[73] E. Moon, D. Blaauw, and J. D. Phillips, "Infrared energy harvesting in millimeter-scale gaas photovoltaics," *IEEE transactions on electron devices,* vol. 64, no. 11, pp. 4554-4560, 2017.
[74] S. Gong and W. Cheng, "Toward soft skin-like wearable and implantable energy devices," *Advanced Energy Materials,* vol. 7, no. 23, p. 1700648, 2017.
[75] Z. Chen *et al.*, "Thin single crystal perovskite solar cells to harvest below-bandgap light absorption," *Nature communications,* vol. 8, no. 1, pp. 1-7, 2017.
[76] Y.-J. Hung, T.-Y. Chuang, C.-L. Chun, M.-S. Cai, H.-W. Su, and S.-L. Lee, "CMOS-enabled interdigitated back-contact solar cells for biomedical applications," *IEEE Transactions on Electron Devices,* vol. 61, no. 12, pp. 4019-4024, 2014.
[77] S. Ayazian, V. A. Akhavan, E. Soenen, and A. Hassibi, "A photovoltaic-driven and energy-autonomous CMOS implantable sensor," *IEEE Transactions on biomedical circuits and systems,* vol. 6, no. 4, pp. 336-343, 2012.
[78] I. Vaisband and E. G. Friedman, "Stability of distributed power delivery systems with multiple parallel on-chip LDO regulators," *IEEE Transactions on Power Electronics,* vol. 31, no. 8, pp. 5625-5634, 2015.
[79] G. Saini, L. Somappa, and M. S. Baghini, "A 500 nW to 1 mW Input Power Inductive Boost Converter with MPPT for RF Energy Harvesting System," *IEEE Journal of Emerging and Selected Topics in Power Electronics,* 2020.
[80] K. Zhang, T. Ye, Z. Yan, B. Song, and A. P. Hu, "Obtaining Maximum Efficiency of Inductive Power Transfer System by Impedance Matching Based on Boost Converter," *IEEE Transactions on Transportation Electrification,* 2020.
[81] M. Carbajal-Retana *et al.*, "Interleaved Buck Converter for Inductive Wireless Power Transfer in DC–DC Converters," *Electronics,* vol. 9, no. 6, p. 949, 2020.
[82] P. H. McLaughlin, Z. Xia, and J. T. Stauth, "11.2 A Fully Integrated Resonant Switched-Capacitor Converter with 85.5% Efficiency at 0.47 W Using On-Chip Dual-Phase Merged-LC Resonator," in *2020 IEEE International Solid-State Circuits Conference-(ISSCC)*, pp. 192-194, 2020.
[83] Y. He, Z. Zhang, R. Wu, W. Guo, H. Zhang, and F. Bai, "On-chip coupled inductors with a novel spliced anisotropic and isotropic magnetic core for inductance and coupling enhancement," *Solid-State Electronics,* vol. 164, p. 107699, 2020.
[84] F. Chen, Y. Lu, and P. K. Mok, "A Fast-Transient 500-mA Digitally Assisted Analog LDO With 30-\mu V/mA Load Regulation and 0.0073-ps FoM in 65-nm CMOS," *IEEE Journal of Solid-State Circuits,* 2020.
[85] P. Hazucha, T. Karnik, B. A. Bloechel, C. Parsons, D. Finan, and S. Borkar, "Area-efficient linear regulator with ultra-fast load regulation," *IEEE Journal of solid-state circuits,* vol. 40, no. 4, pp. 933-940, 2005.
[86] G.-Y. Wei and M. Horowitz, "A fully digital, energy-efficient, adaptive power-supply regulator," *IEEE Journal of solid-state Circuits,* vol. 34, no. 4, pp. 520-528, 1999.

[87] B. N. Alajmi, M. I. Marei, and I. Abdelsalam, "A Multiport DC–DC Converter Based on Two-Quadrant Inverter Topology for PV Systems," *IEEE Transactions on Power Electronics,* vol. 36, no. 1, pp. 522-532, 2020.
[88] P. Hazucha *et al.*, "A 233-MHz 80%-87% efficient four-phase DC-DC converter utilizing air-core inductors on package," *IEEE Journal of Solid-State Circuits,* vol. 40, no. 4, pp. 838-845, 2005.
[89] W. Liu *et al.*, "Switched-capacitor-convertors based on fractal design for output power management of triboelectric nanogenerator," *Nature communications,* vol. 11, no. 1, pp. 1-10, 2020.
[90] H. Greinacher, "The ionometer and its application to the measurement of radium and röntgen rays," *Physikalische Zeitschrift,* vol. 15, pp. 410-415, 1914.
[91] E. Marx, "Verfahren zur Schlagprufung von Isolatoren und anderen elektrischen Vorrichtungen Method for break-down tests of isolators and other electric devices," *German Patent No. 455933,* 1923.
[92] S. Levy, M. Nikolich, I. Alexeff, M. Rader, M. Buttram, and W. Sarjeant, "Commercial applications for modulators and pulse power technology," in *Twentieth Conference Record on Power Modulator Symposium*, p. 8, 1992.
[93] T. Tanzawa, "Innovation of switched-capacitor voltage multiplier: Part 1: A brief history," *IEEE Solid-State Circuits Magazine,* vol. 8, no. 1, pp. 51-59, 2016.
[94] J. D. Cockcroft and E. T. Walton, "Experiments with high velocity positive ions.—(I) Further developments in the method of obtaining high velocity positive ions," *Proceedings of the royal society of London. Series A, containing papers of a mathematical and physical character,* vol. 136, no. 830, pp. 619-630, 1932.
[95] M. D. Bellar, E. Watanabe, and A. Mesquita, "Analysis of the dynamic and steady-state performance of Cockcroft-Walton cascade rectifiers," *IEEE transactions on power electronics,* vol. 7, no. 3, pp. 526-534, 1992.
[96] J. S. Kilby, "Miniaturized electronic circuits," ed: Google Patents, 1964.
[97] J. Brugler, "Theoretical performance of voltage multiplier circuits," *IEEE Journal of Solid-State Circuits,* vol. 6, no. 3, pp. 132-135, 1971.
[98] A. Falkner, "Generalised cockcroft-walton voltage multipliers," *Electronics Letters,* vol. 9, no. 25, pp. 585-586, 1973.
[99] J. F. Dickson, "On-chip high-voltage generation in MNOS integrated circuits using an improved voltage multiplier technique," *IEEE Journal of solid-state circuits,* vol. 11, no. 3, pp. 374-378, 1976.
[100] S. D'Arrigo *et al.*, "A 5 V-only 256 kbit CMOS flash EEPROM," in *IEEE International Solid-State Circuits Conference, 1989 ISSCC. Digest of Technical Papers*, pp. 132-133.
[101] A. Umezawa *et al.*, "A 5-V-only operation 0.6-mu m flash EEPROM with row decoder scheme in triple-well structure," *IEEE Journal of Solid-State Circuits,* vol. 27, no. 11, pp. 1540-1546, 1992.
[102] S. Atsumi *et al.*, "A 16-Mb flash EEPROM with a new self-data-refresh scheme for a sector erase operation," *IEICE Transactions on Electronics,* vol. 77, no. 5, pp. 791-799, 1994.
[103] J.-T. Wu and K.-L. Chang, "MOS charge pumps for low-voltage operation," *IEEE Journal of solid-state circuits,* vol. 33, no. 4, pp. 592-597, 1998.
[104] J. F. Dickson, "Voltage multiplier employing clock gated transistor chain," ed: Google Patents, 1980.
[105] H. Fuketa and T. Matsukawa, "Fully integrated, 100-mV minimum input voltage converter with gate-boosted charge pump kick-started by LC oscillator for energy harvesting," *IEEE Transactions on Circuits and Systems II: Express Briefs,* vol. 64, no. 4, pp. 392-396, 2016.
[106] S. Mondal and R. Paily, "An efficient on-chip switched-capacitor-based power converter for a microscale energy transducer," *IEEE Transactions on Circuits and Systems II: Express Briefs,* vol. 63, no. 3, pp. 254-258, 2015.
[107] M. A. Ansari, W. Ahmad, and S. R. Signell, "Single clock charge pump designed in 0.35 μm technology," in *Proceedings of the 18th International Conference Mixed Design of Integrated Circuits and Systems-MIXDES,* pp. 552-556, 2011.
[108] S. Mondal and R. P. Paily, "A strategy to enhance the output voltage of a charge pump circuit suitable for energy harvesting," in *2013 Annual International Conference on Emerging Research Areas and International Conference on Microelectronics, Communications and Renewable Energy*, pp. 1-5, 2013.
[109] A. Ballo, A. D. Grasso, and G. Palumbo, "A review of charge pump topologies for the power management of IoT nodes," *Electronics,* vol. 8, no. 5, p. 480, 2019.

[110] F. Ueno, T. Inoue, I. Oota, and I. Harada, "Emergency power supply for small computer systems," in *1991., IEEE International Sympoisum on Circuits and Systems*, pp. 1065-1068, 1991.
[111] R.-A. Cernea, "Charge pump circuit with exponetral multiplication," ed: Google Patents, 1995.
[112] Y. Nakagome *et al.*, "An experimental 1.5-V 64-Mb dram," *IEEE Journal of Solid-State Circuits,* vol. 26, no. 4, pp. 465-472, 1991.
[113] R. Gariboldi and F. Pulvirenti, "A monolithic quad line driver for industrial applications," *IEEE journal of solid-state circuits,* vol. 29, no. 8, pp. 957-962, 1994.
[114] R. Gariboldi and F. Pulvirenti, "A 70 m/spl Omega/intelligent high side switch with full diagnostics," *IEEE Journal of Solid-State Circuits,* vol. 31, no. 7, pp. 915-923, 1996.
[115] M.-D. Ker, S.-L. Chen, and C.-S. Tsai, "Design of charge pump circuit with consideration of gate-oxide reliability in low-voltage CMOS processes," *IEEE Journal of solid-state circuits,* vol. 41, no. 5, pp. 1100-1107, 2006.
[116] Z. Luo, M.-D. Ker, W.-H. Cheng, and T.-Y. Yen, "Regulated charge pump with new clocking scheme for smoothing the charging current in low voltage CMOS process," *IEEE Transactions on Circuits and Systems I: Regular Papers,* vol. 64, no. 3, pp. 528-536, 2016.
[117] P. Favrat, P. Deval, and M. J. Declercq, "A high-efficiency CMOS voltage doubler," *IEEE Journal of solid-state circuits,* vol. 33, no. 3, pp. 410-416, 1998.
[118] Y. Tsuji, T. Hirose, T. Ozaki, H. Asano, N. Kuroki, and M. Numa, "A 0.1–0.6 V input range voltage boost converter with low-leakage driver for low-voltage energy harvesting," in *2017 24th IEEE International Conference on Electronics, Circuits and Systems (ICECS)*, pp. 502-505, 2017.
[119] H. Peng, N. Tang, Y. Yang, and D. Heo, "CMOS startup charge pump with body bias and backward control for energy harvesting step-up converters," *IEEE Transactions on Circuits and Systems I: Regular Papers,* vol. 61, no. 6, pp. 1618-1628, 2014.
[120] L. F. New, Z. A. bin Abdul Aziz, and M. F. Leong, "A low ripple CMOS charge pump for low-voltage application," in *2012 4th International Conference on Intelligent and Advanced Systems (ICIAS2012)*, vol. 2, pp. 784-789, 2012.
[121] Y. Wang, N. Yan, H. Min, and C.-J. R. Shi, "A high-efficiency split–merge charge pump for solar energy harvesting," *IEEE Transactions on Circuits and Systems II: Express Briefs,* vol. 64, no. 5, pp. 545-549, 2016.
[122] W. C. Athas, L. J. Svensson, J. G. Koller, N. Tzartzanis, and E. Y.-C. Chou, "Low-power digital systems based on adiabatic-switching principles," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems,* vol. 2, no. 4, pp. 398-407, 1994.
[123] M. Alioto and G. Palumbo, "Performance evaluation of adiabatic gates," *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications,* vol. 47, no. 9, pp. 1297-1308, 2000.
[124] C. Lauterbach, W. Weber, and D. Romer, "Charge sharing concept and new clocking scheme for power efficiency and electromagnetic emission improvement of boosted charge pumps," *IEEE Journal of solid-state circuits,* vol. 35, no. 5, pp. 719-723, 2000.
[125] K.-M. Keung, V. Manne, and A. Tyagi, "A novel charge recycling design scheme based on adiabatic charge pump," *IEEE transactions on very large scale integration (VLSI) systems,* vol. 15, no. 7, pp. 733-745, 2007.
[126] C. Ulaganathan, B. J. Blalock, J. Holleman, and C. L. Britton, "An ultra-low voltage self-startup charge pump for energy harvesting applications," in *IEEE 55th International Midwest Symposium on Circuits and Systems (MWSCAS)*, pp. 206-209, 2012.
[127] Y. Lei, R. May, and R. Pilawa-Podgurski, "Split-phase control: Achieving complete soft-charging operation of a dickson switched-capacitor converter," *IEEE Transactions on Power Electronics,* vol. 31, no. 1, pp. 770-782, 2015.
[128] H. Gi, J. Park, Y. Yoon, S. Jung, S. J. Kim, and Y. Lee, "A Soft-Charging-Based SC DC–DC Boost Converter With Conversion-Ratio-Insensitive High Efficiency for Energy Harvesting in Miniature Sensor Systems," *IEEE Transactions on Circuits and Systems I: Regular Papers,* vol. 67, no. 10, pp. 3601-3612, 2020.
[129] I. Chowdhury and D. Ma, "Design of reconfigurable and robust integrated SC power converter for self-powered energy-efficient devices," *IEEE Transactions on Industrial Electronics,* vol. 56, no. 10, pp. 4018-4028, 2009.
[130] I. Chowdhury and D. Ma, "An integrated reconfigurable switched-capacitor dc-dc converter with a dual-loop adaptive gain-pulse control," in *2008 IEEE International Symposium on Circuits and Systems*, pp. 2610-2613, 2008.

[131] W. C. Huang, J. C. Cheng, P. C. Liou, and C. W. Liou, "A charge pump circuit using multi-staged voltage doubler clock scheme," in *2007 Internatonal Conference on Microelectronics*, pp. 317-320, 2007.
[132] I. Vaisband, M. Saadat, and B. Murmann, "A closed-loop reconfigurable switched-capacitor DC-DC converter for sub-mW energy harvesting applications," *IEEE Transactions on Circuits and Systems I: Regular Papers,* vol. 62, no. 2, pp. 385-394, 2014.
[133] X. Zhang and H. Lee, "An Efficiency-Enhanced Auto-Reconfigurable 2x/3x SC Charge Pump for Transcutaneous Power Transmission," *IEEE journal of solid-state circuits,* vol. 45, no. 9, pp. 1906-1922, 2010.
[134] Y. Beck and S. Singer, "Capacitive transposed series-parallel topology with fine tuning capabilities," *IEEE Transactions on Circuits and Systems I: Regular Papers,* vol. 58, no. 1, pp. 51-61, 2010.
[135] P.-H. Chen *et al.*, "A 120-mV input, fully integrated dual-mode charge pump in 65-nm CMOS for thermoelectric energy harvester," in *17th Asia and South Pacific Design Automation Conference*, pp. 469-470, 2012.
[136] I. Chowdhury and D. Ma, "On-chip reconfigurable SC power supply with adaptive gain/pulse control for self-powered energy-efficient devices," in *IEEE International Symposium on Industrial Electronics*, pp. 1715-1720, 2008.
[137] A. K. Gupta, A. Joshi, V. Gajare, H. Ghanshyam, and A. Dutta, "Power efficient reconfigurable charge pump for micro scale energy harvesting," in *IEEE Asia Pacific Conference on Postgraduate Research in Microelectronics and Electronics (PrimeAsia)*, pp. 73-76, 2013.
[138] T. Tanzawa, T. Tanaka, K. Takeuchi, and H. Nakamura, "Circuit techniques for a 1.8-V-only NAND flash memory," *IEEE Journal of Solid-State Circuits,* vol. 37, no. 1, pp. 84-89, 2002.
[139] T. Tanzawa, *On-chip High-Voltage Generator Design*. Springer, 2013.
[140] T. Tanzawa, *On-Chip High-Voltage Generator Design: Design Methodology for Charge Pumps*. Springer, 2015.
[141] I. Chowdhury, "Efficient Voltage Regulation Using Switched Capacitor DC/DC Converter from Battery and Energy Harvesting Power Sources," Ph.D Thesis, 2010.
[142] G. Palumbo, D. Pappalardo, and M. Gaibotti, "Charge-pump circuits: power-consumption optimization," *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications,* vol. 49, no. 11, pp. 1535-1542, 2002.
[143] H. Chung, "Design and analysis of quasi-switched-capacitor step-up dc/dc converters," in *IEEE International Symposium on Circuits and Systems (ISCAS)*, vol. 6, pp. 438-441, 1998.
[144] H. Chung and Y. Mok, "Development of a switched-capacitor DC/DC boost converter with continuous input current waveform," *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications,* vol. 46, no. 6, pp. 756-759, 1999.
[145] L. Yang, L. J. Martin, D. Staiculescu, C. Wong, and M. M. Tentzeris, "Conformal magnetic composite RFID for wearable RF and bio-monitoring applications," *IEEE transactions on microwave theory and techniques,* vol. 56, no. 12, pp. 3223-3230, 2008.
[146] Y. Hu and M. M. Jovanovic, "LED driver with self-adaptive drive voltage," *IEEE Transactions on Power Electronics,* vol. 23, no. 6, pp. 3116-3125, 2008.
[147] L. Su and D. Ma, "Design and optimization of integrated low-voltage low-power monolithic CMOS charge pumps," in *International Symposium on Power Electronics, Electrical Drives, Automation and Motion*, pp. 43-48, 2008.
[148] M. Evzelman and S. Ben-Yaakov, "Average-current-based conduction losses model of switched capacitor converters," *IEEE Transactions on Power Electronics,* vol. 28, no. 7, pp. 3341-3352, 2012.
[149] T. Das, S. Prasad, S. Dam, and P. Mandal, "A pseudo cross-coupled switch-capacitor based DC-DC boost converter for high efficiency and high power density," *IEEE Transactions on Power Electronics,* vol. 29, no. 11, pp. 5961-5974, 2014.
[150] S. Clerc, T. Di Gilio and A. Cathelin, "The Fourth Terminal: Benefits of Body-Biasing Techniques for FDSIO Circuits and Systems" in *Springer*, 2020.
[151] P. E. Allen and D. R. Holberg, *CMOS analog circuit design*. Elsevier, 2011.
[152] D. Ma and R. Bondade, "Power loss in switched-capacitor power converters: Causes and analysis," in *Reconfigurable Switched-Capacitor Power Converters*: Springer, pp. 59-69, 2013.
[153] X. Wu *et al.*, "A 20-pW discontinuous switched-capacitor energy harvester for smart sensor applications," *IEEE Journal of Solid-State Circuits,* vol. 52, no. 4, pp. 972-984, 2017.

[154] B. Rumberg, D. W. Graham, and M. M. Navidi, "A regulated charge pump for tunneling floating-gate transistors," *IEEE Transactions on Circuits and Systems I: Regular Papers,* vol. 64, no. 3, pp. 516-527, 2017.
[155] X. Liu, L. Huang, K. Ravichandran, and E. Sánchez-Sinencio, "A highly efficient reconfigurable charge pump energy harvester with wide harvesting range and two-dimensional MPPT for Internet of Things," *IEEE Journal of Solid-State Circuits,* vol. 51, no. 5, pp. 1302-1312, 2016.
[156] K. O. Htet, R. Ghannam, Q. H. Abbasi, and H. Heidari, "Power management using photovoltaic cells for implantable devices," *IEEE Access,* vol. 6, pp. 42156-42164, 2018.
[157] Y. Jiang, M.-K. Law, Z. Chen, P.-I. Mak, and R. P. Martins, "Algebraic Series-Parallel-Based Switched-Capacitor DC–DC Boost Converter With Wide Input Voltage Range and Enhanced Power Density," *IEEE Journal of Solid-State Circuits,* vol. 54, no. 11, pp. 3118-3134, 2019.
[158] Y. Lu, J. Jiang, and W.-H. Ki, "A multiphase switched-capacitor DC–DC converter ring with fast transient response and small ripple," *IEEE Journal of Solid-State Circuits,* vol. 52, no. 2, pp. 579-591, 2016.
[159] Z. Hua and H. Lee, "A reconfigurable dual-output switched-capacitor DC-DC regulator with sub-harmonic adaptive-on-time control for low-power applications," *IEEE Journal of Solid-State Circuits,* vol. 50, no. 3, pp. 724-736, 2015.
[160] S. Mondal and R. P. Paily, "An efficient on chip power management architecture for solar energy harvesting systems," in *29th International Conference on VLSI Design and 2016 15th International Conference on Embedded Systems (VLSID)*, pp. 224-229, 2016.
[161] S. Mondal and R. Paily, "Efficient solar power management system for self-powered IoT node," *IEEE Transactions on Circuits and Systems I: Regular Papers,* vol. 64, no. 9, pp. 2359-2369, 2017.
[162] S. Mondal and R. Paily, "On-chip photovoltaic power harvesting system with low-overhead adaptive MPPT for IoT nodes," *IEEE Internet of Things Journal,* vol. 4, no. 5, pp. 1624-1633, 2017.
[163] J. Zhao, K. O. Htet, R. Ghannam, M. Imran, and H. Heidari, "Modelling of Implantable Photovoltaic Cells Based on Human Skin Types," in *15th Conference on Ph. D Research in Microelectronics and Electronics (PRIME)*, pp. 253-256, 2019.
[164] S. Yoon, S. Carreon-Bautista, and E. Sánchez-Sinencio, "An area efficient thermal energy harvester with reconfigurable capacitor charge pump for IoT applications," *IEEE Transactions on Circuits and Systems II: Express Briefs,* vol. 65, no. 12, pp. 1974-1978, 2018.
[165] B. Mohammadi and J. Rodrigues, "Ultra low energy and area efficient charge pump with automatic clock controller in 65 nm CMOS," in *2015 IEEE Asian Solid-State Circuits Conference (A-SSCC)*, pp. 1-4, 2015.
[166] J. S. D. A. Manual, "Newport Beach," *CA: Jazz Semiconductor Products Inc,* 2012.
[167] X. Zhang *et al.*, "A fully integrated battery-powered system-on-chip in 40-nm CMOS for closed-loop control of insect-scale pico-aerial vehicle," *IEEE Journal of Solid-State Circuits,* vol. 52, no. 9, pp. 2374-2387, 2017.
[168] K. O. Htet, H. Fan, and H. Heidari, "Switched capacitor DC-DC converter for miniaturised wearable systems," in *2018 IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 1-5, 2018. doi: 10.1109/ISCAS.2018.8351795.
[169] M. H. Ghaed *et al.*, "Circuits for a cubic-millimeter energy-autonomous wireless intraocular pressure monitor," *IEEE Transactions on Circuits and Systems I: Regular Papers,* vol. 60, no. 12, pp. 3152-3162, 2013.
[170] G. Chen *et al.*, "A cubic-millimeter energy-autonomous wireless intraocular pressure monitor," in *IEEE International Solid-State Circuits Conference*, pp. 310-312, 2011.
[171] C. Corporation. Cymbet Corporation Rechargeable Thin Film Battery 12μAh 3.8 V [Online] Available: https://www.cymbet.com/wp-content/uploads/2019/02/DS-72-04.pdf
[172] A. S. f. Testing, M. C. G. o. Weathering, and Durability, *Standard tables for reference solar spectral irradiances: direct normal and hemispherical on 37° tilted surface*. ASTM international, 2003.
[173] A. Devices. Ultralow Quiescent Current 150 mA, CMOS Linear Regulators [Online] Available: https://www.analog.com/media/en/technical-documentation/data-sheets/ADP160_161_162_163.pdf
[174] S.-K. Kim *et al.*, "Wireless smart contact lens for diabetic diagnosis and therapy," *Science Advances,* vol. 6, no. 17, p. eaba3252, 2020.
[175] T. Instruments. MSP430FR596x, MSP430FR594x Mixed-Signal Microcontrollers [Online] Available: https://www.ti.com/lit/ds/symlink/msp430fr5969.pdf

[176] ARM. ARM Cortex-M3 [Online] Available: https://developer.arm.com/ip-products/processors/cortex-m/cortex-m3
[177] A. Devices. Micropower, 3-Axis, ±2 g/±4 g/±8 g Digital Output MEMS Accelerometer-ADXL362 [Online] Available: https://static6.arrow.com/aropdfconversion/3a0c5e27853ff0557198e6888ac47cc3ef9b8f5c/265330741049582adxl362.pdf
[178] ST. Dynamic NFC/RFID tag IC with 16-Kbit EEPROM, energy harvesting, I²C bus and ISO 15693 RF interface [Online] Available: http://www.farnell.com/datasheets/2308241.pdf
[179] TE_connectivity. TSYS01-FAMILY Digital Temperature Sensors [Online] Available: https://www.te.com/commerce/DocumentDelivery/DDEController?Action=showdoc&DocId=Data+Sheet%7FTSYS01%7FA2%7Fpdf%7FEnglish%7FENG_DS_TSYS01_A2.pdf%7FG-NICO-018
[180] TE_connectivity. MEAS DETECTOR ASSEMBLY EPM-4001 SpO2 Optical Sensor Component [Online] Available: https://www.te.com/commerce/DocumentDelivery/DDEController?Action=srchrtrv&DocNm=EPM-4001&DocType=DS&DocLang=English
[181] J. Kim, J. Kim, and H. Ko, "Low-power photoplethysmogram acquisition integrated circuit with robust light interference compensation," *Sensors,* vol. 16, no. 1, p. 46, 2016.
[182] Infineon. DPS310-Digital XENSIVTM Barometric Pressure Sensor for Portable Devices [Online] Available: https://www.infineon.com/dgdl/Infineon-DPS310-DataSheet-v01_02-EN.pdf?fileId=5546d462576f34750157750826c42242
[183] AnalogDevices. 50 μA, 2 mm × 1.7 mm WLCSP, Low Noise, Heart Rate Monitor for Wearable Products [Online] Available: https://www.analog.com/en/products/AD8233.html#product-overview
[184] AnalogDevices. ADPD4100- Multimodal Sensor Front End [Online] Available: https://www.analog.com/media/en/technical-documentation/data-sheets/adpd4100-4101.pdf
[185] D. Porcarelli, I. Donati, J. Nehani, D. Brunelli, M. Magno, and L. Benini, "Design and implementation of a multi sensors self sustainable wearable device," in *6th European Embedded Design in Education and Research Conference (EDERC)*, pp. 16-20, 2014.
[186] M. Magno, G. A. Salvatore, S. Mutter, W. Farrukh, G. Troester, and L. Benini, "Autonomous smartwatch with flexible sensors for accurate and continuous mapping of skin temperature," in *IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 337-340, 2016.
[187] N. Khosropour, F. Krummenacher, and M. Kayal, "Fully integrated ultra-low power management system for micro-power solar energy harvesting applications," *Electronics Letters,* vol. 48, no. 6, pp. 338-339, 2012.
[188] A. R. Lingley, B. P. Otis, T. T. Shen, and B. A. Parviz, "A contact lens with integrated micro solar cells," *Microsystem technologies,* vol. 18, no. 4, pp. 453-458, 2012.
[189] W. Van Sark, "Simulating performance of solar cells with spectral downshifting layers," *Thin solid films,* vol. 516, no. 20, pp. 6808-6812, 2008.
[190] O. Nizhnik, U. Maksudi, S. Okochi, K. Higuchi, and K. Maenaka, "The availability and statistical properties of ambient light for energy-harvesting for wearable sensor nodes," *management,* vol. 6, no. 6.7, p. 500, 2012.
[191] Z. L. Wang and W. Wu, "Nanotechnology-enabled energy harvesting for self-powered micro-/nanosystems," *Angewandte Chemie International Edition,* vol. 51, no. 47, pp. 11700-11721, 2012.
[192] G. Makrides, B. Zinsser, M. Norton, and G. E. Georghiou, "Performance of photovoltaics under actual operating conditions," *Third generation photovoltaics,* pp. 201-232, 2012.
[193] J. Yoon *et al.*, "Ultrathin silicon solar microcells for semitransparent, mechanically flexible and microconcentrator module designs," in *Materials for Sustainable Energy: A Collection of Peer-Reviewed Research and Review Articles from Nature Publishing Group*: World Scientific, 2011, pp. 38-46.
[194] Y. Arima and M. Ehara, "On-chip solar battery structure for CMOS LSI," *IEICE electronics express,* vol. 3, no. 13, pp. 287-291, 2006.
[195] M. M. Desa *et al.*, "Silicon back contact solar cell configuration: A pathway towards higher efficiency," *Renewable and sustainable energy reviews,* vol. 60, pp. 1516-1532, 2016.
[196] G. Simone *et al.*, "Near-infrared tandem organic photodiodes for future application in artificial retinal implants," *Advanced Materials,* vol. 30, no. 51, p. 1804678, 2018.

[197] N. Butzen and M. Steyaert, "12.2 A 94.6%-efficiency fully integrated switched-capacitor DC-DC converter in baseline 40nm CMOS using scalable parasitic charge redistribution," in *IEEE international solid-state circuits conference (ISSCC)*, pp. 220-221, 2016.

[198] X. Yu, K. Moez, I.-C. Wey, M. Sawan, and J. Chen, "A fully integrated multistage cross-coupled voltage multiplier with no reversion power loss in a standard CMOS process," *IEEE Transactions on Circuits and Systems II: Express Briefs,* vol. 64, no. 7, pp. 737-741, 2016.

[199] T. Kimura and H. Ochi, "A− 0.5 V-input voltage booster circuit for on-chip solar cells in 0.18 μm CMOS technology," in *15th International Symposium on Communications and Information Technologies (ISCIT)*, pp. 193-196, 2015

[200] J. Jiang, W.-H. Ki, and Y. Lu, "Digital 2-/3-phase switched-capacitor converter with ripple reduction and efficiency improvement," *IEEE Journal of Solid-State Circuits,* vol. 52, no. 7, pp. 1836-1848, 2017.

[201] H. Lee, Z. Hua, and X. Zhang, "A Reconfigurable $2\times/2.5\times/3\times/4\times $ SC DC–DC Regulator With Fixed On-Time Control for Transcutaneous Power Transmission," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems,* vol. 23, no. 4, pp. 712-722, 2014.

[202] D. Kilani, B. Mohammad, M. Alhawari, H. Saleh, and M. Ismail, "A Dual-Output Switched Capacitor DC–DC Buck Converter Using Adaptive Time Multiplexing Technique in 65-nm CMOS," *IEEE Transactions on Circuits and Systems I: Regular Papers,* vol. 65, no. 11, pp. 4007-4016, 2018.

[203] D. Kilani, B. Mohammad, M. Alhawari, H. Saleh, and M. Ismail, "Power Management for Wearable Electronic Devices", in *Springer*, 2020.

[204] N. De Clercq, T. Van Breussegem, W. Dehaene, and M. Steyaert, "Dual-output capacitive DC-DC converter with power distribution regulator in 90 nm CMOS," in *Proceedings of the ESSCIRC (ESSCIRC)*, pp. 169-172, 2012.

[205] Y. Zhao, Y. Yang, K. Mazumdar, X. Guo, and M. R. Stan, "A multi-output on-chip switched-capacitor DC-DC converter for near-and sub-threshold power modes," in *IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 1632-1635, 2014.

[206] Y.-C. Lin, Y.-K. Luo, K.-H. Chen, and W.-C. Hsu, "Liquid crystal display (LCD) supplied by highly integrated dual-side dual-output switched-capacitor DC-DC converter with only two flying capacitors," *IEEE Transactions on Circuits and Systems I: Regular Papers,* vol. 59, no. 2, pp. 439-446, 2011.

[207] A. M. Mohey, S. A. Ibrahim, I. M. Hafez, and H. Kim, "Design Optimization for Low-Power Reconfigurable Switched-Capacitor DC-DC Voltage Converter," *IEEE Transactions on Circuits and Systems I: Regular Papers,* vol. 66, no. 10, pp. 4079-4092, 2019.

[208] D. Kilani, M. Alhawari, B. Mohammad, H. Saleh, and M. Ismail, "An efficient switched-capacitor DC-DC buck converter for self-powered wearable electronics," *IEEE Transactions on Circuits and Systems I: Regular Papers,* vol. 63, no. 10, pp. 1557-1566, 2016.

[209] A. Ballo, A. D. Grasso, G. Giustolisi, and G. Palumbo, "Optimized charge pump with clock booster for reduced rise time or silicon area," *IEEE Transactions on Circuits and Systems II: Express Briefs,* vol. 66, no. 12, pp. 1977-1981, 2019.

[210] A. Esmailiyan, J. Du, T. Siriburanon, F. Schembari, and R. B. Staszewski, "Dickson-Charge-Pump-Based Voltage-to-Time Conversion for Time-Based ADCs in 28nm CMOS," *IEEE Open Journal of Circuits and Systems,* 2020.

[211] A. Saeed, S. Ibrahim, and H. F. Ragai, "A sizing methodology for rise-time minimization of Dickson charge pumps with capacitive loads," *IEEE Transactions on Circuits and Systems II: Express Briefs,* vol. 64, no. 10, pp. 1202-1206, 2017.

[212] A. Esmailiyan, F. Schembari, and R. B. Staszewski, "A 0.36-V 5-MS/s Time-Mode Flash ADC With Dickson-Charge-Pump-Based Comparators in 28-nm CMOS," *IEEE Transactions on Circuits and Systems I: Regular Papers,* vol. 67, no. 6, pp. 1789-1802, 2020.

[213] H. Lin, H. Cao, Z. Chen, W. C. Chan, W. K. Lee, and M. Zhang, "Leakage current elimination for Dickson charge pump with a linear regulator," *Microelectronics journal,* vol. 64, pp. 29-34, 2017.

[214] M. El Alaoui *et al.*, "Analysis and design of dickson charge pump for EEPROM in 180nm CMOS technology," in *2018 International Conference on Intelligent Systems and Computer Vision (ISCV)*, 2018: IEEE, pp. 1-5.

[215] Y. Zhou, Z. Wang, and K. Wang, "High-Efficiency Charge Pumps with No Reversion Loss by Utilizing Gate Voltage Boosting Technique," in *IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 1-5, 2020.
[216] S. Yoshida, H. Miyaguchi, and T. Nakamura, "Prototyping of an All-pMOS-Based Cross-Coupled Voltage Multiplier in Single-Well CMOS Technology for Energy Harvesting Utilizing a Gastric Acid Battery," *Electronics,* vol. 8, no. 7, p. 804, 2019.
[217] S. Bose, T. Anand, and M. L. Johnston, "Integrated cold start of a boost converter at 57 mV using cross-coupled complementary charge pumps and ultra-low-voltage ring oscillator," *IEEE journal of solid-state circuits,* vol. 54, no. 10, pp. 2867-2878, 2019.
[218] A. Ballo, A. D. Grasso, and G. Palumbo, "A Subthreshold Cross-Coupled Hybrid Charge Pump for 50-mV Cold-Start," *IEEE Access,* vol. 8, pp. 188959-188969, 2020.
[219] Y. Wang, P. Luo, X. Zheng, and B. Zhang, "A 0.3 V–1.2 V ultra-low input voltage, reconfigurable switched-capacitor DC-DC converter for energy harvesting system," in *13th IEEE International Conference on Solid-State and Integrated Circuit Technology (ICSICT)*, pp. 1333-1335, 2016.
[220] T. Tong, S. K. Lee, X. Zhang, D. Brooks, and G.-Y. Wei, "A fully integrated reconfigurable switched-capacitor DC-DC converter with four stacked output channels for voltage stacking applications," *IEEE Journal of Solid-State Circuits,* vol. 51, no. 9, pp. 2142-2152, 2016.
[221] S.-Y. Chang, P. Cheng, G. Li, and Y. Yang, "Transparent polymer photovoltaics for solar energy harvesting and beyond," *Joule,* vol. 2, no. 6, pp. 1039-1054, 2018.
[222] R. Lotfi, M. Saberi, S. R. Hosseini, A. R. Ahmadi-Mehr, and R. B. Staszewski, "Energy-efficient wide-range voltage level shifters reaching 4.2 fJ/transition," *IEEE Solid-State Circuits Letters,* vol. 1, no. 2, pp. 34-37, 2018.
[223] M. A. Green and S. P. Bremner, "Energy conversion approaches and materials for high-efficiency photovoltaics," *Nature materials,* vol. 16, no. 1, pp. 23-34, 2017.
[224] J. Jiang, Y. Lu, W.-H. Ki, U. Seng-Pan, and R. P. Martins, "20.5 a dual-symmetrical-output switched-capacitor converter with dynamic power cells and minimized cross regulation for application processors in 28nm cmos," in *2017 IEEE International Solid-State Circuits Conference (ISSCC)*, pp. 344-345, 2017.
[225] W. Hong *et al.*, "A Dual-Output Step-Down Switched-Capacitor Voltage Regulator With a Flying Capacitor Crossing Technique for Enhanced Power Efficiency," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems,* vol. 27, no. 12, pp. 2861-2871, 2019.
[226] H. Gi, J. Park, Y. Yoon, S. Jung, S. J. Kim, and Y. Lee, "A Soft-Charging-Based SC DC-DC Boost Converter With Conversion-Ratio-Insensitive High Efficiency for Energy Harvesting in Miniature Sensor Systems," *IEEE Transactions on Circuits and Systems I: Regular Papers,* 2020.
[227] M. A. Green, "Third generation photovoltaics: advanced solar energy conversion," *PhT,* vol. 57, no. 12, pp. 71-72, 2004.
[228] S. R. Wenham, *Applied photovoltaics*. Routledge, 2011.
[229] R. Corkish, M. A. Green, M. E. Watt, and S. R. Wenham, *Applied photovoltaics*. Routledge, 2013.
[230] J.-Y. Kim, S.-J. Park, K.-W. Kwon, B.-S. Kong, J.-S. Choi, and Y.-H. Jun, "CMOS charge pump with no reversion loss and enhanced drivability," *IEEE transactions on very large scale integration (vlsi) systems,* vol. 22, no. 6, pp. 1441-1445, 2013.
[231] D. Li, F. Xia, J. Luo, and A. Yakovlev, "Modelling Reversion Loss and Shoot-through Current in Switched-Capacitor DC-DC Converters with Petri Nets," in *29th International Symposium on Power and Timing Modeling, Optimization and Simulation (PATMOS)*, pp. 69-74, 2019.
[232] A. Rashidi, N. Yazdani, and A. M. Sodagar, "Fully implantable, multi-channel microstimulator with tracking supply ribbon, multi-output charge pump and energy recovery," *IET Circuits, Devices & Systems*. pp 104-120, 2020. DOI: 10.1049/cds2.12007
[233] M. B. DANOUNE, A. DJAFOUR, A. GOUGUI, N. KHELFAOUI, and H. Boutli, "Characterization of photovoltaic panel using single diode and double diode models a comparative study with experimental validation," in *The 5th International Seminar on New and Renewable Energies, Ghardaïa–Algeria*, vol. 24, p. 25, 2018.
[234] J. Zhao *et al.*, "Simulation of Crystalline Silicon Photovoltaic Cells for Wearable Applications," *IEEE Access,* vol. 9, pp. 20868-20877, 2021.

[235] J. Park, H. Joshi, H. G. Lee, S. Kiaei, and U. Y. Ogras, "Flexible PV-cell modeling for energy harvesting in wearable IoT applications," *ACM Transactions on Embedded Computing Systems (TECS),* vol. 16, no. 5s, pp. 1-20, 2017.
[236] P. Löper *et al.*, "Analysis of the temperature dependence of the open-circuit voltage," *Energy Procedia,* vol. 27, pp. 135-142, 2012.
[237] K. O. Htet, J. Zhao, R. Ghannam, and H. Heidari, "Energy-efficient start-up power management for batteryless biomedical implant devices," in *2018 25th IEEE International Conference on Electronics, Circuits and Systems (ICECS)*, 2018: IEEE, pp. 597-600.
[238] H. Kim, J. Maeng, I. Park, J. Jeon, Y. Choi, and C. Kim, "A Dual-Mode Continuously Scalable-Conversion-Ratio SC Energy Harvesting Interface With SC-Based PFM MPPT and Flying Capacitor Sharing Scheme," *IEEE Journal of Solid-State Circuits,* 2021.
[239] W. Hong *et al.*, "Analysis and Design Method of Multiple-Output Switched-Capacitor Voltage Regulators With a Reduced Number of Power Electronic Components," *IEEE Transactions on Circuits and Systems I: Regular Papers,* vol. 67, no. 9, pp. 3234-3247, 2020.
[240] T. Ozaki, T. Hirose, H. Asano, N. Kuroki, and M. Numa, "Fully-integrated high-conversion-ratio dual-output voltage boost converter with MPPT for low-voltage energy harvesting," *IEEE Journal of Solid-State Circuits,* vol. 51, no. 10, pp. 2398-2407, 2016.
[241] R. Hesham and A. Soltan, "Study of Energy Harvesters for Wearable Devices," in *2020 2nd Novel Intelligent and Leading Emerging Sciences Conference (NILES)*, 2020: IEEE, pp. 259-263.
[242] J. Zhao, R. Ghannam, Q. H. Abbasi, M. Imran, and H. Heidari, "Simulation of Photovoltaic Cells for Implantable Sensory Applications," in *2018 IEEE SENSORS*, 2018: IEEE, pp. 1-4.
[243] A. K. Mal and R. Todani, "Non Overlapping Clock (NOC) generator for low frequency switched capacitor circuits," in *IEEE Technology Students' Symposium*, 2011: IEEE, pp. 226-231.
[244] T. Tong, X. Zhang, W. Kim, D. Brooks, and G.-Y. Wei, "A fully integrated battery-connected switched-capacitor 4: 1 voltage regulator with 70% peak efficiency using bottom-plate charge recycling," in *Proceedings of the IEEE 2013 Custom Integrated Circuits Conference*, 2013: IEEE, pp. 1-4.
[245] P. C. Lisboa, P. Pérez-Nicoli, F. Veirano, and F. Silveira, "General top/bottom-plate charge recycling technique for integrated switched capacitor DC-DC converters," *IEEE Transactions on Circuits and Systems I: Regular Papers,* vol. 63, no. 4, pp. 470-481, 2016.
[246] S. Rajapandian, Z. Xu, and K. L. Shepard, "Implicit DC-DC downconversion through charge-recycling," *IEEE journal of solid-state circuits,* vol. 40, no. 4, pp. 846-852, 2005.
[247] A. Mahmoud, M. Alhawari, B. Mohammad, H. Saleh, and M. Ismail, "A gain-controlled, low-leakage Dickson charge pump for energy-harvesting applications," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems,* vol. 27, no. 5, pp. 1114-1123, 2019.
[248] A. Ballo, A. Grasso, and G. Palumbo, "A High-Performance Charge Pump Topology for Very-Low-Voltage Applications," *IEEE Transactions on Circuits and Systems II: Express Briefs,* 2019.
[249] H. Yi, J. Yin, P.-I. Mak, and R. P. Martins, "A 0.032-mm 2 0.15-V three-stage charge-pump scheme using a differential bootstrapped ring-VCO for energy-harvesting applications," *IEEE Transactions on Circuits and Systems II: Express Briefs,* vol. 65, no. 2, pp. 146-150, 2017.
[250] A. Rashidi, N. Yazdani, and A. M. Sodagar, "Fully-Integrated, High-Efficiency, Multi-Output Charge Pump for High-Density Microstimulators," in *2018 IEEE Life Sciences Conference (LSC)*, 2018: IEEE, pp. 291-294.
[251] Y. Allasasmeh and S. Gregori, "Charge reusing in switched-capacitor voltage multipliers with reduced dynamic losses," in *2010 53rd IEEE International Midwest Symposium on Circuits and Systems*, 2010: IEEE, pp. 1169-1172.
[252] J.-Y. Kim, Y.-H. Jun, and B.-S. Kong, "CMOS charge pump with transfer blocking technique for no reversion loss and relaxed clock timing restriction," *IEEE Transactions on Circuits and Systems II: Express Briefs,* vol. 56, no. 1, pp. 11-15, 2009.