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Trench Etched Polarisation Pinned Multimode Vertical Cavity Surface Emitting Lasers

Danqi Lei

School of Engineering

University of Glasgow

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Abstract

In this thesis, stable polarisation VCSELs for SPIC systems are fabricated, characterised and analysed. The application requires VCSELs to satisfy the polarisation preference of a butt-coupling coupler in the structure and be embedded into the planar SPICs system to provide light for an EDWA. The design of the VCSELs considered device polarisation characteristics and device structure. Discussions about it is presented in the thesis.

VCSELs with 30µm wide and 9µm deep trenches etched next to it are fabricated by a repeatable fabrication process. Deep trenches with sharp edges were accomplished by dry etching techniques presented in this fabrication flow. Devices with diameter of 40µm, 30µm, 20µm and 10µm are achieved by this fabrication process that has a potential of large-scale production.

Device characteristics including output power, contact resistance, slope efficiency, wall-plug efficiency, emission spectra, polarisation direction, polarisation ratio and nearfield images are examined. The properties of different diameter devices are discussed. 40µm diameter device achieves the highest output power of 4.6mW with a power loss of 76% in the substrate. It was found that 40µm and 30µm diameter devices produced stable polarisation selection, however, 20µm and 10µm diameter devices show unstable polarisation characteristics.

An investigation of polarisation properties of the fabricated trench-etched VCSELs is carried out using polarised near-field and spectral measurements. The nearfield images took at subthreshold have been compared between orthogonal polarisation states for different diameter devices. A spontaneous emission intensity difference is found for 40µm and 30µm diameter devices. It is possible that gain distribution is different on orthogonal polarisation states. A further birefringence study is presented for 40µm trench-etched VCSELs at around threshold and above threshold. Around threshold, spatially overlapping lasing modes allow the birefringence and hence strain to be mapped, indicating higher strain in the centre of the device. For high currents, it is observed that the lasing of different polarisations occurs in different regions of the device, as opposed to being a temporal phenomenon.

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Preface

This work presented in this Thesis has culminated in the following conference proceedings and journal publication:

1. Danqi Lei, N Babazadeh, RA. Hogg, ‘‘Design, Fabrication and Characterisation of 980nm Linear Polarised Multimode VCSELs for Erbium Doped Waveguide Amplifier Integration’’, Semiconductor and Integrated Optoelectronics Conference(SIOE), Cardiff (UK),A19-46 April 2019
2. Danqi Lei, N Babazadeh, RA. Hogg, ‘‘Linearly Polarised Multimode VCSELs for Erbium Doped Waveguide Amplifier’’, UK Semiconductor 2019 with TMD-UK, Sheffield (UK),B-O-7 July 2019
3. Danqi Lei, Daehyun Kim, Olesya Ignatova, N Babazadeh, RA Hogg, ‘‘Polarisation Pinned Large diameter Substrate Emitting VCSELs”, Submitted to Electronic Letters
4. Danqi Lei, Daehyun Kim, Olesya Ignatova, N Babazadeh, RA Hogg,‘‘Spatial and spectral characteristics of polarisation pinned trench etched VCSEL’’, Submitted to AIP Advances

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Abbreviations

CTLM	Circular Transfer Length Method
DBR	Distributed Bragg Reflector
EDFA	Erbium Doped Fiber Amplifier
EDWA	Erbium Doped Waveguide Amplifier
EEL	Edge Emitting Laser
E_F	Fermi Level
FTIR	Fourier Transform Infrared Spectroscopy
ICP	Inductively Coupled Plasma
IPA	Isopropanol
L_T	Transfer length
MEB	Molecular Beam Epitaxy
MOCVD	Metal-Organic Chemical Vapor Deposition
OPSR	Optical Polarisation Suppression Ratio
PECVD	Plasma Enhanced Chemical Vapor Deposition
PL	Photoluminescence
RF	Radio Frequency
RIE	Reactive Ion Etching
RTA	Rapid Thermal Annealer
SEM	Scanning Electron Microscopy
SPICs	Silicon Photonic Integrated Circuits
TE	Transverse electric
TLM	Transfer Length Method
TM	Transverse Magnetic
UV	Ultraviolet
VCSEL	Vertical Cavity Surface Emitting Laser

Chapter 1

Introduction

1.1 Motivation

Since Miller *et al* [1] proposed the concept of integrated optics, there has been more and more interest to combine electronics and photonics. Nowadays, the silicon chip continuously scales down and almost approaches its size limitation [2]. It is difficult to improve the performance of integrated electronics furthermore since the wires are filled all over the space. A possible way to deal with this issue is to utilize optical signals in silicon integrated circuits. This method is called silicon photonic integrated circuits (SPIC). Compared with electrical signals, light beams have many advantages. Firstly, the optical signals have no problem crossing each other during propagation and they do not suffer the crosstalk issue. Secondly, different optical signals can propagate in the same optical waveguide structure, which provides possibilities to build high density integrated circuits. However, electronic devices are built on silicon that is an indirect band-gap material and is not able to emit light [3]. Therefore, various groups all over the world try to devise a reliable silicon photonic integrated circuits system [4][5][6][7].

A SPIC scheme has been proposed by the University of Leeds who reports an erbium doped silica-on-silicon with a gain of 5dB/cm [8]. This SPIC system is designed as a planar platform to generate 1.53 μm emission on silicon by on-chip optical amplifier erbium doped waveguide amplifier (EDWA). However, EDWA requires an optical pump source and a coupler to excite it efficiently. Two groups from the University of Glasgow and University of York then collaborated in the SPIC project. Figure 1.1 presents the organisation of this project. The University of Leeds provided an EDWA; the University of Glasgow provided the light source to pump the EDWA; the University of York provided a coupler and a photonic crystal membrane to enhance the optical amplification process. The diagram of this SPIC system will be demonstrated in the following.

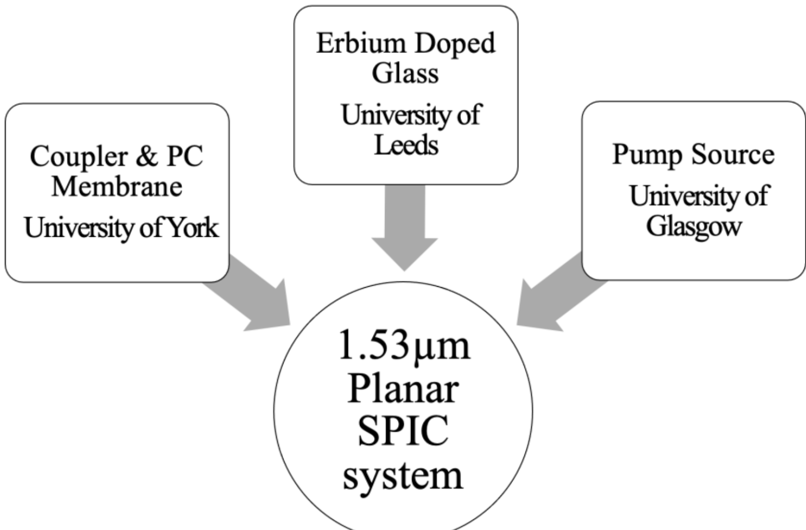


Figure 1.1 Organisation of silicon photonic integrated circuit (SPIC) project. The University of Leeds, the University of Glasgow and the University of York provided erbium doped glass, pump source and coupler respectively.

The target of the University of Glasgow (my PhD project) is to provide a pump source for erbium doped waveguide amplifier (EDWA). In order to explain the design of the pump source, this section presents a brief introduction of the EDWA and its requirements for a pump source.

The EDWA is an alternative to the erbium doped fibre amplifier (EDFA) but has a planar structure. Recently, the erbium doping concentration of the erbium doped glass has reported that it can be increased to ~0.53% [8]. It provides a condition to build a planar waveguide amplifier EDWA. Figure 1.2 presents a comparison between the EDWA structure and the EDFA structure [9]. As it shows, the EDWA has a rectangular shape of ~2 μm that occupies less space than the EDFA that has a length of 4 cm. The host material of the EDWA and the EDFA is silica that is easy to be grown on silicon. Therefore, the EDWA has been considered as an optimal candidate to generate 1.53 μm emission in silicon.

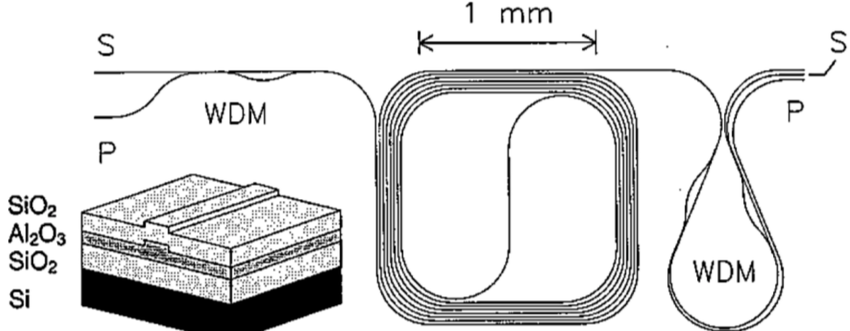


Figure 1.2 A structure comparison of the erbium doped fibre amplifier (EDFA) and the erbium doped waveguide amplifier (EDWA). The fibre characteristic of the EDFA let it occupy larger space in 2-D space, while the EDWA that has a core dimension of 0.6 μm×2 μm [9].

The host material of the EDWA, silica, is an insulator, which prohibits the EDWA to be electrical pumped. So far, optical pump is the only way to excite the EDWA. Two kinds of optical sources with different wavelengths can excite Er^{3+} in silica. Figure 1.3 presents the pumping processes in terms of erbium ions energy level. As figure1.3 (a) shows, 1.48 μm light pumps electrons in the ground state into the first excited state and then these electrons drop down to ground level that generates 1.53 μm emission.

Considering about using 980 nm pump light, shown in figure 1.3 (b), the electrons on the ground state are pumped to the second excited state. Due to a rapid decay of electrons, the population of electrons on the first state increases. Then, the electrons drop to the ground state with a slightly lower speed, which produces 1.53 μm emission. As we can see, 1.48 μm and 980 nm light sources both can excite Er-doped silica.

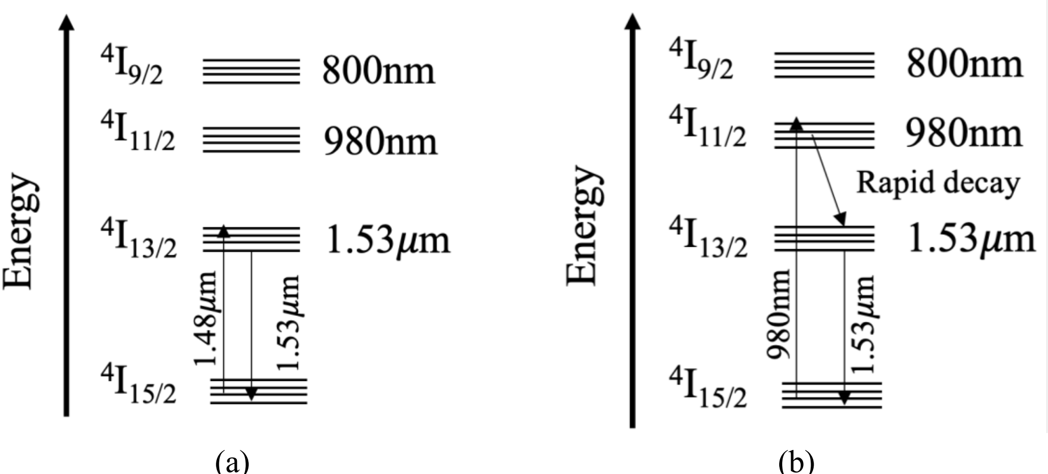


Figure 1.3 The energy level in Er^{3+} ions (a) the process of pumping Er^{3+} by1.48μm light source; (b) the process of pumping Er^{3+} by 980nm optical source.

However, the pump efficiency of the 1.48 μm and the 980 nm light are different. Figure 1.4(a) presents a comparison of them. This diagram plots the net gain of the Er-doped silica as a function of pump power [10]. The erbium doped glass used in this measurement is a 3 cm long fibre with 0.2% erbium doping concentration. As we can see, the Er-doped silica achieves higher gain by using 980 nm light source and this difference becomes obvious at pump power larger than 400 mW. It suggested that 980 nm light has a better performance.

Considering the bandwidth required for a 980 nm light source, a further investigation was carried out. Figure 1.4(b) presents the photoluminescence intensity of 1.53 μm emission generated by an erbium doped silica corresponds to the wavelength of the pumping source. It indicates that a pumping source with a wavelength range of 980±5 nm excites much higher power at a wavelength of 1.53 μm. Thus, light source with 980±5 nm wavelength is considered as an optimal pump source for an EDWA.

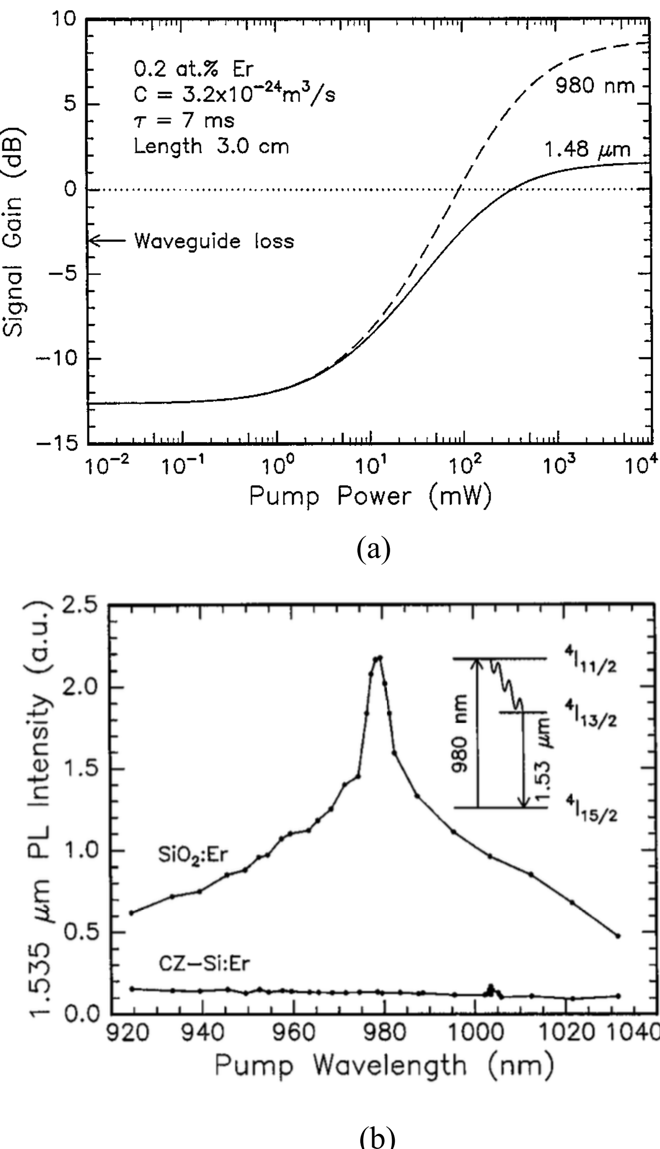


Figure 1.4 (a) The calculated net gain obtained from Er-doped silica as a function of pump power. Results are shown for two pump wavelengths: 980 nm and 1480 nm [10]. (b) The photoluminescent intensity of 1.53 μm emission of Erbium doped glass pumped by different wavelength light [10].

The pump power required by the EDWA varies with the Erbium doping concentration. Figure 1.5 presents the net gain of a 1cm long EDWAs with different doping concentration as a function of pump power. The samples used in this simulation have doping concentration of 0.06%, 0.20% and 1% respectively [10]. Sample with 0.06% erbium concentration approaches the maximum signal gain at a power of 200 mW. The 0.2% concentration erbium doped silica requires 1000 mW to get the saturated net gain. Due to the high Er^{3+} doping concentration, sample with 1% needs higher power that is out of plot range to obtain the the saturated net gain. In this project, 0.4%~0.53% erbium doping concentration glass is provided by the University of Leeds. Suppose the power required for it is double of the power needed for sample with 0.20% doping concentration. Thus, 2000 mW pump power

would be enough for a 1 cm long EDWA. However, EDWA has a size of about ~μm long [10]. Suppose the EDWA has a length of 100 μm, the essential pumping power would be about 20 mW.

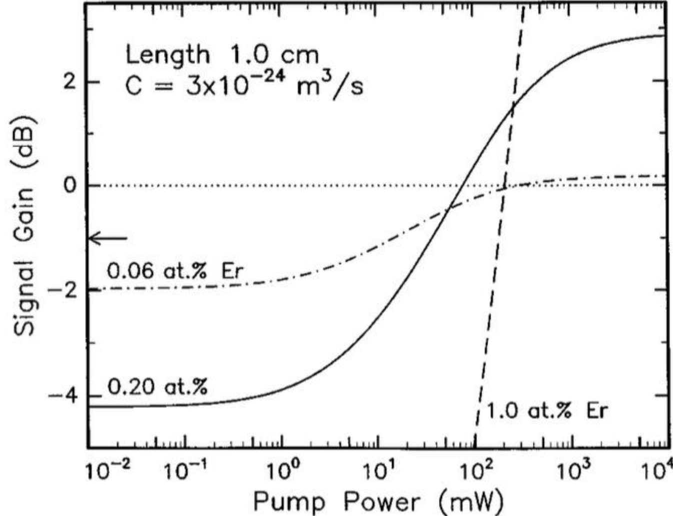


Figure 1.5 Calculation of the net optical gain of 1 cm long erbium doped silica with 0.06%, 0.20% and 1% doping concentration as a function of 980 nm pump power [10].

The structure of pump source decides the way for coupling light into EDWA. There are two methods: edge coupling and butt-coupling. Edge coupling is a way to pump the EDWA by an edge emitting laser. Figure 1.6 (a) presents the diagram of pumping EDWA by an edge emitting laser. This method has its advantage and its disadvantage. The pump light couples into the waveguide directly. So the structure of the whole SPIC system is simple and clear. However, this configuration requires a very precise alignment between the laser beam and waveguide. As the laser is made of III-V material that is separated from the Si wafer, it is difficult to bond it on the Si wafer at one specific position. Any small misalignment or position shift would lead to a significant coupling efficiency reduction. In addition, this alignment will be a very challenging and time-consuming job.

Alternatively, surface emitting lasers can be used to pump the EDWA. This method is called butt-coupling. Figure 1.6(b) depicts the diagram of the SPIC system utilizing surface emitting lasers as a pump source. The VCSELs are selected to demonstrate. The pump light travels into a coupler which converts a vertical emission to a horizontal one at first and then the pump light excites the EDWA. This design circumvents the alignment issue in using edge emitting pump source. The University of York that is involved in this project has reported a grating coupler used for butt-coupling with a coupling efficiency of 69% and a 3

dB bandwidth of 60 nm [11]. This coupler can be constructed on a Si wafer. Therefore, researchers working in the Seamatics project decided to use this butt-coupling design.

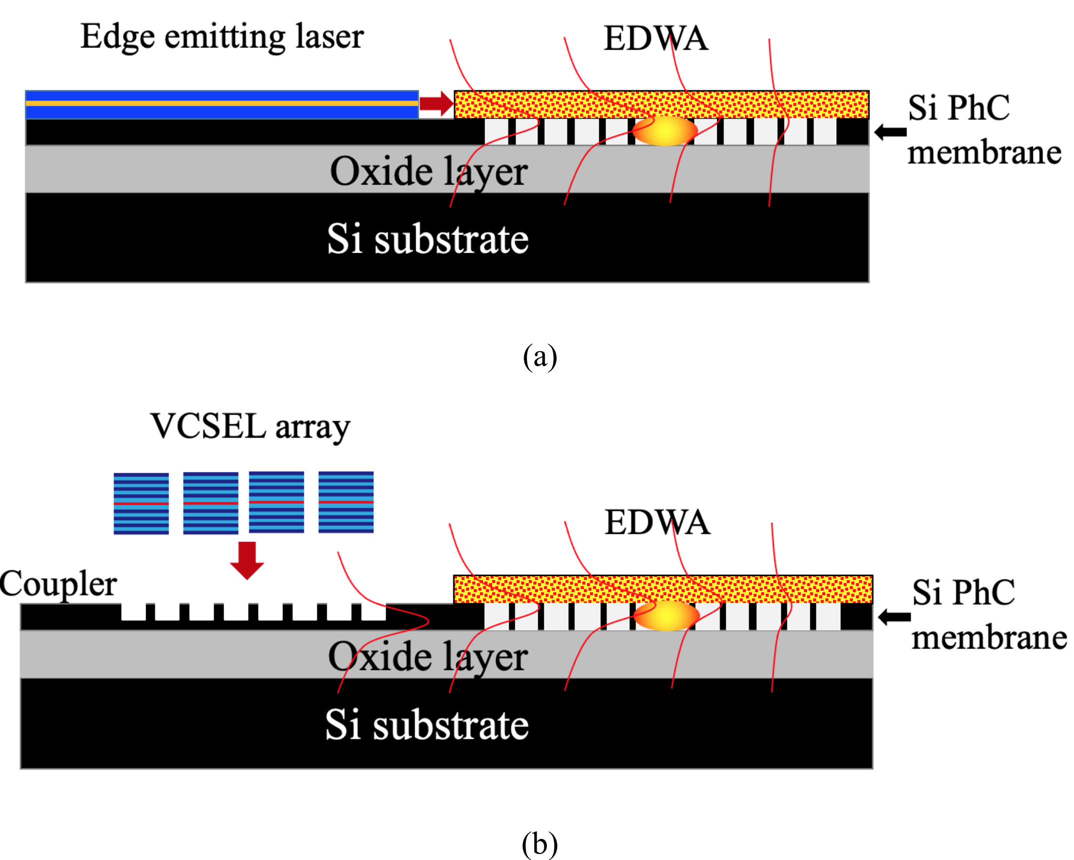


Figure 1.6 (a) A diagram of SPIC system that selects the edge emitting laser to pump the EDWA; (b) A diagram of SPIC system that selects surface emitting lasers to pump the EDWA. a coupler is used to convert the vertical pump light into horizontal. A Si photonic crystal membrane depicted in both (a) and (b) is utilized to enhance the amplification of the EDWA.

For this coupler, the propagation losses for the TM polarisation light are much higher than for the TE polarisation one [12]. The difference in losses suggests that the pump source should have a stable polarisation direction with a linear electrical field. Then the coupling efficiency of the coupler can be optimal. A high coupling efficiency not only reduces the total power required for the pump source but also prohibits extra heating generated in the SPIC system. The SPIC system is a potential commercial product and thus it should has a low-cost characteristic. This requirement also influences the selection of the type of pump source.

The requirements of this pump source for the EDWA are summarized in Table 1.1.

Parameter	Requirements for pump source	Comment
Wavelength	980± 5 nm [10]	Test results in ref [10]
Power	~20 mW for 100 µm long EDWA	Based on calculation results in ref [10] and erbium doping concentration reported in [9] –the University of Leeds.
Polarisation	Stable linear polarisation direction	Polarisation dependent coupling efficiency [11]
Geometry	Surface emission (substrate emitting)	Avoid alignment issue
Low-cost Approach	Minimise processing steps, and maximise yield	For volume applications

Table 1.1 Summarizes the requirements for a pump source used for EDWA in SPICs.

As discussed above, this SPIC system uses the VCSEL as a pump source. Firstly, this project prefers a 980 nm light source for pumping Erbium ions and the GaInAs-GaAs VCSEL can generate 980nm emission [13][14][15][16]. Secondly, VCSEL is a surface emitting laser that has a higher efficiency of generating [17]. The next section will present an introduction of the semiconductor laser system and demonstrate the structure and the characteristics of VCSELs.

1.2 VCSEL Devices

1.2.1 Introduction of Semiconductor Laser

The semiconductor laser is the mainstream of electrically pumped laser. It is popular for its micro-size and robust light emitting capability. The cavity of a semiconductor laser consists of an active region and mirrors. For instance, figure 1.7 presents a schematic of a cavity of VCSEL. The mirrors of VCSEL are placed above and below the active region, which reflects light to the active region and amplifies it continuously. Such structure resembles as an optical oscillator. As it shows, the light travels in a round loop and continuously get amplified until a lasing condition is achieved in this structure.

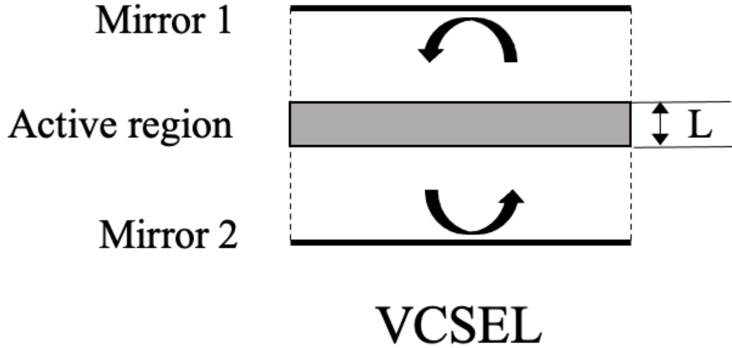


Figure 1.7 The cavity of a VCSEL that consists of two mirrors and an active region with the thickness of L.

The active region of a laser is a double-heterostructure diode made by direct bandgap material. Figure 1.8 presents a band diagram of a double-heterostructure under the forward bias condition. The Fermi level of the n-doped region, E_{Fc}, and the Fermi level of the p-doped region, E_{Fv}, has a potential difference, which induces the electrons and holes to flow into the intrinsic region. Due to the high density of electrons and holes, massive stimulation emissions generated in the semiconductor.

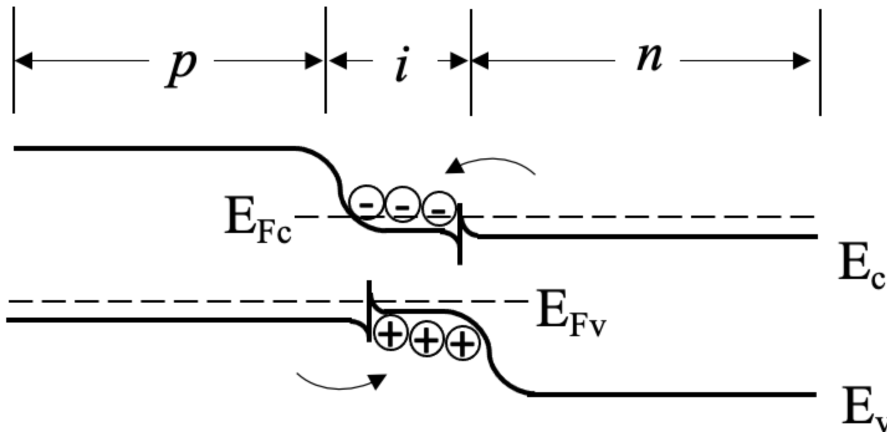


Figure 1.8 Band diagram of forward biased double-heterostructure diode.

Different lasers have different conditions to achieve lasing condition. In other words, each laser must obtain its own threshold gain, $g_{th.}$, to compensate for the loss and the transmission of the light in a cavity. The equation of $g_{th.}$ is presented in equation 1.1. L is the length of the cavity, for VCSEL, L is the thickness of the active region; R_1 and R_2 are the reflectivity of the two mirrors distributed above and below the active region; α is the internal loss. Γ is a confinement factor, defined as the ratio of the cavity volume occupied by photons over the

cavity volume occupied by electrons [17]. According to the equation 1.1, a laser with a short length demands high reflectivity mirrors to achieve a low threshold gain for lasing.

$$g_{th} = \alpha + \frac{1}{L\Gamma} \ln \frac{1}{R_1 R_2} \qquad 1.1$$

For VCSEL, the reflectivity of the mirror is up to 99.99%. The high reflectivity mirror employed in VCSEL is called distributed Bragg reflectors (DBRs). The device firstly applied the DBRs structure as a mirror was reported in 1987 [18]. After that, the researches on DBRs about its growth [19] and doping [20] has been well studied. Nowadays, the DBRs is an optimal high reflective mirror for VCSELs. Figure 1.9 shows a diagram of DBRs. It is a periodic structure that provides strong reflection for a particular wavelength or wavelength range of light [21]. Each period Λ, consisting of two layers with an index difference, works as a weak mirror. The length of each layer equals a quarter of the wavelength.

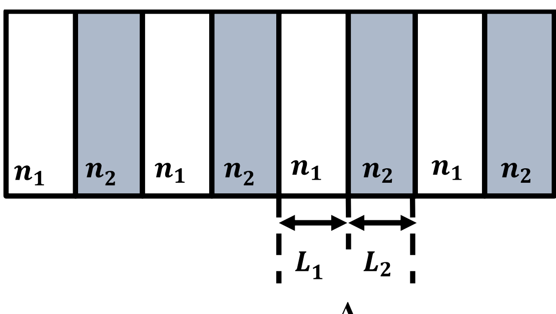


Figure 1.9 A diagram of DBRs that has a period of Λ. Each period consists of two materials with the refractive index of n_1 and n_2 respectively. The length (L_1 and L_2) of each layer equals a quarter of the wavelength.

The reflectivity of the DBRs structure with pairs of m constructed by the quarter wavelength thick layers can be calculated by equation 1.2. As the equation 1.2 shows, the reflectivity of the DBRs varies with the refractive indice of materials. With the same number of pairs, the DBR constructed by the materials with a larger refractive index difference has a higher reflectivity. Apart from the material refractive index, the reflectivity of DBRs also varies with the number of pairs. It rises up by increasing the number of pairs.

$$\boldsymbol{R_{DBR}} = \left(\frac{\mathbf{1} - \left(\frac{\boldsymbol{n_1}}{\boldsymbol{n_2}}\right)^{\boldsymbol{2m}}}{\mathbf{1} + \left(\frac{\boldsymbol{n_1}}{\boldsymbol{n_2}}\right)^{\boldsymbol{2m}}} \right)^{\mathbf{2}} \qquad 1.2$$

Figure 1.10 presents an example to illustrate the reflectivity of DBR with different pairs. As it shows, the 30 pairs DBRs has a reflectivity of 99.99%, while the 10 pairs DBRs only has a reflectivity of 80% for the light with a wavelength range from 0.94 to 1.03 μm. The 20

pairs DBR has a reflectivity slightly lower than the 30 pairs one. Thus, the reflectivity of DBRs increases with the number of pairs. Due to the high reflectivity of the DBRs, many kinds of low threshold VCSELs have been devised [22][23]

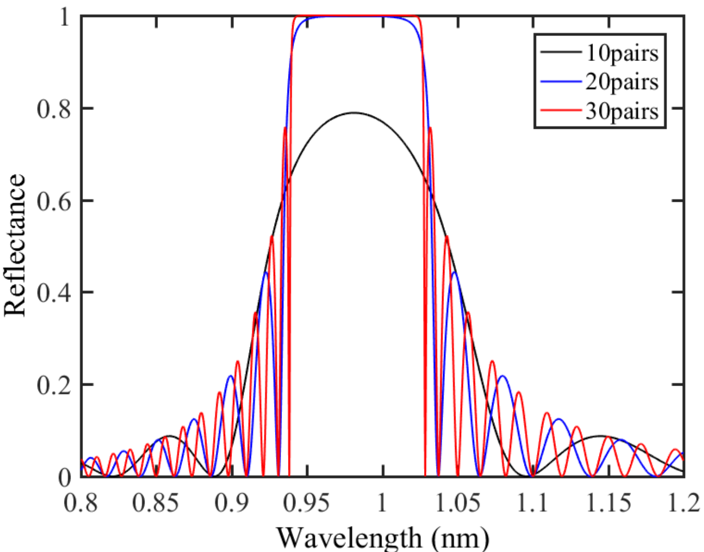


Figure 1.10 The reflectance of different pairs of DBRs versus the wavelength of light. The computed reflectance is based on the refractive indices of AlGaAs DBR materials.

1.2.2 History of VCSEL

The first vertical cavity surface emitting laser (VCSEL) was invented in the Tokyo Institute of Technology in 1979 [24]. It is a milestone of the surface emitting lasers generation. VCSEL is composed of two mirrors and a thin active region about a few micrometres thick. A schematic diagram of a VCSEL is presented in Figure 1.11. The first VCSEL has a diameter of 100 μm and is operated in pulse condition at 77 K. Although the performance of it cannot compare with the devices produced currently, it gave insights on having laser with surface emitting property.

VCSELs have a number of advantages. Firstly, VCSELs are easy to construct two dimensional (2D) array and such laser array is desired for the laser printer and the face reorganisation system. Secondly, the VCSEL with a circular shape can provide a circular beam. As the circular light beam has an higher coupling efficiency in fibre, it is preferred in fibre coupling system. In addition, VCSELs have a low threshold current due to the small volume active region. The lowest threshold of VCSEL reported in the literature is about 77 μA [25].

However, VCSEL also has its disadvantage. It is difficult to achieve devices with emission in blue, green and telecommunicated wavelength (1.3~ μm or 1.5~ μm). The reason of it is that the materials of DBR structure that provides a high reflectivity for these wavelength is difficult to growth on GaN or InP wafer. Therefore, it is challenge to achieve low resistance and low threshold current VCSELs in these emission ranges.

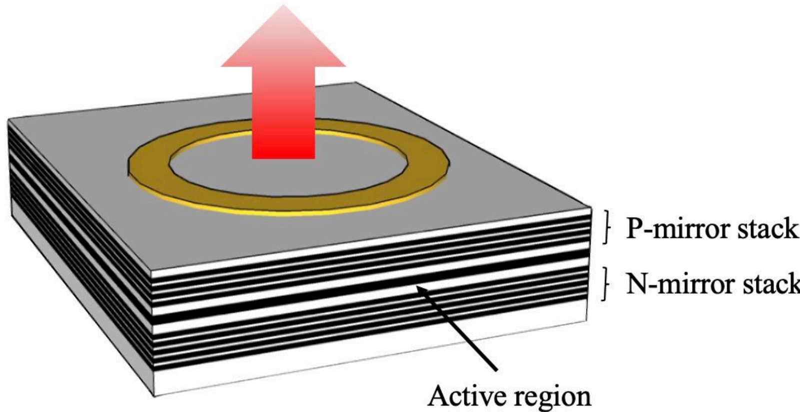


Figure 1.11 A schematic of a typical VCSEL structure. It contains p-doped mirror, n-doped mirror and active region. The current is injected through the circular contact (yellow) and the emission comes out from the surface along the arrow direction.

The VCSEL has been intensively studied during the last four decades because of its superior characteristics compared with conventional edge emitting laser (EEL). The apparent difference between VCSEL and EEL is the emission direction. EEL emits light at the edge. Figure 1.12 presents a schematic of the structure of an edge emitting laser. This structure prohibits it to configure a two-dimensional array. In contrast, VCSEL has the advantage of forming a 2D array due to its structure [26][27][28]. Moreover, a surface emitting laser can be examined on a wafer scale, which reduces the cost. For EELs, devices have to be cleaved from the whole wafer to construct mirrors before testing. In this respect, VCSEL has an advantage in manufacturing. Considered the beam shape, VCSEL with a circular aperture delivers a circular beam pattern [29]. EEL has difficulties to achieve that. As figure 1.12 shows, the light beam of EEL emits from the side of the wafer thereby it has an elliptical shape. Some applications require circular beams, for instance, fibre coupling [30], which prefer VCSELs. In terms of packaging, EEL must be precisely aligned to its heat sink so its output beam will be not obscured. However, VCSEL is easy to be packed as the beam of it can be away from the heat sink [31].

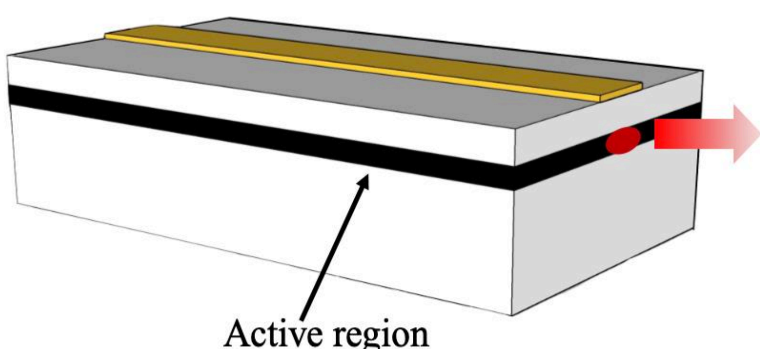


Figure 1.12 A schematic of an edge emitting laser. The elliptical beam shape and the propagation direction of the light output are labelled.

Another advantage of VCSEL compared with EEL is the fabrication simplicity. The top DBRs, active region and the bottom DBRs of VCSEL has been constructed during the growth process. Therefore, the fabrication procedures of VCSEL only requires a few steps of ion-planting (or etching or oxidizing) and contacts deposition [32]. As discussed above, VCSEL has a simpler fabrication process than the EEL and its fully monolithic processes yielding very low-cost chip production. Furthermore, VCSEL has a shorter active region than the EEL. A single longitudinal mode VCSEL can be fabricated effortlessly due to such a short cavity. A single mode EEL has to be constructed with the help of precise grating. Otherwise, the emission inevitably to contain many longitudinal modes. Although single mode edge emitting lasers have been reported, the complex fabrication process is not competitive to VCSEL.

1.2.3 Optical and Electrical Confinement Techniques

This section presents four techniques that are widely employed to configure a VCSEL. They are air-post, ion-implanting, regrowth and oxidized layer method. Figure 1.13 depicts the structure of different types of VCSEL [33]. Each of them has its advantages and disadvantages. The objective of these methods is to deliver strict current confinement in order to pump the device effectively. The following introduce each method in detail.

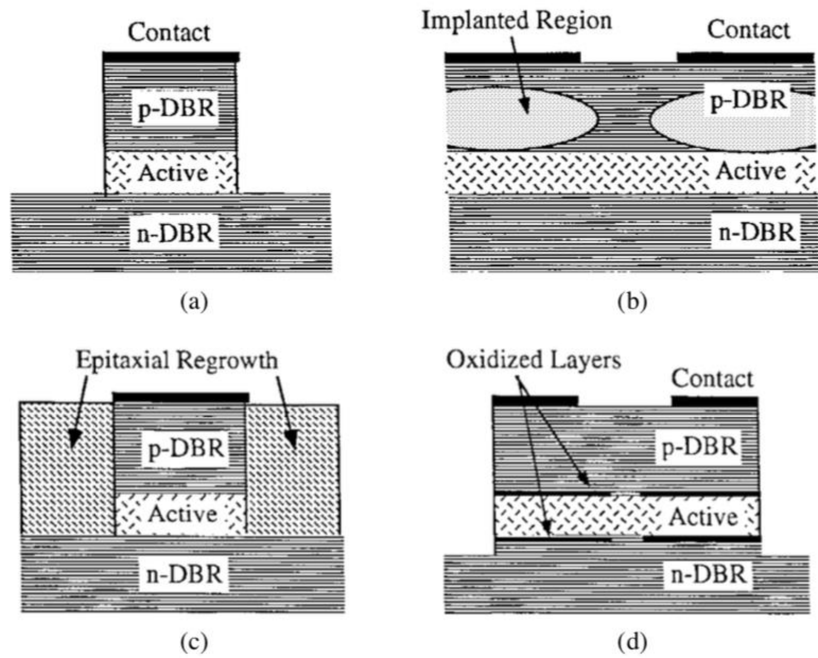


Figure 1.13 Four basic structure of VCSELs: (a) etched air-post, (b) ion-implanted, (c) regrown buried heterostructure and (d) oxide-confined VCSELs [32].

Airpost: The air-post method configures a pillar of VCSEL (shown in figure1.13 (a)) by using an anisotropic etching tool such as dry etching equipment. It is the easy way to fabricate an airpost VCSEL. The natural index difference between air and the semiconductor contributes to good confinement on both electrical field and optical field [34]. However, devices fabricated by air-post suffers from non-radiation recombination at the sidewall [35]. It is a challenge to achieve a low threshold and high efficient air-post VCSEL.

Ion-implanting: Ion-implanting is an alternative way to prevent the current from spreading. As it shows in figure 1.13(b), the region where the ions implanted loses its conductivity, which avoids the current spreading into it [36]. Since the refractive index of material merely changes during the ion planting process, this method has a weakness in optical guiding [37]. Furthermore, it is difficult to precisely control the area of ion implanting. To evade damage, there is a gap between the ion implanting region and the active region. This inhibits a small diameter VCSEL to be constructed with this method [37]. However, this method provides a good heat sink for the device since the material has not been etched away

Regrowth: The regrowth approach makes use of the refractive index difference of two kinds of semiconductor materials then configures a VCSEL shown in figure 1.13 (c). As a range of regrowth materials can be selected, the index difference of materials between VCSEL wafer and regrowth material can be large [38]. This method provides an excellent optical guiding and electric field confinement for devices. However, two epitaxial growth sequences

are time-consuming and they increase the manufacturing cost. VCSELs fabricated by regrowth methods have been reported of low threshold, high efficiency and small aperture available [39][40].

Oxidized layer: A thin layer with high aluminum content that grown above (and below) the active region is used to confine the injected current of VCSEL. This layer is sensitive to oxygen and the refractive index of it varies drastically before and after oxidizing. As figure 1.13(d) shows, a small aperture can be constructed by precisely governing the temperature and time of the oxidizing process [23]. Since the oxidised part turns to be an insulator, the current is blocked to spread into the surrounding material and it funnels into a defined area. Ultra-low threshold VCSEL has been reported by utilizing this method [41]. The challenge of this method is to inspect the shape of the oxidizing aperture and control the flow speed of gas during the oxidizing process. However, the excellent performance of VCSELs constructed by this method leads this method to be widely used in commercial.

VCSELs have been utilized commercially in many optical systems such as optical networks, parallel optical interconnects, laser printers, high-density optical disks and so on [25]. Due to its excellent characteristics such as circular optical beam and surface emitting, VCSEL becomes more and more popular and difficult to be replaced. However, it has its disadvantages including large resistance, low power single mode device and polarisation unstable.

1.3 Polarisation Issue of VCSEL

For the surface emitting device, the electric field of emission lays in the plane of active region. If there is no anisotropic factor, the lasing mode with electric field along any direction in the active region plane can achieve lasing. So, in the VCSEL, it is possible to lase at any polarisation direction. After lasing, if the spatial hole burning effect happened, the selected lasing mode could be switched off and another lasing mode can be selected. Therefore, the polarisation of emission also changes with injected current.

In summary, the VCSEL suffers from randomly polarisation issues. Firstly, the dominant polarisation direction of VCSEL is randomly from one device to another [42]. Figure 1.14 presents a diagram of the random polarisation direction of VCSELs. Thus, the polarisation direction of emission varies from device to device. Secondly, the polarisation direction of emission fluctuates with the injected current for the VCSEL devices.

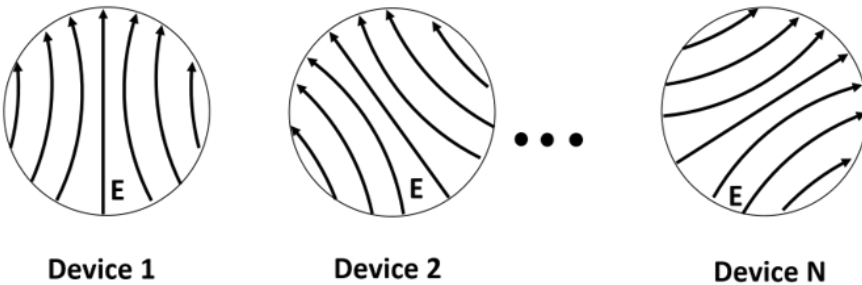
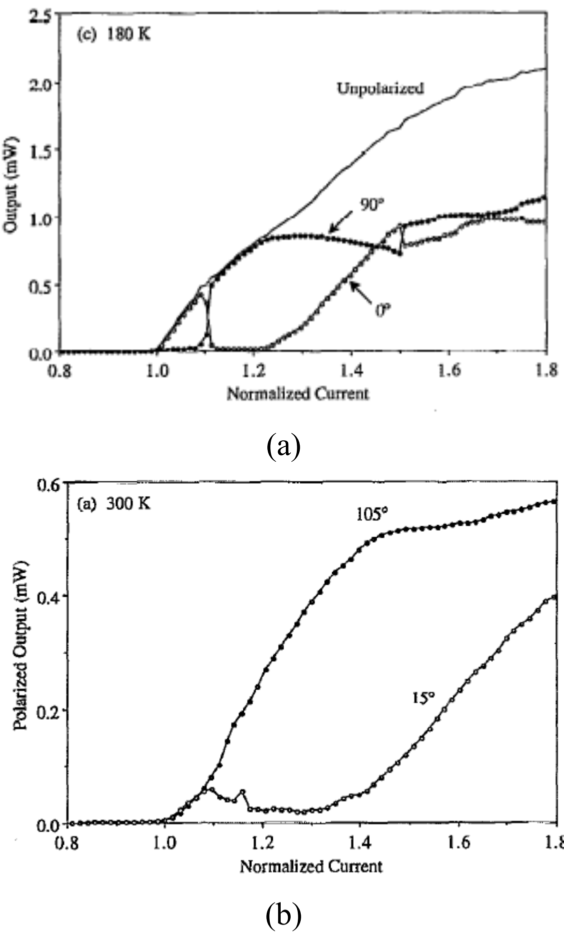


Figure 1.14 A schematic of random polarisation condition of cylindrical VCSEL. The linear polarisation orientation varies from one to the other

It has been reported that the polarisation direction of VCSELs distributes randomly in the plane of the active region and it fluctuates with injected current and temperature [42][43]. Two orthogonal polarisation states were observed in the emission of a proton implanted gain guided, 20 μm diameter VCSEL [44]. The polarised light intensity (LI) curves of a 20 μm diameter proton implanted GaAs/AlGaAs/AlAs VCSEL were investigated as a function of temperature. As figure 1.15(a) shows, the emission consists of 0° and 90° polarised modes, w.r.t the [110] crystal axis at 180K. An abrupt polarisation switching firstly happened at I= $1.1I_{th}$ and then at I= $1.45I_{th}$. The polarisation performance of this device changes significantly with the injected current. Figure 1.15(b) presents the polarisation behaviour of this device at 300 K. Two eigen polarisation states coexisted at this condition. However, the orientation of them rotated to 105° and 15° respectively. There was no polarisation switching observed. As we can see, the polarisation performance of VCSEL is sensitive to injected current and temperature.



(a)

(b)

Figure 1.15 Polarised LI curves of a 20 μm diameter VCSEL measured at 180 K (a) and 300 K (b) respectively [43].

1.4 Methods to Control Polarisation of VCSEL

Several methods have been developed to control the polarisation of VCSELs, and they can be divided into three categories: anisotropic loss, anisotropic feedback, and anisotropic gain. This section demonstrates some typical methods of each category and presents a summary of the developed methods at the end.

1.4.1 Anisotropic Gain Methods

In 1992, T.Mukaihara proposed a method to control the polarisation of VCSEL by inducing anisotropic stress into the device [45]. In this study, an elliptical hole (100 μm deep, 20 μm wide and 30 μm long) was etched into the substrate of a substrate emitting VCSEL. The major and minor axis of the elliptical hole was aligned with the $[01\bar{1}]$ and $[011]$ crystal axis respectively. It was found that the dominant polarisation direction of the emission

orients at the major axis of the elliptical hole, $[01\bar{1}]$ crystal axis, for drive currents up to 1.8 times threshold.

To further enhance the stress of the etched elliptical hole, a thick metal layer was deposited on the top surface [46]. Figure 1.16 presents the schematic structure of this elliptical VCSEL with a bowed substrate. Due to the different thermal expansion coefficient between the GaAs and gold film, a bowed epitaxial layer is formed by heating the device up to 300 °C then cooling it down to room temperature. About 80 percent of devices were shown that their major polarisation direction is along the major (A-A) axis. The elliptical device has a threshold of 60 mA under pulsed condition and has an elliptical beam shape. This method develops a polarisation stable VCSEL and it claims that the etched elliptical hole generates anisotropic stress which leads to a gain difference in orthogonal polarisation states [47].

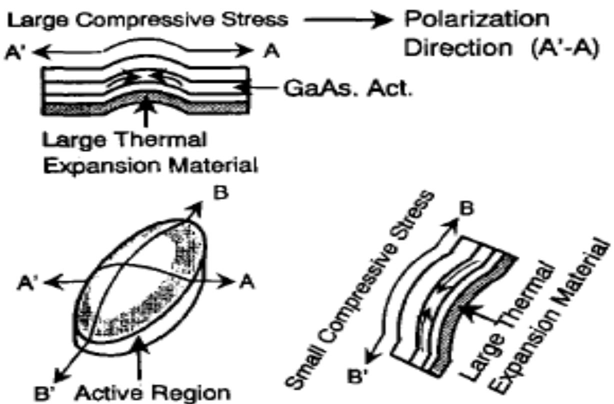


Figure 1.16 VCSEL with an elliptical hole etched into the substrate where the light output coming out. The epitaxy layers was bended due to the thermal expansion coefficient difference between semiconductor and gold film. The anisotropic stress has been introduced by the etched hole and the bended elliptical structure [46].

Another method of controlling the polarisation direction of VCSELs is to grow the structure on a [311] GaAs substrate [48][49][50]. A top emitting rectangular (6 μm ×3 μm) VCSEL was fabricated on this substrate with the long side along with $[\bar{2}33]$ crystal axis. A diagram of the device cross-section is presented in figure 1.17(a). The emission has a stable polarisation direction along with $[\bar{2}33]$ direction. In this study, polarised photoluminescence (PL) spectra of the quantum wells and the reflectivity of DBRs were measured along $[\bar{2}33]$ and $[01\bar{1}]$ directions. Figure 1.17(b) presents the measurement results. The amplitude of the PL spectrum measured along $[\bar{2}33]$ is higher than it measured along $[01\bar{1}]$ direction, while the reflectivity has no difference on two orthogonal polarisation directions. It indicates that

a gain preference along $[\bar{2}33]$ crystal axis generated through using [311] GaAs substrate stabilises the polarisation direction of VCSELs.

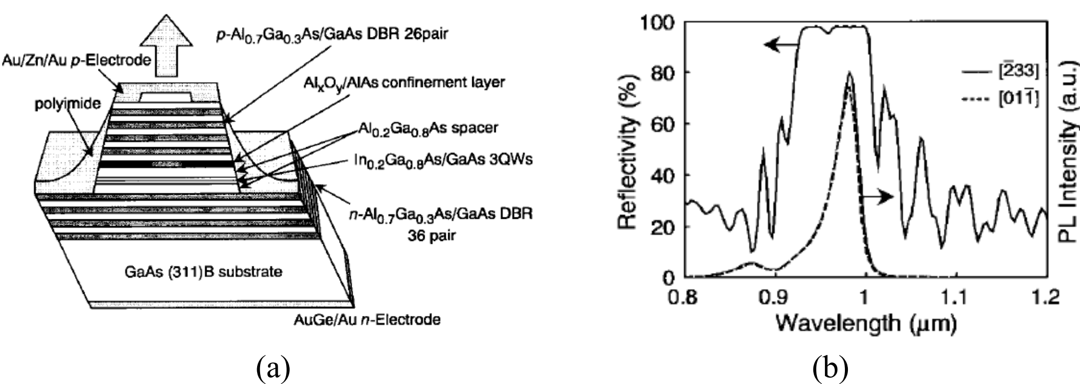


Figure 1.17 (a) A diagram of vertical cavity surface emitting laser fabricated on a GaAs [311] substrate; (b) The reflectivity of the DBRs and PL measurement results of the active region plotted against the emission wavelength [49].

The current injection geometry can influence the polarisation direction of circular VCSELs as well. In 2000, Y.Zheng proposed an intra-cavity VCSEL which is defined with contacts formed above and below the active region with two pairs of p-and n-contacts constructed [51]. Figure 1.18 presents the structure of the device. One pair of contacts, N1P1, controls carrier distribution/injection along the [110] crystal axis and the other pair of contacts, N2P2, controls carrier distribution/injection along the $[1\bar{1}0]$ crystal axis. When current was injected through N1P1 or N2P2 contacts, the polarisation direction of the emission orients at 40° or 120° from the [110] crystal axis, respectively. A polarisation switch was observed by using N2P2 contacts. This method had been found invalid for square VCSELs and suggested a circular VCSEL was a better candidate to study the polarisation property corresponding to the current injection direction. This specific reason for structure preference is unknown.

Previous work indicates that inducing stress and controlling current injection direction both have effects on controlling the polarisation direction of emission. Anisotropic gain can also be achieved through the use of novel substrate but such substrates are not widely available, and of unknown quality [52]. Stress methods seem to provide a way to induce gain difference and then deliver a stable polarisation performance for VCSELs.

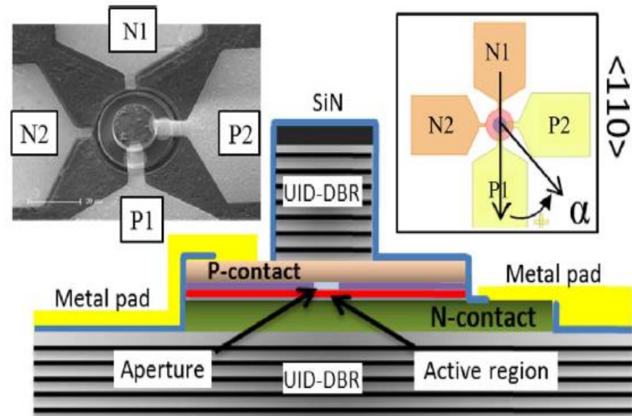


Figure 1.18 A schematic diagram of the intra-cavity VCSEL designed to control the current injected direction with two pairs of p- and n- contacts. Inset at left shows the top view of the VCSEL and the inset at right indicates the orientation of contact pads corresponding to the crystal axis [110] [51].

1.4.2 Anisotropic Feedback Methods

Alternatively, the polarisation direction of VCSELs' emission can be selected through anisotropic feedback. The mirrors used in VCSEL are DBRs that are not sensitive to polarisation. This kind of method aims to provide a reflectivity difference to the different polarisation states. Here introduces two methods that both use gratings as a polarisation sensitivity mirror.

In 1995, a method that builds a metal-interlaced grating at the top layer of top DBRs was developed [53]. The subject of this method are top emitting VCSELs with a diameter larger than 10 µm (so expected to be multimode). Figure 1.19 presents the schematic diagram of the device. As it shows, a grating with a period of 0.9 µm, 1.2 µm or 1.5 µm has been etched on the top layer of top DBRs and the sidewalls of the grating are covered with a metal film. A polariser can also be formed by making a sub-wavelength periodic array of metal lines. It has been found that 15 µm, 20 µm and 30 µm diameter devices with the grating period of 1.2 µm or 1.5 µm operate with a stable polarisation direction perpendicular to grating grooves. However, the devices with a grating period of 0.9 µm have a weaker ability to control polarisation. The 10 µm diameter VCSEL failed to lase and this may be due to misalignment of implant mask as claimed in the paper [56]. In summary, this metal-interlaced grating method achieves polarisation stable multimode VCSELs by providing feedback difference between orthogonal polarisation states.

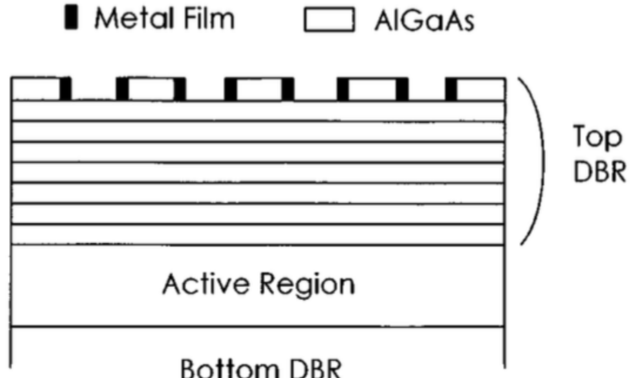


Figure 1.19 Schematic drawing of the top emitting VCSEL with a metal-interlaced grating etched into the top layer of top DBRs. Metal file is deposited at the side wall of the grating that has a period of 1.5 μm [53].

The polarisation properties of grating patterned VCSELs are presented in the following. The grating method was further studied through theory and experiments from 2004 to 2006 [54][55][56][57]. A period of grating without metal at the sidewall is etched into a cap layer grown on top of the top-DBRs. Different grating orientations, grating period, grating depth and even different thicknesses of cap layer have been investigated to control single or multimode surface emitting VCSELs. Figure 1.20 presents a picture of the grating patterned VCSEL [54]. It illustrates a VCSEL having a grating with a period of 1 μm and a depth of 21 nm etched into the cap layer.

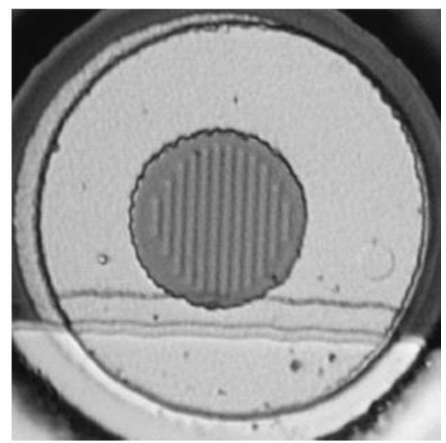


Figure 1.20 Top emitting VCSEL with a surface grating etched into the cap-layer [54].

The polarisation properties of grating patterned VCSELs are presented in the following. The direction of the grating plays an important role in the polarisation direction of the emission for VCSELs. Figure 1.21 presents a comparison between grating etched along $[011]$ and $[1\bar{1}0]$ crystal axis. Both of the 4 μm diameter devices have a 1 μm period grating with an

etching depth of 21 nm patterned on the surface. As figure 1.21 shows, the device with grating patterned along [011] has the dominant polarisation along [011] direction. Similarly, the device with grating patterned along and $[1\bar{1}0]$ has a dominant polarisation along $[1\bar{1}0]$ direction. It seems that the dominant polarisation follows the orientation of the grating. However, it was found that the dominant polarisation direction is perpendicular to the grating grooves when the grating periods change to 1.2 μm. Therefore, the polarisation direction of the emission is not only determined by the orientation of the grating but also related to grating period.

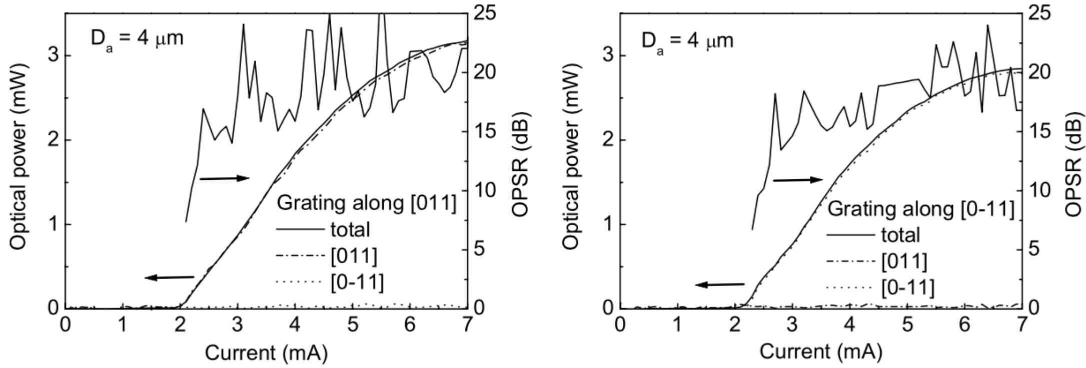


Figure 1.21 Two VCSELs with a surface grating with a period of 1 μm and an etching depth of 21 nm. The grating of them is etched along [011] and [0-11] crystal axis respectively [54].

The performance of the grating device varies significantly with the period of gratings. Different period of grating has a different polarisation direction referred to the grating orientation. For instance, device with 1.0 μm period has the polarisation direction parallel to grating, while device with 1.2 μm period has the polarisation perpendicular to the grating.

Also, the large period grating VCSEL has a smaller mean reflectivity and consequently increases the threshold of devices. The threshold of the grating devices is also affected by the cap layer thickness. It was reported that the transmission coefficient of a top Bragg mirror changes periodically with the thickness of the cap layer [57]. The threshold current of the grating device varies with the thickness of the cap layer.

In addition, the depth of the grating is related to the device characteristics. It was found devices with a shallow grating (35 nm and 52 nm) have a larger threshold than no grating devices but the deep grating (90 nm and 105 nm) ones have a small change for the threshold.

There is a disadvantage to the grating patterned device. A surface grating with a period similar to or larger than the emission wavelength can lead to strong diffraction [57]. It was reported that the far-field pattern of the emission with polarisation direction orthogonal to

the grating grooves has side lobes. The amplitude of these side modes reduces as decreasing the period of the grating. It suggests that small period grating VCSEL would have a better far-field performance.

1.4.3 Anisotropic Internal Loss Methods

Apart from anisotropic gain and feedback, the intrinsic loss of the laser mode can also be made anisotropic. Several methods have been explored to control the polarisation through this principle [58][59].

In 1994, Choquette introduced two kinds of anisotropic transverse cavity VCSEL with dumbbell and rhombus shapes [58]. Their polarisation characteristics were compared with a circular shape VCSEL having an equal cross-section. The shapes of the devices are presented in figure 1.22. It was found that the polarisation direction of the dumbbell shape VCSEL orients at 0° along [110] crystal with an extinction ratio of 14 dB. The polarisation stability reduces for rhombus shape VCSEL and was even weaken for a circular shape VCSEL. It infers that the internal loss of the 90° polarised mode is larger for the dumbbell shape VCSEL. Such loss difference leads the polarisation direction of the dumbbell shape VCSEL performs a stable polarisation direction along 0°. However, this method is only valid for small diameter devices and it is not reliable/applicable for large diameter devices.

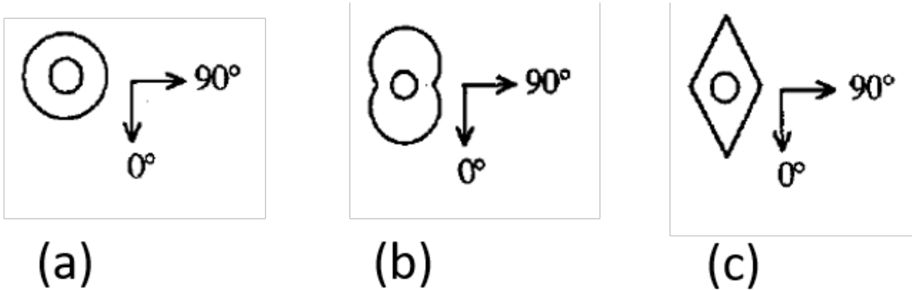


Figure 1.22 Schematics of (a) circular, (b) dumbbell and (c) rhombus shape VCSELs having a diameter of 5 µm. 0° indicates [110] crystal axis [58].

1.4.4 The Method Selected to Study

This section will introduce a method selected for the VCSEL pump source. The technique of this method is to etch trench(es) next to the aperture of the VCSEL [60][61][62]. It was reported that it successfully pin the polarisation of emission to one direction. The first part of this section will present the structure and characteristics of VCSELs with an etched trench(es). Following, it summarizes the investigation of trench effects on pinning

polarisation. In the end, the reasons for selecting this method for the design of a pump source will be given.

In 1997, P.Dowd demonstrated an approach to pin the polarisation direction of VCSEL by etching a single trench [60]. A 20 µm long, 1µm wide trench was etched 1 or 2 µm away from the aperture of the device by the focused ion beam. The diagram of the device is shown in figure 1.23(a). The polarisation direction of this top emitting VCSEL was pinned perpendicular to the trench and the polarisation ratio defined as the maximum polarised power over the minimum polarised power increased from 46 to 105 after trench etched. There was no significant change in threshold and total power of the device before and after trench etched.

Two years later, L.J.Sargent from the same group reported a 13 µm VCSEL with two parallel trenches etched [61]. Figure 1.23(b) presents a picture of the VCSEL with two 20 µm long trenches patterned 3 µm away from the aperture. The dominant polarisation direction of this VCSEL is parallel to the trenches and the emission of the device performs a polarisation ratio of 145 between orthogonal polarisation states. The polarisation ratio significantly increased after etching trenches and further improved after annealing the device. It also reports that the polarisation ratio varies with the trench angle. VCSELs with single trench etched at an angle from 0° to 90° have been examined. Figure 1.23 (c) shows the diagram of this device. The measurement results indicate that the polarisation ratio achieves the maximum value for VCSELs with trench etched at 0° and 90°.

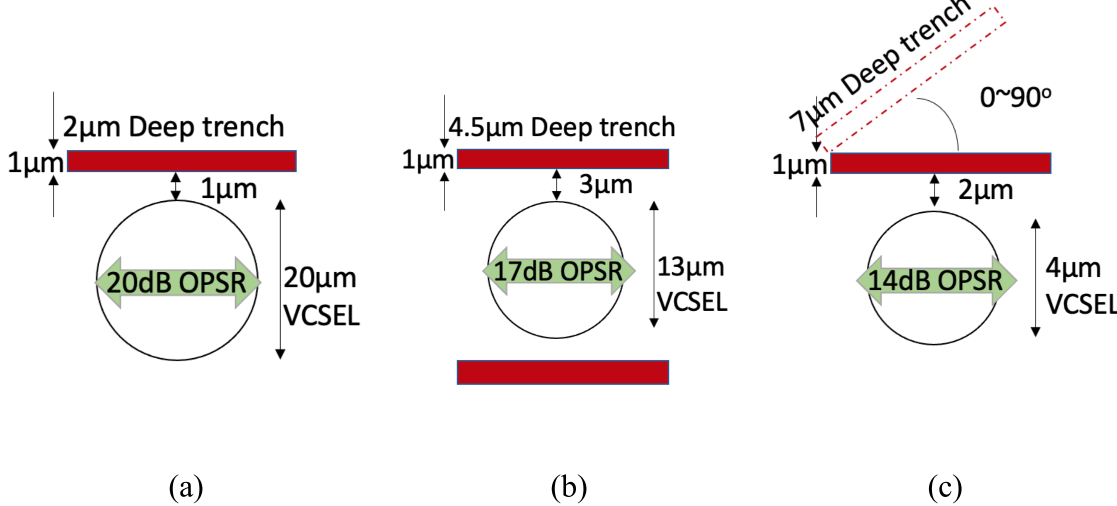


Figure 1.23 Diagrams of trench-etched VCSEL: (a) single trench-etched 20 µm VCSEL; (b) double trench-etched 13 µm VCSEL; (c) 4 µm VCSELs with single trench etched at different angle.

To investigate the effect of the etched trench, photoluminescence spectra were measured for

orthogonally polarised emission with unprocessed VCSEL before trench etch, after trench etch and after device annealed. Figure 1.24(a) present the measurement results. As figure 1.24(a) shows, the peak of the PL spectra for the normal polarised emission shifts 0.2 nm after trench etch. It indicates an anisotropic factor is induced by the line etches in this direction. Such anisotropic factor may be the reason for pinning the polarisation of circular VCSELs. Figure 1.24(b) presents Raman test results of the unprocessed wafer before trench etch, after trench etch and after device annealed. Before etching, there is a peak located at 260 cm^{-1} wavenumber. After etching, the amplitude of this peak decreased significantly and the width of it increases. It infers that the crystal structure is affected by the line etches. The Ramen test result measured after annealing is also different from the result measured after etching. This is due to the effect of the annealing that changes the crystal structure by varying temperatures.

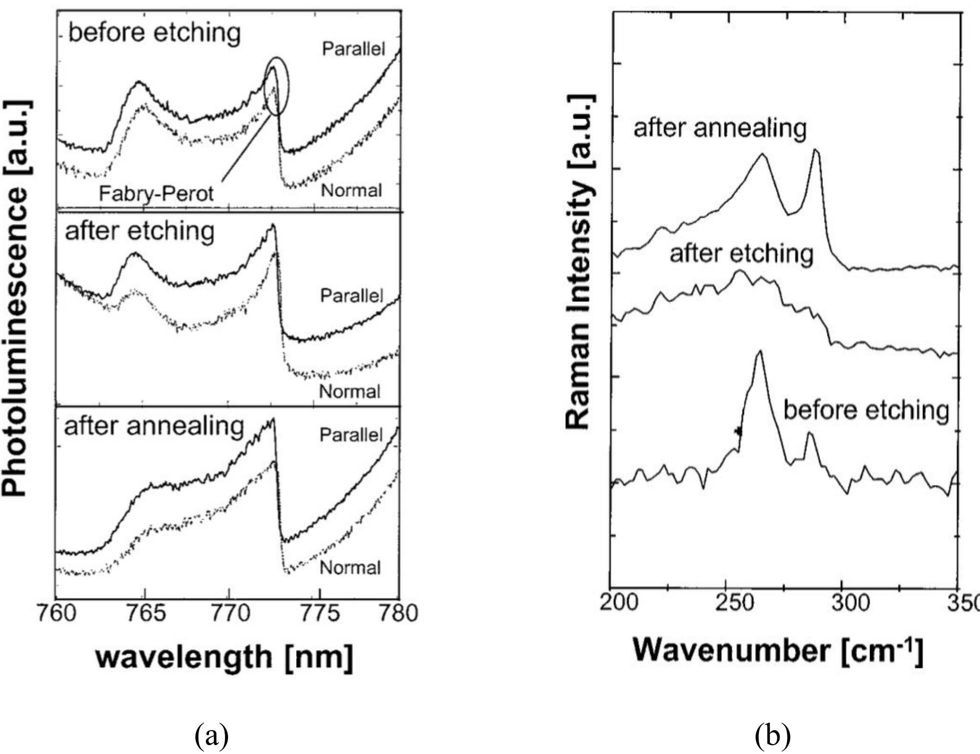


Figure 1.24 (a) Photoluminescence spectra, recorded at 80 K and (b) Raman spectra measured for the unprocessed wafer prior to etching, after etching and after annealing [61].

The shift observed in the measurement results infers that the etched trench leads to a gain difference on different polarisation states. A possible explanation of this phenomenon is that the gain spectrum of orthogonal polarisation states shifts in different distance against wavelength. Figure 1.25 presents diagrams of gain spectrum in different conditions. As shown in figure 1.25(a), the gain spectrum of different polarisation states is overlapped. Thus, the

cavity mode can be excited at both polarisation states that have orthogonal directions. However, as shown in figure 1.25(b), once there is a peak shift of gain spectrum of orthogonal polarisation states, the lasing mode would have a polarisation selection and perform a stable polarisation direction parallel to trench. This may be the principle of trench-etch method.

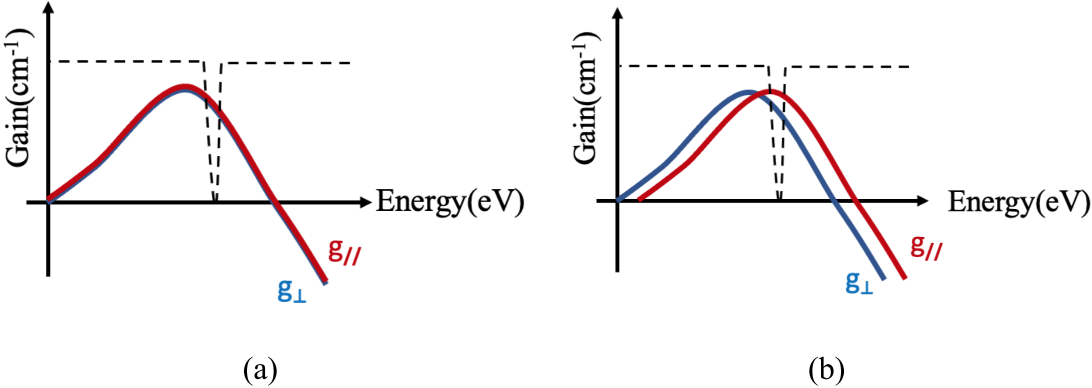


Figure 1.25 Diagrams of gain spectrum of orthogonal polarisation states for : (a) a VCSEL without birefringence property; (b) a VCSEL with an anisotropic factor. The dash line indicates the cavity mode of device.

As discussed above, this trench method induces an anisotropic factor to the device material which stabilises the polarisation of a top emitting VCSEL. The major advantages of this technique include its simple structure; strong pinning effect; availability on large diameter VCSELs. In this project, a substrate emitting VCSEL is preferred. Methods like grating patterns require complex fabrication techniques. For instance, to etch a period of grating on the aperture, the substrate has to be polished at a certain thickness and then etch a grating on it. It is a challenging job. Meanwhile, the emission of a pump source is not necessary to be single mode. The trench method that works on large diameter devices would be an excellent choice for this project.

1.5 New Device Structure

This section aims to present a VCSEL structure designed for this SPICs system. At first, a summary of the requirements for this pump source and the characteristics of previous trench-etched VCSEL is presented in table 1.2. As mentioned before, the requirements for the VCSELs: (1) substrate emitting; (2) metal contacts on top; (3) etching two trenches; (4) suit for SPICs system. In the SPICs system, a coupler is placed below the VCSELs which prohibits the pump source to have a metal contact at the substrate. The trench-etched VCSEL reported in the literature is a top emitting VCSEL and its properties are listed in table 1.2.

Refers to this information, the specific targets that the designed VCSELs needed to be achieved are listed in the last column of table 1.2.

Parameter	Pump Requirements	Previous Work	This Work
Wavelength	980± 5 nm [10]	GaAs quantum well designed for 850 nm	Design VCSEL using InGaAs/GaAsP MQW
Power	~30 mW for 500 μm long EDWA	~1.6 mW	Explore limits using multi-mode laser
Polarisation	Stable linear polarisation direction	14~20 dB	Target ~20 dB
Geometry	Dual top-side contacts	Epi-side emission	Substrate emission
Low-cost Approach	Minimise processing steps, and maximise yield	Single VCSELs modified using FIB	E-beam free approach Trenches formed using conventional optical lithography and etch

Table 1.2 Key developments of the VCSELs described in this thesis.

Considering these requirements, a VCSEL design of this project is presented in figure 1.26. Firstly, the VCSELs have a diameter of 10μm, 20μm, 30μm and 40μm. Since the maximum output power of lasers is proportional to the active region volume, the designed VCSEL devices have a large diameter. However, it is unsure whether the trench method for polarisation pinning is valid for the large diameter devices or not. A set of devices with diameter varies from 10 μm to 40 μm are designed. In terms of trenches, the depth of them is 9 μm. The etched trench feature in this project is also used as a n contact. Thus, the depth of it equals to the total thickness of epitaxy layers. The etched trenches have a width of 30 μm, As a contact, it requires a width larger than the diameter of probes that has a diameter of 20 μm or 50 μm. Therefore, the trenches designed here have a width of 30 μm and depth of 9 μm.

The designed VCSEL is illustrated in figure 1.26. A pillar patterned at the centre defines the diameter of the VCSEL and the injected current area. The p-contact is deposited on top of the pillar, and the n-contact is deposited at the bottom of 30 μm wide trenches as shown in the A-A cross-section. The metal contacts link to the bond pads deposited on top of the surface which is demonstrated in the B-B cross-section diagram. A layer of Si_3N_4 is deposited to provide electrical insulation between the bond pads and the semiconductor material. This structure forces the light emits from the substrate and separates the metal contacts from the light output facet. Two 9 μm deep trenches are designed to deliver anisotropic factors to pin the polarisation direction of emission.

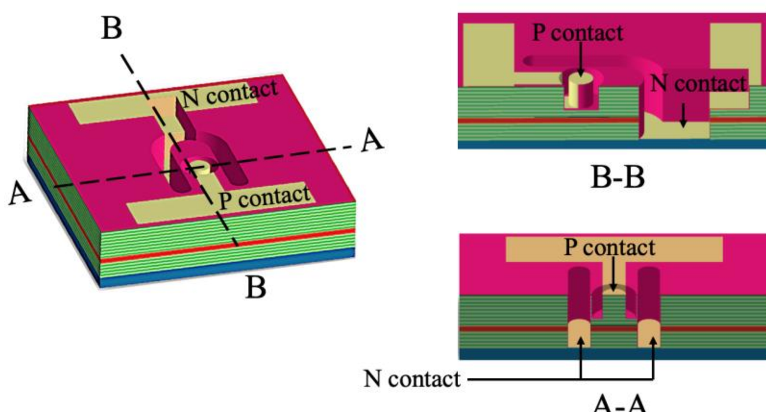


Figure 1.26 A schematic of the designed VCSEL with a pillar patterned in the center and the trenches etched next to it. The A-A and B-B cross-section diagrams present the inside features of the device with p-and n-contacts labelled.

This project will present the characteristics of this substrate emitting trench-etched VCSELs. The work includes fabrication, characterisation and investigation for the designed trench-etched devices. This work aims to give insights on developing polarisation stable substrate emitting VCSEL pump source.

1.6 Thesis Outline

This section outlines the organization of this thesis by introducing the content of each chapter.

Chapter 2 presents a flow of fabrication process to realise trench-etched VCSEL. It describes the techniques and equipment employed in this fabrication process. The measurement results of the VCSEL wafer is also illustrated in this chapter.

Chapter 3 illustrates the characteristics of the fabricated VCSELs including the voltage-current measurement results and light intensity-current measurement results, series resistance, threshold current, wall-plug efficiency and slope efficiency. These parameters are related to the capability of a light source to generate power.

Chapter 4 demonstrates the polarisation characteristics of the trench-etched VCSELs. It presents the polarised light intensity-current curves and the polarised subthreshold nearfield images of different diameter VCSELs.

Chapter 5 provides an investigation on the polarisation performance of the trench-etched VCSELs. It compares the spectra and nearfield images between orthogonal polarisation states and proposes an explanation of these results.

Chapter 6 describes some issues that happened in the fabrication process and gives the solution corresponded. It also presents some modifications to simplify the fabrication process in order to reduce the time and effort cost of this fabrication process.

Chapter 7 summarizes the work completed within this PhD and proposes new structures of trench-etched VCSELs. A future work plan is given in this chapter to gives insights on studying polarisation stable VCSEL for SPIC system.

Chapter 2

Initial Fabrication Process

This chapter focuses on the micro-fabrication process associated with the trench-etched substrate emitting VCSELs. It begins with an introduction of the GaAs VCSEL wafer then it presents an overview of the fabrication process. The major parts of this chapter describe the initial fabrication process supported by diagrams and optical microscope images.

2.1 VCSEL Wafer

The wafer used to fabricate the VCSELs is grown by the metal organic chemical vapour deposition (MOCVD) and provided by IQE. This VCSEL wafer comprises several epilayers constructed top DBRs, bottom DBRs and quantum wells. Figure 2.1 shows a schematic of the epilayers of the wafer. The active region contains three 60 Å thick $In_{0.17}Ga_{0.83}As$ quantum well layers separated by 40 Å thick $GaAs_{0.92}P_{0.08}$ barriers placed at the antinode of the cavity. Such active region designed to achieve 980 nm emission. Below and above the active region, 28 n-doped DBRs and 30 p-doped DBRs are constructed. Each period of the DBR consists of $Al_{0.9}Ga_{0.1}As$-$Al_{0.12}Ga_{0.88}As$ layers with compositional grading between them. These DBRs, use as top and bottom mirrors. Light generated in the active region is engineered to emit from the bottom of the structure. The substrate is a 630 μm thick n-doped GaAs substrate.

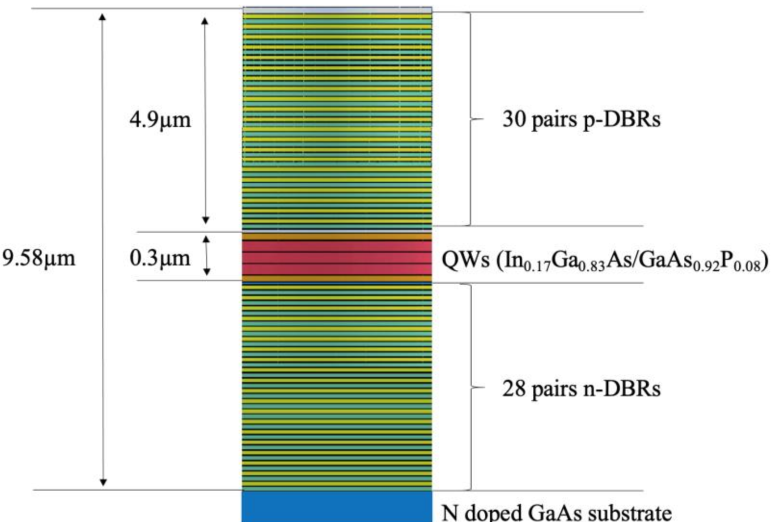


Figure 2.1 A schematic of the epilayers of VCSEL wafer grown on a n doped GaAs substrate. It comprises 30 pairs of p-doped DBRs, 28 pairs of n-doped DBRs and 3 quantum wells.

This VCSEL wafer has two critical factors that are pertinent to the performance of fabricated devices. First, the direction of different crystal axes. When a wafer is separated from a boule of GaAs material, two edges called major and minor flats have been cleaved to identify the $[01\bar{1}]$ and $[0\bar{1}\bar{1}]$ orientations of the crystal axes shown in Figure 2.2. These crystal axes are always selected as references to describe the polarization direction of the emission. The second critical factor is the thickness of each epilayer. During the etching process, the thickness of the layers are used to estimate the etching time. To achieve a precise etching depth, the thickness shall be known beforehand.

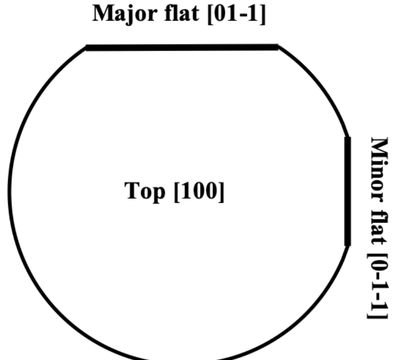


Figure 2.2 A schematic of European and Japanese standard substrate with two edges labelled as major and minor flat.

2.2 Wafer Inspection

For this wafer, it is difficult to recognise on which side has epilayers. Both sides of the wafer have been polished due to the substrate emitting request. Thus, the facet with epilayers cannot identified by the roughness of the surface. The solution applied here is to measure the photoluminescence (PL) for both side of the wafer. Since the composition of the top layer of each side is different, such PL spectrum shall help to identify the top side of the wafer.

Measurements were carried out by equipment Bruker vertex 70 Fourier transform infrared spectroscopy (FTIR) system that provides a helium-neon laser as a light source under room temperature with an InGaAs detector. **Error! Reference source not found.** illustrates the p hotoluminescence spectrum measured at one side of the wafer. A peak has been detected at 793nm, which corresponds the wavelength of material $Al_{0.12}Ga_{0.88}As$. This material is the smallest band-gap material in the p-DBR stack. Thus, the emission measured from PL is expected to be generated from it. There is a thin (40 nm) p-GaAs contact layer grown on top of $Al_{0.12}Ga_{0.88}As$ layers. Due to its thickness and non-radiative recombination issue, the emission of it does not appear on PL.

Figure 2.4 shows the photoluminescence spectrum of the n-doped GaAs substrate. This spectrum comprises two peaks. The narrow peak has a centre at λ=876 nm and the broad peak has a centre at λ=1276 nm. The results suggest that the narrow peak represents epilayer of $Al_{0.12}Ga_{0.38}As$ while the broad peak is attributed to mid-gap defect states in the n-doped GaAs substrate. According to PL measurement results, both sides of the wafer are identified. Next section presents the fabrication process of trench-etched VCSEL.

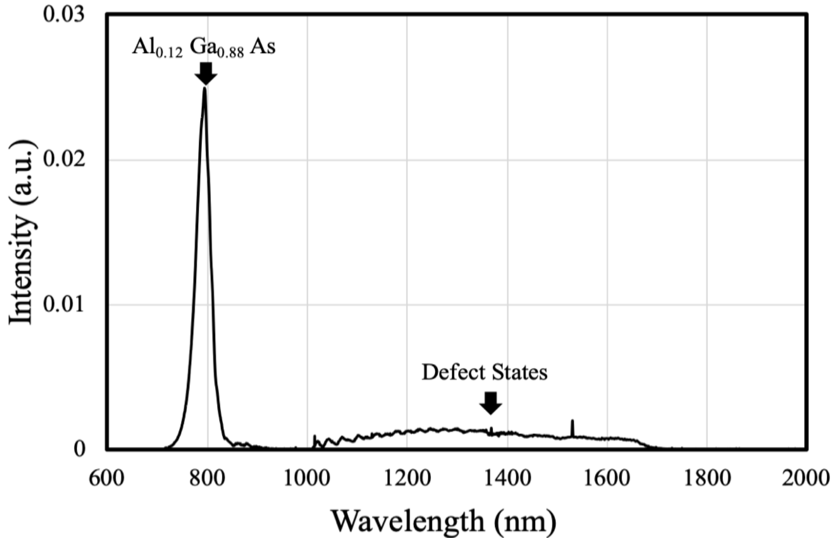


Figure 2.3 The photoluminescence spectrum measured from the side of the VCSEL wafer having epilayers deposited on it.

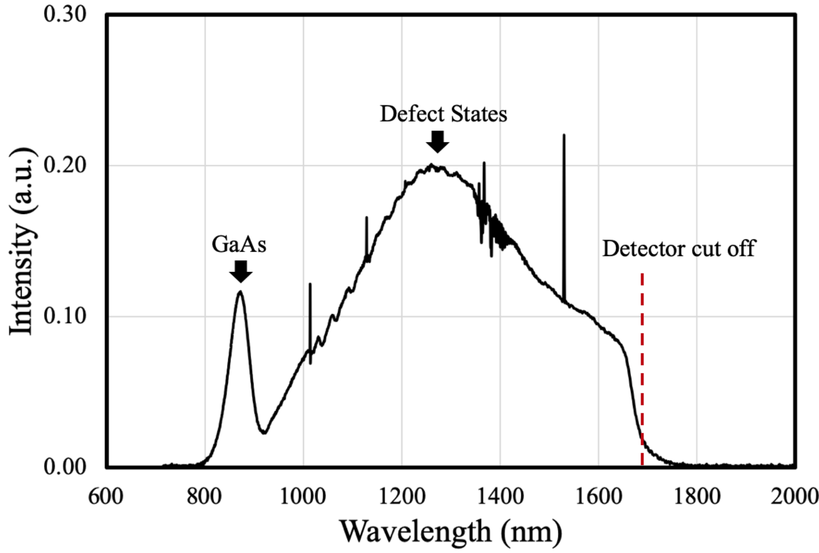


Figure 2.4 The photoluminescence spectrum of the substrate of the VCSEL wafer.

2.3 Overview of the Fabrication Process

The fabrication process is divided into four modules: mesa etch module, trench etch module, insulation module and metal deposition module. Etch modules construct the features of the VCSEL. The other two modules are used to form the metal contacts. Figure 2.5 schematically shows the fabrication process with the A-A cross-section diagrams of the devices:

- Construction of the VCSEL structure: Dry-etching of a pillar (2) and two trenches (3)

- Electrical Insulation: Deposit a layer of dielectric and then open the windows for the contacts (4)
- Contacts deposition: Deposit the p-contact (5), n-contact (6) and the bond pads

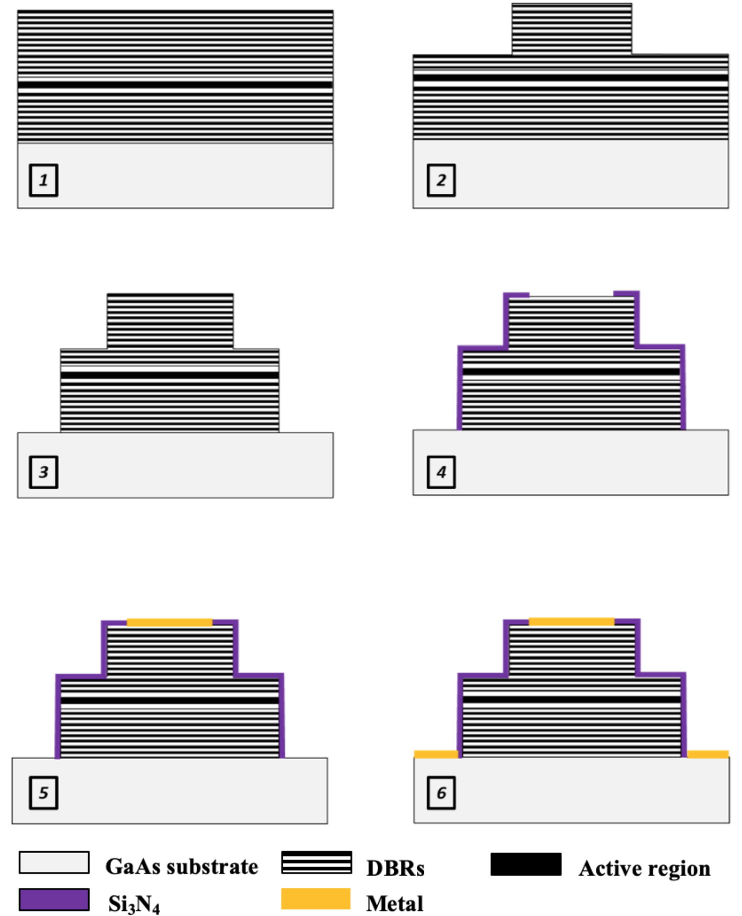


Figure 2.5 Sequential schematics of the cross-section of the devices illustrating the fabrication flow.

2.4 Mesa Etch Module

The aim of the mesa etch module is to define a circular mesa as a current injection area for the VCSEL. This module consists of wafer cleaning, hard mask deposition, optical lithography, and dry etching steps. The following presents the details of each step in the sequence of fabrication process.

Clean:

First of all, samples are cleaned to reduce surface contamination. The contamination could be dust, organic stains, etc. The process is carried out with three solutions: Acetone, IPA (Isopropanol), R.O. (reverse osmosis) water. Figure 2.6 shows a schematic of the standard solvent cleaning process. First, sample is immersed in an acetone solution to rinse away dust

and grease. Then, it transferred into an IPA solution that has low volatility to clean any residue. Finally, sample is rinsed and dried by R.O. water and nitrogen gun respectively. After the surface condition of the sample has been confirmed under optical microscope vision, the sample is ready for the next step. This process can be repeated several times to achieve the required level of cleanliness.

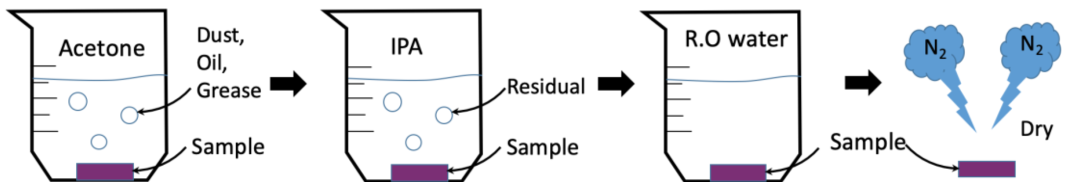


Figure 2.6 A schematic of the standard solvent cleaning process for the semiconductor sample with solutions of acetone, IPA and R.O. water, finished by nitrogen gas drying.

Hard mask deposition:

A thin layer of SiO_2 is used as a hard mask layer in this fabrication process. This layer protects underlying epilayer material during deep etching process. In this case, etch depth are 4 µm and 9 µm respectively. Thus, a hard mask is employed during the etching process.

Figure 2.7 is a schematic of the cross section of the VCSEL sample with a 400 nm SiO_2. In this process, the SiO_2 layer is deposited by an Oxford Instruments PECVD 80+ (plasma enhanced chemical vapour deposition) which dissociates the reactants ($SH_4/N_2O/N_2$) and delivers a uniform deposition by injecting the gases evenly through a showerhead inlet [63].

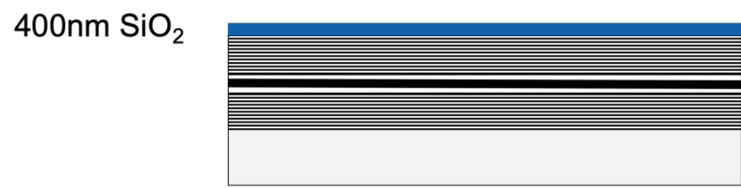


Figure 2.7 A schematic of the cross-section of the sample with a hard mask deposited on top of it.

Optical lithography:

Optical lithography is used to transfer a pattern from a mask to the sample by taking advantage of a light sensitive material called photoresist. This process has been widely employed in the micro-fabrication [64]. The mask contains dark and transparent regions. The dark area is coated with chrome to prevent the ultraviolet (UV) light from exposing the photoresist, while the transparent region defines the area to be patterned. Figure 2.8 schematically presents a procedure of optical lithography. It includes spinning, exposure and

development steps. At the spinning step, the surface of the sample been coated with the photoresist. Then, a mask aligner (Suss MA6, with 1μm accuracy [65]) is used to align the sample with the designed mask, and then expose the un-masked photoresist area on the sample under the UV light.

Turns to developing step, the results are different in terms of different photoresist. In general, there are two kinds of photoresist: positive photoresist and negative photoresist. The positive photoresist can be dissolved in developer after it is exposed, forming a pattern the same as the opaque region of the mask. Negative photoresist, becomes cross-linked after exposure and, the pattern formed by it is the same as the transparent region of the mask upon development. Figure 2.9 illustrates the developing results of employing positive and negative photoresist. In this fabrication process, a positive photoresist called S1818 that has a thickness of 1.8 μm via spinning at a speed of 4000 rpm was selected.

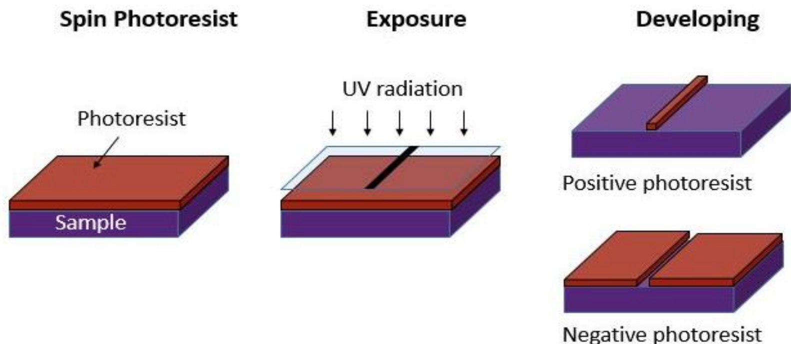
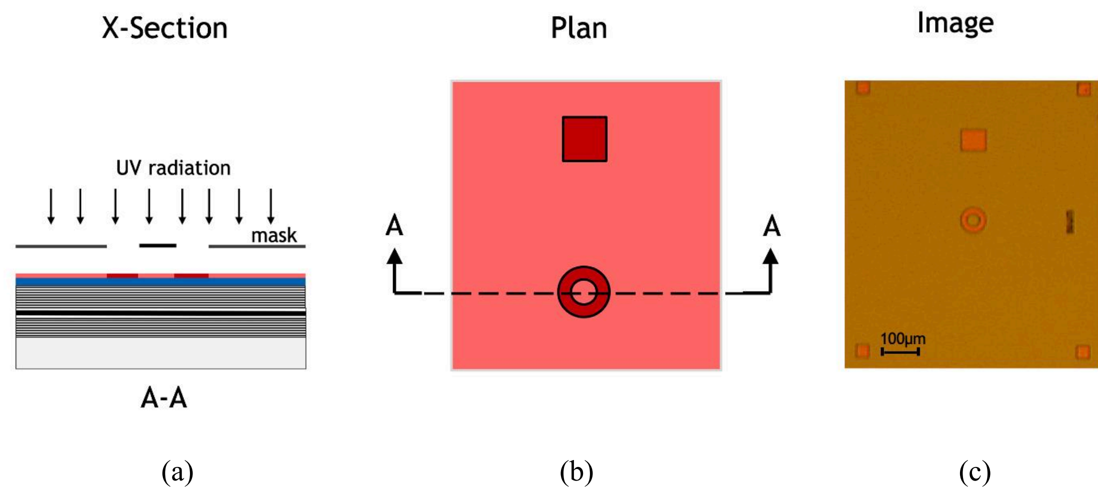


Figure 2.8 A standard procedure of optical lithography, including spinning, exposure and developing photoresist. Two kinds of patterns are formed by employing positive and negative photoresist through the same mask.

Figure 2.9 shows schematic diagrams and an optical image of the sample at this step. The A-A cross-section diagram shown in figure 2.9(a) illustrates a sample coated with S1818 photoresist and placed under the UV light with the cover of a mask. The plan view, figure 2.9(b) shows the exposed area of the sample: the circular mesa and a square. The mesa is engineered to define a current injection area, while a square pattern is used as a stair for achieving a continuous n-contact that will be introduced in the next module. The microscope image, figure 2.9(c) is the real shape of the device at this step.



(a) (b) (c)

Figure 2.9 Diagrams and a microscope image taken under yellow light of the sample at optical lithography step of mesa pattern.

Error! Reference source not found. shows images of 40 µm, 30 µm, 20 µm and 10 µm m esa, from left to right. As an overview picture, it presents a structure changing direction of this set of fabricated devices.

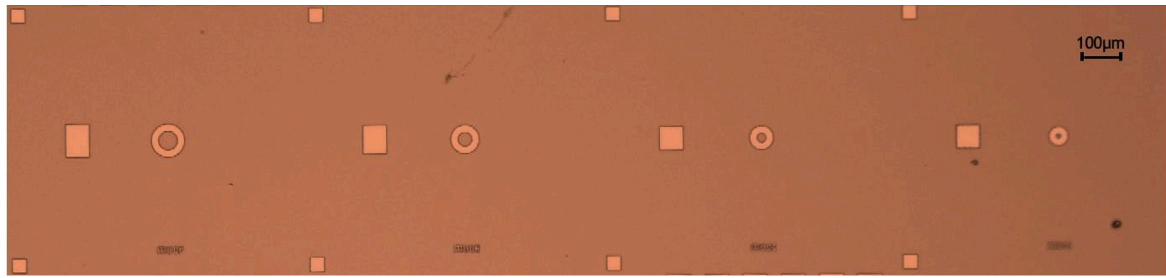


Figure 2.10 A microscope image of a 40 µm, 30 µm 20 µm 10 µm diameter mesa after developing the sample.

The optical lithography process is summarized below:

1. Pre-bake the sample in 120 ^{o}C oven for 5 mins
2. Spin S1818 photoresist at a speed of 4000 rpm
3. Bake the sample on a hot plate at 115 ^{o}C for 90 s
4. Expose the sample for 10 s
5. Develop the sample in MIF319 for 105 s

Dry etching:

The etching process happens after a lithography step. Dry etching is used in this case. It also called plasma etching, is carried out in a sealed reactor where the reactants are dissociated by RF power. The movement direction of ions is controlled by the applied voltage. Thus,

dry etch has high anisotropic etching property. In addition, the etching rate of it can be tailored to suit specific etching demand by adjusting applied power, pressure, gas flow rate and other parameters.

An interferometer was used to inspect the in-situ etch rate. From the interferometer, a laser spots on the sample surface and then reflects back with an offset to the reference light. The intensity of the interferometer signal varies periodically with time [66]. Figure 2.11 presents a graph analogous to interferometer signal measurement result. Defined 'T' is the period of the signal. λ is laser beam wavelength, n is refractive index of etching material. The etching rate can be calculated by equation 2.1.

$$Etch\ rate = \frac{\lambda}{2} \cdot \frac{1}{n} \cdot \frac{1}{T} \tag{2.1}$$

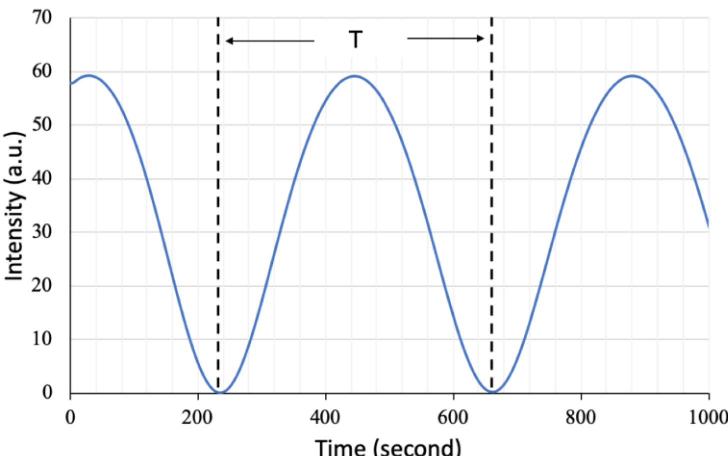


Figure 2.11 A graph analogous to the interferometer measurement result. The detected signal has a period of T (s).

The etching rate links to the period 'T' and the wavelength of the laser beam. In our case, a 632.8nm He-Ne laser is used in the interferometer. To calculate the etching rate, the etching depth has to be larger than λ/2n, here is (318.4/n).

1st Etching step (hard mask etch):

Turn to the etching equipment, Oxford reactive ion etching (RIE80+) was employed to etch the SiO_2 hard mask [67]. The etch recipe is presented in table 2.1. To etch SiO_2, gaseous CHF_3 is selected to generate the reactants, while gas O_2 is supplied to mitigate the plasma density. The RF power is related to ions dissociation 55 mT pressure is linked to the concentration of the reactants in the chamber.

Parameter	Value
Gas flow: CHF_3/O_2	50/5 sccm
RF Power	150 W
Pressure	55 mT
Temperature	20 °C
Etching rate for SiO_2	32 nm/min

Table 2.1 RIE process parameters for etching SiO_2

Figure 2.12 presents the interferometer signal measured during the etching. This signal has a period equal to 410 s. Using Equation 2.1, the etching rate of this step is 32 nm per min and the total etching thickness 400 nm.

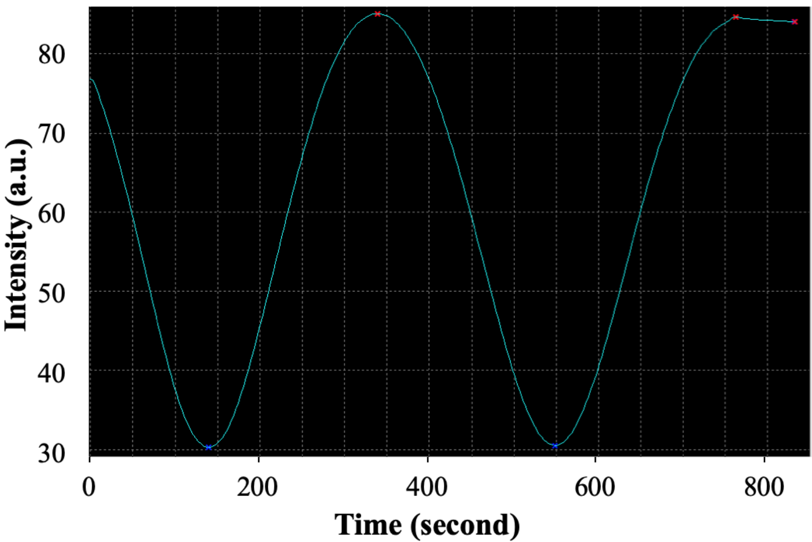


Figure 2.12 The interferometer signal measured during etching which has a period 'T' of 410 s.

Error! Reference source not found. shows the cross-sectional, and plan-view diagrams a nd a microscope image of the sample after etching. As the cross-section and the plane view diagram of the sample shows, the hard mask was etched through and the pattern was replicated into this layer. The microscope image at the left confirms that the pattern in the hard mask layer has clear edges.

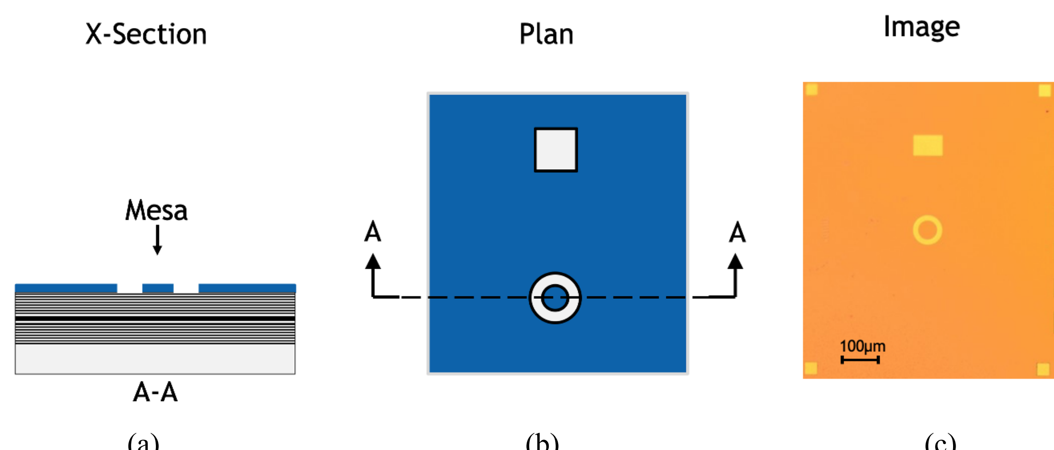


Figure 2.13 Diagrams and an optical microscope image of the sample with etched hard mask after removed the photoresist on top of it.

2nd Etching step (Semiconductor etch):

An inductively coupled plasma (ICP) etch (Oxford Instruments PlasmaPro System 180) is used to etch the semiconductor epitaxial structure through the hard mask [68]. This tool has 2 RF power suppliers. One of those provides the energy to dissociate the reactants and the other one controls the speed of ions of loading on the substrate. Since the ion density and the ion energy are controlled separately, ICP 180 can provide intensive ions in a low-pressure condition. It contributes to a rapid etching rate. Due to the deep etching depth, ICP180 is selected at this step.

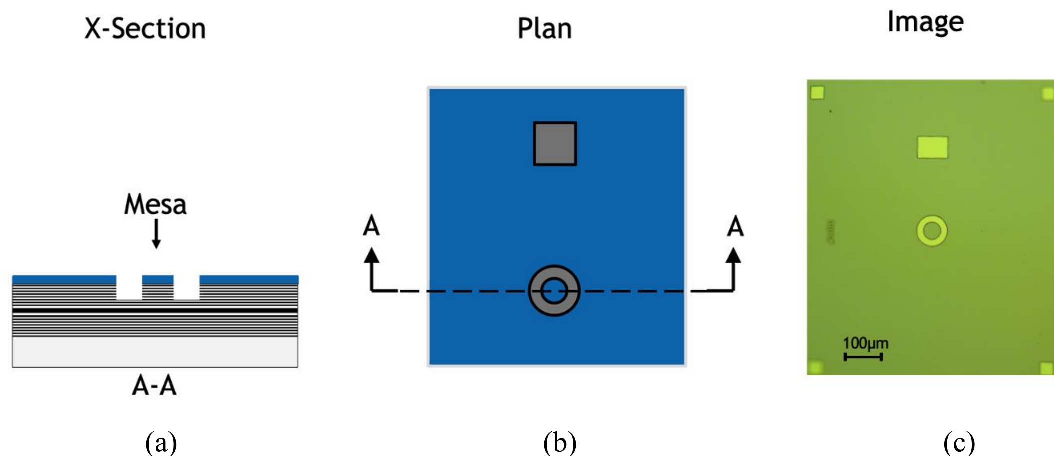
The recipe of the ICP etch process are illustrated in table 2.2. Gaseous $SiCl_4$ supplies the reactive ions, while gas Ar_2 is used to moderate the etching rate for achieving a high anisotropic etching result [69].

Parameter	Value
Gas flow : $SiCl_4$ /Ar_2	7.5/15 sccm
RF Power of ICP/Platen	350/60 W
Pressure	2.5 mT
Temperature	20 ^{o}C
Etching rate for GaAs/AlGaAs	About 600 nm/min

Table 2.2 ICP180 process parameters for etching GaAs/AlGaAs

Three batches of samples have been fabricated with different mesa depth by varying the etching time at this step. They have the mesa height of 4 μm, 4.5 μm and 5.2 μm corresponding to etching through 25 pairs p-doped DBRs, 28 pairs of p-doped DBRs and

through the entire p-doped DBR and the active region, respectively. Figure 2.14 shows a cross-section and plan view diagrams and a microscope image of the sample. The shape of the pattern for the sample is as shown in figure 2.14(b). A representative cross-sectional image of the sample is presented in figure 2.14(a), illustrating the etched sample with a thin layer of hard mask left on top of it.



(a) (b) (c)

Figure 2.14 Diagrams and a microscope image of the sample at the step of etching epilayers.

3rd Etching step:

The final step of this module is to remove the hard mask. The reactor is reactive ion etching tool (RIE 80+) , and the recipe for this step is shown in table 2.1. An interferometer was employed during this step and it indicates the etching thickness is 200 nm (shown in figure 2.15). The thickness reduction of the hard mask is considered as a mask erosion.

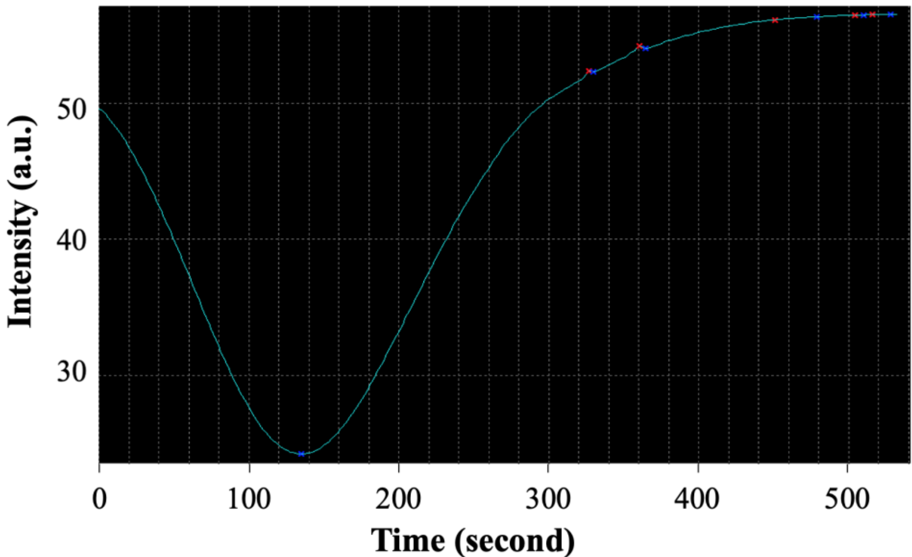
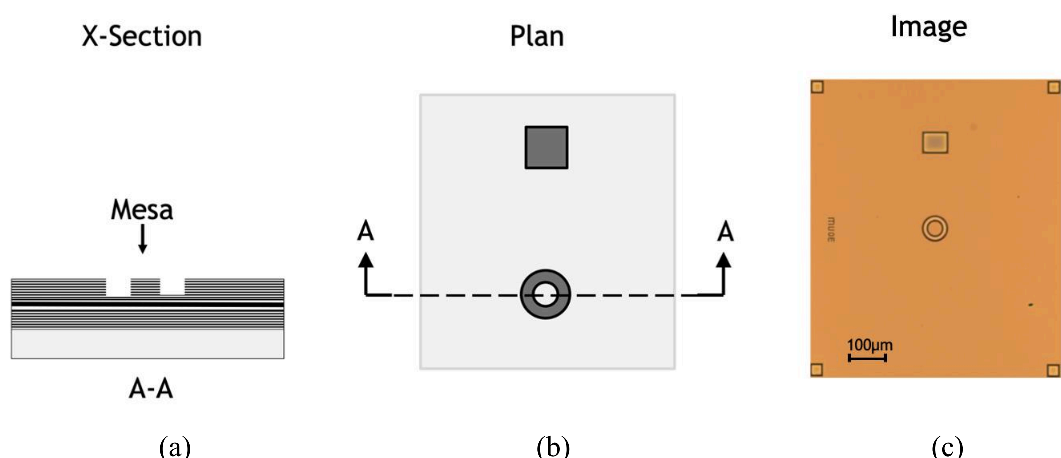


Figure 2.15 The interferometer signal measured at hard mask removal step. The etching process takes about 350 s.

Error! Reference source not found. illustrates the diagrams and a microscope image of the s ample with a mesa patterned into it with the hard mask removed. It implies that a target pattern has been transferred into the sample material.



(a) (b) (c)

Figure 2.16 Diagrams and a microscope image of the sample after hard mask removed

2.5 Trench Etch Module

After the mesa is fabricated, a pair of deep trenches are etched next to it. The trenches have been designed to pin the polarization direction [70]. The depth and width of the trenches are consistent for VCSELs of different diameter. The following introduces the fabrication process used to etch trenches.

2.5.1 Hard Mask Deposition:

A 900 nm-thick SiO_2 hard mask layer is used. Figure 2.17 shows a diagram of the cross-section of a sample with a 900 nm thick SiO_2 deposited on top of it. Such layer is grown by Oxford Instruments PECVD (plasma enhanced chemical vapour deposition).

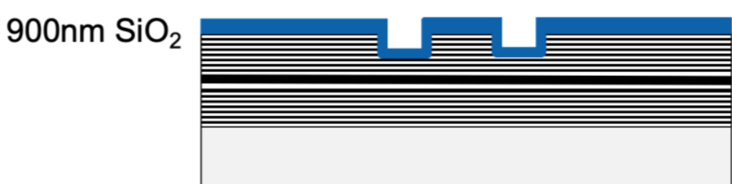
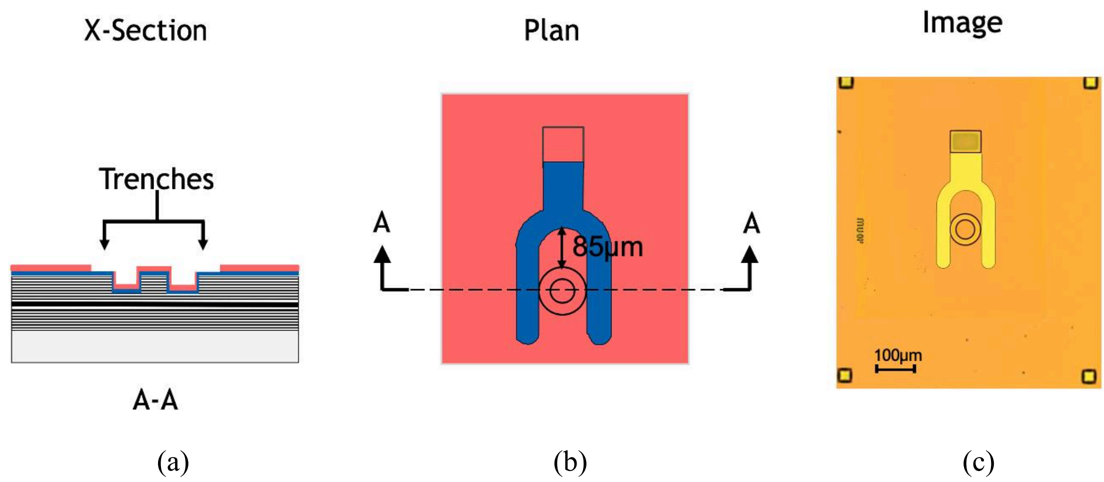


Figure 2.17 A schematic of the cross-section of the sample with 900 nm thick hard mask deposited on top of it.

At this step, a y-shaped pattern is transferred from a chrome mask into the photoresist (S1818) layer. Figure 2.18 shows the diagrams and an optical microscope image of the sample patterned with a y shaped feature. As figure 2.18 shows, the united point of the two trenches is far away (85 μm) from the mesa and connects with the square pattern, which was discussed in the previous module. These trenches are patterned parallel to the $[01\bar{1}]$ crystal axis.



(a) (b) (c)

Figure 2.18 Diagrams and an optical microscope image of the sample with a y shape feature patterned into photoresist layer.

Figure 2.19 shows an optical microscope image that incorporates 40 μm, 30 μm, 20 μm and 10 μm diameter VCSELs. As it shows, the width of trenches is identical for different sizes of VCSELs and the distance from the trench to the edge of the mesa is maintained at 15 μm.

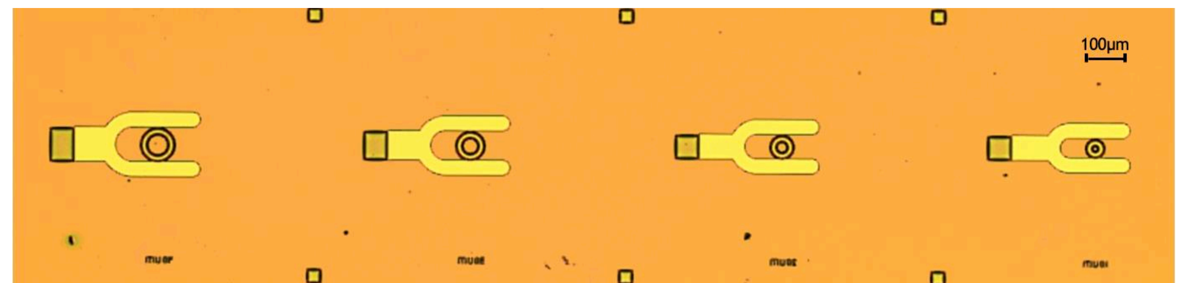


Figure 2.19 An optical microscope image includes 40 µm, 30 µm 20 µm 10 µm diameter VCSELs with trench patterned next to them.

The step sequence of the optical lithography process is summarized below:

1. Pre-bake the sample in 120 °C oven for 5 mins
2. Spin S1818 photoresist at a speed of 4000 rpm
3. Bake the sample on a hot plate at 115 °C for 90 s
4. Expose the sample for 10 s
5. Develop the sample in MIF319 for 105 s

2.5.2 Dry Etching

Resemble to first etch module, here utilizes Oxford RIE 80+ and ICP180 equipment. This etching process is comprised of three steps: hard mask etch, semiconductor etch and hard mask removal.

1st Etching step (Hard mask etch):

At first step, hard mask layer is etched by Oxford RIE 80+. Figure 2.20 presents the interferometer signal measured during the SiO_2 etching. This signal has a time period equal to 450 s. By using Equation 2.1, the etching rate of this step is 30 nm per min.

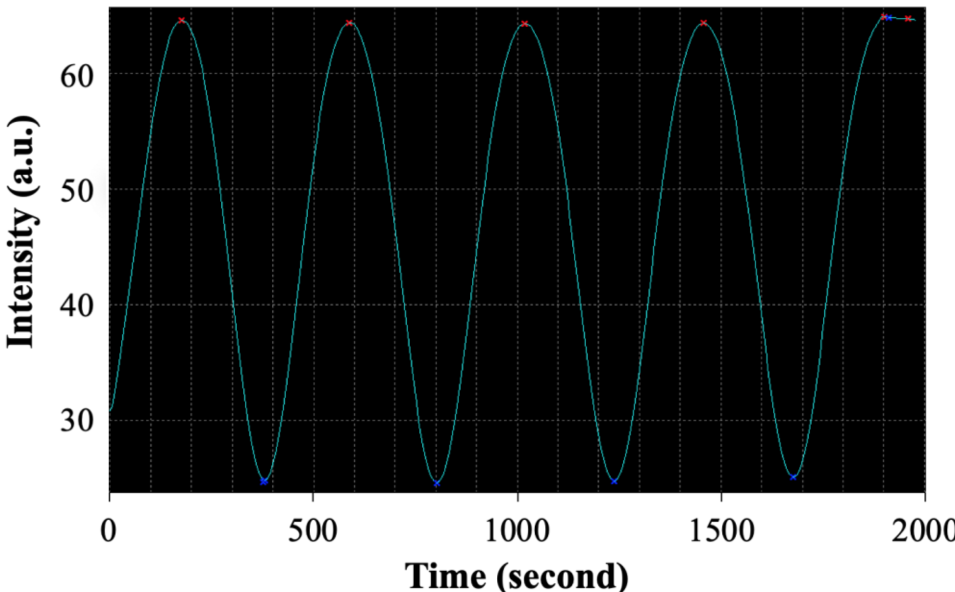
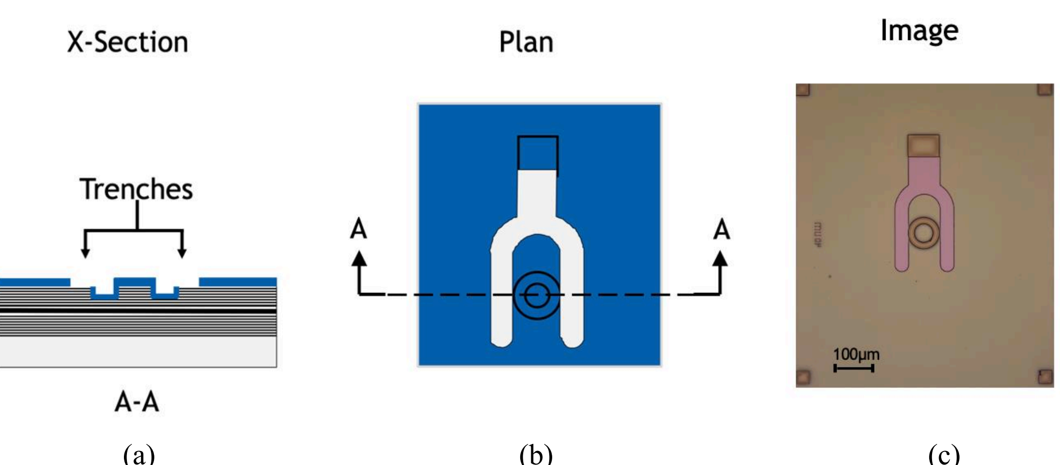


Figure 2.20 The detected interferometer signal measured during RIE etching process. It shows a period of 450 s.

Figure 2.21 illustrates a cross section, a plane view and an optical microscope image of the sample after the trenches etched into the hard mask layer. As figure 2.21(a) shows, the trenches are next to the boundary of the mesa. The microscope image in figure 2.21 illustrates the pattern at this step with the photoresist mask removed.



(a) (b) (c)

Figure 2.21 Diagrams and a microscope image of the sample after a y shape pattern transferred into the hard mask.

2nd Etching step (Semiconductor etch):

An investigation of the etching sidewall was carried out with a GaAs sample by using the recipe in table 2.2. Figure 2.22 shows an SEM image of the post-etch sidewall on a test

sample. As it shows, etching depth is down to 9 μm and the angle of the sidewall is about 89°. It indicates that a steep sidewall is achieved by applying this etching recipe.

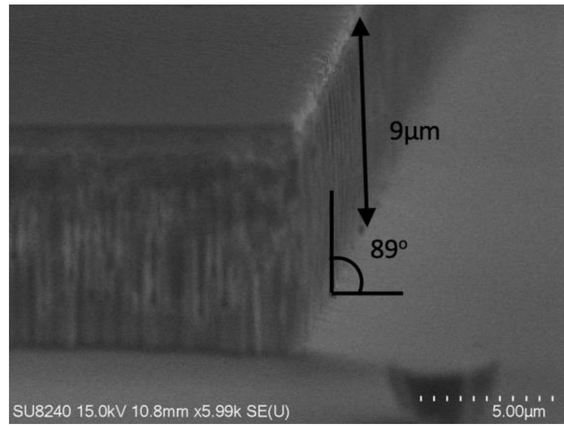
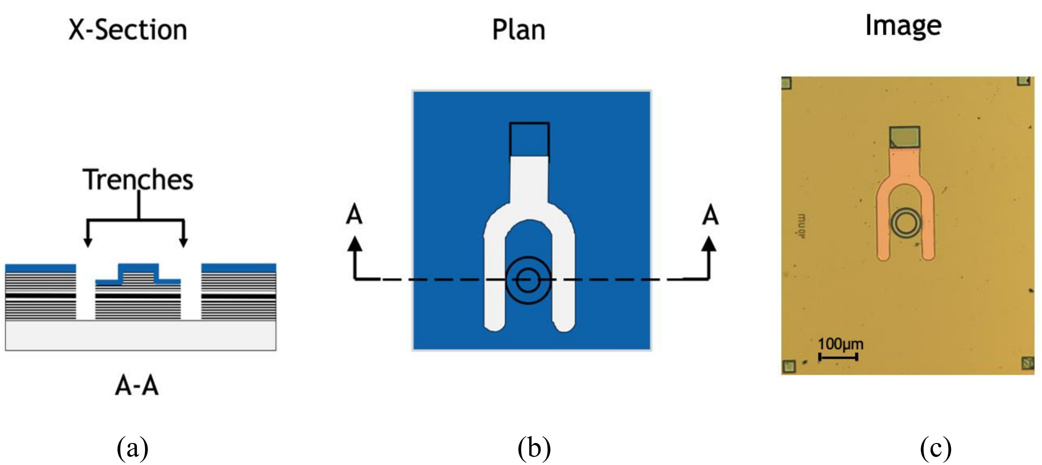


Figure 2.22 A SEM image of the sidewall of a test GaAs sample etched by ICP 180.

Figure 2.23 schematically depicts the feature of the sample after the y shape pattern has been replicated into the material. The etching is down to the substrate of the VCSEL wafer shown in figure 2.23(a). As we can see from the image figure 2.23(c), there were some small dark points left on the hard mask. It is possible that some etch reactants have attached to the surface due to the high-pressure environment within the etch chamber.



(a) (b) (c)

Figure 2.23 Diagrams and a microscope image of the sample at the step of etching y shape trenches.

3rd Etching step:

The hard mask removal step was inspected by the interferometer and the measurement result is presented in figure 2.24. The signal has a period of 400 s that indicates the etching rate is 33 nm per min. As the etching terminated at 600 s, the etch thickness at this step is about

330 nm. Therefore, 570 nm SiO_2 was consumed during the GaAs etching step, which implies that the etching selectivity of SiO_2 to GaAs is 1:16.

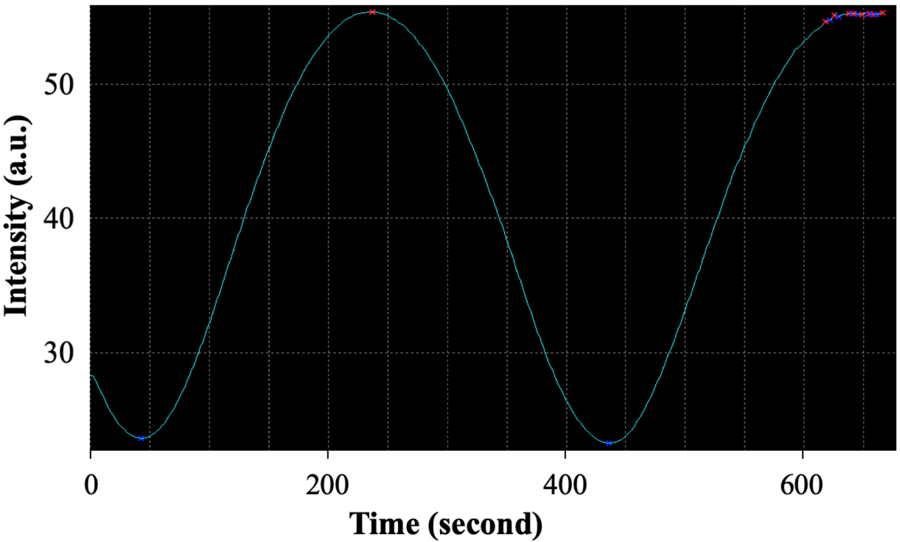
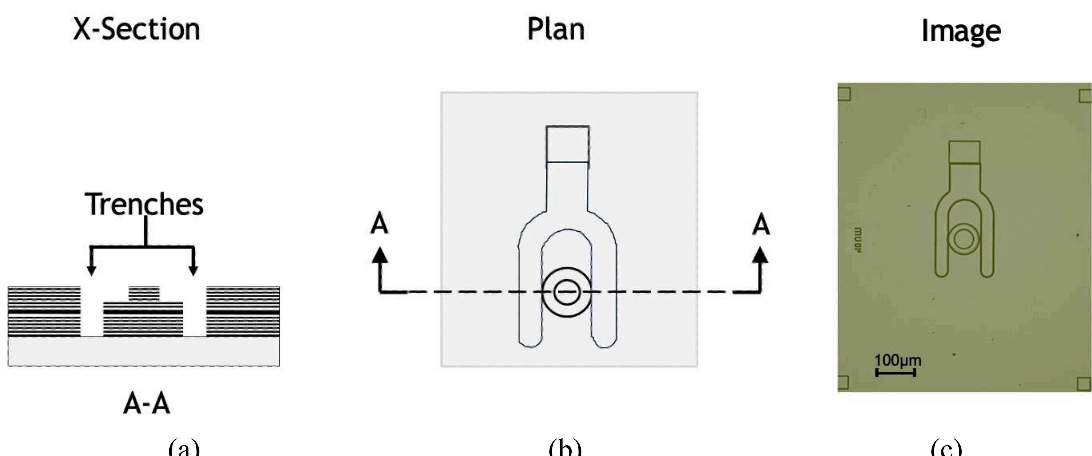


Figure 2.24 The interferometer signal measured during RIE etching process. It shows a period of 400 s.

Diagrams and an image of the sample at this step shown in figure 2.25. The major structure of the trench patterned VCSEL are etched into the sample by this step. The image of the sample shows that the pattern transferred into the sample precisely.



(a) (b) (c)

Figure 2.25 Diagrams and a microscope image of the sample with hard mask removed.

A plan view and a B-B cross-section of the sample are presented in figure 2.26. In this module, a stair was constructed. This stair breaks the steep sidewall at the end of the y trench by creating a platform in the middle. This is used to circumvent the possibility of a metal contact discontinuous at a sharp sidewall.

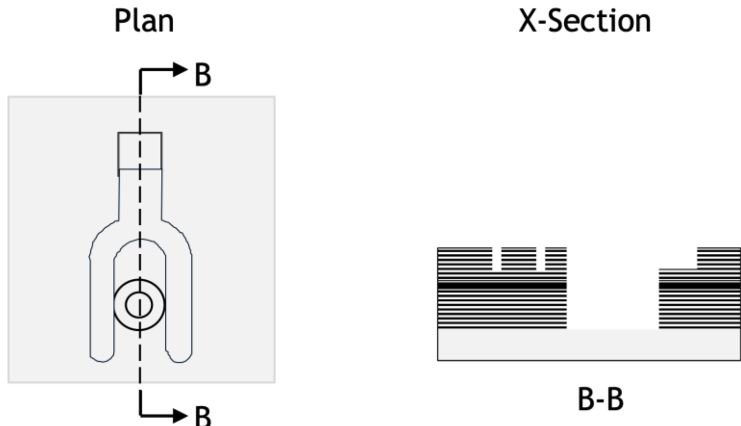


Figure 2.26 Diagrams of a plan view and a cross-section at B-B of the sample at this step. A stair structure is formed at the end of the y shape.

2.6 Insulation Module

This module consists of two steps: dielectric (Si_3N_4) deposition, and contact window open. The equipment involved in this module are Oxford PECVD and Oxford RIE 80+, which are employed for deposition and etching.

2.6.1 Dielectric Deposition:

A 600nm thick Si_3N_4 layer is grown on the surface of the sample. It provides insulation between the metal bond pads (which are added in subsequent fabrication steps) and the semiconductor material. The reacting gases are SiH_4, NH_3 and N_2, that are dissociated by 21 W platen power to form Si_3N_4. In order to achieve a uniform layer, the pressure is set to 1000 mT to reduce the particle density in the chamber.

Parameter	Value
Gas flow : $SiH_4/NH_3/N_2$	10/16/200 sccm
Platen Power	21 W
Pressure	1000 mT

Table 2.3 PECVD 80+ parameters for depositing Si_3N_4

Figure2.27 schematically depicts the cross-section of the sample covered with 600 nm thick Si_3N_4. The colour of a 600 nm Si_3N_4 is purple due to its refractive index (n= 1.9) and its thickness. This dielectric layer distributes evenly on the surface and sidewalls of the sample.

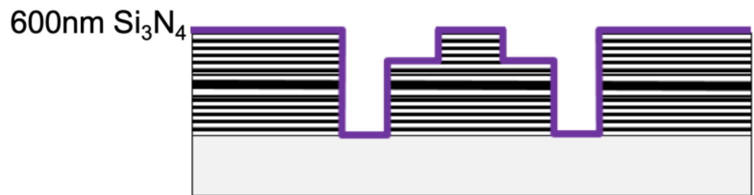


Figure 2.27 A schematic of the cross-section of the sample covered with 600 nm thick Si_3N_4 which is deposited by PECVD 80+ .

2.6.2 Opening P-contact and N-contact Windows:

The aim of this step is to etch the dielectric material where the n-contact and p-contact of the VCSELs are going to be formed. Reactive ion etching tool is used to accomplish this etching step with the recipe provided in table 2.1. The reactive gases and setting parameters are the same as those used for etching SiO_2. However, the etch rate is different.

The interferometer signal detected during this etching process is presented in figure 2.28. It has a period of 120 s, which informs that the etching rate is 85 nm per minute. Such etching rate is two times faster than etching SiO_2.

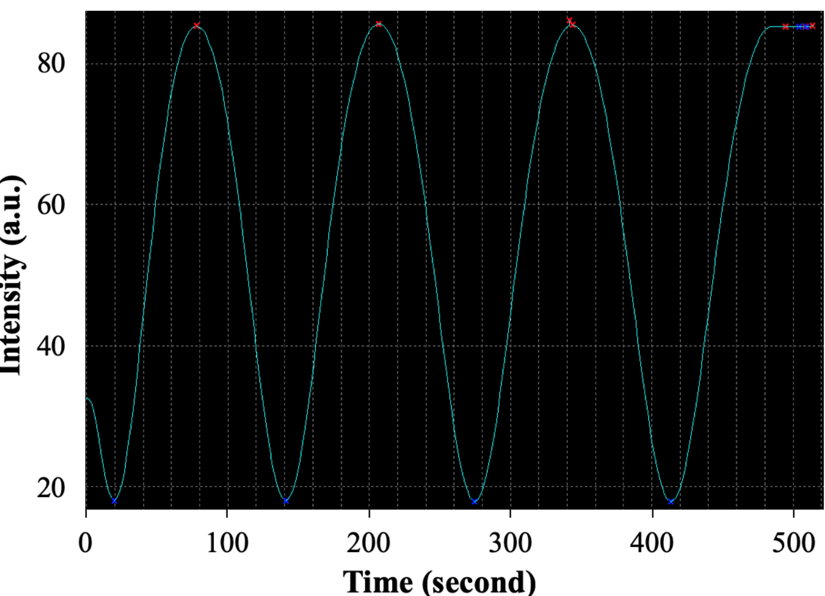


Figure 2.28 The interferometer signal measured during RIE etching process. It shows a period of 120 s.

Figure 2.29(a) shows that the Si_3N_4 material on the top of the mesa and at the bottom of the trench area was etched away by the cross-section diagram. The shape of the n-contact area demonstrated in a grey colour (shown in figure 2.29(b)). It has the same shape of trench by shrinking 2 µm. Such shrink ensures the sidewalls of the y trench remain covered with the dielectric after etching. It prevents a current leakage that may happen at the sidewall of the

devices. For the same reason, the diameter of the p contact window (a grey circle in the plan view) of 10 μm, 20 μm, 30 μm and 40 μm VCSELs are shrank to 8 μm, 16 μm, 26 μm and 34 μm, respectively. Sample after this step is presented in figure 2.29(c).

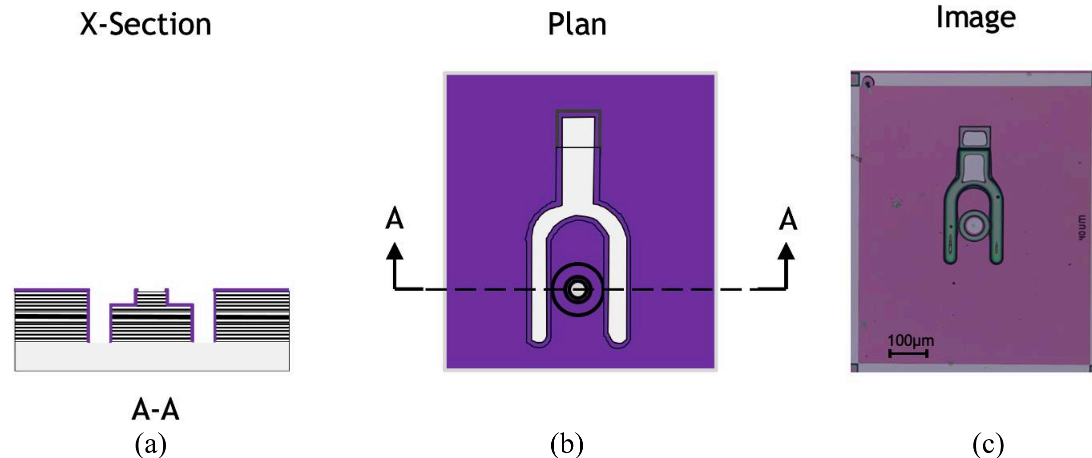


Figure 2.29 Diagrams and a microscope image of the sample with hard mask removed.

However, there are some dielectric residuals left in the trench area after this step. It shows on the microscope image in figure 2.29. This problem has been temporarily solved with a second etching by utilizing the n-contact mask. This mask has the same feature as the n contact window. Figure 2.30 illustrates two optical microscope images (a) and (b) that are the images of the sample before and after the residuals cleaned. As we shall see later in Chapter 6, a new design of the photolithography mask provides a solution to this issue.

Figure 2.30 Microscope images of the sample before (a) and after (b) the residuals cleaned in the trench area.

2.7 Metal Deposition Module

Metal contact is one of the essential components of an electrical pump laser, which offers an area where the current can inject uniformly. This module aims to construct the metal contacts for the devices. The metal evaporator utilized in this fabrication process is an electron-beam evaporator (Plassys MEB400S[71]), which deposits the metal on the substrate in a high vacuum environment. This electron-beam evaporator applies a beam of electrons to bombard the target metal and then causes the metal atoms to move directly to the substrate. Any

particles flowed in the travelling path of the atoms will lead to a block or a deflection. As the density of the particles reduces rapidly with the pressure of the atmosphere, the metal atoms would move to the target substrate with fewer barriers in a high-pressure environment. In terms of Plassys MEB400S, a vacuum environment can be achieved in a short time after loading the sample into it as the chamber is separated into a loading area and an evaporation area by a gate that maintains one section of the chamber in high pressure.

The metal contact deposition process in this module comprises three steps, which are photolithography, metal deposition and lift-off. Figure 2.31 presents the diagrams for each step. First, a pattern of the metal contact is transferred into the photoresist layers during the photolithography step. However, two different photoresists have been applied in this step called S1818 and LOR 5A. They can be developed separately to achieve an undercut at the edge of the pattern. The undercut is used to ease the solvent to penetrate into the photoresist layer during the lift-off process. Second, a layer of metal is deposited by Plassys MEB400S. A thickness difference between the metal layer and the LOR 5A layer attempts to lead to a discontinuous of the deposited metal. Finally, the sample is immersed into an Acetone solution that is used to dissolve the photoresist, and then the metal which distributes on top of photoresists is lift-off. A 50 ^{o}C water bath is usually applied to speed up the lift-off process. In the end, the metal contact with a specific shape is constructed on the surface of the sample.

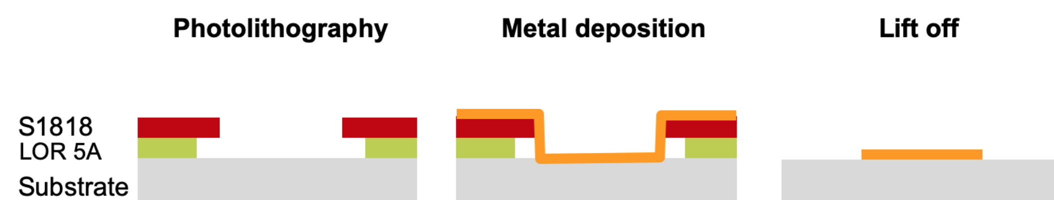
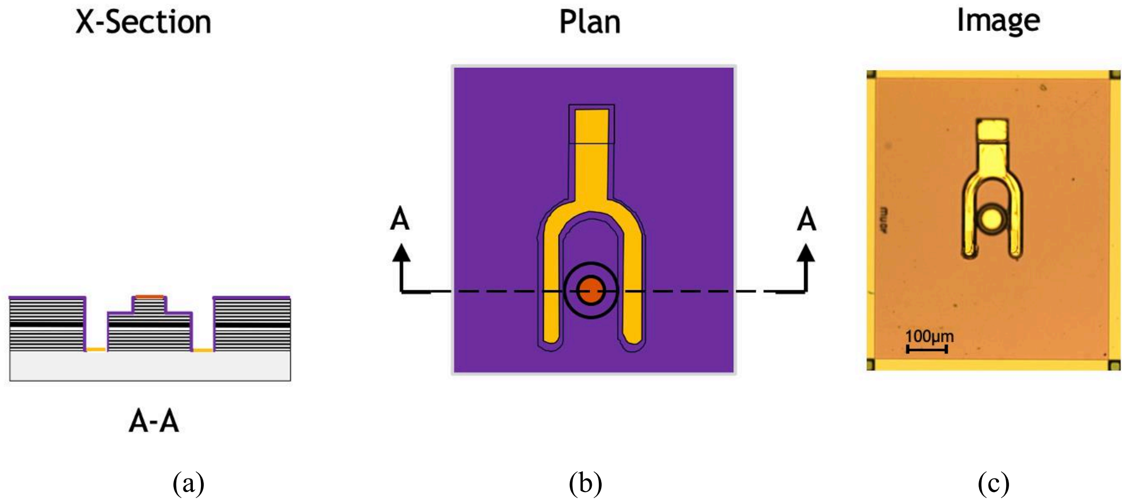


Figure 2.31 The metal contact deposition procedures including photolithography, metal deposition and lift-off steps. The photoresists applied in photolithography step are S1818 and LOR 5A which are developed separately by different developers.

2.7.1 P-and N-contact Deposition:

Figure 2.32 presents the cross-section, plan view diagrams and an optical microscope image of the sample with p- and n- contact constructed on it. P-contact has a circular shape demonstrated in red, while the n-contact has a y shape demonstrated in yellow view. As it shows in the A-A cross-section, the p-contact distributes on top of the mesa and the n-contact is deposited at the bottom of the y trench. The metal composition for p- and n-contacts are Ti/Pt/Au (20:20:200 nm) and Ni/Au/Ge/Ni/Au (5:20 :130:30: 150 nm) respectively. The

contact resistance investigation of the metal contacts will be presented in Chapter 3. Based on the thickness of the metal contacts, a 500 nm thick LOR 5A layer is coated on the surface of the sample by spinning the photoresist at a speed of 4000 rpm A microscope image of the samples is shown in figure 2.32. It indicates there are no metal residuals left on the sample after the lift-off process.



(a) (b) (c)

Figure 2.32 Diagrams and a microscope image of the sample with the p- (red) and n-(yellow) contact deposited on the area where the dielectric has been etched off.

2.7.2 Bond Pad Deposition:

Two bond pads, the composition of which are Ti/Pt/Au (20:20:200 nm), are deposited at this step. These bond pads distribute on top of the dielectric layer and connect with the metal contacts. Figure 2.33 presents a scanning microscope image (SEM) of the device with two bond pads deposited on it. One of the bond pads connects to the bar of the y shape. The other connects to the mesa. Thus, the current injected in the bond pads can flow to the metal contacts area and then pumps the VCSEL, which leads to a probe friendly device without changing the size of the p- and n-contacts.

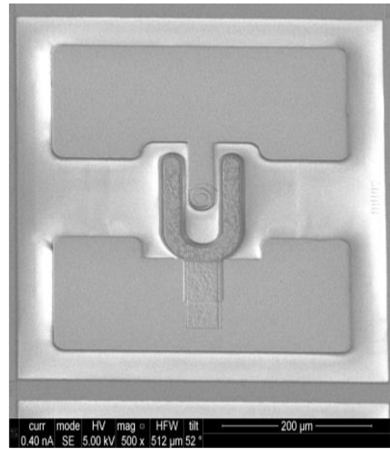


Figure 2.33 A SEM image of the sample with two bond pads deposited on top of it. These bond pads deposited on top of the dielectric connect with the p- and n-contacts.

The step sequence of the metallization process is summarized below:

1. Pre-bake sample in 120 ^{o}C for 5 mins
2. Spin LOR 5A at a speed of 4000 rpm
3. Bake the sample on a hot plate at 200 ^{o}C for 5 mins
4. Spin S1818 photoresist at a speed of 4000 rpm
5. Bake the sample on a hot plate at 115 ^{o}C for 5 mins
6. Expose the sample for 8 s
7. Develop the photoresist S1818 in micro-posit for 1 min
8. Bake sample in 120 ^{o}C for 30 mins
9. Develop the LOR 5A in CD-26 for 1min15 s
10. Bake sample in 120 ^{o}C for 5 mins
11. Deposit metal by the Plassys MEB400S
12. Immerse the sample in a beaker filled with acetone solution for 5 hours
13. Flow away from the lift-off metal from the sample surface
14. Clean and dry the sample

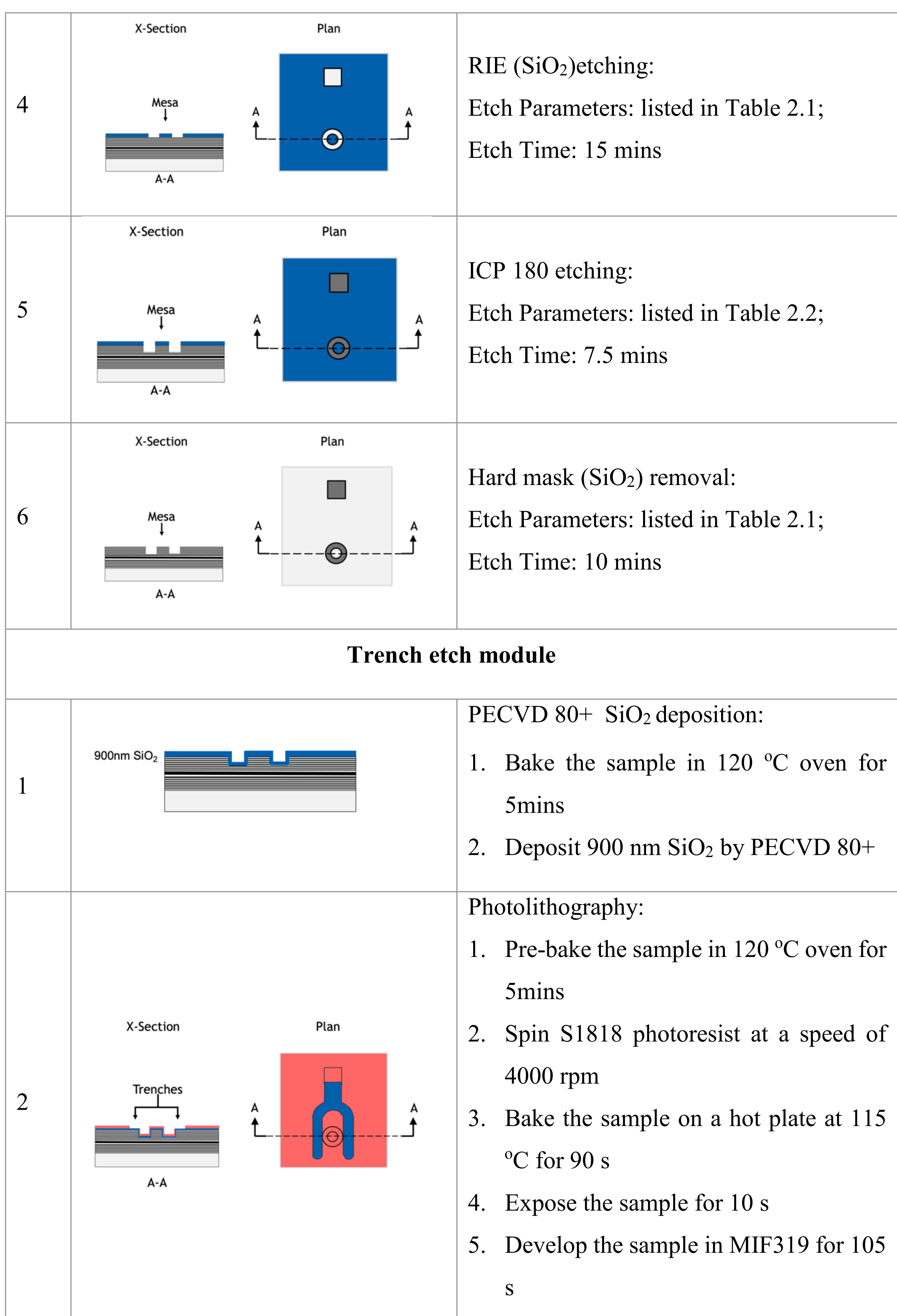
Annealing:

The final step of this module is to anneal the metal contacts at 450 ^{o}C for 30 s by using a rapid thermal annealer (RTA). This facility provides a rapid temperature changing that accelerates the metal atoms diffuse into the semiconductor layer. Thus, the contact resistance of the sample can be reduced profoundly. The measurements of the contact resistance shall see later in Chapter 3.

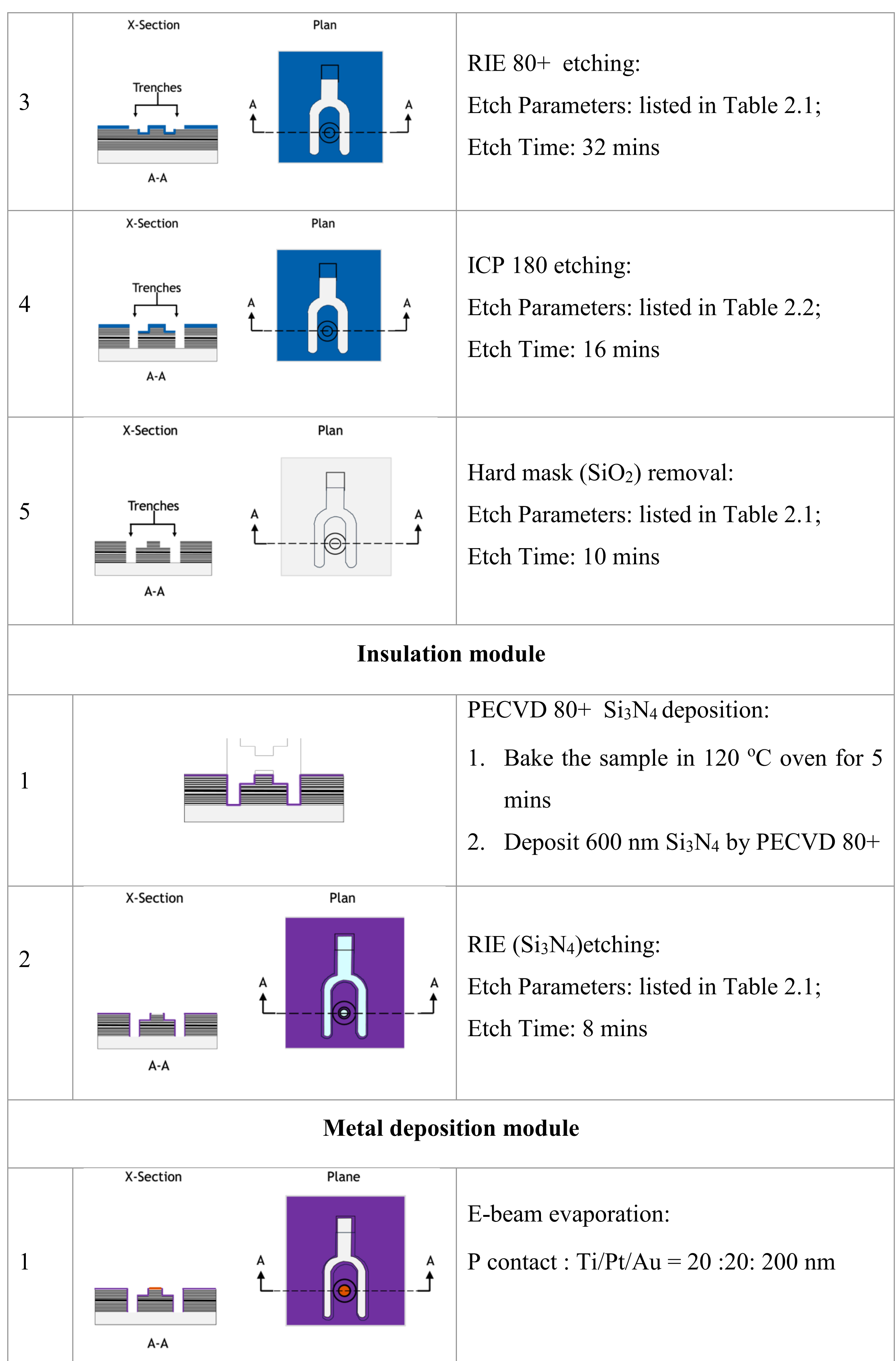
2.8 Fabrication Process Summary

This section briefly summarizes the fabrication process described above and explicitly delivers an overview of the fabrication flow in a form.

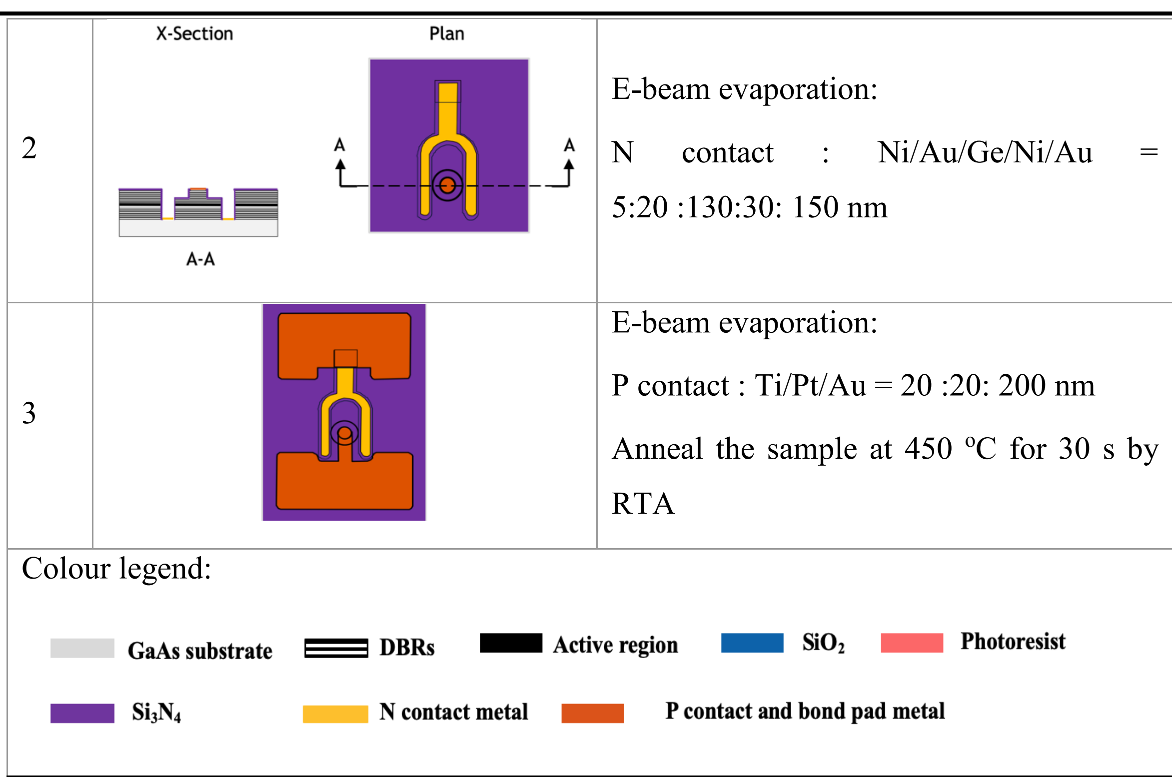
Step	Schematic	Description
	Mesa etch module	
1		Clean sample: 1. Check the sample under the microscope 2. Immerse the sample in acetone for 5mins 3. Immerse the sample in IPA for 5 mins 4. Rinse the sample by R.O. water for 5mins 5. Dry the sample by N_2 gun
2	400nm SiO_2	PECVD 80+ SiO_2 deposition: 1. Bake the sample in 120 °C oven for 5 mins 2. Deposit 400 nm SiO_2 by PECVD 80+
3	X-Section UV radiation mask A-A Plan A A	Photolithography: 1. Pre-bake the sample in 120 °C oven for 5mins 2. Spin S1818 photoresist at a speed of 4000 rpm 3. Bake the sample on a hot plate at 115°C for 90 s 4. Expose the sample for 10 s 5. Develop the sample in MIF319 for 105 s



4	X-Section / Plan; Mesa; A-A	RIE (SiO_2)etching: Etch Parameters: listed in Table 2.1; Etch Time: 15 mins
5	X-Section / Plan; Mesa; A-A	ICP 180 etching: Etch Parameters: listed in Table 2.2; Etch Time: 7.5 mins
6	X-Section / Plan; Mesa; A-A	Hard mask (SiO_2) removal: Etch Parameters: listed in Table 2.1; Etch Time: 10 mins
Trench etch module		
1	900nm SiO_2	PECVD 80+ SiO_2 deposition: 1. Bake the sample in 120 °C oven for 5mins 2. Deposit 900 nm SiO_2 by PECVD 80+
2	X-Section / Plan; Trenches; A-A	Photolithography: 1. Pre-bake the sample in 120 °C oven for 5mins 2. Spin S1818 photoresist at a speed of 4000 rpm 3. Bake the sample on a hot plate at 115 °C for 90 s 4. Expose the sample for 10 s 5. Develop the sample in MIF319 for 105 s



Step	Schematic	Process
3	X-Section / Plan	RIE 80+ etching: Etch Parameters: listed in Table 2.1; Etch Time: 32 mins
4	X-Section / Plan	ICP 180 etching: Etch Parameters: listed in Table 2.2; Etch Time: 16 mins
5	X-Section / Plan	Hard mask (SiO_2) removal: Etch Parameters: listed in Table 2.1; Etch Time: 10 mins
Insulation module		
1		PECVD 80+ Si_3N_4 deposition: 1. Bake the sample in 120 °C oven for 5 mins 2. Deposit 600 nm Si_3N_4 by PECVD 80+
2	X-Section / Plan	RIE (Si_3N_4)etching: Etch Parameters: listed in Table 2.1; Etch Time: 8 mins
Metal deposition module		
1	X-Section / Plane	E-beam evaporation: P contact : Ti/Pt/Au = 20 :20: 200 nm



2	X-Section Plan A A A-A	E-beam evaporation: N contact : Ni/Au/Ge/Ni/Au = 5:20 :130:30: 150 nm
3		E-beam evaporation: P contact : Ti/Pt/Au = 20 :20: 200 nm Anneal the sample at 450 °C for 30 s by RTA
Colour legend: GaAs substrate DBRs Active region SiO_2 Photoresist Si_3N_4 N contact metal P contact and bond pad metal		

Table 2.4 Fabrication flow of trench-etch VCSEL.

2.9 Conclusion

A reproducible fabrication process of the trench patterned VCSELs is presented in this chapter. It consists of four modules, including mesa etch module, trench etch module, insulation module and metal deposition module. Each module has been introduced with the diagrams and microscope images recorded during the fabrication. Considerable time and effort were dedicated to accomplishing the fabrication process with high fidelity and so to achieve a high yield. In the following chapter, the characteristics of the fabricated devices will be examined and analysed systematically. A further simplification and improvement have been developed for addressing specific challenges in some operations, which will be finally presented in Chapter 6 dedicated to future work.

This chapter focuses on the micro-fabrication process associated with the trench-etched substrate emitting VCSELs. It begins with an introduction of the GaAs VCSEL wafer then it presents an overview of the fabrication process. The major parts of this chapter describe the initial fabrication process supported by diagrams and optical microscope images.

Chapter 3

Characterisation of Trench-etch VCSELs

3.1 Introduction

This chapter focuses on the diode characteristics and optoelectronic properties of the fabricated VCSELs. These properties are linked to the capability of a laser to generate light.

A brief initial section introduces the circular transfer length method (CTLM) and reports the contact resistance measurement results. Then the diode characteristics of different diameter devices will be presented with the supported of I-V curves. The following paragraphs demonstrate the optoelectronic performance of these devices.

3.2 Contact Resistance

3.2.1 Circular Transfer Length Method

The metal contact is an essential component of an electrical pump device. It provides an area to inject current. Meanwhile, it provides a resistance, contact resistance, in series with laser diode. Since the heating generated by contact resistance deteriorates the device performance, the value of the contact resistance must be minimized to achieve optimal device performance. The evaluation and optimization of the contact resistance are therefore of critical importance.

The first method proposed to evaluate the contact resistance called transfer length method (TLM) [72]. This method determines the contact resistance based on the linear relationship between the resistance and the gap spacing of two identical metal contacts. This method is prone to a current crowding issue that generates an extra resistance at the edge of the contact [73]. As a result, the contact resistivity can be overestimated. An improved technique called the circular length method (CTLM) circumvents this issue by shaping the metal contact into a circle enabling current to flow out of the metal contact evenly in every direction [74]. In

most cases, the CTLM technique is preferable due to the higher measurement accuracy. This section introduces the CTLM technique and illustrates the CTLM measurement results for the p- and n- contact used for the fabricated VCSELs.

Figure 3.1 shows a schematic diagram of a typical CTLM structure. The top view of the structure is presented in figure 3.1(a). It depicts a set of metal circles with identical radius, r, deposited on the semiconductor surface. Each circle is considered as one segment. The radial distance from one segment to the next is labelled as s_1, s_2 and s_3 in figure 3.1(a). These distances vary sequentially in a set of CTLM features. Figure 3.1(b) shows the cross-sectional diagram of the CTLM and illustrates the four-probe measurement. The total resistance of each segment is measured by two pairs of probes using a four-wire techniques. The aim of using two pairs of probes is to eliminate any parasitic resistance from the probes. Current is injected into the structure through a pair of probes and the voltage of the structure is measured by the other pair of probes.

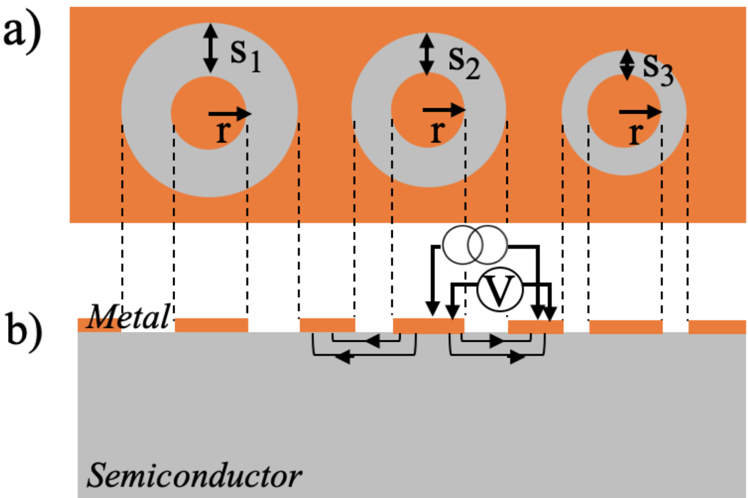


Figure 3.1 a) Top and b) cross-sectional views of the diagrams of a typical CTLM structure. A set of circular metal contacts of radius r are distributed with different gap spacing to the outer metal contact.

The relationship between the total resistance, R_T, measured at each segment and the gap spacing, s, is presented in equation 3.1 [75].

$$R_T = \frac{R_{sheet}}{2\pi r}(s + 2L_T) \cdot c \qquad 3.1$$

In this equation, r is the radius of the metal circle; R_{sheet} is the sheet resistance of the semiconductor; L_T is the transfer length of the contact resistance. The relationship between, R_T, and the gap spacing, s, is transferred into a linear plot by multiplying the correction

factor, c, which accounts for the difference in circumference of the inner and outer circle. This correction factor, c, is calculated as:

$$c = \frac{r}{s} \ln \frac{r+s}{r} \tag{3.2}$$

The other parameters, including the transfer length distance, L_T, and the semiconductor sheet resistance, R_{sheet}, may be extracted from the fitting graph (presented in the next section). A linear relationship has been found between, R_T, and gap spacing, s. The intercept of this linear fitting with the horizontal axes indicates the transfer distance, L_T, and the slope of this fitting line demonstrates, $R_{sheet}/2\pi r$. The contact resistivity, ρ_c, is determined by the expression:

$$\rho_c = R_{Sheet} \cdot L_T^2 \tag{3.3}$$

3.2.2 Evaluation of Contact Series Resistance

The section presents the CTLM measurement results of the p- and n-contact metal used in my work. The p-contact metal is composed of Ti/Pt/Au which has been reported to be a low resistance ohmic contact to p-doped GaAs material [76][77], and is widely used in GaAs device processing. For the n-contact alloy, it is formed of Ni/Au/Ge/Ni/Au that is considered as a low resistance ohmic contact to n-doped GaAs material [78]. It has been applied on many n-doped GaAs based semiconductor devices [79][80]. The p- and n-contact alloys are deposited on the p-doped side and n-doped side of the GaAs sample respectively. A single step of rapid annealing was executed for the sample using an RTA at 450°C for 30s in a N_2 gas atmosphere to achieve a low contact resistance [76].

Figure 3.2 shows the CTLM measurement results of the p-contact alloy. It plots the measured and corrected data of the total resistance corresponding to the gap spacing. This CTLM measurement consists of a set of circles with a radius, r, of 100 μm and the gap spacing, s, varies from 5 μm to 45 μm.

For the circular transfer length measurement (CTLM), the correction factors are applied for modifying the change of the circumference between different segments. This CTLM measurement aims to find the relationship of the total resistance with the gap, ‘s’ and thus obtain the contact resistivity. However, except the gap, ‘s’, the total resistance also changes with the circumference of inner and outer circular contact. Thus, each segment should have the same circumference to eliminate the effect of it in results. The correction factor is used

to correct this circumference difference between these segments. Then a linear relationship can be found between total resistance and gap, 's'. As figure 3.2 shows, the corrected data is plotted and that is fitted linearly with the gap spacing.

The coefficient of the determination of fitting, R^2, is 0.99. The intercept of the fitting with the vertical axis indicates two times contact resistance, $2R_c$, which equals 0.38±0.01 Ω; The intercept with the horizontal axis represents two times transfer length distance, $2L_T$, that is 21±0.1 μm. Combine with the equations mentioned above, the contact resistivity, ρ_c, of the p contact metal determined by this set of CTLM is $(1.30\pm0.01)\times10^{-5}\ \Omega\cdot cm^2$. Using this value of specific contact resistance, I predict the contact resistances to be obtained in table3.1. Previous studies have reported a contact resistivity of $2\times10^{-6}\ \Omega\cdot cm^2$ can be achieved on p-GaAs material [81]. My contact resistivity is one order of magnitude higher than that value. It is claimed that such low contact resistivity can be achieved after 5 mins 450°C annealing. To achieve lower contact resistivity, a further investigation on annealing condition for metal may be required in the future.

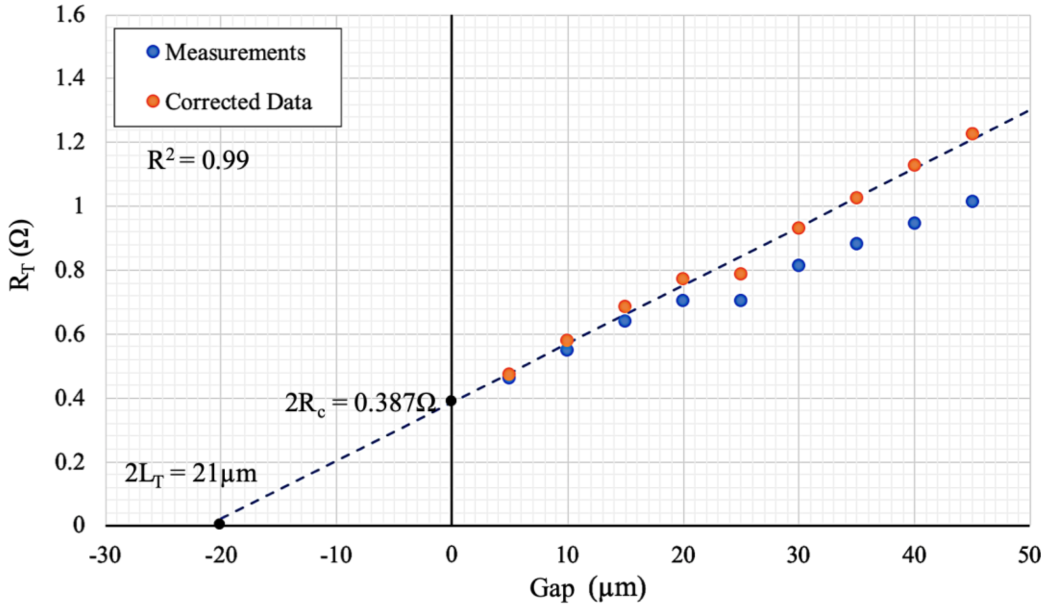


Figure 3.2 Measurement result of a set of CTLM. The measured and corrected data of the total resistance, R_T, is plotted versus the gap spacing. The alloy is composed of Ti/Pt/Au and deposited on the p-type GaAs material.

Analogous to the analysis presented before, the CTLM measurement result for the n contact alloy is illustrated in figure 3.3. However, data of gap spacing at 5 μm and 10 μm are missing. Because the metal in the gap area was not lifted-off successfully in the fabrication process. Figure 3.3 illustrates the fitting results of the corrected data has a R square value of 0.8. Then the contact resistivity determined by this set of CTLM measurements is $(3.80\pm0.83)\times10^{-6}$

Ω·cm². Predicted contact resistance for my devices are laid out in table 3.1. Due to a small R square value, the measured contact resistivity has a broad variation. This value is still one order of magnitude higher than the best reported in the literature that is 6×10^{-7} Ω·cm² is in [78]. It claims that an extra surface clean step before metallisation will improve the contact resistivity slightly. Based the measurement results, both p- and n- contact resistivity are one order of magnitude higher than the lowest values reported in literature. It suggests that lower contact resistance could be achieved by further reducing the contact resistivity. However, for my devices, these values of contact resistance are expected to be acceptable as detailed shown below.

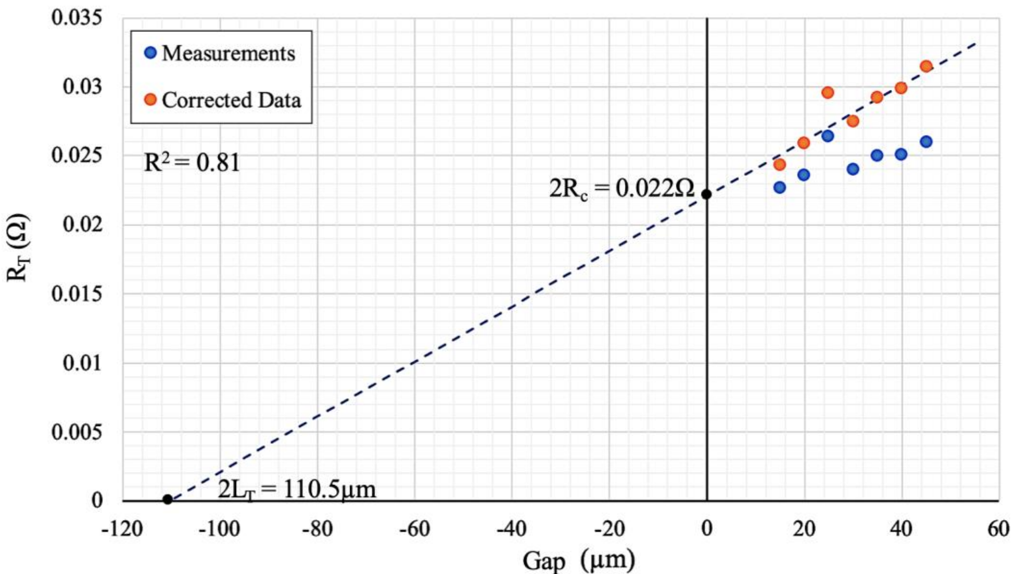


Figure 3.3 Measurement result of a set of CTLM. The measured and corrected data of the total resistance, R_T, plotted versus the gap spacing. The alloy is composed of Ni/Au/Ge/Ni/Au metal composition on n-type GaAs.

In summary, the p- and n-contact resistivity of the p and n metal contacts are $(1.30\pm0.01)\times10^{-5}$ Ω·cm² and $(3.80\pm0.83)\times10^{-6}$ Ω·cm² respectively. Combined with the size of the p and n contact of the designed VCSELs is known, the contact resistance can be evaluated. Figure 3.4 illustrates a diagram of the p and n contact area for the designed VCSEL device.

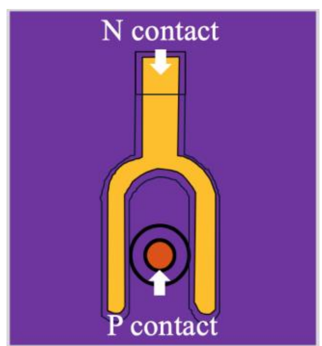


Figure 3.4 A diagram of the VCSEL device for illustrating the p and n contact area.

There are four kinds of VCSELs with the diameter of p contact of 40 µm, 30 µm, 20 µm and 10 µm. Table 3.1 presents the p- and n-contact resistance of different diameter devices. Previous studies reported contact resistance for a 40 µm VCSEL of 10 Ω, a 30 µm VCSEL of 17 Ω, a 20 µm of 30 Ω and a 10 µm VCSEL of 65 Ω [26][82]. Compared with these value, the contact resistance illustrate in table 3.1 are much smaller. However, the real series resistance of devices needs to be checked from device VI curves.

Diameter (µm)	P contact resistance (Ω)	N contact resistance (Ω)	Total contact resistance (Ω)
40	1.30±0.01	0.30±0.04	1.60±0.05
30	2.50±0.02	0.50±0.07	3.00±0.09
20	6.50±0.05	1.20±0.15	7.70±0.20
10	25.8±0.20	4.80±0.60	30.60±0.80

Table 3.1 Summary of the p- and n-contact resistivity measured by CTLM technique.

3.3 Diode Characteristics

This section presents the diode characteristics of the fabricated VCSELs. It focuses on comparing the properties of different diameter VCSELs. Initially, I introduce the equivalent circuit of the device corresponding to the device structure and link it to the measured I-V curve. The second part plots IV characteristics of different diameter VCSELs and presents an analysis of these results.

3.3.1 Device Geometry and Equivalent Circuit

There are four kinds of VCSELs fabricated with the mesa diameter of 40 µm, 30 µm, 20 µm and 10 µm. Figure 3.5 shows a schematic diagram of these devices that have been described

previously in section 2.3. The plan view diagram (left) presents the mesa structure of the device responding to the n-contact area. As it shows, the major difference between these devices is the mesa diameter. The A-A cross-section diagram illustrates the defined mesa of different diameter devices.

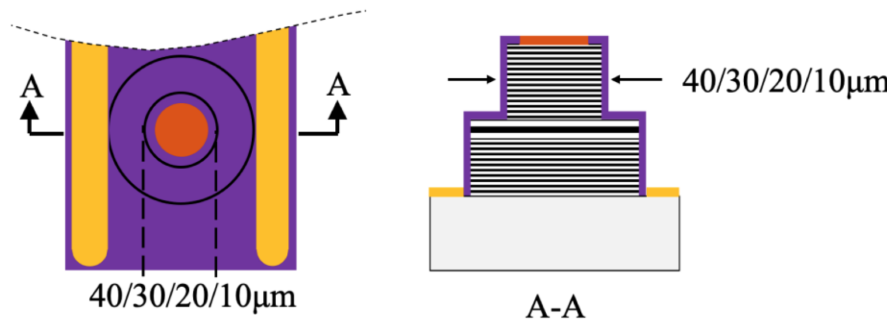


Figure 3.5 Diagrams of four samples with different diameter including 40 μm, 30 μm, 20 μm and 10 μm.

To understand the diode characteristics of the device, an equivalent circuit of the designed VCSEL is shown in the inset of figure 3.6. The diode in the circuit represents the active region of the device and the resistance, R_{series}, in series with it including contact resistance and the semiconductor resistance (from the DBR stacks). In parallel to the laser diode is the shunt resistance, R_{shunt}, which splits part of the injected current, thereby causing current leakage. For an ideal laser diode, the R_{shunt} is infinite and the R_{series} is desired to be negligible.

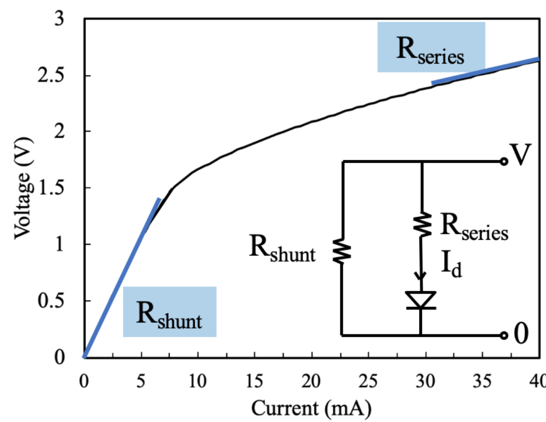


Figure 3.6 The I-V curve of a laser diode linked to the diode characteristics of the device; the inset presents an equivalent circuit corresponding to the VCSEL device.

Figure 3.6 exhibits a typical I-V curve of the device. When a small amount of current flows into the diode, the slope is dominated by R_{shunt}. Further increasing the current, the slope of the curve reduces as the diode turns on. Assuming $R_{shunt} >> R_{series}$, the slope of the I-V curve

after the diode turns on indicates the value of R_{series}. To minimise the effect of the R_{shunt}, the value of the R_{series} shall be determined at large currents.

3.3.2 Electrical Properties of Different Diameter VCSELs

The uniformity of fabricated laser diodes is presented by six 40 µm diameter devices. Figure 3.7 presents the (I-V) curves of these 40 µm diameter VCSELs. The measurements were carried out at room temperature with the CW current source Keithley 2400. As figure 3.7 shows, the soft turn-on indicates that shunt resistance is a common issue for them. However, the I-V characteristic of them varies very little from one to the other. It indicates that the devices have similar property in one fabrication round, may be comparable.

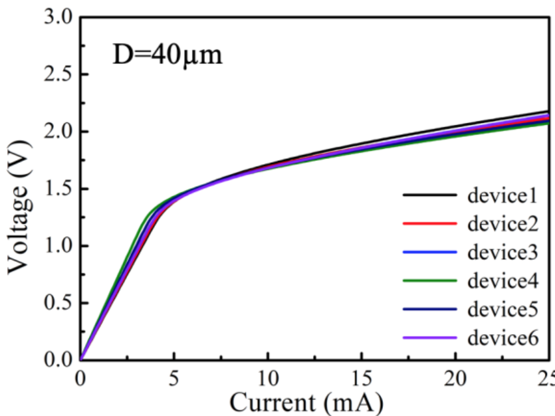


Figure 3.7 Current versus voltage (I-V) curves of six 40 µm diameter devices fabricated on the same batch.

Figure 3.8 presents the I-V curves for different diameter VCSELs. As it shows, 10µm VCSEL has a turn on voltage of 3.2 V. Similar turn on voltage for a 10 µm ion implantation VCSEL is also reported in [83]. However, there is also an oxide VCSEL with a diameter of 10 µm that presents a lower turn on voltage of 1.8V [82]. For 20 µm, 30 µm and 40 µm diameter devices shown in figure 3.8, they have a turn on voltage of 1.6 V, 1.4 V, 1.4 V respectively. In the literature, the lowest turn on voltage of GaAs VCSEL is about 1.4 V [84]. Therefore, the fabricated larger diameter devices achieve good turn on voltage. In the following, a comparison of different diameter devices is presented in terms of their series resistance and shunt resistance.

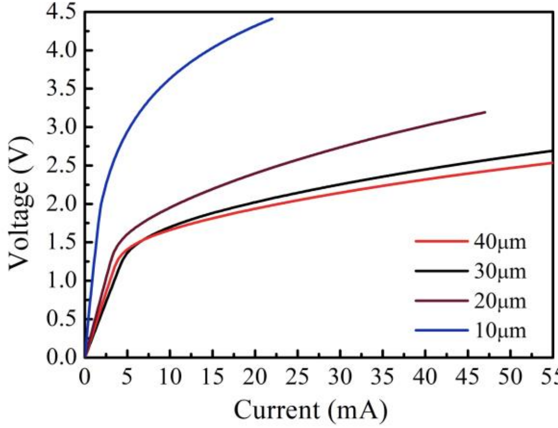


Figure 3.8 The measured I-V curves of 40 μm, 30 μm, 20 μm and 10 μm diameter VCSELs.

The shunt resistances of different diameter devices are plotted as a function of the mesa diameter in figure 3.9. It highlights that the value of the shunt resistance reduces as the diameter of the devices increases. The non-linear relationship between diameter and shunt resistance indicates that shunt resistance is not dictated by carrier leakage at the perimeter of the mesa diode. The shunt resistance is also non-linear in device area indicating that the shunt resistance is not related to e.g. the defects in the epitaxial material. The effect of mesa etch depth plays a role on this shunt resistance, which is described in section 3.5.

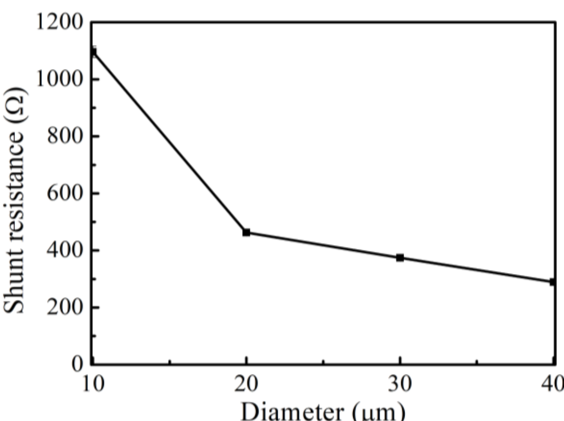


Figure 3.9 The shunt resistance of 40 μm, 30 μm, 20 μm and 10 μm diameter VCSELs determined by the measured V-I curves plots with the mesa diameter.

The measured values of the series resistance of different diameter devices are plotted in figure 3.10. In this figure, measured series resistance are presented referring to the contact resistance evaluated in section 3.1. As the diameter goes up, the value of the series resistance decreases rapidly. The contact resistance occupies large part of series resistance for fabricated devices. Thus, reducing the contact resistance of device would decrease device

series resistance, especially for small diameter devices. The other element of the series resistance is DBR resistance. According to literature, grading doped DBR has a contact resistivity of 9.6×10^{-7} Ω·cm^2/period [85]. For samples with mesa etched through 28 pairs DBRs, the DBR resistance is 2 Ω, 4 Ω, 9 Ω and 34 Ω for 40 µm, 30 µm, 20 µm and 10 µm diameter devices. These values correspond to the gap between evaluated contact resistance and measured series resistance shown in figure 3.10.

The series resistance of 40 µm, 30 µm, 20 µm and 10 µm VCSELs are 14 Ω, 17 Ω , 23 Ω and 78 Ω. A review of literature provides similar series resistance of the same size VCSELs of 10 Ω, 17 Ω, 30 Ω and 65 Ω respectively [26], [82], [18]. As we can see, the fabricated device have series resistance few ohm higher than previous reported VCSELs but in a reasonable range.

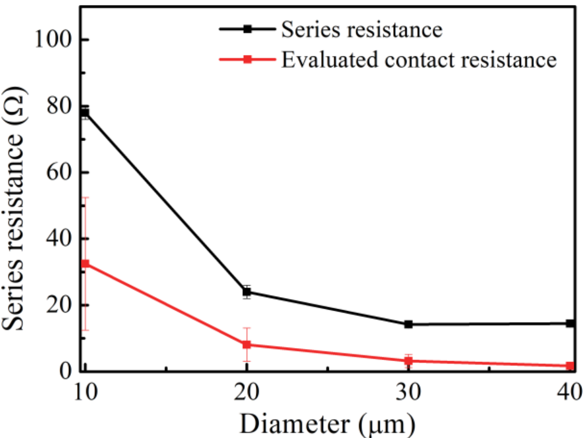


Figure 3.10 The series resistance of 40 µm, 30 µm, 20 µm and 10 µm diameter VCSELs determined by the measured I-V curves.

Overall, a large diameter device would have excellent diode characteristics except for a small shunt resistance. While the small diameter devices are suffered from large series resistance from DBRs and contact resistance which is hard to be avoided.

3.4 Opto-Electronic Characteristics

3.4.1 Substrate Absorption and Reflection

The substrate absorption and the reflection at the substrate/air interface in the device should be considered. This section aims to evaluate the power lost in these processes based on the material refractive index and the doping concentration. Figure 3.11presents a schematic diagram describing where the reflection and the absorption may occur within the device. As

it shows, the emission travels through a 625 μm thick doped substrate, thereby, suffering absorption caused by it. The reflection occurs at the interface between the substrate and the air amid the device, which leads to a part of the light being reflected into the substrate and being lost.

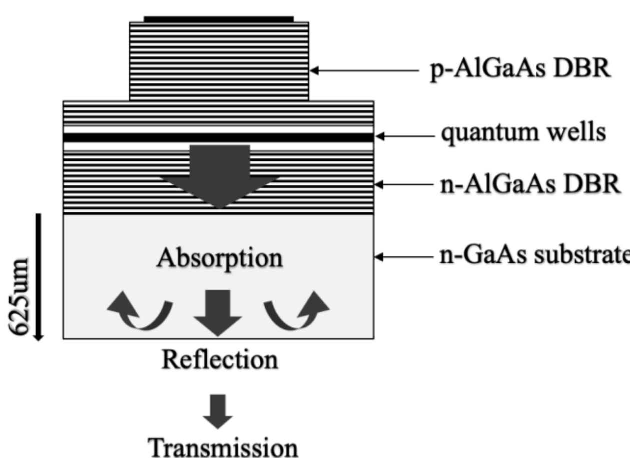


Figure 3.11 The diagram of the reflection and the absorption occurred in the VCSEL

Absorption:
The power absorbed in the substrate can be calculated by equation 3.4. When the light beam travels through a material of length, l, with an absorption coefficient of α, the relationship between the injected power, P, and the output power, P_{out}, can be expressed as [86]:

$$P_{out} = P \cdot e^{-\alpha l} \quad 3.4$$

The free-carrier absorption coefficient,α, of a material relates to its doping concentration and the wavelength of the transmitted light [87]. From the certificate of conformance data for the VCSEL wafer substrate, the expected doping concentration of the substrate is 2.5×10^{18} cm^{-3}, however, it specifies the doping concentration can vary from 0.5×10^{18} to 4×10^{18} cm^{-3}. As we can see, that is a broad range. Private communication with the epi supplier indicates that a value of $2.5\pm0.5\times10^{18}$ cm^{-3} for the doping concentration of the substrate is a more realistic value for both the absolute, and variation in doping. The absorption loss calculated in this section is based on this emission wavelength of 980 nm.

Figure 3.12(a) presents the absorption coefficient measured from six n-type GaAs samples with different doping concentrations [88]. Since emission of our device is at 980 nm, the data presented in figure3.12 selected at λ=1 μm. Figure 3.12(b) plots the selected data against sample doping concentration. Here a linear function is chosen to fit the relationship between absorption coefficient and doping concentration of n-doped GaAs. As shown in figure

3.12(b), the absorption coefficient of 14.5 cm^{-1} and 21.5 cm^{-1} are determined by 2×10^{18} cm^{-3} and 3×10^{18} cm^{-3} sample doping concentration that are corresponding to minimum and maximum doping concentration of the GaAs sample.

Here selects a 2.5×10^{18} cm^{-3} doping concentration of last epilayer to represent the doping condition of substrate. In this case, the absorption coefficient is 17.5 cm^{-1} for the GaAs substrate and 66±6% of output power is lost in absorption process.

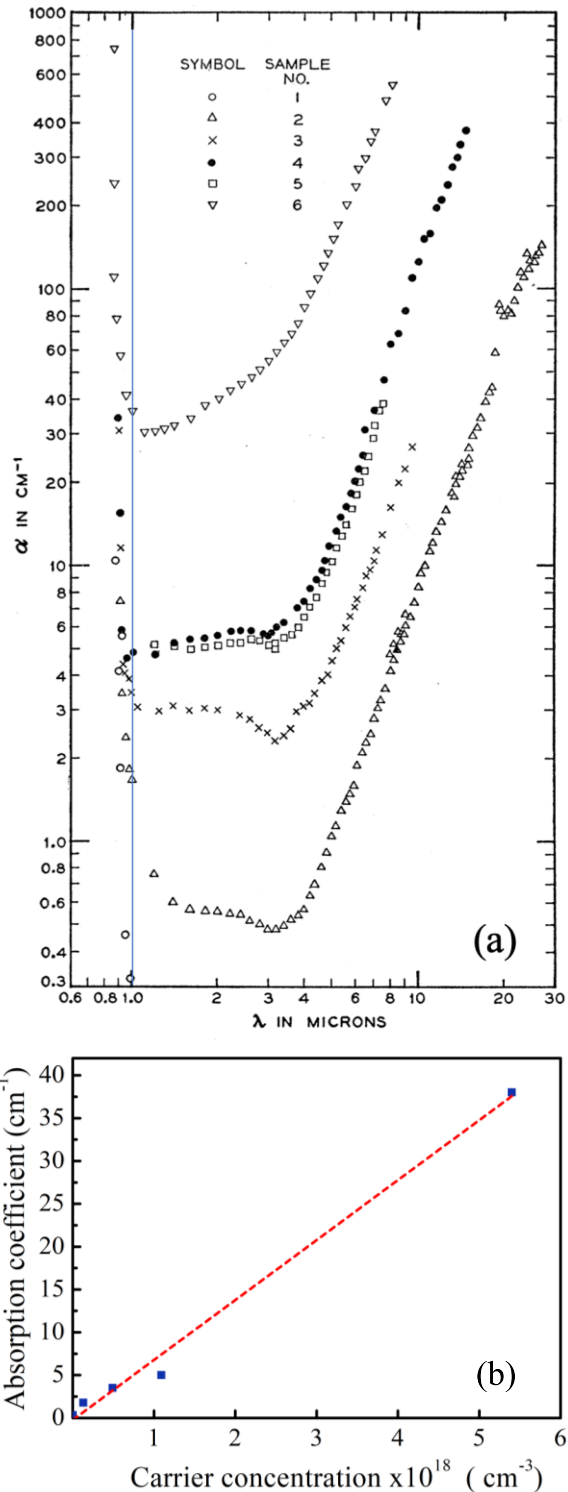


Figure 3.12 (a) Absorption coefficient of six n-doped GaAs samples that have different doping concentration is plotted with emission wavelength [12]; (b) At λ=1 µm, the absorption coefficient of six samples is plotted with sample doping concentration. Suppose a linear relationship is fitted, sample with 2.0×10^{18} cm^{-3},2.5×10^{18} cm^{-3},3×10^{18} cm^{-3} doping concentration has absorption coefficient of 14.5 cm^{-1}, 17.5cm^{-1} ,21.5 cm^{-1}.

Reflection:

Assuming the light generated in the cavity propagates as a plane wave, the reflection of it at the interface between the substrate and the air can be determined by equation 3.5 [89]. The

refractive index of GaAs and air is 3.55 and 1 respectively. Substitute these parameters in equation 3.5, it could be found that 31% of the power reflected by the substrate interface and only 69% light comes out of the device.

$$R = \left(\frac{n_1 - n_2}{n_1 + n_2}\right)^2 \qquad 3.5$$

In total, there is 76% of the generated power lost in the absorption and the reflection processes. The output power should multiply a factor of 4.2 for fabricated substrate emitting VCSELs. However, as it mentioned above, the doping concentration varies in a broad range. Correspondingly, this factor varies from 3.6 to 5.2. Therefore, measurement result does not take this power loss in count in order to display clear figures. The reader should remember that powers should multiply a factor of ~4.2 to consider the power loss in the substrate.

3.4.2 L-I as a Function of Mesa Diameter

The light-current (L-I) characteristics of different diameter devices are presented in figure 3.13. The measurements were carried out at room temperature with the CW current. As figure 3.13(a) shows, the threshold current of 40 μm, 30 μm, 20 μm and 10 μm devices are 7 mA, 7.5 mA, 5 mA and 3 mA, respectively. The threshold current density (J_{th}) of these devices is 0.48, 1, 1.6 and 3.9 kA/cm^2 as shown in figure 3.13(b). As we can see, the threshold current density increases as device size goes down. Such increasing on threshold current density may stem from the extra heating in small cavity device as thermal and series resistance increases [17].

Previous report that a 40 μm VCSEL with 15mA threshold current [26], a 30 μm device with 8.5 mA [18], a 20 μm VCSEL with 2 mA threshold current [90], a 10 μm devices with 1 mA threshold [82]. For large diameter devices as 40 μm and 30 μm VCSELs, the threshold current of fabricated device are lower than previous study. It is interesting to see that shunt resistance of large diameter devices has little effect on threshold current. However, for 20 μm and 10 μm devices, threshold current are 2 mA higher than devices reported in literature. This may due to the extra heating generated in small devices.

These devices achieve the maximum output power at roll-over points. The 40 μm device has a maximum output of 4.63 mW; the 30 μm device has a maximum output of 4 mW. For 20 μm and 10 μm diameter devices, their maximum output power are 2.1 mW and 0.7 mW. Previous study found a 40 μm VCSEL has a maximum output of 56 mW [26]; a 20 μm VCSEL has an output of 30 mW; a 10 μm has an output of 0.6 mW. However, such high

power devices of 40 µm and 20 µm are mounted on a diamond heat spreader and a copper substrate. Since devices fabricated here suffers from substrate loss, the output power of devices is lower than expected. This characteristic is expected to be improved with further mount a heatsink to the epi-side of the devices.

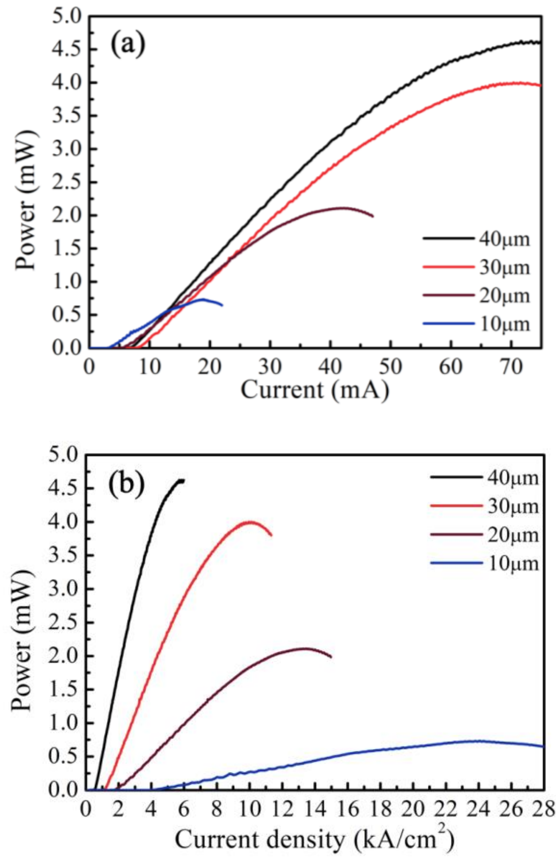


Figure 3.13 The output power of different diameter VCSELs plots against (a) injected current and (b) current density.

The slope efficiency is a parameter used to evaluate the ability of a laser to generate photons [17]. Figure 3.14 illustrates the slope efficiency of fabricated 40 µm, 30 µm, 20 µm and 10 µm diameter devices. The slope efficiency of devices declines as the diameter reduces from 40 µm to 10 µm. It is possible that the small diameter device has a higher thermal impedance which deteriorates the ability of the device to generate photons.

As it shown in figure 3.14, the 40 µm VCSEL has a slope efficiency of 0.1 W/A considering the light exiting the substrate surface. Regardless of the substrate loss, this slope efficiency is possible to be 0.42 with a lower value of 0.36 W/A, and upper value of 0.52 W/A given by uncertainty in substrate-based optical loss. This value is a little lower than best-in-class for oxide confined VCSEL that has a slope efficiency of 0.8 W/A [26]. However, the device in this paper incorporates a heat spreader, heatsinking and anti-reflective coating. The fabricated VCSEL in this work is comparable with a proton implantation VCSEL that has a

slope efficiency of 0.037 W/A [18]. For the small diameter device, the fabricated 10 μm diameter device has a slope efficiency of 0.04 W/A or 0.16 W/A without substrate loss. Prior study reports a slope efficiency of 0.09 W/A for a 10 μm VCSEL [82]. Thus, such slope efficiency is comparable with VCSELs in literature.

The VCSEL devices fabricated in my work has an air-post structure that is less powerful on carrier confinement compared to proton implantation [36], regrown structure [39], oxide aperture [91]. However, such air-post structure simplifies the fabricated process. Since power is not the main factor in this study, the way to improve output power of fabricated device is not involved in my work.

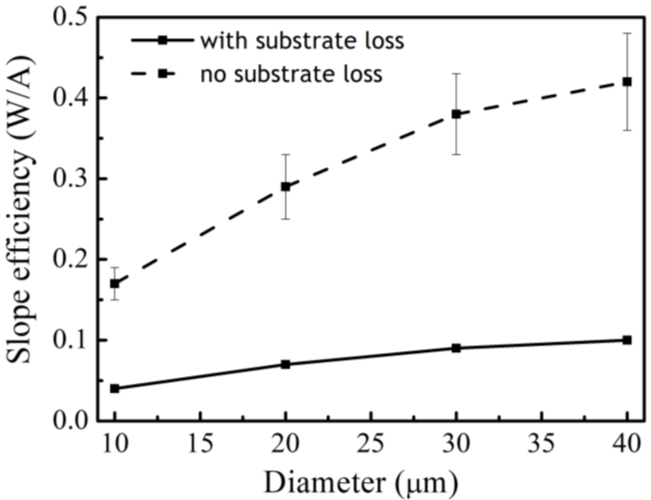


Figure 3.14 The slope efficiency of 40 μm, 30 μm, 20 μm and 10 μm diameter VCSELs.

Here introduces an efficiency defined as the maximum output power per unit area. When the designed device works as a VCSEL array, this parameter is critical. It evaluates that at unit area how much power generated by different diameter devices. Figure 3.15 presents this value for different diameter devices. The smallest diameter device has the highest value of 940 W/cm^2, 40 μm diameter VCSEL has a value of 350 W/cm^2 that is lower than the value of 470 W/ cm^2 reported in the literature [26]. So power loss for large diameter devices is a problem for achieving high efficiency laser array.

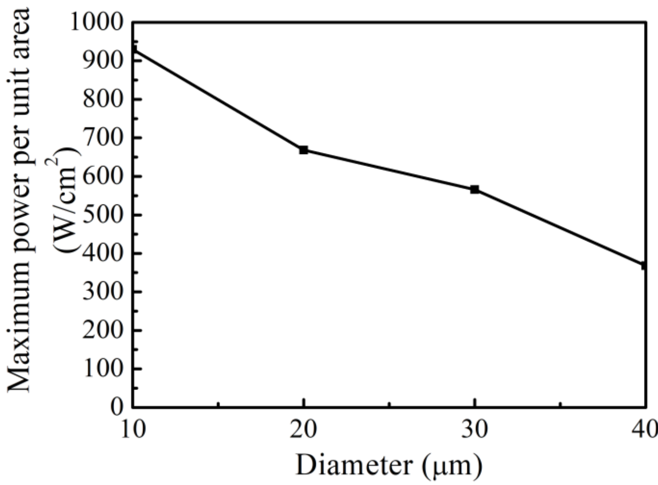


Figure 3.15 The maximum output power per unit area of different diameter devices (power value used here is the maximum power achieved by each kind of device).

To evaluate the device comprehensively, I now introduce another parameter called wall-plug efficiency. It represents the ability of a device to convert electrical power into optical power. Equation of it is shown in Eq 3.6. Figure 3.16 presents the wall-plug efficiency of different diameter devices against the injected current. The power loss in the substrate has been considered in calculating wall-plug efficiency. As it shows, the maximum wall-plug efficiency obtained by 40 μm, 30 μm, 20 μm and 10 μm diameter devices are 14.5±2.1%, 12.5±1.8%, 9.5±1.4% and 4.5±0.6% respectively at 20 mA, 25 mA, 17 mA and 12 mA. Previous study reports a 38% wallplug efficiency for a 20 μm VCSEL that is operated with a diamond heat spreader and a copper stage. For a 10 μm diameter device, 4% wallplug efficiency is illustrated in [82]. So a small diameter devices fabricated in my work has comparable wallplug efficiency with the literature. For our devices, heating and power loss in substrate deteriorate the performance of them and higher wallplug efficiency is expected if these issues can be tackled. Additionally, reducing contact resistance will reduce the required bias, and also increase wall-plug efficiency.

$$\text{Wallplug efficiency} = \frac{P}{IV} \qquad 3.6$$

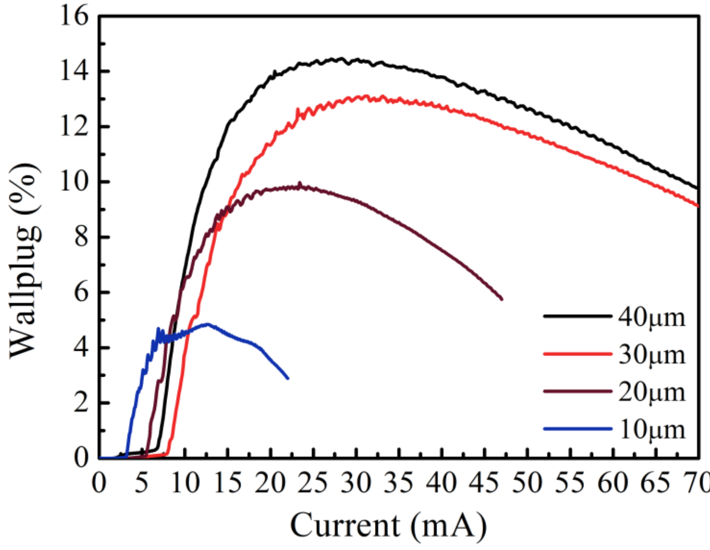


Figure 3.16 The wall-plug efficiency of 40 μm, 30 μm,20 μm and 10 μm diameter devices.

3.5 Characteristics of VCSEL as a Function of Mesa Height

To explore the effect of fabrication process and the device structure on operating characteristics, a series of experiments on different height mesas was carried out. The performance of fabricated VCSELs with different mesa heights of 4 μm, 4.5 μm and 5.2 μm called sample 1, 2 and 3 respectively. The diagrams of these devices are presented in figure 3.17. The plan view (top) of them is identical, however, the A-A cross-section diagrams of them are different from each other. Referring to the position of the active region. Sample 1 has the mesa patterned 0.5 μm above the active; sample 2 has the mesa etched just above the active region; sample 3 has the mesa etched through the active region. The properties of these devices are presented in the following.

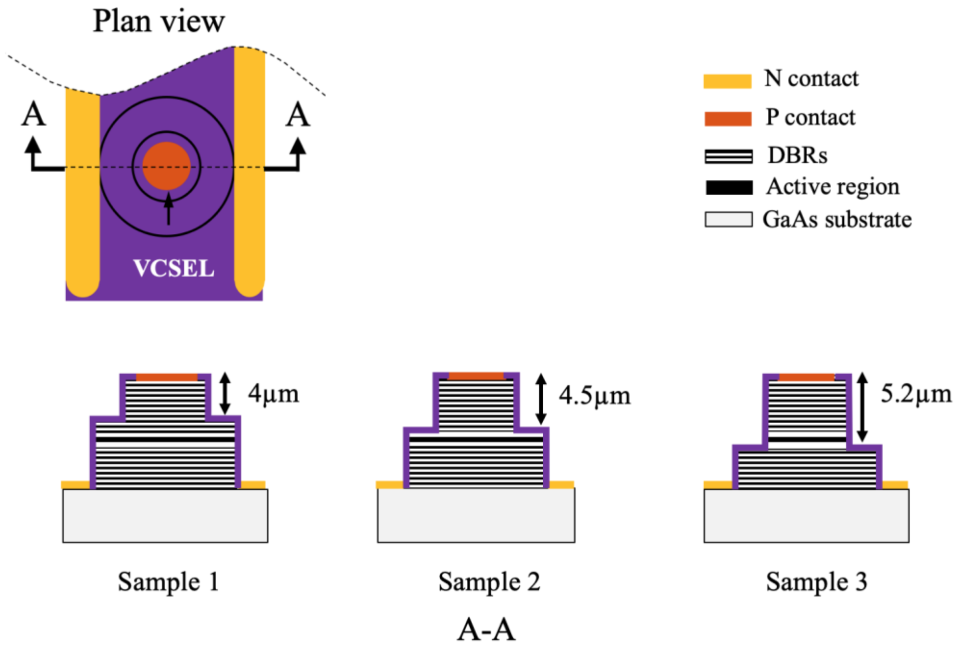


Figure 3.17 Diagrams of three samples with the different mesa height. Top diagram is the plan view of devices and the bottom are the A-A cross-section diagrams of devices.

The diode characteristics of different samples are inspected by measuring the I-V curves (shown in figure 3.18) of them. All devices have the same mesa diameter 40 μm.

The I-V characteristics of three different samples are shown in figure 3.18. Sample 3 with the deepest mesa etching has a higher turn on voltage. Sample 1 and 2 do not have such high turn on voltage but suffer from soft turn on issue. The shunt resistances of sample 1, 2 and 3 can be calculated that are 203±2 Ω, 319±2 Ω and 864±5 Ω respectively. Therefore, the shunt resistance of devices is related to the structure of mesa. It implies that current confinement property affects the shunt resistance of devices. For turn on voltage, it increases with the depth of mesa. This trend is also found in [83]. It reports a 7 V turn on voltage for a VCSEL with mesa etching depth of 6.8μm and a 4.7V turn on voltage for a VCSEL with mesa etching of 1.8 μm. So this high turn on voltage is expected when mesa depth is increased.

For series resistances, samples 1, 2 and 3 have it of 15±1.0 Ω, 14.5±0.5 Ω and 15.5±1.0 Ω. This parameter varies little between samples. This is attributed to identical metal contact area for these devices.

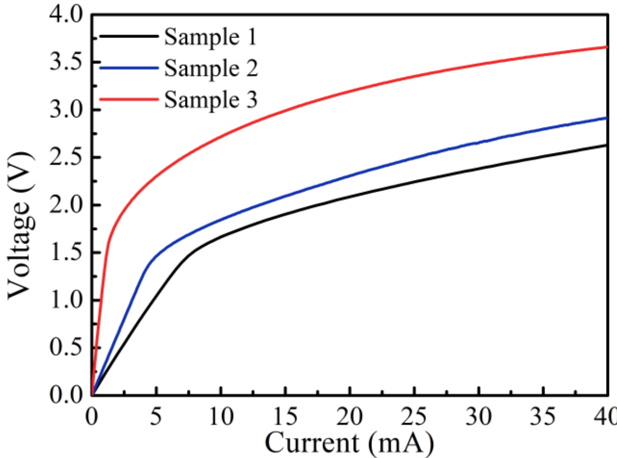


Figure 3.18 I-V curves of 40 μm diameter VCSELs with different mesa height called sample 1, 2 and 3.

The light intensity-current curves of three devices are presented in figure 3.19. The threshold current for sample 1, 2 and 3 are 22 mA, 7.5 mA and 6 mA respectively. Simple 1 with the shallowest etch depth is most likely to have an underestimated driven active region area. Thus, a higher threshold of it is introduced. As we can see, the threshold current reduces as mesa etching depth rises up. It also been observed in previous study [83]. In literature, it reports that 6.5 μm deep mesa VCSEL has a threshold current of 3.2 mA but 1.3 μm mesa deep VCSEL has a threshold of 5.5 mA. Since mesa plays a role to confine the injected current, a deep mesa for air-post structure VCSEL has an impact on threshold current of devices.

As shown in figure 3.19, devices have similar slope efficiencies that are 0.09 W/A, 0.1 W/A and 0.09 W/A respectively. Sample 3 shows roll-over at a lower injected current. It may be due to that the exposed active region. Such exposed boundary of active region causes extra surface recombination. Sample 1 is expected to have a large output. However, it has a threshold current that is double of others, which drops down the conversion efficiency of sample 1. Overall, sample 2 achieves the highest output power equals 3 mW at this range of injected current and delivers better performance than others. So a device structure with mesa etched above active region but close to it is an optimal choice for air-post VCSEL.

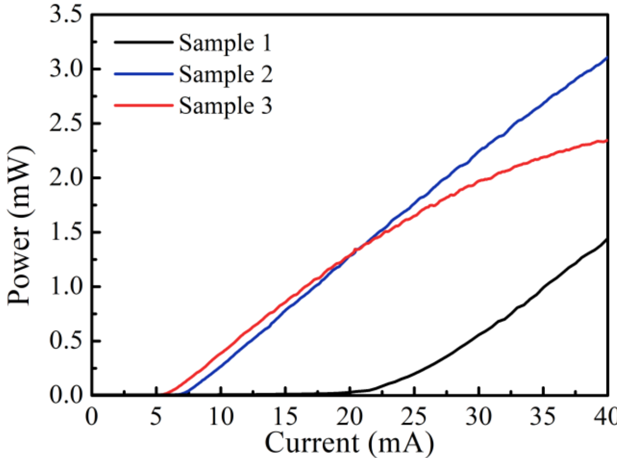


Figure 3.19 I-L curves of 40 μm diameter VCSELs with different mesa height called sample 1, 2 and 3.

3.6 Conclusion

This chapter evaluated the performances of the fabricated VCSELs through their diode characteristics and optoelectronic properties. The performances of different diameter devices have been compared, which indicates that the large diameter device has the higher maximum output power and better slope efficiency but poor current confinement capability. Furthermore, the properties of devices with different mesa height has been illustrated. It has been found that the mesa height affects the current confinement capability and the slope efficiency of the devices. In the following, I will describe the analysis of the polarisation pinning of these device.

3.7 Future Work

With regard to this chapter, future work would lie in reduce contact resistance and improve shunt resistance. In order to achieve higher output power, the wafer substrate should be thinned to reduce substrate loss and thereby understand the internal efficiency of devices more accurately. However, the surface should maintain the quality as its origin. Following suitable thinning, an AR coating could be applied to enhance output power. It is also useful to analyse devices by using a very short pulse and heatsink for engineering better CW performance.

Chapter 4

Polarisation Characteristics of Trench-etched VCSELs

4.1 Introduction

In this chapter, the polarisation characteristics of the fabricated trench etched VCSELs are experimentally determined. Firstly, the measurement system and coordinates are described. Then, the measurement results including polarised LI curves and optical polarisation suppression ratio of different diameter devices are presented. The preferred polarisation direction and ratio is determined, demonstrating polarisation pinned multimode VCSELs.

4.2 Experimental

To examine the polarisation property of fabricated devices, a measurement system was assembled to test the polarised power and polarised nearfield of the devices. A diagram and a picture of the measurement system are presented in figure 4.1. Figure 4.1 (a) shows a diagrammatic representation of the system, and figure 4.1 (b) illustrates the picture of the set-up with a pair of probes placed at the side. This system is designed to test substrate emitting devices with emission from 700 nm to 1100 nm. As it shows in the diagram, the sample is placed on a transparent stage. A CCD camera is installed right above the stage to provide a live magnified image of the sample. The emission generated by the device is collimated by a lens and then it passes through a polariser that has an extinction ratio of 2600. The examining polarisation direction can be selected by rotating the direction of this polariser. The polarised emission then be divided into two parts by a 90:10 beamsplitter. 90% of the light travels into a power detector and 10% of the light forms a nearfield image on the camera. Based on this design, a polarised LI curve and a nearfield image of tested device can be measured at the same time. However, this chapter focuses on the polarised LI curves of different diameter devices.

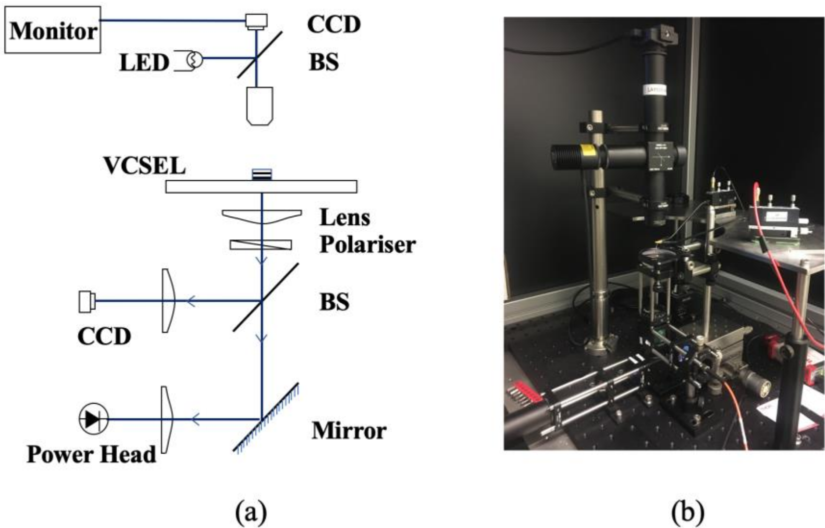


Figure 4.1(a) Diagram of a set-up designed to measure light output at a one polarisation direction and nearfield image of the emission at the same time; (b) A picture of the set-up with the probes placed at the side.

Figure 4.2 shows a SEM image of a 40 μm diameter trench etched VCSEL. In order to describe the polarisation direction of emission, a term θ is used to represent the position of a polariser corresponding to the trench direction. A dash line drawn on this SEM picture is parallel to the trench and it is used to clarify angle θ corresponding to trench direction. In the following, θ=0° indicates that a polariser is placed at trench direction and θ=90° represents a polariser is placed at the orthogonal direction.

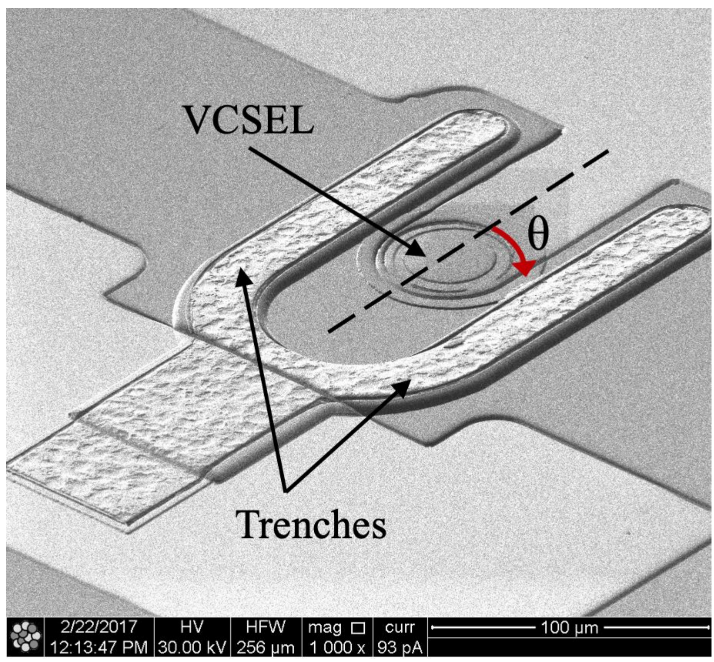


Figure 4.2 A SEM image of a 40 μm diameter trench etched VCSEL, angle θ is used to describe the position of a polariser. Trench direction is set to be 0°.

To evaluate the polarisation ratio of emission, a term called optical polarisation suppressed ratio (OPSR) is demonstrated. This term was firstly mentioned in [56]. It describes the power ratio of the emission between orthogonal polarisation states. The expression is shown in equation 4.1. $P_{0°}$ represents the emission with the electric field along trench direction; $P_{90°}$ represents the emission with the electric field perpendicular to trench. The value of OPSR is described in decibel.

$$OPSR = 10\log\left(\frac{P_{0°}}{P_{90°}}\right) \qquad 4.1$$

4.3 Polarised LI as a Function of Mesa Diameter

The polarisation characteristic of different diameter devices (typical devices selected at random) are presented in this section. Three kinds of emission with different polarisation states are presented in the LI curves. They are 0° polarised emission, 90° polarised emission and a total output of devices.

Figure 4.3 plots 0°, 90°, a total output and the OPSR value of a 10 μm trench etched VCSEL as a function of injected current. As it shows, this device has a threshold of 3.2 mA. At the threshold current, the emission is polarised at 90°. However, the polarisation direction changes to 0° at I=3.5 mA. The polarisation switch happens many times as the current increases. Consequently, the value of OPSR fluctuates between -15 dB and 15 dB with the injected current (shown in dash line). The measurement result shows that the emission of 10 μm VCSEL has unstable polarisation direction. Thus, the 30 μm wide trenches have no apparent effect on pinning the polarisation of a 10 μm VCSEL.

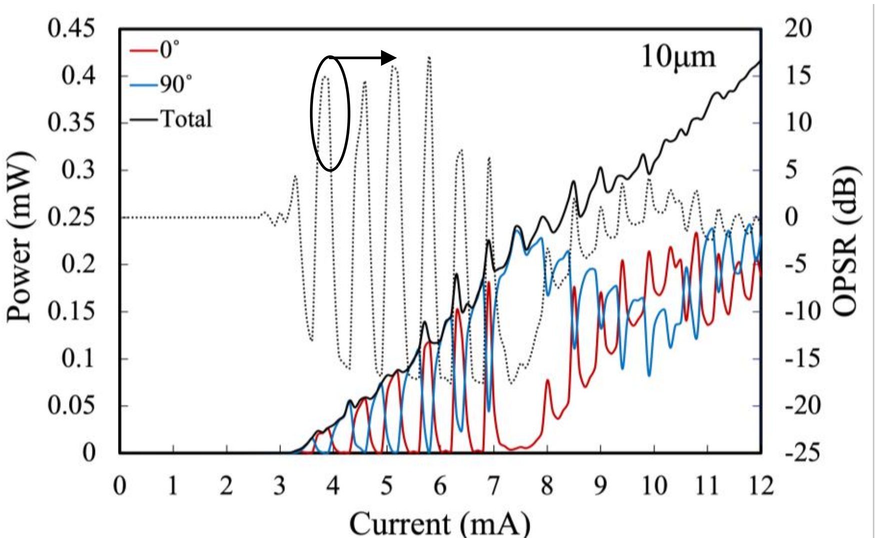


Figure 4.3 0°, 90° polarised emission, total power and OPSR value of a 10 μm trench etched VCSEL are plotted as a function of injected current.

To identify the polarisation direction of the emission, the polarised power of the device is detected as a function of θ. The polariser is rotated from 0° to 360° with a step of 10° and the polarised power was measured accordingly. Figure 4.4 presents the measurement results at a bias of 5.2 mA and 6.2 mA that before and after a polarisation switch. As shown in figure 4.4, the outline of the curves follow a $\cos^2(\theta)$ dependence. It indicates that the emission performs a linear polarisation characteristic. At I=5.2 mA, the peak of the curve locates at 0°, 180° and 360° (labelled as 0° in the following); at I=6.2 mA, the curve peaks at 90° and 270° (labelled as 90°). A half π shift is observed from I=5.2 mA to I=6.2 mA. Therefore, the 10μm trench patterned VCSEL generates linear polarised emission but the polarisation direction of emission jumps between 0° and 90° at different injected current.

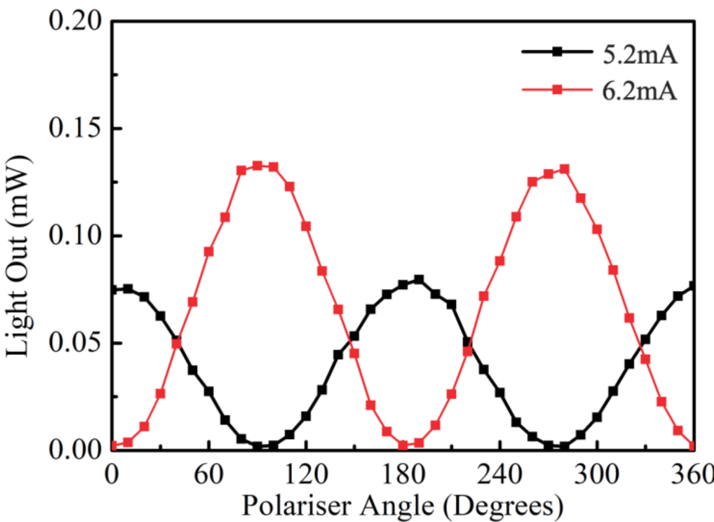


Figure 4.4 Polarised output power of a 10 µm VCSEL is plotted against the polariser angle θ at the bias of 5.2 mA and 6.2 mA.

The measurement results of a 20 µm trench etched VCSEL is presented in figure 4.5. Figure 4.5 presents the 0° polarised output, 90° polarised output and total output of a 20 µm diameter device against injected current. The threshold of this device is 5 mA. As figure 4.5 shows, 0° polarised emission achieves lasing at first. However, 90° polarised output power exceeds 0° polarised output power at 5.8 mA. It induces a polarisation switch. After that, 0° polarised emission obtains higher slope efficiency and becomes the dominant light output at 6.5 mA. The output power difference of orthogonal polarisation states gradually diminishes as current increases. Accordingly, the value of OPSR fluctuates between -14dB and 15 dB at near threshold, however, it gradually goes to zero at 24 mA. For a 20 µm device, 0° polarised emission is slightly higher than 90° polarised emission at injected current much larger than threshold. However, the polarisation switch phenomenon is observed at near threshold for this device.

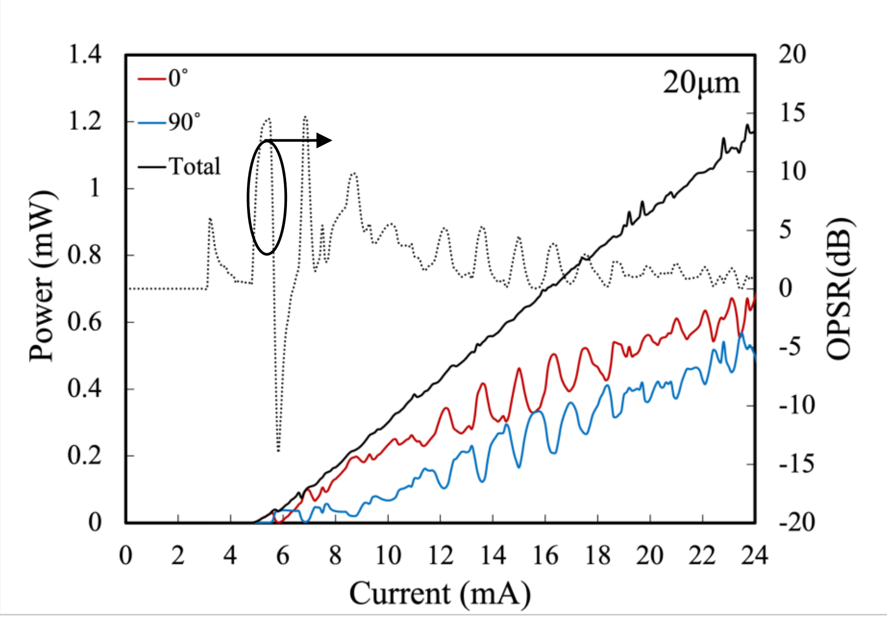


Figure 4.5 0°, 90° polarised emission, total power and OPSR value of a 20 µm trench etched VCSEL are plotted as a function of injected current.

The polarisation direction of the 20 µm device has been examined by rotating the polariser for a round. Figure 4.6 presents the measurement result at I=9 mA. As it shows, the outline of this curve shows a $\cos^2(\theta)$ shape and it peaks at 0°. The valley of this curve is higher than zero, indicating non-ideal behaviour as a linearly polarised emitter. The emission not only contains linear polarised light but also includes other polarisation emission. Therefore, the emission of 20 µm diameter device has a dominant polarisation direction along 0° and it shows a linear polarisation property.[explain random polarisation]

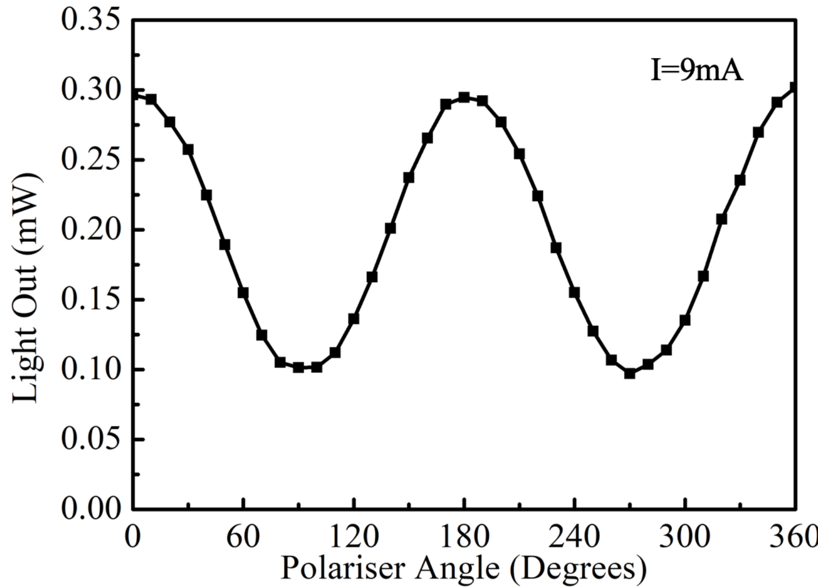


Figure 4.6 Polarised output power of a 20 μm VCSEL is plotted against the polariser angle θ at a bias of 9 mA.

In terms of 30 μm VCSEL, the light output of it is presented in Figure 4.7. As it shows, the 0° polarised output is always larger than 90° polarised output for 30 μm diameter trench etched device. The LI curves of the two polarisation states contain some ripples. The reason of it is unknown but it is probably due to the modes competition between orthogonal polarisation states. Differ from 10 μm and 20 μm diameter VCSELs, no polarisation switch is observed for the 30 μm VCSEL. As a result, the OPSR is positive since the lasing condition is achieved. The value of OPSR goes up and down and gradually stable at 3 dB. As we can see, 30 μm device has a stable polarisation state and the OPSR is positive for this device. This result indicates that the etched trenches probably present a positive effect on pinning the polarisation direction for a 30 μm diameter VCSEL.

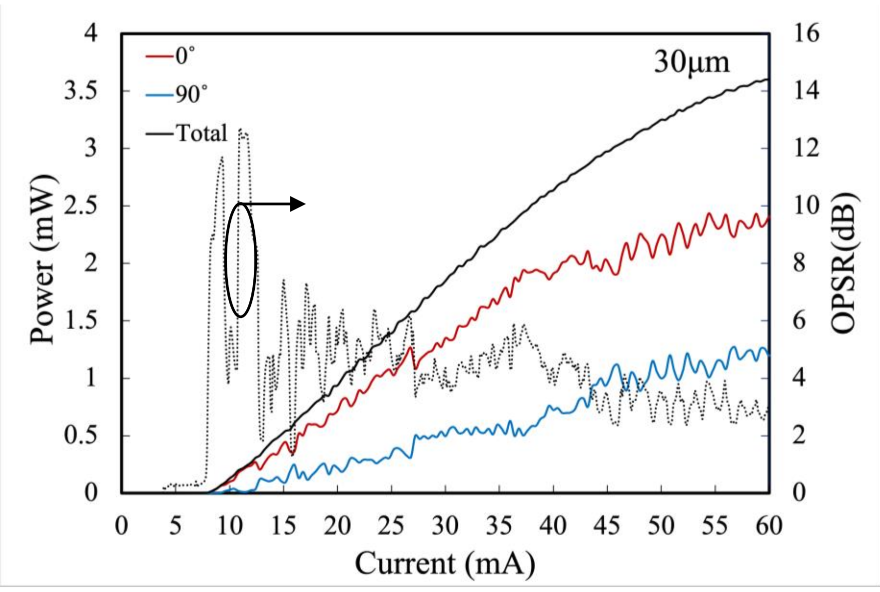


Figure 4.7 0°, 90° polarised emission, total power and OPSR value of a 30 μm trench etched VCSEL are plotted as a function of injected current.

Polarised light output of the 30 μm VCSEL at a bias of 15 mA is plotted referring to the polariser angle. The result is shown in Figure 4.8. The outline of the curve follows a $\cos^2(\theta)$ dependence and the peak of it orients at 0°. The valley of this curve is higher than zero. It indicates that the emission of 30 μm device is linear polarised along trench direction, however, a small part of random polarised light is included.

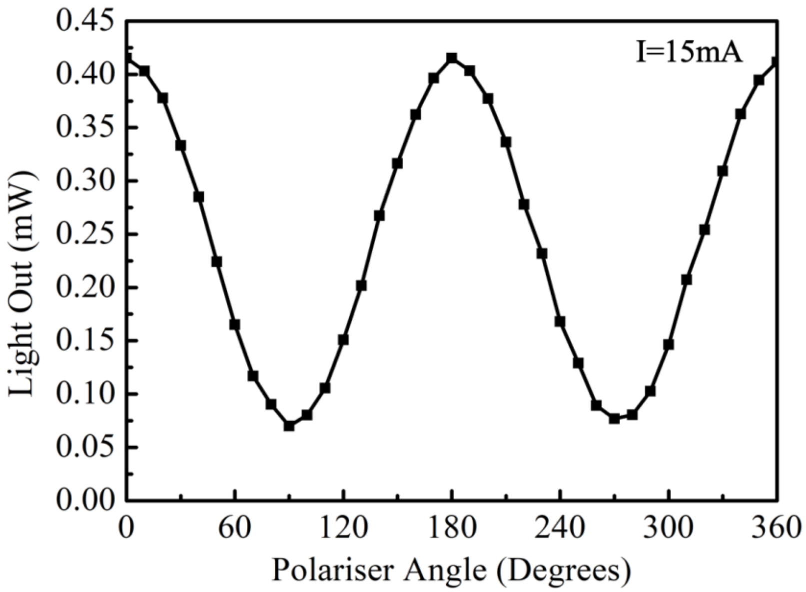


Figure 4.8 Polarised output power of a 30 μm VCSEL is plotted against the polariser angle θ at a bias of 15 mA.

Figure 4.9 presents the 0° and 90° polarised emission, total power of a 40 μm device against the injected current. The emission of the two polarisation states both generates at the

threshold. However, 0° polarised emission has a higher output power than 90° polarised emission. The OPSR is positive for this device. Such OPSR value gradually stable at 8 dB at injected current larger than threshold. Compared to the 30 μm device, the value of OPSR is higher. Therefore, the 40 μm device has a stable polarisation direction at 0°and the OPSR of it obtains 8 dB. The etched trenches probably perform a positive effect on pinning polarisation direction.

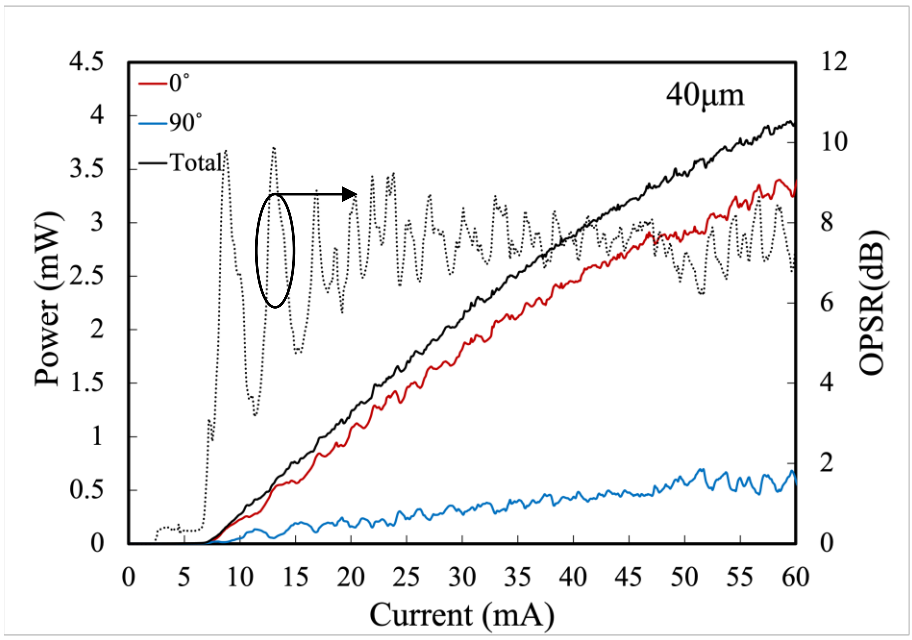


Figure 4.9 0°, 90° polarised emission, total power and OPSR value of a 40 μm trench etched VCSEL are plotted as a function of injected current.

To inspect the polarisation direction of emission, the output of 40 μm diameter device is measured at different polarisation angle. Figure 4.10 presents the measurement results at a bias of 16 mA. The curve has a sinusoid outline and it peaks at 0°. As it shows, the sinusoid curve has a large amplitude of 0.45 mW. It indicates that a large part of the emission is linearly polarised along 0°. For 40 μm diameter VCSEL, the dominant polarisation direction sits at trench direction and it is linear polarised.

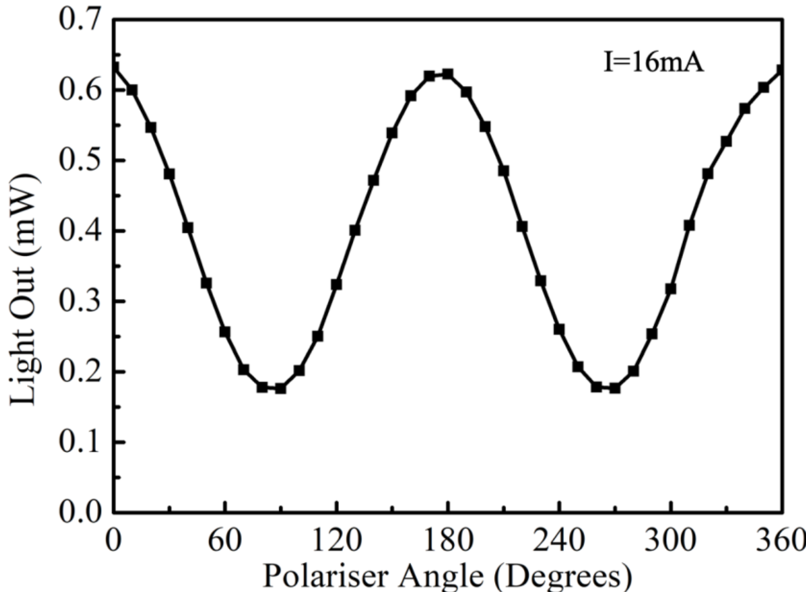


Figure 4.10 Polarised output power of a 40 μm VCSEL is plotted against the polariser angle θ at a bias of 16 mA.

In summary, the polarisation property of the trench patterned VCSELs varies with device diameter. Figure 4.11 summaries the OPSR value of different diameter devices. It rises up from 0 dB to 8 dB as the diameter of device increases from 10 μm to 40 μm. The polarisation stability of the emission improves as the diameter of the device increases. The dominant polarisation direction of trench etched devices is along 0° that is parallel to trench direction.

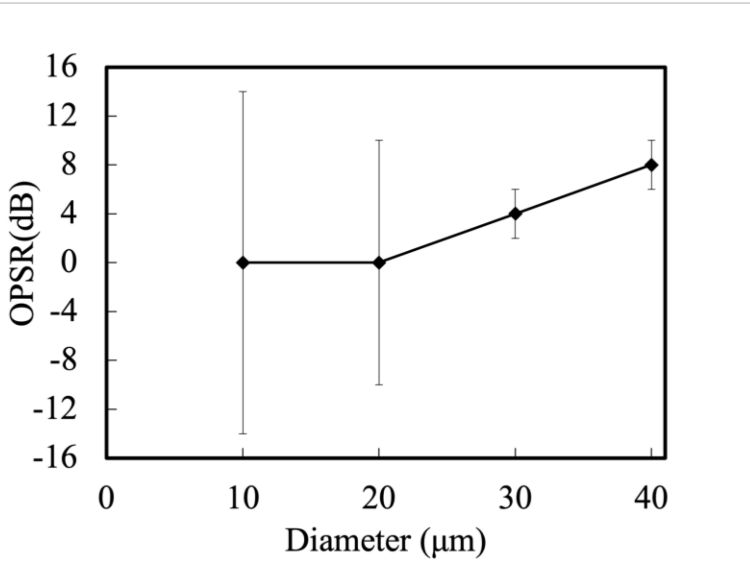


Figure 4.11 The OPSR value of 10 μm, 20 μm, 30 μm and 40 μm diameter devices.

Measurement System Check:
Figure 4.12 illustrates the LI curves of the device measured under different orientations within the test apparatus to confirm that any measured difference is due to the device, and

not a measurement artifact. The inset shows the pictures of the device with the trench aligned to 0° or 90°. As figure 4.12 shows, when the trench aligns to 0°, the 0° polarised output is higher; when the trench aligns to 90°, the 90° polarised emission is higher. The slight differences in the LI traces (OPSR = 5.2 and 6.5 for the two traces) are typical for making multiple up/down sweeps of the drive current. For static measurements, the polarisation ratio changes by no more than 1% in one hour. Therefore, the dominant polarisation direction always follows the trench direction no matter where it points with regard to the measurement system.

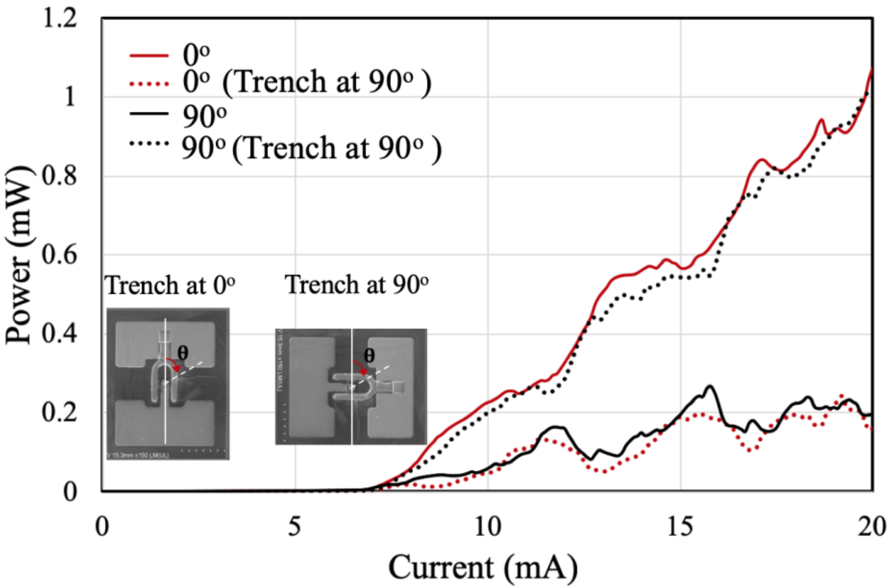


Figure 4.12 Polarised LI curves of a 40 μm VCSEL measured at trench along 0° and trench along 90°.

4.4 Polarised LI as a Function of Mesa Height

As it introduced in section 3.5, there are three samples fabricated with different mesa height. This section presents a polarisation characteristic comparison between these samples. The orthogonal polarisation suppression ratio (OPSR) of the 40 μm VCSELs with different mesa height is plotted against the threshold current in figure 4.13.

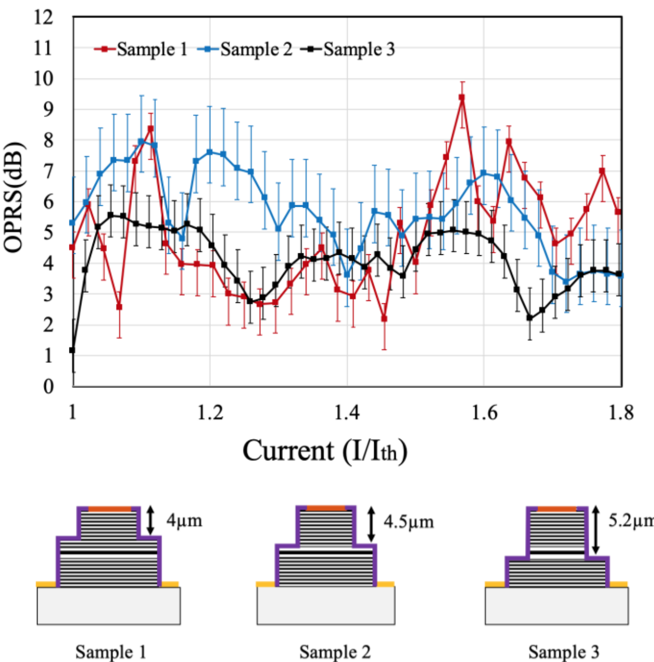


Figure 4.13 OPSR values of three 40 μm trench etched devices with different mesa height.

As figure 4.13 shows, these devices all present positive OPSR value. It indicates that the dominant polarisation direction for all the 40μm diameter devices stabilised at 0°. Secondly, even the values of the OPSR of the samples are different, they varies in a similar range (between 1 dB to 9 dB). No clear tendency is found among these three devices. The average OPSR for sample1, sample2 and sample3 is 4.2±2.0 dB, 6.9±1.2 dB 4.9±0.7 dB respectively. Sample 2 shows the highest average OPSR so was selected for future studies.

4.5 Conclusion

The fabricated trench patterned VCSELs are characterized with respect to their polarisation direction and their optical polarisation suppressed ratio (OPSR). A comparison between different diameter VCSELs has been demonstrated. The 40 μm and 30 μm diameter devices have the most stable polarisation direction and positive OPSR value. However, 20 μm and 10 μm diameter devices have unstable polarisation property It has been found that the stability of the polarisation improves as the diameter of the device increases, and for particular mesa etch depths. The next chapter will present an investigation on the polarisation property of trench etched devices through combined spatial/spectral measurements.

4.6 Future Work

In the following, I will describe the analysis of the polarisation pinning of these devices utilizing polarised spectral and polarised near-field imaging measurement results. With regard to this chapter, future work would lie in investigate the trench etched device with larger diameters. A maximal value of OPSR with device diameter has not been found. It is clear that an infinitely wide mesa device would have zero OPSR but we have not yet determined an optimal value for this device geometry. To draw a concrete conclusion, this investigation should be carried out with many more VCSELs from one wafer, possibly requiring automated test equipment to be developed.

Chapter 5

Spatial and Spectral Analysis of Lasing Modes

5.1 Introduction

This chapter presents an investigation on polarisation characteristics of fabricated trench-etched VCSELs. The first part demonstrates a set-up designed to simultaneously measure polarised spectrum and polarised nearfield emission. The second sections illustrates the nearfield images of polarised spontaneous emission of different diameter trench etched VCSELs. The final part focuses on the polarisation characteristics of stimulation emission. A frequency splitting of orthogonal polarised modes is investigated for a 40 μm diameter trench etched VCSEL. The details are shown in the following.

5.2 Set-up

A schematic diagram of the experimental apparatus is presented in figure 5.1. As it shows, VCSEL device is placed on a glass stage. The emission of the device first be collimated by a lens coated with anti-reflection coating of 700 nm to 1000 nm and passes through a linear polariser with extinction ratio of 2600. The polarised light split into two paths by going through a 90:10 beamsplitter that has no polarisation preference. 10% of the light propagates to a monochromatic camera DCC1545M [92]. Such camera has a resolution of 1280×1024 pixels and it is sensitive to infrared emission. The nearfield of the light output is recorded by this camera. Then, the rest of light is being focused into a multimode fibre connected to the optical spectrum analyser (OSA HP 71450B) that will be introduced in the following. As we can see, this set-up can measure the nearfield image and a spectrum of the polarised emission simultaneously.

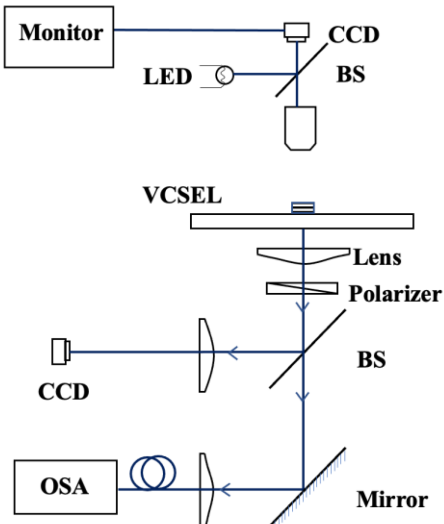


Figure 5.1 Diagram of the set-up used to measure polarised nearfield images and the polarised spectrum of emission simultaneously.

The optical spectrum analyser HP 71450B utilized in the experiment has a minimum resolution of 0.08 nm. Figure 5.2 presents the spectra measured in different resolution provided in the manual of the OSA [93]. With the resolution larger than 0.1 nm, the peak of the spectra are flat. At a resolution of 0.1 nm, the spectrum is described by a Gaussian distribution with 0.1 nm bandwidth shown in figure 5.2. Due to the good overlap, it is possible that the spectrum is presented in form of Gaussian distribution.

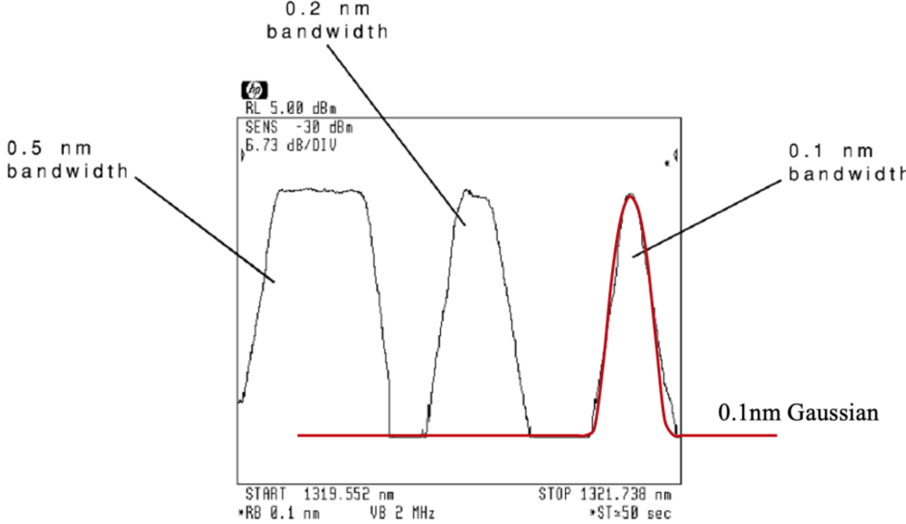


Figure 5.2 Spectra measured at different resolution presented in the manual of optical spectrum analyser HP71450B.

Nearfield concept:

To clarify the near field concept, it is necessary to define the beam width at first. This term is defined as the radius at which the amplitude of light intensity falls to 1/e of its peak value [3]. It varies with the measurement distance 'z' due to the diffraction issue. As equation 5.1 shows, the beam width varies parabolically with z, where k_0 is propagation constant ($2\pi/\lambda$), a, is the beam waist.

$$w^2 = \left(4z^2 + {k_0}^2 a^4\right)/{k_0}^2 a^2 \qquad 5.1$$

In the near field, the beam width 'w' equals to the beam waist 'a' and it is independent with the measurement distance, 'z' [3]. Beam pattern measured in the near field is called near field pattern. In this region $4z^2 \ll k_0^2 a^4$, the beam width can be assumed as a constant. If we write this condition in terms of the beam waist, a, and the emission wavelength, λ, it has an expression as equation 5.2. Suppose for our VCSEL devices, the aperture equals to the beam waist. As equation 5.2 shows, for a 980 nm 40 μm diameter VCSEL, the maximum distance 'z' for measuring the near field pattern is 1.28 mm.

$$z \ll \frac{\pi a^2}{\lambda} \qquad 5.2$$

The fundamental near field measurement set up is illustrated in figure 5.3 [94]. To measure the near field pattern, a lens system should be used to focus the beam at the device aperture. As it shows, the device is set at the focus point of lens L1 and then the laser beam generated from it is transferred to the focus point of lens L2. At the final step, the nearfield pattern is recorded by a CCD camera. In this system, a polariser and a neutral density filter were used. The design of the set up used in this project resembles this set up for measuring the nearfield of the VCSELs.

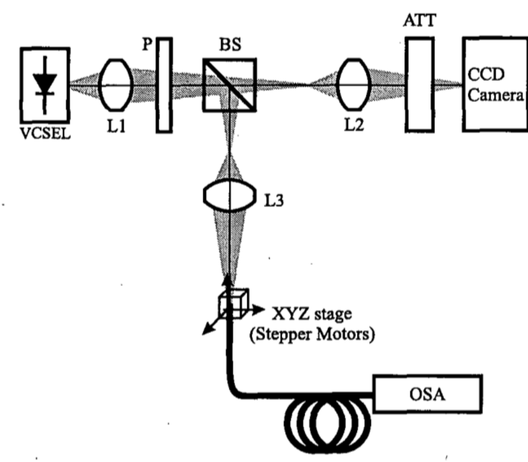


Figure 5.3 Setup for spectrally resolved near field measurements used in literature [94].

5.3 Polarised Spontaneous Emission

Previous study of trench etched method reports a refractive index difference (Δn) of material at parallel and perpendicular to trench directions. Such refractive index difference is expected to generate a shift of spontaneous emission distribution. Figure 5.3(a) presents a diagram of expected polarisation resolved spontaneous emission distribution. As it shows, the shift of spontaneous emission distribution delivers a modal gain difference of cavity modes. As a consequence, the cavity modes generated with electric field parallel to the trench direction achieve higher spontaneous intensity level, shown in figure 5.3(b).

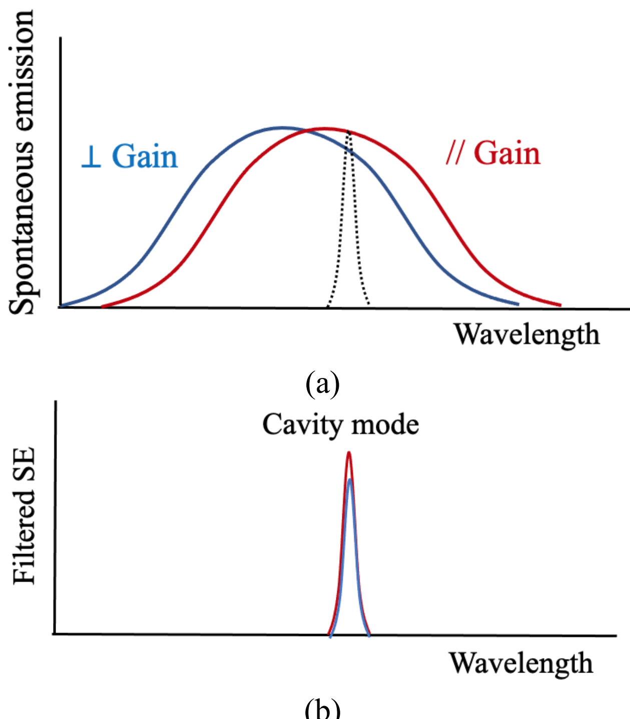


Figure 5.4 (a) Expected polarisation resolved spontaneous emission of trench etched active region. (b) Filtered polarisation resolved spontaneous emission of VCSEL cavity modes.

In this study, the device has a circular current injected area. Figure 5.4 shows a diagram of it. The injected current flows in the device form the top and the current is confined by dielectric boundary. Corresponds to this structure, it will be easy to understand the nearfield images measured for spontaneous emission.

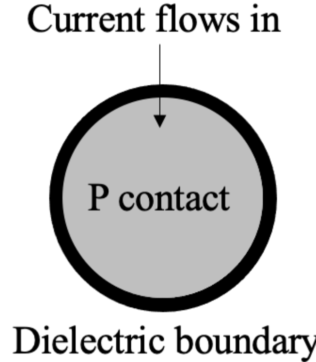


Figure 5.5 A diagram of VCSEL device to clarify current injected direction, p contact area and boundary condition of the device.

The spontaneous emission polarisation property of different diameter devices are shown by the nearfield images in figure 5.5. For these images, the origin is at the centre of VCSEL and the y axis is aligned to the trench direction. In figure 5.5, red colour indicates that 0° polarised emission is stronger; blue colour indicates that 90° polarised emission is stronger. Figure 5.4 (a) and (b) show the results of 40 µm and 30 µm diameter devices. As it shows, red colour occupies larger part of the aperture. So 0° polarised spontaneous emission is stronger for 40 µm and 30 µm devices. For 20 µm devices, the image shown in figure 5.4(c) has white colour in the centre of aperture. It implies the polarisation selection of spontaneous emission is not strong. For 10 µm device shown in figure 5.4(d), half of the aperture shows red and the other half shows blue. So the 0° polarised emission is stronger at the right half of aperture and 90° polarised emission is stronger at the left half of aperture. Compared with 20 µm and 10 µm diameter devices, 40 µm and 30 µm diameter devices perform clear polarisation selection of spontaneous emission. It is encouraging to find that polarisation stable devices, 30 µm and 40 µm diameter VCSEL, have stronger spontaneous emission at 0° polarisation state. The results suggest that a weak link may exist between gain amplitude and polarisation stability.

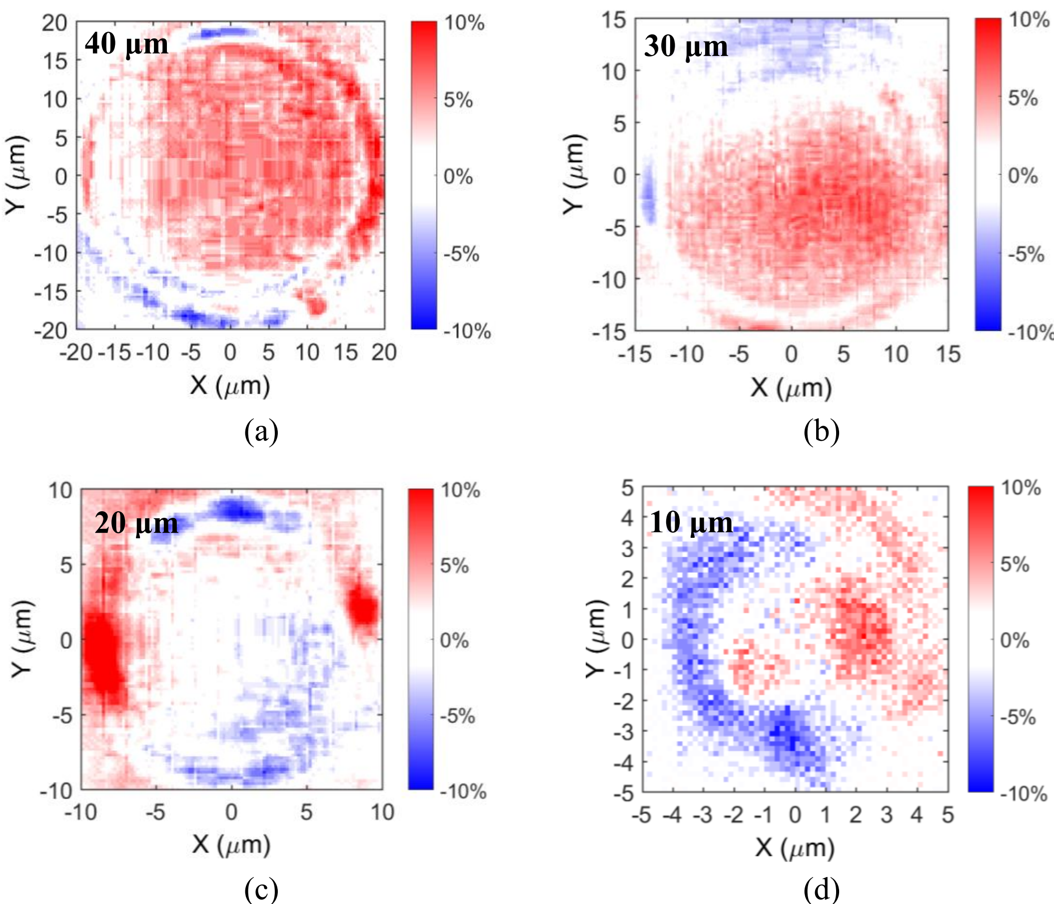


Figure 5.6 Intensity difference of orthogonal polarisation states defined as Δ(0°-90°)/maximum 0° polarised spontaneous emission intensity. The results of 40 µm, 30 µm 20 µm and 10 µm diameter VCSELs are shown in (a), (b), (c) and (d) respectively.

5.4 Detailed Analysis of 40 µm Device

As it presented in Chapter 4, the 40 µm diameter trench etched VCSEL presents a stable polarisation property with OPSR of 8 dB. This section aims to investigation the polarisation property of this device in different current injected regions. Figure 5.6 presents polarised resolved LI curves of the device. Three different current injected sections are selected to examine the polarised nearfield pattern and polarised spectrum of emission. Section A is selected at 4 mA that is about half of the threshold; Section B covers from 6.7 mA to 7.1m A that includes the threshold current of 7 mA; Section C sets from 8 mA to 11 mA where lasing modes start to show the polarisation selection. The measurement results obtained at different injected current section is shown in the following.

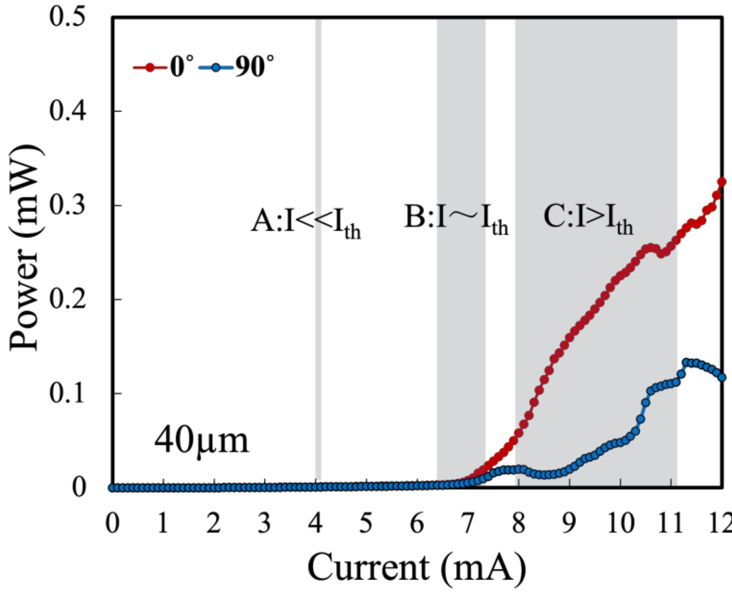


Figure 5.7 Polarisation resolved LIs of an investigated 40 μm diameter device. Section A, B and C are selected to study the polarisation property of the device.

5.5 Nearfield Pattern of 40μm VCSEL in Section A

In section A, the nearfield images of polarisation resolved spontaneous emission are presented. Figure 5.7 (a) and (b) show the 0° polarised and 90° polarised spontaneous emission nearfield images. Both of them show circular patterns correspond to the p contact and dielectric boundary of the device. However, the intensity of emission is slightly different in the centre of the images. To clarify such difference, the intensity difference is plotted in figure 5.8.

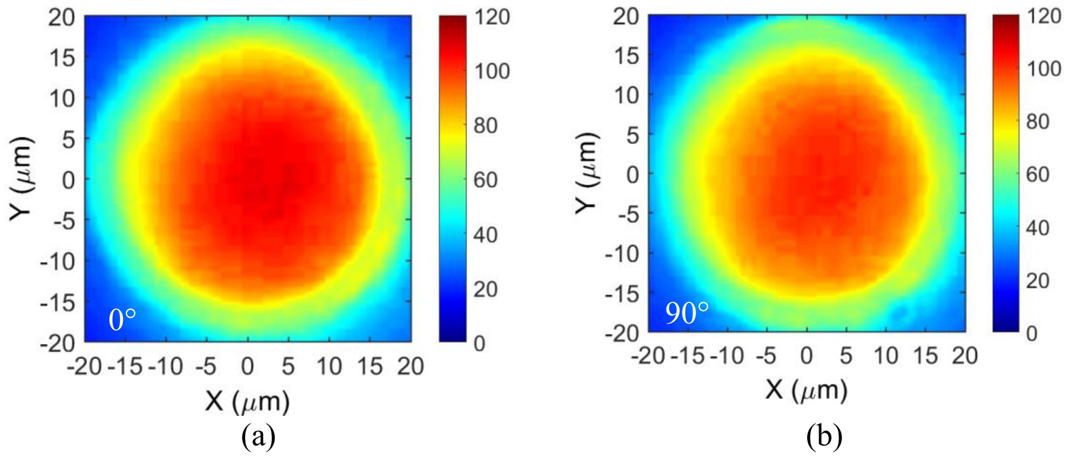


Figure 5.8 (a) 0° polarised nearfield image and (b) 90° polarised nearfield image measured at I=4 mA, ~$0.5I_{th}$.

Figure 5.8(a) reviews the spontaneous emission polarisation characteristic of 40 μm trench etched VCSEL shown above. Here selects the data on the paths of X= 0 and Y= 0 to represent the intensity difference between orthogonal polarisation states. Figure 5.8(b) shows the intensity along X=0. On this path, the intensity of 0° polarised emission is about 10unit higher than 90° polarised emission from y= -15 μm to y= 15 μm. Similar result is found on the path of Y= 0 that is shown in figure 5.8(c). The intensity difference distributes over the entire aperture.

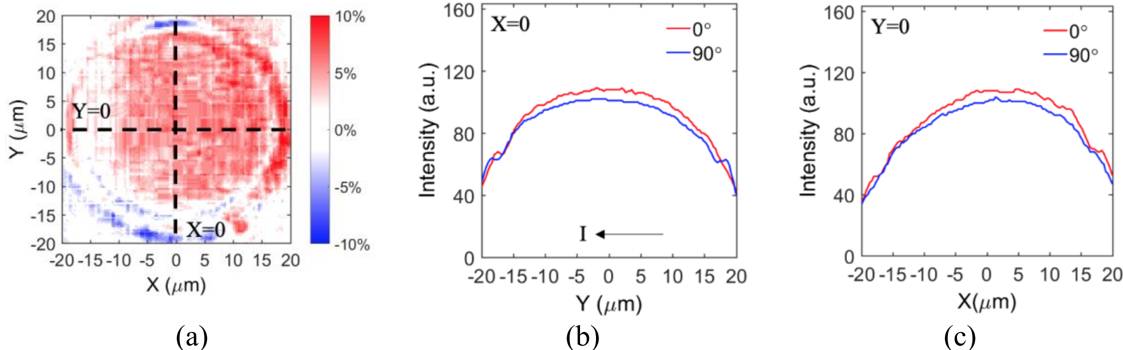


Figure 5.9 (a) 40 μm VCSEL spontaneous emission polarisation distribution obtained by compare the intensity of 0° (red) and 90° (blue) polarised nearfield images; Along X= 0 (b) and Y= 0 paths (c), the intensity level of 0° and 90° polarised emission is plotted with position.

5.5.1 Review of Frequency Splitting to Birefringence and Strain Properties

As mentioned in Chapter 1, the emission of a cylindrical cavity VCSEL contains two orthogonal polarisation states. This is due to the birefringence property of VCSEL. Prior studies reports that birefringence property performs as a frequency splitting of fundamental modes between orthogonal polarisations [95][96]. Figure 5.5 presents the results reported from one of the previous researches [95]. The histogram summarizes the frequency splitting (Δv) of 39 proton implanted VCSELs. Most of the tested devices present a frequency splitting of 10GHz and the maximum frequency splitting obtained is 19 GHz(0.06 nm). Such splitting also has been noted in other works [97][94]. It is possible that such splitting is too small to lead to modal gain difference of orthogonal polarised modes. Thus, lasing can happen at one or both orthogonal polarisation states, which causes an unstable polarisation performance of VCSELs.

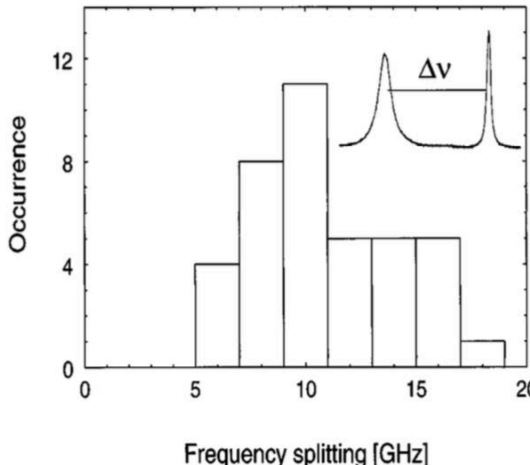


Figure 5.10 A histogram summarised frequency splitting between the fundamental modes of two orthogonal polarisation states from 39 VCSELs [94].

A number of studies have explored the relationship between birefringence and strain for VCSELs [97][98][99][100]. Experimental results presented in figure 5.6 demonstrate the influence of the external force applied by a force tip on frequency splitting of a standard single-mode oxide-confined AlGaAs-based VCSEL [98]. The findings show that the frequency splitting increases linearly with the strength of the force added. This study claims that a linear relationship can be detected when the orientation of the external strain is aligned with internal strain.

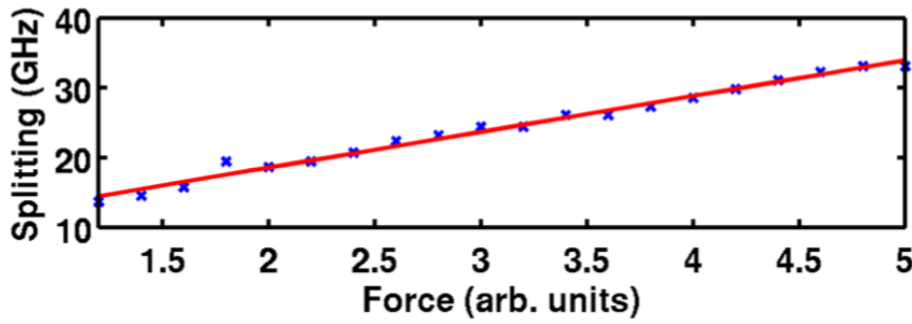


Figure 5.11 Birefringence induced mode splitting as a function of external force [98].

5.5.2 Section B – Spatial-Spectral Analysis of Lasing Modes at ~I_{th}

In section B, emission of the device is studied spectrally and spatially. At first, here illustrates measurement results of 0° polarised emission. Figure 5.11(a) presents a nearfield image of 0° polarised emission at threshold of 7 mA. Four bright spots are shown in the nearfield image and each of them has different size and intensity. Figure 5.11(b) presents a spectrum measured for 0° polarised emission at threshold of 7 mA. The spectrum is

presented with the deconvoluted results. As we can see, 8 lasing peaks are observed and 2 broad peaks are generated in the background. To observe the emission variation, spectra and nearfield images are measured from 6.7 mA to 7.1 mA with a step of 0.1 mA.

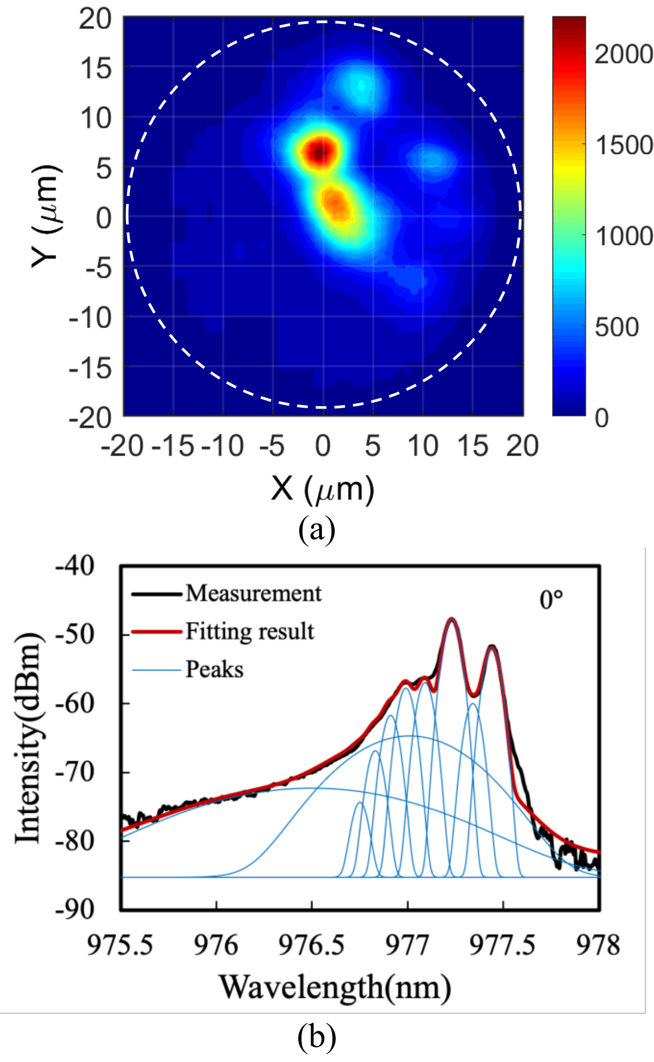


Figure 5.12(a) Nearfield image of 0° polarised emission at I_{th} of 7 mA; (b) Deconvoluted spectra of 0° polarised emission at I_{th} of 7 mA.

In terms of the spectra measured in section B, figure 5.12 presents a summary of the lasing wavelength measured from 6.7 mA to 7.1 mA at 0° polarisation state. From 6.7 mA to 6.8 mA, there is one more mode with wavelength of 976.82 nm generated at 6.8 mA but the wavelength of the rest lasing modes remain the same. As current further increasing, the wavelength of each mode floats within 0.05 nm. It suggests that the intensity change of 0° polarised emission from 6.7 mA to 7.1 mA is caused by the power variation of each mode. To find the mode position on nearfield image, the intensity variation of each modes is examined at every 0.1 mA step.

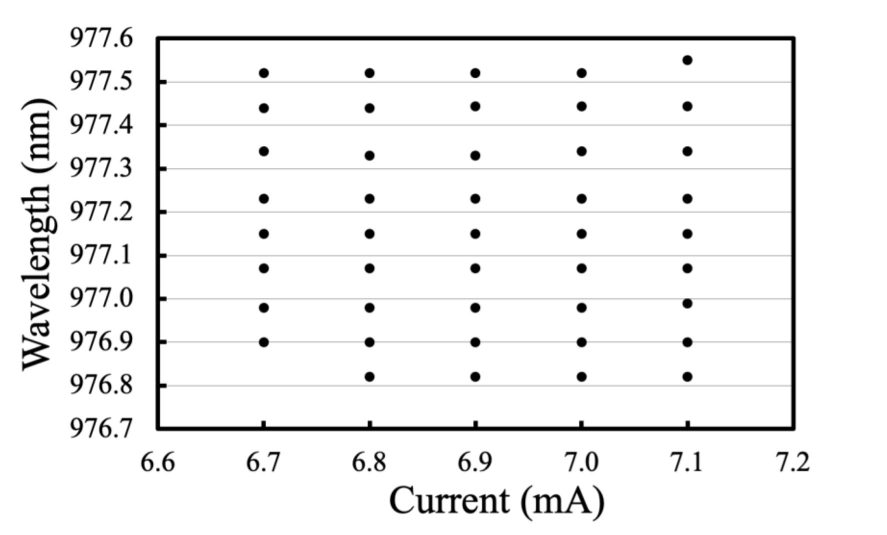


Figure 5.13 Summary of lasing modes wavelength for 0° polarised emission a from 6.7 mA to 7.1 mA.

Figure 5.13 presents a process to find mode position on the nearfield image through lasing modes intensity variations. Figure 5.13(a_1) and (a_2) presents measurement results at 6.8 mA. In the nearfield image, one bright spot is recorded, shown in figure 5.13(a_1). While 9 peaks are found in the spectrum, shown in figure 5.13(a_2). At I= 6.9 mA, the bright spot in the nearfield is enlarged and the intensity of each mode increases in different level, shown in figure 5.13(b_1) and (b_2) respectively. To examine the intensity change, figure 5.13(c_1) plots the intensity variation of nearfield images from 6.8 mA to 6.9 mA. It highlights the intensity increasing place where show two bright spots. Correspondingly, figure 5.13(c_2) plots the intensity variation of each mode from 6.8 mA to 6.9 mA in the histogram. Mode β and α shows the largest intensity variation. It is possible that two hot spots generated in the nearfield image are mode β and mode α. Thus, the locations of lasing mode β and α are found in the nearfield image.

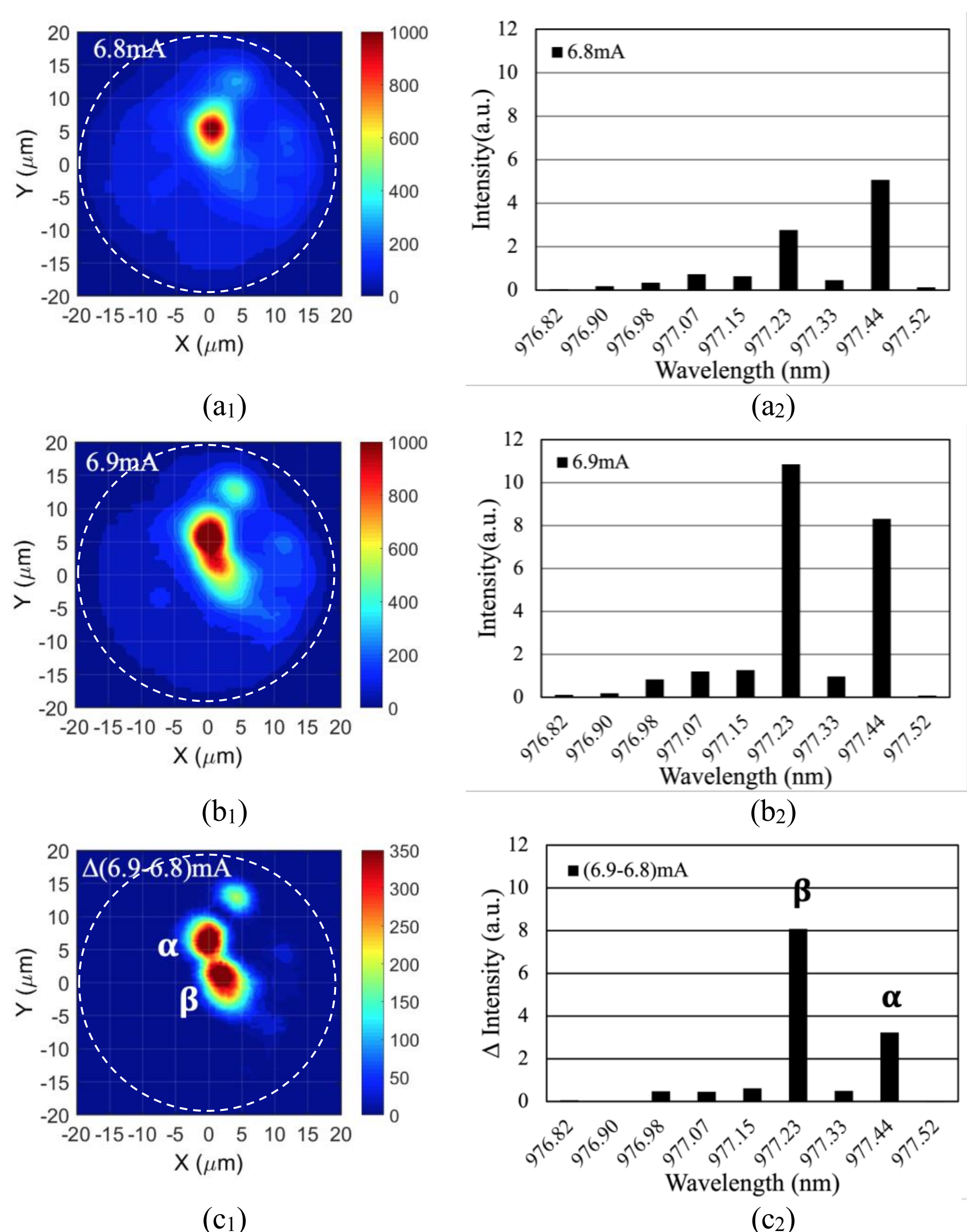


Figure 5.14 Nearfield images of 0° polarised emission at 6.8 mA (a_1), 6.9 mA (b_1) and the intensity difference of two nearfield images (c_1);histograms of lasing modes intensity at 6.8 mA(a_2), 6.9 mA (b_2) and an intensity variation of each mode between 6.8 mA and 6.9 mA(c_2).

The intensity variations of nearfield images and lasing modes are presented from 6.7 to 7.1 mA at each step. The results are shown in figure 5.14. At first, there is only one bright spot rising up from 6.7 mA to 6.8 mA that shown in figure 5.14 (a_1). Correspondingly, peak α with wavelength of 977.44 nm has the highest intensity increasing, shown in figure 5.14(a_2). Thus, this hot spot located at (0 μm,5 μm) should be mode α. Next, the intensity variation of nearfield from 6.9 mA to 6.8 mA is shown in figure 5.14(b_1). Except α, two other bright dots show up at position of (2 μm,0 μm) and (5 μm,15 μm). They could be peak β and κ at wavelength of 977.23 nm and 977.15 nm that show the same intensity increasing. Following

the same process, a new spot is found at (10 µm, 5 µm) called γ with wavelength of 976.98 nm, shown in figure 5.14(c_1) and (c_2). At last step, spots κ and β disappear in the delta nearfield images in figure 5.14(d_1) and their intensity increment shown in the histogram of figure 5.14(d_2) matches with this results. It confirms that the location of these modes are correct.

As current increases from 7.0 mA to 7.1 mA, two more bright spots are generated at position (12 µm,0 µm) and (10 µm,-7 µm) ,shown in figure 5.14(d_1). Accordingly, peaks µ and ω with wavelength of 976.90 nm and 977.07 nm have apparent intensity increasing, illustrated in figure 5.14(d_2). Therefore, the location of mode µ and mode ω is founded. In summary, by using this delta method, six lasing modes are found in the nearfield image for 0° polarised emission. To clarify their location, they have been labelled on a nearfield image measured at 7.1 mA shown in figure 5.15.

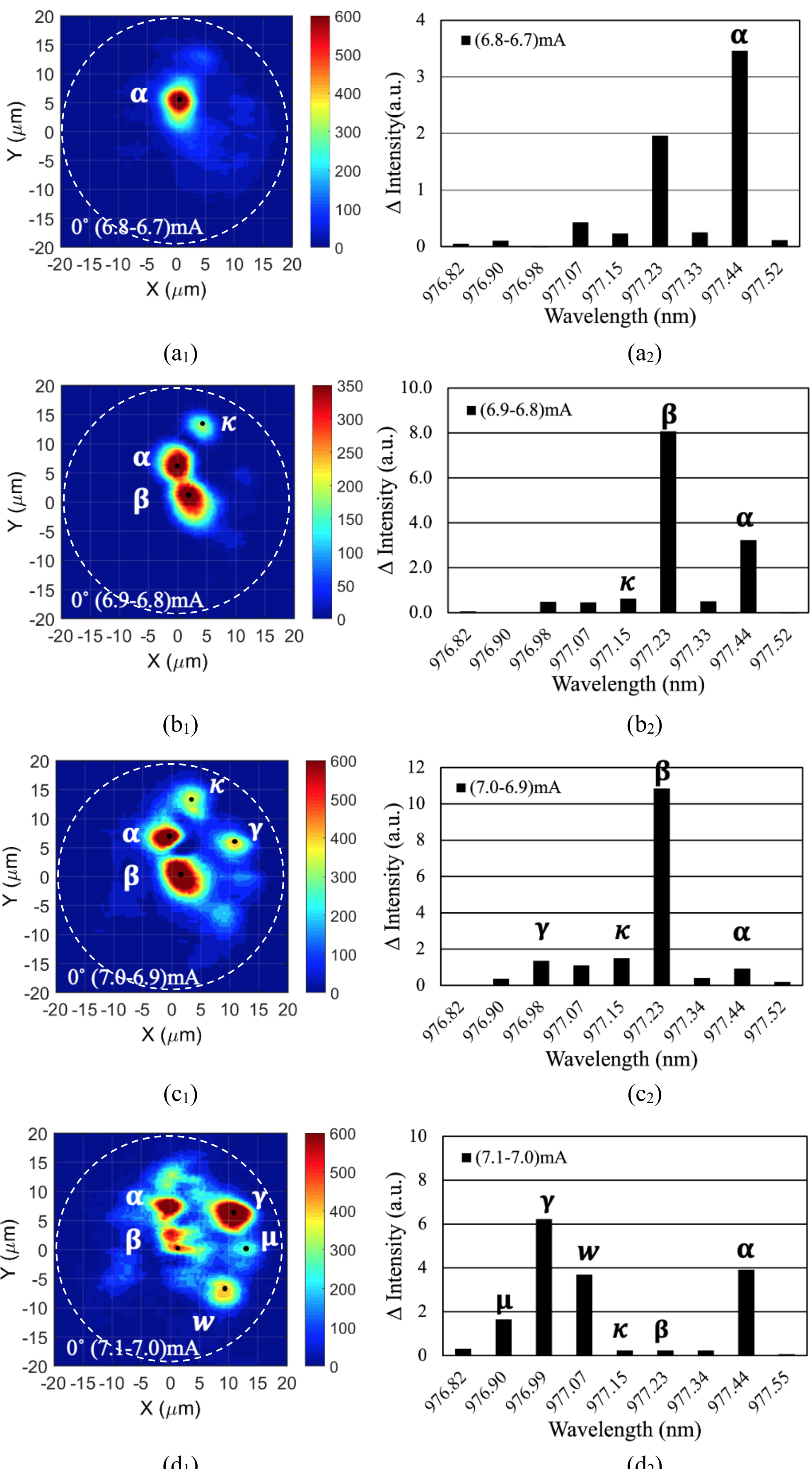


Figure 5.15 (a_1),(b_1),(c_1),(d_1) shows the nearfield intensity variation from 6.7 to 6.8 mA, 6.8 to 6.9 mA, 6.9 to 7.0 mA and 7.0 to 7.1 mA. Histograms of (a_2), (b_2), (c_2),(d_2) shows the intensity variation of each mode corresponded to the same current incremental interval for 0° polarised emission.

Figure 5.15 labels lasing modes on the 0° polarised nearfield image. As it shows, modes distribute at the right half of the current injected area. Mode α and mode β locate at the centre have higher intensity than other modes. Modes κ, γ, μ , and ω lasing at the right side have shorter wavelength than mode α and β. It suggests that mode α and β achieve large overlap with 0° polarised gain.

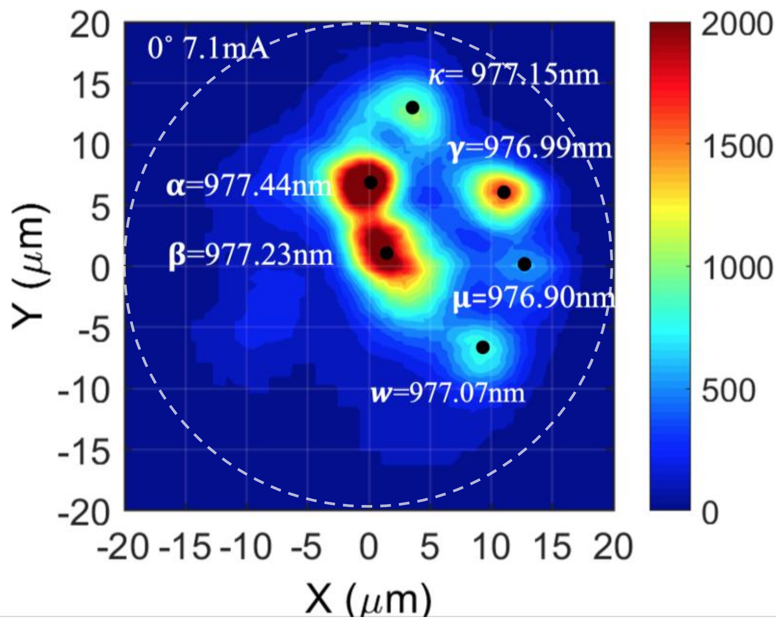


Figure 5.16 A nearfield image of 0° polarised emission measured at 7.1 mA with wavelength of identified modes labelled on it.

Analogous to the delta method used above, the intensity variation of nearfield and lasing modes for 90° polarised emission are illustrated in figure 5.16. As shown in figure 5.16(a_1), two bright regions p and q at (5 μm,12 μm) and (0 μm,5 μm) are generated at current increasing from 6.7 mA to 6.8 mA. Correspondingly, modes with wavelength of 977.45 nm and 977.29 nm have the highest intensity increasing, shown in figure 5.16(a_2). This suggests that bright spots p and q correspond to these modes. From 6.9 mA to 6.8 mA, no other bright spot is generated. At this step, peak p and q still have the most highest intensity variation than other modes shown in figure 5.16(b_2). Further increasing the current to 7.0 mA, one more bright spot, s, generated in the nearfield, shown in figure 5.16(c_1). It corresponds to peak at 977.13 nm. However, there is one peak shown in figure 5.16(c_2) that has a larger intensity variation than mode q. It is possible that this peak r is overlapped with peak p at position (5 μm,12 μm) since no other place shows such large intensity variation in the nearfield. This idea is confirmed when current increases from 7 mA to 7.1 mA. As shown in figure 5.16(d_2), peak r has the highest intensity increasing while peak p only achieves one-third of its increment. Therefore, a hole is appeared in the overlap area shown in figure

5.16(d_1) due to their uneven increasing step. From figure(d_1) and (d_2), we also can see some small peaks u, v and t at (14 μm,3 μm), (-10 μm,-5 μm) and (10 μm,-7 μm) are generated. They have the wavelength of 976.98 nm, 977.37 nm and 977.06 nm. In total, seven peaks are found for 90° polarised emission from 6.7 mA to 7.1 mA.

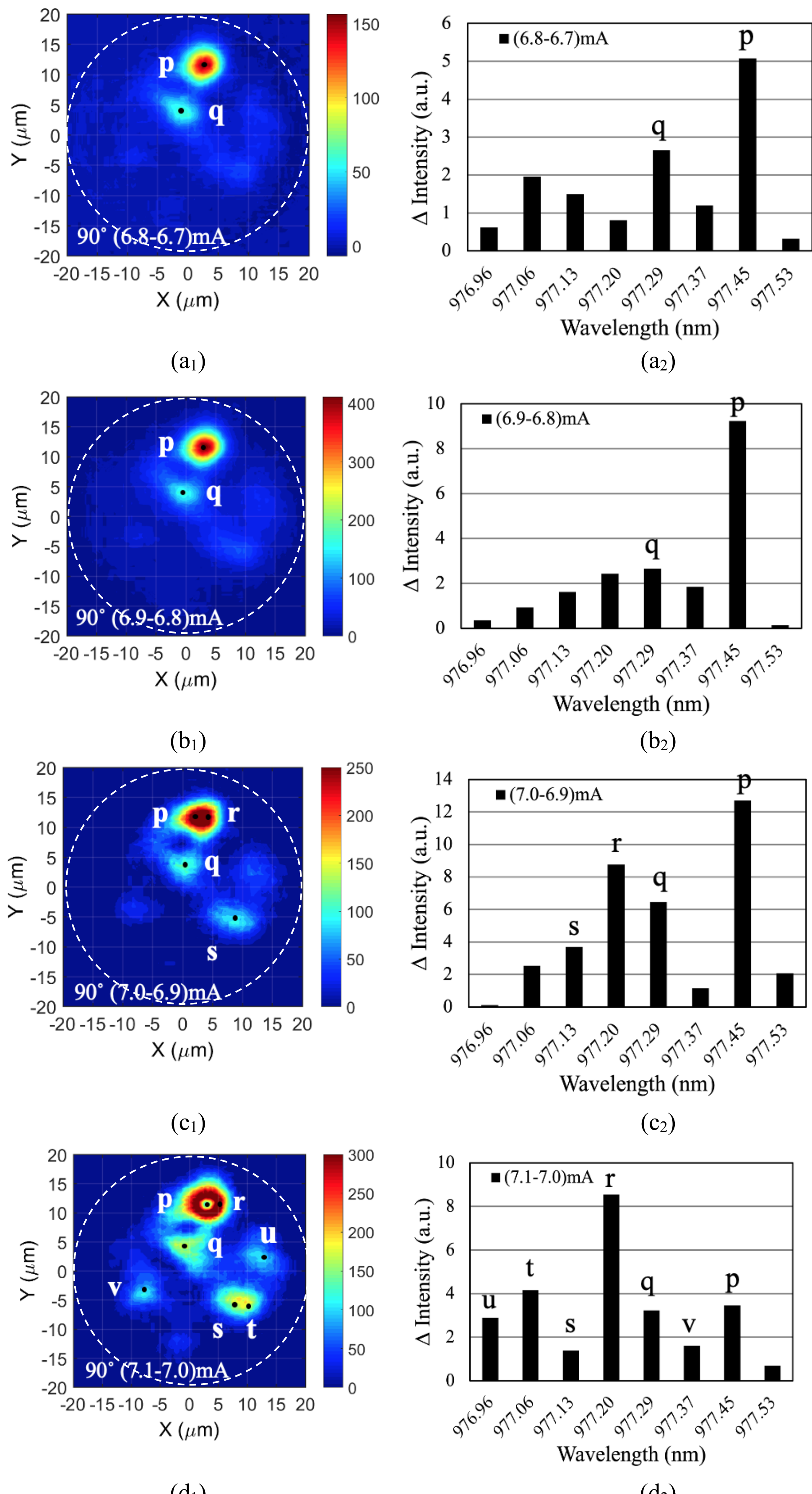


Figure 5.17 (a_1),(b_1),(c_1),(d_1) shows the nearfield intensity variation from 6.7 to 6.8 mA, 6.8 to 6.9 mA, 6.9 to 7.0 mA and 7.0 to 7.1 mA. Histograms of (a_2), (b_2), (c_2),(d_2) shows the intensity variation of each mode corresponded to the same current incremental interval for 90° polarised emission.

A summary of the 90° polarised lasing modes is presented in figure 5.17. The modes positions are labelled on the nearfield image measured at 7.1 mA. Peak p and r that generated at the top half of the aperture have the highest lasing intensity. Peak, q, u, v, s, t, distribute around the centre of aperture. For 90° polarised emission, the modes generated at the top half of aperture obtain higher modal gain and therefore show larger intensity. This result is different with that found in 0° polarised emission.

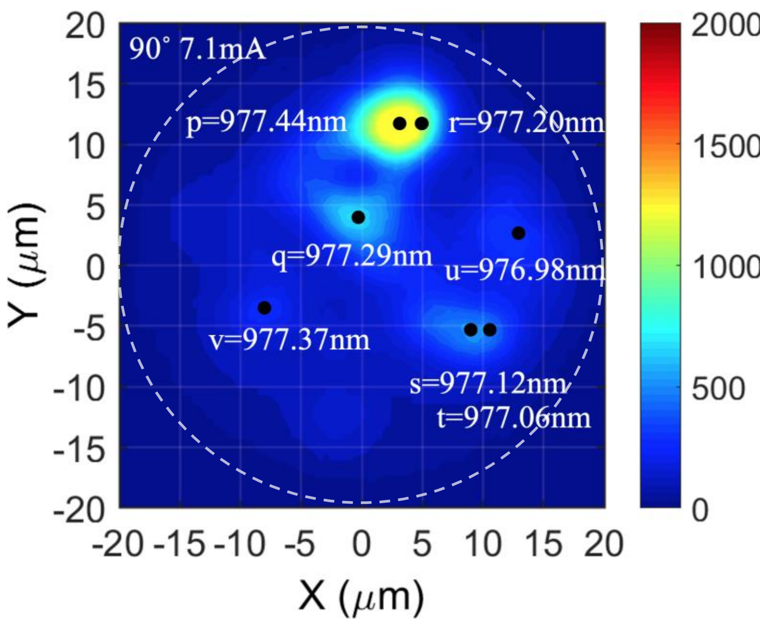


Figure 5.18 A nearfield image of 90° polarised emission measured at 7.1 mA with wavelength of identified modes labelled on it.

I now compare the lasing pattern of 0° and 90° polarised emission. Figure 5.18 presents the pattern of 0° polarised emission at intensity of 1000 on the 90° polarised nearfield image of 7.1 mA. The overlapped modes are marked by purple dots with the wavelength difference labelled at the side. 0° polarised emission has the highest lasing peak at the centre while 90° polarised emission has the highest lasing peak at the top edge. By considering the wavelength difference, of orthogonal polarised modes generated at the same place, they have a splitting of 0.15 nm at the centre of the device. This splitting gradually decreases to 0.05 nm for modes overlapping at the edge of the device. Previous studies noted that the frequency splitting is proportional to the strain strength [98]. Thus, the results reveals that the strain generated at the centre of the aperture is higher than the strain generated at the edge. It indicates that there is an anisotropic strain distribution of these trench etched 40 μm diameter VCSELs. The spontaneous emission measurements in Section A did not indicate such a distribution, rather suggested a uniform polarised emission intensity (strain) difference.

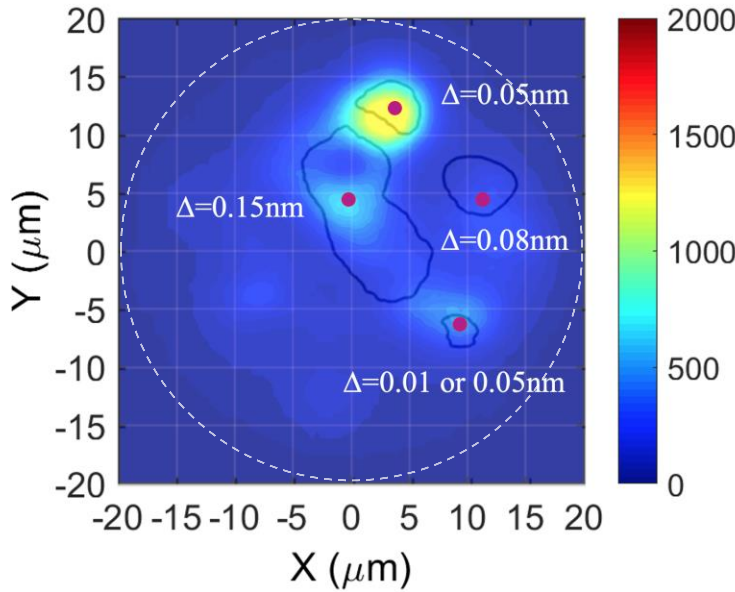


Figure 5.19 Outline of 0° polarised emission pattern at intensity of 1000 plotted on the nearfield image of 90° polarised emission. Both nearfield images are measured at 7.1 mA. The wavelength difference of the overlapped modes are labelled on it.

5.5.3 Section C – Polarised Emission Characteristics of Lasing Emission>I_{th}

Nearfield images and polarised spectra of emissions are also examined for lasing emission at much higher currents than the lasing threshold. Figure 5.19 presents the nearfield images of 0° and 90° polarised emission at I=8 mA. The lasing pattern is distributed discretely for both polarisation states. However, there are more modes generated in the 0° polarisation state. The position difference of lasing modes between two polarisation states is clarified by an overlap image shown in figure 5.19(c). In this figure, I plot the 90° polarised nearfield image of the device along with a contour plot from the 0° polarised nearfield image. The plotted contour corresponds to an intensity equal to 150, around 50% of the maximum intensity in that image. This "overlap" figure shows that modes belonging to different polarisation states are generally separated spatially.

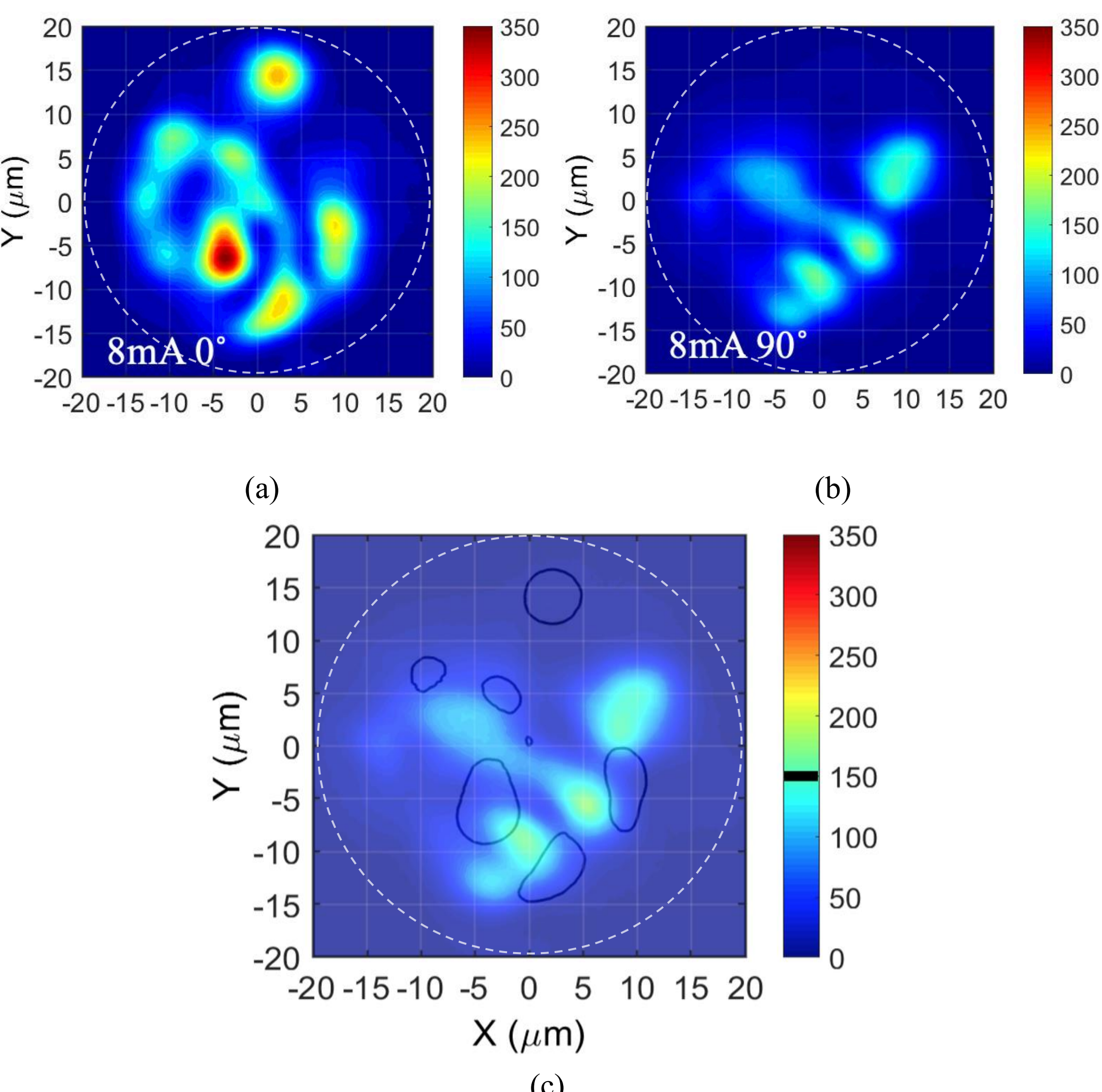


Figure 5.20 Nearfield images measured at I=8 mA: (a) 0° polarised emission ; (b) 90° polarised emission; (c) Outline of 0° polarised emission pattern at intensity of 150 plotted on 90° polarised nearfield image.

The spectrum of the 0° polarised emission at I=8 mA is presented in figure 5.20. More than 9 spatial modes were present on this polarised nearfield image. For the spectrum, there are only 8 lasing modes deconvoluted from the spectrum at the condition of our maximum resolution of 0.08 nm. The number of modes does not match between nearfield image and spectrum. It is possible that some of the lasing modes have wavelength difference less than the resolution. Thus, they have not been observed by this OSA. A more precise spectrum measurement equipment maybe needed to analyse this complex lasing condition.

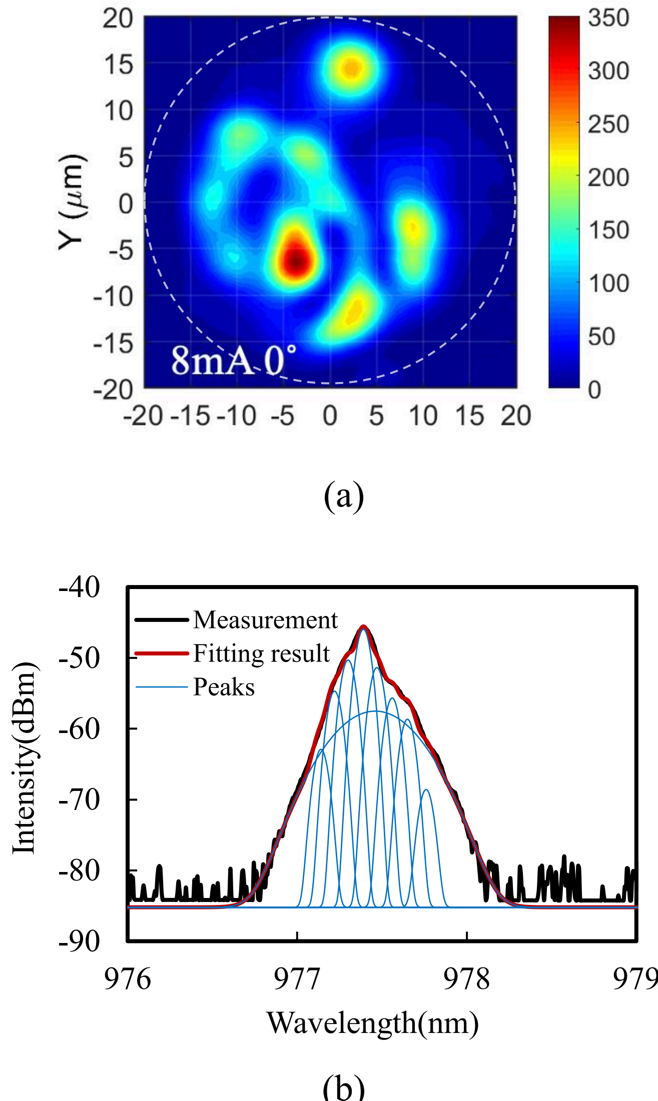


Figure 5.21 (a) Nearfield image of 0° polarised emission at I=8 mA; (b) Spectrum of 0° polarised emission at I=8 mA.

Figure 5.21 presents spectra of 0° and 90° polarised emission measured at I=8 mA. The spectrum amplitude of 0° polarised emission is about -45 dBm, while it is -55 dBm for 90° polarised spectrum. There is a 10 dBm difference of amplitude between two spectra.

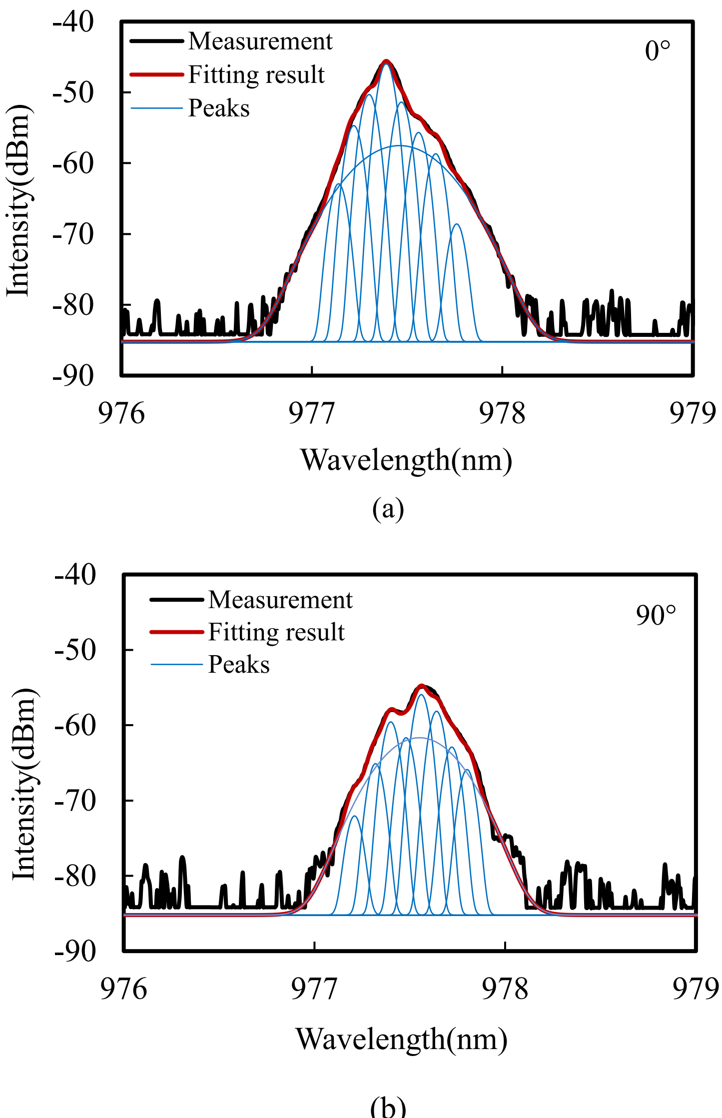


Figure 5.22 Spectra of 0° and 90°polarised emission measured at I=8 mA, shown with deconvoluted results.

Further increases the injected current to 9 mA. Figure 5.22 presents the nearfield pattern of two polarisation states. 0° polarised emission has a denser modes pattern than 90° polarised emission. A clear position selection can be observed from overlap images shown in figure 5.22(c).

The pattern of the 0°polarised nearfield pattern changes significantly in position with 1 mA current increment. Such large current leads to a large discrepancy of the nearfield patterns, which prohibits the tracking of individual mode as a function of injected current as was performed in section B. If this tracking is required in future tests, then much smaller current steps will be required.

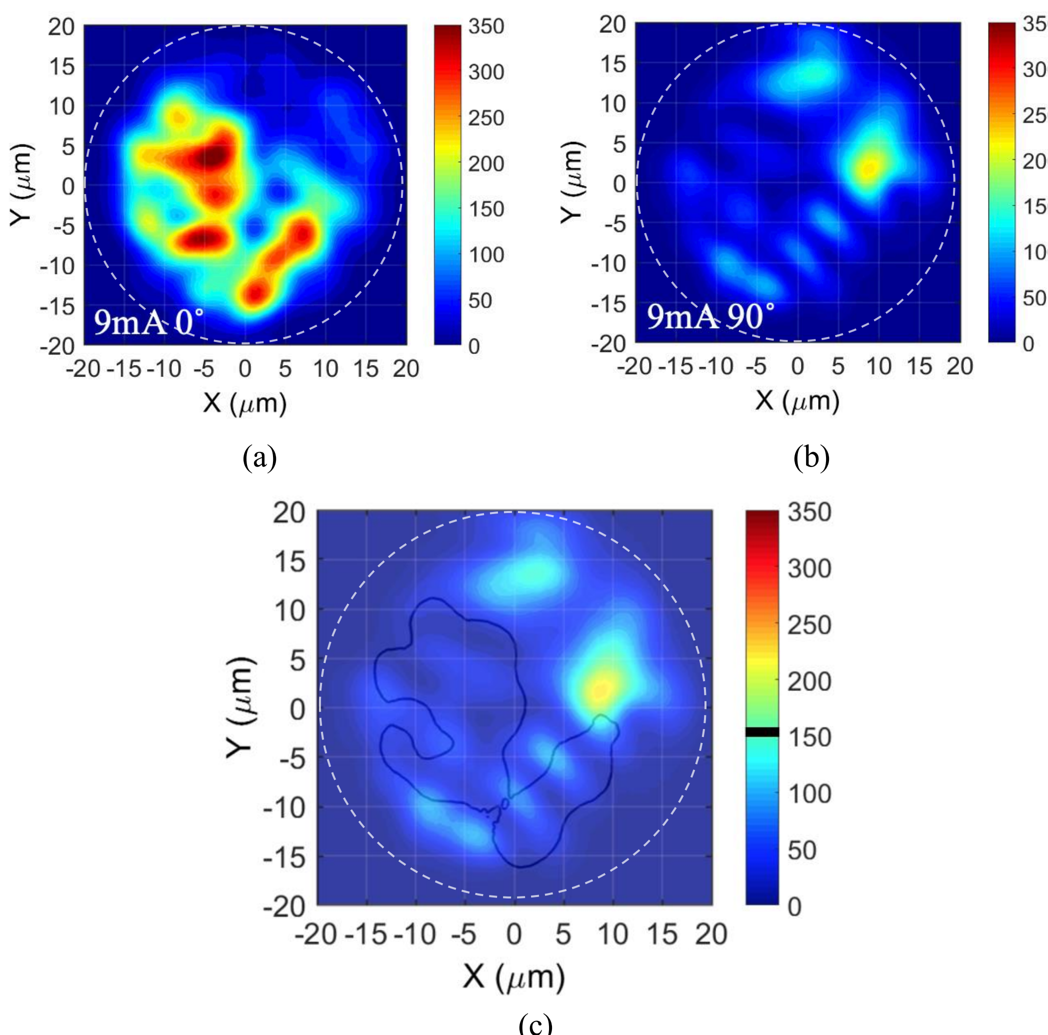


Figure 5.23 Nearfield images measured at I= 9 mA: (a) 0° polarised emission ; (b) 90° polarised emission; (c) Outline of 0° polarised emission pattern on 90° polarised nearfield image.

The spectra of device measured at I= 9mA is shown in figure 5.23. Firstly, a 10 dBm amplitude difference is observed between two polarisation states. Secondly, 0° polarised emission contains 8 lasing peaks, while 90° polarised emission only contains 7 peaks. It indicates that the number of lasing modes begins to show difference in orthogonal polarisation states.

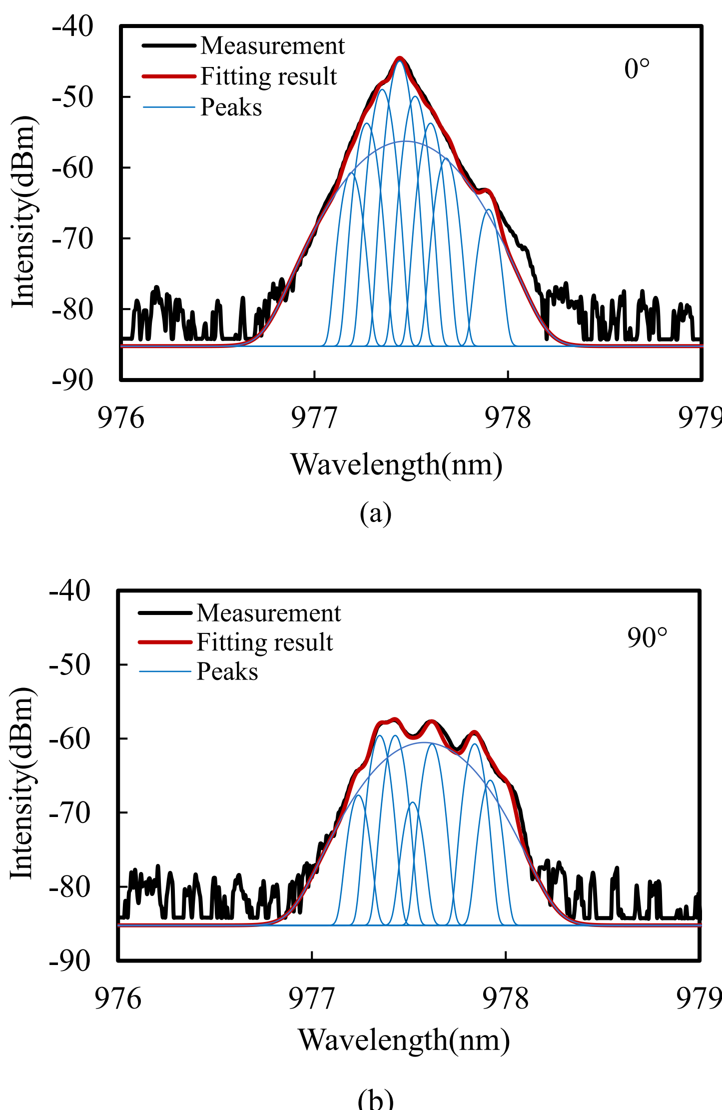


Figure 5.24 Spectra of 0° and 90°polarised emission measured at I=9 mA, shown with deconvoluted results.

When the current increases to 10 mA, the nearfield pattern of 0° polarised emission becomes even broader and more intense (shown in figure 5.24(a)). While 90° polarised emission has a simple profile , only one brightest hot spot located at (0 μm,15 μm) is found on figure 5.24(b). The overlap image shown in figure 5.24(c) again illustrates a distinct position difference of lasing modes between two polarisations.

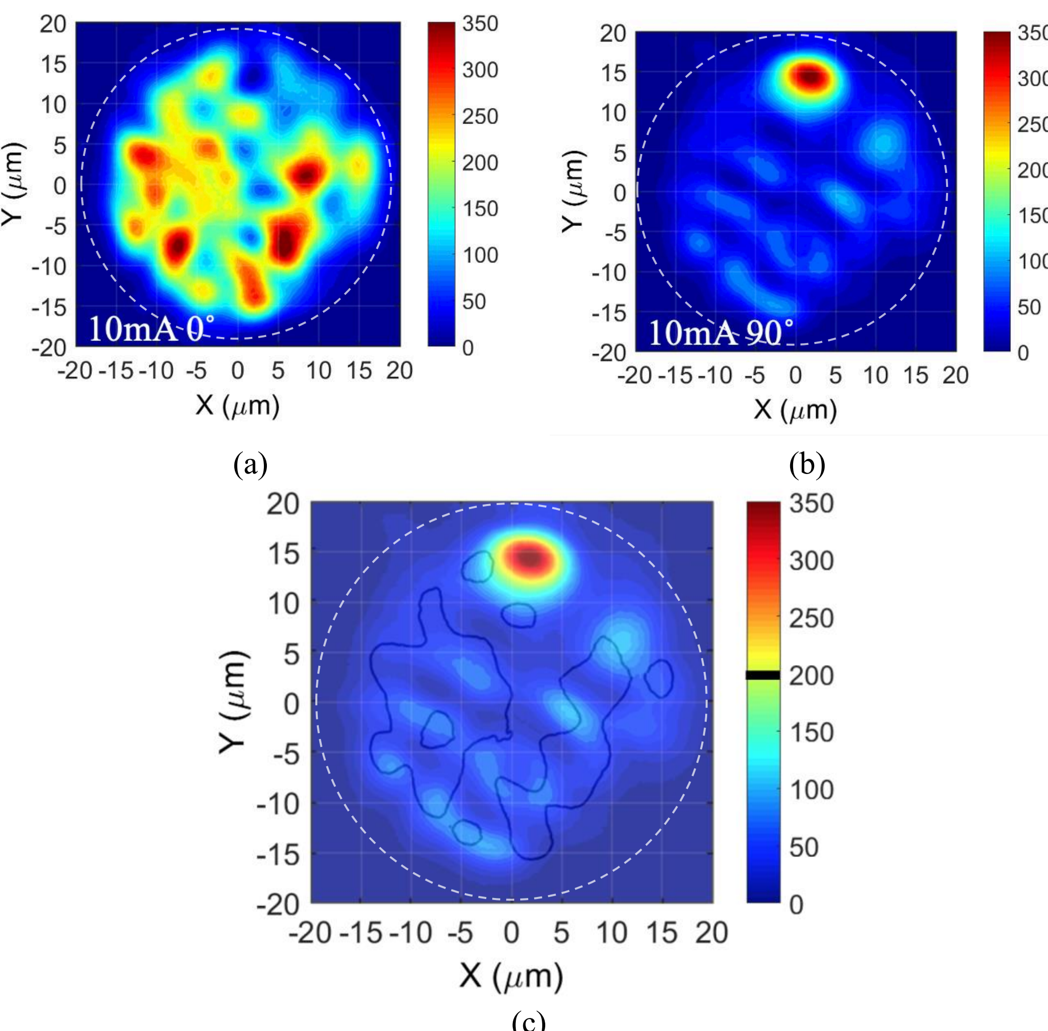


Figure 5.25 Nearfield images measured at I=10 mA: (a) 0° polarised emission ; (b) 90° polarised emission; (c) Outline of 0° polarised emission pattern on 90° polarised nearfield image.

The spectra measured at I=10 mA are presented in figure 5.25. The spectrum of 0° polarised emission is 10 dBm higher than it of 90° polarised emission. No difference in the number of modes is found from the deconvoluted spectra.

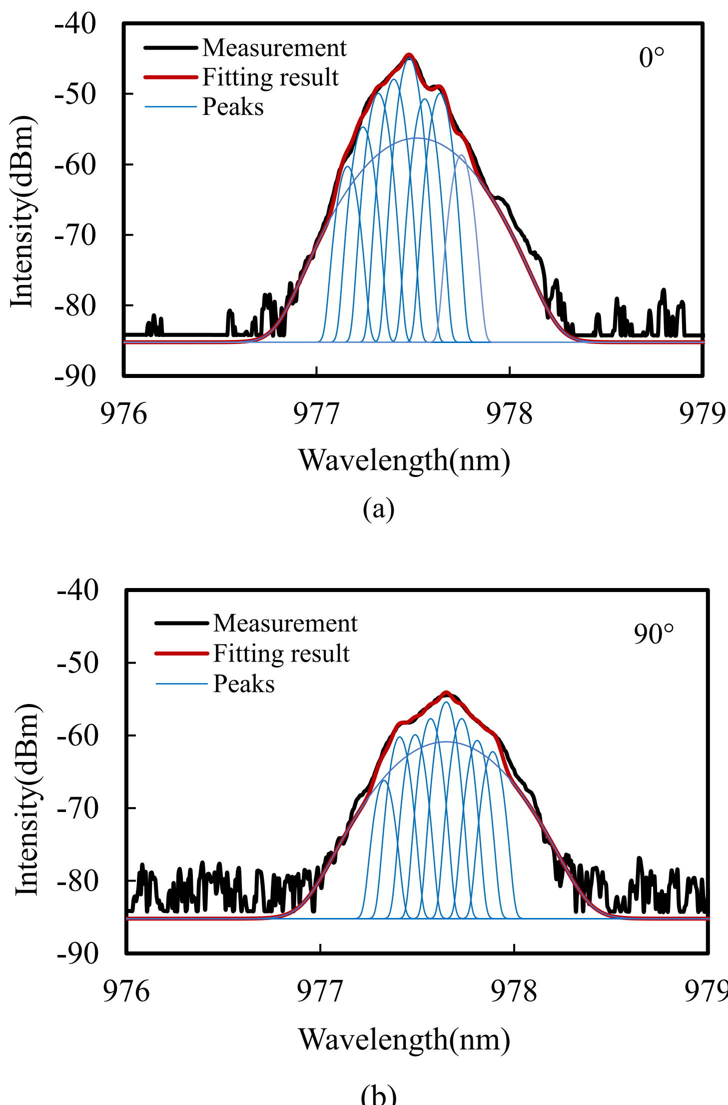


Figure 5.26 Spectra of 0° and 90°polarised emission measured at I=10 mA, shown with deconvoluted results.

Nearfield images measured at I=11 mA are presented in figure 5.26. For 0° polarised emission, the intensity of the lasing emission distributed all over the aperture except one dot at left top. For 90° polarised emission, the bright lasing spot right at this dot. It indicates that there is a lasing mode competition in the area. From the overlap image shown at figure 5.26(c), we can see again that in general the polarised modes lase in spatially separate areas, except for some competition at (0 to 15 μm, -15 to 0 μm). This may indicate that at higher currents, spatial hole burning of gain may occur for the dominant polarisation mode, allowing lasing from the “weaker” polarisation state whilst the gain recovers.

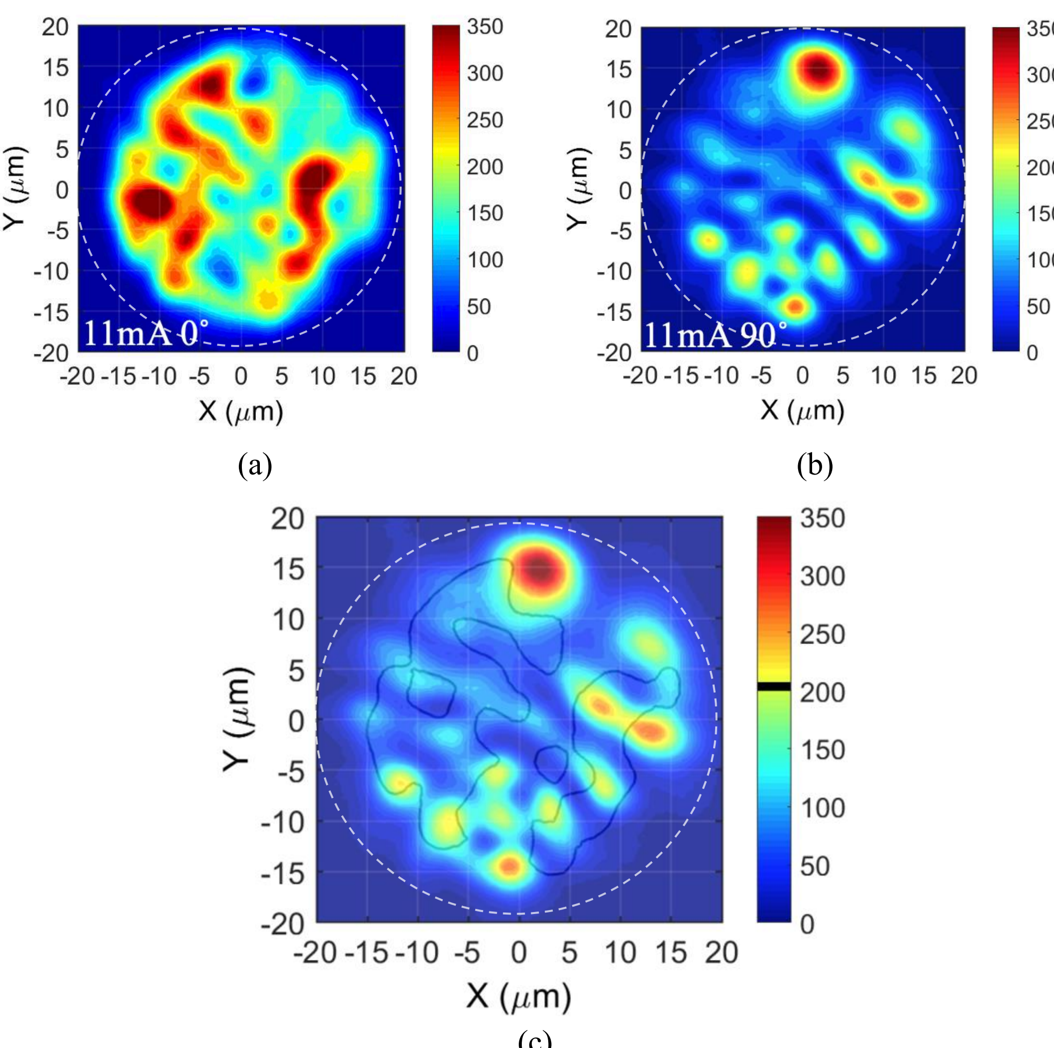


Figure 5.27 Nearfield images measured at I=11 mA: (a) 0° polarised emission ; (b) 90° polarised emission; (c) Outline of 0° polarised emission pattern on 90° polarised nearfield image.

The spectra at I=11 mA presented in figure 5.27. The modes lasing in 90° polarisation states distribute more discretely than 0° polarised emission. However, there are more numbers of modes generated along 0° polarisation states. Modes generated with electric field along 0° have higher emission intensity and a larger mode number.

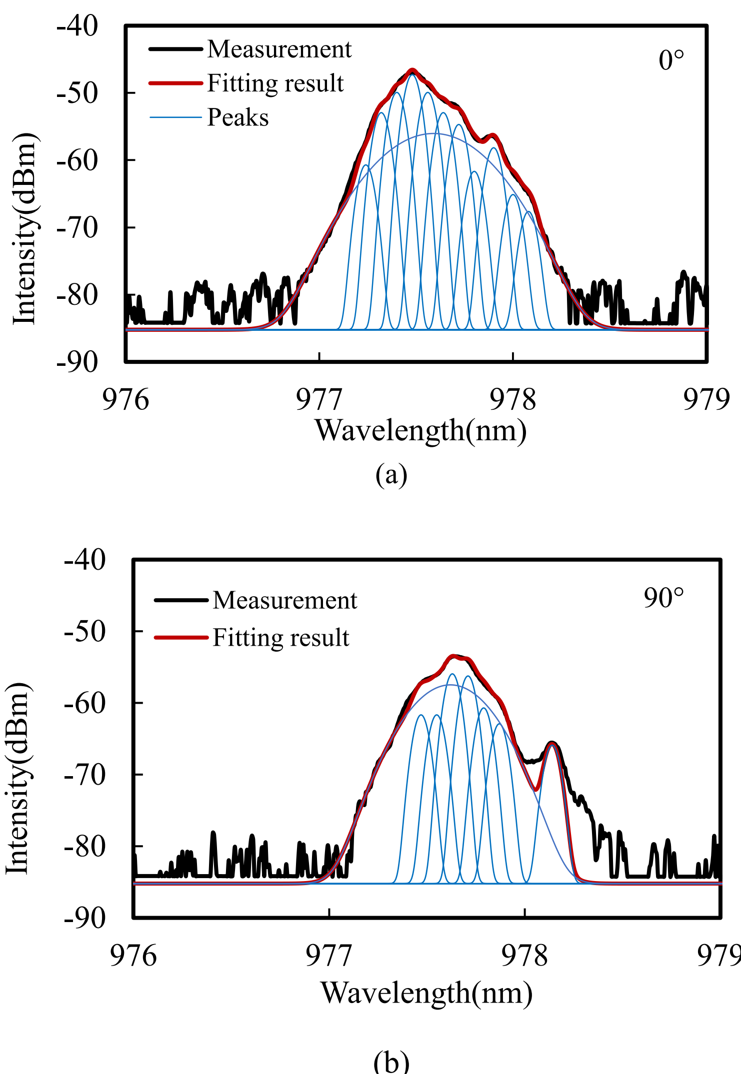


Figure 5.28 Spectra of 0° and 90°polarised emission measured at I=11mA, shown with deconvoluted results.

To summarise this section, above lasing threshold, the nearfield pattern generally shows spatial difference between the two polarisation states. This prevents the use of spectral splitting to map strain as was performed ~I_{th} in section B. As for the emission spectra, the amplitude has a ~10 dB difference. Due to the limited equipment resolution, the number of modes deconvoluted from the measured spectra lacks accuracy to identify and track individual modes. Also, the current step of measurement needs to be reduced in order to conduct lasing mode tracking.

Whilst the individual modes could not be identified and tracked, nor spatially mapped, we are able to compare the central position of the envelope of modes. Figure 5.28 summaries the wavelength splitting for the two polarisations of the highest intensity modes as a function of injected current. We can assume that this wavelength splitting is proportional to the gain shift of orthogonal polarisation states. As it shows, the splitting varies between 0.15 nm to

0.2 nm as the injected current increases from 7 mA to 11 mA. The error bar for this measurement is difficult to assess as there is uncertainty as to which mode is being identified in each data point. If we use the system resolution of 0.08 nm, then this result reveals the gain distribution difference of orthogonal polarisation states is constant at ~0.15 nm over these currents.

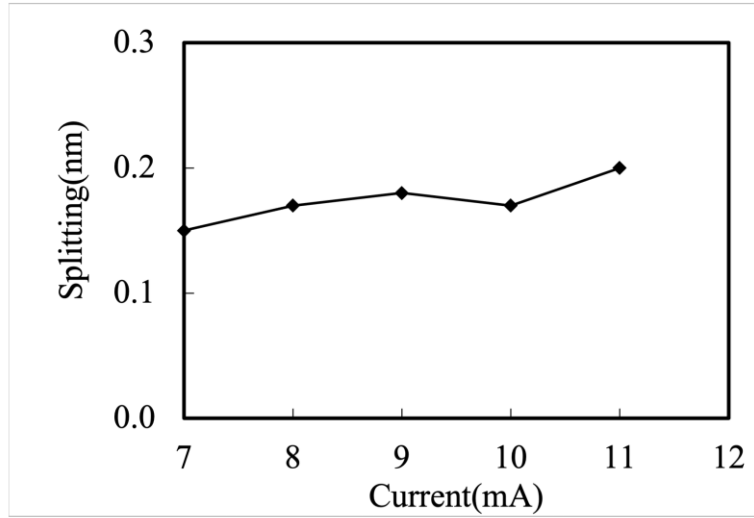


Figure 5.29 Wavelength splitting of the highest intensity lasing mode as a function of injected current.

5.6 Conclusion

In summary, the investigation of polarisation characteristics of trench-etched VCSELs has been carried out over a range of currents. At around half threshold, it was found that, for 30 μm and 40 μm devices, the 0° polarised spontaneous emissions has a higher intensity than the 90° polarisation, and that this difference is roughly uniform across the device area. These measurements suggest that the effect induced by trenches is stronger for 30 μm and 40 μm devices.

At around the lasing threshold, an investigation of frequency splitting of a 40 μm diameter device is carried out. Careful observation of the lasing modes location and the emission spectrum allows the identification of lasing modes spatially and spectrally. Some lasing modes belonging to different polarisation states have been found to be overlapped in space. If the wavelength difference of these overlapped modes is assumed to be proportional to the strain, it is possible that the strain generated at the centre of the mesa is higher than that at the edge.

At much higher currents above lasing (~1.6I_{th}), the emission pattern of orthogonal polarisation states is observed to be generally spatially separated from each other. The

complex lasing pattern and large current interval used during measurement prohibits us to identify the position of individual lasing mode. However, a clear difference between orthogonal polarisations was observed in terms of spatial distribution of the modes. From the spectra, we can see a ~10 dBm amplitude difference between the dominant polarisation state (0°) emission and the emission of the orthogonal polarisation states. It supports the assumption that the gain is different for orthogonal polarisation states.

5.7 Future Work

The spontaneous emission polarisation strength distribution does not explain the spatial lasing patterns. Rather than relying on intensity alone, a spectrally sensitive measurement may be required. Furthermore, in checking to see if we can correlate polarisation of the SE with OPSR it may be necessary to measure and correlate many devices. This would be mode possible by test automation.

Since in section B and C, there is a difference of spatial lasing patterns between orthogonal polarisation states, we should check the polarised lasing output as a function of pumping area. Figure 5.28 presents a diagram of possible device with three separated contact sections. Such a design may allow a reduction of current density in regions with undesirable polarisation, therefore enhancing the OPSR of the device.

In the future work, a more sophisticated spectral measurement set-up, possibly utilise an etalon within the optical path of the imaging system is required. It provides a condition that the spontaneous and lasing emission can be inspected through its spectra and nearfield simultaneously. Thus the birefringence property of device can be mapped by specific lasing wavelength splitting of orthogonal polarised emission.

In future work, to maximise OPSR, these spectroscopic techniques may be utilised to understand the limits to device size, and possibly engineer new solutions such as spatially varying the electrically driven area of the VCSEL.

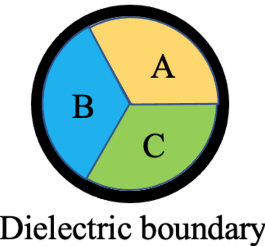


Figure 5.30 A diagram of a VCSEL device with a circular contact that consists of three equal sections A, B and C.

Chapter 6

Fabrication process improvements

In this chapter, improvements made to the fabrication process are discussed. The first section introduces a method to simplify etching modules. The second section describes the difficulties of cleaning dielectric residuals and proposes a solution to deal with it. In the final section, the necessary of adding CTLM structures on the new mask is explained.

6.1 Hard Mask Replacement

A hard mask – a layer of SiO_2 deposited on the sample surface—was applied in the initial fabrication process (as discussed in section 2.5). This layer suffers less mask erosion at the dry-etch step, with a high selectivity of SiO_2 to GaAs material (1:16). Even this process delivers an excellent performance, it has a prominent disadvantage that it consists of many steps in fabrication. Therefore, an alternative method is discussed to replace hard mask in etching process.

First, a review of hard mask etching process is presented in figure 6.1. As it shows, the process comprises five steps: hard mask deposition, optical lithography, hard mask etching, sample etching and hard mask removal. A layer of SiO_2 is deposited on the sample surface serves as a hard mask layer. In order to transfer a pattern into the hard mask, a step of optical lithography and a step of SiO_2 etching are carried out. The desired pattern is etched into the GaAs material by using this hard mask in the following step. The whole etching process is ended by a hard mask removal operation. As we can see, this process involves deposition, optical lithography and dry-etch. For a single etching module, it is relatively complicated. Also, this hard mask has been used twice in the fabrication process. The length of this procedure significantly affects the entire VCSEL fabrication process.

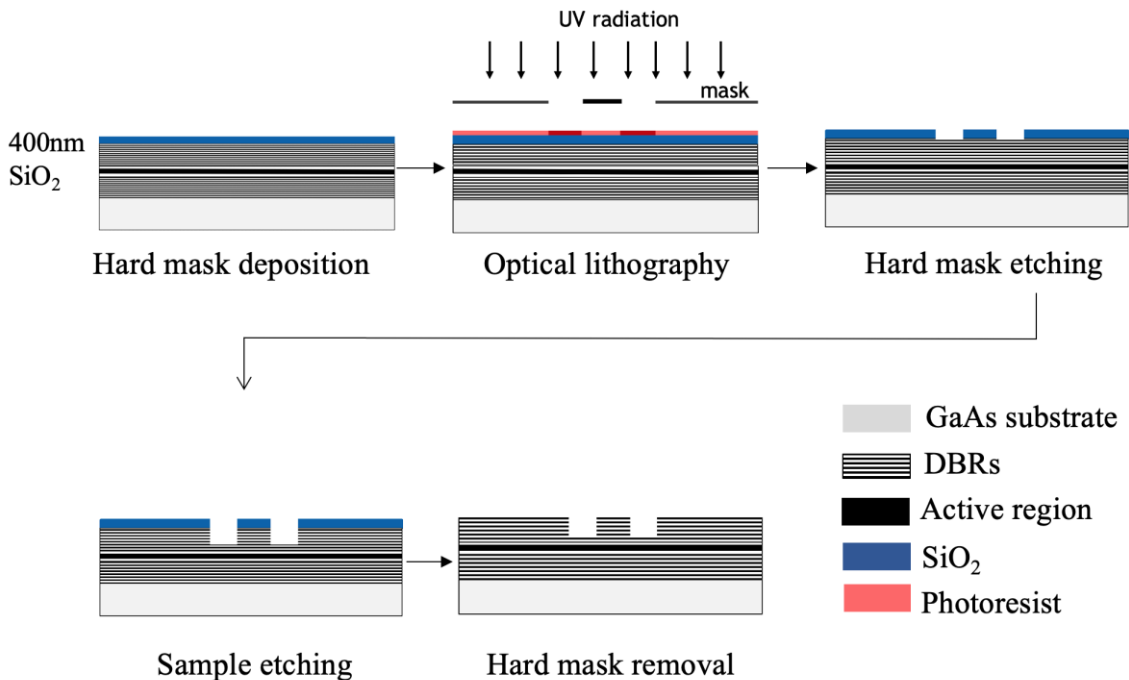


Figure 6.1 A schematic of the sample cross-section when utilizing a hard mask to deliver a pattern. Five steps including hard mask deposition, optical lithography, hard mask etching, sample etching and hard mask removal.

Alternatively, a thick photoresist layer can be investigated as an etching mask. However, the etching profile should be comparable with it achieved by using hard mask. Figure 6.2 shows schematic of etching process by using a photoresist mask. It encompasses only two steps: optical lithography and material etching. However, in this case, photoresist has to satisfy two requirements. First, the photoresist layer must be thick enough to compensate for the rapid mask erosion from the GaAs etching process. Second, the pattern delivered by the photoresist must be comparable with the profile achieved by using hard mask. The following presents an investigation process.

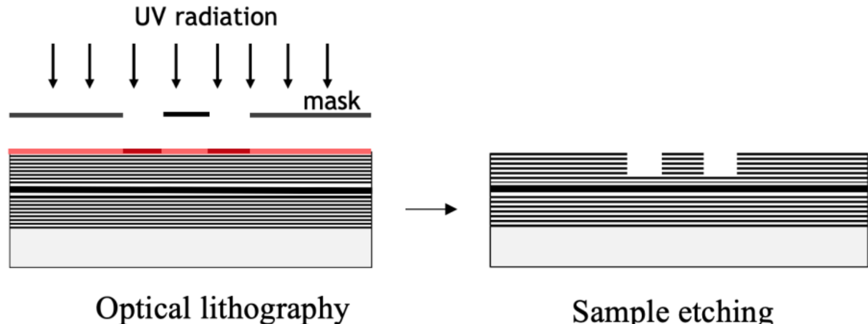


Figure 6.2 A diagram f the cross-sections of the sample when utilizing a photoresist mask to deliver a pattern.

A photoresist called SPR220 has been investigated to accomplish these task. It has a wide range of thickness variation, from 1 μm to 10 μm by changing the spinning speed from 1500

rpm to 6000 rpm [101]. Also, a preliminary study presents a GaAs etching process with SPR220 [102]. Therefore, here selects SPR220 photoresist as a candidate to replace the hard mask.

In this etching profile investigation, a stripe pattern was used. This strip pattern can be easily examined by cleaving. The examination is carried out on a piece of VCSEL wafer, which ensures that the result is repeatable in the fabrication process. The investigation including two parts. The first part discusses the optical lithography process of SPR220 photoresist. The second part illustrates the etching profile. All the results are supported with optical microscope images or SEM images.

Optical lithography:

A 7 µm thick layer of SPR220 is spun onto the sample at a speed of 3500 rpm. The sample is then baked on a hot plate for 90 s. Since this is a thick photoresist layer, it requires 1 hour rehydrate time before it proceeds to photoresist exposure step. This operation avoids the photoresist layer having corrugations. Following, the sample is exposed to UV light for 22 s and developed in CD26 developer for 90 s. An optical microscope image of it is presented in figure 6.3. As it shows, the stripe pattern has distinct edges and the photoresist layer is smooth. Compared with regular optical lithography process, SPR220 takes longer time to prepare. However, it constructs a desired clear pattern.

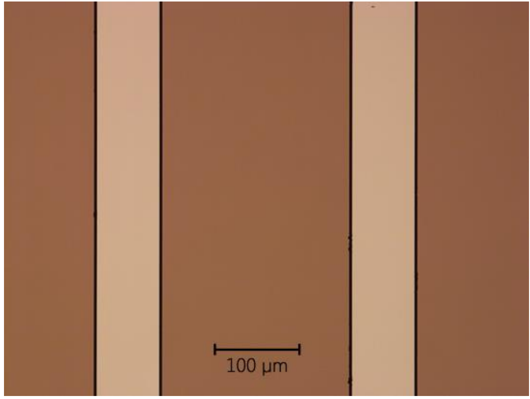


Figure 6.3 An optical microscope image of the strip pattern formed by SPR220-7 photoresist. The strip is 70 µm wide and 200 µm separated from each other.

Moreover, the thickness of the photoresist layer examined by SEM image. The result is shown in figure 6.4. It shows that the thickness of the photoresist layer is approximately 7.05 µm and the slope of the sidewall is 68.5°. The multilayer structure seen in the SEM is the epilayers grown on VCSEL sample. It achieves the target thickness of 7 µm.

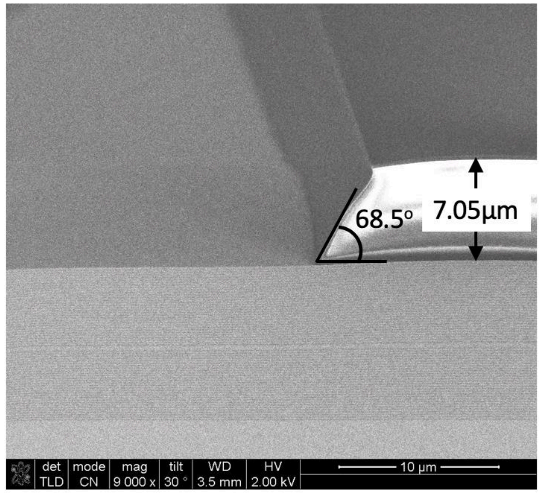


Figure 6.4 SEM image of sample cross-section with 7.05 μm SPR220-7 photoresist layer covers on top. A 68.5°slope is achieved by the photoresist sidewall.

The step sequence of the optical lithography process is summarized below:

6. Pre-bake the sample in 120 ºC oven for 5 mins.
7. Spin SPR220-7 photoresist at a speed of 3500rpm for 30 s.
8. Bake the sample on a hot plate at 115 ºC for 90 s.
9. Store sample in a humility 40-50% environment for 1hour to rehydrate photoresist.
10. Expose sample for 22 s.
11. Store sample in a humility 40-50% environment for 1 hour to rehydrate photoresist.
12. Bake sample on a hot plate at 120 ºC for 90 s.
13. Cool the sample at room temperature for 20 mins.
14. Develop the sample in CD26 for 90 s.

Sample etching:

To etch the sample, here selects dry etching equipment ICP180. The recipe used during etching process is reported in prior studies [69]. It presents smooth etch surface. The parameters of this recipe are presented in Table 6.1. As it shows, the reactive gases used are are Cl_2/BCl_3 /Ar_2/N_2. For these components, gas Cl_2 and BCl_3 provide the Cl^- ions to react with the target materials [103]. The gas Ar_2 controls the etching rate and enhance the thermal property of the discharges [69] and gas N_2 is used to keep the sample cool. In order to achieve a high concentration of ions, the pressure is controlled at 5 mT. The etching rate of this recipe at RF power of 500/50 W. is about 1600 nm per minute. The etching profile is presented in the following.

Parameter	Value
Gas flow : Cl_2/BCl_3 /Ar_2/N_2	10/10/10/7 sccm
RF Power of ICP/Platen	500/50 W
Pressure	5 mT
Temperature	10 °C
Etching rate for GaAs/AlGaAs	About 1600 nm/min

Table 6.1 ICP180 process parameters for etching GaAs/AlGaAs.

The SEM image of the etching profile is presented in figure 6.5. As it shows, 5.6 μm photoresist remains on the sample and 4.8 μm of GaAs/AlGaAs material is etched off. 1.47 μm photoresist is consumed during etching process. The etching selectivity of the SPR220 to GaAs/AlGaAs is about 1:3.3 in this case. As figure 6.5 shows, a steep sidewall with an angle of 85°. For optical devices, a sharp and smooth sidewall can reduce the optical loss such as light scattering happening in the device [104][105]. In addition, a sharp sidewall reduces the exposure area at the side and thus less the surface recombination occurred. This sharp angle is comparable with the result shown in figure 2.22 by using hard mask. It is only about 4° tilted than that.

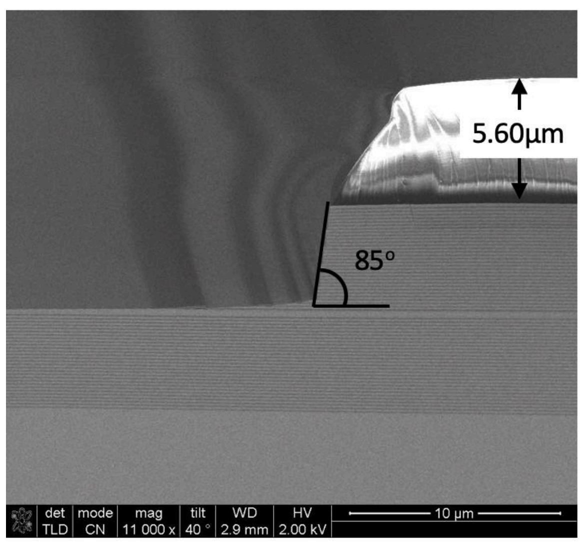


Figure 6.5 A SEM image of the cross section of the sample after a step of dry-etch. It illustrates that 5.60 μm thick photoresist remains and the profile has 85° sidewall.

Therefore, the whole etching process of fabrication flow would be simplified by using SPR220. Replacing the hard mask with 7 μm thick SPR220-7 photoresist maintains the distinct etching profile and sharp sidewalls. Moreover, it reduces the steps, including hard

mask deposition, hard mask etching and hard mask removal. A significant simplification can be achieved by using SPR220 photoresist during etching process.

6.2 Issue in Dielectric Etch Module

During this fabrication process, it always find dielectric residuals on the sample after dielectric etching step. This issue has been mentioned in section 2.5. Figure 6.6 presents a microscope picture of sample with residuals. As shown in figure 6.6, two black arrows point at the residual within the trench area. Such residuals may be caused by two reason.

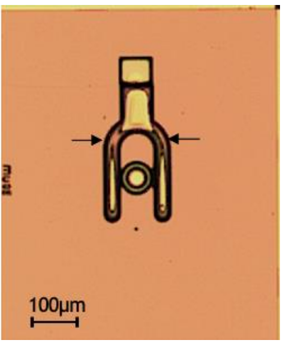


Figure 6.6 An optical microscope image of the sample with dielectric residuals (pointed by black arrows) found in the trench region.

Firstly, the dielectric etching process may stop too early and some dielectric was not yet been etched. Secondly, the photoresist layer was probably not developed completely. Thus, the dielectric under the photoresist residual becomes dielectric residual after etching. In order to examine the first susception, an interferometer signal recorded during Si_3N_4 etching process is presented in figure 6.7. As it shows, the detected signal goes flat after 460 s but the process finished at 520 s. This diagram indicates that the etching process etching process completed accomplished and then the etching process was terminated. So the first susception is not the reason in this case.

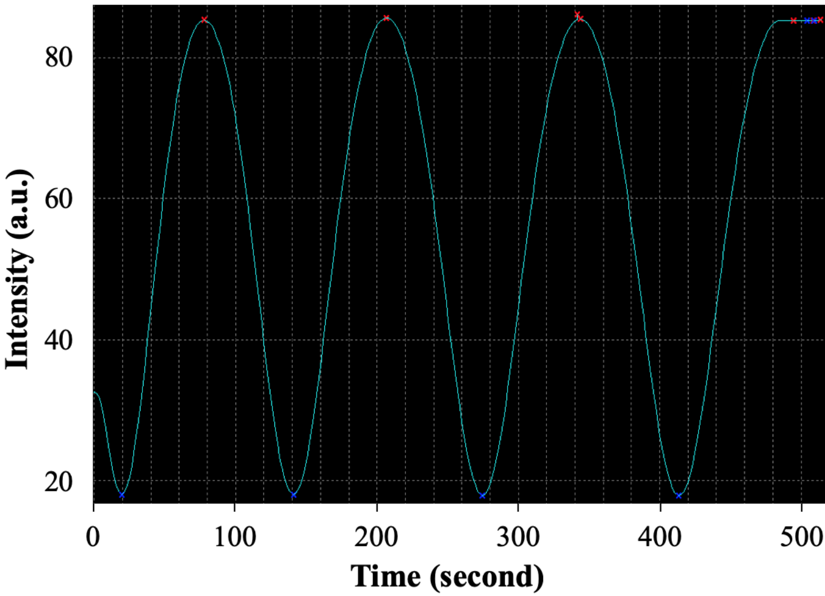


Figure 6.7 The interferometer signal measured during dielectric etching process. Signal goes flat after 460 s and the whole process stopped at 520 s.

To discuss the second possibility, the cross-section and plan view diagrams of the sample at photoresist step in dielectric etching module is shown in figure 6.8. As we can see, two area are exposed at this step. One is a circular area at the centre. The other is the trench area. The cross section diagram in figure 6.8 shows that the depth of these area are different. In the trench area, photoresist has a thickness of 9 µm. While, in the circular area, the photoresist has a thickness of 1.8 µm. It can thus be suggested that the photoresist in the deep trench may has not been exposed totally due to its thickness. Thus dielectric material under the unexposed photoresist becomes dielectric residual. This highly be the origin of having dielectric residuals.

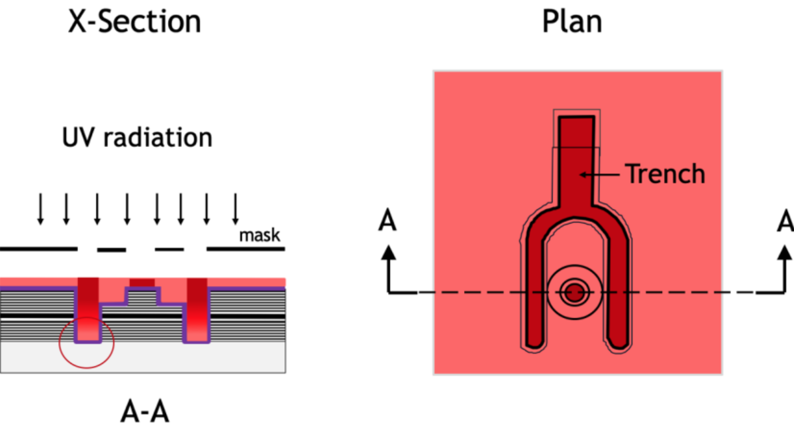


Figure 6.8 The cross-section and plan view of sample at photoresist exposure step in dielectric etching module. Two area are exposed. One is the circular area in the centre and the other is the trench area. These two area have different depth.

To solve this problem, the solution is discussed here. First, increasing the exposure time to

ensure the photoresist in the trench region is exposed fully. However, due to thickness difference of circular area and trench area, it is possible that a long exposure time causes overexposure for the circular region. Alternatively, the dielectric etching process can be separated into two steps based on the photoresist thickness. Then the exposure time for each area can be tailored by the photoresist thickness. Figure 6.9 presents a diagram of a photolithography mask split based on the photoresist thickness in the different regions. A new photolithography mask has been designed to realise this two-step exposure process.

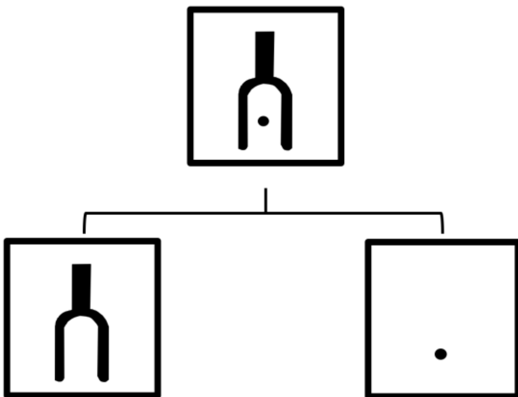


Figure 6.9 Diagram of a mask splitting based on the photoresist thickness in different regions.

6.3 Contact Resistance Evaluation Structure

The CTLM section in the mask has not been designed correctly. Therefore, a correct CTLM test structure is required for the new mask. This allows the contact resistance of each batch of devices being measured. The CTLM structure designed on the new mask is presented in figure 6.10. The gap between the circular metal pad and the external metal contact of the varies from 10 μm to 30 μm with an increment of 5 μm. To examine both p- and n-contact resistance, two sets of CTLM structure are designed with p and n contact deposited on top. Therefore, the p- and n-contact resistance of each batch can be evaluated separately.

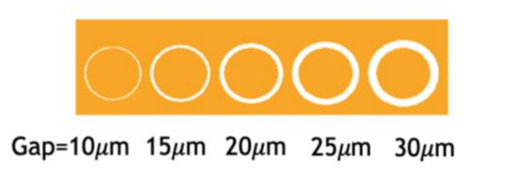
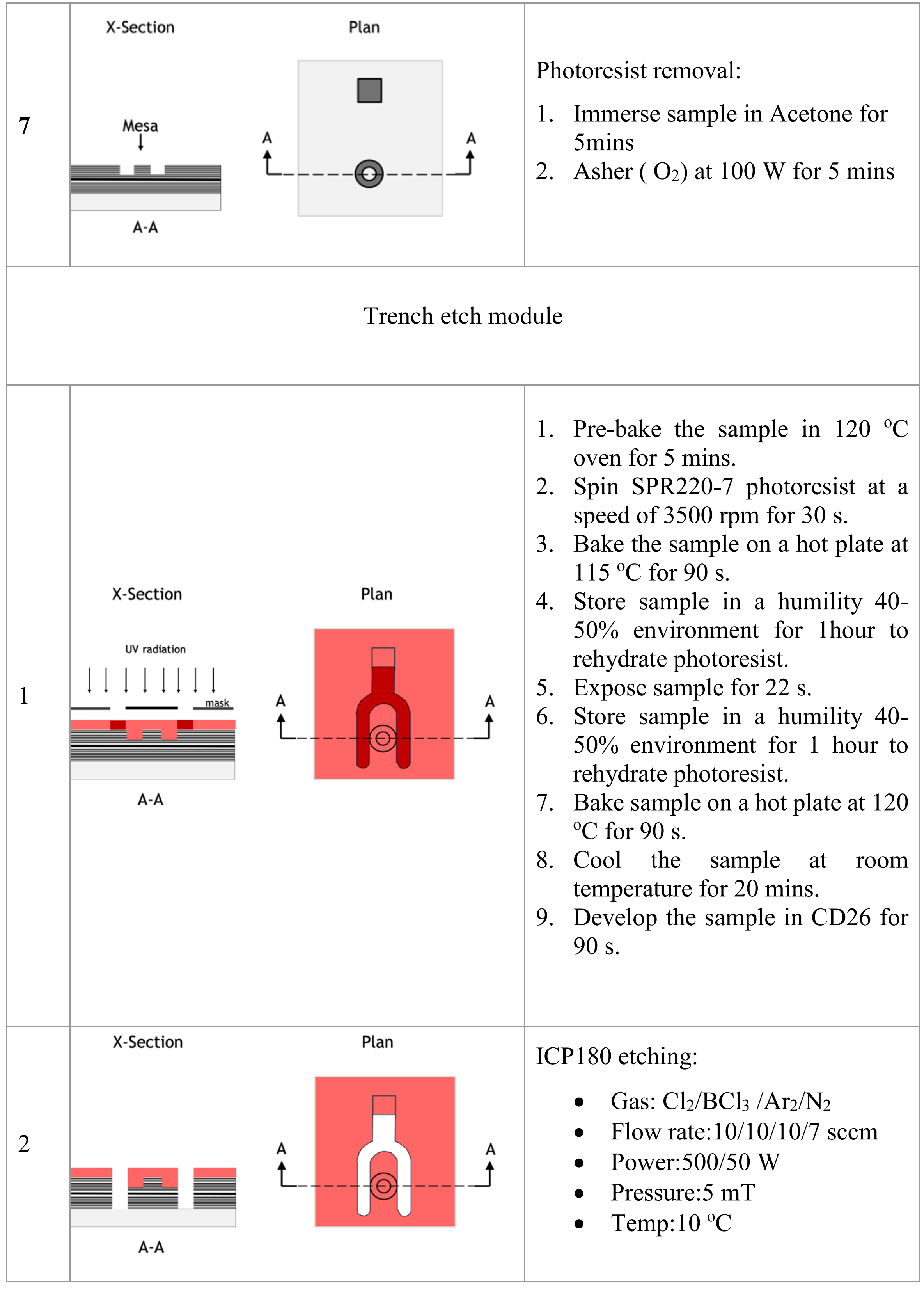


Figure 6.10 Diagram of the CTLM structure designed to be added on the new mask.

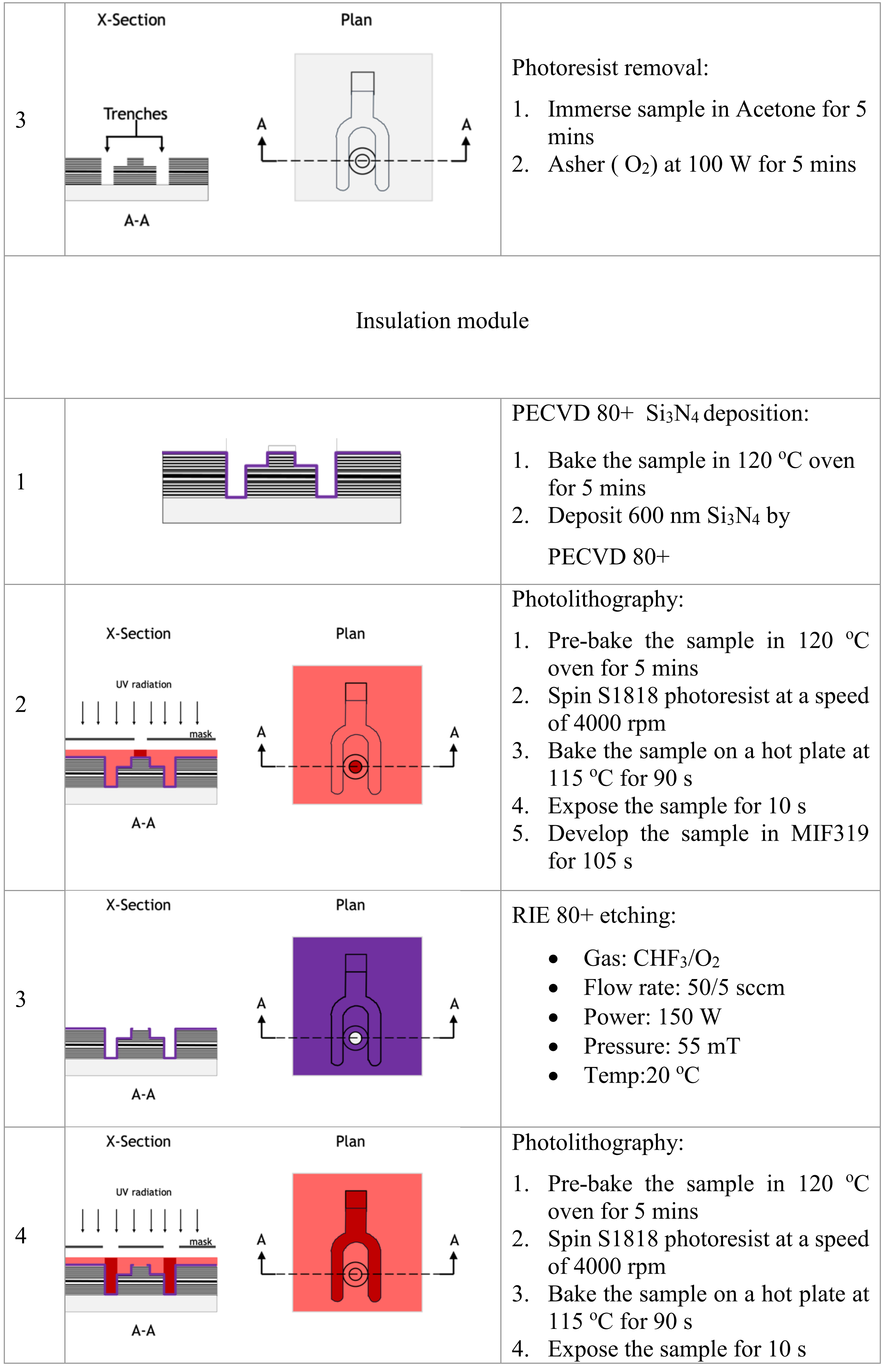
6.4 New Fabrication Flow

This section summarizes the new fabrication process based on modifications mentioned above and delivers an overview of new fabrication flow.

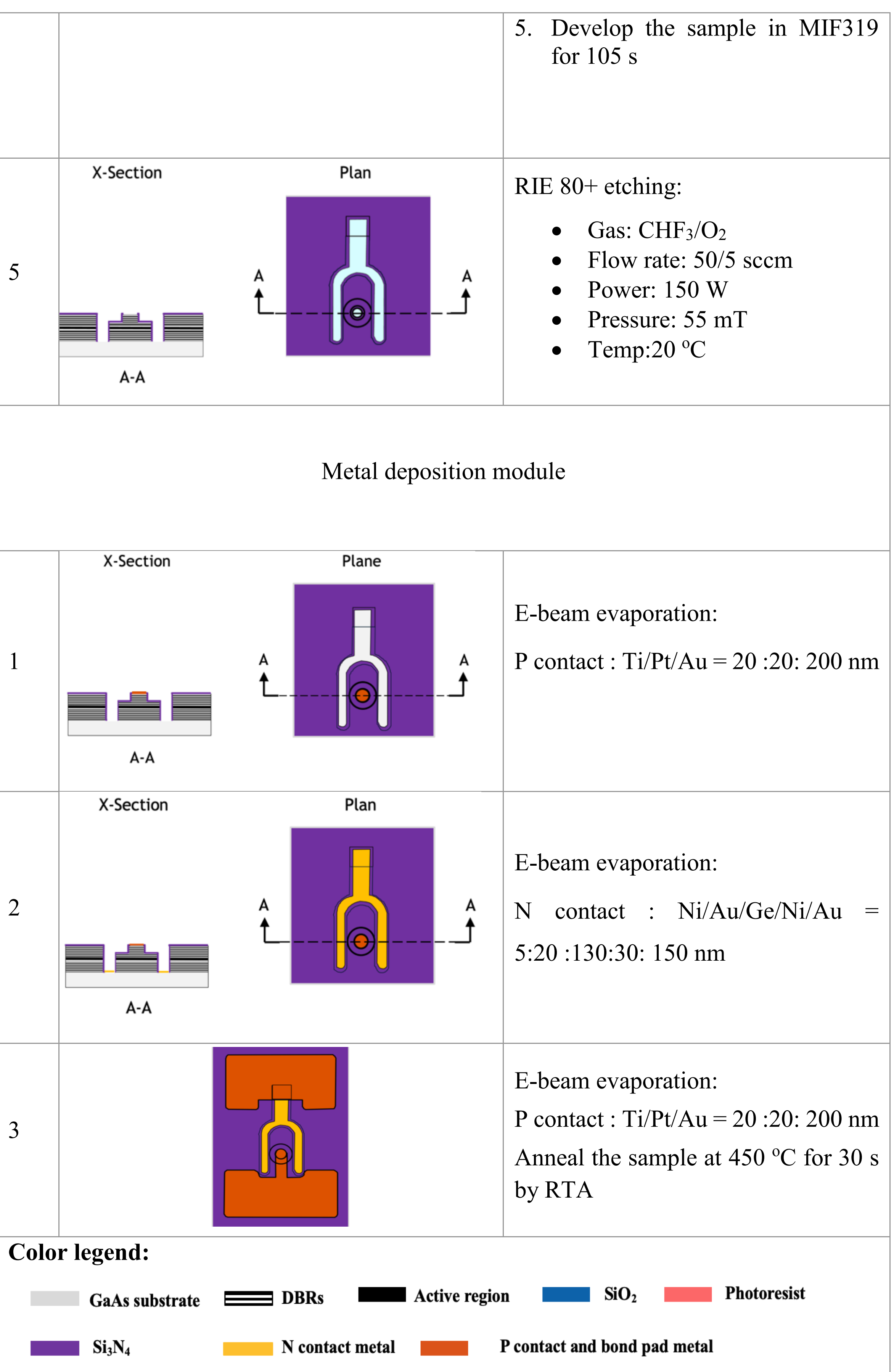
Step	Schematic	Description
Mesa etch module		
1		Clean sample: 1. Check the sample under microscope 2. Immerse the sample in acetone for 5 mins 3. Immerse the sample in IPA for 5 mins 4. Rinse the sample by R.O. water for 5 mins 5. Dry the sample by N_2 gun
2	X-Section Plan UV radiation mask A A A-A	1. Pre-bake the sample in 120 °C oven for 5 mins. 2. Spin SPR220-7 photoresist at a speed of 3500 rpm for 30 s. 3. Bake the sample on a hot plate at 115 °C for 90 s. 4. Store sample in a humility 40-50% environment for 1 hour to rehydrate photoresist. 5. Expose sample for 22 s. 6. Store sample in a humility 40-50% environment for 1 hour to rehydrate photoresist. 7. Bake sample on a hot plate at 120 °C for 90 s. 8. Cool the sample at room temperature for 20 mins. 9. Develop the sample in CD26 for 90 s.
6	X-Section Plan A A A-A	ICP180 etching: • Gas: $Cl_2/BCl_3/Ar_2/N_2$ • Flow rate:10/10/10/7 sccm • Power:500/50 W • Pressure:5 mT • Temp:10 °C



Step	Figure	Description
7	X-Section / Plan (A-A)	Photoresist removal: 1. Immerse sample in Acetone for 5mins 2. Asher (O_2) at 100 W for 5 mins
	Trench etch module	
1	X-Section / Plan (A-A)	1. Pre-bake the sample in 120 °C oven for 5 mins. 2. Spin SPR220-7 photoresist at a speed of 3500 rpm for 30 s. 3. Bake the sample on a hot plate at 115 °C for 90 s. 4. Store sample in a humility 40-50% environment for 1hour to rehydrate photoresist. 5. Expose sample for 22 s. 6. Store sample in a humility 40-50% environment for 1 hour to rehydrate photoresist. 7. Bake sample on a hot plate at 120 °C for 90 s. 8. Cool the sample at room temperature for 20 mins. 9. Develop the sample in CD26 for 90 s.
2	X-Section / Plan (A-A)	ICP180 etching: • Gas: Cl_2/BCl_3 /Ar_2/N_2 • Flow rate:10/10/10/7 sccm • Power:500/50 W • Pressure:5 mT • Temp:10 °C



Step	Figure	Description
3		Photoresist removal: 1. Immerse sample in Acetone for 5 mins 2. Asher (O_2) at 100 W for 5 mins
Insulation module		
1		PECVD 80+ Si_3N_4 deposition: 1. Bake the sample in 120 °C oven for 5 mins 2. Deposit 600 nm Si_3N_4 by PECVD 80+
2		Photolithography: 1. Pre-bake the sample in 120 °C oven for 5 mins 2. Spin S1818 photoresist at a speed of 4000 rpm 3. Bake the sample on a hot plate at 115 °C for 90 s 4. Expose the sample for 10 s 5. Develop the sample in MIF319 for 105 s
3		RIE 80+ etching: • Gas: CHF_3/O_2 • Flow rate: 50/5 sccm • Power: 150 W • Pressure: 55 mT • Temp:20 °C
4		Photolithography: 1. Pre-bake the sample in 120 °C oven for 5 mins 2. Spin S1818 photoresist at a speed of 4000 rpm 3. Bake the sample on a hot plate at 115 °C for 90 s 4. Expose the sample for 10 s



		5. Develop the sample in MIF319 for 105 s
5	X-Section / Plan / A-A	RIE 80+ etching: • Gas: CHF_3/O_2 • Flow rate: 50/5 sccm • Power: 150 W • Pressure: 55 mT • Temp:20 °C
Metal deposition module		
1	X-Section / Plane / A-A	E-beam evaporation: P contact : Ti/Pt/Au = 20 :20: 200 nm
2	X-Section / Plan / A-A	E-beam evaporation: N contact : Ni/Au/Ge/Ni/Au = 5:20 :130:30: 150 nm
3		E-beam evaporation: P contact : Ti/Pt/Au = 20 :20: 200 nm Anneal the sample at 450 °C for 30 s by RTA
Color legend: GaAs substrate, DBRs, Active region, SiO_2, Photoresist, Si_3N_4, N contact metal, P contact and bond pad metal		

Table 6.2 New fabrication flow of trench-etch VCSEL.

6.5 Conclusion

This chapter proposes three modifications of the fabrication process. To simplify etching modules, a 7 μm thick photoresist SPR220 is selected to replace the hard mask. Consequently, six steps have been reduced in the fabrication process. Furthermore, a dielectric residual issue has been discussed. This problem is addressed by splitting the dielectric etching step into two steps. The design of new CTLM metallisation area on previous mask is not correct. Therefore, two CTLM sections are proposed to have on the new mask. This chapter discussed the fabrication issues in this work and proposed solutions. At the end, a new fabrication flow is presented.

6.6 Future Work

The future work would focus on examining the new fabrication process reliability and repeatability. A high yield fabrication process is expected after the dielectric residual is cleaned in the n contact area. It would be better to have device images to support the fabrication improvements proposed in this chapter.

Chapter 7

Summary and Future Work

7.1 Summary

VCSEL has been deployed in applications including data communications, laser printing, image processing, and optical computing [27][25]. In my thesis, the VCSEL was selected to be part of a new generation communication platform - the 1.53 µm SPICs system. The SPICs system is a well-known solution that combines electronics with photonics for achieve high speed and small size silicon integrated circuits. It replaces electrical signals with fast, cross-talk free optical signals. However, the SPICs system has to be excited optically due to silicon's indirect bandgap characteristic. Therefore, a high efficiency, narrow wavelength, compatible optical source is an essential part of this SPICs system. The work carried out throughout my PhD systematically develops a 980 nm, substrate emitting, stable polarisation VCSEL based on the configuration and characteristics of such SPICs systems and components.

In order to propose an optimal design of VCSEL, the property of target SPICs system is discussed at the beginning. This SPICs system encompasses an EDWA that provides 1.53 µm optical signal in silicon. The mission of VCSEL is to excite erbium ions in the EDWA. Thus, a study of erbium energy level and a review of wavelength, bandwidth, power and pump efficiency of previous pump source are presented. The findings suggest that a proper pump source should have a wavelength of 980 nm with bandwidth less than 5 nm and its power has a value of higher than 30 mW for a 500 µm long EDWA [9][10]. The specific parameters are summarised in table 7.1.

Considering the structure stability of the SPICs system, the designed VCSEL is placed on a coupler that takes the light normal to the waveguide and diffracts it to be guided in-plane.

Because such coupler have a distinct coupling efficiency for TE and TM polarised light [12], it requires the pump source to have stable linear polarisation emission. Moreover, to achieve a seamless system, emission from VCSELs should come out of substrate. Therefore, substrate emission and stable polarisation were added into the requirements of VCSEL design.

The characteristics of VCSELs including their operating principle, structure, advantages and disadvantages were reviewed in Chapter 1. The VCSEL is prone to its instable polarisation performance. Due to its birefringence property, two orthogonal polarisation states coexist in the emission of VCSELs and the direction of them randomly distributes in the plane of the active region [44]. Methods used to control the polarisation of VCSEL were summarized. Generally, three kinds of methods are developed to stabilise the polarisation of VCSEL: anisotropic gain, anisotropic feedback method and anisotropic internal loss method. Considering the specific requirements in this project, a trench-etched method was selected to develop a stable polarisation VCSEL. It has been reported that this method has strong effects on pinning the polarisation direction of a proton implanted top emitting VCSELs [60][61][62].

The device designed in this work has two 30 μm wide,9 μm deep trenches etched into it. To realise the designed VCSEL, micro-fabrication processes were developed. A GaAs wafer designed to operate at λ=970 nm with three 6nm thick $In_{0.17}Ga_{0.83}As$ quantum wells, 30 pairs of top-DBRs and 28 pairs bottom DBRs was used in the VCSEL fabrication. The fabrication process contains four modules: mesa etch module, trench etch module, insulation module and metal deposition module. To configure deep etch patterns, a hard mask layer was applied that has a lower etch selectivity to GaAs to transfer the etch pattern into the wafer material. Oxford instruments RIE 80+ and ICP180 were used in this fabrication process. It was found that the etching rate for SiO_2 and GaAs are 32 nm/min and 600nm/min respectively. The profile obtained for the 9 μm deep trench has a 89° sharp edge. By following this nanofabrication flow, different diameter VCSELs with the trenches aligned to $[01\bar{1}]$ crystal axis were constructed. Each device occupies an area of 680×680 μm².

The characteristics of fabricated trench-etched VCSELs were profiled by using a newly constructed set-up. Even though there is 76% power lost in the absorption and reflection processes, a 4.5 mW output power is achieved by a 40 μm diameter trench-etched VCSELs. A comparison of slope efficiency between different diameter VCSELs indicates that largest

diameter device, 40 µm device, has the highest slope efficiency of 0.1 W/A (~0.42 at the device). In addition, a wall-plug efficiency higher than it of other smaller diameter devices was observed for the larger device. However, there is space to improve the power efficiency of designed VCSELs compared to high power device reported in literature.

Polarisation characteristics of fabricated devices are demonstrated for different diameter trench-etched VCSELs. In this work, it is firstly found that the polarisation stability of trench-etched devices is related the diameter. Stable polarisation direction was obtained by 40 µm and 30 µm diameter VCSELs. The optical polarisation suppressed ratio (OPSR) for them is 2 and 8 dB respectively. As the diameter reduced, unstable/unpinned polarisation direction was observed for the 20 µm and 10 µm diameter devices.

The polarisation property has been analysed for different diameter devices. At around half threshold, uniform spontaneous emission distribution has been found for all diameter devices. Comparing the intensity difference of nearfield images between orthogonal polarisation states, it was found that 0° polarised emission has intensity higher than 90° polarised emission and such difference can be found all over the aperture for 40 µm and 30 µm devices. This is in agreement with the preferred polarisation for lasing power for these devices.

An investigation on stable polarisation device, 40 µm trench-etched VCSEL, was carried out around the lasing threshold. It was found that different polarised modes generated at the same location on the aperture have a wavelength difference. This difference is larger at the centre and smaller at the edge. It indicates a birefringence difference in the aperture of 40µm device. At drive currents much higher than lasing threshold, it was observed that orthogonal polarised emissions have lasing area selection (i.e. they are spatially separate). There was no lasing pattern for 90° emission where 0° lasing modes were found. This work firstly reported an emission pattern investigation for stable polarisation trench-etched VCSEL. It guides the research on investigating large diameter stable polarisation VCSELs by using anisotropic gain approach.

The achievement of this work is summarised in table 7.1. It compares the requirements for a pump source of this SPICs system and the work accomplished in my PhD. The required emission wavelength, output power, stable polarisation and desired substrate emitting characteristics have all been developed in this work.

Parameter	Pump Requirements	This Work
Wavelength	980± 5 nm [10]	977±1 nm
Power	~30 mW for 500 µm long EDWA	4 mW for a single 40 µm VCSEL
Polarisation	Stable linear polarisation direction	stable linear polarisation
Geometry	Dual top-side contacts	Substrate emission
Low-cost Approach	Minimise processing steps, and maximise yield	Large scale production potential, optical lithography friendly

Table 7.1 A comparison of device performance with the requirements proposed for a pump source in this SPIC system.

The work carried out through the PhD achieved:

- Designed an optical pump source, substrate trench-etched VCSELs, for EDWA applied in SPICs system.
- Developed repeatable, reliable fabrication process to realise the designed trench-etched VCSELs
- Systematically characterised series resistance, output power, slope efficiency, wall-plug efficiency, and polarisation of different diameter VCSELs. Successfully achieve large diameter stable polarisation VCSEL.
- Investigated the polarisation characteristics of trench-etched devices, especially 40 µm diameter VCSEL, on its nearfield images, spectrum between orthogonal polarisation states.
- Found intensity difference and wavelength difference of emission of different polarisation states for trench-etched VCSELs.

7.2 New VCSEL Designs for Investigating the Effects of the Trench

This section aims to describe the new designs of the VCSELs. Five sets of VCSEL structure are presented. This new mask set was designed during my PhD, but I was unable to realise the due to time constraints.

- Device with diameter from 40 µm to 70 µm are designed.

- Devices with gaps of 15 µm, 20 µm, 25 µm, 30 µm, between VCSEL and trench are designed.
- Devices with trench width of 15 µm, 20 µm, 25 µm, 30 µm are designed.
- Devices with single trench, double trenches and no trench are designed.
- Device with trench depth of 9 µm, 4 µm and 2 µm are designed.

These five sets of VCSEL are introduced in the following.

Large diameter devices:
I found that from 10 to 40 µm in diameter, improving OPSR was observed, and maximal, ideal diameter had not been realised. A set of VCSELs with diameter of 40 µm, 50 µm, 60 µm and 70 µm is designed in the new mask. Figure 7.1 shows a diagram of devices in this group. As it shows, all the devices in this set have two 30 µm wide trenches next to them. The p-contact of devices is deposited on circular area of VCSEL and n contact of devices is deposited on the trench. As it mentioned in chapter 3, large size VCSEL with diameter of 40 µm presents best polarisation stability compared with other small devices. Therefore, large diameter devices are proposed to examine the effect of trenches on large diameter devices.

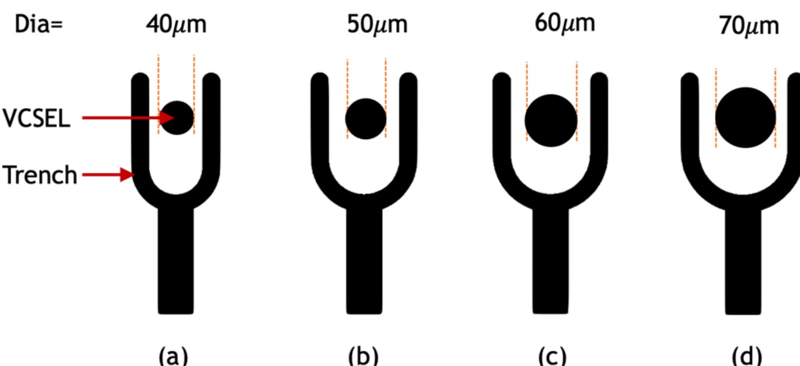


Figure 7.1 Diagram of a set of VCSEL with diameter of 40 µm, 50 µm, 60 µm and 70 µm. Devices have the same trench structure and trench is 15 µm away from the VCSEL.

Trench gap group:
For my devices, the distance from trench to mesa was constant, and the effect of varying this parameter has not yet been investigated. A set of VCSELs with the trench distributed at a different distance is presented in figure 7.2. For this design, the four devices have the same diameter of 40 µm. However, the distance from VCSEL to trench varies from 15 µm to 30 µm with an incremental of 5 µm. The diagrams of devices are presented in figure 7.2(a), (b), (c) and (d). For this set of VCSELs, the trenches area is united with the n-contact, which decides the depth of the trench.

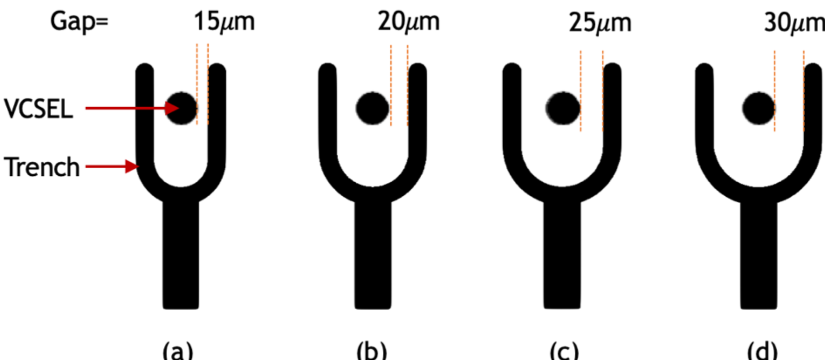


Figure 7.2 Diagrams of a set of VCSELs with different distance from the VCSEL to the closer trench.

Trench width group:

The design of this set of devices aims to examine the effect of trench associated with the trench's width, which has not yet been explored. It is expected that the trench sidewall is significant and trench width does not play a role, but it is worth checking. Figure 7.3 presents a set of VCSELs with a diameter of 40 μm but different trench width. It can be found that the trench gap of these devices is the same (15 μm). Only the width of the trench gradually increases from 15 μm to 30 μm as shown in figure 7.3(a), (b), (c) and (d).

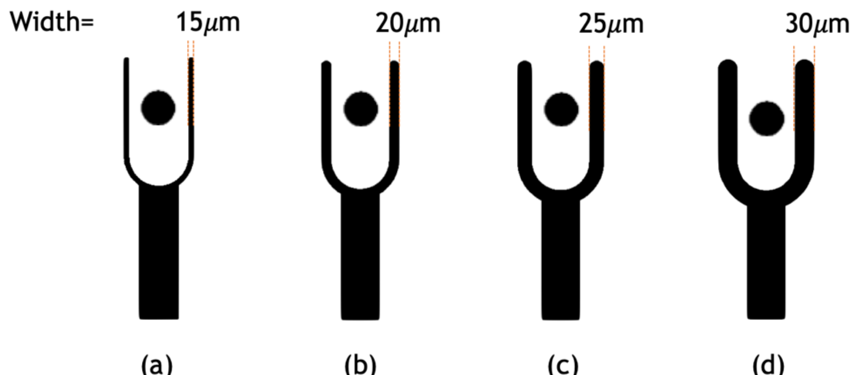


Figure 7.3 Diagrams of a set of VCSELs with the trench width increasing from 30 μm to 15 μm with an incremental step of 5 μm.

Trench number group:

In my work only a symmetric trench structure was employed. It would be interesting to see what effects can be obtained by varying the trench structure. This group proposes four kinds of devices with a single trench, double trenches and no trenches. **Error! Reference source not found.** presents the diagram of each device in this set. Figure 7.4(a) illustrates a device with two parallel trenches; Figure 7.4(b) demonstrates a device with a single trench at the left side and is 15μm away from device; Figure 7.4(c) depicts a device with a single trench at the right of VCSEL. All the trenches in Figure 7.4(a), (b) and (c) have the same width of 30 μm and depth of 9 μm to VCSELs. Figure 7.4(d) presents a device without trench. A rectangular area (shown in figure 7.4(b)) is designed as a n-contact for this device. This set

of devices is designed to investigate the capability of controlling polarisation direction with the numbers of trench.

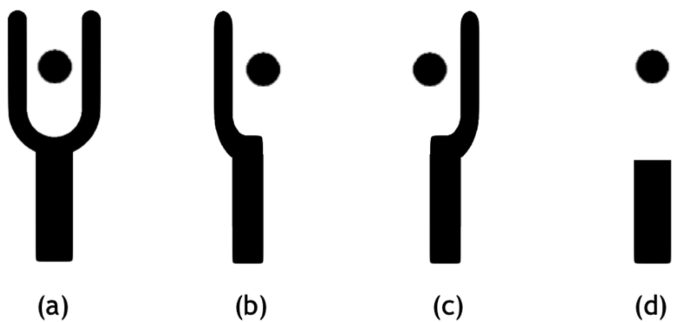


Figure 7.4 Diagrams of the devices: (a) a VCSEL with two parallel trenches; (b) a VCSEL with a single trench distributed at the left; (c) a VCSEL with a single trench distributed at the right; (d) a VCSEL without trench but has a rectangular n contact far away from it.

Trench depth group:

During my work, the n-contact and trench were realised using the same feature. For this set of VCSELs, the function of the trenches is separated from the n-contact. To clarify this design, a diagram is shown in figure 7.5. As it shows, the structure consists of three rectangular region. Two of those represent trenches that are next to the VCSEL with a distance of 15 μm. The rectangular at the end is a n contact area for device.

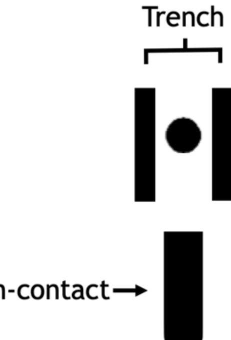


Figure 7.5 Diagram of the designed VCSELs has two trenches separated to the n-contact.

Figure 7.6 presents the diagrams of the devices in this set. As the A-A cross-section diagram shows, the depth of the trenches varies at three different levels. They are designed to be etched down to 9 μm, 4 μm and 2 μm corresponding to the depth of substrate, active region and a few layers of top DBRs. The aim of comparing devices with different trench depth is to see whether the effect of trench changes with it.

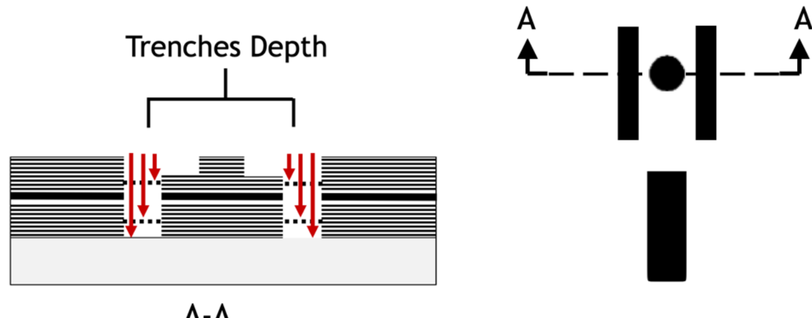


Figure 7.6 Diagrams of a set of VCSELs with the trenches etched at different depth.

Overall, five sets of VCSELs have different trench geometries are proposed to understand the effect of the trench on the performance of VCSELs comprehensively.

7.3 Conclusion

Throughout my PhD, I have developed and fabricated a stable polarisation VCSEL that satisfies specific requirements of a SPIC system. Such trench-etched method is valid for 40 μm and 30 μm diameter substrate emitting VCSELs. It is encouraging to find that a strong relationship between polarisation stability of devices and the spontaneous emission polarisation direction. An investigation of the birefringence properties of a 40 μm device has been presented in this work. The results suggest that the trench-etch induced birefringence property is strong at the centre of device aperture, and that high drive currents the polarised lasing occurs from different spatial regions of the device, opening up opportunities for novel new devices with structured p-contacts to enhance OPSR. This finding has important implications for developing stable polarisation substrate emitting VCSELs in the future. It delivers the insights to achieve large diameter, high power, and stable polarisation VCSELs arrays for this new application.

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