Development of Electronics for Microultrasound Capsule Endoscopy

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ABSTRACT

Development of intracorporeal devices has surged in the last decade due to advancements in the semiconductor industry, energy storage and low-power sensing systems. This work aims to present a thorough systematic overview and exploration of the microultrasound (μUS) capsule endoscopy (CE) field as the development of electronic components will be key to a successful applicable μUSCE device. The research focused on investigating and designing high-voltage (HV, < 36 V) generating and driving circuits as well as a low-noise amplifier (LNA) for battery-powered and volume-limited systems.

In implantable applications, HV generation with maximum efficiency is required to improve the operational lifetime whilst reducing the cost of the device. A fully integrated hybrid (H) charge pump (CP) comprising a serial-parallel (SP) stage was designed and manufactured for > 20 V and 0 - 100 μA output capabilities. The results were compared to a Dickson (DKCP) occupying the same chip area; further improvements in the SPCP topology were explored and a new switching scheme for SPCPs was introduced. A second regulated CP version was excogitated and manufactured to use with an integrated μUS pulse generator. The CP was manufactured and tested at different output currents and capacitive loads; its operation with an US pulser was evaluated and a novel self-oscillating CP mechanism to eliminate the need of an auxiliary clock generator with a minimum area overhead was devised.

A single-output universal US pulser was designed, manufactured and tested with 1.5 MHz, 3 MHz, and 28 MHz arrays to achieve a means of fully-integrated, low-power transducer driving. The circuit was evaluated for power consumption and pulse generation capabilities with different loads. Pulse-echo measurements were carried out and compared with those from a commercial US research system to characterise and understand the quality of the generated pulse. A second pulser version for a 28 MHz array was derived to allow control of individual elements. The work involved its optimisation methodology and design of a novel HV feedback-based level-shifter.

A low-noise amplifier (LNA) was designed for a wide bandwidth μUS array with a centre frequency of 28 MHz. The LNA was based on an energy-efficient inverter architecture. The circuit encompassed a full power-down functionality and was investigated for a self-biased operation to achieve lower chip area. The explored concepts enable realisation of low power and high performance LNAs for μUS frequencies.

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DECLARATION OF AUTHORSHIP

I hereby declare that this thesis entitled "Development of Electronics for Microultrasound Capsule Endoscopy", submitted in partial fulfilment of the requirements of the University of Glasgow for the degree of Doctor of Philosophy, represents my own work. No part of the work referred to in this thesis has been supported in application of another degree or qualification of this university or any other university or institute of learning.

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Signed: Bartas Abaravicius

Date: 07/07/2022

LIST OF TERMS

Abbreviations

µUS	Microultrasound
µUSCE	Microultrasound capsule endoscopy
ADC	Analog-to-digital converter/convertion
AF	Autofluorescence
AFE	Analog front-end
ASIC	Application specific integrated circuit
BCD	Bipolar-CMOS-DMOS
BSW	Bootstrapped switch
BVD	Butterworth-Van Dyke
BW	Bandwidth
CC	Cross-coupled
CCCP	Cross-coupled charge pump
CE	Capsule endoscopy
CFA	Capacitive-feedback amplifier
CM	Current mode
CMOS	Complementary metal-oxide-semiconductor
CMUT	Capacitive micromachined ultrasonic transducers
CP	Charge pump
CUC	Current comparator
DC	Direct current
DCT	Discrete cosine transform
DK	Dickson
DKCP	Dickson charge pump
DPCM	Differential pulse code modulation
EM	Electromagnetic
FEA	Finite element analysis
fps	Frames-per-second
FSC	Fast-switching condition
GC	Gastric cancer
GI	Gastrointestinal
GIT	Gastrointestinal tract
H	Hybrid
HCP	Hybrid charge pump
H2L	High-to-low
HBC	Human body communication

HS	High-side
HV	High-voltage
IA	Inverter-based amplifier
IBD	Inflammatory bowel disease
ICE	Intracardiac echocardiography
IO	Input-output
IVUS	Intravascular ultrasound
JPEG-LS	Lossles Joint Photographic Experts Group
L2H	Low-to-high
LED	Light-emitting diodes
LNA	Low-noise amplifier
LPF	Low-pass filter
LS	Low-side
Mb	Megabit
Mbps	Megabits per second
MEMS	Microelectromechanical system
MIM	Metal-insulator-metal
MIMcap	Metal-insulator-metal capacitor
MOM	Metal-oxide-metal
MOMcap	Metal-oxide-metal capacitor
MOS	Metal-oxide-semiconductor
MOScap	Metal-oxide-semiconductor capacitor
MRI	Magnetic resonance imaging
Msps	Megasamples per second
NBL	N-type isolation layer
PCB	Printed circuit board
PMUT	Piezoelectric micromachined ultrasonic transducers
POR	Power-on reset
ppm	Parts per million
PRF	Pulse repetition frequency
PSRR	Power supply rejection ratio
PVDF	Polyvinylidene fluoride
PVT	Process, voltage, temperature
RF	Radiofrequency
RFA	Resistive-feedback amplifier
RFT	Rising/falling time
RGB	Red-green-blue
RX	Receiver
SiP	System-in-package
SNR	Signal-to-noise ratio
SO	Self-oscillating
SOI	Silicon-on-insulator

SP	Serial-parallel
SPCP	Serial-parallel charge pump
SPAD	Single photon avalanche diode
SSC	Slow-switching condition
TEE	Transoesophageal echocardiography
TGC	Time-gain control
TIA	Transimpedance amplifier
TSMC	Taiwanese Semiconductor Manufacturing Company
TX	Transmitter
US	Ultrasound
VA	Voltage amplifier
VCO	Voltage controlled oscillator
VF	Volume fraction
VGA	Variable gain amplifier
VM	Voltage mode
VVRUS	Verasonics® Vantage™ Research Ultrasound System
WCE	White-light capsule endoscopy
WPT	Wireless-power transfer

Symbols

μ_0	Permeability of free space ($4\pi * 10^{-7}$ H/m)
Cdd	Stray capacitance associated with the MOSFET's drain.
Cgg	Stray capacitance associated with the MOSFET's gate.
C_{PAR}	Parasitic (stray) capacitance
f	Frequency
I_{OUT}	Output current
M_X	Sizing ratio of a MOSFET; width/length
Q_{PAR}	Charge required to charge the parasitic capacitance.
T	Time period, defined as 1/f
t_{OVL}	Non-overlap time
V_{DD}	Supply voltage
V_{DIODE}, V_T	Diode forward-bias drop voltage
V_{OUT}	Output voltage
V_{PP}	Peak-to-peak voltage
α	Ratio of parasitic capacitance to CP's pumping capacitance
α_r	Clock-boosted optimum rise-time
ε_r	Relative permittivity
η	Power efficiency
Φ, φ	Clock signal

1 INTRODUCTION

The progress of complementary metal-oxide-semiconductor (CMOS) technology has led to continuous reduction of power consumption and advanced functionality in the same chip area, facilitating the development of low-power intracorporeal devices [1]. Although the majority of these devices rely on low-voltages with minimal current requirements [2], some intracorporeal applications demand high-voltage (HV) supplies and high current drives. These include ultrasound (US) sensing and therapy [3], [4], neural stimulation [5], [6] and autofluorescence (AF) using single-photon avalanche diodes (SPADs) [7], [8]. While some of these applications require > 30 V supplies, modern CMOS technologies are continuously optimised for lower supply voltages (often down to 1 V). Typically, DC-DC conversion can be achieved to boost the supply voltage using widely available off-the-shelf switched voltage supplies; however, their implementations suffer from area constraints, magnetic non-compatibility and the need for additional external components. As a result, custom integrated solutions for HV generation are called for.

Charge pumps (CPs) are a subgroup of DC-DC converters and are the first line of choice for intracorporeal applications as they can be fully integrated and achieve a satisfactory performance whilst comprising only switches, capacitors and a single clock signal. Furthermore, they can be magnetically compatible, which is compulsory in instances with a potential need for magnetic resonance imaging (MRI) procedures. Prior work has shown their use in neural stimulators [9]–[11], AF capsule endoscopy (CE) devices [7], [12], retinal prostheses [13], [14] and bio-sensing implants [15]. The area constraints in intracorporeal applications are limited by the human anatomy. So the development of CPs with improved area and power specifications is vital to free up the design space and realise better primary functionality of these systems. Furthermore, the generated HV must be appropriately controlled using device stacking, floating circuits, and other techniques to satisfy safe operating limits while ensuring minimum power consumption.

Some small form factor devices require HV and low current power sources, such as in SPAD imagers [8] or microelectromechanical system (MEMS) resonators [16]. In SPAD systems, HV is required to reverse-bias the diodes above their breakdown voltage. In this configuration a single incident photon is enough to trigger an avalanche event which, in turn, is applied in fluorescence lifetime imaging. MEMS resonators are used in RF systems, but require

a HV to drive the MEMS switch. For both purposes, area-efficient HV CP designs are necessary, particularly if the system is to be used in a human body. Additionally, there are applications with more demanding current requirements, like neurostimulation and US.

US describes acoustic waves above the human hearing range (> 20 kHz) used for human body imaging, therapy, cancer treatment, and non-destructive testing. It has recently seen developments in targeted drug delivery and neuromodulation as well. Advancements in US array manufacturing, the birth of piezoelectric and capacitive micromachined ultrasonic transducers (PMUTs and CMUTs) and improvements in system integration strategies have enabled exploring US applications in significantly area constrained environments such as implantables [17], 3D US catheters [18], wearable patches [19], point-of-care portable scanners [20] and even injectable motes [21]. Whilst some of these systems are already widely available, others are significant work away from a clinically viable solution, for example, a microultrasound (µUS) capsule endoscopy (µUSCE) device.

Microultrasound defines US waves above 20 MHz that can be used to image cellular structure and have already been applied in bulky commercial systems for prostate cancer detection [22]. Its use has also been researched in CE devices to one day have a new means of investigation and a clinically viable solution for higher accuracy early diagnosis of numerous gastrointestinal (GIT) disorders [23]. The challenge of these systems is the simultaneous HV, and high current demand coupled with high-frequency HV pulse generation and signal sampling requirements, dictated by the physics of US transducers. Previous µUSCE prototypes were tethered or operated in a lower frequency domain; an integrated prototype is yet to be created, awaiting research in the electronics and full US system necessities. Consequently, the work presented here aims to fill some of the technological gaps by exploring voltage conversion, pulse generation and amplification designs in 0.13 µm and 0.18 µm HV bipolar-CMOS-DMOS (BCD) technologies. The findings discussed here are applicable and relevant to other biomedical HV applications and are the basis for future µUSCE device research.

1.1 CONTRIBUTIONS TO KNOWLEDGE

The goal of this thesis is to contribute to the development and realisation of low power and low area HV application specific integrated circuit (ASIC) for biomedical intracorporeal applications while focusing on a µUSCE system as the medium of application by:

- Development of a new HV charge pump comprising an intermediary regulated stage and a newly proposed self-biased serial-parallel (SP) charge pump in a 0.13 µm HV BCD process [24]. The design utilises low-voltage capacitors across the whole circuit, leading to significant area savings and operation within compliance limits. An optimisation strategy for the SP stage is proposed, and strategies to further improve the behaviour of the proposed architecture are discussed in detail.
- The design, manufacture and testing of an HV high-current CP with two regulation schemes, with complete testing and characterisation of the designs carried out. The CP was used to test transmitter pulse generation for a variety of µUS arrays. It will allow for future evaluation of effects on the US image quality due to regulation variations and testing of tetherless prototype CE devices.
- Inception and verification of a self-biased CP with minimum energy and area requirements, an integrated frequency control capability and compatibility with a duty cycle control scheme. Integrated US systems require thoughtful design consideration to ensure noise isolation from the transmitter to the receiver sub-systems. The design offers a minimal area solution that is stable across process corners in the biomedical temperature range and eliminates the need for an external clock generator. The low power of the design is crucial to extending the operation of a CE device.
- Design, manufacture and testing of a HV pulser that provides a very-low power operation and < 3 ns edge time for driving large capacitive loads at µUS frequencies [25]. The circuit was tested with different US arrays, and their performance was evaluated with a HV CP and against commercial systems. The adaptation of the manufactured pulser is further explored toward a single array system. The suggested optimised pulser design lays the basis for future ultra-low-power US systems.
- Development and simulation of a low-voltage LNA for interfacing with µUS arrays that achieved ultra-low power and low-area with power-down functionality, self-contained biasing and bandwidth extension. A self-biased LNA is proposed as the basis for further power consumption and area improvements that are crucial in CE devices with a limited power budget and a high count of elements.

1.2 THESIS STRUCTURE

This thesis was written during the global SARS-CoV-2 pandemic that started in 2019, which led to national lockdowns and resulted in a global semiconductor manufacturing and chip supply shortage. All designs described in this thesis were initially planned to be implemented in the TSMC 0.13 µm BCD process and manufactured with the help of Dialog Semiconductor (purchased by Renesas during the work, hereafter called Dialog) but, due to the global circumstances, only two out of three chips were manufactured (Chapters 3, 4 and 5). The third chip was to include an updated pulser version (Chapter 5) with the self-oscillating CP (Chapter 4) and the LNA (Chapter 6) but it was voided due to discontinuation of all relevant future tape-outs. However, the designs were ported and further developed in TSMC 0.18 µm BCD technology within the academic setting; the final tape-out could not be realised within the timeline of the project. For these reasons, results of corner and Monte-Carlo circuit simulations are provided to characterise the circuits that could not be manufactured. The structure of the thesis is shown in Figure 1-1.

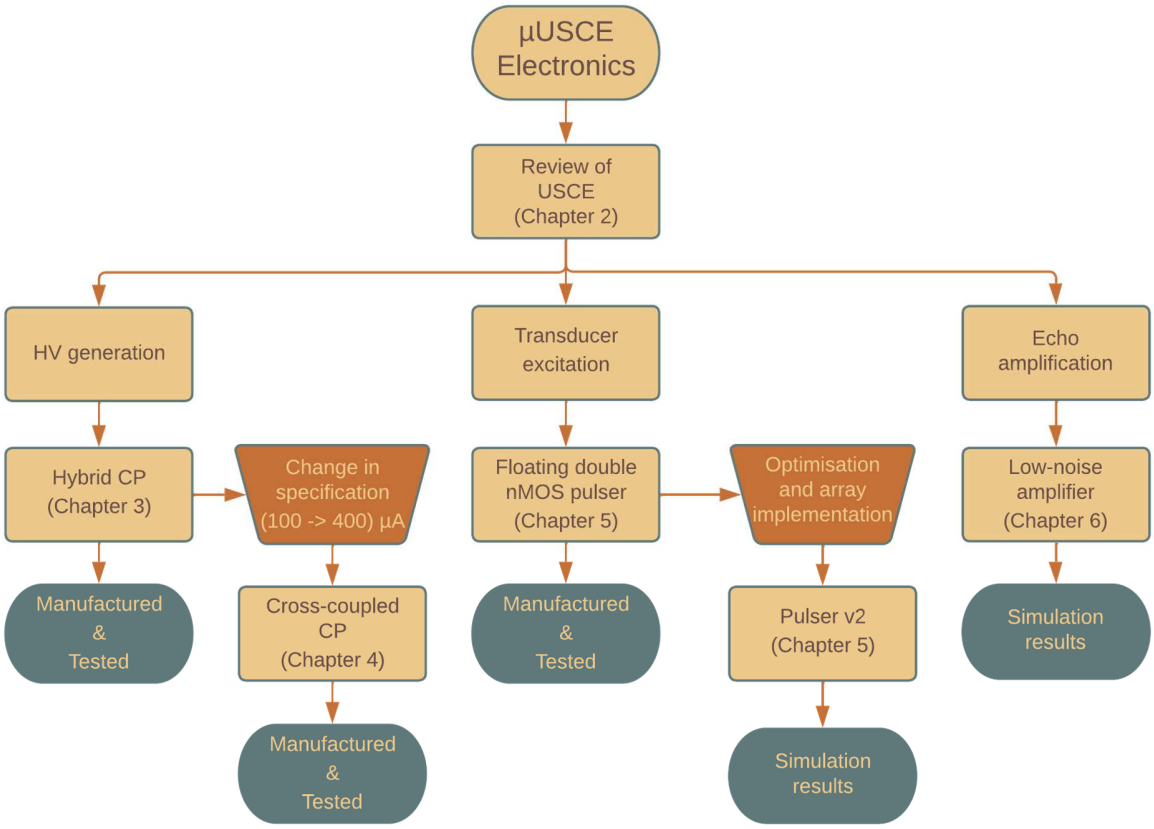

Figure 1-1. Thesis structure diagram.

Chapter 2 is an overview of state-of-the-art CE devices focusing on their system challenges and power requirements. The chapter begins by defining some health issues arising in the GIT and their importance to the common person and society. This lays the motivation of the work described in this thesis, followed by a section on concepts and considerations of an US system. Subsequently, present-day diagnostic methods for the GIT are presented, and US use is introduced, including US application in other probe-type devices and their power considerations. This chapter evaluates academic and commercial achievements in white-light capsule endoscopy (WCE), ranging from imaging to wireless-power transfer (WPT), and then covers research in the US and auto-fluorescence CE fields.

Chapter 3 describes a fully integrated low-current (< 100 µA) area-saving hybrid charge pump (HCP) comprising cross-coupled (CC) and newly proposed SP CPs to achieve an unregulated > 20 V output. The chapter begins with a review of switched-inductor and switched capacitor voltage regulator usage for HV generation within the framework of highly integrated designs suitable for intracorporeal applications. The review is continued with an investigation of different CP topologies regarding their intrinsic characteristics and chip-level implementation. The HCP description is separated into sections on the CC and SP stages, and an optimisation methodology is described for the latter. To better compare the results of the new SPCP, a reference Dickson (DK) CP was manufactured and the CCCP, SPCP, DKCP, and HCP results are discussed. As a mismatch between measurement and simulation results was observed, a close analysis of potential causes is explored, and solutions to improve the SPCP are provided.

Chapter 4 continues the topic of integrated CPs, but focuses on requirements dictated by an integrated µUS system. The chapter builds on the CCCP stage presented in Chapter 3 and describes a five-stage CP to supply up to 400 µA output current (I_{OUT}) with two output voltage regulation schemes for low power or low-ripple regulation. The chapter then describes a new self-oscillating CP based on a current comparator with low area requirements, high efficiency (η) and low oscillator circuit power consumption. The proposed architecture is compatible with both duty-cycle and frequency control regulation concepts.

Chapter 5 presents a low-power bootstrapped HV pulser for driving a µUS array at 28 MHz and designed to be integrated into a CE device. The chapter has two main sections. The first one discusses a single-channel pulser for driving high-capacitance piezoelectric elements in a CE system with receive and transmit arrays separated. Considerations of an integrated high-frequency system are provided, followed by an evaluation of the HV power source and pulser

switching requirements. The first section is closed with results obtained from testing the pulser with 1.5 MHz, 3 MHz and 28 MHz arrays and compared to a Verasonics® Vantage™ Research Ultrasound System's (VVRUS) pulse generating capabilities. Equivalent measurements were carried out with a CP used as a HV power source. The second part of the chapter is dedicated to the second iteration of the pulser designed to drive a full US array in a single array implementation. Two different architectures are investigated, and qualitative estimation of power consumption is provided. This section also discusses a new floating level-shifter for feedback-based pulser control. Finally, techniques to reduce the area of the bootstrapped array pulser are discussed.

Chapter 6 presents a low-noise amplifier (LNA) design for µUS transducers operating in the bandwidth (BW) 19.6 – 36.4 MHz with a centre frequency of 28 MHz. The LNA was built on an inverter-based amplifier (IA) architecture to achieve the highest current efficiency for the desired noise performance. The design utilises a dynamic biasing scheme and proposes an implementation which requires no external biasing elements and allows for full power-down and a fast turn-on. A method to extend the BW is introduced, followed by an explanation of a self-biased LNA architecture. Simulation results are then provided to support and exemplify the design choices.

Chapter 7 concludes this work and elaborates on the future research toward the realisation of a fully integrated µUSCE device.

1.3 Publications Based on the Current Work

Peer-Reviewed Journal Papers:

- **B. Abaravicius**, S. Cochran, and S. Mitra, "High-Efficiency High Voltage Hybrid Charge Pump Design With an Improved Chip Area," *IEEE Access*, vol. 9, pp. 94386–94397, 2021, doi: 10.1109/ACCESS.2021.3091808.

Conference Proceedings:

- **B. Abaravicius**, A. Moldovan, S. Cochran, and S. Mitra, "Development of a Point-of-Care Ultrasound Driver for Applications with Low Power and Reduced Area Requirements," in *2021 IEEE International Ultrasonics Symposium (IUS)*, Xi'an, China, Sep. 2021, pp. 1–4. doi: 10.1109/IUS52206.2021.9593342.
- **B. Abaravicius**, S. Cochran, and S. Mitra, "An area-efficient hybrid high-voltage charge pump design for IoT applications," in *2018 30th International Conference on Microelectronics (ICM)*, Sousse, Tunisia, Dec. 2018, pp. 36–39. doi: 10.1109/ICM.2018.8704073.

2 ULTRASOUND CAPSULE ENDOSCOPY

2.1 INTRODUCTION

This chapter lays down the context for ASIC design in Chapters 3 - 6. In the context of small capsule devices, the introduction of additional modalities can only be considered if the full capabilities and limitations of currently existing systems are understood. As a result, this chapter investigates the technology of commercial and academic research devices to verify the viability of a multi-modal CE system, with power and integration being at the centre of attention.

The chapter begins by describing the importance of GIT ailments and trends seen in developed countries. This is followed by a description of an US system and the main concepts relevant to the discussion of its application in GIT imaging. A short description of conventional endoscopy, as well as new advancements in the field, is presented.

Afterwards, contemporary WCE is discussed, including alternative sensing modalities in CE that have emerged recently. The discussion then covers prior work in particular areas, namely data compression, data transmission, and wireless power transfer. The final section is dedicated to US and fluorescence CE devices due to their similar energy and supply voltage requirements and challenges. Other relevant CE research is mentioned and research in the field is then briefly described followed by conclusions of the review.

2.2 CLINICAL RELEVANCE

Recent studies show that around 20% to 40% of the population currently suffer from a GI disorder [26]. In the United States, this number results in an estimated 60 to 70 million affected people and more than 54 million ambulatory visits to a clinic each year [27]. In the United Kingdom, GI diseases are the number three cause of death after circulatory and respiratory diseases [27]; however, the impact of some related chronic and less deadly illnesses has been shown to extend to other physiological and psychological symptoms, affecting both individuals' social and private lives [28]. An increasing number of studies are also finding a connection between inflammatory bowel disease (IBD), dementia and depression [29]–[33]. These findings are further emphasised by the statistics of the increasing prevalence of IBD over the last few decades [34], [35]. At the same time, major depression has been projected to rank as the first cause of burden of disease by 2030 [36].

The GIT comprises multiple organs involved in digestion, nutrient absorption, and other processes. Not only is it in constant contact with the environment, but it is also directly dependent on lifestyle, food and drink choices, which are habitual and can persevere for extended periods. Apart from unintended toxic element ingestion, humans are constantly exposed to the ubiquitous use of food additives that have been shown to affect the gut microbiota, cause adverse effects and be carcinogenic [37]–[39]. Lack of choice and economic reasons lead the majority of the population to be exposed to them daily, and, coupled with genetics, epigenetics, and other factors, this leads to an increase in both chronic IBDs and cancers.

Prior literature has identified the need for early detection and management of GIT diseases [40], [41]. For example, gastric cancer (GC) was ranked sixth for cancer incidence and fourth for cancer deaths in 2020, while its incidence has been shown to be increasing in younger populations [42]. While early diagnosis leads to high survival rates of 90%, due to the lack of specific symptoms, more than 70% of cases lead to advanced stages and worse outcomes [43]. Gastroscopic screening has been identified as a means of early detection and reduction in GC-related deaths [44]. Furthermore, studies have shown that subjective aspects such as disgust [45] can prevent patients from complying with screening protocols. Treatment using a capsule device that eliminates a need for bowel preparation [21] or using a capsule instead of a tethered endoscope can increase willingness to undertake an exploratory GIT procedure [46].

The number of GIT-associated diseases is increasing while their symptoms can lead to other systemic or deadly consequences. Exploration of economically viable technological solutions to improve early detection and acceptability to patients is vital.

2.3 Ultrasound System Considerations

US is an acoustic wave above the defined audible maximum frequency range of 20 kHz. It can be generated through capacitive coupling, electromagnetic and piezoelectric effects. The latter is an ability of some materials, such as piezoelectric crystals and ceramics, to generate an electric field in response to mechanical stress and the primary method of generating US. In medical imaging, an US pulse is transmitted into tissue, and an echo signal, arising due to acoustic impedance mismatches between different tissue structures, is recorded. The imaging time is thus determined by the desired maximum imaging depth, while the US frequency defines the sampling rate of an imaging system.

A primary design challenge for any medical US system is the extremely high energy loss in the path from the transmitter to the receiver. Limited efficiency of a transducer, energy loss due to acoustic impedance mismatches between different media and acoustic attenuation due to absorption and scattering result in only a tiny fraction of the input power returning as the echo signal [47], [48] with a typical loss of 80 – 100 dB. The attenuation in tissue is proportional to the propagation depth and frequency [49], and at 28 MHz can reach a loss of approximately 9 dB/cm in human blood [50] and > 10 dB/cm for skin [51].

To improve the signal-to-noise ratio (SNR), a HV electrical pulse is necessary to transmit enough energy for a viable echo signal to be received from the desired penetration depth [52]. Advantageously, the thickness of the GIT wall varies across different regions of the tract and has been shown to be between 0.9 mm - 3 mm in thickness [53], resulting in maximum attenuation of approximately 6 dB for a round trip of an ultrasonic pulse. As it is significantly lower than that of a typical US system imaging from outside the body, the amplitude of the transmit signal can be reduced from hundreds to tens of volts or lower. A particular amplitude value is hard to define analytically, and can vary significantly based on the transducer, noise performance of the RX circuitry and the desired US image quality. In this work, due to the requirements of generating the HV supply in a capsule from a battery or a wireless-power transfer system, and being limited by the maximum voltage tolerances of the CMOS BCD technology, the TX pulse voltage chosen was 20 V. Nonetheless, the US system operates together with a low-noise, high-gain RX circuitry [54] and, thus, the TX amplitude can be reduced by increasing the SNR gain of the RX chain, transferring power consumption from the transmitter to the receiver.

Similarly to visual imaging, the resolution of an US image must be high enough to allow making clinically relevant decisions. The axial resolution of an US system is defined as the smallest distance that can be distinguished between two reflectors in the direction away from the transducer. It is directly proportional to the pulse duration and can be expressed as [55]:

$$d_{amin} = \frac{\tau c}{2} \tag{2.1}$$

where d_{amin} is axial resolution, τ is the pulse duration and c is the speed of sound in the medium. If a single cycle pulse is used, the formula equates to half the wavelength of the excitatory signal, identifying that the resolution is determined by the US frequency. In case of the 28 MHz array used in this work and an average speed of sound in tissue of 1540 m/s, the achievable axial

resolution is 27.5 µm at the centre frequency, indicating that lesions in the range of a few tens of micrometres could be potentially identified with the chosen transducer array.

While increasing the ultrasonic pulse frequency directly corresponds to better axial resolution, it imposes constraints on the system as the attenuation specification has to be met at the same time [49]. Coded excitation has been proposed as a means of enhancing SNR by prolonging the duration of the US pulse, leading to higher energy levels being emitted [56]. The pulse is also coded to correct the degraded axial resolution with the help of matched filtering, which correlates the transmitted code with the received radiofrequency (RF) signal [57]. This increases the complexity of both the transmit and receive circuitry, leading to higher power consumption, and was, thus, not pursued in this work due to power limitations in a CE.

The lateral resolution of a scan in the direction parallel to the face of the transducer is mainly determined by the width of an US beam and element directivity [58]. It is spatially variant and depends on the transducer's focal depth, aperture, centre frequency and bandwidth. Lateral resolution is maximised at the focal distance and deteriorates moving away from it. A phased array can be used to allow imaging at various depths and angles. Compared to linear arrays that determine the image shape based on the transducer setup, a phased array allows for full electronic steering of the beam by controlling the timing of the excitation of individual elements of the array [59]. Beam generation is conventionally performed by imposing delays between excitation pulses driving the array of elements. The delays are often implemented using high-frequency clock signals and, thus, impose high dynamic power demands on the system.

Integration of US devices with electronics was impossible for a long time due to HV and low-noise requirements. However, continuous technological process and device miniaturisation has led to improved US devices which can be integrated into probes [60] and potentially into ingestible CE [61] and intracorporeal devices [62]. As the imaging depth and attenuation is reduced by placing the scanner within the human body, µUS becomes a viable option for high resolution tissue imaging.

2.4 Conventional Endoscopy and Enteroscopy

2.4.1 Endoscopy

The first attempt at endoscopy is attributed to Philipp Bozzini (born in 1773), who used candle-illumination, mirrors and tubes to enable examination via human orifices. The devices

were primitive and rigid and, as a result, only allowed superficial access to the human body. A semi-flexible oesophagoscope took over a hundred years to be designed, followed by the first rudimentary camera integration in 1898 [63].

Current day endoscopy (also called push enteroscopy) is a giant leap forward from its predecessors. The conventional contemporary endoscope is a flexible probe with a steerable tip fitted with a camera, an illumination source, a biopsy channel and – sometimes - an US system – all of which allow for a multifaceted investigation and treatment of the upper GIT, the part of the small intestine most proximal to the stomach and the large intestine [64]. The probe is semi-rigid to allow for manual insertion and movement of the device into the human body using only the pressure applied by an examiner. Its flexibility is limited to prevent folding due to resistance, while still conforming to the anatomy of the GIT. As a result, push-enteroscopy is not possible in the small bowel due to its tortuous nature [65].

To reach deeper into the GI tract, a device-assisted push enteroscopy or CE is used [66]. The push enteroscopy approaches can be grouped into single or double-balloon enteroscopy and, more recently, spiral [67] and motorised spiral [68] enteroscopy procedures. The double-balloon procedure incorporates two inflatable balloons: one at the end of the overtube and one balloon at the tip of the enteroscope. By inflating the balloons with air, a grip on the small intestine is achieved, and it can be pleated backwards over the endoscope, achieving visualisation of the whole small intestine [69]. In the much newer spiral enteroscopy procedure, a semi-rigid, helical spiral moves independently of the enteroscope and drives it forward or backwards based on its rotational direction, similar to a drill. Both procedures allow for imaging of most of the small intestine and produce much better diagnostic yields than traditional endoscopy; however, they are time-consuming and require special training, patient sedation and two professionals to complete [70].

Alternatively, CE, discussed in Section 2.5, has been shown to reach sites beyond push enteroscopy capabilities without sedation and with a low chance of side effects [13], [14]. The technique utilises a pill-sized device with one or more cameras and onboard electronics for data compression and wireless communication. The swallowed devices are battery-powered, which suffices to image most of the small bowel at a minimum of 4 frames-per-second (fps). The image data is sent to external storage and is later evaluated by a medical professional. The main complication of CE is capsule retention, which has been shown to be infrequent, at around 1.4% in a 1000-capsule study [71] and can be further prevented by using fully-dissolvable capsules

to check patency before the introduction of the CE device [73]. The large amounts of imaged data generated by the procedure have also been addressed by some manufacturers with the help of artificial intelligence, reducing viewing time spent per patient [74], [75].

2.4.2 Ultrasound in Endoscopy

Endoscopic US, Figure 2-1, describes an imaging procedure that is carried out using an US array situated on an endoscopic probe [76]. Generally, higher frequencies, > 5 MHz, are used for medical imaging applications due to the required resolution of the scan [77]. The advantage of US over visual/video inspection is that it allows imaging within the tissue of the GI tract to evaluate biological formations that are obscured or only partially visible via an endoscope camera. US also permits imaging of organs proximal to the GI tract, such as the liver, gallbladder, pancreas and lungs, from within the bowel [78]. For example, US-guided fine-

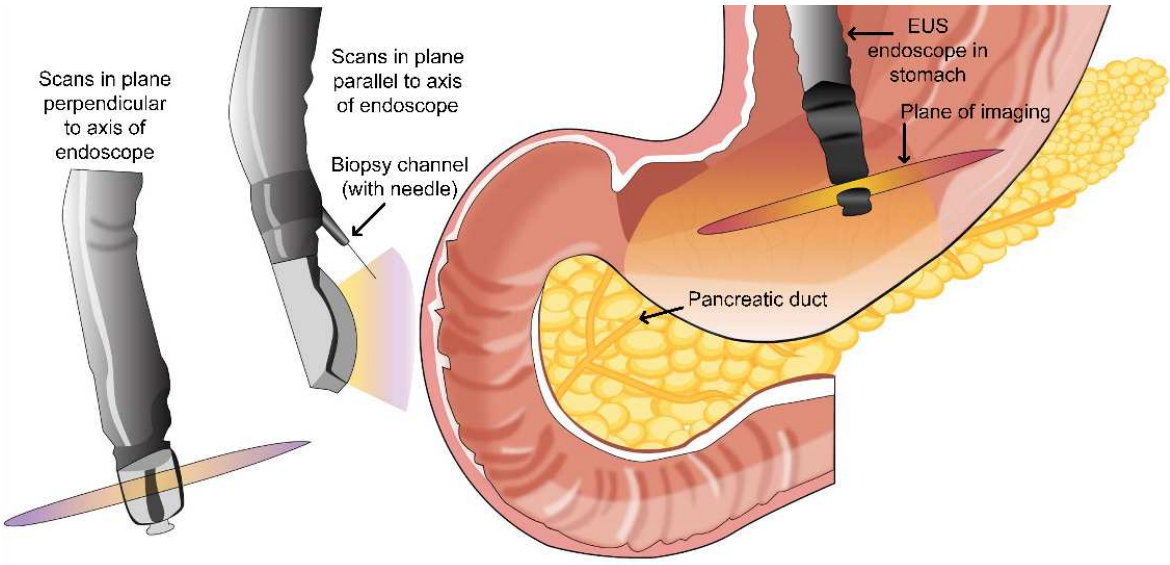

Figure 2-1 Endoscopic ultrasound procedure diagram

needle aspiration biopsy has been successful in identifying malignancies [79]. Finally, endoscopic US can also be used for monitoring various treatment procedures such as US-guided drainage of pancreatic fluid collections and cryothermal ablation [80] or future localised drug delivery systems [4].

2.4.3 Other Intracorporeal Ultrasound Probes and Devices

US system miniaturisation challenges have been extensively investigated in other applications not related to the GIT inspection, namely transoesophageal echocardiography (TEE) and intracardiac echocardiography (ICE).

TEE is a catheter-based procedure that uses the oesophagus as an access point for ultrasound imaging of the heart, Figure 2-2 (a). It is used in multiple heart-related conditions such as atrial septal defects and aortic valve replacement but requires general anaesthesia and an echocardiographer to operate the TEE probe [81]. Alternatively, the heart can be imaged with an intravascular ultrasound (IVUS) probe. The ICE procedure eliminates the need for general anaesthesia and is considered superior to 2D TEE for some applications [82]. In comparison to TEE, ICE probes impose significantly more size and power dissipation restrictions whilst providing adequate imaging resolution and speed.

A front-facing pitch-matched ASIC for a piezoceramic US array system detailed in [83] comprises 64 receive, 16 transmit elements and only four wires. A 13 MHz, 28 V transmit pulse

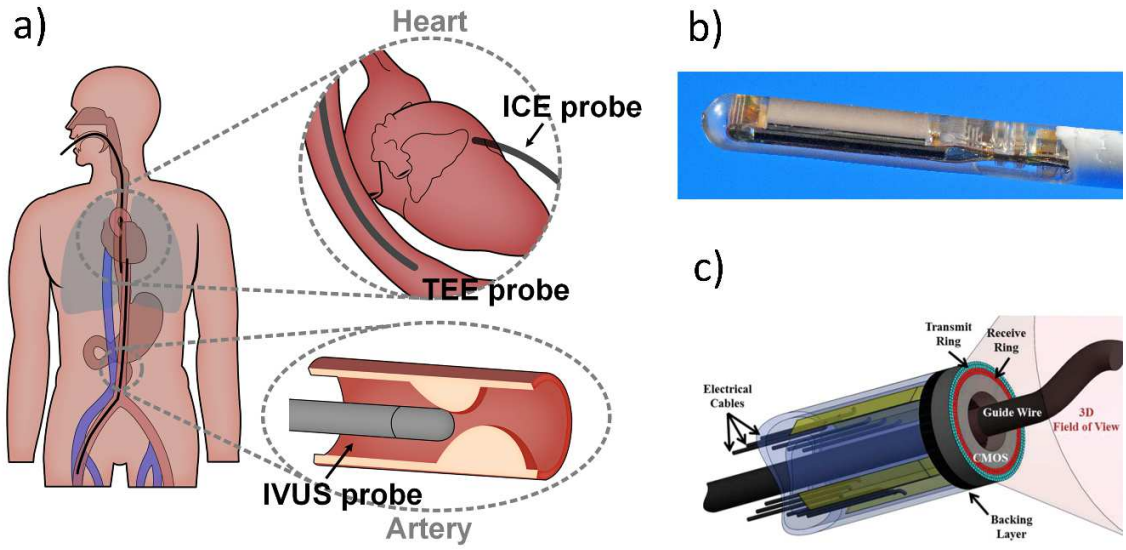

Figure 2-2 (a) Transesophageal echocardiography (TEE), intravascular echocardiography (ICE) and intravascular ultrasound (IVUS) (© 2021 IEEE) [18]. (b) Side-facing ICE probe (© 2016 IEEE) [84]. (c) Conceptual front-facing ICE probe (© 2014 IEEE) [88].

was used, with a total system power consumption of only 9.1 mW. A different implementation of a side-looking US array probe for 4D-ICE with 60 elements was proposed by Wildes et al., Figure 2-2 (b) [84], in which the total power dissipation was limited to 100 mW; however, it operated at a much higher transmit voltage of 90 V in order to improve the total system SNR.

Another miniaturised ultrasound system was reported by Chen et al. [85]. By applying a subarray beamforming scheme to achieve a 36-fold channel count reduction, a 144-element 5 MHz system was realised with a total power consumption of 131 mW (0.91 mW per channel).

As an attempt to improve TEE and ICE devices whilst meeting size constraints, researchers have turned to capacitive micromachined ultrasound transducer (CMUT) [86] and piezoelectric micromachined ultrasound transducer (PMUT) technology [87]. These ultrasound devices enable transducer integration with the general CMOS process, which reduces size and power requirements, leads to reduced parasitic effect, and simplifies the integration process of the probe with the electronics. Whilst CMUT integration utilises the already existing process steps of a CMOS process, PMUT integration requires additional steps for piezoelectric material deposition on the CMOS chip. A single CMUT chip operating at 20 MHz for a forwarding-looking IVUS probe was proposed in [88] with a total power dissipation of 20 mW over 56 transmit (at 25 V_{PP}) and 46 receive elements, Figure 2-2 (c). The configuration used 13 cables and acquired volumetric data up to 60 fps. A 36-channel front-end ASIC for a PMUT ultrasound system, using standard low-voltage CMOS technology, was proposed by Lee et al. [18]: the design used a 13.2 V_{PP} transmit pulse and achieved a total power consumption of 41 mW.

The dimensions of the proposed TEE and ICE systems are well below the CE device size used in medicine and have low power consumption even at high imaging rates, indicating that ultrasound imaging, which was possible only in tethered devices before, has the potential to be introduced in CE and implantable applications.

2.5 WHITE LIGHT CAPSULE ENDOSCOPY

2.5.1 Introduction

Such a device, Figure 2-3 [89], is a swallowable small camera device in the shape of a pill that measures around 11 mm x 26 mm (diameter x length) and travels through the GIT collecting white light images of the gut mucosa to identify irregularities [90]. The device takes

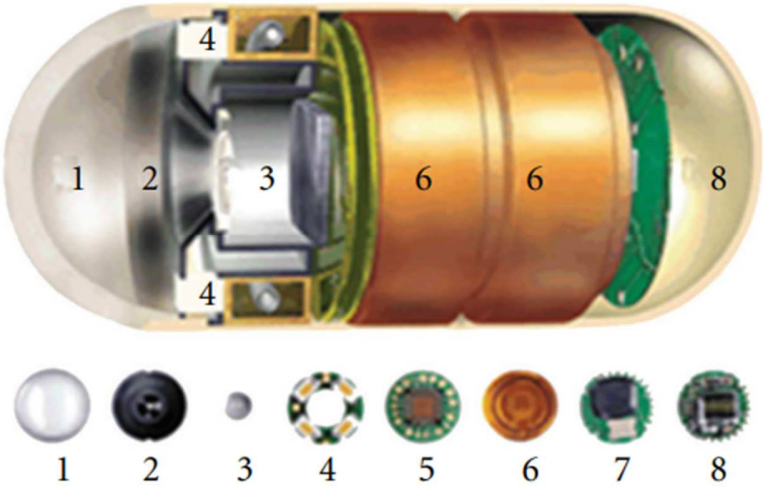

Figure 2-3. Inside of a capsule endoscope (M2A capsule): 1. Optical dome. 2. Lens holder. 3. Lens. 4. Illuminating light emitting diodes (LEDs). 5. Complementary metal oxide semiconductor (CMOS) imager. 6. Batteries. 7. ASIC. 8. Antenna. (© 2014 Nature) [89]

at least 2 fps and is expected to transmit data for around 8 hours. Currently, white light is the only modality approved for medical applications, whilst other modes, such as auto-fluorescence and US, are in the development stages.

The essential WCE endoscope components are shown in Figure 2-3 [91]. The general structure is shared among all white-light CE devices available on the market and includes two batteries, a processing unit to obtain and compress imaging data, an RF transmitter, a number of light-emitting diodes (LEDs) and a CMOS camera [92]. The capsule is usually activated just before ingestion into the patient's body, but a delayed start-up can be implemented to save power if the upper GI tract imaging is of no interest.

2.5.2 Commercial WCE Devices

The first commercial capsule endoscope, Pillcam SB™, was presented in 2000 by Given Imaging Ltd.[1] [93] and measured 11 mm x 30 mm, with a single front-facing camera and a maximum operational time of 6 hours. Since then, the system has been improved significantly, and several other companies have developed their own CE solutions. Table 2-1 summarises currently available commercial white-light devices on the market. Oesophageal and colonoscopic capsules are omitted due to close similarity in their structure: they utilise the same

[1] Now: Medtronic

technology as other capsules but operate at different frame rates and are sometimes equipped with an additional camera facing backwards to improve GIT coverage.

Table 2-1. Commercially available capsule specifications.

Device	Company	Size (mm)	Weight (g)	Imaging Sensor (Pixel Res.)	Frame Rate (fps)	Angle of View (°)	Battery Lifetime (h)
Pillcam® SB3	Medtronic	Ø11.4 x 26.2	3.0	CMOS (256 x 256)	4 - 6	156	8
Pillcam® COLON2		Ø11.6 x 32.8	3.0	CMOS x2 (256 x 256)	4 - 35	172	10
Pillcam® Crohn's Capsule		Ø11.6 x 32.8	3.0	CMOS x2 (256 x 256)	4 - 35	168	10
Pillcam® UGI		Ø11.6 x 32.8	3.0	CMOS x2 (256 x 256)	18 - 35	172	1.5
Pillcam® PATENCY		Ø11 x 26	3.3			N/A*	
Endo-Capsule	Olympus	Ø11 x 26	3.8	CCD (1920 x 1080)	2	160	12
Mirocam	IntroMedic	Ø10.8 x 24	3.3	CMOS (320 x 320)	3	170	12
OMOM HD	Jinshan Sci. & Tech	Ø13 x 27.9	6.0	CMOS (640 x 480)	2 - 10	172	12
CapsoCap Plus	CapsoVision	Ø11 x 31	4.0	CCD (221 x 184)	20	360	15

*A dissolvable capsule with no electronics.

The most recent Pillcam version SB3 [73] has an improved battery life of 12 hours achieved by using an adaptive sensing mechanism that varies the frame rate between 2 and 6 fps, based on the capsule's movement speed, which is determined by peristalsis of the GI tract muscles. The same strategy is employed by the OMOM capsule [94], which is also larger, but can reach 10 fps. The Endocapsule by Olympus [75], on the other hand, does not use an adaptive technology but has a similar system specification for the minimum operational time of 12 hours, using a CCD sensor for improved quality images.

The MiroCam device [95] uses human body communication to reduce the power consumption of the data transmission and, as a result, has a minimum battery life of 11 hours, even at a constant 3 fps. Human body communication is a method for transmitting information using the human body as the medium and, in essence, uses the same technology as an electrocardiogram [96]. It will be discussed further in Section 2.5.5.

CapsoCam [97] has four lower-resolution cameras placed perpendicularly to the capsule's length to image 360° around the capsule. However, its reduced resolution of 221 x 184 per camera results in a similar amount of data as other forward-facing camera devices.

The Sayaka capsule [98] is not FDA approved but offers a conceptually different way of addressing power requirements whilst offering a complete 360° bowel imaging. The device comprises two capsules placed inside each other. A permanent magnet and an electromagnet rotate the inner capsule in a stepped fashion to image the whole GI tract with a single camera sensor. Most of the available space in the device is occupied by the rotational mechanism, and thus wireless power transmission is required; the total delivered power can be significantly higher in comparison to battery-powered operation.

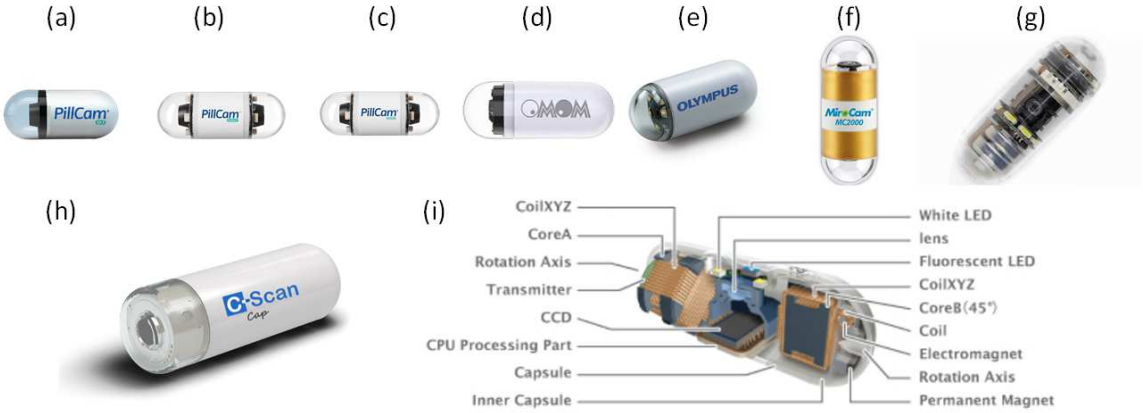

Figure 2-4. Commercially available capsules: (a) Pillcam SB3. (b) Pillcam Crohn. (c) Pillcam COLON 2. (d) OMOM. (e) Endo-capsule. (f) Miro-Cam. (g) CapsoCap Plus. Capsules in development and testing phases: (h) C-Scan Cap. (i) Sayaka capsule.

The CheckCap [99] is not yet commercially available, but pilot studies have already been carried out [76] – [78]. It is different from the other reviewed capsules as it uses X-ray as the sensing modality: the information generated by the device is similar to white-light imaging. This modality permits the CE procedure to be carried out without bowel cleansing, which, in turn, improves patient participation in the procedure [100]. Although the power requirements are reduced by substituting an active power source with a passive X-ray emitting system that uses a short-lived radioisotope, the minimum battery life of 8 hours relates to higher power requirements imposed by data acquisition and/or transmission subsystems.

Commercial WCE devices have made significant progress since the first introduction, doubling the minimum operational time from 6 to 12 hours and increasing the frame rate from 2 to 10 fps using adaptive control. Both advancements result in higher completion rates and diagnostic improvements. However, they can be regarded as modest gains over a two-decade period and only demonstrate how the WCE technology operates to the extent of technological limits.

2.5.3 WCE System Implementations

All the control and imaging tasks in a CE device, including data compression and transmission, will be performed by one of more ASICs. The power consumption of these chips depends on the complexity of the circuit, which is determined by the processing requirements as well as the duty cycle of the system. However, the total power consumption is highly dependent on the capsule subsystems: illumination LEDs, frame rate and data transmission.

A few capsule endoscope systems have been proposed in the academic literature over the years Table 2-2. A low frame rate capsule with a total power consumption of 24 mW was suggested in 2009 and achieved similar specifications as commercial capsules of that time [103]. Although the system dissipated only 1.3 mW in the digital block at the operational voltage of 0.95 V, it was operating at a supply voltage of 3 V, leading to energy losses in voltage regulators.

Wireless power transfer was demonstrated in [104]: although its total power consumption of 46.2 mW was well above commercial specification, it allowed for unlimited procedure time at 24 fps. A spherical capsule was also proposed for colonoscopy applications, but it was limited to 20 minutes of operational time and in image quality while being significantly larger, 4 cm in diameter. Although serving well as a proof-of-concept, these downsides are significant hurdles to be accepted by both patients and clinicians.

The research systems are already lacking in capabilities compared to commercially available devices regarding operational times, image quality or other parameters. Consequently, little research is now done on full system implementations for white-light modality.

Table 2-2. Comparison of WCEs from academic research.

Ref.	Year	Size (mm)	Frame Rate (fps)	Pixel Resolution	Battery Lifetime (h)	Supply voltage (V)	Total power (mW)
[103]	2009	Ø11.3 x 26.7	0 - 2	307 x 200	6 - 8	3	24
[105]	2013	Ø11.5 x 37	3	640 x 480	2 - 3	3	18 - 27
[106]	2015	Ø16 x 36	55	320 x 240	9.75	1.55	12.42
[104]	2016	Ø11 x 25	24	400 x 400	WPT	2 - 3.6	46.2
[107]	2015	Ø40	1 - 24	480 x 480	> 12	1.55	7.5
[108]	2017	Ø26	1.5	640 x 640	0.43	3.7	115

2.5.4 Data Compression in WCE

The main challenge in WCE is reducing chip area and power consumption without sacrificing image quality [61], [62], [111], whilst large compression ratios can be achieved due to the unique nature of the GI tract images among any imaging environments. In red-green-blue (RGB) colour space, 98% of image pixels are dominated by their red components and possess a different cross-correlation between pixel components [112] which allows simplifying the hardware compressor.

Multiple compression schemes have been proposed over the years, mainly built on three algorithms: lossless Joint Photographic Experts Group (JPEG-LS), differential pulse code modulation (DCPM) and discrete cosine transform (DCT) with additional strategies applied with them (Table 2-3). The intricacies of the algorithms are out of the scope of this study, but it is essential to note the critical characteristics of each approach. The JPEG-LS is a standard for lossless or near-lossless compression and is compatible with the row-by-row data stream provided by imaging sensors. However, it requires a 1.9 kb register array to store essential context and parameters, irrespective of the size of the image [104]. With DPCM, the image data can be compressed in a pipeline fashion without additional registers and this has approach has thus been pursued in many low power compressors [112]–[115], whilst DCT-based compression works on 8 x 8-pixel blocks, requiring additional buffer memory [116].

Compression circuits listed in Table 2-3 were designed for a varying number of pixels and data rates. As a result, the best comparison is based on a power per pixel (nJ) that uses the average power consumption of the system and the number of pixels per image. It can be observed that most implementations, except for a few outliers, achieved less than 2.51 nJ/pixel, while this value has not changed much since 2009. The other observation is that energy consumption mainly depends on a proposed compression architecture, and trade-offs are made with compression quality, it being lossless or near-lossless. The image quality must be high to maintain the clinical relevancy of the images and is reflected in the SNR of < 48 dB. Still, a compression rate of up to 93.6% has been achieved.

It is also important to note that most of the designs seen in Table 2-3 were implemented in a 0.18 µm feature size technology. Although it is a well-matured technology suited for analogue circuit designs, it is suboptimal for digital circuits, which could be integrated with lower-voltage 90 nm or 65 nm CMOS technologies. Still, complete utilisation of power-saving methods due to lower voltages cannot be achieved due to the lack of lower-voltage alternatives

to the 1.55 V silver oxide batteries used for WCEs. Nonetheless, some 0.18 µm designs have achieved sub-nanojoule energy-per-pixel expenditures [114], [117].

The most recent work on compression techniques has demonstrated a deep-learning algorithm for intelligent classification inside the capsule to reduce the number of bits transmitted and power consumption [118]. Two experiments with ~ 12k and ~ 42k training samples were carried out that resulted in a maximum classification accuracy of 99% and compression rate of up to ~ 76%. Similar improvements in deep-learning applications can be expected in other imaging modalities such as US [96] and fluorescence [97] imaging in the near future.

Table 2-3. Comparison table of publications on data compression for wireless capsule endoscopes.

	Year	Power (mW)	Energy per pixel (nJ)	Frames per second	Compression (%)	PSNR (dB)	Pixels	Primary Algorithm	Colour plane	Chip Size (mm)	Gate count	Technology (nm)	Compression quality
[119]	2006	6.2	11.1	8	90.9	47	320*288	JPEG-LS	RGB	3 x 4.2	41.4 k	180	Near-lossless
[120]	2009	1.3	2.11	2	84.7	46.43	640*480	JPEG-LS	RGB	3.4 x 3.3	23.4 k	180	Near-lossless
[113]	2011	0.77	5.87	2	80.0	45	256*256	DCPM	YUV	N/A	2 k	180	Near-lossless
[114]	2011	0.042	0.32	2	80.0	48	256*256	DCPM	YUV	0.7 x 0.7	592	180	Near-lossless
[116]	2013	7	1.11	24	91.9	35.7	512*512	DCT	RGB	N/A	N/A	65	Lossy
[121]	2014	0.33	2.51	2	80.4	43.7	256*256	Predictive	YEF	0.67 x 0.71	2.5 k	180	Near-lossless
[115]	2014	1.63	0.488	50	78.0	∞	256*256	DCPM	YEF	8 x 8	226	65	Lossless
[112]	2015	0.01	0.076	2	90.4	40.66	256*256	DCPM	YUV	0.134 x 0.134	2.3 k	130	Lossy
[122]	2016	4.2	1.18	24	72.8	46.2	400*400	JPEG-LS	RGB	4.8 x 4.8	27.8 k	180	Near-lossless
[123]	2016	4.704	0.0196	N/A	83.3	46.4	640*480	JPEG-LS	RGB	0.175 x 0.175	10.9 k	90	Near-lossless
[124]	2016	1.03	2.24	2	93.6	40.9	480*480	DCT	RGB	1.5 x 2.0	N/A	180	Near-lossless
[125]	2017	0.94	N/A	N/A	85.3	∞	640*640	Predictive	RGB	0.172 x 0.72	3.78 k	65	Lossless
[117]	2017	0.88	0.167	20	74.6	46.5	512*512	DCT	RGB	0.96 x 0.54	1.8k	180	Near-lossless
[126]	2018	0.78	1.26	2	75.0	N/A	640*480	DCPM	YEF	0.5 x 0.85	N/A	65	Lossy
[127]	2019	4.5	N/A	N/A	80.7	∞	352*240	JPEG-LS	RGB	0.24 x 0.24	4.8 k	180	Lossless
[128]	2020	1.63	21.05	2	82.7	N/A	256*256	DCPM	YUV	N/A	N/A	N/A	Near-lossless

2.5.5 WCE Data Transmission

Data transmission has been shown to constitute a significant fraction of the total power use and defines the maximum data throughput from the visual sensors. The majority of commercial and research capsules use RF for communication. Most commercial capsules operate at around 2 Mbps (megabits per second) transmission rate, but low energy power transfer is possible for much higher data rates. In 2009, Thoné et al. identified the need for a system to operate below 500 MHz to reduce attenuation and presented a system based on frequency shift keying modulation to achieve a 2 Mbps rate with 2 mW consumption - the state-of-the-art in low energy of the time [129]. As a result of new techniques and semiconductor technology miniaturisation, data transfer power requirements have been substantially reduced: a 33 Mbps FinFET-based transmitter operating at 144 MHz was shown to use only 1 mW from a 0.85 V battery [130], whilst the system presented by Youn et al. [131] achieved a 40 Mbps transmission rate while consuming 2.66 mW, thus achieving 20 times the data throughput with only a 30% increase in power consumption in comparison to Thoné et al. [129].

Human body communication (HBC) is an RF/EM data transfer alternative. The technology uses the human body as the propagation medium, and due to the lower frequency of a transmitted wave, it results in lower energy requirements and less attenuation in tissue [132]. Transmission rates of 6 Mb/s with 3.7 mW consumption have been demonstrated to be possible [133]. The main disadvantage of an HBC system is the limited data transmission rate and the need for multiple electrodes to be attached to a patient's body. Still, the application of the technology in the MiroCam and other feasibility studies have shown that HBC systems are viable for WCE data transfer whilst meeting operating safety limits and maintaining leakage currents below 10 μA in normal conditions or 50 μA for single fault conditions [134].

New communication strategies have increased data transmission rates whilst reducing power requirements, opening the door for improved image quality or integrating additional modalities into the capsules without detrimentally affecting the rest of the system.

2.5.6 Energy Source and Wireless Power Transfer in WCE

All FDA approved CE devices use clinically approved silver oxide batteries as the power source [135]. The cell's capacity is determined by its thickness and width. Based on commercial CE device specifications, the maximum battery diameter is 9.5 mm to fit in a capsule enclosure, while its thickness and stored energy vary, e.g., storing 53 mAh of energy per cell at 3.6 mm in thickness.

The literature indicates that two batteries are used in a series configuration, providing a 3.1 V supply at 53 mAh. Based on the minimum operational time of current CE devices at 12 hours, this results in approximately 13.7 mW power consumption – a 31.5% decrease in total power consumption over the last decade [135]. In the case where a newer CMOS technology permits operation at 1.55 V, but the minimum operational time is the same, the power consumption could be doubled to 27.4 mW, based on the doubling of the charge available from parallel-connected cells.

The alternative energy source to batteries is wireless power transfer (WPT) which allows energy transfer through a medium without interconnects. The technique is based on a wave generating transmitter and a receiver which converts the incident wave into electrical energy to be delivered to the load. The main methods of WPT for biomedical applications are based on capacitive or inductive coupling, RF/EM, acoustic (US) and others [136]. Still, due to the non-uniform capsule movement inside the bowel [137] and varying orientation of the bowel structure, misalignment of the transmitter and the receiver occurs, and power delivered to the device varies significantly. As a result, inductor-based WPT has been explored as the most promising approach, exemplified by the battery-less Sayaka capsule.

To address the receiving coil's misalignment issue, a 3-D cross-type receiver system was proposed by Khan et al., Figure 2-5 (a) [138], which reached efficiencies of 0.9% and delivered power of 90 mW but demonstrated only an 8.4% variation with change in coil orientation. Improved power transfer efficiency and magnetic field distribution using an improved 2-3D

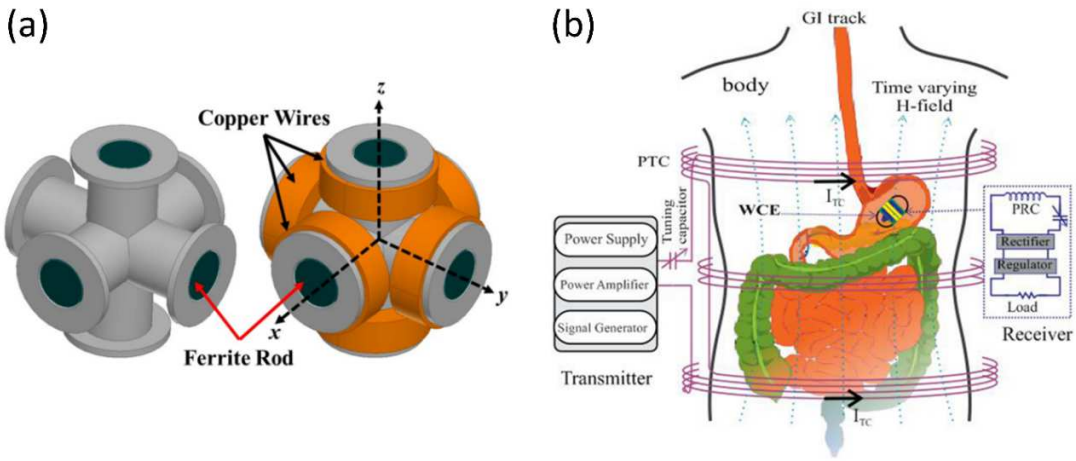

Figure 2-5. (a) Proposed 3-D cross-type RX coil with (right) and without (left) copper wires (© 2019 IEEE) [138]. (b) Schematic of a magnetic resonance-based wireless power transfer system for wireless capsule endoscopy (© 2018 IEEE) [139].

power receiving coil configuration and a three power transfer coil setup was also demonstrated, Figure 2-5 (b) [139]. The system under test reached more than 8% efficiency whilst transferring 758 mW, although the tissue attenuation was not included. Similar results in air were achieved in [140], reaching 750 mW transfer and 3.55% efficiency. Further attenuation of the transmitted signal can be expected for time-varying magnetic fields above the frequency of 30 MHz inside the human body, but most of the presented WPT systems operate below this value [141].

The potential for wireless power transfer is not unlimited – the power dissipation in a capsule must be limited to ensure the temperature due to attenuation in the tissue does not exceed 43°C and damage the tissue surrounding the capsule [142]. Lay et al. [95] identified the power dissipation-temperature relationship using a power resistor inside a test capsule, finding that power dissipation of 100 mW is the safe upper limit inside the GI tract.

Based on current WCE devices that use 20 mW of power on average at most, it can be concluded that an additional modality requiring 4x the power can be implemented whilst maintaining safe operating limits, given that WPT is available.

2.6 NON-WHITE LIGHT CAPSULE ENDOSCOPY

2.6.1 Ultrasound

The main drawback of WCE imaging is the failure to identify disorders early if they lack visual indicators in the superficial layer of the GI tract. At the same time, alternatives such as virtual endoscopy using MRI, or the conventional US are expensive or not accurate enough and lead to a need for cheaper and safer imaging modalities.

µUS is an imaging method that uses higher frequency ultrasound (> 20 MHz) than conventional US systems [143]. The higher frequency allows for increased resolution and, thus, can be employed to differentiate between different layers of tissue. It has been shown that µUS can distinguish premalignant structures in tissue where traditional three-dimensional high-resolution US imaging failed [144]. A concept capsule for µUS imaging was proposed by Cox et al., Figure 2-6 (a) [145]. The study investigated the quality and usefulness of µUS images of the bowel wall, comparing them to histology and establishing µUS as suitable for direct imaging of the GIT wall structure. A potential to characterise a lesion *in situ* to reduce the number of invasive follow-ups was also identified. Ultrasound can also be used to evaluate the physical

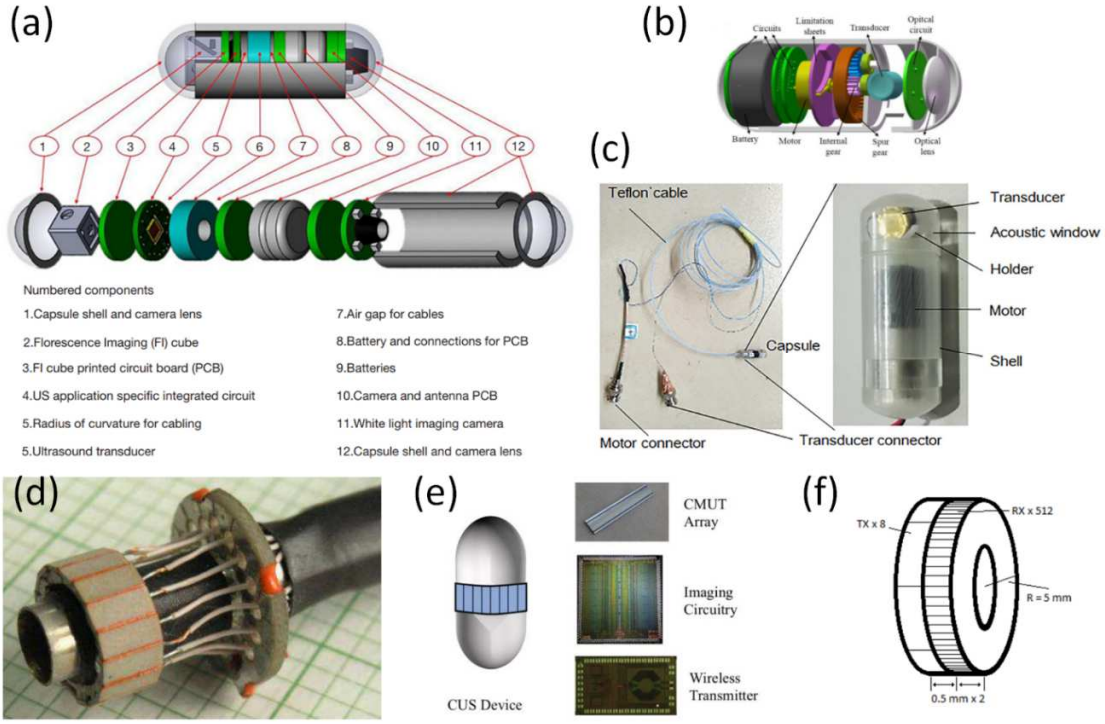

Figure 2-6. (a) Conceptual capsule endoscope [145]. (b) 3D model of a CE with a single element rotatable transducer (© 2017 IEEE) [149]. (c) Tethered system tested with the single element transducer [150]. (d) 16-element circular array tested in TROY project [151]. (e) CE device with CMUT electronics (© 2017 IEEE) [148]. (f) Concept ringular array with separate TX and RX arrays (© 2017 IEEE) [147].

and acoustic properties of the imaged tissue, named qualitative ultrasound. Based on *in vivo* measurements on porcine subjects and *in vitro* measurements on phantoms, it was concluded that µUS data allowed both quantitative and qualitative evaluation of changes in the GIT.

This data can be used to detect cancerous lesions before they become visible in the lumen of the GIT, leading to better survival rates and disease outcomes. It can be also used to identify and monitor chronic inflammatory bowel diseases such as Ulcerative colitis and Crohn's disease, both of which also increase the risk of bowel cancer. Furthermore, 1 in 5 people with ulcerative colitis have severe symptoms that cannot be improved with medicine, and 60 – 75% of patients with Crohn's disease require surgery to remove damaged tissue and treat complications [146]. µUSCE could be used to provide accurate data for better monitoring practices, leading to faster response times and management of the disease. In cases where surgical intervention is required, it could be used to identify flare-ups and GIT regions affected by the illness, minimising the healthy tissue that is removed during surgery.

Tetherless US implementation restricts the design even further, as the need for wireless data compression, transfer, and local HV generation all rely on battery power. A 25 MHz

circular array was proposed and validated through simulation by Lay et al., Figure 2-6 (f) [147]. The system incorporated two arrays with 8 transmit and 512 receive elements and had a power budget of 100 mW. A synthetic aperture was used to reduce the complexity of the electrical driving and receive circuits and reduce the power consumption by lowering the electrical load from the transducer elements at any given time. Similarly, a 128 element CMUT implementation was manufactured and tested for capsule applications at 7.5 MHz by Wang et al., Figure 2-6 (e) [148]. Although the frequency was too low to be useful for intramural imaging of the GI tract, its power consumption was only 5.4 mW at 4 fps, with a 20 V transmit pulse created with an integrated CP. A different approach was proposed by Wang et al., Figure 2-6 (b) [149], and Qiu et al., Figure 2-6 (c) [150], where a 49 MHz, single element transducer was used in tandem with a mechanical system to produce a full 360° imaging coverage around the capsule. The system optimisation was not the purpose of the study and it therefore utilised commercially available components. A single channel data path consumed 140 mW at ±48 $V_{pp,}$ and wireless transmission of more than 3 Mbps used 415 mW; the total average power consumption of the system was 337 mW.

The manufacturing of a circular US array is a challenge for imaging applications at frequencies above 100 kHz because of the reduced element size. A 16-element radial array was manufactured and tested *ex-vivo* as part of the TROY project, Figure 2-6 (d) [151], but the resultant array was larger than the dimensions required to fit into an ingestible capsule. Therefore, the feasibility of a larger number of elements (128 – 512) and smaller-scale integration was not proven. Wang et al. [148] tested their electronics with a straight linear array, and Wang et al. [149] used a single element device with a rotary mechanism to image a radial part of the bowel. The circular array with 512 elements proposed by Lay et al. [147] was only tested in simulations. Given today's technology, a single-chip radial CMUT is not manufacturable as a single CMOS chip.

Generally, high peak currents and voltages are required for an US transducer to transmit an ultrasonic pulse with the required amplitude. An integrated CP is the most compact solution in CE and some wearable applications [130] [131]. For example, Wang et al. [148] used a 17-stage CP to power an US pulser and showed how the transmitter excitation voltage directly corresponds to the surface pressure observed. CP efficiency is directly and inversely correlated to the number of stages required, which can be excessive in battery-powered devices with low

supply voltages. Excessive current draw from the HV rails can be detrimental to the operational time, and means of reducing it or, alternatively, reducing HV requirements have been sought.

The overall power consumption is significantly reduced when using synthetic aperture imaging, which reduces the total number of active array elements at one time [147]. This diminishes dynamic losses associated with switching and parallel processing but does not eliminate the average power as the total number of transmit events taken to compose a single image increases. As a result, lowering the excitation voltage of a transmit pulse can be beneficial in improving the efficiency of the HV generator. Coded excitation was identified as a way to improve the SNR of μUSCE systems, permitting lowering of the pulser's supply voltage [152], although processing and pulser complexity increases. To the best of the author's knowledge, no studies evaluating hardware complexity and cost versus HV generation requirements exist.

US scans can generate large amounts of data. For example, a 512-element US imager operating at 30 MHz centre frequency and using a 10-bit 125 Msps analogue-to-digital converter (ADC) to interrogate a 6 mm depth would generate 5.4 Mbps. If higher frequency or higher resolution images are required, this value becomes even larger and could not be accommodated by traditional wireless transmission protocols. As discussed in Sections 2.5.4 and 2.5.5, even lower amounts of data have been a significant challenge for WCE and have led to two-decade-long analysis and development to reduce power losses without sacrificing image quality. In contrast, the compression specification process of USCE is not yet known due to the absence of practical implementations of such devices. Some examples of near-lossless compression using entropy-coded DPCM [153] have achieved reduction ratios up to 4.39, while higher ratios up to 30x have been achieved using lossy algorithms [154], [155].

Furthermore, for USCE devices, the importance lies in understanding the balance between the compression rate, hardware requirements, power consumption and image quality. Such developments are yet to be shown, but it is evident that US data acquisition, processing and transfer will cause the greatest difficulties in a wireless capsule endoscope. This also leads to the necessity of ensuring minimum power requirements for the rest of the system's components.

To conclude, in contrast to WCE, USCE is still in its infancy. Previous work has identified challenges and possible solutions for incorporating an US system in a capsule, but the achievements have been limited to tethered test systems. A practical battery-powered system requires further work on both the transducer implementation and the sensing front-end. As a fully integrated prototype is yet to be tested, significantly more work is needed to verify the

overall system capabilities, diagnostic potential, safety, and viability before a clinically relevant device can be created.

2.6.2 Fluorescence Imaging

Like µUS imaging, fluorescence imaging can help differentiate between healthy and diseased tissue and is particularly useful for detecting early-stage carcinomas, when they are penetrated below the mucosa, the top layer of the GIT wall. HV generation and excitation is often required in such systems as well, having the potential to be integrated together with the µUS modality or as its lower-power alternative.

Fluorescence imaging can be split into two types: autofluorescence (AF) and photodynamic imaging, Figure 2-7 (a) [156]. The former relies on the intrinsic characteristic of some substances found in tissue, such as collagen, to generate fluorescence: cancerous tissue significantly lacks AF when excited by particular frequency light. Hence, in photodynamic imaging, fluorescent drugs are administered systemically, and imaging relies on an increased uptake in the cancerous tissue [157]. AF imaging requires no additional photo synthesisers but is a weak phenomenon and requires higher intensity excitation light and high sensitivity sensors compared to photodynamic imaging.

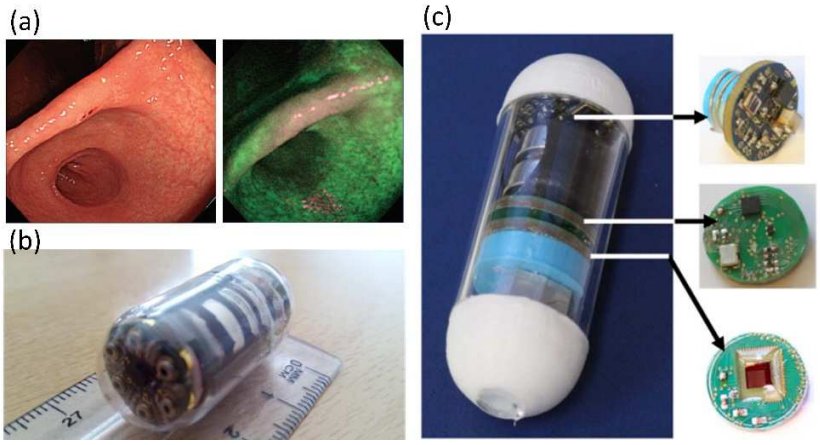

Figure 2-7. A representative case with flat elevated type early gastric cancer. On the left, a flat elevated lesion of 25 mm diameter is depicted by white-light endoscopy. On the right, the same lesion shows a magenta colour in autofluorescence imaging [155]. (b) Infrared fluorescence CE system (© 2015 IEEE) [158]. (c) A SPAD-based system [12].

Most AF capsules are based on SPAD technology due to manufacturing compatibility with standard CMOS technology [158]. These devices are diodes that are reverse biased above their breakdown voltage to the point where a single photon incident on the active silicon area of the sensor can create an avalanche event. The current through the diode during the event rises

exponentially, and the device must be reset afterwards – in this manner, individual photons can be measured.

Several capsule endoscopes for fluorescence imaging have been reported over the years. A full infrared (IR) fluorescence CE device was reported by Demosthenous et al., Figure 2-7 (b) [159], who designed the system using commercially available components (approximate cost: $500). Rather than generating high-quality images, fluorescence intensity was measured, which reduced the amount of data and enabled onboard storage. The capsule was operated at two samples per second and consumed 6.3 mA from a 3.3 V battery, equivalent to 20.8 mW power consumption. An approximately 7x cheaper prototype was also proposed [160]. However, its power consumption was 49 mW. A capsule endoscope for auto-fluorescence imaging using a 32 x 32 SPAD array was presented by Al-Rawhani et al., Figure 2-7 (c) [12]. An integrated charge pump was used to bias the diodes at 18.5 V and simultaneously power a row of 32 elements. The total power consumption of the capsule was measured to be 30.9 mW from a 3 V battery at 1 fps. The ASIC incorporating the charge pump and the SPAD array drew only 1.79 mA on average, while the LEDs consumed 5.2 mA.

To conclude, based on state-of-the-art fluorescent imaging, the power requirements of current capsule fluorescence imagers are significantly higher than the already-matured WCE. Nonetheless, SPAD sensors can achieve low power consumption and provide considerably more data than just intensity measurements without incurring intolerable energy losses, at the cost of additional circuitry and energy losses from onboard HV generation.

2.6.3 Other Capsules

Apart from white light, ultrasound and fluorescence, other sensing modalities exist, such as for motility [161], pressure [162] and optical coherence tomography [163]. Even more effort is put into CE movement control [164]–[166]. Enabling controlled movement could shorten the capsule procedure and allow partial or complete automation, so that medical professionals could be able to inspect specific regions of the tract in more detail and could apply targeted drug delivery and biopsy procedures. Automated imaging systems have already been introduced commercially [94] and have been shown to provide better results at the cost of longer procedure times [167]. These CE research areas are out of the scope of the present review, hence this brief discussion.

2.7 CONCLUSIONS

The GIT is a very complicated system and one of the harshest in the human body due to its constant exposure to the external environment through ingestion of food and drink. State-of-the-art commercial and research WCE technology shows that current white-light capsule devices have moderately advanced from the first devices more than 20 years ago and are now used to investigate the small intestine and other parts of the GIT. At the same time, further advancements in alternative sensing modalities that permit deeper tissue imaging or cancer cell identification, namely ultrasound and fluorescence, may significantly improve diagnosis yields by complementing visual gut inspection.

Complete system integration of a multi-sensory device, economic viability, and acceptance by medical professionals of such systems was not discussed in this chapter, and significant challenges remain to a commercially viable product. Nonetheless, continuous miniaturisation of the CMOS technology, coupled with improvements in wireless power transfer, machine learning, and robotics, indicates that a multi-modal CE system is feasible. It is not hard to foresee that, with further developments in wireless power transfer, robotic manipulation, and machine learning, in time, a multimodal CE procedure will be a semi-automatic process. The capsule will be controlled autonomously until a region of importance is detected, and the practitioner's intervention will be required for a more in-depth examination.

Power consumption and imaging quality have been the major challenges in WCE devices. Implementation of μUS in a capsule is even more challenging due to increased supply voltage and high data rate or data processing requirements. Previous work has laid the basis for μUS CE viability, but developing an optimised ASIC is crucial to meet specifications and enable tetherless *in-vivo* experiments and further advances in integration.

3 FULLY INTEGRATED HYBRID CHARGE PUMP FOR LOW CURRENT APPLICATIONS

3.1 INTRODUCTION

Chapter 2 discussed CE devices and high-voltage specifications imposed by US and fluorescence imaging systems. Prior work has indicated that CPs are often chosen as a HV generator due to its integration capabilities. CP designs have been widely explored in the literature analytically and experimentally, but a need still exists to improve the area / volume requirements of these circuits, particularly for biomedical applications (e.g., implantable, ingestible, wearable devices). This chapter therefore describes the development of a 20 V hybrid charge pump (HCP) for low-current (< 100 μA) applications, based on CCCP and new self-biased SPCP circuits for biasing integrated circuits for applications with a high level of integration and optimised performance.

The chapter begins with a focused review of switched inductor and switched capacitor circuits for integrated high-voltage generation, followed by a comparison of different CP topologies with regards to efficiency and technology requirements. The following section discusses the proposed HCP and is split into two subsections that focus on single-stage CC and four-stage SP subcircuits in detail. Optimisation of the SP stage is provided based on an analytical CP model and parasitic values extracted from the design environment. A comparative four-stage Dickson charge pump (DKCP) is then briefly presented, and the results of the manufactured and tested CCCP, SPCP, DKCP, and HCP are described.

Discussion of the results follows, concentrating on the simulation and measurement mismatches observed in the SP design during testing. The discussion is complemented by potential circuit solutions for improving the performance of the self-biased SP stage. The specification for the CP changed over the duration of the project and, as a result, these fixes were not explored further in simulations or manufacturing.

3.2 Design Framework

A diagram of a potential HV system is shown in Figure 3-1. The supply voltage is generated from two serially-connected 1.55 V silver oxide batteries, a standard choice for CE applications. Although connecting batteries in this manner reduces the total available charge by half, it double the supply voltage and allows the total number of stages required in the CP to be reduced by half. To limit dynamic losses due to switching, the CP's clock frequency was limited to 20 MHz. A drop-out regulator is used for the low-voltage domain, and another one can be used for the 3.1 V, but it was omitted from the diagram for simplicity. In this application the CP is powered directly from the 3.1 V supply.

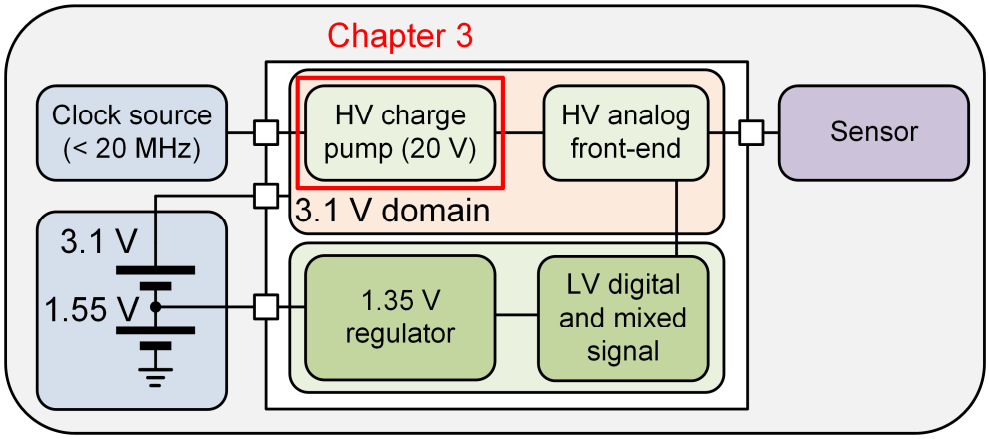

Figure 3-1. Battery-powered HV sensing front-end.

3.3 Converter Type and Circuit Topology Comparison

HV generation from lower voltage supplies for intracorporeal applications can be achieved with the use of switched-inductor or switched-capacitor based converters, which, on a fundamental level, utilise passive components for intermittent energy storage. It is worth noting that transformers are excluded from this discussion due to their size constraints. A basic boosting switched-inductor regulator is shown in Figure 3-2 (a). When the switch S_{A1} is enabled, the current flows from the supply to ground through the inductor L_{A1}, storing energy in its magnetic field. When the switch is disabled, the inductor must maintain the current flow and, thus, the magnetic field polarity is flipped, leading to a boost in voltage at node V_A whilst C_{LOAD} gets charged through diode D_{A1}. A basic boost switched-capacitor circuit is shown in Figure 3-2 (b), although most designs use active switches instead of diodes to improve efficiency. The circuit is controlled by the voltage V_{CLK}. When S_{B1} is connected to ground, the top plate of capacitor

C_{B1} (i.e., flying capacitor) is charged through diode D_{B1}. When S_{B1} connects to V_{DD}, the voltage at node V_B is the sum of the potential across the capacitor and V_{DD}, and the capacitor is discharged to V_{OUT}. By quickly alternating the states of S_{A1} and S_{B1}, respectively the two converters can produce boosted voltages at their outputs.

Both converters can achieve high efficiencies, but their integration capabilities are different. A switched inductor supply utilises only a single passive component, the inductor, which is challenging to implement in standard CMOS technology, whilst the switched capacitor circuit requires a number of capacitors to reach voltage gains higher than two but can be realised using the several integrated capacitors available in the bulk CMOS technology. Area and interconnect requirements of CP designs based on discrete elements quickly become excessive compared to switched inductor supplies.

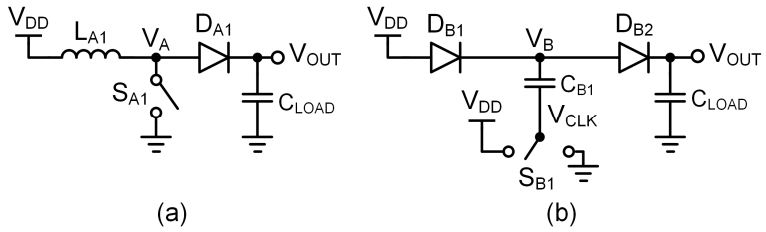

Figure 3-2. Basic diagram of: (a) boost switched inductor converter. (b) single stage Dickson charge pump

A comprehensive review of voltage-boosting techniques was published in 2017 by Forouzesh et al. [168] and the techniques will not be explored to the same extent here. Nonetheless, the capabilities of integrated converters for voltage boosting must be understood to make the most suitable choice. A comparative study [169] between the two types of converters has shown that both types can achieve similar peak efficiencies. Switched capacitor converters operate at lower power density figures, in the range of a few mW/mm^2, but this can be improved by a factor of 1000 with the use of SOI (silicon-on-insulator) technology or deep trench capacitors [170]. Switched inductor converters aim for higher density and higher power applications. Still, they necessitate the monolithic inductor or system-in-package (SiP) approach, which complicates the manufacturing process and increases costs. Only recently, fully integrated voltage regulators have been tested for commercial applications by Dialog Semiconductor [171] and integrated transformers with an inductance density of 108 nH/mm^2 were manufactured by Ferric Inc. [172]. However, it is essential to note that most switched inductor innovation focuses on processing applications that demand accurate regulation, low

voltage and high supply current, as well as improvements in power density [173]–[176], rather than high-voltage and low current integrated sensing applications.

The work on voltage boosting using highly or fully integrated inductors is also developing rapidly. A 1.8 V to 6 V fully integrated converter was proposed by Richelli et al. and others [177]–[179], which, at a 3 V input, achieved an output of over 14 V, but it only had 28% efficiency at 600 µA output current. A fully-integrated design comprising two chips was presented in [180] that achieved 20 V at a 29.6% efficiency. The overall efficiency of these devices is limited compared to some CP designs that can achieve close to 50% efficiency and multiplication ratios of > 10 in standard CMOS technology [181]. Nonetheless, the field is constantly evolving. With the trend of decreasing feature sizes and increasing operating frequencies, coupled with innovation in solenoid implementation on silicon, better designs are expected to follow [182], [183].

Different CP architectures are used to achieve voltage boosting, and they vary in their switch and capacitor voltage tolerance requirements as shown in Table 4. The first published charge pump circuit was developed by Cockcroft-Walton and consisted only of diodes and capacitors [184]. Its applications required large capacitors to counter the stray capacitance C_{PAR} effects. The Dickson charge pump [185] was proposed for integrated applications where capacitor sizes are limited and the proportion of C_{PAR} is more significant. Over the years, other topologies have been proposed, namely cross-coupled [186]–[188], Fibonacci [189]–[191], 2N [7], [192]–[194] and serial-parallel (also: heap) [195]–[199] CPs. Extensive comparisons and analyses of different topologies have been produced in [200]–[202].

Table 4. Parameters of different charge pump topologies.

	V_{MAX} Gain (GV)	Current Efficiency	V_{CAP} (Max)	V_{SW} (Max)
Cockroft-Wilton	N + 1	1/GV	1	1
Serial-Parallel			1	N
Cross-Coupled			N	1
Dickson			N	1
Fibonacci	F(N+1)		F(N-1)	
2N	2N		2N-1	

The DKCP and CCCP charge pumps are now the two most popular topologies for integrated applications for two reasons. They have a single V_{DD} drop across the switches, desired in bulk CMOS technologies, and minimal performance degradation due to parasitic capacitances

compared to other topologies such as exponential, Cockcroft-Walton and others. The number of inputs in a charge pump determines the sensitivity to parasitic effects. All topologies, excluding DKCP and CCCP, only have one or two inputs through which a finite amount of charge can flow. This charge is then used to increase the voltage with a progressively more significant difference in every stage, which leads to a charge loss proportional to $Q_{PAR} = C_{PAR} \cdot \Delta V$, where Q_{PAR} is the charge required, C_{PAR} is the parasitic (also: stray) capacitance in the stage, and ΔV is the voltage difference between two charge pump phases. As a result, the charge loss between the input and the output is accumulated and increasingly proportional to the higher number of stages in the circuit. Alternatively, in linear designs, the amount of charge injected and lost in every stage is constant, and the parasitic effects on the output current and efficiency are mitigated [203].

The effects of parasitic capacitances on a linear CP's output can be explained using a single-stage DKCP where MOS switches are connected in a diode configuration, Figure 3-3. Assuming steady-state, when the switch S_1 is connected to ground, capacitor C is charged through M_1 to V_{DD}-V_{DIODE}, where V_{DIODE} is the diode drop-out voltage. Unless the output voltage V_{OUT} is below $V_{DD} - 2V_{DIODE}$, no current flows through M_2. The switch is then connected to $V_{DD,}$ node V_X becomes $2V_{DD} - V_{DIODE}$, and the output is charged to $2(V_{DD} - V_{DIODE})$. In most cases, the output is connected to a constant resistive load, which leads to an output ripple proportional to the output capacitor value and affecting the steady-state output voltage. Assuming that a CP with N stages is used, the output can be written as [204]:

$$V_{OUT} = V_{IN}\left(1 + N\frac{C}{C + C_{PAR}}\right) - (N+1)V_T - \frac{I_L T}{C} \tag{3.1}$$

where V_{IN} is the input voltage, C is the stage capacitance, $C_{PAR} = C_T + C_B$, , I_L is load current, and T is clock period with a 50% duty cycle. This expression is strictly valid for linear CPs only, but illustrates that parasitic capacitances must be minimised to improve the desired output voltage at a specific load current, whilst other variables are constant.

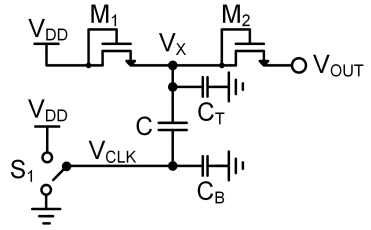

Figure 3-3. Single stage Dickson CP.

Regardless of the circuit topology, losses in the main CP path depend on the region of operation [205]. Under the slow-switching condition (SSC), a complete charge transfer between stages happens during the clock cycle ($T >> RC$, where R is the "on" resistive component and C is the total node capacitance). The losses incurred in the circuit depend on the parasitic capacitances charged every cycle (C_B and C_T in Figure 3-2 b). If the operational frequency is increased, a fast-switching condition (FSC) is reached ($T << RC$), and the cycle duration becomes too short for complete charge transfer to take place. Instead, it is limited by the equivalent switch resistance, which leads to an increase in the output impedance and energy losses. It has been shown that the optimum operating point for any charge pump is the transition point between SSC and FSC [206]. The last condition occurs when the output current draw is high enough to completely discharge flying capacitors in every cycle. With the right design choices, this region is never reached. Other losses, such as master clock generation, non-overlapping signal generation and shoot-through currents in the drivers are also present in the system but are excluded from efficiency evaluations of the primary voltage amplification path for practical reasons.

In integrated applications, due to the proximity of the capacitor plates and neighbouring interconnects, substrate, etc. the parasitic effects are more extensive than in standalone capacitors, leading to increased losses. In bulk CMOS, three types of capacitors are available: metal-insulator-metal (MIM), metal-oxide-metal (MOM) and metal-oxide-semiconductor (MOS). The latter has the highest capacitance per unit area, but its value is highly dependent on the voltage drop across it. This leads to non-linearity, which degrades performance – although this effect is exploitable to increase the efficiency in some charge pump designs [207].

The MIM capacitor (MIMcap) is a dedicated CMOS component usually situated in the top two metal layers with a limited operating voltage of a minimum of 5.5 V in the technology used, limiting its application in high-voltage designs[2]. Its parameters depend on the CMOS mask settings, and it had a density of 1.5 fF/μm^2 in the TSMC 0.13 µm process. Due to their placement further from the substrate and other routing nets, MIMcaps exhibit low parasitic degradation.

The MOM capacitor (MOMcap), on the other hand, is based on interdigitated metal tracks and is placed across multiple metal layers. The technology defines the minimum distance between the tracks; no additional manufacturing steps are required for their implementation.

[2] Breakdown voltage: minimum – 5 V, typical – 22.5 V

However, the capacitance is proportional to the number of metal layers available in the technology, reaching approximately 1.22 fF/um^2 if metal layers 1 – 5 are used. These capacitors can tolerate high voltages in the 0.13 µm technology but have been shown to exhibit a varying breakdown voltage and parasitic effects based on the distance between the fingers in smaller feature technologies [181]. At the same time, MOMcaps are situated much closer to the substrate and have significantly higher parasitic capacitances due to this. They are mainly used for decoupling applications due to their varying capacitance based on the voltage across them and frequency of the variation.

The SPCP is unique as it exchanges the HV tolerance requirement from capacitors to switches. Although this could be a disadvantage in general low-voltage CMOS technologies where drain-source voltage is limited, it becomes advantageous for low area requirements in BCD technology where high drain-source voltage V_{DS} is permitted. Hence, it enables MIMcaps to be used instead of MOMcaps for all charge pump stages. The area improvement is approximately 0.3 fF/um^2 greater than MOMcaps. This value can be further increased because MIMcaps can be situated in the uppermost metal layers (e.g., layers 5 and 6), enabling placing MOS devices and routing under them – something impossible to implement with MOMcaps.

It is important to note that MIMcaps can also be used in stages above their maximum operating limit by connecting the capacitors serially. Connecting two equally-sized capacitors serially, results in the voltage drop across each being halved, but the total equivalent capacitance is also reduced by half, according to $1/C_{TOTAL} = 1/C_1 + 1/C_2$. Consequently, if all CP stages maintain the same equivalent capacitance, the size of each stage will increase proportionally to the stage number. The technique can achieve low parasitic capacitance but, due to area constraints, is rarely used in high-voltage applications.

To conclude, based on the characteristics of different topologies, the DK and CC linear charge pumps are the most practical solutions for fully integrated devices; however, in BCD technology, given that the parasitic effects can be accurately evaluated, SPCP design can be advantageous for chip area reduction. Based on these observations, a HCP comprising CC and SP stages is proposed for area-efficient implementation.

3.4 AREA EFFICIENT HYBRID CHARGE PUMP DESIGN

3.4.1 System Overview

The system diagram of the proposed hybrid charge pump is shown in Figure 3-4. The design comprises five stages in total: the first stage is based on a zero-reversion loss CCCP, which operates at 15 MHz and increases the 3.1 V input to a regulated output of 6 V. This voltage is then used to power the input and the clock signal inputs of the following 4 SP stages, operating at 2.5 MHz and using only MIM flying capacitors. The total theoretical gain of the design is then close to 10 (reduced due to regulation), resulting in 30 V at 0 A output current.

Based on the nominal input voltage $V_{IN} = V_{DD} = 3.1$ V and theoretical gain of a single

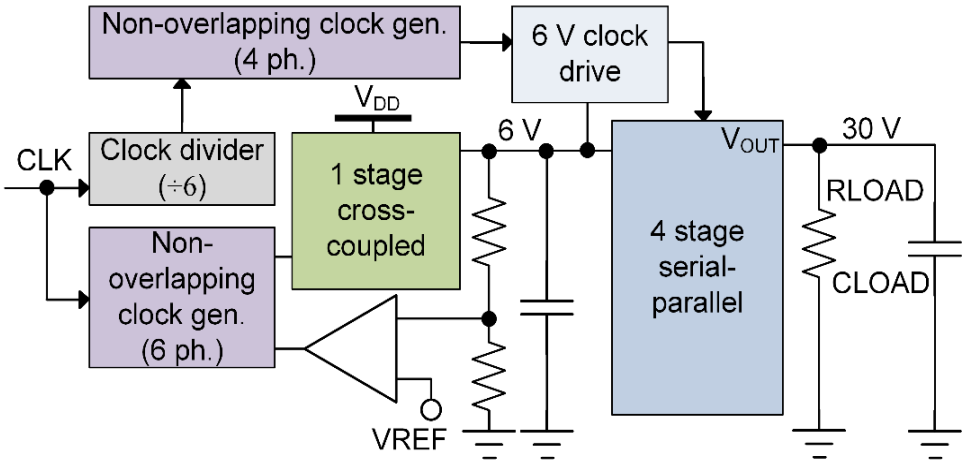

Figure 3-4. Hybrid charge pump diagram.

CCCP of 2, the maximum theoretical drain-source voltage seen between stages would be 6.2 V only under prolonged no-load conditions. The CC stage is powering the SP stages and its output current is never zero. Simulations showed that parasitic effects in the CC stage alone contribute to a voltage drop towards 6.1 V, and the additional current required by the SP stage would result in the drop to below 6 V. As a result, it was deemed reliable and safe to operate the system from a 3.1 V supply. However, an additional regulator before the CC stage could be implemented for applications with strict requirements based on default technology limitations.

The CC stage operates at a high frequency and includes regulation for four reasons. Firstly, based on simulation data, it was observed that the efficiency of the SP stages that follow is maximum for the highest input voltage. Increasing the CC output voltage from 5.5 V but limiting it to 6 V, the total charge deposited in the SP capacitors increases and improves the final output voltage. Secondly, as discussed later, a SPCP operates asymmetrically: the current

requirements are increased during the charge phase and are almost zero during the output (discharge) phase. Regulation of the CC stage ensures that its output voltage is maintained below 6 V while supplying adequate current. Thirdly, by doubling the 3.1 V input voltage first, the total number of stages required is reduced, and the transient response of the overall design is improved. Finally, most HV chips do not use CPs in isolation - they are needed to provide power to the HV drivers used to generate a voltage or current to drive a specific load (e.g., ultrasound transducer). The driver's control is implemented using HV devices driven by voltages of up to 5.5 V, which can be tapped from the output of the CC stage, thus, simplifying the overall system.

3.4.2 Technology

All circuits described in this chapter were designed in TSMC 0.13 µm BCD, six metal layer technology, which permits low-voltage (V_{DS} = 1.8 V), driving voltage (V_{DS} =5.5 V) and high-voltage (V_{DS} = 28 V) fully isolated devices, as well as the triple-well manufacturing process. The design rules specify the maximum V_{DS} limit for 5 V rated devices to be 5.5 V but based on the safe operating area (SOA) of the devices defined by TSMC as well as short operational time of a µUSCE, a 6 V gate voltage can be used for operation within the electrical SOA for both direct current (DC) and pulsed current operation.

3.4.3 Cross-coupled Charge Pump

The CCCP is a linear charge pump obtained by combining two DKCP branches that operate in opposite phases to each other, Figure 3-5 (a) [186], [188]. The circuit utilises an nMOS and a pMOS switch in each branch; the opposite branch node controls the gates of these devices. Compared to a Dickson charge pump, the output ripple is reduced due to each branch's opposite charge and discharge phases. The main problem with the basic structure is reversion losses [208]. Both pMOS and nMOS transistors are partially 'on' during the clock transition, Figure 3-5 (c), and the charge can flow from the output to the top plate of the capacitor and to the input port. However, the solution is straightforward: the switch control of the pMOS and nMOS devices must be separated to ensure that the pumping nodes are set into a high-impedance state between charge and discharge phases. This can be achieved by: a) introducing a non-overlapping period between separate clock phases; and b) adding two additional phases to

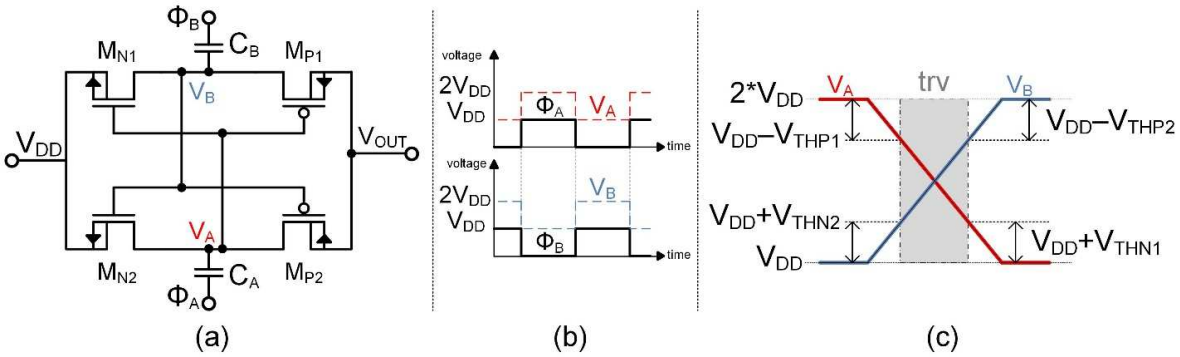

Figure 3-5. (a) Basic cross-coupled charge pump. (b) Timing diagram of (a). (c) Clock transition of (a).

separate nMOS and pMOS control. Together with the two main clock phases, four separated phases are used for control.

A fully-integrated CCCP with zero-reversion loss was proposed by Yu et al. [209], where an auxiliary capacitor pair was used to generate boosted voltage and control pMOS switches. Later, a similar structure was proposed utilising only n-type devices, at the cost of an additional auxiliary capacitor pair and two clock signals [210]. Extremely high efficiency has also been achieved without any additional capacitors and with only two non-overlapping clock phases with the help of four floating inverters [179]. However, this circuit imposes $V_{GS} = 2V_{DD}$ and has a 4.4% reversion leakage current. Other CCCPs exist, but drawing an explicit comparison is complicated due to varying design specifications.

Based on the previous multistage zero-reversion loss architectures tested in stimulator applications before [11], the topology chosen here was designed to use the minimum number of auxiliary components. This design is similar to the work done by Yu et al., Figure 3-6 (a), but uses an auxiliary circuit to control the nMOS (rather than pMOS switches) separately, whilst the main pumping branches are set to control the pMOS of the opposing branch, Figure 3-6 (b). All devices shown are 5.5 V. The auxiliary circuits (boxed in red) in both cases are an additional CP without an output. The energy lost is based on the amount of charge redistributed from the capacitors to the gates of the switches connected to them, dependent on the node's interconnects and the gate size of the switches.

The voltage level generated by the auxiliary circuit is:

$$V_{BOOST} = V_{IN}\left(1 + \frac{C_{CX}}{C_{CX} + C_{PAR}}\right) \tag{3.2}$$

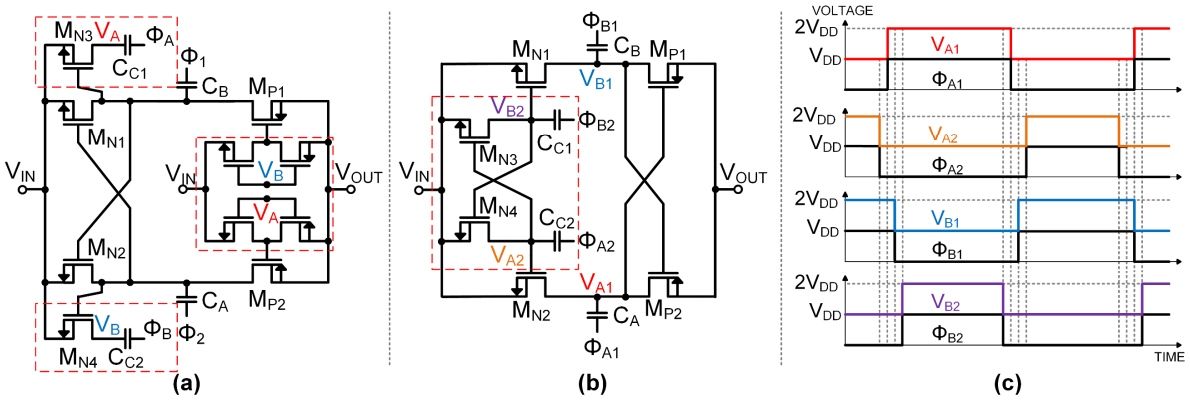

Figure 3-6. Schematics of a cross-coupled charge pump stage: by (a) Yu et al. (timing diagram not shown) and (b) proposed as the CC stage [52]. (c) Timing diagram of the proposed stage in (b).

where V_{BOOST} is the maximum level-shifted voltage at nodes V_{Ax} and V_{Bx}, V_{IN} is voltage to the CP input and clock, C_{CX} is auxiliary circuit capacitance, and C_{PAR} is the stray capacitance at nodes V_{Ax} and V_{Bx}, with x = 1, 2. To achieve V_{BOOST} as close to V_{OUT} as possible, C_{PAR} must be minimised, or C_{CX} must be increased, albeit at a larger chip area cost.

Another way to reduce the size of C_{CX} is to minimise the requirement of V_{BOOST}. An nMOS switch can be assumed to be fully on when its voltage is greater than (V_{IN} + V_{TH-N}). In contrast, the theoretical voltage requirement for the pMOS is to be greater than (V_{OUT} - V_{TH-P}), but any voltage lower than V_{OUT} still increases reversion losses and degrades the performance. If a pMOS switch is connected to the auxiliary circuit, a large C_{CX} is needed to reach V_{BOOST} close to V_{OUT}. In Yu's design, this issue was eliminated by using inverters to control the pMOS gate, the former being controlled by V_A and V_B, Figure 3-6 (a). Alternatively, in the case where the nMOS is already small, it is beneficial to connect it straight to the C_{CX}: the size of the auxiliary capacitors can be reduced whilst still meeting the requirement of (V_{IN} + V_{TH-N}); at the same time, the pMOS gates are connected to the primary pumping nodes, ensuring their V_G can never be lower than V_{OUT} when turned off, Figure 3-6 (b).

The charge pump was implemented using 5.5 V devices. To reduce the gate-bulk voltage and eliminate the body effect of the input nMOS, its body was connected to the source of the device and V_{DD}, and the body of the pMOS was connected to V_{OUT} [181]. The general practice in such circuits is to place the nMOS switches and pMOS switches in separate isolation wells, which increases area due to distance requirements between differently biased deep n-wells. At the same time, the isolation well, which has to be tied to the highest potential to avoid latch-up conditions, would have to be connected in a floating n-well setup [211]. This significantly increases parasitic capacitances seen on the top plates of the pumping capacitors.

For this reason, both n-type and p-type devices in the proposed design were placed in the same isolation well and connected, as shown in Figure 3-7. Such implementation reduces the area but introduces a path comprising two body diodes, from the supply to the output, which cannot be turned off and can be an issue if the charge pump is not operating continuously. The second issue is that this biasing can create a condition where the p-well, deep n-well (NBL) and substrate form a parasitic 'PNP' transistor which could cause a latch-up. As is shown in the experimental results, Section 3.5.2, the latch-up condition was not observed even after repeated circuit start-ups. The CP operated as intended, suggesting that the path created between the switch terminals is significantly lower, preventing the substrate-related transistor from turning on. Furthermore, in applications where periodic operation is needed, the isolation well can be dynamically biased at the cost of area increase.

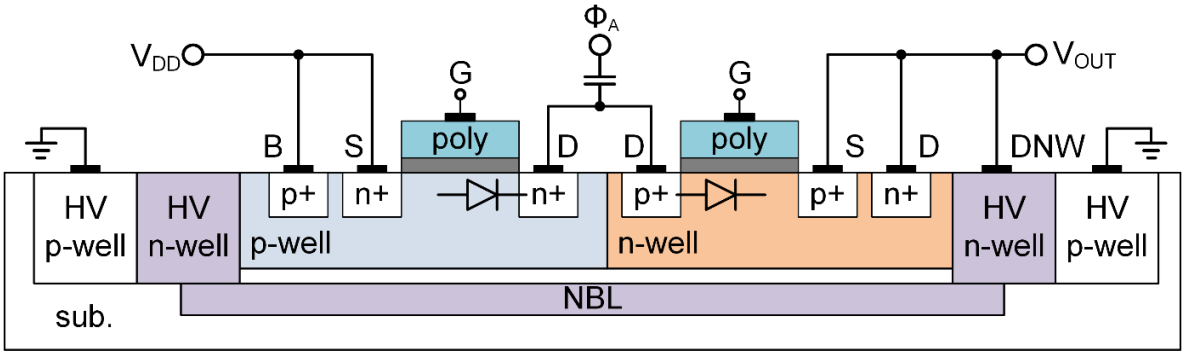

Figure 3-7. Diagram of the triple well biasing in the cross-coupled stage.

3.4.4 Serial-parallel Charge Pump

The SPCP operates in two phases that charge or discharge the capacitors of all stages simultaneously, unlike other topologies where some stages are charging whilst others are discharging. The simplified SPCP diagram is shown in Figure 3-8. Switches S_A connect the top sides of flying capacitors to the supply, switches S_B alternate between the ground and the top-plates of the previous stage capacitor (V_{DD}, in the case of the first stage) and the switch S_C connects the charge pump to the output. In a CMOS circuit, S_B positions 1 and 2 are implemented with two separate CMOS devices. Capacitor C_L is the load capacitor. During phase 1, switches S_A are connected, S_B is in position 1, and all capacitors are charged in parallel to V_{DD}. During phase 2, switches S_A are disconnected and switches S_B are connected in position 2. This results in capacitors being connected in series, giving a theoretical output voltage equal to $V_{DD}(N+1)$, where N is the number of stages.

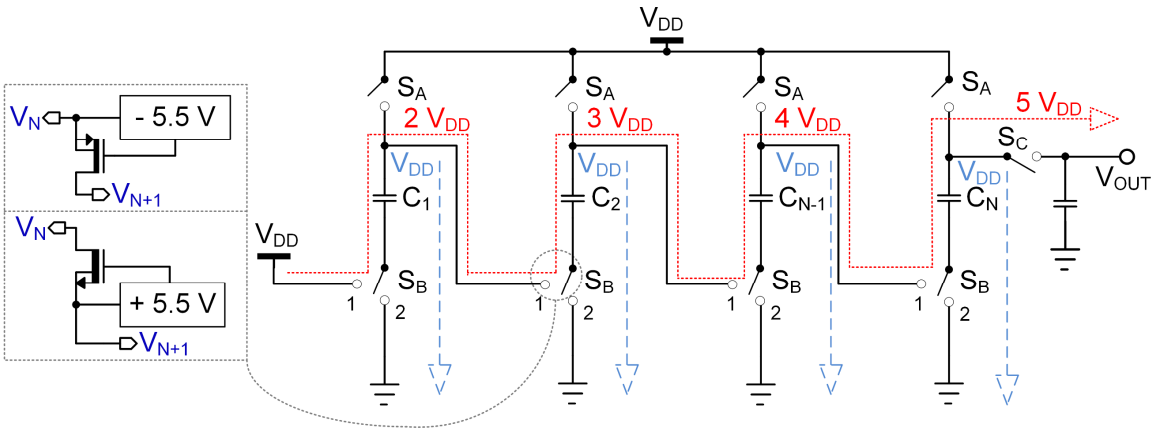

Figure 3-8. Basic 4-stage SPCP diagram. Parallel charging indicated by blue broken lines; serial output indicated by a red broken line. Circuit on the left shows the bootstrap mechanism required for interstage switches S_B.

The SPCP has a maximum voltage drop equal to V_{DD} across the capacitors, whilst switches S_A and S_B (in position 2) must tolerate voltages proportional to the stage number, which results in a topology not possible to implement for HV applications in standard CMOS technology. Even in BCD technology, where high-voltage switches are used, their gate-source breakdown voltage is still limited to 5.5 V, which increases the complexity of controlling the S_B switches. Consequently, this has led to limited interest, with only a few practical examples [212], [213].

Using HV nMOS for interstage switches S_B is complicated: turning on a device even partially causes current to flow to the source of the switch. At the same time, the device's gate voltage must be kept above the threshold voltage for the rising source current. An auxiliary charge pump with predefined levels and dynamic biasing can be used, but it would incur significant losses. Furthermore, the stages must be turned on sequentially [40], increasing the time between charge/discharge phases and reducing the performance (the slow-switching limit is reduced). The logical solution is then to resort to HV pMOS devices. However, an auxiliary circuit is still needed to ensure the gate voltage follows its source voltage by no more than V_{DD} for all stages simultaneously.

The proposed solution to reduce the complexity of the SPCP is shown in the fully self-biased design with its timing diagram (Figure 3-9), based on the principle of generating biasing voltages from subsequent stages [187]. Different tolerance HV devices are used based on the maximum tolerable voltage at a particular stage, to optimise its area. The bulk of each of the devices, M_{B6}, M_{B7} and M_{B8}, is tied to the source whilst the gate is connected to the preceding

stage. All isolation wells of the switches with the maximum drain voltage above V_{DD} are tied to the output.

The circuit, Figure 3-9 (a), is controlled by four non-overlapping phases at 3.1 V: Φ_{X1}, Φ_{X2}, Φ_{Y1} and Φ_{Y2}. The two signals, Φ_{X2} and Φ_{Y2}, are level-shifted to 3.1 – 6 V range – signals Φ_X and Φ_Y. The timing diagram is shown in Figure 3-9 (b). Assuming a steady-state, the circuit operates as follows. Initially, Φ_{X1} and Φ_X are low, which shifts V_{SP0} to $2V_{DDSP}$ and turns switches M_{B1} - M_{B4} on. At the same time, Φ_{Y1} and Φ_Y are high, connecting the bottom plates of C_1 - C_4 to the ground. After the charging phase, Φ_X turns high, and Φ_{Y1} turns low, driving the CP in a semi high-impedance state. Following this, Φ_{X1} goes high, disabling M_{B1} - M_{B4}. The voltage increase is mirrored to V_{SP1} until it increases to $V_{DDSP} + V_{THP}$, where V_{THP} is the threshold voltage of the HV pMOS. M_{B6} then starts to conduct into the bottom plate of C_2. This potential increase is then propagated throughout the circuit almost instantaneously, boosting the voltage at the output to $V_{OUT} = V_{SP4} - V_{DIODE}$, where V_{DIODE} is the Schottky diode threshold voltage ≈ 0.4 – 0.5 V.

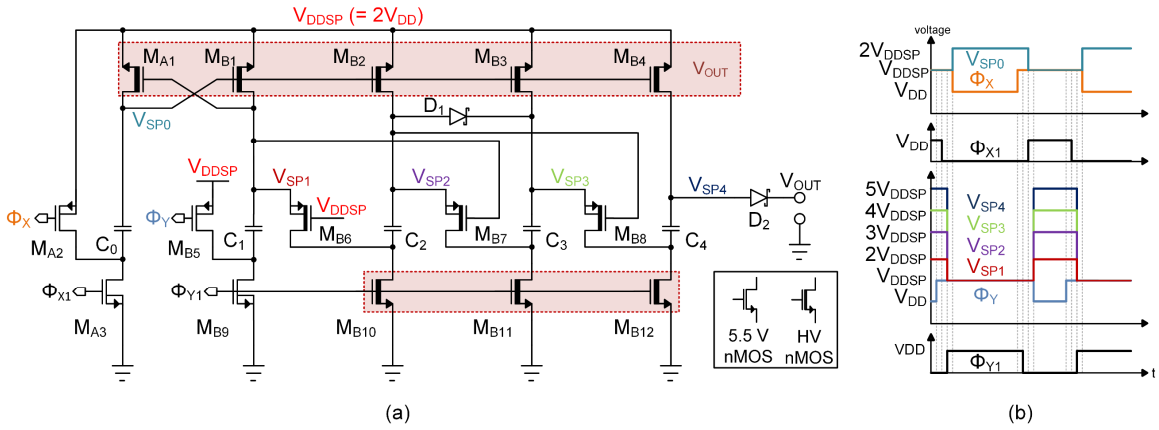

Figure 3-9. (a) Simplified schematic of the self-biased SPCP and (b) its timing diagram.

Two Schottky diodes are used in the circuit. One diode (D_2) serves as an output switch of the CP instead of the self-biased pMOS in the preceding stages, to reduce reversal losses. The diode eliminates the current flowing from the output back into the fourth stage during the serial to parallel transition without the need of an auxiliary level-shifter and complex control scheme. During this transition and on start-up, the isolation voltages of devices M_{B1} - M_{B4} and M_{B10} - M_{B12} is at $V_{NBL} \leq V_{SP4}$-V_{DIODE}, which can cause an intermittent current flow from different stages to the output through NBL. Furthermore, during start-up, a condition similar to the one observed in the CC stage happens in the last stage of the circuit, where the body diode of M_{B4} and D_2 create a direct current path from the input to the output. When needed, that

drawback can be eliminated with an additional dynamic body biasing scheme, which was not pursued further here.

It is important to note that based on the original technology specification, a Schottky device should have a substrate leakage of less than 1 nA at 25°C. Still, a yield degradation was observed in a design that used Schottky diodes, which led to an observation that the device's leakage current can, in some cases, be 10x higher (personal communication, J. Brown, Dialog Semiconductor, 2020). As this is a probabilistic event that could not be evaluated with the limited number of chips tested in the present work, it could not be confirmed to have affected the measurements of the manufactured chips. The comparison between the original specification and initial measurement results of Schottky diodes with multipliers of one and nine are shown in Figure 3-10.

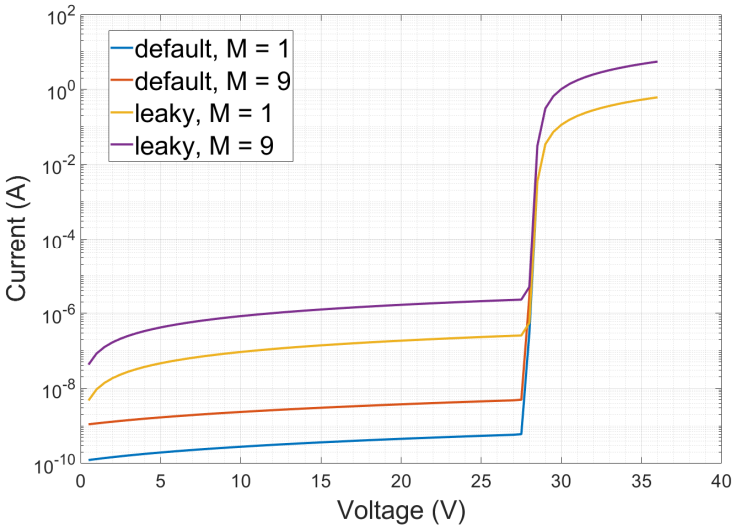

Figure 3-10. Default vs measured (leaky) Schottky diode results.

3.4.5 SPCP Optimisation

The SPCP is sensitive to parasitics significantly more than other topologies [203]. For this reason, this topology works best with a limited number of stages or with discrete capacitors. Any CP can be expressed as a two-port system, and its matrix transfer functions can be derived. By investigating charge and discharge phases of a CP, assuming a steady-state, and including the parasitic effects present at the top and bottom plates of the flying capacitors, a single-stage SPCP matrix expression can be derived as [201]:

$$K(1)_{12} = \begin{bmatrix} 1 & 0 & 0 & 0 \\ -(1+\alpha_T) & (1+\alpha_T) & 0 & R \\ 0 & 0 & 1 & 1 \\ -1/r_T - (1+\alpha_T)/r_B & 1/r_T - (1+\alpha_T)/r_B & 0 & (1+\alpha_B) \end{bmatrix} \quad (3.3)$$

where $\alpha_i = C_i/C$, is the ratio of the parasitics to the stage pumping capacitance, $r_i = T/2C_i$ is the CP's effective resistance coefficient and R = T/2C and $i = T$ (top), B (bottom). The complete transfer function of the CP can be expressed by raising a single stage function to the power of N:

$$K_{SP}(N) = (K(1)_{12})^N \quad (3.4)$$

The full expression to relate input and output voltages and currents can then be expressed as a matrix:

$$[V_{DD}\ V_{DD}\ \ I_{IN1}\ I_{IN2}]^T = K_{SP}(N)\ [V_{OUT}\ V_{OUT}\ \ 0\ \ 2I_{OUT}]^T \quad (3.5)$$

The expression facilitates evaluating a SP topology based on its operating frequency, pumping and parasitic capacitances, and the number of stages.

The SP topology permits the use of MIMcaps for every CP stage. Still, it can only be effectively implemented if the parasitic capacitances in each stage are low. Parasitic effects in the MIMcap plates arise from cross-coupling between tracks in the vicinity of the capacitor. Assuming that the top and side C_{PAR} can be eliminated with proper layout techniques, C_{PAR} is then mainly dependent on the capacitive coupling to the closest metal layer M4 below the MIMcap, which can be left functionally empty and thus filled with floating dummy metal planes which reduce electrical field coupling to layers underneath. Routing can be carried out solely in the bottom three metal layers, allowing for minimisation of the M4 track count.

To evaluate parasitic effects, four layout arrangements with maximum size MIMcap (C_{MIM} = 2.4185 pF; W/L = 40 x 40 μm^2) were extracted, Figure 3-11. Case A provided the base CC capacitance of the MIMcap with no other metal layers present, case B included a floating metal plane under the MIMcap on layer M4, case C had the same M4 plane that was grounded and cases D – F had different numbers of floating metal planes under the MIMcap, with the bottom-most layer grounded.

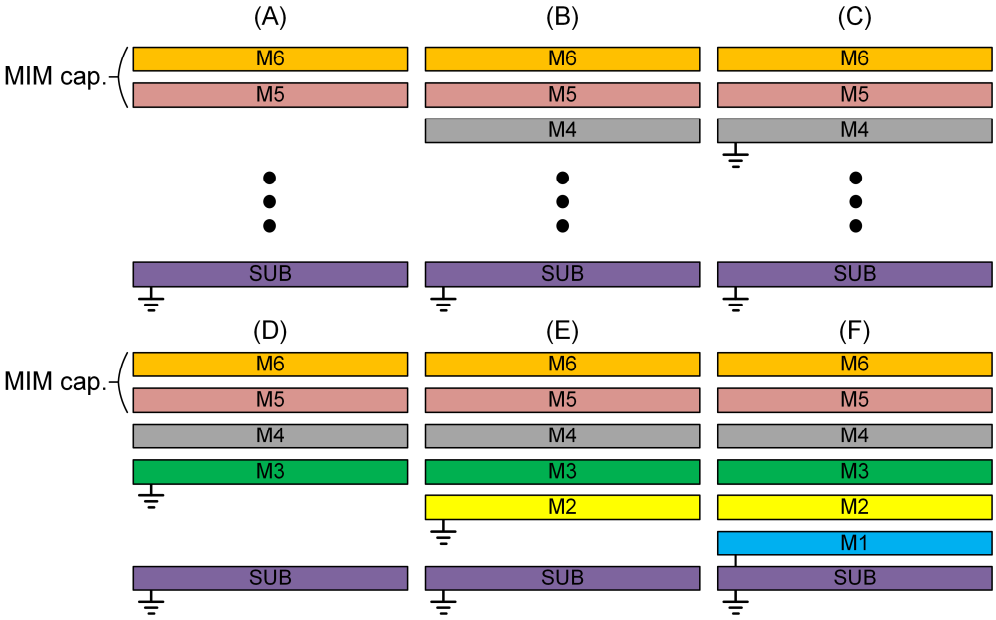

Figure 3-11. Arrangements for parasitic capacitance extraction.

The results of the parasitic extraction are summarised in Table 5. The top plate value $C_{CC\text{-}TOP}$ varied by only 3.19% across conditions A - F, and the bottom plate $C_{CC\text{-}BOT}$ value varied depending on its proximity to a ground plane. The base α_T and α_B (case A) were found to be 0.78% and 3.25% of C_{MIM}. In reality, the metal route number increases, moving from M1 to M4. Most tracks are kept in the first three layers, leading to additional parasitic capacitance to the substrate. The overall impact of the parasitic effects is highly dependent on individual layouts and cannot be precisely evaluated. Case D, where M4 is left unused, and M3 is occupied by a single ground plane provides a valid approximation of the total parasitic effect. Complete grounding on this layer is extremely unlikely; however, cross-coupling with signal paths on other layers will exist.

Table 5. Parasitic extraction results. Values of femtofarads (fF).

Parasitic capacitance	A	B	C	D	E	F
$C_{CC\text{-}TOP}$ (fF)	16.61	16.42	16.64	16.46	16.95	16.58
$C_{CC\text{-}BOT}$ (fF)	35.52	37.2	98.43	70.64	59.34	51.36

With α_T = 0.78%, α_B = 3.25%, and V_{DD} = 3.1 V for an output current I_{OUT} = 40 µA in Equations (3.1) and (3.3), a sweep for the operating frequency and capacitor values can be performed. The resultant output voltage and efficiency graphs versus pumping capacitors and operational frequency for three and four stages are shown in Figure 3-12. The efficiency for the three stages reaches 52%, dropping to ~ 40% with the introduction of an additional stage. Both three and four-stage SPCPs can achieve V_{OUT} > 20 V output voltage, but the active region is sub-optimal for the three-stage charge pump, given the initial conditions. Grey dots in Figure 3-12 (b) and (d) signify the peak efficiency points where V_{OUT} > 20 V output voltage is achieved for three and four stages, respectively. It can be observed that for this voltage the three stages operate in a suboptimal region across the full parameter sweep range.

All plots in Figure 3-12 are symmetrical across the x = y line. Still, this behaviour is not accurate in real-life applications. Increasing the area of a flying capacitor reduces the fractional parasitic effect, whilst increasing operating frequency does not. Furthermore, the SPCP operates

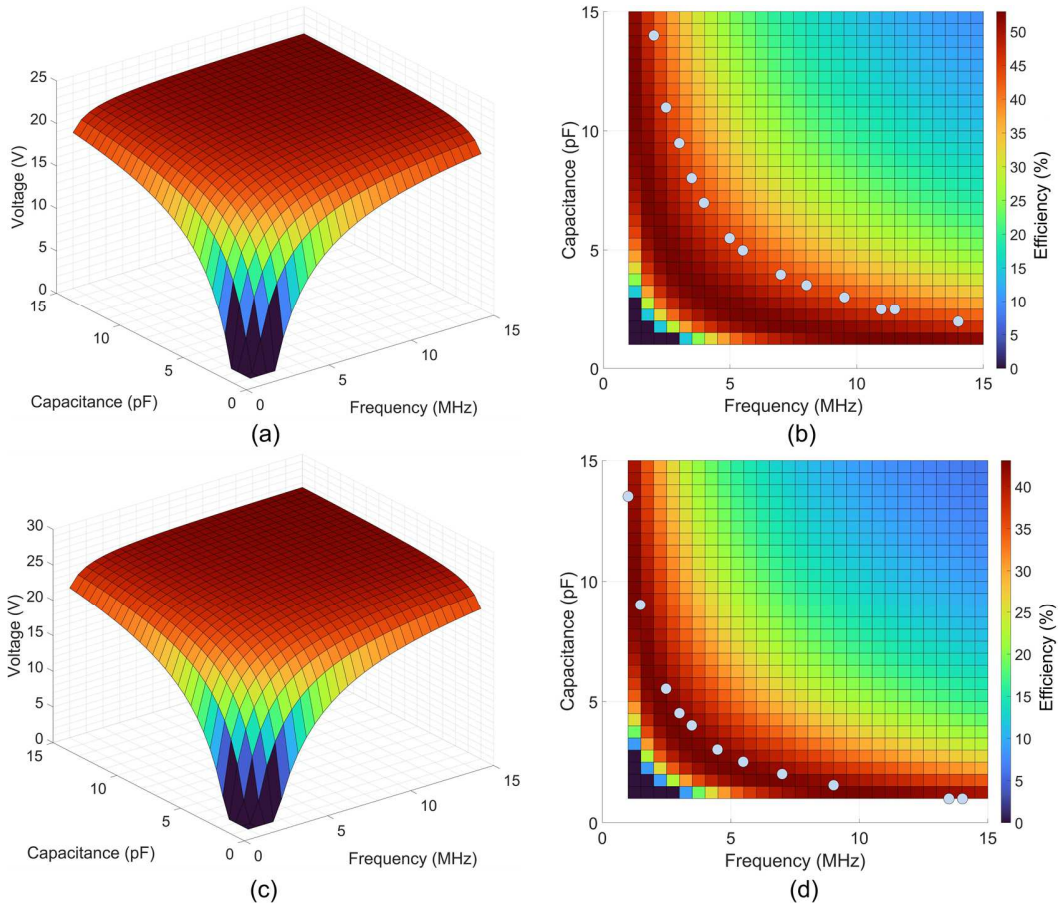

Figure 3-12. Three-stage SPCP: (a) output voltage, and (b) efficiency; four-stage SPCP: (c) output voltage and (d) efficiency vs stage capacitance and operating frequency. Blue dots indicate peak efficiency for the desired voltage of 20 V.

significantly better under slow-switching limit conditions [202]. Thus, increasing the flying capacitor value whilst maintaining or decreasing the frequency leads to better results overall.

3.4.6 Hybrid Charge Pump

The complete HCP schematic is shown in Figure 3-13. The CCCP is shown on the left and is composed of M_{N1}, M_{N2}, M_{P1}, M_{P2} and the components connected to them. The stage is driven by four non-overlapping phases Φ_{A1}, Φ_{A2}, Φ_{B1} and Φ_{B2}, which are generated from a clock signal CLK_{FAST}, gated with a comparator output. The SPCP is driven by four clocks Φ_{X1}, Φ_{X2}, Φ_{Y1} and Φ_{Y2}, which are generated from a separate slower clock CLK_{SLOW}. The 3.1 V amplitude of all clocks is not enough to drive the SP stage, operating with twice as high input voltage. Consequently, an auxiliary CC stage (M_{K1}-M_{K2}, C_X, C_Y) and two inverters (M_{K3}, M_{K5} and M_{K4}, M_{K6}) produce a level-shifted signal alternating between V_{DD} and V_{OUTCC} to control SP input high-side switches M_{A2} and M_{B5}. Furthermore, to generate a gate voltage higher than V_{OUTCC} and enable M_{B1}-M_{B4}, the first stage of the SP (V_{SP1}) was doubled and cross-coupled with an auxiliary stage (V_{SP0}).

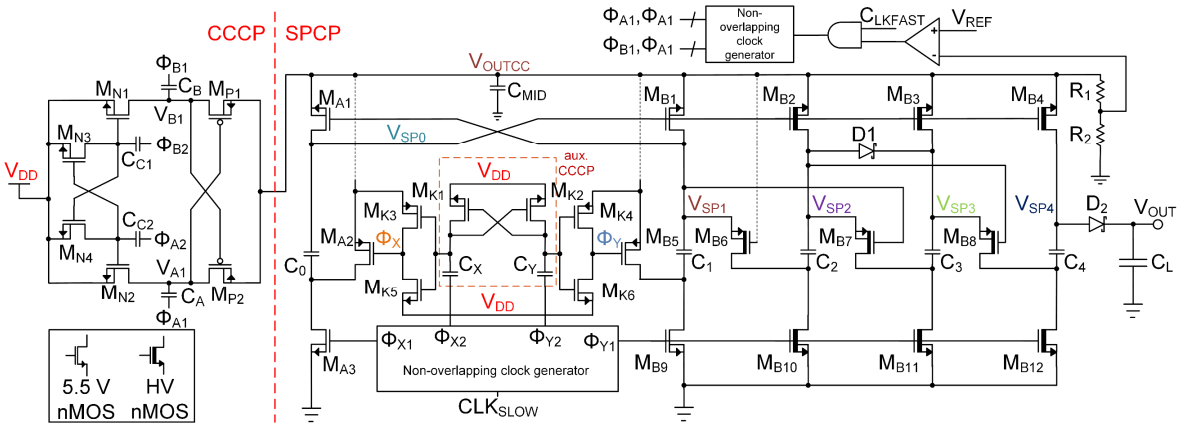

Figure 3-13. Full schematic of the hybrid 3.1- 20 V charge pump.

3.4.7 Non-overlapping Clock Generator

The non-overlapping clock generator separates the control of individual switches in the charge pump by introducing varying delays derived from a single clock source. By introducing delays between the phases, reversion and crowbar currents can be eliminated, thus improving the CP's efficiency and current sourcing capabilities. Nonetheless, to achieve the maximum charge transfer rate, symmetrical charge/discharge timing must be ensured whilst reducing the delay time to the absolute minimum across process, voltage and temperature (PVT) variations.

A fully feedback-based scheme was chosen for this design. Two clock generators (four and six-phase) were used at different operating frequencies. Both clock generators, Figure 3-14 (a) and (c), are based on nesting NAND gate based cells and rely on the circuit's intrinsic signal propagation delay. Their timing diagrams are shown in Figure 3-14 (b) and (d). This implementation eliminates the need for current starved delay cells or other delay elements whilst ensuring the minimum non-overlap time. Furthermore, the phase relationships remain unchanged due to the feedback mechanism, even with PVT variations. Simulations with a 20 fF capacitive load and the signal outputs connected to the feedback inputs showed the delay between the two most separated-in-time phases, A1-B1 in Figure 3-14, (b) and A3-B3 in Figure 3-14 (d), to be 2.2 ns and 3.6 ns, respectively.

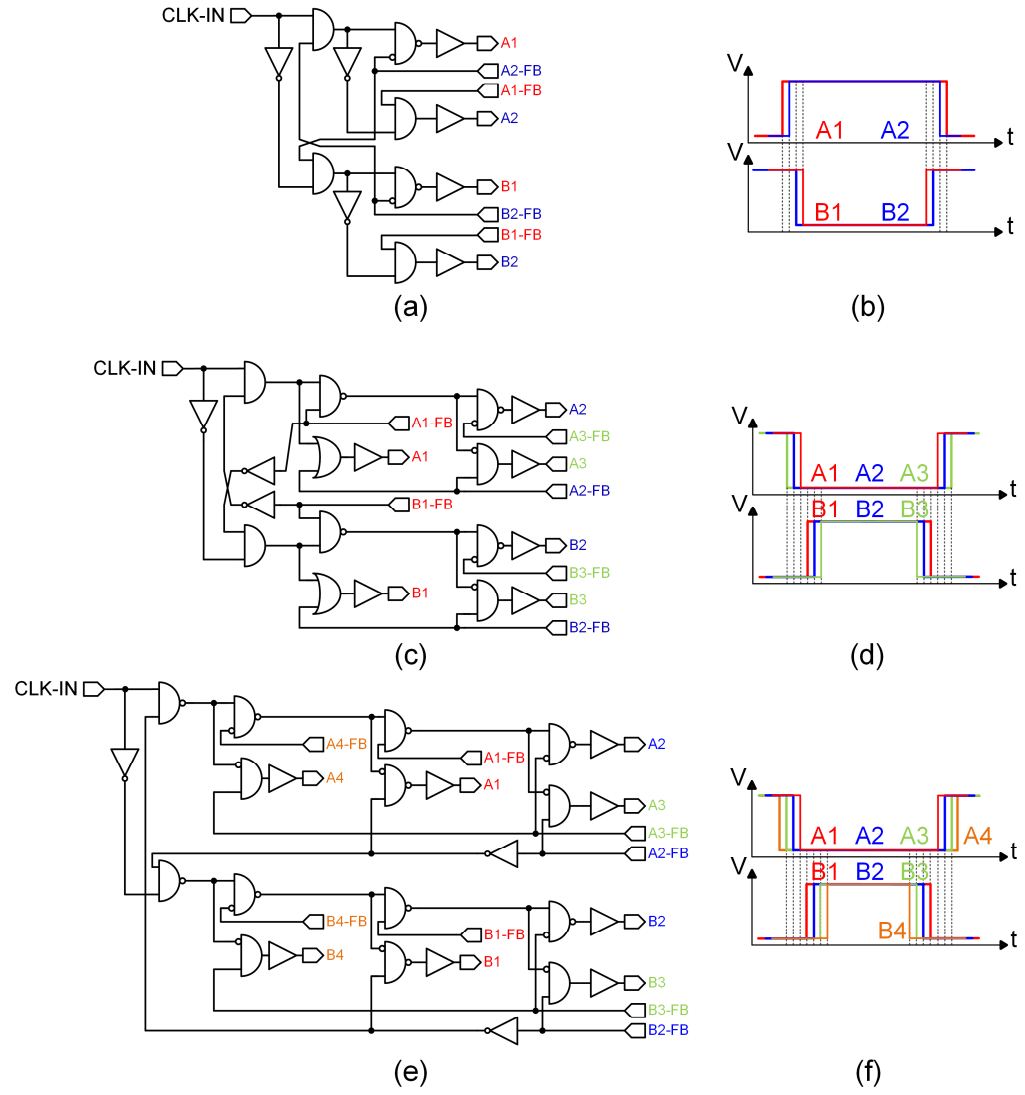

Figure 3-14. Non-overlapping clock generator circuits: (a) Four-phase (c) Six-phase (e) Eight-phase. Timing diagrams: (b) Four-phase (d) Six-phase (f) Eight-phase.

A four-phase clock can ensure zero reversion loss in the cross-coupled doubler. However, given a large stage capacitance, 30 pF, and a fast operating frequency of 15 MHz, a six-phase clock was used: the two additional phases were employed to separate control of the pMOS and nMOS of the clock buffers generating signals Φ_{A1} and Φ_{B1}, Figure 3-13, and eliminating crowbar currents.

An implementation for an eight-phase clock was also achieved, Figure 3-14 (e), with a nominal delay of 5.1 ns, which was 41% higher than that of the six-phase version. The timing diagram is shown in Figure 3-14 (f). The limitation of the nested feedback-based clocking scheme can be identified from this change. By increasing the number of phases, the full path the logic transition has to travel increases, leading to an increased duration of the non-overlapping period. Although a feedback-based method ensures robustness, it might be undesirable in systems where consistent phase delays and non-overlapping times below 5 ns are required.

3.4.8 Output Regulation

The output of the CP can be regulated in multiple ways, the main options being: control of the clock frequency or duty cycle (pulse-skipping), variation of the number of stages used for voltage multiplication and control of the clock voltage [214].

The frequency modulation approach requires an additional voltage controlled oscillator (VCO) to be implemented on-chip. This increases the circuit's power consumption and design complexity, particularly in cases where precision is needed, regardless of PVT variations. Pulse skip regulation is most widely used in CPs due to its simplicity and capability to produce a wide range of regulated output currents. It requires a single comparator used to gate the clock to the charge pump if the output voltage is below a predefined threshold. The output voltage of the CP using a pulse-skip regulation is highly dependent on the comparator's hysteresis and speed. Sometimes, a second comparator for the lower/upper limit can also be used.

Regulating the charge pump by controlling the number of stages, the capacitor connection arrangement or the supply voltages is less common due to the intrinsic limitations of these schemes. The number of stages and variation in their connections can only produce V_{OUT} equal to discrete values or half increments of the input voltage. Such a control scheme cannot be used for precision control of V_{OUT} and can only be achieved with additional circuitry, introducing losses in the main charge pump path. Nonetheless, it is an attractive scheme for

applications where a wide output voltage range at the highest efficiency is required [215] or a finite number of output voltages is desired [216].

Clock voltage regulation is also possible but is practical only in applications where an additional DC-DC converter is available. A boosting converter can reduce rise time and silicon area [217], while reducing the supply voltage can decrease switching losses [218]. Voltage boosting can be achieved with an additional CP circuit and is, in essence, the technique applied in the proposed HCP, although it is not used to regulate its output. With feedback from the output of the HCP ($V_{OUT\text{-}HCP}$), and assuming that the CC output can be controlled in the range 3.1 V – 6 V, the output could be regulated in the range $V_{OUT\text{-}HCP}$ > 15.5 V. Nonetheless, this mode of regulation was not used due to a degradation in the efficiency of the SP pump stages proportional to the drop in the supply voltage.

The proposed HCP uses pulse-skip (duty cycle) regulation for the CC stage and relies on its output voltage definition based on the output current. A fraction of the output voltage of the CC stage, defined by a voltage divider, is compared to a reference voltage of 1.25 V and a comparator is used to evaluate the two voltages on the rising edge of the input clock: if the voltage is below the limit, the signal is gated through to the CCCP circuit.

A fast, low power comparator is needed to provide practical output evaluation in all regulation schemes. Although there are a few considerations, both dynamic and static comparators can be used for this purpose. Firstly, dynamic comparator has zero static power consumption but has dynamic power losses proportional to the clock frequency. As a result, a continuous static comparator could be advantageous for high-frequency conversion. Additionally, a dynamic comparator generates kickback noise due to voltage swings in the

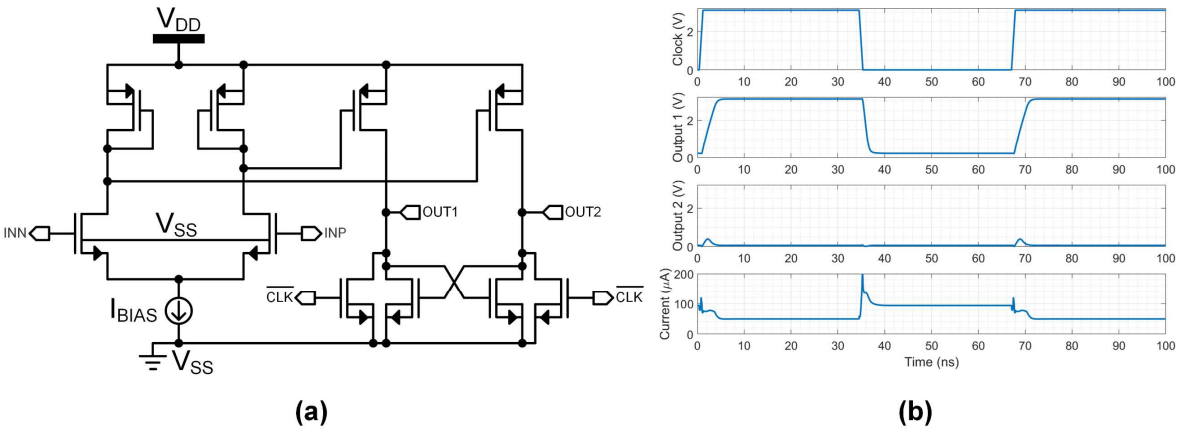

Figure 3-15. (a) Static latched comparator. (b) Transient simulation of the latched comparator with a 15 MHz input clock.

circuit that couple through the gate capacitance to the input. This is an issue with the high impedance input from the voltage divider, but it can be eliminated by introducing a static buffer or an additional sampling circuit [219]. Alternatively, a low current static comparator can be used whilst its speed and power consumption can be reduced by implementing a dynamic current biasing scheme [220].

For the present design, a latch-based differential pair design was used to regulate the output of the cross-coupled stage, Figure 3-15 (a). The differential input pair was biased at 37 µA and the total current consumption was 74.5 µA at 15 MHz input clock frequency, ensuring that the propagation delay of the comparator was only a fraction of the total CCCP period. The transient simulation diagram is shown in Figure 3-15 (b). The comparator was simulated with a 15 MHz clock and input voltages of V_{INN} = 1.25 V and V_{INP} = 1.35 V. It can be observed that when CLK goes high, the comparator enters the evaluation phase and quickly propagates logic high to OUT1. The total current consumption during this time is mainly determined by I_{BIAS}, but it increases when CLK goes to logic low. While the implementation is not the most energy-efficient, it permits fast comparison without kickback noise and allows to adjust the speed of the comparator through I_{BIAS}.

3.4.9 Comparative Dickson Charge Pump Design

A DKCP with the same chip area as the SPCP was designed to compare the efficiency of the SPCP. It had four stages and had 6 V, 12 V, 18 V and 24 V maximum voltage drop across stage capacitors with an input voltage of 6 V. The design used a total of 40 pF across the four stages: the first stage was implemented using MIMcaps placed above the switching circuitry, whilst stages two to four were implemented as MOMcaps spanning metal layers 1 – 5 with no circuitry under them. This resulted in the highest MOM capacitance per area of 1 fF/µm^2 and 10 pF per stage.

The DKCP utilised high-voltage Schottky diodes as the passive switches between stages, which resulted in a forward drop-out voltage of 0.4 V per stage. The reduced diode drop improved V_{OUT} compared to diode-connected nMOS but led to a voltage loss of 2 V compared to an actively switched DKCP. The design was tailored to occupy the same area as the SPCP for area-utilisation comparison between the two designs. The DKCP switching scheme was equivalent to the auxiliary boosting stage presented in the HCP, Section 3.4.4.

3.5 RESULTS

3.5.1 Realisation

The CC, SP and DK CPs were manufactured and tested using the a PCB. Their layout views are shown in Figure 3-16 (a), (b) and (c), respectively, while a macrograph of the chip with the exact placement of the circuits is shown in Figure 3-16 (d). The CCCP occupies an area of 0.04293 mm^2, the total size of the SPCP is 0.04393 mm^2, and the four-stage DKCP area is 0.04385 mm^2. However, the space under the flying capacitors of the SPCP is 0.025 mm^2 or 60% of the total Dickson CP area. The empty area under the MIM capacitor of the CCCP, excluding its output MOScap, was also 0.025 mm^2. Thus, the total effective area of the overall HCP is 0.036 mm^2. This area could be utilised for other circuits, such as an oscillator, regulation circuitry or others, at the cost of increased parasitic capacitances.

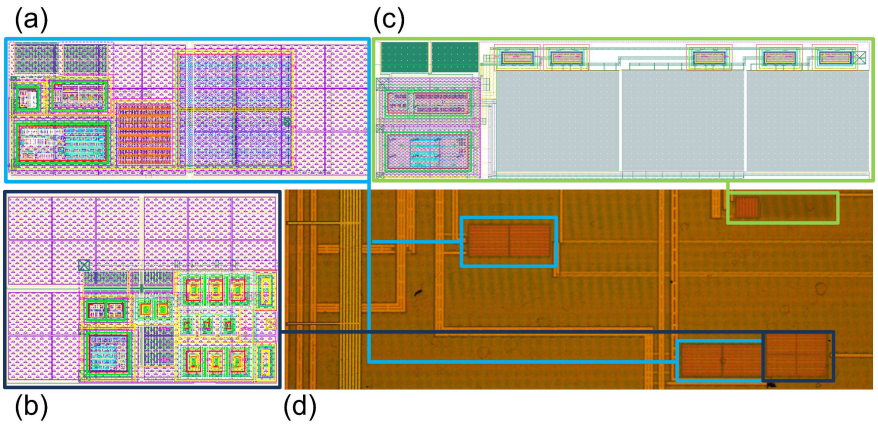

Figure 3-16. Layout views of the: (a) cross-coupled (338 x 127 μm^2), (b) serial-parallel (251 x 175 μm^2) and (c) Dickson (395 x 111 μm^2) charge pumps; (d) a macrograph of the manufactured chip.

3.5.2 Cross-coupled Charge Pump

The deep n-wells in both the CCCP and SPCP were biased by connecting them to the outputs of the circuits. As a result, a significant current in-rush occurs on start-up, which could cause a latch-up event or degrade the circuit's performance over time. To investigate this, 100 start-up conditions (power up, power down) were carried out at the minimum output current of 1 µA for three CCCP circuits. V_{OUT} and efficiency measurements were taken before and after the test across the entire output current range. The values were compared for the same conditions: the maximum V_{OUT} and efficiency differences across the three chips were 0.01 V and 1.2%, respectively. The maximum average difference across the chips was 0.005% for

voltage and 0.19% for efficiency. Based on the precision of the measurement setup, these fall within the range of standard error and do not show a degradation in the circuit's performance.

V_{OUT} and efficiency of a CCCP operating at 15 MHz were measured for output currents up to 800 µA. The results are shown in Figure 3-17 and exhibit a peak efficiency of 76% at 450 µA output current, which drops to 73% at 500 µA output current for the regulated version. The regulation scheme introduces efficiency improvements of up to 18% in the 0 – 100 µA range, where output is limited to 5.93 V. The goal of limiting the circuit's output voltage to below 6 V is achieved at the cost of reduced maximum efficiency.

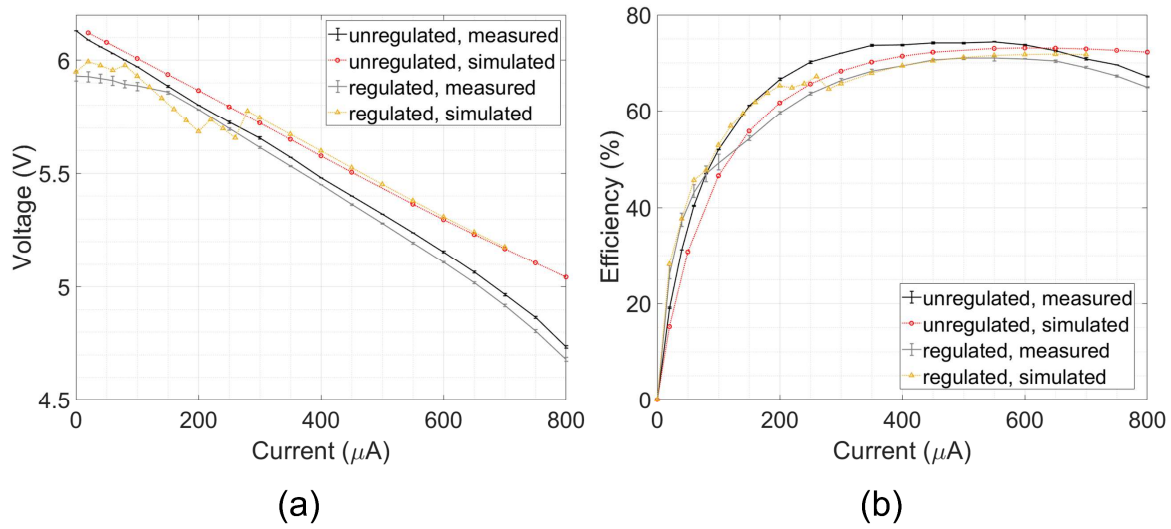

Figure 3-17. (a) V_{OUT} versus output current, (b) Efficiency versus output current of the CCCP.

3.5.3 Serial-parallel and Dickson Charge Pumps

The SPCP and DKCP were evaluated and compared to post-layout simulation results regarding efficiency and output voltage. It is important to note that the electrostatic discharge (ESD) protection circuitry for the high-voltage output pads was a reverse-biased diode with a nominal voltage rating of 28 V. As observed, both CP outputs were limited to approximately 27.4 V at I_{OUT} = 0 µA. The post-layout simulation data shown includes the updated leaky Schottky diode model.

Output voltage and efficiency graphs of the two designs are shown in Figure 3-18 – the centre line and the vertical extensions indicate the mean and the standard deviation of measuring three different chips. The results from the DKCP show a close match between the simulated and measured results, suggesting appropriate Schottky diode modelling. The behaviour observed in the SP circuit is different: the maximum measured efficiency is lower by 17% compared to the simulated data. The difference is present for the full range of output currents, and an abrupt drop in V_{OUT} can be observed at higher currents, which is the mode of operation when the charge utilised and lost within the circuit is too large and cannot be replenished anymore. The results indicate a leakage current or significantly higher than estimated parasitic values present in the CP – both of which could be due to insufficient modelling of parasitic structures in the triple well process.

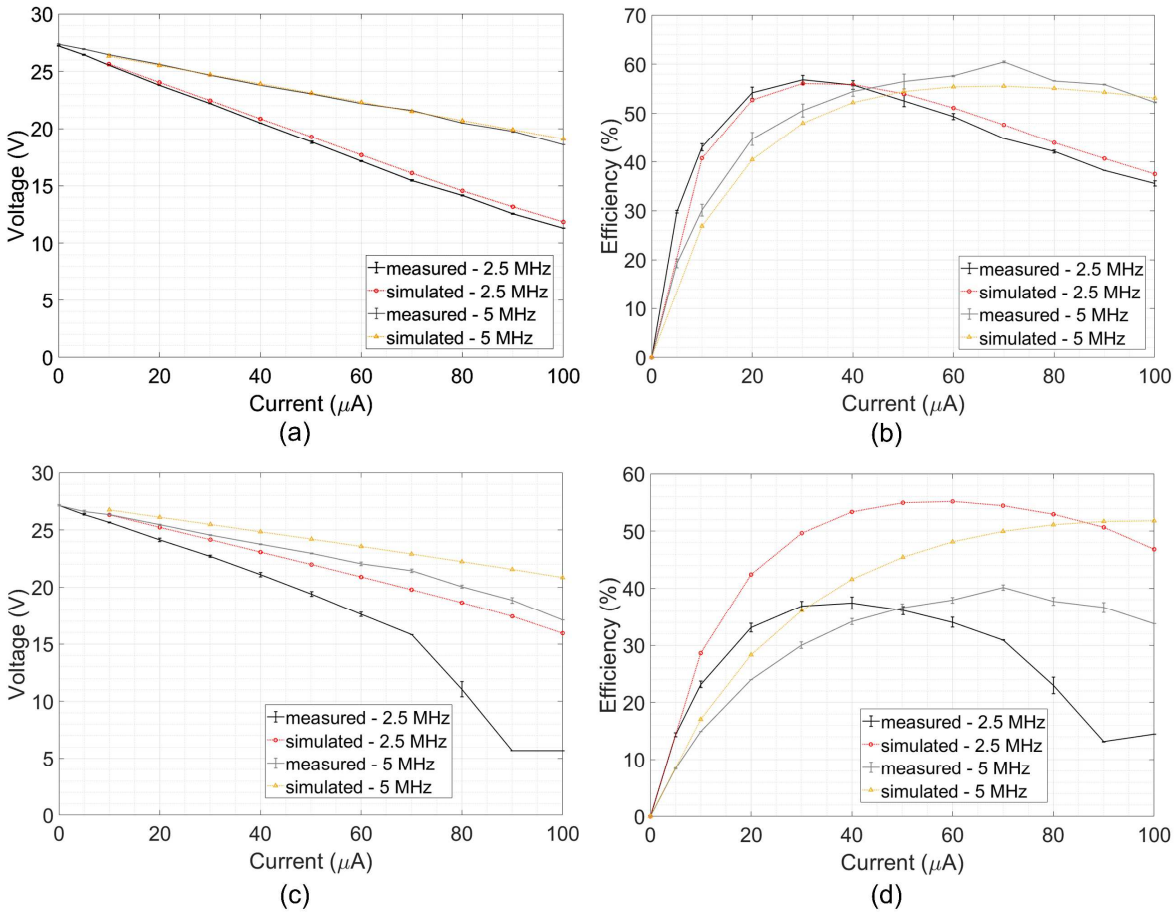

Figure 3-18. (a) Output voltage and (b) efficiency of the DKCP. (c) Output voltage and (d) efficiency of the SPCP.

The HCP is a combination of the SP and CC circuits, resulting in its V_{OUT} and efficiency values being the product of theirs. Figure 3-19 shows the measurement results for the entire

hybrid implementation with a constant CC frequency and SP, operating at 2.5 MHz and 5 MHz. All of the effects observed in the measurements of individual stages can be seen here as well.

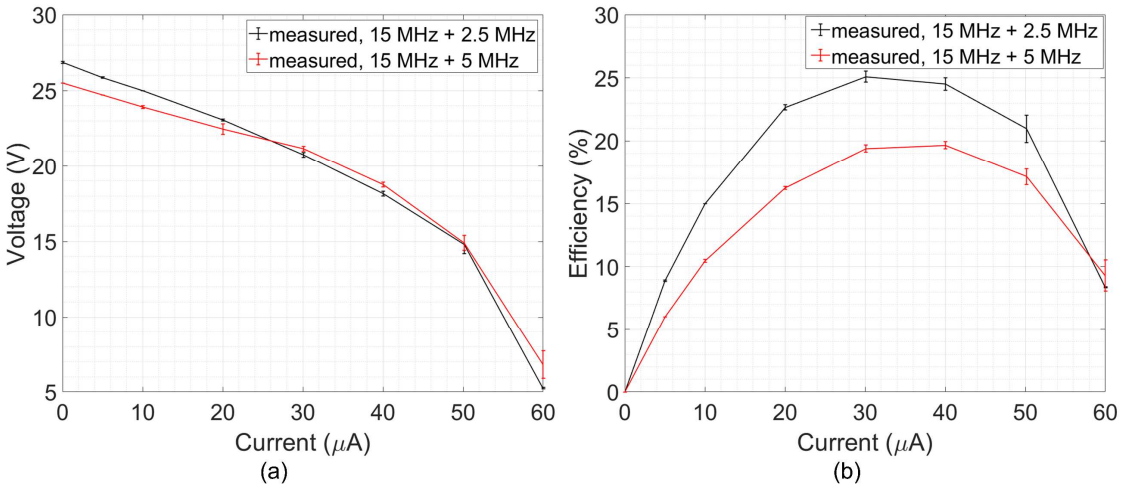

Figure 3-19. (a) Output voltage and (b) efficiency of the HCP.

The maximum measured efficiency of 25% is close to the product of the maximum measured efficiency of the CC stage and SP stages calculated from their individual measurements. However, the output voltage drops abruptly at 60 µA rather than at 90 µA observed in the standalone SPCP due to the limited current sourcing capability.

The complete HCP was intended to operate in a battery-powered application. Due to the low, but finite output impedance of the battery, increases in the load current can cause a drop in the supply voltage. Consequently, the circuit was evaluated for input voltages from 3.1 V to

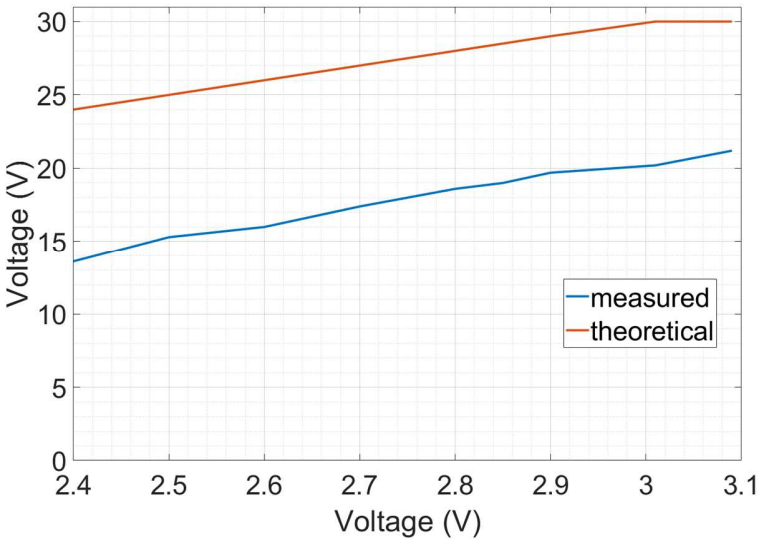

Figure 3-20. Output voltage vs input voltage of the HCP.

2.4 V at I_{OUT} = 30 µA. The CC stage operated at 15 MHz, while the SP stage switched at 2.5 MHz. Figure 3-20 shows that the measured V_{OUT} was 9 V lower than the theoretical value, but changed the same with V_{IN}, eliminating the possibility of any non-linear effects in the circuit.

3.5.4 Discussion

The data from the previous section identifies a discrepancy in the measurement and post-layout results of the SPCP. At the same time, test results of the CCCP and DKCP circuits match well, thus suggesting an issue within the SP circuitry, even if it could not be observed in simulations. This section discusses two aspects - underestimated parasitics and leakage due to improper biasing that could have led to a mismatch between simulations and measurement results and outlines strategies to improve the proposed design.

As mentioned in Section 3.4.4, the two Schottky diodes D_1 and D_2 used in the SP stages of the HCP, Figure 3-21, have higher than specified leakage current. As this leakage can vary between devices, it was impossible to confirm these two devices as the sole cause of performance degradation. Furthermore, both diodes strongly couple to the substrate, introducing additional parasitic capacitances to the top plates of C_2, C_3 and C_4, Figure 3-21; parasitic effects are further increased due to routing to the top plates of these capacitors. Both diodes should be removed from the circuit to eliminate the uncertainty.

The diode D_1 between stages prevents an overvoltage condition during the charge-to-discharge transition. The voltage spike exists due to the in-rush current and lag in the charge transfer from stage two to three through M_{B7}, Figure 3-21. The overvoltage duration is below a nanosecond and could be avoided by slowing down the turn-on time of the input switch M_{B5}, Figure 3-21. Alternatively, the current could be regulated by simply increasing the device

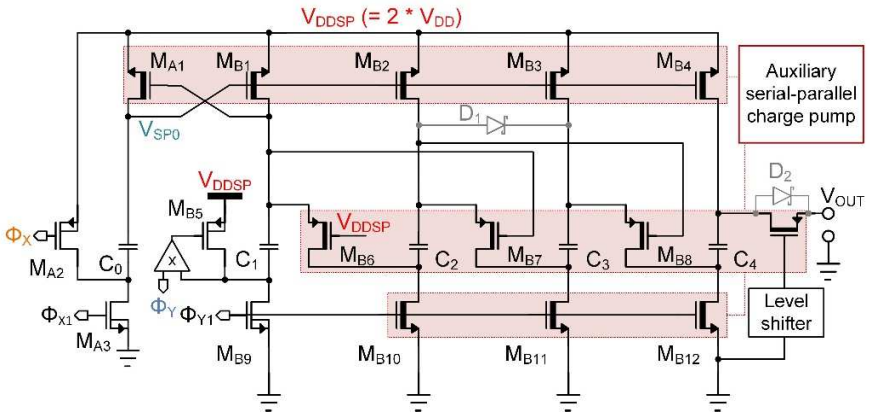

Figure 3-21. Serial-parallel CP with reduced parasitics using slow charging, auxiliary bias CP and active output switch.

length, or using an active control by sensing voltage at the bottom plate of C_1. The second diode D_2 could be substituted by an actively switched leve-shifter, Figure 3-21, that eliminates the forward voltage drop and reverse leakage, and reduces the parasitic capacitance of C_4, at the cost of increased silicon area.

A different way to improve the overall efficiency is by minimising parasitic effects due to the gate of the interstage HV pMOS. The self-bias circuit could be extracted as a smaller replica circuit, operating parallel to the main branch, similarly to the auxiliary circuit in the CC stage – a different linear CP could also be used. The current requirements of the secondary circuit would be significantly lower, and its capacitor size would be determined by the gate capacitance of the switches in the main branch. The circuit could be implemented using MOMcaps in layers M1-M3 under the main SPCP capacitors, incurring no additional area overhead.

Bodies of the HV pMOS M_{B6} - M_{B8} were shorted to the devices' source terminals, generating significant parasitic coupling between the deep n-well of the HV devices and the substrate. Although it provided the most straightforward solution in a self-biased version, it is not optimal. The auxiliary biasing structure would allow the bulk to be constantly biased to the maximum output voltage, eliminating the charging cycle of the bulk parasitics.

The weakness of the SP design is the incrementally larger amount of charge needed to charge ($\propto N^2$, N = number of stages) the parasitic capacitances in each stage. Apart from the methods mentioned before to reduce the absolute value of parasitic effects, the output current capabilities of the device could be potentially improved by a laddered clocking scheme to change the parallel-charge to serial-discharge transition. Figure 3-22 shows a three-stage self-biased SPCP with an additional set of nMOS connecting to bottom plates of the pumping capacitors, and its clocking scheme. The additional inputs to the circuit transform it into a semi-linear CP, and reducing the sensitivity to parasitic capacitances and improving its current efficiency. It is assumed that an auxiliary biasing circuit is used for all HV wells.

The behaviour of the circuit is as follows. Assuming a V_{DD} supply voltage, after capacitors C_1, C_2 and C_3 are charged in parallel to V_{DD}, $M_{1\text{-}3}$ are disabled and, instead of connecting the bottom plate of C_1 to V_{DD} (as in the original self-biased SPCP design), switch M_8 is turned on first: node V_{B3} is charged to V_{DD}, which increases V_{T3} to $2V_{DD}$. A full V_{DD} swing at the capacitor bottom plates is achieved with the help of capacitive level shifters used to boost the gate voltage of M_6, M_7 and M_8. After a delay, M_7 is enabled: V_{B2} is charged to V_{DD},

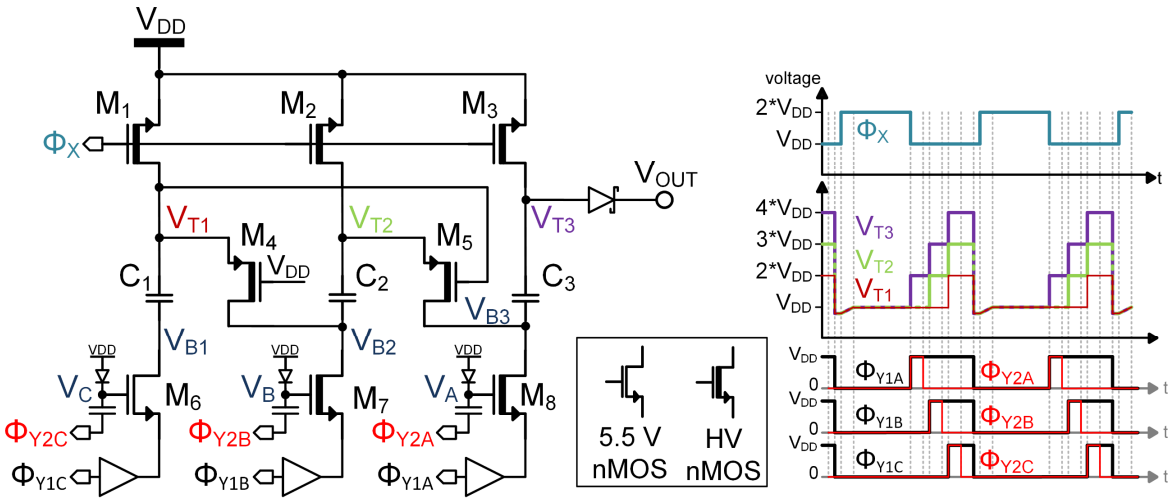

Figure 3-22. Incremental charging example for a three-stage SPCP for reduced parasitic effects (left) and its timing diagram (right).

which raises V_{T2} to $2V_{DD}$. As the gate of M_5 is at V_{DD}, V_{B3} is charged to $2V_{DD}$ as well, leading to $V_{T3} = 3V_{DD}$. The same cycle is repeated for M_6 and the output reaches $4V_{DD}$ - $V_{SCHOTTKY}$. In the traditional SPCP, $Q_{PAR} \propto 12V_{DD}$, excluding the initial parallel precharge, and with the loss occurring simultaneously in every stage. In the incremental scheme, the total Q_{PAR} is the same, but the last charging phase Φ_{Y2C} needs to supply stray capacitance with $Q_{PAR} \propto 6V_{DD}$. As a result, its current sourcing capabilities improve by 50% in a three-stage SPCP, although it still cannot surpass linear CPs that, in every output phase, charge only $2V_{DD}$ worth of Q_{PAR}.

The three-stage circuit also allows for configurable output gain x2/x3/x4 and, with the introduction of an additional output monitoring circuit, dynamic control of the duration of each phase (Φ_{Y2A}, Φ_{Y2B}, Φ_{Y2C}) can be achieved for improved output sourcing capabilities. Nonetheless, due to discrepancies between measurements and simulation of the SPCP stage and a shift in research focus to higher HV current specification, the circuit solution presented in Section 3.5.4 was not pursued further in either simulation environment or in later tape-outs.

3.6 Conclusions and Future Work

This chapter concentrated on a new HCP design comprising a zero-reversion loss CC and self-biased SP stages. Reasons for utilising a CP rather than a switched inductor supply and choosing a particular CP topology have been discussed, together with an investigation into the viability and optimal design of an integrated SPCP and CCCP design.

Measurements of the single-stage CCCP and four-stage DKCP matched closely with the post-layout simulation results; however, a significant discrepancy in the self-biased SP circuit was observed. Although the exact cause of the issue could not be verified, two reasons were identified. The first one was unaccounted leakage currents that were communicated by Dialog Semiconductor during the testing stage, and that exist within the vertical structure of HV MOS devices as well as Schottky diodes. While effects of the former could be magnified by the self-biased scheme, the contributions due to the latter were observed to match simulation results in the DKCP. The second reason was potentially higher parasitics. Solutions to this issue were suggested, namely, the incremental switching scheme of the SPCP has been introduced to create a multi-input charge injection setup to improve CP's current efficiency.

Based on the measurements, the proposed HCP design cannot be recommended for fully integrated circuits in CMOS BCD technologies, but its use could be found in more advanced SOI processes that exhibit lower parasitic and leakage effects. At the same time, the CCCP and the DKCP have shown strong support for using them in fully integrated circuits.

4 HIGH-VOLTAGE GENERATION IN ULTRASOUND CAPSULE ENDOSCOPY APPLICATIONS

4.1 INTRODUCTION

High-voltage generation for intracorporeal devices is often limited to low current (< 200 µA) applications such as MEMS, SPAD biasing or flash memory [221]–[224]. Some higher current designs exist but are often directed towards niche applications [225], are unregulated [181], [226] or do not reach > 20 V output voltage [227], [228]. These drawbacks are not an issue of concern but rather a consequence of tailoring the CP architecture to specific requirements and technology capabilities. As a result, it leads to ambiguity when a different specification is needed. In the case of a USCE, both high voltage and high output current are required to improve the SNR of the US system while maintaining amplitude levels with a > 20 kHz pulse repetition frequency (PRF).

This chapter focuses on HV generation for an USCE, although the presented design is viable for other HV applications, e.g. fluorescence sensing [229], [230]. It is split into two sections: the first describes the design and manufacture of a 20 V output, high output current, fully-integrated, regulated CP. The characterisation of the CP is provided, and measurements of hysteresis and latched regulation is discussed. The second section discusses a fully-integrated self-oscillating charge pump (SOCP), comprising a current-comparator (CUC) and a cross-coupled charge pump (CCCP) to achieve a 5.5 – 6 V unregulated output voltage from a 3 V input. It utilises the CUC for clock generation with minimum area requirements and improvements in the input current transients.

The two CPs presented in this chapter were designed in the TSMC 0.13µm BCD process. The first design was manufactured, characterised, and tested, whilst the second circuit could not be manufactured due to global chip supply chain difficulties that led to delays and a change in technology, halting the development of the design in the initially chosen technology. As a result, extensive corner simulations are provided to validate the performance of the proposed SOCP design.

4.2 HIGH-CURRENT CHARGE PUMP

4.2.1 Specification and System Architecture

The CP's specifications were derived from the µUSCE system with a split transmit/receive array, as shown in Figure 4-1. The system included two serially-connected 1.55 V silver oxide batteries generating 3.1 V as the input supply. This voltage then had to be multiplied to a regulated 20 V output to be used as the supply to the HV pulser driving the ultrasound TX array, which was designed in the form of eight 1 x 4 mm^2 transducers situated around the circumference of the capsule. For a high precision 20 V output, a CP in series with a low drop-out (LDO) regulator would be required; however, it was decided that the LDO could be avoided to reduce the area overhead. This would result in a ripple defined by the regulatory scheme in the 20 V output, but the noise could be potentially filtered out in data post-processing due to periodic and predictable voltage variation patterns.

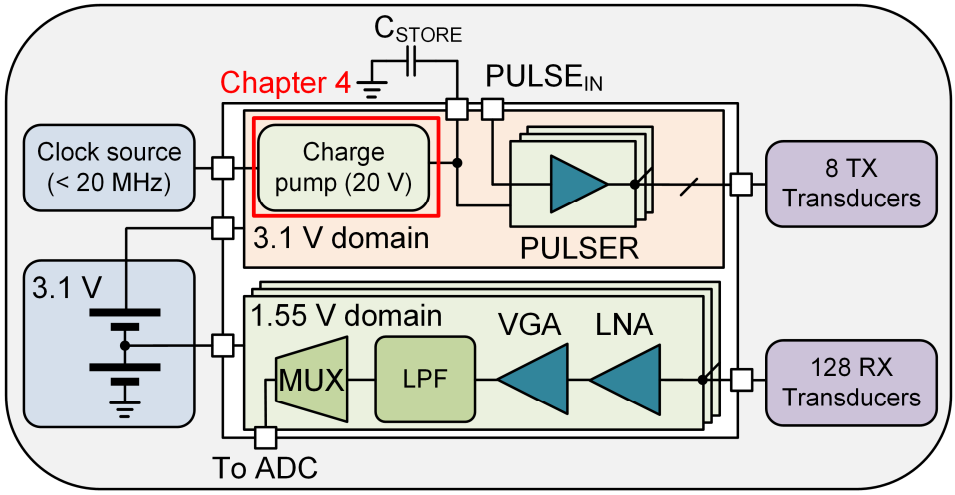

Figure 4-1. Outline µUSCE system diagram.

The CP's current sourcing requirements were evaluated by simulating the HV pulser operating at a 30 µs repetition period with an equivalent Butterworth-Van Dyke (BVD) model of each TX element. The detailed description is provided in Chapter 5: the instantaneous peak current was 6 A, which could not be provided by the charge pump alone, leading to a need for an external capacitor, C_{STORE} = 0.47 µF. The average current was then found to be 525 µA at a lower PRF of 25 kHz (40 µs period) and was used as the target specification at which a 20 V supply must be maintained. Generally, the current capabilities of a CP are proportional to its operating frequency and pumping capacitor size [231], leading to an exchange between switching power losses and chip area. In the CE, the clock would be generated from an

oscillator: whilst using maximum frequency can minimise the CP's area, it would increase not only switching CP's losses but also, in case of an external oscillator, losses from buffering the signal in the transmission lines between the controller and the chip, as well as their input-output (IO) ports.

Given that the CP uses a 3.1 V input rather than 1.55 V to reduce the number of CP stages, 5 V devices were used in the CP's control block, leading to slower propagation times in. At the same time, the optimal theoretical charge transfer happens when a 50% duty cycle of charge-discharge of the capacitors used in the CP is ensured. However, a non-overlap time t_{ovl} is always required to prevent losses due to reverse-leakage and buffer crowbar currents. The t_{ovl} generated by a 5 V non-overlapping clock generator was evaluated for propagation times, and the 20 MHz clock was chosen as the compromise for both high-operating frequency and charge transfer time.

The HV charge pump was based on the 3.1 to 6.2 V CCCP presented in Chapter 3, suggesting a single stage could achieve up to 78 % efficiency and a maximum of 1.98x (≈ 2) voltage multiplication, Figure 4-2 (a). The timing diagram is shown in Figure 4-2 (b). The same CC stage can be stacked linearly to achieve $V_{OUT} = N \cdot V_{IN}$, where V_{IN} = 3.1 V and N is the number of stages, resulting in a 10-stage design with a maximum 30 V output. To improve the CP's rise time, a boosted-clock scheme [217] was used to double the voltage from 3.1 V to 6.2 V initially and use it to drive both the input and the clock of the following four stages, Figure 4-2 (c), resulting in a 5-stage CP. Furthermore, the first stage output was tapped to be able to test its use as a 6 V input to an US pulser, if needed. As shown in Chapter 5, a system with only a single TX channel operating at time draws 38 µA current from the 6 V supply at a 40 kHz PRF.

In a system with a total charge capacitance $C_T = C_{CP} + C_{CKB}$, where $C_{CP} = \alpha C_T$ is the total CP capacitance across all stages, $C_{CKB} = (1-\alpha)C_T$ is the boosted stage capacitance of the first stage, generating $2V_{DD}$, α is the scaling factor (0 – 1) and C_{OUT} is output capacitance, it has been shown that the optimum rise time follows [217]:

$$\alpha_r = 3\frac{C_{OUT}}{C_T}\left(\sqrt{1+\frac{1}{3\frac{C_{OUT}}{C_T}}}-1\right) \tag{4.1}$$

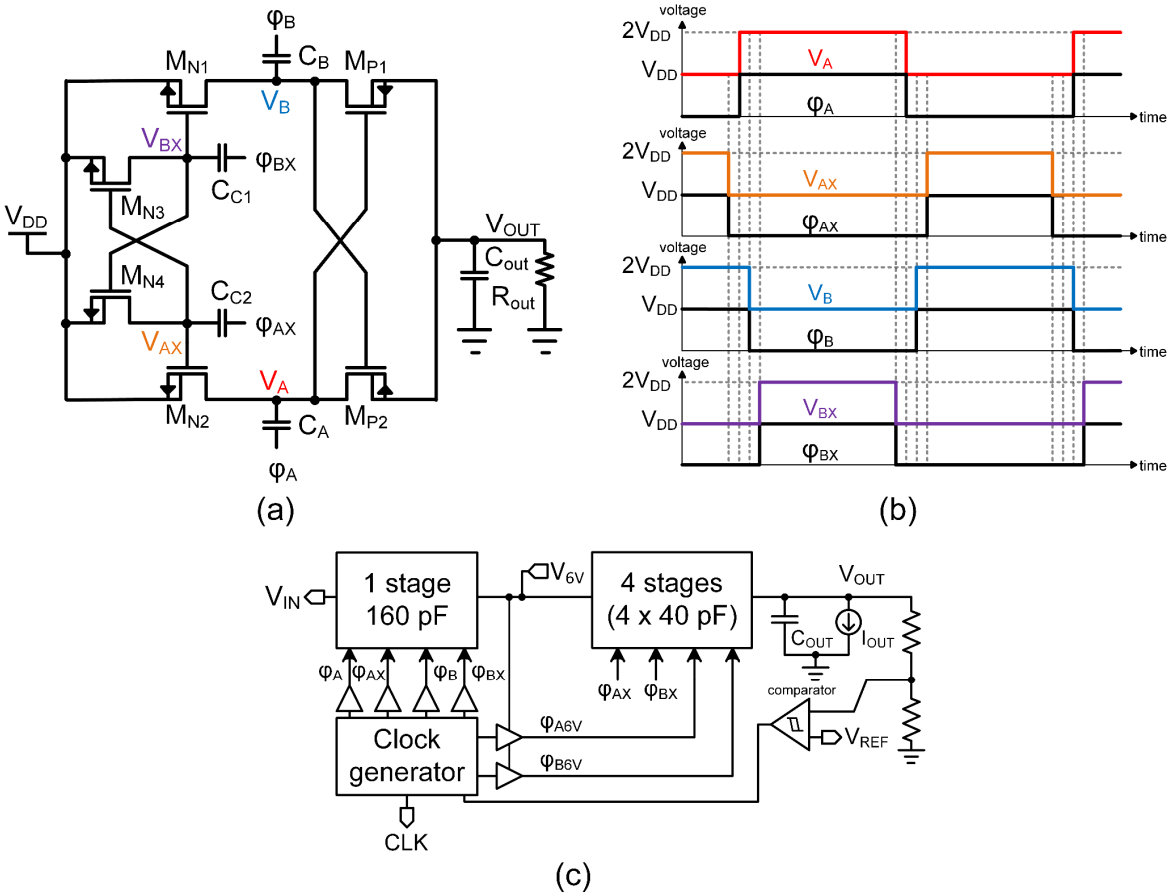

Figure 4-2. (a) Single stage cross-coupled charge pump. (b) Timing diagram of the circuit. (c) Five-stage regulated HV charge pump.

For systems where $C_{OUT} >> C_T$, $\alpha = 0.5$. Based on this observation and the current requirements of the CP, the first stage capacitance was set to 173.6 pF (86.8 pF x 2) and all subsequent stages to 43.4 pF (21.7 pF x 2). These values were based the specification and determined by multiplying the maximum size MIMcap to reduce the effects of the parasitic connection structure in it. It is also important to note that the boosted clock from the first stage had a limited driving capability in comparison to a battery source. Although the size of the first stage could then be increased to accommodate larger currents, it was left unchanged to save chip area whilst still meeting the $I_{OUT\text{-}HV}$ requirements.

4.2.2 Circuit Implementation

The CP schematic is shown in Figure 4-3 (a). The CP is controlled by four phases– φ_A, φ_B, φ_{AX}, and φ_{BX}. Large buffers are required to drive these signals, and so they are generated using a six-phase clock generator presented in Chapter 3, ensuring make-before-break operation

in the driver and reducing switching losses as a result, Figure 4-3 (b). The clock generator was based on a feedback mechanism, but to maintain the non-overlapping time to a minimum, the feedback signals for φ_{A1} and φ_{A2} were tapped from the outputs of the clock generator rather than the gates of the signal drivers. The CP uses the same building block across all stages, but the first stage has an additional inverter comprising M_7-M_{10}. It connects to the internal nodes V_A and V_B and is used to generate $0 – 2V_{DD}$ clock signals (φ_{A6V}, φ_{B6V}) for stages 2-5. Voltages V_A and V_B vary from V_{DD} to $2V_{DD}$ and mirror inputs φ_A and φ_B. Thus, the pMOS M_7 and M_8 were tied to V_{DD} to eliminate the need for additional level-shifters.

The CP's timing diagram is shown in Figure 4-3 (c). Signals φ_A and φ_B that are numbered denote signals from the non-overlapping clock generator, and signals φ_A, φ_B, φ_{AX} and φ_{BX} are the main CP inputs. It is important to note that the timings of signals φ_{A6V} and φ_{B6V} correspond to φ_A and φ_B, respectively. Assuming steady-state operation of the CP, initially, Figure 4-3 (c), marker Z, φ_A and φ_{BX} are at 0 V, and φ_B and φ_{AX} are at V_{DD}; signals φ_{A6V} and φ_{B6V} are at V_{DD} and $2V_{DD}$, respectively. Node V_A is charged from the input and V_B is discharged to the output and into φ_{B6V}. On the next clock transition, φ_{AX} drops to 0 V, disconnecting V_A from the input, while φ_A rises to V_{DD} and M_6 is turned off. During the transition, when V_A rises above $V_{DD}+V_{TH-P}$, M_8 becomes conductive, and φ_{A6V} is pulled to $2V_{DD}$. The signal φ_B goes low, and V_A begins to discharge to the output. After φ_{BX} reaches V_{DD}, node V_B begins to recharge.

When V_A or V_B rises to $2V_{DD}$, the other node is still high, and there is no current flow from these nodes to the output V_{6V}. If the parasitic capacitances in nodes φ_{A6V} and φ_{B6V} are low, V_A and φ_{A6V} will reach 6.2 V during the non-overlapping time before the connection to the output is established. In that case, the CP was set to operate at 20 MHz, and the overvoltage duration was approximately 4 ns or 8% of the period. This transient spike would degrade the long-term reliability of the circuit, even though the CP is required to work only a fraction of the time defined by the frame rate of the CE device. Compliance can be ensured by reducing the

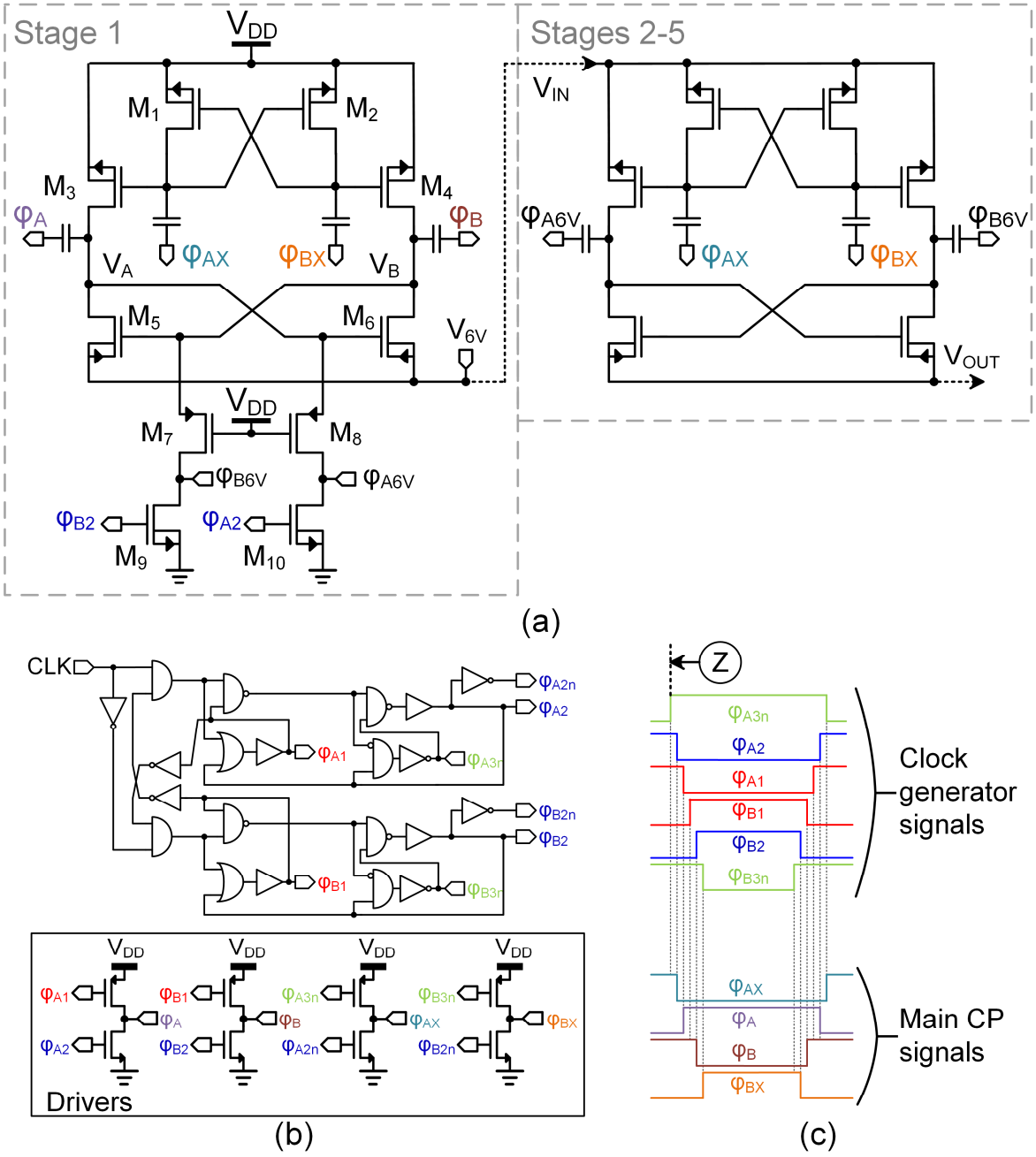

Figure 4-3. (a) Schematic of the HV CP. (b) Clock generation and driving of the charge pump. (c) Timing diagram of the CP. The 'n' at the end of the clock name identifies the inverted phase. E.g., φ_{A1n} is an inverted clock of φ_{A1}.

input to 3 V, but it would result in a 1 V loss in the output and reduced efficiency. Furthermore, the CE system is disposed of after a single 15-hour use, and the effects of the prolonged over-voltage exposure should not become evident in such a short operational lifetime. However, the safe operating area (SOA) defined by the technology does not define gate-source voltage

conditions > 6 V. Furthermore, this could not be verified experimentally, and further investigation is needed if the 3.1 V input voltage is to be used.

4.2.3 Regulation

Due to the limited amount of charge a CP can transfer over time from the input to the output, its output resistance is finite, and the output voltage is inversely proportional to the load current. The formula for R_{OUT} can be derived as [232]:

$$R_{OUT} = \frac{N}{fC_{ST}(1+\beta)} + \frac{3}{4fC_{OUT}} \tag{4.2}$$

where N is the number of CP stages, f is the operating frequency, C_{ST} is the stage capacitance, and $\beta = C_{PARA}/C_{ST}$ is the fractional parasitic capacitance. The same expression applies to a CCCP, where C_{ST} is the summed capacitance of the two branches. In the USCE application, a large external storage capacitor is used, which is at least 1000x larger than $C_{ST,}$ and the above equation can be simplified to:

$$R_{OUT} = \frac{N}{fC_{ST}(1+\beta)} \tag{4.3}$$

This expression determines the fundamental limit of the output current, below which the output voltage can be regulated, given a fixed frequency. This limitation can be circumvented by a frequency-based conversion scheme where f is generated and regulated by a VCO, but such systems exhibit a significantly smaller output current range for a given efficiency. They also do not permit complete disabling of the CP – a crucial feature for USCE applications, where the CP might be unused for extended periods.

The CP was designed to be used as an input to a high-voltage US pulser, and its output was expected to be regulated at a voltage < 22 V to ensure that the lower hysteresis limit is > 20 V for all corners. Two versions of a duty-cycle regulation scheme were implemented to meet this demand, differing in the comparator type used.

The first version was based on a static comparator, as shown in Figure 4-4 (a), with its hysteresis defined by:

$$\frac{M_3}{M_5 + M_7} = \frac{M_2}{M_4 + M_6} \tag{4.4}$$

where $M_X = W_{DEVICE}/L_{DEVICE}$ defines the sizing ratio. The output stage used a CCCP that allowed the decision to occur without a clocking circuit and incurred no static losses through M_4, M_8 and M_5, M_9. Resistors $R_1 = R_2 = 20\ k\Omega$ were added to allow smaller and weaker $M_{2/5}$ to

be used to turn on $M_{3/4}$. The hysteresis was implemented with an approximately 1 V output ripple. As this ripple was dependent on the current draw from the CP and was defined by the pulser operation and transducer load, it would potentially be reflected in a varying amplitude of the excitation US signal, leading to imaging quality degradation.

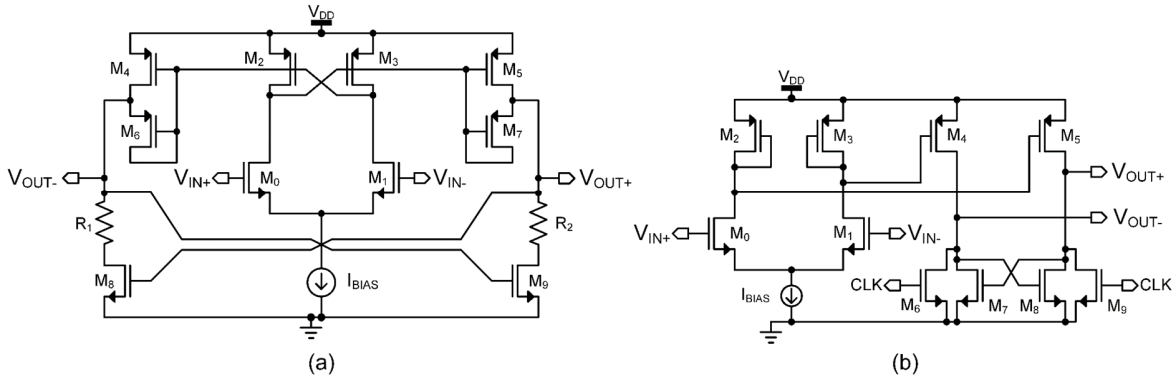

Figure 4-4. Comparators used for output regulation of the output: (a) hysteresis; (b) latched.

Nonetheless, signal post-processing could still be used to eliminate the noise due to voltage ripple in the excitation signal. Its implementation could potentially take the periodicity and amplitude variations into account, based on the well-defined nature of the ripple that is defined by the output capacitance of the CP and load current. However, the effects of the ripple were not within the scope of the study and were not evaluated in greater detail.

Consequently, a second CP using a static latched comparator was implemented, Figure 4-4 (b). The advantage of the second implementation is that there are no PVT-dependent hysteresis variations. In contrast, the comparison is carried out every clock cycle, which results in a very close output voltage definition. This introduces additional power losses but ensures regulation with minimum ripple proportional to the charge loss over a single clock cycle, excluding mismatch in the comparator itself.

4.2.4 Results and Discussion

The CP with two types of regulation was implemented in TSMC 0.13 µm BCD, 4-metal process and occupied an area of 0.385 mm^2, Figure 4-5. To achieve the highest possible efficiency, MIMcaps in layers M3 and M4 were used instead of MOMcaps due to their higher capacitive density and lower parasitic capacitance. The use and placement of the MIMcaps resulted in the highest possible efficiency at the cost of long-term reliability defined by the typical breakdown voltage of V_{MIM} = 22.5 V. The chip was bonded to a test PCB, as shown in Figure 4-5 (b).

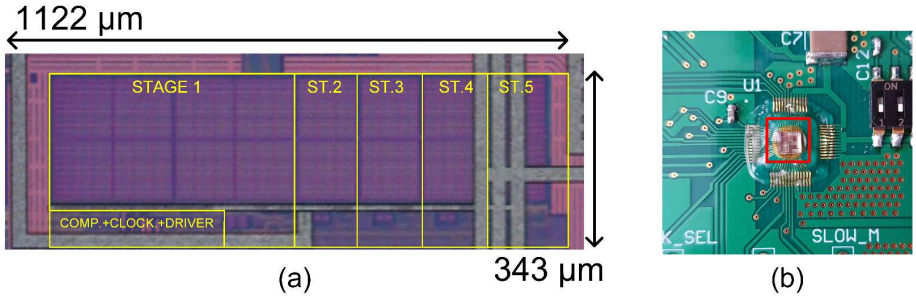

Figure 4-5. (a) Macrograph of the manufactured CP. (b) Wire-bonded chip on a test PCB.

The CP was initially tested with regulation disabled and using a constant current load ranging from 0 to 800 µA, provided by a source measurement unit (SMU). The circuit was tested with nominal voltage of 3.1 V and 2.8 V to evaluate battery voltage drop under large load currents (I_{OUT}). Measurement results and post-layout simulation data of V_{OUT} and efficiency at the 20 MHz input clock are shown in Figure 4-6 (a) and (b), respectively. The output voltage measurements, Figure 4-6 (a), closely matched simulation data with a 3.1 V supply for I_{OUT} < 350 µA but degraded faster when I_{OUT} increased up to 700 µA. At the same time, a lower gradient was observed at 2.8 V, resembling the gradient of the simulation results more closely, which can indicate that due to larger circuit resistance, the complete charge transfer to reach 3.1 V could not take place when more charge was consumed at the output.

Furthermore, for both supply voltages, the CP's V_{OUT} dropped to zero at I_{OUT} = 700 µA, indicating its limit. Nonetheless, the CP could generate the required minimum of 20 V up to 500 µA with 3.1 V input and up to 400 µA with 2.8 V input voltage. These values are close, but below the 525 µA specification, which indicates that lower operating voltages or lower PRF must be used in the pulser, powered by this CP. The efficiency data, Figure 4-6 (b), also differed from the simulation results: the peak measured efficiency was achieved at 350 µA rather than the simulated 450 µA, although its peak value matched closely at ≈ 58% compared with the simulated value of ≈ 58.7%. With 2.8 V supply, the efficiency was higher (≈ 61%), which corroborates the hypothesis of insufficient charging time with the 3.1 V supply.

The output resistance and input power were measured across input clock frequency, Figure 4-6 (c), with a 100 kΩ resistor. Based on the measurements, the charge pump is operating above the FSL. Under this condition, the resistance associated with the switches, capacitors, and interconnects dominates the overall resistance [233] and leads to lower performance metrics. The input power at 20 MHz was measured to be close to 10 mW, which is a considerable figure in a battery-powered USCE system that operates with an ADC and other components

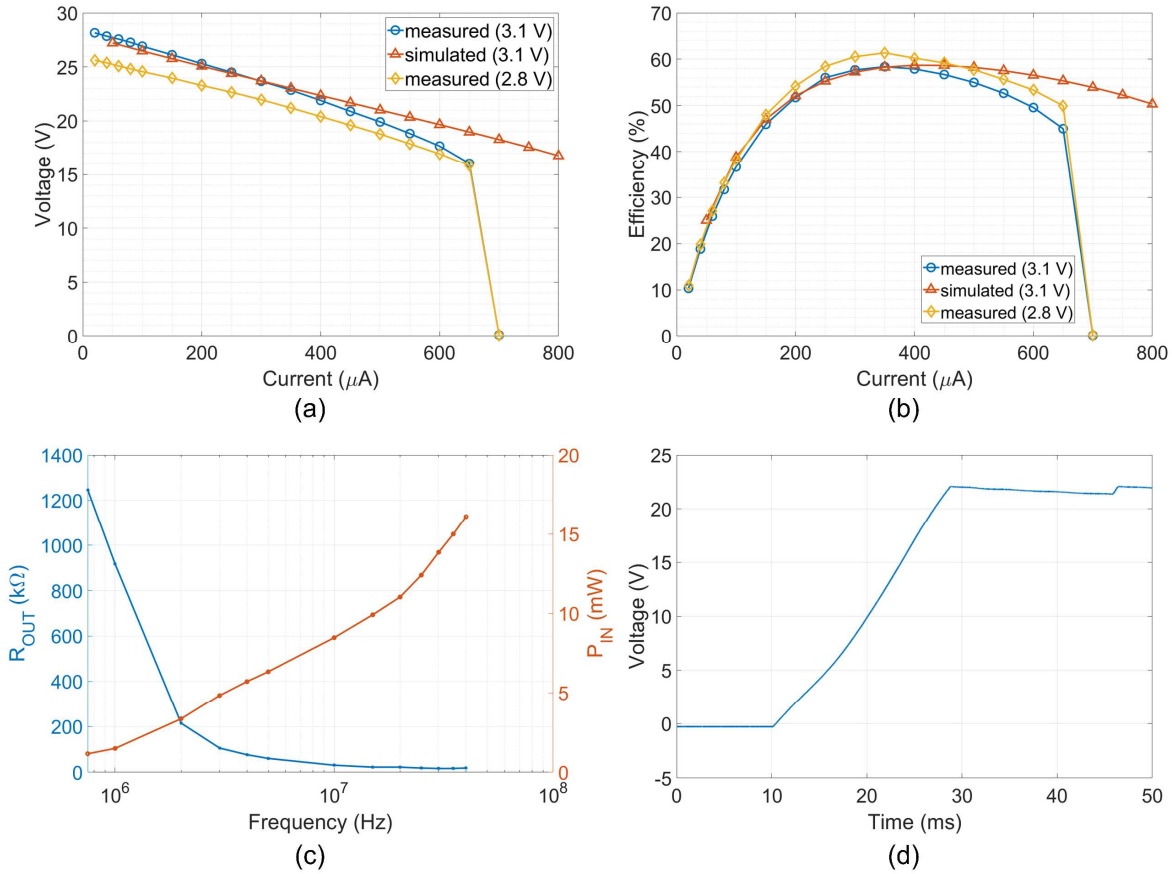

Figure 4-6. (a) Output voltage vs output current, (b) Power efficiency vs output current, (c) Output resistance and input power vs operating frequency. (d) Transient rise time with a 0.47 µF load capacitor.

simultaneously. The transient rise time with a 0.47 µF external storage capacitor is shown in Figure 4-6 (d). The total duration can be observed to be ≈ 18 ms. The CP acts as a constant current source during this time, supplying a constant 574 µA at > 50% efficiency.

The efficiency variation with the operating frequency f_{IN} is shown in Figure 4-7 (a): the CP achieves a maximum efficiency of 66% at 5 MHz and then decreases with increase in f_{IN}. The data suggest that controlling f_{IN} is necessary to achieve the optimal operating point. Two regulation methods were tested using a hysteresis and a latched comparator as described in Section 4.2.3. The goal was to evaluate the difference in ripple observed at the output of the CP. The measurements of the output ripple at I_{OUT} = 100 µA are shown in Figure 4-7 (b). The hysteresis control resulted in ripple of 2 V_{PP}, whilst the latched control reduced this to 0.4 V_{PP}.

V_{OUT} vs I_{OUT} for the two regulation methods is shown in Figure 4-7 (c). The hysteresis control resulted in a well-defined V_{OUT} up to I_{OUT} = 400 µA, while the latched control had a continuous negative gradient even at lower currents, in the range 0 - 100 µA. An output voltage

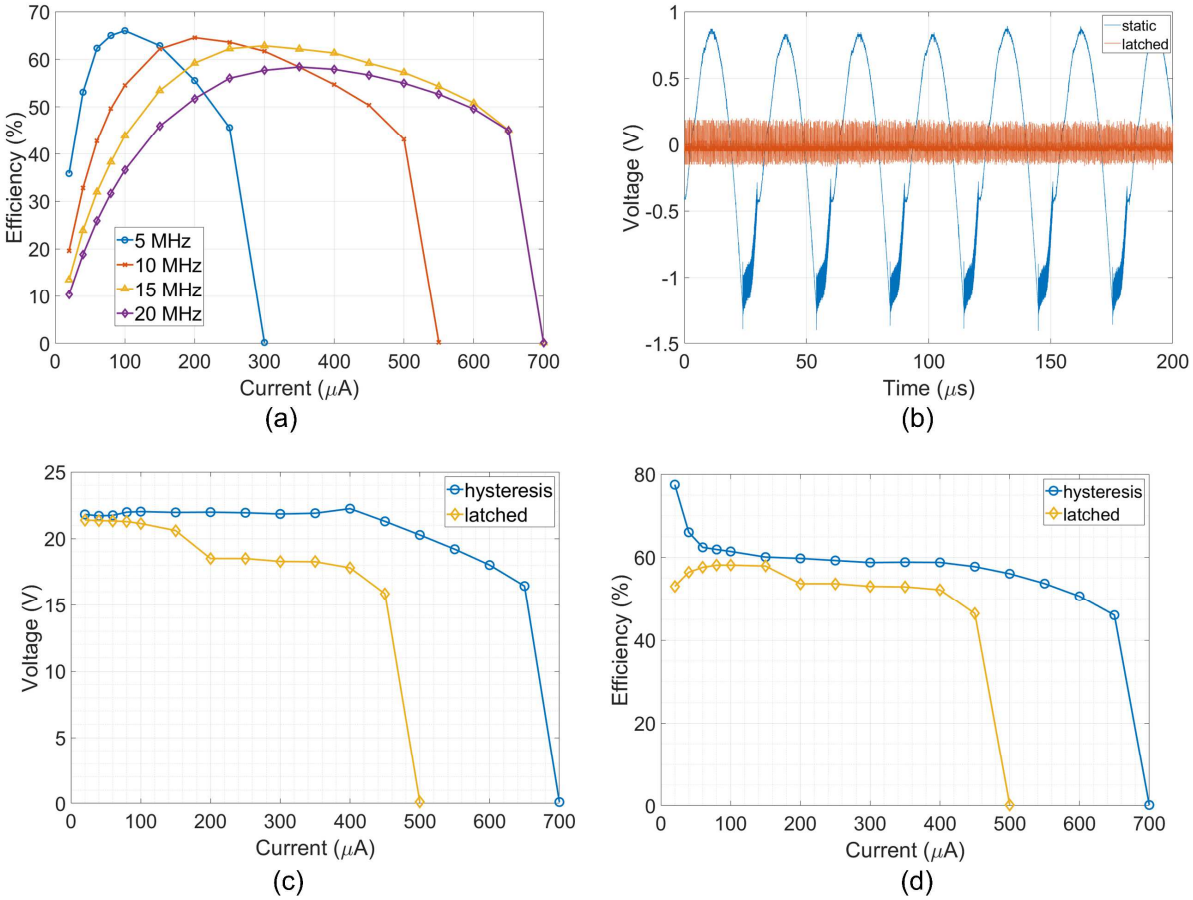

Figure 4-7. (a) CP efficiency vs clock frequency. (b) Output ripple voltage of hysteresis and latched comparator regulation. (c) Output voltage and (d) efficiency of the two regulation schemes.

drop was observed between 100 µA and 200 µA in the latched version, after which a new stable range 200 – 400 µA was reached. Moreover, the output voltage dropped to zero at I_{OUT} = 500 µA in the latched version compared to I_{OUT} = 700 µA observed in the hysteresis implementation for Vin = 3.1V. Whilst the former step-down action between 100 - 200 µA could not be explained, the latter reduction in range was attributed to the reduction in the operating period: the latched comparator was triggered simultaneously with the non-overlapping clock generator. Due to the delay in the comparator, this led to reduced time for charge transfer, resulting in lower I_{OUT} capabilities. The efficiency measurements, Figure 4-7 (d), also indicated that the hysteresis control allows significant power savings at low I_{OUT}, reaching 78%, while the latched version was limited to 58%. In a USCE device, the HV system is likely to be disabled most of the time, and, thus, output regulation using a hysteresis comparator is a better choice unless an auxiliary power-down controller is available.

A summary of the HV CCCP parameters and comparison to prior work are shown in Table 4-1. The HV CCCP achieves the highest efficiency for one of the highest output currents. Although its output power density is lower than the design in [234], it operates at 2.5x lower frequency and achieves 1.7x higher efficiency. The summary in [235] also illustrates that significantly higher output currents can be achieved without any external components, at the price of power efficiency and larger stage capacitance.

Table 4-1. Design parameters and comparison to prior work.

Reference	This Work	[236]	[234]	[235]	[181]
Input Voltage (V)	3.1	2.5	3.3	3.7	2.5
Output Voltage (V)	28	21	19.6	14	36
Load Current (µA)	600	100	150	11000	20
Number of Stages	1 + 4	10	11	4	12
Stage Capacitor (pF)	160 + 4 x 40	6	1.2	264	8
Frequency (MHz)	20	25	50	20	4
Efficiency, η_{MAX} (%)	58	48	34	29	49
Area (mm^2)	0.385	0.13	0.063	-	0.18
Output Power Density @ η_{MAX} (mW/mm^2)	20.9	16.1	38	-	2.8
Technology	0.13 µm HV BCD	65 nm CMOS	0.18 µm CMOS	0.18 µm HV BCD	65 nm CMOS
***Post-layout simulation.**					

4.2.5 Conclusions

This section has discussed a fully-integrated HV high output current CCCP designed in the TSMC 0.13 µm BCD process. The circuit was manufactured and fully characterised for use in an USCE system. The results indicated that the design could achieve maximum efficiency of 78% at 5 MHz and 58% at 20 MHz. Two regulation schemes using a hysteresis and a latched comparator were tested with regard to V_{OUT} ripple. Whilst the former allowed for a wide range of regulation and improved efficiency, it led to 2 V ripple that could affect the generated US pulse quality. Alternatively, the latched version reduced the ripple to below 50 mV, but its clocking scheme degraded the output current sourcing capabilities. The measurements confirmed that a fully-integrated CP could be used to generate V_{OUT} > 20 V stably and meet the specification of the desired output current.

4.3 SELF-OSCILLATING CHARGE PUMP

4.3.1 Introduction

A clock source is fundamental for CP operation. The universal choice is to assume that the clock can be generated from a constant frequency external or internal oscillator source. The externally generated clock is considerably the most disadvantageous solution as it incurs overhead energy losses associated with IO buffering and charging capacitance of interconnects as well as injecting high-frequency noise into other parts of a system. These effects are further exacerbated in tiny form factor systems for intracorporeal applications, e.g., CE devices or neural implants, leading to the need for an on-chip clock source.

The clock frequency set for a CP is chosen based on the technology while considering switch sizes and the charge required to transfer over time. Increasing the frequency reduces the CP's capacitor size and saves chip area but leads to higher switching losses [205]. As a result, most of the reported CPs operate below 50 MHz [181], [237]–[239]. In this frequency range, relaxation oscillators are an attractive choice as they allow for clock generation with power consumption ranging from a few hundred nW/MHz to a few tens of μW/MHz from < 1.8 V supplies [240]–[242]. Most of these circuits are focused on improving power consumption whilst reducing the temperature drift, the latter of which is not a crucial design corner in intracorporeal applications due to the narrow temperature range (36 - 41°C).

Integrating a clock generator with feedback from a CP output can also be used for frequency-based regulation [243]. Most CPs are unregulated and are designed to operate at optimal efficiency at specified V_{OUT} and I_{OUT} [7], [221], [244]. In other applications where regulation is required, feedback from a resistively-divided output is compared to a stable reference voltage, enabling or disabling a constant frequency clock source (pulse-skip regulation). As has been practically demonstrated in Section 6.2.4, the downside of this technique is the existence of a large, hysteresis-defined ripple or the necessity to perform a comparison on every clock cycle, leading to higher energy losses. Alternatively, for lower ripple regulation, control of the frequency of the clock itself can be employed, using a current-controlled ring oscillator [223], [228], allowing for ripple amplitude reduction down to 18 mV. At the same time, reducing the clock period of the oscillator can further reduce the system's power losses.

This section presents a self-oscillating (SO) voltage doubler, using a current comparator (CUC) as a current-controlled delay element functioning in tandem with the feedback from the CP. The proposed circuit allows for stable clock generation using very few components in intracorporeal applications. Furthermore, the proposed implementation flattens the charging current, eliminating or lowering requirements of an input smoothing capacitor and providing better compatibility with power-limited WPT systems [245]. It also requires no additional phase generator previously reported by Luo et al. [227] to smooth the input current. Results of the corner analysis in the TSMC 0.13 µm BCD process with a 3 V supply are presented and discussed, including methods for frequency and pulse-skip regulation.

4.3.2 System

SOCPs belong to a very narrow topic with only a few examples available in the academic literature. To the best of the author's knowledge, there have been only two SO CPs reported at the time of the writing. The first one was invented by Ivanov and Jancij [246] and is a current-mode (CM) CP designed for generating a low-ripple boosted voltage to bias a current source used in an operational amplifier. The design, Figure 4-8 (a), achieved self-oscillation by using a current source controlled by a comparator (1B) to charge and discharge flying capacitors of the CP in tandem with a comparator (1A) to sense the voltage of the bottom plate of the capacitors. A voltage-mode SO CP was presented by Jung et al. for energy harvesting applications [247]. The implementation fully internalised the oscillator in the 23 serially-connected, parallel-connected element CP circuit, reducing operating power consumption and chip area. Additional voltage-controlled delay elements were included between stages to set optimum conversion efficiency.

The two SO CPs are ideal for their niche applications but exemplify the fundamental issues with applying SO in a generic voltage-mode (VM) CP design: the need to actively sense the charge delivered to the output. In the current-mode CP, the charge/discharge characteristics and time constants are known and can be used to derive comparator speed requirements and prevent the CP from saturating. In the energy-harvesting CP, saturation is not essential as the

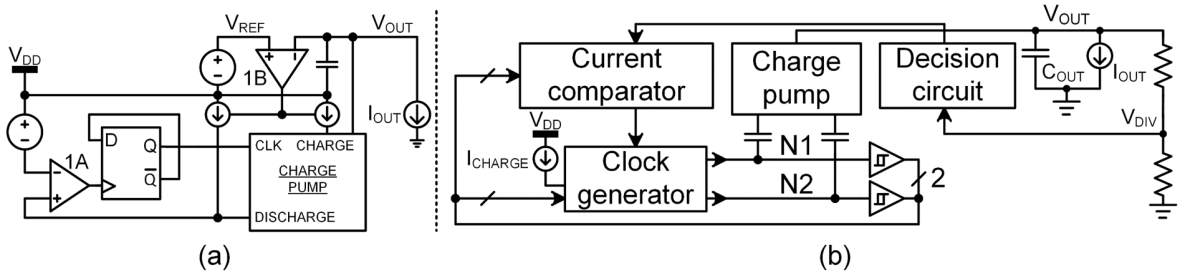

Figure 4-8. SO current-mode CP by Ivanov and Jancij. (b) Proposed SO voltage-mode CP.

circuit is oscillating continuously and independently from the output current. These aspects are not applicable in VM CPs, where the output current can drop to ~ 0 A, leading to saturation and cessation of oscillation. At the same time, using CM imposes limits on I_{OUT} and on the recharge time of V_{OUT}. Consequently, SO in a VM CP becomes non-viable, with any benefits that it could offer being offset by high-speed sensing circuitry.

The SOCP proposed here is shown in Figure 4-8 (b). The system uses a CUC to generate a clock signal using its input-current-dependent propagation delay as the basis for clock frequency definition. The clock generator limits the charge time of N1 and N2 with a current source until a threshold is sensed by Schmitt triggers, enabling a pull-up action in the nodes, resetting the comparator, and completing the cycle. The present work did not include the decision circuit used for regulation, but the CP is compatible with both current-controlled frequency regulation and voltage-based pulse-skip regulation. The whole circuit was implemented with 5.5 V devices and a 3 V[3] supply to maintain a single voltage domain across the whole system whilst generating a boosted output of < 6 V. However, the CUC and clock generation circuits can be moved to the 1.5 V domain available in the same technology to reduce the overall power consumption and increase oscillation frequency.

4.3.3 Current Comparator Oscillator

A CUC is a comparator circuit that evaluates polarity of the input current flowing into its input terminal. Generally, the input current is a sum of two currents being compared. The propagation time is determined by its gain and input current, which was advantageously used as a current-controlled delay element for clock signal generation. For this application, Traff's architecture was chosen, Figure 4-9 (a) [248]. It uses a source follower (M_1, M_2) and an inverter (M_3, M_4) in a positive feedback configuration to reduce input impedance and increase evaluation

[3] note the reduction from 3.1 V

speed. If the input current, $I_{IN,}$ is the difference between two currents being compared when I_{IN} is positive, V_1 is pulled to $V_{DD,}$ and because of the positive feedback, M_1 is disabled, and M_2 is enabled. Input impedance is then defined by M_2 and is low. When I_{IN} becomes negative, the current cannot be supplied through $M_{1,}$ and V_1 enters a high-impedance state until it drops low and causes the positive feedback (V_2 goes high) to enable M_1. This dead-band region is defined by threshold values of M_1, M_2 and is the feature that is used in this SOCP to generate an oscillation proportional to the input current.

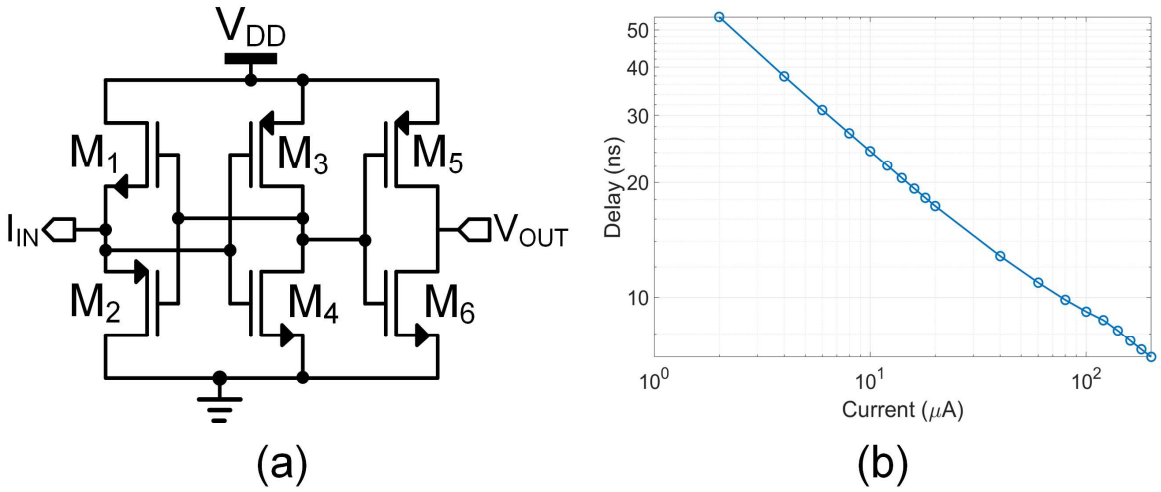

Figure 4-9. (a) Schematic of Traff's current comparator. (b) Propagation delay vs current step. Current value is half of the simulated step (e.g. -2μA to 2μA step is marked as 2μA in the plot).

Several improvements to eliminate or reduce the dead-band region for faster propagation time with lower input currents have been presented in the literature [249]–[251]. However, they lead to lower propagation times and higher average power consumption than Traff's comparator across the same range of input currents or require additional biasing circuits. Reducing the input-output propagation time is beneficial in native comparator applications but is disadvantageous in this instance, where the clock frequency specification chosen was < 50 MHz. Assuming that the CUC is the main delay contributor in an oscillator, this results in T_{CLK} = 20 ns and a required propagation time of 10 ns. Traff's CUC results in the fewest components compared to alternative CUCs, simplifying the design and leading to the minimum chip area, but lower propagation time CUCs can be used for CPs with shorter clock period demands.

The average I_{IN} and propagation times as a function of I_{IN} to Traff's comparator are shown in Figure 4-9 (b). The propagation time can be observed to be linearly proportional to

the current in a log-log plot which means that the delay time is linearly proportional to I_{IN} defined as:

$$t = 10^{b} I_{IN}^{-m} \tag{4.5}$$

where t is propagation delay, b is the y-axis intercept point, I_{IN} is the input current, and m is the slope of the log-log graph. The non-linear control of the delay that determines the oscillation period of the circuit described in Section 4.3.4 can be advantageous in providing a faster response time [252]. Nonetheless, the log-log relationship can be conditioned into a linear relationship with the help of exponential current-mode signal conditioning circuits [253]–[255].

4.3.4 SOCP Architecture

The complete proposed circuit of the CP is shown in Figure 4-10. The oscillator is depicted in Figure 4-10 (a); M_7, M_8 are sized 1:1. The operation can be described as follows. The CUC's input node is V_{CI}, with the negative current component defined by I_{BIAS1} and the positive component by I_{M3}. During the power-on-reset (POR), V_{CI} is pulled to V_{DD} through M_3 and V_{CO} is pulled high; the gate of M_2 is charged to V_{DD} through R_1. After POR, M_3 is disabled, and $I_{IN} = I_{BIAS}$. After a delay defined by I_{BIAS}, V_{CO} will be pulled low, triggering a D-flip-flop, causing its output to toggle. When the change occurs, two feedback signals, V_{N1} and V_{N2}, generate $V_{AN} = 0$, which enables M_2 and, after a delay defined by the current difference ($I_{IN} = I_{M2} - I_{BIAS}$), V_{CO} is pulled high. When the V_{N1} and V_{N2} change, M2 is disabled, and the process begins again. The reset time is determined by the current sourced by M_2 and should be larger than the current sunk by M_8. The maximum reset duration is defined by the size of R_1 and should be longer than the lengthiest duration of the dynamically generated signal V_{AN}, occurring at the beginning of CP's operation.

The CUC oscillator is followed by a clock circuit, generating phases $\varphi_{A1\text{-}3}$ and $\varphi_{B1\text{-}3}$, Figure 4-10 (b). This, in turn, controls the main CP drivers, Figure 4-10 (c), which result in four phases – φ_{X1}, φ_{X2}, φ_{Y1}, φ_{Y2} – used to drive a CP. A simplified timing diagram of the buffer outputs is shown in Figure 4-10 (d). The current mirror comprising $M_{12\text{-}13}$ is used to limit the in-rush current into V_{DI}, which is needed to allow for V_{AN} to reset the CUC. This also limits the current flowing into the CP after a change in its state. The driver's operation, Figure 4-10 (c) can be described as follows. Initially, $\varphi_{X1\text{-}X2}$ are low, and $\varphi_{Y1\text{-}Y2}$ are high. When V_{CO} changes, φ_{B3} goes low, which pulls φ_{Y2} low and disables the pull-up device M_{18}. At this point, V_{AN} is pulled low, and the comparator begins to reset. Next, φ_{B2} and φ_{B1} become low one after another,

resulting in a break-before-make in node φ_{Y1}, pulling it low. Signal φ_{A1} goes high, followed by φ_{A2}, disabling M_{16}, enabling M_{14} and starting to charge φ_{X1} from V_{DI} at a constant rate until it reaches the upper threshold of ST_1 leading to the turn-on of M_{15}. This pulls φ_{X1} completely to V_{DD} and sets V_{AN} high (end of reset signal), restarting the comparator. After a short delay, φ_{X2} is pulled high, and the cycle is complete.

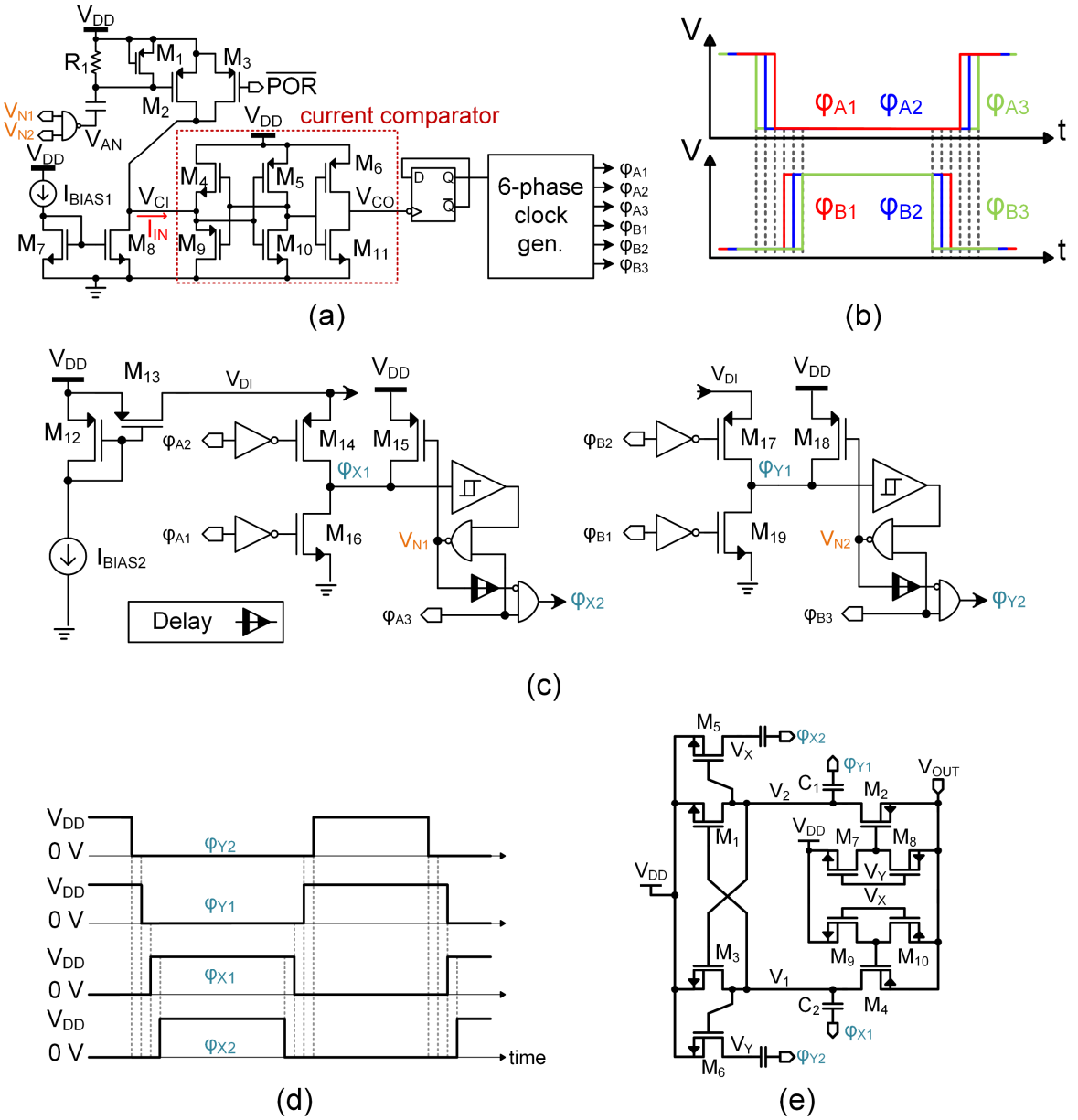

Figure 4-10. (a) Oscillator schematic. (b) 6-phase clock generator timing diagram. (c) CP input buffer with a feedback mechanism. (d) Timing diagram of the CP input signals. Phase relationship is equivalent to the buffer outputs in (c). (e) CCCP by Yu et al. [36].

The Schmitt triggers' threshold values and the limited current input from V_{DI} operate as dynamic delays that complete the reset once φ_{X1} or φ_{Y1} go high. As the reset signal V_{AN} begins after φ_{X1} or φ_{Y1} goes low, it is completed throughout the non-overlapping clock period, resulting in a negligible effect on the total period of the oscillation. If the period of the oscillation is proportionally larger than the time needed to reach the upper threshold of the Schmitt trigger, the designer has a choice to increase the current limit, leading to shorter reset times, at the cost of an increase in the M_2 current, required for resetting the comparator.

A CC voltage doubler by Yu et al. was chosen as the CP stage [209]. The circuit and its default timing diagram are shown in Figure 4-10 (e) and (d), respectively. The main CP branch comprises switches $M_{1\text{-}4}$ and $C_{1\text{-}2}$ – other components carry out switching functionality necessary for zero reversion loss operation. Its timing allows it to operate with the clocking scheme described in Section 4.3.4, but its original mode of operation is reiterated here for consistency and clarity. Assuming a steady-state, $\varphi_{Y1\text{-}2}$ are initially at V_{DD}, and $\varphi_{X1\text{-}2}$ are at 0 V, charging V_1 and V_X to $V_{DD,}$ while V_2 and V_Y are boosted to $2V_{DD}$. In this state, M_3 is enabled, and the boosted charge is deposited into the output. Clock, φ_{Y2} is then pulled to the ground, connecting the gate of M_2 to V_{OUT} and disabling it, followed by φ_{Y1} dropping to 0 V and disabling M_3. At this point, both V_1 and V_2 are in a high-impedance state. After a non-overlapping delay, φ_{X1} transitions to V_{DD}, boosting V_1 to $2V_{DD}$, enabling $M_{1/6}$ and recharging V_2 and $V_{Y.}$ Finally, φ_{X2} rises to V_{DD}, resulting in the turn-on of M_4 and discharge of V_1 to the output. The same series of events occurs for the opposite clock change. The transient simulation of the CP's input clocks generated by the SO scheme in a steady-state is shown in Figure 4-11 and shows the relationship between the clocks and comparator nodes.

The SOCP architecture allows for regulating the output using pulse-skip or frequency control. In pulse-skip mode, the V_{CI} node can be pulled high to repeat a POR state. The pull-up strength must be larger than I_{BIAS1}, although disabling I_{BIAS1} to reduce power consumption is also possible. The frequency control can be implemented through the control of I_{BIAS1}. I_{BIAS2} can be moved from the V_{DD} side to the ground side to control the discharge rate of φ_{X1} and φ_{Y1} nodes and permit the SO functionality in different CP designs.

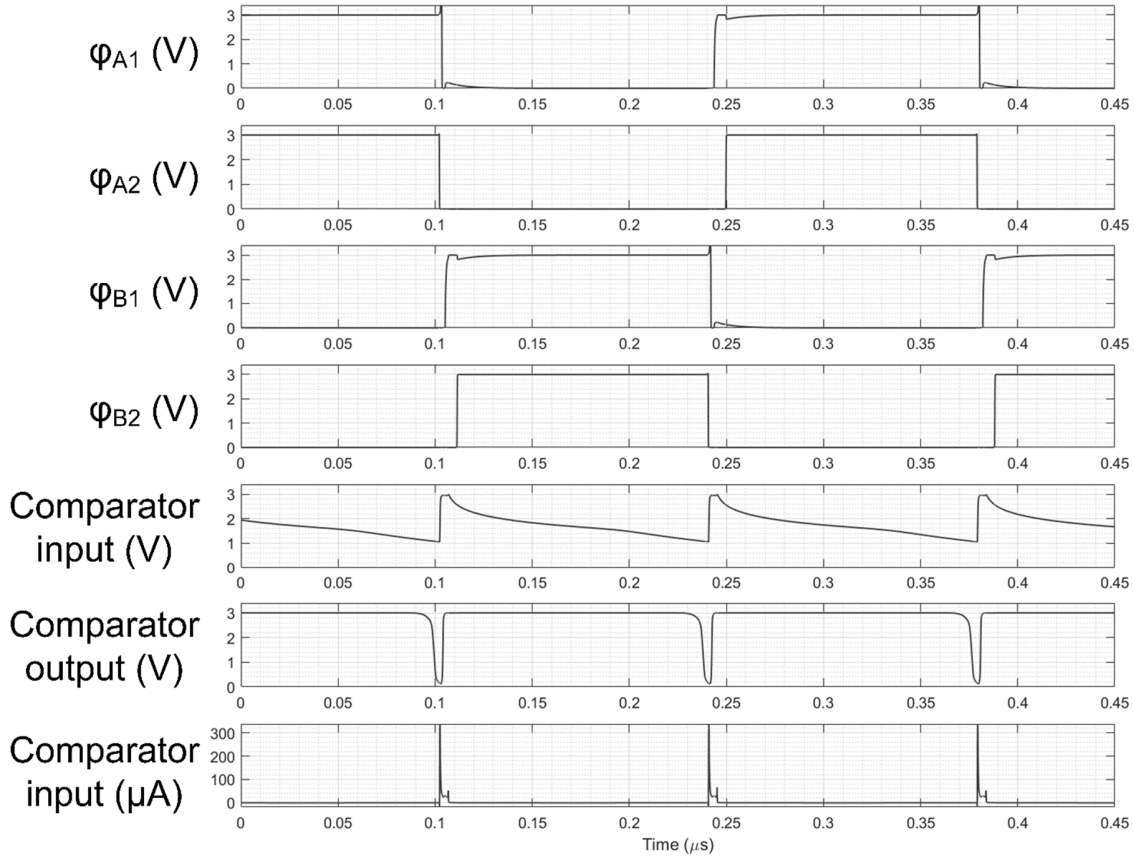

Figure 4-11. Transient simulation results of the SOCP in steady state.

4.3.5 Results and Discussion

The single-stage CCCP was integrated and simulated with the TSMC 0.13 µm BCD technology clock generating circuit. Supply inputs to the CP, comparator circuit, and clock generation were separated to evaluate each block's power consumption, and a single 3 V supply was used for powering the circuit. The total pumping capacitance was 29 pF, and the auxiliary capacitors were set to 250 fF each – all implemented with MIMcaps.

The oscillating frequency was evaluated for I_{BIAS1} from 100 nA to 20 µA for different manufacturing corners – Figure 4-12 (a) shows simulation results only up to 14 µA because, above this value, the oscillator operation was not consistent across corners. Nonetheless, this is a limitation associated with the device's size and, thus, speed, both of which can be adjusted to increase the nominal frequency. Furthermore, faster CUC architectures can be used for even lower power consumption and delay. The results indicate a logarithmic relationship for I_{BIAS1} below 2µA which becomes more linear in the 4 µA – 14 µA range.

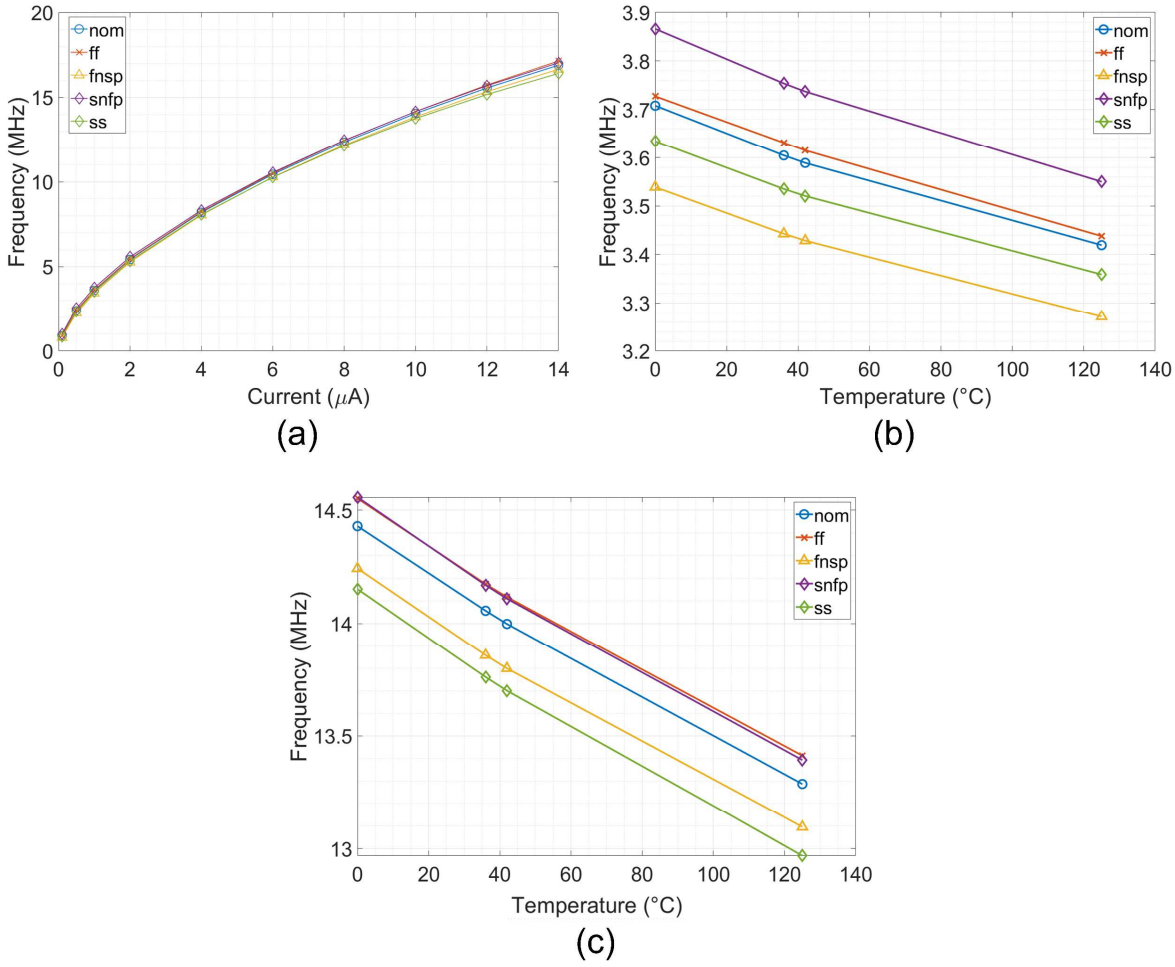

Figure 4-12. (a) Frequency dependence on I_{BIAS1} Frequency dependence across corners and temperature for: (b) I_{BIAS1} = 1μA and (c) I_{BIAS1} = 10 μA. The letters in the legend describe the corners as: 'nom' – nominal nMOS and pMOS; 'ff' – fast nMOS, fast pMOS; 'fnsp' – fast nMOS, slow pMOS; 'snfp' – slow nMOS, fast pMOS; 'ss' – slow nMOS, slow pMOS.

The absolute frequency variation increases with the increase in frequency. A closer look across corners and temperature is shown in Figure 4-12 (b) and (c), for I_{BIAS1} = 1 μA and 10μA, respectively. Relying on the fact that the slope across temperatures is the same for different corners, at 36°C, the variation is 8.66% for I_{BIAS1} = 1 μA and 4.7% for I_{BIAS1} = 10 μA. Furthermore, at 10 μA, the 'ff' corner is almost equivalent to 'snfp', indicating that the change in the nMOS does not affect the oscillation speed due to the input switching characteristics.

The CP's output voltage and efficiency at the nominal corner are shown in Figure 4-13. The average oscillating frequency was 3.6 MHz and 14 MHz for I_{BIAS1} = 1 μA, 5 μA, respectively. The results for V_{OUT} show a linear decline with an increase in I_{OUT}, and the maximum efficiency was 95% at 3.6 MHz. The results confirm that the switching scheme has no negative effects on the CP structure.

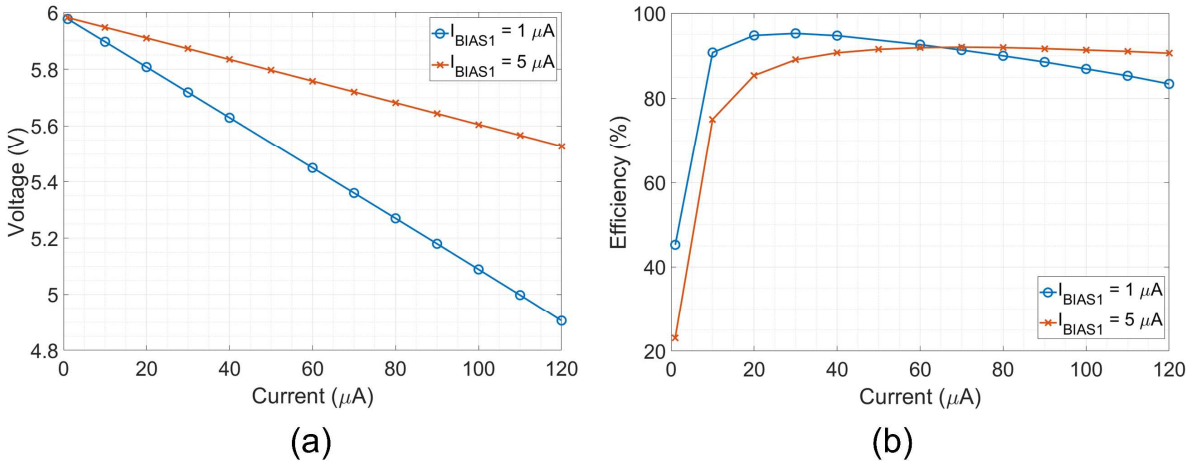

Figure 4-13. (a) Output voltage and (b) efficiency of the SO CCCP.

The power consumption of the oscillator operating at I_{BIAS1} = 1 µA, 10 µA is shown in Table 4-2. The results do not include I_{BIAS1} to represent better power contribution from the comparator and the reset circuit. A more considerable power variation exists at 1 µA rather than 10 µA bias current because of the contribution from the comparator. It is not biased at a constant current, resulting in static power consumption depending on the device manufacturing corners. At lower I_{BIAS1}, the oscillation frequency is lower, and most energy loss is due to its static current draw. When I_{BIAS1} increases, the dynamic losses associated with switching in the comparator and reset current start to dominate, reducing the relative variation of the power consumption across corners. The figure-of-merit (FOM) to describe the efficiency of the oscillator can be described as:

$$FOM = \frac{P_{TOT}}{f_{OSC}} \left(\frac{\mu W}{MHz}\right) \tag{4.6}$$

where P_{TOT} is the total power consumption of the circuit and f_{OSC} is the oscillation frequency. The FOM value in Table 4-2 is based on the power value at a specific corner and the frequency observed. At higher frequencies, FOM improves and is close to the mean of the total sweep of 9.93. This value is better than or similar to some relaxation oscillators seen in prior work [240], [242], [243]. Nonetheless, it is essential to emphasise that all relaxation oscillators incorporate

Table 4-2. Power consumption and FOM (µW/MHz) of the oscillating circuit, excluding the bias current.

	Power (µW)			FOM (µW/MHz)		
Bias current	Min	Max	Mean	Min	Max	Mean
1 µA	26.94	58.17	86.82	7.41	16.92	9.93
10 µA	81.03	132.42		5.73	9.38	

temperature and process into consideration to deliver a highly stable frequency and deliver even better results than the simple architecture proposed in this chapter at the cost of a much larger chip area [241], [256].

Furthermore, relaxation oscillators exhibit large random fluctuations in the produced output waveform due to their broadband nature (timing jitter), which can be detrimental in applications with stringent periodicity requirements. The jitter is often above 1000 parts per million (ppm), although design strategies to reach jitter of 1.5 ppm rms have been demonstrated in practise before [257]. It is dependent on the noise of active devices and the chosen architecture and is consequently proportional to the power consumption of the circuit. As the SOCP is influenced by the charging and discharging of the flying capacitors in addition to noise of the CUC and the remaining circuit, its jitter is deemed to be larger than that of a dedicated relaxation oscillator. This results in variations of the duty cycle of the CP and could affect its efficiency. However, the SOCP is designed in a closed loop system with the oscillator which ensures complete charge transfer to the output of the CP, and coupled with adequate pulse-skip or frequency regulation schemes, results in minimum loss in SOCP performance.

4.4 CONCLUSIONS

This chapter discussed a HV, high current CCCP for US and other current-intensive integrated applications with a nominal specification of 525 µA. Its operation was evaluated with hysteresis and latched comparators, resulting in 2 V and 50 mV ripple voltage at the output. The CP has been demonstrated to supply > 20 V at I_{OUT} < 500 µA at 20 MHz, to operate with large capacitive loads, and reach up to 65% efficiency with a 5 MHz clock. Nonetheless, the measurements have shown that latched comparator was functioning sub-optimally, resulting in a shortened charge transfer period and a loss in output sourcing capabilities above a 400 µA load.

A SO single-stage CCCP, based on a new CUC oscillator, was presented to generate an on-chip clock and reduce clocking energy losses and system noise. The structure allows for linear-like frequency control and is compatible with pulse-skip regulation schemes. The oscillating frequency was to supply voltage variations and did not affect the CP used in tandem with it. Frequency variations due to temperature were observed, but were minimal across intracorporeal temperature ranges, whilst corner effects could be tolerable, given the capability to compensate for them with bias current adjustments. Overall, the proposed architecture can be

used with any CP architecture, resulting in very low area and power design. It is compatible with two regulation schemes and smooths the input current, supporting its use in battery-powered devices.

5 ULTRASOUND PULSER FOR CAPSULE ENDOSCOPY

5.1 INTRODUCTION

This chapter discusses functional US electronics for use with µUS transducers operating at 28 MHz in CE applications. The contents are split into two main sections. The first section is dedicated to a pulser designed to drive a 4 x 1 mm^2 single-element transducer, while the second part discusses the design, optimisation, and performance evaluation of a pulser for array applications. Both designs aimed to produce a unipolar square wave pulse using on a floating double-nMOS output stage to achieve sub-100 µA current and transient times below 2 ns with up to 600 pF loads while delivering 8 A transient currents. Measurements of the pulser with 1.5 MHz, 3 MHz and 28 MHz arrays are presented and compared with a benchtop research US system [258].

The chapter begins with background and motivation of developing a new pulser for capsule applications, followed by the description of a USCE system operating using synthetic aperture imaging with only a single TX channel activated at a time. A simulation-based analysis of the high-frequency (HF) transducer is then discussed, and a BVD equivalent circuit model is derived. The text then delves into the explanation of the pulser's architecture and analysis of parasitic effects of a wire-bonded chip with large transient currents. An in-depth characterisation of the pulser's subcircuits is provided and results of the manufactured chip tested for power consumption, transient and frequency characterization are provided. This circuit was developed in TSMC 0.13 µm HV BCD technology.

The second part of the chapter is based on the single element pulser described in previous sections and is dedicated to the description of adapting and improving the pulser for multiple-element shared array operation. Two architectures are discussed, and a quantitative comparison is provided. The subcircuits of the array pulser are then described and a new feedback-based floating HV level shifter is introduced. This design was implemented in TSMC 0.18 µm BCD technology rather than initially used 0.13 µm technology, because of the global chip supply chain issues and lack of tape-out opportunities in the original technology as the project progressed. Consequently, the pulser was not taped out; instead its Monte Carlo and corner simulations are provided to verify its operation.

5.2 MOTIVATION

US imaging in a CE device is one of the few alternatives to WCE which can provide a more in-depth scan of the tissue in comparison to the white-light imaging approach that can only evaluate visible lesions in the GIT [144], effectively missing early-stage illnesses that do not manifest in the superficial layers and allowing assessment of penetration into deeper layers. By utilising µUS, a high-resolution image can be achieved to permit evaluation of the cellular structure of the GIT wall and allow earlier diagnosis leading to improvement in successful treatments [259].

The development of compact BCD technologies that allow for efficient integration of high and low voltage devices in the same chip and the invention of CMUTs that can be fabricated into large arrays and integrated with the driving/sensing circuitry led to a wave of newly-developed ASICs for the use in IVUS [84], [260]–[262] applications. As discussed in the Chapter 2, previous work on integrating US transducers with electronics inside a capsule has concentrated mainly on the proof-of-concept and clinical relevance of µUSCE. The devices that were developed had limited imaging capabilities and were tethered, with most electronics situated outside the capsule, emphasising the need for low-power onboard ASIC development.

At the same time, similar work in IVUS was mainly focused on deeper tissue imaging and frequencies below µUS (< 15 MHz), with more relaxed specifications in comparison to higher frequency µUS electronics. These systems also had the advantage of a tether, which facilitates HV supply and low-power data transmission. Similar designs must be significantly more power-aware in solely battery powered capsule devices whilst still meeting high-voltage generation, pulsing and sensing demands. Therefore, a standalone analysis, design and testing are required to actualise a viable battery-powered µUSCE device, which can only be achieved through a µUS dedicated ASIC.

5.3 ULTRASOUND CAPSULE ENDOSCOPE

5.3.1 System Overview – Split TX/RX

The diagram of the proposed US front-end is shown in Figure 5-1 (a): the system is split into TX and RX subcircuits. The transmit circuit incorporates a charge pump to increase the supply voltage from the 3.1 V supply to a regulated value of 20 V and a low output impedance, HV pulser for driving US transducers at 30 MHz. The receive circuitry comprises at least 128

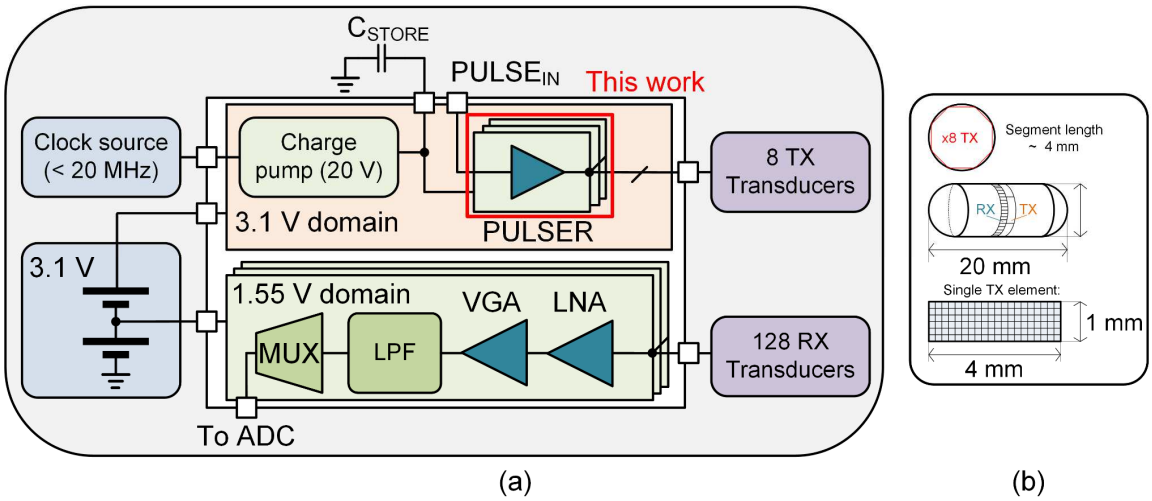

Figure 5-1. (a) Diagram of the CE US front-end. (b) Diagram of the CE device and transducer array dimensions and positioning.

low-noise amplifiers (LNAs), time-gain compensated variable gain amplifiers (TGC, VGA), low-pass filters (LPF) and a multiplexer, all of which are to be implemented in the low-voltage (1.55 V) domain. A single external capacitor C_{STORE} = 0.47 µF was used: due to high instantaneous current requirements dictated by the transducer capacitance that must be charged on every TX event, using a fully integrated CP alone was not feasible due to its limited output current sourcing capability. As a result, a very low leakage C_{STORE} was used as the charge storage device which was pre-charged by the CP in between separate TX pulses.

Two serially connected silver oxide batteries, each providing 1.55 V, are used in the design. In such a configuration, the total charge available to the system is equal to a single battery's charge, but the output voltage is doubled to 3.1 V. The factor by which the integrated CP needs to increase the voltage is then reduced by half, which leads to increased efficiency and reduced power losses associated with US transmission. Furthermore, the instantaneous current draw from the pulser is dependent on the load and can be significantly larger than the capability of the integrated CP and, thus, an external storage capacitor is required. It is important to note that the battery supply must be regulated with a drop-out of at least 100 mV, although this does not influence the HV supply, which can use the supply straight from the batteries. The bottom battery cell is drained to both the 3.1 V and 1.55 V domains and will discharge faster if the two cells are the same and thus might be sized thicker to compensate for it.

The diagram of the ideal array placement in the capsule is shown in Figure 5-1 (b). Two separate arrays are used for TX and RX. They are situated next to each other along the length of the capsule. The TX array comprises eight elements that are 4 mm in length to fit in a capsule

with a diameter of 11.6 mm, whilst the reception array comprises 128 elements placed so that an equal number of elements is dedicated for each transmitter. A separate pulser is used to drive each TX element, but as proof of concept, a single pulser channel will be considered throughout the further discussion.

Only a fraction of the transmitted US energy is returned to the receiver. Most of it is lost in the electrical to mechanical power conversion, the acoustic impedance mismatch between the transducer and the tissue, and signal attenuation in the tissue. As a result, high sensitivity and SNR sensing systems are necessary for high quality imaging. This requires a high-power pulse and a high conversion efficiency on the TX side. Whilst the former is achieved through supply voltage boosting, the latter can sometimes be done through the matching of the output electrical impedance of the pulser with the input electrical impedance of the transducer using discrete components. In a CE, space is minimal, and matching cannot be achieved; thus, a low-impedance output pulser is chosen to drive a wide range of loads. Alternatively, adaptive impedance matching techniques with on-chip-only components exist but are only practical for high-frequency RF applications where small component values are enough [263].

Another challenge is the power consumption of the overall system. Transducers operating at 30 MHz require an ADC with > 120 Msps sampling rate to satisfy typical over-sampling requirements. To obtain an image depth of 10 mm and assuming at least a 10-bit resolution with a 128-element array operating at 1 fps, approximately 1 Mb of data is generated every second. A base limit of 4 fps would increase it to 4 Mbps, exceeding the data limits of state-of-the-art commercial WCEs discussed in Chapter 2. This system would not achieve prolonged operation, so synthetic aperture imaging is required [264]. It allows for operating only a fraction of TX channels, significantly reducing the average power consumption. The concept was initially presented by Holly et al. [265] and, even when the capsule moves due to peristalsis in the GIT and errors are introduced due to the capsule displacement, was shown to be theoretically viable. The detailed timing diagram of a single frame with a 30 µs single channel acquisition period is shown in Figure 5-2. The ADC is started first to allow for it to settle before the data is received. A broadband pulse is sent on the first of the eight TX elements, and the first RX element is enabled to capture the data. This process repeats until 32 RX elements are used in the vicinity of the TX element. Afterwards, the second TX element starts to transmit, and the whole process repeats until signals from all 128 RX elements are captured.

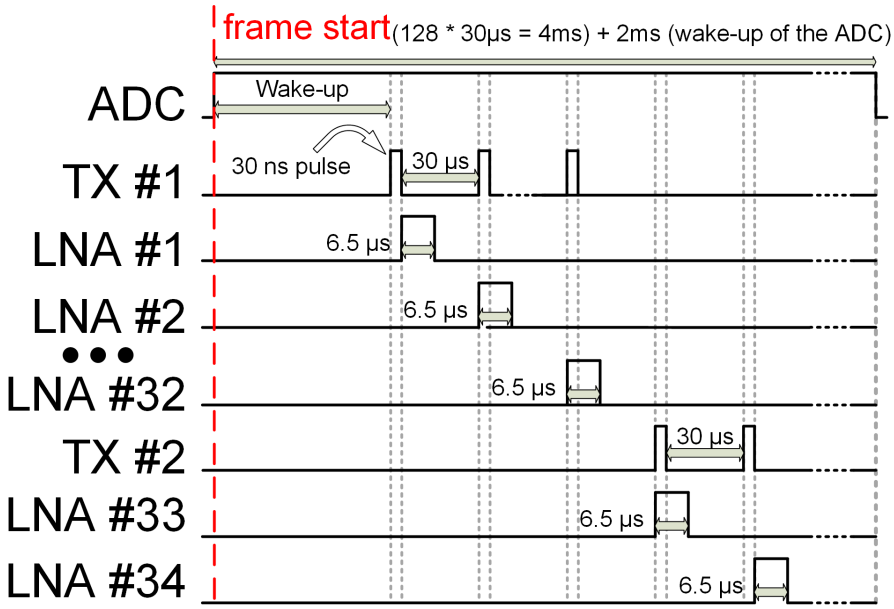

Figure 5-2. Timing diagram of the US AFE of the first 34 elements.

The exact minimum period between individual pulses is not set but rather depends on the current capabilities of the charge pump and average current requirements of driving a specific transducer, so there is a need to estimate the transducer characteristics. The ADC considered in this work was based on widely available commercial ADC chips operating with a 1.8 V supply and dissipating approximately 100 mW of power when active. This contributed to the need of the two serially-connected batteries to generate the 3.1 V supply, which could then be down-regulated to the required ADC supply voltage. Whilst, alternatively, an additional switched-inductor boost converter could be used to generate the 1.8 V from the 1.55 V battery, it was dismissed due to space limitations of the CE.

Nonetheless, it is important to note that the commercial ADCs that were available during this work do not accurately reflect the general state-of-the-art of ADC devices or their future trends. An accurate prediction of future ADCs can be made using the yearly ADC survey compiled by B. Murmann [266]. Based on the historical data up to year 2022, it can be established that many 10-bit and 12-bit ADC architectures have been proposed over the years for operating below 1.55 V, with some designs operating with power consumption below the milliwatt range. These results are overwhelmingly better than currently available commercial devices and identify the potential of improving the system architecture and the power consumption of future µUSCE devices.

5.3.2 Transducer Specification and Mode of Operation

Using finite element analysis (FEA) and an optimisation algorithm developed by Moldovan [267], a composite transducer (Figure 5-3 (a); image taken from [268]), measuring 1 x 4 mm^2 with a resonant frequency of 28 MHz was created and simulated in free space using

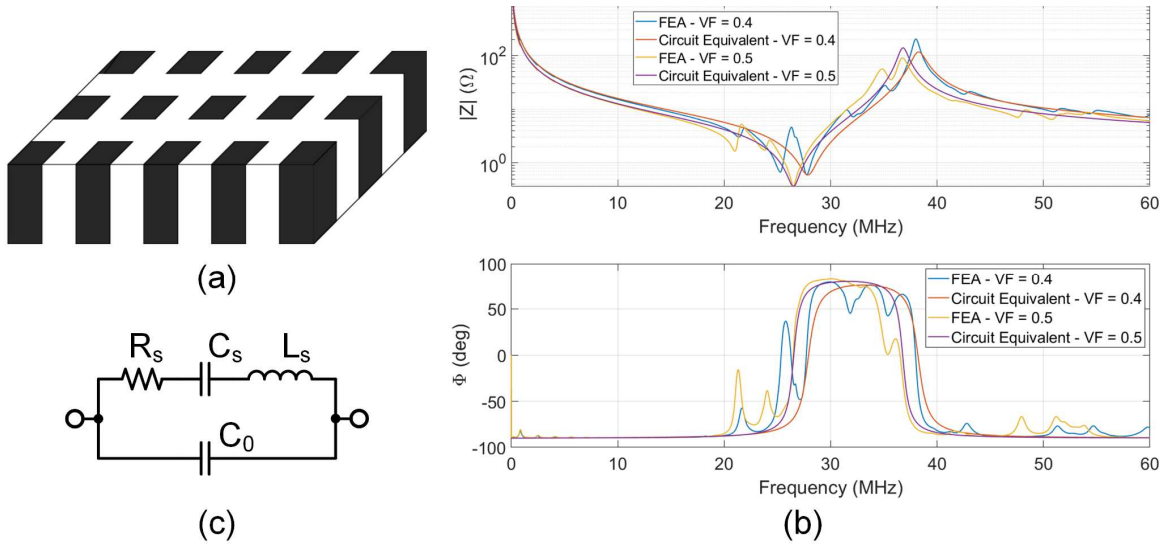

Figure 5-3. (a) Composite transducer. (b) Simulation results of the input impedance of the FEA and equivalent BVD circuit. (c) BVD circuit model.

OnScale FEA software [269]. The ratio between the width of pillars (black space) and gaps (white space) is defined as volume fraction (VF). The designer determines its value to achieve the highest efficiency at the resonant frequency whilst mitigating other modes of operation. As only software modelling was available and transducer optimisation and manufacturing were not in the scope of the study, two different volume fraction transducers (VF = 0.4 and VF = 0.5, referred to as VF04 and VF05) were simulated.

The impedance versus frequency data, Figure 5-3 (b) was used to derive an equivalent BVD circuit model of the transducer, Figure 5-3 (c) [270]. Capacitor C_0 defines the charge required to drive the transducer, whilst the series resonant circuit (R_S, C_S, L_S) defines the frequency response of the transducer. The model has a limitation: it can only describe the transducer's behaviour close to one specific resonance. An expanded model is required for a more accurate derivation [271]. The FEA and equivalent circuit frequency response results are shown in Figure 5-3 (b). The simulations show that the resultant transducer resonance was below the specification: VF05 version resulted in a resonance frequency of 26.5 MHz, while VF04 had two significant local minimums at 27.8 MHz and 25.3 MHz.

Based on theory, a composite transducer has only a single resonance, determined by the transducer's thickness. Other local minima are generated by spurious or lateral resonances, negatively affecting the overall efficiency and introducing additional noise to the system [272]. Practically, further investigation would be required to optimise the transducer, but this was not in the scope of the project and, thus, was not investigated further. Furthermore, VF04 had a significantly more uneven response with additional modes across the whole sweep range. Overall, however, the BVD circuits' response matched the FEA simulations sufficiently, and the model was deemed appropriate for further use as the first-order estimation for evaluating power requirements. The resultant values are shown in Table 5-1. VF05 has a 17% larger C_0 than VF04, and it was used as the primary model for circuit simulations.

The BVD model was employed as a load for an ultrasound pulser in an analogue circuit simulation, and both its average and peak currents were measured (Table 5-1). At the same time, the pulser's output stage sizing requirements were obtained. The values were based on the pulser operating at a 33 kHz PRF (T = 30 µs) with less than 3 ns rising/falling time (RFT), each pulse entailing only a single square wave period. This resulted in a single charge-discharge cycle of a transmit pulse. The average current required to excite the transducer was 700 µA. The resultant value was then scaled down to 25 kHz PRF to reduce the current specification and used together with a 20 V output voltage as the specification for the high-current CP, discussed previously in Chapter 4.

Table 5-1. BVD model components values and measured currents.

Transducer VF	**C_0 (pF)**	**C_S (pF)**	**R_S (Ω)**	**L_S (nH)**	**Average current (µA)**	**Peak current (A)**
0.5	607	561	0.36	64.2	700	6
0.4	500	440	0.59	74	800	5.7

5.3.3 Pulser Subsystem

Ultrasound imaging systems are based on sending an US pulse into the tissue and forming the image from the echo signals that return to the sensor. In generic low-voltage CMOS technology, HV pulsing is achieved through device stacking [273], but it results in limited transient capabilities, which degrade the further the supply voltage exceeds the nominal technology voltage. Furthermore, the stacked devices require additional biasing circuits, leading to dynamic and static losses. In such cases HV BCD technologies are mainly used [27]–[31].

For compact integration and optimised efficiency, ASICs are developed that encompass both the transmitting and HV-isolated receiving circuits near the transducers to reduce parasitic effects and energy losses associated with them.

The pulse in an ultrasound system is usually generated in a unipolar or bipolar fashion. The former has the advantage of reduced switch count and area and is easier to implement in single-supply systems (e.g. battery). On the other hand, the latter can be used with return-to-zero switching to reduce dynamic losses [33], [34], but it also requires an additional negative HV supply rail, which incurs additional power and chip area losses. In any USCE, a second charge pump would be needed to generate the negative supply rail, effectively doubling the power loss. Nonetheless, a unipolar pulse can also be adapted to behave in a step fashion to improve the power efficiency of the pulser without affecting the quality of the transmitted wave [278].

In this US analogue front-end (AFE), an internal charge pump provides a single 20 V rail and, thus, a unipolar pulser is provided. There are two primary configurations of the output stage, depending on whether the high-side (HS) switch is a HVpMOS, Figure 5-4 (a), or an HVnMOS, Figure 5-4 (b), device. The former option is the most widely used, as it allows for simple control by generating a lower gate voltage than $V_{DDHV.}$ This can be achieved with a single resistor and an HVnMOS but leads to an extended current draw from V_{DDHV} when enabled. Generating an additional rail (V_{DDHV} - 5.5 V) [279] or using a capacitive level shifter [280] is also possible, but these solutions lead to continuous power consumption and increased area requirements. Alternatively, a high-side (HS) nMOS in a bootstrapped switch (BSW) configuration can be used [274]. The circuit requires a floating level-shifter and a capacitor, C_{BOOT}, which bootstraps the HS switch relatively to the output potential. The size of C_{BOOT} must

be made large enough to power the level shifter and drive the switch whilst charging the stray capacitances associated with the bootstrapped node.

The main drawback of the pMOS version over the nMOS one is the area of the switch. The HVpMOS in most technologies can be up to three times larger than the HVnMOS for the same resistance, which was also the case for the TSMC 0.13 µm, based on simulation results [281]. In US applications where RFTs are particularly important, this directly corresponds to a large HS switch area. Furthermore, the occupied area is proportional to an increase in the gate capacitance of the switch, leading to higher energy losses in both static and dynamic level

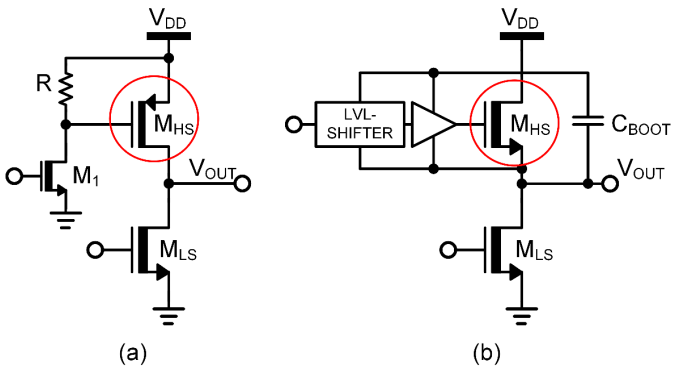

Figure 5-4. Output stage: (a) High-side pMOS. (b) High-side nMOS.

shifters. As a result, the double HVnMOS driver is the most advantageous choice in a unipolar application, leading to the minimum silicon area as well as dynamic-only energy loss, the majority of which is from the 5.5 V supply; the current draw from V_{DDHV} in this implementation is determined only by the transducer load, parasitic effects, and the leakage current of the output stage.

The schematic of the proposed pulser is shown in Figure 5-5. The circuit has three supply inputs: 3.1 V is supplied by the two series batteries, and both 6 V and 20 V are generated by an on-chip charge pump. Although the pulser's instantaneous current is large, with a limited PRF and an external storage capacitor, C_{STORE}, the charge pump is able to meet the current demands of the pulser. On start-up, the CP is not operational: to ensure the correct state of the high-voltage level shifters, a supply switch is used to allow for 3.1 V input to supply V_{BOOT} and the low-side (LS) buffer nodes, setting the correct initial state of the circuit. Furthermore, a MOScap, C_1, is used to smooth current requirements in the (LS) gate buffer. In an 8-channel implementation, only a single channel would be transmitting at any time, which allows for a

single capacitor to be shared among elements. As will be shown in Section 5.3.8, in a four-metal layer process, C_1 can be entirely placed under C_{BOOT}, incurring no additional area penalty.

Commonly, the HV isolation block, Figure 5-5, is a single diode that allows current to flow into V_{BOOT} and power the HV level-shifter and buffer before potential increases in node V_{OUT} and the bootstrapping are initiated. However, if the charge consumed by the two components is lower than $Q_{TH} = C_{BOOT} \cdot V_{TH}$, it is more beneficial to eliminate V_{TH}, improving

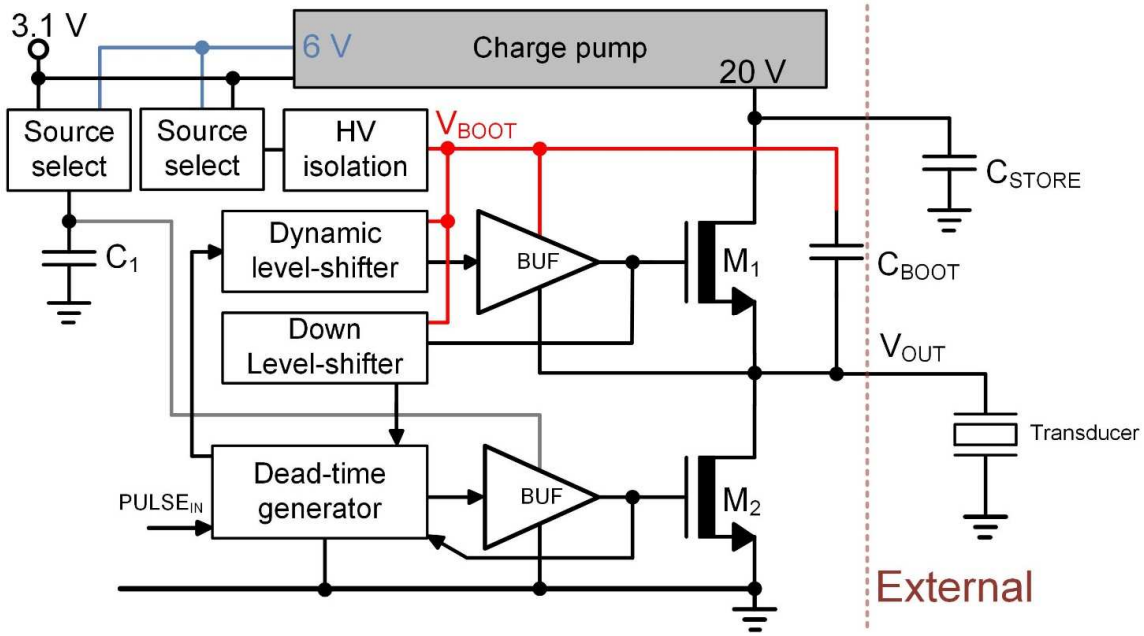

Figure 5-5. Proposed pulser diagram.

the charge retained in V_{BOOT}. Here C_{BOOT} is the bootstrap capacitance, V_{TH} is the diode voltage drop, and Q_{TH} is the additional charge stored in C_{BOOT} by eliminating V_{TH}. Due to the large area of M_1, this was observed to be the case, and a bootstrapped switch was used.

The pulser uses a non-overlapping clock generator to ensure the break-before-make operation of switches M_1 and M_2. The clock uses the gate voltage of M_2 and a down level-shifter from the gate of M_1 as feedback signals. As a result, additional delays are introduced, dependent on the propagation time in both the buffers and up/down level-shifters. Such an implementation ensures a short-circuit condition is always prevented but, as discussed in Section 5.3.5, it can lead to limitations on the minimum pulse width.

5.3.4 Parasitic Effects and Current Evaluation

Simulation results of the instantaneous current of the US pulser showed currents up to 6 A due to high load capacitance and low R_{ON} of the output stage. A gold bond-wire process

was used to connect the chip to a carrier package. The parasitic values of a bondwire connecting a chip to a package are generally small and can be neglected under low frequency or low current conditions. However, high currents can exacerbate the effect of a parasitic inductance (L_{PARA}) and cause power dissipation issues or even lead to bond-wire melting if the current is too high due to path contact resistance (R_{PARA}). It has been shown that L_{PARA} can be analytically evaluated as [282]:

$$L = \frac{\mu_0}{2\pi} * l \left[\ln\left(\frac{l}{r} + \sqrt{1 + \frac{l^2}{r^2}} \right) - \sqrt{1 + \frac{l^2}{r^2}} + \frac{l}{r} + \frac{1}{4} \right] \quad (5.1)$$

where μ_0 is permeability of free space ($4\pi * 10^{-7}$ H/m), l is bondwire length and r is bondwire radius. If l >> r, the formula can be simplified to:

$$L = \frac{\mu_0}{2\pi} * l \left[\ln\left(\frac{2l}{r} \right) - 0.75 \right] \quad (5.2)$$

The radius and length of the bondwire were 33 µm and 3.5 mm respectively, and resulted in L_{PARA} = 3.23 nH; the resistance of a single bondwire was ~70 mΩ whilst its fuse current was rated at 1 A. The width was based on the available bondwire type [283], and the length was derived from the chip size and packaging geometry.

To eliminate the unknown variables of different chip packages, it was decided to wire-bond the chip straight to the test PCB and reduce the parasitic effects of PCB tracks by ensuring a minimum distance from the point of contact of the bondwire to the transducer connector. A minimum impedance model of a PCB microstrip can be analytically described by formulas described in the IPC-2141 standard [284] and discussed elsewhere [285]:

$$Z = \frac{87}{\sqrt{\varepsilon_r + 1.41}} \ln\left(\frac{5.98H}{0.8W + T} \right) \quad (5.3)$$

$$C = \frac{0.67(\varepsilon_r + 1.41)}{\ln\left(\frac{5.98H}{0.8W + T} \right)} \ (in\ pF/in.) \quad (5.4)$$

$$L = 5.071 \ln\left(\frac{5.98H}{0.8W + T} \right) (in\ nH/in.) \quad (5.5)$$

where ε_r is relative permittivity, W is microstrip width, H is the distance between the strip and ground/ power plane, T is the thickness of the strip and 1 inch = 25.4 mm.

However, this model is limited in accuracy [286], and due to the logarithmic component, it can only be used when 0.1 < W/L < 3. The technology used here had ε_r = 3.9, H = 125 µm and T = 43 µm, resulting in ≈ 0.15 nH/mm (3.8 nH/in) for W = 250 µm. As the PCB tracks can be made much wider to reduce the inductance, their contribution to the total L_{PARA} can be neglected. Consequently, the pulser was simulated with parasitic elements representing one, eight and no bond-pads connected to supply, ground, and output nodes. The output stage of the pulser was simulated with a 20 mm wide HVnMOS and a BVD equivalent circuit of a 1 x 4 mm^2 transducer with VF = 0.5 (higher total capacitance). The circuit was excited by a half-period of 30 MHz square pulse equal to 16.7 ns and a 2 ns RFT. The simulated circuit is shown in Figure 5-6 (a). Although the estimated bondwire resistance was only 70 mΩ, a 1 Ω resistor was used in simulations to take on-chip track, contact of bondwires and PCB track resistances into account as the worst-case scenario. The transient results, Figure 5-6 (b), show that with only resistive component the output voltage remains below 20 V and the current remains below 6 A. When inductance due to bondwires is introduced, the maximum output voltage increases, and an overshoot can be observed. The worst response was seen at lower inductance values that led to ≈ 8.58 A instantaneous current and maximum voltage of 23.6 V. The maximum current in this case is above the sum of the 1 A fuse current limit of eight bondwires and could result in a

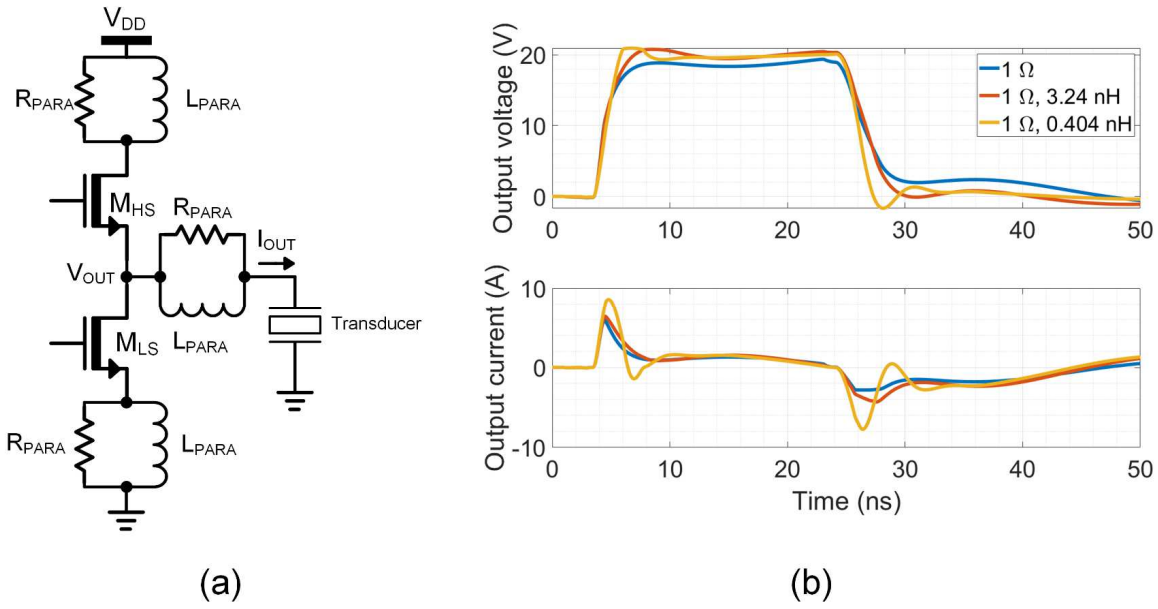

Figure 5-6. (a) Circuit for parasitic simulations. (b) Transient simulation results of the transducer input.

thermal failure. It can be concluded that the L_{PARA} component should be eliminated or chosen

based on the load to reduce voltage and current increase at the output node and ensure operational compliance limits.

5.3.5 High-voltage Level-shifters

The three primary loss sources in the bootstrap node of a pulser are the charging of the HS switch gate, HV level-shifters and stray capacitances in the floating circuit. The latter cannot be avoided and mainly depend on the layout and size of the design, whilst charge loss of the HS gate is determined by the size of the output stage, in turn dependent on the rise time of the output pulse. Consequently, the power reduction can only be achieved with the minimisation of losses in the level-shifters, which also leads to a reduction in the size of C_{BOOT}.

The lowest power consumption can be achieved by a capacitive level-shifterm, Figure 5-7, that utilises HV MOMcaps to separate the bootstrapped node from the LV node, eliminating any current draw from the former to the latter. In particular, a 4.1 pJ per switching cycle and 1.45 ns propagation time design, Figure 5-7 (a), was implemented and tested as the choice with the lowest energy loss [287]. The shifter operated well in ideal circumstances with a capacitive load that exhibited square wave behaviour. However, simulations with the BVD model of the transducer and parasitic elements resulted in oscillations and undefined behaviour, making it unusable in US applications where different transducer loads are possible.

Three state-of-the-art alternatives were then investigated. The “fast” mode design, Figure 5-7 (b) is based on the general symmetrical CC topology, which provides high reliability due to a single stable state defined by V_{IN} [288]. The design includes four HV devices and two high capacitance nodes due to their drain terminals that must be charged/discharged every transition, leading to sub-optimal propagation time and power consumption. Alternatively, a fast low-power level shifter was proposed by T. Lehman, Figure 5-7 (c) [289]. The circuit includes only two HVnMOS to isolate the LV side and uses a pulse to trigger the signal conversion. The drawback of the design is the requirement of careful layout to prevent a latch-up through the LV nMOS if their source is pulled below V_{SSH}. Alternatively, a biasing circuit ($V_{BIAS} > V_{SSH} + V_{TH\text{-}N}$) can be used instead of V_{SSH} at the gate of M_3/M_4 but that would incur energy losses from the V_{BOOT} node.

As a result, a current-mode pulsed level-shifter was chosen, Figure 5-7 (d) [290]. The design includes only a single pair of pulse-triggered HVnMOS, leading to low power

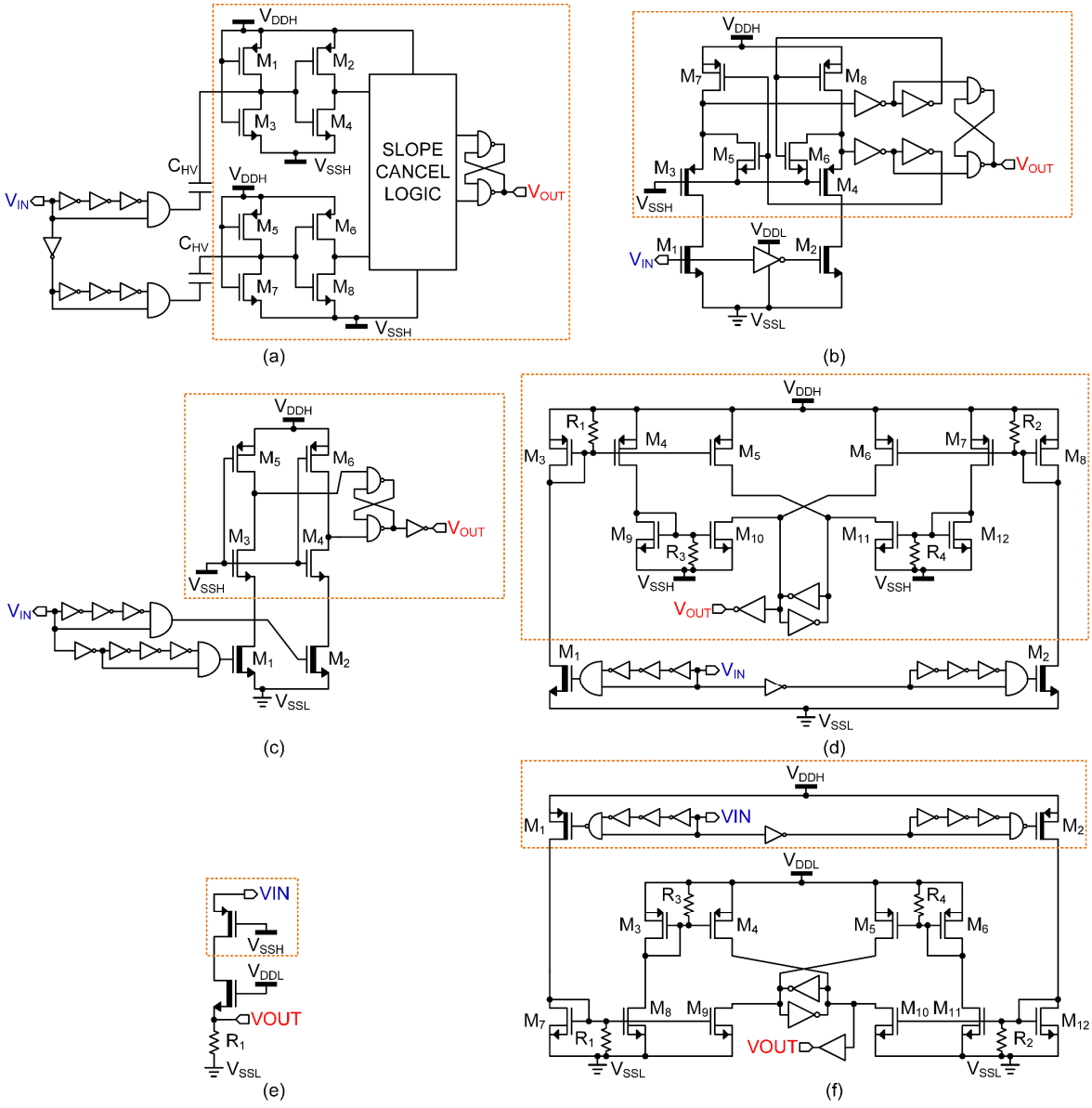

Figure 5-7. (a) Capacitive level-shifter. (b) "Fast" mode level-shifter. (c) Low-power level-shifter. (d) Pulsed current level-shifter. (e) Simple H2L level shifter. (e) Inverted pulsed H2L current level-shifter.

consumption. Furthermore, the symmetrical current mirror topology ensures that any stray current induced by oscillations in the output V_{DDH} is equally sourced to both inputs of the L_1 latch, preventing switching into an erroneous state. Finally, this arrangement is robust under high slew rate conditions required for high-frequency transducers and can be adapted to operate as a H2L level-shifter.

The H2L level-shifter was implemented to prevent a catastrophic failure that can occur if both output switches of the pulser are enabled at the same time. The same functionality can

be achieved by carefully considering LS and HS propagation delays, but it cannot be guaranteed without feedback. The most straightforward H2L feedback is shown in Figure 5-7 (e). It operates as a static level-shifter while the input is "high" and thus, leads to a high current draw if low propagation time is required. For this reason, the pulsed L2H level-shifter, Figure 5-7 (f), was adapted to provide the same functionality for H2L conversion whilst maintaining all the topology benefits.

5.3.6 Supply Switch

The pulser has a single stable supply of 3.1 V, while the 6 V and 20 V supplies are generated by a charge pump which is not operational during POR. To ensure that the pulser enters the correct state (determined by the latch of the HV level-shifter), a supply switch with hysteresis was used to initially supply the V_{BOOT} node using V_{3V} = 3.1 V. The simplest circuit with such functionality is formed with two CC pMOS as shown in Figure 5-8 (a), but it lacks continuity. Assuming a constant V_{3V} and V_{TH-P} is the pMOS threshold voltage, when $V_{CP} > (V_{3V} - V_{TH-2})$, M_2 reduces conduction and becomes fully disabled when $V_{CP} = V_{3V}$; only after $V_{CP} > (V_{3V} + V_{TH-1})$, M_1 becomes enabled. To maintain continuity, a supply switch with hysteresis was implemented, Figure 5-8 (b) [291]. The design was tapered to satisfy the current requirements of the V_{BOOT} node, and an additional POR switch was added to facilitate the operation of the switch on start-up regardless of I_{BIAS}. As shown in the transient simulation, that implementation allows the output to follow input voltages with minimal delay and V_{OUT} deviation, Figure 5-8 (c).

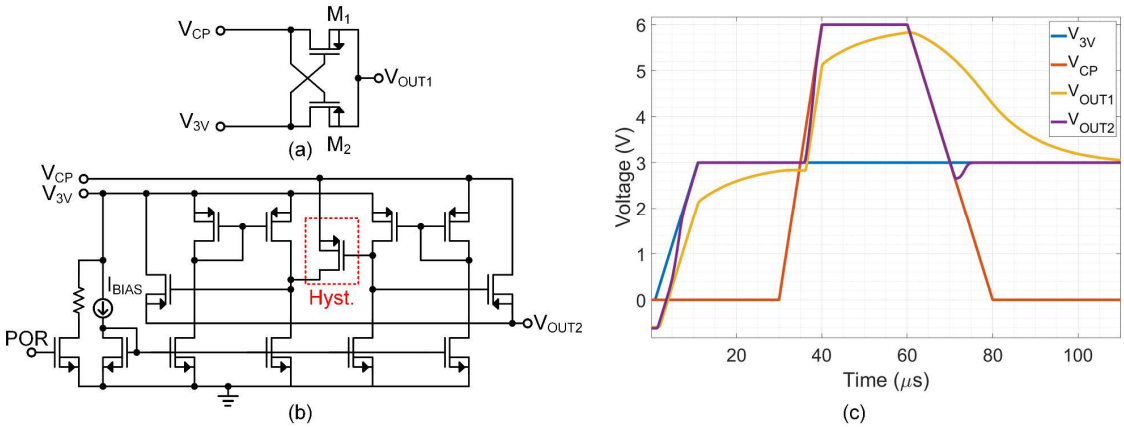

Figure 5-8. (a) Simple cross-coupled switch. (b) Switch with hysteresis. (c) Transient comparison of the simple and hysteresis switches.

5.3.7 Non-overlapping Clock Generator and Slowed Slope Buffer

The instantaneous current of the pulser's output stage was observed to be up to 8.6 A. To improve circuit reliability in case higher currents are generated, a way to limit RFTs was needed whilst still maintaining the slope time under 5 ns. By limiting the turn-on time of the output stage, a more gradual increase in the current can be generated. The functionality was achieved by adding a narrow M_{N2}, Figure 5-9, which is turned on before the main pull-up transistor, M_{P1}, and slowly begins to charge the gate during the time a feedback signal takes to travel from V_X through AN1 and B2 (under a nanosecond).

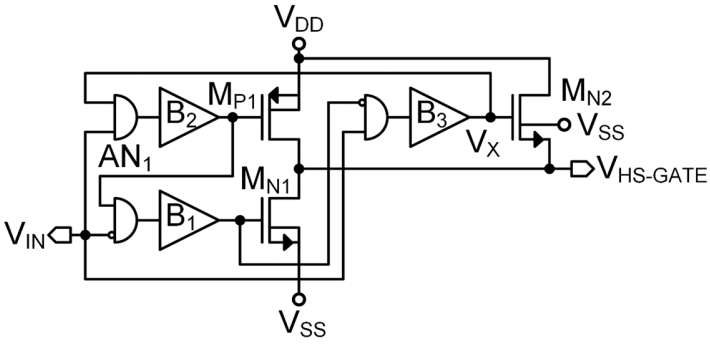

Figure 5-9. Schematic design of the output stage gate driver

5.3.8 Results

The layout view and macrograph are shown in Figure 5-10 (a) and (b). The total chip area was 3 x 3 mm^2 and the pulser occupied an area of 1280 x 750 μm^2, most of which was taken by the bootstrap capacitor and output nMOS, measuring 20 mm each to meet RFT requirements for high-capacitance loads. Eight bondwires were used to connect high-voltage supply, ground, and output nodes each; the lowest resistivity top-metal and AP layers were used for in-chip routing.

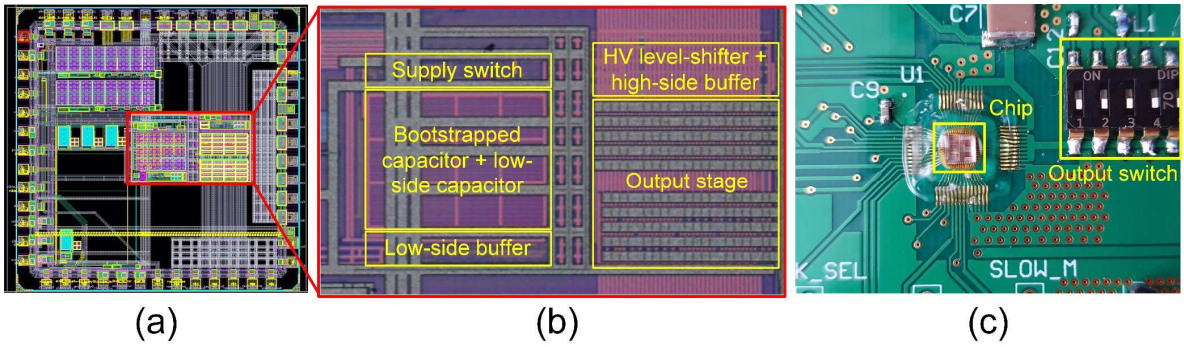

Figure 5-10. (a) Layout view of the manufactured chip. (b) Macrograph of the manufactured pulser. (c) Chip location on a test PCB.

The manufactured chip was wire-bonded directly to a test PCB, Figure 5-10 (c). Initially, a switch was included at the output of the pulser to allow testing with varying transducer connectors (SMA and jumper wires). Tests have shown that the stray capacitance at the output strongly influences ringing in the node and leads to higher overshoot voltages. As a result, the output track was manually disconnected, and only a single jumper connector was soldered to the available PCB track. A high-voltage and extremely low leakage (200 pA) capacitor was used at the V_{DDHV} supply of the pulser to measure leakage during the off-state accurately.

5.3.8.1 Transient: 1.5 MHz and 3 MHz Arrays

The pulser was initially tested with two 1.5 MHz and 3 MHz ultrasonic arrays manufactured by Moldovan et al. [267]. Measurements were performed with one, three and seven elements connected in parallel. An additional measurement with a 600-pF load was also performed, representing the 4 x 1 mm^2 VF05 transducer load discussed in Section 5.3.2. The transient response is shown in Figure 5-11 (a). Evaluation of the rise and fall times shows that the pulser achieved an edge time < 3 ns for all loads with the highest value of 2.4 ns for the 600 pF capacitor. Propagation times of the rising and falling edges were 14 ns and 12 ns respectively. Overshoot and undervoltage were observed at the output, measuring up to 9 V, and were most prominent with a purely capacitive load. Due to the bootstrap mechanism, this would result in approximately (20 V + 9 V + 4.5 V = 33.5 V), but based on simulation results, this variation is not seen internally within the chip, preceding the bondwires of the output node, and should remain within safe operating limits. Nonetheless, a transient current of 13 A was

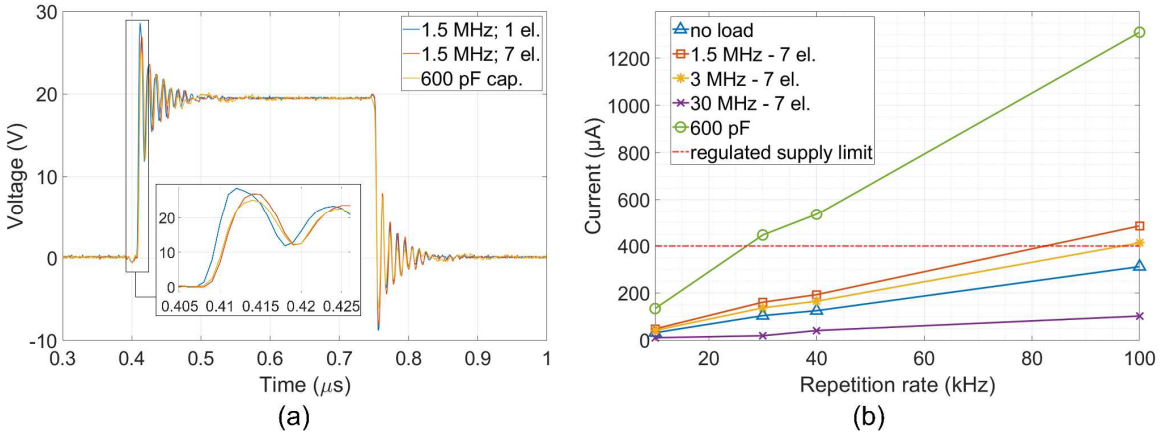

Figure 5-11. (a) Transient measurement results of a 1.5 MHz array one and 7 elements in parallel, and a capacitive load. (b) Output current consumption vs repetition rate.

measured when driving a capacitive load, which is 62.5% higher than observed in simulations and has the potential to degrade the reliability of the bondwires in the test setup.

The pulser's input currents were measured for its three input supplies (3.1 V, 6 V, 20 V) when operating at a PRF between 100 kHz and 10 kHz. The test was carried out with the pulser set to send a single pulse at a 100 kHz repetition rate; the current consumptions were independent of the pulse width and measured 1.21 µA and 95 µA from 3.1 V and 6 V power supplies, respectively. The output leakage from the 20 V supply was only 70 nA on average. HV current draw was also measured with different loads, taking parasitic capacitances of the PCB into consideration, and subtracting them from the result. The resultant current consumption for 1.5 MHz, 3 MHz and 30 MHz is shown in Figure 5-11 (b). The red line at 400 µA defines the maximum average current at which the integrated CP (Chapter 4) can generate a regulated 20 V output, even if the input voltage drops from 3.1 V to 2.8 V. Based on the results, the maximum theoretical capacitive load could be powered from a HV CP with PRF < 26 kHz.

5.3.8.2 Pulse-Echo: 30 MHz Array

The pulser was tested with a 30 MHz transducer array in a pulse-echo setup. This experiment comprised two tests and had seven elements used, as shown in Figure 5-12: the central element was used for receiving and three elements on the left and right sides were used for transmission. In the first test, a Verasonics® Vantage™ Research Ultrasound System (VVRUS) was used to transmit a bipolar 20 V_{pp} at the transducer resonant frequency of 28 MHz. The received echo was saved on the VVRUS and oscilloscope. In the second test, a 20 V_{PP} unipolar pulse was generated using the proposed pulser. In both tests, the receiving array element was connected to the VVRUS and an oscilloscope probe to maintain consistent

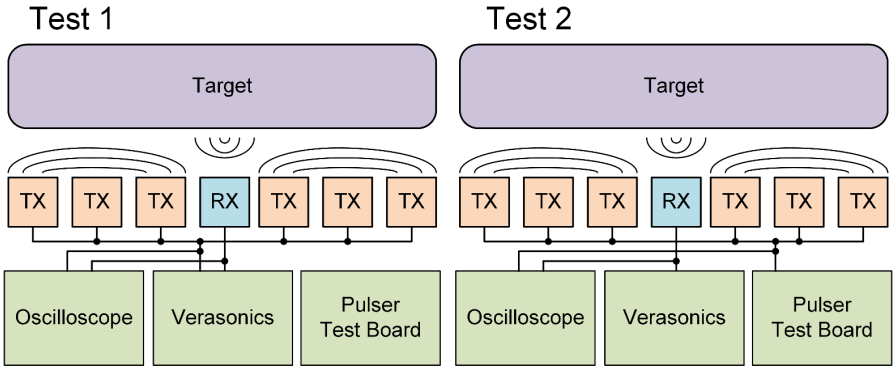

Figure 5-12. Experimental setup; transmitting (TX) and receiving (RX) element configuration.

experimental conditions between tests. The pulser was controlled by an arbitrary waveform generator outputting a 5 V pulse with a 5 ns edge time. In both tests, the transducer was immersed in a purified water container with a quartz reflector target, and the echo signal was recorded. The pulser was tested with a 20 V benchtop supply and the HV CCCP (Chapter 4).

The non-normalised transient result of the transmitted pulse is shown in Figure 5-13 (a). The pulser output deviated from the expected square wave and was more similar to a triangular pulse as a result of the 5 ns edge time limit of the pulse generator and propagation times in the pulser itself. The plot also shows that -7.5 V was reached on the falling edge due to parasitic elements within the pulser's output interface. A variation can be observed in the VVRUS output as well, which resulted in a wavelet pulse lower than 20 V_{PP}. The use of a CP resulted in a marginal drop in the pulse amplitude, compared to a benchtop supply. The returning echo of the

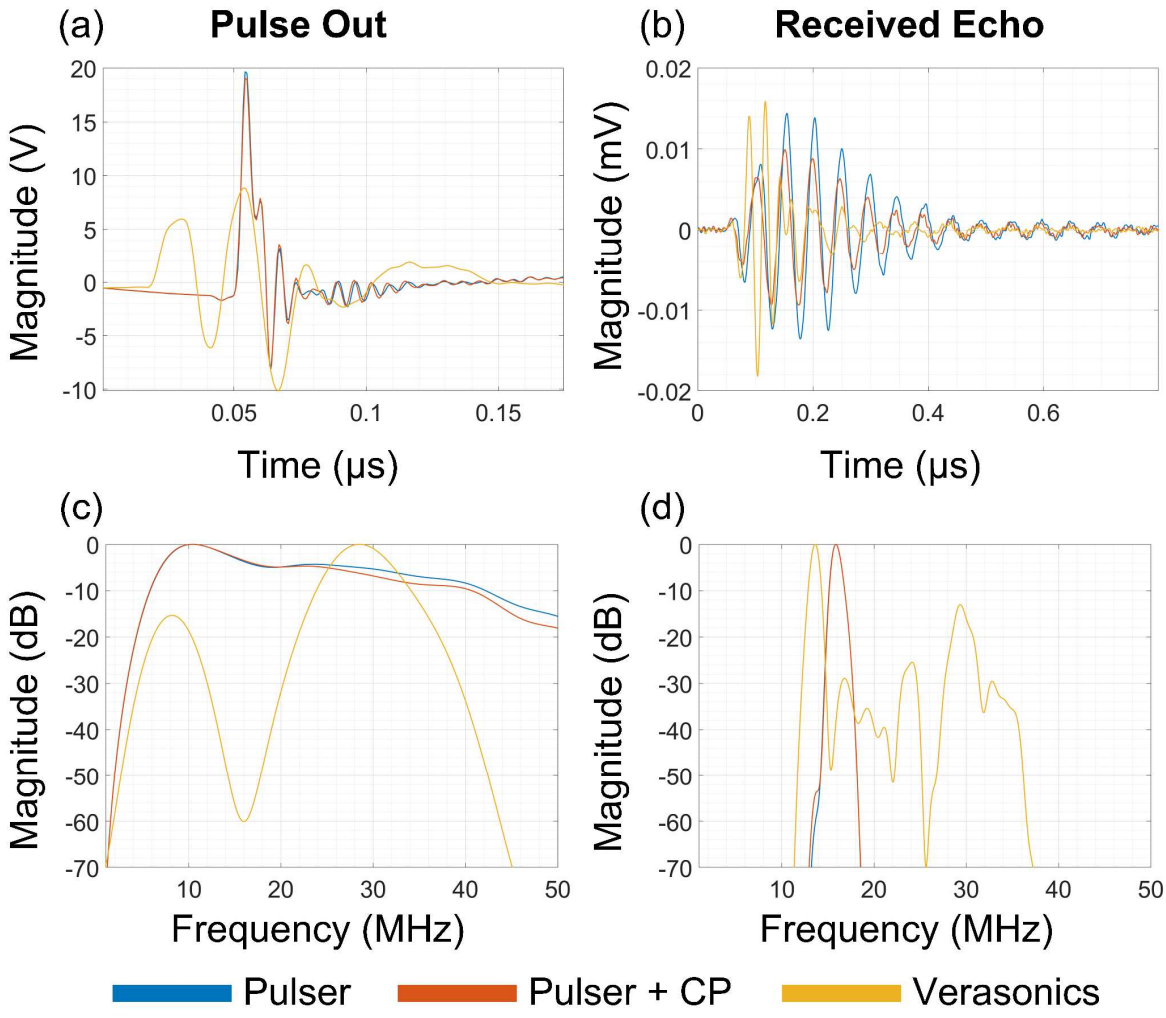

Figure 5-13. (a) Transient output pulse comparison. (b) Non-normalised transient of the received echo. (c) Frequency response of the output pulse. (d) Frequency response of the received echo.

two pulsing systems is shown in Figure 5-13 (b). The amplitude of the echo generated by the fully-integrated pulser was 18% lower than VVRUS echo and 43% lower when a CP was used. Such amplitude loss could lead to an equivalent loss in imaging depth but could be tolerated with a higher SNR in the RX.

The frequency spectra of the echo signals from the three setups were compared and are shown in Figure 5-13 (c) and (d). It can be observed that the VVRUS pulser excited transducer elements at their natural resonance at around 28 MHz, although an additional peak below 10 MHz was present as well, Figure 5-13 (c). At the same time, the pulser exhibited a flat response across the frequency range. The maximum transmitted power was at approximately 10 MHz, with a -4.9 dB drop at 19 MHz. The magnitude then remained flat up to 24 MHz and started to roll off afterwards, reaching -7.3 dB at the 36.4 MHz upper bandwidth limit. The behaviour of the CP-powered pulser was equivalent up to 20 MHz, but decreased faster, reaching -8.8 dB at the upper BW limit. The echo frequency response is shown in Figure 5-13 (d). The pulser achieved an almost identical low BW response, peaking at 16 MHz for the two supply variations. Simultaneously, the VVRUS results showed maximum power at 13.6 MHz and a secondary peak at the 28 MHz array resonance.

Based on the echo results, the proposed pulser could not excite the array at the required 28 MHz frequency. However, its echo response region overlapped with the VVRUS BW region with the highest power component. This indicates that a large portion of the output pulse echo was directed towards lower frequency components, formed due to large parasitic elements in the test setup interconnects. Nonetheless, the pulser allowed generation of short, high-frequency, HV pulses and a wide BW. The CP-powered version demonstrated reduced performance which can indicate larger current requirements or the need for larger supply storage capacitors to mitigate high-transient current effects on the pulse amplitude.

5.3.8.3 Output Impedance

The main drawback of the integrated pulser is its bootstrap capacitor, C_{BOOT}, which connects to the output node even when the low-side and high-side switches are turned-off. The top plate of C_{BOOT} connects to a significant parasitic capacitance associated with the bootstrapped node and acts as a low impedance path to ground for AC signals. The pulser's output impedance in a shut-down state is depicted in Figure 5-14, showing that it remains below 100 Ω up to 50 MHz and below 500 Ω up to 100 MHz. In applications where a single transducer

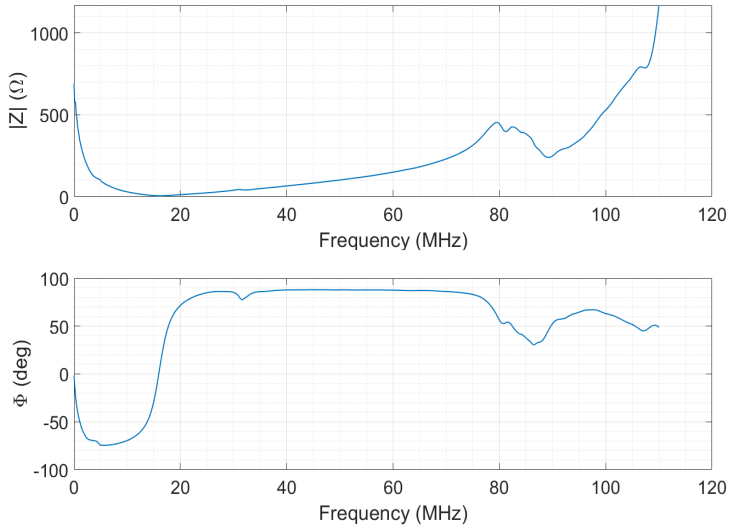

Figure 5-14. Measured magnitude (top) and phase (bottom) of the pulser's output impedance.

array is used for both TX and RX, such low impedance values would effectively ground the returning echo signals leading to an imaging failure. For this reason, in shared array applications, additional bootstrap circuitry is required between C_{BOOT} and the transducer input to allow for full isolation of the TX circuitry during reception.

5.3.9 Single-element Pulser - Summary

The pulser developed in this work achieved the specification of driving loads up to 600 pF with < 5 ns RFTs. The measurements showed that the maximum instantaneous current was 13 A and no damage throughout the testing of the pulser was observed. The pulser's average current consumption was only 96 µA, most of which can be attributed to charging the large gate capacitance of the output stage switch, the size of which is determined solely by the load and RFT specification. Evidently, the power consumption and area can both be reduced even further for lower frequency and load requirements.

A comparison between the proposed circuit and the state-of-the-art is shown in Table 5-2. The pulser achieves the fastest signal propagation time and fastest RFTs for the highest output load reported in the literature. It also achieves the lowest continuous average power consumption of 173.9 mW per channel. For a clear comparison, average power consumption of 100% duty cycle was used, with the power value of each publication derived based on this reported PRF, burst number and pulse frequency. The pulser had a significantly larger total area, which was determined by the bootstrap capacitor and output stage dimensions needed to achieve

the RFT specification. The output stage was also identified as the main contributor to the power consumption. Hence, reducing its size by eliminating bond-wire parasitic effects and PCB interconnects would result in even lower power consumption per channel.

The main drawback of the pulser circuit in question is the capacitive loading effect associated with the bootstrap capacitor, which presents a low-impedance port at its output and prevents the transducer to be used with array elements shared by both transmission and reception. As a result, additional functionality, enabling isolating the bootstrap node from the array elements, is required. This functionality is further discussed in Section 5.4.

Table 5-2. Comparison of integrated ultrasound pulsers.

Reference	This Work (2021)	[292] 2021	[260] 2020	[293] 2019	[212] 2016	[273] 2014
Pulse Shape	2-level unipolar	3-level unipolar	3-level bipolar	3-level bipolar	2-level unipolar	Unipolar
Input Voltage (V)	3.1, 6	3.3 V	1.8, 5.5	5	1.8	1.1
Output Voltage (V)	20	60	±60	±70	32	15
Transducer Frequency (MHz)	30	5	9	5	3.2	2.6
Input-output Delay (ns)	14/12	-	6.3	-	28	30.8
Rise/Fall Time (ns)	2.4	-	-	10.6/ 10.5	-	57/30
Output Load	600 pF	10 pF	18 pF	100 pF// 1 kΩ	80 pF	12 pF
Power Consumption (mW)	173.9	263.4	571.7	610	-	-
Chip Area (mm^2)	0.96	0.2	0.167	0.024	2	0.15
Technology	0.13 µm HV BCD	0.13 µm HV BCD	0.18 µm HV BCD	0.18 µm HV CMOS	0.18 µm HV BCD	0.18 µm CMOS

5.4 PULSER FOR ARRAY CONTROL

The single element pulser, presented in Section 5.3.1, was designed for a system with separate TX and RX arrays. Such an implementation can be helpful in applications where there are fewer TX than RX elements or they are separated for other reasons, such as to exploit difference transducer characteristics. For example, some piezoelectric materials, such as polyvinylidene fluoride (PVDF), can be used to produce high-sensitivity receivers but are not suitable for transmission [294], thus, different materials and manufacturing process are required for the TX array.

Conversely, separating RX and TX circuits leads to alignment variations due to manufacturing errors. This can be avoided by advanced manufacturing techniques such as stacked transducers [295] or utilisation of the same array for both TX and RX – a viable solution for piezoceramic, CMUT and PMUT applications. For single array operation, the pulser must be adapted to drive smaller loads, eliminate its capacitive output impedance element (full-isolation) and have low delay variability between individual transmission channels.

This section discusses a low-power pulser circuit for shared-array operation. Two system implementations are presented and power optimisation, based on the load and rise time requirements, is presented to define the most suitable solution. Furthermore, a new HV feedback level-shifter is presented that simultaneously achieves a sub-nanosecond low-to-high (L2H) transition delay and a high-to-low (H2L) conversion with lower power consumption and statistically better propagation time. A new control scheme and a new non-overlapping clock generator are presented. Finally, simulation results are presented to validate the performance of the designs in question.

The diagram of an analogue-front-end of an μUSCE device using a shared array is shown in Figure 5-15 (a), and the position of the arrays in the capsule is shown in Figure 5-15 (b). The system is divided into two subcircuits: HV, which comprises pulser elements and a charge pump, and LV, composed of the signal amplification and filtering circuits (LNA, VGA and channel multiplexer). Additionally, a pulse generator circuit was included on-chip to solve the issue of signal propagation delays that limit minimum HV pulse width. The LV domain includes registers for choosing TX and RX elements and analogue and digital delay components for defining pulse width and the time between the TX and RX phases of operation.

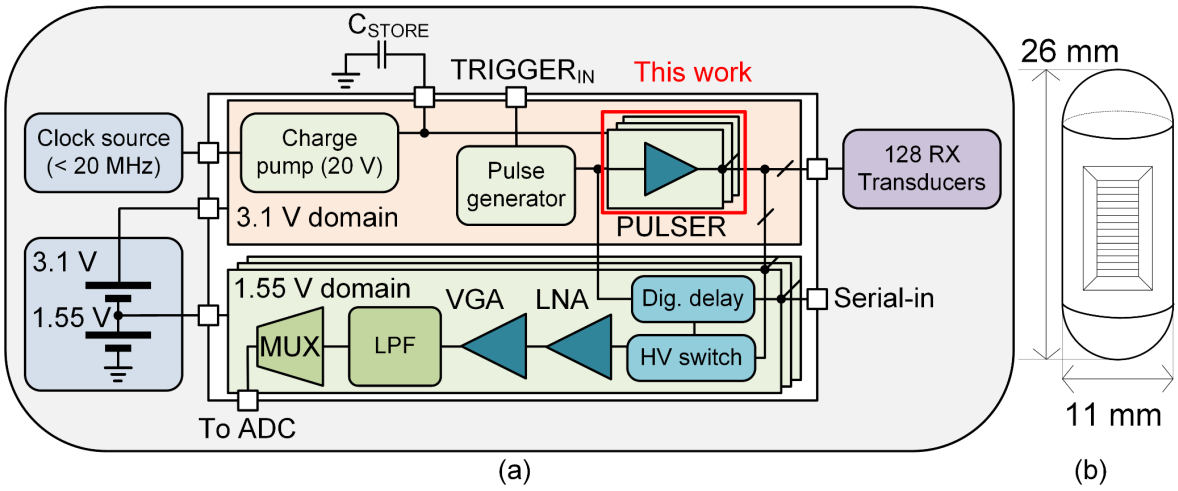

Figure 5-15. US analogue front-end for shared array CE device: (a) System diagram. (b) Array position.

5.4.1 Technology

The technology of the system presented in this section is different from the single-element design (Section 5.3.1). Due to the global chip shortage, the previously used TSMC 0.13 µm BCD process was no longer available for manufacture. A decision was made to shift to TSMC 0.18 µm BCD process at this stage of the project. Apart from the larger feature size, this technology has an increased voltage limit from 1.5 V to 1.8 V for low-voltage devices, which is less optimal for the CE device operating with 1.55 V batteries. Furthermore, in comparison to the previous Section 5.3, the nominal voltage of the pulser was reduced from 3.1 V to 3 V to take the potential voltage drop due to the limited output impedance of the battery into consideration.

5.4.2 Pulser Array System

Only a single additional output BSW is required per channel to isolate C_{BOOT} from the output, but two architectural choices exist to drive each BSW, depending on whether a single pulser per channel is used, *arch-A*, Figure 5-16 (a), or if a number of channels are actuated as a group, *arch-B*, Figure 5-16 (b). The two architectures can be explained by separating the pulser into the main switch, Block X, and the bootstrapped switch, Block Y, Figure 5-17. The first architecture, *arch-A*, is based on every array element using a pulser block with an additional BSW situated between C_{B1} and the element, and Block X being optimized for the minimum area that is required to achieve a single channel driving specification. The advantage of this implementation is that only a single additional HV switch, Block Y, is needed for each channel, therefore, the "on" output resistance and associated parasitic capacitances are minimised. A dedicated single element pulser also means that the power consumption of each block is

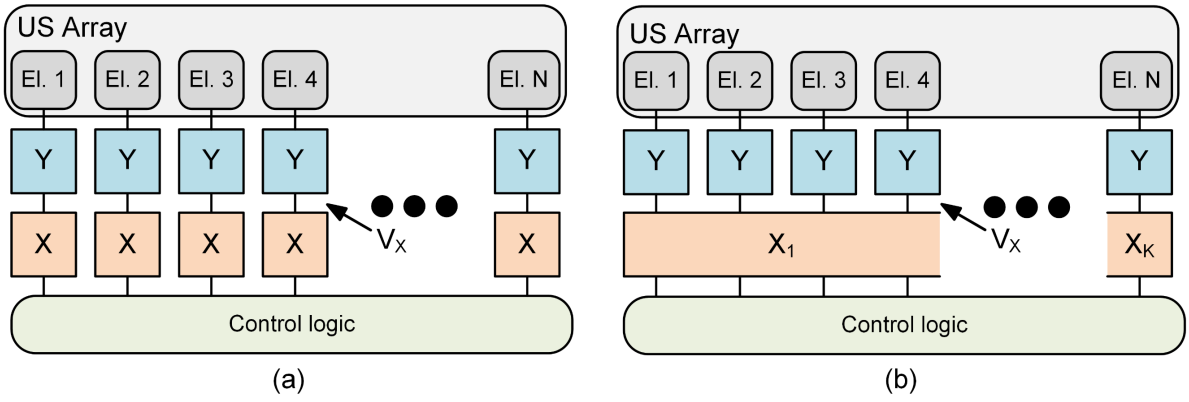

Figure 5-16. (a) Architecture A, arch-A. (b) Architecture B, arch-B. For detailed views of X and Y refer to Figure 5-17.

independent of neighbouring pulser blocks which can be beneficial if only a sub-group of channels is active at a time. The disadvantage of the system is that a dedicated non-overlapping signal generator and an HV level-shifter are required for each channel, leading to an increase in power consumption from the 5.5 V node and introducing timing mismatches between individual channels.

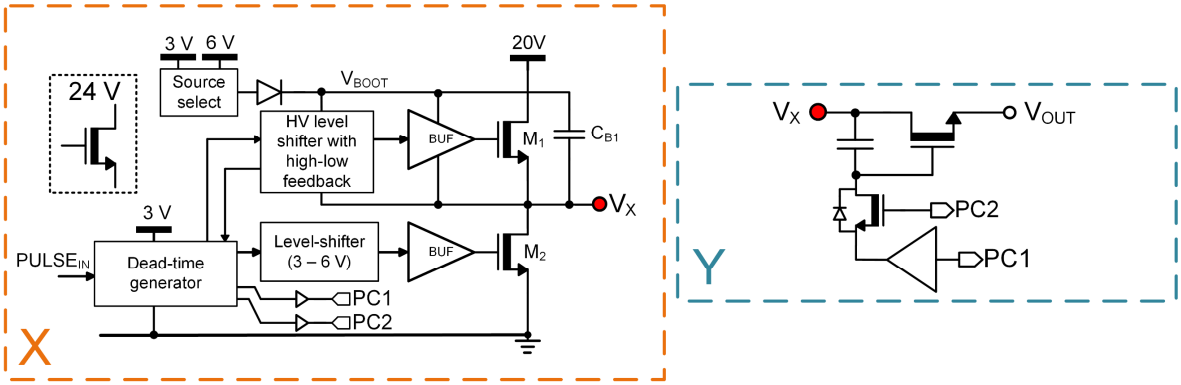

Figure 5-17. Blocks: (X) Core of the bootstrapped pulser. (Y) BSW with a single-side isolation.

The second option, *arch-B,* is to have a large initial stage pulser that generates a shared V_{DDHV} pulse per block of BSW, with Blocks Y controlling elements that are enabled. The number of Blocks Y used per single Block X is determined by the designer and application. In essence, *arch-B* with a single Block X (k =1) is an implementation that is used in some AFEs with strict area constraints, where pulse is generated by an external HV generator X_1 and only Blocks Y are included on the chip. In *arch-B* both M_1 and M_2 in Block A are scaled based on the number of channels connected to a single Block X. Such a system has only a single HV level-shifter and a non-overlapping clock generator per group, which results in simultaneous activation of all enabled channels within it; a timing mismatch exists only between separate blocks. The disadvantage of this architecture comes from all the Blocks Y being connected to V_X that must be charged for every TX event, regardless of the number of elements used.

The two architectures have advantages and disadvantages that stem from the different number of components used. Although the power consumption of each architecture scales linearly with the frequency of operation and the number of elements employed, it is not evident which has lower power consumption. Therefore, an analysis was performed to approximate the power consumption of each architecture by evaluating stray capacitances and power consumption of *arch-A* and *arch-B* designed for a specific capacitive load. The charge loss and

device scaling values are presented in Table 5-3 and are based on the values extracted from circuit simulations.

Table 5-3. Parameter values used for optimisation.

Coefficient of rise/fall time increase with adding serial HVnMOS in comparison to a single HVnMOS for each architecture:		Unit length:	10 µm
		HVnMOS capacitance per unit length (F):	
Name	Scaling factor		
b	1.07 - 1.26	C_{ggu}	16 f
		C_{ddu}	8.4 f
Charge consumption of each component in a single pulse cycle			
Name	Symbol	Charge (C)	
HV level-shifter - 3 V	$Q_{HV\text{-}3V}$	2.04 p	
HV level-shifter - V_{BOOT}	$Q_{HV\text{-}VB}$	24.22 p	
LV level-shifter (1.5 V -> 3 V)	Q_{LV}	0.381 p	
Non-overlapping clock gen.	Q_{clock}	0.477 p	

The charge requirements for Block Y included gate capacitance C_{gg} and drain capacitance C_{dd} as the two major contributors to the power consumption. The resistance of a path from the supply/ground to the load was evaluated for a single and two HVnMOS in series. A scaling factor *b* was then defined as the value to which the width of each HV transistor in series must be increased to maintain the same resistance as a single HVnMOS. This allowed extracting parameters from a single switch and capacitor setup and use them to extrapolate to *arch-A* and *arch-B*. It is important to note that the scaling factor *b* is dependent on both the number of devices in series and their orientation. When the current path includes a source-to-drain direction, the body diode of the HV transistor contributes to the conduction and the effective resistance is reduced. As each TX event involves both charging and discharging the transducer, the higher scaling factor was used to ensure both RFTs meet the specification.

The power consumption of each component in the pulser is fully dynamic and can be expressed as:

$$P = V_{DD} * Q * f \tag{5.6}$$

where V_{DD} is the supply voltage, Q is the charge lost on every clock transition, and f is the operating frequency. The total power consumption of each architecture is then equal to the sum of power consumption of individual components, plus the charge lost in charging the gates and

drains of all BSW switches. The principle is different in *arch-B* because the power consumption is non-uniform in time and is dependent on the number of elements in the Block X (k) and the number of Blocks Y used for TX at the same time (n), resulting in two blocks being driven at once for a fraction of the total time. The relationship between operating a single and two Blocks X in *arch-B* can be described as:

$$p_{double} = \frac{n-1}{k_x - (n-1)} \tag{5.7}$$

$$p_{single} = \frac{k_x - 2(n-1)}{k_x - (n-1)} \tag{5.8}$$

where $k_X = 2k$, and p_{double} and p_{single} are the proportions of the time that the circuit is activating one and two Blocks X. Equations (5.7) and (5.8) are valid for solutions where $n < k$. Otherwise, multiple blocks are operating simultaneously, converging to *arch-A*. By taking these values into consideration, the power consumption from V_{DDHV} (output driving voltage) and V_{DD5V} (pulser supply voltage) due to stray capacitances and charging of the BSW gates (in both Blocks X and Y) for *arch-A* and *arch-B* can be expressed as:

$$P_{HV-A} = (V_{DDHV}^2 * C_{paraA} * f)(h_A - 1) * n \tag{5.9}$$

$$P_{BSW-A} = (V_{DD5V}^2 * C_{ggA} * f) * h_A * n \tag{5.10}$$

$$P_{HV-B} = (V_{DDHV}^2 * C_{paraB} * f)\left[k * p_{single} + 3k * p_{double} + (h_B - 1) * n\right] \tag{5.11}$$

$$P_{BSW-B} = (V_{DD5V}^2 * C_{ggB} * f)\left[k * p_{single} + 3k * p_{double} + (h_B - 1) * n\right] \tag{5.12}$$

$$C_{ggx} = C_{ggu} * \frac{w_d}{w_u} * b_x;\ C_{parax} = C_{ddu} * \frac{w_d}{w_u} * b_x, \qquad x \in [A, B] \tag{5.13}$$

where $P_{HV\text{-}A}$ and $P_{HV\text{-}B}$ are power losses due to C_{parax}, $P_{BSW\text{-}A}$ and $P_{BSW\text{-}B}$ is power required to charge bootstrapped HVnMOS, C_{ggx} is the scaled drain and gate capacitance of each architecture, h_x (= 2) is the number of series HVnMOS with $x = A, B$ for *arch-A* or *arch-B,* w_u = 10 µm and w_d is the width of the HVnMOS needed to achieve the desired RFTs in a single HVnMOS implementation (single Block X).

The two architectures were compared for PRF of 25 kHz, n = 5 and different k values, and it was observed that under all circumstances power consumption due to parasitic capacitances dominates the overall power consumption. The resultant plots (k = 10) against output voltage and HVnMOS device width are shown in Figure 5-18. It can be observed that *arch-A* is superior in total power consumption under all conditions, even with lower parasitic capacitance values used in this evaluation. The highest power consumption was attributed to

charging C_{PARA} of the output node, which increases as a square of V_{DDHV}, overwhelming other power loss sources. It can be concluded that, for low-power applications with integrated HV supplies, *arch-A* is the optimal solution.

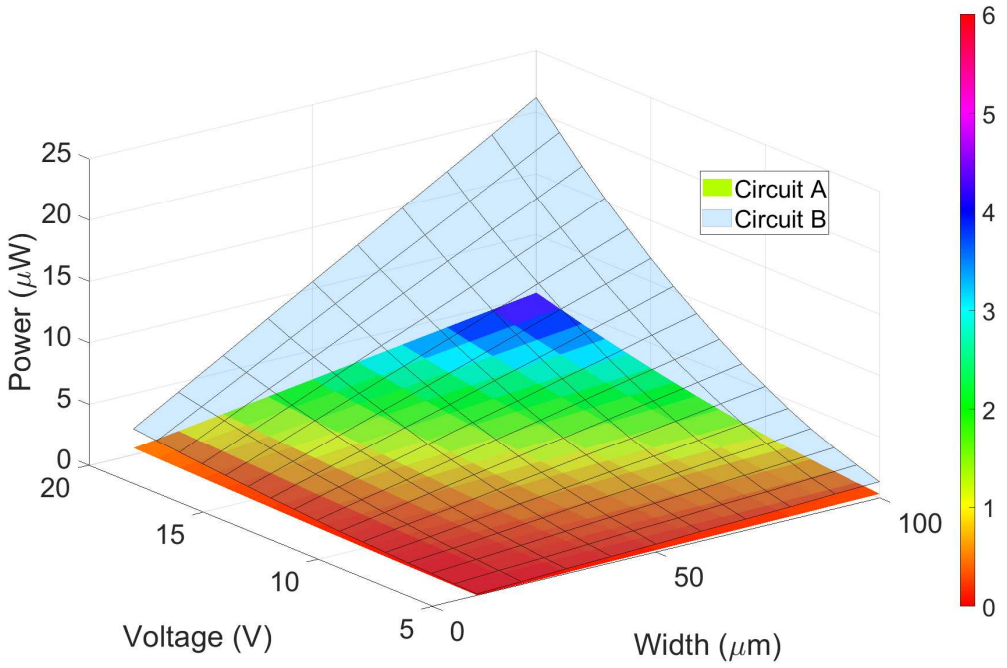

Figure 5-18. Total power consumption of architectures A and B.
The colour bar on the right indicates power consumption levels of architecture A.

The secondary concern with channels operating in individual clock feedback loops is their propagation time differences. Due to process variation, the propagation characteristics will vary between channels, with the biggest difference between the first and the 128th element. However, in the proposed CE application, only seven array elements are triggered simultaneously. It can also be assumed that the process variation would affect all elements similarly. As a result, a mismatch Monte Carlo (MC) simulation of 500 runs at 36°C and 1.35 V, 3 V and 6 V supply voltages were carried out at nominal, 'ss' and 'ff' corners to estimate the variation in propagation time Δt_d between individual pulser elements. Assuming a sine excitation pulse of equivalent amplitude with a phase shift only, the difference between two neighbouring elements was evaluated to be 2% at Δt_d = 220 ps, resulting in high reliability in activating multiple elements in parallel without significant output pulse pressure loss.

Based on the reduced temperature range required for biomedical applications (35 - 42°C), a MC analysis for all active device process corners was carried out at a nominal temperature of 36°C. The MC results of the nominal propagation time and charge loss from the V_{BOOT} node are shown in Figure 5-19 (a) and (b), and the summary of the complete corner MC results is shown in Table 5-4. Although the rise time was affected more due to the feedback from the HS node, the maximum propagation delay was only 5.85 ns, and the highest power consumption was P_{5V} = 7.43 µA, P_{3V} = 0.62 µA per single channel at a 100 kHz repetition rate. Repeated measurements with different pulse widths also confirmed the pulser's capability to produce short (< 16 ns) output pulses at the slowest propagation time. It is important to note that the process variation would also influence the propagation time between the chips and within the same ASIC, albeit this variation would be gradual. The difference would be increasingly prominent with more channels activated simultaneously, but experimental tests are needed to evaluate its effects practically.

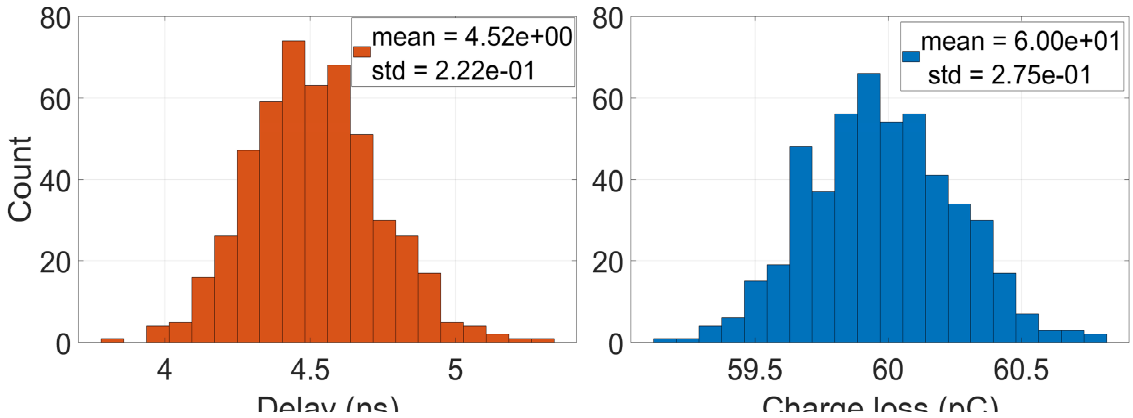

Figure 5-19. Pulser's nominal MC results: (a) in-out delay; (b) Charge loss from VBOOT.

Table 5-4. Summary of the corner MC simulations.

Edge propagation time (ns)	**Min**	**Max**	**Mean**	**Standard dev.**
Rising edge	2.95	5.201	3.988	0.917
Falling edge	3.562	5.854	4.637	0.935
Charge loss (pC)				
V_{BOOT} = 6 V	55.9	74.34	63.41	7.865
V_{DD} = 3 V	5.129	6.217	5.64	0.432

5.4.3 Final Pulser Architecture

The full diagram of the pulser based on *arch-A* is shown in Figure 5-20 (a). The pulser has two supplies of 3 V from two serially-connected 1.55 V batteries and a maximum 6 V supply from an integrated CP. A source switch is used to power the pulser node V_X during the POR, while the output of the CP is below the supply. Furthermore, a 3 V supply is used to power the non-overlapping clock, although a lower voltage of 1.55 V could also be used. This choice was found to lead to lower propagation delays and time variations and result in an easier layout

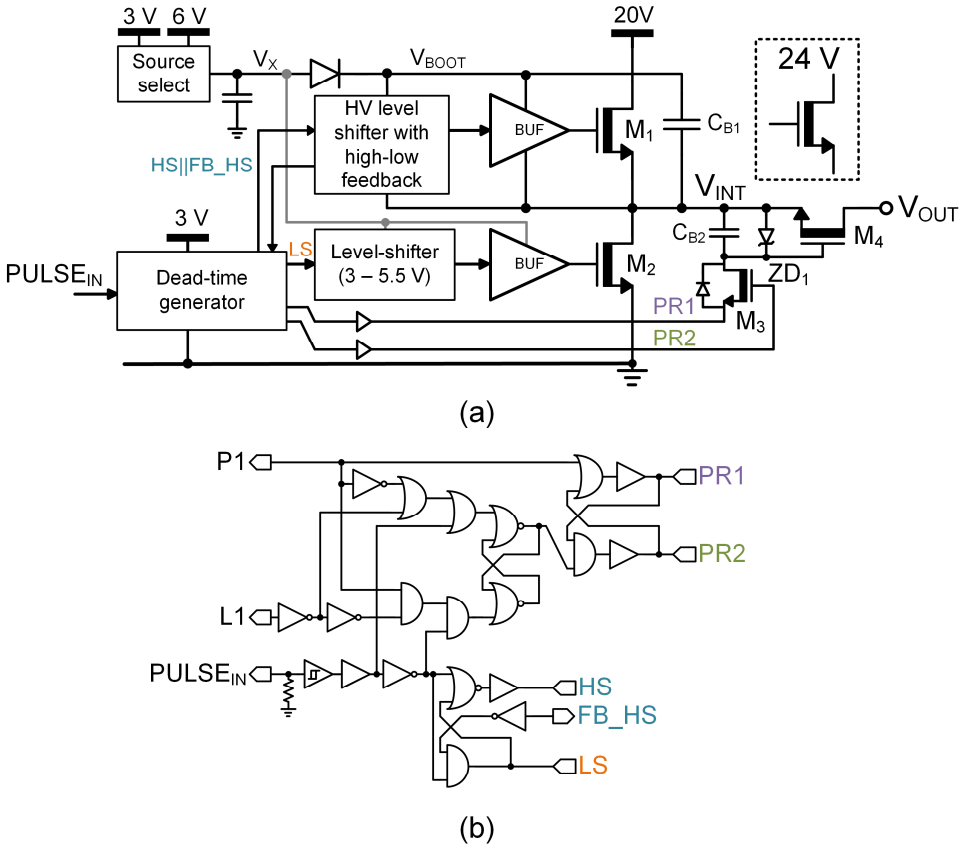

Figure 5-20. (a) Pulser diagram (single element). (b) Dead-time generator.

implementation due to the reduced number of supply rails and level-shifters. The 3-to-5.5 V level shifter was based on the work by Kabirpour and Jalali [296] while the HV level-shifter was a new implementation of a pulsed level shifter discussed in Section 5.3.5. An additional BSW, comprising switches $M_{3\text{-}4}$, a Zener diode, ZD_1, and a bootstrap capacitor, C_{B2}, was included to isolate V_{OUT} from V_{INT}. Switch M_3 is used to pre-charge the gate of M_4 which is then bootstrapped to node V_{INT} with the help of C_{B2}. The capacitor C_{B2} in this case could be significantly smaller than C_{B1} as the gate of M_4 is pre-charged from the supply prior to the output

operation. In this case C_2 had to be just large enough to compensate for parasitic capacitances associated with V_{G4}. The Zener diode is included to limit $V_{GS} < 6$ V.

The pulser's control circuit is shown in Figure 5-20 (b). The pulser requires a control scheme that allows for $M_{2\text{-}4}$ to be disabled before M_1 is enabled. Furthermore, $M_{3\text{-}4}$ has to be maintained "on" (PR1 = 5.5 V) longer than the desired pulse duration to allow for V_{OUT} to be discharged before being disconnected from the transducer. Signals P_1 and L_1 are from an external array control block and are followed by a non-overlapping clock to control $M_{3\text{-}4}$ whilst ensuring $V_{GS} = 5.5$ V during the discharge of the M_4 gate. $PULSE_{IN}$ is also used as a trigger to disable M3 automatically even if L1 remains high to prevent erroneous operation. Finally, the LS output is shorted to feedback instead of using the gate voltage of M_2, to reduce the rising edge propagation time from $PULSE_{IN}$ to V_{OUT}.

5.4.4 High-voltage Latched Level-shifter

The current mirror-based floating level-shifter presented in Section 5.3.5 has proven functional and low-power, with a high output slew rate, producing high-frequency oscillations at the output node. The flipped topology was also used for H2L signal conversion to generate a feedback path to the dead-time generator. To eliminate the need for set-delay elements in the two L2H and H2L level-shifters and improve its robustness across manufacturing corners, a new fully feedback level-shifter was explored for the use in the shared-array pulser Figure 5-21. The L2H circuit was based on the design by Liu et al. [47] but, instead of the predefined pulse duration, a feedback mechanism was used as the end condition of the pulse using a H2L level-shifting circuit, preventing the potential for failure in the pulse generating circuits. All non-HV devices in the circuit are 5.5 V.

The proposed circuit can be explained by describing a rising edge propagation ($V_{IN} = V_{SSL} >> V_{DDL}$). At the initial state, $V_{IN} = 0$, $V_{OUT} = 0$, $Q = 1$ ($\overline{Q} = 0$), $\overline{S} = 1, \overline{R} = 1$. When V_{IN} goes high, M_1 is enabled, and current flows through M_{19}; it is then copied into V_2 and out of V_1, setting the latch LA1, $V_{OUT} = 1$ and turning on M_{14}. The current flows through M_{12} and is then copied through the current mirror $M_{6\text{-}7}$, pulling V_{RST} low and setting $Q = 0$, which, in turn, disables M_1 and M_{12}. At this point, node V_4 goes into a high-impedance mode, and $V_3 = V_{DDH}$ begins to discharge through the newly enabled M_9. This current flows through M_2 and would be large enough to pull V_{SET} low and re-enable M_1, leading to oscillations. Additional current is also induced by the capacitive coupling through M_{13} by the rising of V_{DDH}. To prevent

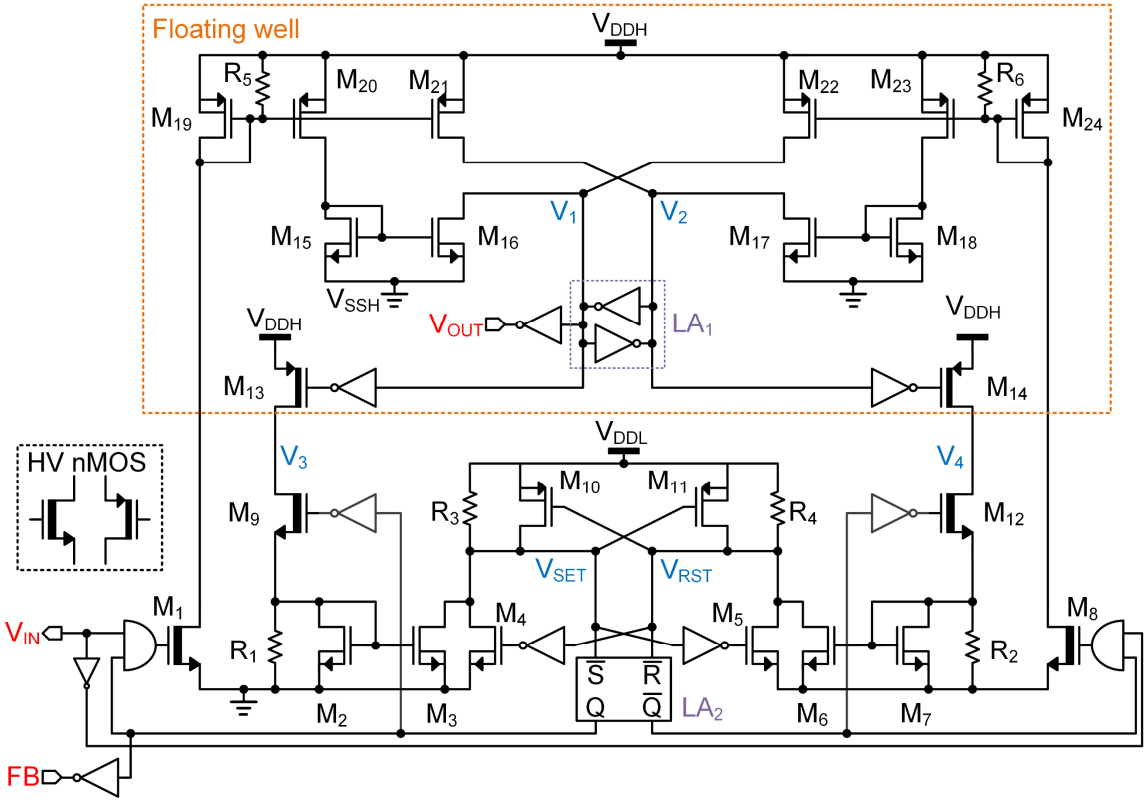

Figure 5-21. High-voltage floating level shifter with high-to-low feedback.

the level-shifter from oscillating, a CC pair, $M_{4\text{-}5}$ and $M_{10\text{-}11}$, is added: when V_{RST} is pulled low, V_{SET} is pulled to V_{DDL}, and M_4 discharges V_3 to the ground. The duration of this network activity is defined by the speed at which V_{RST} and V_{SET} can be recharged through R_3 and R_4. As a result, their values must be maintained larger than the RFTs of the floating network but low enough to permit short pulses. Simulations have shown that the CC pMOS pair, $M_{10\text{-}11}$, is enough to prevent a circuit reset from occurring after the initial transition, but the inclusion of $M_{4\text{-}5}$ increases settling speed, allowing for operation with V_{IN} duration down to 5 ns.

The operation of the level-shifter was described with the correct initial conditions given. However, it is crucial to understand what happens when LA_1 sets to a different state than indicated by V_{IN}, a condition that can occur after POR. If the top side latch results in $V_{OUT} = V_{DDH}$ and $V_{IN} = 0$ V, M_{14} will be enabled and, assuming that M_{12} is "on" as well, latch LA_2 will flip, leading to $\overline{Q} = 1$ and M_8 being "on". As a result, V_{OUT} will be reset, and the level shifter will enter the same process to turn M_8 off. Alternatively, if $\overline{Q} = 1$, M_8 will already be on, and V_{OUT} will not be able to enter an erroneous state. This mechanism removes the need for additional POR logic that would, by default, enable M_8 on start-up, leading to lower propagation

times and reduced area. Furthermore, R_3 and R_4 can be sized differently, or V_{RST} can be pulled low to force the reset state ($\overline{Q} = 1$) during POR. The only limitation of this mechanism is that it can lead to a transitional 'high' state at the output and a short-circuit condition in the output of the pulser. For this reason, the HV supply must be enabled only after POR has been completed.

The new HV level-shifter was evaluated for V_{DDL} = 2.5 V to 3 V and V_{DDH} = 5.5 V for all active device corners and was compared to the previous implementation with two pulsed level-shifters in the single element design. Simulation results of the power consumption and propagation times versus supply voltage are shown in Figure 5-22: 'V1' refers to the two previously implemented pulsed level-shifters for H2L and L2H conversion in TSMC 0.13 µm; 'V2' refers to the newly presented pulsed level-shifter with feedback in TSMC 0.18 µm. All measurements shown are based on the rise time. Whilst the falling edge propagation times are longer, they exhibited the same relationship as the rising edge results and are thus omitted. The

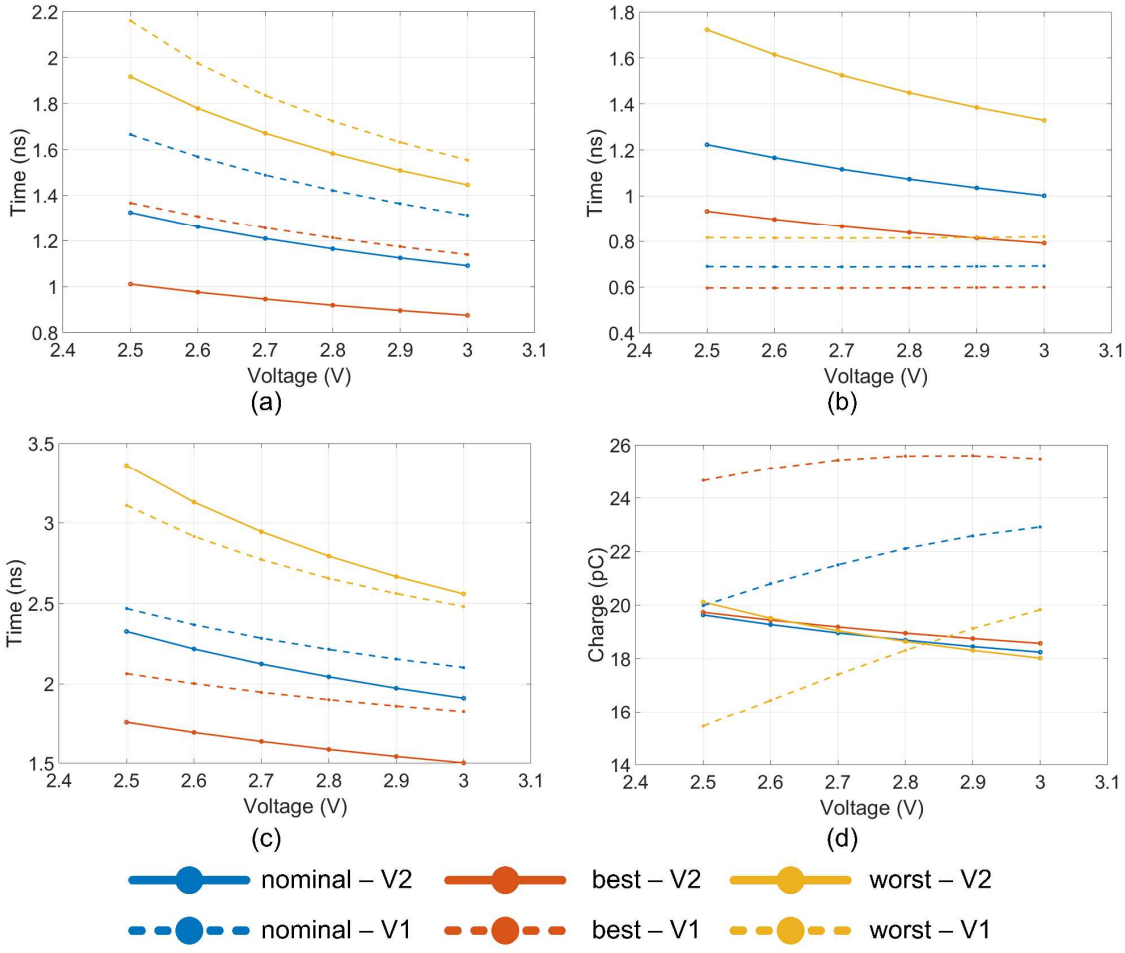

Figure 5-22. (a) Rising edge time L2H. (b) Falling edge time L2H. (c) Rising edge propagation time input to feedback. (d) Charge loss per single pulse.

rising time of V1 was faster across all process corners, Figure 5-22 (a), with a difference of approximately 400 ps or 27% and reduced with an increase in V_{DDL}. In contrast, V1 implementation showed a significantly faster H2L conversion time of around 700 ps at the nominal process corner, Figure 5-22 (b). It was independent of the supply voltage and was more than two times smaller at V_{DDL} = 2.5 V and the slowest process corner, although the difference reduced with increasing V_{DDL}.

The full rising edge propagation time from input to feedback is shown in Figure 5-22 (c). On the one hand, the V2 level-shifter propagation time varied significantly more than V1, attributed to the stronger influence of the process corners in the feedback mechanism. On the other hand, both typical and fast corners exhibited better results in V2. It also featured a significantly better power consumption, Figure 5-22 (d), which was almost identical across process corners and diminished with the increase in the supply voltage. At the nominal capsule supply voltage of 3 V, it was ≈ 25% lower than V1.

Based on simulation results, it can be concluded that the new feedback-based level shifter managed to achieve both improved feedback propagation time and lower power consumption whilst still being implemented in the larger feature technology. It is also important to note that to allow for the comparison to be as accurate as possible, minimum HV MOS and equal resistor values were used in the two designs. However, the true comparison in the same technology is needed for an empirically correct evaluation.

5.4.5 Pulse Generator and Digital Delay

Measurement of the single element pulser, Section 5.3.1, has shown that, due to the propagation delays seen in the IO of the chip, coupled with the delays in the feedback-based pulser control, the input pulse width could not be < 32 ns. Furthermore, such short pulses resulted in distortion of the input signal because of input impedance mismatch. These issues were addressed by including a pulse generator on-chip in the pulser version for an array.

Many benchtop US systems utilise a high-frequency clock (e.g., 250 MHz in VVRUS) that allows for high-resolution programmable digital delays to be used to define the pulse width accurately. They are both area and power demanding and are not viable in USCE applications. Thus, a low-power variable analogue pulse generator was chosen, Figure 5-23 (a), based on delay cells for asynchronous delays [297], [298]. The circuit allows for an extensive range of delay times from 16 ns to 2 µs and is helpful for testing purposes with a wide range of US

transducers. The drawback of the implementation is its simplicity: the delay is defined by the discharge rate through M_{A4} and the size of C_{A1}. Although its power consumption is independent of the delay time, its delay varies significantly with the PVT corners of up to ≈ 50%, limiting its use in a commercial CE device. As the discharge rate is controlled by adjusting the discharge current, a digital-to-analogue converter (DAC) can be used to adjust the pulse width between individual chips. Furthermore, both M_{A1} and C_{A1} can be segmented to trim the coarse delay to compensate for the significant corner deviations or substitute the DAC.

High-accuracy,wide range pulse generation is unnecessary in a commercial USCE device. In contrast, stability and low variability due to PVT are required. Whilst temperature is well defined in biomedical applications, the PT influence remains. An in-depth review by Abdulzazzaq et al. [299] concluded that analogue-tuneable delays should be preferred over digital counterparts for high-resolution, low-jitter and good intrinsic calibration of the PVT. In particular, a delay-locked loop (DLL) has high-performance metrics for robustness and noise immunity compared to alternatives. Nonetheless, the power consumption of the DLL can still

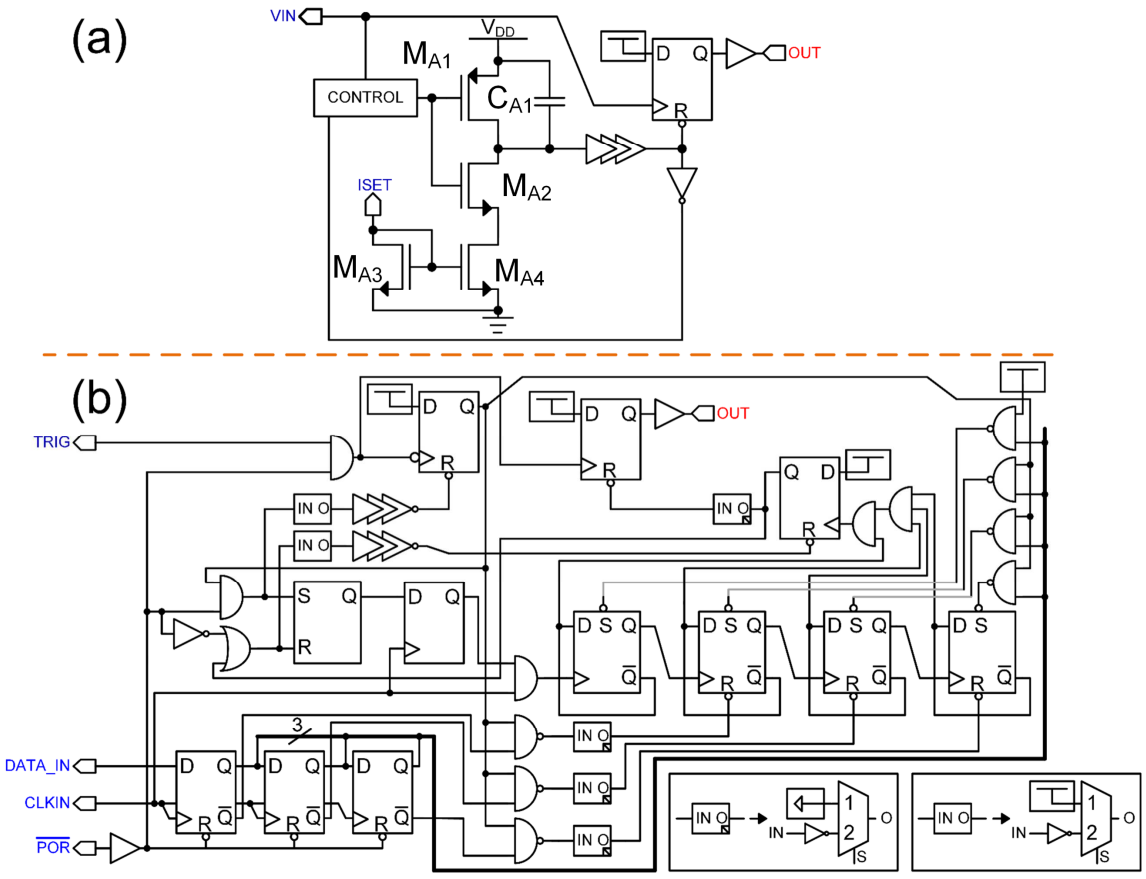

Figure 5-23. (a) Analog delay for pulse generation. (b) 4-bit digital delay

be excessive [300], and, thus, a single-time programmable delay with a DAC-controlled current for both coarse and fine-tuning is highly compatible with the low-power requirements of the USCE.

The second delay circuit was used to generate a time-out period before RX after the end of TX. The measurements of a single element pulser (Section 5.3.1) showed the existence of prominent oscillations after the falling edge, which require time to settle. The HV pulser signals are also propagated as noise on non-excited neighbouring elements. Consequently, a time-out period is required to prevent damage and over-saturation of the LV sensing front-end. Although the oscillations induced in the test PCB would be reduced in a USCE by minimising interconnect length, a delay is still required.

In essence, this function can be carried out by an external controller, but it would result in an additional signal line and power consumption, and worse delay control. Integration in the same chip solves the issue; however, a digitally generated delay is more suitable due to a limited DAC input number and low delay resolution requirement. Furthermore, the capability to adjust the delay allows for extending sensing capabilities in the near-distance of the imager. The digital delay was implemented using the available digital logic cells and is shown in Figure 5-23 (b). The resolution of the delay does not have to be high, hence a 4-bit asynchronous counter is used to provide the functionality. The falling edge of $PULSE_{IN}$ is used to start the counter automatically and is used in tandem with a f_{CLKIN} = 5 MHz to allow for delays up to 3 µs with increments of 200 ns.

5.4.6 Future Work - Area Reduction Techniques

The future work section for the whole thesis is included in Chapter 7. Nonetheless, area reduction techniques exist which require a more in-depth discussion and reference to Chapter 5, and so for the convenience of the reader, it is presented here.

Power requirements of the proposed bootstrapped pulser are low, with most of the charge being used in the V_{BOOT} node. The pulser's area requirements are still demanding, particularly in the case of a large output stage with a proportionally sized C_{BOOT}, which must meet the charge requirements of the high-side nMOS, the high-voltage level shifter and C_{PARA} of the isolation well (NBL). This section discusses circuit techniques hypothesized which can be potentially used to reduce the area further, but which were not implemented due to a limited risk tolerance associated with the tape-out schedule.

The first technique was proposed by A. Seidel et al. [301] and relies on a secondary capacitor C_{BOOT2}, charged to a higher voltage than C_{BOOT}, Figure 5-24 (a). During the turn-on, the charge from C_{BOOT2} is redistributed into the gate of the output switch M_2 through M_5 and then to the V_{BOOT} node through M_6. The amount of charge that a capacitor can store is proportional to the voltage drop across it. In this example, with V_{DDHV} = 20 V and V_{BOOT} = 5.5 V, and assuming V_{BOOT} = 5 V after charge redistribution, the total capacitor area can be theoretically reduced by a factor 29 times, assuming an ideal redistribution process. In an actual circuit, the value of capacitors $C_{BOOT1-2}$, C_{gg-M2} and the current draw of the HV level shifter vary. If C_{BOOT2} is too large whilst other capacitances and charge loss values are low, V_{GS-M2} can rise above the compliance voltage. At the same time, the minimum permitted dip voltage V_{DIP} - the voltage drop observed in V_{BOOT} after outputting '*high*' - must meet design specifications. As a result, the sizing of each capacitor must be based on the technology tolerances and charge losses, which limits the practical area improvement to well below the theoretical value.

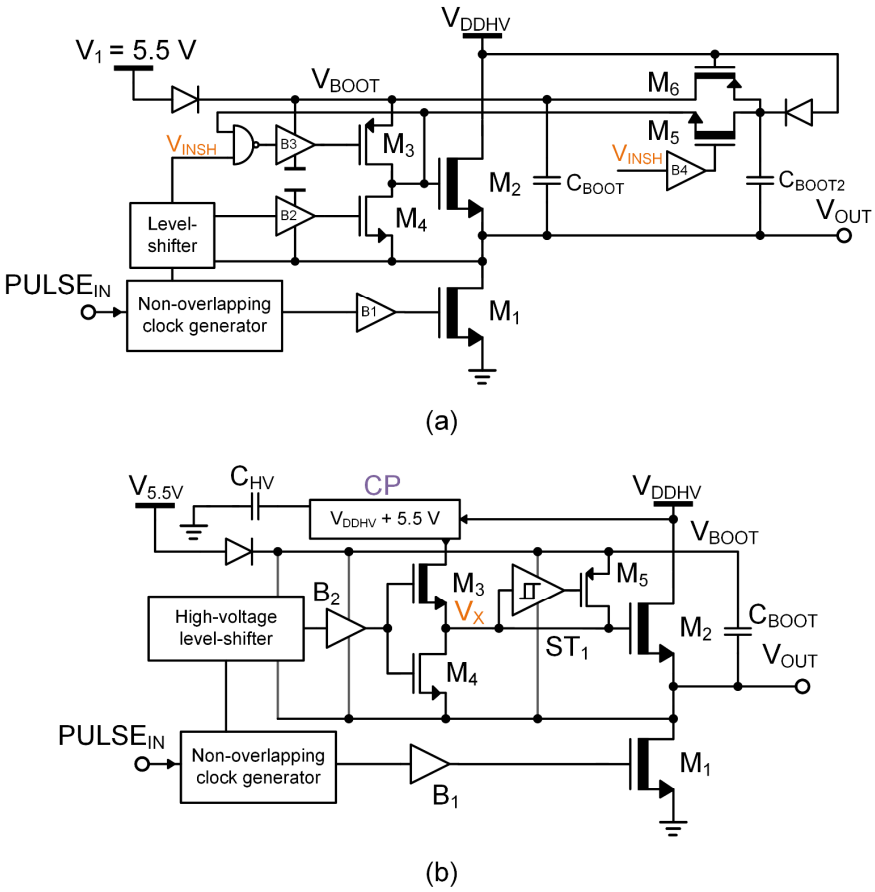

Figure 5-24 (a). High-voltage charge storing by Seidel et al. [55] (b) Reduced-area bootstrap pulser.

The high-voltage charge storage is mainly limited by the maximum voltage specification of the technology. Based on measurement results from the single element pulser (Section 5.3) that showed overshoots at the output due to high currents and a capacitive load, the top-plate voltage of C_{BOOT2} runs into the danger of generating voltages close to $2V_{DDHV}$, which would bring the device above the NBL breakdown of 36 V. To prevent such an event, devices M_5 and M_6 must be wide enough to discharge C_{BOOT2} during the rise time of V_{OUT}. Alternatively, in a system where V_{DDHV} is generated from a linear CP and assuming a linear topology, an intermediate stage of the CP can be tapped to limit V_{CBOOT2} to satisfy $(V_{DDHV} + V_{CBOOT2} < V_{MAX})$.

The parasitic capacitance between the floating high-side NBL (connected to V_{BOOT}) and the substrate is substantial. In the case of a floating supply, NBL voltage must be maintained above V_{OUT}, which leads to an increase in C_{BOOT} size. A way to circumvent this issue is to introduce an additional charge pump stage that generates a regulated voltage (V_{DDHV} + 5.5 V), Figure 5-24 (b). All NBLs can be connected to this node without charging stray capacitances every cycle. If the CP stage is used only for biasing NBL, it can be small in area, although care must be taken to ensure correct biasing during the start-up and shut-down before V_{DDHV} reaches the highest potential in the system.

Furthermore, when used in multiple channel applications, this configuration allows for further C_{BOOT} reduction if the number of simultaneous channels operating in parallel is known. If every channel requires a bootstrap capacitor, C_{BOOT}, with an area of A_{CB} for a single channel and assuming N is the number of elements in an array, the total area occupied is $(A_{CB} \cdot N)$. However, in some applications such as the USCE device in question, only K channels are required to operate simultaneously, meaning that most bootstrap capacitors (N-K) are unused.

The solution is to increase the size of the CP used for NBL biasing and use it to charge node V_X, Figure 5-24 (b), the size of C_{BOOT} can be significantly reduced. In such a case, the driving stage for the gate of M_2 requires a HV M_3. The latter is enabled first, charging node V_X to $(V_{BOOT} - V_{TH\text{-}N})$ and maintaining it until it reaches $(V_{OUT} + V_{BOOT} - V_{DIP} - V_{TH\text{-}N})$, where V_{DIP} is the dip in V_{BOOT} due to charge redistribution and $V_{TH\text{-}N}$ is the threshold voltage of a HV nMOS. A high-threshold Schmitt trigger ST_1 is then used to delay the turn-on of M_5 that pulls V_X to V_{BOOT}, and the C_{BOOT} size is reduced to supply HV level-shifter, buffer and only the remaining charge of V_X. At the same time, C_{HV} is sized in such a way to provide enough charge for $(K \cdot C_{BOOT})$, and M_3 is made wide enough to allow V_X to match the rising edge of V_{OUT}. In a

128-element system with only seven elements activated simultaneously, the total C_{BOOT} area is then theoretically reduced by a factor up to 18, although this figure is smaller due to the area of the additional CP circuitry and M_3 size.

There are three primary considerations in this the implementation. Firstly, the additional CP stage used only for NBL biasing can be made small and, even at lower efficiencies, does not increase the system overhead. Substituting a part of C_{BOOT} and using the additional CP stage for charging the gate of multiple pulsers, specifically in systems with V_{DDHV} already generated with an integrated CP, its overall efficiency drops. Secondly, the C_{BOOT} can generally be implemented using 5.5 V MIMCAPs, but the proposed implementation would require larger HV MOMcaps, reducing the actual area gain. It is not a significant drawback in some cases, where an external capacitor or a six-metal process is used. Thirdly, the source-butted M_3 contributes to C_{PARA} that can outweigh the gains of reduced C_{BOOT} and has to be carefully considered.

To conclude, assuming technology specifications are not exceeded, a combination of HV storing, improved well-biasing to reduce stray capacitances, and layout techniques for integrated capacitor placement, the area of C_{BOOT} can be significantly reduced with minimal cost to the overall efficiency, leading to a higher number of channels that can be implemented in the same area.

5.5 CONCLUSIONS

A HV pulser is the highest power consumption block in the US front-end and is crucial to achieve a viable μUS implementation in a capsule form factor with limited space and sources of energy. Two implementations of a HV pulser using a floating high-side switch for low-power US applications were presented and discussed in this chapter. The first pulser was designed to drive US transducer loads up to 550 pF and was evaluated with 1.5 MHz, 3 MHz and 28 MHz arrays. It showed the lowest power consumption among other designs whilst driving the largest transducer load.

The evaluation of the pulser using a 28 MHz array showed that excitation of the array can be achieved, but it was not optimal due to propagation times in the chip. Furthermore, the pulser energy levels dropped in the desired frequency range when a HV CP was used as the 20 V supply, indicating a need for further investigation. Parasitic effects were considered in this work and led to a larger pulser output stage. Furthermore, the evalaution identified a transient response which was stable across different loads, leading to the conclusion that parasitic effects

of the test setup were dominating the output pulse behaviour. Additional work is needed to manufacture the chips in a flip-chip and highly integrated configuration with US transducers to mitigate parasitic effects and allow reducing pulser size and energy requirements.

The second pulser circuit was presented for use in single array shared by both the TX/RX circuitry. The design was based on the single pulser architecture and showed reduced propagation delay, power consumption and bootstrap capacitor isolation. Two possible architectures were explored, with power consumption being used to evaluate their performance and show that individually controlled channels lead to the lowest power consumption. Propagation delay variations between different transmit channels were shown to be small and not to affect US characteristics. However, extensive in-vitro measurements and data evaluation are needed to verify the clinical validity of the US echo data.

A latched HV level-shifter with a maximum L2H + H2L propagation time of 2.6 ns was presented for a reduced total feedback propagation delay and to provide a mechanism for accurate high-side switch control. It relied on already published high-speed level-shifters and offered a mechanism for feedback-based break-before-make operation, without significant overhead energy costs. Finally, delay circuits for pulse generation and delay control between TX and RX phases were presented and two implementations, based on fundamental digital logic cells were presented. Finally, additional strategies for potential improvements to reduce area requirements were presented.

It can be concluded that bootstrapped HV double-nMOS pulsers are a viable low-power choice for µUS applications in CE systems. These designs can be fully integrated and offer better energy response without compromising RFTs.

6 LOW-NOISE AMPLIFIER FOR CAPSULE ENDOSCOPY

6.1 INTRODUCTION

A low noise amplifier (LNA) is the first amplifier in a chain that interacts with a sensor and has the function of amplifying the signal without degrading its SNR. In US applications, many transducers exist which, in intracorporeal environments, becomes a challenge due to the strict area and power dissipation constraints. These become even more aggravated in µUS applications with high BW requirements and lower imaging depths that necessitate fast turn-on of RX circuits following the TX pulse.

In this work, an ultra-low-power LNA for a piezoelectric transducer is proposed, based on the previous work of Chen [302]. The design is based on a capacitive feedback topology and optimises low noise while still meeting the µUS system's BW requirements of 19.6 – 36.4 MHz. The adaptated LNA allows complete turn-off and fast settling time without any additional current bias circuits and caters for a µUSCE system with only a single RX channel active at a time. Additionally, BW extension is proposed using a single integrated resistor, and dynamically self-biased LNA results are covered.

The LNA presented in this chapter was initially designed in the TSMC 0.13 µm BCD process, which comprises low-voltage devices with a maximum V_{DD} = 1.5 V, corresponding well with the 1.55 V supply available on the capsule. Due to global chip shortages, the 0.13 µm process became unavailable, and the design was ported to a new 0.18 µm BCD process, which was also halted at the time of the writing. As a result, the circuit was evaluated in simulations using corner and MC analysis with an expectation to manufacture and test the design with alternative technologies in the future.

6.2 SYSTEM ARCHITECTURE

The system specifications were derived from the µUSCE system with a split TX/RX array, as shown in Figure 6-1. It is the same as presented in Chapter 5, but a brief description is provided here as well for continuity. There are two main sub-systems: TX and RX. The latter includes an array of LNA, VGA with time-gain control (TGC), an LPF and a multiplexer, the output of which is connected to an ADC, operating at approximately 4x the centre frequency, f_C = 28 MHz. Additionally, a switch precedes the LNA to protect it from HV pulses generated

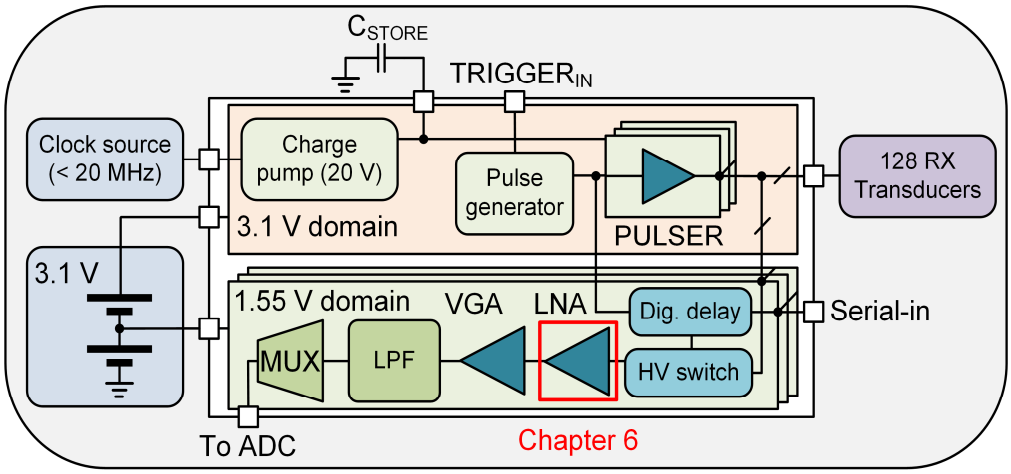

Figure 6-1. Ultrasound CE system diagram.

by the TX, and a delay element ensures that the HV switch is not connected to the array before the transmit operation is complete under any circumstances. Each RX channel has a dedicated LNA, TGC and LPF with a goal to achieve high SNR, reduce cross-talk and mitigate parasitic effects.

The system included two serially-connected 1.55 V silver oxide batteries generating 1.55 V and 3.1 V as input supplies. While the CP uses the 3.1 V supply, other circuitries require a LDO regulator (not shown) to provide a stable and noise-limited voltage. Switched-inductor regulators can be generally utilised for this functionality, but considering the limited space in the CE device and electromagnetic compatibility, an LDO was deemed a superior choice. The regulation is essential for the RX circuit to reject the noise from the CP and high transient current TX circuits. At the time of writing, most commercial LDOs operate with a drop-out of < 200 mV, which defines the minimum RX supply voltage as 1.35 V. Finally, the array used in this work had f_c = 28 MHz and a 60% fractional BW.

6.3 LNA Architectures

The characteristic impedance of a transducer determines the LNA architecture for an US system. CMUT devices generate a charge displacement due to an impinging force of a returning echo and are generally interfaced with transimpedance amplifiers (TIAs) that possess input impedance lower than the transducer. In contrast, piezoelectric transducers can have a significantly lower impedance at their resonant frequency, and again is generally implemented with voltage amplifiers [303].

Sautto presented an extensive comparison between an open-loop voltage (VA), resistive-feedback (RFA) and capacitive-feedback (CFA) TIAs for CMUT applications [304]. It has been shown that CFA resulted in the best noise performance among the three, which in their particular case was ~ 2.2x lower than that of an RFA mainly due to the absence of noise from the feedback resistor. On the other hand, the RFA exhibited a higher frequency band-pass response, while the VA and CFA showed low-pass characteristics, hinting at a better RFA compatibility for high-frequency applications. In the case of a μUSCE devices, as long as the BW requirements are satisfied, noise reduction is prioritised due to its direct link to lower power consumption or better SNR. The latter is extremely important due to higher signal attenuation in tissue at μUS frequencies [49].

A different CFA was proposed by Chen, Figure 6-2 [302], which was based on prior work on a ΔΣ modulator for MEMS applications by Christen [305]. The architecture offers a mid-band gain of C_{IN}/C_F, BW determined by the transconductance of the input devices and its impedance determined by C_I. The amplifier was based on an inverter amplifier (IA) that uses a complementary pair of nMOS and pMOS devices, allowing to effectively double the transconductance of the amplifier for the same current [306]. Furthermore, the architecture split C_{IN} and C_F for the n-type and p-type devices to isolate their gates, allowing biasing them independently, Figure 6-3 (a), whilst maintaining the gain defined as:

$$A_M = \frac{1}{2}\left(\frac{C_{IN1}}{C_{F1}} + \frac{C_{IN2}}{C_{F2}}\right) = \frac{C_{IN}}{C_F} \tag{6.1}$$

Consequently, additional cascode devices were included to increase the LNA gain, and local voltage regulators were applied to improve the power supply rejection ratio (PSRR), which is low in inverter-based amplifiers, Figure 6-3 (b). Finally, a dynamic biasing scheme was

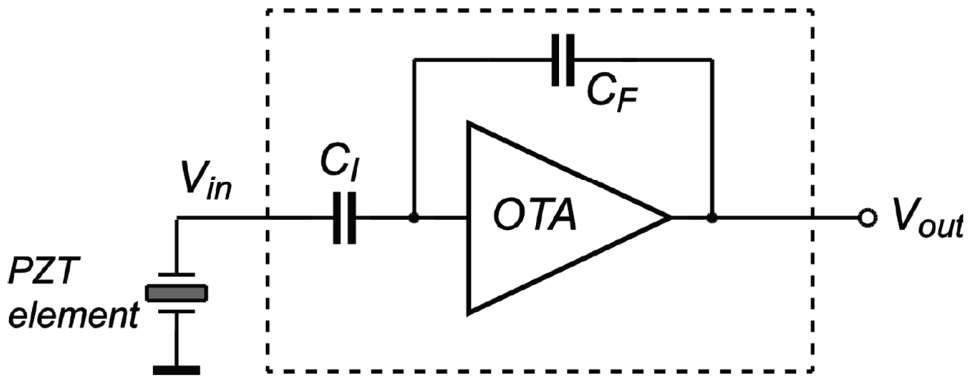

Figure 6-2. proposed LNA architecture for piezoelectric transducers (reprinted from [302]).

proposed to eliminate pseudo-resistors and reduce parasitic input capacitances and the noise from the DC control loop required to bias the inverter at the reference voltage.

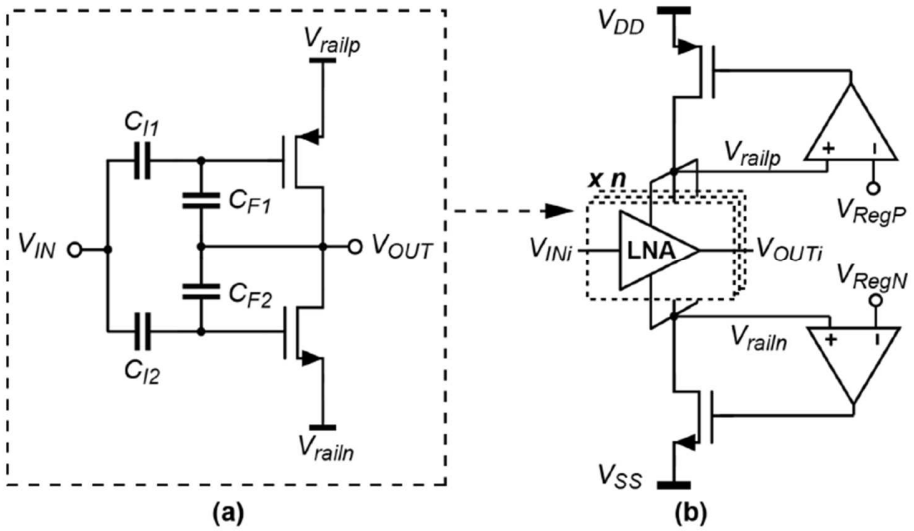

Figure 6-3. Techniques presented by Chen [302]: (a) Capacitor splitting. (b) Dual-rail local regulation.

Based on the work of Chen and prior LNA design for US transducers, three main CFA design aspects were taken into consideration for the µUSCE applications:

1. A need to fully disable the LNA and enable it with minimal delay. Previous architectures have proposed using pseudo-resistors for biasing cascode and input devices which contribute to the device noise and chip area and are detrimental to settling time after a power-on. While some architectures might require the LNAs and their supporting circuits to operate continuously, this is not needed in CE devices that activate only a tiny fraction of total channels at a time. Furthermore, the LNA settling time must be lower than the time defined by the minimum imaged depth. Assuming that imaging must commence after the first millimetre of tissue depth, the settling time must be below 3.1 µs.

2. Achieve 16.8 MHz bandwidth with f_C = 28 MHz.

3. Verify LNA operation with a 1.35 V supply in 0.18 µm technology.

6.3.1 Biasing

The dynamic biasing scheme proposed by Chen [302] is shown in Figure 6-4, and relies on periodically activating a DC control loop to bias the LNA using an error amplifier (EA).

During the TX phase, the EA inputs are connected to the LNA output and a reference voltage, and the output to the gate of the input nMOS of the LNA. The feedback loop sets the nMOS bias so that V_{OUT} is set to mid-supply. The EA is disconnected from the CFA during the RX phase, effectively putting the input gate into a high-impedance state. The bias point is maintained by the parasitic capacitances associated with the gate node of the input device. Its inputs are shorted together and connected to the mid-supply reference voltage to reduce the amplifier's offset voltage [307].

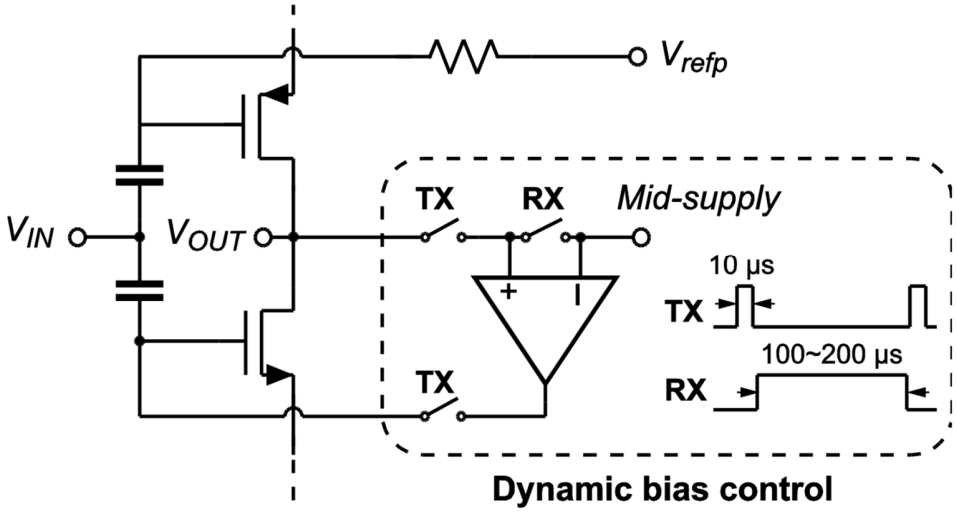

Figure 6-4. Dynamic bias control by Chen (reprinted from [302]).

The reference voltage for an IA (the LNA) is generally created using a replica bias circuit which utilises a scaled-down copy of the input inverter with the pMOS and nMOS connected in a diode configuration[4]. The main drawback of the replica bias is that it cannot be directly used to bias the IA, as any offset due to mismatches between the IA and the replica bias would result in the IA output eventually being pulled to one of the supply rails. For this reason, a DC bias control requires an EA. The dynamic bias proposed by Chen mitigated noise addition from the DC control loop and eliminated the need for pseudo-resistors for biasing the input nMOS, but it was tailored for a continuously operated LNA.

The proposed biasing and control method builds upon the same dynamic biasing scheme but adapts the operation to a synthetic aperture scheme in which most RX channels are disabled and turned on only before the RX interval. Under these conditions, the LNA bias voltage must be pulled to one of the rail voltages during turn-off and settle quickly after being enabled. The

[4] Other IA biasing schemes also exist, such as presented by Christen [305], and Harjani and Palani [308].

LNA turn-on time is mainly determined by the slew rate of the EA, which introduces a contradiction between low power, low BW and fast settling time. To eliminate this issue, an adaptive biasing scheme, not related to dynamic biasing of the CFA, can be utilised. Adaptive biasing relates to adjusting the bias current based on the magnitude of the difference between input signals [220]. The higher it is, the larger the biasing voltage and the faster the amplifier's response.

The EA chosen for this design was based on a self-biased differential inverter amplifier presented by Bazes, Figure 6-5 (a) [309] for two reasons. Firstly, it requires no additional biasing circuit, resulting in lower area and power savings. Secondly, its bias current is dynamically proportional to the input voltage levels. Moreover, when V_{IN+} is connected to V_{DD} or V_{SS}, the amplifier is disabled. As a result, the EA's output can be alternated between a disabled state and mid-supply from the replica circuit. The EA is also powered from the same 1.35 V supply to accurately predict its power consumption and BW.

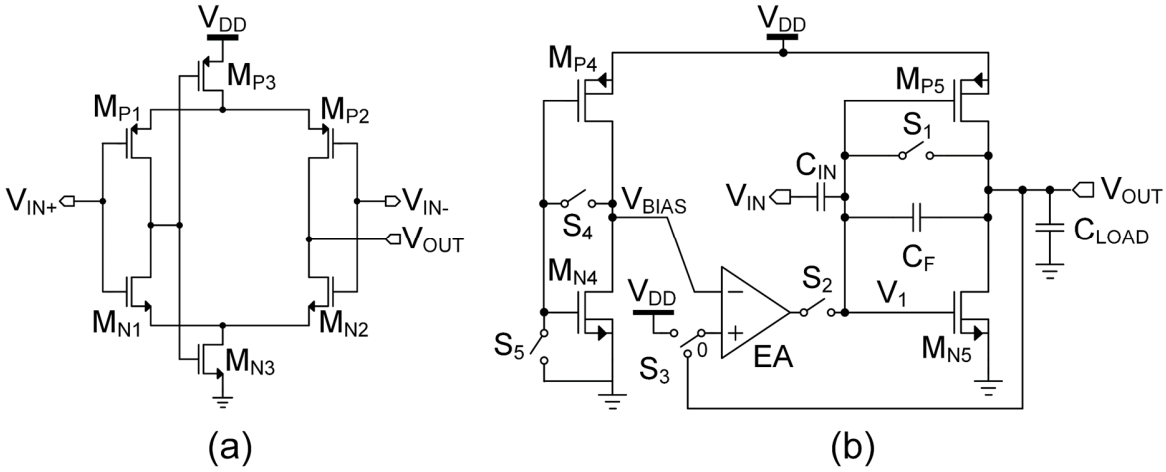

Figure 6-5 (a) Self-biased CMOS differential amplifier [309]. (b) Dynamic biasing scheme.

The biasing scheme is shown in Figure 6-5 (b). To shorten the settling time of the LNA, switch S_1 shorts input and output during the power-on; S_2 is disabled only during the RX phase; S_3, S_4 and S_5 connect EA's inputs to ground/V_{DD} during power-off or V_{BIAS} and V_{OUT} during the RX phase. The transient response of the LNA at the nominal process corner at 36°C is shown in Figure 6-6. The LNA is disabled at t = 0 µs. The EA inputs are pulled to the supply rails and its output is pulled to V_{DD}, forcing V_{OUT} to ground and disabling the whole circuit. After 1 µs, the EA inputs are connected to V_{BIAS} and V_{OUT}, and the DC control loop starts to discharge the gate node of the LNA. At the same time, S_1 is enabled momentarily, equalising V_1 and V_{OUT} to

the intrinsic mid-supply operating point of M_{P4} and M_{N4}. When S_1 is omitted, the settling time depends entirely on the current sink capabilities of the EA and capacitance at V_1. The settling time is 0.3 µs with S_1 and 1.4 µs without it, resulting in an improvement of 78.6%.

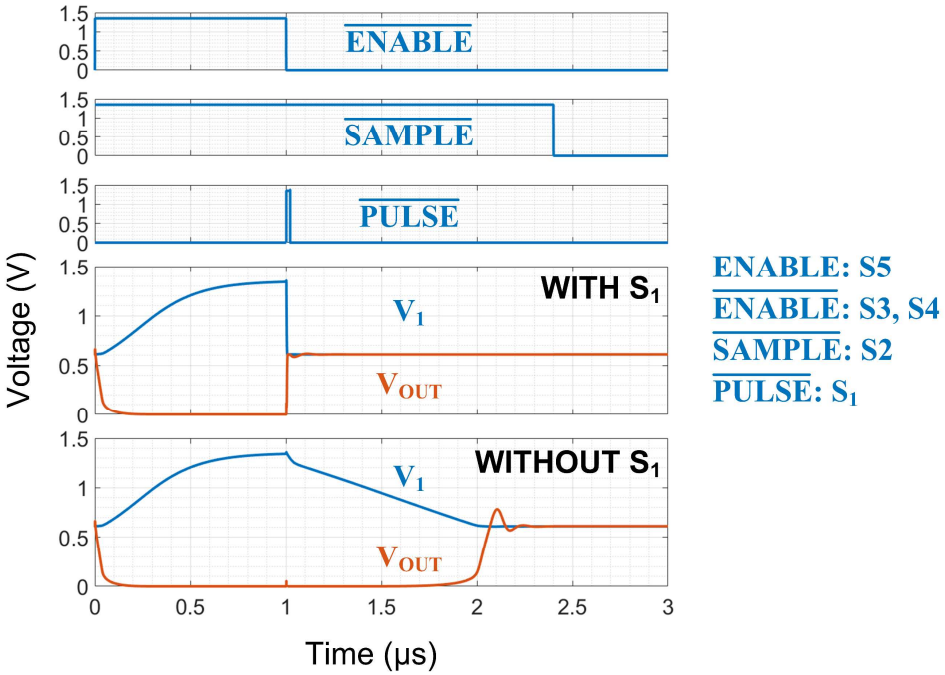

Figure 6-6. Transient response of the dynamic bias.

A closer examination of the LNA structure allows it to be that using the input-output switch can eliminate the need for the whole DC bias control scheme without sacrificing dynamic biasing functionality. This follows the concept of self-biased inverter amplifiers [310], [311]. The self-biased LNA is shown in Figure 6-7: the EA is substituted by M_{PA} and S1, which pulls

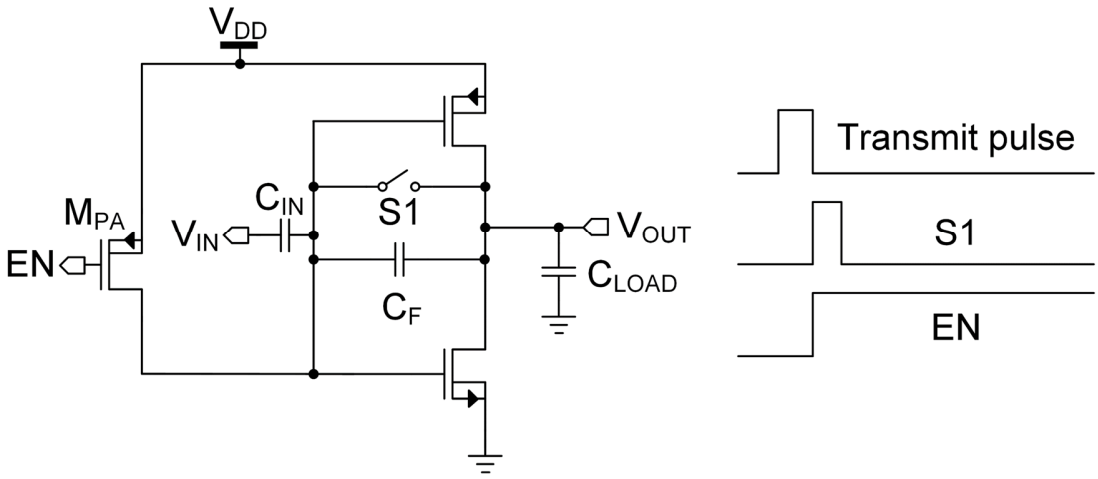

Figure 6-7. Dynamically self-biased LNA and its timing diagram.

the bias to V_{DD} and disables the LNA when not in use. Before the RX phase, M_{PA} is disabled, and S_1 is enabled for 10 ns, resulting in the LNA settling to its mid-supply operating voltage. The switch is then disabled and the LNA operates in the same way as the original version, Figure 6-5 (b). Because no additional replica bias is used, there is no need for an EA or other circuitry, reducing the total power consumption and chip area.

6.3.2 Complete LNA Design

The complete LNA circuit is shown in Figure 6-8. To increase the bandwidth of the LNA, cascode devices were not used. The ratio of C_{IN}/C_F was set to 16, for 24 dB gain, with C_{IN} = 2 pF and R_F = 0 Ω. A high-side LDO with a 200 mV drop-out voltage was chosen to regulate the 1.55 V supply down to 1.35 V, and low-side regulation was omitted altogether. The LNA output load capacitance (C_L) was set to 20 fF.

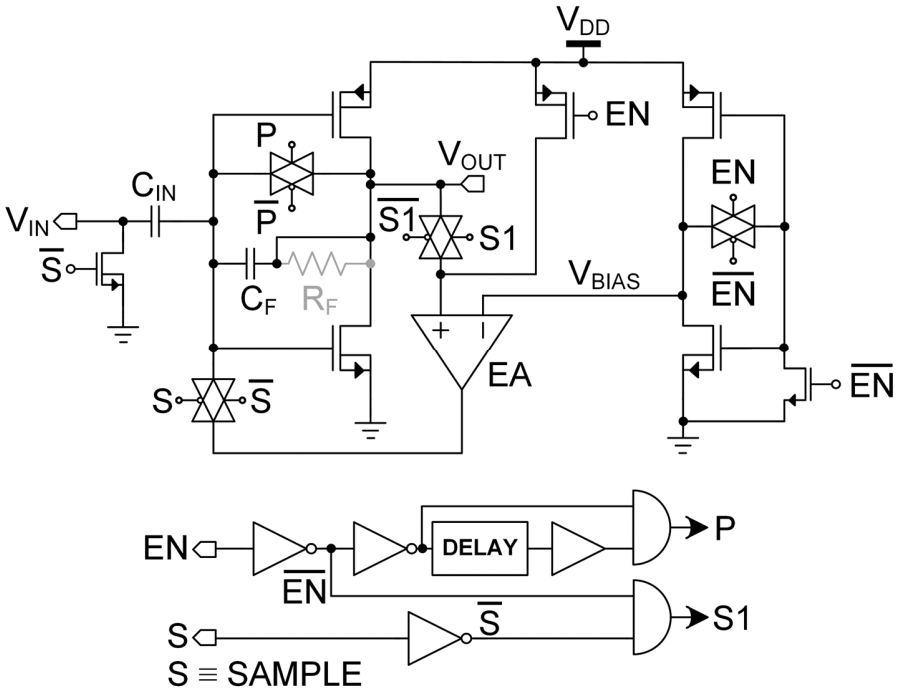

Figure 6-8. Full LNA implementation with dynamic biasing and shut-down functionality.

While the input impedance of the CFA can be easily sized to a few kΩ at general US frequencies, it is inversely proportional to f and must be evaluated together with the impedance of the transducer. The impedance of the piezoelectric μUS array used in this work was measured to be below 50 Ω at the centre frequency f_C = 28 MHz, while the CFA input impedance at this frequency was ~ 2.8 kΩ at f_C and 2.2 kΩ at f = 36.4 MHz. As a result, the input impedance of

the LNA is around 50x larger and does not significantly attenuate the signal, but the CFA architecture can be suboptimal if used with higher impedance transducers or higher frequency μUS systems.

Adding a resistor R_F in series with C_F was considered as a way to increase the LNA bandwidth. Increasing resistance can significantly extend the cut-off point, but it must be tailored to C_L to prevent gain peaking at higher frequencies. It must also be remembered that, depending on the process, the integrated resistor value can vary by ± 20%, and careful consideration should be paid to ensure the required frequency response is achieved under all conditions. Finally, an additional nMOS was added between the input and ground to reduce noise coupling from the HV switch preceding the LNA during the TX phase.

6.3.3 Results

The LNA area was defined primarily by C_{IN} and C_F, estimated to be 0.04 mm^2. The current consumption was 145 μA for the main LNA and 1.35 μA for the EA with a mid-supply common-mode voltage at the nominal corner. The replica bias consumed 5.45 μA. The noise floor was -87.6 dBm (BW = 16.8 MHz) but was -76.6 dBm when considering the full LNA BW = 212 MHz. The input-referred 1 dB compression point was P1dB = -21.27 dBm, which resulted in a dynamic range of 66.33 dB for the transducer's BW.

The gain plot of the LNA across corners is shown in Figure 6-9 (a). It can be observed that the flat-band gain is 21.5 dB and it starts to decrease over the BW of interest. The upper -3 dB limit is worst in the "ss" condition and results in 18.5 dB gain at 100 MHz. A flatter response or wider BW might be preferred in other circumstances. The effect of adding a series feedback resistor, R_F, is plotted in Figure 6-9 (b). Noise simulations show that the addition of the resistor has a negligible contribution to the total noise value. Finally, a comparison of gain and noise between an EA-biased and a self-biased LNA at the nominal corner is shown in Figure 6-9 (c) and (d), respectively. The simulation was carried out by running a transient response and saving the circuit's operating point at the time that the LNA is correctly biased. As the circuit operates without any switching during the sampling operation, a periodic noise analysis was not required. The data shows that, while the gain-frequency response in the BW of interest is almost identical, the noise response varies significantly. The self-biased version exhibits lower noise than the EA-biased version up to the crossover at 7 MHz and 4.85 nV/√Hz due to the additional noise generated from the output of the EA. Going up in frequency, the input-referred voltage

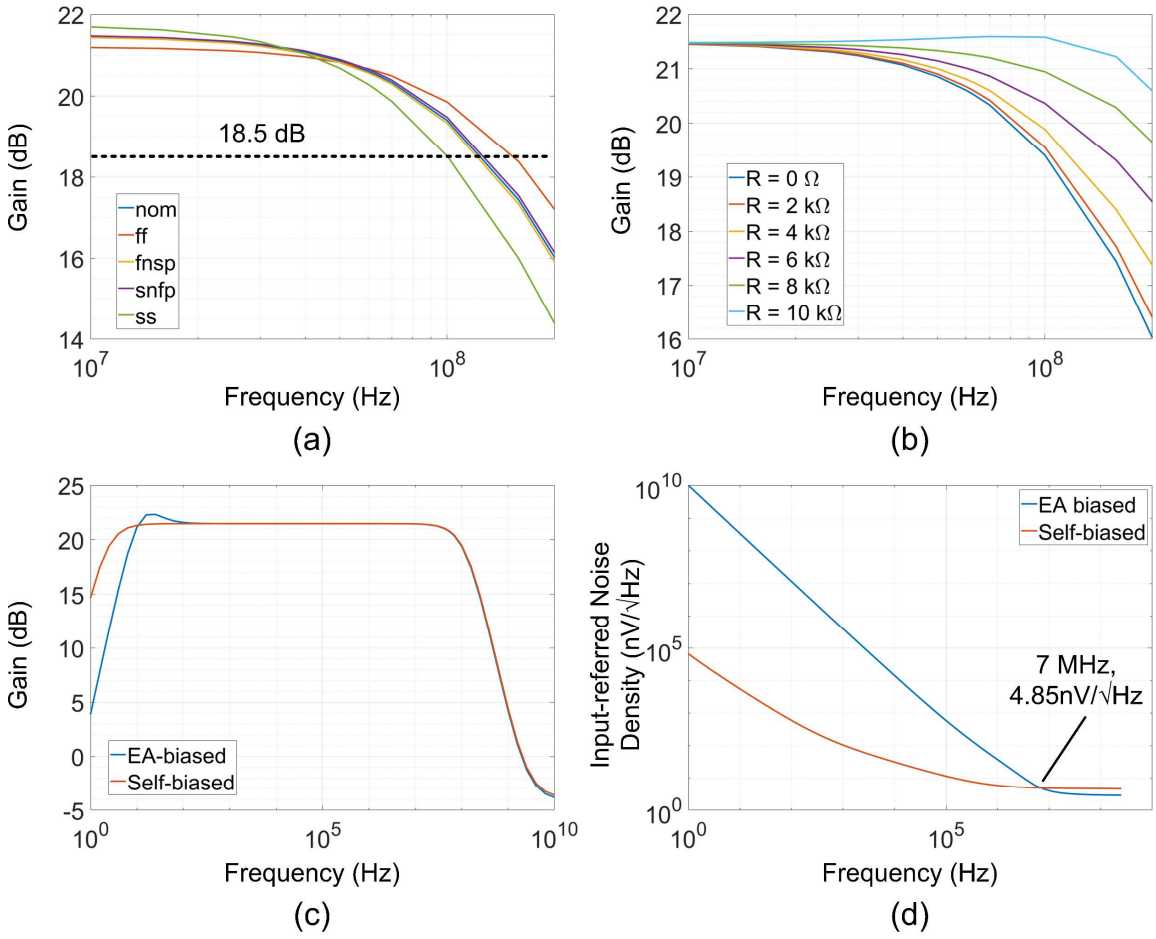

Figure 6-9. (a) LNA gain at different process corners. (b) Gain variation with different R_F values. (c) Gain comparison and (d) noise response of the EA-biased and self-biased architectures.

noise density of EA-biased LNA decreases further and reaches 3.11 nV/√Hz at 28 MHz. The equivalent noise in the self-biased version at the same frequency is 33% higher, 4.66 nV/√Hz, which proves the necessity of EA biasing to achieve the best noise performance. The integrated input noise voltages within the BW of the transducer are 12.84 μV_{RMS} and 19.13 μV_{RMS} for the EA-biased and self-biased versions, respectively.

A comparison with the state-of-the-art is shown in Table 6-1. The proposed circuit achieves low area whilst its power consumption is higher than some designs due to higher f_C. The design achieved a very low noise density figure at f_C and the highest BW.

Table 6-1. Performance summary and comparison.

Ref	Supply Voltage (V)	Target Transducer	Area (mm^2)	Bandwidth (MHz)	Power Consumption (mW)	Dynamic Range (dB)	Input Referred Noise (nV/√Hz)
[312]	1.5	PMUT	0.0006	22	0.3	69	7.1 @ 3 MHz
[278]	1.8	CMUT	-	5.2	14.3	60	0.144 @ 3 MHz
[304]	1.8	CMUT	0.18	11	1	70	8.48 @ 10 MHz
[302]	1.8	piezoceramic	0.01	11.2	0.135	81	5.9 @ 4 MHz
This Work*	**1.35**	**piezoceramic**	**0.05****	**211**	**0.196**	**55**	**3.5 @ 28 MHz**

* Simulation results.
** Estimated from layout.

6.4 CONCLUSIONS

This short chapter discussed the design and simulation of an ultra-low-power LNA design based on a capacitive feedback inverter amplifier. The prior state of the art was overviewed, and different biasing schemes were discussed that would easily disable the LNA without any external reference currents or eliminate the biasing circuit. Circuit-level simulations showed consistent results across design corners whilst delivering low noise and power consumption. The self-biased approach has significantly improved noise results for the lower frequency range but exhibited poorer performance in the relevant BW. It can be concluded that the self-biased LNA is a perfect candidate for high-integration US systems, whilst dynamic biasing using an EA should be used to achieve better noise performance in µUS systems.

7 CONCLUSIONS AND FUTURE WORK

7.1 CONCLUSIONS

The main contributions of this thesis were to examine traditional CE technologies and engineer circuit solutions for an integrated μUSCE device, with a focus on HV power management, HV pulse generation and low-noise amplification. Although the work was negatively affected by the SARS-CoV-2 pandemic and the disruption in the chip manufacturing industry, leading to changes in technology and hindering tape-out possibilities, many engineering goals were achieved.

A coherent review of traditional GIT imaging methods was provided, focusing on the detailed investigation of currently available CE devices and including emerging technologies in the field, for higher image performance, clinical convenience and operational time. The technology was considered from the perspective of power requirements, and two HV imaging modalities, namely US and autofluorescence, were analysed. The chapter looked at previous prototypes in the field, showing the design challenges needing to be addressed to advance CE technology further. Based on the literature survey, it was made evident that, whilst conventional WCE devices have advanced significantly in operational time and image quality, same and new challenges remain to be solved for μUSCE devices. In particular, a need for high efficiency HV generation and piezoelectric transducer driving exists.

A novel HCP, based on conventional CCCP and SPCP, was proposed for HV and low current US, fluorescence and other intracorporeal applications. An optimisation methodology was provided for a practical implementation of the SPCP, while the CC was investigated for latch-up risks and showed no long-term performance degradation. A detailed measurement comparison between the proposed SPCP and a conventional DKCP was provided. The SPCP was found to perform worse than its post-layout simulations, and an extensive analysis of possible causes and methods to address them was carried out. Although it was found that the model of the Schottky diode, used in both SPCP and DKCP, was inaccurate, the DKCP circuit simulation matched experimental measurements, indicating existence of unmodeled parasitic elements detrimental to the SPCP architecture.

Nonetheless, the results of the CCCP stage showed promising results and the architecture was used as the basis of a second HV and high current CCCP version, described in Chapter 4.

The design incorporated a boosted clock switching scheme and two comparator-based duty-cycle control schemes. The CP was fully characterised and showed efficiencies of up to 60% and a regulated output voltage of up to I_{OUT} = 500 µA. Furthermore, a SO CP implementation was proposed, compatible with any CP architecture. The scheme offered a means of generating a clock with minimal area and power overhead. At the same time, it included the functionality of frequency control which was consistent within the biomedical temperature range of operation and produced a smoothed operating current to improve operation in battery-powered systems. High efficiency with large I_{OUT}, and an area and power efficient SO offers a self-contained solution for HV generation in a CE device.

Operation of a µUSCE was then described and a HV bootstrapped pulser with a double-nMOS output stage for µUS transducers was proposed. The design involved a description of system operation and an evaluation of the parasitic effects for large transducers. It was tested with 1.5MHz (US), 3 MHz (US) and 28 MHz (µUS) arrays and indicated meagre power consumption, dominated by the 100 µA current from the 6 V supply. Power requirements of the HV supply were also evaluated for different operating voltages, and output pulse frequency response was characterised and compared to a VVRUS. These results indicated a flat response across frequency and elucidated a low-performance loss when powered from a CP supply in comparison to a benchtop supply.

The single element pulser was elaborated on to suit a TX/RX array. The work entailed a qualitative evaluation of two different pulser architectures, showing that individual rather than group control of channels was more beneficial to power consumption under all circumstances. A new low-power version that offered minimal propagation time variations and incorporated a newly presented latched HV floating level shifter with a HV to LV feedback mechanism with an average feedback time of < 2.5 ns. The pulser also distinguished itself with stable charge consumption across manufacturing corners and low variation between individual channels. Finally, strategies to reduce the bootstrapped pulser's area were suggested.

Work on an LNA was based on the previously reported IA for conventional US. We investigated the complete turn-off mechanism of the circuit using a self-biased differential amplifier switching scheme, which additionally improved the LNA settling time. A self-biased version, allowing for the elimination of the biasing circuit altogether, was also covered, and a comparison to the original dynamically biased LNA was carried out. It was shown that the LNA was compatible with a 28 MHz ultrasonic array and its BW could be increased even further.

The work presented in this thesis on CPs has led to a new method of voltage amplification, output regulation and input current smoothing. The proposed pulser verified the performance of bootstrapped architectures for transducer excitation and enabled a single-chip framework for µUS transducer testing; the work on the LNA has laid the groundwork for the development and realisation of ultra-low-power sensing in CE devices. All of these circuits represent a multifaceted step towards µUSCE. Most importantly, it is the urgency of catching GIT diseases in early stages as well as understanding the cellular mechanisms involved that made this work relevant to further development of this field.

7.2 FUTURE WORK

Some of the future work was outlined in Chapter 5, but several tasks remain in the field of µUSCE and HV implantable devices that should be mentioned. These can be split into work required in ASIC design and system-level work on a required for a µUSCE device.

7.2.1 ASIC Design

The HV HCP presented in Chapter 3 gave an in-depth look into a new SP architecture and proposed a new switching scheme which could improve the performance degrading effects analysed in the chapter. A complete analysis of an improved version of the proposed SP should be carried out, including testing fewer stages and different HV isolation bias schemes. The design could be evaluated for two, three and four stages to understand variations in efficiency whilst comparing the circuit's behaviour to its theoretical model. It is also important to note that, assuming the design suffered performance degradation due to underestimation of parasitic capacitances of leakage currents, it should be manufactured in silicon-on-insulator technology that significantly reduces parasitic structures and stray capacitances, resulting in improved circuit behaviour while maintaining the practical area improvements offered by the original design.

The results of the manufactured high-current CP (Chapter 4.2) have shown that the ripple at the output is significant under hysteresis control, and switching noise is present under both hysteresis and latched comparator regulation approaches. The switching frequency of 20 MHz was also within the bandwidth of the US imaging system powered by the HV supply, potentially leading to a noise increase in US imaging data. As a result, the presented CP requires further testing and evaluation of the US image data to verify the compatibility of the high-frequency

CP and different regulation schemes. The addition of a HV low-dropout regulator should be explored if high noise figures are found.

The SOCP (Chapter 4.3) was proposed as a low-area, low power solution that suits intracorporeal environment to generate a stable clock frequency inside a chip. This work needs to be practically tested and validated. Additionally, a frequency control scheme must be included to allow low-ripple and high-efficiency regulation. The SOCP can also be tested with additional stages to confirm its operation and robustness for generating HV outputs. Furthermore, the SOCP could be re-engineered to include charge-recycling, a technique which shorts the two opposite CCCP clock inputs during the non-overlapping period, allowing for half of the charge to be re-used in the next cycle [313] and increasing the CP's efficiency. No such implementation has been demonstrated to date.

A HV pulser was tested for large capacitive loads and μUS frequencies. Future work in this topic involves manufacturing and testing a bootstrapped pulser with a piezoelectric array and characterising the performance of the generated US wave. Although propagation delays in individual pulser elements were discussed, their effects must be further verified with experimental measurements, followed by tests using the entire TX/RX system. The quality of the acquired US image data must be investigated for different TX/RX configurations. Potential architectures to reduce area requirements of the bootstrapped pulser were discussed and can be tested further, including designs for reducing dynamic losses and generating multi-level output waveforms.

The future work associated with the LNA presented in Chapter 6 should start with the addition of an LDO to improve the PSRR of the amplifier circuits. This is a significant issue as ensuring high PSRR at $f_C = 28$ MHz with an area-aware implementation and low-power requirements is challenging. The LNA is also only the first amplifying element in the receiver front-end and has to be followed by a VGA with suitable TGC and a multiplexing scheme. The LNA results show that further filtering is also required to limit the circuit's BW. The section on the LNA also included a self-biased design variation which simplified the circuit at the cost of noise increase within the BW of interest. Further manufacture, testing and comparison between the self-biased and replica-biased circuits should be conducted to confirm the results. Furthermore, new techniques beyond a good LDO should be explored to improve the PSRR. As mentioned in Chapter 6, the replica bias can be used as a second input to the VGA to reject common-mode variations in the LNA so as to improve the supply rejection. The same approach

could be explored in a self-biased implementation using neighbouring elements to extract common-mode voltages, but a close analysis of mismatch effects will be necessary.

7.2.2 General µUSCE Systems

A few engineering milestones need to be reached to move towards a fully wireless µUSCE device. The first is the electronic system which has to fit on a few approximately 10 mm diameter circular PCBs, interconnected with flexible PCBs or other means. It has to entail a processing unit likely integrated with the US front-end, ADC, and a multitude of connectors to the transducer array. Interconnects also pose an issue because the array has to be placed perpendicular to the PCBs or around the circumference of the capsule wall. This engineering challenge requires thoughtful consideration for a financially viable device.

The second issue is the energy storage or WPT. Although the device needs to operate for only a fraction of the time, most of its instantaneous power consumption coincides (TX, RX, ADC, processing, data storage or transmission). While it has been shown in this work that the pulser and US array both draw only 100 µA under some operating conditions, most currently available ADCs alone can draw > 100 mA. Such large current requirements would affect the supply voltages and thus the performance of the US front-end circuitry. This issue could be compensated by WPT or super-capacitor implementations, which must also minimally impact the already limited space. The issue can be approached from another angle by utilising state-of-art ADCs with lower current and voltage requirements, which would then meet the battery operating voltage range (< 1.55 V).

The last milestone is clinical relevance. The µUSCE device must provide quantifiable medical information superior or complementary to conventional WCE and enteroscopy methods. At the same time, it must be financially viable and accepted by both patients and clinicians; the latter must also be trained to interpret the data effectively. Furthermore, current WCE devices cost around $500 and are single use only [314]. A multimodal capsule endoscope with both white-light imaging and US would potentially require customly manufactured arrays and cost more. Methods for reuse need to be explored and characterised, including creating a hermetically sealed and durable capsule package integrated with the array.

Overall, the realisation of a µUSCE device entails many challenges spanning a wide range of engineering and clinical disciplines. From the perspective of electronic design, a fully integrated single-chip solution is needed; it would entail US front-end, digitisation and

processing units, and power management system blocks. With time, constant effort and technological advancements, μUSCE will become a cheap and accurate method for GIT inspection and open possibilities for much earlier diagnosis, better screening practices, and improved quality of life.

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