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Integrating high efficiency energy conversion nanostructures on flexible substrates

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Prof. Ravinder Dahiya

Abstract

Flexible electronics that can bend, fold, stretch, or conform to curvy surfaces continue to have a huge impact on numerous aspects of our daily lives, such as in healthcare, prosthetics, etc. Recent developments have shown that high-performance flexible electronics are required to advance several applications, particularly where faster communications and computation are required. In this regard, the use of high-quality inorganic semiconductors such as monocrystalline silicon and compound semiconductors can open new opportunities for flexible electronics. These materials formed the basis of the semiconductor industry over last several decades and transformed almost every sector of the economy worldwide. For more than 60 years the electronic devices have been manufactured using a sequence of lithographic processes and chemical processing steps, creating in the end electronic circuits on planar silicon (Si) and/or other rigid semiconductor substrates. These process sequences do not work well for flexible electronics due to thermal budget-related issues. For instance, the implementation of certain fabrication process steps, such as doping by thermal diffusion and dielectric deposition via chemical vapor deposition (CVD), becomes challenging on flexible substrates due to their incompatibility with harsh temperatures required by these processes. To this end, transfer printing of silicon and compound semiconductor micro/nanostructures on flexible substrates such as nanoribbons (NRs) provides an attractive solution. This thesis explores this direction to address the longstanding issue of attaining electronic on flexible substrates and at the same time exhibit the performance similar to conventions micro/nanofabricated Si based electronics. In particular, the thesis explores the transfer printing approach, and its advanced version i.e., direct roll transfer printing, to integrate high mobility inorganic nanostructures on flexible substrate. First, the conventional transfer printing method is modified to achieve high transfer yield of silicon nanoribbons on flexible polyimide substrate. Here, the new part with respect to conventional transfer printing -is that the high-quality dielectric layer is deposited after the transfer printing step. The developed method led to high mobility Si nanoribbon based flexible transistors (> 600 $cm^2/V.s$). However, the developed devices suffered from shortcomings such as poor uniformity over

large areas, impurities, lower transfer yield, presence of elastomeric residues on Si nanoribbons and poor registration. Such issues would limit the scalability of presented approach and to mitigate the potential adverse consequences, I developed a novel direct roll transfer printing method to print micro/nanostructures arrays of high mobility inorganic semiconducting materials such as Si, GaAs in a single step. These micro/nanostructures arrays were printed on a variety of flexible substrates including polyimide, polyethylene terephthalate, and metal foils, etc. The developed technique has the following distinct advantages: (i) unlike conventional transfer printing, the presented method does not require an elastomeric (e.g., Polydimethylsiloxane (PDMS)) transfer stamp (hence, named as direct transfer printing). Besides solving the challenges issues related to conventional transfer printing, this method also led to a reduced number of printing steps and hence saving in terms of cost and time. Further, it reduces the chance of breakage and/or wrinkling of printed nanostructures and hence helps to preserve their morphology and structure. This also offers an excellent opportunity to enhance the transfer yield and registration of printing nanostructures; (ii) The process helps to achieve high device-to-device uniformity by avoiding contamination from PDMS stamps, and (iii) the process is compatible with R2R fabrication which is advantageous for future large area electronics (LAE) manufacturing. The versatility of direct roll printing is demonstrated by obtaining the high-performance flexible field-effect transistors based on n- and p-channel silicon nanoribbons, high speed broadband photodetectors based on GaAs microstructures and multifunctional Si NR based micro solar cells. The silicon NR based n-channel transistors consistently show high performance i.e., high on-state current (Ion) >1 mA, high mobility (μ_{eff}) >600 cm^2/V.s, high on/off ratio (Ion/off) of around 10^6, and low hysteresis (<0.4 V). The direct roll transfer printed GaAs microstructures-based photodetectors exhibit excellent performance under ultraviolet and near-infrared illumination, including ultrafast response (2.5 ms) and recovery (8 ms) times, high responsivity (>10^4 A/W), detectivity (>10^{14} Jones), external quantum efficiency (>10^6), and photoconductive gain (>10^4) at low operating voltage of 1 V. Furthermore, the developed direct roll transfer printing has been demonstrated as an effective method to realize miniaturized solar cells with dual functionality: energy harvesting and self-powered photodetection. These micro solar cells have an area of approximately 315 µm^2 and exhibit a

maximum power density of around 11 $\mu W/cm^2$. The developed photodiodes or micro solar cells can also function as a self-powered photo sensors with distinctive photo response under visible-UV-NIR light illumination. This photo sensor module shows high-speed response, peak responsivity of 2.48 A/W at 365 nm, external quantum efficiency of 8.30×10^2 %, and detectivity of 2.74×10^{13} jones. Additionally, the device demonstrates an exceptionally fast response speed (rise time τ_{Rise} = 205µs and fall time τ_{Fall} = 200µs) and stable detection performance. These flexible photodiodes present a potential pathway to develop self-powered broadband photodetectors for future smart optoelectronic applications, such as light imaging, light wave communication, integrated wireless sensor networks (WSNs), and wire-free routes for artificial e-skin. Heterogeneous integration of high mobility inorganic nanostructure such as silicon and compound semiconductors on flexible substrates, shown in this thesis work, also provides a potential route towards implementation of the high-performance energy autonomous flexible electronic systems.

List of Publications

The work in this thesis is based in full on the previously published articles listed below.

Journal Articles

1) Direct Roll Transfer Printed Silicon Nanoribbon Arrays based Multifunctional Micro Solar Cells.
Zumeit, A., Dahiya, A.S., Nair, N.M., Ma, S., Christou, A., Dahiya, R.
Advanced Electronic Materials (In progress) (2023)

2) Printed n- and p-Channel Transistors using Silicon Nanoribbons Enduring Electrical, Thermal, and Mechanical Stress.
Neto, J., Dahiya, A.S., **Zumeit, A.**, Christou, A., Ma, S., Dahiya, R.
ACS Applied Materials and Interfaces 15(7), 9618-9628 (2023)

3) Printed GaAs Microstructures-Based Flexible High-Performance Broadband Photodetectors.
Zumeit, A., Dahiya, A.S., Christou, A., Mukherjee, R., Dahiya, R.
Advanced Materials Technologies 7(12), 2200772 (2022)

4) High-performance p-channel transistors on flexible substrate using direct roll transfer stamping.
Zumeit, A., Dahiya, A.S., Christou, A., Dahiya, R.
Japanese Journal of Applied Physics 61, SC1042 (2022)

5) High-Performance n-Channel Printed Transistors on Biodegradable Substrate for Transient Electronics.
Dahiya, A.S.#, **Zumeit, A.#**, Christou, A., Dahiya, R.
Advanced Electronic Materials 8(9),2200098 (2022) *# Equal contribution*

6) Printing of Nano- to Chip-Scale Structures for Flexible Hybrid Electronics.
Christou, A., Ma, S., **Zumeit, A.**, Dahiya, A.S., Dahiya, R.
Advanced Electronic Materials (Article in Press) (2022)

7) In Tandem Contact-Transfer Printing for High-Performance Transient Electronics.
Dahiya, A.S., Christou, A., Neto, J., **Zumeit, A.**, Shakthivel, D., Dahiya, R.
Advanced Electronic Materials 8(9),2200170 (2022)

8) Direct roll transfer printed silicon nanoribbon arrays based high-performance flexible electronics.
Zumeit, A., Dahiya, A.S., Christou, A., Shakthivel, D., Dahiya, R.
npj Flexible Electronics 5(1),18 (2021)

9) Nanoribbon-Based Flexible High-Performance Transistors Fabricated at Room Temperature.
Zumeit, A., Navaraj, W.T., Shakthivel, D., Dahiya, R.

Advanced Electronic Materials 6(4),1901023 (2020)

10) High-performance printed electronics based on inorganic semiconducting nano to chip scale structures.
Dahiya, A.S., Shakthivel, D., Kumaresan, Y., **Zumeit, A.**, Christou, A. and Dahiya, R. ***Nano Convergence*** 7(1), 33 (2020)

11) Printing Routes Toward High-Performance Electronics on Flexible Substrates.
Applied Physics Review (In progress) (2023)

Conference Proceedings

1) Dual-Gate Transistors using Contact Printed ZnO Nanowires.
Neto, J., Dahiya, A.S., Christou, A., **Zumeit, A.**, Pamphilis, L.D, Dahiya, R.
FLEPS 2023 - IEEE International Conference on Flexible and Printable Sensors and Systems, Proceedings (2023)

2) High performance n-and p-channel flexible transistors using roll printed silicon nanoribbons.
Zumeit, A., Dahiya, A.S., Christou, A., Dahiya, R.
FLEPS 2022 - IEEE International Conference on Flexible and Printable Sensors and Systems, Proceedings (2022) (**Nominated for a Best Paper Award**)

3) Silicon nanoribbons based printed transistors for high-performance flexible electronics.
Zumeit, A., Dahiya, A.S., Shakthivel, D., Dahiya, R.
FLEPS 2021 - IEEE International Conference on Flexible and Printable Sensors and Systems, 9469776 (2021) (**Best Paper Award**)

4) Direct roll transfer printed transistors for high-performance flexible electronics.
Zumeit A., Dahiya A. S., Christou A., Shakthivel D., Liu F. and Dahiya
SSDM 2021 - Solid States Devices and Materials conference (2021)

5) Si Nanoribbons based High Performance Printed FETs using Room-Temperature deposited Dielectric.
Zumeit, A., Shakthivel, D., Dahiya, R.
FLEPS 2020 - IEEE International Conference on Flexible and Printable Sensors and Systems, 9239533 (2020) (**Best Paper Award**)

6) High Performance Printed Electronics on Large Area Flexible Substrates.
Soni, M., Shakthivel, D., Christou, A., **Zumeit, A.**, Yogeswaran, N., & Dahiya, R.
EDTM 2020 - 4th Electron Devices Technology and Manufacturing Conference, Proceedings (2020)

7) Reliability investigation of Via-bridges for flexible electronics.
Neto, J., **Zumeit, A.**, Navaraj, W., Dahiya, R.
FLEPS 2019 - IEEE International Conference on Flexible and Printable Sensors and Systems, Proceedings, 8792275 (2019)

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Author’s Declaration

I, Ayoub Zumeit, hereby declare that except where explicitly reference is made to the contribution of others, this thesis is the result of the work of the named and has not been submitted for any other degree at the University of Glasgow or any other institution.

List of Abbreviation

PE	Printed Electronics
IoT	Internet-of-Things
E-skin	Electronics skin
RT	Room temperature
RFID	Radio frequency identification
E-waste	Electronic waste
ICT	Information and Communication Technologies
CMOS	Complementary metal-oxide-semiconductor
1D	One-dimensional
2D	Two-dimensional
3D	Three-dimensional
NSs	Nanostructures
NWs	Nanowires
NRs	Nanoribbons
NCs	Nanocones
NMs	Nanomembranes
CNTs	Carbon nanotubes
SOI	Silicon on insulator
BOX	Buried oxide
SOD	Spin-on-dopant
MOSFETs	Metal oxide semiconductor field effect transistors
UTCs	Ultra-thin chips
LAE	Large area electronics
R2R	Roll-To-Roll
AFM	Atomic Force Microscopy
SEM	Scanning Electron Microscopy
HF	Hydrofluoric
RIE	Reactive ion etching
SAM	self-assembled monolayer
SAND	Self-assembled monolayer
PDMS	Polydimethylsiloxane
EMG	Electromyography
PET	Polyethylene terephthalate
PI	Polyimide
SMPs	Shape memory polymers
Tg	Glass transition temperature
CBSMP	Carbon black-shape memory polymer
ALD	Atomic Layer Deposition
LPCVD	Low-Pressure Chemical Vapor Deposition
PECVD	Plasma-enhanced chemical vapor deposition
ICP-CVD	Inductively Coupled Plasma-chemical vapor deposition
DRTP	Direct Roll Transfer Printing
RMS	Root means square
PDs	Photodetectors
sccm	Standard cubic centimeters per minute
MS	Metal-semiconductor
MSM	Metal-semiconductor-metal
LED	Light Emitting Diode
FEA	Finite Element Analysis
ELO	Epitaxial lift-off

Chapter 1.

Introduction

Since the middle of the 20th century, the third industrial revolution also known as 'the digital revolution' has revolutionised almost all socio-economic sectors (e.g., healthcare, aerospace, manufacturing, retail etc.) through developing electronics and information technology for faster communication, and computation. The well-known Moore's Law was the driving force during the digital revolution which states that the number of transistors on an electronic chip will double roughly every two years, and the overall processing power and functionality for computers will double within a fixed cost, power, and area. The developed electronics following the Moore's Law was and is still on rigid Silicon (Si) wafers. While significant innovations in electronics design and process technologies continue to drive Moore's Law based Si technologies, but the economics and performance are clearly saturating. The flattening of the Moore's curve is pushing the semiconductor industry/scientists to find a technology beyond CMOS and Moore's law, which can also satisfy the growing demands of emerging technologies such as the internet of things (IoTs), robotics etc. where human-machine interaction is critical.

Along with the high device performance (high speed computation), new form factors such as flexibility and bendability are needed for these emerging technologies. The large area flexible systems that convert physical and/or chemical stimuli into electrical signals will make the core of next-generation smart electronics in the post-Moore era. Because of these electronics characteristics, there is growing interest in large-area flexible electronics as they find applications across numerous sectors, including wearables, robotics, consumer electronics, and healthcare. This will also have an impact on the development of IoTs, where smart objects are expected to be aware of and interact with the environment. Flexible electronics have several advantages such as conformability to different shapes, which make them indispensable for the above applications. Accordingly, significant research efforts are

ongoing to develop electronic devices and systems with flexible form factors by developing novel manufacturing technologies.

1.1 Research Motivation (Context and Background)

There is a rapidly growing interest in developing flexible electronics that has enabled advancement in several emerging applications such as wearable electronics [8-10], electronic skin (e-skin) for robotics [11, 12], energy harvesting [13], Internet-of-Things (IoT) [14, 15], epidermal electronics [16], flexible display [17], health care monitoring [18, 19], and energy generation and storage [20], etc. Printed Electronics (PE) is an emerging alternative to conventional fabrication processes which is changing the way electronics are manufactured and being used. From resource efficient and low-cost fabrication of electronics over large areas (larger than the commercially available wafers), to electronics with flexible and stretchable form factors, printed electronics is changing the face of electronics in several ways. It encompasses various printing technologies including contact and non-contact with destination flexible substrate. These printing methods have led to the development of electronic devices such as transistors, displays, sensors, radio frequency identification (RFID) tags, etc. on a variety of substrates including plastics and paper that can bend, fold, stretch, or conform to curvy surfaces without losing functionality. Further, the efficient use of various materials by printed electronics technology makes it attractive in terms of reduced electronic waste (e-waste) and environmental friendliness. This is an important attribute considering the growth of Information and Communication Technologies (ICT) and digitalisation in our daily lives.

Along with the flexible form factor, many of these applications also demand high performance at par with Si-based technology leading to fast computation and communication suitable for machine-to-machine and/or human-to-machine connectivity [21]. To this end, high performance (i.e., faster response, robust, high efficiency, low-power consumption, etc.) of flexible complementary metal-oxide-semiconductor (CMOS)-based electronics is highly needed so that data can be collected, transmitted, and processed in a

fast manner [22, 23]. However, printed electronics today is not considered as a substitute for conventional Si-based electronics because of the low integration density, long switching time, and modest performance of the state-of-the-art all-printed device and circuits. The limited device performance offered by printed electronics is due to (i) the use of low-mobility materials and (ii) long channel lengths (>10 µm) of printed transistors, limited by the printer resolution. In this regard, the development of high performance printed flexible electronics demands innovations in terms of the fabrication of printable high mobility materials, design, and construction of printing technologies to integrate these high mobility materials onto flexible substrates and high resolution and throughput printers in order to meet high performance requirements.

Based on that, significant effort has been made by researchers to further investigate novel material inks, structural engineering approaches, integration/printing techniques, and fabrication processes for the development of high-performance printed electronics [10]. During the past decade, thin films of organic semiconductors [24], inorganic amorphous oxides [25], carbon nanotubes (CNTs) [26], 2D metal oxide thin films [27, 28], and transition metal dichalcogenides (TMDs), etc [29]. These materials have been widely considered for realizing printed electronic applications, such as active-matrix display drivers, wearable biosensors, bendable smartphone screens, etc [27-29]. This is because of their inherent flexibility and low-temperature materials processing, which is compatible with flexible substrates such as plastics [30, 31]. However, the modest performance achieved with devices realized based on organic semiconductors and metal oxides-based materials is not sufficient for many of the next-generation flexible electronic applications that require fast communication and computation and hence faster switching (see Figure **1.1**). For example, wireless communication in IoT, smart cities, or mHealth will require fast switching under ultra-high frequencies (0.3–3 GHz) [15]. Higher bandwidth, fast communication, and efficient distributed computational platforms with high switching speeds are necessary for smart cities and IoT, hence making high-performance requirements necessary to achieve smart connectivity among flexible objects. Since the carrier mobility of organic semiconductor materials is in the range of 0.01-10 cm^2/Vs, which is significantly lower

compared to Si-based planar devices that show mobility in the order of 1000 cm^2/Vs [32, 33], flexible high-performance electronics are being explored with novel technologies that lead to devices with performance on par with conventional microelectronic technologies. In this regard, some of the approaches followed in recent years for realizing high-performance flexible electronics include thinning silicon chips down to a few micrometres ($\leq$ 50 μm) using a range of technologies such as mechanical or chemical/mechanical polishing [32, 34-37]. Currently, silicon chips or wafers can be thinned down to 10 μm in fabrication facilities, and these chips are referred to as ultra-thin chips (UTCs) [38]. Such UTCs offer a promising avenue for implementing innovative solutions to address the increasing demands of emerging applications, including electronic skin, Internet of Things (IoT) and wearable applications. These applications require superior flexibility and high performance, making UTCs well-suited to meet their specific bendability and performance requirements [32, 34]. However, their application is limited to small and compact areas due to economic reasons and integration-related difficulties, along with complex packaging and bending due to the brittle nature and dislocation defects in the silicon. This approach is classified as a subtractive method, which means more material wastage.

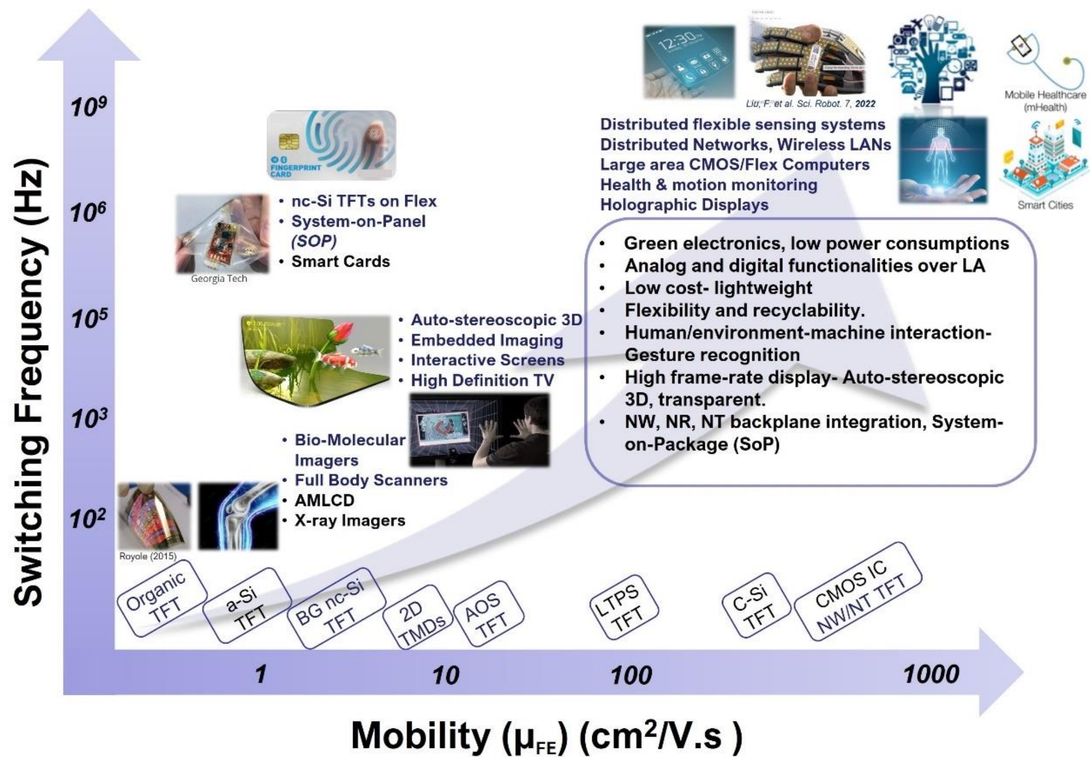


Figure 1.1: Emerging Applications Landscape enabled by High Performance Printed/Flexible Electronics, showing the Trad-off between materials mobility (μ) and transistor switching frequency.

Additionally, printed devices and circuits technologies based on one-dimensional (1D), and two-dimensional (2D) single crystal silicon and other inorganic semiconducting nanostructures (NSs) have gained significant interest due to their high mobility and other electronic, optical, high energy conversion efficiency and mechanical properties. A range of alternative solutions are being explored for high-performance flexible electronics, by employing high mobility nanostructured materials in the form of nanowires (NWs), nanoribbons (NRs), nanocones (NCs), nanomembrane (NMs), nanosheets, carbon nanotubes (CNTs), etc. However, a major challenge with NSs based electronics is that some of the critical fabrication steps (e.g., NSs fabrication/growth, selective doping, high-k dielectric deposition) require high-temperatures that are incompatible with the flexible substrates such as plastics. In traditional semiconductor fabrication, such as silicon, controlled doping methods such as ion implantation, in situ co-deposition, or doping furnaces are crucial for creating p–n junctions at defined locations [39]. These techniques enable the fabrication of electronic devices such as transistors, solar cells, photodetectors, and other fundamental components for flexible electronics. However, achieving effective

doping, such as through ion implantation requires post-implantation annealing treatment, to reconstruct the crystal and activate the implanted impurities, achieving the desired doping concentration. This annealing process typically requires very high temperatures, which poses challenges when transferring these structures to flexible substrates due to thermal budget limitations. While advanced processes for low-temperature doping, such as non-equilibrium laser-annealing methods, offer a potential solution by driving dopant atoms into the lattice without melting the plastic substrate, these methods are complex and require further investigation to ensure large-area uniformity [40]. Despite some progress in this direction, the technology is still not at a stage where large-scale integration can be considered [41].

Currently, the popular method to address this issue is to print NSs from the native or growth substrates to the receiving flexible substrate using transfer printing and contact printing [33, 42-44]. Transfer printing, particularly for inorganic NSs, is a promising method for integrating flexible structures onto flexible substrates. It allows the transfer of laterally aligned photolithography-defined arrays of inorganic semiconducting NSs from a donor rigid substrate to a target flexible substrate using elastomeric stamps. Since the high temperature fabrication steps are carried out before transfer (i.e., when NSs are still on the native or growth substrates), this method decouples the high temperature process steps from the low-temperature steps (e.g., metallisation) that are carried out after transfer to realise devices on flexible substrates. In addition to this, the development of flexible and printed electronics based on inorganic materials is an emerging field that aims to create devices with novel form factors and features to meet the demands of emerging high performance flexible applications such as wearable electronics, deformable displays, conformable biosensors, electronics skin (e-skin) for robotics, Internet-of-Things (IoT), etc. A crucial step in the realisation of these novel electronic applications relies significantly on integration of inorganic materials with polymeric substrates as well as fabrication process limitations. For such applications, electronics based on inorganic nanostructures from high mobility materials such as single crystal silicon and compound semiconductors (E.g., GaAs, GaN,

InGaAs, etc.) in the form of NMs, NRs, etc., offer promising high-performance solutions compared to conventional organic materials [45-48].

The controllable and reproducible transfer of NSs from the donor to the receiver substrate is critical for large area electronics (LAE), thus precise control over the interface properties (stamp/donor and stamp/receiver) is required during transfer printing. It is challenging to have complete control over printing parameters (e.g., retrieval/pick up velocity, adhesion switchability, stamp surface recovery, etc.) and interface properties and as a result, it is difficult to obtain high yield and reproducibility. This is due to the viscoelastic properties of soft stamps, which may cause unexpected tilt, orientation, and buckling of NSs under applied force during the printing process. Further, it is challenging to print sub-100 nm thick NSs using conventional transfer printing. This is because at such thicknesses the strain energy release rate at the stamp/NSs interface decreases with respect to the NSs/substrate interface, which leads to lower printing yield. Few attempts have been made to address these challenges with modified transfer printing involving surface morphology, interface engineering, thermal modulation and kinetically controlled velocity, magnet-controlled, and laser-driven method, etc. These modified transfer printing methods improve the yield and reliability of the process. These modified transfer printing methods have shown good potential for flexible electronics, but they also require additional excitation equipment such as a laser system, and magnet actuating system, etc. In this regard, it is highly desirable to develop a precise transfer printing process that enables higher transfer yield, excellent registration, and compatibility with roll-to-roll (R2R) printing without adding complex printing equipment.

1.2 Objectives and Key findings

The deterministic integration/printing of advanced classes of single crystalline inorganic/compound semiconductor based NSs on a flexible substrate has not been widely explored to fabricate high performance flexible electronics. This is a result of temperature limitation and relative fragility of the active material. It is critical to use the high-mobility materials to attain performance (at par with today's silicon-based electronics) needed to

meet fast computing and communication requirements (i.e., 500MHz-1GHz) of many applications (e.g., IoT, wireless implants, epidermal sensors, wireless sensing networks, etc).

This research has the following objectives and key findings:

- Demonstration of inorganic material fabrication of high mobility and high energy conversion efficiency nanostructures and show the electrical properties of inorganic semiconductors that can be retained when the material structures are transferred to a flexible substrate. Single crystalline inorganic materials (primary silicon) and compound semiconductors (GaAs) are the material of choice for this research, especially when it comes to realising high performance flexible electronics. In this context, compound semiconductors could open new avenues for power electronics on flexible substrates.
- Illustration of conventional transfer printing of these nanostructures to the desired flexible substrate using an elastomeric stamp. Thus, the demonstrated fabrication step allows the transfer printing process to be very robust for the development of flexible high-performance devices, by decoupling the high temperature process step (e.g., selective doping) from the low temperature step (e.g., metallisation) that are carried out after transfer to realise devices on flexible substrates. Followed by the advancement of conventional transfer printing toward roll-printing for integrating arrays of high mobility nanostructures directly on the bendable substrate without using an intermediate stamp. As a result, excellent transfer yield, higher registration accuracy, less material wastage can be achieved.
- Development of a low temperature CMOS compatible process for the fabrication of high-performance top gate Si NRs based FETs in thin format on flexible substrates. This entails the integration process of Si nanoribbons and process development for a free residue printing process on a polymer substrate for dielectric deposition and electrode deposition.
- To apply the above technology as a means to realise flexible CMOS based electronics with a performance at par with today’s silicon-based electronics. For those advanced applications to meet high efficiency and low power consumption requirements for flexible

electronics such as mHealth, IoT, etc., among some of the following components are needed such as n- and p-channel transistors, solar cells, photodetectors, energy harvesting devices, antennas, etc.

1.3 Scope and Structure of the thesis

This thesis covers the aspects highlighted in the previous section and is arranged into seven chapters plus appendix. During the development of the integration method for transferring high mobility and high energy conversion efficiency nanostructures on flexible substrates for realizing flexible electronics, several other meaningful findings were obtained. These include the structural design of the nanostructures, selective doping of silicon using a thermal diffusion process, and the development of a low-temperature CMOS-compatible process that uses high-quality room temperature (RT) deposited dielectric (SiN_x) for realizing high-performance top-gate Si nanoribbon-based transistors. Additionally, several studies were conducted to investigate the pros and cons of utilizing the conventional transfer printing process for realizing electronic devices on bendable substrates. This includes the process limitation toward achieving high-performance complementary CMOS logic circuits. Based on that, the direct roll transfer printing method was optimized to integrate arrays of high energy conversion efficiency nanostructures such as Si nanoribbons and GaAs wires in a single step on a variety of flexible substrates. Consequently, significant improvements were achieved in terms of the accuracy of printed structures and excellent transfer yield over a large area. This Ph.D. thesis covers the studies mentioned above, and each chapter provides a brief description of its content to give a detailed overview of the research.

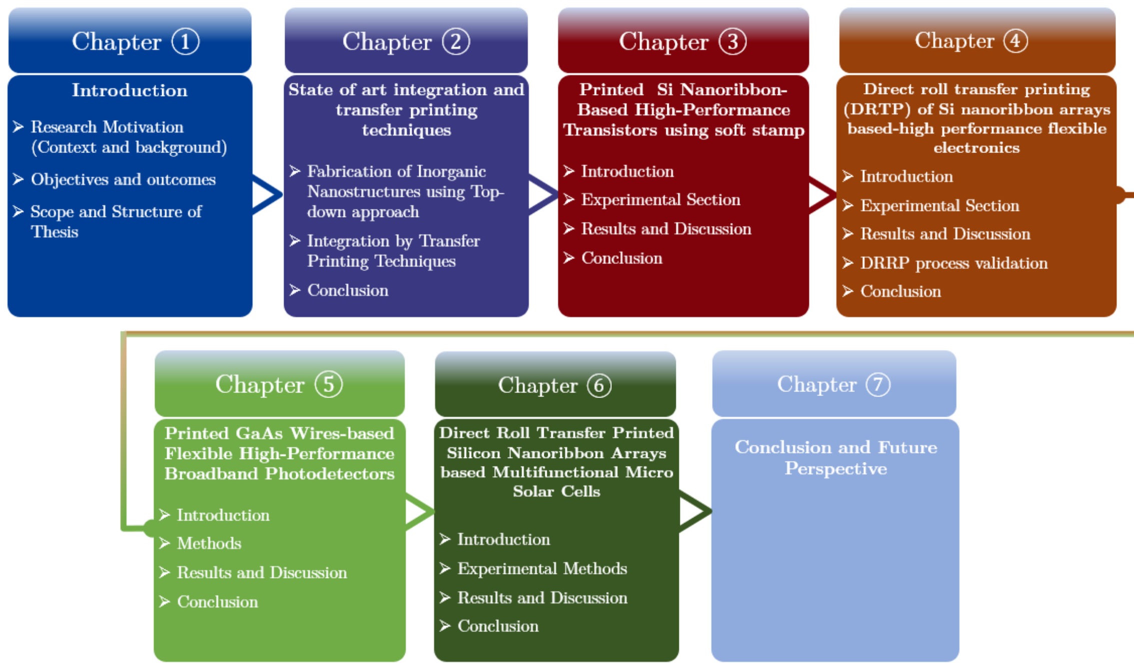


Figure 1.2: Organisation of thesis chapters

Organisation and content of the thesis are as follows:

Chapter 2 presents an overview of the state of the art and recent advances in transfer printing techniques to integrate NSs in a high mobility inorganic semiconductor. Initially, this chapter summarises the aspects of releasing high mobility inorganic semiconductor nanostructures. These are formed by using “top-down” methods to achieve the desired mechanical flexibility of these nanostructures prior to integrating them onto flexible substrates. This includes highlighting the donor wafers, synthesis and fabrication strategies adopted for releasing a printable form of nanostructures; nanoribbons (NRs) or nanomembranes (NMs). These could be utilised for the transfer printing process and integration over flexible substrates. This chapter explores both conventional and advanced printing techniques for integrating nanostructures onto flexible substrates. Advanced techniques such as bio-inspired transfer printing, which uses soft elastomers adapted from geckos and aphids, are also discussed. Room temperature processing on flexible substrates is crucial to realise flexible electronics and circuits. The transfer printing methods presented in this chapter are classified based on their basic approach concept and working principles. A comparison among advanced transfer printing techniques in the literature is made to classify their advantages and disadvantages in terms of transfer printing performance,

followed by a brief summary. The review described in this chapter established the foundation for the following work presented in this thesis, which aims to integrate nanostructures generated from inorganic semiconducting materials such as Si, GaAs, etc. Such a material can provide a combination of high efficiency, high mobility, and excellent stability.

Chapter 3 presents a complete low-temperature compatible process for releasing high-performance flexible devices on flexible substrates using conventional transfer printing with a soft elastomer stamp. The approach involves integrating a releasable form of Si NR arrays from their source wafer onto a flexible substrate, demonstrating great potential for achieving high-performance flexible electronics. The chapter provides a detailed study of the fabrication and characterization of Si NR-based field-effect transistors (FETs), including the development of a selective doping process using thermal diffusion in silicon on an insulator (SOI) thin film through a spin-on-dopant process (SOD) to optimize the desired final doping concentration. Additionally, a high-quality silicon nitride (SiNx) gate dielectric deposited at room temperature (RT) is investigated. The work demonstrates the potential of both n-type and p-type transistors operating with comparable performance to the state-of-the-art. The impact of cyclic bending on device performance is evaluated, and the device characteristics are compared with previous works based on Si-membrane/ribbon-based devices with best-reported performance for various dielectric materials. The RT process used in this work is compatible with low-temperature polymer substrates, which could potentially lead to large areas of flexible electronics over polymer-based flexible substrates.

Chapter 4 presents a novel printing technique and Roll-To-Roll (R2R) compatible process developed based on direct roll transfer printing. The chapter starts by describing the proposed integration approach, which is classified as a simple, cost-effective, and robust direct roll transfer printing technique. The chapter demonstrates the capability of the proposed printing process using a custom roll system, including large area transfer printing of Si nanoribbon (NR) arrays (≈70 nm) directly onto the target substrate and integration over multiple flexible substrates. The chapter provides a detailed study of the transfer printing capabilities, such as transfer yield, registration accuracy, printing quality, etc., and

compares them with the results obtained from direct roll transfer printing. The morphology and structural characterization of the transfer printed Si NR arrays are studied using Scanning Electron Microscopy (SEM) and Atomic Force Microscopy (AFM). This section also covers a discussion of perspectives and challenges for realizing high-performance electronic circuits. Finally, the printing system's efficacy is demonstrated by the electrical characterization of high-performance n- and p-channel transistor devices over fully flexible substrates. The Si NRFETs were developed using a low-temperature CMOS compatible process, which allows the direct adoption of direct roll transfer printing techniques for developing energy-efficient, high-performance, and flexible complementary CMOS circuits. The obtained results show great potential and open an exciting new avenue for achieving energy-efficient and high-performance flexible electronics.

Chapter 5 describes the process adopted for releasing integrated arrays of laterally aligned GaAs microstructures, using semi-insulating (undoped) and doped GaAs bulk wafers as source material. The chapter also presents the optimisation of the process for developing high-performance flexible broadband photodetectors using direct roll transfer printing techniques. The performance of the devices has been systematically evaluated under a wide range of illumination wavelengths (UV and NIR), and the electrical characterisation and mechanical stability of the flexible GaAs photodetectors are presented.

Chapter 6 covers various methods for producing flexible solar cells based on inorganic micro/nanostructures. Specifically, this chapter focuses on the fabrication of multifunctional solar cell devices using ultrathin silicon nanoribbons. To achieve this, the chapter outlines the fabrication process and integration approach that I developed using the direct roll transfer printing technique. Additionally, the chapter includes a systematic investigation of the device's performance under visible-UV-NIR light illumination, as well as the electrical characterization and mechanical stability evaluation of the flexible multifunctional Si solar cell. By detailing these aspects, this chapter provides valuable insights into the fabrication and performance of flexible solar cells based on inorganic micro/nanostructures.

Chapter 7 summarizes the key findings of the research presented in this thesis and suggests some possible directions for future studies.

Chapter 2.

State of the art of transfer printing techniques to integrate inorganic nanostructures

The transfer or microcontact printing represents a set of techniques that enable the integration of nano to chip scale electronic structures into organised arrangements from a donor substrate to a receiver substrate [33, 47, 49]. Traditionally, the approach provides a way to pattern metal structures, but later the technique gained interest to assemble microelectronic chips/dies over rigid as well as flexible substrates, enabling 'heterogeneous integration' [49, 50]. Considering the nature of the process, they are termed as "pick-and-place" approaches in which a soft elastomeric stamp is conventionally employed as an intermediate tool to facilitate the transfer process. The printing or releasing step of inks, particularly the inorganic nanostructures from the stamp onto the receiving substrate is more complicated than picking up from the donor. Several transfer printing methods are developed using adhesive/glue or tunable/reversible adhesive modulation strategies [47, 51, 52]. The modified approaches have been successful in the transfer of inorganic nano/microstructures on flexible substrates [45, 53, 54].

To examine the full potential of the recently reported transfer printing techniques towards realising flexible inorganic-based electronics, it is important to understand the basic working principles and the mechanism of different techniques. A variety of advanced transfer printing methods have been proposed and demonstrated. This chapter is dedicated to the description of the conventional transfer printing mechanism to integrate inorganic micro/nanostructures mainly onto compliant (flexible) receiver substrates. Further, the chapter will summarise the working principles of a few representative methods of modified versions of transfer printing techniques including the advantages, disadvantages, and key challenges of each technique. Integration strategies based on different transfer printing

techniques will be described and compared for large-scale integration of inorganic nanoscale structures and different parameters that control the registration, uniformity, and yield of the printing process. To this end, the recent development of transfer printing techniques is summarised and classified under two categories based on the underlying mechanism: 1) Stamp based transfer printing techniques, 2) Bio inspired transfer printing techniques. Lastly, some interesting devices and applications include field effect transistors, photodetectors, and solar cells are presented using inorganic micro/nano scale transfer printed structures. These are realised from high mobility and high energy conversion efficiency material such as Si and GaAs. Before describing the printing mechanism, the first section of the chapter will present the synthesis of micro/nanostructures toward realising high performance and energy efficient flexible electronics.

2.1 Fabrication of Inorganic Micro/Nanostructures using Top-down approach

The research work in flexible electronics over the past decade has demonstrated that materials can provide a potential route toward realising active electronics on polymeric substrate at low temperature using printing techniques [14, 24, 55]. However, there are several flexible electronic applications that are restricted by the performance limitation of these materials [9, 10]. Recently, most of the research in the flexible electronics field aims to address this limitation by exploring various strategies to use high quality inorganic semiconductor material to generate bendable structures such as nanoribbons/nanowires [10]. These can be released from their donor wafer, transferred, and printed on the destination substrate. The top-down approach using lithography and chemical etching processes is one of the techniques for realising these printable structures [56]. In this context, many inorganic semiconducting materials exhibit high mobility, excellent energy conversion efficiency with good stability [25, 33, 55]. The main bottleneck for obtaining active electronics on low temperature polymeric substrates such as plastic, is that realising high quality layers of these material along with the associated microelectronics processing steps (e.g., oxidation, dialectic deposition, selective doping, etc) toward final device fabrication.

These require a high temperature that exceed the thermal decomposition temperature of the flexible substrates and/or glass-transition temperature [57, 58]. In this regard, research progress in the last several years has led to establishing the foundation for developing several methods that avoid such limitations.

In this section, a brief description of the synthesis methods for obtaining functional micro/nanostructures in printable and bendable form (e.g., NRs, NMs, etc.) using top-down approaches will be presented. The top–down synthesis route to realising nano/microstructures is attractive owing to better uniformity control with excellent alignment and registration accuracy as compared with the bottom–up synthesis. These attributes are essential to ensure uniform and repeatable device performance over large areas. The fabricated structures are formed from high mobility and energy efficient inorganic materials such as Si, GaAs, etc. These structures can be employed as active building blocks to realize high-performance and large-area flexible electronics.

2.1.1 Releasing printable micro/nanostructures from bulk wafers

To achieve flexibility in electronic devices, one straightforward approach is to use micro to nanoscale semiconductors with thicknesses ranging from tens of nanometers to a few micrometers integrated over ultrathin substrates, which enable bendability while maintaining high performance [32, 34, 37]. Previous studies have extensively investigated the mechanical properties, underlying physics and fabrication processes of 2D nanostructures, such as nanomembranes, realised from inorganic nanomaterials [59, 60]. Recent advancements in synthesis techniques have enabled the creation of nanomembranes with exceptional properties and diverse configurations. Some of these configurations take advantage of quantum and other size-dependent effects, further enhancing their potential for various flexible applications. Additionally, the development of integration methods has further expanded the possibilities in nanomembrane research [46, 61]. The top-down method is a promising strategy for obtaining horizontally aligned, loosely bound nano to micro scale inorganic structures, which can be achieved from high quality single-crystalline bulk wafers such as Si or GaAs [62]. Fabricating printable structures from bulk wafers typically involves

photolithography and etching processes to define micro and nano scale structures with high dimensional control and maintain the arrangement and alignment of the fabricated structures [63-66]. One example of this process involves defining anchor points and trenches of ribbon/bars on the top surface of a bulk wafer with <111> orientation, followed by preparing the substrates for anisotropic chemical etching along the <110> directions [64]. Figure 2.1 depicts the schematic representation of the fabrication procedures involved in achieving the flexible form of micro-nanostructures, such as ribbons or membranes, from a bulk Si wafer [65, 67, 68]. The process begins with conventional photolithography steps and patterning to define the lateral dimensions of the ribbons that are connected together to form an array, but with a separation region of >10 µm to allow the etching solution to access underlying regions. Plasma etching using a reactive ion etching tool is performed on the exposed Si regions in a direction perpendicular to the Si surface <110> to define the thickness of the ribbons/bars and to enable subsequent steps related to anisotropic etching of the underlying region. After the passivation step, the realisation of these structures from their bulk wafer is carried out by immersing the substrates in hydrofluoric (HF) etchant solution, where undercut etching of structures in the <110> direction is performed.

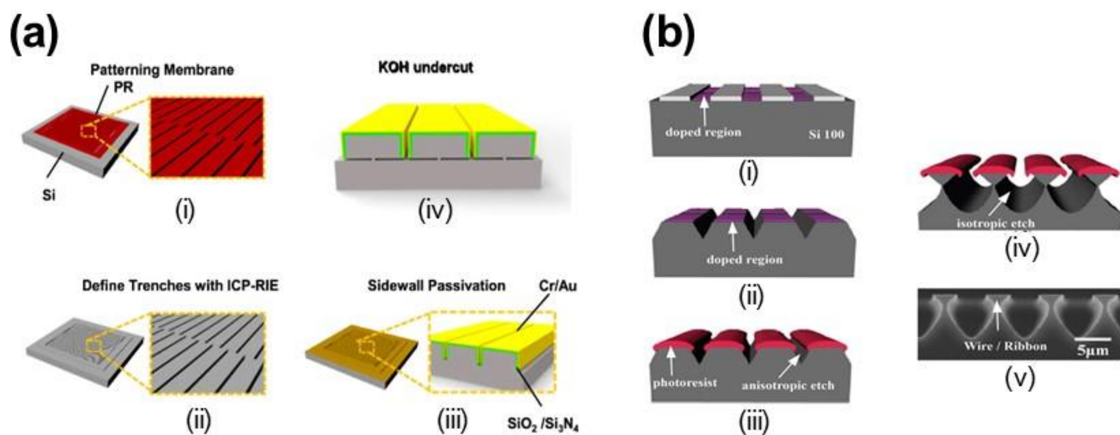


Figure 2.1: **(a)** Schematic representation of fabrication steps using top-down approach to form ultrathin Si nanoribbons/nonmembrane from bulk silicon (111) wafer: (i) defining photoresist patterns on Silicon (111) wafer; (ii) Anisotropic reactive ion etching (RIE) the Si nonmembrane (NMs) to define the trenches using photoresist as an etch mask; (iii) passivating the square side walls of the NMs structures using SiO_2/Si_3N_4 and evaporated Cr/Au; (iv) anisotropic etching of exposed (unprotected) silicon with KOH performed in contuse manner to perform undercut etching releasing flexible free standing ultrathin structures of NRs/NMs from Si bulk wafer [67]. **(b)** Alternative

approach of releasing Si wires from bulk Si (100) wafer using photolithographically controlled, top-down method where the photoresist is selected as an etchant mask for defining the Si wires trenches as well as during isotropic RIE process [63].

2.1.2 Releasing printable micro/nanostructures from epitaxial grown wafer

The top-down approach could also be used to fabricate ultrathin NSs using high quality wafers designed with epitaxially grown thin multi-layers on bulk material, where these layers can be selectively etched in order to facilitate the releasing step [33, 58, 69]. A thin film wafer with multiple layers such as silicon-on-insulator (SOI) is commonly used to fabricate Si NSs. The SOI wafers are commercially available and can provide high quality NSs with thickness ranging from a few tens' nm to µm and lateral dimensions between a few tens of µm to cm as defined by the lithography mask. The fabrication scheme of releasable ultrathin silicon nanoribbon (Si NR) using SOI wafer is presented in Figure 2.2a. The thickness of the active Si layer can vary from 5nm to a few microns. The Si NR's geometry (length and width) can be defined using conventional UV or e-beam lithography (step ii). Next, anisotropic wet or dry etching of selected exposed regions on the top side of the Si wafer is carried out, and then undercut removal of the BOX with hydrofluoric acid to achieve loosely bound Si NRs structures. This technique produces horizontal aligned arrays of NRs over SOI source wafers, and these are eventually transfer printed over flexible substrates. Many compound semiconducting materials including GaAs [70], GaN [71, 72], InAs [73] and InP [74] have been obtained in a conceptually similar manner to that of Si shown in Figure 2.2a. However, the dimensional control of the printable structures with SOI wafer and other epitaxial grown wafers are much better compared to bulk wafers, therefore the capability to realise highly thin flexible electronics through this technique is much higher compared to generating nanostructures from bulk wafers [56, 65]. In another example, using multi-layered wafer of GaAs/AlAs/SIGaAs can also provide a reliable substrate as a source material that can be used to generate functional flexible structures. Where the GaAs micro/nanostructures can be generated by selective removal of the sacrificial layer (AlAs) with HF etching [70]. Figure 2.2b shows an illustration of the fabrication process of ultrathin structures of GaAs nanomembranes (NMs) with thickness around 200nm released from

GaAs and AlAs stacks on a bulk GaAs wafer by selective HF etching [70]. The epitaxial transfer method was employed for integration of the ultrathin nanoribbon (~18nm thick) of single crystal InAs by using an epitaxially grown wafer with multilayers (InAs/AlGaSb/GaSb) as shown in figure 2.2c, the InAs nanoribbons can be released from their donor wafer by etching the sacrificial layer (AlGaSb) selectively using hydrofluoric acid [75, 76]. In this context, these multi-layered wafers (e.g, SOI, GaAs/AlAs/SIGaAs, InAs/AlGaSb/GaSb, AlGaN/GaN/AIN/Si, etc.) can be patterned selectively based on the desired geometries using various etchant masks e.g., photoresist, SiOx, SiNx, PMMA, etc. and then followed by chemical etching to remove the sacrificial layer (e.g. SiO_2 for SOI, AlAs for GaAs/AlAs/SIGaAs, AlGaSb for InAs/AlGaSb/GaSb and Si for AlGaN/GaN/AIN/Si) as shown in figure 2.2d [72]. Herewith allowing the integration of micro to nano structures in form of ribbons, wires, membranes, etc. to be transferred from the source wafer onto the destination substrate.

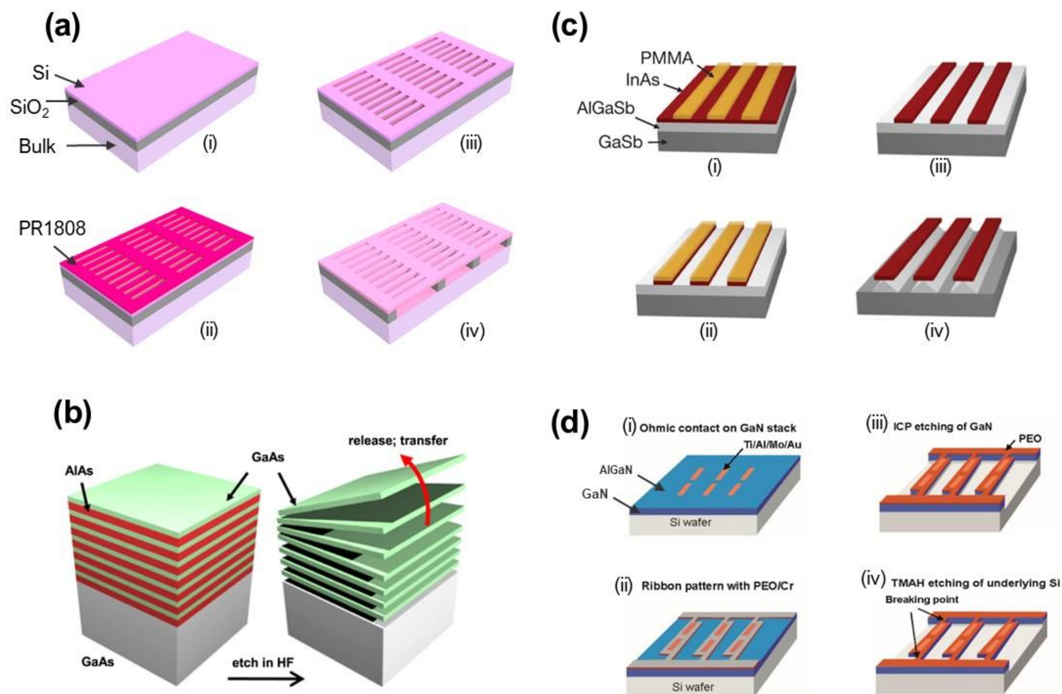


Figure 2.2: **(a)** Schematic illustration of the top-down fabrication approach for generating ultrathin arrays of Si nanoribbon using SOI wafers as donor substrate. **(b)** Schematic representation of epitaxially grown multilayers of GaAs and AlAs on bulk GaAs wafer and procedures for releasing ultrathin structures e.g., NRs and NMs of GaAs by selective etching of the sacrificial layers of AlAs [70]. **(c)** Fabrication scheme of InAs nanoribbons generated from the epitaxially grown wafer (InAs/AlGaSb/GaSb). (i) (Polymethylmethacrylate) PMMA ribbons were patterned by photolithography process (ii) the trenches of InAs nanoribbon arrays were defined by selective

chemical etching using PMMA as etchant mask. (iii) PMMA patterns removal. (iv) the subsequent step is performed to release a printable and flexible form of InAs nanoribbons by etching the underlying material or the sacrificial layer of AlGaSb [73]. **(d)** Fabrication processing steps of microscale GaN ribbons toward realising flexible form of high electron mobility transistors (HEMTs) on plastic substrate, the multi-layered wafer (AlGaN/GaN/AIN/Si) was employed as a source substrate generating microscale GaN ribbons. The final step of forming a printable structure of GaN ribbons was performed by wet etching the underlayer Si layer [72].

Recent reports have demonstrated the realization of different classes of flexible electronic devices, such as field-effect transistors, solar cells, photodetectors, and other functional devices, using printable inorganic micro/nanoscale structures such as ribbons, wires, platelets, bars, etc. These functional bendable electronics exhibit high electrical performance, energy efficiency, cost-effectiveness, and excellent flexibility [68].

2.2 Flexible substrates for printed electronics

Polymeric substrates offer highly promising solutions for applications that require high bendability, thermal stability, and emissive properties. These materials offer a balanced combination of physical, chemical, thermal, and mechanical characteristics, as detailed in Table 2.1. Moreover, polymeric substrates fulfill the criteria for cost-effective flexible electronics, enabling Roll-to-Roll (R2R) manufacturing [77, 78]. To replace traditional planar rigid substrates, flexible substrates must possess specific properties, including dimensional stability, thermal stability, low coefficient of thermal expansion (CTE), excellent solvent resistance, and effective resistance against moisture and gases. In the context of transfer printing, ensuring the successful and reliable integration of micro and nanostructures is highly dependent on the suitability of the receiving substrates. Some key material properties that indicate the suitability for transfer printing are:

- Mechanical Flexibility: Receiving substrates should be mechanically flexible to accommodate the deformation and bending during the transfer process without damage or delamination of the printed structures.
- Surface Smoothness: Smooth surfaces are essential to ensure good contact and adhesion between the stamp and the receiving substrate during the transfer process, preventing defects and alignment issues.

- Surface Energy: Receiving substrates should have appropriate surface energy to facilitate strong adhesion between the printed structures and the substrate surface.
- Thermal Stability: Thermal stability is crucial, as some transfer printing processes may involve elevated temperatures during curing and integration steps.
- Chemical Compatibility: The receiving substrate material should be chemically compatible with micro-fabrication processes such the aqueous development and water-based processing during UV photolithography inks or micro/nanostructures to prevent undesirable interactions or reactions with material substrate.
- Low Defect Density: Receiving substrates with low defect density ensures high-quality transfer of structures without interference from substrate defects.

Table 2.1: Comparison of flexible polymeric substrates [77-79].

Substrate	PI	PET	PEN	PC	PS
Tg (°C)	270	70	120	145	203
Upper Tm (°C)	250–320	115	268	115-160	180-220
Y. Modulus	2.5	2–2.7	0.1–0.5	2.6	-
CTE (ppm/°C)	8–20	33	20	75	54
Water absorption (%)	2–3	0.6	0.4	0.25	1.4
Solvent resistance	Good	Good	Good	Poor	Poor
Surface roughness	Good	Poor	Poor	Good	Good
Dimensional stability	Fair	Good	Good	Fair	Fair

Tg: glass transition temperature, Tm: melting temperature, CTE: coefficient of thermal expansion.

Among the common materials used as receiving substrates for printed electronics are flexible polymer films, including polyimide (PI), polyethylene terephthalate (PET), polyethylene naphthalate (PEN), polycarbonate (PC), and polystyrene (PS). Ensuring the mechanical flexibility, surface smoothness, appropriate surface energy, thermal stability, chemical compatibility, and low defect density of the receiving substrates is essential for successful integration of micro/nanostructures on bendable substrates. Making the appropriate

selection of receiving substrate with the desired material properties is crucial for achieving successful transfer printing and integration of micro/nanostructures on flexible substrates.

2.3 Integration by Transfer Printing Techniques

The concept of transfer printing was first introduced in 1993 by the Whitesides Research Group to produce well-defined features of gold [80]. The reported technology begins with the patterning of a self-assembled monolayer (SAM) on a gold substrate using an elastomer stamp, followed by selective etching in an aqueous, basic solution of cyanide ion and dissolved dioxygen (Figure 2.3). However, integrating high mobility semiconducting materials with polymeric flexible substrates, requires processing temperatures below the glass-transition or thermal-decomposition temperatures of the flexible substrate. Figure 2.3 shows various steps involved in the reported transfer printing/integration approach. Since the first report, huge efforts both from academic and commercial research have extended the capabilities of transfer printing to print a wide range of materials as well as the patterning of varied materials [49, 52, 57, 58, 81]. Thereby, the technology has evolved into a practical approach to transfer micro to chip scale structure over rigid/compliant substrates providing an efficient route to implement heterogeneous integration. In the last decade, intensive efforts have been made to develop modified transfer printing techniques for the heterogeneous integration of diverse functional nanostructured materials (thickness <100nm) from their grown substrates onto receiving substrates [52, 57, 58]. Thanks to the advancement in developing various modified transfer printing techniques which have allowed proof-of-concept functional systems on compliant substrates which has led to new avenues in various applications such as high-resolution rollable displays [82], flexible high-speed optoelectronics [64], energy conversion devices [83], bio-integrated electronics [84], transient electronics [85, 86], and many other advanced applications. These devices have shown potential but are still at a nascent stage of development and thus, far away from commercialisation.

This chapter will present state of the art printing/integration techniques which facilitate the transfer of functional inorganic micro/nanostructures onto flexible substrates to enable

the realisation of high performance flexible inorganic semiconductor-based devices and optoelectronics ranging from high performance field effect transistors to energy efficient solar cell and photodetectors. Different transfer printing techniques will be discussed for efficient transfer of these inorganic elements. Different strategies of advanced integration developed employing transfer printing techniques will be presented in the following sections. Before we discuss the transfer of nano and micro scale inorganic structures, the following section briefly presents the fabrication process to realise them by using high mobility and energy efficient inorganic material as a source element.

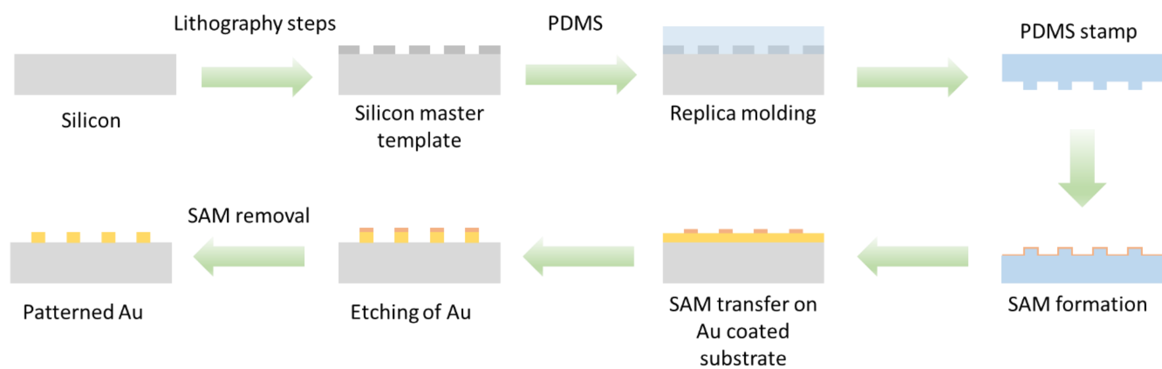


Figure 2.3: Schematic description of crucial steps for conventional micro-contact printing (MCP).

As one of the most promising technologies that have been used to integrate high quality single crystalline semiconducting micro/nanostructures for realising functional flexible devices, transfer printing has been extensively explored [33, 46, 49]. Thus, the development of integration techniques to integrate bendable structure forms of inorganic semiconducting materials such as Si, GaAs is highly required to meet the growingly technological demands for futuristic flexible electronics application, where high performance and high energy efficiency is needed [83, 87]. In this context, micro/nanostructures of Si and GaAs are attracting immense interest as promising materials for advanced energy conversion applications, due to their unique structural, optical, electrical, and thermal properties. Additionally, Si and GaAs have a band gap of 1.1 and 1.42 respectively, close to the value reported peak solar cell efficiency [88]. In the following section, a description of the transfer

printing techniques including conventional and advanced approaches for integrating inorganic micro/nanostructures is presented.

2.3.1 Operating principle of conventional transfer printing

The transfer printing technology was mainly explored to overcome the manufacturing problems (e.g., thermal budget issues) associated with the use of conventional microfabrication processes on natively flexible substrates such as plastics [12, 49, 58]. Most of the polymeric flexible substrates have limited stability under harsh fabrication processing steps such as annealing at higher temperatures (>200 °C), vacuums, wet etching using extreme basic/acidic solutions, etc [49]. The concept is depicted schematically in Figure 2.4. The conventional microfabrication steps that require high temperatures, etching, etc. are first carried out on a rigid wafer (described in section 2.1), which has high stability under harsh processing conditions. The microfabrication process yields micro/nanostructures which could be subsequently transferred over the flexible receiver substrate using the transfer printing process. As shown in the Figure 2.4, fabricated structures are 'picked or detached' (step 1) from the donor wafer and 'placed or attached' (step 2) to flexible substrates, where further low-temperature device fabrication steps are carried out to finalise the electronics device/system.

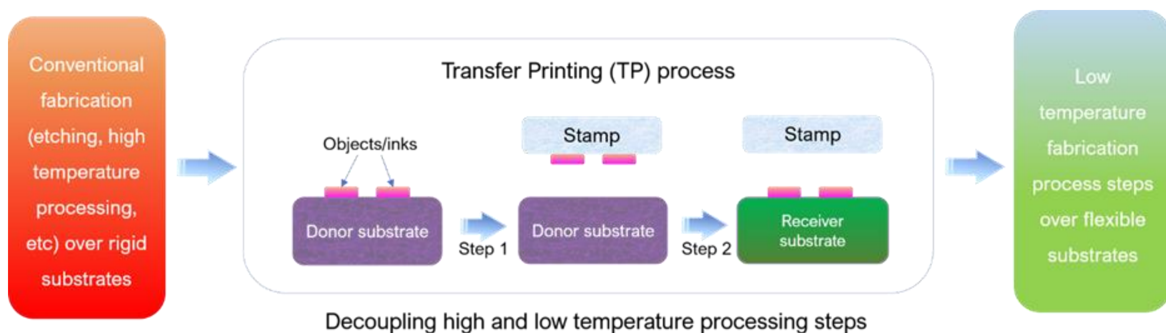


Figure 2.4: Schematic illustration of the concept and mechanism of transfer printing. The figure also shows the overview of transfer printing approach enabling transition from high to room temperature processing steps. Reprinted from the Ref. [49].

The printing mechanism is as follows: To transfer the fabricated micro/nanostructures from their rigid donor wafer, a soft elastomeric stamp (generally made of poly(dimethylsiloxane)

(PDMS)) is gently applied to the fabricated structures. The soft nature of the stamp with optimised applied contact force leads to a conformal contact between the stamp and ink/structures. The bonding between structures and stamp are governed by Van der Waal forces [89, 90]. The mechanism of integration of micro/nanostructures by transfer printing can be understood by investigating the competing interfacial fracture between the structures/stamp and stamp/structures. In step 1, Figure 2.4 i.e., retrieval process, the stamp/structures interface must have stronger adhesion strength than the structure/substrate interface energy. On the other hand, during the printing step 2, as shown in Figure 2.4, the stamp/structure interface should be weaker. To achieve reproducible integration of structures, precise control over interface properties (stamp/donor, stamp/structures, and stamp/receiver) is necessary for transfer printing. It is generally assumed that the adhesion strength at the micro/nanostructure's substrate interface is not influenced by the applied force/stimulus and does not play an important role during the printing process. Therefore, precise control over the micro/nanostructures stamp interface is key to a successful printing. Because of the viscoelastic properties of soft stamp such as PDMS, unexpected tilt, rotation, and even buckling and drop of structures during the transfer printing process are very common [52, 83]. This leads to poor transfer yield. Moreover, registration issues of printed structures could be dominant. These challenges are more common and could arise particularly during the transfer of nanoscale structures and UTCs hence require fundamental, innovative advances in printing process mechanism and materials engineering to develop a printing process which allows the transfer of high-quality semiconducting structures with a wide dimension range (nano to chip scale) with satisfactory transfer yield and in a controlled manner over large areas to meet high performance flexible electronics requirements [49, 91]. In this regard, many advanced and modified transfer printing techniques have been developed. These are described in the following section.

2.3.2 Stamp based transfer printing methods:

2.3.2.1 Surface treatment and adhesive assisted transfer printing technique

Toward realising high performance and efficient flexible electronics, improving the adhesion switchability is crucial to ensure the reliability of the pick-up process to transfer the structures/inks from their donor substrate and followed by the printing/releasing them on the receiving substrate. Surface interface modification or adhesive assisted transfer printing techniques have been employed to assist the modulation of the interfacial adhesion strength [42, 92-94]. Traditionally, elastomeric stamps are widely employed in most reported transfer printing processes, especially for transferring inorganic micro/nanostructures from their rigid source material onto flexible substrates. So, after realising the structures/inks on the source wafer, the sufficient adhesion strength between the stamp and the structures is required to allow the structures/inks to be picked up via intermediate stamp, and this only occurred through the chemical bonding between silicon and oxygen atoms (Si-O-Si) between the PDMS stamp and SiO_2 film [42, 56, 95] via a condensation reaction [96]. In this context, to reach strong bonding energy and achieve sufficient adhesion to conduct the retrieval process of the micro/nanostructure from their source material such as GaAs, GaN, etc., [48, 71] the PDMS stamp is oxidised slightly along with coating a thin film of SiO_2 on the target structures/inks. The SiO_2 is used as a bonding layer on the releasable structures, due to its electrical insulation property and high bonding strength that it exhibits during contact with soft stamps e.g., PDMS, even at room temperature. This approach was adapted to integrate different dimensions of bendable and stretchable semiconducting structures on PDMS substrate [97]. Another approach to increasing the interfacial adhesion for the printing step is to coat the receiving substrate with a thin layer of adhesive in an uncured or semi-cured state [52, 91, 93]. Several printing techniques adopted for conventional transfer printing using elastomeric stamps, employ uncured or semi cured adhesive [42, 53, 93, 98] to increase the bonding energy between the receiver and structures to facilitate the printing step before curing the adhesive fully (Figure 2.5b, c). This step is usually carried out by applying heat or UV exposure [98, 99]. However, the selection of an appropriate UV-curable adhesive is critical. Several types of adhesives, such as photoresist SU8, epoxy and adhesive tapes have

been employed in transferring inorganic micro and nanostructures [94-96], However, to enhance the controllability over the interfacial delamination steps during the printing step, the use of a thermal stage or UV source is being explored to allow for precise control over printing process [94-96]. For instance, the utilization of UV curable adhesives facilitates accelerated printing, reducing the overall duration of the process [100]. The curing time of the UV curable adhesives can be adjusted to accommodate different substrates, providing flexibility in the printing process. In this regard, it is essential to be aware of the limitations associated with these adhesives, particularly the generation of residues and contamination during the transfer process, must be carefully considered. These residues can adversely affect device performance by compromising the interfaces within the device structures. Moreover, the curing conditions of the adhesive need to be optimized carefully to assist the transfer yield during attachment and the detachment steps between the structures/inks and soft stamp. Optimization of curing conditions contributes to improved adhesion strength and efficient transfer, thereby enhancing the overall performance of the transfer printing process. The careful selection and optimization of UV curable adhesive plays a crucial role in minimizing potential issues and maximizing the advantages of transfer printing techniques. When dealing with the transfer of nanostructures fabricated from compound semiconductors such as GaAs, GaN, it is necessary to add an additional layer of SiO2 to enhance the chemical bonding and interfacial adhesion between the stamp and the structures [42, 89]. This additional layer may introduce complexities to the process and lead to defects on the printed structures. Additionally, integrating the structures on the receiving substrate may require multiple intermediate stamps, potentially resulting in contamination from glue/adhesive and/or stamp residues and increased material wastage. Addressing these challenges becomes crucial in achieving successful transfer printing of nanostructures fabricated from high-mobility materials such as silicon and compound semiconductors.

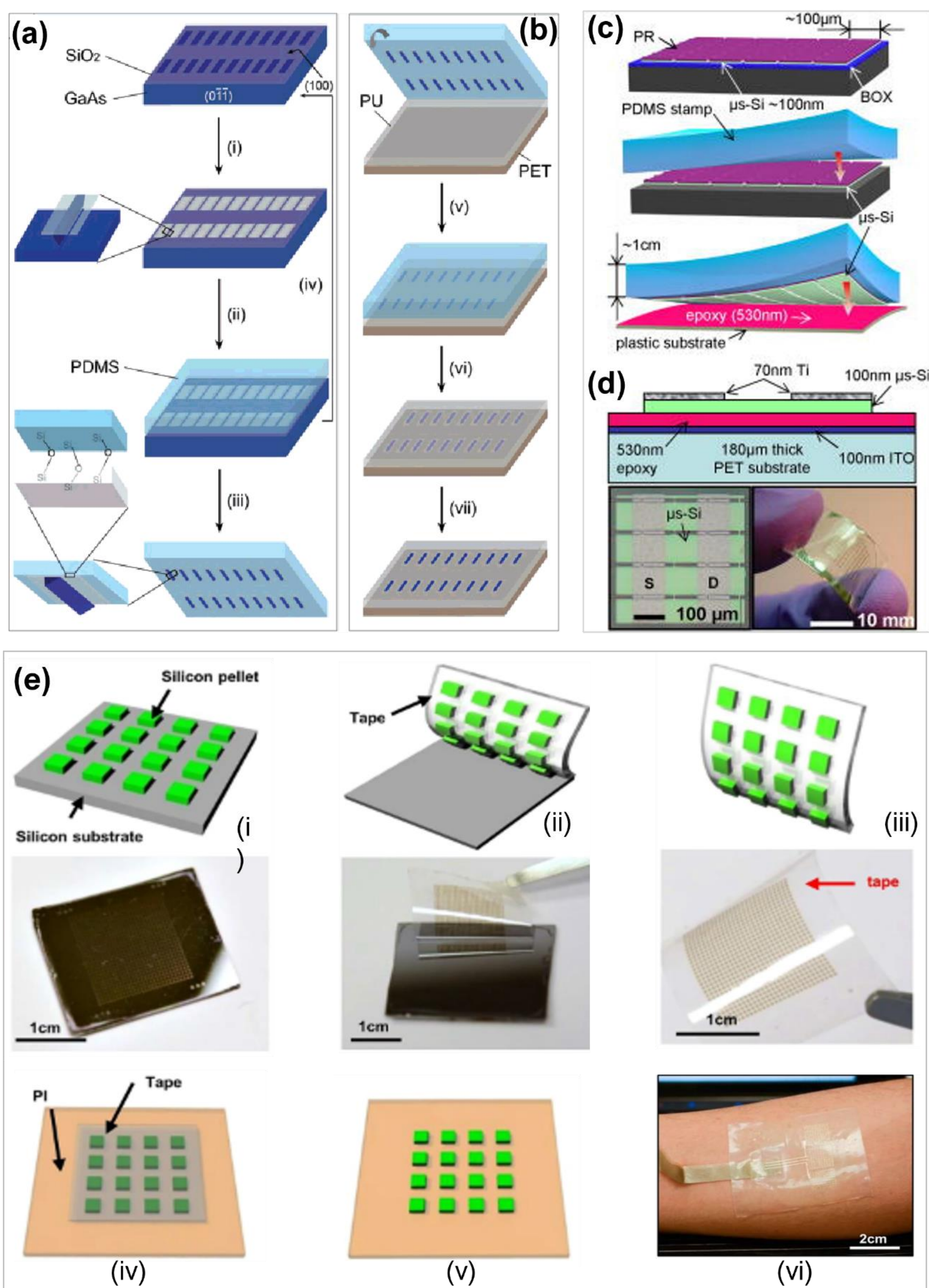


Figure 2.5: Surface treatment and adhesive assisted transfer printing technique. **(a)** Pick up step of the released GaAs wires from their bulk wafer performed by employing the chemical bonding between the PDMS stamp and thin layer of SiO_2 deposited on top surface of GaAs wires. **(b)** Schematic illustration of glue assisted transfer printing of GaAs wire arrays form intermediate PDMS stamp to PET substrate coated with thin layer of PU [42]. **(c)** Adhesive/epoxy assisted

transfer printing process utilising PDMS as intermediate stamp to transfer micro scale structures of Si ribbons from SOI wafer to flexible substrate. **(d)** cross-sectional schematic of the fabricated high-performance transistor realised on PET substrate [93]. The bottom right inset shows high magnification optical image of the device, bottom right inset shows low magnification optical image of the device arrays formed on PET substrate. **(e)** Illustration of tape transfer printing process steps. (i-v) The tape transfer printing process enabled by chemically induced dramatic modulation in tape adhesive strength to integrate Si pellets array fabricated from SOI and transferred onto flexible substrate (PI). (vi) An electromyography (EMG) sensor mounted on the skin of forearm for measurement realised by solvent releasable tape [101].

To improve the adhesion strength of transfer printing, another technique has been explored [101-103], which involves surface chemistry (Figure 2.5e). Compared to other integration techniques, it is a more straightforward process since it eliminates the use of elastomeric stamps. The commercially available solvent or thermal releasable adhesive tapes are used as stamp to pick up the fabricated structures/inks from their donor substrate and transfer print onto receiving substrate. In this technique, the reliability of the interfacial adhesion strength between the structures/inks and the tape is sufficient to allow the inks to be retrieved from the donor substrate. However, for the printing process, the interfacial adhesion strength between the tape and structures becomes significantly weak due to the use of solvents to decompose the adhesive layer or even the whole tape, which allows the structures to be transferred onto the destination substrate. This approach provides a simple route for the heterogeneous integration of various materials including metal patterns onto flexible substrates. However, this method produces surface contamination on the transferred structures after transfer printing process which leads to a negative impact on the device performance. To overcome these limitations, the modified transfer printing techniques based on tunable and reversible adhesion using elastomeric stamps have been developed and will be discussed in the following section. Figures 2.5 demonstrates the traditional integration techniques enabled by surface chemistry (Figure 2.5a,b) and adhesive assisted transfer printing methods (Figure 2.5c,d) to pick up the structures/inks from their donor substrate and integrate them on a flexible substrate with satisfactory transfer yields, and typical transfer printing process based on a commercially available solvent releasable adhesive tape (Figure 2.5d).

2.3.2.2 Transfer Kinetically controlled transfer printing technique

The traditional transfer printing technique is a simple integration technique that utilises an elastomeric stamp as an intermediate step to transfer the releasable micro/nanostructures from their donor substrate and print them onto a receive substrate [103-105]. However, as mentioned above, this conventional method has several limitations such as poor transfer yield and registration accuracy. To this end, several techniques and modification strategies have been adopted to improve the registration factor and achieve a higher transfer yield [33, 106]. Many modified transfer printing techniques have been developed. For instance, the dependency of the kinetical nature of the elastomeric stamp, the adhesion strength between the active device structures, and the intermediate stamp is critical. These are important as the viscoelastic effect of the stamp plays a crucial factor in this technique i.e., kinetically controlled [82, 107, 108]. The critical energy release rate at the functional structures and the stamp interface is sensitive to the rate at which the viscoelastic stamp is peeled away from the donor substrate. In this regard, the adhesion at the interface between the releasable structures and the stamp interface can be modulated by modifying the peeling velocity applied on the stamp, which leads to controlled delamination [47]. The peeling velocity can be adjusted based on the printing process step. For instance, it was shown that when the applied peeling velocity is sufficiently high, the adhesion strength is sufficient to pick up the released structures from their donor substrate onto the viscoelastic intermediate stamp [89, 109]. While during the printing step, the stamp is brough into contact with the target device substrate and retracted with lower peeling velocity, leading to weak adhesion to the viscoelastic stamp. The concept of this technique is based on kinetically controlled switching between adhesion and release structures to and from the viscoelastic stamp, and that depends on the peeling velocity rate of the stamp. This kinetically controlled transfer printing technique provides a solution for the integration of active micro and nano scale structures onto various flexible substrates (Figure 2.6a).

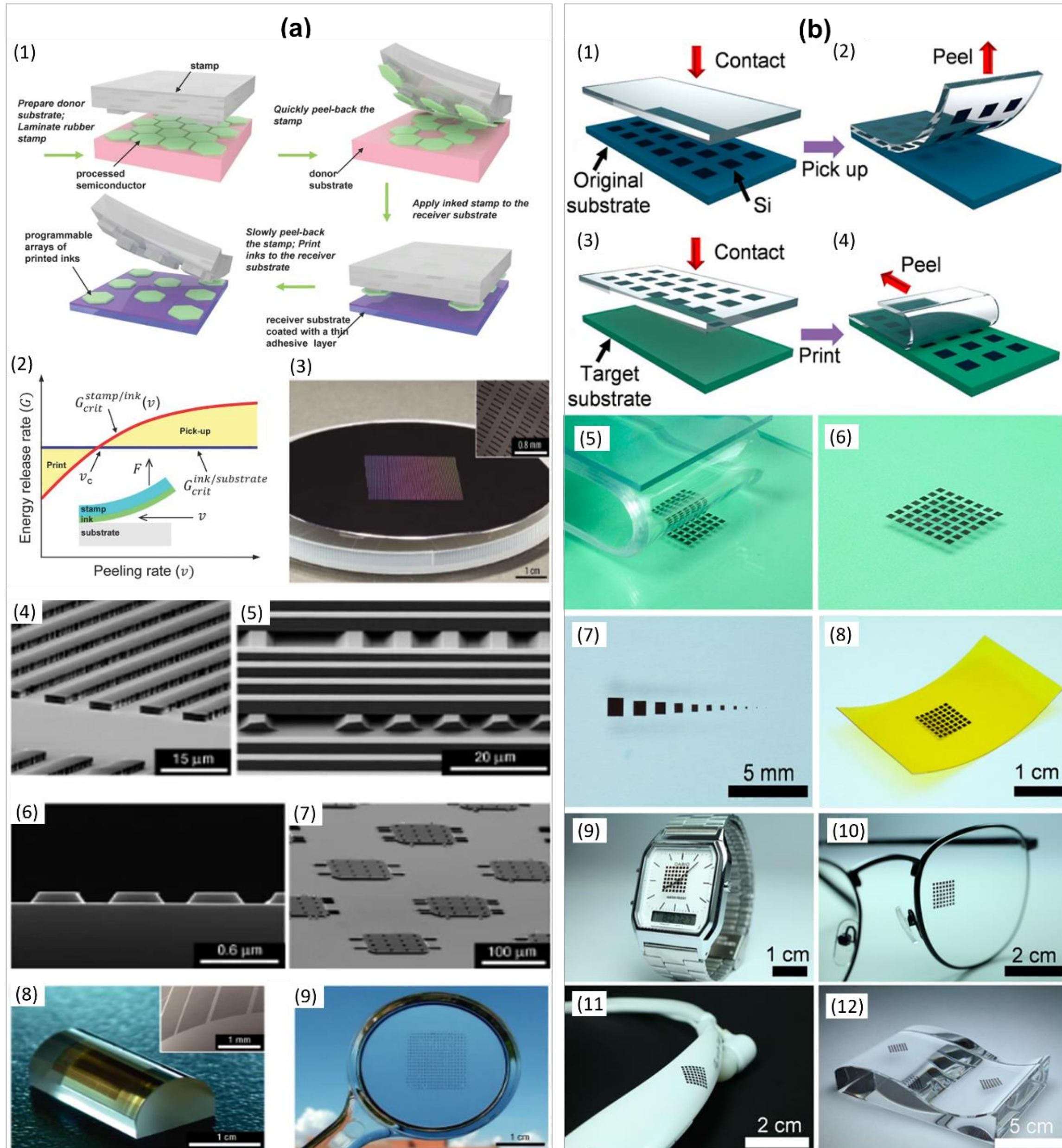


Figure 2.6: **(a)** Kinetically controlled transfer printing technique: **(1)** Schematic representation of the process flow for transfer printing using a soft, elastomeric viscoelastic stamp to transfer inks/structures from a donor material at high velocity (retrieval step) and integrate them at low velocity on the destination substrate (printing step). **(2)** A schematic diagram of the criterion for kinetically controlled transfer printing, with critical energy release rates shown for the ink/substrate interface and for the stamp/ink interface. The intersection of the horizontal line (blue) with the curve (red) represents the critical peel velocity (v_c) for the kinetically controlled pick-up and printing processes [110]. **(3)** An image of large-scale arrays of silicon microstructures with I shape (3cm × 3.8cm) transfer printed onto GaAs wafer, with an inset SEM image showing a few missing Si microstructures from the array [104]. **(4)** Printed micro-scale structures (ribbons) of GaN on a silicon wafer. **(5)** A multilayer stack of silicon microstructures integrated onto a silicon wafer. **(6,7)** multiple shapes of Si microstructures printed on wafers, **(6)** p-type Si microstructures printed onto InP, and **(7)** n-type Si printed onto a p-type silicon wafer. **(8)** Si microstructures-based solar cells integrated on a curved surface by rolling a cylindrical glass over an elastomeric stamp with printed Si

microstructures, with an inset of the corresponding SEM image. **(9)** Printed arrays of micro-scale Si ribbons formed by stamping the soft stamp inked with the Si structures over a plastic substrate (double-convex polycarbonate) using kinetically controlled transfer printing technique [104]. **(b)** Schematic illustrations of an adhesive-less transfer printing procedure, with optical images after transferring to various substrates: **(1-4)** Schematic illustration demonstrating the transfer of micro Si plates from a donor to a receiver substrate through an elastomeric stamp; **(5)** An optical image while transferring to a glass substrate; and **(6-10)** Photographs of Si-micro plates transferred to various substrates, such as **(6)** a glass slide, **(7)** micro-scale Si plates transfer printed on a glass substrate with different geometries (smallest, 30 × 30 µm; largest, 750 × 750 µm) **(8)** a flexible substrate (polyethylene terephthalate (PET) coated with PI), **(9)** a wrist watch, **(10)** an eye glass, **(11)** a curved surface of an earphone, and **(12)** a concave/convex surface [111].

The underlying physics associated with kinetically controlled transfer printing process was investigated [110]. The peeling process of the stamp from the substrate was modeled as the steady propagation of interfacial cracks, enabling the establishment of a criterion to predict whether retrieval or printing would occur (Fig. 2.6a(2)). The critical energy release rate, $G_{\text{crit}}^{\text{ink/substrate}}$ at the ink/substrate interface is rate-independent since both the ink and the substrate are elastic. On the other hand, the critical energy release rate, $G_{\text{crit}}^{\text{ink/stamp}}(v)$, at the stamp/ink interface is rate-dependent due to the viscosity of the stamp. The condition $G_{\text{crit}}^{\text{ink/substrate}} = G_{\text{crit}}^{\text{ink/stamp}}(v)$, corresponding to the intersection of the two curves in Fig. 2.6a(2), determines the critical peeling velocity v_c, which separates the retrieval and printing regimes. Retrieval occurs when the peeling velocity is greater than v_c, while printing occurs when the peeling velocity is smaller than v_c. However, the kinetically controlled transfer printing may face challenges. For instance, in cases with a strong ink/substrate interface, the range of modulation in adhesion strength may be limited, leading to the failure of ink retrieval from the donor substrate. Similarly, for weak ink/substrate interfaces, there may be difficulties in printing the inks onto the receiver substrate. To enhance the yields of printing for weak ink/substrate interfaces and address these limitations, further investigations and optimizations are necessary. These efforts could lead to significant improvements in the efficiency and success rate of kinetically controlled transfer printing, making it a more viable technique for various applications in the field of flexible electronics and micro/nano-system integration.

Despite the merit of this approach, it depends on the kinetic control of the soft stamp which requires sufficient interface forces to delaminate the structures from one substrate to another. There have been several challenges related to speed control and contact area due to the high dependency of the peeling velocity [109, 110, 112]. Furthermore, this method has some drawbacks in terms of poor registration accuracy and reproducibility. This is due to limited control range of the adhesion strength and viscoelastic property of the intermediate stamp, and deformation behavior under applied force during the integration/printing process. kinetically controlled transfer printing is a promising technique for the assembly of micro/nanoscale devices. However, using a viscoelastic receiver substrate can pose a significant challenge in achieving high transfer yield with high reproducibility and large-scale printing capability. The limitations of the current transfer printing method may lead to the need for further optimization to improve the integration process [47]. There have been attempts to improve the control over the adhesion strength by investigating the impact of directional peeling off the patterned stamp. It has been shown that peeling the stamp away in perpendicular and parallel directions can enhance transfer yield and lower the critical energy release rate [109]. Another study has been carried out recently using flat stamps for integrating inorganic micro scale structures on flexible substrates without using interlayer adhesive. As shown in figure 2.6b, it was shown that by modulating the peeling speed and bending radius of a flat stamp can contribute towards achieving high integration efficiency [111].

2.3.2.3 Transfer Printing Based on Shape Memory Polymer

The elastic deformation of the patterns of the active stamp during the recovery state i.e., pressured balloon structure of capping membrane [113, 114] collapsed micro-pyramid structures [115], these elements are passive and time sensitive due to the viscoelastic properties of PDMS, which may yield unexpected tilt, rotation and even drop of structures during the transfer printing process [47]. In order to improve the reliability and controllability over transfer printing process, shape memory polymers (SMPs) are used instead of conventional PDMS stamp (Figure 2.7). The SMPs have the capability of switching between temporary and original shape, also they can memorize the short-term deformation formed by various pre-loads and easily recover their permanent shape, after being activated by an external stimulus [115]. In this regard, the SMPs have the characteristics of elastic modulus dependency over the polymer's glass transition temperature (Tg), securing the temporary shape along with permanent shape recovery, both can be controlled by applying heat as shown in figure 2.7(1). The design of SMP stamp has pattern features similar to the micro-pyramid structures used for surface relief assisted transfer printing technique, which can be defined as the original or permanent shape of the stamp. This process begins with heating the SMP stamp to above its Tg till it becomes compliant, then a preload is applied to allow the micro-pyramid structures to deform to take the temporary shape. Then, the SMP stamp cooled down to maintain its temporary shape. During this step, the stamp is brought into contact with the structures/ink to pick up the structures from the donor substrate. The temporary shape with a large area contact is used in the pickup step where the high interfacial adhesion is needed. For the printing step, the SMP stamp is heated above its Tg to recover to its permanent shape which significantly reduces the contact area to be within only tip contact and therefore, the interfacial adhesion strength becomes weak to achieve a reliable printing. However, this step is performed by using a laser pulse to heat the regions selectively to enable selective/programmable printing as shown in figure 2.7(2,3) [106, 116]. This technique has several limitations since the use of SMP stamp requires high temperatures which may introduce damage to the printable structures, substrate and final fabricated device,

especially for inorganic micro/nanostructures-based electronics. Moreover, this process is not compatible with large area electronics as its quite challenging to apply in industrial scale manufacturing [47, 117].

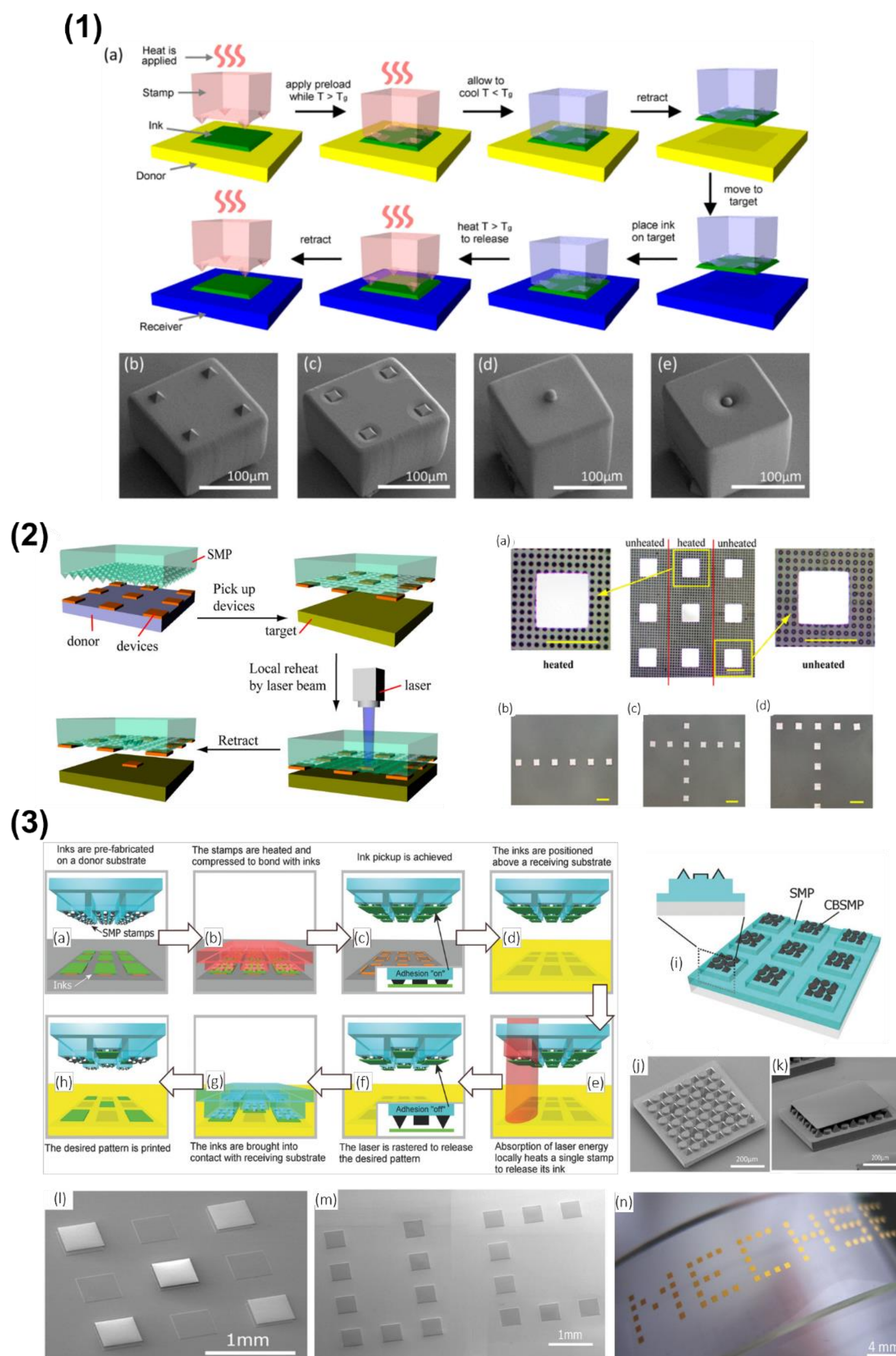


Figure 2.7: (1) Schematic illustration for transfer printing technique based on shape memory polymers (SMP). **(a)** schematic of the process flow for implementation of SMP microtips using heat source to trigger thermal transition in SMP used for micro scale integration by transfer printing.

(b) microtips on the soft stamp surface in original shape toward achieving off state adhesion, **(c)** toward achieving on state adhesion. **(d)** spherical tip on the soft stamp surface in original shape toward achieving off state adhesion. **(e)** spherical tip on the soft stamp surface in temporary shape toward achieving on state adhesion [118]. **(2)** Schematic representation of programmable integration by transfer printing using automated laser beam as heating source to trigger a micropatterned SMP stamp. **(a-d)** obtained results from transfer printing by induced laser writing. **(a)** selective integration of releasable of Si squares via laser beam. The red lines demonstrate the heated region via laser beam, where the micro-pyramid patterns on the stamp becomes darker, indicating the adhesive is off state, whereas unheated region remain coloured, indicating the adhesive is on state. **(b-d)** printed Si squares selectively on elastomeric stamp forming different shapes (scale bars: 100µm) [106]. **(3a-h)** implementation of the NIR laser driven carbon black-shape memory polymer (CBSMP) assisted transfer printing process. Carbon black composite is selected as the absorbing agent to allow the stamp activation selectively, and thus selective printing of structures is performed. **(i)** schematic image of final form of the micropatterned stamp showing SMP and CBSMP patterns. **(j)** corresponding high magnification SEM image of SMP stamp. **(k)** Si square with 3µm thickness on contact with stamp after laser illumination where the micropatterns on the stamp are released to the desired permanent shape. **(l)** selectively printed arrays of Si microstructures. **(m)** printed Si structures on Si substrate forming the letters ''UC'', **(n)** printed gold coated Si structures on PDMS substrate. [116].

2.3.2.4 Laser-Assisted Transfer Printing using PDMS stamp

As mentioned in the previous section and as shown in figure 2.7(3), laser illumination under a specific wavelength e.g., NIR spectrum (peak 807nm wavelength) has been employed to activate SMP stamp based on the modified composite polymer (CMSMP) [116]. This section summarizes transfer printing techniques assisted by pulsed laser beams using an intermediate elastomeric stamp (PDMS) to facilitate the printing process, based on reported works in the literature. The concept of laser-assisted transfer printing was developed based on the idea of thermal mismatch from the thermo-mechanical response of multilayered structures with various materials. A laser pulse-based process was developed in the printing step to improve delamination of the structures from the elastomeric stamp, enabling the structures to be transferred to a destination flexible substrate without the need for direct physical contact (Figure 2.8) [119, 120]. The successful implementation of non-contact laser-assisted transfer printing is highly dependent on the laser pulse used in the printing process. Due to the absence of a strict requirement for direct physical contact between the functional structures and the receiving substrate, this technique demonstrates the potential to integrate functional structures onto various flexible substrates, such as flat, curved, or even unconventional ones. it is noteworthy that the high temperatures generated by the laser

pulse may damage the functional structures, potentially affecting device performance. Additionally, precise control over parameters such as laser pulse intensity and irradiation time is required for successful printing, which may require expensive equipment.

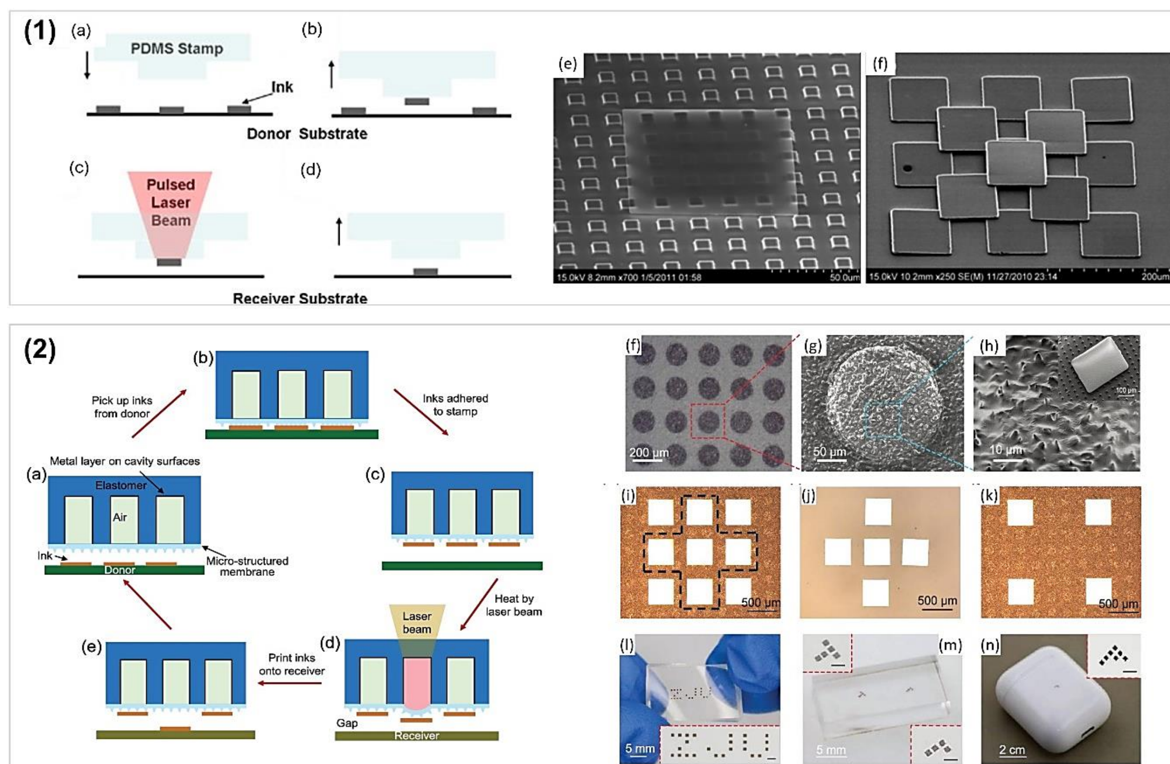


Figure 2.8: **(1)** Schematic illustration of the laser-assisted transfer printing process: **(a)** align the elastomeric stamp (PDMS) with the donor substrate, **(b)** selectively pick up releasable structures from the donor apply pulsed laser beam to heat up the interface between the stamp and structures, **(d)** perform the printing step on the receiver substrate, and **(e)** print a Si square with lateral dimensions of 100 µm and thickness of 0.32 µm onto a patterned substrate. **(f)** A 3-D structure of 100 µm × 100 µm × 3 µm silicon squares formed by multiple printing cycles of silicon squares [120]. **(2)** **(a-e)** Schematic representation of the process steps of the laser-driven programmable non-contact transfer printing process using a micropatterned elastomeric stamp. **(f)** Optical image of the micropatterned stamp surface with cavity structures. **(g)** SEM image of a single pattern. **(h)** High magnification SEM image of the micro-structure stamp surface, the inset shows the SEM image of a Si platelet transferred onto the micropatterned PDMS stamp. **(i)** Array of Si platelets picked up by the micropatterned stamp, where the structures surrounded by dotted lines are thermally and selectively treated via pulsed laser beam. **(j)** Then printed on the destination substrate. **(k)** The unheated Si platelets remained on the stamp surface. **(l)** Printed Si structures on the PDMS substrate forming letters ‘‘ZJU.’’ **(m)** Printed Si plates forming a letter ‘‘T’’ and ‘‘L’’. **(n)** Printed Si structures forming a letter ‘‘F’’ onto the cover of Apple AirPod [121].

2.3.3 Bio inspired transfer printing methods:

2.3.3.1 Gecko-inspired Transfer Printing technique

Geckos have evolved a set of adhesive structures which give them the ability to move and adhere to vertical objects like walls and ceilings against their body weight (Figure 2.9). This provides a piece of valid evidence that the adhesion capability of geckos' is due to the van der Walls interaction at the contact area interface between the surface and hundreds of thousands of micro scale structures called setae on the geckos' foot, where each setae has hundreds of nanoscale structures called "spatulae", the spatulae are arranged in arrays that create an adhesive contact area, which can be as much as 200 times greater than the total area of setae [122]. Thus, during the last decade gecko has inspired several strategies for transfer printing development [123-125]. In this regard, the performance of transfer printing is critically relying on the transition status of the interfacial adhesion strength (elastomeric stamp/released structures) in reversible fashion, i.e., from the strong adhesion state for successful pick up to the weak adhesion state for efficient printing on receiving substrate. In this regard, several studies on advanced transfer printing techniques have been carried out to minimise the limitations of the conventional stamp-based integration techniques and enhance printing reliability, in terms of increasing the controllability of the reversible dry adhesion strength for strong attachment, easy detachment, repeatability, and printing compatibility on multiple substrates, etc.

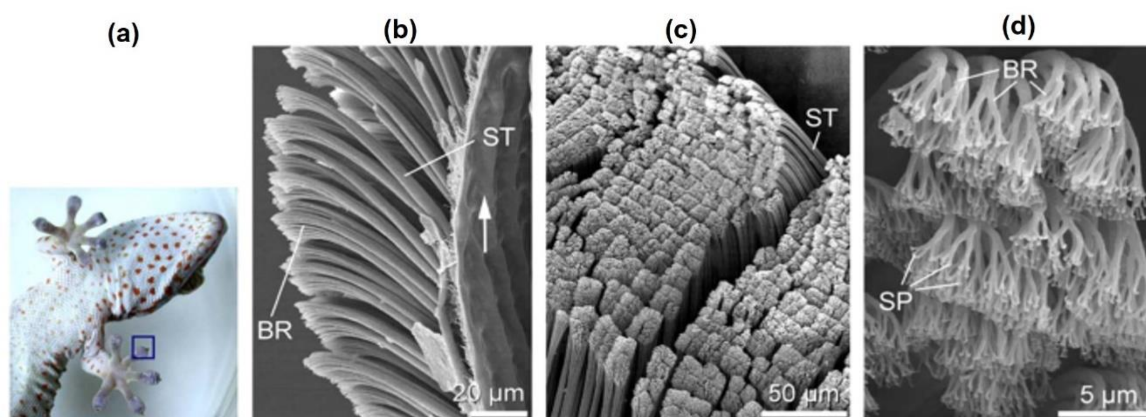


Figure 2.9: Structural hierarchy of the Gecko dry adhesive system. (a) represents a photograph of a gecko climbing a vertical glass wall. (b) is a SEM image of arrays of setae (ST) with branched structures (BR). (c) is another SEM image at a different magnification, demonstrating hundreds of

(ST). (d) is a SEM image of the finest structures of hundreds of spatulae (SP) branched with each seta [122].

To this end, various strategies of reversible, and tunable dry adhesive have been inspired by Gecko's toe pad, by introducing relief micro scale patterns and engineered microstructures on the stamp surface [125], such as hierarchical, spatulae [123, 124], fibrillar [126], angled setae [127]. These micro scale structures are characterized by controlling the mechanical deformation induced under applied pressure either in vertical or lateral directions. This provides a unique capability in terms of achieving a weak adhesion strength for integrating the released structures on flexible substrates, thus leads to an increase in the efficiency of integrating micro-nanostructures with high transfer yield. Several gecko-inspired integration/assembly techniques have been developed such as transfer printing using an angled microflap stamp [128], shear assisted transfer printing [129], transfer printing using isolated gecko seta array stamp [124], and pedestal stamp assisted transfer printing [130].

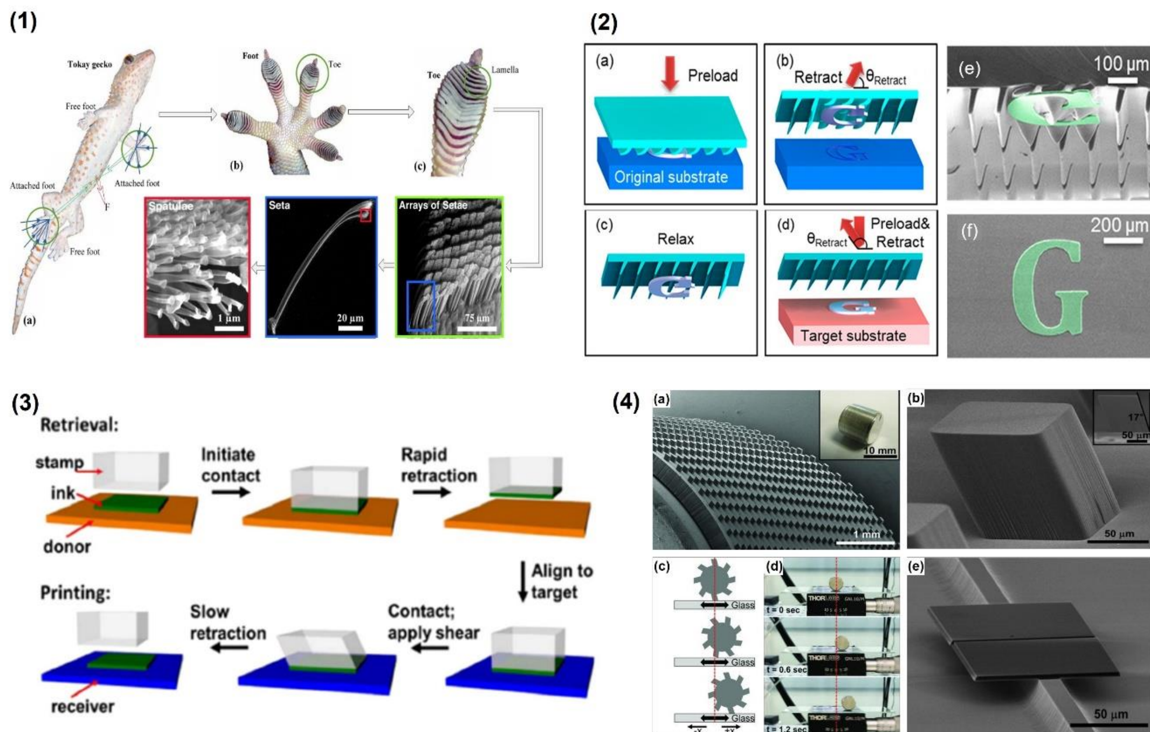


Figure 2.10: Schematic illustration of Gecko inspired transfer printing: shear assisted transfer printing: **(1)** Gecko dry adhesive system [131]. **(2)** Schematic representation of transfer printing using an angled microflap array stamp [51]: The SEM images **(a-d)** depict the transfer printing process, while **(e)** shows a microscale Si membrane with a thickness of 7 µm still in contact with

angled microflaps prior to being printed on the receiver substrate. **(f)** shows the printed Si membrane on the receiver substrate without any adhesive layer [51]. **(3)** Schematic representation of shear-assisted transfer printing with horizontal displacement to minimize adhesion strength during the printing process [129]. **(4)** Demonstration of transfer printing using an elastomer stamp roller with directionally dependent adhesion. The SEM image **(a)** shows the stamp roller with an array of angled microscale patterns, and the inset depicts a photograph of the stamp roller. The high magnified SEM image **(b)** shows a single angled post on the stamp surface. **(c-d)** demonstrate the process procedure of an angled patterned roller stamp moving on a glass substrate. **(e)** shows SEM image of printed Si platelets (100 μm × 100 μm × 3 μm) on a patterned rigid Si substrate [132].

In this context, one of the modified transfer printed techniques was demonstrated by Yoo et al. adopted based on the same inspiration from the gecko's foot, as shown in figure 2.10(2) [51]. The development of this approach was based on the directionally dependent dry adhesion using an angled micro flap elastomeric stamp. The stamp design was engineered to have compliant micro flaps on its surface that can provide strong retraction angle dependent adhesion. An experimental qualitative study was conducted to investigate the adhesive properties of angled microflaps under various manipulation conditions, including applied preloads, manipulation speeds, and retraction angles [51]. The results revealed that higher adhesion is achieved by retracting the angled microflap stamp at an angle of approximately 40−60° and at a relatively high speed. This creates a shear force between the stamp and the Si membrane, increasing the frictional energy and the number of intermolecular contacts. As a result, stronger van der Waals forces are engaged, leading to enhanced adhesion. Additionally, the higher retraction speed effectively overcomes adhesive forces, contributing to improved adhesion. However, for lower adhesion, it is recommended to place the membranes on a surface at an angle greater than 90° and at a relatively low speed. This reduces the contact area between the stamp and the surface, resulting in decreased frictional energy and van der Waals interactions, leading to lower adhesion. Moreover, the slower placement speed allows more time for the van der Waals forces to relax, further reducing the adhesion strength. Therefore, this indicates the switching of the adhesion strength between strong and weak can be controlled by the retraction angle. Thus, picking up the structures from their donor substrate and placing them onto the destination substrate can be achieved at the retraction angle of 60° and 100°, respectively as shown in figure 2.10(2). The angled micro-flap stamp assisted transfer

printing has been employed to integrate structures with irregular micro-scale geometries on dry surfaces using custom-built motorised micro stage [132], as shown in figure 2.10(4).

Carlson et al. [129] developed another transfer printing technique inspired by Gecko's toe pad (Figure 2.10(3)). In this technique, the modulation of dry adhesion strength occurred based on the directional shear displacement of the stamp. The stamps were designed and realised with three-dimensional vertical micro scale patterns that can be utilised to perform shear assisted transfer printing, [125]. The analytical model supported by experiment [133] indicates the validity of the shear displacement on the elastomeric stamp to minimise the adhesion strength at the interface between the stamp and structures toward achieving easy delamination of the structures from the stamp. The structures are picked up from their donor substrate when the stamp is pulled off rapidly and the printing is then assisted by a lateral shear displacement.

Yang et al. [132] made another attempt to enhance the performance of shear enhanced transfer printing further by adopting a novel design of directional microstructures on the stamp surface that is compatible with roll-to-roll (R2R) applications. As demonstrated in figure 2.10(4), the soft stamp was realised with angled vertical posts, the geometric designs of angled posts are defined as relief features on the stamp, which facilitate the adhesion switching by control of the direction of retraction. In particular, the angled vertical post was designed in such a way that can lead to a change in slope for crack formation, subsequently the crack propagation is decreased when the lateral movement is applied along the inclination direction and increased when the lateral movement is applied in opposite direction, thus leading to high and weak adhesion strengths, at the stamp/structure interface respectively [132].

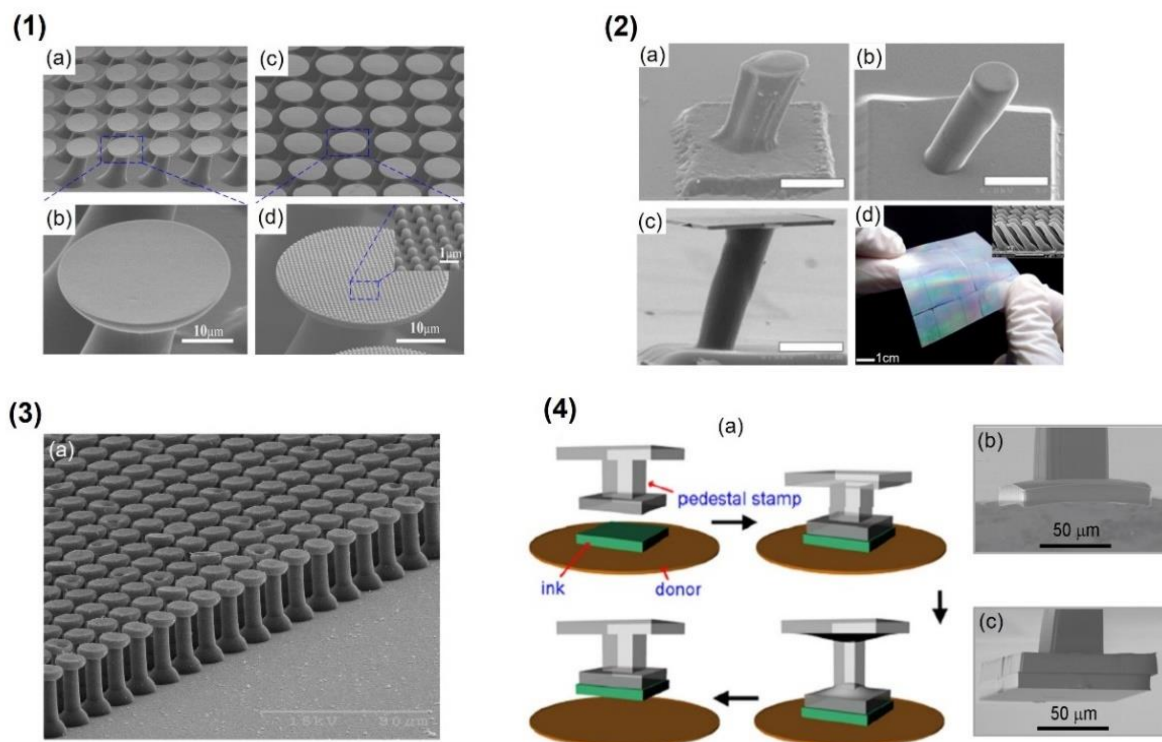


Figure 2.11: (1) (a-d) SEM images of intact PDMS stamp fabricated with tilted micro scale **(a-b)** pillars and **(c-d)** hierarchical structures [134]. **(2)** SEM images of **(a)** round tip micropillar, **(b)** flat tip micropillar, and **(c)** Si platelet structure (100 μm × 100 μm × 3μm) picked by flat tip pillar. The micropillars are made of elastomeric polyurethane. Scale bar represents 50μm [125], **(d)** A photograph represents large area of fabricated PUA nanostructures on PET substrate. Inset represents the corresponding magnified SEM image of tilted polymer nanostructures fabricated from UV curable PUA resin [135]. **(3)** SEM image of gecko dry adhesive inspired micro scale adhesive realised by microfiber array [136]. **(4)** Gecko inspired dry adhesive-based transfer printing technique: **(a)** Schematic representation of transfer printing procedure using pedestal stamp, **(b)** SEM image of pedestal PDMS stamp, **(c)** SEM image of the stamp during pick up step of 10 μm thick Si platelet. From ref [130].

Excellent modulation control over the interfacial adhesion strength between the stamp and releasable structures is highly needed. Most of the previously reported studies indicate that the design geometries of the micro/nano structured patterns on the stamp surface play a critical role in reversible adhesion strength control [137]. Buckling actuated assisted transfer printing has been reported as an effective technique [125]. The basic working principle of this technique is inspired by a gecko foot-hair using angled pillar microstructures with flat or cylindrical tip ending shapes [125, 134], as shown in Figure 2.11(1,2). The stamp with surface angled cylinder pillar is utilized to modulate the adhesion strength. The releasable structures are transferred from their source material onto the intermediate stamp by

applying an optimized contact force vertically, leading to create a vertical compression of the tip on the structures until the pillar is compressed to buckle. Thus, the contact area between the stamp and the structures is maximized. Then, the separation of the stamp is performed rapidly to secure a strong attachment during the retrieval step. During the transfer process, the adhesion between the stamp and the structures is sufficient to withstand sudden disturbance or any gravitational forces that can be dominated by the weight of structures. As a result, this approach can address the limitations introduced with previously demonstrated micromanipulation reported by Kim et al. [115]. During the printing process, where the structures should be released from the elastomeric stamp onto a receiver substrate, the contact area between the pillar and the structures is significantly minimized by the deformation of the pillar due to the vertical or shear movement control process. Thus, the interfacial adhesion strength between the stamp and structures becomes weak. Adhesion switchability can be accomplished by the buckling actuated transfer printing technique.

Most of the gecko-inspired transfer printing techniques mentioned above focus on the printing process where the reduction of adhesion strength is required. However, in the retrieval process, less attention is given to enhancing the adhesion strength. Although actual adhesion can mostly meet the retrieval process requirement for inorganic materials such as silicon. However, some other materials such as GaAs, GaN, etc. suffer from poor bonding strength when it comes to physical contact with an elastomeric stamp [95]. Further optimization of adhesion strength and interfacial modification is needed to ensure reliability and reusability, thus allowing the potential of these printing strategies to be adapted for practical flexible electronic applications. Toward improving the adhesion and enhancing the reliability of the retrieval process, it has been shown that a sufficient strong adhesion strength inspired by the gecko's toe pad can be enabled by spatulate tips [136], as shown in Figure 2.11(3). Similarly, Figure 2.11(4) represents another inspired study by the gecko's toe pad reported by Kim et al. [130], where the strong adhesion strength was achieved by a pedestal stamp with a rectangular post on an end pad. In this approach, a pedestal stamp designed with a rectangular post on an end pad is utilized to improve the reliability of the

retrieval process. Based on these studies, it has been shown that optimizing the stamp design geometries by adding the end pad to the vertical post with a flat contacting surface has a significant influence on the adhesion behavior [138]. Since it initiates cracks at the center of the pad instead of the edge, the strength adhesion associated with the retrieval process is further enhanced by employing micro-patterned stamp design with engineered geometries such as pedestal, spatulate tips, and mushroom-shaped micropatterns [138], compared with a flat bulk pillar [138].

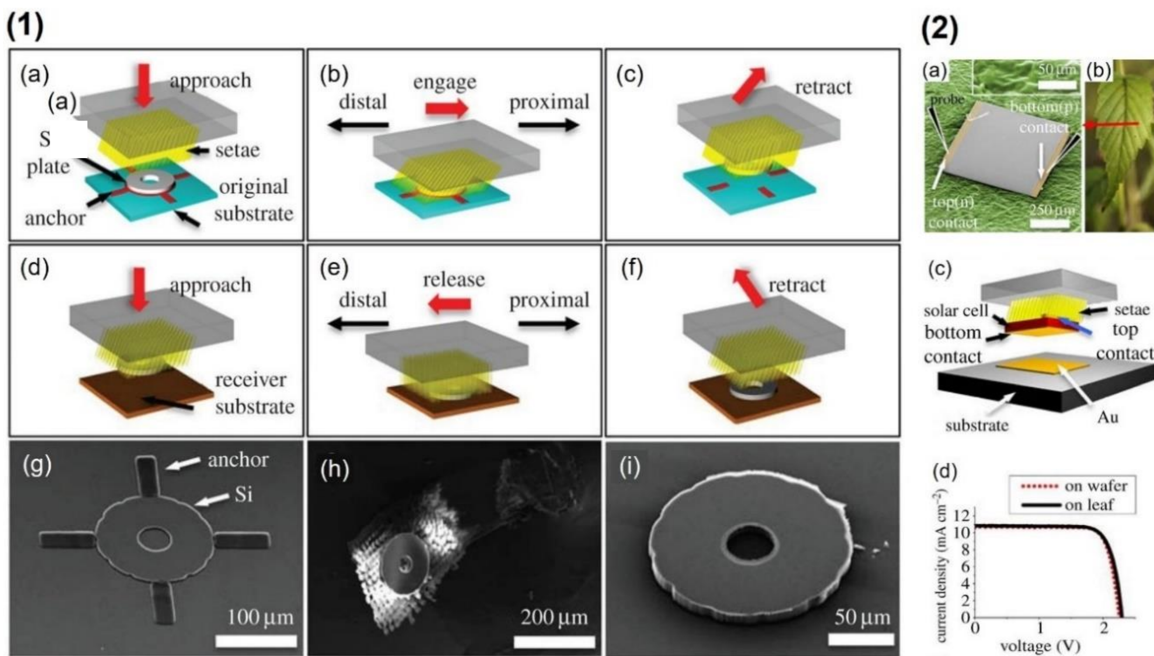


Figure 2.12: **(1)** **(a-d)** Schematic representation of natural gecko adhesive inspired transfer printing procedure using seta array stamp that mimics the gecko adhesive foot setae. **(g)** SEM image of printable 10 µm thick Si plate that anchored to the source substrate. **(h)** Si plate retrieved from the source substrate by seta array stamp **(i)** placed on silicon substrate. **(2)** Transfer printed micro scale functioning device on unconventional substrate. **(a)** colorized SEM image of 6.7µm GaAs based micro solar cell transfer printed **(b)** on a leaf. **(c)** Schematic illustration of vertical structure solar microcell to be transferred by seta array stamp on top of metal contact (Au) for direct electrical connection. **(d)** The electrical performances of printed solar microcells [124].

Jeong et al. developed a dry adhesive-based integration strategy for inorganic microstructures, inspired by the seta arrays on gecko toes [124]. Unlike traditional adhesive solutions like glue, this technique avoids negative impacts on the interface between the final device and destination substrate caused by applied force or temperature (Figure 2.12). Retrieval of the microstructures is enabled by physical contact between the gecko seta array

stamp and the structures, followed by pulling the stamp horizontally in the proximal direction with a displacement of tens of microns. This provides sufficient adhesion to retrieve the structures from their source material. Printing is performed in the same manner as picking up, where the microstructures held by the seta array stamp are brought into contact with the destination substrate and the stamp is pulled in the opposite direction to minimize adhesion. This minimizes the risk of delamination and facilitates integration of structures onto various flexible substrates.

Gecko-inspired transfer printing techniques have demonstrated effectiveness in integrating micro and nanoscale inorganic semiconducting structures, especially in enhancing adhesion strength and switchability. Nevertheless, these techniques possess certain limitations and fabrication challenges, making them less suitable for large area electronics. The fabrication of gecko-inspired soft stamp structures typically demands complex and costly equipment, which may not be commonly available in conventional micro/nanofabrication electronics laboratories. However, the simplicity of stamp fabrication with micro-scale patterns offers an advantage compared to the hierarchical adhesive structures found in the natural setal arrays of geckos. Despite their advantages, these techniques may encounter issues related to registration accuracy and alignment of printed structures on the destination flexible substrates. Vertical movement during the transfer process can induce buckling and shear displacement due to stamp deformation under compressive load, resulting in misalignment/poor registration accuracy and compromising the precision and uniformity of printed features. Such challenges become more prominent when scaling up to larger areas. In summary, gecko-inspired transfer printing techniques have a great potential in micro and nanoscale integration of inorganic semiconducting structures, their limitations in large area applications require further research and development. The unique capabilities of the gecko adhesive serve as a valuable reference for advancing transfer printing techniques [47, 126].

2.3.3.2 Aphid-inspired transfer printing techniques:

To improve the adhesion control of transfer printing, a strategy inspired by aphids was developed. Aphids use a pneumatic mechanism to control adhesion strength by changing the effective shape and tension of their adhesive structures/pads, resulting in a change in the contact area [113, 139]. Many aphid-inspired techniques based on contact area change have been developed, such as the surface-relief assisted transfer printing technique [114, 115] and transfer printing using an inflatable stamp [114]. Kim et al. [115] developed a pyramidal microtips stamp-based transfer printing technique, as demonstrated in Figure 2.13(1). This technique is based on minimizing the contact area at the interface between the stamp and structures to achieve a lower critical energy release rate [89, 115]. The adhesive surface of the soft stamp was designed to mimic the adhesion organs (pulvillus) of aphids. The micro-scale patterns of the elastomeric stamp (pyramidal microtips) induce pressure sagging, which provides reversible adhesion strength switchability by transitioning interfacial adhesion strength from stronger to weaker (Figure 2.13(1)). When fabricated structures are picked up from the donor substrate by the viscoelastic stamp, the applied pressure deforms the pyramidal microtips, which increases the contact area and provides sufficient adhesion strength to lift the released structures. During the printing step of the inked stamp on the receiving substrate, the patterns of the pyramidal microtips on the stamp surface recover to their original shape after removing the applied pressure. This significantly reduces the contact area and weakens the adhesion strength at the stamp/structure interface (Figure 2.13). To further improve control over the interfacial adhesion strength, this approach can be combined with a kinetically controlled technique. By lifting the structures from their donor substrate with high peeling velocity during pick up, and slow retraction velocity during printing, greater control over adhesion can be achieved.

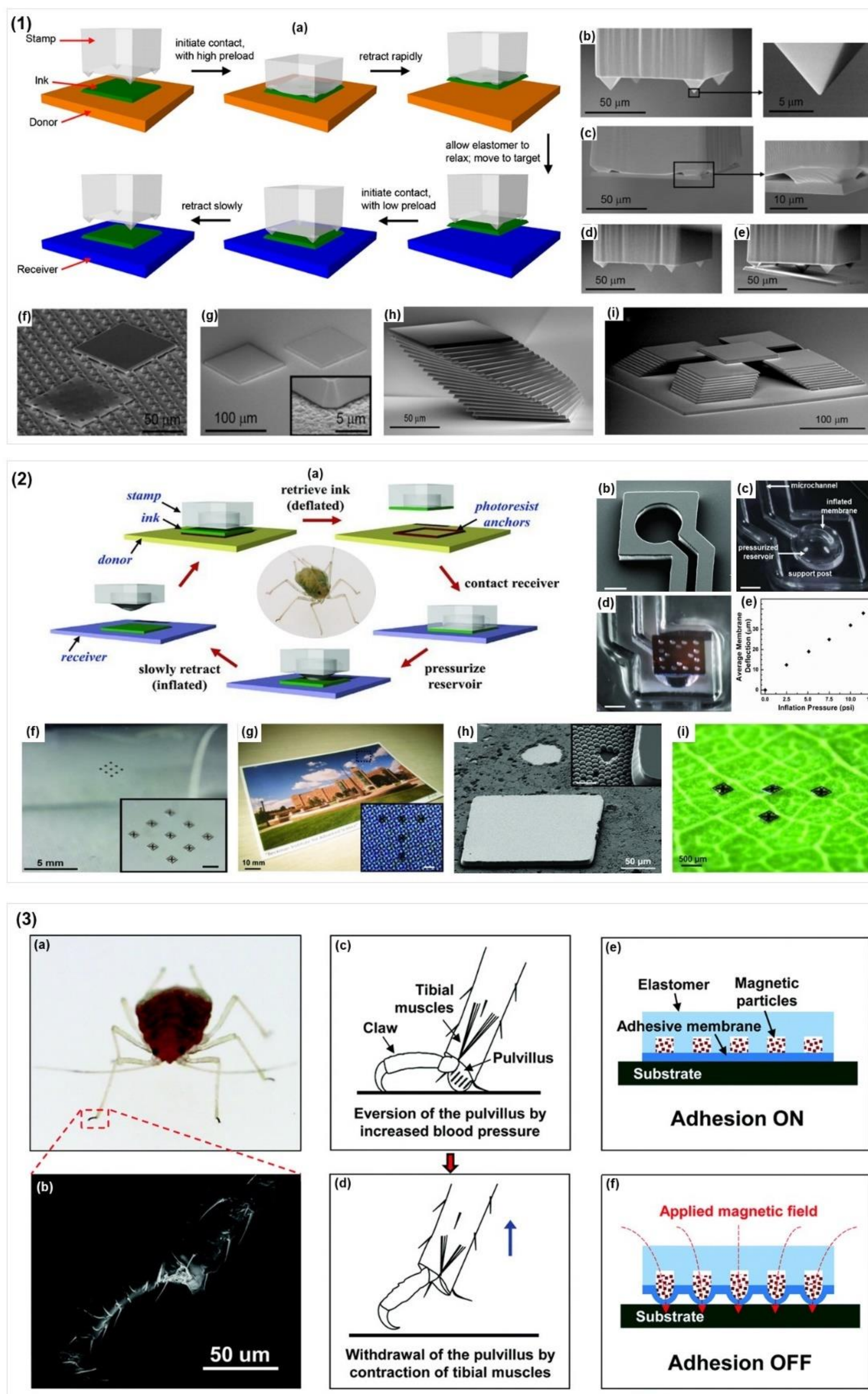


Figure 2.13: Aphid-inspired transfer printing techniques. **(1)** Schematic illustration of transfer printing process and corresponding SEM images obtained from various stages. **(a)** process procedure of using elastomeric stamp surface implemented with micro pyramids tips for microstructures

integration by transfer printing. **(b-i)** corresponding SEM image obtained at various stages of the process. **(b)** elastomeric stamp realized with micro pyramids tips. **(c)** Si platelets (100 μm × 100 μm × 3 μm) in contact with micro tipped stamp. **(d)** micro tips on stamp surface after recovery. **(e)** Si microstructures not fully in contact with micro tips, during the final stage of printing process on the receiving substrate. **(f)** printed 3μm and 260nm thick of Si platelets on micropatterned surface. **(g)** printed on rough surface as shown in inset image. **(h)** multilayer of printed 3μm thick Si platelets in a single stack. **(i)** printed in a multi stacks on silicon substrate [115]. **(2)** Another integration technique by transfer printing inspired from aphid: **(a)** image of an aphid with process procedures for transfer printing using inflatable elastomeric stamp for controlling adhesion state. **(b)** SEM image of active stamp without implementing the layer of PDMS capping membrane. **(c)** optical image of the actuated stamp with inflated capping membrane. **(d)** actuated stamp with Si plate (250μm × 250μm × 3μm). **(e)** Graph of average deflection of the capping layer during inflation. **(f-i)** demonstration of printed Si microstructures on different substrates: **(f)** PET. **(g)** glossy card. **(h)** photonic crystals based on SiO_2 microspheres. **(i)** leaf [114]. **(3)** Transfer printing technique based dry adhesive inspired by aphid: **(a)** optical image of aphid. **(b)** SEM image of an aphid leg. **(c-d)** structural representation of dry adhesive system of an aphid. **(e-f)** schematic representation of the bio dry adhesive inspired transfer printing technique actuated by a magnetic field [113].

Another aphid-inspired transfer printing strategy was developed by Carlson et al. [114] using an inflatable stamp. The stamps used in this approach have features of microchannels on the bottom surface, which opens the reservoir on the bottom surface of the active stamp, and a thin PDMS capping membrane to encapsulate the reservoirs, as demonstrated in Figure 2.13(2b-d). Inflation of the active stamp is performed by applying pressure in a controlled manner on the capping membrane, which leads to the desired surface deformation in localized regions, in a fashion similar to that of a balloon. The contact area between the stamp and the structures/ink is minimized by reducing the deformation of the capping membrane, which weakens the adhesion strength at the interface of the stamp/structures. (Figure 2.13(2a)) shows the transfer printing procedures using the inflatable pattern for controlling the adhesion strength. For instance, picking up the structures from the donor substrate, the stamp in the deflated state is brought into contact with structures to achieve large contact area and high adhesion strength between the capping membrane and the structures. Therefore, the retrieval of the structures/ink onto the stamp surface is performed. Then, for the printing process, the structures/ink which the stamp is holding are brought into light contact with the receiving substrate. To allow the required detachment for the printing process, the thin capping membrane is pressurised in a controlled manner through the reservoirs to reduce the contact area, leading to weak

adhesion for printing, therefore the active stamp releases the structures onto the receiver substrate. In this context, the adhesion strength at the interface between the stamp and structures decreases with reducing the applied pressure on the active stamp's reservoirs or the capping membrane, which offers continuously tuneable and reversible adhesion strength with a high control. Figure 2.13 (2f-i) demonstrates the capability of this transfer printing technique to integrate inorganic microstructures, such as silicon plates, onto flexible substrates. The inflatable stamp has provided valuable proof for selective/programmable printing (Figure2.13 (2c-d)). However, this integration method introduces considerable complexity in terms of fabrication, particularly when it comes to realising the microchannels to implement the connections between the gas channels/pipes and each actuation site, and thus leads to several limitations for integrating ultra-thin inorganic micro/nanostructures for large area flexible electronics. An alternative strategy of modified transfer printing was demonstrated by Linghu et al as shown in figure 2.13(3), where the transfer printing process is triggered by employing an external field [113, 140], magnetic assisted transfer printing was developed by adding the magnetic particles into the reservoirs to deform the membrane or the elastic film and change the state of the adhesion strength based on the external magnetic field. Compared to the previous method, magnetic assisted transfer printing is considered as a simple, yet robust design realised by a built-in magnetic driving system, where there is no need to implement any complex connections to gas channels/pipes.

2.3.4 Summary and comparison of performances of transfer printing techniques

Transfer printing technology was originally developed to overcome the thermal budget challenges associated with conventional microelectronics processing for flexible electronics manufacturing. However, it can also serve as a promising approach to establish a pilot line for heterogeneous integration of smart systems in a semiconductor foundry environment for flexible electronics manufacturing. Each transfer printing integration approach has distinct assembly methodologies and characteristics determined by its working principles. As a result, the transfer printing technique has enabled the production of high-performance electronic devices on non-conventional substrates such as flexible or stretchable materials,

leading to diverse applications ranging from individual functional components, including transistors, energy-harvesting devices, light-emitting diodes, flexible capacitors, thin-film solar cells, memories, and sensors, to integrated device systems like printed flexible integrated circuits, transient electronics, flexible displays, and more. To facilitate comparison and better understanding of these techniques' differences and performances, Table 2.2 summarizes and compares their operational principles, advantages, and limitations.

Table 2.2: Summary of recent advanced strategies of transfer printing techniques used for integrating inorganic semiconducting micro/nanostructures on flexible substrate. N/A – data not available

Transfer Printing Method	Printing Principle	Material /Structures printed and dimensions	Printing process parameters			Devices	Ref.
			Fabrication difficulties	Yield	Registration accuracy		
Kinetically controlled	Adjusting the viscoelasticity of stamps at different peeling velocity	Si membrane (300nm thick)	low/ issue: high contrast in adhesion switchability	N/A	N/A	n-type FET	[141]
Bending radius controlled	Peeling velocity bending radius	Micro-scale Si plate array (7 µm thick; 760 × 760 µm)	Medium/ issue: limited to micro-scale structures	97.4 %	≈ 2000 nm	N/A	[111]
Glue assisted	Using epoxy SU8 as adhesive	Si membrane (100nm thick)	low/ issue: surface contamination	N/A	N/A	n-type FET	[93]
Adhesion promoter assisted	Using adhesion promoter (VM652)	Si NRs arrays (70 nm thick; 5 µm x 50 µm)	low/ issue: poor registartion quality	N/A	≈ 2000 nm	n-type FET	[58]
Shear-assisted inspired by Gecko	Peeling velocity with angular direction dependent	Micro-scale Si plates. (10 µm thickness)	meduim/ issue: low contrast in adhesion switchability)	N/A	N/A	Micro scale solar cell	[124]
Surface-relief assisted inspired by Aphid	Changing in contact area from stamp's shape memory effect	Micro-scale Si inks (squares, conical shapes, etc)	High/ issue: adhesion switching and temperature	N/A	1000 nm	N/A	[118]
Laser-assisted transfer printing	Laser-induced thermal mismatch	Micro-scale Si plates (100 µm× 100 µm× 0.32 µm)	High/ issue: temperaturte and require expensive equipment	N/A	1000 nm	InGaN- based µ-LEDs	[142]
Shape memory assisted polymer & laser assisted	Changing in contact area from stamp memory shape & thermal mismatch	Si nanoribbons 200 nm thick.	High/ issue: possible thermal damage, and require expensive equipment	100%	N/A	N/A	[106]

2.4 Conclusions

Transfer printing techniques facilitate the transfer, assembly, and patterning of intrinsically bendable electronic micro- to chip-scale materials, leading to significant breakthroughs in the development of flexible large-area electronics (LAE). One key advantage of transfer printing is the ability to decouple the semiconductor growth process on a rigid substrate from the device on a flexible substrate, enabling the fabrication of functional devices such as transistors, solar cells, and light-emitting diodes without the traditional requirements for epitaxy and thermal budget. These methods can be performed at temperatures compatible with plastic substrates, while still maintaining the ability to incorporate high-quality single-crystal semiconductor building blocks. However, technical challenges such as nonuniform material growth and transfer, limited scalability, and integration issues in heterogeneous and 3D integration must be addressed for the next generation of high-performance large-area electronics using printing technologies. Residues from intermediate stamps, glue/adhesive, solvent-releasable tapes, and other sources may remain on the surface of transferred micro/nanostructures, degrading device performance. Advanced modified transfer printing techniques based on dry adhesive mechanisms, such as kinetically controlled and bio-inspired transfer printing, have the potential to address these issues, but require complex and costly equipment not available in conventional microfabrication laboratories. This equipment is needed to control adhesion modulation and to design and fabricate complex micro and nanostructured geometries for the intermediate elastomeric stamp to mimic biological adhesives such as micro/nanostructured adhesives inspired by gecko. Laser assisted transfer printing can be considered the only technique that provides non-contact printing. but the process introduces high temperature, which may damage the stamp and printed structures. Recent works have demonstrated transfer printing techniques, including laser-assisted, gecko-inspired, and aphid-inspired methods, but there is still a lack of demonstration regarding their feasibility for achieving high-performance flexible electronics and circuits. In the following chapters of this thesis, I will illustrate the direct roll-based transfer printing techniques that I have developed during my research. These techniques involve printing nanostructures directly onto flexible substrates and highly

curved surfaces using high-mobility materials such as Si and GaAs. I will demonstrate the unique device-level capabilities of these techniques by showcasing p- and n-channel transistors, photodetectors, and solar cells integrated directly on flexible substrates.

Chapter 3.

Printed Nanoribbon-Based High-Performance Transistors using Soft Stamp

The work Adapted from:

Journal Articles

- **Zumeit, A.,** Navaraj, W.T., Shakthivel, D., Dahiya, R. "Nanoribbon-Based Flexible High-Performance Transistors Fabricated at Room Temperature," Adv Electron Mater, vol. 6, no. 4, p. 1901023, 2020, doi: 10.1002/aelm.201901023.

Conference Publications

- **Zumeit, A.**, Shakthivel, D., Dahiya, R. "Si Nanoribbons based High Performance Printed FETs using Room-Temperature deposited Dielectric," in 2020 IEEE International Conference on Flexible and Printable Sensors and Systems (FLEPS), 2020: IEEE, pp. 1-4. (**Best paper award**)
- **Zumeit, A.**, Dahiya, A.S., Shakthivel, D., Dahiya, R. "Silicon nanoribbons based printed transistors for high-performance flexible electronics," in 2021 IEEE International Conference on Flexible and Printable Sensors and Systems (FLEPS), 2021: IEEE, pp. 1-4. (**Best paper award**)

Abstract

Printed electronics (PE) is not yet considered a substitute for conventional Si-based electronics due to the use of low-mobility materials and long channel lengths (≥10 µm). The effective mobility of an electronic device determines important performance parameters such as switching speed, current density, power efficiency, and transit frequency (fT). While transistors based on organic thin-film transistors (OTFTs) have been developed, those realized on flexible substrates with oriented inorganic nanostructures offer a great potential for the next generation of flexible applications, such as IoT, where high performance e.g., faster communication and computation is required. However, realizing fully flexible, high-performance, and energy-efficient based electronics is still challenging due to several processing steps, such as doping profiles, deposition of high-quality gate dielectric, and

forming ohmic contacts, especially when performed at room temperature (RT). In this context, this research addresses the thermal budget associated with standard fabrication processes, optimizing the fabrication process for realizing a printable and functional high-mobility nanostructure, defining the doping profiles, transfer printing of functional elements on flexible substrates with high transfer yield, deposition of high-quality dielectric at RT, forming ohmic contacts, etc. This chapter presents a detailed study of the fabrication and characterization of Si nanoribbons (NRs) based FETs with RT-deposited dielectric for emerging flexible applications that require high performance. The distinct feature of these devices is the high-quality SiNx dielectric deposition at RT, directly on the transfer-printed nanoribbons, which is compatible with most flexible substrates.

The electrical characteristics of the fabricated devices, including mobility and current on/off ratio (e.g., for n-type FET: mobility ≈656 $cm^2\ V^{-1}.\ s^{-1}$. and current on/off ratio $>10^6$ and for p-type FET: mobility ≈85 $cm^2\ V^{-1}.\ s^{-1}$. and current on/off ratio $>10^3$) are on par with the highest performance of similar devices reported with high-temperature processes, and significantly higher than devices reported with low-temperature processes. This chapter covers the properties of room temperature-deposited SiN_x dielectric, such as gate dielectric stability under cyclic bending test, gate dielectric leakage current, surface roughness, and other properties that have been exploited in the development of both n and p-type Si-NRFETs. The demonstrated fabrication step allows the transfer printing process to be very robust and compatible with CMOS technology for the development of high-performance devices and circuits. The electrical characteristics evaluation of nanoribbon-based field-effect transistors under multiple bending cycles (100) shows excellent mechanical stability of the devices as they retain performance. The excellent response of nanoribbon-based FETs and the fabrication compatibility with diverse flexible substrates make the presented approach attractive for realizing a wide range of flexible devices, including high-performance flexible transistors, photosensors, solar cells, light-emitting diodes, etc. These functional components are highly needed in numerous emerging applications, such as conformal tactile active-matrix sensors for e-skin, digital imaging, and energy convergence systems.

3.1 Introduction

Recent progress in flexible electronics [143] has enabled advances in several emerging applications such as wearable electronics [144], electronic skin [145], epidermal electronics [146], and flexible display [147], etc. Many of these applications require fast computation and communication, which require performance at par with Si based technology. The widely explored thin films of organic semiconductors [148], 2D layered materials [149] and inorganic amorphous oxides [150] lead to devices with modest performance due to their low mobility (1-10 cm^2 $V^{-1}.s^{-1}$ against ~1000 cm^2 $V^{-1}.s^{-1}$ by Si devices), and large device channel lengths (>20 µm), etc. [151]. The ultra-thin chips (UTCs) [32, 34] have partly helped to meet the performance requirements, even if their application is limited to small and compact areas as for economic reasons and integration related difficulties, it is not practical to have them over the large areas. As a result, the printed devices and circuits based on nanostructures (NSs) of high-mobility materials such as Si nanowires (NWs), Si nanoribbons (NRs), carbon nanotubes (CNTs), GaAs NWs etc. have been explored. [33, 50, 152]. The excellent performance (e.g., high mobility and current on/off ratio etc.) offered by some of the NS-based devices is summarised in Table 3.1. A major challenge with NSs based devices is that some of the critical fabrication steps (e.g., NSs fabrication/growth, doping, high-k dielectric deposition etc.) require high-temperatures that are incompatible with the flexible substrates such as plastics. Currently, the popular method to address this issue is to transfer print NSs from the native or growth substrates to the receiving flexible substrate using a stamp or career substrate [33, 63]. Since the high temperature fabrication steps are carried out before transfer (i.e., when NSs are still on the native or growth substrates), this method decouples the high temperature process steps from the low-temperature steps (e.g., metallisation) that are carried out after transfer to realise devices on flexible substrates, as shown in Figure 3.1.

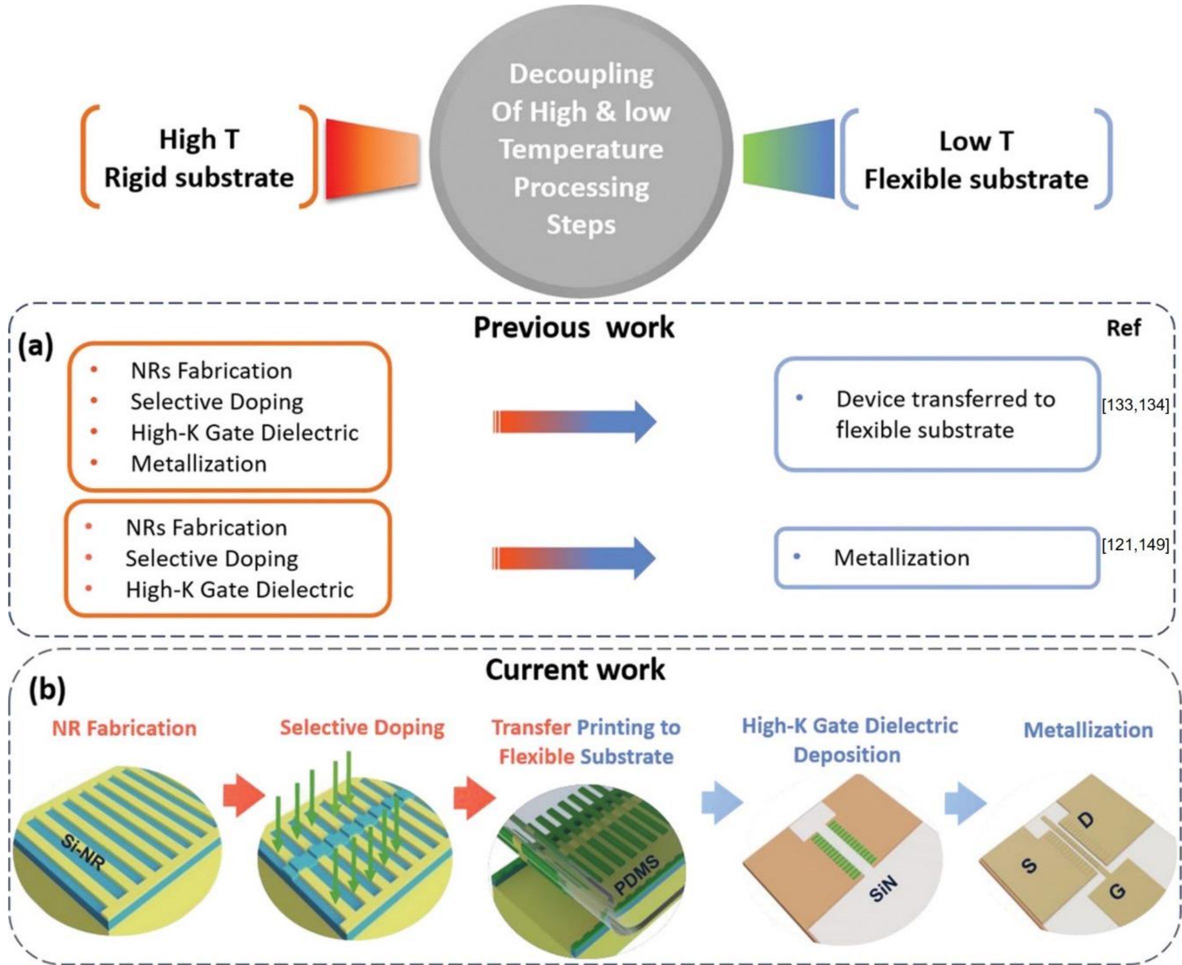


Figure 3.1: Overview of the NRFET fabrication by transfer printing process with transition from high to room temperature steps. **(a)** The previously reported works have majority of the fabrication steps requiring high temperature. **(b)** The critical fabrication steps in this work are carried out at low temperature regime suitable for flexible electronics.

Table 3.1: Si membranes or NR-based FETs with various reported gate dielectrics.

S.No.	Dielectric	Dielectric deposition temperature ($^\circ$C)	Si Micro/nano-structure morphology	Source	Channel dimensions			Mobility (cm^2/Vs)	On /Off ratio	Ref.
					L (μm)	W (μm)	T_{Si} (nm)			
1	≈2 μm SU-8	RT	Sub-μm <111> ribbons	Bulk <111> Si	100	10	115-130	360 (Lin.) 100 (Sat.)	~10^3	[63]
2	≈15 nm SAND[a]	RT	μs-Si	SOI	250	100	300	680	>10^7	[141]
3	≈90nm Tg-SiO_2	1100	Fully formed n-type MOSFETs	Custom SOI with <111> base	20	150	~2000	~710 (Lin.) ~600 (Sat.)	>10^6	[153]
4	200 nm a-SiO	RT	Sub-μm Membranes	SOI	1	2x20	200-300	423		[105]
5	100nm PECVD SiO_2	250	Fully formed n-type NR MOSFETs	Custom SOI with <111> base	10	40	~100	650 (Lin.) 530 (Sat.)	>10^5	[154]
6	100nm RT ICP CVD SiN_x	RT	Nanoribbons - Ribbon Length (55 μm)	SOI	5	50 (5x10)	70	656 (Lin.)	>10^6	This work

a) Self-Assembled Nanodielectrics

Previous works have carried out most of the steps, including high temperature dielectric deposition which yielded good device characteristics, [153, 154] before transfer printing. Transfer printing of such fully formed devices such as FETs increases the process complexities which also raises the technology cost. An alternative method is to use substrates such as metal foils, which can withstand higher processing temperatures. However, additional fabrication steps such as insulation on foils etc. increase the cost of fabrication and for this reason manufacturing through low-temperature processing steps is preferred. The low-temperature processing keeps the transfer printing process highly robust and could aid fabrication of FETs over large area flexible substrates as it is compatible with methods such as roll-to-roll technology. Thus, the key challenge is to develop high-performance NRFET by dielectric deposition preferably at RT. Many experimental techniques, such as Atomic Layer Deposition (ALD), Low-Pressure Chemical Vapor Deposition (LPCVD), Plasma Enhanced (PE)-CVD, Inductively Coupled Plasma (ICP)-CVD, e-beam evaporation etc., have been successfully used to develop high quality dielectric films in the past[155]. ALD and LPCVD techniques typically use growth temperatures more than 250 ˚ C, which are not suitable for direct deposition of dielectrics over flexible materials. Similar issue arises using PECVD along with additional problems such as plasma induced damage, active layer degradation, high charge trapping, increased concentration of defects (dangling Si bonds), ohmic contact degradation, etc. [156]. In this regard, the ICP-CVD offers unique advantage as it allows high quality dielectrics (SiO_x, SiN_x etc.) at room temperature without any harmful effects [157, 158]. SiN_x is a widely explored gate dielectric material for III-V devices and oxide thin film transistors (TFT) exhibiting good performance [156]. Herein, we demonstrate the flexible Si NRs (55 µm (L) x 5 µm (W) x 70 nm (T)) based FET developed over flexible PI substrates using a room temperature ICP-CVD deposited SiN_x (100 nm thickness) as the gate dielectric. The SiN_x dielectric film was observed to be very smooth (~0.4 nm roughness), crack-free and deposited with high stoichiometry (Si:N ratio). The low deposition temperature, appreciable dielectric constant (~9), low interface traps, CMOS compatibility, combined with ICP-CVD process is highly beneficial for Si NRFETs, which operate with high current on/off ratio ($>10^6$), low leakage

current and high mobility (~656 cm^2/Vs) under multiple mechanical bending cycles. The NRFET device characteristics show that the low temperature SiN_x dielectric film holds advantage compared to the SiO_x and a-SiO deposited using other techniques. The RT ICP-CVD dielectric deposition process is compatible with flexible polymeric substrate and could be a key step forward for the development of high-performance large area flexible Si NRFETs.

Advantages of NRs array structure:

The structure of nanoribbon (NR) arrays has been selected as such since the frame structures plays a significant role in terms of improving the transfer yield particularly when it comes to transfer nanoscale structures onto flexible substrates [159]. In previous work, an optimization study of the dependency of Si frame architectures on transfer yield was demonstrated, and the highest transfer yield was found for structures with frames that have densely spaced strips with a 1:1 spacing ratio (NR width: NR spacing) [159, 160]. The aim of selecting multiple Si NRs connected in a single frame (Single array) is to enhance the device on-current and reduce the device-to-device performance variation which is critical for realising high performance transistors over large area.

Working principle and main electrical parameters of Si NRs FET

Si-NRs FETs operate on a principle similar to MOSFET transistors, and their performance can be evaluated by measuring crucial electrical parameters. These include the threshold voltage (V_{th}), subthreshold slope (S), on/off current ratio (I_{ON}/I_{off}), and field effect mobility of charge carriers in the on state (μ_{eff}).

A Si-NRs FETs device consists of three terminals (source, drain and gate), working in either enhancement/depletion. The source (S) and drain (D) of the Si-NRs FET are separated by 2D nanostructured of semiconductor material (Si-NRs) called “channel length” which is electrostatically coupled to the third electrode of the transistor called “gate”. Since a transistor performance is dominantly operated by the electrostatic control over the device channel, carried out by the applied gate-source voltage (V_{GS}) rather than drain to source voltage (V_{DS}). Therefore, the operation principle of Si-NRs FET depends on enrichment of

charge carries in the channel region. It means that, when the device operates under enhancement mode, there is no channel between the source and drain terminals, so when the gate to source voltage applied and reaches a certain value (V_{th}). A conductive path (channel) is created by accumulation of the majority of charge carriers (electrons for n-type FET or holes for p-type FET), this allows the majority of the charge carriers to enter the channel and current flow from source and drain terminals is established.

Off state condition:

In enhancement mode, the Si-NRs FET operates by creating a conductive path (channel) between the source and drain terminals through accumulation of the majority charge carriers (electrons for n-type FET or holes for p-type FET) when a gate-source voltage of a certain value (V_{th}) is applied. Under off-state conditions ($|V_{GS}| < |V_{th}|$), the gate voltage is insufficient to create a conductive channel, and weak leakage current (I_{off}) can still flow between the source and drain due to inverse polarization.

On state condition:

When the gate-source voltage exceeds the threshold voltage ($|V_{GS}| > |V_{th}|$), a channel of charge carriers is induced between the source and drain, allowing current to flow through the conductive channel by drain-source polarization. The Si-NRs FET is then in the on state and operates in either the linear regime or saturation regime, as shown in figure 3.2b.

Si-NRs FET electrical characteristics

a) <u>Transfer characteristics</u>

The transfer curve as shown in figure 3.2a corresponds to the electrical measurement of current I_{DS} as a function of the gate voltage V_{GS}, when the drain voltage V_{DS} is constant. Figure 3.2 presents a typical transfer characteristic. Four operation regions of Si-NR FET can be defined from graph (a) shown in figure 3.2. The region (1) represents the operation condition of Si-NRs FET under Off state, with $I_{DS} = I_{off}$ due to trapped charge carriers in the channel region and accelerated by the strong inverse polarisation at the drain region. The region (2) represents the ohmic conduction for intrinsic semiconductors. The region (3) represents the formation of the conductive channel, resulting in a significant increase in I_{DS}

with applied gate voltage V_{GS}. The region (4) represents the on-state current of Si-NRFET ($I_{DS} = I_{ON}$). Overall, the Si-NRs FET's operation depends on the creation of a conductive channel between the source and drain terminals, controlled by the gate-source voltage. The transfer curve can be used to identify the different operation regions of the Si-NRs FET, including the off state, ohmic conduction, formation of the conductive channel, and on state.

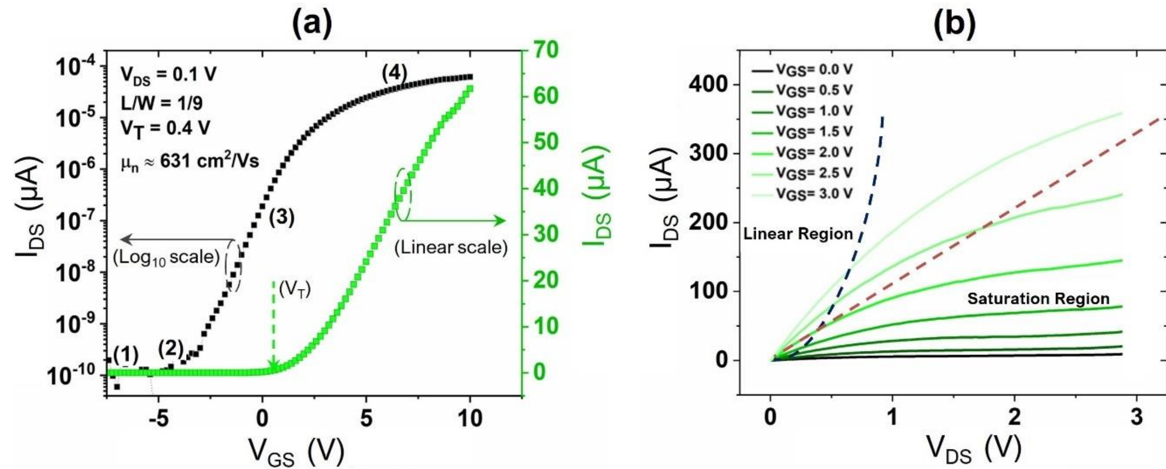


Figure 3.2: (a) Transfer characteristic for n-type Si-NRs-FET; drain current I_{DS} in both linear (right y-axis, green coloured showing the threshold voltage) and logarithmic (left y-axis, black coloured, showing the main operation regions of FET 'numbered'). **(b)** Output characteristic for the device; showing linear and saturation regions at different applied gate voltage (V_{GS}= 0 to 3V, step of 0.5V) [161].

b) Output characteristics

Figure 3.2b illustrates a typical output characteristic of a Si-NRFET and the corresponding I_{DS} values at different gate biases. The output characteristics indicate the variation of I_{DS} with respect to the drain-source voltage V_{DS} under constant input gate voltage V_{GS}. As depicted in Figure 3.2b, the linear region is evident under low VDS, whereas the saturation region occurs when the drain voltage V_{DS} exceeds ($V_{GS} – V_{th}$).

Linear Region

When low drain-source voltage bias applied ($V_{DS} \leq V_{GS} – V_{th}$), the drain-source current I_{DS} is expressed by:

$$I_{DS}=\frac{W}{L}\mu C_{OX}(V_{GS}-V_{th})V_{DS}-\frac{V_{DS}^2}{2}) \qquad (3.1)$$

Where W is representing the width of the device channel (µm), L(µm) is the channel length (µm), µ is the field effect channel mobility (cm^2/V. s), C_{OX} is the gate capacitance per unit area (F/cm^2), V_{th} is threshold voltage.

When a very low drain-source voltage bias is applied ($V_{DS} << V_{GS} – V_{th}$), the channel region of the device has a constant conductance and behaves like a resistor. The channel resistance is determined by the dimensions of the transistor's channel (W/L), and resembles an ideal resistor based on Ohm's Law. The channel resistance depends on the charge carrier concentration in the channel region, which is a function of the gate bias. As shown in Figure 3.2b, as the gate voltage increases, the slope of the current-voltage characteristic gradually increases based on the connectivity of the channel. The current variation is directly proportional to the applied drain-source voltage V_{DS} for small V_{DS}. Equation (3.2) describes the drain current I_{DS}, and the expression for drain current is given by:

$$I_{DS}=\frac{W}{L}\mu C_{OX}(V_{GS}-V_{th})V_{DS} \quad (3.2)$$

The transconductance g_m or “transfer conductance” and is given the unit of Siemens (S), g_m is another important parameter of the FET that characterizes the relationship between the drain current I_{DS} and the applied gate-source voltage V_{GS}. It is defined as follows:

$$g_m=\frac{\partial I_{DS}}{\partial V_{GS}}= \frac{W}{L}\mu C_{OX}V_{DS} \quad (3.3)$$

The value of transconductance indicates the quality of gate control over the channel, since it relates the drain current to the gate voltage. Additionally, transconductance has a special significance, as the gain of the transistor is directly dependent with the transconductance g_m with a relation:

$$A_v = g_m/g_d \quad (3.4)$$

Where A_v is the intrinsic gain of FET and g_d is the output conductance of the drain and it’s defined by ($\partial I_{DS}/\partial V_{DS}$), and it can be extracted from the slope in the output characteristics (I_{DS}-V_{DS}).

Saturation Region

When the value of drain-source voltage V_{DS} reaches (V_{GS} - V_{th}), a pinch-off occurs on the drain side, and V_{DS} (saturation) is reached. If the drain-source voltage continues to increase

from V_{DS} (saturation), the pinch-off point moves from drain to source. The resistance of the depletion region is greater than that of the channel region, resulting in the drain current remaining at an approximately constant value known as the saturation current (I_D saturation), which becomes independent of V_{DS}. The expression for the drain current in saturation can be derived from the current in the linear region, as shown in Equation (3.5). Therefore, $I_{DS(sat)}$ can be given by:

$$I_{DS_{Sat}} = \frac{W}{L} \mu C_{OX} (V_{GS}\text{-}V_{th})^2 \qquad (3.5)$$

Subsequently, the transconductance can be derived from the relation as shown below:

$$g_{m\ (Sat)} = \frac{\partial I_{DS}}{\partial V_{GS}} | V_{DS} = \frac{W}{L} (V_{GS}\text{-}V_{th}) = \text{constant} \qquad (3.6)$$

Threshold voltage

The working principle of Si-NRs FET is based on the conventional MOSFET design, where the threshold voltage V_{th} is the gate voltage at which sufficient inversion of charge carriers occurs to create a low-resistance conducting path called the channel or inversion layer. V_{th} is a critical parameter required to extract other device parameters, such as mobility. The threshold voltage is typically determined using the linear extrapolation method, based on the I_{DS}-V_{GS} characteristics obtained at low drain voltage to ensure operation in the linear region. The threshold voltage can be calculated using the following equation:

$$V_{th} = V_{GS} - \frac{V_{DS}}{2} \qquad (3.7)$$

Where V_{GS} is the voltage intercept of the extrapolated linear region in I_{DS}-V_{GS} characteristics.

Effective mobility (μ_{eff})

Effective mobility is a key performance parameter for Si-NRFETs, as it determines the speed at which carriers can be transported through the active channel, ultimately influencing the device performance. The mobility is defined as the ratio of carrier velocity to the applied electric field. In general, higher effective mobility corresponds to higher drain current that can be driven by the transistor. To extract the effective mobility, the I-V characteristics are typically measured in the linear region. Specifically, at low V_{DS}, the effective mobility can be estimated using the following equation:

$$\mu_{eff}= \frac{L}{W}\frac{g_d}{C_{ox}(V_{GS}-V_{th})} \quad (3.8)$$

Sub-threshold swing (s-s)

The subthreshold swing (s-s) of the transistor corresponds to the amount of change in the channel conductivity with respect to the change of applied gate voltage, At the subthreshold regime, the subthreshold swing (s-s) can be extracted from the logarithmic transfer characteristics (I_{DS}-V_{GS}) by numerical differentiation based on following equation (3.8) and it's expressed in V/dec.

$$\text{s-s}= \frac{1}{\partial \log(I_{DS})/\partial V_{GS}} \quad (3.9)$$

For standards MOSFETs, s-s value can also be determined by:

$$\text{s-s}= \frac{KT}{q}\text{In}10\left(1+\frac{C_D}{C_i}\right) \quad (3.10)$$

Where k is the Boltzmann's constant, T is the temperature, C_D is the depletion layer capacitance and Ci is the insulator capacitance. From Eq. 3.9 if $C_D = 0$, s-s will be equal to ~60 mV/dec, which is the fundamental limit and the ideal case for MOSFETs. However, when the applied gate voltage is less than the threshold voltage, the subthreshold slope depends significantly on the defects in the active material and at the gate insulator/active layer interface, leading to a reduction in the channel conductivity dependence on the applied gate voltage, which increases the s-s value. Therefore, a high subthreshold slope indicates a large number of trap charges in the channel of the transistor or at the gate insulator/active layer interface. The current state-of-the-art value of s-s in Si MOSFETs is ~70 mV/dec. A low value of s-s is required for fast switching between an on-state and off-state in the transfer characteristics of the transistor.

Current on/off ratio (I_{on}/I_{off})

The current I_{ON}/I_{OFF} ratio is a measure of the ratio between the drain current at the highest V_{GS} and the off-state current, and the higher this ratio is, the better the performance of the transistor. It is important for the drain current I_{DS} in the on-state to be as high as possible, while the off-state current should be low. These two current values, I_{ON} and I_{OFF}, can be obtained from the I_{DS}-V_{GS} curve in a linear-logarithmic plot. I^{ON} represents the maximum I^{DS} on the transfer characteristic, while I^{OFF} corresponds to the minimum I^{DS} at off-state.

The on-state current is primarily determined by the effective mobility, quality at the metal/semiconductor interface, and quality of gate coupling, while the off-state current depends on the semiconductor bandgap, doping concentration in the active material, and quality at the metal/semiconductor interface. A high value of the on/off current ratio ($>10^6$) is essential for applications that use digital logic, as this parameter represents the variation between the levels of the logic gates '0' and '1'. In this work, we have attempted to utilize the transfer printing of Si NRs on a flexible substrate to create flexible FET devices with performance parameters close to that of an ideal FET.FET.

3.2 Experimental Section

3.2.1 Si nanoribbons (NRs) fabrication

A top-down approach is used to fabricate silicon (Si) nanoribbon with uniform geometry been realised using commercial SOI wafers, which consist of 70 nm top Si (100) layer over 2 µm of buried oxide, supported by 600 µm bulk Si as shown in Figure 3.3. SOI wafer is employed in this process as a source wafer, mainly because it is ideal choice to obtain single crystal Si nanoribbon, through lateral etching of SiO_2 buried oxide layer using wet etching solution. Figure 3.3 illustrates the steps involved in fabrication of NR-FETs. The diced wafer samples were cleaned using acetone, iso-propyl alcohol (IPA) and deionized (DI) water to remove the surface contaminants. Si NRs (5 µm (W) x 55 µm (L)) were defined by employing spin-coated S1805 photoresist (4000 rpm for 30 s), followed by soft baking at 115 °C for 60 s (Figure 3.3a–d). The samples were exposed to UV source (Suss MicroTec-MA6) for 4 s and subsequently the NRs patterns were developed by using MF 319. The photoresist served as a mask to protect Si nanoribbons (~5 µm wide and ~55 µm long) for subsequent step of wet etching the exposed top silicon layer of SOI wafer.

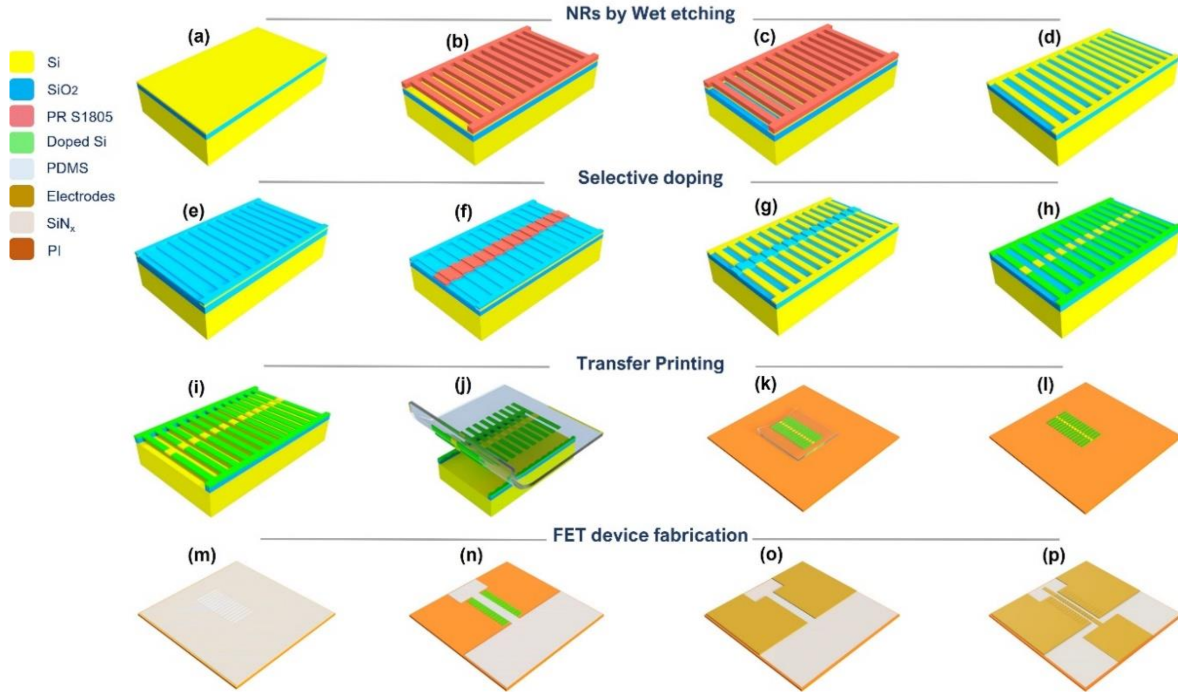


Figure 3.3: Schematic diagram of the four stages of the Si NRs based device array fabrication (a-d) Si NR array patterning, **(e-h)** Doping process, **(i-l)** Transfer printing, **(m-p)** FET device fabrication.

The wafer was baked in 120°C for 10min in a convention oven followed by oxygen O_2 plasma treatment at 150 W RF power for 1 minute. The etching of UV exposed Si regions, using solution of nitric acid, ammonium fluoride, and DI water in a ratio of (126 HNO_3 : 60 H_2O : 5 NH_4F) for an optimized 120s, the etching solution has the etch rate of ~150 nm/min. The sample was deliberately etched for 2mins to ensure that silicon is completely etched away in order to achieve the following steps successfully. The unexposed photoresist was removed using acetone and isopropanol (IPA) with ultrasonic agitation, then abundantly rinsed with de-ionized (DI) water and dried with stream of nitrogen, thus resulted in the array of NRs attached with Box (Figure 3.3d). The selective source–drain doping of NRs was carried out using 150 nm thick SiO_2 mask layer deposited using plasma-enhanced chemical vapor deposition (PECVD) (Figure 3.3e). The SiO_2 film served as a mask burrier during diffusion doping process and to control where the dopant diffuses into silicon layer. The active regions (source and drain) of NRFET device were defined over SiO_2 mask layer by spin-coating photoresist (S1805, 4000 rpm) followed by UV exposure (3 s) (Figure 3.3f). The resist served as a mask for selective dry etch process of the doping mask and open up the active regions

of source and drain. The exposed SiO_2 mask areas were etched by reactive ion etching (RIE) system (40 sccm CH_3/Ar gas sources with a chamber base pressure of 30 mTorr, 200 W RF power for 4 min) (Figure 3.3g). The high temperature selective doping of source/drain regions was carried out in a resistive heating tubular furnace system under inert N2 gas ambience (Figure 3.3h). The spin-on dopant process was optimised and carried out at temperatures of 950 °C and 1050 °C for p-type and n-type doping respectively [39]. The selective doping via thermal diffusion of phosphorous and boron from spin on dopant (SOD) process was optimised, leading to desired final doping concentration $8\pm 2 \times 10^{18}$ cm^2 s^{-1}. The n+ and p+ doping was performed by employing diffusant source of phosphorus (P509, Filmtronics) and boron (B202, Filmtronics) dopants respectively in order to achieve an ohmic contact. Further, the SiO_x dopant diffusion barrier layer was removed using buffered oxide etchant (BOE-5:1). At this stage, the Si NRs with defined doped regions were firmly attached with the bottom BOx layer. The next process is releasing Si nanoribbons from the buried oxide of SOI source wafer, this step was achieved by etching the exposed 2µm thick buried oxide. A wet etching step using hydrofluoric acid HF acid leads to the releasing of NRs from the bulk wafer with anchoring points at both ends (Figure 3.3i), this step is very critical to ensure the Si ribbons are completely released into free-standing structure, and suspended after etching underlying buried oxide layer, thus ribbons can be transferred onto a flexible substrate using elastomeric a polydimethylsiloxane (PDMS) stamp. The optical images obtained after doping Si NRs arrays and etching the buried oxide layer are shown in Figure 3.4.

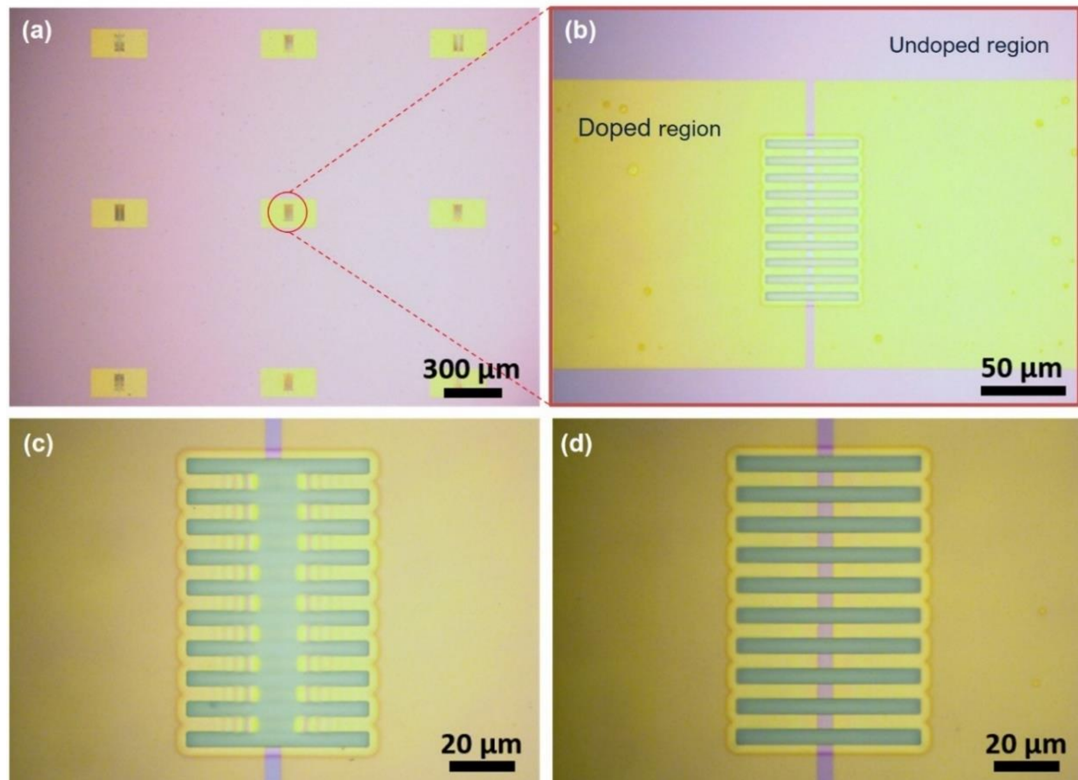


Figure 3.4: (a-b) Optical microscopy images of Chemical etching and NRs releasing. After selectively doped Si NRs are released from the wafer and suspended by removing the buried oxide layer underneath. **(c)** buried oxide overly etched where the central regions of Si NR array started touching the base bulk silicon (handle layer).

3.2.2 Conventional Transfer printing of ultrathin Si nanoribbons

The doped NR arrays were then transferred to polyimide (PI) substrate using an intermediate PDMS stamp (Figure 3.3j). A thin PDMS stamp (Sylgard 184 with 10:1 ratio of base and curing agent) of ≈2 mm thickness was prepared by casting and curing on a bare Si wafer. The printing process of Si nanoribbons is achieved in two steps via PDM stamp. First by placing the PDMS stamp with Si nanoribbons on its surface against the source SOI wafer, however before retrieval process, the PDMS and the ribbon wafer were exposed to oxygen plasma to functionalise the PDMS surface and enhance the adhesion, which allows the ribbons sample and PDMS to be bonded together by hydrophilic interactions. The PDMS stamp with a gentle pressure (≈50 kPa) was applied over the suspended NR arrays to form conformal contact between PDMS stamp and the top surface of the donor wafer, this force is sufficient to break the connections between the ends of the ribbons and their substrate. Thus, peeling off the PDMS carefully from the source substrate, led to retrieve

the array of Si ribbons, figure 3.5 represents the resultant optical images of process procedures of transfer printing, begins from transferring the Si NRs from the donor substrate (SOI) onto receiving substrate (PI) via intermediate elastomeric stamp (PDMS). The transfer of NRs on the stamp over PI

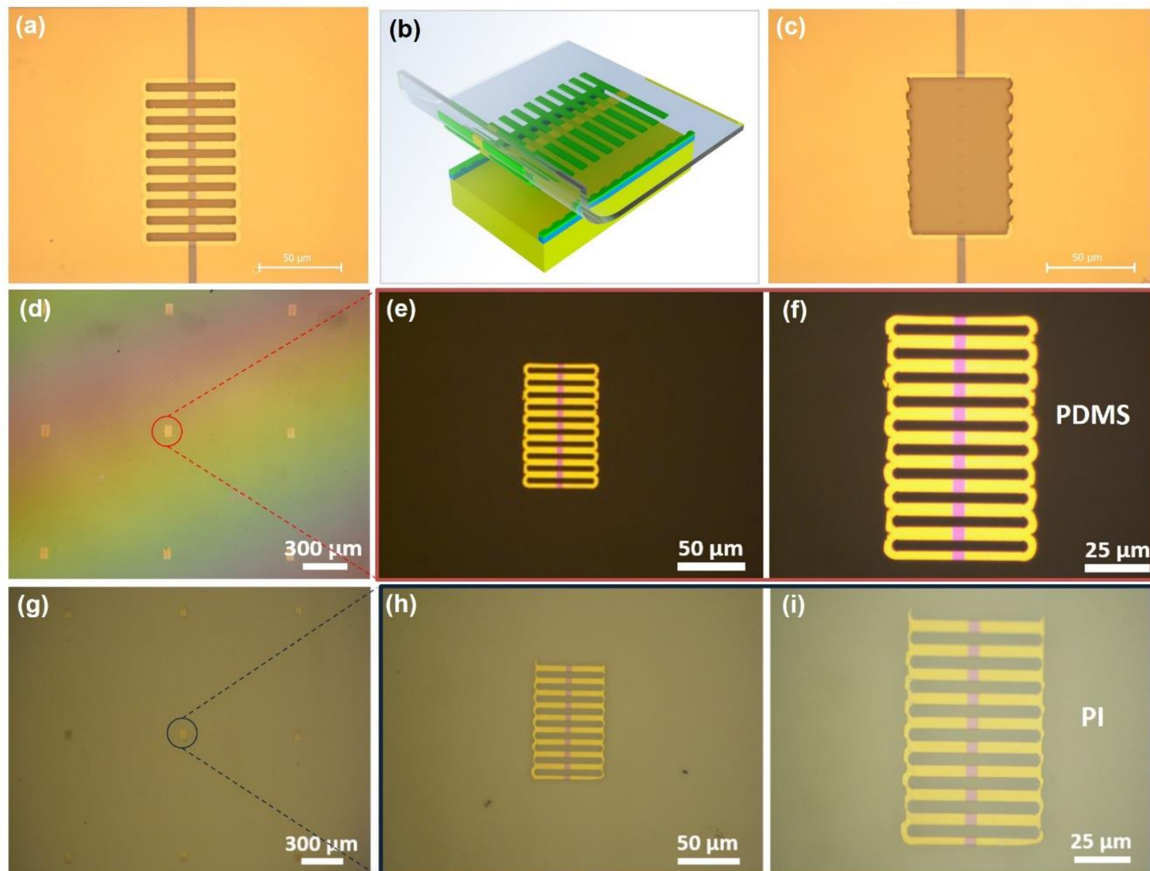


Figure 3.5: (a) Selectively doped Si NR array on the SOI donor substrate before transfer printing. **(b)** Schematic illustration of transfer printing (retrieval step) using elastomeric stamp. **(c)** SOI donor substrate after transferring Si NR array. **(d-f)** Optical microscopy images at different magnifications of selectively doped Si NRs transfer printed on elastomeric (PDMS) stamp. **(g-i)** Si NRs transfer printed onto polyimide (PI) substrate from the elastomeric stamp.

substrates were enhanced by coating a thin layer adhesion promoter, VM652 on PI substrate. Next soft baking at 90°C for 30 min was carried out to increase the Si NRs bonding to the PI film, and finally stamp with Si NRs on the PI substrate dipped into PDMS etchant solution, to carry out, wet etching process of the stamp, using etchant solution (1% weight concentration) of tetrabutylammonium fluoride in propylene glycolmethyl ether acetate [162] to expose the NRs. The process ensured that the integrity of as fabricated NRs was preserved during transfer printing over PI substrate, as shown in Figure 3.5 (g-i).

The capability of this transfer printing technique has been demonstrated by realising high performance field effect transistor (FET), where the gate dielectric film, SiN_x (100 nm), was deposited over NRs using RT Inductive coupled plasma (ICP-CVD) system [158] to form the gate dielectric. The optimized SiN_x recipe consisted of SiH_4/N_2 flow rate 7/6 sccm, ICP source RF power of 100 W; chamber pressure of 7 mTorr. The active regions were selectively patterned by dry etching of SiN_x. It is very critical to ensure that the dielectric layer is sufficiently etched to avoid a poor source-drain contact after defining the metal contacts. The metal contacts (Ti (10 nm)/Au (90 nm)) for gate, source, and drain were deposited using e-beam evaporation tool, this is followed by lift-off process, the fabrication of the device finalised with post metallisation annealing at 250°C for 30 minutes in a forming gas ambient (N_2+4% H_2) to improve the contact interface and form a low resistance ohmic contact to the device structure, as depicted in (Figure 3.6).

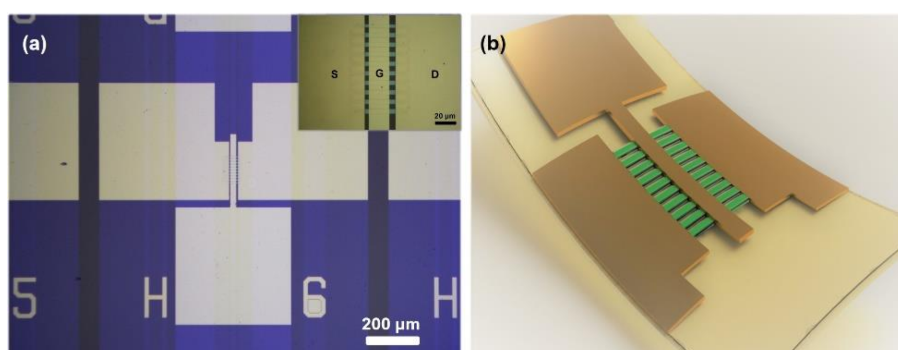


Figure 3.6: (a) Optical microscopy image represent Si NRFETs fabricated on flexible substrate (PI) based on transfer printing process using elastomeric stamp. Inset shows a magnified image of the corresponding Si NRFET. **(b)** Schematic illustration of the final device.

3.3 Results and Discussion

3.3.1 n-type Si NRs FET by conventional transfer printing

Si NRFETs fabrication process involves four major steps, (1) Chemical etching, (2) n+ doping of source and drain regions, (3) transfer printing of functional nanoscale element and (4) FETs fabrication. The detailed fabrication processes are illustrated schematically in Figure 3.3. The schematic diagram of the obtained devices and the microscopy images of various stages of the development of flexible Si NRFET are shown in Figure 3.7. The selective wet etching of top Si layer results in well-defined Si NRs with uniform interspacing

(Figure 3.7c). The channel region was protected from source and drain n^+ spin-on-doping process by the SiO_x mask (Figure 3.7d). The devices have a channel length of 5 µm, gate overlap length of 5 µm and the effective channel width of 50 µm (10 ribbons × 5 µm each). The BOx layer etching process led to the suspended Si NRs strongly anchored at both NR ends with the Si layer (Figure 3.7e). As observed in the cross-sectional image of Si NRs (Figure 3.7f), the etching process produced smooth sidewalls without any undercut. The process steps depicted through microscopy images in Figure 3.7(c-e), were carried out using a commercial SOI wafer resulted in suspended Si NRs array. The transfer printing is introduced at this stage and the remaining steps in the device fabrication are carried out at low temperature. The microstructure of RT ICP-CVD deposited SiN_x dielectric thin film (thickness-100 nm) over Si NR is shown in Figure 3.7g. The key factors that govern the effectiveness of any dielectric material are internal stress, chemical composition, surface roughness, interfacial defects etc. These factors are mostly influenced by their deposition technique. Here, the dense dielectric film was found to be uniform across the NR thickness with good surface adhesion. Typically, the tensile stress in dielectric films promotes cracking and compressive stress enhances its peeling. The microscopic observations (Figure 3.7g) show that these were found to be absent in the SiN_x film. The stoichiometry of the SiN_x analyzed using EDX measurement (Hitachi SU8240-EDX) (Figure 3.7h), shows strong peaks of Si and N with an estimated Si/N ratio ~0.7, which is close to the stoichiometry of Si_3N_4. The weak oxygen signal could have been raised from the ambient or surface adsorbed atoms.

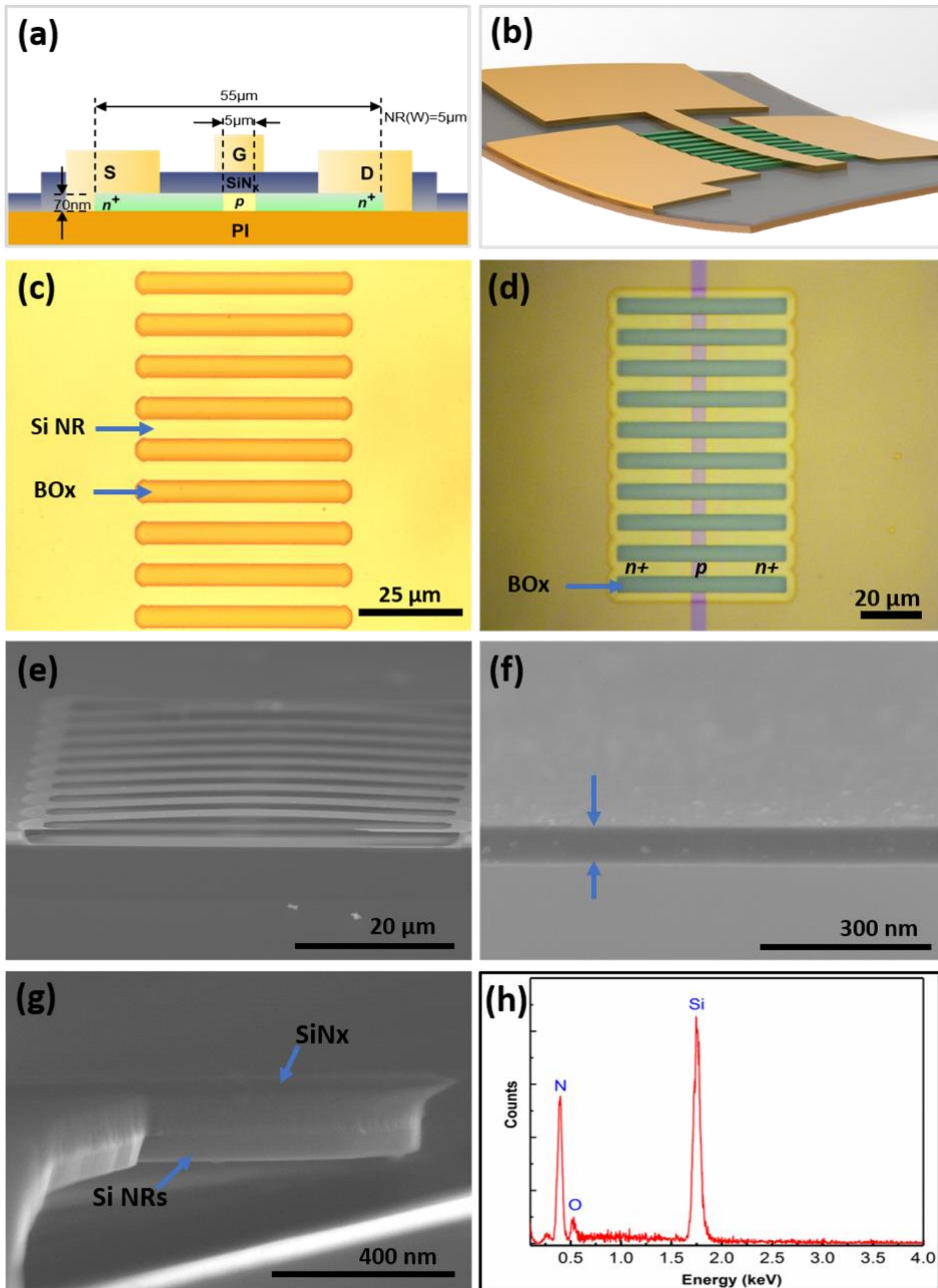


Figure 3.7: **(a)** Schematic 2D cross sectional structure of the single NRFET. **(b)** Schematic 3D illustration of the array of NRFETs on flexible substrate. Structural characterization of Si NRFETs at various fabrication stages. **(c)** Si NRs definition **(d)** selective doping at source and drain regions **(e)**. Cross section SEM image of suspended NRs array **(f)** Cross section of single Si NR structure **(g)** Cross section of Si NRs with SiN_x dielectric (h) EDX spectrum of the SiN_x dielectric film.

The good stoichiometry ratio of Si/N confirms the high quality of film deposited at the room temperature. This eliminates the issues with other deposition processes such as LPCVD and PECVD which deteriorate the flexible substrates and the channel. For example, high energy plasma could affect both the PI substrate and the NRs surface, which eventually affects the device performance. Figure 3.8(a) shows the SEM image of a NRFET, comprising of 10 nanoribbons as active channel, with the Source (S), Drain (D) and Gate (G). Figure 3.8(c) shows the photograph of fabricated Si-NRFET array with RT deposited ICP CVD SiN_x wrapped around a vial with radius of curvature 7.5mm.

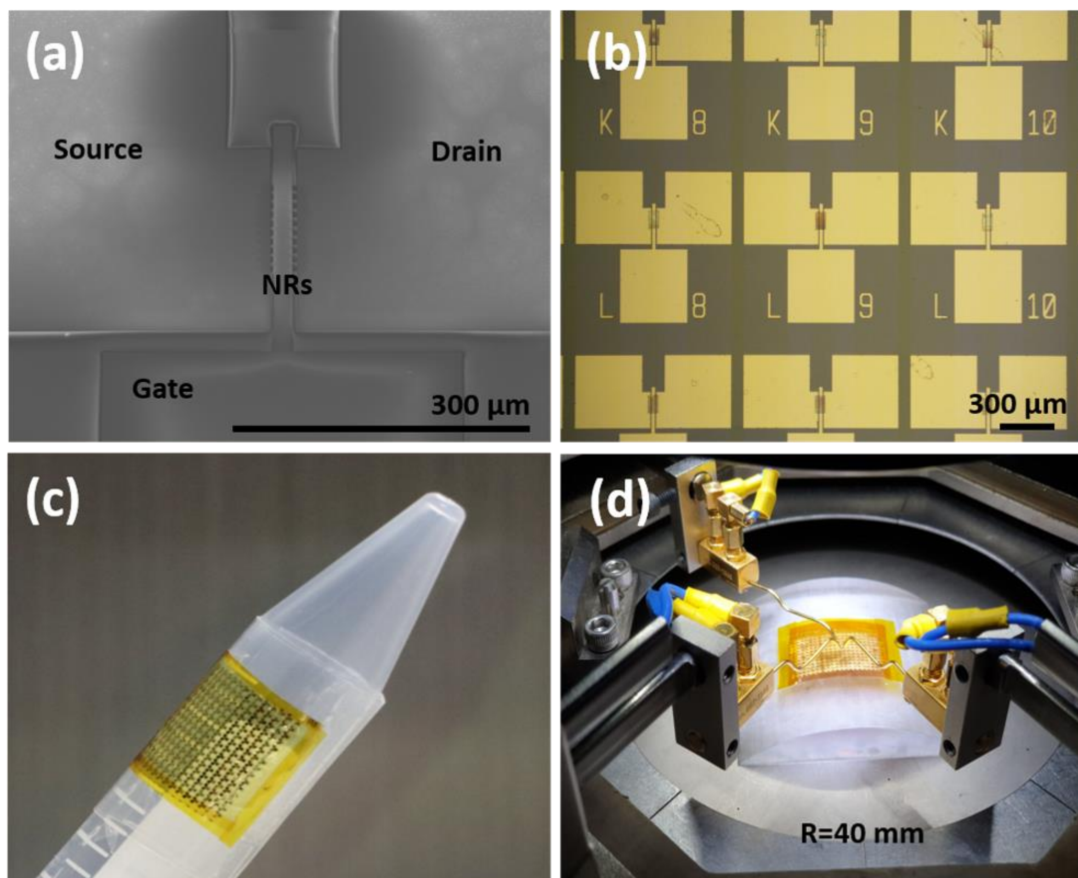


Figure 3.8: **(a)** SEM image of a representative NRFET with the Source (S), Drain (D) and Gate (G) electrodes labelled in it comprising of 10 nanoribbons as active layer. **(b)** Optical microscopy image of NRFETs array transferred on PI substrate. **(c)** Photograph of flexible NRFETs on PI substrate wrapped on a curved surface. **(d)** Illustration of electro-mechanical characterization of the fabricated NRFET with bending.

The devices were tested using Cascade Micro-tech Auto-guard probe station interfaced to an Agilent B1500A semiconductor device parameter analyzer. The fabricated devices were tested for their flexibility and mechanical stability as illustrated in Figure 3.8(d) to observe

the effect of bending stress. For this purpose, the device arrays were placed on to 3D printed convex and concave structures both with radius of curvature of 40 mm. In convex bending, the device comes under tensile stress whereas it experiences compressive stress in the case of concave bending. The transfer and the output characteristics of the transistor are shown in Figure 3.9(a) and Figure 3.9(b) respectively.

The mechanical bending and the resulting strain are known to affect the band structure of the material, which affects the effective mass and hence the mobility of the charge carriers [34, 163]. Analytical equations relating the stress with the mobility and drain current can be used to model these variations [34, 36].

$$\mu_{(stress)}=\mu_o\left(1\pm\Pi_\mu\sigma\right) \quad (3.1)$$

Where μ_o, $\mu_{(stress)}$, Π_μ and σ are the mobility under normal condition and stressed condition, piezo-resistive coefficient, and the stress, respectively. Since the NRFET is fabricated as n-channel device, the resistance decreases with tensile bending as it leads to overall increase in the current. Conversely the compressive strain leads to a decrease in the drain current. This is reflected both in the transfer characteristics and the output characteristics. Table 3.2 indicates a summary of the main parameters calculated using the electrical characterization of the fabricated NRFET under planar and bent conditions. The effective surface mobility μ_{eff} was calculated by using following equation:

$$\mu_{eff}=\frac{L}{W}\frac{g_d}{C_{ox}(V_{GS}-V_{th})} \quad (3.2)$$

Where L and W refer to the channel length and the effective width of the NRFET, g_d is the drain conductance, C_{ox} is the oxide capacitance, V_{GS} is the gate source voltage and V_{th} is the threshold voltage. Since the NR is 70 nm thick, the thickness was considered negligible, and the effective width was considered as 50μm (10 ribbons × 5 μm each). The threshold voltage (extracted from linear extrapolation method [164]) is -0.87 V, which may not be suitable for CMOS digital application because of the high current at V_{GS} of 0 V. However, this could be tuned by channel ion implantation or by optimizing the work function of the

gate metal to push the threshold voltage toward enhancement mode operation. The drain conductance is given by the equation:

$$g_d = \frac{\partial I_D}{\partial V_{DS}} |V_{GS}=\text{Constant} \quad (3.3)$$

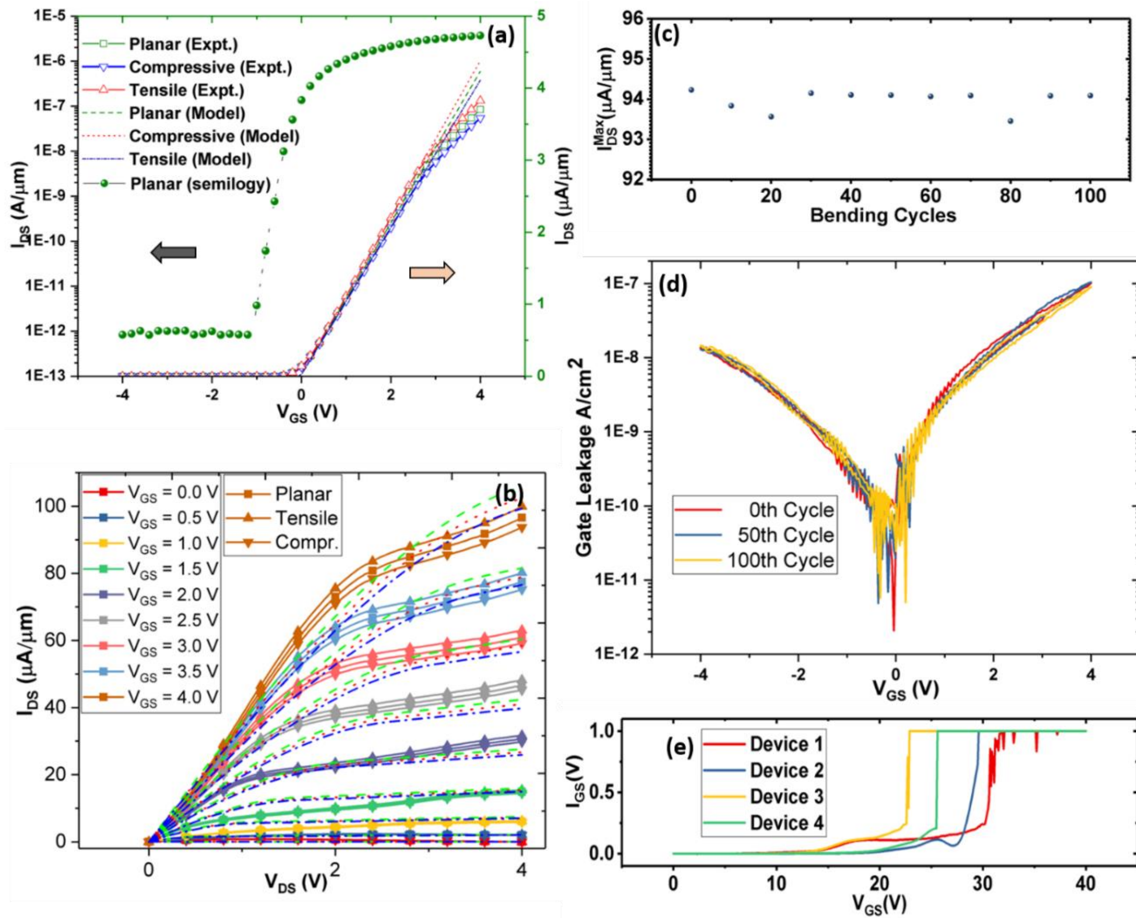


Figure 3.9: **(a)** Transfer characteristics [Experimental (line) versus model (dashed) simulations [34]] and **(b)** output characteristics of the NRFET at planar, tensile and compressive bending conditions (Rc=40 mm). **(c)** Variation of the drain current at planar condition after cycles of compressive and tensile bending at $V_{DS}=V_{GS}=4$ V. **(d)** Gate dielectric leakage current Vs gate voltage after subjecting it to cyclic bending. **(e)** Breakdown voltage characteristics of four randomly chosen devices after subjecting to cyclic bending of 100 cycles.

Table 3.2: Various parameters related to NRFET characteristics.

Parameters	Tensile Strain	Planar	Compressive Strain
Bending Radius of Curvature R_C	40 mm (Convex)	-	40 mm (Concave)
Effective Mobility (Experimental) μ_{eff}	679 cm^2/V-s	656 cm^2/V-s	637 cm^2/V-s
Saturation Current ($I_{D\text{-}sat}$) at V_{DS}=V_{GS}=4V	96.24µA/µm	93.67µA/µm	90.86 µA/µm
Drain Conductance (g_d)	42.72 µS/µm	41.28 µS/µm	40.08 µS/µm
Transconductance (g_m)	1.129µS/µm	1.093 µS/µm	1.058 µS/µm

Based on the obtained output characteristics, the drain conductance at tensile, planar and compressive conditions were estimated by numerically differentiating the drain current with reference to the drain-source voltage and their values were 42.72, 41.28 and 40.08 µS/µm respectively. Peak transconductance (g_m) of the NRFET was calculated under planar and bending conditions, by numerically differentiating the values extracted from I_D-V_{GS} data, according to the following equation:

$$g_m = \frac{\partial I_D}{\partial V_{GS}} \Big| V_{DS} = \text{Constant} \qquad (3.4)$$

The estimated effective surface mobility for the three conditions, tensor, planar and compressive were 679, 656 and 637 cm^2/Vs, respectively.

The performance of NRFETs is compared in Table 3.1 with previous works based on Si-membrane/ribbon-based devices with best reported performances for various dielectric materials. In this regard, NRFETs with ultra-violet (UV) curing and spin coating of SU8 have been explored in the past as the gate dielectric [43, 93]. Spin-coating leads to non-uniform films compared to other conventional processes such as chemical vapor deposition (CVD), thermal oxidation or atomic layer deposition (ALD) [165]. The devices using SU-8 based dielectric showed ~360 cm^2/V.s maximum linear-regime electron mobilities (μ_{eff}-lin) and the on/off current (I_{on}/I_{off}) ratio in the order of 10^4 [63, 93]. Other low-temperature gate dielectric deposition is PECVD based silicon oxide, which resulted in μ_{eff}-lin ~650 cm^2/Vs and I_{on}/I_{off} of 10^6 [154, 166]. However, 250°C, at which the PEO was deposited, is suitable only for high heat-resistant polymers such as PI [167]. The highest mobility (~710 cm^2/Vs) with Si NSs has been achieved with thermally grown SiO_2 as dielectric, where instead of

membranes or ribbons, the process has been modified to transfer print fully fabricated FETs to destination substrate [153, 154]. The comparison of previous reports (Table 3.1) shows that the device characteristics of room-temperature processed dielectrics are not in par with the high temperature deposited dielectrics. The electrical characterisation of 14 Si NRFETs has been conducted. The statistical distribution of peak field effect mobility among these devices is presented in figure 3.10.

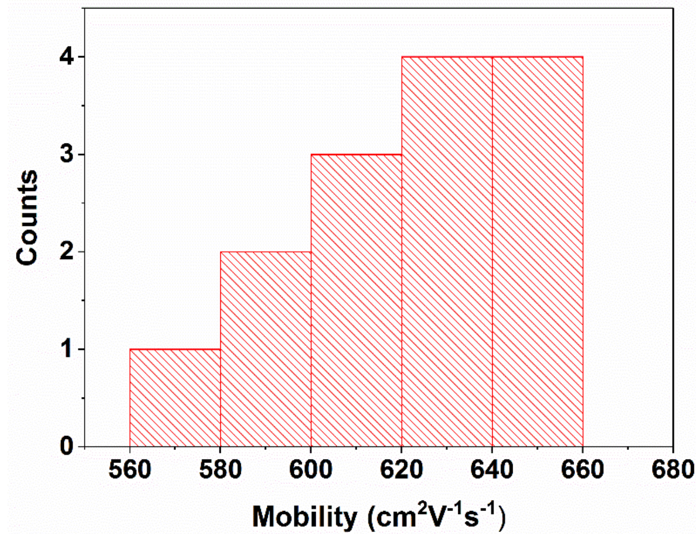


Figure 3.10: Statistical data distribution of peak field effect mobility obtained from 14 NRFET devices.

The saturation mobility (μ_{sat}) of the presented device obtained from its output characteristics under planar condition is 612 cm^2/V-s while it was 632 cm^2/V-s and 594 cm^2/V-s with convex (tensile) and concave (compressive) strain tests respectively. The saturation currents (at V_{DS}=V_{GS}=4V) were 96.24, 93.67 and 90.86 µA/µm for tensile, planar, and compressive conditions respectively. The on-to-off current ratio for the device was 4.4×10^6 or 6.644 decades. This is slightly lower than the previously reported value employing SAND dielectric (15 nm). [30] Further improvement could be achieved by using a thinner SiN_x dielectric. At the subthreshold regime, the subthreshold swing (SS) was extracted from the logarithmic transfer characteristics by numerical differentiation based on the equation:

$$\text{S-S}= \frac{1}{\partial \log(I_D)/\partial V_{GS}} \tag{3.5}$$

The subthreshold slope was found to be 182 mV/decade. This value is significantly higher than previously reported a-SiO while the SAND dielectric has better subthreshold performance [61, 105, 141]. This could be further enhanced by reducing the thickness of the gate dielectric, thereby the gate can have a better control on the channel. The cyclic bending impact on the performance of the device was also evaluated.

The peak values of the drain current (at $V_{DS} = V_{GS} = 4$ V) were obtained under planar condition after every 10 cycles of compressive and tensile bending (Rc= 40 mm). A total of 100 bending cycles were performed and the result is shown in Figure 3.9c. It can be observed that the device performance in terms of the drain current remains unchanged even after 100 bending cycles with negligible variation in the gate leakage current (less than 1%). The maximum gate leakage current density was ~ 10^{-7} A/cm^2 at 4V. To evaluate the gate breakdown voltage after applying cyclic bending test of 100 cycles, four randomly chosen NRFET devices were characterised, and the results are shown in Figure 3.9e. The breakdown field strength of the dielectric was >2.2 MV/cm which is excellent for a room temperature deposited gate dielectric.

3.3.2 p-type Si NRs FET by conventional transfer printing

In previous sections, I detailed the successful fabrication of n-type Si nanoribbon-based field-effect transistors (NRFETs) on fully flexible polyimide (PI) substrates at room temperature. The high-quality silicon nitride (SiN_x) dielectric was directly deposited on the printed nanoribbons, enabling the NRFETs to achieve high performance (mobility ≈656 cm^2 V^{-1} s^{-1} and current on/off ratio >10^6) similar to conventional silicon-based devices that require high-temperature processes. In this work, I used the previously reported fabrication process to realize high-performance p-type Si NRFETs, which also showed excellent device performance, with a charge carrier mobility of 85 cm^2 V^{-1}. s^{-1}. and current on/off ratio >10^3. To perform electrical characterization of the p-type Si NR-based FET on a flexible PI substrate, I used a Cascade Micro-tech Auto-guard probe station interfaced to a semiconductor parameter analyzer (B1500A, Agilent) in ambient environmental conditions (Fig. 3.11f). I obtained transfer characteristics (I_{DS}-V_{GS}) of the Si NR-FET with a drain bias

(V_{DS}) of -200 mV by varying the gate-source voltage (V_{GS}) from 1.5 to -3 V, as shown in Fig. 3.11a. The current on/off ratio was found to be $>10^3$, and I extracted the subthreshold swing (SS) at the subthreshold regime from the logarithm transfer plot, which was ~600 mV/decade. Fig. 3.11c displays the transfer characteristics (I_{DS}-V_{GS}) of p-type Si NR-FET at various values of drain–source voltages (VDS). Notably, the threshold voltage (V_{th}) remained constant even when V_{DS} was varied, indicating high stability. I determined that the threshold voltage (V_{th}) through extrapolation in the linear region of p-type Si NRFET was ~0.5V. I obtained the output characteristics (V_{DS} - I_{DS}) of the Si NR-FET by varying gate bias (V_{GS}) from 0 V to -3V with a step of 0.5V and varying V_{DS} from 0 V to -3 V (Fig. 3.11b). It was observed that the drain current (I_{DS}) increased as the negative gate bias (V_{GS}) increased, thus confirming the p-channel behavior of the fabricated NR-FET. The extracted field-effect mobility was ~85 $cm^2V^{-1}. s^{-1}$, which is higher than that of reported p-type-based FETs [15]. However, the performance of the p-type Si NRFET was relatively lower than our previously reported n-type-based device [58]. This variation is expected, as the mobility is inversely proportional to the effective mass, and the effective mass of holes is much higher than that of electrons. I also evaluated the stability of the NRFET device under cyclic bending conditions (tensile and compressive) at a 40 mm radius of curvature, performing 100 bending cycles. The variation of the peak I_{DS} values corresponding to on-state current at -6V_{GS} and 1V_{DS} was demonstrated in Fig. 3.11d.

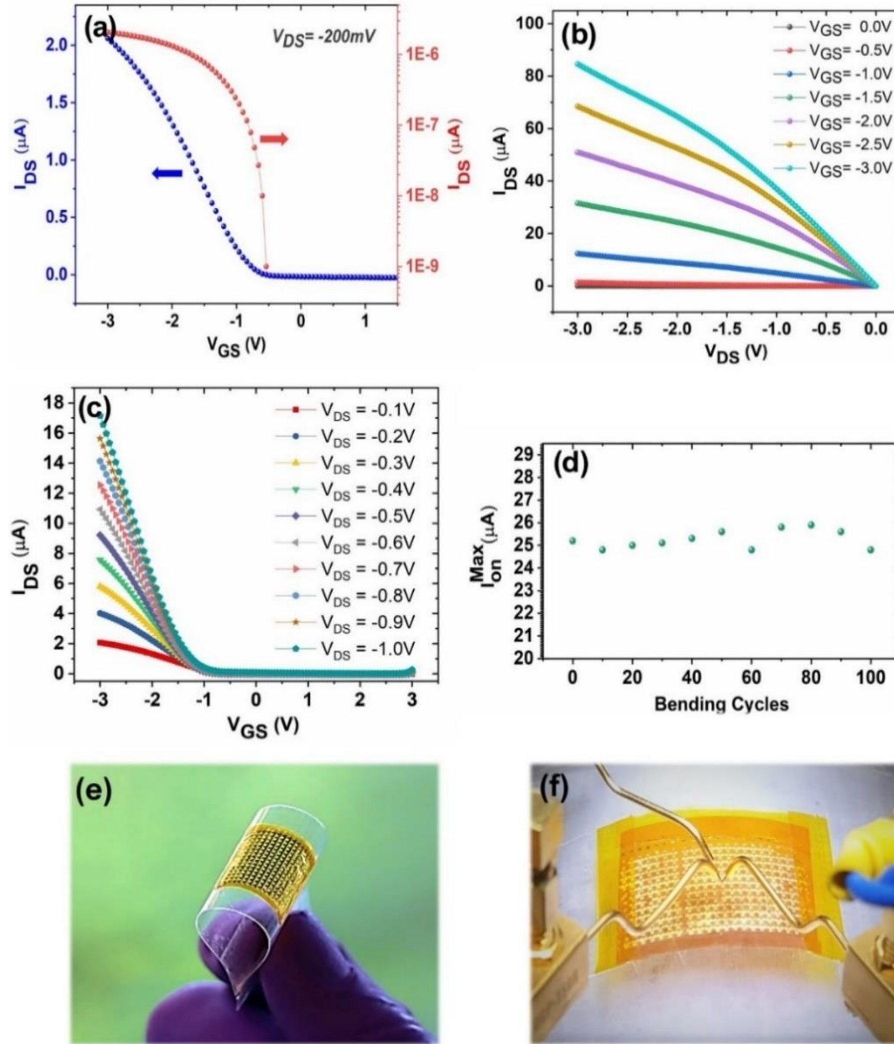


Figure 3.11: **(a)** Typical transfer characteristic (I_{DS}-V_{GS}) of the fabricated p-type device at negative gate bias with -0.2 V of source-drain voltage with illustration of logarithm curve of transfer plot. **(b)** presents the output characterisation of representative p-type NRFET, the gate voltage range is from 0 to -3V with step of -0.5V. **(c)** Transfer curve with varies V_{DS}, the range of V_{DS} is from -0.1 to -1.0 V. **(d)** The variation of peak on state current after bending cycles (Tensile and compressive) at 6V of V_{GS} with 1V of source-drain voltage (V_{DS}). **(e)** Photograph image of array of p-type NRFET devices fabricated on PI substrate. **(f)** Electrical characterization of p-type NRFET under planner and cyclic bending (Tensile and compressive) conditions.

3.4 **Conclusions:**

In summary, this chapter presented a room temperature fabrication process to realise the n-type and p-type Si nanoribbons-based field effect transistor (NRFETs) on flexible substrates. The Si nanoribbons are top-down fabricated and integrated over flexible substrates using conventional transfer printing approach with adhesive. The resulting NRFETs, with room temperature deposited SiN_x gate dielectric, exhibit excellent

performance (n-type mobility ~656 $cm^2.V^{-1}s^{-1}$, current on/off ratio $>10^6$, and p-type mobility ~85 $cm^2.V^{-1}s^{-1}$, current on/off ratio $>10^3$), comparable with the highest performing devices reported so far. However, in comparison to state-of-the-art silicon CMOS structures, the mobility performance of n-type FETs is approximately 3 to 4 times higher than that of p-type FETs. Consequently, the mobility of p-type transistors appears to be relatively lower. This observation suggests the necessity for further optimization in terms of the doping process. The doping technique employed in this work is carried out by spin-on dopant process, which may not be the ideal approach. Instead, the ion-implantation method of doping is preferred, as it offers more effective and uniform doping. Utilizing ion-implantation could potentially enhance the performance of p-type transistors and address the current mobility disparity between n-type and p-type FETs. The mechanical flexibility, robustness, and stability of the devices were evaluated by performing tensile and compressive cyclic bending measurements. The transfer printing process has great potential for integrating high energy conversion efficiency nanostructures such as Si NRs as building blocks for realizing FETs. The room temperature inductively coupled plasma (ICP) process used for the deposition of high-quality dielectric (SiN_x) of thickness 100 nm leads to enhanced device performance. The NRFETs retained their excellent electrical characteristics after 100 cycles of bending test, which indicates their potential for use in flexible CMOS circuitry-based applications, such as IoT and for the integration of miniaturized energy sources, like solar cells.

However, the conventional transfer printing method using a viscoelastic stamp with adhesives presents some limitations. While the transfer yield is good, the PDMS stamp used in the process is etched, which introduces PDMS residues and contamination issues. Additionally, the process is not compatible with R2R manufacturing, and the use of chemical etchant is not environmentally friendly. Therefore, further efforts are needed to develop a transfer printing process that is low-cost, R2R compatible, environmentally friendly, and provides high transfer yield, good registration factor, and no contamination. The next chapter will present the efforts made to develop such a transfer printing method and the transistor devices made from the printed NRs.

Author Contributions:

In this chapter, the work was conceptualized by me and Dahiya, R. The initial experiments and fabrication tasks were undertaken and led by me, with valuable assistance from Navaraj, W.T. and Shakthivel, D. Subsequently, I conducted the optimization of transfer printing and device fabrication. Navaraj, W.T. contributed to the simulation of the device's characteristics, while the device characterizations were performed by me, with support from Dahiya, A.S. Throughout the project, all the authors mentioned in this chapter actively participated and made valuable contributions through regular discussions. Overall, Dahiya, R. provided supervision and guidance for the project.

Chapter 4.

Direct Roll Transfer Printed Silicon Nanoribbon Arrays Based-High Performance Flexible Electronics

The work Adapted from:

Journal Articles

- **Zumeit, A.**, Dahiya, A.S., Christou, A., Shakthivel, D., and Dahiya, R. Direct roll transfer printed silicon nanoribbon arrays based high-performance flexible electronics (2021) npj Flexible Electronics, 5 (1), 18, DOI: 10.1038/s41528-021- 00116-w
- **Zumeit, A.**, Dahiya, A.S., Christou, A., Dahiya, R. High-performance p-channel transistors on flexible substrate using direct roll transfer stamping (2022) Japanese Journal of Applied Physics, 61, SC1042, DOI: 10.35848/1347-4065/ac40ab
- Dahiya, A.S.[#], **Zumeit, A.[#]**, Christou, A., Dahiya, R. High-Performance n-Channel Printed Transistors on Biodegradable Substrate for Transient Electronics (2022) Advanced Electronic Materials, 8(9),2200098, DOI.org/10.1002/aelm.202200098 *[#] Equal contribution*

Conference Publications

- **Zumeit, A.**, Dahiya AS, Christou A, Dahiya R. "High performance n-and p-channel flexible transistors using roll printed silicon nanoribbons, " in2022 IEEE International Conference on Flexible and Printable Sensors and Systems (FLEPS) 2022: IEEE, pp. (1-4), DOI: 10.1109/FLEPS53764.2022.9781569 (**Nominated for a Best paper Award**)
- **Zumeit, A.**, Dahiya, A.S., Christou, A., Shakthivel, D, Liu, F., and Dahiya, R. Presented at Int. Conf. on Solid States Devices and Materials (SSDM), 2021

Abstract:

In the previous chapter, I have demonstrated the potential of the conventional stamp-based transfer printing method for integrating high mobility inorganic nanostructures to construct high performance transistors on flexible substrates. The printing methods was modified with the use of adhesives to provide high transfer yield but issues such as contamination were observed. The present chapter presents the Direct Roll Transfer Printing (DRTP) approach

for the integration of high mobility inorganic structures. It is a single-step process, i.e., without using any elastomeric stamp, to print nanoribbons (NRs) on different substrates, which means reduced number of printing steps and hence reduced printing cost and time. Further, it reduces the chance of breakage and/or wrinkling of printed nanostructures and hence helps to preserve their morphology and structure. This also offers an excellent opportunity to enhance the transfer printing performance. The performance of the novel roll-based printing approach is demonstrated using a series of morphological characterisations such as Scanning Electron Microscopy (SEM) and Atomic Force Microscopy (AFM): (a) near-perfect registration of the printed structures ($<0.1\,\mu m$), (b) high transfer yield (~95%), (c) residue-free transfer of Si NRs and (d) large area transfer ($9\,cm^2$). Furthermore, the process is compatible with R2R fabrication which is advantageous for future LAE manufacturing. The semi-automated DRTP system has been used for printing sub-100 nm thick (≈70 nm) Si NR arrays directly on the target flexible receiver substrate using a custom roll system. To this end, the silicon NR based field-effect transistors (both n- and p-type FETs) are realised using the direct roll transfer printed NRs which consistently show high performance i.e., n-type FETs show high on-state current (I_{on}) >1 mA, high mobility (μ_{eff}) >600 cm^2/Vs, high on/off ratio (Ion/off) of around 10^6, and low hysteresis (<0.4 V). The developed versatile and transformative method can also print nanostructures based on other materials such as GaAs and thus could pave the way for direct printing of high-performance electronics on large-area flexible substrates.

4.1 Introduction

Advances in flexible large-area electronics (LAE) have enabled novel applications across numerous areas including wearable systems, soft robotics, bendable displays, and healthcare [8, 9, 11, 12, 18]. This will also have an impact on the development of the Internet of Things (IoT) concept where smart objects are required to be aware of and interact with the environment [21]. Conformability of electronic devices to different shapes is indispensable for the above applications [58, 168-172]. Further, fast computing and communication needed in many of these applications to enable myriad human-machine interactions with low

latency also call for high performance of the devices. As a result, significant research efforts are being made to manufacture electronic devices and circuits with flexible form factors and high performance. For example, taking advantage of the high-performance Si technology, ultrathin chips (UTCs) have been developed for system-in foil applications [32, 34]. However, due to economic reasons and integration-related difficulties their use is limited to areas requiring compact electronics. The heterogeneous integration of advanced nanomaterials/nanostructures through printing is another manufacturing route that can bring innovations in high performance flexible electronics [49, 58, 173].

Among various printing technologies, transfer printing has shown good potential for realising high-performance flexible electronic devices and circuits [58, 59] with silicon and compound semiconductor material-based nanostructures (NSs) such as micro-/nano-membranes (NMs), nanoribbons (NRs), nanowires (NWs), etc. as building blocks. In a conventional transfer printing process, the NSs are picked up from their growth/fabrication rigid substrates using soft polymeric stamps, usually made of Polydimethylsiloxane (PDMS), and then printed onto flexible substrates to obtain the electronic devices and circuits [59, 70]. The controllable and reproducible transfer of NSs from the donor to the receiver substrate is critical for LAE, and hence a precise control over the interface properties (stamp/donor and stamp/receiver) is required during transfer printing. It is challenging to have complete control over printing parameters (e.g., retrieval/pick up velocity, adhesion switchability, stamp surface recovery, etc.) and interface properties and as a result, it is difficult to obtain high yield and reproducibility. This is due to the viscoelastic properties of soft stamps, which may cause unexpected tilt, orientation, and buckling of NSs under applied force during the printing process [47]. Further, it is challenging to print sub-100 nm thick NSs using conventional transfer printing. This is because at such thicknesses the strain energy release rate at the stamp/NS interface decreases with respect to the NS/substrate interface, which leads to lower printing yield [90]. Several attempts have been made to address these challenges with modified transfer printing involving the surface morphology [99, 102], interface engineering [51, 115], thermal modulation and kinetically controlled velocity [104, 174, 175], magnet-controlled [113], and

laser-driven method [176], etc. (summarised in table 4.1). These modified transfer printing methods improve the yield and reliability of the process and further extend the transfer printing capacities to: (i) selective printing [106], (ii) arbitrary substrate integration [121], and (iii) deterministic assembly of nano to chip-scale structures [49, 115, 177]. These modified transfer printing methods have shown good potential for flexible electronics, but they also require additional excitation equipment such as laser system, and magnet actuating system, etc. In this regard, it is highly desirable to develop a precise transfer printing process that enables higher transfer yield, excellent registration, and compatibility with R2R printing without adding complex printing equipment [23, 49, 178]. The direct transfer printed Si NRs were further processed to obtain NRFETs are accomplished following our recently demonstrated room temperature (RT) fabrication process including a dielectric deposition. The developed NRFETs exhibit excellent electrical properties: average device effective mobility of ~631 cm^2/Vs, and high on/off current ratio ($I_{on/off}$) of around 10^6. The response after cyclic bending tests shows the device having excellent mechanical stability and flexibility. The obtained results are also compared with the Si NRFET devices obtained using conventional transfer printing. The presented results show the significant potential of direct transfer printing as a new route towards high-performance printed LAE.

Table 4.1: Performance comparison for the conventional and modified transfer printing process with the developed direct troll printing technique.

Transfer Printing Method	Printing Principle	Material /Structures printed and dimensions.	Printing process parameters				
			Fabrication difficulties	**Yield**	**R2R Compatibility**	**Registration accuracy**	**Ref.**
Bending radius controlled	Peeling velocity bending radius	Micro-scale Si plate array (7 µm thick; 760 × 760 µm)	Medium/ issue: limited to micro-scale structures	97.4 %	**No**	≈ 2000 nm	[111]
Adhession promoter assisted	Using adhession promoter (VM652)	Si NRs arrays (70 nm thick; 5 µm x 50 µm)	low/ issue: poor registartion quality	N/A	**No**	≈ 2000 nm	[58]
Shear-assisted inspired by Gecko	Peeling velocity with angular direction dependent	Micro-scale Si, membranes, plates, etc. Si platelets (3 µm thick, 100 µm × 100 µm)	meduim/ issue: low contrast in adhesion switchability)	≈ 90%	**No**	< 4000 nm	[51]
Surface-relief assisted inspired by Aphid	Changing in contact area from stamp's shape memory effect	Micro-scale Si inks (squares, conical shapes, etc.)	High/ issue: adhesion switching and temperature	N/A	**No**	1000 nm	[118]
Laser-assisted transfer printing	Laser-induced thermal mismatch	Micro-scale Si plates (100 µm× 100 µm× 0.32 µm)	High/ issue: temperaturte and require expensive equipment	N/A	**No**	1000 nm	[142]
Shape memory assisted polymer & laser assisted	Changing in contact area from stamp memory shape & thermal mismatch	Si nanoribbons 200 nm thick.	High/ issue: possible thermal damage, and require expensive equipment	100%	**No**	N/A	[106]
Direct Roll Transfer Prinitng (DRTP)	**Adhession-assisted**	**Si NRs (70nm thick; 55 µm x 5 µm)**	**low/issue: limited to PI substrate**	**≈ 95%**	**Yes**	**<100 nm**	**This work**

4.2 Experimental section

4.2.1 DRTP of Si NR array

In the previous section (3.2.1), the fabrication process flow to create Si NR structures was described in detail. In this work, we have developed a custom-made direct roll printing technology to transfer the releasable Si NRs to flexible substrates. The semi-automated printing setup is shown in Figure 4.1. This approach involves carrying out all steps at low temperature to complete device fabrication. A commercial PI foil with a thickness of 25 µm was used as the receiver substrate for statistical data study and device fabrication. To ensure successful transfer printing, an adhesion promoter was applied to the receiver substrate before printing. Then, an ultrathin layer of PI-2545 precursor from HD Microsystems was spun onto the PI sheet at 2000 rpm for 60 seconds to achieve a thickness of approximately 1.0 µm. The adhesion between the receiver substrate and the PI layer was promoted by coating with VM652 from Microsystems. The spun PI layer was partially cured at 120 °C for 2 minutes to provide an ultrathin layer of adhesive. The donor substrate, containing the released NRs, was placed on the planar stage of the roll printing setup, and the PI substrate was wrapped around the roller as shown in Figure 4.1. During the direct roll transfer printing (DRTP) process, the receiver substrate was brought into direct physical contact with the donor substrate, allowing the NRs to detach from the anchor points and transfer directly onto the flexible PI substrate. Subsequently, the receiver substrate was fully cured at 250 °C for 2 hours to ensure solidification through the thickness of the thin film and to enhance the adhesion of the NRs on the receiver substrate. Successful direct roll printing depends critically on conformal contact at the interface of the donor/interfacial adhesion of the semi-cured PI on the receiver substrate.

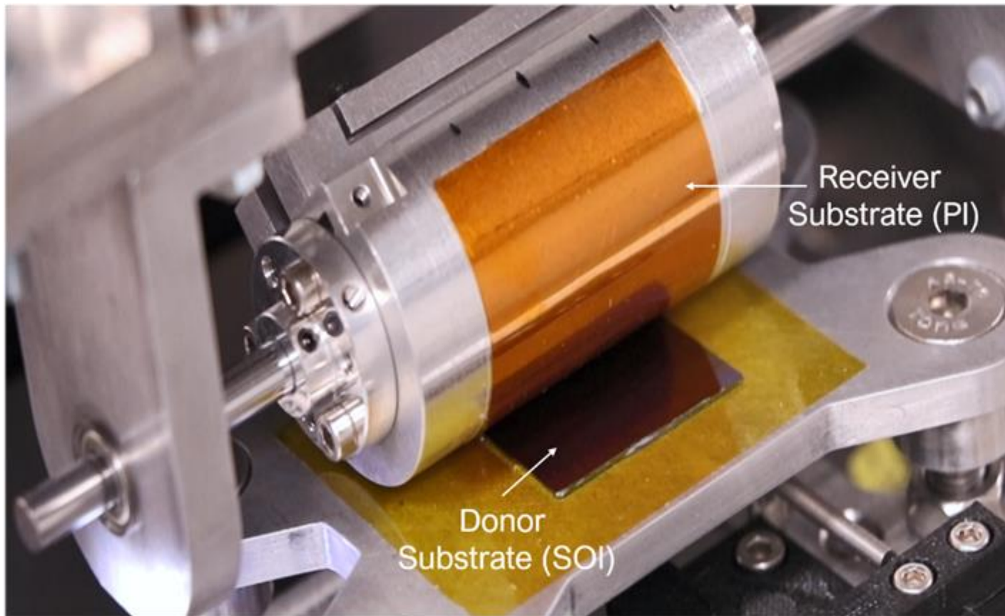


Figure 4.1: Demonstration of automated experimental setup for DRTP process of Si NR arrays from SOI wafer onto flexible substrate.

The fabrication process of Si NRFETs using direct roll printing technology are schematically demonstrated in figure 4.2. Since the key elements and the details of the fabrication process are mentioned in section 3.2.1. To draw the comparison, Fig. 4.2 illustrates the processing steps for conventional transfer printing. For both printing techniques, silicon NRs are first fabricated on the rigid wafer using a conventional nanofabrication process, as described in our previous works [58]. Briefly, the fabrication process involves anisotropic wet etching of selected exposed regions on the top side of the Si wafer, followed by undercut etching of the buried oxide (Box) using hydrofluoric acid to eventually release Si NRs structures [33, 46, 92]. Figure 4.2a shows the fabrication steps to obtain Si NRs from a commercial silicon-on-insulator (SOI) [58]. This method produces horizontal arrays of NRs over SOI source wafers, which are transfer printed onto flexible receiver substrates. The process steps for conventional transfer printing are shown in Fig. 4.2b. It can be seen from this figure; it is a two-step process where the transfer mechanism can be understood by studying the competing fracture between the stamp/NS interface and the NS/substrate interface [47]. The kinetically controlled conventional transfer printing process has shown poor yield for sub-100 nm thick NRs because of difficulties in controlling the mechanics of viscoelastic PDMS stamp. As a major advance over the traditional processes, direct roll printing

addresses the above issue by avoiding the use of PDMS stamp (Fig. 4.2c) and thus also reducing the complexity of the fabrication process. In this process, the SOI wafer with Si NRs (donor substrate) is brought into direct physical contact with the semi-cured PI thin film over the receiver substrate.

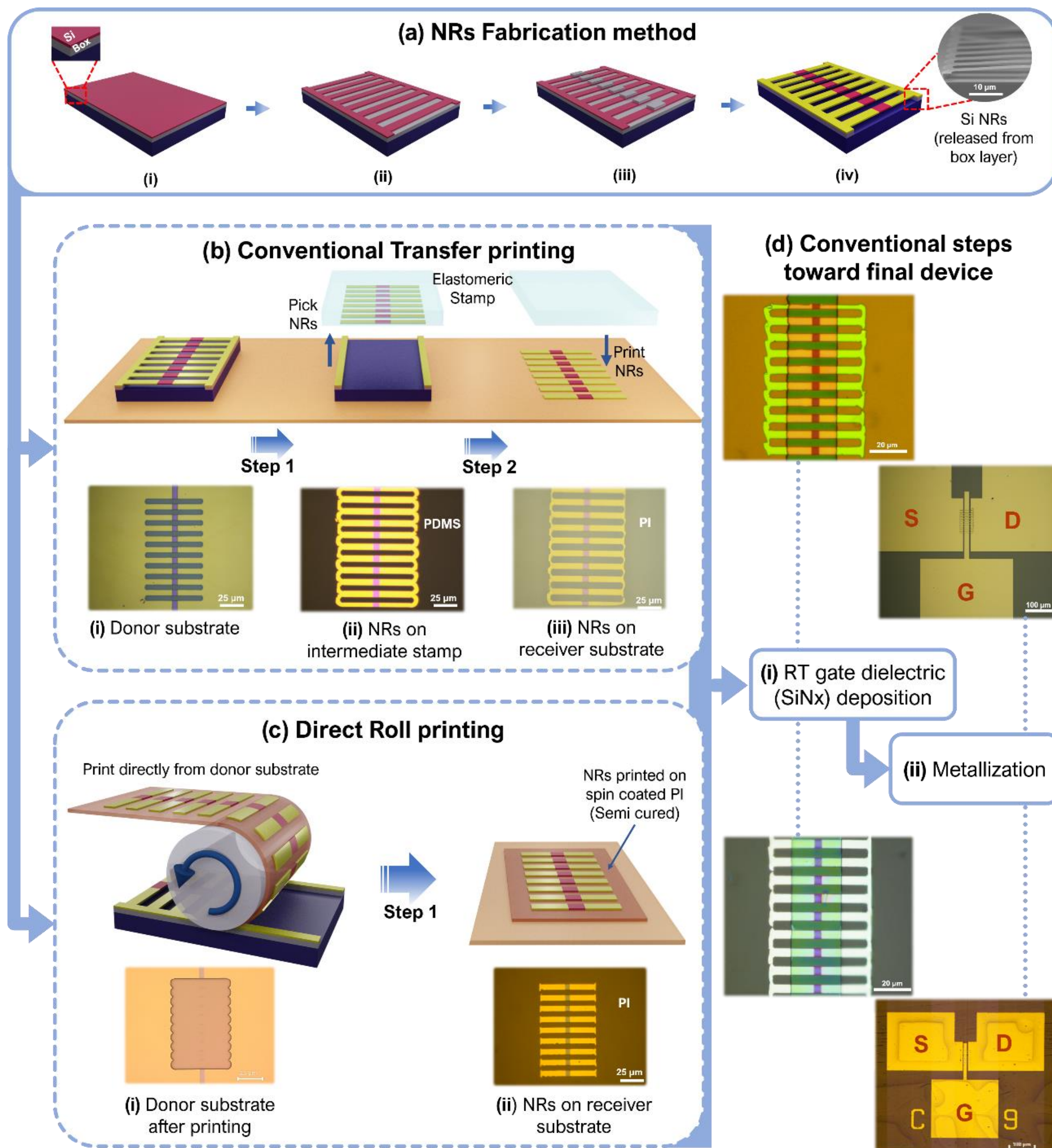


Figure 4.2: Schematic illustration of the steps involved in direct roll printing process with corresponding optical and SEM images. **(a)** Fabrication steps of Si NRs carried out on the donor substrate with n+ selective doping followed by releasing the NRs from buried oxide (Box) layer. **(b)** Conventional transfer printing steps using elastomeric stamp (PDMS). **(c)** Direct roll printing of NRs from donor to semi cured PI substrate. **(d)** Conventional microfabrication processing steps toward a final NRFET device (i.e., room temperature dielectric deposition, metallization, etc).

4.2.2 Simulation of PDMS deformation under compressive load

A FEA (finite element analysis) simulation was carried out, using COMSOL, to study the deformation experienced by the PDMS stamp under the loading conditions during the transfer printing process (Figure 4.3). A typical PDMS stamp used in our experiments has one cm^2 area and 2 mm thickness. A simplified 2D model was implemented for the simulation. The typical compression force applied on the stamp during transfer printing is 2N. The compressive modulus of PDMS when cured at 100 ^{o}C is ~150 MPa. The displacement of the stamp's top surface about the Y axis is shown in the graph (red line), indicating an average decrease in height around 0.25µm. Since PDMS has a Poisson's ratio of 0.5, the stamp increases in length along the horizontal direction. Given the stamp's length to thickness ratio, the expansion of the top surface about X axis is 1.4µm (blue line). The combined X and Y displacement of the top surface is shown by the green line.

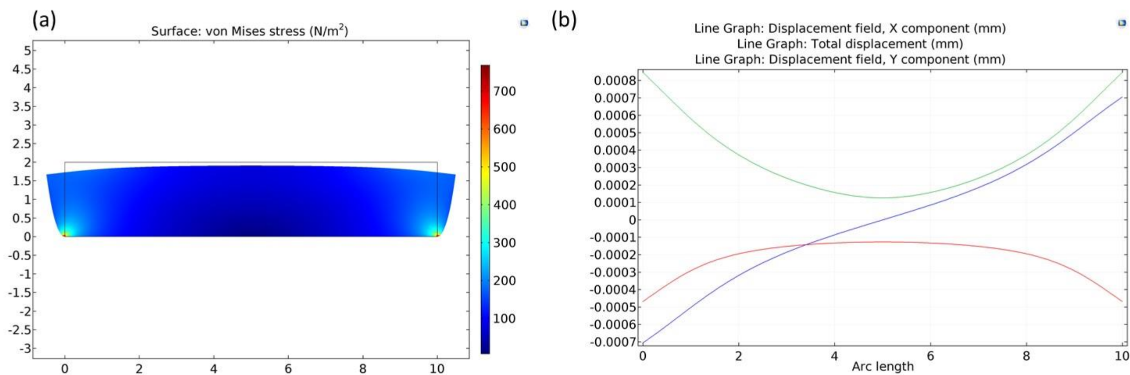


Figure 4.3: COMSOL simulations showing the lateral displacement of PDMS with applying 2N of vertical compressive force. **(a)** 2D image. **(b)** Corresponding plot

It is to be noted that, the use of a viscoelastic soft stamp in conventional transfer printing may degrade the registration quality of the printed NSs [107, 108]. For instance, periodic wavy/buckled structures formed spontaneously with specific amplitudes defined by the moduli of the materials and the thicknesses of the structures. This leads to little control over the geometries or the phases of the waves [179]. This is because of the mechanical properties of soft stamps such as PDMS. We studied this aspect using COMSOL simulations and noted that a 2 N compressive force on the PDMS surface to retrieve the NSs could introduce a lateral displacement of more than 1µm in PDMS due to the shear strain as shown in Figure 4.3. This means, during the retrieval step, the release of strain energy may

lead to wavy/ buckled structures and hence the misalignment of at least 1 µm. This misalignment is significant when we consider printed electronics in large areas. For example, this 1 µm misalignment from on a 1 cm stamp can become 10 µm on a 10 cm long substrate, which is fatal for the realisation of electronic circuits on such areas, particularly when the device's dimensions are smaller than the misalignment. If the channel length of a FET device is 1 µm, one can expect huge variations in electrical performance from device to device. Although controlled wavy/buckled structures could be used for the development of small-scale stretchable electronics but for LAE it is likely to lead to poor uniformity in device-to-device performance.

4.2.3 Si NRFETs fabrication and characterization

After integrating the functional elements of Si nanoribbons on flexible substrate by DRTP process, n and p-type field effect transistors were fabricated using room temperature processes, based on the previous demonstrated work [58], the detailed description of the fabrication process is presented in the previous section 3.2.1 This includes deposition of high-quality gate dielectric (SiN_x, 100nm) using ICP-CVD followed by metal deposition (Ti (10 nm)/Au (120 nm)) for gate, source, and drain using e-beam evaporation and lift-off. A short dip in diluted HF was performed prior to metallisation to remove the native oxide on the active Si regions, source and drain (S/D). Electrical characterisations of fabricated Si NRs based field-effect-transistors (Si-NRFETs) on flexible (PI) substrate were performed using Cascade Micro-tech Auto-guard probe station interfaced to a semiconductor parameter analyser (B1500A, Agilent). Linkam PE120 Peltier system was used for heating and cooling the p-type NRFETs to perform temperature dependence electrical measurements.

4.3 Results and discussion

4.3.1 Morphological analysis of direct roll printed Si NR arrays

A thin layer of partially cured PI is utilised to enhance the adhesion between NRs and receiver substrate during the printing process. As an immediate benefit, the direct roll printing approach leads to lower process steps, reduced complexity, shorter printing time,

and lower fabrication cost compared with conventional transfer printing. Following the direct transfer printing of NRs, low-temperature steps (e.g., dielectric and metal deposition) were carried out to realise devices on flexible receiver substrates, as shown in Fig. 4.2d. For high transfer yield in LAE, it is important to have good control over the shape, and geometrical configuration of the printed structures (high registration). To obtain the statistical data on registration, yield and to evaluate the quality of direct roll printed NRs, the morphological analysis was performed using Scanning electron Microscopy (SEM) of Hitachi SU824 optical microscopy, and Atomic Force Microscope (AFM from Bruker Nano). It is to be noted that this statistical data is obtained for NRs printed over PI substrate. Figure 4.4 shows the images of released Si NRs, before and after the direct roll printing. Figure 4.4a shows an optical microscopy image of selectively doped Si NR arrays over donor substrate; the inset shows the magnified SEM image of a single Si NRs array in releasable form, prepared to allow direct retrieval onto the surface of PI substrate. The inset of Fig. 4.4a shows the suspended NRs are anchored at both edges (5 µm width at both sides and supported by the underlying 2 µm thick of Box layer) to maintain the correct alignment. Figure 4.4b shows the corresponding optical image of arrays of 70 nm thick Si NRs, directly transferred onto a target PI substrate using direct roll printing. The SEM image in the inset of Fig. 4.4b illustrates a defect-free transfer of NRs. The statistical data on transfer yield was obtained for direct roll transfer printed nanoscale structures (contact area of donor/receiver during direct roll printing ~ 2.25 cm^2) as shown in Figure 4.4c, d. This study utilised SOI sample with a releasable Si NRs that consists of 11 $\times$ 12 arrays, where each single Si NR array consists of 9 NRs). The surface quality of transferred Si NRs on receiving substrate (PI) was investigated by AFM surface morphology. Figure 4.4e shows an AFM image (25 µm $\times$ 25 µm) of a single Si NR array directly transferred on PI substrate.

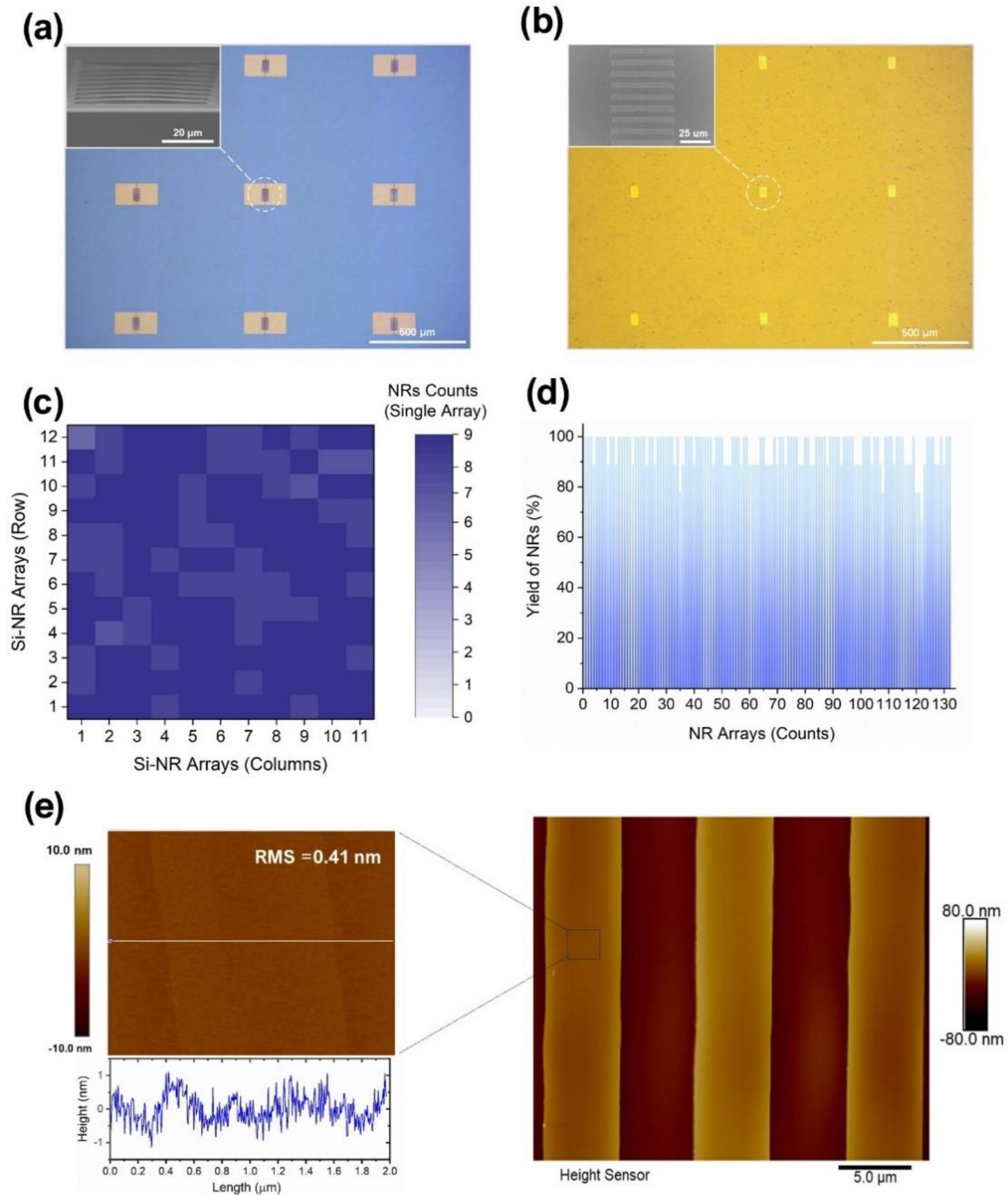


Figure 4.4: Morphological analysis of direct roll printed Si NR arrays. Optical images of **(a)** Si NR arrays on the donor wafer before printing. (**b**) Transferred Si NR arrays onto flexible receiver substrate. **(c)** and **(d)** Study of the yield based on presented direct printing approach (contact area of donor/receiver during direct roll printing ~ 2.25 cm^2). **(e)** Atomic force microscopy (AFM) image of the surface of single Si NR (scan size 25µm x 25µm) on PI substrate. The figure also shows a high-resolution AFM scan (2 µm x 2 µm) to monitor the roughness of Si NRs. SEM cross-sectional images of anchored Si NR array after etching the Box layer with top view image of the anchor point (inset) (scale bar, 20 µm). **(f)** Gap anchor point = 55 µm. **(g)** Gap anchor point >55 µm.

The surface topography of the printed NRs was found to be free from polymer residues/contamination. Further, the surface roughness of the printed NR was calculated using a high-resolution AFM image (2 µm × 2 µm), as shown in Fig. 4.4e. The calculated root means square (RMS) roughness of transferred ribbons is 0.41 nm. It can be seen from Fig. 4.4e that sidewalls of ultrathin NS are formed on PI substrate without any polymer residues, unlike other reported approaches such as glue-assisted transfer printing [42, 53, 99]. The presence of residues may lead to surface contamination and defects and failures in transferred NSs, eventually degrading the device performance [162].

4.3.2 Transfer Yield Studies

The reliability and robustness of the presented printing approach were evaluated by the transfer yield of NRs from the donor to receiver substrate. High transfer yield (~100%) is desired for any practical application. To have a uniform and high printing yield over a large area, conformal contact between the semi-cured PI layer and Si NRs is needed for DRTP approach. To achieve an excellent conformal contact and thus, the printing yield, dependency of applied force on transfer yield was evaluated. The contact force is one of the critical parameters that affect the final yield of the process. The optimisation study with the applied force is shown in figure(a-d), where each single Si NR array consists of 9 NRs, the width and spacing between them are 5 µm, the length and thickness are 50 µm and 70 nm, respectively. The transfer yield results were obtained and characterised based on different applied forces from 2 to 12 N while the printing speed was fixed to 1 mm/s. As shown in figure 4.5e, the transfer yield increases with the increase in applied force and reaches 95% for the applied contact force of 12 N (the printed area was 2.25 cm^2 chip). This observation is based on the data from 11 × 12 Si NR arrays. These results can be explained as higher forces lead to more conformal contact of NRs with the semi-cured PI, which in turn enhances the adhesive strength between them. Eventually, this helps to achieve a uniform and high transfer yield. The applied 12 N is close to the max loading capacity of the present roll printing system (load cells, motors). However, with further modifications of our roll printing setup, it would be possible to apply larger forces to further enhance the transfer yield.

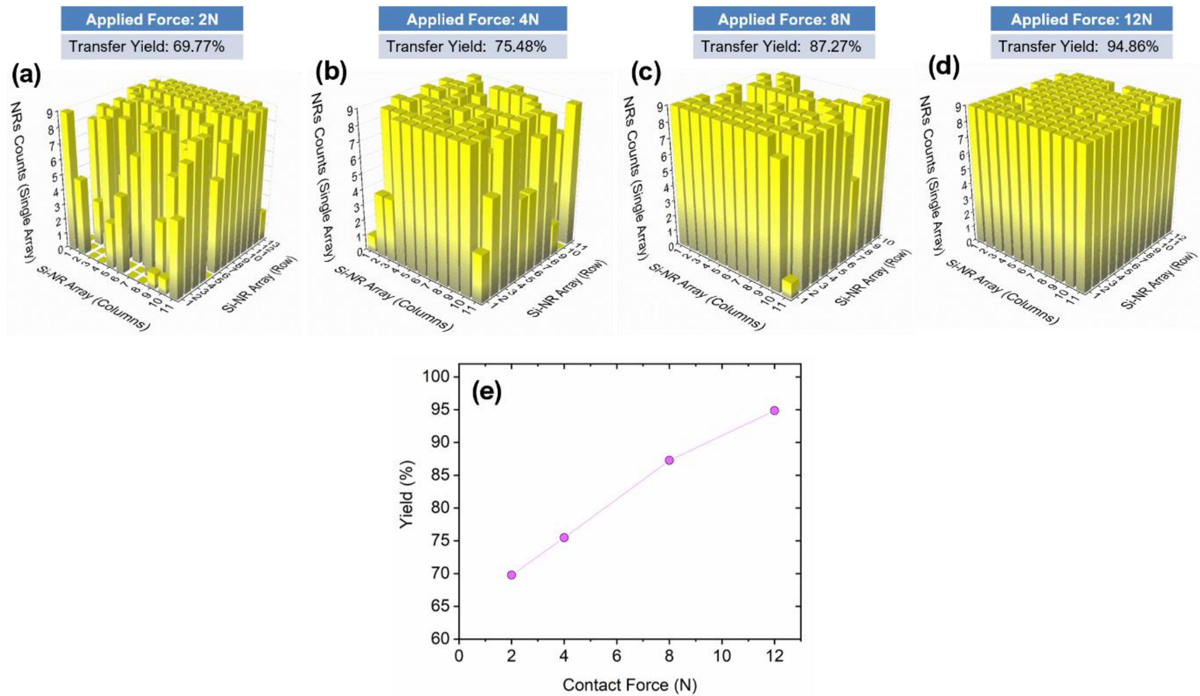


Figure 4.5: Transfer yield experiment based on applied force. The applied speed was 1mm/s for all tests, sample size ~2.25 cm^2 chip. The total number of Si NR arrays ranging from 110 to 140 array were directly transfer printed on flexible substrate. **(a-d)** The resultant transfer yield of Si NR arrays under various applied force. **(e)** Transfer yield dependency over applied contact force.

4.3.3 Large area printing

It is worth noting that the gap between the anchor points plays a crucial role in achieving a higher transfer yield. In order to optimize this gap, various durations of Box layer etching were performed. The SEM images of the NRs anchored at two ends, with different etching durations of the Box layer, are shown in Figure 4.6. It was observed that the transfer yield is nearly zero when the gap between anchor points is greater than 55 µm. This is because, for larger gaps between anchor points, the suspended NRs come into contact with the base of the silicon wafer and create a bond with the bulk substrate, which eventually leads to broken ribbons or the ones that cannot be retrieved from the source substrate during direct roll printing.

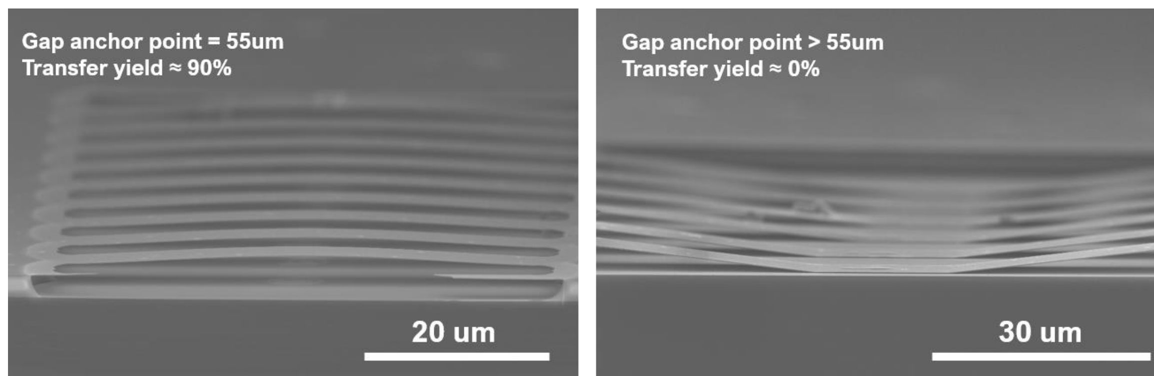


Figure 4.6: Illustration of Scanning electron microscopy (SEM) images showing the released Si NR arrays after buried oxide removal step.

Following the optimisation study, large-area printing was performed using SOI donor substrate having a size of 3 × 3 = 9 cm^2 (close to 2-inch wafer size) with an optimised roll printing parameter (12 N force @ 1 mm/s), as illustrated in the (Figure 4.7). By carefully optimising the process and the etching time (shown above), I managed to achieve highly uniform printing with ~95% transfer yield averaged over the printed large area.

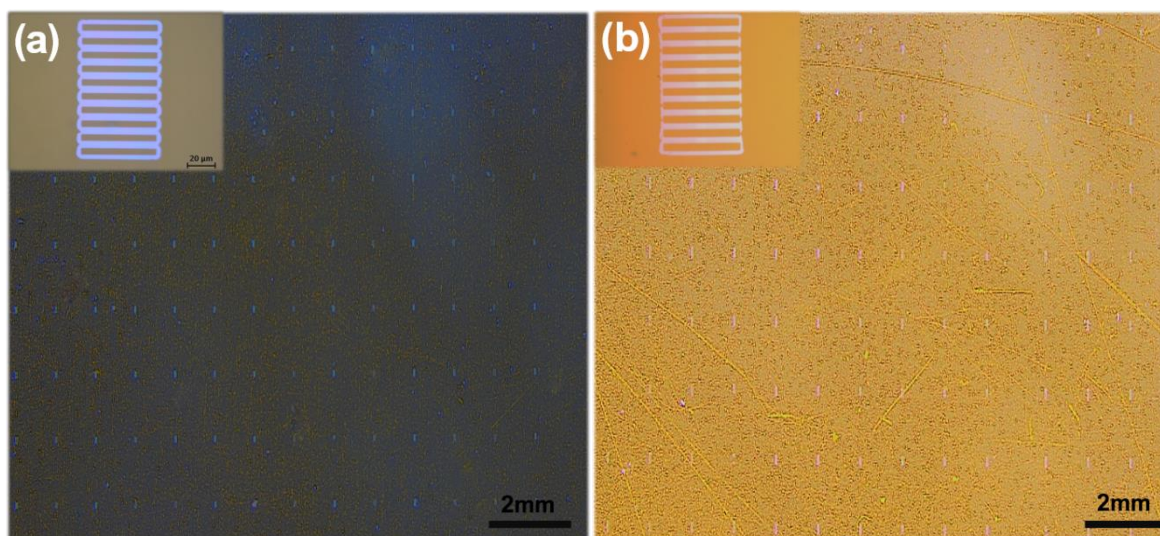


Figure 4.7: Optical images of direct roll printing approach of large area Si NR arrays transferred onto receiver substrate (commercial PI sheet) 3.1 × 3.1 cm^2 (2-inch wafer size): **(a)** Dark-field microscopy, and **(b)** bright field microscopy of printed nanoribbons directly on commercial PI sheet with high magnification images (inset).

4.3.4 Registration Studies

From Figure 4.8, it is clear that the arrays of Si NRs with perfect registration were transferred over the PI substrate (separated by 930 µm in X-direction and ~990 µm Y-

direction). These registration values perfectly match with the NRs on the donor wafer. A high registration quality of printed structures is critical for the high-performance LAE as poor registration may lead to poor control over device dimensions and hence greater variation in device-to-device performance [49].

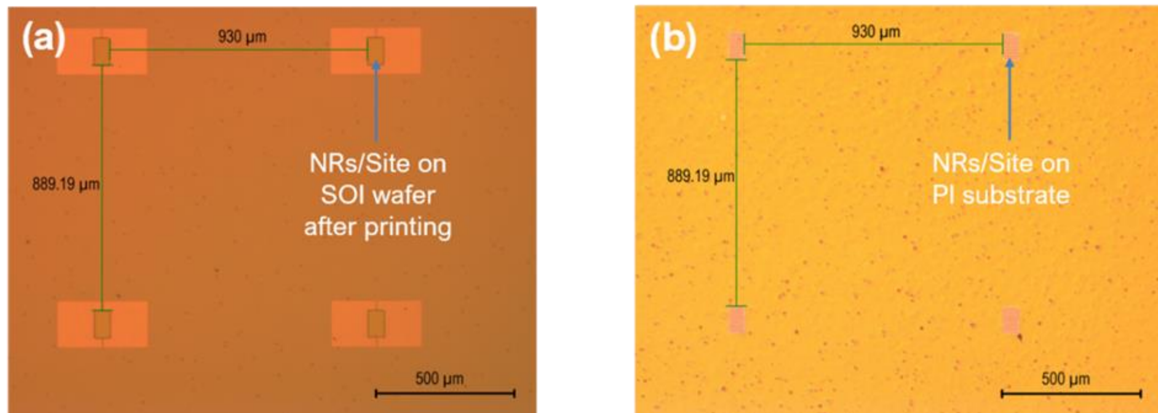


Figure 4.8: Optical images. **(a)** Selectively doped n+ Si NRs arrays on the donor wafer (100 x 55 μm^2 separated by 930 µm) after printing. **(b)** Si NRs (4 arrays, each array consists of 9 NRs) printed directly onto flexible substrate (PI).

The low probability of misalignment during the direct roll printing process can be observed in Figures 4.8a-b since the process does not involve viscoelastic stamps. This feature helps to maintain the alignment of the Si NRs, thereby reducing the variation in NR density across the substrate and the overlapping of adjacent NRs, which ultimately leads to improved device-to-device uniformity. Moreover, it also results in a higher transfer yield of the Si NRs. Section 4.1 presents Table 4.1, which summarizes these results and provides a comparison with the conventional transfer printing process.

4.3.5 Substrate Independence

The semi-cured PI layer allows us to perform direct roll printing of NSs with enhanced transfer yield. However, this step could potentially make the printing process slow and pose challenges in terms of printing over different substrates. This is because, after direct transfer printing, the annealing of the coated PI layer is needed. To investigate this, we have printed Si NRs over various flexible substrates such as metal foils (e.g., Al, Cu, and Mg) and polymers (e.g., Kapton sheet, PET, and PI). The data is shown in Figure *4.9*. Depending

on the underlying substrate and its glass transition temperature, the curing time could vary from 2 h (for PI, Kapton, and metal foils) to 4 h (PET). Indeed, 2–4 h of curing makes the printing step slower, but this drawback could be overcome by using UV-cured polymers as an adhesive layer. Employing UV can effectively speed up the process [100] and reduce the time duration of the entire printing process. It is worth mentioning here that the present printing area is restricted only by the size of the roller and not the process itself. By increasing the roller size, it will be possible to increase the print area. This marks a significant advantage over the conventional two-step transfer printing process, which usually shows a low printing yield for sub-100 nm thick NSs [90]. This is because the adhesion forces that are considered insignificant at the macro scale become dominant at the micro/nanoscale. As a result, releasing the micro-/ nano structures from stamps has been a major challenge for a 'pick-and-place' assembly technique. Thereby, accuracy, yield, and throughput of the printing process are majorly compromised.

Finally, after conducting the studies related to the surface topography of the printed NRs. It is worth mentioning that the use of an intermediate stamp in conventional transfer printing may leave residues on the surface of the NSs due to high bonding strength and strong adhesion between PDMS stamp and native oxide (SiO_2) layer [68, 96]. The post-surface treatment is normally needed to remove the residues will also add few extra fabrication steps and increase the process complexity. The removal of PDMS residues typically involves plasma treatment or wet etching which could damage or introduce roughness over the NRs of sub-100 nm thickness. The elastomeric stamp residues (non-conducting material) strongly influence the electrical performance and reliability of nanostructures-based electronics since the interfacial contact between the nanostructures and deposited metal contacts are not desirable. Therefore, there is a possibility of performance degradation in the case of traditional transfer printing. Surface chemistry technique has also been demonstrated by depositing/ sputtering thin SiO_2 layer on the top of the target NS to enhance stamp/NS adhesion [56]. Such steps increase complexities in the printing process and produce surface contamination on top of printed NSs, which may subsequently lead to variation in terms of device performance. The capability of the

developed direct transfer printing approach has been evaluated further by demonstrating NRFETs, following our recently demonstrated room temperature (RT) fabrication process including a dielectric deposition [58].

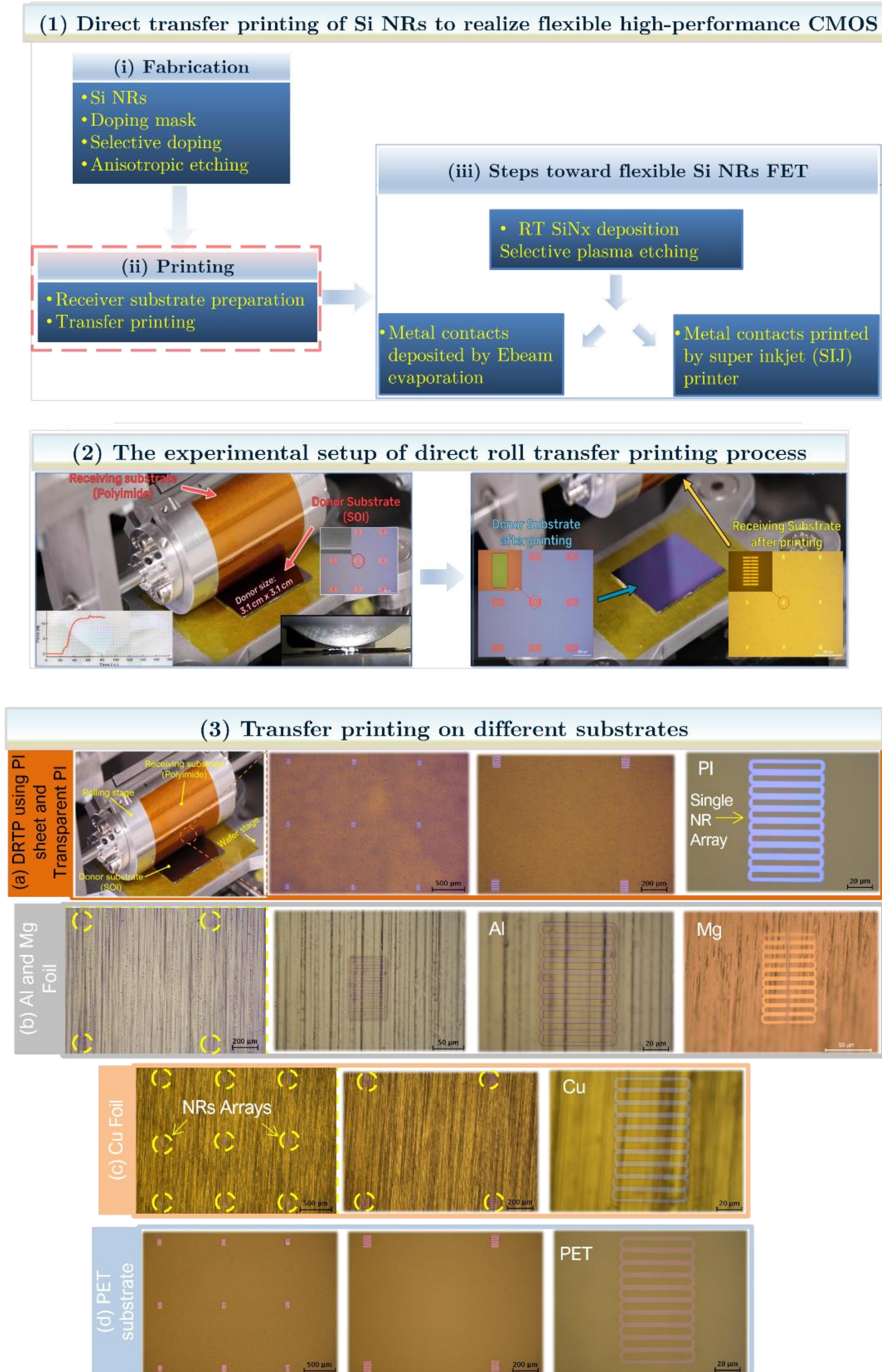


Figure 4.9: **(1)** Block diagrams of key fabrication process steps performed to fabricate flexible Si NRs FETs by transfer printing technique. **(2)** Experimental direct roll transfer printing setup. **(3)**

Corresponding optical images demonstrating the successful transfer printing of Si NR arrays onto different receiving substrates, showcasing the substrate independence and the capability of printing nanostructures on diverse materials. The Si NR arrays, composing (3 × 3), (2 × 2), and single NR arrays, were directly printed from the SOI wafer onto (a) PI sheet, (b) Al and Mg foils, (c) Cu foil, and (d) PET substrate. The optical images were captured at different magnifications. Notably, the high surface roughness of the metal foils, such as Al and Cu substrates, poses difficulties in identifying the printed ribbons, particularly in low-magnification images, unlike in low magnification images in low-magnification images, single NR array is clearly visible, free from physical defects such as micrometre-sized cracks or wrinkles.

4.4 DRTP process validation

The following section aims to demonstrate the effectiveness of employing direct roll transfer printing (DRTP) in realizing n- and p-type silicon nanoribbon field-effect transistors (Si NRs FETs) with high performance. This validation serves as a foundation for the subsequent sections, which detail the fabrication and characterization of these devices. Through this analysis, we will provide a comprehensive evaluation of the performance and potential of DRTP technology for producing high-quality Si NRs FETs. The results obtained will provide a deeper understanding of the factors that influence the device's performance and serve as a guide for further optimization of the DRTP process.

4.4.1 Printed n-Type Si NRFET by DRTP

The direct roll printing technique was employed to fabricate top-gated field-effect transistors (FETs) using the Si NRs printed on a flexible PI substrate. Top-gate geometry was preferred due to its ability to wrap the electrode around the nanostructure, enabling effective control of charge transport. For the fabrication of the top-gated FETs, a gate dielectric needed to be deposited at room temperature (RT) with minimal defect density at the semiconductor/dielectric interface while providing a large capacitance per unit area. The ICP-CVD technique was used to deposit high-quality dielectric (SiOx, SiNx, etc.) at RT without any plasma-related harmful effects [58]. We have used RT deposited SiN_x as our top-gate dielectric material as it has been widely explored gate dielectric material for III–V devices and oxide thin-film transistors exhibiting good device performance. Figure 4.10a presents the schematic and optical images of fabricated top-gated n-type Si NR-FET devices.

4.4.1.1 Electrical characterisation of n-type Si NRFETs

The output characteristics (V_{DS}–I_{DS}) of Si NR-FET in Fig. 4.10b show the varying gate bias (V_{GS}) from 0V to 4V with the step of 1V by sweeping drain source bias (V_{DS}) from –3V to +3V (only positive V_{DS} voltages illustrated). As V_{GS} increases towards positive voltage, the corresponding drain current (I_{DS}) is also increased, confirming that the device is n-channel. Due to the n+ doping and low energetic contact barriers, the variation of I_{DS} with V_{DS} is linear without any inflection point at low-V_{DS} region (V_{DS} ≤~0.1 V). The transfer characteristics (I_{DS}–V_{GS}) of Si NR-FET with V_{DS} of 0.1 V were obtained by varying V_{GS} from −10 to 10 V (Fig. 4.10c). In terms of the electrical performance of the NR-FET, the main parameters to consider are on-state (I_{on}), off-state current (I_{off}), current on/off ratio (I_{on}/I_{off}), and effective mobility (μ_{eff}), and subthreshold slope (SS). The logarithmic plot of the transfer curve in Fig. 4.10c revealed an Ion (~60 µA)/I_{off} (<0.1 nA) current ratio of >10^6 suggesting an excellent gate-channel control.

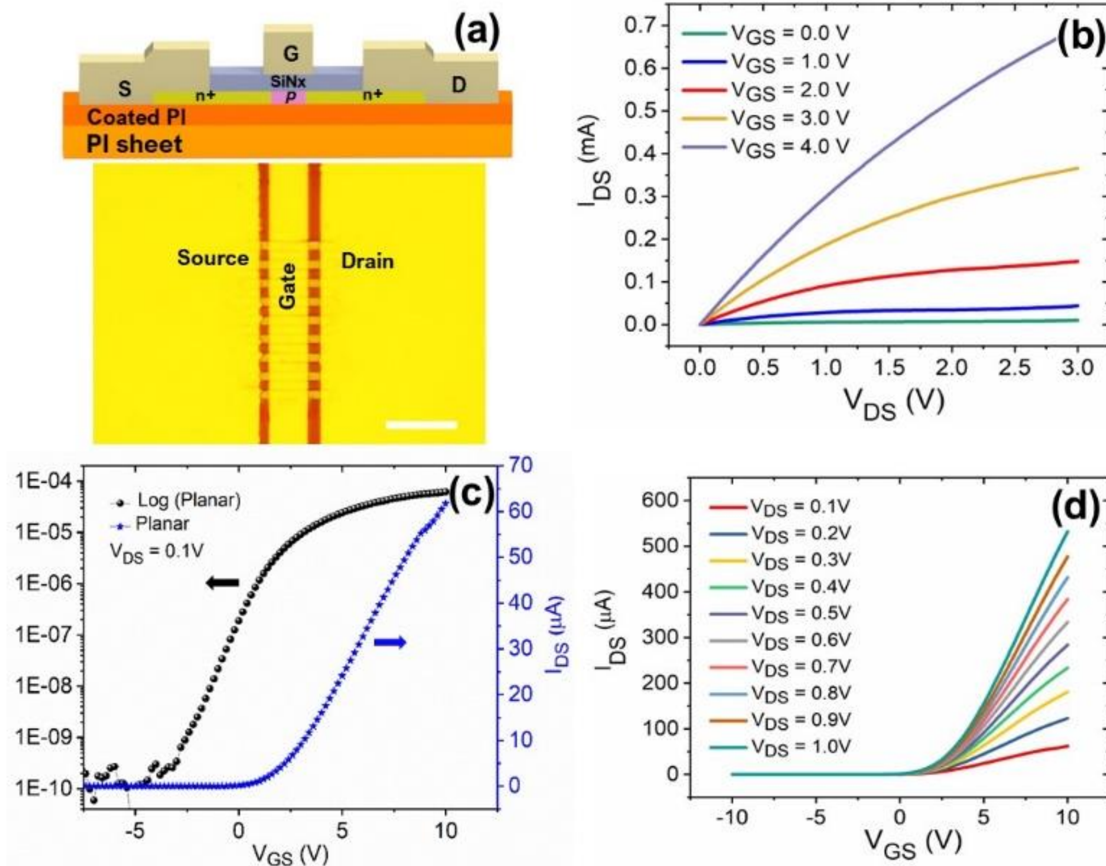


Figure 4.10: Electrical characteristics of Si NRFETs. **(a)** Schematic cross-sectional view of the Si NRFET device (Scale bar=50um). **(b)** Output characteristics of Si-NRFET. **(c)** Transfer

characteristics (I_{DS}-V_{GS}) of Si NRFET with V_{DS} = 0.1V in logarithmic and linear scales. (d) Transfer characteristics (I_{DS}-V_{GS}) of Si NRFET with V_{DS} varying from 0.1V to 1V with the step of 0.1V.

Figure 4.10d shows the transfer characteristics of Si NRFET at various values of V_{DS}. It is worth noting from Fig. 4.10d that the threshold voltage (V_{th}) remains constant with applied voltage V_{DS}, indicating high stability charge transport behaviour under different voltages. The mobility of the device was extracted based on the conventional MOSFET model in the linear regime [58] (see section 3.3). The extracted effective mobility (μ_{eff}) is ~ 631 cm^2/Vs. The threshold voltage (V_{th}) measured through extrapolation in the linear region of Si NRFET is ~ 0.4 V. The extracted subthreshold slope (SS) is ~1000 mV/decade (using the semi-logarithmic plot of the transfer scan). Table 4.2 compares the extracted electrical parameters of n-type Si NRFETs fabricated using NRs transferred through direct roll printing process and those using other transfer printing techniques. It can be seen that the extracted mobility compares well with most of the state-of-the-art Si NR based devices and is higher than nanomeshed Si nanomembrane based FET devices [180]. The μ_{eff} value is marginally lower than the previously reported value (680 cm^2/Vs) employing self-assembled nanodielectrics (SAND) dielectric (15 nm thick). However, process to deposit SAND is time consuming and requires additional efforts in terms of solution processing in controlled ambient and hence may not be suitable for scalable high throughput processing [58]. Instead with deposition of a thinner a thinner SiN_x dielectric, the mobility of roll printed devices could be enhanced further. The extracted subthreshold slope (SS) value is significantly higher for the roll printed devices. It may be noted that, in the absence of surface anomalies, the theoretical limit of SS is around 60 mV/dec. The calculated subthreshold swing is ~8 times higher than one of the best examples in literature (∼120 mV/dec) using SAND [141], and ∼16 times larger than the theoretical limit in CMOS. As mentioned above, thin gate dielectric could improve the gate control over the channel and thus reduce the SS values close to the state of the art. To evaluate the performance of the fabricated transistors using printed Si nanoribbons (NSs) as the active device channel.

Table 4.2: The table compares the fabricated transistor performance using printed NSs as an active device channel.

S.No.	Transfer printing method	Si Micro/nano-structure morphology	Source wafer	Threshold Voltage (V)	Subthreshold slope (mV/decades)	Mobility (cm^2/Vs)	On /Off ratio	Ref.
1	Kinetically controlled transfer printing	Si membrane (300nm thick)	SOI	~1.1 ± 0.05 V	120	680	10^7	[141]
2	Glue assisted transfer printing	Si membrane (100nm thick)	SOI	~ 0.0 V	N/A	240	10^5	[93]
3	Conventional transfer printing using elastomer stamp	Nanoribbons ribbon Length (55 µm), thickness (70 nm thick)	SOI	~ -0.87 V	182	656	10^6	[58]
4	Flip transfer printing using SU8 as adhesive	Si membrane (340nm thick)	SOI	~ 0.95 V	480	160	10^6	[172]
5	Flip transfer printing using SU8 as adhesive	Si membrane (270nm thick)	SOI	~ 0.85	550	160	10^6	[181]
6	Conventional transfer printing using elastomer stamp	Si ribbons	Bulk Si <111>	N/A	N/A	360	10^3	[63]
7	Direct roll transfer printing (DRTP)	Nanoribbons ribbon Length (55 µm), thickness (70 nm thick)	SOI	~ 0.4 V	1000	631	10^6	This work

N/A – data not available

The table 4.2 summarizes the electrical characteristics such as on/off ratio, threshold voltage, subthreshold swing, and field-effect mobility, as well as the dimensions of the devices such as channel length and width. These parameters are crucial in determining the suitability of the printed NSs for use in high-performance transistors. The data presented in the table provide insights into the performance of the printed NSs-based transistors and demonstrate their potential for use in various electronic applications.

In nanomaterial-based FETs, working in depletion/accumulation mode, the dielectric/ semiconductor interface quality plays a dominant role is defining the transistor performance and electric-bias stability. To this end, we quantified the occupied trap charge density at the SiNx/Si NR interface (D_{it}) using the following relation [55, 182]:

$$\Delta Q = \Delta V_{th} \times Cox \qquad (4.1)$$

To calculate the hysteresis (i.e., ΔV_{th}), the forward and reverse transfer scans were performed between −5 V_{GS} to +10 V_{GS}. As shown in the Fig. 4.11, negligible hysteresis (0.4V) is observed for the NRFETs. Using the hysteresis data, the Si NRFET showed a D_{it} value of 1.7×10^{11} /cm^2 (ΔV_{th} = 0.4V, and $C_{ox} = 7\times10^{-4}$ F/m^2). The estimated value of D_{it}

at the SiNx/Si NR interface is an order of magnitude less than the SiO_2/semiconductor interface for nanomaterial-based FETs [182, 183].

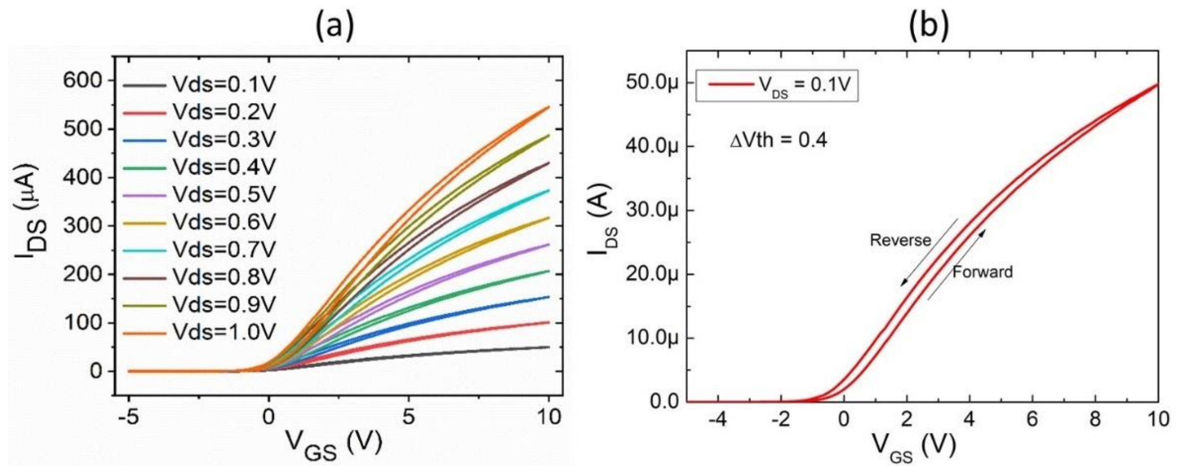


Figure 4.11: Measured forward and reverse transfer characteristics (I_{DS} VS V_{GS}) to follow the hysteresis of the device at different V_{DS}**.** **(a)** at various values of V_{DS} from 0.1V to 1V with the step of 0.1 V. **(b)** At V_{DS} = 0.1V.

4.4.1.2 Electromechanical characterization of n-type Si NRFETs

The mechanical robustness and device stability of the fabricated flexible Si NRFETs were evaluated under different bending conditions. The electrical characterisation results under bending are shown in Fig. 4.12. The device was subjected to tension and compression by mounting it on to a 3D printed convex and concave structures. For both bending types, the radius of bending curvature was 40 mm, as shown in the inset of Fig. 4.12a. The transfer and output characteristics under bending are shown in Fig. 4.12a and 4.12b, respectively.

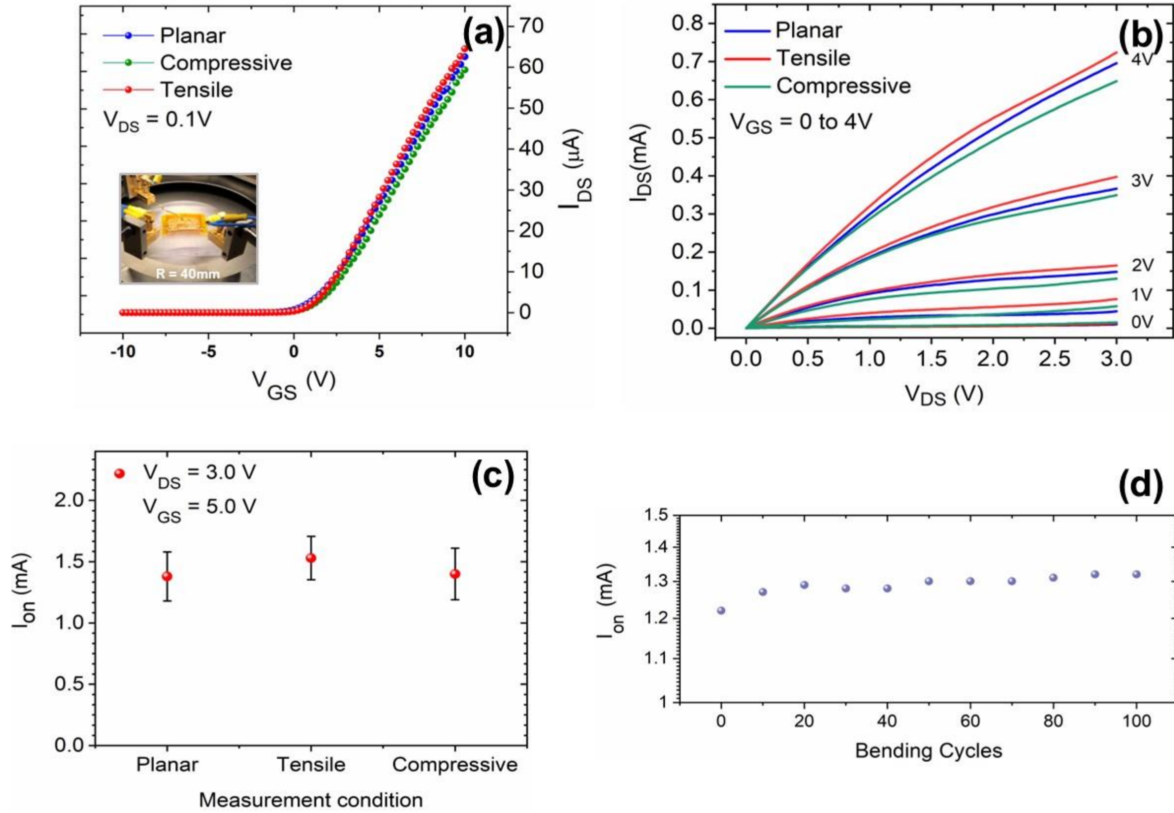


Figure 4.12: Electro-mechanical characterization of printed Si NRFETs. **(a)** Measured transfer characteristic (I_{DS} vs. V_{GS}) of Si-NRFET under planar, tensile and compressive bending conditions. **(b)** Output characteristics of Si-NRFET at planar, and under bending conditions (Radius of curvature (Rc) =40mm)). **(c)** Variation of the on-state current at V_{GS} = 5V at compressive and tensile bending cycles. **(d)** Variation of the drain current at planar condition during compressive and tensile bending cycles at V_{DS}= 3V, V_{GS}= 5 V.

As can be seen, the device showed slight variation in I_{on} while V_{th}, SS and other device parameters were largely remained unchanged. The effect of mechanical stress on the I_{on} of NRFET under compressive and tensile bending cycle were investigated with V_{GS} = 5V and V_{DS} = 3V for five randomly chosen n-type NRFET devices (Fig. 4.12c). The mechanical bending and the resulting strain are known to affect the semiconducting material's band structure, which affects the effective mass and hence the mobility of the charge carriers [34, 163]. The change in mobility has a direct effect over the source current of the transistor. As expected, a tensile bending strain led to a slight increase in the I_{DS}, whereas a compressive bending led to decrease in I_{DS} [58]. To inspect the mechanical robustness the fabricated NRFETs were subjected to 100 bending cycles and corresponding drain currents are illustrated in Fig. 4.12d. The peak values of drain current under planar condition after every

10 cycles of compressive and tensile bending (Rc = 40 mm) were obtained. As can be seen from this set of data, the I_{on} showed near stable response with repeated bending. The minor variation in the electrical properties during cyclic bending is attributed to two main factors. First, the mechanical bending results in the change of the band structure of the active material (Si), affects the effective mass and hence the mobility of the charge carrier [32, 163]. Second, is the delamination of device layers including metal contacts. These can be mitigated and addressed by adding an encapsulation layer on top of the final device/circuits. Such a layout has been demonstrated in the past with a thin layer of polymer as an encapsulant (usually the same material as substrate) on top of Si NRFET. Such a configuration enables high flexibility along with stable electrical properties by bringing the devices at the neutral mechanical plane and prevents the device from experiencing any strain induced variations caused during cyclic bending. This could enhance the bendability, device stability and also resolve the slight variation of the electrical properties under bending conditions [45].

4.4.2 Printed p-Type Si NRFET by DRTP

Recently, the metal-oxide based thin-film transistors TFT technology has been used to develop a 32-bit flexible microprocessor. The limitation here is that only n-channel transistors can be fabricated because there is currently no viable p-type metal oxide material available for large-area commercial fabrication [23, 184, 185]. In this case, a more complicated layout based on n-type transistors and resistors is needed to implement the logic functions. This will result in higher power consumption as compared with CMOS architecture which is detrimental to flexible electronics as higher power dissipation could degrade the plastic substrate. Moreover, the modest-mobility of metal oxides lead to slower circuit operation (switching frequency – 29 kHz). Whilst these are interesting developments, they do not meet the need for flexible CMOS circuits having performance at par with conventional integrated circuits (ICs). This is much needed to drive advances in several application areas of flexible electronics.

The efficacy of DRTP approach was shown in the previous section by demonstrating high-performance n-type Si nanoribbons-based field effect transistor (NRFETs) over flexible polyamide (PI) substrate [52]. Further, the potential of extending this approach towards high-performance printed CMOS circuits was demonstrated through preliminary analysis of *p*-type NRFET presented in SSDM 2021 conference [52, 186]. Advancing this work further, herein we present the in-depth analysis of direct roll transferred p-type Si NR-based FETs. The fabricated devices have shown excellent device performance; charge carrier mobility of 100±10 $cm^2\ V^{-1}.\ s^{-1}$ and current on/off ratio $>10^4$. Further, we have done detailed electrical characterization under mechanical bending (40 mm) and at wide temperature range (15 to 90 °C) conditions to confirm the robustness of fabricated transistors for high-performance flexible electronic circuits. The work presented on p-type FETs complements previous research on n-type FETs and creates new opportunities for realizing both device types on the same substrate. This development is critical for achieving high-performance printed CMOS circuits on diverse plastic substrates in the future.

4.4.2.1 Electrical characterisation of p-type Si NRFETs

Following the device structures used for n-type Si NRFET [58] (as described in Section 3.3.1), p-type NRFET devices were fabricated with dimensions similar to the n-type NRFET devices. The devices were characterized under ambient dark conditions, with a channel length of approximately 45 µm and a width of approximately 5 µm on flexible PI substrates. The electrical characterization results of a typical p-type FET device are presented in Fig. 4.13(b-d).

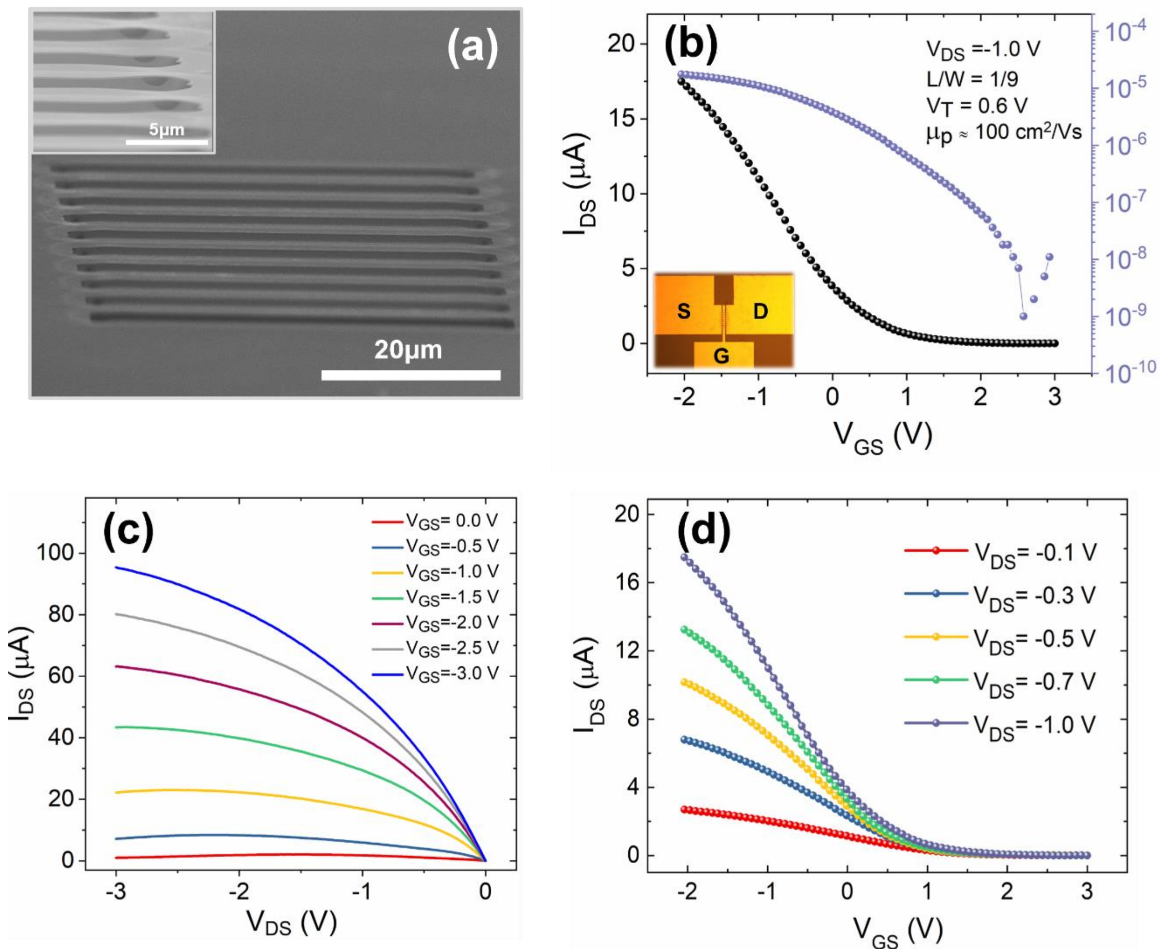


Figure 4.13: p-type Si NR-based FET and its electrical characteristics: **(a)** SEM cross-sectional image of an anchored single Si NR array after etching away the Box layer. The inset shows the magnified image of the anchor point. **(b)** Transfer characteristics with $V_{DS} = -1$ V in logarithmic and linear scales. The bottom inset shows an optical image of a typically fabricated transistor. **(c)** Output characteristics, and **(d)** transfer characteristics with varying V_{DS} from −0.1 to −1V.

The transfer characteristics (I_{DS}-V_{GS}) with drain bias (V_{DS}) of -1 V were obtained by varying gate-source voltage (V_{GS}) from 3 to -2 V and shown in both linear and logarithmic scale in Fig. 4.13b. Critical FET performance parameters to consider were extracted using the transfer scan: on-state (I_{on}), off-state current (I_{off}), current on/off ratio (I_{on}/I_{off}), effective mobility (μ_{eff}), and subthreshold slope (SS) [187]. The measured devices showed typical I_{on} (>10 µA) / I_{off} (<1 nA) current ratio of $>10^4$ suggesting an excellent gate-channel control. The extracted SS from the logarithm transfer plot is 1±0.3 V/decade. Large variation in SS suggests non-uniformity in the deposited SiN_x dielectric film and/or presence of interface traps between the channel and SiN_x interface non-uniformly. Further experiments are

needed to confirm the exact reason for variation in SS. Next, threshold voltage (V_T) was extracted using the linear extrapolation method. For this, the linear extrapolation of I_{DS}–V_{GS} graph, intercepting the $I_d = 0$ at x-axis (V_{GS}) gives the V_T value (0.6V). This was followed by the calculation of transconductance (g_m), according to equation 3.6 highlighted in section 3.1. The extracted g_m was used to calculate the field-effect (effective) mobility, μ_{eff}, using equation 3.8 where W and L are the gate width and length respectively and C_{OX} stands for the dielectric capacitance (W/L = 45μm/5μm, thickness of SiN_x dielectric = 100nm). The extracted effective mobility was found to be ~100 ± 10 $cm^2.V^{-1}s^{-1}$ which compares well with most of the state-of-the-art p-channel Si NR based FETs. Further, the performance of DRTS p-channel NRFET is compared with the other p-channel devices fabricated using conventional transfer-based technique (Table 4.3).

Table 4.3: Si micro/nanostructures-based flexible p-type FETs realised using transfer-printing based techniques.

S. No	Transfer Techniques	Si -structure morphology	Mobility ($cm^2.V^{-1}s^{-1}$)	I_{ON}/I_{OFF}	Ref.
1.	Flip-transfer printing	Sub-μm membranes (340-nm thick)	34	~10^6	[172]
2.	Conventional transfer printing	Nanoribbons (100-nm thick)	14	10^5	[188]
3.	Conventional transfer printing	Sub-μm ribbons (290-nm thick)	85 ± 10	~10^6	[189]
4.	Direct Roll Transfer stamping	Nanoribbons (70-nm thick)	100 ± 10	>10^4	This work

Next, the output characteristics (V_{DS} - I_{DS}) was obtained by varying V_{GS} from 0 V to -3V with step of 0.5V. Notably, the low-V_{DS} region shows a linear dependence of I_{DS} with increasing V_{DS} without any inflection point. This device characteristic (low-resistive metal-semiconductor (MS) contacts) is needed for achieving high device performance. Further, the output characteristics shows strong drain current saturation (I_{DS}^{SAT}) with increasing V_{DS}, confirming the excellent gate-channel capacitive coupling. To confirm the MS contact ohmicity, we have calculated the ratio of the change in the saturation voltage (V_{DS}^{SAT}) with V_{GS}. In conventional transistors with ohmic contacts, gradual channel approximation model

is used to describe the drain current saturation [187]: $V_{DS}^{SAT} \approx [V_{GS}–V_T]$. According to the theory, the ratio of the change in the saturation voltage with gate voltage, for FETs with ohmic contacts, would be close to unity. The fabricated p-type FETs showed $\frac{\partial V_{DS}^{SAT}}{\partial V_{GS}} \approx 1$ (confirming formation of ohmic contacts). Fig. 4.13d shows the transfer characteristics of Si NRFET at various values of V_{DS}. It is worth noting from Fig. 4.13d that the V_T remains constant with varying V_{DS}, indicating high stability charge transport behavior under different drain voltages. We have further studied the device stability under bending and varying temperature conditions in the following sections.

4.4.2.2 Stability analysis of flexible p-type Si NRFETs

The mechanical robustness of the flexible p-type NRFETs were evaluated under different bending conditions. We obtained the transfer characteristic under planar condition after bending by mounting the device on a 3D printed convex and concave structures both with radius of curvature of 30 mm. The cyclic bending measurement was performed after every 10 cycles (up to 100 cycles). An optical image showing durability test by repeating device bending up to 100 times is included in the inset of Fig. 4.14a. Using the transfer characteristics, variation in the on-current (Fig. 4.14a) and threshold voltage (Fig. 4.14b) of the device were extracted. The peak values of drain current were obtained at V_{GS} = -3V. As can be seen from this set of data, the I_{on} showed a 23% rise after 100 bending cycles. On the other hand, the V_T of the device showed slight random variations initially (up to 60 bending cycles) but it eventually stabilized to the initial V_T value. As shown in figure 4.14, this change in the electrical performance after bending could be attributed to the change of the band structure of the active material (Si), which affects the effective mass and hence the mobility of the charge carrier [36, 190]. Such a bending related variation in device performance could be solved by adding an encapsulation layer on top of the final device or by placing the device in the neutral plane [45, 191]. This could enhance the bendability, device stability and also resolve the slight variation of the electrical properties under bending conditions [45].

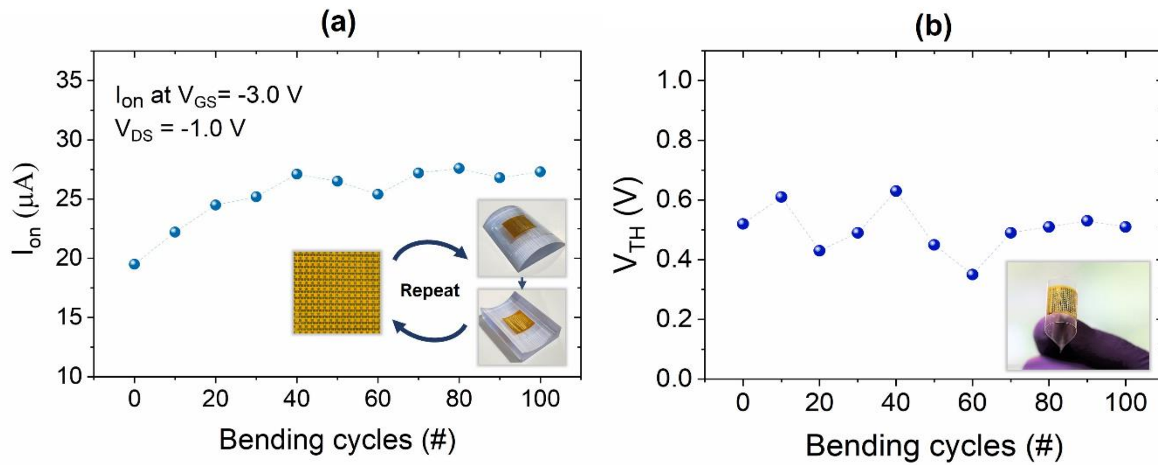


Figure 4.14: Variation of the I_{DS} **(a)** and V_T **(b)** measured in planar condition after compressive and tensile bending cycles at $V_{DS} = -1V$, $V_{GS} = -3V$.The inset of panel **(a)** shows optical images of devices during durability test when being under planar and bent conditions. The inset of **(b)** shows a photograph of flexible p-type NRFET arrays fabricated on PI substrate.

The temperature dependence device stability is also studied in this work (Fig. 4.15). Before we measured the transfer characteristics, gate leakage current was monitored at different temperatures of the present device under investigation. This was performed to evaluate the dielectric stability at different temperatures. The mechanical robustness of the RT deposited SiN_x under different bending conditions was tested and reported in our previous work [58]. In this work, we have studied temperature dependent stability. As shown in Fig. 4.15a, there is one order decrease in gate leakage current from 3 nA to 0.3 nA at $5V_{GS}$ when temperature was increased from 15 to 90 °C. Although there is variation in leakage current, the values remain very low which confirms high quality, and robustness of the RT deposited dielectric at wide temperature range. Next, transfer scans (in forward (+5 to -2 V_{GS}) and reverse (-2 to +5 V_{GS}) direction) were obtained at different temperatures (15 to 90 °C with a step of 5 °C), as shown in Fig. 4.15b. Important FET parameters were extracted using temperature varying transfer scans and are shown in different figure panels of Fig. 4.15 As can be seen in Fig. 4.15b, the I_{on} of the device showed sharp decrease after 35 °C with a stepwise increase in temperature. Similarly, I_{off} showed a slight decrease with an increase in temperature. This could be explained through increase of scattering events (acoustic-phonon assisted and Coulombic) in the channel and/or at the semiconductor/dielectric interface, which degrades the charge transport efficiency [192].

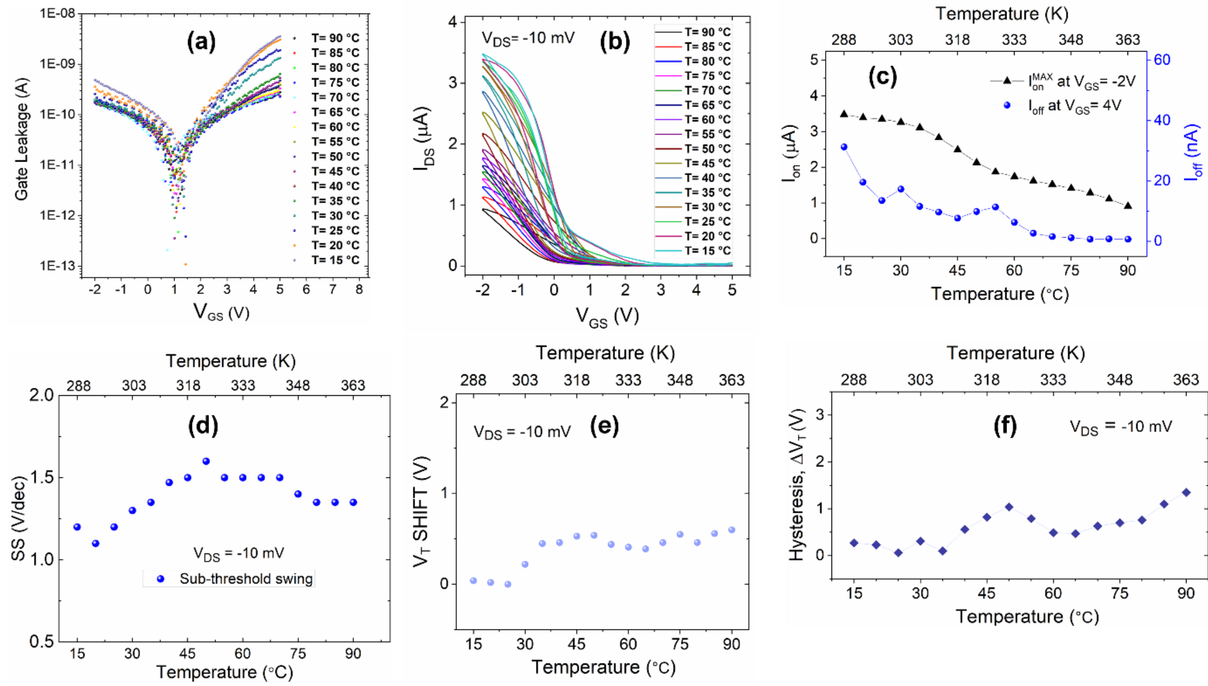


Figure 4.15: Temperature-dependent (From 15 °C to 90 °C) electrical characterizations to investigate the stability of p-type NRFETs. **(a)** Gate dielectric leakage current, and **(b)** transfer scans. Important FET parameters data extracted using temperature-dependent transfer scans: **(c)** on-current and off-current, **(d)** S–S, (e) V_T, and **(f)** hysteresis.

In fact, the gain in kinetic energy of the charge carrier, with increasing temperature, alters two distinct phenomenon that could affects the charge transport in FETs (in the range of temperature we have performed measurements): (i) scattering events in the channel and/or channel/dielectric interface, and (ii) increase of thermionic current. Which one of these will dominate the charge transport depends on the nature of MS contact in FETs. For Schottky contacted FETs, the I_{on} and I_{off} should show an increase in values [187]. This is because charge carriers acquire sufficiently high kinetic energy with increasing temperature to overcome the MS contact potential barrier and thus, thermionic emission current component will increase. On the other hand, for an ideal ohmic contacted FETs, scattering events will dominate the charge transport as there will be negligible increase in the thermionic emission part. As we showed above using the family of output scans, the FET device demonstrated electrical behavior of a typical ohmic MS contact device which could explain the negative temperature dependence of FET current with temperature. To gain further insight on the

decrease in I_{on}, we have analyzed other important FET parameters including SS, V_T, and hysteresis. The change in SS with temperature change is shown in Fig. 4.15d. This figure reveals that, the absolute SS value increases sharply above RT (1.1 V/dec) up to 45-50 °C (1.5 V/dec). After 50 °C, SS saturates, remains constant until 70 °C, and shows slight degradation after that. It is well known that SS of a FET device is largely affected by the interface (channel/dielectric) trap charge density. Also, these interface charges lead to shift in FET threshold voltage. To corelate the change in SS trend to interface traps, we have calculated the magnitude shift of V_T with temperature (Fig 4.15e). The data in Fig. 4.15e shows a similar trend like SS change with temperature. Accordingly, both SS and V_T change can be correlated to the transfer of mobile charges to immobile trapping states at the semiconductor/insulator interface. Finally, we have monitored the magnitude of these interface charges by calculating the hysteresis value (change in V_T of forward and reverse transfer scan) at each temperature (Fig. 4.15f). As expected, after 35 °C, there is sharp increase of the hysteresis up to 50-55 °C and then it saturates. The analyzed data shows a significant increase in the interface trap density above 30-35 °C which leads to an increase in the scattering events at the channel/dielectric interface. Thus, the sharp decrease in the device on-current after 35 °C could be related to the thermal activation of interface traps that degrade the charge transport.

4.4.3 DRTP for high-performance transient electronics

Transient Electronics is on the rise as practical difficulties related to electronic waste (e-waste) requires greater attention [193-197]. The unique characteristics of this emerging class of technology is that it completely disintegrates and/or dissolves into environment friendly by-products within a programmed period [198]. With these features, transient electronics has huge potential to transform and expand the functional capabilities of vertical sectors including consumer electronics, medical etc. with minimal adverse impact on environment through generation of electronic waste (e-waste). Towards this, environmentally benign organic/bio-organic based electronic materials have been explored to fabricate transient device/circuits including flexible complementary metal-oxide semiconductor (CMOS) circuits [194]. However, due to the poor charge carrier mobility, these electronic circuits do

not match the performance of conventional integrated circuits (ICs) and as a result their application is restricted to low-end. High-performance is much needed to drive advances in nearly all conventional and emerging application areas of electronics including connected systems, Industry, digital healthcare, digital agriculture, and interactive systems etc., where high speed electronics is required to reduce the data latency [199, 200]. In this regard, nanostructures such as nanowires (NWs), nanoribbons (NRs) [57, 58] etc. and thin-films of high-mobility inorganic materials offer a viable alternative. Their performance is on par with conventional silicon-based devices, and they can also be dissolved or disintegrated in controlled environments (**Table 4.4**) [49, 196, 197].

Towards this, sputtered thin-films of semiconducting inorganic oxides (zinc oxide and indium gallium zinc oxide) on green (biodegradable) substrates have shown potential for physically transient forms of electronics for applications such as active-matrix light emitting diode backplanes [196, 201]. The obtained n-channel device mobility of ~7 cm^2/Vs is sufficient for such applications but still not enough for high-speed applications. Further, lack of viable p-type metal oxide materials resulted into implementation of a more complicated layout based on n-channel transistors and resistors for the logic functions [23]. The drawback is the higher power consumption as compared with the complementary metal oxide semiconductor (CMOS) architecture. A significant impulse to transient electronics came from the use of silicon nanostructures including NRs and nanomembranes (NMs) as an active transistor channel material enabling electron mobility of >500 cm^2/Vs and hole mobility of ~100 $cm^2/V.s$ [195, 197, 202] Accordingly, innovative attempts have been made to integrate high mobility silicon nanostructures over variety of biodegradable substrates such as organic polymers, metal foils etc. using transfer and contact printing methods [49]. In these cases, transfer printing has received intense research interest due to facile pick-and-place approach. It allows integration and assembly of nano to chip scale structures from the donor to the target substrate [49].

4.4.3.1 n-Type Printed Transistors on Biodegradable Substrate

In this work, we have used direct roll printing to transfer silicon NRs arrays over biodegradable magnesium (Mg) metal foils as device substrates. Mg was chosen as device substrate due to its inherent advantages including high thermal stability, chemical stability, hermeticity, biodegradability, and biocompatibility [203]. In the past, metal foils such as Mo, Fe, W etc. have been explored for fabrication of high performance transient transistors using conventional transfer printing technique [203]. We show here for the first time the capability of the direct roll transfer printing approach to integrate arrays of Si NRs on Mg foils for high-performance transient transistors. It is important to mention that surface roughness plays a crucial role in the integration performance of inorganic nanostructures on flexible substrates [204]. To address the issue of high roughness commonly found in metal foils including Mg, a 2 µm thick layer of SiO_2 was deposited using plasma chemical vapor deposition (PECVD) to enhance surface smoothness. The SiO_2 layer acts as an insulating layer and helps prevent defects such as wrinkles and cracks on the substrate surface, thereby improving the transfer yield. For the transfer printing process, a roll stage printing setup was employed to hold the target Mg foil coated with a semi-cured PI layer on top. The PI was selected as the adhesive layer due to its ability to withstand in vivo conditions and its certification as biocompatible [205]. Next, the donor SOI wafer was brought in contact with the semi-cured PI to transfer the Si NRs. Following the transfer printing of NRs, a room temperature (RT) fabrication process including dielectric (SiN_x) deposition was performed to realize high-performance n-type transistors. The developed transient transistors exhibit excellent electrical properties including high effective mobility of >600 cm^2/Vs, high on/off current ratio ($I_{on/off}$) of $>10^4$, and low gate leakage (0.2 nA). Along with the biodegradability, transient devices are expected to have a stable device operation over a predefined time frame. This could be difficult to achieve due to the intrinsic water-soluble nature of the biodegradable materials used during the fabrication. In this regard, we have performed in-depth study of the device stability which includes ageing effect, temperature dependent stability, and electrical gate-bias stress study. Our stability study confirms robust device performance under applied temperature and gate-bias stress and for more than three months

of the collected data. This confirms the high-quality of the developed fabrication process. Further, the effects of transience on the electrical functioning of devices on Mg foils in aqueous solution of pH-8 at 37°C are systematically studied by hydrolysis. Finally, we have performed the biodegradable studies of the transistor devices in aqueous solution at different pH scales and constant temperature of 37°C to extract the etching rate of the Mg foil.

Table 4.4: State-of-the-art high mobility biodegradable substrates for high-speed transient electronics. NMs – nanomembranes; NRs – nanoribbons; PLA – poly lactic acid; PLGA – poly lacticco- glycolic acid; PGA – poly glycolic acid; Mg – Magnesium.

Channel material	Channel dimensions (µm)	Performance (Mobility, cm^2/Vs)	Electronic layer deposition method	Dielectric Material	Biodegradable Substrate	Ref.
Si NMs	P-type (L = 5; W = 300)	70	Transfer Printing	SiO_2	PLGA, PLA, PGA	[195]
	N-type (L = 15; W = 100)	400				
Si NMs	N-type (L = 20; W = 900)	660	Transfer Printing	MgO	Silk	[197]
ZnO film	N-type (L = 20; W = 500)	0.95	Sputtering	MgO	Silk	[196]
Si	N-type (L = 1.8; W = 6)	630	Transfer Printing	SiN/SiO_2	PLGA substrate	[202]

4.4.3.2 Electrical characterisation

The fabricated n-type transient transistors with length ~5 µm and width ~45 µm on Mg foils were characterised in ambient dark conditions. The electrical characterisation results and schematic/optical image of fabricated n-channel devices are shown in Figure 4.16. The transfer characteristics (I_{DS}-V_{GS}), with drain bias (V_{DS}) of 10 mV, were obtained by varying gate-source voltage (V_{GS}) from -5 to 10 V and shown in both linear and logarithmic scale.

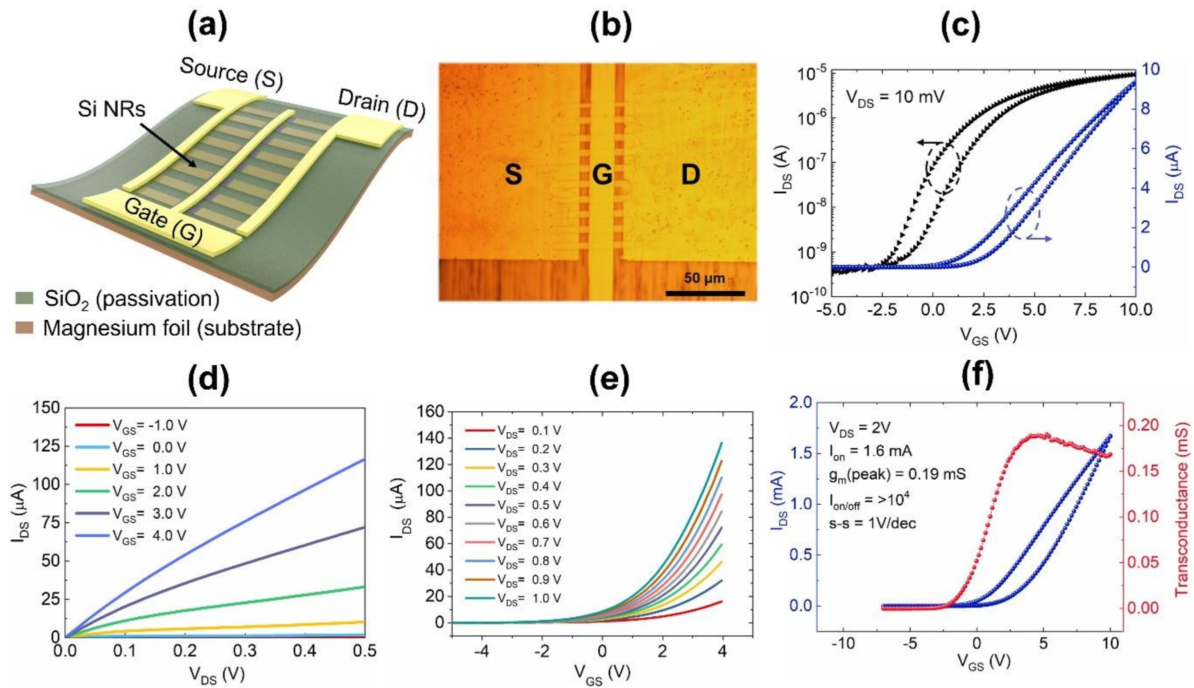


Figure 4.16: n-type transient transistor and its electrical characteristics: **(a)** schematic and **(b)** optical image, **(c)** transfer characteristics at V_{DS} = 10 mV in logarithmic and linear scales, **(d)** output characteristics, **(e)** transfer characteristics with varying V_{DS} from 0.1V to 1V, and **(f)** transfer characteristics at V_{DS} = 2V (transconductance is shown as secondary y-axis).

The high-grade electronic properties of the printed NRs such as mobility allowed the device to operate at ultra-low V_{DS} of 10 mV. The critical FET performance parameters to consider were extracted using the transfer scan: on-state (I_{on}), off-state current (I_{off}), current on/off ratio (I_{on}/I_{off}), effective mobility (μ_{eff}), and subthreshold slope (S-S) [187]. The measured devices showed typical I_{on} (~10 µA) / I_{off} (<1 nA) current ratio of >10^4 suggesting an excellent gate-channel control. The extracted S-S from the logarithm transfer plot is 0.9±0.2 V/decade. Next, threshold voltage (V_T) was extracted using the linear extrapolation method. For this, the linear extrapolation of I_{DS}–V_{GS} graph, intercepting the I_d = 0 at x-axis (V_{GS}) gives the V_T value (1.4 V). This was followed by the calculation of transconductance (g_m), according with Equation 3.6, section 3.1. Next, the field-effect (effective) mobility was extracted using the conventional MOSFET model in the linear regime [52, 57]. The extracted effective mobility was found to be ~640 ± 10 cm^2/Vs which compares well with most of the state-of-the-art n-type Si NR based FETs on biodegradable substrates. Further, the performance of direct transfer n-type transient transistor is compared with the similar

n-type devices on flexible PI substrates (Appendix, table 8.4). Interestingly, the performance of the transient transistor devices is like the one fabricated on PI substrates. This confirms the efficacy and substrate-independency of the developed RT printing and overall fabrication process. To evaluate the potential of the fabricated transient transistor in the high-speed (computation and/or communication) applications such as IoT, the theoretical cut-off frequency f_T is extracted using the following equation [206]:

$$f_T = \frac{\mu_{eff} V_{DS}}{2\pi L\ (L + L_{ov,GS} + L_{ov,GD})} \qquad (4.2)$$

Where $L_{ov,GS}$ is the parasitic gate-to-source overlap, and $L_{ov,GD}$ is the parasitic gate-to-drain overlap. Neglecting the parasitic capacitances, the f_T of n-type transient transistor with a channel length of 5µm and mobility of 640 cm^2/Vs is estimated to be more than 800 MHz which can be further enhanced by reducing the channel length and contact resistance in future optimized design. Nevertheless, it is already few orders higher than the state-of-the-art transistor devices based on organics and metal oxides [22, 206, 207]. Such a high device performance can provide excellent opportunities for biodegradable implantable electronics that do not require removal. The transient Integrated Circuits (ICs) fabricated using the demonstrated transistors, could also perform complex logic functions enabling self-monitoring implantable systems [208, 209]. For continuous recording of the sensed signals, implantable wireless communication devices need to operate inside the body. Recently, the feasibility of Bluetooth Low Energy (BLE) technology for ingestible and implantable medical device applications has been demonstrated by studying radio frequency (RF) signal attenuation in different tissue types [210]. It was experimentally shown that the device orientation as it moves through the body has negligible impact on the RF signal attenuation. In future, such high-performance transient ICs can be integrated with BLE devices applications for biomedical implants.

Next, the output characteristics (V_{DS} - I_{DS}) was obtained by varying V_{GS} from -1 to 4V with step of 1V. Notably, the low V_{DS} region shows a linear dependence of I_{DS} with increasing V_{DS} without any inflection point. This device characteristic (low-resistive metal-semiconductor (MS) contacts) is needed for achieving high device performance. Figure 4.16e

shows the transfer characteristics of n-type transient transistors at various values of V_{DS}. It is worth noting from Figure 4.16e that the V_T remains constant with varying V_{DS}, indicating high stability charge transport behavior under different drain voltages. Finally, the device transfer characteristics were measured at high V_{DS} of 2V (Figure 4.16f). At this bias voltage, the developed biodegradable n-type transistors presented a high on/off current ratio ($I_{on}/_{off}$) of $>10^4$, transconductance of 0.19 mS, and an on-current of 1.6 mA.

4.4.3.3 Bias Stress Dependent Stability Study

Stable and reliable transistor operation is critical for any practical application to allow correct execution of programmed duties of ICs over its lifetime. This becomes even more crucial for transient devices which could easily collapse from different available ambient sources including hydrolysis triggered by light [211], heat [212], moisture [201], electrochemical [213], or physicochemical [198]. For this, we have assessed the stability of our transistor devices under different stress conditions including electric (gate bias and continuous cycles), temperature, and evaluated the degradation of devices performance related to ageing for more than 3 months. Figure 4.17 shows results of the continuous electric bias stress where the transfer scans were performed continuously for up to >3000 cycles (~24h). The I_{DS} was monitored by sweeping the V_{GS} from −6 to +6 V (forward voltage sweep) and from +6 to −6 V (reverse voltage sweep) at a constant V_{DS} = 10 mV. A full transfer scan (from forward to reverse voltage sweep) is treated as one stress cycle. The transfer scans were used to extract the key transistor performance parameters namely, I_{on}, I_{off}, $I_{on/off}$ ratio, S-S, and hysteresis (from the V_T value of forward and reverse scan). Both I_{on} (Figure 4.17b) and I_{off} (Figure 4.17c) decrease with the increase in stress time.

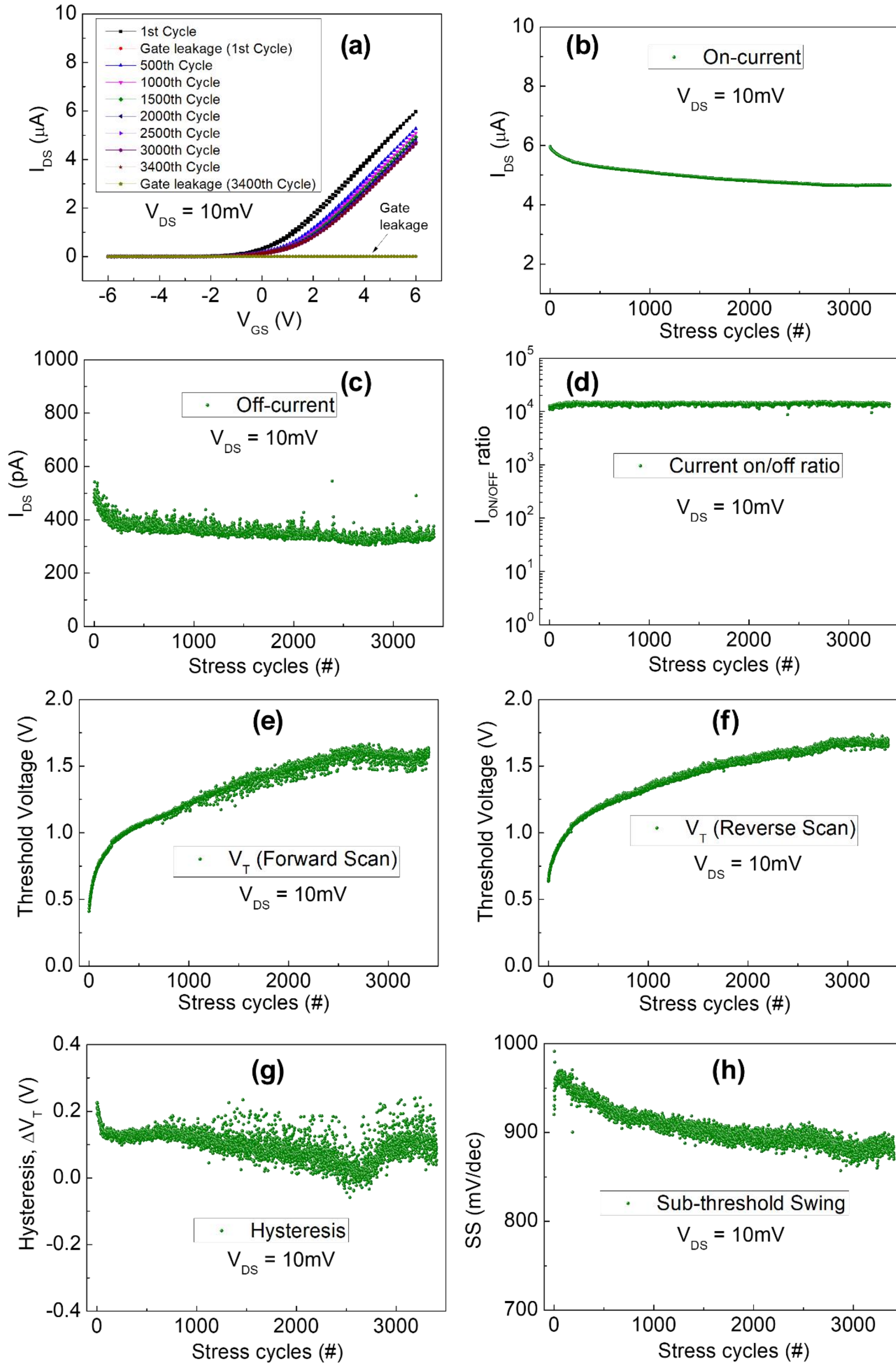


Figure 4.17: Electrical bias stress performance evaluation of n-type NR based transient transistors on Mg substrate. **(a)** continuous transfer scan measurements (~3400 cycles) with V_{DS} = 10 mV up to 24h of operation. **(b-g)** extracted key transistor parameters from the continuous transfer scan to observe the device performance stability: **(b)** on-current, **(c)** off-current, **(d)** current on/off ratio, **(e)** threshold voltage (forward scan), **(f)** threshold voltage (reverse scan), **(g)** hysteresis, and **(h)** sub-threshold swing.

The extracted data reveals that there is small decrease in the device I_{on} (~22%) and I_{off} (~26%) after more than 3000 operational cycles, confirming robust device operation. Because of the almost similar change in the I_{on} and I_{off}, no change is observed in the I_{on}/I_{off} ratio ($>10^4$) for all stress cycles (Figure 4.17d). Next, hysteresis (Figure 4.17g) is calculated based on the difference in V_T value for forward (Figure 4.17e) and reverse (Figure 4.17f) transfer scans. For both forward and reverse scans, small positive V_T shift (~1V) with the stress time is observed. This value compares less with the reported transistors-based metal oxides [187, 214]. Also, the maximum hysteresis noticed for all stress cycles is ~0.25V for the transient transistors. Using the hysteresis data, the transient transistors showed a maximum interface trap charge density of ~1×10^{11} /cm^2 ($\Delta V_T = 0.25$ V, and $C_{ox} = 7\times10^{-4}$ F/m^2). The extracted value of interface trap charge density is an order of magnitude less than the SiO_2—semiconductor interface for nanomaterial-based transistors [182]. Finally, S-S values were extracted and plotted in Figure 4.17. The data shows ~12% change in S-S value after 24h of continuous operation.

Next, gate bias stress studies were performed to understand the interface quality of the transistor. This is critical because poor interface quality could lead to V_T shift and thus, changes in an on-current of the device [187]. The test results are shown in Figure 4.18. To evaluate the effect of both positive gate bias stress (PGBS) and negative gate bias stress (NGBS), transfer scans were performed immediately after PGBS and NGBS (Figure 4.18a). First, transfer scan was performed under no stress condition by sweeping the V_{GS} from -5 to +5 V at a fixed 10 mV drain-source bias. Then, a PGBS was applied for 30 min (1800 s) (Figure 4.18b) and sequentially the transfer characteristic was measured. A shift in the threshold voltage towards negative gate voltages and increase in on-current is clearly visible from the measured transfer scan after PGBS. This could be explained as follows: During the continuous applied gate field in transistors, trapping or de-trapping of the free electrons (or in general charge carrier) could occur from interface and/or bulk defects (depending on the direction of the gate field) [187]. More electrons could be added in the channel through the de-trapping of free electrons, and thus an increase in the I_{DS} may be detected. The enhancement of the device on-current with PGBS could be explained due to de-trapping of

the trapped electrons. The free electrons could be trapped either at shallow energy level or deep energy level trap states at the channel/dielectric interface or bulk of dielectric [215]. The charge-trapping has been explained by two models [187, 214]: (i) the first one is specific to amorphous silicon (a-Si) and arises because of the motion of bonded hydrogen in the a-Si channel during prolonged gate bias stress and creates extra defect sites in the channel, and (ii) the other is common to all materials and is the transfer of mobile charges to immobile trapping states at the semiconductor—insulator interface or at the semiconductor—ambient interface [187, 216, 217]. Monitoring the S-S values could help to identify the dominant mechanism. Generally, S-S remains constant when the electrons are trapped at the shallow energy level trap centers and the device V_T comes back to its initial value after applying gate bias stress in the opposite direction [215, 218]. The S-S of the device remains constant, which hints that the electrons were trapped at shallow energy levels. To confirm this, NGBS was applied for 1800 s (Appendix, figure 8.4) and the transfer characteristic under similar conditions was measured. Interestingly, the V_T of the device comes back to its initial value which confirms the charge trapping at the shallow traps.

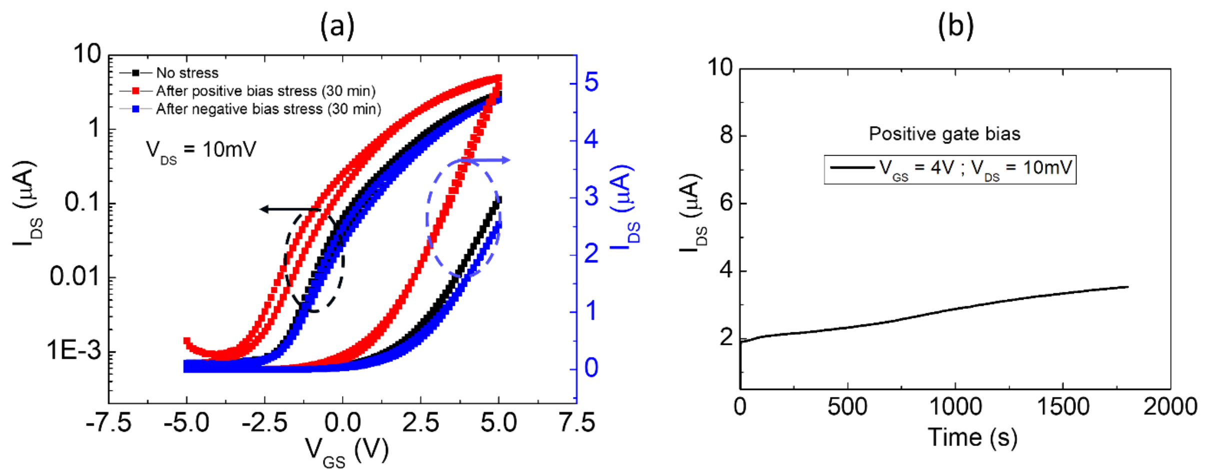


Figure 4.18: Gate bias stress study at V_{DS} = 10 mV: **(a)** transfer scans performed under different conditions (no-stress, after positive gate bias stress and after negative gate bias conditions). **(b)** I_{DS} – time curve during the applied positive gate bias condition.

4.4.3.4 Temperature Dependent Stability Study

The temperature dependent performance variations of transient transistors are analyzed and shown in Figure 4.19. The transfer scans in forward direction (-5 to +5 V_{GS}) were

performed at different temperatures (5 to 50°C with a step of 5°C), as shown in Figure 4.19a. The transconductance (Figure 4.19b) and I_{on} (Figure 4.19c) of the device were extracted from the transfer scans shown in Figure 4.19a. The extracted data shows a decrease in both I_{on} and transconductance values above 30°C and below 15°C. The decrease at higher temperatures (>30°C) is understandable because of the increased scattering events (acoustic phonon assisted and Coulombic) in the channel and/or at the semiconductor/dielectric interface. Thus, at higher temperatures the device performance is limited by scattering events [192]. The hypothesis is further confirmed by analyzing the extracted S-S and V_T values at different temperatures. The variations in S-S and V_T with temperature are shown in Figure 4.19d. This figure reveals that the absolute S-S value increases above 35°C (~0.9 V/dec) and reached to ~1.4 V/dec at 50°C. The S-S of transistors is largely affected by the interface (channel/dielectric) trap charge density. Also, these interface charges lead to shift in threshold voltage of transistors. To correlate the change in S-S trend to interface traps, we have calculated the magnitude shift of V_T with temperature. The V_T data shows a similar trend such as S-S change with temperature. Accordingly, both S-S and V_T change can be correlated to the transfer of mobile charge carriers to immobile trapping states at the semiconductor/insulator interface. The device performance degradation, as shown in figure 4.19(b-c), observed at lower temperatures (<15°C), may be attributed to the influence of ambient conditions during the measurements. Specifically, at lower temperatures, the presence of condensed water molecules can lead to the degradation of charge transport as demonstrated in previous studies [219-221]. However, it is important to note that that this degradation in device performance can be mitigated by conducting the device evaluation under low-temperature conditions within a vacuum ambient environment. Before performing biodegradation studies, last test related to transistor reliability was performed. Transistor performance degradation related to ageing for more than three months were studied (Appendix, figure 8.5) The data shows negligible change in the I_{on} of the transient transistor after 100 days.

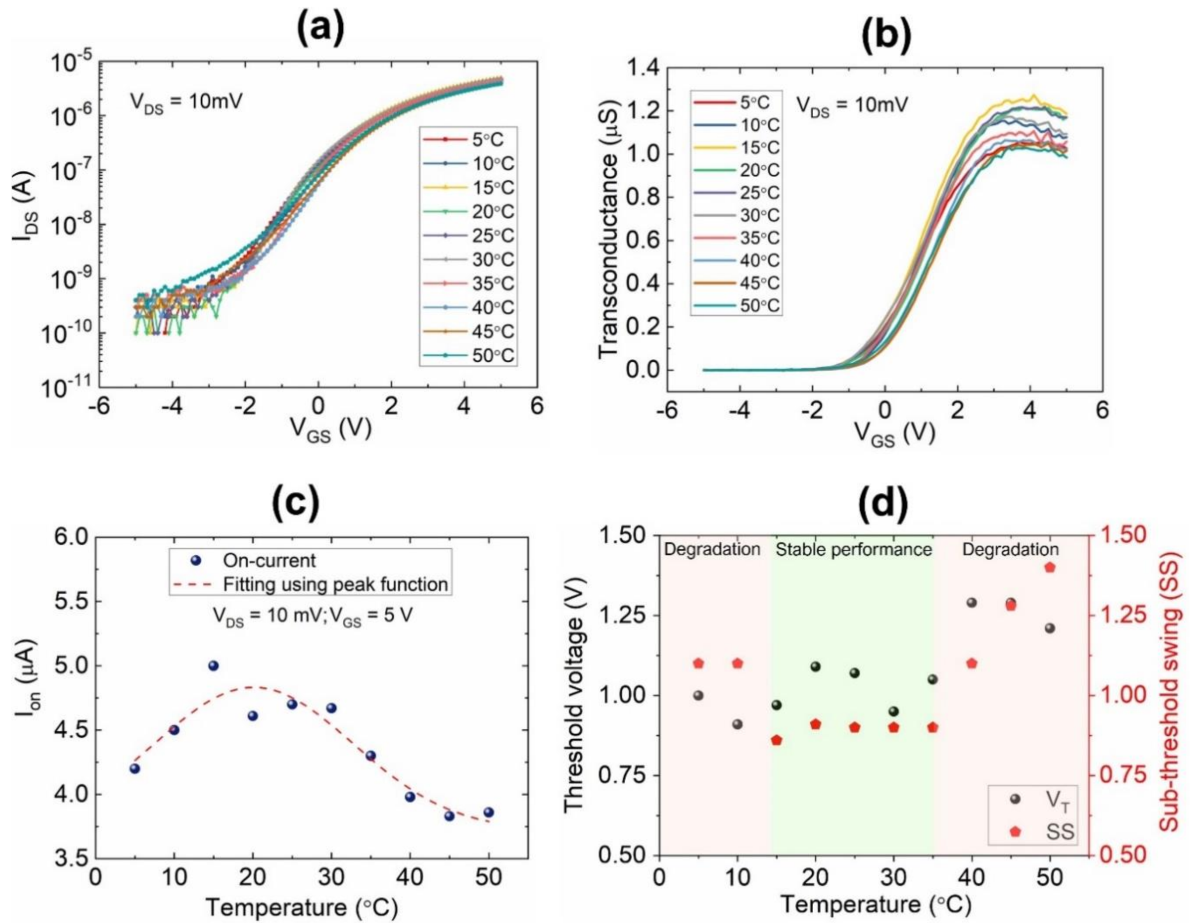


Figure 4.19: Temperature dependent (5-50 °C) electrical characterizations to investigate the stability of n-type transient transistors. **(a)** transfer scans. Important transistors parameters data extracted using temperature dependent transfer scans: **(b)** transconductance, **(c)** on-current and **(d)** S-S and V_T.

4.4.3.5 Transience Study

Previous studies have explored the transience behavior of the biodegradable devices. It is shown that the hydrolysis kinetics of the constituent device materials depends on many factors including pH, temperatures, and the thickness, grain structure, and surface morphology [203, 222]. Here, we have studied the biodegradation behavior of the developed transient transistors in different aqueous solutions with varying pH values but kept at constant temperature (37°C) (Figure 4.20). It is to note that 37 °C is chosen as it represents the body fluid temperature. First, the effect of transience on the electrical performance of transistors is studied by hydrolysis at pH 8 (close to body fluids). For these experiments, the transistor sample was placed inside the aqueous solution and the electrical

measurements were performed at regular intervals after removing it from the solution. Figure 4.20a illustrates the transfer scans of transient transistor at V_{DS} = 10mV performed after different times. Further, the drain current is extracted at V_{GS} = 6V using the transfer scans and plotted in graph shown in Figure 4.20b. The data indicate stable operation for ≈6 h, followed by slow loss of function. To better understand the decrease in transistor on-current, we have collected optical micrographs of the device before performing the electrical measurements (Appendix, figure 8.6). The figure shows that the disintegration process starts ~10h after the sample was placed inside the solution. The partial disintegration of one of the metal electrodes could be the reason for the observed slow transience (due to an increase in the contact resistance). After 55h (3300 min) in the solution, the transistor stopped functionating as the gate metal electrode completely disintegrated from the channel.

The disintegration process and rate of Mg etching is further studied for different pH values 2, 4, 6, 8, and 11. Figure 4.20c presents series of images taken during the transience process by hydrolysis of transistor devices on a Mg foil (≈20 µm). It was observed that first, the transistor layers start to disintegrate (Ti/Au electrodes observed to float in the solution). This is schematically shown in Figure 4.20d. The disintegration starts because of the etching of biodegradable interface layers between the different layers (SiO_2/Mg and SiO_2/metal). It was further noticed that the rate of etching was directly proportional to the pH values. This means that the disintegration step occurred earlier for transistors kept in more basic solution than the ones kept in more acidic. Day 0 images represent the first day of transistor devices placed inside the solution. A distinct disintegration process was noted from the device kept in pH≈11 on day 0. Once disintegrated, further etching of the individual layers continued to occur. The rate of degradation for silicon oxides and nitrides is well known for films deposited using different techniques [193, 208, 222] and is therefore, not monitored. After 13 days, the Mg foil (the rest of the other layers disintegrated) was lifted out of the solution and thickness was monitored using an optical profilometer and SEM to extract the rate of dissolution. The cross-sectional SEM images of the Mg foils kept at different pH values are shown in (Appendix, figure 8.7). The average changes in Mg foil thickness rate in solution

(at 37 °C) are 0.23, 0.27, 0.36, 1.08, and 1.31 μm day^{-1} for devices in pH 2, 4, 6, 8, and 11, respectively (Figure 4.20e).

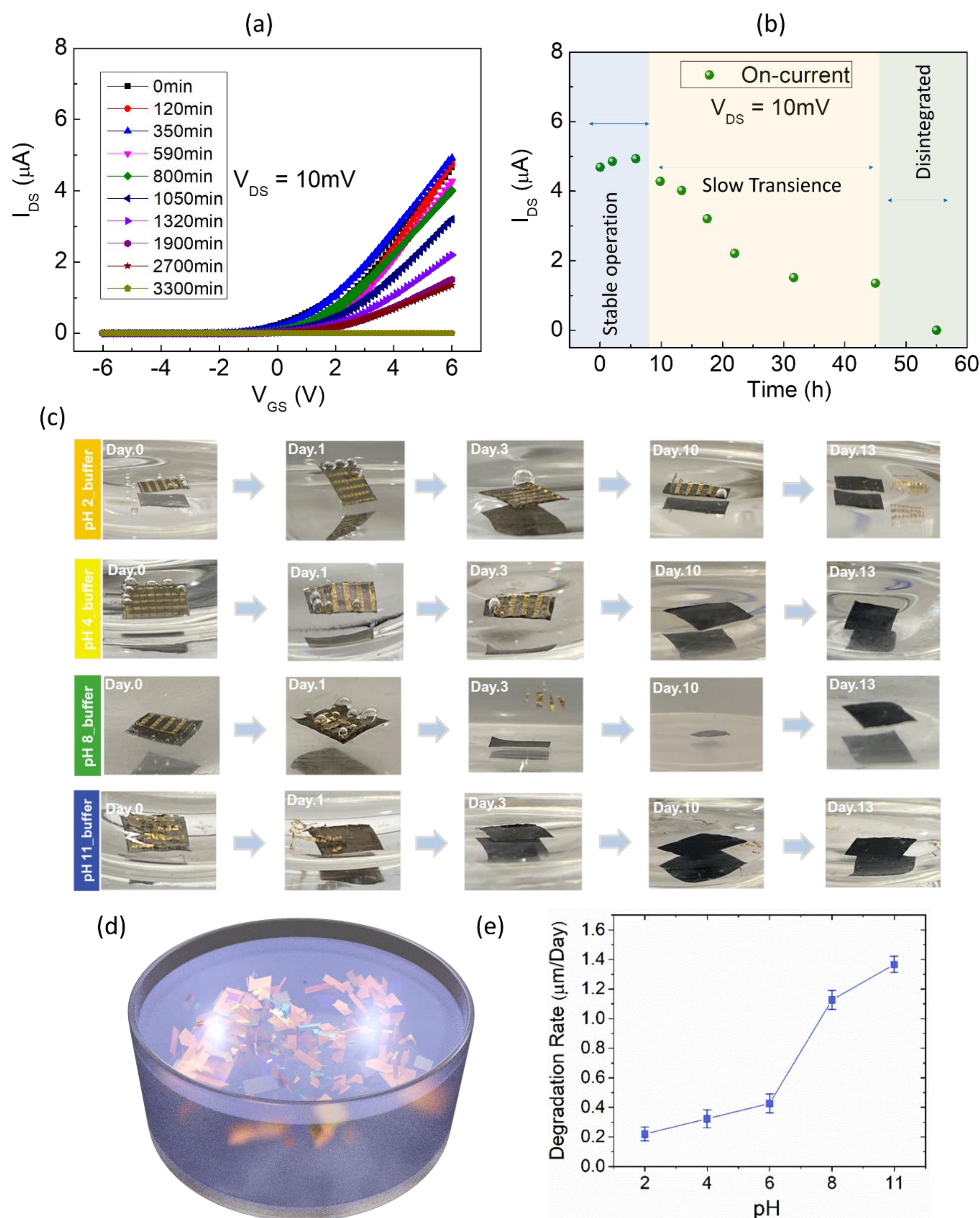


Figure 4.20: Biodegradation studies of the n-channel transistors on biodegradable Mg foils: **(a)** Measured transfer scans at V_{DS} = 10 mV after placing the sample for different times in the aqueous solution of pH 8 and kept at 37°C. Different colored curves indicate responses at different times. **(b)** The drain current extracted at V_{GS} = 6V as a function of time showing various stages of the transient transistor operation namely, stable, slow transience, and loss of functioning. **(c)** sequential images

collected at various stages of dissolution for devices immersed in different pH (pH-2, pH-4, pH-8, and pH-11) at 37 °C. **(d)** schematic representation of the biodegradation, and **(e)** is the rate of biodegradation of Mg foil.

This clearly shows the etching rate of the Mg foil is more in solution of higher basicity. At this rate, the complete dissolution of the Mg foil would occur after ~87, ~74, ~55.5, ~18.5, and ~15 days for transistor in pH 2, 4, 6, 8, and 11, respectively. It is important to note that the presented transient transistors also comprise of some non-biodegradable layers i.e., metal contacts (Ti/Au), and a semi-cured PI. Although the metals are non-biodegradable, but hydrometallurgical treatments could be used to extract most of the disintegrated metals including gold [223, 224]. For instance, it has been shown that by using environmentally friendly lixiviants such as thiosulfate during the hydrometallurgical treatment, almost 95% of the Au could be recovered [223]. The recovered Au can be recycled to enhance the circularity in electronics. Thus, circular electronics connects the recycling and degradable approaches. Accordingly, in the near to mid-term, transient electronics could be explored to complement the current recycle and reuse approach[1g]. Nevertheless, by exploring biodegradable metals such as Mg, Fe etc. and biodegradable adhesive layer such as MICA MC-634 and spin-on glass, direct transfer printing has the potential for the fabrication of high-performance transient integrated circuits and thus, eventually replace the present recycle and reuse approach.

4.5 Conclusions

In this chapter, we have presented an effective route for developing high-performance flexible transistors for next-generation electronic applications. The developed approach involved the direct roll printing technique (DRTP) to transfer and integrate nanostructures such as silicon nanoribbons (Si NRs) directly onto flexible PI substrates, without the use of elastomeric transfer stamps. This innovative printing method demonstrated a high transfer yield of ~95% with perfect registration, which led to the fabrication of high-performance n-type and p-type channel flexible FETs for flexible CMOS circuitry. The fabricated transistors showed excellent performance with high device mobility, and current on/off ratio

at par with devices reported previously using traditional transfer printing processes. The n-type Si NRFET showed a high mobility of >630 $cm^2/V.s$ and a current on/off ratio of ~10^6, while the p-type transistors showed a high device mobility of ~100 $cm^2/V.s$ and a current on/off ratio of >10^4. Furthermore, the n-type NRFETs retained their excellent electrical characteristics after 100 cycles of bending tests, making them an excellent candidate for high-performance flexible CMOS electronics for next-generation LAE. However, the cyclic bending measurement was conducted after every 10 cycles, with a total of 100 cycles performed. The choice of 100 cycles was made to evaluate the device's stability, and it is a common practice for evaluating flexible and printed electronics utilizing inorganic and/or organic semiconductor materials [225-227]. However, for future work, it is suggested that the number of cycles be increased to further evaluate the device's stability and explore the maximum bending cycles that the device can withstand while maintaining its functionality. This will enable a more comprehensive understanding of the device's long-term performance under cyclic bending and electrical stressing conditions and provide valuable insights for potential practical applications. Furthermore, there is still room for improvements in the performance reproducibility of the devices, such as the uniform and controlled doping of the donor substrate. The doping step in this work is performed using the SOD approach under ambient pressure, which is not an ideal approach and could bring non-uniformity in the devices. Despite this, the device endurance evaluations have been carried out, and we have shown the high device robustness to mechanical bending and at wide temperature range. Finally, analyzing the temperature dependent transfer scans, we have shown the role played by interface traps towards degrading the on-current of the device. Furthermore, we have developed high-performance n-channel transient transistors on biodegradable metal magnesium foils. We employed direct transfer/stamp printing to transfer high-quality and biodegradable electronic layers (Si nanoribbons) on Mg foils, which demonstrated high performance, including high effective mobility (>600 $cm^2/V.s$), high on/off current ratio (Ion/off) of >10^4, negligible hysteresis, and an on-current of 1.6 mA at a bias of 2 V. The transient device performance was compared with similar devices on flexible PI substrates, confirming the robustness and substrate independency of the developed fabrication process.

Furthermore, we confirmed stable and reliable transistor operation in ambient conditions using a series of systematic tests, including continuous transfer scans, gate bias and temperature stress, and ageing studies for more than three months. The transient transistors were also able to operate at very low V_{DS} of 10 mV, demonstrating their high electron mobility and high ohmicity of the metal-semiconductor contact. The developed transistor constituents/layers are mostly, but completely biodegradable. That leads to opens new avenues for commercial electronics with reduced e-wastage, sustainable environment/soil monitoring, and implantable biomedical devices. This is demonstrated by transience studies performed in aqueous solutions at different pH values at 37 °C, where the loss of transistor function was observed after 55h for devices placed inside the solution of pH 8 as shown in Fig. 4.20b. Additionally, the study showed that the device at higher pH (higher basicity) disintegrated and degraded at a faster rate as shown figure 4.20c-e and appendix figure 8.6). In future work, the exploration of alternative metals such as zinc (Zn), tungsten (W), iron (Fe), and molybdenum (Mo) is proposed for use in the fabrication of printed transistors on biodegradable substrates, considering their biocompatibility [204]. The investigation of these alternative metal contacts can further enhance the development of fully biodegradable high-performance n-channel printed transistors for transient electronics applications. This technology offers a promising direction for the development of sustainable electronics and implantable devices with reduced environmental impact. To summarise, the n and p-channel NRFETs fabricated using the direct roll printing technique hold great promise in realizing high-performance large-area flexible CMOS circuits. The presented integration method is a promising direction for future research in the field of high-performance flexible electronics. Additionally, the demonstrated success of the DRTP approach suggests its potential applicability for printing ultrathin micro/nano structures using other high-mobility materials such as SiC, GaAs, GaN, etc. These findings not only offer new possibilities for flexible electronics but also have the potential to contribute to the development of advanced electronic devices.

Author Contributions:

In this chapter, the conceptualization of the overall work was done by me and Dahiya, R. The experiments and fabrication tasks were carried out and led by me. The Automated experimental setup for direct roll transfer printing (DRTP) process was built, developed and led by Christou, A. The transfer printing experiments were carried out and led by me, with valuable assistant from Christou, A. The finite element analysis (FEA) simulations using COMSOL Multiphysics simulation software was carried and led by Christou, A. The device characterisation was carried out by me with support from Dahiya, A.S. The work related to "High-Performance n-Channel Printed Transistors on Biodegradable Substrate for Transient Electronics" was the result of equal contribution of Dahiya, A.S. and myself as first authors in the corresponding publication. All authors mentioned in this chapter contributed to the work through regular discussions. Dahiya, R. provided overall supervision for the project

Chapter 5.

Printed GaAs Wires-Based Flexible High-performance Broadband Photodetectors

The work Adapted from:

Journal Articles

Zumeit, A., Dahiya, A.S., Christou, and Dahiya, R. Printed GaAs Microstructures-Based Flexible High Performance Broadband Photodetectors. (2022). Adv. Mater. Technol. DOI: 10.1002/admt.202200772

Abstract:

In the previous chapter, a novel R2R compatible direct roll transfer printing (DRTP) method to integrate inorganic nanomaterials was presented. We demonstrated the effectiveness of this approach by transferring Si nanoribbons and fabricating high-performance transistors on flexible substrates. Other nano/microstructures of compound semiconductors such as gallium arsenide (GaAs) have also shown enormous potential for advanced photonic technologies as they provide realistic means for miniaturization of optoelectronic devices that feature better performance and low power consumption. However, intimately integrating them onto flexible substrates is challenging and restricts their use in the next generation of applications such as wearables and soft robotics. In this chapter, DRTP approach will be used to print arrays of well-defined and laterally aligned semi-insulating (undoped) and doped GaAs microstructures to develop high-performance flexible broadband photodetectors. To achieve this, first, high quality GaAs microstructures will be fabricated using top-down approach. Then, DRTP method will be optimised to

transfer high yield of GaAs structures over flexible substrates and photodetector devices will be fabricated using conventional microfabrication. The direct roll transfer printed GaAs microstructures-based photodetectors exhibit excellent performance under ultraviolet and near-infrared illumination, including ultrafast response (2.5 ms) and recovery (8 ms) times, high responsivity (>10^4 AW^{-1}), detectivity (>10^{14} Jones), external quantum efficiency (>10^6), and photoconductive gain (>10^4) at low operating voltage of 1 V. The achieved performance is among the best reported for broadband photodetectors but with an added benefit of the developed devices having a flexible form factor. Further, the photodetectors show stable performance under mechanical bending (500 cycles) and twisting loading. The developed materials and manufacturing route can enable high-speed communications and computation via high-performance flexible electronics and optoelectronics and transform numerous emerging applications such as wearable systems and internet of things (IoT).

5.1 Introduction

High-speed, efficient and low-power flexible electronic devices such as photodetectors [50, 76, 228], transistors [52, 229, 230], etc. are needed in numerous applications including medical diagnostics [230-232], high speed communication [233-235], environmental monitoring [236, 237], wearable and neuromorphic computing [22, 23, 238, 239], etc. This will also have an impact on the IoT where smart objects are wirelessly connected to interact with the environment and the human body [21, 240]. The high-performing electronic devices made of compliant materials can add new capabilities in terms of high-speed communications, efficient image sensing and so on [70, 235, 241-244]. For example, the transmission rate, the transmission capacity, and the efficiency of wireless communication could significantly enhance if a single photodetector (PD) device could operate under wide spectra with low power consumption and latency. Furthermore, the demands for wide spectral switches [245], or memory storage [246], could be satisfied from the single PD. However, the studies so far have primarily focused on the development and characterization of high-performance flexible PDs under certain wavelength (i.e., UV [76, 246, 247] or visible

[24, 248], or NIR [249] spectrum). Recently there have been few attempts to develop ultrafast and conformable broadband PDs [242, 250-252]. Among these, the heterostructures based on two-dimensional (2D) materials and perovskites have shown potential to expand the working wavelength of PDs [250-252]. This is owing to their direct bandgap and large absorption coefficient [253, 254]. Specifically, perovskites have garnered more interest for optoelectronic applications as they are solution processable, and their fabrication cost is low. However, due to low mobility (~1-10 cm^2/Vs) [255], and poor stability [256] their performance metrics (e.g., responsivity (R), specific detectivity (D*), and so on) for PDs are modest. The poor stability in ambient conditions is attributed to the adsorption of water and oxygen molecules which greatly accelerate the degradation of the perovskite photosensitive layer [253]. Efforts are on-going to enhance the stability of perovskite-based devices exploring different encapsulations, but low intrinsic mobilities will still be a challenge. Thus, the efforts to develop the next generation of flexible and high-performing PDs, with wide spectral sensitivity and robust fabrication route, are still on.

In above context, the nanostructures and thin films of inorganic compound semiconductors such as Gallium Arsenide (GaAs) have shown considerable potential for optoelectronic devices owing to their direct bandgaps (1.42 eV), high intrinsic electron mobilities (≈8500 cm^2/Vs), chemical and thermal stability, and flexibility [70, 75, 241, 242]. Particularly, because of the large surface to volume ratio, the compound semiconductors based 1D nanostructures have many surface trap states which enhance the photocarrier lifetime. Simultaneously, the low dimensionality of nano/microscale devices helps in the miniaturization, and limits the effective sensing area, which results in a large R, and photoconductive gain (G) etc. [243]. This is evident from several examples related to efficient photovoltaic devices, ultrafast optical switches, high-performance UV and NIR PDs, etc. - most of which have been developed over rigid substrates and/or using single nanostructure [241, 242, 257, 258], as it is challenging to integrate compound semiconductors-based nanostructures on flexible substrates. To this end, transfer printing technique, which allows deterministic assembly of laterally aligned photolithography-defined arrays of 1D nanostructures over plastic substrates [48, 58, 259], has shown potential.

Transfer printing and/or modified transfer printing approaches have been used to demonstrate various high-performance devices on flexible substrates, including both *n*- and *p*-channel transistors [52, 57], photovoltaic and optoelectronic devices, etc. [47, 49, 70].

In this work, DRTP approach is used to integrate the arrays of well-defined and laterally aligned GaAs microstructures for high-performance flexible broadband PDs. In our previous works, DRTP was employed to transfer silicon nanoribbons from silicon on insulator (SOI) wafer to flexible substrates [52, 57]. In this work, we have demonstrated for the first the use of direct roll printing to obtain GaAs microstructure arrays on flexible substrates. To achieve high transfer yield, we optimised the process for developing GaAs microstructures and also tuned the printing parameters. The arrays of GaAs microstructures were obtained using top-down fabrication approach, which includes the use of bulk wafer-based source materials, photolithography, and chemical etching procedures [42, 56]. The top-down synthesis route to realise nano/microstructures is attractive owing to better uniformity control with excellent alignment and registration accuracy as compared with the bottom-up synthesis [54]. These attributes are needed to have uniform and repeatable device performance over large areas. The next step involves transferring these well-defined nano/microstructures from the source substrates (bulk wafer) to a device substrate (flexible polyimide (PI)). To this end, we have selected DRTP as it is a single step printing method, which does not require viscoelastic polymeric stamps (typical of conventional transfer printing) to obtain nano to macro scale structures over the donor substrate. The donor substrates with GaAs microstructures is directly brought into physical contact with the semi-cured thin polyimide (PI) film over the receiver substrate [52, 57]. Because of the strong adhesion between the fabricated microstructures and the receiver substrates (due to the semi-cured nature of PI layer) high transfer yield is achieved (≈95%). The process is compatible with roll-to-roll (R2R) fabrication, which is advantageous in terms of high throughput and large-scale electronics manufacturing. Lastly, it is worth noting that the adopted printing route can help in reduce the fabrication cost because the donor substrate (bulk GaAs wafer) can be reused multiple times after the transfer of GaAs microstructures to the receiver substrate. Following the direct roll printing step, the high-performance

metal-semiconductor-metal (MSM) back-to-back Schottky contact-based PDs were realized using conventional microfabrication process. The sensing performance of the semi-insulating undoped (Resistivity at RT, $>10^7$ Ω.cm) GaAs microstructures-based PDs was systematically evaluated in ambient conditions. Under UV (365 nm), and NIR (850 nm) light conditions they showed high R ($>10^4$ A/W), D* ($\sim10^{15}$ jones), photoconductive gain, G ($>10^4$) and external quantum efficiency, EQE (10^6%), and high dark to light current on/off ratio values ($>10^2$). Furthermore, the optimized fabrication steps were used to realize doped GaAs microstructures (carrier concentration 2.7×10^{18} cm^{-3}) based low-powered PDs (operating voltage = 1V). These PDs showed better performance (except for current on/off ratio values) as compared with undoped microstructures-based devices (characterized under similar conditions). The PDs based on both doped and undoped GaAs microstructures showed ultrafast response/recovery (2.5/8 ms) times. Finally, the PDs were evaluated under mechanical bending and twisting conditions for up to 500 cycles and they showed robust device performance. This shows that the developed material and fabrication scheme holds considerable potential for large-area flexible and high-performance optoelectronic sensors/circuitry based ultrafast optical communication.

5.2 Methods

5.2.1 Fabrication of GaAs array of microstructures

Top-down fabrication process was employed to realise well-defined arrays of GaAs microstructures. The fabrication process involved patterning of 650 µm thick bulk undoped and Si-doped GaAs wafer (5×10^{18} cm^{-3}) from Wafer Tech. A SiO_2 mask layer (thickness ~250 nm) was deposited on the top of the wafer surface via plasma-enhanced chemical vapor deposition (PECVD). To define the patterns of the GaAs microstructure arrays using typical photolithography steps, a layer of photoresist (PR; S1805) was spin-cast (4000 rpm, 30 s) on top of the deposited PECVD SiO_2 on (100) GaAs bulk wafer. This was followed by soft baking at 115°C for 1min. A UV light exposure was carried out (MA/BA6 mask aligner from Suss MicroTec) through a photomask with desired patterned lines (length of 40µm and width of 5µm) aligned in parallel to the (011) orientation of GaAs wafer. The exposed

wafer was developed in MF-319 developer for 75s. The wafer was baked in 120°C for 20 min in an oven followed by oxygen O_2 plasma treatment at 150 W RF power for 30s. The SiO_2 was patterned using photolithography and Reactive Ion Etching (RIE) system (40 sccm CH_3/Ar flow with a chamber base pressure of 30 mTorr, 200 W RF power for 5 mins). Then, the photoresist mask was dissolved using acetone and isopropanol (IPA) with ultrasonic agitation, followed by abundant rinsing with de-ionized (DI) water and dried using nitrogen air. These steps lead to the formation of SiO_2 mask patterns on the GaAs bulk wafer (as shown in Figure 5.1). These photolithographically patterned lines of SiO_2 were used as mask for subsequent wet etching step. The chemical etching solution for GaAs was prepared by mixing of H_3PO_4 (85 wt.%): H_2O_2 (30 wt.%): H_2O = 1:13:12 by volume and kept at 40°C [56]. Subsequently, the anisotropic etching was carried out by dipping GaAs samples with SiO_2 patterns in the etchant solution to form the GaAs microstructure arrays (the optimization of anisotropic etching process with respect to etching time and methodology characterisation are demonstrated in Figure 5.1. Then, the deposited SiO_2 mask was etched using diluted HF solution. The samples with released microstructure arrays on the donor wafer were rinsed with ethanol, DI water and dried in the fume hood respectively and prepared for DRTP on flexible substrate.

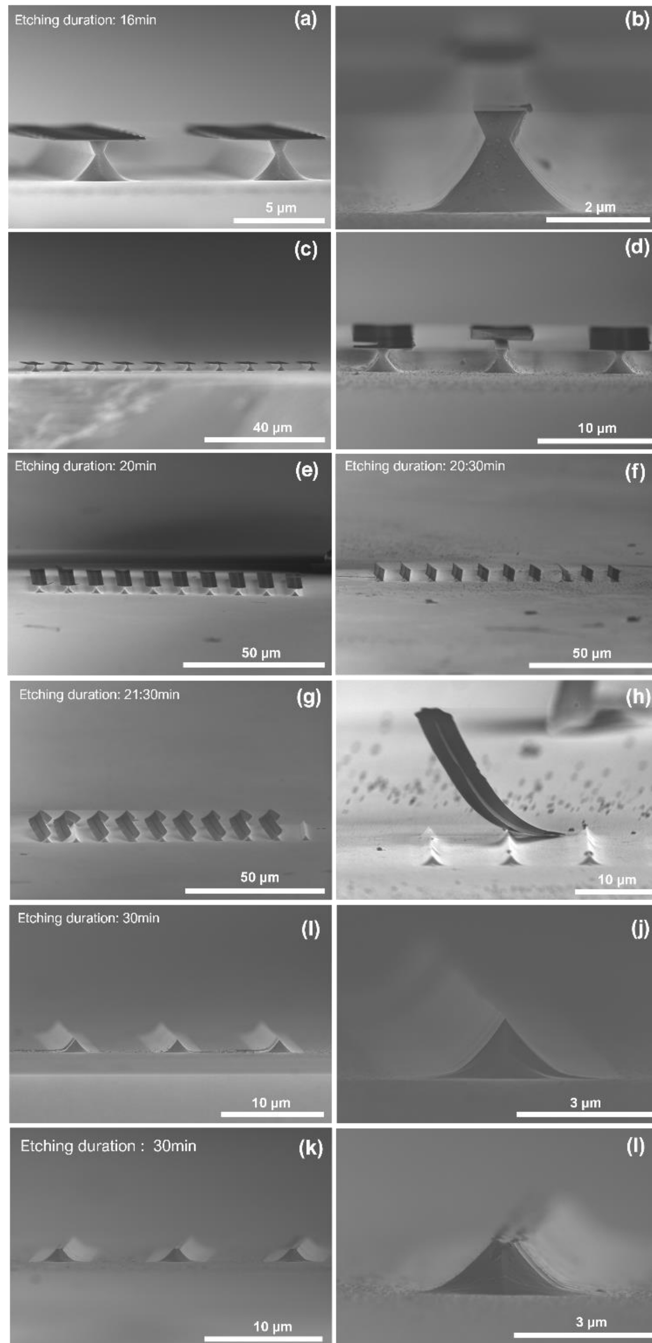


Figure 5.1: The corresponding SEM images of GaAs microstructures obtained during the optimisation process under different stages of anisotropic chemical etching of the bulk wafer with etching rate: 35nm/min.

5.2.2 Printing GaAs wires by DRTP

The developed direct roll transfer printing (DRTP) system [52] was used to transfer and integrate well-defined arrays of GaAs microstructures from bulk wafer. As mentioned in the previous work (see section 4.2.1), It is a single step process. For a successful DRTP with high yield and high registration, an adhesion promoter of ~1.0 µm (PI-2545 precursor from

HDmicrosystems) was applied on commercial PI substrate. The spin coated PI was semi-cured by heating at 70°C for 4 min. Subsequently, GaAs wafer with microstructures was brought into direct physical contact with the semi-cured PI receiver substrate. The applied force during roll transfer stamping is 10N, and roll speed is 0.1mm/s. After NR transfer, the PI substrate is subsequently cured at 250°C for 2 hours.

5.2.3 Flexible photodetectors Fabrication

The fabrication process for the presented PDs is schematically shown in Figure 5.2 The top-down fabrication approach forms the well-defined periodic arrays of single-crystal GaAs microstructures. Figure 5.2a-d schematically show the fabrication steps for array of GaAs microstructures, which includes photolithography and anisotropic wet chemical etching steps. As a first step, a thin (~250nm) layer of plasma enhanced chemical vapor deposition (PECVD) assisted SiO_2 was deposited on a bulk GaAs source wafer (Figure 5.2b). Then, photolithography and dry etching steps were performed to define the geometries of the microstructures (Figure 5.2c). Next, the critical anisotropic chemical etching step was carried out. This step was cautiously optimised to have higher transfer yield (discussed later) during the DRTP step (Figure 5.2d-e). Etching and release of GaAs microstructures by DRTP method onto a target flexible substrate represents one conceivable route to device integration. The employed roll transfer printing assembly steps, described elsewhere [52] were followed for bringing the laterally aligned photolithography-defined arrays of inorganic semiconducting nanostructures on donor wafer in conformal contact with the target substrate (Figure 5.2f). Before printing, the target substrate was coated with a semi-cured polyimide (PI) layer to enhance the adhesion between the printed structures and the target flexible substrate. This simple, yet innovative, single step process leads to a higher printing yield and registration accuracy without the need for complicated pick and place equipment. The printing approach, with yields (>95%), excellent registration accuracy (<100 nm) and throughputs is needed for large area electronics with high device-to-device uniformity. Finally, the PDs were fabricated from the printed GaAs microstructures arrays by following conventional microfabrication steps including photolithography and lift-off (Figure 5.2g).

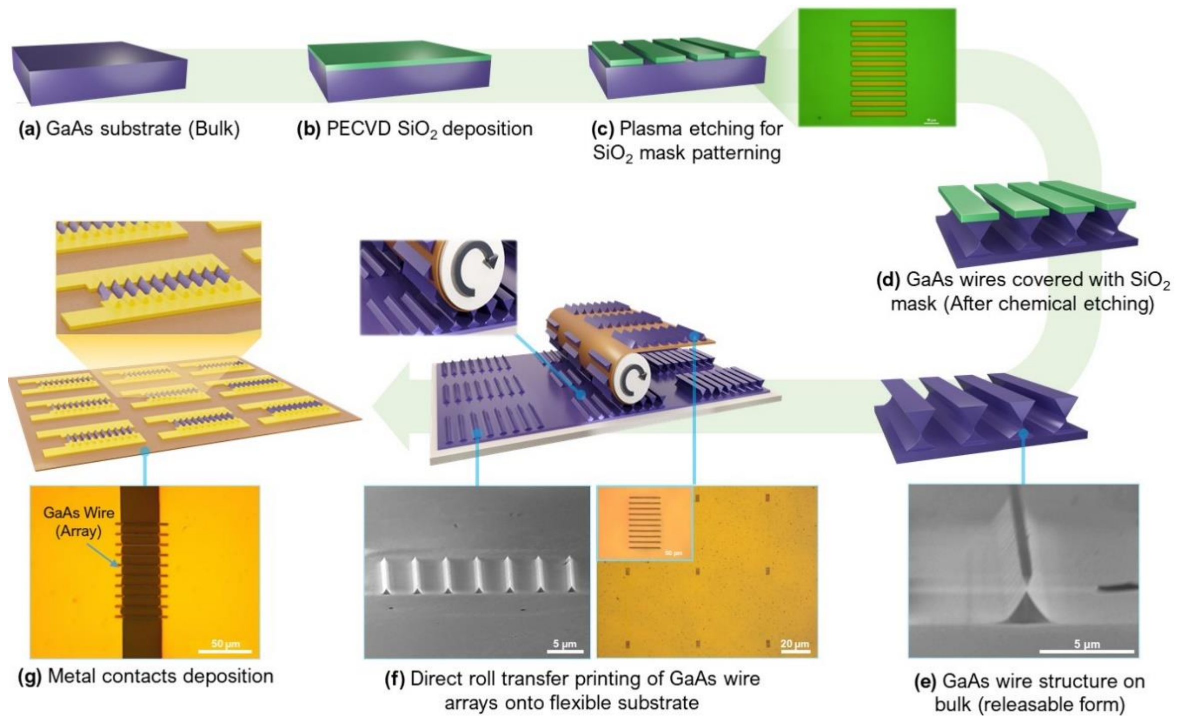
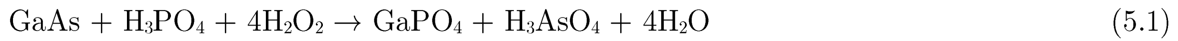


Figure 5.2: Schematic illustration of GaAs microstructures-based PD fabrication process and related optical and SEM images: **(a)** bulk (100) oriented GaAs source wafer; **(b)** PECVD assisted SiO_2 deposition on GaAs bulk wafer; **(c)** using patterned SiO_2 as an etch mask with 40 µm length and 5 µm width; **(d)** anisotropic chemical etching step to form GaAs microstructures; **(e)** SEM image showing formation of GaAs microstructures after wet etching step; **(f)** an illustration of DRTP of GaAs microstructures. The figure also shows an optical image of arrays of printed GaAs microstructures onto the target PI substrates and the SEM image of the donor substrate after transfer process. **(g)** fabricated PDs with metal deposited using conventional microfabrication steps.

The fabrication process for GaAs microstructures includes mask layer deposition (SiO_2), conventional lithography steps, dry (plasma) etching to define the mask geometries and wet etching. The wet etching is a critical step as it determines the final yield of the printing process. Figure 5.3 shows the schematic and SEM images of GaAs microstructures during various stages of chemical etching. The SiO_2 pattern had width of 5 µm and thickness of 150 nm which served as an etching mask during the anisotropic chemical etching of GaAs. The first frame (Figure 5.3a) shows a strip of the SiO_2 patterned along the $(0\bar{1}\bar{1})$ crystalline direction on the GaAs (100) bulk source wafer. The second frame (Figure 5.3b) shows profiles after the start of the wet etching in a phosphoric acid and hydrogen peroxide solution according to the following equation:[56]



$$GaAs + H_3PO_4 + 4H_2O_2 \rightarrow GaPO_4 + H_3AsO_4 + 4H_2O \quad (5.1)$$

The etchant solution for GaAs is made of H_3PO_4 (85 wt.%): H_2O_2 (30 wt.%): H_2O = 1:13:12 by volume and kept at 40°C. The anisotropic etching of the bulk GaAs using such a solution of acid mixtures is well reported[42, 56, 62]. Structures with variety of morphologies such as reverse mesa, nanowires, etc. can be realised using this etching technique.

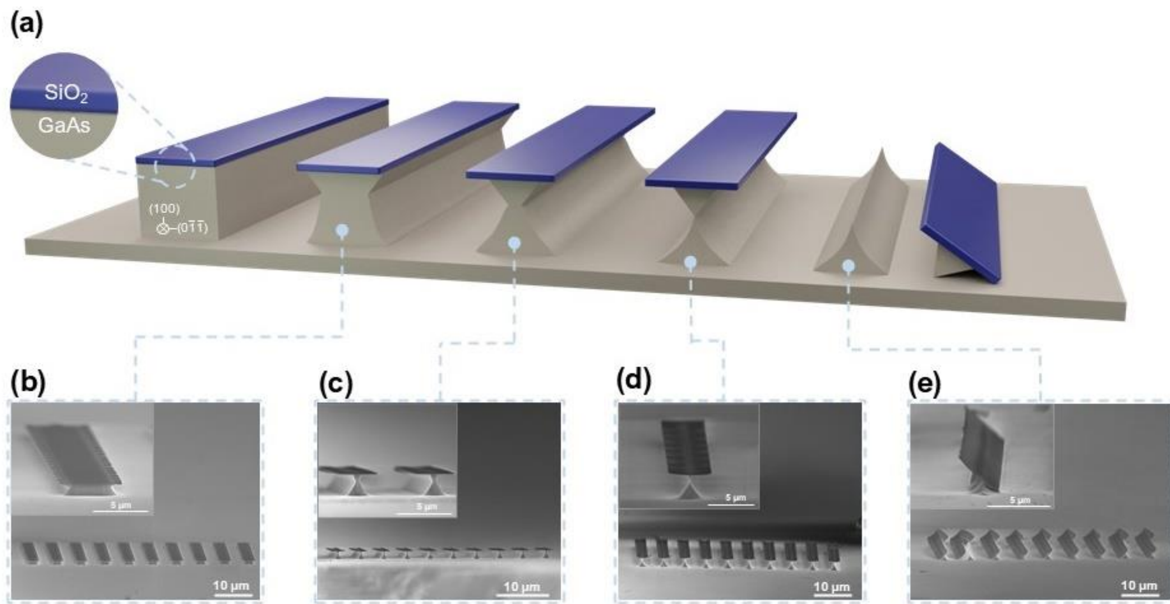


Figure 5.3: Schematic description and SEM images from various stages of development of GaAs microstructures from single crystalline GaAs bulk wafer using anisotropic chemical etching: **(a)** schematic representation of the process; **(b)** SEM image showing the profile of microstructures after start of the wet etching (7 mins); **(c)** after 16 min; **(d)** SEM image of an optimised GaAs microstructure array after 20 mins and **(e)** SEM image of the collapsed GaAs microstructures after prolonged reaction time (20:30 mins).

Generally, over etching of the GaAs bulk wafer could lead to nanowires realised in the etching solution. In the present case, we do not want the fabricated microstructures to be released into the solution. Instead, we need rather weakly anchored microstructures on the donor substrate so that they can be transferred using direct roll printing. Therefore, the printable GaAs structures were optimised to be weakly attached at the anchor point by carefully monitoring the etching rate of the GaAs. Briefly, the process includes, first, the oxidation of GaAs and subsequent dissolution of the oxide product. Prolonged reaction times yielded sharply defined micro/nanostructures under the mask stripes (SiO_2 in the

present case), as shown in the Figure 5.3c. Based on the obtained results, the etching rate was extracted to be ≈ 35nm/min. It was noted that if the wafer was left for higher etching times, the two side walls of each reverse-mesa structures will intersect, which then results in the collapse of the GaAs microstructures (Figure 5.3e) or release of microstructures in the solution. Therefore, the etching time was carefully optimised to obtain reverse-mesa sides close enough to enable efficient release of the nanostructures during direct roll transfer printing (optimisation studies using Finite Element Analysis are the following section). Figure 5.3d shows the SEM image of an array of GaAs microstructures obtained using the 5 × 50 µm SiO_2 mask strips and subsequent anisotropic chemical etching. Prior to DRTP of GaAs microstructures, the oxide mask on top of GaAs microstructure arrays was etched away with a short dip in diluted HF solution.

Next, the large area transfer of as-patterned GaAs microstructures array onto PI substrates was attained using DRTP. As mentioned earlier, the etching of the two sides of the reverse-mesa structures was carried out carefully to facilitate easy release of the microstructures from the donor substrate. This is important for the efficient, and successful transfer printing of large arrays of GaAs microstructures down to nanometre scale. In this regard, we also performed Finite Element Analysis (FEA) simulation studies to optimize the printing conditions such as force, rotation speed etc. for different width of the microstructures (Figure 5.4).

5.2.4 Finite element analysis (FEA) simulations

FEA simulations were carried out using COMSOL Multiphysics simulation software. A 2-dimensional linear elastic model of a single microstructure was implemented (Figure 5.4a) The base of the bottom mesa structure was assumed to be fixed and a normal force was applied uniformly on the top surface of the microstructure.

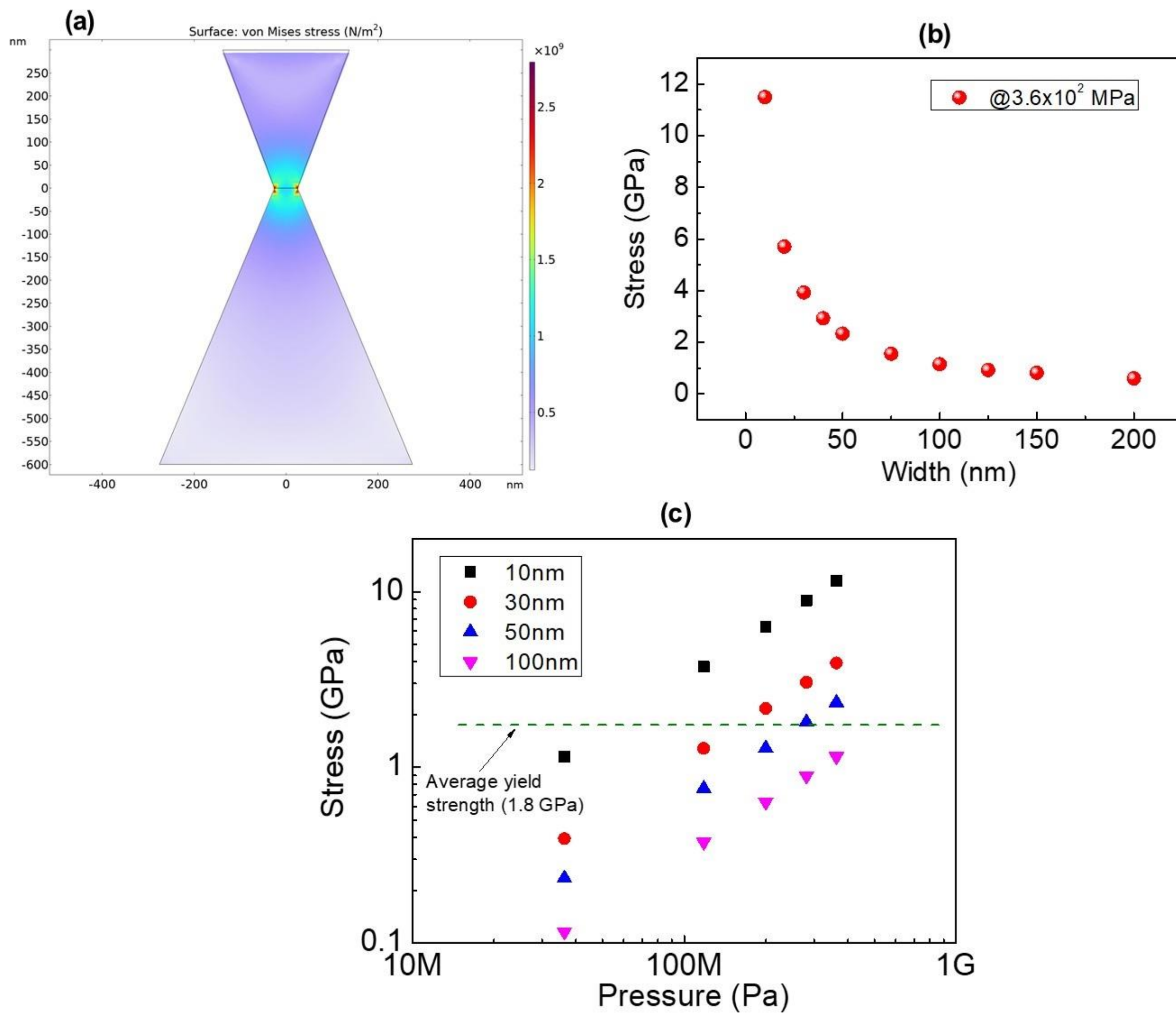


Figure 5.4: Finite Element Analysis studies to optimise the transfer efficiency of direct roll transfer printing: **(a)** 3D representation of the reverse mesa GaAs microstructures used for the simulations, **(b)** stress as a function of GaAs microstructure width at constant compressive force (10N) applied on top of the structures, and **(c)** the fixed width of microstructures, we studied the minimum force required to develop strain equivalent to reach the brittle fractures.

Our recent work on DRTP showed that the applied force plays a significant role in defining the transfer yield [52]. It was shown that a 10N force is needed to bring the suspended silicon nanostructures in conformal contact with the target semi-cured PI layers to have a high transfer yield (>95%). However, in the previous study, printing parameters were optimised to transfer suspended Si nanoribbons (NRs) anchored at the two ends with the bulk Si. Differently form that, in the present case, the GaAs microstructures are anchored with the bulk wafer, all along their length, as shown in Figure 5.3 c-d. In the present case, along with the force, the width (anchor side) of the microstructures also plays a critical role

in defining the transfer yield. For this, first, we applied a constant compressive force (10N) on top of the microstructure and stress distribution as well as yield strength was monitored in Figure 5.4 a-b). The maximum stress was observed at the anchor point between microstructures and bulk of the substrate. Previous studies have shown that the yield point/strength for vertically aligned top-down fabricated GaAs micropillars is around 1.8 GPa [260]. Above this the pillars develop fractures. Accordingly, we set this as our threshold limit above which the anchor point could be broken, and microstructures can be transferred over the PI substrate. The Figure 5.4b shows that the width of microstructures should be ≤ 75nm for a 10N of force applied over 1 cm^2 area. Further, for the fixed width of microstructures, we studied the minimum force required to develop strain equivalent to reach the brittle fractures (Figure 5.4(c)). According to these simulations and SEM images (displaying width of ~50 nm), we applied a 10N force using our custom-built roll system (see section 5.2.4) to attain conformal contact of microstructures with the semi-cured PI and to have sufficient applied pressure to reach fracture limit of the anchors. The optimised transfer parameters were used to print GaAs microstructure arrays on to flexible PI with good retention of the orientation and relative position of individual microstructures with respect to each other. Strong bonding between the semi-cured PI layer and the GaAs microstructures resulted in their breakage or release from the bulk donor.

5.2.5 Fabrication of photodetectors

The GaAs microstructures printed on polyimide (PI) substrates using the direct roll transfer printing (DRTP) method were used to fabricate metal-semiconductor-metal (MSM) microstructure-based photodiodes (PDs). The metal contacts on the printed GaAs microstructure arrays were formed using typical photolithography and lift-off procedures. Schottky contacts were formed on transfer-printed undoped and n-type Si-doped GaAs wires using sequential electron beam evaporation of (Pd(35)/Ge(65)/Au(200nm)) and AuGe(14)/Ni(11)/Au(240nm) [261]. The fabricated devices were annealed in a horizontal tube furnace under Ar ambient at 150°C for 15 minutes.

5.2.6 Electro-optical characterisation

The electrical characterization of the fabricated GaAs microstructures based flexible PDs such as time resolved photo response etc. were performed in the ambient environment using semiautomated summit 12k Auto prober and semiconductor device parameter analyzer (B1500A, Agilent). A UV light emitting diode (LED) with the wavelength of 365nm and a NIR LED (850nm) was used for evaluating photodetection capabilities of the fabricated devices, the corresponding electro-optical characterisation results of printed GaAs wires-based photodetectors are presented in the following sections (see section: 5.3.1).

5.2.7 Mechanical endurance studies

The mechanical endurance studies included testing under bending and torsional loading conditions, the obtained results are presented in section 5.2.7. These were conducted using a desktop endurance test machine for bending tests (Yuasa System DMLHP-P150) and torsion tests (Yuasa System DMLHP-TW). The devices were attached onto a flexible carrier substrate (polypropylene) to facilitate loading on the testing machines. The testing machines can repeatably apply bending/torsional loading while controlling the bending radius/ twisting angle as well as the loading cycle duration.

5.2.8 Photodetector performance parameters extraction

Responsivity (R) is one of the critical parameters to quantitatively evaluate the performance of PD, and it is numerically expressed by the ratio of the response photocurrent (electrical output) to the incident power (optical input), which is calculated from the following equation [242]:

$$R = \frac{P_{ph}}{P_{in} \times A} \qquad (5.1)$$

Where, I_{Ph} is the photocurrent, P_{in} is the input power of the incident light and A is the effective area of the fabricated device. The photoresponsivity of the fabricated device is extracted when the device is exposed to UV or NIR light illumination at room temperature, with different input power intensities and under fixed bias voltage. The effective area of the detector was found to be 550 μm^2. Here we used the cross-sectional area dimensions of

triangular prism structures of ten GaAs microstructures as demonstrated in Figure 5.5. The product of channel length and number of printed microstructures were extracted to estimate the effective area of the PD.

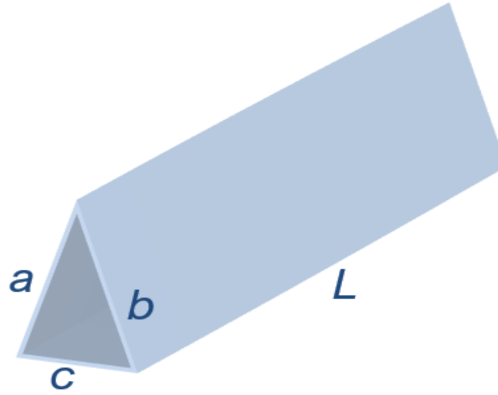


Figure 5.5: Schematic showing the morphology of the fabricated GaAs microstructures.

The detectivity (D*) is another fundamental parameter which indicates the capability of the detector to distinguish the minimum detectable signal, which is closely related to the shot noise from dark current, signal to noise ratio, taking into account the background radiation, and thermal fluctuation noise. Considering that the shot noise generated by I_{dark} is the dominant part of the total noise, the D* can be expressed as [242]:

$$D^* = \frac{R}{(2qJ_{dark})^{0.5}} \qquad (5.2)$$

Where, R is the responsivity, e is the electron charge, J_{dark} is the dark current density, A is the effective area of the detector.

Along with responsivity and detectivity, other important PD performance parameters, such as external quantum efficiency (EQE) and photoconductive gain (G) etc. were also extracted. The EQE, typically defined as the ratio of the number of photogenerated charge carriers to the total number of excitation photons, is given by[242]:

$$EQE\ (\%) = \frac{R \times hc}{e\lambda} \times 100\ (\%) \qquad (5.3)$$

Where, R is responsivity, h is Plank's constant, c is the velocity of light, e is elementary charge, and λ is the wavelength of the incident light.

The photoconductive gain (G) is another figure of merit for evaluating the performance of the PDs. It is defined as the ratio of number of the charge carriers contributing to photoconduction to the number of incident photons absorbed by the effective area of the device. It can be represented using the following equation:

$$G = \frac{(I_{Ph} \times hv)}{(P_{in} \times A \times e)} \qquad (5.4)$$

Where, I_{ph} is the photocurrent, hv is the photon energy, P_{in} is the illumination power on the active area, A is the effective irradiated area of the PD and e is the absolute value of the electron charge. The table 5.1 below summarised all the extracted values.

Table 5.1: Representation of the extracted photodetector performance parameters values.

UV_Semi insulating GaAs based photodetctor_ λ=365nm

Pin (µW/cm2)	Active Area_A (cm2)	Pin*A	Current_Ion®@ 20V	Responsivity_R (A/W)	Current_Idark® @20V	EQE1	R*A^0.5	(2*q*Idark)^0.5	Detectivity_D (Jones)	on/off	G_Gain
0.1	5.55E-06	5.55E-07	1.07E-08	1.92E+04	1.03E-09	6.44E+06	4.53E+01	1.81284E-14	2.50E+15	1.04E+01	6.53E+04
0.3	5.55E-06	1.67E-06	2.47E-08	1.48E+04	1.03E-09	4.96E+06	3.49E+01	1.81284E-14	1.9244E+15	2.40E+01	5.03E+04
0.5	5.55E-06	2.78E-06	4.45E-08	1.60E+04	1.03E-09	5.38E+06	3.78E+01	1.81284E-14	2.08412E+15	4.33E+01	5.45E+04
1	5.55E-06	5.55E-06	9.44E-08	1.70E+04	1.03E-09	5.70E+06	40.09009429	1.81284E-14	2.21145E+15	9.20E+01	5.78E+04
1.5	5.55E-06	8.33E-06	1.43E-07	1.72E+04	1.03E-09	5.75E+06	4.04E+01	1.81284E-14	2.23038E+15	1.39E+02	5.83E+04
2	5.55E-06	1.11E-05	1.76E-07	1.59E+04	1.03E-09	5.33E+06	37.45982653	1.81284E-14	2.06636E+15	1.72E+02	5.40E+04
2.5	5.55E-06	1.39E-05	2.10E-07	1.51E+04	1.03E-09	5.07E+06	35.60354896	1.81284E-14	1.96396E+15	2.04E+02	5.13E+04

NIR_Semi insulating GaAs based photodetctor_λ=850nm

Pin (µW/cm2)	Active Area_A (cm2)	Pin*A	Current_Ion®@ 20V	Responsivity_R (A/W)	Current_Idark® @20V	EQE1	R*A^0.5	(2*q*Idark)^0.5	Detectivity_D (Jones)	on/off	G_Gain
0.1	5.55E-06	5.55E-07	1.58E-08	2.85E+04	1.03E-09	4.16E+06	6.71E+01	1.81284E-14	3.70E+15	1.54E+01	9.68E+04
0.3	5.55E-06	1.67E-06	2.81E-08	1.69E+04	1.03E-09	5.66E+06	3.98E+01	1.81284E-14	2.19515E+15	2.74E+01	5.74E+04
0.5	5.55E-06	2.78E-06	4.02E-08	1.45E+04	1.03E-09	4.85E+06	3.41E+01	1.81284E-14	1.88031E+15	3.91E+01	4.92E+04
1	5.55E-06	5.55E-06	6.35E-08	1.15E+04	1.03E-09	3.84E+06	26.9750482	1.81284E-14	1.488E+15	6.19E+01	3.89E+04
1.5	5.55E-06	8.33E-06	8.38E-08	1.01E+04	1.03E-09	3.37E+06	2.37E+01	1.81284E-14	1.30804E+15	8.16E+01	3.42E+04
2	5.55E-06	1.11E-05	1.02E-07	9.16E+03	1.03E-09	3.07E+06	21.58101486	1.81284E-14	1.19045E+15	9.90E+01	3.11E+04
2.5	5.55E-06	1.39E-05	1.21E-07	8.72E+03	1.03E-09	2.92E+06	20.53277048	1.81284E-14	1.13263E+15	1.18E+02	2.96E+04

UV_Doped GaAs based photodetctor_λ=850nm

Pin (µW/cm2)	Active Area_A (cm2)	Pin*A	Current_Ion®@ 1V	Responsivity_R (A/W)	Current_Idark® @1V	EQE1	R*A^0.5	(2*q*Idark)^0.5	Detectivity_D (Jones)	on/off	G_Gain
1	5.55E-06	5.55E-06	4.52E-07	8.14E+04	3.73E-07	2.73E+07	1.92E+02	3.45485E-13	5.55E+14	1.21E+00	2.77E+05
2.5	5.55E-06	1.39E-05	5.32E-07	3.83E+04	3.73E-07	1.29E+07	9.03E+01	3.45485E-13	2.61454E+14	1.43E+00	1.30E+05
5	5.55E-06	2.78E-05	6.01E-07	2.17E+04	3.73E-07	7.26E+06	5.10E+01	3.45485E-13	1.47682E+14	1.61E+00	7.36E+04
7.5	5.55E-06	4.16E-05	6.21E-07	1.49E+04	3.73E-07	5.00E+06	35.14664261	3.45485E-13	1.01731E+14	1.66E+00	5.07E+04
10	5.55E-06	5.55E-05	6.38E-07	1.15E+04	3.73E-07	3.85E+06	2.71E+01	3.45485E-13	7.83871E+13	1.71E+00	3.91E+04

NIR_Doped GaAs based photodetctor_λ=850nm

Pin (µW/cm2)	Active Area_A (cm2)	Pin*A	Current_Ion®@ 1V	Responsivity_R (A/W)	Current_Idark® @1V	EQE1	R*A^0.5	(2*q*Idark)^0.5	Detectivity_D (Jones)	on/off	G_Gain
0.5	5.55E-06	2.78E-06	3.11E-06	1.12E+06	2.99E-06	1.64E+08	2.64E+03	9.78162E-13	2.70E+15	1.04E+00	3.81E+06
1	5.55E-06	5.55E-06	3.22E-06	5.80E+05	2.97E-06	8.47E+07	1.37E+03	9.74885E-13	1.40203E+15	1.08E+00	1.97E+06
1.5	5.55E-06	8.33E-06	3.30E-06	3.96E+05	2.98E-06	5.79E+07	9.34E+02	9.76524E-13	9.56298E+14	1.11E+00	1.35E+06
2.5	5.55E-06	1.39E-05	3.32E-06	2.39E+05	2.98E-06	3.49E+07	563.7046061	9.76524E-13	5.77256E+14	1.11E+00	8.13E+05
5	5.55E-06	2.78E-05	3.34E-06	1.20E+05	2.97E-06	1.76E+07	2.84E+02	9.74885E-13	2.90855E+14	1.12E+00	4.09E+05

5.3 Results and Discussion

5.3.1 Electro-optical characterisations of undoped GaAs wires-based photodetectors

After printing, the standard fabrication steps were carried out to define the sensing channel regions. The high conformability of the fabricated devices is shown using Figure 5.6a where the sample is conformally placed over glass tube. Figure 5.6b, c respectively shows the optical image and schematic of a fabricated device. The length and width of the sensing channel was 40µm and 50µm (10 GaAs microstructures with each having ~5µm width), respectively. With undoped microstructures obtained from a semi-insulating (high resistivity) bulk GaAs wafer and depositing multi-layer metals (Pd/Ge/Au) on them, the high-quality Schottky source and drain contacts were realised. The high-quality Schottky metal-semiconductor (MS) contact are needed to decrease the level of dark current and hence to enhance the detectivity value of the PDs and to obtain a high signal-to-noise ratio.[262] Current-voltage (I-V) curves for the fabricated device are shown in the Figure 5.7, with the measurements conducted in the dark and different intensities of UV light illuminations. In the dark conditions, the output current, obtained at ±20V, was of the order of few nanoamperes. Such a low off-device current in dark conditions is needed for higher detectivity, high value of the on/off current ratio and high signal-to-noise ratio. The low dark current could be attributed to the high resistivity of the undoped microstructures and the high-quality of Schottky contacts formed using multi-layered contacts. Further, the figure 5.7 shows that under light illumination, the photocurrent increases, particularly at high voltage bias, demonstrating a nonlinear and asymmetrical I-V behaviour. The photocurrent increases from ~1 nA (dark current) to ~40 nA (2.5 µW/cm^2) at bias voltage V_D = 20V. This is more than one order change in the photocurrent. Next, the electrical measurements were performed under dark conditions with varying applied voltage and intensity of UV (365 nm) and NIR (850 nm) wavelengths to verify the photodetection performance of the fabricated devices (Figure 5.6). Before this, the temporal response was obtained for an annealed and as-made device (Figure 5.8) at different UV light intensities from 0.1 to 2.5 µW/cm^2. The annealed PD device showed a reasonably high sensing response

as compared to the pristine device (as made). The photocurrent increased by 65% after annealing step. This could be attributed to the efficient charge transport after annealing. Thus, all further measurements were performed using annealed devices. Effect of the bias voltages and varying light intensity on important PD performance parameters including R, D*, EQE, G, I_{Light}/I_{Dark} ratio, and linear dynamic response (LDR) are extracted from the time-resolved photo response curves. The details related to the extraction of these performance parameters are given in the previous section. Table 5.1 summarises the calculated values.

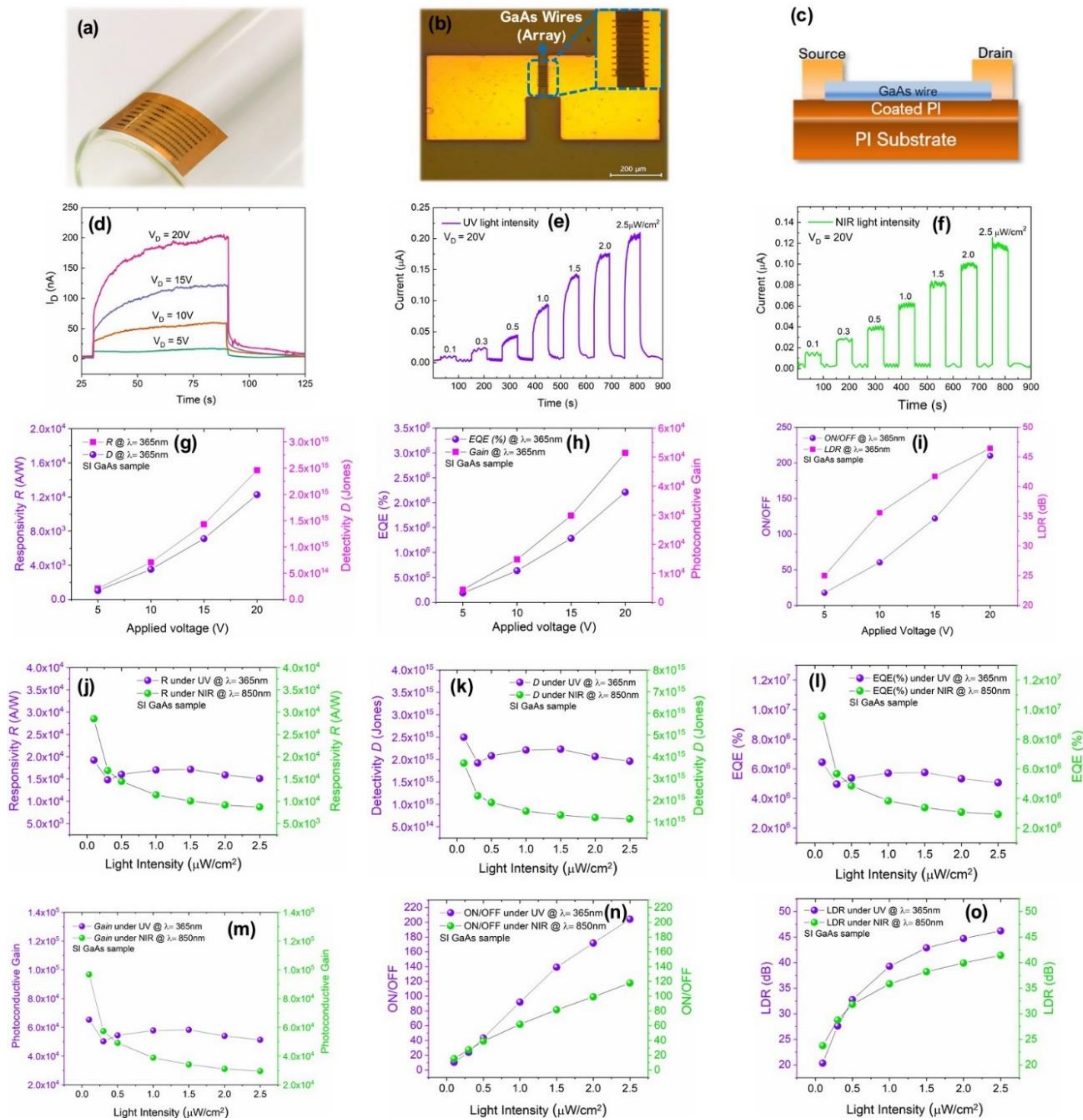


Figure 5.6: Static electro-optical characterisation of direct roll transfer printed undoped GaAs microstructures-based UV PDs; **(a)** optical image of the PD placed on a glass tube showing its high

flexibility; **(b)** optical image of the fabricated device; **(c)** schematic of the device; **(d)** temporal device response measured at fixed intensity of 2.5μW/cm^2 UV light illumination and for different bias voltages; **(e)** response to UV light with different intensities from 0.1 μW/cm^2 to 2 μW/cm^2; **(f)** response to NIR light with different intensities from 0.1 μW/cm^2 to 2 μW/cm^2; **(g-i)** extracted R, D*, EQE, G, I_{Light}/I_{Dark} ratio, and LDR as a function of applied voltage vias (from data shown in figure panel **5.6d**); **(j-o)** extracted R, D*, EQE, G, I_{Light}/I_{Dark} ratio, and LDR under both UV and NIR illumination at different intensities (from data shown in figure panel **5.6e** and **5.6f**).

As shown in Figure 5.6d, the photocurrent under the UV illumination as a function of time was measured at different bias voltages of 5, 10, 15 and 20 V. From the curves, the saturated photocurrent increases when the applied voltage is increased at the identical incident power intensity (2.5 μW/cm^2). Interestingly, the PD can reversibly switch between the high (under light illumination) and the low conductivity (under dark) state, demonstrating the capability to act as a high-quality photosensitive switch. Further, the extracted R, D*, EQE, G, I_{Light}/I_{Dark} ratio, and LDR values showed progressive increase with the applied bias voltage (Figure 5.6g-i). The maximum respective values of R, D*, EQE, G, I_{Light}/I_{Dark} ratio, and LDR at 20V are approximately 10^4, 6×10^{14}, 2×10^6, 5×10^4, 200, and 45 respectively. The efficient extraction of photo-generated carriers due to the high lateral field at 20V contributes to the rise of the photocurrent and thus, the PD performance. Next, PD performance parameters were obtained using the time-resolved photo response for different UV and NIR intensities (0.1– 2.5 μW/cm^2) at the fixed 20V (Figure 5.6e, and f). Under a bias of 20V, the devices exhibited a peak responsivity of $>2\times10^4$ A/W in the UV, and $>3\times10^4$ A/W in the NIR wavelength region. Under both UV and NIR excitations, the peak R value remained high showing device's applicability for wide spectra sensing (Figure 5.6j). Like R, the other PD parameters including D*, EQE, G, and LDR showed high values under both UV and NIR illuminations. For instance, the highest D* value of $>2\times10^{14}$ Jones was observed at the low illuminated power intensity of 0.1μW/cm^2 (under both UV and NIR). Further, the PDs showed negligible decrease in the R, D*, EQE, and G with increasing the incident power intensity for both UV and NIR. This small decrease can be attributed to the charge carriers scattering caused by internal-photothermal heating and enhanced carrier recombination effects [263]. Nevertheless, it noteworthy that the PD demonstrates high performance even at the higher power intensities.

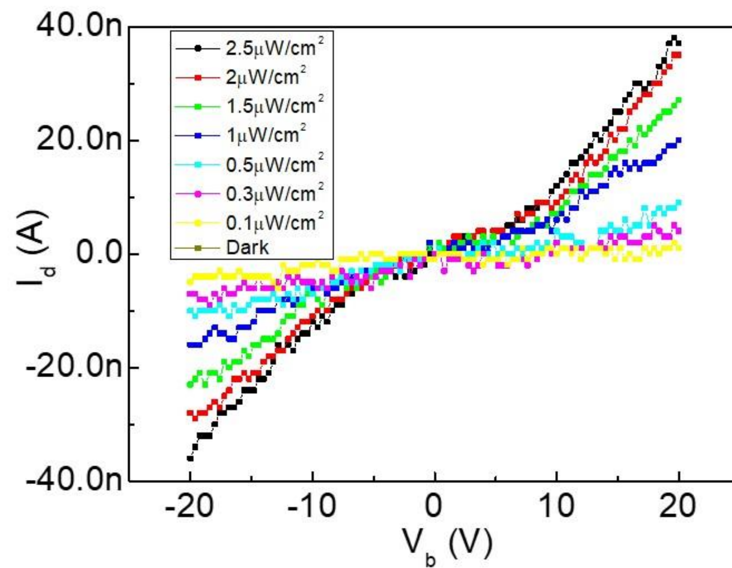


Figure 5.7: Current-Voltage (I-V) characteristics under dark and UV light at different intensities for undoped GaAs microstructure based flexible PDs.

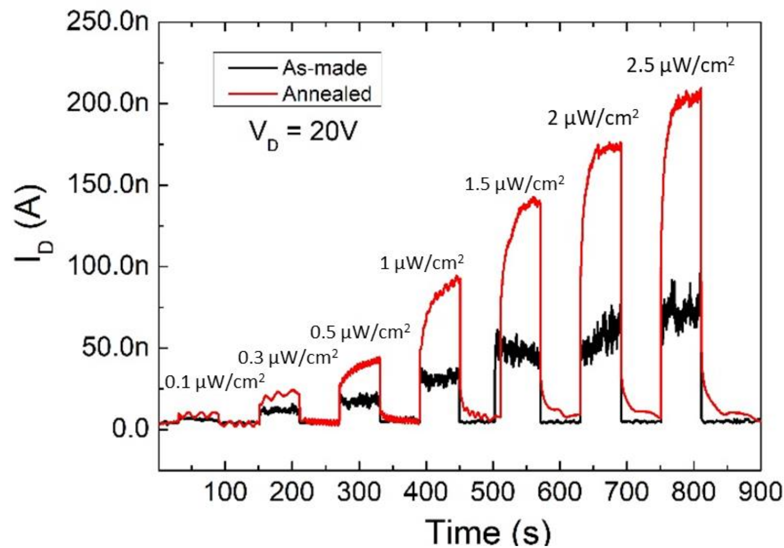


Figure 5.8: Temporal response characteristics for as made and annealed devices measured at the fixed bias voltage of 20V under UV light with different intensities from 0.1 to 2 μW/cm^2.

5.3.2 Electro-optical characterisations of doped GaAs wires-based photodetectors

Ultra-fast and low-power PDs are required for next-generation of energy efficient high-performance flexible electronics. Because of the low charge carriers (due to lack of doping), a high 20V bias voltage was needed to drive the semi-insulating GaAs microstructures-based PDs. To improve this the doped GaAs bulk wafer (carrier concentration 2.7 × 10^{18}

cm^{-3}) was used to realize high performance PDs with low power consumption. Doping dependent adjustment of the Fermi level has been shown to enhance the GaAs NW PD performance [258]. Similar fabrication process and device dimensions, as described above for undoped GaAs microstructures, was adopted to fabricate doped GaAs microstructure-based PDs. Next, the fabricated PDs were characterised under similar conditions as described above to extract the performance parameters. For this set of experiments, the electrical measurements were performed under UV illumination only. Although similar high performance was obtained under NIR light illumination (Figure 5.9).

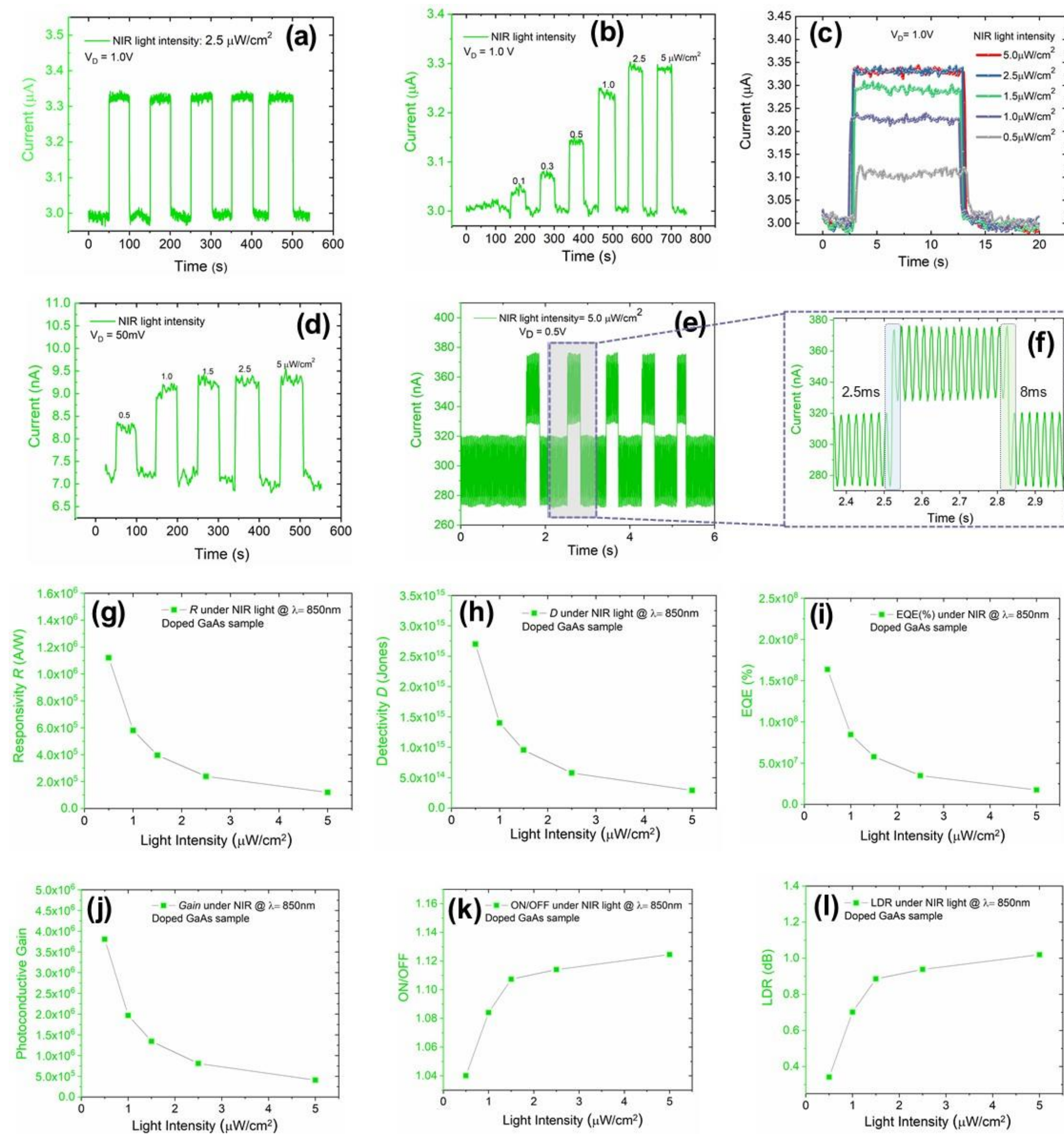


Figure 5.9: Static electro-optical characterization of the direct roll transfer printed doped GaAs microstructures-based NIR PDs; **(a)** cyclic response to NIR intensity of 2.5 μW/cm² confirming the repeatability of device performance; **(b-c)** response to NIR light with different intensities from 0.1

μW/cm^2 to 5 μW/cm^2 at fixed bias voltage of 1V. **(d)** response to UV light with different intensities at fixed ultra-low bias voltage of 50mV. **(e-f)** a high-resolution transient photo response under 5 μW/cm^2 UV light intensity at 0.5V to illustrate the rise and decay time constants. **(g-l)** Extracted PD performance parameters under UV illumination at different power intensities **(g)** responsivity (R), **(h)** detectivity (D*), **(i)** external quantum efficiency (EQE%), **(j)** Photoconductive gain (G), **(k)** $I_{ON\ (Light)}/I_{OFF\ (dark)}$ ratio, and **(l)** linear dynamic response (LDR).

Using the time-resolved photo response for different UV intensities at the fixed 1V, the PD performance parameters were extracted and are displayed in Figure 5.10. As expected, an increase of photocurrent is observed in doped GaAs microstructure-based devices with an increase of illumination power intensity (Figure 5.10a). The R, D*, EQE, and G associated with incident UV light power intensities are shown in Figure 5.10b, c, d, and e respectively. These results indicate that R, D*, EQE, and G of the device decreased with an increase of power intensity (similar trend like undoped GaAs microstructure-based PDs). The R, D*, EQE, and G of the PD with 1 μW/cm^2 UV power intensity could reach up to 8×10^4 A/W, 5×10^{14} Jones, 2.7×10^7 and 2.7×10^5, respectively. On the other hand, the extracted I_{Light}/I_{Dark} ratio and LDR values progressively increased with increasing illuminated power density. The I_{Light}/I_{Dark} ratio and LDR under 10 μW/cm^2 of UV power intensity can reach 1.2 and 1.5.

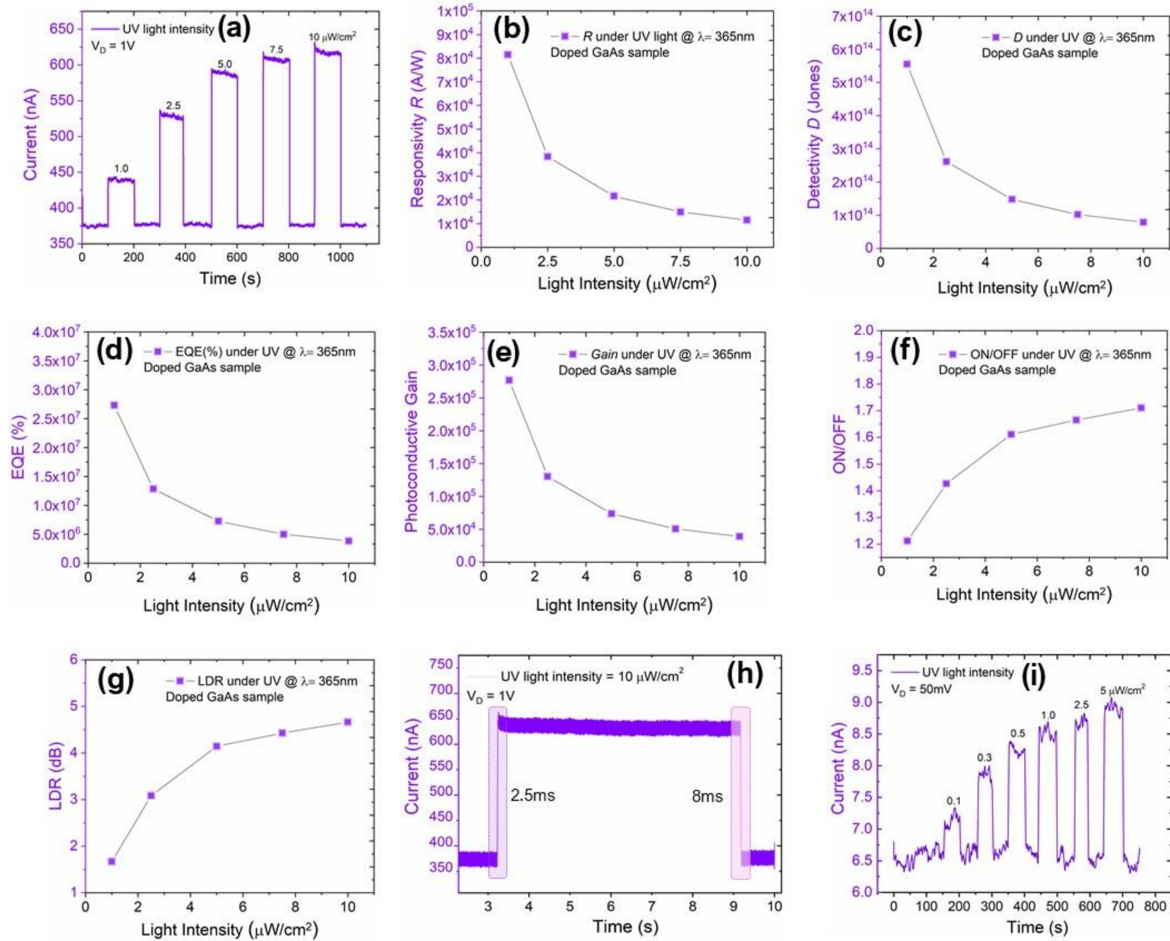


Figure 5.10: Static electro-optical characterization of the direct roll transfer printed doped GaAs microstructures-based UV PDs: **(a)** temporal device response measured under UV light with different intensities from 1 μW/cm² to 10 μW/cm² at fixed bias voltage 1V. Extracted PD performance parameters under UV illumination at different power intensities, **(b)** responsivity (R), **(c)** detectivity (D*), **(d)** external quantum efficiency (EQE%), **(e)** Photoconductive gain (G), **(f)** $I_{ON\ (Light)}/I_{OFF\ (dark)}$ ratio, and **(g)** linear dynamic response (LDR), **(h)** A high-resolution transient photo response under 10 μW/cm² UV light intensity at 1V to illustrate the rise and decay time constants. **(i)** response to UV light with different intensities at fixed ultra-low bias voltage of 50mV.

Next, the switching speed of the PD was investigated at an illuminated wavelength of 365nm. To evaluate the response speed of the GaAs PD, the response time (rise time) and recovery time (decay time) were extracted using the graph shown in Figure 5.10h. The response and recovery time were found to be 2.5ms and 8ms, respectively. Finally, we show that the PDs using doped GaAs microstructures can function at ultra-low voltage. The time-resolved photo response for different UV intensities at an operating voltage of 50 mV shows the capability of the device to detect low intensities with low power consumption. Table 5.2 and figure 5.11 summaries and compares the extracted PD performance parameters for

doped and undoped GaAs microstructures-based devices with the state-of-the-art photodetectors realised using GaAs and other compound semiconductors. The sensing performance of printed GaAs microstructures is further compared with other state-of-the-art sensing materials employed to detect broad band spectrum (Table 5.3). Although the current on/off ratio and response time of the GaAs microstructure-based PDs are modest, they stand out in terms of consistent high responsivity and detectivity across the UV to NIR range.

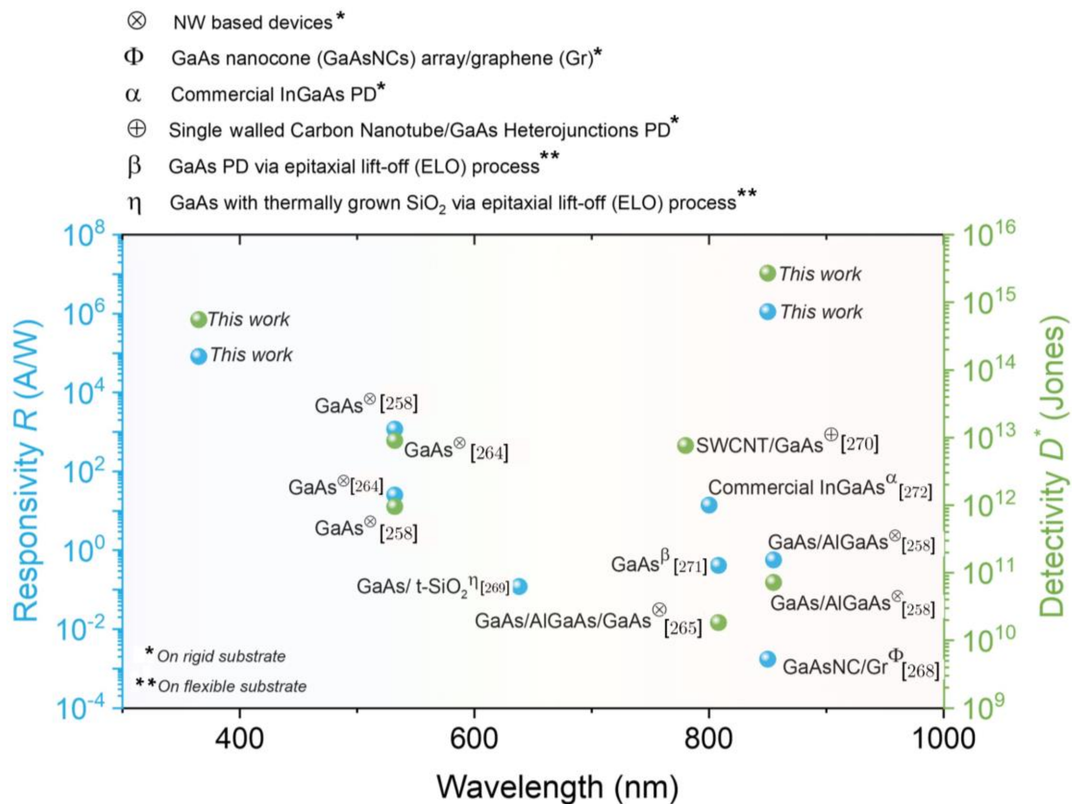


Figure 5.11: Comparison of flexible GaAs microstructures-based broadband PDs with state-of-the-art devices: Responsivity and detectivity comparison of direct roll transfer printed GaAs microstructure array-based PDs with other state-of-the-art GaAs and compound semiconductors-based PDs on flexible/rigid substrate. These PDs are based on different structures such as nanowires, thin film, and heterostructures etc.

Table 5.2: Comparison of undoped and doped GaAs microstructures-based flexible PDs with GaAs and other compound semiconductors based state-of-the-art light detectors.

Material	Excitation wavelength (nm)	Substrate	Bias Voltage (V)	Peak R (A/W)	Peak D* (jones)	Peak EQE (%)	Peak G	Peak on/off	Response/ recovery times (ms)	Ref.
Semi-insulating (undoped) GaAs microstructures	365	Flexible	20	1.92×10^4	2.50×10^{15}	6.44×10^6	6.53×10^4	2×10^2	3/10	This work
	850	Flexible	20	2.85×10^4	3.70×10^{15}	4.16×10^6	9.68×10^4	1.18×10^2	3/10	This work
n-type doped GaAs microstructures	365	Flexible	1	8.14×10^4	5.55×10^{14}	2.73×10^7	2.77×10^5	1.71	2.5/8	This work
	850	Flexible	1	1.12×10^6	2.70×10^{15}	1.64×10^8	3.81×10^6	1.12	2.5/8	This work
Single GaAs NW	532	Rigid	1	25	9.04×10^{12}	-	-	2.49×10^3	-	[264]
GaAs NW	532	Rigid	1	1175	9.52×10^{11}	2.74×10^5	-	-	-	[258]
GaAs/AlGaAs /GaAs NW	808	Rigid	5	0.75	1.83×10^{10}	50	-	$>10^2$	175/190	[265]
GaAsSb NW	1300	Rigid	0.15	2.37	1.08×10^9	-	-	1.66	-	[266]
InGaAs NWs	1100-2000	Rigid	0.5	6.5×10^3	-	5.04×10^5	-	~17.3	-	[267]
GaAs/AlGaAs NW	855	Rigid	2	0.57	7.2×10^{10}	-	-	145	-	[257]
GaAsNC/Gr	850	Rigid	0	1.73×10^{-3}	1.83×10^{11}	-	-	10^4	0.07/0.12	[268]
GaAs film/SiO	638	Flexible	-1	0.12	-	-	-	-	-	[269]
SWCNT/n-type GaAs	780	Rigid	0	274×10^{-3}	7.6×10^{12}	-	-	$\sim 10^2$	1.41/0.27	[270]
GaAs PDs arrays	808	Flexible	-	0.41	-	48	-	-	-	[271]
Commercial InGaAs	800	Rigid	-100	-	10^{12}	-	-	-	-	[272]

Table 5.3: Comparison of GaAs microstructures-based flexible PDs with state-of-the-art photo sensing materials used to detect wide range of wavelength.

Device structure	@Voltage bias (V)	Wavelength (nm)	Responsivity (R) (A/W)	Detectivity (D*) (Jones)	Ref.
FTO/$MAPbI_{3-x}(SCN)_x$ NW network/FTO	2	490	0.23	7.1×10^{11}	[1]
Al/Ca/$NH_3Pb(I_{1-x}Br_x)_3$ NW arrays/Al/Ca	5	550	12.5×10^2	1.73×10^{11}	[2]
FTO/$CH_3NH_3PbI_3$ nanonets arrays/FTO	10	700	10.33	-	[3]
ITO/SWWCNT/PbS-QDs/$MAPbI_{3-x}Cl_x$/ITO	1	500	0.5	1.4×10^{11}	[4]
ITO/$CsPbBr_3$ nanosheet/CNTs/ITO	10	-	31.1	-	[5]
ITO/Gd-doped ZnO NRs/$CH_3NH_3PbI_3$/ITO	1	740	0.67	1.4×10^{13}	[6]
Au/2D perovskite/Au	-	550	-	2.1×10^{13}	[7]
AuGe/Ni/Au- / n-type GaAs microstructure / AuGe/Ni/Au	1	365	8.14×10^4	5.55×10^{14}	This work
AuGe/Ni/Au / n-type GaAs microstructure / AuGe/Ni/Au	1	850	1.12×10^6	2.70×10^{15}	This work

5.3.3 Wide range sensing mechanism

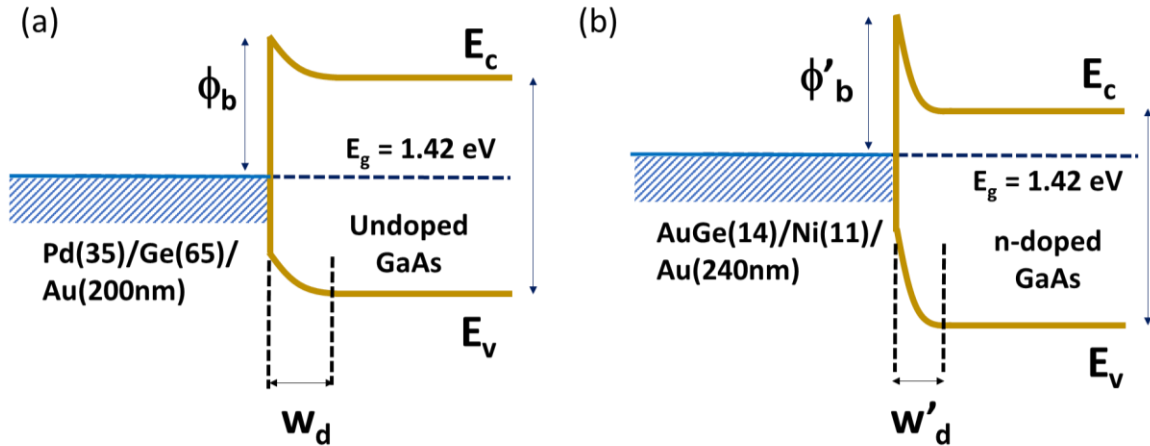


Figure 5.12: Band diagram of the GaAs microstructure-based photodetector, taking into consideration Schottky barriers at the metal-semiconductor contacts: **(a)** for undoped GaAs and **(b)** for n-type doped GaAs. Φ_b and W_d is the Schottky barrier height and depletion width, respectively for undoped GaAs microstructures whereas Φ'_b and W'_d is the Schottky barrier height and depletion width, respectively for n-type doped GaAs microstructures.

The measured photo response for GaAs wires-based PDs shows a broadband detection with wavelength ranging from 365nm to 850nm. The observed broadband detection behavior can be explained using energy band diagram (see Figure 5.12). The energy band diagrams for the Schottky contacted GaAs based PDs are shown in its equilibrium state i.e., under no light illumination and no bias voltage. Upon illumination with a wavelength corresponding to photoenergy larger than that of the GaAs bandgap, large number of electron-hole pairs are generated, which leads to increase in the device current. The illuminated wavelength in the present case, under both UV (3.3 eV) and NIR (1.45 eV) light, is sufficiently high to generate electron-hole pair in GaAs (Eg = 1.42 eV). The presence of Schottky contact helps to achieve better sensing performance. For semi-insulating GaAs, high quality Schottky contacts (larger depletion width with sufficiently high barrier height) were obtained (Figure 5.12a). This resulted in the low dark current density. The increase in charge density in GaAs upon light illumination lowers the effective barrier height, leading to easy transport of carriers, and thus, to a significantly higher detectivity and current on/off ratio. However,

because of the low doping, the high operating bias (20V) was needed to drive the photocarriers. Therefore, PDs using doped GaAs microstructures were also fabricated and they showed similar high sensing performance at much lower bias voltage of 1V. However, for doped GaAs microstructures-based PDs, the on/off ratio was 2 orders lower than the devices based on undoped GaAs microstructures. This is because of the higher dark current due to difficulties in realizing high quality Schottky junctions on n-type GaAs (Figure 5.12b) [273]. Because of the high charge carriers and surface states in microscale materials, it is practically difficult to have high quality Schottky contacts (smaller depletion width). The smaller depletion width leads to large tunnelling current. The reduction of the surface trap concentration by surface passivation technique can help in the formation of high quality Schottky contacts [274]. This could help increase the on/off ratio and decrease the response time down to microseconds.

5.3.4 Mechanical stability evaluation of flexible GaAs photodetectors

The reliable and robust performance of flexible PDs is critical for their applications in wearable systems, robotics, and healthcare, etc. where these devices typically experience mechanical deformations such as bending and twisting. In this regard, the stability and reliability of presented devices was examined under different mechanical deformations. For this study, bending and twisting mechanical loadings were applied using Yuasa endurance testing system (see Figure 5.13) and subsequently, the electro-optical measurements were made. First, the samples were subjected to 500 bending cycles at a bending radius of 20 mm. After every 100 bending cycles, we measured the PD performance parameters (R, D*, and EQE) at fixed UV light intensity of 2.5 µW. As shown in Figure 5.13a-c., the R, D*, and EQE as did not show any appreciable degradation for 500 bending cycles. Further, the mechanical reliability of PDs during repeated twisting loadings was evaluated (Figure 5.13 d-f). The presented data shows that there is a small degradation in sensing performance due to twisting deformation over 500 cycles. The R, D*, and EQE data for the ±30° twisting showed 1.5, 2.5, and 1.5 percent decrease in the values respectively, after 500 cycles. The observed negligible decrease in the device performance after mechanical bending could be

due to residual strain in the GaAs microstructures or metal stacks or there may be minor cracks. We have observed several devices before and after mechanical loadings (bending and twisting) under SEM. Typical SEM images for as-made devices and after mechanical loadings are shown in the figure 5.14. The experimental data shows NO cracks are developed in the metal stack and GaAs microstructures after mechanical loadings. In the absence of any cracks, the minor performance degradation could be due to residual strain. This requires further in-depth analysis, which will plan to present in our future works.

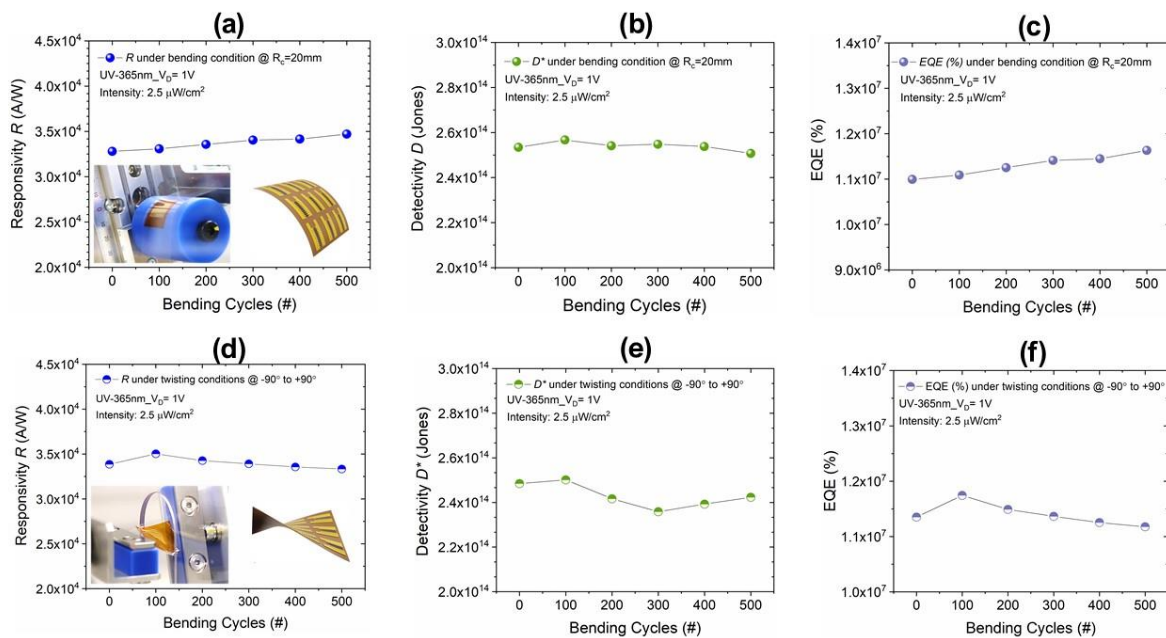


Figure 5.13: Evaluation of the PD performance under bending and twisting: Effect of bending loading (20 mm) on responsivity **(a)**, specific detectivity **(b)** and external quantum efficiency **(c)**. The inset in figure panel 'a' shows schematic/optical image of devices under bending loadings. Stability of responsivity **(d)**, specific detectivity **(e)** and external quantum efficiency **(f)** under twisting loading of ±30° up to 500 cycles. The inset in figure panel 'd' shows schematic/optical image of devices under twisting motions.

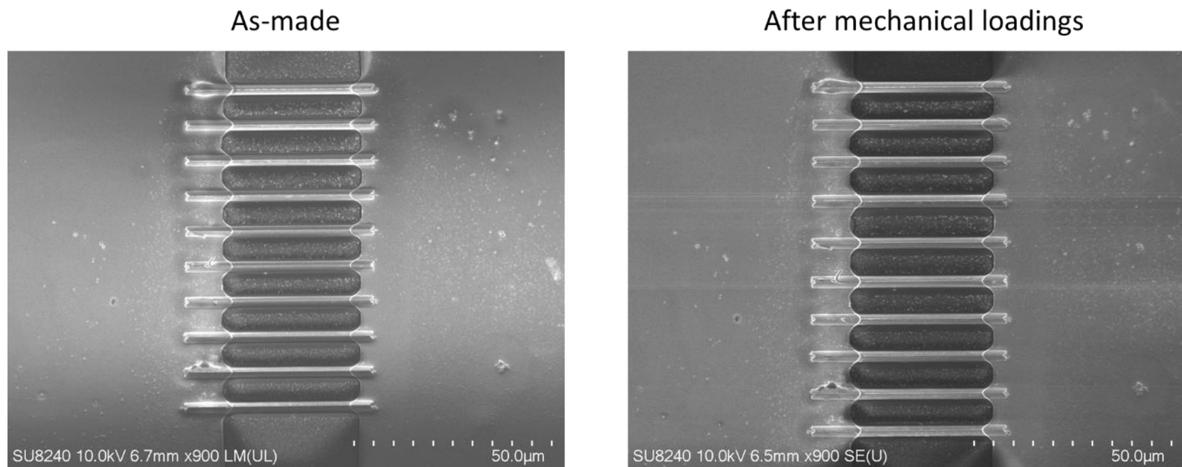


Figure 5.14: SEM images of the GaAs microstructure-based photodetectors showing influence of bending and twisting on the GaAs microstructures and metals.

5.4 Conclusions

Nano/microstructures of III-V semiconducting materials have demonstrated enormous potential for advanced electronics and optoelectronic applications, but with devices fabricated mainly on rigid substrates. Due to the lack of suitable integration techniques, it has been challenging to transfer and integrate these nano/microstructures on flexible substrates and large areas. In this regard, the arrays of well-defined and laterally aligned printed semi-insulating (undoped) and doped GaAs microstructures, obtained here, present, and important advancement. For the first-time, the integration of arrays of GaAs microstructures over PI substrates has been achieved using DRTP. It is noteworthy to mention that the optimized DRTP technique showed excellent registration (<0.1 µm) and high transfer yield (~95%). The performance of the GaAs microstructures-based devices was systematically investigated under wide range of illumination wavelengths (UV and NIR) and the results shows important advantages over the previous reports using GaAs thin-films, nanostructures etc. Firstly, high-performance undoped GaAs microstructures-based devices illustrated the capabilities of DRTP for large-scale integration of device with high R (>10^4 A/W), D* (~10^{15} jones), G (>10^4), EQE (10^6 %), and light to dark current on/off ratio values (>10^2) under wide spectrum (365 and 850 nm). The obtained performance values are among the best reported GaAs based PDs including the devices on rigid and

flexible substrates. This high PD performance is attributed to low dimensionality of the device and high mobility of the GaAs microstructures, which resulted in an efficient charge transport, contamination free transfer of arrays of GaAs microstructures, and high quality of the Schottky contacts. These resulted in the low dark current density and thus, high detectivity and on/off ratio. However, for doped GaAs microstructures-based PDs, the on/off ratio was 2 orders lower than the devices based on undoped GaAs microstructures. Although the on/off ratio of the doped GaAs microstructures-based PD are not the best, their consistent high performance across the broad spectral range from UV to NIR at low bias voltage over flexible substrate is worth noting as this has not been reported so far. Further, owing to the high carrier mobility of GaAs, the response time is observed to be short (2.5ms) for both doped and undoped GaAs. Likewise, devices showed high photoconductive gain. The obtained response time of few milliseconds represents one of the fastest responses among reported PDs in the literature. Finally, the robust operation of devices under highly bending conditions was confirmed by systematic experiments performed with bending and torsion set up. The experimental data showed negligible performance degradation under bending loading and slight decrease in performance with torsional loading up to 500 cycles. Nevertheless, it is noteworthy that the PDs continued to provide high performance and no mechanical failure of the device was observed. Thus, it was evident that the GaAs microstructures and the demonstrated integration technique have huge potential to realize the next generation of flexible high performance and broadband PDs. Whilst the application of printed arrays of GaAs microstructures has been demonstrated for high-performance flexible broadband PDs, the presented approach could be followed for development of highly efficient solar cells or high-performance electronics for power devices.

Author Contributions:

In this chapter, the conceptualization of the overall work was done by me and Dahiya, R. The experiments and fabrication tasks were carried out and led by me. The Automated experimental setup for direct roll transfer printing (DRTP) process was built, developed,

and led by Christou, A. The transfer printing experiments were carried out and led by me, with valuable assistant from Christou, A. The COMSOL simulation using finite element analysis (FEA) model was carried and led by Christou, A. The device characterization was carried out by me with support from Dahiya, A.S. All authors mentioned in this chapter contributed to the work through regular discussions. Dahiya, R. provided overall supervision for the project.

Chapter 6.

Direct Roll Transfer Printed Silicon Nanoribbon Arrays based Multifunctional Micro Solar Cells

Abstract

The progression of artificial intelligence (AI) has led to the development of computing systems capable of collecting, processing, and utilising metadata from human activities and surrounding environments. Consequently, there is a growing need for self-powered electronic systems/networks supported by energy harvesters. This has been facilitated by the reduction of power consumption in contemporary Internet of Things (IoT) electronics, including wireless sensors. Remarkably, low-light energy harvesting photovoltaic cells have emerged as a promising self-sustainable and eco-friendly power source, as they can be operated under ambient indoor lighting conditions. In this regard, powering the ever-increasing number of sensor nodes in a wireless sensor network (WSN) is critical to implementing the Internet of Things. At present, sensor nodes are typically powered by conventional batteries. The economic and toxicity issues of battery-powered devices mean that low-cost, green and sustainable energy harvesting technology will be needed. Printed large-area electronics could provide a solution. The chapter outlines the fabrication method for miniaturised solar cells on flexible substrates that can perform dual functionality: energy harvesting and self-powered photosensors. The active elements, which incorporates p-intrinsic (i, moderately doped)-n silicon nanoribbons structures for converting light into electricity is fabricated using the top-down approach that was previously introduced in the thesis chapters. The direct roll transfer printing route is further used to integrate these energy conversion elements onto flexible substrates over large areas and use them to realize miniaturized solar cells with an area of just ~315 µm^2. The maximum power density

of ~11 μW/cm^2 is obtained by connecting 32 identical micro cells in parallel. In addition to the light energy harvesting, the fabricated micro solar cells can also work as wideband photodetectors. As photodetectors, these devices showed excellent current rectification characteristic ratio of up to 8 orders, when measured under dark and indoor white light illumination. The developed photodiodes or micro solar cells can act as self-powered photo sensors with distinctive photo response under visible-UV-NIR light illumination. It is found that the fabricated device exhibits excellent performance of broadband photoresponse from UV to NIR, with high-speed response, showing a peak responsivity R of (2.48 A/W) at 365 nm at zero bias voltage, corresponding to an external quantum efficiency, EQE reaching (8.30×10^2 %), detectivity D* (2.74×10^{13} jones), which relatively comparable with most values reported for silicon-based flexible PDs. In addition, the device shows an extremely fast response speed (rise time τ_{Rise} = 205μs and fall time τ_{Fall} = 200μs) and stable detection performance with good mechanical flexibility. The high-performance PD described here indicates a potential method that could be beneficial for a range of flexible applications, including sensors, optical detectors, imaging systems, and optical communication systems.

6.1 Introduction

The portable sensor-laden systems such as electronic-skin (e-skin) and wearables could enable a wide range of Internet of Things (IoT) applications in areas such as healthcare, smart homes, digital agriculture etc [64, 275, 276]. Green power sources in miniature forms are expected to play a significant role in the development of future IoT, specifically for intelligent homes and mobile health. To operate the sensors and electronics in real-time, a reliable source of energy is needed [12, 277, 278]. Currently, the energy in these systems is supplied through conventional batteries, which have drawbacks such as bulkiness, non-flexible, and toxicity etc. [54, 279, 280]. Further, the periodic replacement or frequent charging of these power reservoirs is not ideal, particularly for applications where minimal human intervention is required such as soft robots performing surgeries [281]. Depending on the number of sensors, the power requirement could vary from a few tens of microwatt for low power components to few mW for short active periods during which the data collection,

analysis and transmission is performed [282, 283]. This range of power could be met with smart nanogenerators (NGs) and that is why several green energy sources are being intensively investigated [9, 284]. Some of these energy devices could also perform multiple function i.e., in addition to generating or storing energy they could be used as self-powered sensors [285]. Considering theses aspects, the miniaturized energy sources, in flexible and/or stretchable form factors, are being explored for effective usage in portable and wearable electronic systems. Among wide variety of energy harvesters (e.g., piezoelectric, triboelectric, pyroelectric etc.) explored so far, the solar cells are closest to meeting the power requirements of portable and wearable electronic systems [20]. In this regard, miniaturized flexible energy sources that can convert indoor light into electric energy are highly advantageous for low-powered wireless sensor networks that play a vital role in IoT systems. These components don't require direct access to conventional power sources like batteries etc. [286-288]. Developing a miniaturized solar cell module that possesses features such as high stability, low cost, and lightweight can be considered a key element in IoT systems [289, 290]. For instance, the stability and reliable operation of indoor solar cells is a critical requirement when it comes to powering indoor applications such as wireless sensor networks. The indoor environment can include office spaces, cold or warm rooms, warehouses, etc. Wireless sensing-based electronics are highly expected to be deployed in these environments, hence likely to experience variations in temperature and relative humidity during daily life.

For decades, solar cells have been explored as green energy devices, and recently it has been shown that they could be employed to gather environmental information [285], which considered an attractive proposition for the wearable and portable systems. However, most of the commercial photovoltaic (PV) cells are rigid and stiff, which make it difficult to integrate them over the curvy surface of robots and/or human bodies [12, 279]. For this reason, solution-processed solar cell technologies such as organic (OSCs), perovskite (PSCs), and dye-sensitized solar cells (DSSCs) have gained significant attention since they have flexible form factors, low cost, adjustable bandgap capability, large area manufacturing, and low temperature processing. There has been a considerable research interest focused on

deploying these technologies for harvesting artificial indoor light, including powering IoT-related electronics. For instance, perovskite solar cells provide higher efficiency in the indoor environment (η~25%), in addition to the structural flexibility to conform to curvy surfaces [291, 292]. However, the low stability and high toxicity of perovskite solar cells remain a concern, which could prevent them from being employed in practical applications [290]. Most solution-processed solar cells made from organic or perovskite materials degrade under high humidity and heat due to their sensitivity to moisture and oxygen, resulting in end-of-life challenges in terms of electronic waste [293, 294]. Dye-Sensitized Solar Cells (DSSCs) tend to have higher stability and non-toxicity compared to Organic Solar Cells (OSCc) and Perovskite Solar Cells (PSCs). Although DSSCs have shown great potential for low light environments with an efficiency of (η~13%), they can experience degradation and potential leakage due to the utilization of liquid electrolytes [295]. Table 6.1 summarise the performance parameters for state-of-the-art of indoor solar cell reported under indoor white LED lighting. For indoor applications, Si thin film solar cells made from amorphous silicon (a-Si) and polycrystalline Si (pc Si) are attractive due to low-cost manufacturing and compatibility with low-temperature processing [296]. However, a-Si-based solar cells have limitations due to active material degradation caused by the light-induced creation of defects called Staebler Wronski effect [295, 297], and pc Si solar cells have limited performance due to poor material quality and high defect content compared to high quality monocrystalline Silicon (*mc*-Si) [296]. The efficiency of energy conversion in indoor light environments is reported to be higher in solution-processed solar cells, such as OSCs and PSCs, as illustrated from Table 6.1. The low light intensity within the visible spectrum, typically ranging from 200-1000 Lux, emitted by white LEDs in indoor ambient light [290]. To ensure the reliable operation of solar cells for indoor applications, such as wireless sensor networks and IoT-related electronics, they must be designed to minimize degradation and maintain their performance over time. This requires the use of high-quality materials and manufacturing processes that are resistant to environmental factors. One such attractive semiconducting material is monocrystalline silicon.

Table 6.1: summarise the solar cell performance parameters for state-of-the-art indoor solar cell reported under indoor white LED lighting.

Device structure morphology	Method	Light source	Illuminance (Lux)	P_{in} (µW/cm²)	J_{SC} (µA/cm²)	V_{OC} (mV)	Fill Factor FF [%]	efficiency (η) [%]	Ref
Monocrystalline Si-NRs (70nm Thick) p-i-n solar cells	Direct Roll Transfer Printing (DRTP)	LED	**900**	257	20.25	184	47.31	0.69	This Work
			1050	300	27.53	191	50.42	0.89	This Work
			1250	358	36.44	206	50.29	1.06	This Work
Hydrogenated amorphous Si (*a*- Si:H)	Large area deposition	LED	**1000**	371	113	0.67	68	21	[296]
Monocrystalline Si (*c*-Si)	N/A	LED	**1000**	371	94	0.4	35	5.6	[296]
polycrystalline Si (*pc*-Si)	N/A	LED	**1000**	371	86	0.3	35	3.7	[296]
polycrystalline Si (*pc*-Si)	N/A	LED	**500**	N/A	77.5	0.22	45.4	4.73	[298]
Organic solar cell (OSC)	Solution casting	LED	**300**	104	28.0	0.702	46	8.7	[299]
Organic solar cell (OSC)/ZnO nanoparticle	R2R slot-die-coating and screen printing	LED	**1000**	N/A	77.8	0.61	55	7.2	[300]
Organic solar cell (OSC)/SnO_2 nanoparticle	R2R slot-die-coating and screen printing	LED	**1000**	N/A	111	0.61	62	13.9	[300]
Perovskite solar cell ($FA_xMA_{1-x}PbI_yBr_{3-y}$)	Solution casting	LED	**1000**	680	251	0.967	73.3	25.7	[291]
Inverted P3HT–ICBA Organic solar cell (OSC)	Spin coating and deposition	LED	**500**	170	43.8	0.7	71.9	13.0	[301]
Dye-sensitized solar cell (DSSC)	Screen printing/ Dye soaking	LED	**1000**	N/A	114	0.49 V	75	12.82	[302]
Semi-transparent organic solar cell (ST OSCs)	Deposition and spin coating	LED	**1000**	N/A	99.2	0.67	64.82	15.46	[303]

N/A – data not available

Monocrystalline-based silicon solar cells offer the highest conversion efficiency among outdoor solar cells due to their incredible purity form [275, 304]. Additionally, electronic layers can be printed based on monocrystalline silicon, making printed electronics an attractive, resource-efficient, and low-cost manufacturing route for realizing electronics on any substrate [52, 161, 305, 306]. While printing techniques have been used for electrode

fabrication in bulk silicon-based cells, transfer printing of active silicon layers has not been fully explored. This chapter explores the transfer printing approach for integrating photoactive layers based on monocrystalline silicon on flexible substrates. From a material perspective, monocrystalline silicon remains one of the most superior semiconductor materials for realizing solar cells due to its high reliability, ideal band gap, absorption across the wide solar spectrum, high mobility, and excellent transport properties. Most commercially available solar cells have reached their theoretical limit in terms of energy conversion efficiency [288, 304, 307]. However, the low material consumption, competitive cost, and compatibility with microelectronics fabrication technology make monocrystalline silicon an excellent candidate for solar cell fabrication. New strategies are required to improve the efficiency and flexibility of solar cells and reduce their manufacturing cost. These features are particularly critical for IoT applications, where billions of connected devices require power sources at a low cost. Therefore, the development of green, miniaturized energy sources that can be realized at a low cost with high flexibility could significantly contribute to the progress of future IoT [308]. Therefore, a significant progress has made towards developing novel material fabrication strategies, optimizing active structure geometries for light trapping, doping techniques, advanced manufacturing techniques, and cost-effective manufacturing to improve the efficiency and flexibility of solar cells.

Flexible solar cells based on inorganic micro/nanostructures

In recent years, flexible solar cells based on silicon micro/nanostructures have been extensively studied using various fabrication methods. Among these, the top-down approach using anisotropic chemical etching has gained significant attention due to its precise patterning capability, excellent control over micro/nanostructure geometries, and the ability to selectively control doping profiles using high-quality inorganic semiconducting materials as source wafers. One of the methods that have recently been developed involves using high-quality bulk wafers to generate printable microcells based on Si microstructures, such as wires and ribbons. The dependency of the output conversion efficiency on the thickness of

microstructures has been investigated [309]. This approach relies on a spatially anisotropic wet etching rate that depends on the crystallographic orientation of the Si wafer [309-311]. However, it is most likely limited to generating releasable micro-scale structures that are compatible with micro-scale transfer printing techniques. Another approach that has been explored involves employing an anisotropic chemical etching scheme to obtain micro-scale Si cells (~14 µm) with hexagonal shapes [312]. Additionally, some recent works have demonstrated several concepts of transfer printing combined with an epitaxial liftoff (ELO) process to yield a potential path towards flexible solar cell-based devices [313]. The working principle of epitaxial lift-off is that it simply enables the release of the active material from the source wafer to be transferable from the handled substrate by selective chemical etching of a sacrificial layer. This strategy has been widely explored in various III-V- based solar cells, such as GaAs, InP, etc. Although the approach is still in its nascent phase and has not yet been used for commercialization due to several limitations, including the high cost associated with epitaxial growth of materials, poor reliability in undercut etching, and challenges related to material handling due to its fragility. Recent approaches for high-efficiency flexible solar cells include thinning of silicon wafers (~500 µm) down to a few micrometers (~2.7 µm) using mechanical or chemical/mechanical polishing [314]. However, this approach has limitations in terms of complex packaging and bending due to the brittle nature and dislocation defects in silicon. To obtain a releasable form of micro-scale cells, all strategies mentioned above are compatible with the conventional transfer printing process using soft stamps. These provide a solution to manipulate and integrate micro thick functional solar cells onto flexible substrates.

In this regards, miniaturized forms of high-quality silicon nanostructures e.g., wires and ribbons, along with the bendability factor might provide a potential route toward achieving high yield, low cost, and large area scalability for large cell production in the photovoltaic industry. Conceptually the cost reduction for producing solar photovoltaics can be achieved by reducing the active material usage e.g., silicon (≈50% of the total manufacturing cost in traditional silicon solar cells) [311]. The unique nanoscale thickness of a few tens of nanometer can effectively contribute toward achieving low-cost and efficient photovoltaics

for low light intensity harvesting and wide absorption spectrum [315], making them an excellent candidate for indoor energy harvesting applications [316]. The obtained results in this work contribute toward achieving this goal, by introducing high-quality silicon nanostructures-based solar cells that are much thinner than most of the reported works [309, 311]. This chapter demonstrates the efficacy of a printing method for transferring Si nanostructures onto flexible substrates to create a release nanoscale p-i-n solar cell array. As shown in figure 6.1, the developed method combines an established anisotropic wet etching scheme with a roll-based direct transfer printing process, which enables the transfer of ultrathin structures with thickness below 100 nm directly onto flexible substrates, without the need for a multistep transfer printing process using an elastomeric stamp. [52, 57, 64]. This direct roll transfer printing technique is more cost-effective and resource-efficient than traditional integration techniques, and produces less material wastage in the form of unusable transfers [52].

While the validity of direct roll transfer printing has been demonstrated previously for high-performance devices such as transistors and photodetectors, this work focuses on the lateral structure of p-i-n for solar cell fabrication, as it is better suited for ultrathin structures such as Si NRs with a thickness of 70 nm. The p-i-n structures offer several advantages for light absorption enhancement in the depletion region and efficient carrier generation. The depletion region formed from the surface to the depth of the junction creates an internal field that leads to efficient carrier separation and transport, increasing the carrier's lifespan and density in the undoped region [317]. This, in turn, leads to a higher output current as both types of carriers are injected into the intrinsic layer. Ultimately, the charge carriers are confined in the intrinsic region, further increasing the carrier density and output current [318].

To this end, the direct roll transfer printing method is utilized to integrate energy conversion elements onto flexible substrates, resulting in miniaturized p-i-n Si NRs-based solar cells with a device area of approximately 315 μm^2. By connecting 32 identical micro cells in parallel, a maximum power density of approximately 11 $\mu W/cm^2$ is achieved. The electrical characteristics obtained for the fabricated solar cells show current rectification ratio up to

~8 orders when measured under dark and light illumination conditions. These micro solar cells can also function as wideband photodetectors in addition to light energy harvesting. The wide absorption bandwidth of the fabricated p-i-n Si NRs based photodiodes for photon absorption shows distinctive photo response under visible-UV-NIR light illumination. As photodetectors, these devices demonstrate outstanding performance in terms of broadband photoresponse, from ultraviolet (UV) to near-infrared (NIR) regions, featuring high-speed response and a peak responsivity (R) of 2.48 A/W @ 365 nm under zero bias voltage. This translates to an external quantum efficiency (EQE) of 8.30×10^{2} % and a detectivity (D*) of 2.74×10^{13} jones, comparable to the reported values of silicon-based flexible photodetectors (PDs). Moreover, the device exhibits exceptional response speed, with rise time (τ_{Rise}) and fall time (τ_{Fall}) of 205 µs and 200 µs, respectively, and it maintains stable detection performance while offering excellent mechanical flexibility.

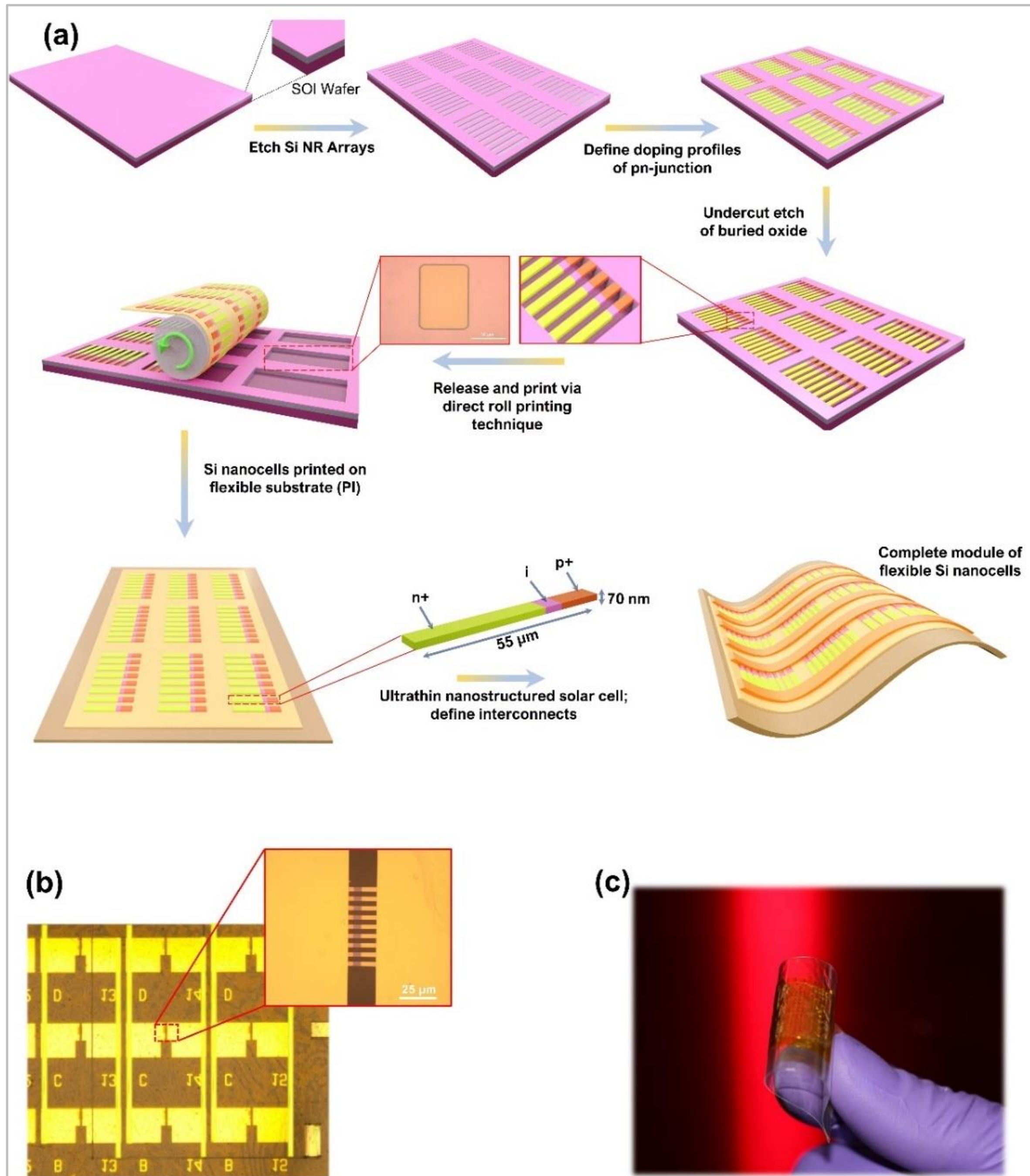


Figure 6.1: Schematic representation and optical images of key steps performed in the fabrication of flexible nanostructured silicon solar cell that incorporate array of integrated nanoribbons using direct roll transfer printing. **(a)** Key fabrication steps for obtaining flexible ultrathin solar cells from SOI wafer by direct roll transfer printing of array of nanoribbons. **(b)** An optical microscope image of identical photodiodes/cells connected in parallel, the electrical contact (Ti/Au) of each cell formed by e-beam evaporation, followed by printing the interconnection lines (silver (Ag) nano paste, width ~5 µm, thickness ~2µm) between the cells using an extrusion-based direct ink writing (DIW). The inset shows an optical image of a single Si based p-i-n solar cell based on printed Si NRs on PI substrate. **(c)** A photograph of flexible solar array realised on flexible substrate.

6.1.1 Basic operating principles of p-i-n solar cell

In general, the solar cells can be regarded as sunlight to electricity converter. One of the most important elements of a solar cell is the semiconducting material or light absorber layer that can sufficiently absorb photons from the incident sunlight to excite the electrons to higher energies. This accelerates them from the valence band to the conduction band, leaving the positive charge carriers i.e., holes behind. The separation of the charge carriers must diffuse in the opposite direction where the charge concentration is low to prevent electron and hole recombination. From material prospective, high quality silicon remains the material of choice, especially when it comes to releasing applications that rely on light for electricity conversion because of its abundance, non-toxicity, high and stable energy conversion efficiency [311], this due to its sunlight-wavelength suited bandgap (1.12 eV). In other words, photons with energy higher than >1.12 eV the absorber's bandgap (Si) can employ their energy to generate electron-hole pairs, hence generated carriers can be extracted from the solar cell. That leads to achieving solar energy conversion as illustrated in figure 6.2. Generally, the most frequent structure of solar cell structure is used with p-i-n junction semiconductor, since the internal electric field present in the depletion region formed in undoped or intrinsic region contribute toward electron-hole pairs separation and hence increase the output current. Furthermore, the larger depletion layer, the greater the amount of light absorption. On the other hand, to reach a higher internal electric field, a smaller depletion layer is needed. Thus, the size of the depletion region is a trade-off between photo response speed and photosensitivity, since it has to be sufficient to allow the largest possible number of photons to be injected in the intrinsic region, and small enough to reduce the transit time of the generated carriers [318, 319]. The structures of p-i-n junction based solar cell are developed by defining an undoped or intrinsic region between 'i' between highly doped n- and p-type regions, ideally the intrinsic region has very low charge carrier concentration, i.e., in order of 10^{10} cm^{-3}. The n-type and p-type doping regions are formed by doping the material such as Si with phosphorus (P) or boron (B) respectively. The basic structure of p-i-n solar cells is schematically illustrated in figure 6.2.

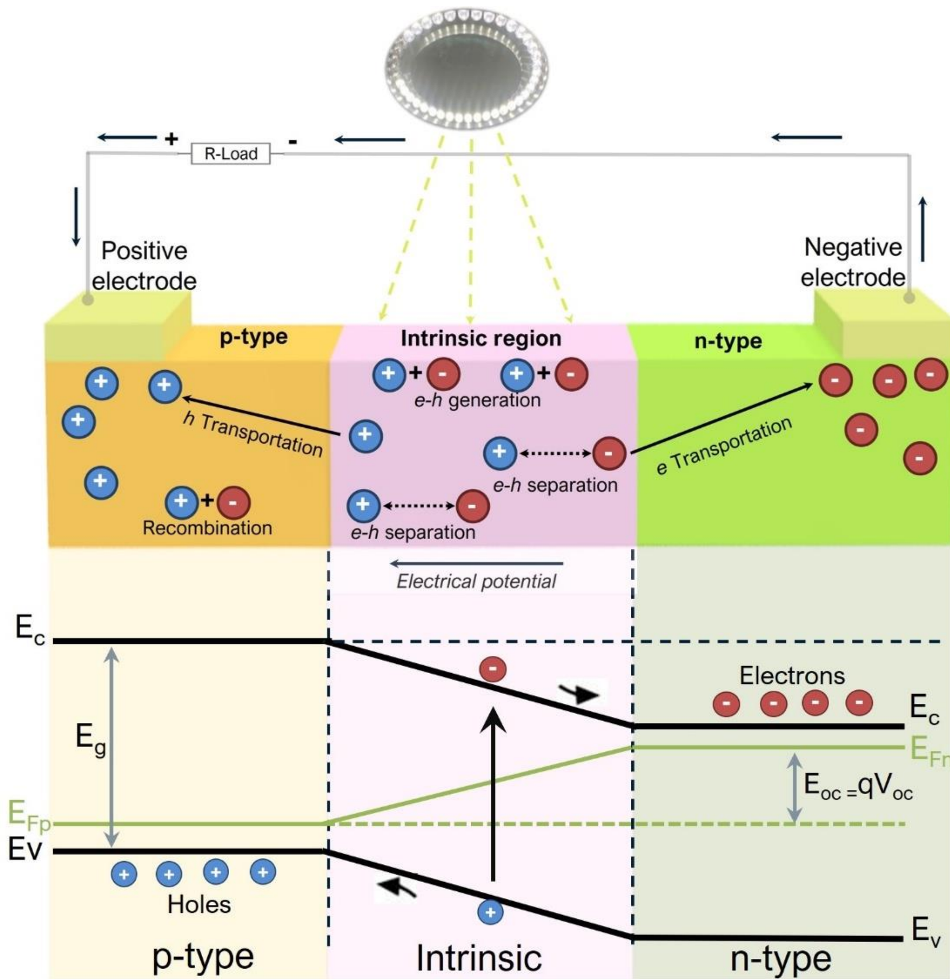


Figure 6.2: Schematic illustration of the working principles of p-i-n junction solar cell for converting light photons to electricity. Energy band diagram and charge flow at the p-i-n junction.

As mentioned in previous section, forming the doping profiles to create p-n junction is a highly important step when it comes to solar cell fabrication, since it allows the internal electric field to be performed and drives the device which facilitates the separation of the photogenerated electron-hole pairs and drive these carriers to the respective electrodes for photocurrent generation even in absence of external bias. During the light radiation as demonstrated in Fig. 6.2, the presence of the internal electric field within depletion region facilitates the separation of the charge carriers (electron-hole pairs). However, in case if the separation between the generated charge carriers didn't take place in a relatively short time, the charge carrier will be annihilated and that's what is called recombination, and hence the light to electricity conversion cannot be achieved. During the existence of the electric field, the charge carriers with opposite polarities are drifted in opposite directions toward

the metal contacts of the solar cell device. Thus, electricity is generated. However, the solar cell cannot convert the light into electricity if the light photon's energy is less than the energy band gap of the active material of the solar cell device. Moreover, there are other factors that may contribute significantly toward energy loss such as reflection/non-absorption, metal contact-ohmic loss, recombination, etc.

6.1.2 Key Performance Parameters

The performance of a solar cell is typically evaluated by the energy conversion efficiency (η), which corresponds to the percentage of incident optical energy that is converted to electrical energy. This parameter is critical to determine the performance of solar cell device, and it can be defined by the ratio of maximum electrical output power (P_{Max}), measured in in (W/cm^2) divided by the product of the input power of incident light (P_{in}) measured in W/cm^2 at the surface area of the cell.

$$\eta = \frac{P_{Max}}{P_{in}} = \frac{J_m \times V_m}{P_{in}} = \frac{J_{SC} \times V_{OC} \times FF}{P_{in}} \quad (6.1)$$

The conversion efficiency is related by J_{sc}, V_{oc}, and FF. Where the P_{Max} is determined by the product of J_{SC}, V_{OC}, and FF. Where J_{SC} is equal to short circuit current or photo-generated current density, and it's defined as the current that flows through external circuity when the applied voltage across the solar device is zero (i.e., when the solar cell is short circuited). J_m is current density at which the maximum power generated by solar cell, V_{OC} is expressed as open-circuit voltage, the voltage at which no current flow through the external circuit, V_m is the applied voltage which gives the maximum power generated by solar cell. FF is the fill factor and is an essential parameter that determines the quality of a solar cells. In other words, FF represents the ability to produce charge carriers that are photogenerated by incident light irradiation absorbed inside the solar cell. FF can be extracted from J-V characteristic demonstrated in figure 6.3. It's defined by the ration between the maximum generated power by a solar cell P_{Max} and the product of short circuit current and open circuit voltage.

$$FF = \frac{p_{Max}}{J_{SC} \times V_{OC}} = \frac{J_m \times V_m}{J_{SC} \times V_{OC}} \quad (6.2)$$

The main parameters that are utilised to characterize the performance of Si NRs solar cells can be determined form the illuminated J-V characteristic, as shown in figure 6.3. The conversion efficiency η is extracted from these parameters, fill factor, peak power, etc. Since the Si NR solar cell with p-i-n junctions, corresponds to I-V diode characteristics, The total current derived from the solar cell is the superposition of the photodiode current in the dark with current generated under light illumination. The equation of the total current of solar cell can be extracted from the diode equations, as follows:

$$J_{total} = J_{ph} - J_{dark} \quad (6.3)$$

$$J_{dark} = J_0 \left[e^{\frac{qV}{nKT}} - 1 \right] \quad (6.4)$$

$$J_{total} = J_{ph} - J_0 \left[e^{\frac{qV}{nKT}} - 1 \right] \quad (6.5)$$

$$J_{SC} = J_{Total} \Big|_{V=0} = J_{ph} \quad (6.6)$$

Where, J_{total} is the total current density, J_{ph} is photo-generated current density, J_{dark} is the current density of the solar cell diode in the dark, J_0 is the diode leakage current density in the absent of illumination. q is absolute value of electron charge, V is voltage applied across the diode, n is the diode ideality factor, K is boltzmann's constant, and T is absolute temperature (K). The open circuit voltage V_{OC}, can be extracted from equation 6.5, considering the total current flows through solar cell diode is equal to zero, therefore V_{OC} can be calculated as follows:

$$V_{OC} = V \Big|_{J_{total}=0} \quad (6.7)$$

$$V_{OC} = \frac{nKT}{q} \mathrm{In} \left(\frac{J_{ph}}{J_0} + 1 \right) \quad (6.8)$$

Similarly, the short circuit current density (J_{SC}) can be extracted from equation 6.5, by considering the voltage generated is equal to zero as:

$$J_{SC} = J_{Total} \Big|_{V=0} = J_{ph} \quad (6.9)$$

So, ideally, J_{SC} is equal to the photogenerated current density.

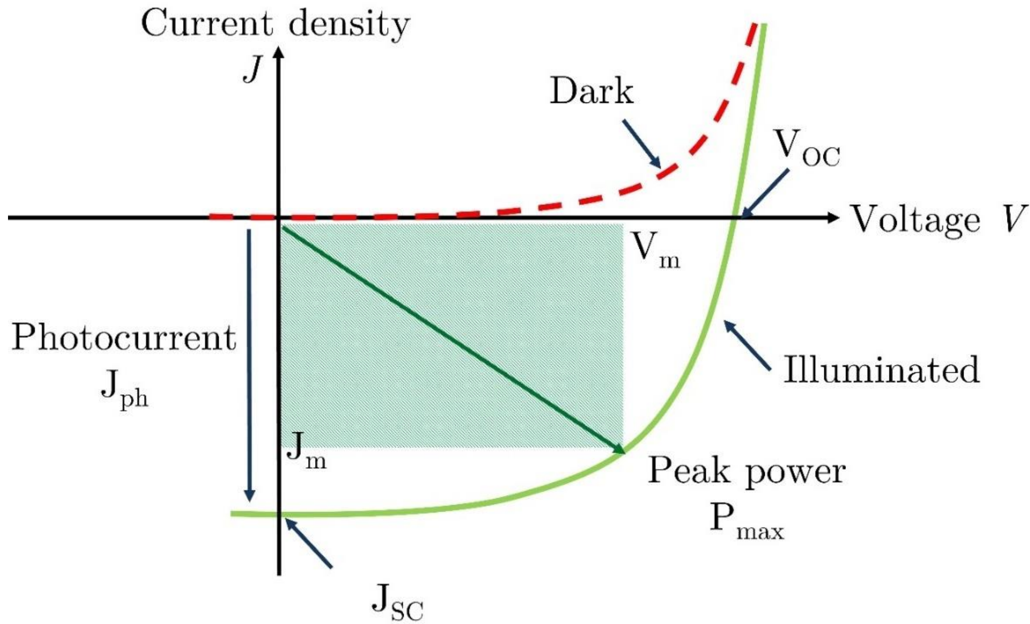


Figure 6.3: Typical current density-voltage (J-V) characteristics of solar cell measured in dark and under illumination.

6.2 **Experimental methods**

6.2.1 Fabrication of p-i-n Si NRs structures

The fabrication process of Si NRs solar cells is fully compatible with the process used to realize flexible Si NRFETs, which was presented in chapter 4. The Si NR solar cell is realized with a p-i-n structure, where the intrinsic region 'i' is lightly p-type doped due to unintentional doping from the source wafer. The SOI sample used for device fabrication consists of a lightly doped p-type Si layer with a resistivity of 10-15Ωcm, corresponding to a boron doping level of ~1×10^{16} cm^{-3}, which is consistent with a previous study [320]. Highly doped n^+ and p^+ regions are formed in designated locations defined by doping mask deposition, photolithography, selective etching, and doping using a thermal diffusion process [39]. The same design geometries of Si NRs array are selected to fabricate p-i-n Si NRs structure arrays, using SOI wafer with 70nm thick single crystalline Si on top. Each cell of Si NRs is composed of 9 NRs with 5um spacing between the ribbons (The dimension of each single NR is 5um width and 55um length). The device design and architecture of single Si

NR solar array is schematically shown in Appendix, figure 8.8. The initial fabrication steps of defining the 32 cells of Si NRs were carried out in a similar fashion to those for the Si NRs FET described previously [52, 58], except both n- and p-type doping steps were performed. The array of Si NRs was patterned by reactive ion etching (RIE) with CHF_3/O_2 with a gas flow of 50/5 sccm for 5 min. To form the doping regions, a SiO_2 layer with a thickness of 250 nm is deposited by plasma-enhanced chemical vapor deposition (PECVD) and utilised as a doping mask. Reactive ion etching (RIE) using CHF_3/O_2, with a gas flow of 50/5 sccm, RF Power: 150 W, Pressure: 55 mTorr. is performed for etching PECVD SiO_2 to create a selective area for dopant diffusion. Next, the selective doping step is achieved by thermal diffusion of solid-state phosphorus (n+) and boron (p+) diffusant source materials. The n-type doping step is processed using a phosphorus-based spin-on dopant (P509, Filmtronics). The doping mask and dopant residues are etched away by concentrated 48% hydrofluoric acid. Similarly, the mask formation for p-type doping is carried out by duplicating the process of SiO_2 deposition used for n-type doping, and the selective p-type doping is based on spin-on dopant (B202, Filmtronics). The spacing between the n-type doped region and p-type doped region is defined by lightly p-type doped region and has a length of 7 µm. After performing both types of doping processes, the rectifying p-n junctions are created through patterned diffusion barriers of SiO_2. The patterning step of Si NRs array was performed selectively and that contributes toward defining the ribbon geometries as well as the anchor points. These are very critical factors that contribute significantly towards completing the printing step successfully with the desired transfer yield. Thereafter, the 2 µm thick exposed buried oxide layer on the source SOI wafer as shown in figure 6.1a was etched using concentrated hydrofluoric solution (49%). The etching time was carefully chosen to be approximately 4 minutes to obtain a releasable form of the Si NR structures with delicate anchors at both ends. This step was based on my previous results. After the releasing step using an HF solution, as shown in Figure 6.4(a-b), it was observed that the etching rate of buried oxide regions beneath p-type doped Si nanoribbons was slightly higher than for oxide under p-type doped regions. Therefore, greater control over the etching rate was required to prevent cracks on the ribbon structures due to the presence of a thin layer

of oxide. If the buried oxide was not completely etched, cracks could occur, as demonstrated in Figure 6.4(a, b), or the ribbons could float away after fully undercut etching of the SiO_2, as shown in Figure 6.4(c, d). To prevent these issues, the etchant solution was further diluted to allow greater controllability over the undercut etching rate of buried oxide. This resulted in satisfactory transfer yield without introducing any cracks in the printed structures after the transfer printing process.

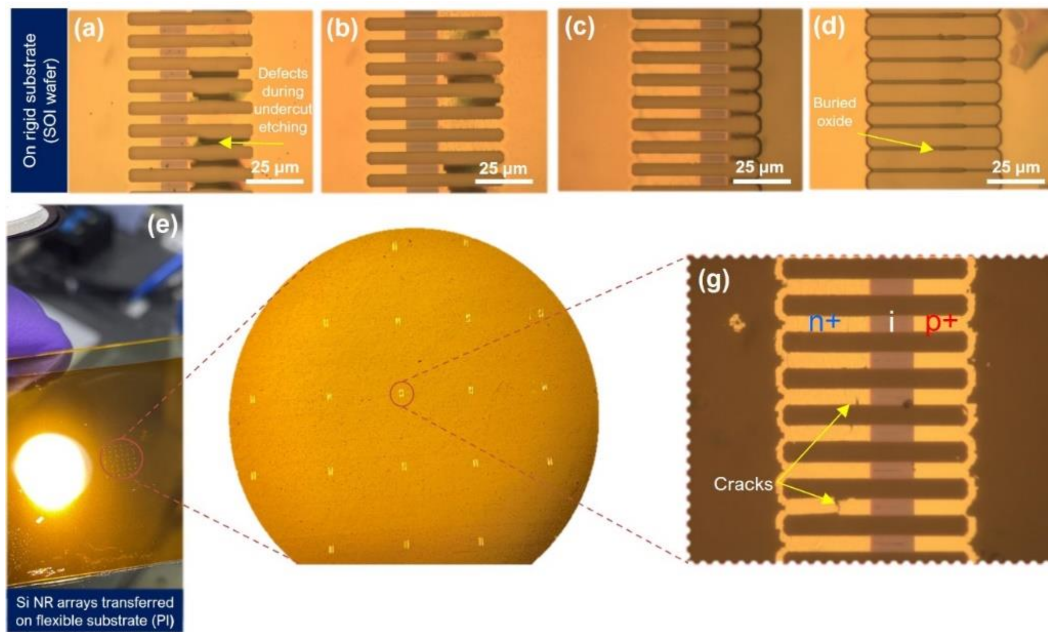


Figure 6.4: Optical microscope images of nanoscale p-i-n based Si NR arrays showing the defect introduced during releasing step. **(a-d)** show the fabricated Si NR array on the rigid source wafer with the representation of the introducing defects such as cracks, NRs floating in etchant solution during the undercut etching of buried oxide prior to the transfer printing process. **(e-g)** Si NR arrays transferred onto flexible substrate by rolling based transfer printing approach. **(e)** Image of large area printed Si NR arrays on flexible substrate (PI) realised from 1.2×1.2 cm^2 chip from silicon-on-insulator wafer. **(g)** magnified optical microscope image of the printed single array of Si NRs, showing the corresponding defects and cracks presented on printed Si nanoribbon array.

After optimizing the etching conditions, p-i-n Si NR structures were printed directly on a flexible substrate using DRTP technique, resulting in a successful and defect-free transfer yield. Figure 6.5(a, b) shows the optical image of selectively doped Si NR arrays, including a magnified view of a single array of p-i-n Si NR structure, recorded prior to transfer printing. Ultrathin NR arrays were released by anisotropic wet etching and transferred onto a PI substrate via rolling-based direct transfer printing, as illustrated in Figure 6.5(c), with

the doping layout of Si NR arrays based solar cell shown in Figure 6.5(d). The ribbons were printed directly in a single step, with high transfer yield and perfect registration accuracy, without any defects, demonstrating the versatility of direct roll transfer printing, as shown in Figure 6.5(e, f). Figure 6.5e shows a photograph of large area integration of a selectively doped Si NR array structured with p-i-n junctions printed on a PI substrate. The solar cell was designed by connecting arrays of NRs in parallel to form the interconnects using direct ink writing (DIW), allowing for large-scale integration of nanostructured ribbon arrays without introducing any cracks in the solar module.

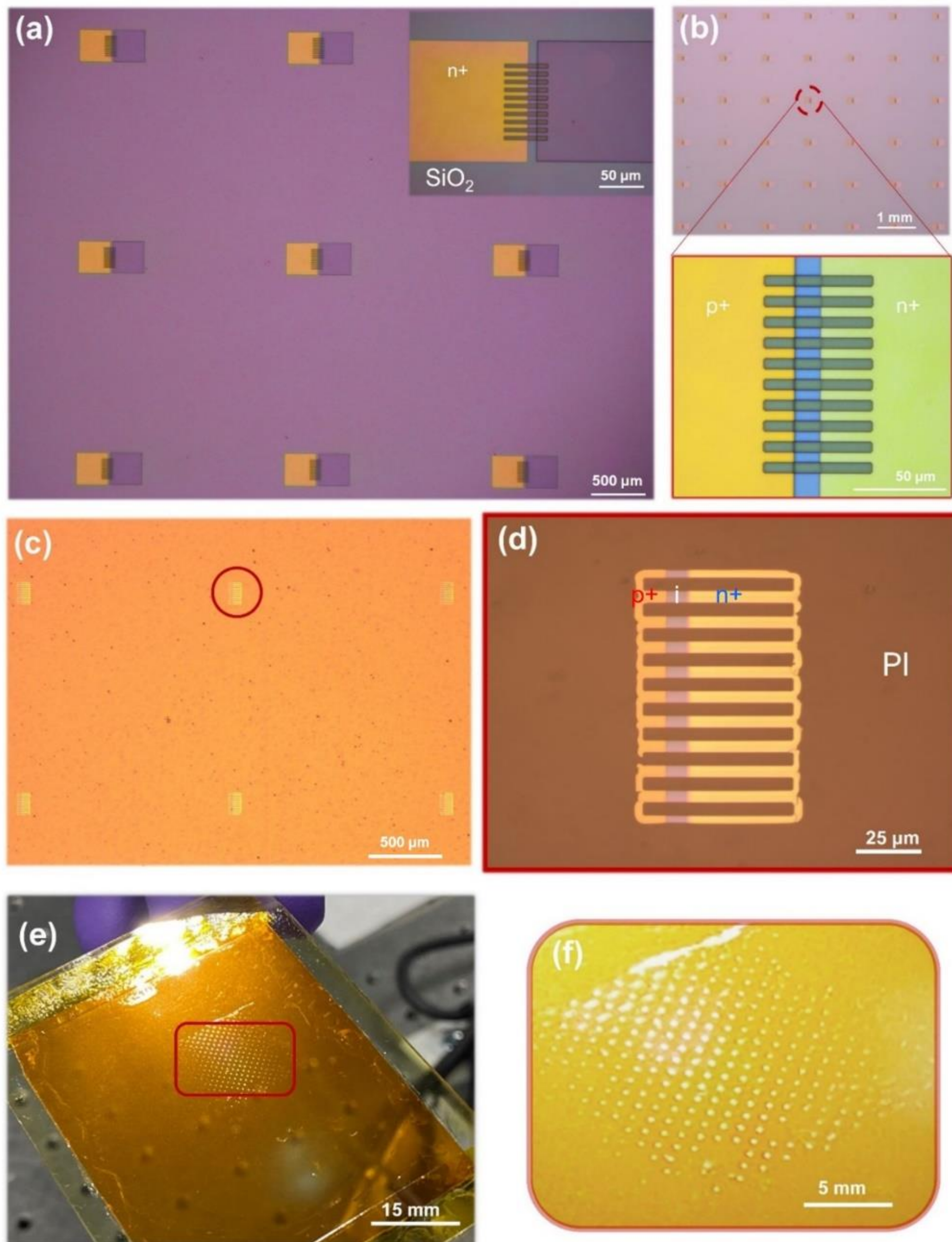


Figure 6.5: **(a)** Optical microscope image of the Si NR arrays fabricated on SOI wafer after performing a selective n-type doping via thermal diffusion process using PECVD deposited SiO_2 layer as diffusant doping mask. **(b)** Fabricated Si NR arrays based on p-i-n structures, the magnified image shows the Si NR arrays realised based on p-i-n regions after defining both doping profiles; n- and p-type. **(c)** printed p-i-n nanostructured Si cells on flexible substrate (PI) achieved by direct roll transfer printing approach. **(d)** optical image with magnified view of printed single cell, with highlighting the doping profiles of lateral p-i-n Si NRs structure. **(e)** Optical microscope image of nanostructured Si NR arrays transferred on PI substrate over 1.2 × 1.2 cm^2 area. **(f)** Optical image with magnified view.

6.2.2 Direct roll transfer printing

The direct roll transfer printing system was utilized to transfer the well-defined arrays of ultrathin Si NRs having lateral p-i-n structures from SOI wafer onto flexible PI substrate. The DRTP was employed to transfer the released p-i-n Si NRs photodiodes in a single step on PI substrate. Thus, high-performance printing with excellent transfer yield and high registration accuracy with defect free have been achieved. The critical steps of integrating the Si NR arrays on flexible substrate via DRTP process have been already elaborated in our previous work [52, 57]. Importantly, the attained Si NR arrays can be printed directly on multiple flexible substrates [52]. These include PET, transparent PI, glass, etc. such substrates can be used to achieve efficient transparent self-powered sensing elements as well as solar energy harvester for indoor applications, subsequently, which demonstrate promising prospective of Si NRs for future smart solar cell devices.

6.2.3 Electrode fabrication

The electrical contact pads ($300 \times 300 \mu m^2$) of titanium (10 nm) and gold (100 nm) were deposited on the transferred Si NR based devices array using a lift off process based on photolithographic patterning and followed by depositing the desired metals via electron-beam evaporator.

6.2.4 Printed interconnects for solar array

The extrusion-based direct ink writing (DIW) Delta Printing System (from XTPL) was utilized here to print the high-resolution interconnects. The nozzle adopted in this work has an opening size of 3.5 µm. The printing angle between the nozzle and substrate was set at 50°. The main parameters that have been optimized and applied in this work to print the interconnects are pressure (~8 bars) and velocity (~0.02 mm/s). Following this the conductive silver (Ag) nano-paste, XTPL CL85 (viscosity ≥100,000cP, metal content = 82 wt.%), was printed to obtain the interconnects. The parallel connection was realized between the printed Si NRs based solar cell arrays by depositing the metal contacts (Ti/Au) on the Si photodiodes as shown in Fig.1d. The conductivity of the printed interconnects was improved by annealing at 150 °C for 15 min.

6.2.5 Electrical characterisation

Light and dark *I-V* characterisations of printed Si NRs solar cell on flexible PI substrate were performed in an ambient environment using Cascade Micro-tech Auto-guard probe station interfaced to a semiconductor parameter analyser (B1500A, Agilent). The nanostructured solar array sample was tested under white LED illumination in ambient conditions at room temperature. The light intensity was measured in Lux via Pro RS-3809 Light Meter and calibrated on the basis of bright sunlight (1 sun equal to 120,000 Lux) which gives an equivalent value of light intensity around 100 mW/cm^2 [321]. The device measurement carried out in the illumination intensity range 900-3000 Lux at room temperature.

6.3 Results and Discussion

6.3.1 Solar cell array characterization

We demonstrated a nanostructured Si NR arrays based solar cell using direct roll transfer printing. The nanoscale solar cell utilises Silicon NR arrays realised with p-i-n junction prefabricated by selective doping using spin on dopant (SOD) process. Further, an array is formed by connecting 32 p-i-n photodiodes/cells in parallel configuration to enhance the output current. Each cell has 9 NRs, configured with p-intrinsic (i, unintentionally doped)-n (p-i-n) solar cell, which has a surface area of ~315 µm^2. The interconnects between NR devices (solar cells) are formed using an extrusion-based direct ink writing (DIW) printer, XTPL, lead to solar array. The flexible nanostructured solar cell was tested under illumination of white LED in ambient conditions at room temperature. The light intensity was measured in Lux via Pro RS-3809 Light Meter and calibrated on the basis of bright sunlight (1 sun equal to 120,000 Lux) which gives an equivalent value of light intensity around 100 mW/cm^2 [321]. The current-voltage measurement of nanostructured solar cells was carried out in the dark, then followed by measuring the devices under illumination intensity of 300 µW/cm^2 at room temperature. Figure 6.6a represents an equivalent electrical circuit layout of a solar cell module based on multiple devices, the devices configured in parallel to enhance their photocurrent generation [322]. The corresponding

current-voltage (I-V) curve recorded from Si NRs based solar array, represents photodiode characteristics in the dark and under illumination of 900lux, with forward bias condition, the applied bias voltage carried out from -10V till 10V (Figure 6.6b). Figure 6.6c demonstrates the corresponding semi-log plot of the dark current-voltage characteristics (I-V). The linear fit illustrates the diode ideality factor (n) of ~2.23 at room temperature, this value was extracted from Eq. 6.5, and it was found to be close to a typical value (n ~ 2) for commercial planar Si p-i-n diode [323].

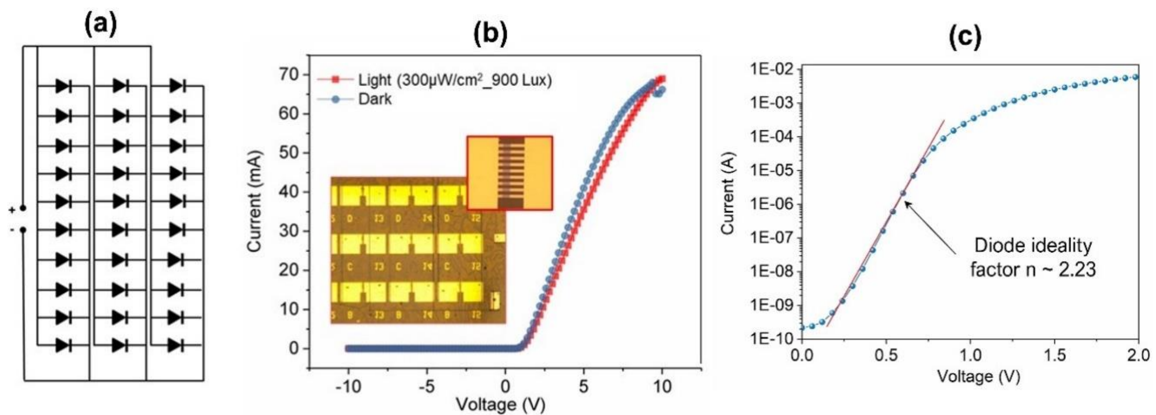


Figure 6.6: **(a)** Equivalent electrical circuit of a solar cell module based on multiple cells (32 cells connected in parallel configuration). **(b)** resultant current-voltage (*I-V*) characteristic of a p-i-n junction Si NRs solar cell (linear plot) and optical image of nanostructured solar cell module in an arrays of Si NRs nano-cells integrated on polyamide substrate via direct roll transfer printing. Inset represent a magnified optical image of a single device, the electrical contact pads were formed by lithography and evaporation of metals (Ti/Au: 10nm/100nm). **(c)** Corresponding semilog curve of dark-current (I-V) characteristics of Si NRs solar cells. The linear fit corresponds to a diode ideality factor (n) of ~2.23.

Obtaining the current density-voltage (*J-V*) characteristics of a solar cell is critical in extracting the important parameters such as short circuit current density J_{SC}, open circuit voltage V_{OC}, power density, fill factor FF, etc. These parameters determine the device's output performance such as maximum harvested power P_{max} and output efficiency η, etc. The corresponding optoelectrical response of direct roll printed Si NRs solar cell have been investigated, as illustrated in Fig. 6.7. The current density versus voltage (*J-V*) characteristics of 32 devices connected in parallel is shown in figure 6.7a at different illumination intensities, each device consists of a single array of printed p-i-n nanoribbons as shown in figure 6.6b. Through evaluating the device performance parameters under

illumination condition of 3000 lux. It can be found that, the open circuit voltage (V_{oc}), short circuit current density (J_{SC}), fill factor (FF) and overall energy conversion efficiency (η) are 0.252 V, 78.57 µWcm^{-2}, 57.34% and 1.34%, respectively. The calculations dependent on the device surface area, considering one dimensional structure of single cell consists of 9 nanoribbons. Whereas the physical separation between n^+ and p^+ represents the intrinsic (i-region), and that determines the channel length and width of 7 µm and 5µm respectively of a single ribbon. The I-V measurements of the solar cell devices are recorded under different light illumination intensities, ranging from 900 lux to 3000 lux. Figure 6.7b shows the dependence of open circuit voltage V_{OC} and short circuit photocurrent density J_{SC} on the illumination intensities. The I-V characteristic curves obtained from printed nanostructured Si solar cell arrays demonstrate a slight increase with increasing light intensities. Furthermore, it is clear that photocurrent density J_{SC} is highly dependent on the illumination intensity level. Although the J_{SC} for the Si NRs solar cells was 20.25 µA/cm^2 for illumination of 900 lux. This value increases around four times under illumination intensity of 3000 lux to be 78.57 µA/cm^2. That shows the short current generation increases linearly with increasing the illumination intensity. A similar result has been theoretically and experimentally proved by several reported works based on flexible Si solar cell devices [288]. These illuminated electrical characteristics determine the main parameters that indicate the solar energy conversion ability and efficiency under varied illuminance intensities with respect to the corresponding light source power. The dependence of the output power density on illumination intensity has been investigated. The extracted output power-voltage characteristics of printed Si nanostructured solar cell under varied illumination conditions are illustrated in figure 6.7c. The maximum power density of printed Si NRs solar cells for illumination intensity of 900 lux was only 1.77 µW/cm^2. Increasing the illumination intensity to 3000 lux leads to an increase of the output power by 82.5% to reach a value of 10.14 µW/cm^2.

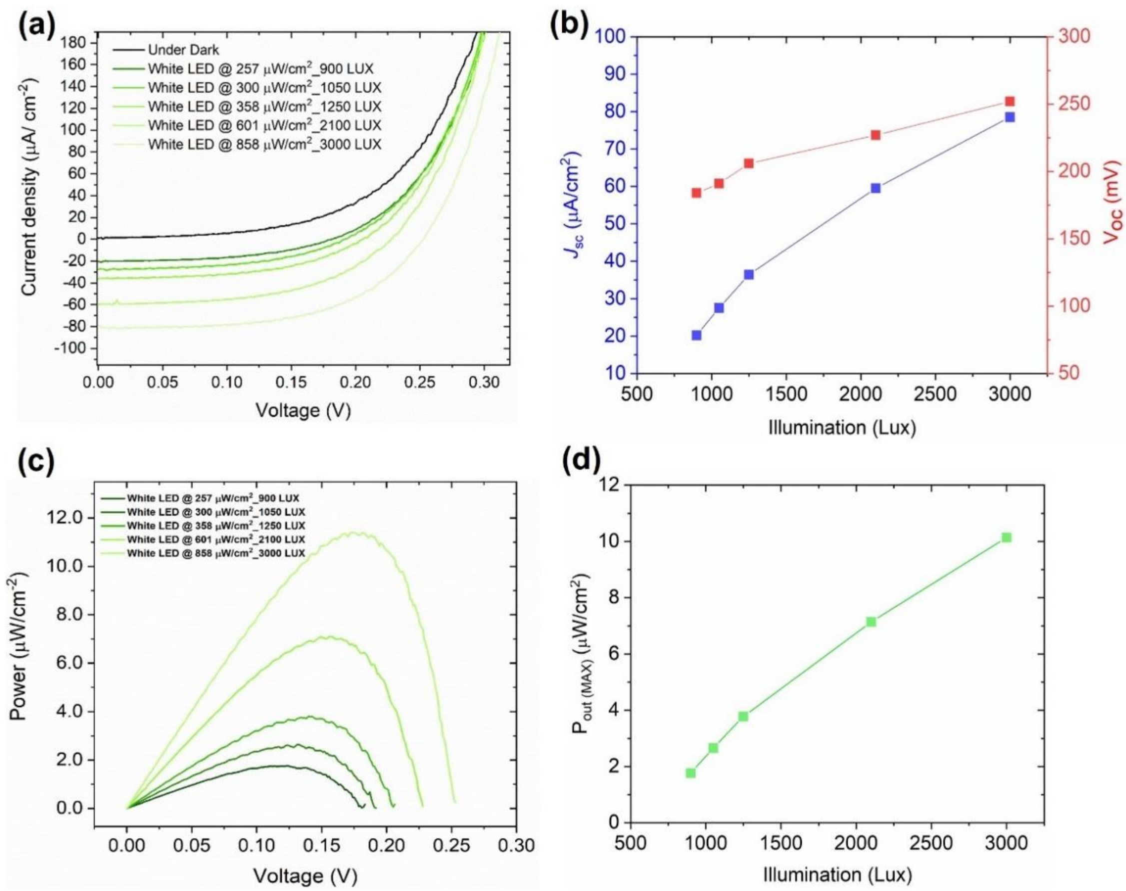


Figure 6.7: performance characteristics of Si NRs solar cells **(a)** Current density-voltage characteristics of Si nanoribbons based solar cells operated under different light illumination intensities. **(b)** Illumination intensity dependency of short current density J_{SC} and open circuit voltage V_{OC}. **(c)** the output power generated by solar cell versus applied bias voltage *(I-V)* curve under different light illumination intensities. **(d)** light intensity dependency of power conversion efficiency (PCE) of printed Si NRs solar cell.

Solar cell efficiency is an essential characteristic that determines the performance related to energy conversion efficiency of solar cells. The conversion efficiency of the fabricated nanoscale Si NRs based solar cell devices is calculated using the equation (6.1). The dependence of efficiency on light intensities is shown in figure 6.8a. It has been found that the efficiency of printed Si NRs solar cells indicated around 50% increase by increasing the optical illumination intensity from 900 lux to 3000 lux. The maximum peak efficiency ~1.5% was recorded under light illumination of 3000 lux. The dependence of the fill factor on illumination intensity is shown in figure 6.8b.

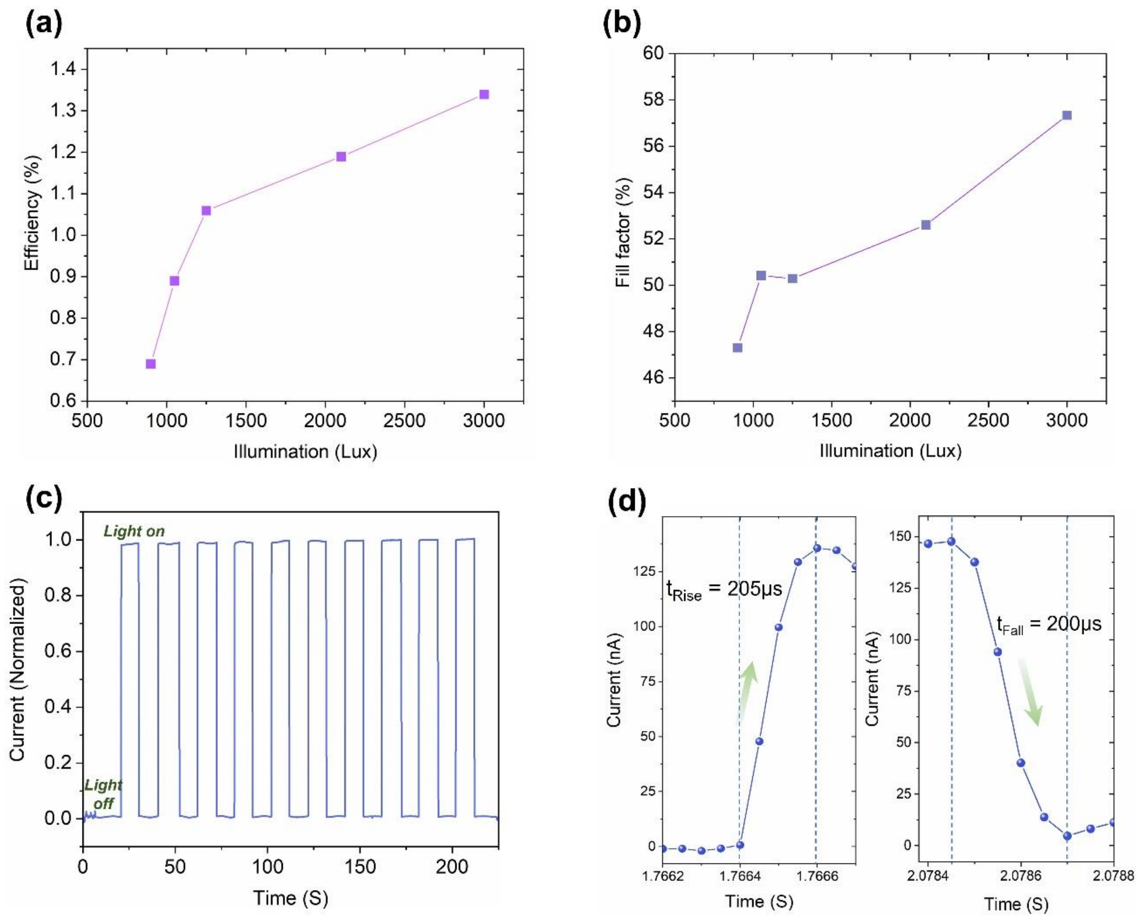


Figure 6.8: Light illumination dependent of printed Si NRs solar cells parameters: **(a)** power conversion efficiency PCE (%). **(b)** fill factor FF. **(c)** normalized photocurrent response of Si NRs solar cells during light on-off cycles, short-circuit current versus time curve obtained at 0V, light intensity ~1050 lux. **(d)** a high-resolution photocurrent response under 1050 lux light intensity at 0V to illustrate the obtained rise and decay time ~ 200µs.

The fill factor is one of the performance parameters that measures the quality of the solar cell, and it can be expressed by equation (6.2). It is clear that the fill factor of Si NR solar cells was shown to increase linearly, as a function of the illumination intensity. The response time is another critical parameter in a photodetector (PD), representing the device's ability to perform switching in response to transient optical signals. The photocurrent generation of printed Si solar array has been investigated during light on-off cycles. The rapid switching behavior of the fabricated device when biased at 0 V is demonstrated in Figure 6.8c. Ten cycles have been applied using white LED as a light source with a constant illumination intensity of ~1050 lux. In the tenth cycle, the maximum photocurrent is stabilised to 100% of the initial maximum photocurrent. Within 225 s, the generated photocurrent I_{sc} of Si

NRs solar cell demonstrate remarkable reproducibility during on and off cycles, with quick response and recovery characteristics. A detailed examination of a single on/off cycle, as depicted in Figure 6.8d, reveals rise and fall times of 205 μs and 200 μs, respectively. This flexible Si NRs PD exhibits superior photoresponse in comparison to previously reported flexible PDs based on 2D materials [324].

The extracted values of Si NRs solar array are comparable with other Si solar cells fabricated based on ultrathin silicon structures. It's to be noted that the thickness structures of Si NRs selected in this work is much thinner than other reported lateral Si structures, which confirms that the thickness has a significant influence on the device performance. For example, absorption enhancements and output efficiency, thus reducing the thickness of silicon can be considered as a potential route toward achieving cost effectiveness and enhancing the flexibility of Si solar cells. It can also lead to degradation of their performance, which is attributed to weak optical absorption [325]. Several methods have been implemented to enhance the cost-effectiveness and optimize the optical absorption of solar spectra in Si thin-structured devices, while preserving their performance, as discussed in reference [326]. In the case of inorganic solar cells, several factors contribute significantly to enhancing device performance and increasing energy conversion efficiency. These factors include the active material's thickness, light-trapping structures, surface texturization, surface passivation layers, antireflection coatings, and others. Each of these factors exhibits a significant potential for improving the device's optical absorption and overall performance, as indicated in reference [309]. To have a close view of the previously reported work of ultrathin Si structures based solar cells with respect to Si NRs solar cells, the device related parameters are summarized in table 6.2. Typically, the efficiency of energy conversion is increasing with light intensity[288]. Compared to other reposted works [306, 309, 311], unlike other Si solar cells, the Si NRs solar array was subjected to evaluation under low light intensity (0.85 mW/cm^{-2}), thereby demonstrating its potential for deployment in indoor applications. Table 6.3 displays the parameters extracted for the performance of Si NRs solar cells under varied light intensities (from 900 lux to 3000 lux).

Table 6.2: Performance properties of flexible ultrathin Si solar cell with various reported transfer printing techniques.

Device structures/ Si structure morphology	Transfer printing process	Light source	P_{in} (mW/cm²)	J_{SC} (mA/cm²)	V_{OC} [V]	Fill Factor FF [%]	Efficiency PCE [%]	Ref
µSi cells array (15µm Thick) on PET	Conventional transfer printing	AM 1.5G	100	23.6	0.50	61	7.2	[309]
µSi cells (~8 µm Thick) on PET	Conventional transfer printing	AM 1.5G	100	16.64	0.44	67	5.06	[311]
Si-pellets array (1.25 µm Thick) on hemispherical PDMS	Additive stamp (CAS) printing	AM 1.5G	100	14.46	0.35	50.39	2.56	[306]
Si-NRs array (70nm Thick) on PI	Direct roll transfer printing (DRTP)	White LED	0.85	78.57 µA/cm²	0.25	57.34	1.34	**This work**

Table 6.3: Parameters of Si NRs solar cell performance extracted under varied light intensities, these parameters include, maximum output power $P_{out\,(MAX)}$, incident power P_{in}, short-circuit current density J_{SC}, open-circuit voltage V_{OC}, efficiency η, fill factor FF. The device integration on flexible substrate performed via direct roll transfer printing process.

Light Intensity White LED (Lux)	P_{in} (µW/cm²)	$P_{out\,(MAX)}$ (µW/cm²)	Jsc (µA/cm²)	Voc (mV)	Efficiency η (%)	Fill Factor FF (%)
900	257	1.77	20.25	184	0.69	47.31
1050	300	2.66	27.53	191	0.89	50.42
1250	358	3.78	36.44	206	1.06	50.29
2100	601	7.14	59.52	227	1.19	52.61
3000	858	11.14	78.57	252	1.34	57.34

Regarding the performance of Si solar cell based on thin structures, an investigation was conducted to evaluate the impact of varying thicknesses of microscale Si ribbons, ranging from approximately µ8 to µ45, on efficiency, as reported [309]. The results indicated a significant enhancement in efficiency with increasing thickness, up to µ15, primarily due to increases in optical absorption length [309, 326]. To achieve further improvements in the performance of Si NRs solar cells, it is recommended to increase the thickness of printed Si NRs beyond 70nm, utilize higher density over printed structures, and employ antireflection coating strategies, among other approaches. For instance, the efficiency can be improved remarkably by releasing micro/nanostructures designed for light trapping and minimising optical loss [308], such as nano/micro-pyramid [327], nanocones (NCs) [328], nanopillars [329], spherical nanostructures [330], etc. Advanced light trapping strategies can be

employed to enhance optical absorption, including the utilization of micro pyramid structures or micro texturing approaches, which are the most widely implemented techniques for increasing light trapping and absorption in crystalline silicon solar cells [311, 326]. Nonetheless, the implementation of surface texturing techniques on ultrathin structures with high yield presents challenges, particularly in the nanoscale fabrication of solar cells, where the active material is only several tens or hundreds of nanometres thick [326]. A comparison with previously reported micro silicon solar cell arrays with micro-scale thickness shows that further enhancements can be made to utilize silicon in flexible solar cell devices for high-performance, efficient, and stable futuristic indoor applications. It can be concluded that the fabrication of large-area Si NRs-based solar cell arrays with further structural optimization is a promising area for future research. However, it should be noted that comparing the obtained results for indoor solar cell use with those of different reported cells or modules is challenging due to the lack of standard indoor solar cell measurement practices and the use of non-calibrated lux meters [290].

6.3.2 Photodiode array characterisation for UV and NIR sensing

The photocurrent measurements were conducted using LEDs of various wavelengths, including visible, ultraviolet (UV), and near-infrared (NIR). The recorded photogenerated current at 0 V depended on the intensity of the illumination. This phenomenon can be attributed to the excess photogenerated carriers in the fabricated device, which exhibit a p-i-n Si NRs photodiode's solar cell behavior, thereby allowing the device to operate as a self-powered photodetector. To examine the electrical measurement of photocurrent generation by the fabricated devices, we measured the device at 0 V bias voltage. Given the bandgap of Si (1.12 eV) allows for the generation of visible-UV-NIR light, we investigated the photo sensing response of the fabricated devices for broadband detection by evaluating them under UV ($\lambda = 365$nm) and NIR ($\lambda = 850$nm) illumination. In Figure 6.9(a) and (b), we present the light switching characteristics with respect to photocurrent under different UV and NIR intensities measured at 0 bias voltage. The results indicate that, in both cases, with the step

high of each cycle representing the ON current, an increase in illumination power density led to an increase in photocurrent.

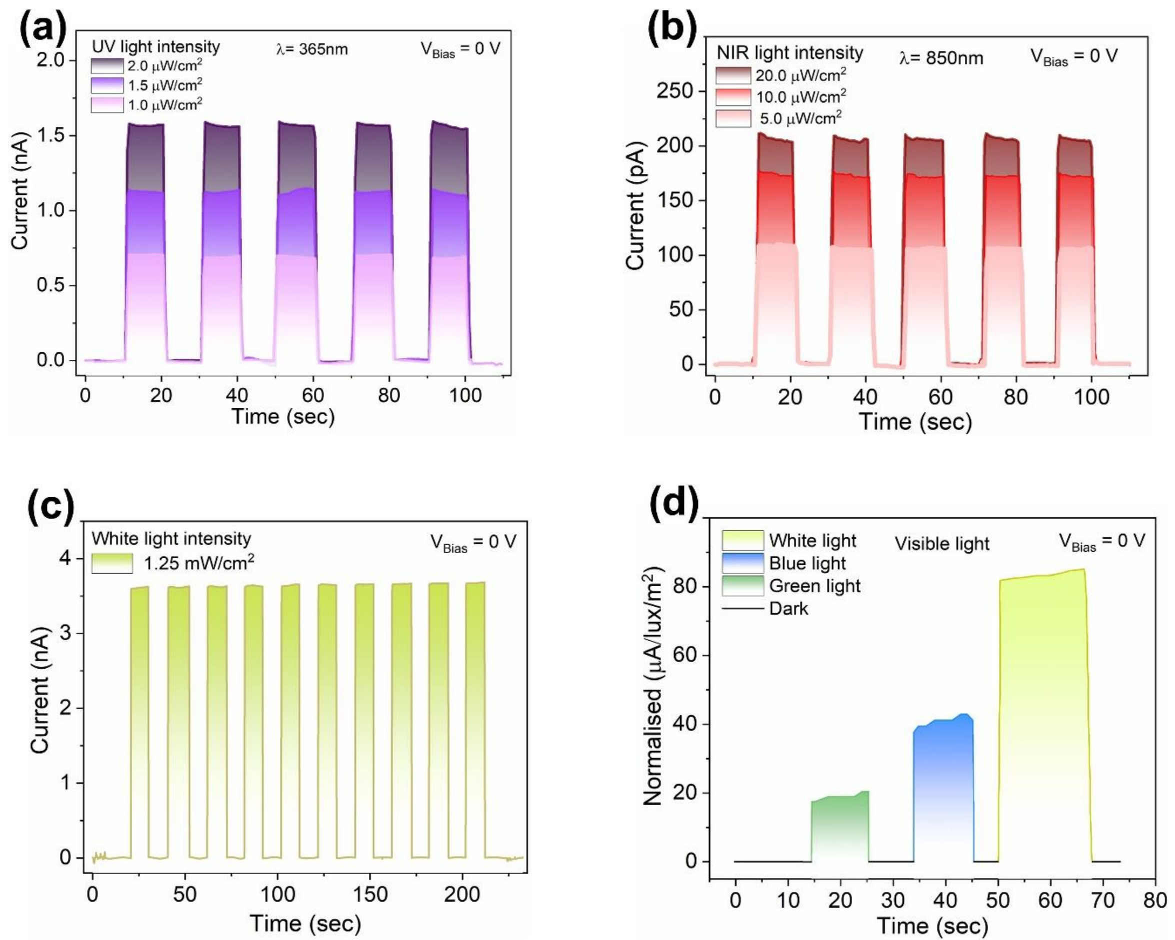


Figure 6.9: **(a)** Photocurrent response of Si NRs photosensor during light on-off cycles under ultraviolet (UV). **(b)** near infrared (NIR) upon illumination at different light intensities. **(c)** Visible light (white LED) switching characteristics. **(d)** Colour detection of visible light (green, blue and white) performed at 0V bias.

It is found that the fabricated device exhibits excellent performance of broadband photoresponse from UV-NIR, with high-speed response, showing the maximum responsivity R ~2.48 A/W achieved under UV at wavelength of 365 nm at zero bias voltage, corresponding to an external quantum efficiency, EQE reaching (8.30×10^{2} %), detectivity D* (2.74×10^{13} jones).

Table 6.4: Illustration of the extracted performance parameter values for the Si NRs photodetector.

UV_Si NRs based PDs_λ= 365nm

Pin μW)cm2	Area (cm2)	Pin*A	Current_Ion @ 0V	Responsivity_ R (A/W)	Current_Idar k@0V	EQE1	R*a^0.5	(2*q*Idark)^0.5	Detectivity_ D (Jones)	on/off
2	3.15E-04	6.30E-04	1.56E-09	2.48E+00	8.03E-12	8.30E+02	4.39E-02	1.6027E-15	2.74E+13	1.94E+02
1.5	3.15E-04	4.73E-04	1.13E-09	2.39E+00	8.03E-12	8.02E+02	4.24E-02	1.6027E-15	2.65E+13	1.41E+02
1	3.15E-04	3.15E-04	7.06E-10	2.24E+00	8.03E-12	7.51E+02	0.039779	1.6027E-15	2.48E+13	8.80E+01

NIR_Si NRs based PDs_λ=850nm

Pin μW/cm2	Area (cm2)	Pin*A	Current_Ion @ 0V	Responsivity_ R (A/W)	Current_Idar k@0V	EQE1	R*a^0.5	(2*q*Idark)^0.5	Detectivity_ D (Jones)	on/off
20	3.15E-04	6.30E-03	2.12E-10	3.37E-02	5.12E-11	4.91E+00	5.97E-04	4.04772E-15	1.48E+11	4.14E+00
10	3.15E-04	0.00315	1.76E-10	5.59E-02	5.12E-11	1.87E+01	9.92E-04	4.04772E-15	2.45E+11	3.44E+00
5	3.15E-04	0.001575	1.11E-10	7.05E-02	5.12E-11	2.36E+01	0.001251	4.04772E-15	3.09E+11	2.17E+00

Si NRs based PDs_Visible (White LED) light

Pin μW/cm2	Area (cm2)	Pin*A	Current_Ion @ 0V	Responsivity_ R (A/W)	Current_Idar k@0V	EQE1	R*a^0.5	(2*q*Idark)^0.5	Detectivity_ D (Jones)	on/off
1250	3.15E-04	3.94E-01	3.65E-09	9.27E-03	7.63E-11	1.35E+00	1.65E-04	4.94125E-15	3.33E+10	4.78E+01

6.3.3 Photodiode array characterisation for visible light colour sensing

The photocurrent generation of printed devices was investigated under visible light utilising white LED as a light source as illustrated in figure 6.9c. Ten on-off cycles were applied with a constant illumination intensity of 1.25 mW/cm^{-2}. In the tenth cycle, the maximum photocurrent stabilised to 100% of the initial maximum photocurrent. Therefore, the presented Si NRs photosensor demonstrates remarkable reproducibility during on and off cycles, with quick response and recovery characteristics under white light illumination. The wider absorption bandwidth and the excellent photoresponse of the fabricated p-i-n photosensor arrays under Visible, UV and white light, displayed in figure 6.9(a-c), suggest the potential use of fabricated device for selective colour detection. To demonstrate this capability, the illumination of visible light was applied separately (green, blue, and white), as shown in Fig. 6.9(d). This measurement was performed using a commercial multicolored LED.

6.3.4 Mechanical stability evaluation of flexible Si NRs solar cell array

Owing to the high flexibility of high-quality ultrathin Si NR arrays integrated by direct roll transfer printing possess great potential for flexible solar cell application. To further investigate the mechanical stability and flexibility of the direct roll printed Si NRs solar cells for flexible applications, the solar array performance of printed Si NRs was evaluated

under cyclic bending conditions at 40 mm radius of curvature; 500 bending cycles were performed as presented in Fig. 6.10a. The solar cell performance parameters of the direct roll printed Si NR solar cells were evaluated under planar, tensile and compressive bending conditions followed by testing the optical response under illumination of 3000lux. The normalised parameters (Voc, Jsc, FF and PCE) after every 100 bending cycles, until 500 cycles have been recorded. The performance parameters evaluation with bending cycles are plotted in figure 6.10(b, c). Although the printed Si NRs based cell was repeatedly bent for 500 cycles, all the value of the solar cell parameter such as J_{SC}, V_{OC}, FF, and efficiency remained relatively stable as shown in Fig. 6.10(b, c). It can be observed that during the cyclic bending process, the V_{OC} of the Si NR solar cells dropped down from 250 mV to 225 mV after applying 100 bending cycles, with slight decrease of ~10% compared to initial value (See Table 6.2). From figure 6.10b, it can be observed that during performing the initial 100 bending cycles, the short circuit current J_{SC} reduced to 18% less compared to the initial value, this slight decrease can be attributed to the increase of the extra series resistance added by the printed interconnects, which ascribed by the nature of stress (tensile or compressive) due to repeated bending deformation [331], while the functionality of the solar cell devices was observed to be unaffected- and stable.

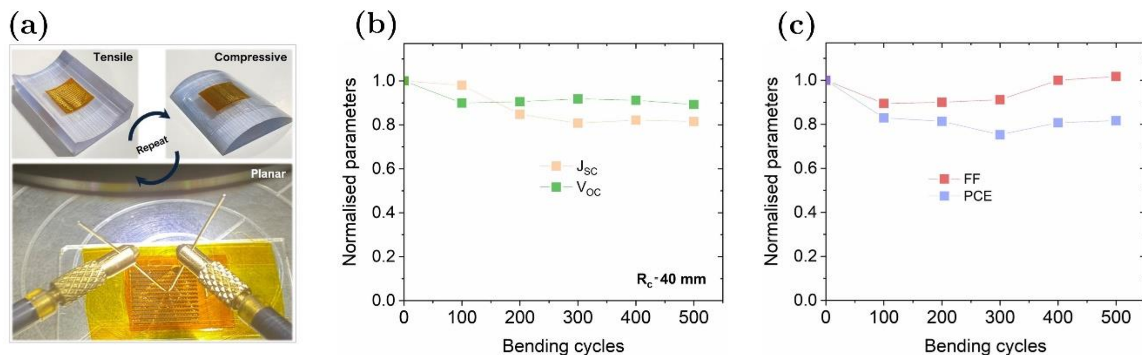


Figure 6.10: Bending stability test of printed devices under 500 bending cycles with radius of 40mm. **(a)** Optical images of solar cell devices during durability test when being under planar and bent conditions. **(b)** Photograph of large area Si NRFETs in PI substrate attached over PVC foil with bent condition. **(c)** normalised values of J_{SC} and V_{OC} **(d)** FF, and PCE as functions of the bending cycle.

The power conversion efficiency (PCE) and fill factor (FF) dependency on bending cycles are presented in figure 6.10c, where PCE of the Si NRs solar cell shows a negligible change

after 400 cycles, demonstrating an excellent flexibility and good stability of the printed device. It can be seen from figure 6.10c, the efficiency decreased during the initial 300 bending cycles, led to a relatively low conversion efficiency loss of ~23% of its initial value (See Table 6.2). However, the small drop in output efficiency of Si NR solar cell can mainly be attributed to the decreased FF during the cyclic bending test. Afterward, the PCE started to increase gradually after 300 bending cycles to some extent, maintaining above 80% of the initial value. While for fill factor (FF) dependence of bending cycles, it can be clearly seen that, the change of FF with bending cycles is almost negligible and remained close to the initial value after performing 500 cycles, keeping 99.5% of its initial value. The results clearly demonstrate the excellent flexibility as well as high durability of solar cell realised by direct roll transfer printing of Si NRs arrays. Overall, we can conclude that the printed Si cell arrays by DRTP process, have been observed to exhibit stable mechanical bending performance during performing 500 bending cycles, where even at 500 bending cycles, the efficiency of printed Si NR cells remains constant, thus the of printed Si cells have been shown an outstanding mechanical stability, since the flexibility factor is critical for advanced flexible application such as energy autonomous e-skin, smart contact lenses, epidermal sensors, and IoT ecosystem, etc [332]. However, the minor performance degradation that has been noted during applying mechanical bending conditions, can be prevented by applying encapsulation over the printed interconnects and performing surface passivation, such a configuration allows high flexibility and stable electrical properties by preventing them from experiencing any strain-induced variations caused during cyclic bending. Moreover, these optimisations will be considered for future work. Additionally, there are several strategies that can be implemented in the future plan, to enhance the light absorption and thereby the overall absorption efficiency, such as increasing the thickness of silicon nanoribbons, employing transparent substrate such as transparent PI, PVC foil, PET, etc. to allow the light absorption from both sides and also incorporation of the surface to increase the light path, such optimisations strategies can significantly contrite toward enhancing the overall performance of printed ultrathin Si solar cell based modules. Thus, the presented integration approach based on DRTP process shows good potential for

realising fully printed self-powered Si NRs based CMOS based electronics on flexible transparent substrate with robust and cost-effective interconnects by printing.

6.4 Conclusion

In summary, we have demonstrated a promising alternative approach for realizing flexible, multifunctional silicon nanorod (Si NR) solar cells. Building upon previous work, we have shown the effectiveness of this technique in developing flexible p-i-n Si photodiode arrays by printing Si NR arrays (~70 nm thick) onto a flexible substrate. The light intensity dependency of the output performance parameters of the Si NR solar cells was experimentally evaluated, and the performance characteristics of the representative Si NR solar cells were compared with indoor flexible solar cell technologies, also compared with respect to those reported in other studies that employed different integration techniques (e.g., conventional transfer printing, additive stamp (CAS) printing, etc.). The photoconductive characteristics of the devices were investigated under different light illuminations, including visible, UV, and NIR. The Si NR photodiode demonstrated a peak responsivity of 2.48 A/W @ 365 nm at zero bias voltage, with an external quantum efficiency (EQE) of $8.30\times10^{2}\%$ and a detectivity (D*) of 2.74×10^{13} jones, which are comparable with most values reported for silicon-based flexible PDs. Moreover, the devices demonstrated exceptionally fast response times (rise time (τRise) = 205μs and fall time (τFall) = 200μs) and had reproducible characteristics and a wide range of detection. The results showed that the devices performed more efficiently with white light than with blue and green light, mainly due to the strong absorption of Si in the white colour region, which leads to more generation of photocarriers than with other coloured light. The broadband sensing and self-powered capability of the flexible photodiode offer a potential route for developing self-powered broadband photodetectors for future smart optoelectronic applications, including light imaging, light wave communication, integrated wireless sensor networks (WSNs), and wire-free routes for artificial e-skin.

Compared with other indoor flexible solar cell technologies, the fabricated Si NR solar array show a relatively low output efficiency (Table 6.1). The reason of this is primarily due to the doping concentration in the intrinsic region of the lateral p-i-n structure as well as the thickness of printed Si structures. In this regard, the intrinsic layer of Si NR solar cell is moderately p-type doped due to the unintentional doping of source wafer. This allows the electrons and holes generated by injected photons to recombine more easily and lead to increase the recombination losses. Thermal diffusion doping of boron and phosphorus dopants can induce structural defects and an elevated impurity concentration, potentially resulting in increased carrier recombination. Furthermore, the thickness of the active material is considerably low, resulting weak optical absorption [325]. To improve energy conversion efficiency for indoor applications, the absorption coefficient of silicon needs to be optimized by increasing the thickness of the silicon layer. Studies have indicated that the optimum thickness of a silicon solar cell for indoor use should be on a micro scale, approximately 1.8 µm [333]. However, as indicated in Table 6.1, ultrathin monocrystalline silicon structures are unable to achieve the same level of efficiency as perovskite thin films with high absorption coefficients, despite having similar film thicknesses. This implies that material purity may be a concern, resulting in a trade-off between device performance and material usage [295]. However enlarging the device density can significantly improve optical absorption and increase conversion efficiency [294]. Nevertheless, the Si NRs solar array shows the potential of the direct roll transfer printing method as a promising route for providing energy harvesting elements in indoor applications such as IoT, smart sensing networks, smart labels, food sensing related electronics and RFID.

Chapter 7.

Conclusion and Future Perspective

7.1 Conclusion

Heterogeneous integration of high mobility inorganic nanostructures such as silicon and compound semiconductors having different functionalities on flexible substrates provides a potential route towards the implementation of high-performance energy autonomous flexible electronic systems. For example, a variety of devices could be fabricated using materials with different functionalities such as transistors, photodetectors, solar cells, etc. which are needed to construct the electronic system. This thesis was dedicated to progress this field of research. In chapter two, I presented strategies to obtain bendable nanostructures from bulk and epitaxially grown wafers using the top-down approach which uses standard micro-nanofabrication techniques. This was followed by presenting a detailed survey of various transfer printing techniques explored so far to integrate these top-down constructed nanostructures of inorganic materials. Transfer printing techniques range from stamping-based methods (including surface treatment and adhesive assisted transfer printing, kinetically controlled transfer printing technique, laser-assisted transfer printing and shape memory polymer-based transfer printing), to modified versions of transfer printing such as gecko-inspired transfer printing techniques, and aphid-inspired transfer printing techniques. The working principles and the performances of these techniques were overviewed and compared. Following this thorough literature review, I found that there still exists a large number of challenges. These include: (i) the reported transfer printing approaches are a batch-to-batch process and thus, provide low throughput, (ii) the transfer yield is low to print nanoscale materials, and (iii) not R2R compatible. Thus, there is a lot of potential to tap into. Innovations are required to develop transfer printing technology that can integrate inorganic nanostructures with high transfer yield, and perfect registration and should be R2R compatible for high throughput printed process. While achieving these process features,

printing should allow integration of high electronic grade quality nanomaterials to provide high performance flexible devices at a reduced cost, and complexity.

In chapter three, I demonstrated the use of a modified transfer printing approach to obtain high transfer yield of Si nanoribbons. A detailed study of the printing process and results are presented for the fabrication of high-performance flexible Si nanoribbons (NRs) based transistors. The chapter further presents a room temperature process to deposit gate dielectric, directly on silicon nanostructure integrated on flexible substrates followed by the metallisation steps to define source/drain/gate electrodes. The optimised fabrication process yielded Si nanoribbons-based field effect transistors (NRFETs) with RT deposited high quality gate dielectric. This study provided a base to understand the capability of NRs as semiconducting channel and the challenges associated to realise devices on flexible substrates. The electrical results demonstrated that the combination of utilising high mobility inorganic semiconductors with room temperature compatible processes to integrate nanostructures on a flexible substrate can produce high performance transistors with mobility reaching to the state-of-the-art values (>600 cm^2/Vs). Further, the electromechanical studies performed on the fabricated transistors showed no performance degradation. However, it was noticed that the modified transfer printing route which uses PDMS had drawbacks as it could introduce impurities on the NR surface. Further, there is a room to further enhance the transfer yield, registration and speed of the process (which are drawbacks common with most of the reported transfer printing methods). Motivated by these limitations, I attempted to develop an R2R compatible transfer printing approach and the results were shown in chapter 4.

Chapter 4 presented a novel printing approach named ‘direct roll transfer printing’ (DRTP) to directly transfer the inorganic nano/microstructures from donor to various receiver flexible and biodegradable substrates. This promising printing technique avoids the use of viscoelastic stamps (this is why called “direct” transfer) and thus, reduces the number of fabrication steps with respect to the conventional transfer printing approach. In this method, structures over the donor substrate were brought into direct physical contact with the spun semi-cured thin polyimide (PI) film over the receiver substrate. Because of the

semi-cured nature of the polyimide, a strong adhesion is developed between the structures on the donor substrate and the receiver which eventually leads to a high transfer yield. Furthermore, the approach leads to high registration (<100 nm) with reduced printing time, and lower fabrication cost. These printing features can lead to resource-efficient electronics manufacturing. The presented approach enables the integration of high-quality Si nanostructures with excellent registration of <100nm (retaining spacing, orientation, etc.) and transfer yield (~95%). The developed approach addresses several issues that were observed in conventional and modified transfer printing techniques (depicted in chapter 4), such as polymer residues/contamination, poor registration accuracy, process complexity, and material wastage. Using the developed approach, Si NRs were transferred onto a variety of substrates including flexible and biodegradable metal foils. In this chapter, following the transfer printing of NRs on flexible polyimide substrate, similar RT fabrication processes including dielectric (SiNx) and metal deposition were performed to realize high-performance n-channel and p-channel transistors (as presented in the previous chapter). The silicon NR based n-channel transistors (fabricated on direct roll transfer printed NRs) consistently showed high performance i.e., high on-state current (I_{on}) >1 mA, high mobility (μ eff) >600 cm^2/Vs, high on/off ratio ($I_{on}/_{off}$) of around 10^6, and low hysteresis (<0.4 V). Further, the fabricated p-channel transistors demonstrated high linear mobility ~100 ± 10 cm^2 $V^{-1}.s^{-1}$, current on/off ratio >10^4, and low gate leakage (<1 nA). The fabricated transistors showed robust device performance under mechanical bending and at a wide temperature range (15°C – 90°C), showing excellent potential for futuristic high-performance flexible electronic devices/circuits.

The direct printing approach was also used to transfer silicon NRs arrays over biodegradable magnesium (Mg) metal foils as device substrates [86]. Mg was chosen as the device substrate due to its inherent advantages including high thermal stability, chemical stability, hermeticity, biodegradability, and biocompatibility. Due to the poor elasticity of Mg foils, a flat stage printing set-up was used to hold the target Mg foil having semi-cured PI layer on top. The PI was used as an adhesive layer due to its capacity to accommodate in vivo conditions and is certified as biocompatible. Along with biodegradability, transient devices

are expected to have a stable device operation over a predefined time frame. This could be difficult to achieve due to the intrinsic water-soluble nature of the biodegradable materials used during the fabrication. In this regard, I performed an in-depth study of the device stability which includes the ageing effect, temperature-dependent stability, and electrical gate-bias stress study. The stability study confirms robust device performance under applied temperature and gate-bias stress and for more than three months of the collected data. This confirms the high quality of the developed fabrication process. Further, the effects of transience on the electrical functioning of devices on Mg foils in aqueous solution of pH-8 at 37 °C were systematically studied by hydrolysis. Finally, I performed the biodegradable studies of the transistor devices in aqueous solution at different pH scales and a constant temperature of 37 °C to extract the etching rate of the Mg foil. This study will open many interesting avenues to construct the next generation of biodegradable ICs to reduce the growing burden of e-wastage leading to the next generation of sustainable electronics while keeping intact the performance of conventional electronics.

The results presented in chapter 4 suggests that the versatile DRTP method can also be used to print nanostructures based on other materials such as GaAs on large area flexible substrates. Chapter 5 is dedicated towards printing of other high mobility structures. In this chapter, I demonstrated the capability of DRTP for integrating bendable structures fabricated from compound semiconductors (GaAs). The printed GaAs structures were used to produce high-speed flexible broadband photodetectors (PDs). To achieve high transfer yield, I optimized the synthesis process to obtain GaAs microstructures and then tuned the direct printing process parameters to obtain high transfer yield. The arrays of GaAs microstructures were obtained using top–down fabrication approach, which includes the use of bulk wafer-based source materials, photolithography, and chemical etching procedures. It is worth noting that the adopted printing route can help in reducing the fabrication cost because the donor substrate (bulk GaAs wafer) can be reused multiple times after the transfer of GaAs microstructures to the receiver substrate. Following the direct roll printing step, the high-performance metal‑semiconductor‑metal (MSM) back-to-back Schottky contact-based PDs were realized using a conventional microfabrication process. The sensing

performance of the semi-insulating undoped (resistivity at RT, $>10^7$ Ω .cm) GaAs microstructures-based PDs was systematically evaluated in ambient conditions. Under UV (365 nm) and NIR (850 nm) light conditions, they showed high R ($>10^4$ A/W), D* ($\approx 10^{15}$ jones), photoconductive gain, G ($>10^4$), and external quantum efficiency, EQE (10^6%), and high dark to light current on/off ratio values ($>10^2$). Furthermore, the optimized fabrication steps were used to realize doped GaAs microstructures (carrier concentration 2.7×10^{18} cm^{-3})-based low-powered PDs (operating voltage = 1 V). These PDs showed better performance (except for current on/off ratio values) as compared with undoped microstructures-based devices (characterized under similar conditions). The PDs based on both doped and undoped GaAs microstructures showed ultrafast response/recovery (2.5/8 ms) times. Finally, the PDs were tested under mechanical bending and twisting conditions for up to 500 cycles and they showed robust device performance. This shows that the developed material and fabrication scheme holds considerable potential for large-area flexible and high-performance optoelectronic sensors/circuitry-based ultrafast optical communication.

In the last chapter, chapter 6, I illustrated the use of direct roll printing to integrate Si NRs to fabricate miniaturised indoor light energy harvesters on flexible substrates. These energy harvesting devices are important to power the portable sensor-laden systems such as electronic-skin (e-skin) and wearables which could enable a wide range of Internet of Things (IoT) applications in areas such as healthcare, smart homes, digital agriculture etc. The active element (p-i-n silicon nanoribbons) for converting light into electricity are fabricated using the top-down approach discussed in the previous chapters. The direct roll transfer printing approach was used to integrate these energy conversion elements onto flexible substrates over large areas. The direct roll transfer printed Si NRs with a p-i-n structures were used to miniaturized solar cells with an area of just ~315 μm^2. The maximum power density of ~11 $\mu W/cm^2$ is obtained by connecting 32 identical micro cells in parallel. In addition to light energy harvesting, the fabricated micro solar cells could also work as wideband photodetectors. As photodetectors, these devices showed excellent current rectification characteristic ratio of up to 8 orders, when measured under dark and indoor

white light illumination. The developed photodiodes or micro solar cells can act as self-powered photo sensors with distinctive photo response under visible-UV-NIR light illumination. The fabricated device exhibits excellent broadband photoresponse from UV to NIR, featuring high-speed response and peak responsivity R of (2.48 A/W) at 365 nm at zero bias voltage giving them self-powered features. This corresponds to an external quantum efficiency EQE of (>10^2 %) and detectivity D* of (~10^{13} jones), which were relatively comparable to most values reported for silicon-based flexible photodetectors. Additionally, the device demonstrates an exceedingly fast response speed (rise time τ_{Rise} = 205 μs and fall time τ_{Fall} = 200 μs) and stable detection performance, coupled with good mechanical flexibility. The presented work provides exciting opportunities for indoor energy harvesting to power connected sensors for IoT applications.

7.2 Future Perspective

The work presented in this thesis, along with the capabilities demonstrated in realizing micro/nano-scale structures, such as nanoribbons (NRs) derived from high-mobility inorganic semiconducting materials and integration techniques, holds great potential for achieving flexible, high-speed, and efficient electronics. Considering the uniquely addressable application areas, this provides excellent motivation for further exploration in the rapidly emerging field of printed electronics and sensing technologies. Chapter 2 explored the fabrication using top-down approach and patterning techniques employed to release bendable forms in micro and nanoscale structures fabricated from high-quality inorganic semiconductors and integrated with flexible substrates. These techniques complement the widely examined source wafers in microelectronics that use epitaxially grown multilayers of high-quality single-crystalline and compound semiconductors. They not only serve as a method for printing and integrating micro/nanoscale device arrays but also enable the realization of stretchable forms of silicon and other brittle inorganic materials. The design choices and material diversity offer a promising direction for research in flexible and stretchable electronics that are challenging to address using other approaches.

The opportunity for heterogeneous integration in 2D or 3D layouts, coupled with unusual mechanical characteristics including stretchability and flexibility, presents interesting route for future research in the field of flexible electronics. Developing new chemistries and materials, investigating physics and reliability upon bending, and stretching, and designing are promising areas for further investigation. Advanced transfer printing technologies, including bio-inspired transfer printing techniques, have been widely applied in the fabrication of flexible and stretchable electronics. While existing reports mainly demonstrate the viability and investigate the related mechanisms and optimization, future work should focus on providing further evidence of the feasibility of these transfer printing techniques in practical applications. This will advance the field of flexible electronics, enabling the realization of high-performance, flexible, and stretchable inorganic electronics for a broad range of applications and paving the way for transformative advancements in the field of printed electronics and beyond.

The performance comparison of the Field-Effect Transistors (FETs) presented in Chapter 3 with state-of-the-art conventional microelectronics silicon CMOS-based transistors clearly indicates that the performance of the printed transistors, particularly the p-type FETs, appears relatively lower in comparison to the n-type FETs. This finding underscores the necessity for further optimization in terms of the doping process. The current spin-on dopant process used for doping may not be the ideal approach. Therefore, for future work direction, the adoption of ion-implantation as the doping method should be considered. The utilization of ion-implantation holds promise for achieving more effective and uniform doping, which could significantly enhance the performance of both n and p-type transistors. By addressing the current mobility disparity between n-type and p-type FETs and improving the uniformity among the devices, this advancement can lead to performance improvements, thereby paving the way for the development of high-speed, low-power printed CMOS circuitry.

In Chapter 4, the novel printing approach of 'direct roll transfer printing' (DRTP) was introduced, enabling the direct transfer of inorganic nano/microstructures onto flexible and biodegradable substrates. To optimize and advance this technique, a key focus area should

involve the design and optimization of an active, programmable roll elastomeric stamp to enable efficient assembly of structures with intricate patterns. An important step is the upgrade of the semi-automated roll system setup to incorporate additional functionalities, including thermal platforms for precise curing control and the utilization of UV sources to facilitate UV-curable adhesives for enhancing printing speed, transfer yield required in large-area flexible electronics integration. Furthermore, exploring the potential of the roll-to-roll transfer printing process offers a promising route, but its successful implementation will require major innovations in machine design, process recipes, material handling, and system integration. Additionally, investigating transfer printing techniques for integrating functional devices onto curvilinear substrates with various materials, including biological ones, holds great promise for the development of bio-integrated electronics and human-machine interfaces, offering diverse applications from healthcare to flexible displays and beyond. By focusing on these areas, future research can expand the capabilities of roll transfer printing and drive advancements in flexible electronics, creating versatile and impactful technologies for numerous fields.

Chapter 5 has successfully demonstrated the validity of direct roll transfer printing for realizing printed arrays of GaAs microstructures, leading to the achievement of high-performance flexible broadband PDs. Building upon this progress, the presented approach holds promise for further development of highly efficient electronic layers based on high-quality nanostructures, such as NR and NMs, that can be derived from customized epitaxial grown wafers utilizing sacrificial layers to enable the realization of final device layers. Future investigations should focus on exploring the integration of roll transfer printed silicon nanoribbon arrays with diverse materials and devices, enabling the creation of complex and multifunctional components, including microwave and power electronics. To this end, valuable insights can be gained by investigating the integration of silicon nanoribbon arrays with other materials such as SiC, GaAs, GaN, AlGaAs, and 2D materials, such as graphene, TMDs, and MoS_2. In this regard, the exploration of various types of electronic layers, such as sensors, actuators, or energy harvesters, offers exciting prospects for developing advanced flexible electronics capable of diverse functionalities and applications.

In Chapter 6, the development of flexible multifunctional Si NRs solar cells using direct roll transfer printing techniques has demonstrated promising results; however, there is still considerable room for enhancing their performance. For future directions, the engineering of device structure morphology can be investigated to create advanced, high-performance flexible solar cells. Exploring several optimization factors, including light-trapping structures, surface texturization, surface passivation layers, antireflection coatings, and others, holds significant potential for improving the device's optical absorption and overall performance. Thus, the incorporation of the developed printed high-performance CMOS electronics building blocks, sensory platforms powered by sustainable energy harvesting technologies, and smart packaging techniques on flexible substrates provides an efficient pathway to realize energy-autonomous flexible systems for emerging applications where high performance and conformability are required.

Appendix

A1: Nanofabrication techniques/photolithography steps.

Table 8.1: The detailed fabrication steps that has been carried out on SOI wafer for realising Silicon NRs structure.

Steps	Operation
Surface cleaning	• The wafer should be cleaned for 3 min sequentially in acetone, isopropanol, deionized water and blow dried with N_2 gun.
Photoresist spin-coating	• The wafer was mounted on the vacuum chuck of the spinner system and vacuum was enabled. • HMDS and Photoresist S1805 were spin-coated on the wafer, both at 4000 rpm for 30 seconds. • The coated wafer is baked at 115°C for 1min.
Exposure	• The wafer and the designed mask were loaded in MA6. The position of the sample was aligned with respect to the mask under the assistance of an optical lithography equipped in MA6. • Exposure was carried out in hard contact mode for 3s.
Development	• The exposed wafer was developed in MF319 for 75 s and then rinsed in RO water for 3 minutes. The wafer is then blow dried with N_2 gun.
Hardbake	• 120°C oven for 30 mins
Si-NR Patterning	• Dry etch was applied to define the NRs structure. • Etching Tool: RIE 80 Plus. • Gases used: CHF3 / O2 Temp: 20 °C. • Mask Material: PR S1805 • Time required to etch 70nm thick: 4min (Etching rate: 17.5nm/min)
Strip resist	• Acetone 5min ultrasonic, IPA 5mins ultrasonic, N2 dry.
Plasma treatment	• Plasmafab @ 150W for 1min to remove residues after Si dry etch.

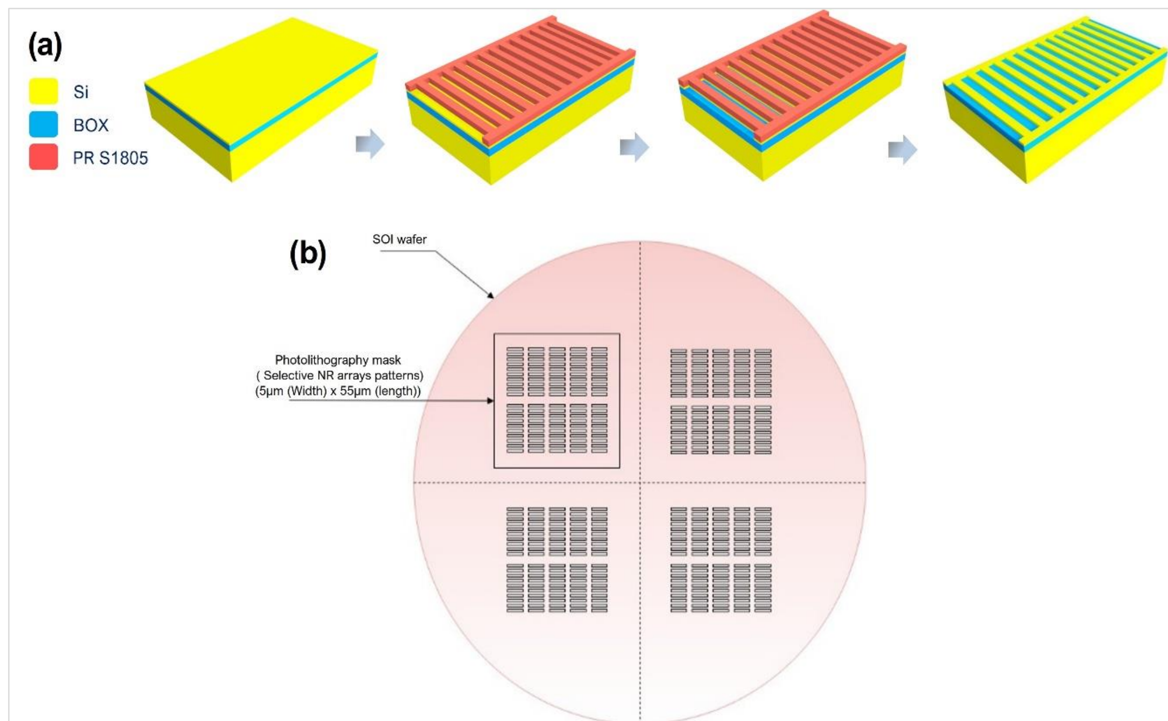


Figure 8.1: **(a)** The schematic illustration of the fabrication process flow for realising Si NR arrays structures on SOI wafer. **(b)** Photolithography mask layout, showing the geometries of the Si NR structures.

Table 8.2: Recipe used for depositing SiO_x via Plasma Enhanced Chemical Vapour Deposition (PECVD) and SiNx via Inductively Coupled Plasma Chemical Vapour Deposition (ICP-CVD)

Material	**Tool**	**Recipe**
SiO_x	PECVD 80+	SiH_4: 7 sccm N_2O: 200 sccm N_2: 85 sccm RF Power: 15 W Pressure: 1000 mTorr Temperature: 300°C
SiN_x	ICP 180	SiH_4: 7.2 sccm N_2: 6 sccm RF Power: 100 W Pressure: 4.4 mTorr Temperature: 35°C

Table 8.3: Recipe used for dry/plasma etching of deposited PECVD SiO_x and ICP 180 SiN_x using Oxford Instrument Reactive Ion Etching (RIE)

Material	**Tool**	**Recipe**
PECVD SiO_x	RIE 80+	CHF_3: 25 sccm Ar: 18 sccm RF Power: 200 W Pressure: 30 mTorr Temperature 20 ˚ C Etch rate: 30nm/min
ICP180 SiN_x	RIE 80+	CHF_3: 50 sccm O_2: 5 sccm RF Power: 150 W Pressure: 55 mTorr Temperature: 20 °C Etch rate: 25nm/min
Si	RIE 80+	Same as ICP180 SiNx recipe Etch rate: 18nm/min

The Oxford Instruments RIE 80+ tool was one of the major equipment that was used substantially in this research for etching PECVD SiO_x and room temperature deposited ICP-180 SiN_x with applying etching gases of trifluoromethane/argon (CHF_3/Ar) and trifluoromethane/oxygen (CHF_3/O_2), respectively.

A2: Thermal diffusion doping using horizontal thermal furnace.

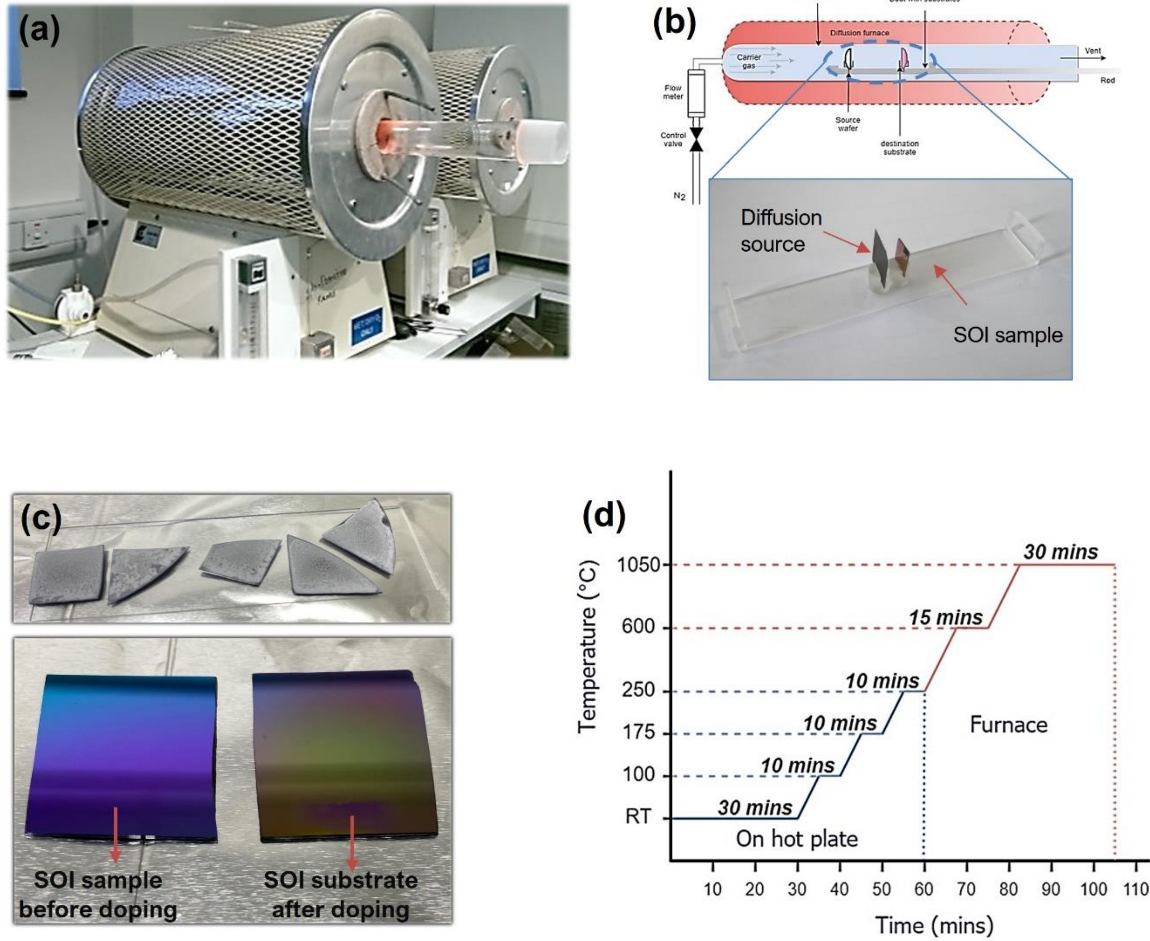


Figure 8.2: **(a)** Optical picture of horizontal thermal furnace utilised for doping processes of SOI wafers through thermal diffusion. **(b)** Schematic illustration of the furnace setup. **(c)** The top optical picture represents the diffusant source samples coated with dopant agents and prepared for doping process using Spin on Dopant (SOD) technique, the bottom optical picture shows the SOI sample before and after doping and cleaning procedure. **(d)** Schematic representation of the optimisation of the SOD treatments and doping procedures (annealing time versus applied temperatures) that have been carried out in this research.

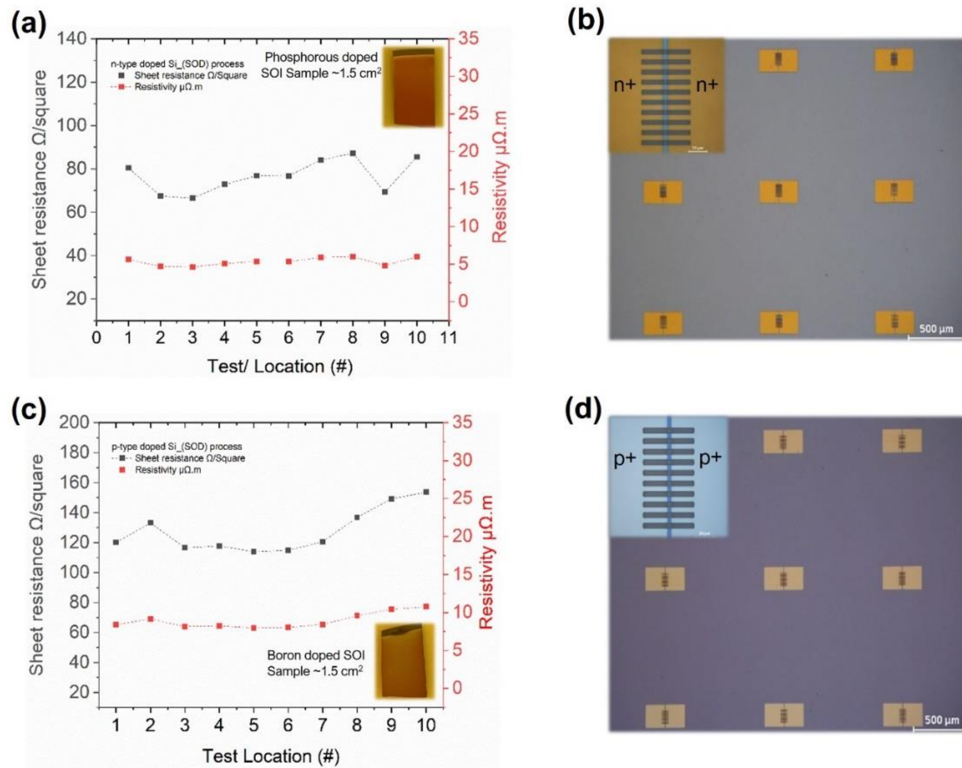


Figure 8.3: **(a)** Sheet resistance and resistivity data obtained from four-probe measurements of n-type doped Si sample. **(b)** Optical image **of** n+ selective doping performed for source and drain contacts toward fabricating n-type SiNRs-FETs. **(c)** Sheet resistance and resistivity data obtained from four-probe measurements of p-type doped Si sample. **(d)** Optical image **of** p+ selective doping performed for source and drain contacts toward fabricating p-type SiNRs-FETs.

A4: High-Performance n-Channel Printed Transistors on Biodegradable Substrate for Transient Electronics

Table 8.4: A performance comparison with the similar transistor realised on flexible polyimide (PI) substrates.

S. No.	Transfer printing method	Si nanostructure morphology (n-channel SiNR FET)	Device substrate	Mobility (cm^2/Vs)	$I_{on/off}$ ratio	Threshold Voltage (V)
1	Direct Roll Transfer Printing	Nanoribbons, thickness (70 nm)	PI	~630	10^6	~0.4
2	Direct transfer printing	Nanoribbons, thickness (70 nm)	Mg	~640	$>10^4$	~1.4

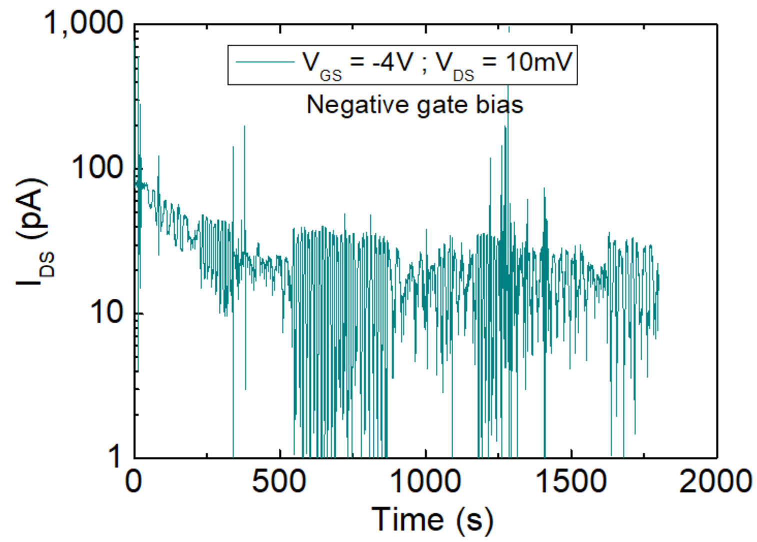


Figure 8.4: I_{DS} – time curve during the applied negative gate bias condition.

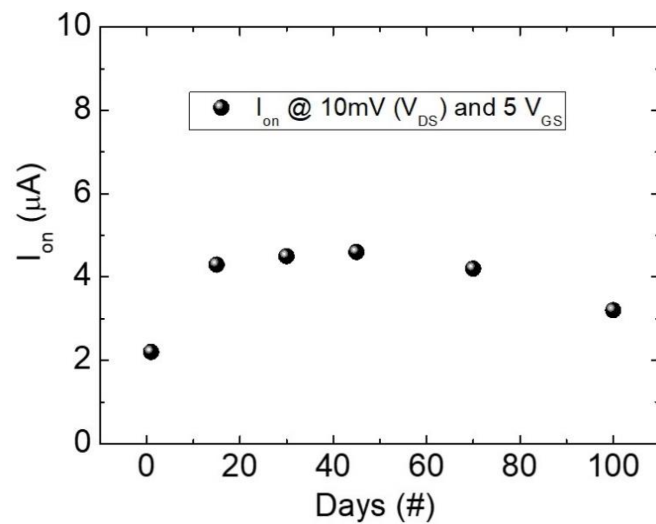


Figure 8.5: Ageing study of the transient n-channel transistors. The device on-current was measured under similar ambient conditions.

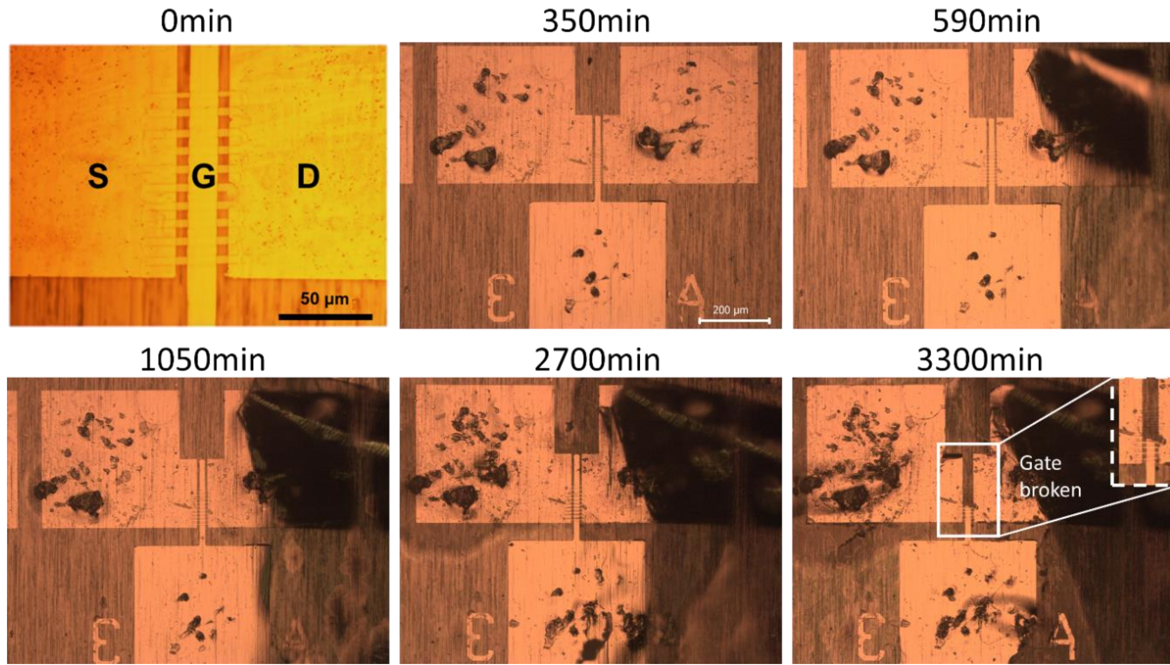


Figure 8.6: Optical micrographs of the transient transistor on Mg foil captured at different time kept in aqueous solution of pH 8 and temperature of 37°C. The experiment was done to understand the reason for decrease in device function (I_{on}). The scale bar in optical images for 590min, 1050min, 2700min, and 3300min is same as shown in the optical image for 350min.

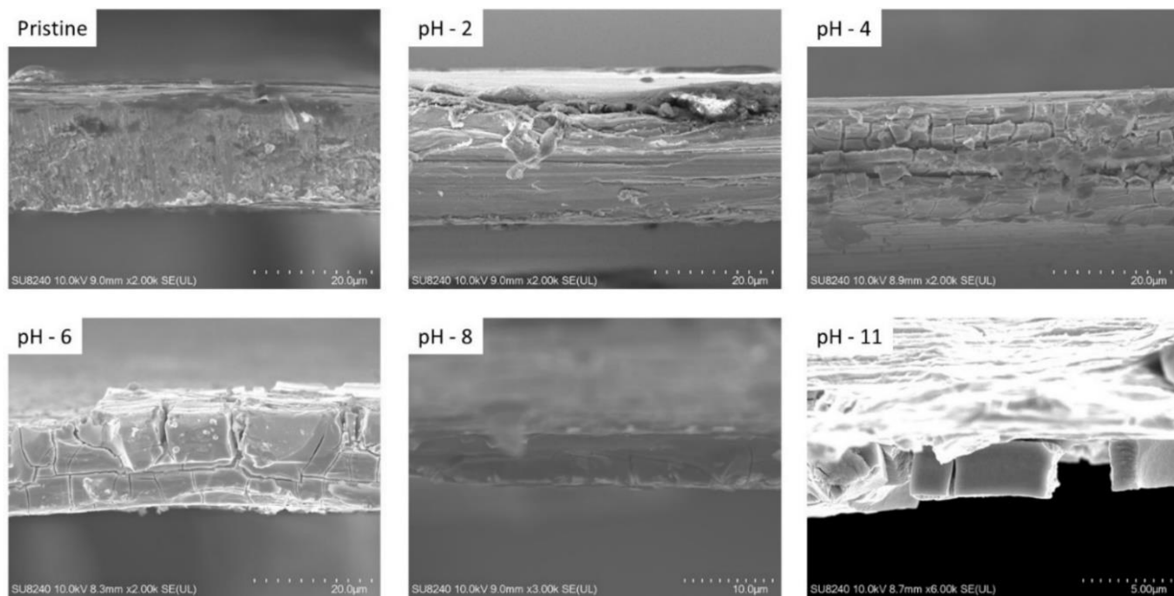
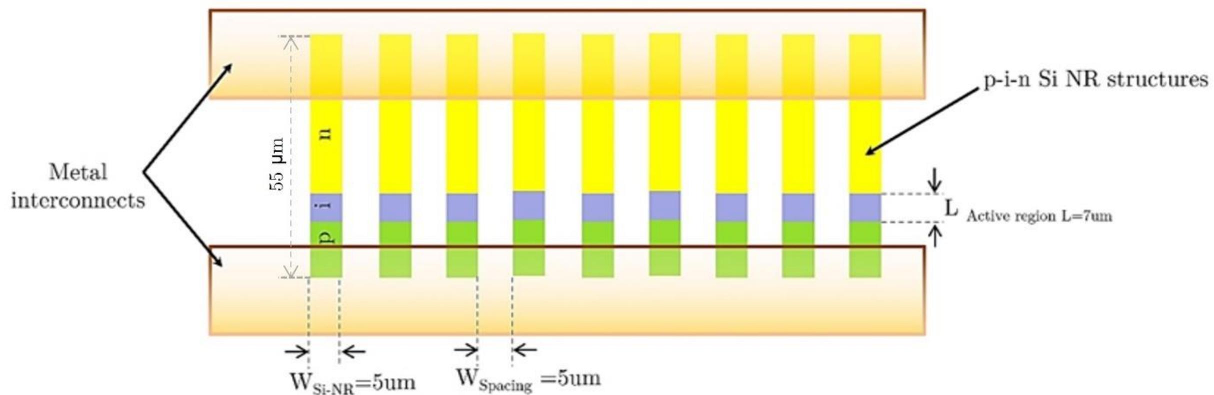


Figure 8.7: Cross-sectional SEM images of the transient devices on Mg foil kept in aqueous solution at different pH values and same temperature of 37°C. The experiment was done to extract the thickness of the Mg foil after etching in aqueous solution.

A5: Direct Roll Transfer Printed Silicon Nanoribbon Arrays based Multifunctional Micro Solar Cells



D = ($W_{Si\text{-}NR}$ + $W_{Spacing}$) x (Number of NRs) − $W_{spacing}$

$W_{Si\text{-}NR}$: width of NRs= 5 µm. $W_{Spacing}$: spacing between NRs = 5 µm.

D: total length of the single array composed of 9 NRs/nano-cells = 85 µm.

$L_{Active\ region}$: Length of active region.

Figure 8.8: Schematic illustration of the device design and architecture of single Si NR solar array

A6: The typical recipes used in this research for photolithography processes are described below.

- Conventional photolithography steps using **photoresist S1805**

Generally, the photoresist **PR S1805** was used where a pattern with a minimum resolution of ~5 µm or less was required. This recipe was primarily used to define the Si NRs structure and GaAs wire arrays on SOI wafer and GaAs bulk wafer respectively.

1	Sample cleaning: 5mins ultrasonic acetone, 5mins IPA and 5mins running RO rinse water, and blow dried with N_2 gas.
2	O_2 plasma treatments for 2 mins at 100W
3	The sample was mounted on the vacuum chuck of the spinner system and vacuum was activated.
4	The photoresist adhesion promoter; Hexamethyldisilazane (HMDS) was drop casted and spun on to the sample at 4000 RPM speed for 30 seconds.
5	The photoresist S1805 was applied immediately using a Poly Tetra Fluoro Ethylene (PTFE) syringe filter and spun on to the sample at 4000 RPM for 30 seconds.
6	The sample was pre-baked on 115 ˚ C hotplate for 60 seconds
7	The sample was loaded in the mask aligner MA6 and exposed for 2.3 seconds using hard contact
8	The sample was developed for 75 seconds in MF319 developer at room temperature
9	The sample was rinsed under RO water for 75 seconds, followed by blow dry with N_2 gas
10	The sample was observed through an optical microscope

➢ Metal Lift-off using **photoresist S1818** and LOR10A:

The patterned metallisation step was performed using bi-layer metal lift-off to form the metal contacts for the fabricated devices that are presented in this thesis, the following recipe involves lift off resist LOR10A, which serves as a sacrificial undercut layer in lift-off processing. The process recipe steps are described below:

1	Sample cleaning: 5mins ultrasonic acetone, 5mins IPA and 5mins running RO rinse water, and blow dried with N_2 gas.
2	The sample was then treated with dehydration bake at 120 ˚ C for 30 minutes.
3	O_2 plasma treatments for 2 mins at 150W
4	The sample was mounted on the vacuum chuck of the spinner system and vacuum was activated.
5	LOR10A was drop casted and spun on to the sample at 6000 RPM speed for 30 seconds.
6	The sample was pre-baked on 160 ˚ C hotplate for 120 seconds
7	The photoresist S1818 was applied using a Poly Tetra Fluoro Ethylene (PTFE) syringe filter and spun on to the sample at 4000 RPM for 30 seconds.
8	The sample was pre-baked on 115 ˚ C hotplate for 180 seconds
9	The sample was loaded in the mask aligner MA6 and exposed for 6 seconds using hard contact
10	The sample was developed for 2 minutes in MF319 developer at room temperature
11	The sample was rinsed under RO water for 3 minutes, followed by blow dry with N_2 gas
12	The sample was observed through an optical microscope
13	The sample was treated in O_2 plasma asher at 100W, just before performing the metallisation step.
14	The sample was mounted inn electron-beam evaporator for metal deposition, the desired metal stack was deposited on the patterned bilayer resist.
15	Lift-off of the undesired metal on top of the photoresist stack by soaking the sample in 1165 stripper for at least 3 hours to remove the photoresist stack.
16	The sample was rinsed in IPA followed by RO water and blow dry with N_2 gas.

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