GaN HEMT Technology for W-Band Frequency Applications

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Abstract

Owing to the technological advancement, and rapid industrial growth which stimulate a rapidly growing demand for more efficient transistor devices for high-power high-frequency applications, gallium nitride (GaN) material has been one of the most intensively researched semiconductor materials in the past two decades. Apart from its exceptional material properties, GaN exhibits a unique attribute of an ability to generate a sheet of high density highly mobile two-dimensional electron gas (2DEG) without the need of any intentional doping. Due to the high mobility (~2000 $cm^2/V.s$) and concentration ($1X10^{13}$ cm^{-2}) of the 2DEG, and the large energy band gap (3.4 eV), gallium nitride devices can efficiently deliver high-power at high operating frequencies. Its low intrinsic carrier density (~$10^{-12}/cm^3$) enables operating GaN devices at much high operating temperatures than other conventional semiconductor materials.

Despite this propound potential, due to some critical performance and reliability challenges, GaN transistors are yet to meet an acceptable industrial performance which leads to still limited deployment in the semiconductor market for electronic applications. The focus of this project is to improve in the device processing technology which has been one of the major causes of poor performance of GaN devices in high-power high-frequency applications. GaN devices suffer from high ohmic contact resistance, gate-to-source capacitance C_{GS}, and inefficient heat dissipation property which severely results in high power losses, low efficiency, and low cutoff frequency. These affects the output power and high-frequency parameters (such as the unit power gain f_{max} and unit current gain f_t cut-off frequencies). The conventional method of realising low ohmic contact using heavily doped GaN contact layer requires complex and time-consuming regrowth

processes. In this work, we present a new approach of realising low ohmic contacts using the heavily doped GaN cap layer technique, but without regrowth. Instead of using the usual undoped 2 nm GaN cap layer, the approach involves growing a heavily doped 5 nm GaN cap layer with a Si-doping density of $1x10^{19}$ cm^3 on the AlN/GaN HEMT using molecular beam epitaxy (MBE). This technique is cost effective and minimises complexity and processing time. We obtain a very low ohmic contact resistance of 0.132 Ω.mm with 428 Ω/sq sheet resistance, for AlN (aluminium nitride) barrier GaN high electron mobility transistors (HEMTs).

Reduction of gate length is required to realise a high-frequency device. However, such reduction results in high gate resistance which affects the maximum cut-off frequency of the device. A T-shape structure of gate is normally used to reduce the gate resistance. Because of the need of very small gate lengths in high-frequency devices, any further reduction of the gate length to sub-100 nm, could lead to a severe instability due to weakening mechanical strength of the gate structure. This has become a serious reliability concern, and consequently the T-shape gate is conventionally supported using thick passivation layer of dielectric materials such as Si_3N_4. This layer in turn results in an unwanted parasitic capacitance which affect the frequency performance of the device. In this work, we present a new fabrication technique which yields a robust and stable T-shape gate structure without the use of any supporting insulator such as Si_3N_4. While this approach has not been tested on a full wafer (>4 inches) yet, it shows promising potential for using it in commercial manufacturing.

In another strand of the research, we have demonstrated the benefit of AlGaN/GaN HEMTs on diamond as efficient heat extraction mechanism for GaN devices by using three identical AlGaN/GaN on diamond wafers with varying thicknesses of GaN buffer and the diamond substrates. Due to the efficient heat extraction property, a transistor with high power density, effective unity power gain and current-gain cut-off frequencies of 32.04 W/mm at V_{GS} = 0 V and V_{DS} = 60 V, 90 GHz and 128 GHz are realised, respectively. We analysed the impact of the buffer and substrate thicknesses and found that self-heating of the device is less in devices with thinner diamond substrate and even lesser when the buffer is thinner.

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1. Karami, K. , Dhongde, A., Cheng, H., Reynolds, P. M. , Reddy, B. A., Ritter, D., Li, C. , Wasige, E. and Thoms, S. (2023), "Robust sub-100 nm T-Gate fabrication process using multi-step development." Micro and Nano Engineering, 19, 100211.

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Author's declaration

Statement of Originality to Accompany Thesis Submission

Name: Kaivan Karami
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I certify that the thesis presented here for examination for a PhD degree of the University of Glasgow is solely my own work other than where I have clearly indicated that it is the work of others (in which case the extent of any work carried out jointly by me and any other person is clearly identified in it) and that the thesis has not been edited by a third party beyond what is permitted by the University's PGR Code of Practice.

I declare that the thesis does not include work forming part of a thesis presented successfully for another degree.

I declare that this thesis has been produced in accordance with the University of Glasgow's Code of Good Practice in Research.

I acknowledge that if any issues are raised regarding good research practice based on review of the thesis, the examination may be postponed pending the outcome of any investigation of the issues.

Signature:
Date: 01/06/2023

Abbreviations

- 2DEG - 2-Dimensional electron gas
- Al - Aluminium
- Au - Gold
- AlGaN - Aluminium gallium nitride
- AlN - Aluminium nitride
- Ar - Argon
- BCL_3 - Boron trichloride
- Cl_2 - Chlorine
- CPW - Coplanar waveguide
- CTLM - Circular transmission line model
- CVD - Chemical vapour deposition
- DC - Direct current
- e-Beam - Electron beam
- E_C - Conduction band energy
- E_f - Fermi level energy
- E_g - Bandgap energy
- f_{max} - Maximum frequency of oscillation or unity power gain cut-off frequency
- f_T - Unity current gain cut-off frequency
- Ga - Gallium
- GaN - Gallium nitride
- GaAs - Gallium arsenide
- g_m - Transconductance
- HEMT - High electron mobility transistor

- IV – Current-Voltage
- InP - Indium phosphide
- InAlN- Indium aluminium nitride
- JWNC - James Watt Nanotechnology Centre
- k - Thermal conductivity
- L_{SD} - Source - drain distance
- L_T - Transfer length
- LOR - Lift-off resist
- MMIC - Monolithic microwave integrated circuit
- MBE - Molecular beam epitaxy
- MOCVD - Metal organic chemical vapour deposition
- N_2 - Nitrogen
- N_s - Sheet carrier concentration
- Ni - Nickel
- P_{PE} - Piezoelectric polarization
- PSP - Spontaneous polarization
- PECVD - Plasma enhanced chemical vapor deposition
- PMMA - Poly methyl methacrylate
- q - Electron charge
- RIE - Reactive ion etching
- R_C - Ohmic contact resistance
- RO - Reverse Osmosis
- R_{sh} - Sheet resistance
- R_F - Radio frequency
- RTA - Rapid thermal annealing
- SiC - Silicon carbide
- $SiCl_4$ - Silicon tetrachloride
- Si - Silicon
- SiN_x - Silicon nitride
- TBR - Thermal boundary resistance
- TiN - Titanium nitride
- Ti - Titanium
- V_{DS} - Drain - source voltage
- μ_n - Electron mobility

- ε - Absolute permittivity
- ε_0 - Vacuum permittivity
- ε_r - Relative permittivity
- Φ_b - Schottky barrier
- σ - Polarisation charge

Chapter 1

Introduction

1.1 Overview

Silicon (Si) based semiconductor technology has grown remarkably during the past several decades due to its availability, low cost, and the suitability of its lattice structure to doping. Although silicon technology has recorded tremendous achievements over this period, the quest for more efficient and compact systems in high-power high-frequency applications has exhausted the limit of silicon in terms of switching speed, operation temperature, and power handling capability. Efforts invested to improve on the performance of certain parameters of radio frequency (RF) silicon transistors, result in the compromise of other important device parameters. For example, the optimum operating temperature of silicon device is less than 200 °C, even at this, a cumbersome heat sinking mechanism is required to keep the device within an optimal cooling condition, which compromises in the system size. Gallium arsenide (GaAs) and indium phosphide (InP) have been popular in high-speed electronic applications owing to their high electron mobility and high saturated electron velocity compared to silicon. As a result, they are mostly used in low power high-frequency applications.

High RF power is fundamentally required for efficient transmission of signals. Recent developments in wireless communication, military applications, satellite and TV communications, advent of 5G technology etc. requiring wider bandwidth, increased data speed, high-power and high-frequencies is exhausting the switching and power handling capabilities of silicon, triggering the search for newer semiconductor technology. Although GaAs and InP have been used for decades in producing wide range of high-speed electronic devices, they are disadvantaged by limited power handling and thermal characteristics. Wide bandgap semiconductor materials (WBG) such as silicon carbide (SiC), gallium nitride (GaN), and the ultra-wide bandgap materials (UWBG), such as gallium oxide (Ga_2O_3), aluminium nitride (AlN) and aluminium gallium nitride (AlGaN) can achieve much power density at radio frequency range compared to Si and other conventional materials (GaAs and InP), thus enabling higher power, and frequency applications using a smaller device footprint.

Owing to their remarkable properties, SiC and GaN with a wide bandgap (of 3.26 eV and 3.46 respectively) 2 to 3 times larger than that of conventional semiconductor materials (Si:1.1eV, GaAs: 1.43 and InP: 1.34), and a large critical electric field (SiC:3 MV/cm and GaN: 3.3 MV/cm) 8 to 10 times larger (Si: 0.3 MV/cm, GaAs: 0.4 MV/cm and InP: 0.5 MV/cm), have been the most focused materials in modern day high-frequency applications. Figure 1.1 shows that the power level that could be achieved with GaN at any given frequency above 1 GHz is far beyond what could be obtained with Si material. In Table 1.1, SiC and GaN have comparatively shown superiority in the figure of merits, which measure the fundamental relationship between the material property and performance limits of a semiconductor. Due to their material attributes, are believed to be a better replacement of Si. By contrast, GaN has slight superiority over SiC with regards to some important material properties such as energy bandgap, electron mobility and electron saturation velocity. The high thermal conductivity of SiC is about twice higher than of GaN, which offers it thermal advantage in high temperature applications.

GaN possesses some unique attributes such as piezoelectric and spontaneous polarizations which allow for generation of high density of 2D charge carriers without any intentional doping. This attribute enables high-frequency operation

of GaN based devices compared to SiC. The energy bandgap of GaN alloys can be tuned from the lowest of 3.4 eV (as GaN) through various intermediary energy levels as AlGaN, to the maximum of 6.2 eV (AlN). This allows for flexibility in AlGaN/GaN heterostructure design geometry. GaN devices have been profoundly developed in some applications such as light emitting diodes, photodetectors, and semiconductor lasers in the ultraviolet range etc. Because of its high-power density, GaN can achieve high-power levels with smaller die size [1, 2]. Today GaN-based transistors have been receiving increased attention in RF and microwave applications such as RADARs, base station transmitters, C-band satellite communications (Satcom), very small aperture terminal (VSATs) and broadband satellites, 5G telecommunication technology.

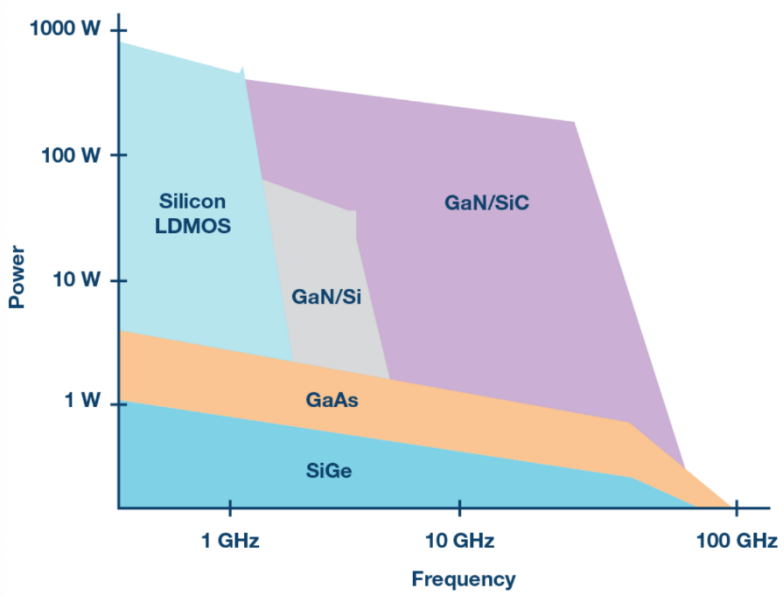


Figure 1.1 Comparing power and frequency of different materials in the microwave range, which includes mmWave [3].

In Figure 1.2 and Table 1.1 the material properties of GaN, SiC, and Si for high-power and high-frequency applications. It focuses on several key parameters including:

1. Bandgap: GaN and SiC have wider bandgaps compared to Si which allows them to operate at higher voltages and temperatures.
2. Electric Field: GaN and SiC can withstand higher electric fields compared to Si making them suitable for high-power applications.

3. Thermal Conductivity: SiC generally has higher thermal conductivity than GaN and Si, enabling better heat dissipation and improved reliability in high-power devices.
4. Electron Velocity: GaN and SiC exhibit higher electron velocities than Si, which is beneficial for high-frequency operation and faster switching speeds.
5. Electron Mobility: Si typically has higher electron mobilities compared to GaN and SiC, resulting in better charge transport and improved device performance at high-frequencies. However, during the epitaxial growth of GaN-based high electron mobility transistors (HEMTs), the electron mobility can be significantly increased, reaching values over 2000 cm^2/Vs. This improvement in electron mobility is a result of carefully controlling the growth process and optimising the epitaxial structure of the GaN HEMT.

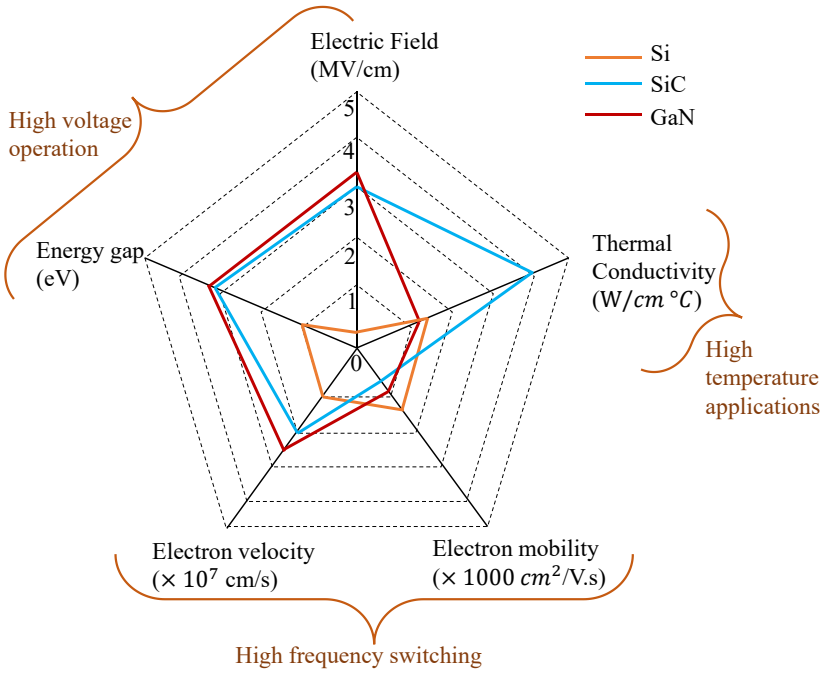


Figure 1.2 Comparison of material properties between GaN, SiC and silicon in high-power high-frequency applications [4].

Even though GaN is identified as one of the most important semiconductor materials of the day, it exhibits some challenges (outlined in Section 1.3) critical to its successful deployment in various applications. University and industry-based researchers have investigated approaches of mitigating the critical shortcomings

of GaN devices for effective deployment into high-power high-frequency applications such as high-frequency monolithic microwave integrated circuit (MMIC), aerospace, radar, and base station applications etc. It is worth mentioning that GaN devices are currently commercially available in communications, radars, and electronic applications among others [1, 5-7].

Table 1.1 Materials properties of GaN compared to other competing materials (Si, GaAs, InP, SiC and diamond) [8-11].

Semiconductors	*Energy bandgap, E_g [eV]*	*Thermal conductivity, κ [W/cm.K]*	*Breakdown electric field, E_C [MV/cm]*	*Saturated electron velocity, V_{sat} [X10^7 cm/s]*	*Electron mobility, μ_n [cm^2/V.s]*
Si	1.12	1.5	0.3	1	1500
GaAs	1.43	0.54	0.4	1	8500
InP	1.34	0.67	0.5	1	5400
SiC	3.26	4.0	3	2	700
GaN	3.44	1.3	3.3	2.5	900
Diamond	5.45	22	10	2.7	4800

1.2 Gallium Nitride Semiconductor Material

Gallium nitride (GaN) is a direct bandgap III-V binary compound material which is the by-product of the chemical reaction between gallium (III) oxide (Ga_2O_3) and ammonia (NH_3) at very high temperature (~1000^{o}C).

$$Ga_2O_3 + 2NH_3 \rightarrow 2GaN + 3H_2O$$

Because of the position they occupy in the periodic table, gallium and nitrogen atoms lack centre of symmetry in the crystal lattice of GaN which results in the formation of hard, stable crystal structure known as *wurtzite* [12] shown in Figure 1.3. This structure gives GaN a unique property of spontaneous and piezoelectric polarization which results in the formation of high density of high mobile charge carriers in the AlGaN/GaN heterojunction without any intentional doping. As

mentioned earlier, GaN possesses some remarkable material properties shown in Table 1.1, such as wide energy bandgap, large critical electric field, high electron mobility, and good thermal conductivity which makes it a material of interest in today's modern electronic applications. These properties described in the sections below, mostly arise from the strong atomic bonding between gallium and nitrogen in the lattice.

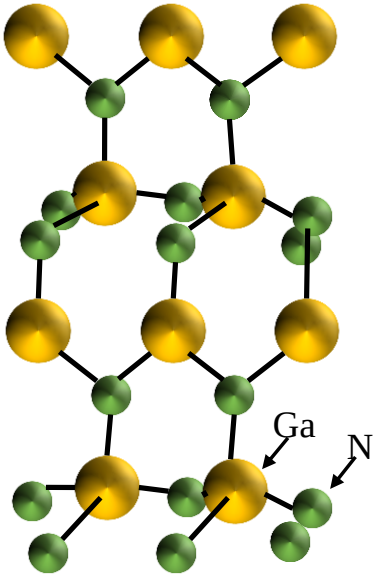


Figure 1.3 Schematic structure of wurtzite gallium nitride.

1.2.1 Energy Bandgap

GaN is a wide bandgap semiconductor material with energy gap of 3.4 eV, 3 times larger than Si (1.12 eV). In the wide bandgap semiconductor materials, electrons require higher energy to jump from the valence to conduction band, which results in lower intrinsic carrier concentration at room temperature. As shown in Figure 1.4, the intrinsic carrier concentration (n_i) for GaN at 300 ^oK is around 9.8×10^{-12} cm^{-3} [13]. This property allows GaN devices to operate at very high temperature enabling them to handle higher power density with smaller heat sinks or not at all [14]. In literature, GaN high electron mobility transistors (HEMTs) operating in a temperatures around 400 ^oC have been reported [15, 16]. Higher n_i results in avalanche breakdown. For example, the n_i of silicon at 300 ^oK is 1.38×10^{10} cm^{-3} [13], and at higher temperatures the n_i increases significantly. This

limitation makes it challenging to operate silicon devices at temperatures above 150 ºC.

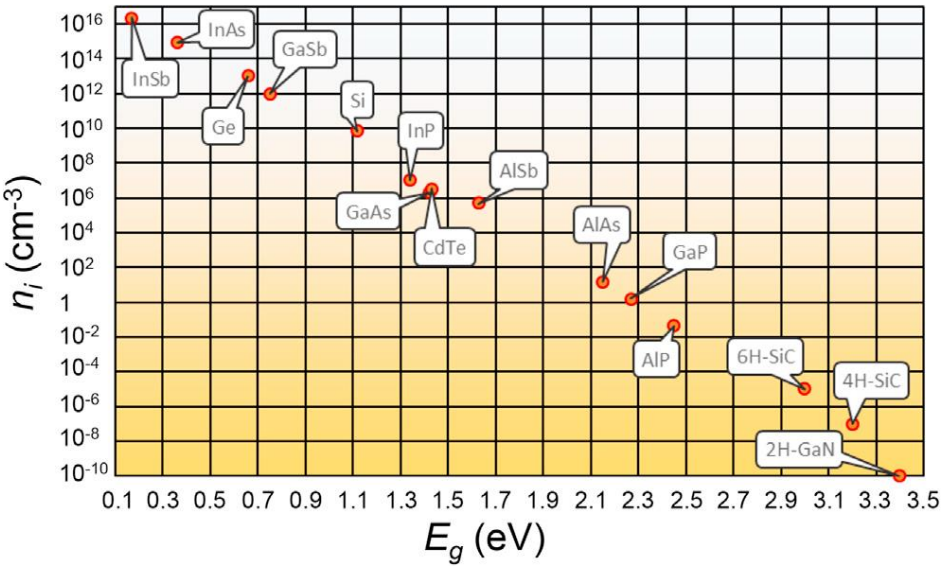


Figure 1.4 Intrinsic carrier concentration of semiconductors at 300 °K [17].

1.2.2 Breakdown Electric Field

Breakdown electric field (E_{cr}), sometimes called critical electric field, is the electric field that a material withstands before it breaks down. It is one of the most important parameters needed for high-power and high-frequency applications. The breakdown electric field of GaN material (3.3 MV/cm) is more than 10 times that of conventional semiconductor materials (Si: 0.3 MV/cm, GaAs: 0.4 MV/cm and InP: 0.5 MV/cm) used in radio frequency applications, and by implication, GaN devices can withstand voltages 8 to 10 times higher than the conventional semiconductors (Si, GaAs and InP) devices of equal size. Smaller footprint enables operating a transistor at higher frequency due to reduced capacitive loading. Higher E_{cr} also helps reduce the on resistance which is very crucial to realising higher cut-off frequency and gain for RF applications. It allows a transistor to support high terminal RF voltage which is a component in realising high-power density. Equation 1.1 shows the relationship between on-resistance and critical electric field E_{cr}. It can be deduced that the higher the E_{cr}, the lower the on-resistance ($R_{DS(on)}$), which translates to much lower conduction losses in

GaN devices compared to Si. Lower on-resistance is fundamental component of realising high current gain cut-off frequency and high gain [18].

$$R_{DS(\ on\ )} = \frac{4V_{BR}^2}{E_{cr}^3 \varepsilon_s \mu_n} \tag{1.1}$$

Where $R_{DS(on)}$ is on-resistance, V_{BR} is breakdown voltage, e_0 is the permittivity of a semiconductor material, and μ_n is electron mobility.

Figure 1.5 illustrates the breakdown voltage and cut-off frequency for a different competing semiconductor material. These figures of merit are important figures for high-power high-frequency applications. As shown in the Figure 1.5, there is a trade-off between breakdown voltage and cut-off frequency, which GaN devices have the highest breakdown voltage below 200 GHz compared to other materials. GaN HEMTs have a great potential to outperform other competing materials for high-power in high-frequency applications. This makes GaN HEMTs very promising for W- and V- band applications.

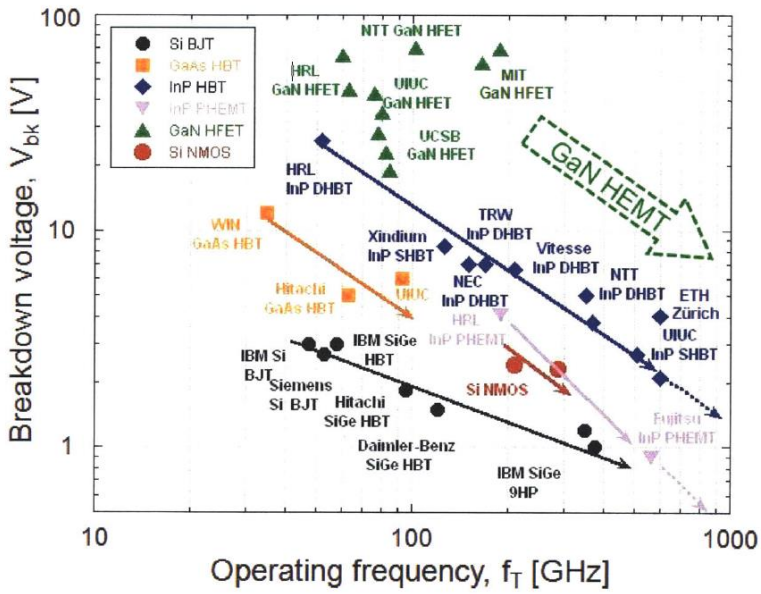


Figure 1.5 Trade-off between breakdown voltage (V_{Br}) and cut-off frequency (f_t) of transistors made from different material systems [19].

1.2.3 Electron Mobility

Electron mobility is a measure of how quickly an electron can move in a semiconductor material when subjected to an electric field. Electron mobility is a function of temperature, electric field, doping concentration and material quality of a semiconductor. Thus, switching loss can be reduced by using a semiconductor with higher electron mobility. Although the mobility of intrinsic Si (1400 cm^2/Vs) is shown to be higher than that of the intrinsic GaN material (~1000 cm^2/Vs), however, much high electron mobility up to 2000 cm^2/Vs can be obtained in form of 2-diemetional electron gas (2DEG) by appropriate growth of thin AlGaN layer on the GaN intrinsic material, as will be explained in detailed in Chapter 2, Section 2.5.

1.2.4 Thermal Conductivity

Thermal conductivity is a critical factor in the operation of wide band gap semiconductors devices for high-power density radio frequency applications. It is a measure of the extent of which a material can dissipate power to its surrounding. Heat generated due to the flow of current across the device raises the temperature of the device resulting in self-heating. If the heat is not extracted outside the device, the temperature will keep rising leading to output power poor performance and destructive breakdown of the device. Conventionally, cumbersome heat sinking system is used to maintain an optimum device temperature. However, the need for highly efficient compact systems necessitates the need to get rid of heat sinks or reduce their sizes to possible minimum. Device lifetime and size is the determining factor of the number of dies per wafer, which in turn dictates the cost, is dependent on the thermal conductivity of the material [20, 21]. As shown in Table 1.1, , thermal conductivity of GaN (1.3 W/cm.K) is significantly lower than its major competing semiconductor material, the silicon carbide (SiC = 4 W/cm.K), but much better than of InP and GaAs and about the same as that of Si.

1.2.5 Dielectric Constant

Dielectric constant determines the terminal impedances of a transistor. GaN has dielectric constant about 20% lower than the conventional semiconductor materials (GaAS and InP) which makes its transistors to be comparatively larger in area of for a given impedance resulting in high RF currents for higher power density [22].

1.3 Research Challenges

It is a fact that in recent years, apart from optoelectronic applications that gallium nitride (GaN) devices where originally meant for, significant progress has been achieved in the quest to replace Si technology with GaN in many high-power high-frequency applications. In literature, GaN HEMTs achieving a high drain current (I_{DS}) up to 3.5 A/mm [23], transconductance (g_m) up to 1.36 S/mm [24], cut-off and maximum oscillation frequencies up to 454 GHz [24] and 518 GHz [23] respectively have been reported. Although GaN transistors with RF power up to 800 W in the S-band range [25] and power density of 8.84 W/mm in W-band [26] have been demonstrated in literature, increasing power density is still desired for the growing needs in applications such as broadband satellites, 5G telecommunication and radar technologies. The constraint of achieving the projected target generally arises from the device design, material imperfections and seemingly unavoidable trade-offs between some fundamental performance parameters. Common problems are listed below are discussed in the next chapter:

- Current collapse and self-heating phenomena [27, 28]
- High cost of native GaN substrate [29].
- Lattice and thermal mismatches for GaN grown on affordable foreign substrate [30, 31]
- Ohmic contact resistance [32, 33].
- Thermal management and other reliability issues [34, 35].

1.4 Research Goals and Objectives

This project is intended to improve the processing technology of some RF GaN devices in the design and fabrication processes to mitigate the effect of some of the mentioned constraints and improve in the performance parameters. The goals are planned to be achieved through the following objectives:

1. Design and development of fabrication process for achieving a rugged dielectric free T-Gate structure for high-frequency applications.
2. Design and fabricate a low resistance ohmic contact using a cost-effective less time-consuming non-regrowth heavily doped cap layer.
3. Design and fabrication of GaN-on-diamond devices using three different epilayer structures to investigate the effect of self-heating, thermal and electric performance of the devices.

1.5 Thesis Structure

The thesis comprises 7 chapters. Chapter 1 provides the general background of the GaN material, why GaN is as important material for future power electronic applications and the major challenges the technology faces to date. The chapter further identifies key challenges of GaN as applied to high-frequency high-power applications and outlines steps taken in this project to minimise the critical challenges.

Chapter 2 is the literature review. The chapter reviews the previous works reported on GaN devices. It provides the operational mechanism and improvements made in the state-of-the-art GaN devices to suit modern day requirements in high-power high-frequency applications.

Chapter 3 explains the fabrications processes using various equipment in James Watt Nanofabrication Centre (JWNC), University of Glasgow. Photolithography and electron beam lithography metallisation, passivation processes etc are explained in detail.

Chapter 4 describes the robust, improved techniques of achieving a rugged T-gate structure on AlGaN/GaN devices without the need of dielectrics. It discusses the results obtained and their significance in the high-power RF applications.

Chapter 5 focuses on the realisation of low-resistance ohmic contacts with regrown-free heavily doped GaN cap. The fabrication process is discussed in detail followed by discussion on the results obtained and its contribution in high-power RF applications.

Chapter 6 gives an overview of the thermal constraints of the GaN devices on foreign substrates, the general fabrication process of AlGaN/GaN epilayers on diamond followed by a discussion of results and their significance in high-power RF applications.

Chapter 7 is the summary of this thesis with plans for future work.

Chapter 2

Literature Review on Gallium Nitride High Electron Mobility Transistor

2.1 Introduction

In the previous chapter, we discussed the limitations of silicon-based devices and the need for alternative materials in high-power, high-frequency applications. Gallium nitride (GaN), a III-V material, has gained attention due to its unique advantages. Among GaN devices, the heterostructure-based high electron mobility transistor (HEMT) stands out as a promising device. GaN HEMTs can produce a high concentration of a highly mobile two-dimensional electron gas (2DEG) without intentional doping. While other III-V nitride materials like gallium arsenide (GaAs) and indium phosphide (InP) have higher electron mobility than GaN, they are inefficient for high-power, high-temperature applications due to their low energy bandgap and thermal conductivity. GaN, on the other hand, exhibits a higher thermal conductivity and a wider energy bandgap, making it suitable for high-power, high-frequency applications.

2.2 Review on GaN Devices

GaN-based transistors can be classified into two types: vertical and lateral. Vertical GaN devices have been demonstrated in various research papers but are not yet commercially available. These devices are primarily designed for high-power applications such as high-power AC and DC converters. The commercially available GaN devices are mostly of lateral design and are commonly known as GaN HEMTs. In lateral GaN devices as shown in Figure 2.1, the current flows laterally from the drain to the source. GaN HEMTs have gained popularity due to their ability to generate a high concentration of 2DEG without the need for intentional doping. This allows for high current density with lower channel resistance.

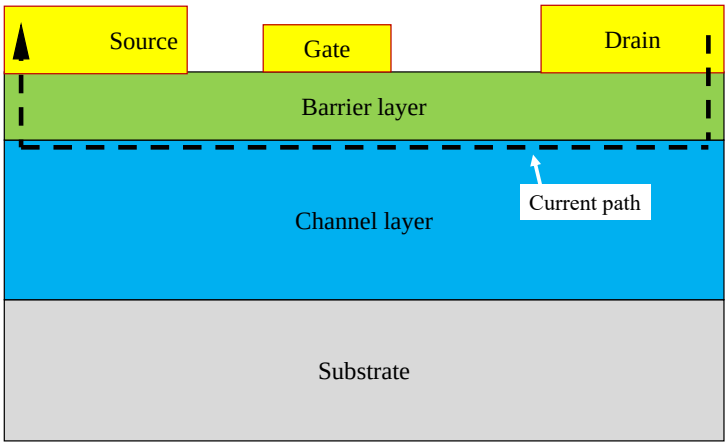


Figure 2.1 Lateral design of HEMT with current flow from drain to source.

2.3 GaN-based HEMTs for High-Power High-Frequency Applications

The AlGaN/GaN heterostructure is capable of generating a 2DEG with a high carrier density and high mobility. Since its first report in 1991 [36] and subsequent developments in 1993 [37, 38], GaN HEMTs have been extensively researched for their potential in high-power, high-frequency applications. The high carrier density (~1 × 10^{13}/cm^2) and high mobility (~ 2000 cm^2/V.s) of 2D electrons in GaN HEMTs make them suitable for such applications. GaN HEMTs offer several

advantages for high-power, high-frequency applications. They exhibit low on-resistance, high breakdown voltage, and fast switching speeds. These characteristics enable efficient power amplification and high-frequency signal processing. GaN HEMTs are widely used in RF amplifiers, wireless communication systems, radar systems, and satellite communications.

2.4 Basic Structure of GaN HEMT

A basic cross section of a GaN HEMT is shown in Figure 2.2. Thick GaN channel/buffer layer (typically 1 to 3 µm) is grown on a substrate followed by a thin AlGaN barrier layer, beneath which a 2DEG is naturally formed due to spontaneous and piezoelectric polarization effects at the GaN/AlGaN interface. The source and drain electrodes are fabricated to establish a low resistance ohmic metal-semiconductor contacts alongside Schottky gate. In order to reduce gate leakage current, a thin dielectric layer (usually of SiO_2, Si_3N_4 or high-κ dielectrics) is deposited (as shown in Figure 2.3) between the metal gate and the semiconductor layer (AlGaN). The oxide layer needs to be optimised to avoid introducing traps under the operational biases. However, In high-frequency devices, the dielectric layer has a significant impact on device performance. The presence of a dielectric layer increases the gate capacitance, which, in turn, lead to longer switching times and reduced high-frequency performance.

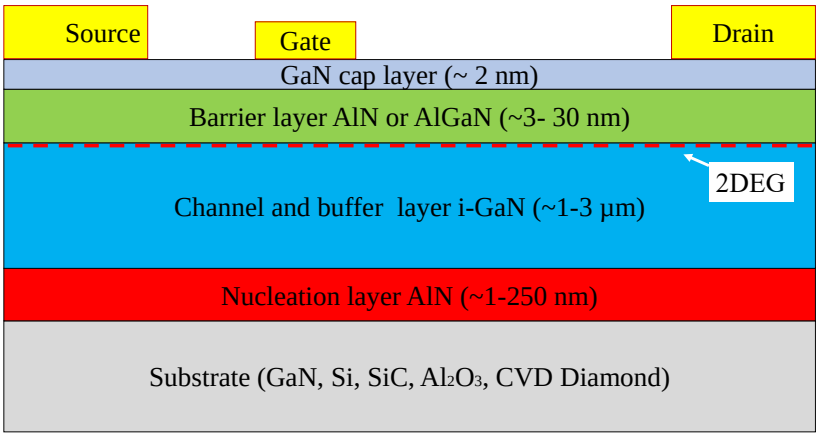


Figure 2.2 Basic GaN HEMT schematic structure.

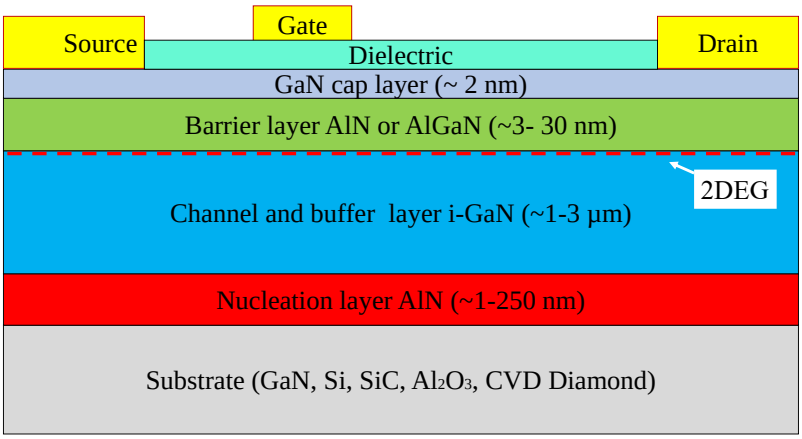


Figure 2.3 Basic GaN HEMT schematic structure with gate dielectric.

Growing GaN HEMT on foreign substrate such as Si and sapphire requires stress mitigation layers to relieve the channel layer from the effect of lattice and thermal expansion coefficient (TEC) mismatches responsible for defects and dislocations. For example, a step-graded Al-containing AlGaN buffer layers with variable thicknesses are often grown as reinforced GaN buffer on silicon substrates [39] (as shown in Figure 2.4). Epitaxial layers in GaN HEMT are commonly grown using metal organic vapour deposition (MOCVD) or molecular beam epitaxy (MBE) growth techniques. Although MOCVD is the commonly used grown technique for GaN HEMT, but MBE offers precise control over epitaxial film growth, allowing for accurate manipulation of layer thickness, composition, and doping. Operating under ultra-high vacuum conditions, it minimises impurity incorporation and produces high-purity films. MBE enables the growth of well-defined interfaces, resulting in sharp transitions in heterostructures. It produces high-quality single crystal films with excellent uniformity and crystalline quality, leading to high carrier mobility and improved device performance. Integrated in situ monitoring provides real-time feedback for precise control [40]. Below are the descriptions of some common GaN HEMT epilayers.

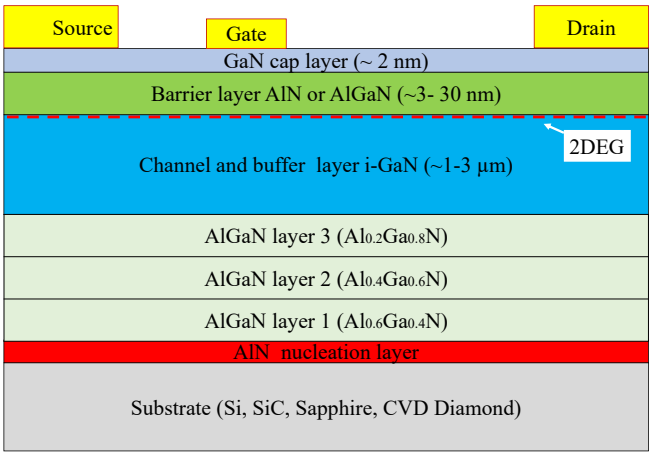


Figure 2.4 Stress mitigation layers such as nucleation and transition layers grown between GaN and substrate.

2.4.1 Cap Layer

In GaN-based high electron mobility transistors (HEMTs), the cap layer (undoped), typically composed of GaN, plays a crucial role in GaN-based high electron mobility transistors (HEMTs). It serves multiple functions in the device structure. Firstly, it prevents the relaxation of the barrier [41], leading to reduced gate leakage current by increasing the barrier height [42]. The cap layer also provides surface passivation, which helps in preventing oxidation and improving the density of the two-dimensional electron gas (2DEG) in the device [43]. Additionally, the lower band gap of GaN cap layer (3.4 eV) compared to the barrier layer (4-6.2 eV) helps in reducing the ohmic contact resistance in GaN HEMTs structure [44]. Furthermore, it has been observed that incorporating a p-doped GaN cap can improve the breakdown voltage of AlGaN/GaN HEMTs [45]. The typical thickness of a GaN cap in these devices ranges from 1 to 2 nm.

2.4.2 Barrier Layer

The barrier layer in a HEMT structure is of utmost importance as it determines the electron density and mobility in the two-dimensional electron gas (2DEG) channel. The choice of barrier material significantly influences the device performance. The two commonly utilised barrier layers are aluminium gallium nitride (AlGaN)

[46] and aluminium nitride (AlN) [47]. AlGaN barrier has been widely adopted in the GaN community due to its earlier development. It typically consists of varying Al-Ga ratios, usually ranging from 20% to 40%. Higher Al content increases the bandgap but may result in poorer material quality [48], although there have been reports of structures with Al content exceeding 40% [49]. The typical thickness of an AlGaN barrier is between 20 and 30 nm, and deviations in thickness can impact device performance. It's important to note that defect density significantly increases for Al content above 30% at a typical thickness of 20 nm.

AlN barrier has attracted increasing research attention as the technology employing AlGaN barriers approaches maturity. In AlN/GaN HEMTs, the bandgap can increase up to 6.2 eV [50], resulting in a higher charge density of up to $3X10^{13}$ cm^{-2} [51]. This increase in charge density is attributed to the significantly higher spontaneous polarization (spontaneous and piezoelectric polarizations explained in Section 2.5.3) present in AlN compared to $Al_{0.25}Ga_{0.75}N$ barriers, which have a bandgap of up to 4.0 eV and a charge density of $1x10^{13}$ cm^{-2} [52]. The use of AlN barriers offers the advantage of higher charge densities and wider bandgaps, leading to improved device performance. However, there are several challenges that need to be addressed when using AlN barriers. These challenges include growth-related issues, the realisation of ohmic contacts, and surface degradation during processing which leads to traps, higher power losses, and reduced efficiency. These aspects require further research and development to optimise the performance and reliability of AlN/GaN HEMTs. The thinner AlN barrier, typically around 3 nm, allows for aggressive device scaling, enabling higher current densities and frequencies.

2.4.3 Channel Layer

The channel and barrier layers are vital components in the formation of the two-dimensional electron gas (2DEG) within a heterostructure. The channel layer, positioned beneath the barrier layer, is typically thicker, often exceeding 200 nm, and possesses a lower band gap energy compared to the barrier layer. In GaN-based HEMTs, the channel layer is commonly made of GaN, which has a band gap energy of approximately 3.4 eV. This band gap energy is lower than that of the

barrier layer, such as $Al_{0.25}Ga_{0.75}N$, which has a band gap energy of 4.0 eV. The difference in band gap energies between the GaN channel and the barrier layer creates a confinement potential, leading to the formation of the 2DEG.

2.4.4 Nucleation Layer

The nucleation layer, typically made of AlN, is grown on the substrate to mitigate stress and lattice mismatch between the substrate and the subsequent layers, particularly the buffer layer. In the case of AlN/GaN HEMTs, the nucleation layer is typically around 20 nm thick, while for AlGaN/HEMTs, it is typically around 200 nm thick. The nucleation layer serves as a transitional interface, facilitating the growth of high-quality epitaxial layers above it. By reducing the strain and lattice mismatch, the nucleation layer helps to enhance the structural integrity and electrical properties of the device, ultimately improving its performance.

2.4.5 GaN on Substrate

Due to unavailability of larger size (>100mm) and low cost of GaN wafers, GaN HEMT structure is normally grown on foreign substrates such as SiC, Si or Sapphire. Growing GaN-on-GaN is the most desirable as it eliminates lattice constant and thermal expansion coefficient (TEC) mismatches. Table 2.1 shows the TEC mismatches of GaN with respect to its common substrates. A major challenge in growing GaN epilayers on foreign substrates lies on the critical issue of lattice and thermal mismatches between the two materials which significantly affects the quality of the material and therefore ultimately the frequency and power performances of the GaN transistors.

Table 2.1 Thermal and lattice mismatches of gallium nitride with respect to its common substrates [53]. Hexagonal Close-Packed (HCP) has a coordination number of 12 and contains 6 atoms per unit cell and Face-Cantered Cubic (FCC) has a coordination number of 12 and contains 4 atoms per unit cell.

Mismatch	**Si**	**SiC**	**Sapphire**	**AlN**	**GaN**
Crystal structure	FCC	HCP	HCP	HCP	HCP
Lattice constant (å)	5.43	3.08	4.758	3.112	3.189
Lattice mismatch (%)	-16.9	3.5	16.08	2.4	-
Thermal expansion (10^{-6} k)	3.59	4.3	7.3	4.15	5.59
Thermal mismatch (%)	55	30	-23	34	-

2.4.5.1 GaN-on-Silicon

Due to low cost and availability of large wafer size (up to 12 inches), Si wafers have been the predominantly used substrates for electronic GaN devices. As shown in Table *2.1*, the percentage lattice and thermal mismatches for GaN on silicon is around 17% and 55% [53], respectively. In the typical GaN-on-Si HEMT structure, several interlayers (discussed in the previous section) are typically introduced to relieve the mismatch stress on the active regions. Such include nucleation and superlattice layers apart from the thick GaN buffer. On the other hand, the mismatch in the thermal expansion coefficients for the growth of GaN on Si result in thermal stress during the post-growth cooling leading to cracks [54, 55].

2.4.5.2 GaN-on-SiC

Growing GaN-on-SiC yields the smallest lattice constant mismatches due to the closeness in their lattice as shown in Table 2.1. Owing to the high thermal expansion coefficient of SiC, devices fabricated on the GaN-on-SiC materials exhibit efficient heat extraction property compared to GaN on silicon substrate or sapphire. However, there is still exists some lattice mismatch and so an AlN interlayer is commonly grown between the GaN epilayers and the SiC substrate

[30]. Because AlN is a good wetting agent on the SiC, and its intermediary lattice constant between GaN and SiC, its presence enhances significantly improves quality growth of GaN on SiC. The influence of TBR on the effective heat transport from the GaN to the SiC substrate is one of the limitations of AlN interlayer on SiC. Other problems include high cost and smaller diameter of the GaN-on-SiC wafer (commonly 6” or less).

2.4.5.3 GaN-on-Sapphire

The technology for growing GaN on sapphire is very mature due to its use in the light emitting diodes (LED) applications. It is comparatively less expensive, however, due to its poor thermal conductivity (0.3 W/cm.K) [11], it is unsuitable for high-power high-frequency applications. High lattice mismatch (Table 2.1: ~16%) is another disadvantage of deploying GaN-on-sapphire technology in high-power high-frequency applications [56].

2.4.5.4 GaN-on-CVD Diamond

GaN-on-diamond technology has in recent years become common due to the need for an efficient heat extraction technology. The thermal conductivity of (CVD) diamond (2000 W/mK) is much higher than any of the substrates GaN is commonly grown on. Apart from the high thermal conductivity, large GaN-on-CVD diamond are available with reasonable sizes (4 inches) [57]. Complexity of growing GaN on diamond and high cost are some of the major limitations of the technology.

2.5 Generation of Two-Dimensional Electron Gas (2DEG)

Two-dimensional electron gas is a sheet of electrons confined to move in only two directions. It generated under the influence of crystal polarization when two dissimilar wurtzite materials are brought together. The process of the generation of the 2DEG is discussed in the section below.

2.5.1 N-polar vs Ga polar growth in GaN

There are two ways of growing GaN, either N-polar or Ga polar. In N-polar GaN, the nitrogen atoms occupy the surface positions, and the crystal growth occurs along the c-axis, which is the vertical direction of the crystal lattice. N-polar GaN has unique electronic and optical properties, including a higher two-dimensional electron gas (2DEG) mobility and lower interface trap density compared to Ga-polar GaN. The higher 2DEG mobility in N-polar GaN makes it attractive for certain device applications, especially in high-frequency and high-power devices like HEMTs. However, N-polar GaN is less commonly used in commercial applications due to challenges in crystal growth and device processing. The growth of high-quality N-polar GaN is more difficult compared to Ga-polar GaN, limiting its widespread adoption [58-60].

In Ga-polar GaN, the gallium atoms occupy the surface positions, and the crystal growth also occurs along the c-axis. Ga-polar GaN is more commonly used in practical applications because it is easier to grow high-quality crystals and process devices compared to N-polar GaN. Ga-polar GaN devices have excellent performance in various applications, including high-frequency RF devices, power electronics, and optoelectronic devices like LEDs and laser diodes. The dominant use of Ga-polar GaN in commercial applications is primarily due to its superior crystal growth properties and better device manufacturability. Overall, while N-polar GaN offers unique advantages in certain cases, Ga-polar GaN remains the more widely adopted orientation in commercial semiconductor device manufacturing due to its better growth characteristics and processability [58, 59, 61].

2.5.2 Polarization in GaN and AlN Crystal Structures

Like other wurtzite group III nitrides, GaN and AlN are direct band gap semiconductors, highly piezoelectric, having a hexagonal lattice structure constituting four atoms per unit cell. Due to their piezoelectric property, they

exhibit a polarization behaviour known as piezoelectric polarization. As mentioned in Chapter 1, because of the non-Centro-symmetricity in the lattice structure, and the strong ionization factor of the metal-nitrogen bond [62], the materials exhibit a large polarization along the hexagonal *c*-axis. This polarization is called spontaneous polarization.

2.5.3 Spontaneous and Piezoelectric Polarizations

The spontaneous and piezoelectric polarization properties found in GaN and AlN is ten times larger than other III-V and II-VI nitride materials [63]. The wurtzite GaN crystal structure is formed by two closely spaced hexagonal layers of gallium and nitrogen atoms. In the wurtzite structure, the centre of the positive ion does not coincide with the centre of the negative ions resulting in a polarization as shown in Figure 2.5. The polarization shift along *c*-axis and can add-up microscopically to cause an electric field of up to 3 MV/cm [63]. This type of polarization is called spontaneous polarization because it occurs without any external influence.

Growing a thin layer of AlGaN epitaxially on a thick layer of GaN material results in piezoelectric polarization due to the strain caused by the lattice mismatch between the two materials as shown in Figure 2.5. This polarization can cause high piezoelectric field (up to 2 MV/cm) [63]. Since the two materials have different lattice constants, during growth, the lower (thicker) GaN layer tends to keep its original lattice constant, causing a strain of the top thinner AlGaN layer such that it grows with the same lattice mode as the lower GaN layer as illustrated in Figure 2.6.

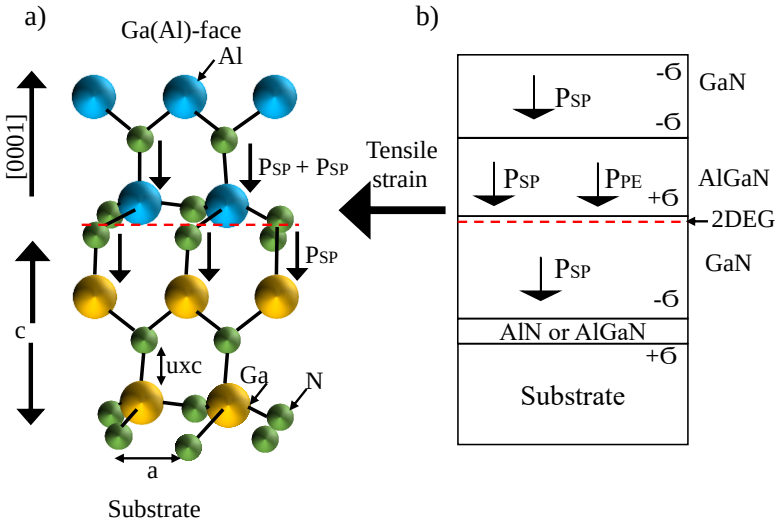


Figure 2.5 (a) Illustration of crystal structure of Ga (Al) face, (b) polarization induced sheet charge and direction of the spontaneous and piezoelectric polarization in Ga-face strained AlGaN/GaN heterostructures [64].

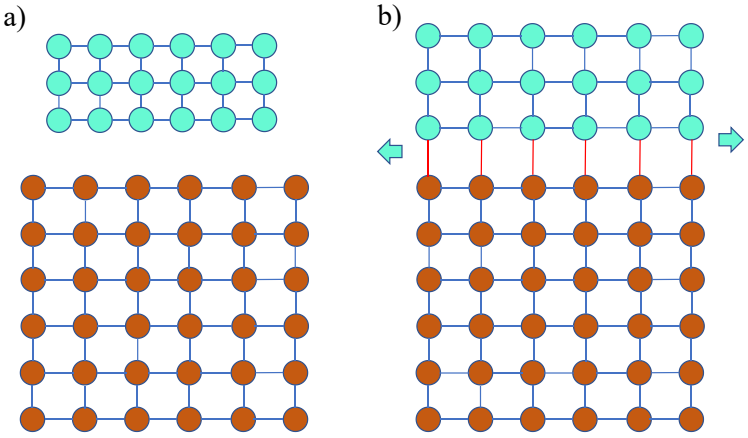


Figure 2.6 Growth of the materials with different lattice constant, (a) before growth and (b) after growth.

For a given aluminium mole fraction (x), the value of the piezoelectric polarization (P_{PE}) along the *c*-plane can be determined from Equation 2.1, and the polarization increases with increasing strain of the AlGaN layer.

$$P_{PE} = 2\frac{a(x) - a_0(x)}{a_0(x)}\left(e_{31}(x) - e_{33}(x)\frac{C_{13}(x)}{C_{33}(x)}\right) \qquad (2.1)$$

Where a (x) and a_0 (x) are lattice constant, e_{31} and e_{33} are piezoelectric coefficients, C_{13} and C_{33} are elastic constants.

The total induced polarization charge density, σ at the $Al_X Ga_{(1-X)}$ N/GaN interface given by Equation 2.2.

$$\sigma(x) = P_{SP,AlGaN}(x) + P_{PE,AlGaN}(x) - P_{SP,GaN} \quad (2.2)$$

where $P_{SP,\ AlGaN}$ (x) is the spontaneous polarization and x is the aluminium mole fraction in the AlGaN layer, $P_{PE,\ AlGaN}$ (x) is the piezoelectric polarization and x is the aluminium mole fraction in the AlGaN layer, and $P_{SP,GaN}$ is the spontaneous polarization GaN layer.

Owing to the fact that the induced charge density, σ depends on the bandgap differences between the two dissimilar materials, increasing the aluminium mole ratio of the strained AlGaN layer results in the increase in the polarization.

$$E_g(x) = xE_g^{AlN} + (1-x)E_g^{GaN} - bx(1-x) \quad (2.3)$$

The bandgap of the AlGaN can be modulated using Equation 2.3 where *x* is the aluminium mole ratio, *b* is the bowing parameter and E_g is the energy bandgap of the material. When the bandgap of AlGaN is appropriately tuned by increasing the aluminium content, the polarization induced density increases. The piezoelectric field results in the band bending forming a potential well at the AlGaN/GaN interface. The energy band diagram of AlGaN/GaN structure is shown in Figure 2.7.

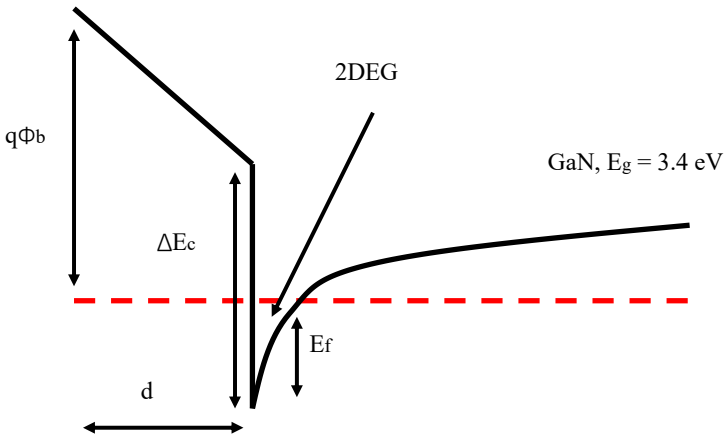


Figure 2.7 Energy band diagram of AlGaN/GaN.

2.6 Operation of GaN HEMTs

A basic structure of HEMT is shown in Figure 2.8. Because of the presence of the 2DEG directly shorting the source and the drain, GaN HEMT are naturally depletion mode devices as shown in Figure 2.8 (a). By applying drain-source bias voltage, electrons move from source to drain at zero gate voltage. At positive gate voltage (1 V or 2 V), the drain current increases further. To turn the transistor off, a negative gate bias must be supplied which eventually depletes the 2DEG exposed to the gate potential beneath, thus preventing further flow of current from drain to the source as shown in Figure 2.8 (b).

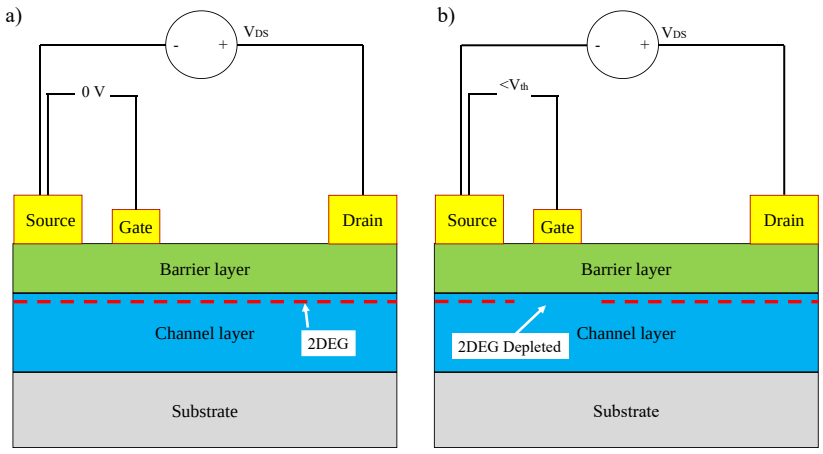


Figure 2.8 D-mode HEMT in general, (a) at V_{GS}= 0 V current flow from source to drain, and (b) Appling negative gate voltage to turn-off the transistor.

GaN-based HEMTs function similarly to conventional field effect transistors (FETs). During operation in the linear region, the current flowing between the source and drain results from the charge present in the channel and the time taken for this charge to move across the channel due to an applied voltage. The time required for electrons to traverse the channel with an effective velocity (v_{eff}) is given by the ratio L_{DS}/v_{eff}. Furthermore, the total charge in the channel is expressed as qn_s ($L_{DS}W_G$), where qn_s denotes the charge density and $L_{DS}W_G$ is the product of the drain-source separation and the gate width. So, the output current can be achieved using the following equation:

$$I_{DS} = \frac{qn_s L_{DS} W_G}{\frac{L_{DS}}{v_{eff}}} = qn_s v_{eff} W_G \quad (2.4)$$

Where I_{DS} is the output current, q is the electron charge, n_s is the sheet carrier concentration, L_{DS} is the drain-source separation, W_G is the gate width, and v_{eff} is the effective velocity of the electrons in the channel. The electrons' velocity can be calculated using the applied electric field and the mobility of the electrons in the channel, expressed as follows:

$$v_{eff} = \mu_n E_{cr} = \mu_n \frac{V_{DS}}{L_{DS}} \quad (2.5)$$

Where μ_n is the mobility of the electrons in the channel, E_{cr} is the applied electric field, and V_{DS} is applied voltage between source and drain.

Figure 2.9 illustrates the typical current-voltage characteristic of a GaN HEMT. It demonstrates the drain current behaviour as the drain voltage is increased for specific gate voltages. With the increase in gate voltage, more electrons accumulate in the 2DEG channel, consequently leading to a rise in the drain current.

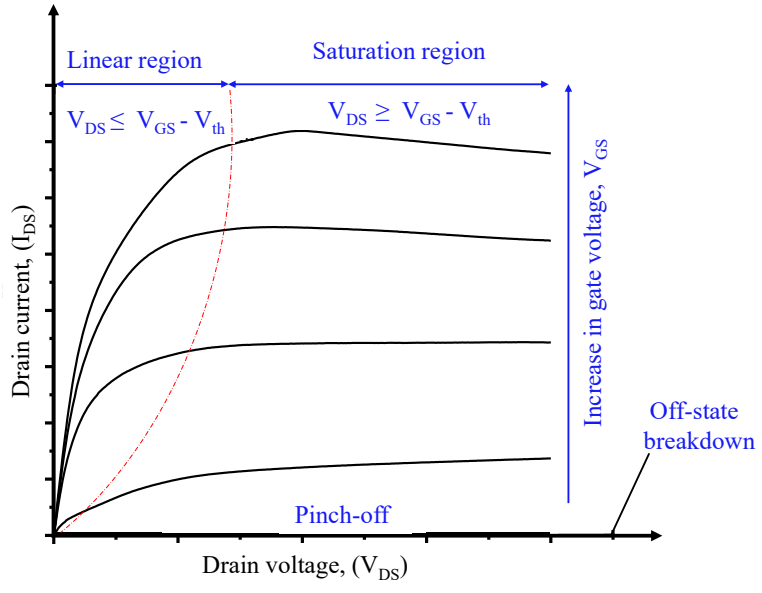


Figure 2.9 DC Output current-drain (IV) characteristic of a typical GaN HEMT.

Using the following relationship, the charge in the channel can be expressed in terms of the gate voltage.

$$Q = CV \tag{2.6}$$

Where C is the gate capacitance, and V is the effective voltage ($V = V_G - V_{th}$). The gate capacitance can be expressed using the following equation:

$$C = \frac{\epsilon L_G W_G}{d_{barrier}} \tag{2.7}$$

Where $d_{barrier}$ is the barrier thickness, and L_G and W_G are the gate length and width respectively. The gate metal and 2DEG channel can be regarded as a capacitor, which allows the sheet charge density to be expressed as:

$$n_s = \frac{\epsilon_{barrier}}{q(d_{barrier} + \Delta d)}(V_G - V_{th}) \tag{2.8}$$

Where n_s is the sheet charge density, Δd is the distance of the 2DEG from the heterointerface, V_G is the gate voltage, and V_{th} is the threshold voltage. At the point where the gate voltage equals the threshold voltage, the sheet charge density becomes zero, blocking the current flow between the source and drain.

In the low drain voltage regime, where $V_{DS} < V_G - V_{th}$ (linear region as shown in Figure 2.9), the electron velocity is linearly related to the electric field strength. However, at high drain biases, $V_{DS} > V_G - V_{th}$ (saturation region as shown in Figure 2.9), the effective electron velocity reaches a saturation point, becoming independent of the drain bias. This saturation is caused by electron scattering and leads to a pinch-off of the channel at the drain end of the gate. Consequently, the channel gradually restricts the flow of electrons, limiting their quantity and causing the device to operate in the saturation region. To achieve high output powers, devices are typically biased with high drain voltages. In this scenario, the drain current is calculated using following equation:

$$I_{DS} = \frac{\epsilon_{barrier} v_{sat} W_G}{d_{barrier} + \Delta d}(V_G - V_{th}) \tag{2.9}$$

Transconductance (g_m) is a measure of the change in drain current concerning the change in gate voltage at a specific operating point in a field-effect transistor (FET) or HEMT voltage. It can be define as follow:

$$g_m = \frac{\delta I_{DS}}{\delta V_G} \tag{2.10}$$

Where δI_{DS} is change in drain current, and δV_G is the change in gate voltage.

2.7 Critical Issues Affecting GaN-based HEMTs

Although GaN HEMT is deeply researched, there critical issues affecting the performance of the device still not satisfactorily solved. Some of these challenges are discussed in the following sections.

2.7.1 Current Collapse

GaN HEMTs are susceptible to a phenomenon called current collapse, where the actual current capability of the device is reduced during operation. This phenomenon is attributed to the trapping of electrons at the surface or within the bulk of the epitaxial layers. It is believed that trap levels are generated during the crystal growth stage and device processing in a heterostructure. Current collapse leads to an increase in the device's on-resistance, posing a significant challenge for GaN devices to be effectively used in power switching applications. Additionally, it results in reduced transconductance for RF devices, further impacting their performance. Addressing and resolving current collapse is crucial for the successful deployment of GaN devices in practical applications.

To suppress current collapse in RF devices, several strategies can be employed. Passivation techniques involve applying dielectric layers [65, 66] to the device surface to reduce surface states and enhance interface stability, improving linearity and transconductance [67, 68]. Material and process optimisation, such

as optimising crystal growth and fabrication processes, can minimise trap generation and enhance RF performance. Interface engineering focuses on optimising heterostructure interfaces to minimise trap formation and scattering, leading to improved RF characteristics [69].

2.7.2 Effect of Material Mismatches

As mentioned early, lack of availability of high-quality and large size GaN wafers made GaN heterostructures to be grown on foreign substrates such as silicon, silicon carbide and sapphire. Thermal and lattice mismatches that occur during epitaxy result in dislocations as illustrated in Figure 2.10, causing serious issues in GaN-based device technology. The dislocations generated in the buffer during growth due to mismatches results in a high density of free carriers which significantly affect the electrical properties of the GaN HEMT especially breakdown voltage. The GaN buffer which is originally intended to be of high resistivity to prevent drain leakage and AC coupling, exhibits a background doping, typically n-type, requiring the introduction of p-type dopant to compensate for the n-type and retain the resistive property of the layer, as a result Carbon (C) or iron (Fe) are commonly used as p-type dopants. Figure 2.11 shows the relationship between density of carbon doping and the off-state breakdown voltage of GaN material. To limit the transmission of mismatch stress to the GaN buffer, multiple interlayers are usually transitionally grown between the substrate and the GaN layer depending on the type of substrate used. Example of such layers include nucleation and AlGaN inter layers shown in Figure 2.4.

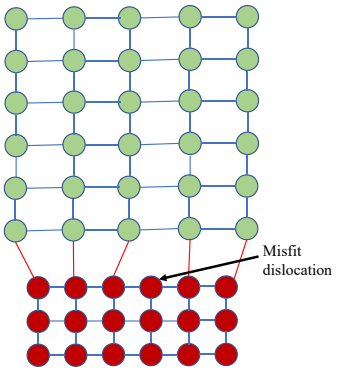


Figure 2.10 Thermal and lattice mismatches that occur during epitaxy result in dislocations.

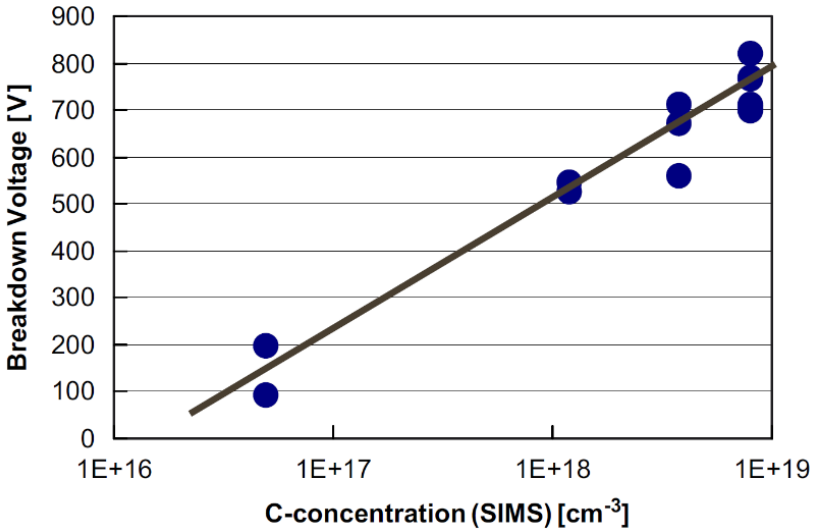


Figure 2.11 Relationship between C-doping concentration and off-state breakdown voltage in GaN [5].

2.8 Formation of Ohmic Contacts

For efficient operation of transistor devices, low resistance thermally stable ohmic of the device's performance including frequency response and noise performance, output power and efficiency. In the RF application, ohmic contacts provide efficient electrical connections, low resistance, high thermal stability, and good RF matching, enabling optimal signal transmission and maximising device performance in high-frequency operation [70, 71].

Emission of electrons from metal to the semiconductor is determined by the height potential barrier formed when two materials are intimately joined together. When the contact is made, electrons flow from the semiconductor to the metal until the fermi energy of the two materials come to equilibrium and a potential barrier is formed which electron must overcome to further move from the semiconductor to the metal. This potential barrier is a rectifying contact which allows a flow of current only from the metal to the semiconductor depending on the height. Depending on the metal work function, the height of the barrier for electrons is determined by the electron affinity of the semiconductor material and the metal work function. Figure *2.12* illustrates the energy band diagrams at the interface between the metal and the n-type semiconductor contact. Due to the abrupt

discontinuity of the semiconductor material at the junction, interface charges whose energy level occupy a state within the bandgap can influence the barrier height by pinning the Fermi-energy, thereby discrediting the dependence of the height on any of the materials property (energy bandgap or metal work function). To establish an ohmic contact, the Fermi energy must be raised towards the edge of the conduction band, and this is achieved by altering the intrinsic property of the semiconductor through doping. The higher the doping density, the lower will be the barrier height. The heavily doped cap layer forms a narrow barrier through which electrons tunnel.

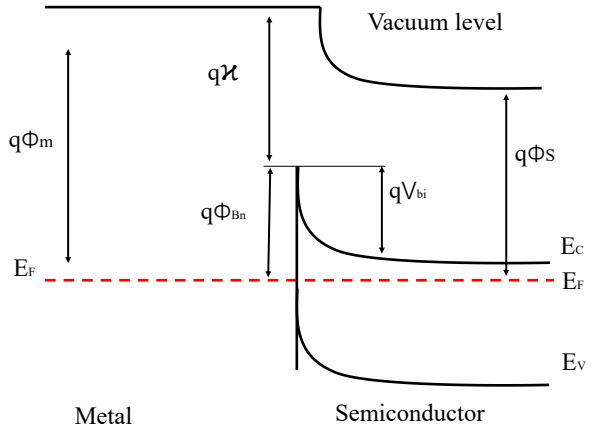


Figure 2.12 Energy band diagram for metal – semiconductor contact in thermal equilibrium. Where $q\Phi_m$ is metal work function, qX is electron affinity, $q\Phi_{bn}$ is barrier work function, qV_{bi} is built in voltage, $q\Phi_S$ is the semiconductor work function, E_c is conduction band, E_F is fermi level, and E_V is the valance band.

Generally, it is easier to form ohmic contacts on materials with lower energy band gaps. Lower band gap materials tend to have a higher density of available states for carrier injection, making it easier for current to flow through the contact interface. This can result in lower contact resistance and better ohmic behaviour. However, in GaN HEMTs, due to wide bandgap and large electron affinity, achieving low resistance ohmic contacts with III-nitride materials are comparatively more difficult than conventional semiconductors resulting in the high Schottky barrier [6]. This is because the metals do not have low enough work function to establish a low Schottky barrier height. In AlGaN/GaN heterostructure, low ohmic contacts are achieved by high temperature annealing (~800°C). Ti/Al/Ni/Au is the ohmic contact metal stack conventionally used for GaN-based

HEMT devices. In the AlGaN/GaN-Ti ohmic contact topology, Titanium reacts with nitrogen to form TiN resulting in the formation of the nitrogen vacancies which act as donors in the AlGaN layers which facilitate tunnelling of the n-type carriers at the interface [72]. ohmic contacts using Ti/Al/Ni/Au were reported with a contact resistance as low as resistance (~0.2 Ω.mm) [73, 74] with high temperature annealing. Non-annealed ohmic contacts were also reported with lower ohmic contact resistance (~0.025 Ω.mm [75]) by etching the ohmic contact regions down to channel layer and regrowing the areas with heavily doped GaN [23], however, this regrowth adds to manufacturing cost and complexity. A 0.12 Ω.mm was reported Y. Lu et al [72] by recessing part of the contact to form an array of square columns which the metal stack rests upon. In Section 2.9.2, the dependence of frequency response on the contact resistances in discussed and shows the critical roles played by device contacts in obtaining efficient high-power high-frequency performance.

2.9 GaN HEMT for High-Frequency Applications

Technological developments in wireless communications, radar, space exploration etc requires ultra-speed semiconductor devices capable of operating at microwave (0.3-100 GHz) and millimetre wave (100-300 GHz) frequency spectrum depending on the application. The ability of gallium nitride HEMT to effectively meet these performance requirements lies in its high electron mobility, the high saturated velocity, and the large wide bandgap (which enables achieving higher voltages at smaller device footprint). The most important performance metric of a material in high-power high-frequency transistors are the unity gain cut-off frequency (also known as maximum frequency of oscillation) which determines the bandwidth gain [76]. The Johnson figure of merit is used to judge the performance of RF device.

2.9.1 Johnson Figure of Merit

Johnson figure of merit (JFOM) [77], is a metric used to evaluate the performance of a HEMT or other RF power devices. The Johnson figure of merit expressed in Equation 2.4 [78], shows the reliance of the ultimate power and frequency

performance of a transistor on the critical electric field (E_{cr}) and the saturated drift velocity (v_s) of the semiconductor material.

$$\text{JFOM} = \frac{E_{cr} \cdot v_s}{2\pi} \tag{2.11}$$

Where E_{cr} is the critical electric field and vs is the saturated drift velocity (v_s) of the semiconductor material.

Table 2.2 gives some of the contending semiconductor materials and their respective JFOM. A higher Johnson FOM indicates better performance in terms of power handling capability and high-frequency operation. It evaluates and compare the high-frequency performance of semiconductor devices, particularly in radio frequency (RF) applications. Because of the high E_c and v_s, GaN shows a better performance metric compared to Si or GaAs.

Table 2.2 JFOM of some of the semiconductor materials [79].

Semiconductors	**Si**	**GaAs**	**SiC**	**GaN**	**Diamond**
E_C (V/cm*10^6)	0.3	0.4	2.4	3	5.7
v_s (cm/sec*10^7)	2.3	4.4	1.9	1.5	2.7
JFOM	1	2.55	6.61	6.52	22.3

2.9.2 Baliga High-Frequency Figure of Merit

Equation 2.12 is the Baliga high-frequency figure of merit (BHFFOM) which defines the fundamental relationship between the high-frequency and the material property of semiconductor [78]. It relates the influence of the carrier mobility in the minimisation of switching losses in the power field effect transistor devices as defined in Equation 2.12.

$$\text{BHFFOM} = \mu_n \cdot E_G^2 \cdot \sqrt{\frac{V_G}{4V_{Br}^3}} \tag{2.12}$$

Where μ_n is electron mobility, E_G is the bandgap of the semiconductor, V_G is the gate drive voltage, and V_{Br} is the breakdown voltage.

2.9.3 Frequency Response of GaN HEMT

Some state-of-the-art RF devices are in Table 2.3, showing contacts resistances and frequency parameters. GaN HEMTs have made significant advancements in frequency coverage, enabling their deployment in high-speed and high-power applications across a wide range of frequencies, from several gigahertz (41.4 W/mm at 4 GHz [80]) up to several hundred gigahertz (296 mW/mm at 180 GHz [81]). To achieve a high gain amplification in millimetre wave application (30-300 GHz), for example, the maximum frequency of oscillation (f_{max}) or unity power gain requires to be increased [46]. The small signal model is an essential tool for analysing the behaviour of transistors, including HEMTs. It provides a simplified equivalent circuit representation that focuses on the linear operation of the device and allows for the analysis of small variations around the bias point.

Table 2.3 Some state-of-the-art GaN RF HEMTs showing resistance and RF frequency performances.

L_g [nm]	R_C [Ω.mm]	R_{on} [Ω.mm]	I_{Dmax} [A/mm]	Gm [S/mm]	f_t [GHz]	f_{MAX} [GHz]	Ref	year
50	0.1	-	1.65	0.553	170	347	[82]	2023
50	0.43	-	1.6	0.415	125	270	[83]	2021
100	0.16	0.54	1.85	0.525	88	204	[26]	2020
40	0.13	1.3	2.3	0.6	161	70	[84]	2019
110	0.45	-	1.2	0.4	63	300	[32]	2019
90	0.25	-	1.2	0.461	98	322	[73]	2018
40	-	0.95	1.5	-	140	280	[85]	2017
60	-	1.29	1.65	0.65	183	191	[86]	2017
90	0.32	1.4	1.25	0.33	113	160	[33]	2017
20	-	0.26	3	1.36	454	444	[24]	2015
27	0.1	0.3	2	1.0	302	301	[87]	2013
40	0.27	-	1.8	0.77	230	300	[88]	2013
80	0.09	0.42	1.7	-	148	351	[89]	2012
20	0.101	0.23	4	1.0	342	518	[23]	2012
60	0.025	0.29	2.77	1.105	260	20	[75]	2012

Figure 2.13 illustrates this small signal model. In the small signal model of a HEMT, various components such as resistors, capacitors, and current sources are included to represent the different elements of the transistor structure and their effects. These components enable the characterisation of the device's input and output impedance, transconductance (g_m), output conductance (g_{DS}), and capacitances. By employing the small signal model, engineers can analyse and design HEMTs for specific applications, particularly in amplifier design. The model enables the examination of the transistor's small signal response to input signals, facilitating the determination of key parameters such as gain, bandwidth, noise figure, and stability. This information is crucial for predicting and optimising the performance of HEMTs in high-frequency applications, where small signal behaviour plays a critical role.

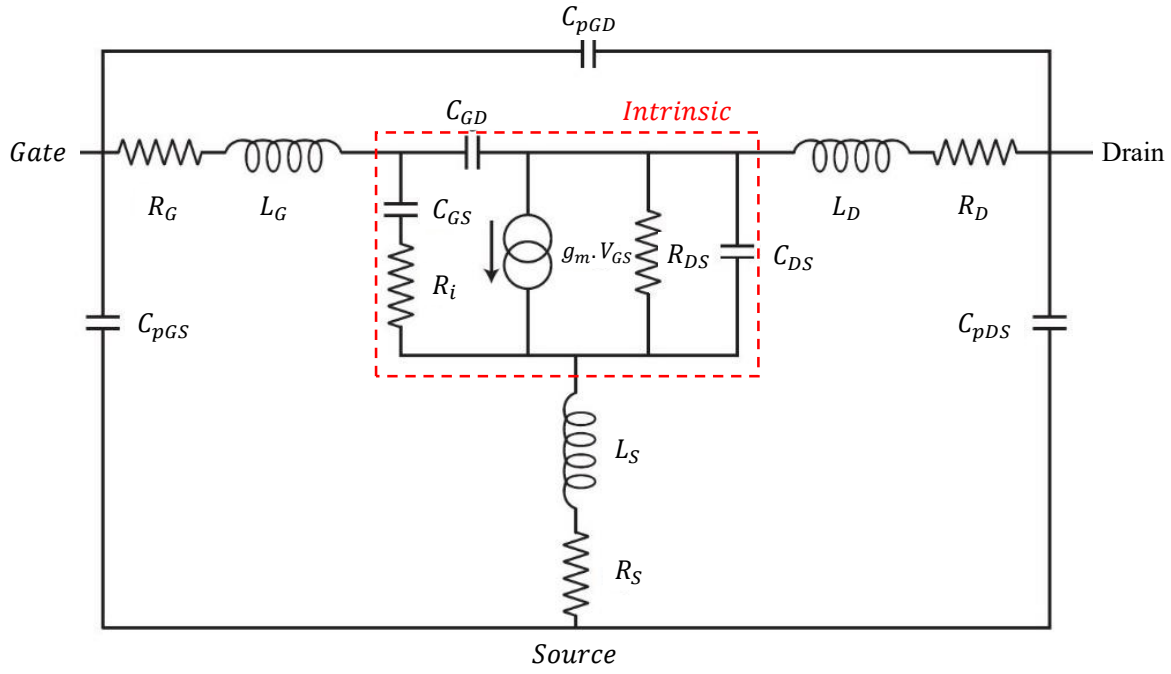


Figure 2.13 HEMT small-signal equivalent circuit model.

Where g_mV_{GS} is the current source that is controlled by voltage across gate capacitance, R_{DS} is output resistance, the inverse of output conductance, C_{GS} is source gate capacitance and controls current source, C_{GD} is the drain gate capacitance, half of the distributed capacitance, R_i is the intrinsic channel resistance that models the finite conductance of the channel, C_{DS} is the source-drain capacitance that models transverse capacitance along channel due to varying electron density, C_{pGS} and C_{pGD} are parasitic gate capacitances for source

and drain respectively, C_{pDS} is parasitic source-drain capacitance. In Equation 2.5 and 2.6, the f_{max} is expressed in terms of the current gain (cut-off frequency (f_t)), the gate-drain capacitance (C_{GD}), and input, source, gate and output resistances (R_i, R_S, R_G and R_{DS} respectively). To obtain a high f_{max} and f_t, the contact must be effectively reduced.

$$f_{max} = \frac{f_t}{2 * \sqrt{(R_i + R_S + R_G)g_d + 2\pi f_t R_G C_{GD}}} \tag{2.13}$$

$$f_t = \frac{g_m}{2\pi(C_{GS} + C_{GD})\left(1 + \left(\frac{R_S + R_D}{R_{DS}}\right)\right) + C_{GD} g_m (R_S + R_D)} \tag{2.14}$$

Unity gain cut-off frequency (f_t) is related to the effective saturation velocity v_{sat} and the gate length (L_G) from Equation 2.7 [76]. While v_{sat} is a material property, gate length can be used to scale the cut-off frequency.

$$f_T = \frac{v_{sat}}{2\pi L_G} \tag{2.15}$$

2.9.4 Size Scaling for High-Frequency Operation

In GaN HEMTs, gate length is one of important device parameters that determines the operating frequency. Because the smaller device size plays a key role in achieving high operating frequency, device size is scaled by scaling the gate length, the gate-drain and gate-source spacing. Smaller gate lengths, gate-source, and gate-drain spacing is significantly required while scaling down the device footprint. Sub-nanometre gate lengths result in reduced capacitances which enables high-frequency operation. Figure 2.14 shows the typical relationship between gate length (L_G) and current gain cut-off frequency (f_t) [90]. Since high breakdown voltage of HEMT is determined by the gate to drain spacing as shown in Figure 2.15 [91], this translates to a compromise between high-frequency and breakdown voltage of the device.

As the gate length is made smaller, the parasitic gate resistance becomes larger increasing proportionally as $1/L_g$ which deteriorates the transconductance and the frequency response of the device [92]. The parasitic gate resistance (R_G) can be reduced by employing T-Gate technology, with head and foot as shown in Figure 2.16. The wider the head, the lower the R_G, but larger the gate capacitance [92]. Thus, the T-gate structure has to be properly optimised by properly trading-off between the scaling parameters. T-shape gates at sub nanoscale have been demonstrated in the literature and will be discussed in Chapter 4, where they are summarised in Table 4.1. Figure 2.16 shows a typical T-gate structure of GaN HEMT consisting of gate foot and head.

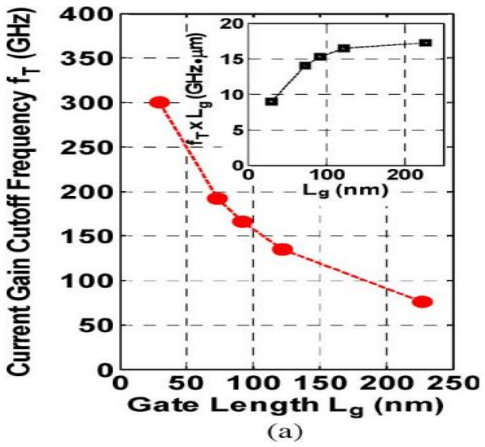


Figure 2.14 Relationship between gate length (L_G) and cut-off frequency (f_t) [90].

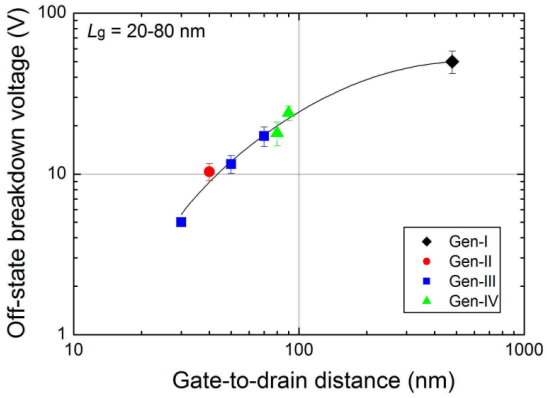


Figure 2.15 Relationship between gate to drain spacing and off-state breakdown voltage [91].

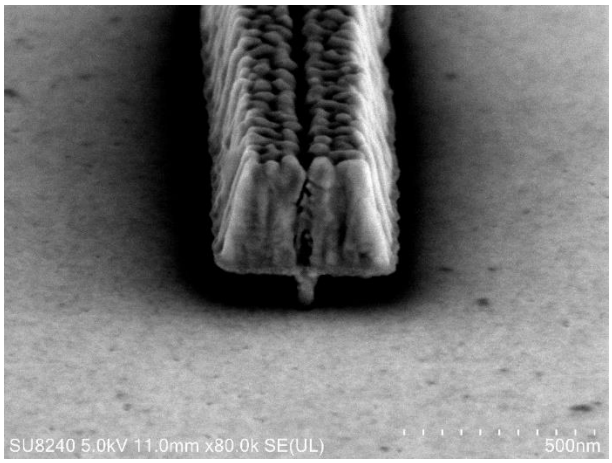


Figure 2.16 SEM scan of a T- shape gate.

2.10 Summary

This chapter offers a comprehensive examination of GaN HEMTs, encompassing key aspects ranging from the structure of the epitaxial layers to the operational principles of the devices. It delves into the formation of the 2DEG channel, the process involved in creating ohmic contacts, and the impact of spontaneous and piezoelectric polarization on the formation of the channel. Additionally, the chapter highlights the significance of the small signal equivalent circuit model in comprehending the behaviour of GaN HEMTs, and it explores the methods for determining the cut-off frequencies of the transistors. Overall, this chapter provides a thorough understanding of the theoretical foundations and principles that underpin GaN HEMTs.

Chapter 3

Device Fabrication Techniques and Characterisation

3.1 Introduction

This chapter describes the general techniques of device fabrication and characterisation. It focuses on the GaN based HEMT structures. Fabrication techniques are crucial for realising a functional, performing device. Using effective recipes is a fundamental need for various fabrication steps. The chapter describes processes with illustrations of various fabrication steps from material growth through sample preparation, lithography, mask plate production, metallisation, mesa isolation and annealing to a complete device structure. The chapter further illustrates the fundamental techniques for device measurements and characterisation out of which the device performances are analysed. This is a necessary requirement which enables obtaining basic device parameters used to analyse effectiveness of the design and fabrication process.

3.2 Epitaxial Material Growth

Epitaxial material growth is the process of forming a crystalline film of a particular material species on top of another crystalline film or substrate through a single or repeated atomic layering, in suitable growth conditions and parameters such as temperature, pressure and flow rates. When the grown materials are made from the same material, the process is referred to as homoepitaxy, otherwise heteroepitaxy. Because our focus is on AlGaN/GaN based heterostructures, the technique of reference is generally heteroepitaxy. Two main techniques that are commonly used to grow GaN-based heterostructures are molecular beam epitaxy (MBE) and metal organic chemical vapour deposition (MOCVD), and wafers used in this project were grown using these techniques. Figure 3.1 shows an epilayer structure of an AlGaN/GaN based heteroepitaxial wafer.

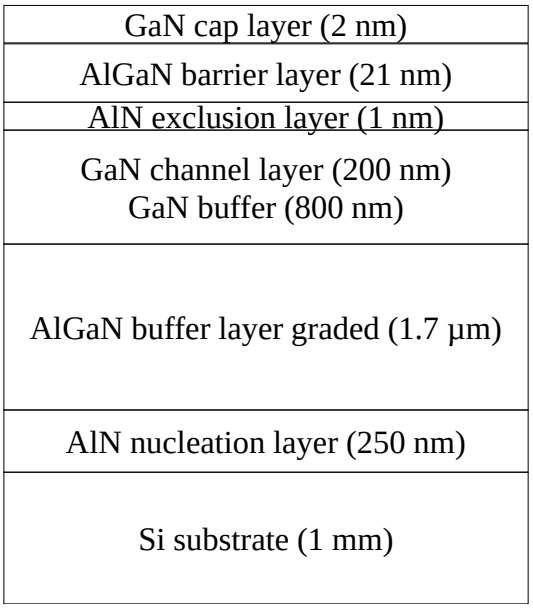


Figure 3.1 Epilayers of an AlGaN/GaN based heteroepitaxial wafer grown using MOCVD [93].

3.3 Device Fabrication

To fabricate a transistor device from a given wafer, three metallic electrodes are necessary; source, drain and the gate. Other key necessary steps include device isolation and pads from probing the device. The fabrication steps typically

required to obtain the basic GaN based HEMT device structure are described below.

3.3.1 Sample Preparation

Sample cleaning is done prior to any fabrication processes to remove debris, and other possible contaminations. In some cases, samples are coated with protective photoresist to avoid contamination of the surface. This protective photoresist of the wafer surface is usually applied prior to dicing up of the wafer into smaller pieces/samples. This resist must be removed prior to further fabrication activity. In GaN-based wafers, samples are cleaned using 1165 stripper followed by reverse osmosis (RO) water or acetone, followed by isopropyl alcohol (IPA) then RO water or combination of both.

3.3.2 Lithography

Lithography is the process of transferring the (device) pattern onto the surface of the substrate. There are two types of lithographic patterning processes, photolithography and electron beam lithography (EBL) which are described in the next sections.

3.3.2.1 Photolithography

Photolithography is the process in which light is used to transfer pattern from a hard mask into a photoresist layer on the surface of a substrate. The photoresist's chemical structure under direct ultraviolet (UV) light ($\lambda \approx$ 200-400 nm) changes according to its properties. The key component required for pattern transfer is a transparent plate consisting of chrome pattern called photomask shown in Figure 3.2. The lithography machine used in this project is Karl Suss mask aligner 6 (MA6) machine shown in Figure 3.3. Various lithography steps may be required to realise a given device structure onto a wafer depending on the structure complexity.

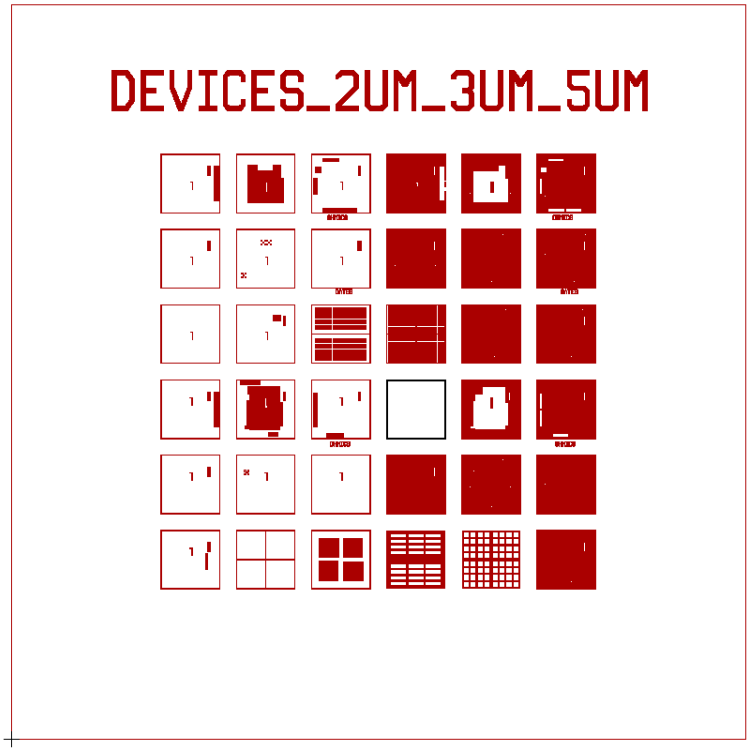


Figure 3.2 Chrome pattern called photomask.

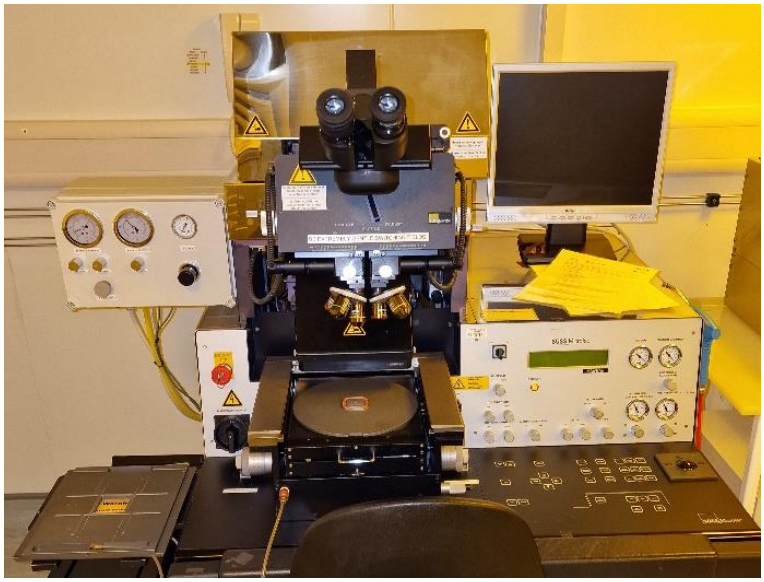


Figure 3.3 An image of the Suss Mask Aligner (MA6) in the JWNC.

The mask is produced by designing a device footprint using computer aided design tools. In this project Tanner EDA L-Edit by Mentor Graphics is used for designing the devices. The shape of the footprint is translated on the mask using opaque and transparent regions. Graphic Data System, Version II (GDSII) file format consisting of all the designed features of the device is then exported to the

commercial vendor for fabrication. In the project, the files were exported and sent to Compugraphics International Ltd for fabrication. Example of the device footprints with various layers designed in L-Edit is shown in Figure 3.4.

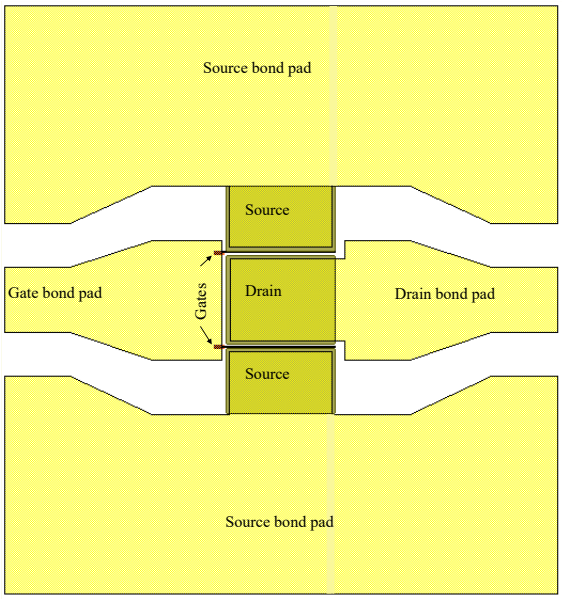


Figure 3.4 Device footprints with various layers designed in L-Edit.

Transfer of the pattern from the mask to the substrate requires coating the latter with either negative or positive photoresist depending on the mask design. Positive resist becomes soluble in developer when exposed to light, while negative resist, which is normally soluble, becomes hardened and insoluble. To transfer a pattern, the mask is placed between the substrate and the source of light in the MA6. During exposure, UV light incident on the surface of the mask is blocked on the opaque regions and reaches the photoresist on the substrate in the transparent regions of the mask. The substrate is then developed into a development solution. The developers used in this project is micro-posit MF319 and micro-posit concentrate.

In photolithography, a single mask could be consisting of a few individual layers (steps) of the device design where each layer will be transferred onto the substrate one after the other using the photolithography machine (MA6 in this project). One of the crucial layers in pattern transfer is the markers layer (step) for the mask alignment to align each layer to the corresponding patterns. In device fabrication, alignment is crucially required after the first exposed pattern has

been developed. Misalignment could result in shorting some features intended to be separate, resulting in total damage of the device.

3.3.2.2 Electron Beam Lithography (EBL)

EBL is a process of maskless transfer of patterns into resist on the substrate. It was primarily used for mask plate production. However, due to submicron or deep submicron patterning requirements, the technique can be used to write a direct pattern onto the resist covering the wafer surface by a focused electron beam without a mask plate. EBL operates by generating a high-quality beam of electrons to interact with polymer-based resist coated on the surface of the substrate. Unlike in the case of photolithography, various exposure doses can be selected making it possible to expose different regions of the substrate with specific dose required by each region which offers effective resolution, high precision, and alignment accuracy. Other advantages of this technique include patterning of submicron and deep submicron features, highly automated and precisely controlled operation, positioning/alignment accuracy, ultra-high resolution, direct patterning on a semiconductor wafer without using a mask plate and can be easily accessible for corrections since the layout design for EBL are stored and used electronically in the machine tool system. In this project, Raith 100 kV EBPG 5200 electron beam lithography tool (shown in Figure 3.5), capable of transferring a nanoscale pattern (up to 3 nm) with high accuracy alignment of ±0.5 nm was used.

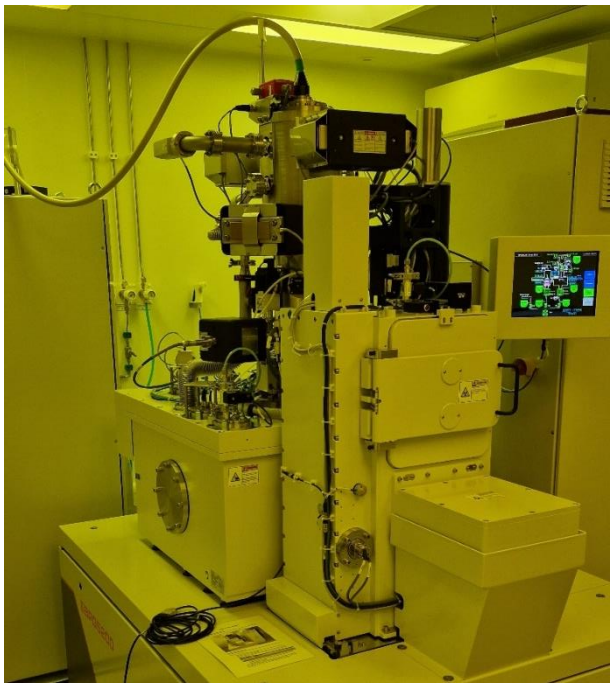


Figure 3.5 An image of Raith 100 kV EBPG 5200 electron beam lithography tool in the JWNC.

3.3.3 Markers

The markers are used as a reference to align the different pattern for the different steps required to realise a device. Markers always should be the first layer to be deposited. Sometimes markers and the second layer are deposited together. So, each fabrication step is aligned according to the design, to avoid overlapping and so fabricate functional devices. Figure 3.6, illustrates an example of a 10×10 mm sample design layout in L-Edit with transistors and different markers in the 4 sides of the design. There is a long bar in the design to help for the orientation of the design to load the sample in the correct position for exposure. As shown in the Figure 3.6, there are photolithography markers along with E-beam markers. In this particular design, the combination of photolithography for larger pattern dimensions >1 μm (for example ohmic contacts, bond pads, etc), and EBL to align more precisely (0.5 nm accuracy) for smaller design dimensions <1 μm (for example gates) are used.

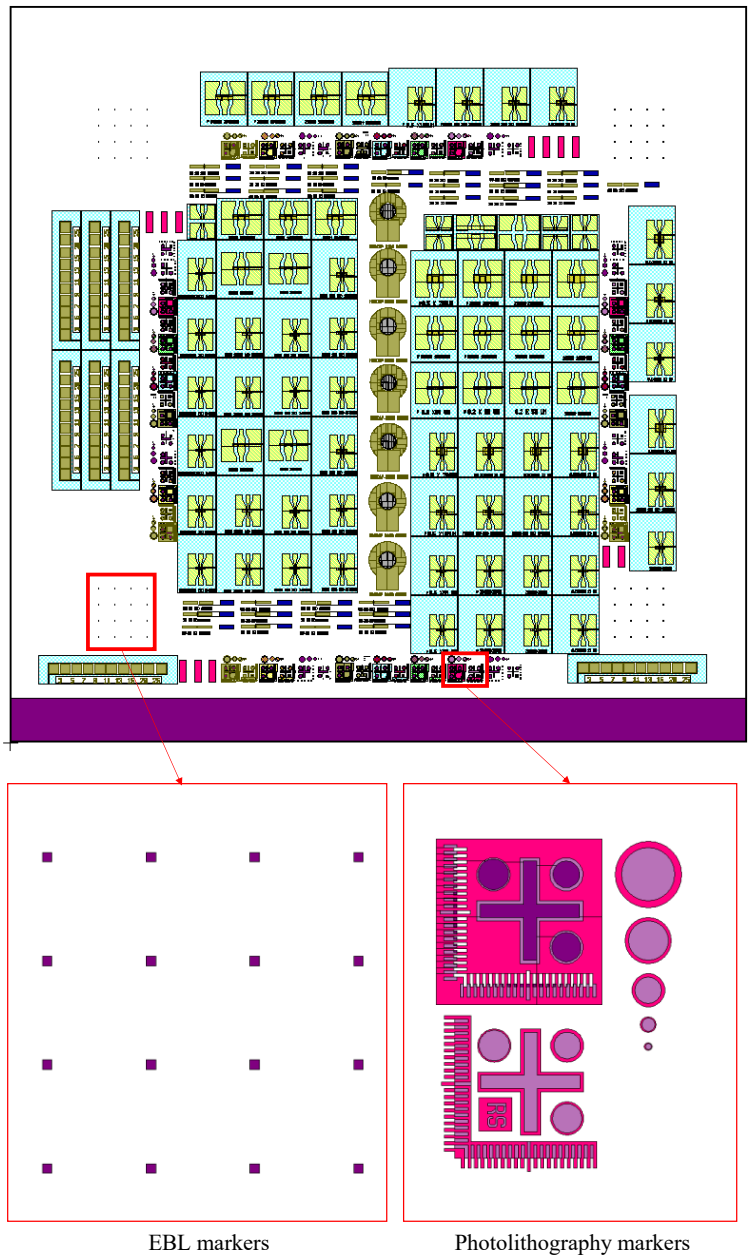


Figure 3.6 An example of a 10×10 mm design layout in L-Edit with transistors and different markers in the 4 sides of the design.

3.3.4 Metallisation

Metallisation is another important step in the fabrication process to form metal semiconductor contacts. A number of different methods are used to deposit metals onto the wafers, which includes electron beam evaporation, sputtering, and electroplating. In this project, electron beam evaporation was the main technique deployed for deposition.

3.3.4.1 Electron Beam Metal Evaporation

In electron beam metal evaporation, the source material intended to be coated onto the surface of the substrate is bombarded with electron beam from a charged filament which causes the material to evaporate, thereby coating the entire surface of the substrate. In this project, metal evaporation Plassys MEB 550S and Plassys MEB 450 shown in Figure 3.7 were used. Before metal deposition using these tools, the deposition chamber must be evacuated to establish a vacuum in the rage of $<1\times10^{-6}$ Torr after which the electron gun is turned on to vaporise the source material. To ensure precision and uniformity, the substrate is protected against any vapourised metal by a shutter, until a stable evaporation rate is reached. The substrate holder can be adjusted at an angle to the source material and can be rotated around its axis to establish a uniform coating on the target areas of the sample. At this point, the shutter opens, and the vapourised metal begins to coat the substrate at a stable rate. Plassys MEB 450 is equipped with ion gun with Argon plasma source for cleaning/etching the substrate prior to metallisation.

Figure 3.7 Metal evaporation Plassys MEB 550S and Plassys MEB 450 in the JWNC.

3.3.5 Metal Lift-Off Technique

Lift-off in the next step after metallisation for most of the fabrication processes. Lift-off is the process of removing all the unwanted metals after metallisation. In order to have a successful lift-off, resist undercut is required for the resist remover to “lift-off” the unwanted metals on the resist. This could be achieved using one layer resist by optimising the baking time and temperature, exposing time, and developing time. Bilayer resist is most common technique for metal lift-off, where the first resist layer is used as an undercut layer and the top layer used for the pattern structure to get metallised. In this project for the photolithography, LOR 10A and LOR 3A were used as the undercut layer and S1818 or S1805 (depend on the structure sizes) were used as the top layer. For EBL the E-beam resist such as polymethyl methacrylate (PMMA) with low molecular weight of 50K (resists with low molecular weight develop faster) as the undercut layer and PMMA with high molecular weight of 950K as top layer were used. Figure 3.8 illustrate a typical fabrication process involving metallisation and lift-off.

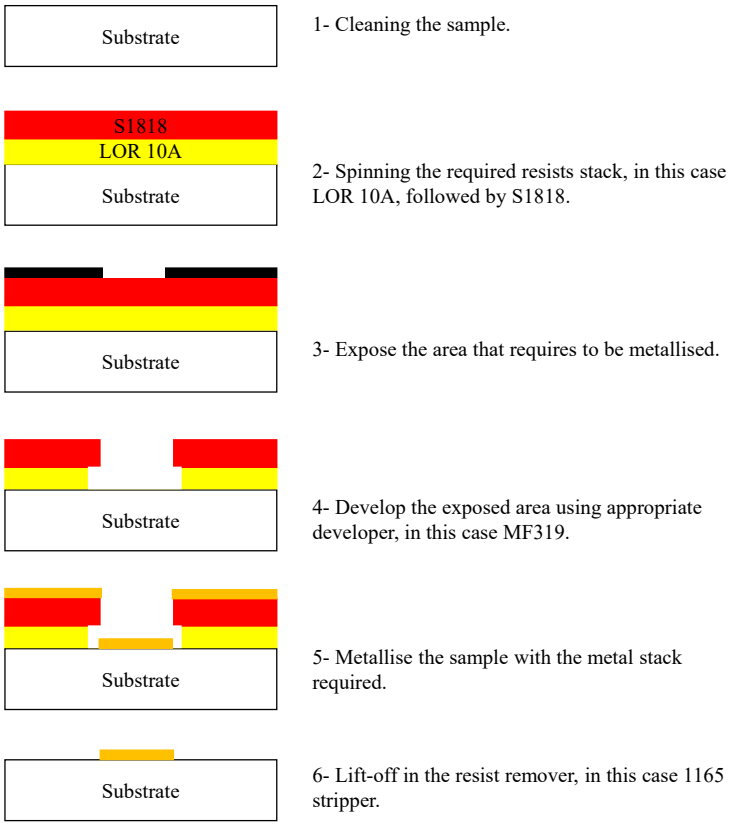


Figure 3.8 Fabrication process, including metallisation and lift-off process.

3.3.6 High Temperature Annealing

In semiconductor device processing, rapid thermal annealing (RTA) is widely used for the activation of dopants and the interfacial reaction of metal-semiconductor contacts. It involves the heating of wafer to a very high temperatures (~800 °C in GaN HEMT devices) for a given time, usually <60 seconds. In GaN HEMT with Ti/Al-based metal stack, RTA is used to lower the ohmic contact resistance by heating the wafer to temperature between 750°C - 950°C for 30 seconds in the N_2 ambient. This process causes the Ti metal to react with the nitride layer underneath resulting in the formation of TiN alloy beneath the contact. In this project, Jipelec JetFirst 200 rapid thermal annealing (RTA) machine shown in Figure 3.9 was used.

Figure 3.9 An image Jipelec JetFirst 200 rapid thermal annealing (RTA) machine in the JWNC.

3.4 Measurement and Characterisation Techniques

Characterisation is a fundamental component in research and device manufacturing processes. In this project, DC measurements were carried out using Keysight's B1500A Semiconductor Device Analyzer while the vector network analyser (VNA) was for RF measurements as shown in Figure 3.10. The main characterisation techniques discussed in this section are for the analysis of contact resistance using the linear transmission line model (TLM) and circular transmission line model (CTLM) structures, output characteristics, transfer characteristic,

breakdown voltage, leakage current, and scattered parameters (S-Parameters) measurements to obtain maximum and cut-off frequencies.

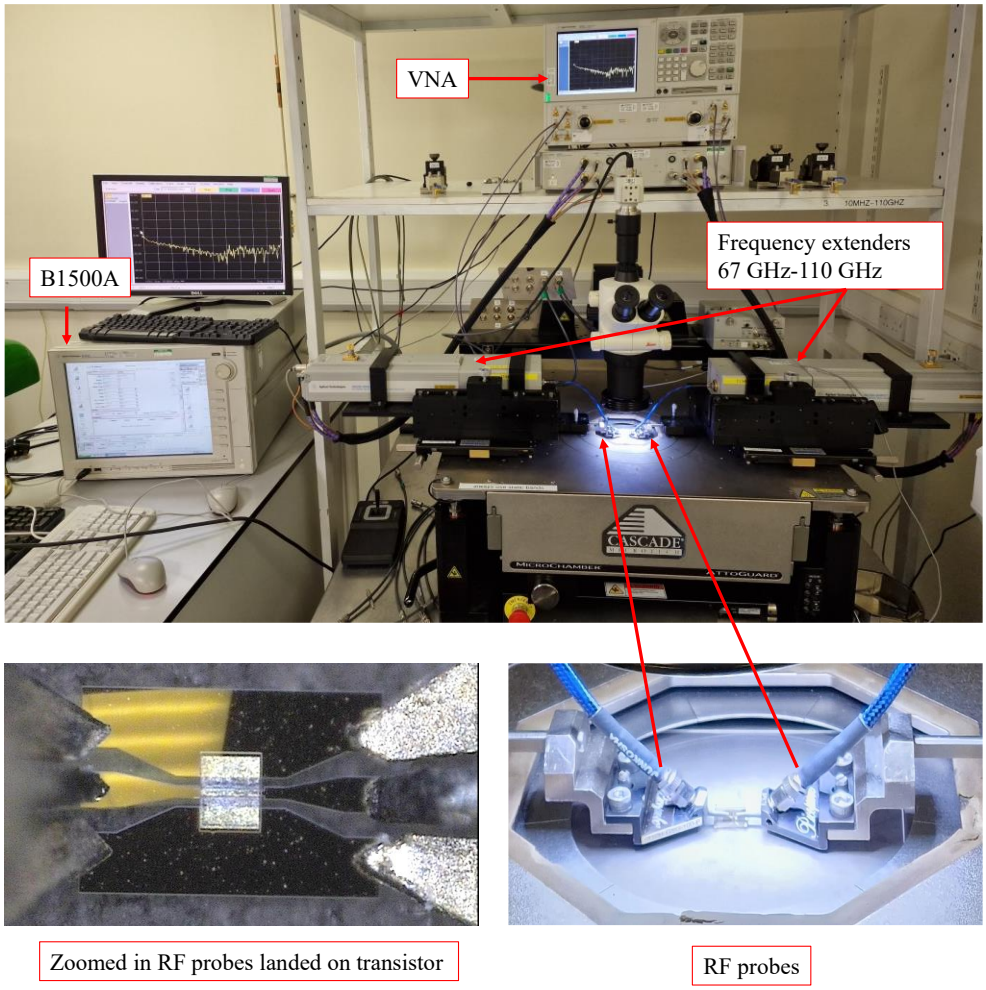


Figure 3.10 Keysight B1500A Semiconductor Device Analyzer and Vector network analyser (VNA).

3.5 DC and RF measurements

Two main types of measurements were carried out in our project, the direct current (DC) and radio frequency (RF) measurements. As mentioned earlier, the DC measurements such as output characteristics, ohmic contact resistances, transfer characteristic, leakage current, and breakdown voltage are obtained using B1500A semiconductor device analyser. For the gate wrap around drain device measurements, three probes are required source, drain, and gate one each. For RF layout devices, RF probes are required for DC and RF measurements.

In this project, both gate wrap around drain and RF devices have been fabricated and measured.

3.5.1 DC Characterisation

3.5.1.1 Linear and circular Transmission Line Model (L-TLM & CTLM)

Transmission Line Method (TLM) method was first proposed by Shockley to determine specific contact resistance [94], then optimised by Reeves and Harrison to get more accurate results including contact resistances [95]. The typical TLM structure consists of 3 or more equal square contacts (>150 μm^2) placed one after the other, separated by an increasing distance (L) from pair to pair as shown in Figure 3.11. Mesa is defined by etching the surrounding fabricated contact structures (as shown in the yellow area in Figure 3.11), required to isolate the contacts from the active area. The purpose of this isolation is to achieve more accurate results by confining the current to one direction (from a contact pad to its next neighbouring pad). Followed by depositing ohmic contact pad metals, then resistance measurements between each neighbouring pair of pads to obtain total resistance as described below. The measurement with B1500 Keysight device analyser is carried out using Kelvin probe methods. It has two pairs of measurement probes to accurately measure the resistance of a device or material while compensating for the wire resistance. Two wires (one from each pair of probes) carry the measurement current, and two wires (from each pair of probes) measure the voltage across the device. Using Equation 3.1 where R_{sh} is the sheet resistance, R_C is the contact resistance, *W* is the width of the pad, the total resistance (R_T) between two neighbouring pads place apart by a distance L is obtained. Increasing L of between any two pads results in an increasing R_T. Figure 3.12 Figure *3.12*shows a linear relationship of 6 pads with 5 gaps (L_x) plotted for an increased L between pad to pad.

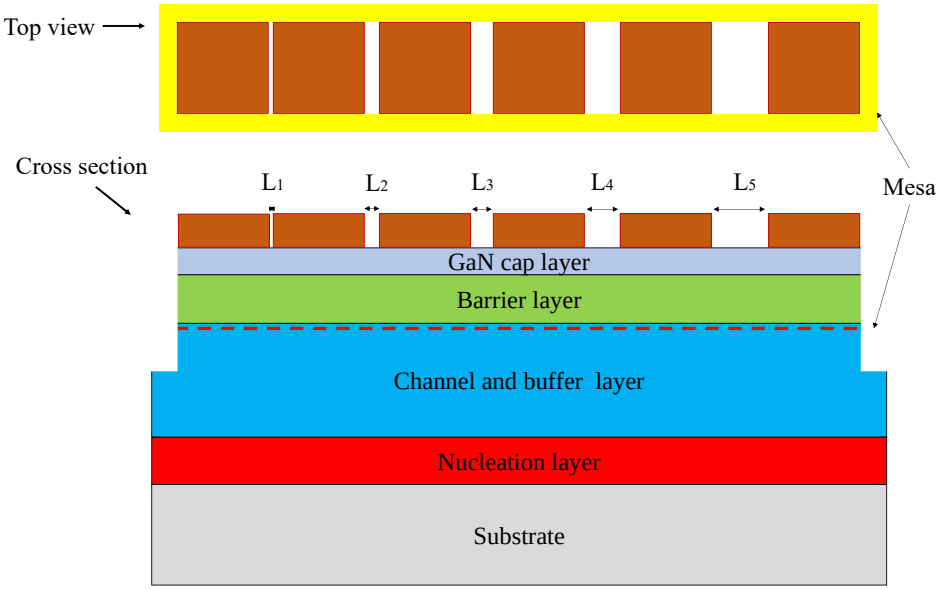


Figure 3.11 Linear TLM with varies spacing between them, the yellow area is the mesa around the contacts pads. Top and bottom image are representing the top view and the cross-section of a linear TLM respectively.

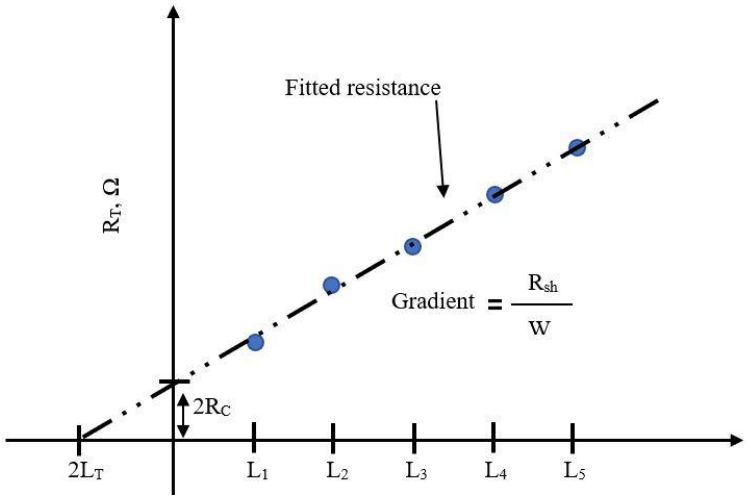


Figure 3.12 TLM plot, results of the resistance against the spacing.

From the plotted curve shown in Figure 3.12, the best fitted line is drawn to obtain the slope of the curve R_{sh}/W and the intercepts of the x-axis (L_x) at $2L_T$, and of the y-axis at $2R_C$. L_x is related to the transfer length L_T by Equation 3.2. Since R_C is only dependent on the width of the contact *W*, the generated value of R, should be multiplied by the width to get a value Ω.mm.

$$R_T = 2R_C + \frac{R_{sh}L}{W} \tag{3.1}$$

$$L_x = 2L_T = \frac{2R_C W}{R_{sk}} \tag{3.2}$$

From those results obtained, contact resistivity could be generated as Equation 3.3.

$$\rho_C = R_C W L_T \tag{3.3}$$

The linear TLMs is one dimensional (1D-TLM), which assumes that the contact pad width is equal to the mesa width, which causes the current to flow laterally and confined from one contact to the other only. This condition is not always met during lithography and makes this method not very accurate. If the width of the pad is smaller than the width of the mesa, the lateral current crowding occurs in the gap between the contact edge and the semiconductor mesa, which causes parasitic effects. However when the gap between them is very small compared to the width of the pads, the current crowding could be neglected [95, 96].

To overcome the problem of current crowding in the case of a bigger gap between the pad and the mesa, a 2D-TLM is used to get more accurate value of the specific contact resistivity. CTLM is modified TLM, which instead of using squares, it uses circles. It is easier to fabricate, as it is only one step fabrication process and no recess required (as shown in Figure 3.13 for a typical CTLM structure). In CTLMs, current can flow from the central contact to surrounding contact. They are more accurate than the rest of the measurement methods and it is widely used [96].

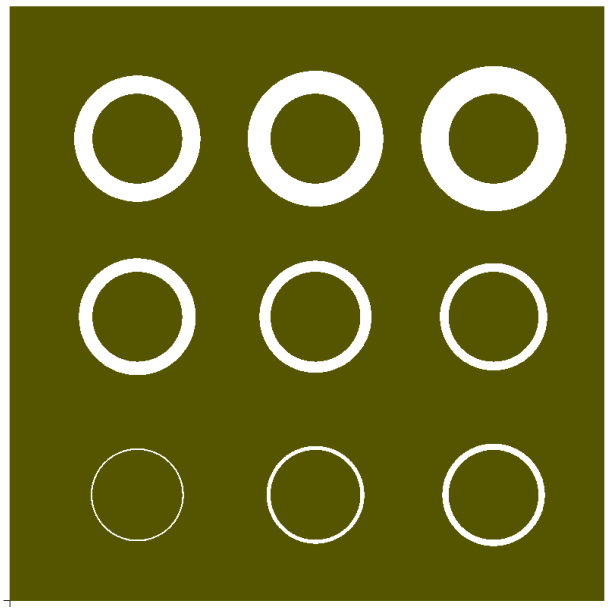


Figure 3.13 L-Edit of a CTLM structure.

Same equations used to extrapolate TLM measurements are used in the case of CTLM. However, for circular TLMs a correction factor required to compensate for the differences between linear TLM and circular TLM. This correction provides a linear fit to the experimental data [95, 96]. The correction factor could be obtained using Equation 3.4.

$$C = \frac{L}{d} ln\left(1 + \frac{d}{L}\right) \tag{3.4}$$

So, to get R_T:

$$R_T = \frac{R_{sh}}{2\pi L}(d + 2L_T)C \tag{3.5}$$

Where d is the gap between the contact and surrounding area and L is the radius of the contact pad.

In this project, both TLM and CTLM were used, and similar results were obtained. For linear TLM, the measured contact resistances will be plotted against the gap length and relative parameters were extracted such as contact resistance, specific contact resistivity, and sheet resistance. However, in the case of CTLM, as mentioned above, the measured contact resistances should be multiplied by the correction factor (C) before plotting and extracting the required parameters. Then

extracted results for linear TLMs should be multiplied by pad width size to get the results per common use of unit (mm) and for CTLM should be multiplied by the circumference of the inner circle.

3.5.2 RF Characterisation

After fabrication the next step is to measure and characterise the devices. Accurate measurements provide essential feedback for any further improvements required for the design and fabrication processes. In this section, maximum and cut-off frequency characterisation are discussed.

3.5.2.1 Transistor Cut-Off Frequencies

Transistor performance is influenced by the operating frequency, and understanding its behaviour at specific frequency ranges is crucial for achieving high-performance transistor devices. As the frequency increases, the gain of the transistor tends to decrease. Two important parameters used to determine the operating frequency of a device are the unity current gain cut-off frequency (f_t) and the maximum frequency of oscillation or unity power gain cut-off frequency (f_{max}). These parameters are obtained from the hybrid parameters (h-parameters), which in turn are derived from the S-parameters obtained through RF measurements. S-parameters, or scattering parameters, represent the linear characteristics of electronic devices and are used to determine various device characteristics such as gain, RF power, losses, and impedances, which are essential for overall system performance. They provide a fundamental relationship between the transmitted, incident, and reflected waves in a transistor. In the case of a HEMT, it is considered a two-port network with the gate-source terminals serving as the input port and the drain-source terminals as the output port as shown in Figure 3.14.

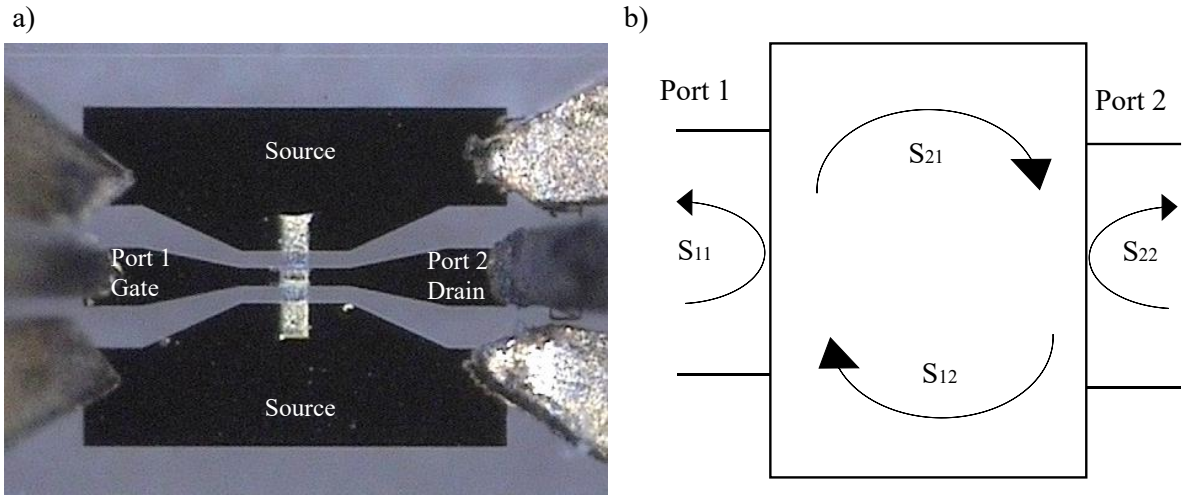


Figure 3.14 A typical RF device, (a) RF probes are landed on fabricated device, and (b) two port networks system measured with VNA.

By using a vector network analyser (VNA), the S-parameter matrix can be measured, and it can be used to determine the impedance of the network by measuring the incident and reflected voltage vectors of the two ports. To obtain the S-parameters, the device needs to be biased with drain voltage and gate voltage. For achieving the best performance of the device in high-frequency operations, the drain voltage is selected from the maximum output current, and the gate voltage is selected the maximum transconductance of the device as shown in Figure 3.15.

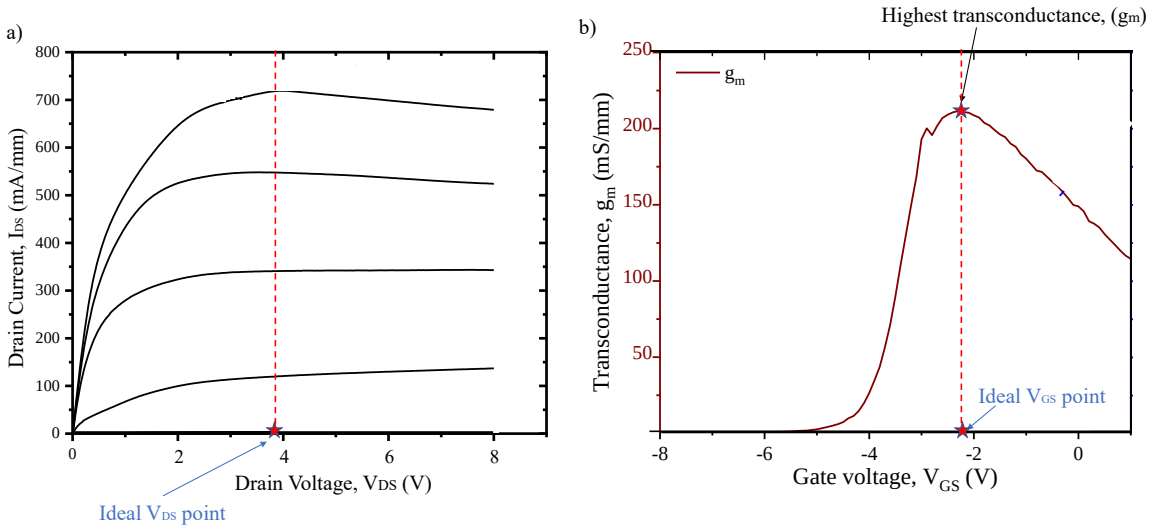


Figure 3.15 A graphical image of choosing the ideal biasing point of (a) V_{DS} and (b) V_{GS} for RF measurements.

S-parameter matrix is represented as $S = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix}$, where S_{11} is the input reflection coefficient, S_{12} is the reverse transmission coefficient, S_{21} is the forward transmission coefficient and S_{22} is output reflection coefficient. S_{11} is the S-parameter at Port 1 that represents the ratio of the reflected wave at Port 1 to the incident wave at Port 1, while Port 2 is terminated in its characteristic impedance. S_{12} is the S-parameter at Port 1 that represents the ratio of the wave incident at Port 1 to the wave transmitted to Port 2, with Port 2 terminated in its characteristic impedance. S_{21} is the S-parameter at Port 2 that represents the ratio of the wave incident at Port 2 to the wave transmitted to Port 1, with Port 1 terminated in its characteristic impedance. S_{22} is the S-parameter at Port 2 that represents the ratio of the reflected wave at Port 2 to the incident wave at Port 2, while Port 1 is terminated in its characteristic impedance. When a network is characterised by S-parameters, it can be viewed as a black box with two ports. The incident wave at each port causes a combination of reflections and transmissions, which are represented by the S-parameters.

The cut-off frequency where the current gain falls to unity (f_t) can be obtained from hybrid parameter h_{21}. h_{21} could be determined from the measured S-parameters using Equation 3.6, while the maximum frequency of oscillation (f_{max}) can also be determined from S-parameters using the Masons unilateral power gain (U) in Equation 3.7.

$$h_{21} = \frac{I_{\text{out}}}{I_{\text{in}}} = \frac{-2S_{21}}{(1-S_{11})*(1+S_{22})+S_{12}S_{21}} \tag{3.6}$$

$$U = \frac{P_{\text{out}}}{P_{\text{in}}} = \frac{\left|\frac{S_{21}}{S_{12}}-1\right|^2}{2\left[K\left|\frac{S_{21}}{S_{12}}\right|-\text{Re}\left(\frac{S_{21}}{S_{12}}\right)\right]} \tag{3.7}$$

In Equation 3.7, *k* is the stability factor which determines the of the two-port network and can be obtained using Equation (3.8), where $\Delta = S_{11}S_{22} - S_{12}S_{21}$.

$$K = \frac{1-|S_{11}|^2-|S_{22}|^2+|\Delta|^2}{2|S_{12}S_{21}|} \tag{3.8}$$

Using K and Δ, we can determine whether the device is conditionally stable or unconditionally. When K >1, Δ<1, the device is unconditionally stable, which means there will be no oscillation. In satellite communication systems or radars, RF power amplifiers need to be unconditionally stable to ensure reliable and continuous signal transmission without the risk of oscillations or instability that could disrupt communication links. When K <1, the device is conditionally stable, where stability is depends on load and source terminations (a stabilising network is required to prevent it from oscillating). RF signal generators used in some research or testing scenarios may not require unconditional stability as they can be intentionally designed to generate specific types of signals, including modulated or swept-frequency signals, for experimental purposes.

3.6 Summary

In this chapter, the growth of GaN HEMTs is explained, followed by an overview of the main fabrication techniques for GaN devices, such as lithography and metallization. The corresponding equipment used in this project is also described. Furthermore, the measurements and characterisation of the fabricated GaN HEMT devices, including DC and RF measurements, are discussed in detail.

Chapter 4

Development of Sub-100 nm T-Gate HEMTs

4.1 Introduction

In Chapter 2 the principles underlying HEMT operation were reviewed. Also, in Section 2.9.3, the principal of reduction of physical dimensions of the device were explained for high-power high-frequency devices. This reduction in the physical dimensions of device improves the frequency properties of GaN HEMT as required in high-frequency application. Reduction in the size of a device can be achieved by reducing the gate length. Reduction of the gate size to nanoscale is desirable in high-frequency applications. The shorter the gate length, the higher the cut-off frequency of the device as shown in Equation 2.15 in Chapter 2, this however leads to a fundamental problem of high gate resistance as shown in Equation 4.1, which severely affects the maximum cut-off frequency of the device.

$$R_G = \rho \cdot \frac{W_G}{L_G h} \tag{4.1}$$

Where R_G is gate resistance and W_G, L_G, ρ, and h are the gate width, gate length, resistivity, and gate height respectively.

To mitigate the effect of increasing gate resistance with scaling of gate length, a T-shape gate design becomes very effective. T-gate consists of a narrow gate foot with a larger gate head which helps keep the resistance relatively small. Realising the gate is one of the most important steps in the fabrication of high-frequency HEMT devices. For crucial need of high resolution, electron beam lithography (EBL) is usually the choice in the fabrication of T-gate HEMTs. Scaling of the gate to sub100 nm dimensions becomes a challenge due to mechanical instability. This problem is can be solved by depositing a thick layer of Si_3N_4 and etch the gate foot area, then deposit the T-gate to support the gate head [97, 98]. However, the drawbacks of this method are decreasing frequency performance due to increased gate channel capacitance, increase in the fabrication complexity, and the etch based damage.

In practice, various combinations of resists and fabrication approaches were used in the fabrication of T-gate, some of them are listed in Table 4.1. Different sizes of gate foot and heads have been reported in the literature based on those multi-resists layering and multi-exposure techniques shown in Table 4.1. The fabricated gate foot size compared to the designed size poses one of the main challenges in achieving sub 100 nm T-gate fabrication. The size of the fabricated gate foot in relation to the designed size presents a significant challenge when aiming to achieve sub-100 nm T-gate foot fabrication. Some of these challenges related to sub-100 nm T-gate include mechanical stability, dealing with misalignments, and addressing gate pad bloating.

In order to tackle mechanical stability, some researchers employ a thick supporting layer, such as SiO_2 or Si_3N_4 which is provides improved mechanical stability of the gate foot but introduces unwanted parasitic capacitances [99-102]. The supporting layer could cause damage on electrical properties due to etching [97, 98]. Also, this means two-step fabrication process which could lead to misalignment of the gate foot and gate head. Some researchers have emitted the supporting layer but still employed a two-step fabrication process, which this approach can introduce misalignments in nanoscale features (gate foot and gate head), even when EBL is used.

On the other hand, opting for a single-step process tends to result in an increase in the fabricated gate foot size compared to the intended design [103-105]. One of the challenges associated with using a single-step process is gate-pad bloating, which arises due to the high dose ratio between the gate foot and gate head. Maintaining the right sensitivity ratio is crucial because an optimal region exists for its value. If the ratio is too low, it becomes challenging to distinguish between the head and foot processing, resulting in a narrow process window for a well-formed T-gate structure with a controlled gate length. Taken to its ultimate limit, it is impossible to form a T-gate with a sensitivity ratio of 1. Conversely, if the ratio is too large, then there is a danger of the head layer 'bloating' when larger structures such as the gate pads are written [106]. This is caused by the backscattered electrons from the large dose required to write the gate feed at the foot dose.

The primary goal of this project is to establish a robust fabrication process for sub-100 nm T-gates. This objective is accomplished through the utilisation of a single-exposure electron beam writing technique, effectively reducing both writing time and complexity due to multiple exposure and development steps. To achieve this, a novel resist stack (PMMA/LOR/CSAR) is introduced, serving dual purposes. Firstly, it allows for meticulous control over the sensitivity ratio, optimising it within an appropriate range. This control mechanism addresses concerns such as poor gate length control, and bloat around larger features such as gate pads. Secondly, this resist stack mitigates the requirement of using a supporting layer (such as Si_3N_4 or SiO_2) for T-shape gates for its mechanical stability issues.

Table 4.1 Varies fabrication approaches toward fabricating T-Gates in nano scale.

Designed gate foot(nm)	Fabricated gate foot (nm)	Gate Head fabricated (nm)	Exposure steps	Development times	Resist stack	Undercut	Supporting layer	Ref	Year
-	350	-	-	-	PMMA/Al/PMMA	No	No	[107]	1983
-	150	800-900	-	-	PMMA/PMMA-MAA/PMMA	Yes	No	[108]	1983
40	120	4000	1	2	PMMA/Al/UVIII	No	-	[103]	1999
-	35	-	1	2	ZEP/PMGI/ZEP	Yes	SiO_2	[101]	2000
30	25-30	400	2	2	PMMA/LOR/UVIII	Yes	SiO_2	[100]	2004
-	10	450	2	2	ZEP520A/PMMA/LOR/UVIII	Yes	SiN_X	[99]	2009
-	162-240	630-650	1	1	PMMA 950K/ EL-11	No	No	[109]	2011
-	150-250	620-710	1	3	PMMA 950K/LOR 5B/PMMA 495k	Yes	No	[109]	2011
-	157-260	500-560	1	3	EL-6/ PMMA 950K/ LOR 5B/ PMMA 495K	Yes	No	[109]	2011
-	60	-	1	2	PMMA100K/PMMA350K/Al/ UVIII	No	SiN_X	[102]	2015
50	141	440	2	2	PMMA/Al/UVIII	No	No	[104]	2016
30	88	482	2	2	PMMA/Al/UVIII	No	No	[104]	2016
50	101	380	1	3	PMGI/ZEP520A/PMGI/ZEP520A	Yes	No	[105]	2016
30	66.8	350	1	3	PMGI/ZEP520A/PMGI/ZEP520A	Yes	No	[105]	2016
-	110	520	1	3	PMMA/PMGI/PMMA	Yes	No	[110]	2018
100	-	-	1	3	PMMA/LOR5B/PMMA-MMA	Yes	No	[111]	2020
-	80	400	1	1	PMMA /P(MMA-MAA)/ P(MMA-MAA)	Yes	No	[112]	2020
-	190	470	1	2	PMMA, co-polymer, ZEP, and E-spacer	Yes	No	[113]	2020

4.2 Experimental Procedures for the Fabrication of Sub-100 nm T-Gate Using Tri-layer Resist

In this section the process of the design and fabrication development are explained. The experiment process is broadly categorised into computer aided and experimental processes.

4.2.1 Computer Aided Processes

Various software's were used to design the layout of the device prior to the fabrication of its physical features, while other software is needed as intermediary tool for submitting a job to the EBL.

L-Edit is used to design the various layers required in the proposed device which include markers, ohmic contacts, mesa, gate foot, gate head, gate pad, bond pads and passivation layers. The layout contains entire device footprints to be printed onto the surface of the substrate.

Other important software is BEAMER used to optimise and assign correct doses to each of the various regions of the pattern of the T-shape gate. The layout GDSII file designed in the L-Edit is imported into the beamer to perform the above-mentioned function.

Additionally, alongside the experimental fabrication development of T-gates, GenIsys LAB is used. This software integrates precise simulation capabilities with a range of features for automated analysis, metrology (dimension measurement), and evaluation. These functionalities aid in simulating and analysing complex systems or processes, enabling efficient optimisation and evaluation of various scenarios [114].

4.2.2 Experimental Processes

As mentioned earlier, T-gates are generally fabricated using electron beam lithography. In the multi-step fabrication process, two main steps are required for the T-gate formation, the lithography process which transfers patterns to the resist using EBL and the metallisation process.

Lithography Process

I. Resist Coating

In lithography technology, to write on a substrate requires coating a certain thickness of polymer on the surface of the substrate onto which the device pattern is to be written. Coating of resist is accomplished by placing a required quantity of the resist on the substrate then spinning to a rotational speed of some typically few thousand revolution per minute (RPM) for particular period of time depending on the type of resist and the required thickness. Resist coating on the cleaned substrate is always the first step of the lithography process.

The mechanically robust sub-100 nm T-gate structure was formed using tri-layer resist stack of PMMA/LOR/CSAR. The process was begun by spinning one layer of PMMA (950K 2%) at 1500 rpm for 60 seconds and soft baked at 180 °C for 5 minutes. Followed by LOR3A spun at 6000 rpm for 30 seconds and soft baked at 150 °C for 3 minutes. A layer of CSAR was finally spun at 2000 rpm for 60 seconds and soft baked at 150 °C for 2 minutes.

II. Resist Exposure

The next step after the resist coating is the resist exposure which writes the pattern (gate foot and head) on the substrate using the EBL. The exposed parts are softened and become easily removable in solution appropriate to the resist, while non-exposed part remains unaffected. EBL operates by generating a high-

quality beam of electrons to interact with polymer-based resist coated on the surface of the substrate. Using this process, films of resists on the surface of a substrate are exposed to high electron radiation which eventually transfers patterns onto the substrate without the need of using a mask plate. Unlike in the case of photolithography, various exposure doses can be selected making it possible to expose different regions of the sample with specific dose required by each region during the same exposure step, which offers effective resolution, high precision, and alignment accuracy.

We demonstrate the novel technique using a T-gate with a sub-100 nm gate foot. For the purpose of optimisation of the sub-100 nm T-Gate, we have used AlGaN/GaN HEMT on 1 mm thick Si (Figure 4.1 (a)) as a testing substrate and multilayer resist stack consisting of PMMA (950k), LOR-3A and CSAR, as shown in Figure 4.1 (b).

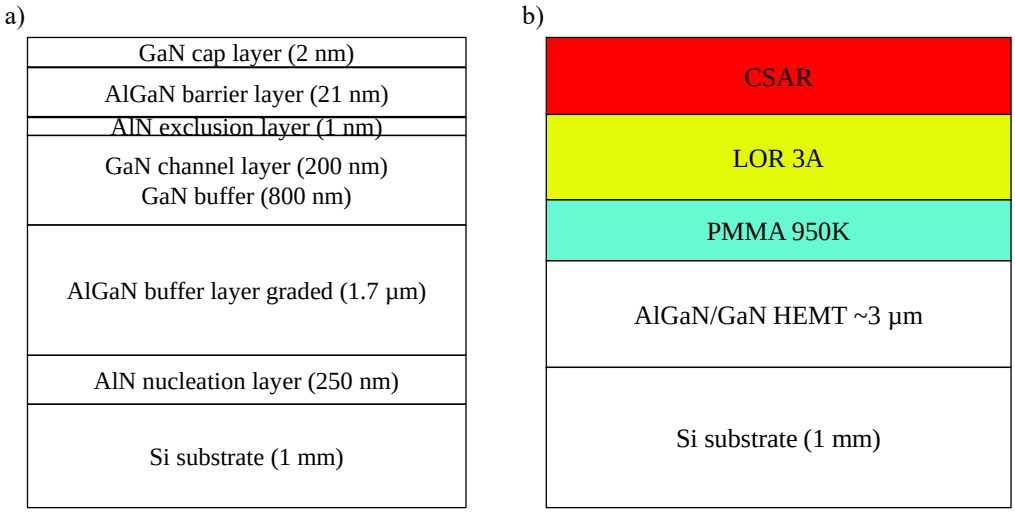


Figure 4.1 (a) AlGaN/GaN HEMT on Si, (b) proposed resist stack for T-Gate fabrication.

For fabricating such a narrow gate length (sub-100 nm), Raith 100 kV EBPG 5200 electron beam lithography tool, capable of transferring a nanoscale pattern (up to 3 nm) with high accuracy alignment of ± 0.5 nm was used. T-gates layouts with various gate lengths and wings shown in Table 4.2 were designed using L-Edit. T-gate design consists of gate foot in the centre and two wings one at each of the two opposing sides of the foot as shown in Figure 4.2. Each T-Gate was 100 µm

wide, with various gate foot lengths from 50 to 100 nm at an interval of 10 nm gap and each foot was supplied with pair of three different wings sizes 100, 150, and 200 nm. The GDSII file of the T-gate layout was imported to BEAMER, which transforms the file into a single layer for dose correction and optimisation.

Table 4.2 Varies L-Edit T-Gate design.

Gate length (nm)						Gate wing (one each side of the foot) (nm)		
50	60	70	80	90	100	100	150	200

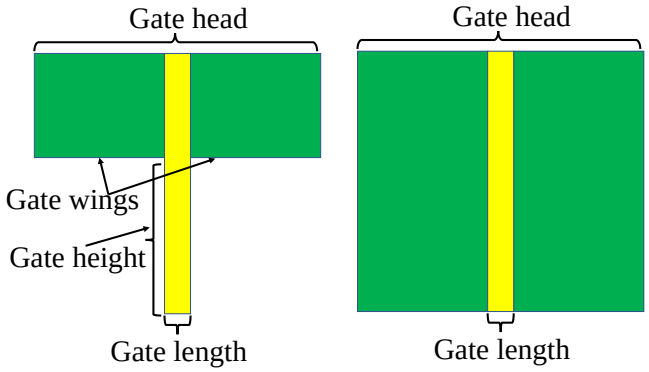


Figure 4.2 Schematic diagram of T-Gate sections.

Prior to attempting to write the T-gate patterns, contrast curves were required for PMMA and CSAR resists, by characterising them individually. This was done by designing and writing forty rectangular shaped patterns each sized 200 µm × 500 µm and spaced 400 µm from one another with varied of doses from 50 to 800 µC/cm^2 for one layer of PMMA (120 nm total thickness) and from 50 to 500 µC/cm^2 for one layer of CSAR (250 nm total thickness) using EBL. The shapes were developed using IPA:MIBK 3:1 for PMMA resist whereas Amyl acetate (pentyl acetate) was used to develop CSAR each for 30 seconds development time. A single profilometer scan (Dektak XT) was used to measure the depth of the remaining resist in the exposed areas (rectangles) after development. From those measurements, contrast curves shown in Figure 4.3 were generated for each resist by plotting the remaining resist thickness against dose intensity. The next step was to simulate the resist stack profile on corresponding substrate to feed into the BEAMER to get more defined dose correction. Point spread function (PSF) file was computed by Monte-Carlo simulation tool (in this project TRACER) to simulate

the transfer of electrons passing through resist into the corresponding substrate. For this simulation, resist thicknesses and their material properties (mass density [g/cm^3], excitation energy [eV], stoichiometry) is required. This simulation process improves the resist stack lateral development edges. The total thicknesses were 120, 220, and 250 nm for PMMA, LOR 3A, and CSAR respectively.

The contrast curves from experimental results of each resist and PSF from Monte-Carlo simulation for the resist stack, were then imported into the BEAMER software which enables 3-D Proximity Effect correction [115] and calculation of the best effective dose for clearing the gate foot (PMMA resist) and gate head (CSAR resist) structure [115]. The output results then transferred to EBL to write the given pattern on the sample.

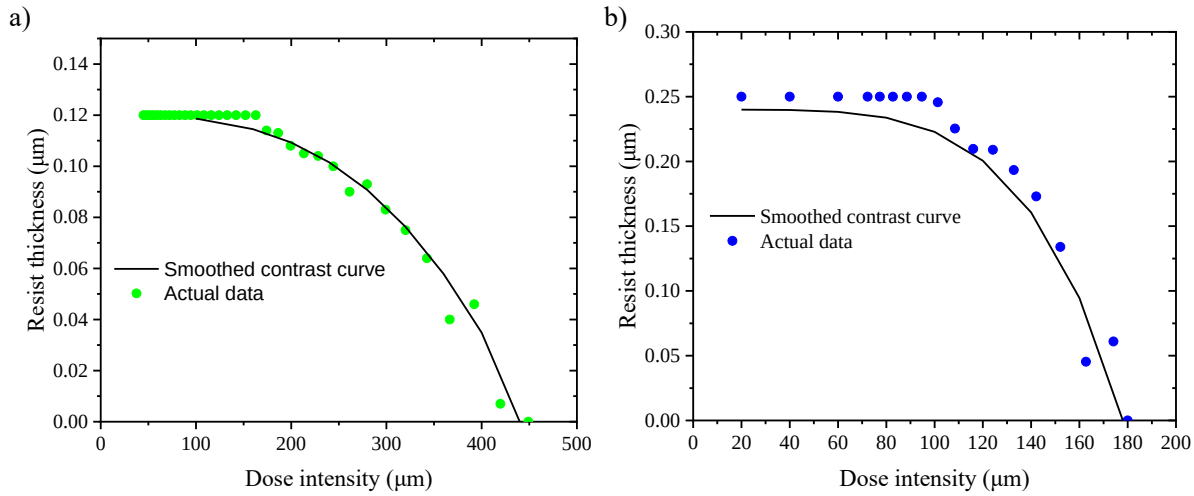


Figure 4.3 Contrast curves of PMMA (a) and CSAR (b), solid line is the fitted curve line and circles are the actual measurement results.

III. Resist Development

Resist development is the process of removing the exposed resist from the substrate using a solution which eventually reveals out the pattern engraved on the surface of the substrate. The solution used for the development is called resist developer. Each type of resist may have a different type of developer. Development is achieved by placing the substrate in a developer solution for a certain period of time.

For fabricating the robust T-gate structure, three different types of resists were used, each requiring a different type of developer. The idea behind producing T-gate structure in a tri-layer stack of resists using EBL is based on the differences in their sensitivity to electron beam exposure. The stack consists of PMMA as the bottom layer to define the gate foot, LOR the middle layer for the undercut purpose, and CSAR the top layer to define the gate head. The top layer (CSAR) is more sensitive than the bottom layer, hence it was fully exposed on the prescribed dose without affecting the bottom layer (foot layer). Also, bloating problem [106] was eliminated for the contact pads of the gates by using a compromised dose ratio between the gate head resist and gate foot resist. The dose ratio of 1:3, CSAR:PMMA was used to have CSAR cleared without interacting with PMMA resist and to prevent gate pad bloating.

Resists developments were carried out in three different developers separately. So, each layer gets developed independently without effecting the other layers, which gives a fine control over their relative sensitivities. CSAR was developed by placing the substrate in the solution of Amyl Acetate at 23 °C for 30 seconds, followed by 30 seconds rinse in isopropyl alcohol (IPA) then blow dried using N_2. LOR-3A is non-electron-beam sensitive resist, it was however removed in a controlled way using TMAH, in this case using CD-26 for 25 seconds, followed by 30 seconds rinse steps in baths of reverse osmosis (RO) water then blow dried. PMMA was finally developed using IPA:MIBK 3:1 at 23 °C for 30 seconds, followed by IPA then blow dried.

IV. Metallisation Process

a) Metal Deposition

The region exposed and made free of resist was prepared for metal deposition. In this process, metal stack is deposited to form the T-shape structure. It was accomplished by electron beam evaporation technique using Plassys MEB 450. 20 nm of nickel (Ni) was first evaporated and deposited on the surface of the

substrate followed by 200 nm of gold (Au). The process of metal evaporation using Plassys MEB 450 was discussed in Chapter 3.

b) Metal Lift-off Process

Metal lift-off is the final process of forming the T-gate structure. The technique was discussed in detail in Chapter 3. The evaporated metal stack in Plassys MEB 450 covers the entire surface of the substrate. The LOR3A in the middle layer of the tri-layer resist was introduced into the stack to create an undercut profile. The resist remover (acetone) penetrates and gradually erodes the entire bottom resist (PMMA) causing the collapse of the bottom support and eventually lifting-off the metal supported by the resist.

4.3 Experimental results and discussion

The clearing doses of CSAR and PMMA resists were identified from the dose test measurements to be 180 μC/cm^2 and 440 μC/cm^2 respectively as shown in Figure *4.3*. PMMA requires higher exposure dose than CSAR with a sensitivity ratio of ~2.5:1. The development time for these resists at the prescribed dose is 30 seconds in development solution.

The fabricated structures using this innovative resist layering technique enable us to achieve well defined T-shape gates and eliminate the problem of gate contact pad bloating. However, during the exposing top layer (CSAR) for the gate head, over 40 nm of the gate foot resist layer (PMMA) also gets exposed which means reducing the gate height. For the T-gates, the larger gate height is fundamental to achieving a lower gate resistance. Using single PMMA layer, the maximum gate height achieved was 61nm as illustrated in scanning electron microscope (SEM) in Figure 4.4. The difficulty in achieving larger gate height in single PMMA layer is because of the unwanted exposure on the PMMA resist layer that occurred while exposing the gate wings pattern on CSAR resist layer. In this case, a portion of the PMMA layer is incidentally exposed and developed during PMMA development.

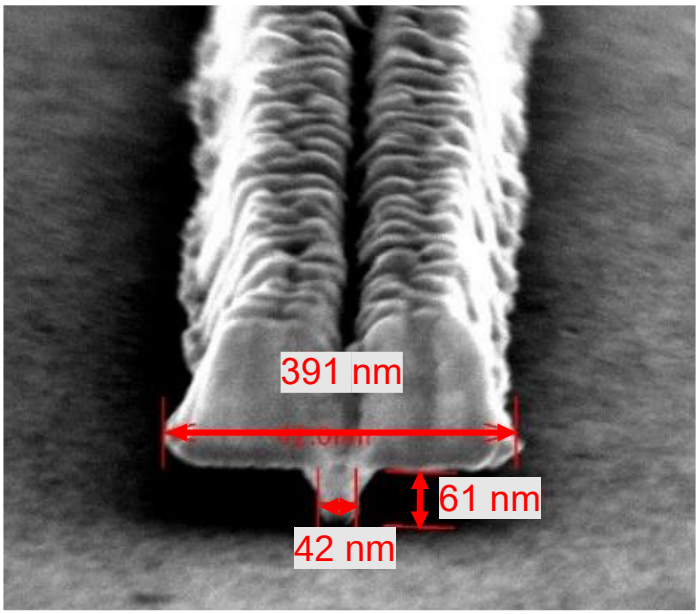


Figure 4.4 SEM of the fabricated T-Gate using PMMA/LOR/CSAR at 75-degree angle.

4.4 Sub-100 nm T-Gate foot height

To overcome this issue, two layers of PMMA individually spun at 4000 rpm and baked at 180°C for 5 minutes. This results in uniform PMMA across the sample and total thickness of 150 nm. A new contrast curve obtained for the new PMMA resist as before (shown in Figure 4.5) and a new electron PSF file for the new resist stack and material system was generated to feed into BEAMER software. Figure 4.5 shows the clearing dose has changed to 610 μC/cm^2 with the same developing time (30 seconds) so the sensitivity ratio has increased to PMMA:CSAR ~3.4:1 which still an excellent ratio.

An individual experimental test was carried out to see the dose effect on the two-layer PMMA resist. This was done by designing a T-gate consisting of a gate foot of 500 nm and two gate wings of each 500 nm. The reason for larger designing of the T-gate was to be able to measure the resist loss using available tools within the facility. After spinning the PMMA layers only, then writing the whole T-gate design (foot and wings) on the sample using EBL, this was followed by developing in IPA:MIBK 3:1 at 23 °C for 30 seconds, then dip in IPA and blow dried. The depth of the developed areas was measured with atomic force microscopy (AFM) as

shown in Figure 4.6. These measurements clearly show the loss of ~20 nm of PMMA due to exposing the wings layers. But these results are promising as the desired gate height is over 100 nm and it could be achieved using this resist stack.

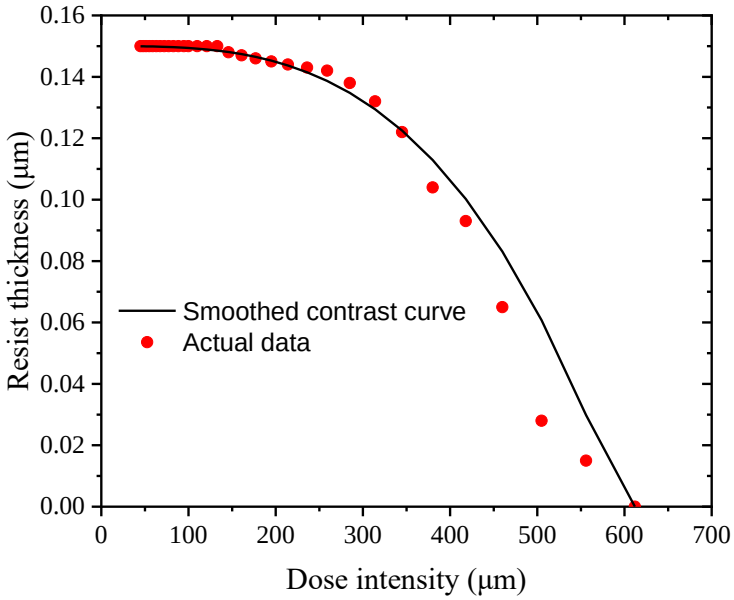


Figure 4.5 New contrast curve for 2 layers of PMMA.

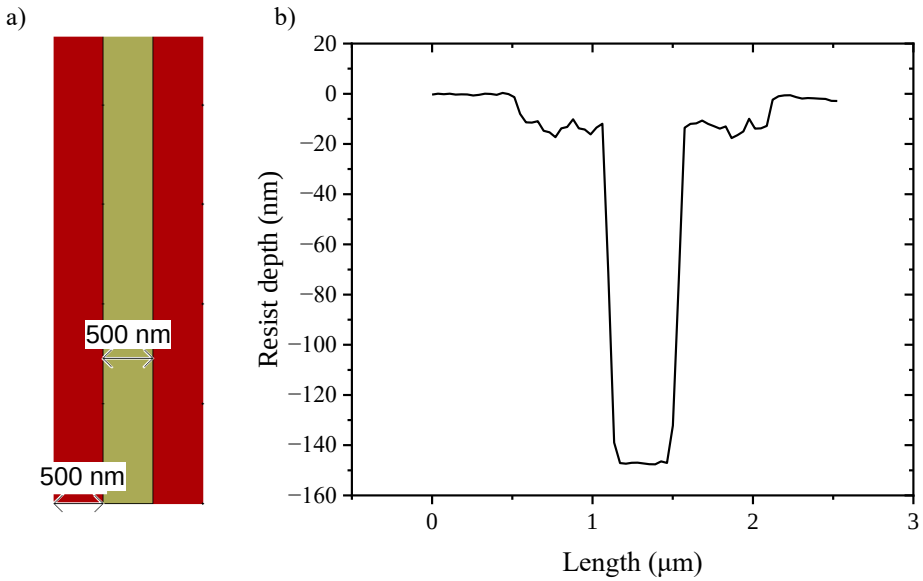


Figure 4.6 Test T-Gate, (a) design of the test T-Gate, (b) AFM scan of the test T-Gate starting from unexposed resist area, followed by first wing, then gate foot, then the second gate wing, and back to unexposed resist surface.

The new process was begun by individually spinning two layers of PMMA (950K 2%) at 4000 rpm for 60 seconds and soft baked at 180 °C for 5 minutes. Followed by

LOR 3A spined at 4000 rpm for 30 seconds and soft baked at 150 °C for 3 minutes. A layer of CSAR was finally spun at 2000 rpm for 60 seconds and soft baked at 150 °C for 2 minutes. The design of gate widths was increased from 100 µm to 4000 µm as compared to the previous experiment to cleave the sample into two parts, but the other parameters remained as mentioned in the previous experiment. So, a high dose for the foot line (centre) and a lower dose for gate wings with no digital gap between wing and foot. After the sample got developed, it is cleaved into two parts. One part is for SEM inspection of the resist profile after developing. It is sputtered with 2 nm Pt (platinum) to be able to see the cross section in SEM (scanning electron microscope). Figure 4.7 shows the SEM image of the cross section of the developed resist profile for 50 and 100 nm gate length each with 100, 150, and 200 gate wings one the two sides of each T-gate. The other part was metallised with Ni/Au (20/300 nm). This is an increase of 100 nm to the total metal stack due to increase in PMMA (gate foot resist) to increase the gate foot height and to keep resistance low.

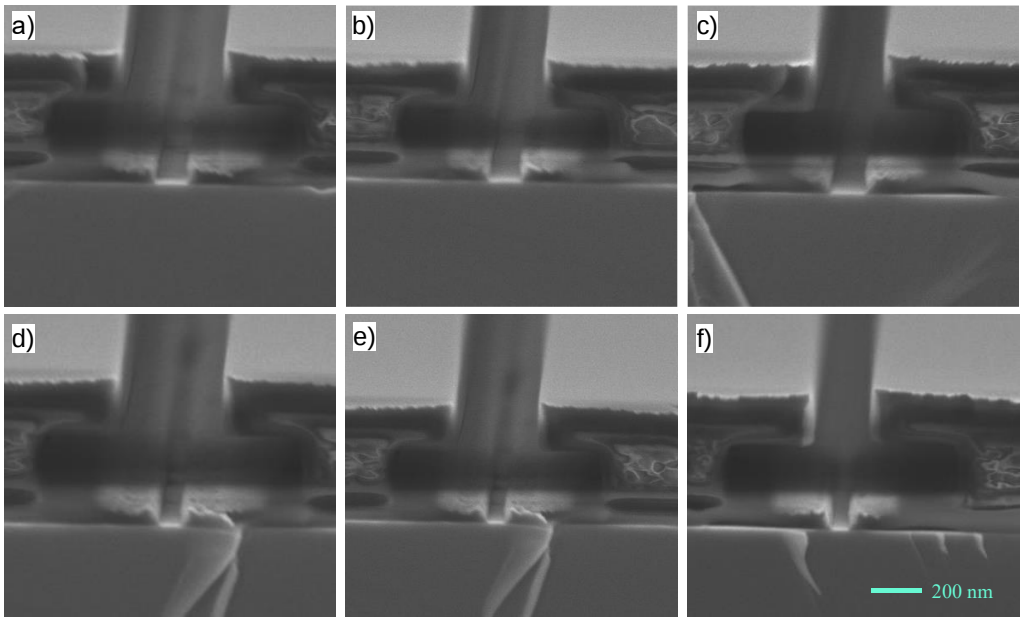


Figure 4.7 Cross section of resist profiles of the cleaved sample with 2 nm Pt coated. Figures a)-c) are for 100 nm gate lengths with 500, 400, and 300 nm gate head respectively. Figures d)-f) are for 50 nm gate lengths with 450, 350, and 250 nm gate head respectively.

It is possible to adjust the sensitivity ratio by varying the exposure dose or developing time of PMMA for example, to a higher or lower scale factor. However, higher sensitivity ratio affects larger features that are required to write along with gate foot such as gate pads which cause the bloating effect [106]. This effect is caused by the backscattered electrons for the high dose. On the other hand, if the sensitivity ratio is too low for example to 1:1.4, the gate foot becomes extremely reduced such that it become inseparable with the gate head and the T-shape structure possibly becomes undefined. In the various dose test measurements carried out on various test samples, we found that 3:1 ratio provides better resolution providing excellent control of the foot-length and keeping it free from bloating effect [106].

The use of GenIsys LAB modelling software in conjunction with the experimental work allowed for the simulation of the resist cross-section after development. By importing various data such as contrast curves, Point Spread Function (PSF) file, resist thickness, and their properties, the software was able to accurately predict the resist profile. The simulation results obtained from GenIsys LAB were found to agree with the experimental observations, indicating the reliability of the software. Figure 4.8 provides an example of the simulation results for a T-gate with a 50 nm gate foot, considering the same developing time for each layer. This figure demonstrates the capability of the software to accurately represent the resist profile and validate its predictive power. This software offers several benefits such as enabling researchers to explore different scenarios and optimise device parameters by modifying various parameters within the simulation environment. In the context of the T-gate structure, the software could be used to further reduce the gate foot to sub-50 nm by adjusting the resist stack or exploring other modifications. By leveraging the modelling software, researchers can save time and resources by virtually testing different designs and process parameters before committing to fabrication. This allows for iterative improvements and optimisation, leading to enhanced device performance.

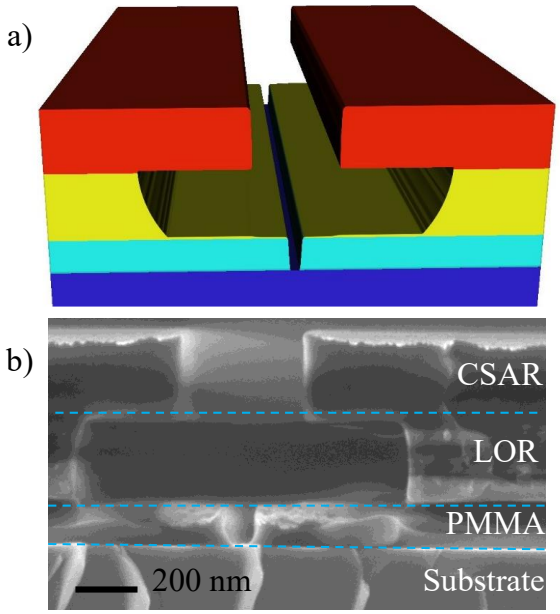


Figure 4.8 Cross section of developed images of 50 nm gate foot with 294 μC/cm^2 dose exposure and using 30 seconds Amyl Acetate, 25 seconds in CD-26 and 30 seconds in MIBK. a) LAB simulated cross section, b) SEM image of developed resist profile.

The results demonstrated well-defined T-gate profiles using the new resist stack, resulting in a high yield. Out of 162 T-gates fabricated, only 2 gates toppled during blow drying after the fabrication process. This indicates a robust fabrication process with excellent stability. Figure 4.9 illustrates a series of fabricated T-gates, showcasing a wide range of sizes and doses. This figure provides a visual representation of the diversity in dimensions and profiles achieved during the fabrication process. Table 4.3 presents a comparison between the designed and fabricated dimensions of various T-gates with different foot and head sizes (2 wings plus gate foot), based on two different doses. The table displays the results for two different gate foot lengths (50 and 100 nm), with each foot showing the corresponding three gate heads of the designed versus fabricated T-gates. This allows for a comprehensive analysis of the variations in size between the intended design and the actual fabrication. As illustrated, the fabricated gate foot closely matches the designed gate foot in both doses. However, the gate heads appear slightly larger than the intended design. This discrepancy may be attributed to the specific location of the measurement taken for the gate head. It is possible that the measurement point differs from the exact intended location, resulting in slightly larger measured dimensions.

Table 4.3 Summary of measurements of T-Gate dimensions for two different doses. In all case the target foot height was 150 nm.

Foot length (nm)			Gate Head (nm)			Foot height (nm)	
Design	294 μC/cm²	414 μC/cm²	Design	294 μC/cm²	404 μC/cm²	294 μC/cm²	404 μC/cm²
50	52	68	250	317	304	110	117
50	55	59	350	402	414	110	110
50	47	61	450	506	522	112	100
100	102	119	300	341	363	114	105
100	89	106	400	456	463	104	115
100	104	110	500	543	575	113	111

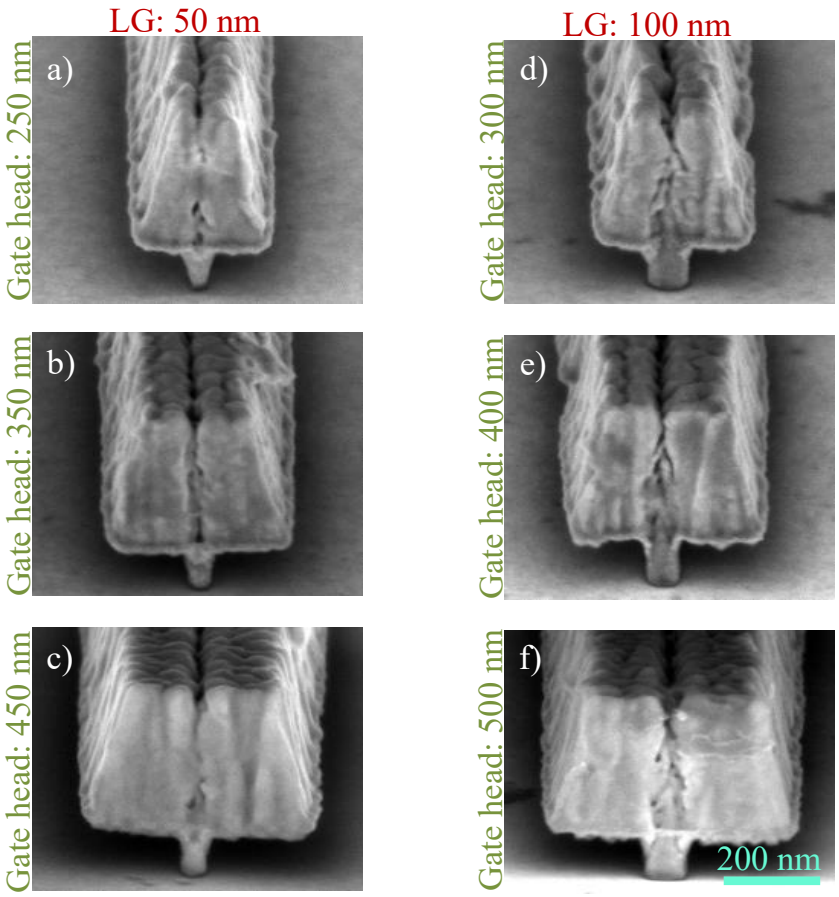


Figure 4.9 SEM images at 75-degree angle of fabricated T-Gates after metallisation and lift-off. There are two different gate foots 50 nm and 100 nm as indicated on the top of the images and different gate heads as indicated next to each image.

4.5 Conclusion

In this work, a novel nanofabrication technique for T-shape gates of sub-100 nm gate lengths has been discussed. The results of this fabrication process are robust, and well-defined T-shape gates were fabricated. We also eliminated the bloating problem for the contact pads of the gates by using a compromised dose ratio between the gate head resist and gate foot resist. We used 3 resist layers, CSAR for the gate head, LOR for the undercut, and PMMA for the gate foot. The dose ratio of 1:3, CSAR:PMMA was used to have CSAR cleared without interacting with PMMA resist and to prevent gate pad bloating. Also, each resist gets developed independently without interacting with other resists, which means we have very good control over the resists profile shape. Also, various sizes of different gate length and gate head designed and fabricated on the same EBL run without affecting their dimensions. Using this technique, a mechanically stable, large gate height was achieved without using any supportive layer as has been the practice in the previous experimental work.

Chapter 5

Heavily n-Doped GaN Cap Layer on AlN/GaN HEMTs

5.1 Introduction

One of the major technological challenges in the effective deployment of efficient GaN based HEMTs is achieving high quality ohmic contacts with low resistance, and smooth surface morphology. In RF applications, low ohmic contact resistances results in higher transconductance and high cut-off frequencies. In GaN-based HEMTs, realising good ohmic contact profile is often hindered by the material property of GaN (AlGaN or AlN). Owing to the high insulating characteristics caused by wideband gap, obtaining lower Schottky barrier (<< 2.5 eV) is difficult making it challenging to optimise the metal/GaN ohmic contacts. Basically, metals with appropriate work functions are usually required to achieve lower barrier for the emission of majority carriers [116]. Conventionally, Ti/Al and Ti/Al/X/Au (X stands for Pt, Ni or Mo) schemes thermally annealed at optimum temperature in nitrogen (N_2) ambient are used to realise low resistance ohmic contacts on GaN [117-120]. The aluminium (Al) is employed to reduce the tendency of Ti-GaN reaction which could lead to high nitrogen vacancies resulting in void formation

[121]. These schemes are however found to exhibit bumpy surface morphology after the high temperature anneal. The bumpy surface morphology is attributed to the residual elemental Al metal after the anneal which often results in the increasing sheet resistance of the device upon aging. This was however reported to occur only when a thick Al layer is used [122]. Various fabrication techniques were applied on these stacks with a view to achieving substantial reduction in the ohmic contact resistance [74, 123-125]. To achieve even lower contact resistances, contact regions are normally etched through to the channel layer followed by regrown of a heavily doped GaN (> $7x10^{19}cm^3$) layer to establish a direct contact with 2DEG. This technique however is disadvantaged by the need for a complex, time consuming and expensive regrowth process.

In this project, we report a new technique for achieving low ohmic contact resistance devoid of the need for regrowth, using a highly n-doped 5 nm thick GaN cap layer on AlN/GaN HEMT structure which helps reduce the contact resistance of the device. We achieved very low ohmic contact resistance of 0.13 Ω.mm and sheet resistance of 473 Ω/sq as will be described in the following section.

5.2 Device Structure and Experiment

The epitaxial structure used in this work was grown by Qrona technologies, USA, using molecular beam epitaxy (MBE), on sapphire substrate as shown in Figure 5.1. The aim of this study was to examine the impact of a heavily doped GaN cap layer on ohmic contact resistances. Due to low cost, a sapphire substrate was used for the experimentation. In these chapter three experiments were carried out. Experiment one (Gate-wrap around standard HEMTs) was carried out by etching the heavily doped GaN cap layer under the gate region and then fabricating a standard AlN/GaN HEMT using gate wrap-around drain technique. Experiment two (Gate-wrap around MOS-HEMTs) was carried out by etching cap layer under the gate region to fabricate AlN/GaN MOS-HEMT employing SiO_2 gate dielectric using gate wrap-around drain technique. Experiment three (High-Frequency T-shaped gate HEMT) was carried out by etching heavily doped GaN cap layer under the gate region and fabricate standard AlN/GaN HEMT using RF layout device structure. All fabrication steps for experiments one and two were defined using

photolithography. However, in experiment three, EBL was utilised for certain nano-features such as T-gates, as well as critical steps like ohmic contacts and gate recess. This incorporation of EBL in experiment three allowed for greater precision and control over these specific features, enhancing the overall fabrication process.

In order to analyse the ohmic contact resistance, prior to the implementation of the above-mentioned experiments, a CTLM structure was fabricated on the wafer subsequent to which measurements were carried out. Moreover, the heavily doped GaN cap layer had to be removed at the gate region. For that purpose, we required to develop an appropriate recipe for a precise etching of the layer without affecting the 3 nm AlN barrier layer beneath. These processes are discussed in the sections below.

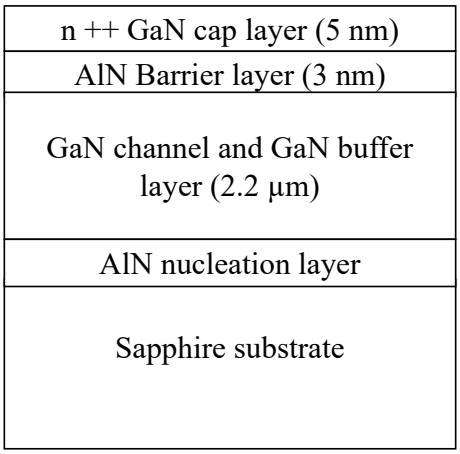


Figure 5.1 Epitaxial structure of heavily doped GaN cap layer on AlN/GaN HEMT grown using MBE. The cap layer was 5 nm GaN layer with a Si-doping density of $1x10^{19}$ cm^3 [126].

5.2.1 Analysis of Ohmic Contact Resistance with CTLM

As mentioned earlier, the circular transfer length method (CTLM) was used for contact resistance measurements. The diameter of the centre circle of the CTLM structure was 150 μm with the gap spacings, (L) of 4, 8, 12,16, 20, 24, 28, and 32 μm. The fabrication starts with the standard cleaning procedure for the samples. Then, the ohmic metal stack of Ti/Al/Ni/Au (20/180/40/100 nm) was

deposited using electron beam evaporator, followed by a lift-off process, and annealing at 800°C for 30 secs. The designed CTLM structure is as shown in Figure 5.2 (a). Measurements were carried out before and after performing the high temperature annealing step. Comparison in the measurements between the non-annealed and annealed ohmic contact is shown in Figure 5.2 (b). The measured contact resistance and sheet resistances were in the range of 3.29 Ω.mm to 10.89 Ω.mm and 204 Ω/sq to 442 Ω/sq for non-annealed ohmic contacts, respectively. The measured contact resistance and sheet resistances were in the range of 0.132 Ω.mm to 0.696 Ω.mm and 346 Ω/sq to 473 Ω/sq for annealed ohmic contacts, respectively. These measurements obtained with the heavily doped 5 nm heavily n-doped GaN cap layer demonstrated that low ohmic contact resistance could be achieved.

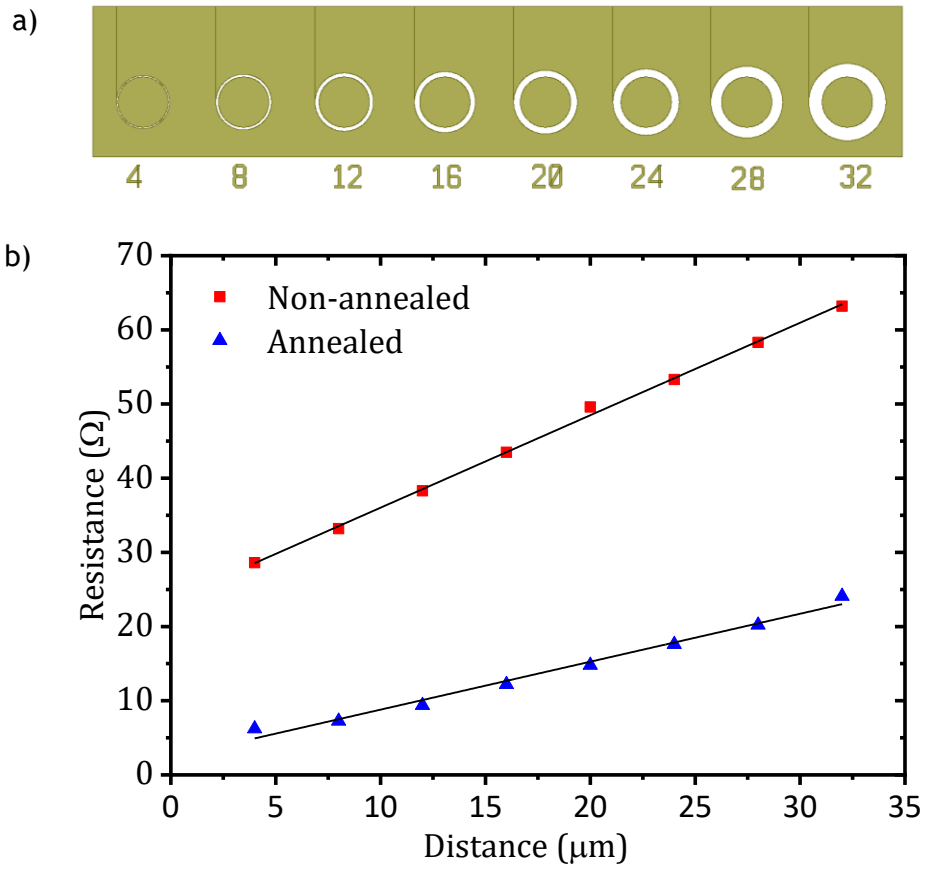


Figure 5.2 (a) Top-view layout of CTLM structure, (b) CTLM measurements for both non- annealed and annealed contact resistance of heavily doped n++GaN/AlN/GaN HEMT structure.

5.2.2 Development of Etching Recipe for 5 nm n++ GaN Cap Layer

The etching recipe for the removal of 5 nm heavily n-doped GaN cap layer in the gate region was developed and optimized prior to commencing the fabrication of the devices. This step was necessary to avoid the gate contact to the heavily doped cap layer.

Four (4) samples were prepared and processed to find the etch rate of the heavily doped n-GaN cap layer using the SF_6/N_2 with flow rates of 20/20 sccm, RF power of 70 W power and pressure of 50 mTorr at etching times of 30, 60, 120, and 180 seconds, respectively. The microscopic images of the processed samples were viewed and measured using the atomic force microscopy (AFM) tool upon which very rough surface morphology was observed on the etched regions for samples with etching time of 30-, 60-, and 120-seconds causing difficulty in measuring a precise etch depth. In contrast, samples with 180 seconds etch time, a smooth surface was obtained and the measured etch depth was ~10 nm as shown in Figure 5.3. This result shows that the recipe etches beyond the AlN barrier layer. It is crucial to precisely stop the etch exactly at 5 nm to avoid eroding the thin 3 nm AlN barrier layer, to achieve uniform transistor characteristics, in particular the gate threshold voltage. To solve this problem, a process of selective etching of n-GaN with respect to AlN was developed using the mixture of SF_6 and O_2, whereby the O_2 reacts with aluminium (from the AlN barrier layer) forming Al_2O_3 layer which drastically slows down etching rate. The optimised recipe obtained from this process was SF_6/O_2 with flow rates of 20/20 sccm, RF power of 70 W power and pressure of 50 mTorr using etch times of 60, 120, 180 seconds. From the AFM images obtained in Figure 5.4 (b), the etching time of 120 seconds shows the complete removal of 5 nm n-GaN cap layer. The etched surface of this sample was smooth, and the measured surface roughness of 2.28 nm and 2.10 nm were obtained both for the etched and as-grown samples respectively as shown in Figure 5.4 (a). Figure 5.5 shows the top view of scanning electron microscope (SEM) image of the fabricated AlN/GaN HEMT structure with an n-GaN cap layer.

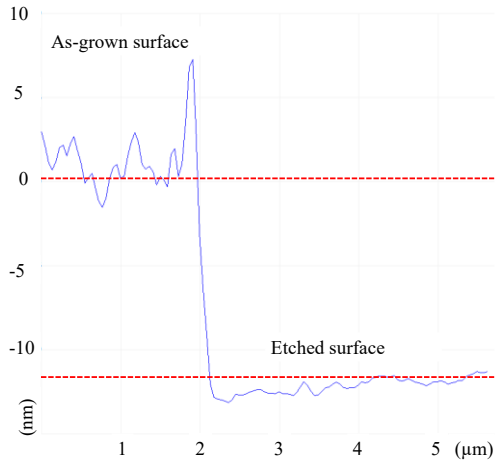


Figure 5.3 AFM step height of 180 seconds etch time using SF_6/N_2.

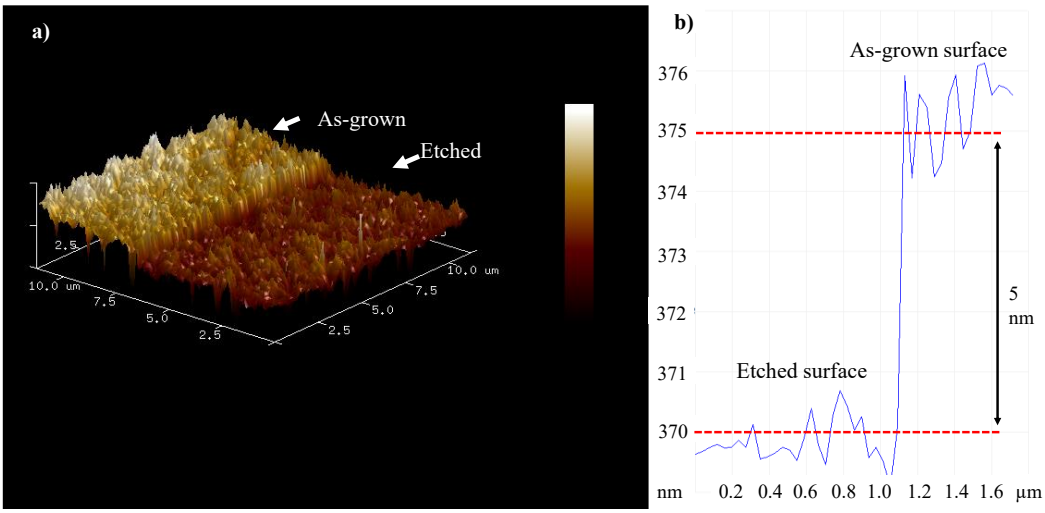


Figure 5.4 AFM scan of the heavily doped GaN cap layer, showing the roughness of cap layer as-grown and etched area (a) AFM 3D image showing the roughness of as grown and etched of the sample, (b) AFM step height.

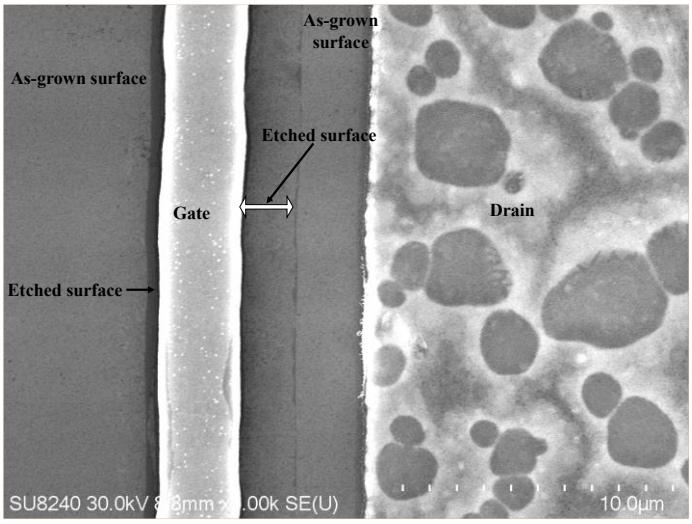
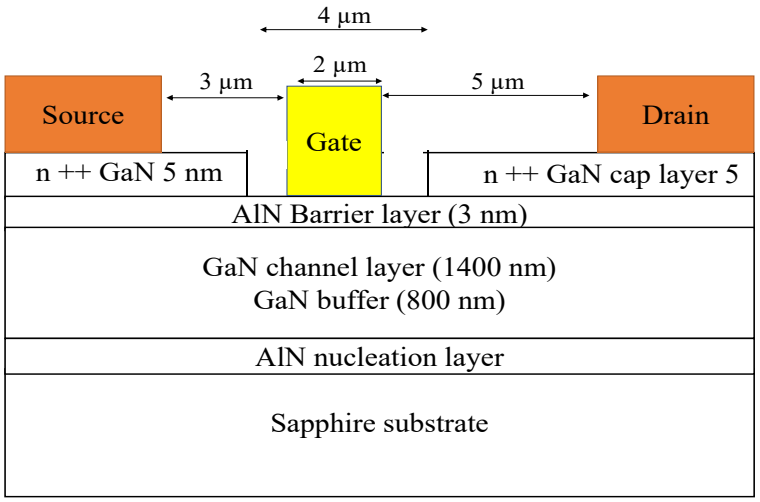


Figure 5.5 Top view of SEM image of n++ GaN/AlN/GaN HEMT structure.

5.2.3 Gate-Wrap Around Standard HEMT (Experiment One)

In this experiment, an AlN/GaN HEMT on sapphire substrate was designed and fabricated with a gate length, L_G, of 2 µm, gate-to-source distance, L_{GS}, of 3 µm, gate-to-drain distance, L_{GD}, of 5 µm, and gate width, W_G, of 75 µm as illustrated in Figure 5.6 (a). A fabricated gate wrap around device layout was used in this experiment as shown in Figure 5.6 (b).

a)



b)

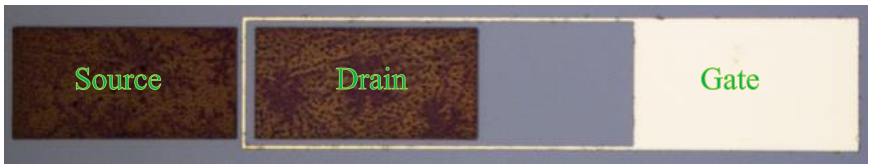


Figure 5.6 (a) Cross-section schematic diagram of fabricated n++ GaN/AlN/GaN HEMT structure. Device dimension used in this work is as follows: Gate length, L_G = 2 µm, gate-to-source distance, L_{GS} = 3 µm, gate-to-drain distance, L_{GD} = 5 µm, and gate width, W_G = 75 µm. (b) Top view of fabricated gate wrap around drain device on n++ GaN/AlN/GaN HEMT.

The fabrication process was started by depositing metal stack of Ti/Al/Ni/Au for ohmic contacts followed by high temperature anneal at 800 °C for 30 seconds in N_2 atmosphere. Prior to gate metallisation, a 5 nm n++ GaN cap layer in the gate region was selectively removed using the recipe developed in Section 5.2.2 (SF_6/O_2). The gate was then formed by depositing metal stack of Ni/Au (20/400 nm) at the etched region. The fabrication processes are illustrated in Figure 5.7 (a)-(d). DC measurements were carried out on the fully completed device at room

temperature using Keysight's B1500A Semiconductor Device Analyzer and the results are discussed in the following sections.

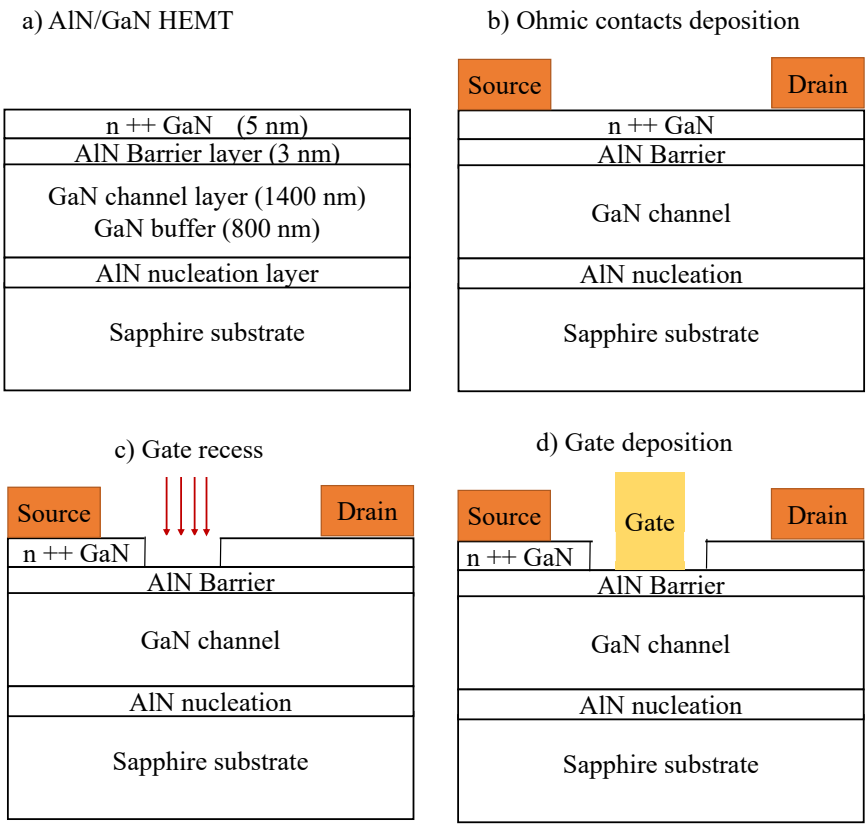


Figure 5.7 Schematic views of the process flow for fabrication flow of AlN/GaN HEMT on sapphire using gate wrap around drain technology. (a) Cleaned wafer, (b) Deposition of Ti/Al/Ni/Au metal stack, ohmic contacts, (c) Removing heavily doped cap layer under gate region by dry etch method, (d) Gate formation.

5.2.4 Gate-Wrap Around MOS-HEMTs (Experiment Two)

Experiment two is similar to Experiment one in terms of fabrication process, material and device structure, except that after etching out the 5 nm n-GaN cap layer, a layer of 5 nm thick SiO_2 was deposited over the entire surface of the device using PECVD, followed by the deposition of Ni/Au metal stack at the gate region. The 5 nm thick SiO_2 layer in the ohmic contact regions was removed using the mixture of CHF_3 and Ar gases at a flow rate of 25 and 25 sccm respectively, RF power of 50 W, and 30 mTorr at 20 °C for 60 seconds for measurement

purposes. Figure 5.8 shows the cross-sectional view of the device consisting of a layer of SiO_2 gate dielectric layer.

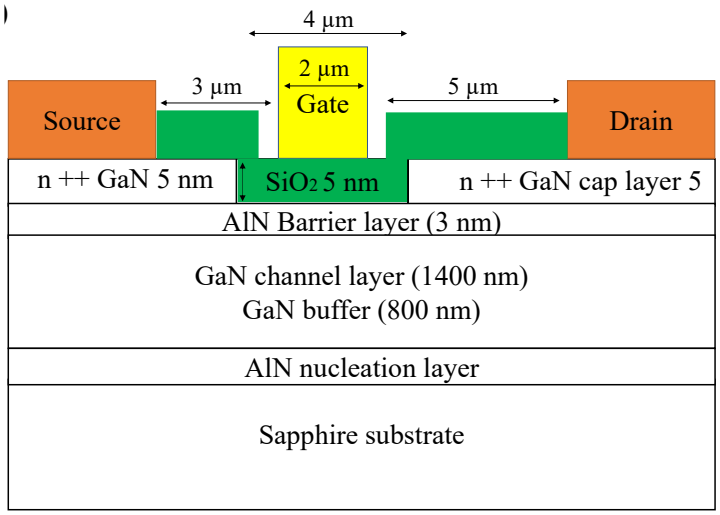


Figure 5.8 Cross sectional view of fabricated device on heavily doped cap layer employing SiO_2 gate dielectric layer.

5.2.5 T-Gate RF HEMT (Experiment Three)

To further analyse the influence of the heavily doped GaN cap layer on the performances of the high-frequency devices, a T-gate RF-device layout was designed on the same wafer. For this experiment the fabrication requires the use of both photolithography and electron-beam lithography (EBL) patterning techniques. The EBL is used where critical fabrication and device features in markers, gates, gate recess region and ohmic contacts, while photolithography used on mesa and bond pad patterning.

Device fabrication began by the depositing metal stack of Ti/Pt (20/100 nm) for makers defined using EBL. Because platinum (Pt) has poor adhesive to gallium nitride, titanium (Ti) was used as a base layer between the GaN cap and the Pt. In order to achieve proper alignment, deposition of markers prior to any fabrication steps is fundamentally important. But this requires the use of metal with better resolution while using EBL and high temperature tolerance due to annealing. Platinum (Pt) is specially selected due to its property of good contrast

for pattern recognition, and tolerance when exposed to high annealing temperature during the formation the ohmic contacts.

A metal stack of Ti/Al/Ni/Au (30/180/40/100 nm) was deposited for ohmic contacts defined using EBL, followed by high temperature anneal at 800 °C in the N_2 atmosphere. Mesa isolation was achieved using plasma-based dry etch tool with Cl_2/Ar, to isolate the active area defined using photolithography. The 5 nm heavily doped GaN layer under the gate region was etched out using the recipe optimised in Section 5.2.2, followed by deposition the T-gate structure in the recessed region defined using EBL. RF bond pads were finally deposited, and measurements were carried out on the completed device. Fabrication steps are illustrated in Figure 5.9 (a)-(f), and the design and SEM image of one of T-gate devices are shown in Figure *5.10* (a-c) and Figure 5.10 (d) respectively. Results obtained are discussed in Section 5.3.

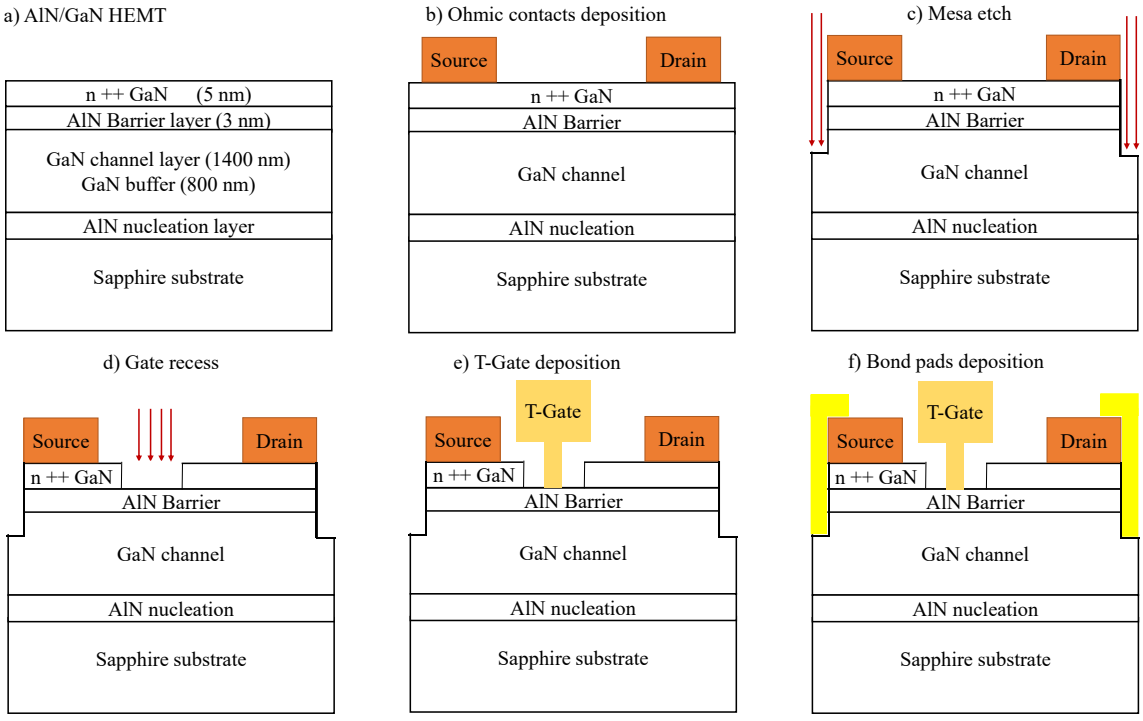


Figure 5.9 Schematic views of the process flow for fabrication flow of AlN/GaN HEMT on sapphire using T-gate technology in RF layout. (a) Cleaned wafer, (b) Deposition of Ti/Al/Ni/Au metal stack, ohmic contacts, (c) Photolithography to expose deep mesa-etch pattern, (d) Removing the cap layer under the gate region (e) T-gate formation, (f) Bond pads contacts deposition.

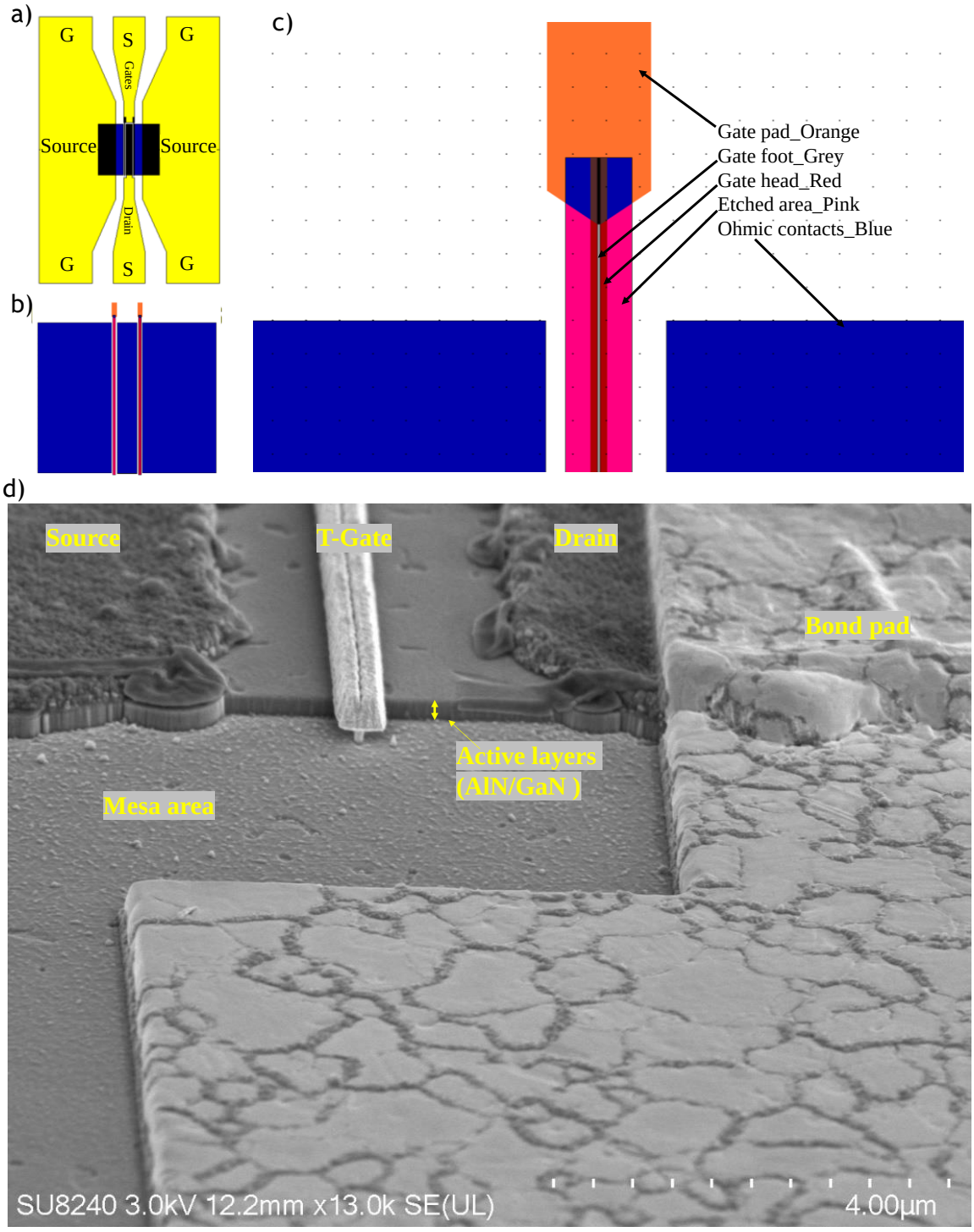


Figure 5.10 (a) RF layout design of the T-gate using L-Edit, (b) two finger T-gates between source and drain, (c) Zoomed-in on the T-Gate structure, (d) SEM image of fabricated device using T-Gate technology.

5.3 Measurements, Results, and Discussion

5.3.1 Gate-Wrap Around Devices (Experiments One and Two)

DC measurements were conducted using the Keysight's B1500A Semiconductor Device Analyser. The gate wrap around devices were measured using three single probes, one assigned to each of the source, drain and gate electrodes.

DC parameters of devices in experiments one and two were measured by sweeping the gate voltage from V_{GS} = -4 to +3 V for the Schottky gate HEMT, and V_{GS} = -9 to +3 V for MOS-HEMT at the step of 1 V and drain voltages from V_{DS} = 0 to +10 V. Measured output, transfer characteristics, gate leakage current, and off-state breakdown voltage were obtained as shown in Figure 5.11, Figure 5.12, Figure 5.13, and Figure 5.14 respectively.

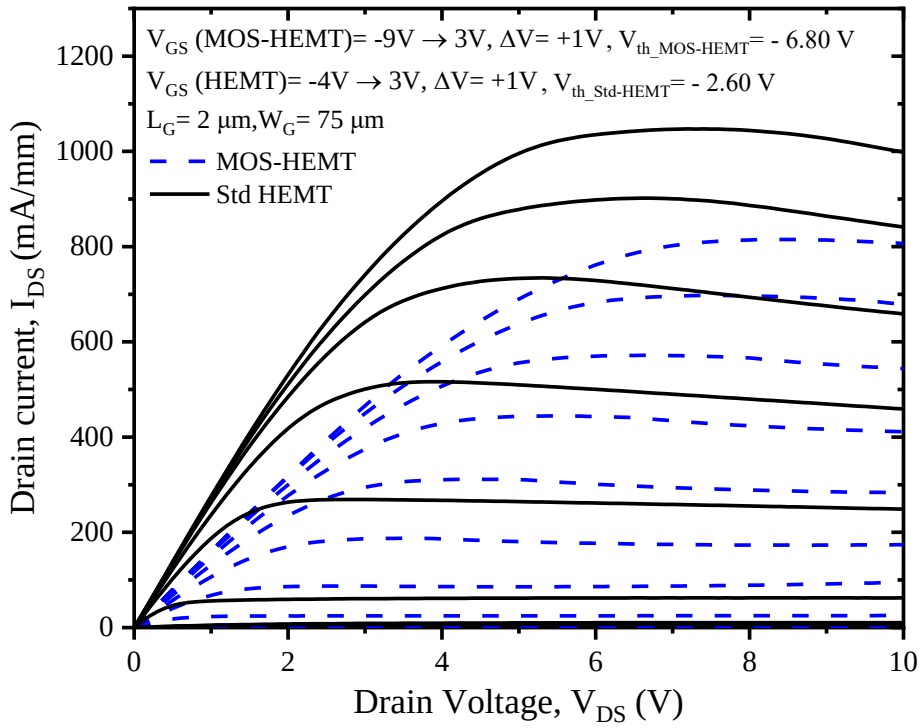


Figure 5.11 Measured output characteristics of fabricated devices with a gate-to-source voltage, V_{GS}, biasing from -4 V to 3 V (with step size of 1 V) for the standard AlN/GaN HEMT and -9 V to 3 V (with step size of 1 V) for MOS-HEMT.

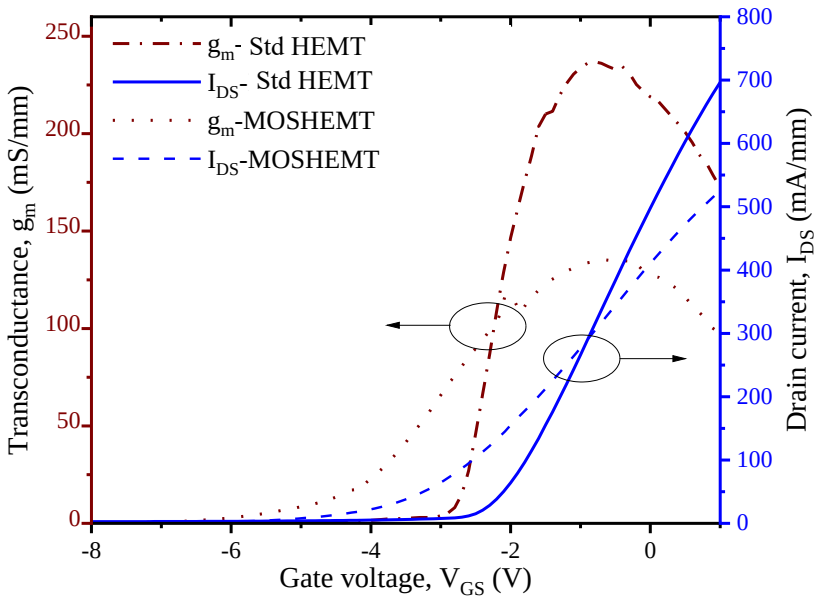


Figure 5.12 Measured transfer characteristics of fabricated devices (Std HEMT and MOS-HEMT) at a drain-to-source voltage, V_{DS} = 5 V.

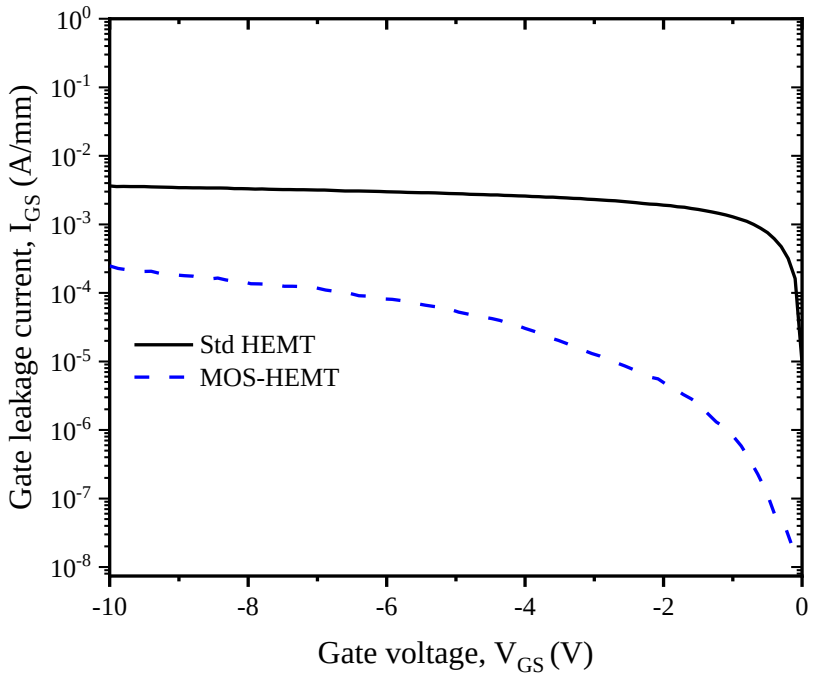


Figure 5.13 Gate leakage current of standard AlN/GaN HEMT and AlN/GaN MOS-HEMT.

Output characteristics curves in Figure 5.11 show the maximum drain current obtained from gate-wrap around Std HEMT and gate-wrap around MOS-HEMT to be 1000 mA/mm and 300 mA/mm respectively at $V_{GS} = V_{th}+6$ V (~$V_{GS\_Std\ HEMT}$ = +3V, and ~$V_{GS\_MOS\text{-}HEMT}$ = -1V). A short circuit test using 2 probes using Keysight's B1500A Semiconductor Device Analyser was conducted to determine the presence of any

unetched heavily doped GaN caped layer on the MOS-HEMT devices. In this test, one probe was connected to the gate contact, while the other probe was connected to the drain/source. A voltage of up to 2V was applied, and the resulting current was measured. By analysing the current response, it is possible to identify whether there are any remaining unetched heavily doped GaN caped layers in the devices. As shown in Figure 5.15, there is some leakage current ~13 μA flowing from gate to source and ~23 μA from gate to drain.

In the transfer characteristic curve shown in Figure 5.12, the maximum transconductance (g_m) in standard HEMT 237 mS/mm higher than 135 mS/mm for the MOS-HEMT because of the higher drain current and smaller gate-to-2DEG separation in the former. The output characteristics (Figure 5.11) show a very high knee voltage (e.g +5 V for MOS-HEMT) cause by high contact resistance and surface traps.

The measured threshold voltage, V_{TH}, for standard HEMT, and MOS-HEMT were -2.6 V, and -6.80 V (extracted value at I_{DS} = 1 mA/mm) respectively. There is a shift toward the negative value of the measured threshold voltage of the MOS-HEMT due to the insertion of 5 nm SiO_2 gate dielectric.

Figure 5.13 clearly shows high gate leakage in all the devices, however, as expected the leakage is significantly supressed in MOS-HEMT compared to the standard HEMT. This reduction due to the surface passivation using the dielectric layer. Figure 5.14 shows the off-state breakdown voltage for standard HEMT and MOS-HEMT to be 95 V and 73 V respectively. Ideally, the passivated device is expected to have much higher breakdown than the un-passivated HEMT contrary to what is obtained. This can also be linked to the leakage path created by the under etched heavily doped GaN layer. Table 5.1 summaries the results of experiments one and two on gate wrap around standard HEMT and MOS-HEMT.

Table 5.1 Summary of the results of Std HEMT and MOS-HEMT using wrap around gate technology.

Parameters	Std HEMT	MOS-HEMT
V_{th} [V]	- 2.6	- 6.8
I_{DS_max} @ V_{GS} = V_{th}+6 V [mA/mm]	1000	300
g_m [mS/mm]	237	135
V_{BR} [V]	95	73
I_{GS} @ V_{GS}= -10 V [A/mm]	$6x10^{-2}$	$7x10^{-3}$

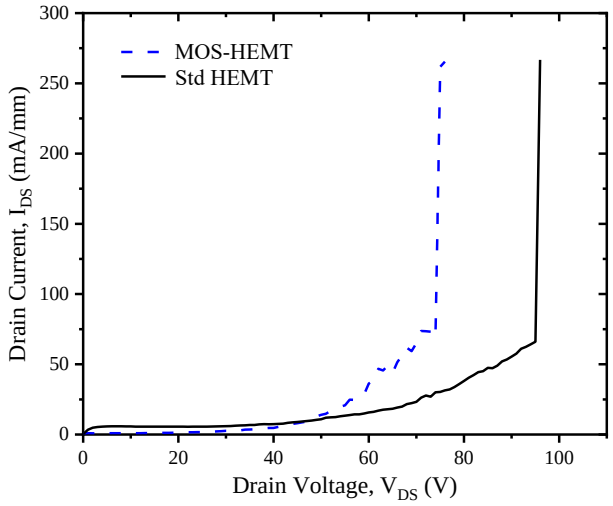


Figure 5.14 The off-state breakdown characteristics of fabricated devices for standard AlN/GaN HEMT and AlN/GaN MOS-HEMT.

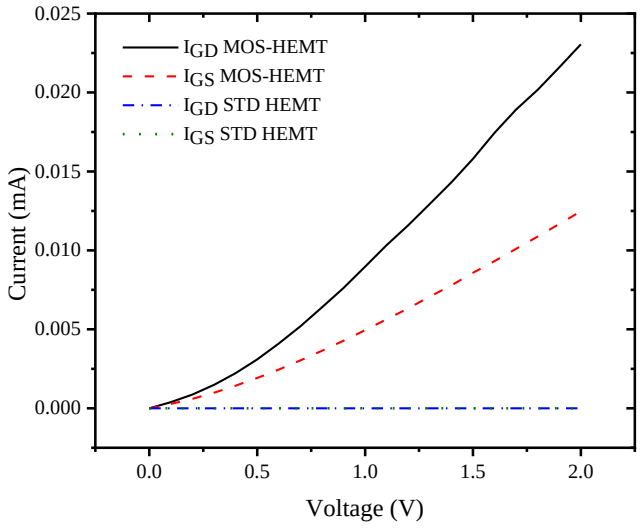


Figure 5.15 Short circuit test for the AlN/GaN MOS-HEMT with heavily doped cap layer compared to a standard AlN/GaN HEMT.

5.3.2 T-Gate RF HEMT (Experiment Three)

Figure 5.16 shows the output DC characteristics of the fabricated 100-nm T-gate Standard Schottky gate AlN/GaN HEMT. The maximum drain current at V_{GS} = 1 V was 988 mA/mm, and the peak extrinsic transconductance at V_{DS} = 7 V was 193 mS/mm as shown in Figure 5.17. In theory, higher drain current and transconductances are expected for devices with smaller gate length. However, results obtained from gate wrap around experiment compared to this experiment (T-gate RF HEMT) show a contrary, that may arise from fabrication issues such as poor surface morphology due to dry etch, which could yield traps responsible for the reduction in drain current. Figure 5.18 illustrating the gate leakage current of fabricated device which shows an improvement as compared to experiment one and comparable with experiment two where a dielectric layer is used.

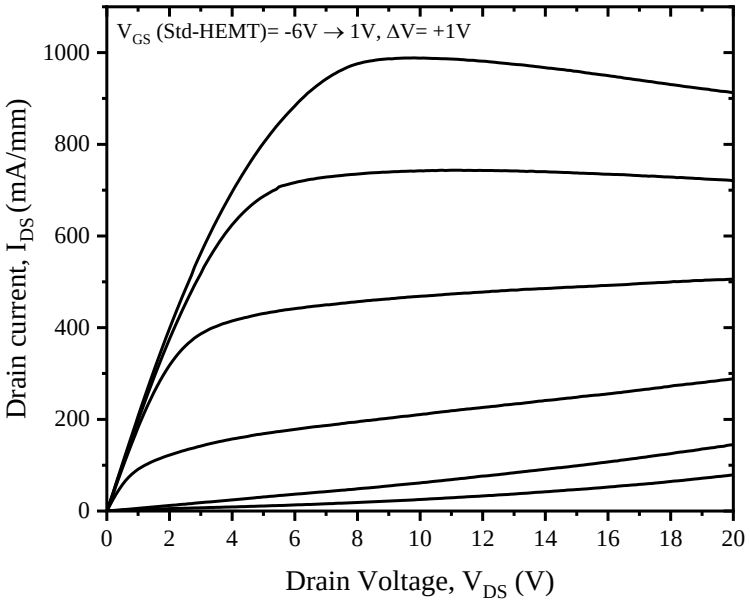


Figure 5.16 Measured output characteristics of fabricated 100 nm T-gate on AlN/GaN HEMT with a gate-to-source voltage, V_{GS}, biasing from -6 V to 1 V (with step size of 1 V).

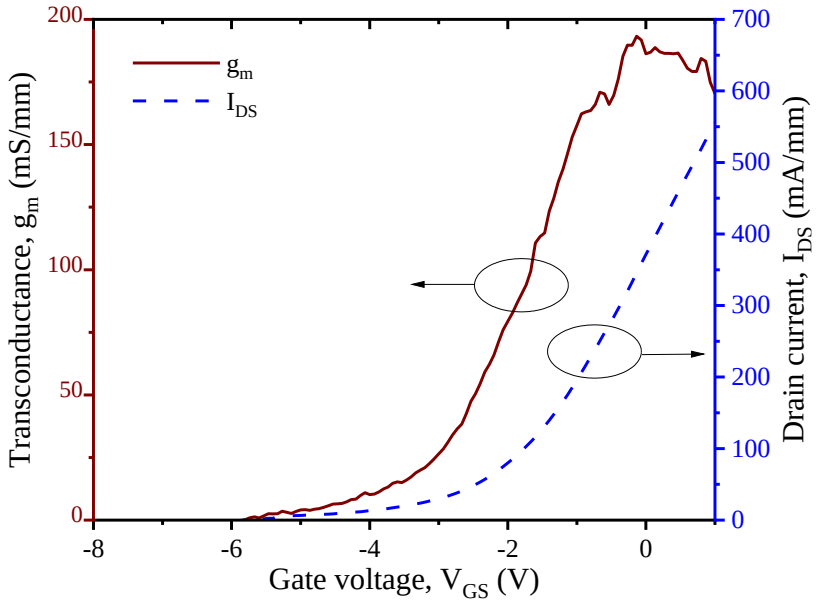


Figure 5.17 Measured transfer characteristics of fabricated AlN/GaN HEMT using T-gate technology at a drain-to-source voltage, V_{DS} = 7 V.

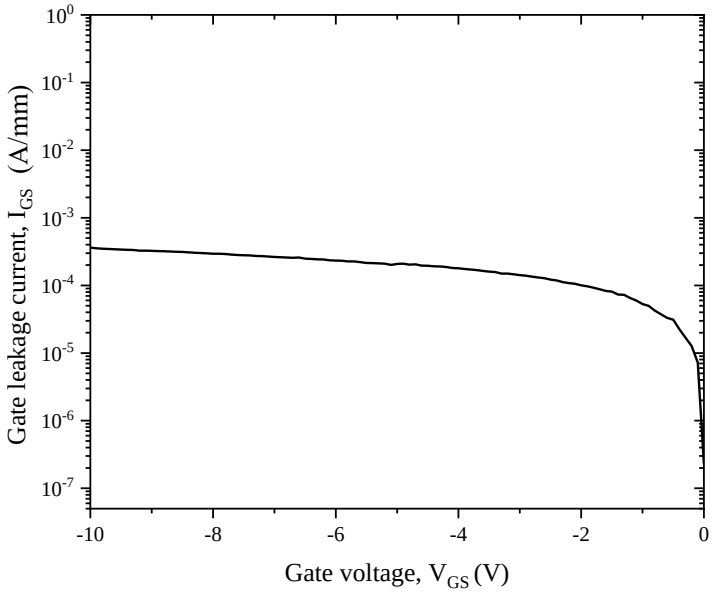


Figure 5.18 Gate leakage current of standard AlN/GaN HEMT using T-gate technology.

To obtain accurate cut-off frequencies (f_t) and maximum frequencies (f_{max}) of the devices, on-wafer measurements of open and short patterns on the related devices bond pads were performed using a Vector Network Analyzer (VNA). The RF performance of these devices was characterised from 0.45 to 110 GHz using Agilent Technologies E8361A VNA (10 MHz-67 GHz) with frequency extender using Agilent Technologies N5260 (up to 110 GHz). To start, the system was calibrated with a short-open-load-through (SOLT) calibration procedure. This is standard

approach used by many other researchers in the characterisation of high-frequency devices [46]. The calibration accuracy was checked by measuring the known 50 Ω standards. The magnitudes of S_{12} and S_{21} were less than ± 0.01 dB and S_{11} and S_{22} are less than −45 dB within the measured frequency range after the calibration as shown in Figure 5.19.

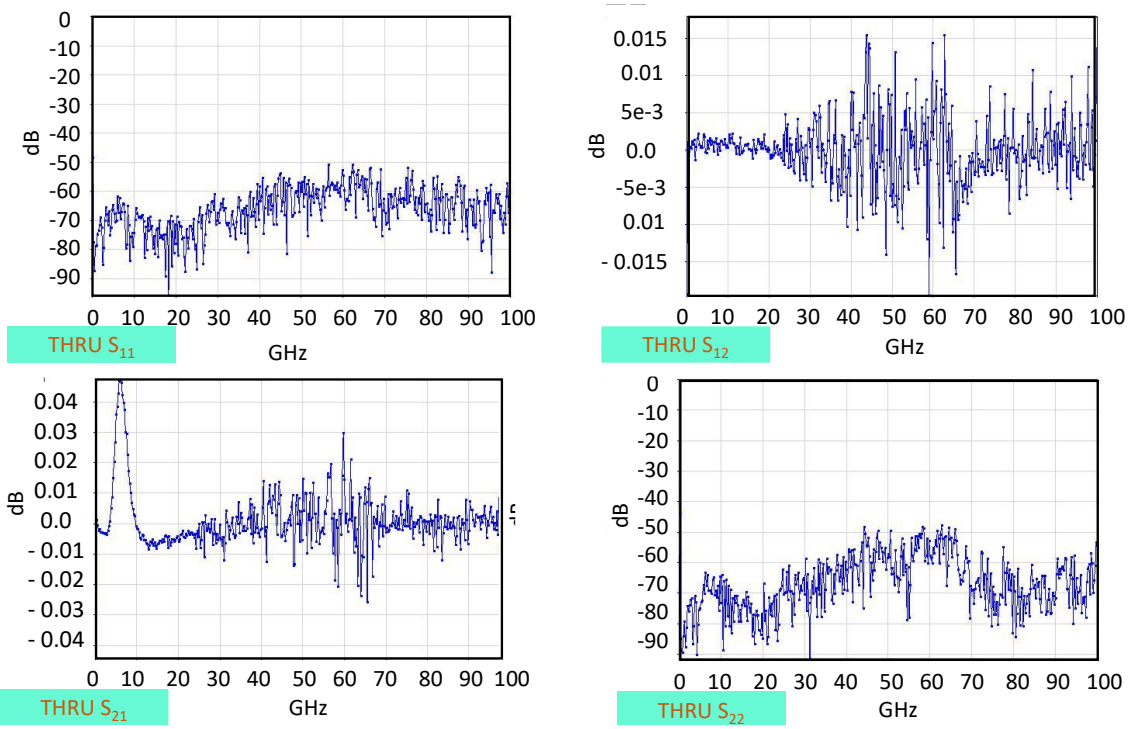


Figure 5.19 Magnitude and phase of the THRU measurement after correction with a SOLT calibration.

The obtained measurements provide information about the parasitic capacitances and inductances associated with the bond pads. After measuring the scattering parameters (S-parameters) of the devices with the bond pads, the effects of the parasitic pad capacitances and inductances were subtracted or de-embedded from the measured S-parameters. This de-embedding process is necessary to isolate the intrinsic performance of the devices by removing the unwanted effects introduced by the bond-pad parasitic. Cascade Microtech WinCal XE software was used for the de-embedding process. The software analyses the measured device S-parameters along with the known characteristics of the open and short patterns to separate the contributions of the parasitic elements from the overall measurements. Open pads are used to remove the effects of parasitic capacitance, while short pads are used to remove the effects of parasitic

inductance. By accurately de-embedding the parasitic effects, the cut-off frequencies (f_t) and maximum frequencies (f_{max}) can be determined with improved precision, providing valuable insights into the high-frequency performance of the devices.

Figure 5.20 shows the current gain H21 and Mason's gain (power gain U) which are used to obtain f_t and f_{max} frequency, respectively, by extrapolating measured data with a slope of −20 dB/dec using a least- squares fit. As shown in Figure 5.20, f_t and f_{MAX} are 73 GHz and 78 GHz respectively for 100 nm gate length at V_{DS} = 7 V, and V_{GS} = 0.5 V.

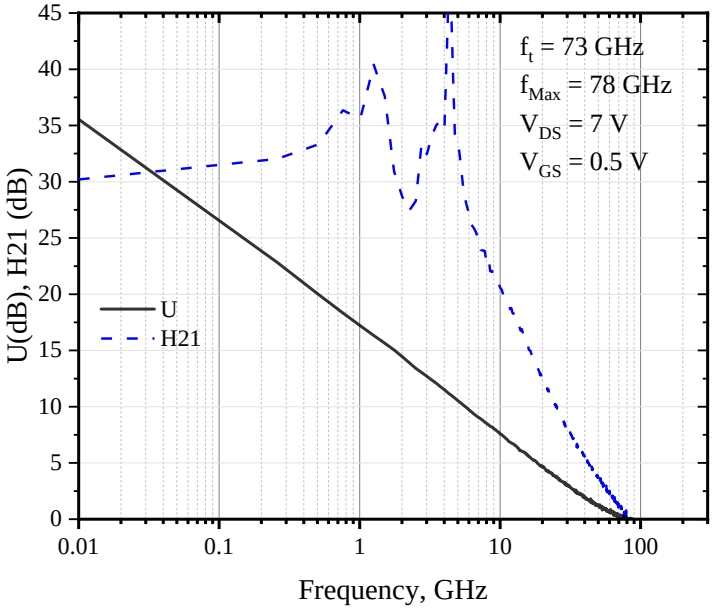


Figure 5.20 Cut-off and Maximum frequency of the T-Gate on AlN/GaN HEMT.

5.4 Summary and conclusions

Standard AlN/GaN HEMT and AlN/GaN MOS-HEMT devices have been successfully fabricated and characterised. The DC performance of the devices, including output characteristics, transfer characteristics, gate leakage current, and breakdown voltage, have been measured. For the AlN/GaN HEMT with T-gates technology in experiment 3, the device had a gate length of 100 nm, gate to source of 1 µm, and gate to drain of 2 µm. The measured results showed the following

performance characteristics: output current = 988 mA/mm at V_{GS} = 1 V, transconductance (g_m) = 193 mS/mm at V_{DS} = 7 V, and gate leakage current was Between $1x10^{-3}$ A/mm and $1x10^{-4}$ A/mm. Additionally, a cut-off frequency of 73 GHz and a maximum frequency of 78 GHz were achieved, with an associated current of over 700 mA/mm at V_{GS} = 0.5 V. Comparatively, state-of-the-art AlN/GaN HEMTs with a gate length of 20 nm, gate to source/drain of 50 nm, and regrown ohmic contact regions with heavily doped cap layers have achieved higher performance levels. These devices demonstrated a cut-off frequency of 454 GHz and a maximum frequency of 444 GHz, along with an associated current of I_{DS} = 900 mA/mm and a transconductance (gm) of 1.36 S/mm at V_{GS} = - 0.8 V [24]. While the results obtained in [24] are desirable, an observation can be made from their I-V curve indicating that the device does not exhibit complete pinch-off and the measurements were only taken up to a V_{DS} = 4 V. However, in this work, despite demonstrating slightly lower performance metrics, including cut-off frequency, maximum frequency, associated current, and transconductance, it introduces an improvement by incorporating an n-doped GaN cap on the AlN barrier. Notably, this improvement is achieved without resorting to the complex and expensive process of ohmic regrowth. Additionally, the design can be further optimised by rescaling through the reduction of gate length and source-to-drain spacing, which holds the potential for further enhancing the device performance.

Chapter 6

GaN on Diamond HEMTs

6.1 Introduction

As mentioned earlier, due to high cost and smaller size of gallium nitride wafers (2 inches), GaN HEMTs are commonly grown on foreign substrates such as sapphire, SiC and silicon. Despite the exceptional material properties of GaN, there are several challenges that hinder the widespread deployment of GaN devices in high-frequency applications across industries such as automotive, radar, communication, and space. One of the current challenges of RF GaN HEMTs is the lack of efficient heat extraction technology which results in the increasing channel temperature while the device is in operation, detrimental to the performance and reliability of the device [127-130]. Overcoming this problem requires growing the GaN active layers directly on an excellent heat extracting material.

Advantages of low cost and large wafer size, makes silicon a commonly used substrate for GaN electronic devices. However, the poor thermal properties (130 W/m-K) and high lattice mismatch (17%) [131] of GaN on Si, limits the realisation of the achievable power density of GaN material. SiC with smallest lattice mismatch (3.5%) [131] resulting in lower dislocation density, and high thermal conductivity (450 W/m-K) [132] has been used as substrate to extract

heat out of the operating device. Apart from the high cost, SiC also requires nucleation layer to limit the effect of lattice mismatch which results in thermal barrier resistance and growth defects at the interface, limiting the thermal dissipation property [133].

In recent years, attention has been given to GaN on diamond substrate technology (through some bonding/adhesion process), owing to its high thermal conductivity of diamond (up to 2000 W/m-K) [128, 132, 134]. The use of chemical vapour deposition (CVD) diamond as substrates has been demonstrated with promising results of increased power density in GaN HEMTs without an increase in the junction temperature [129, 135]. The enhanced performance is attributed to the reduction in the thermal boundary resistance (TBR) between the heat spreading diamond and the GaN layers [128]. However, direct bonding of GaN on diamond results in poor material quality and film cracking due to high lattice (~13%) and thermal (GaN~1.0×10^{-6} K^{-1}, diamond~3.17×10^{-6} K^{-1}) mismatches between GaN and diamond [136, 137]. To limit the effect of mismatches, an adhesion layer (typically Si_3N_4) is usually used between the GaN and the diamond substrate. Insertion of an interlayer introduces thermal boundary resistance which affects the thermal conductivity. Various techniques for an improved integration of GaN wafer on diamond substrate have been reported [34, 132, 137-139].

This chapter focuses on carrying out experiments to investigate the impact of varying thicknesses of CVD diamond substrates and buffer/channel layers on the performance of GaN HEMTs. The experiments leverage T-gate technology to analyse the behaviour of these devices under conditions of high-frequency and high-power operations. The goal is to understand how changes in substrate and buffer/channel layer thickness influence the overall performance characteristics of GaN HEMTs in the context of these demanding operational scenarios. The experiments were carried out using three identical wafers with differences in the thicknesses of buffer and substrate layers as described in the coming section.

6.2 Device Structure and Fabrication Process

The AlGaN/GaN HEMT epitaxial structures were realised on 4-inch CVD diamond wafers using metal organic chemical vapor deposition (MOCVD) by Akash Systems. We evaluated the electrical performance of devices from three different wafer structures shown in Figure 6.1, each consisting of 2 nm GaN cap, 20 nm AlGaN barrier with 25% aluminium content, and 30 nm Si_3N_4 seeding layer. Wafers 1 and 2 also consist of 750 nm and 350 nm thick GaN buffer/channel layer each on 250 µm CVD diamond, respectively. Wafer 3 has 750 nm GaN buffer/channel on 150 µm CVD diamond substrate. The 2DEG sheet resistance (R_{sh}) of the wafers 1, 2 and 3 were 352 Ω/sq, 360 Ω/sq and 393 Ω/sq, respectively.

Fabrication began by depositing Ti/Al/Mo/Au (15/60/35/50 nm) metal stack for ohmic contacts, followed by mesa isolation achieved by dry etch using Cl_2/Ar in inductively coupled plasma (ICP) etching tool. Ni/Au (20/300 nm) metal stack for the T- shape gate with length L_G = 100 nm. Bond pads were also deposited using Ti/Au (20/400 nm) metal stack. All device features were defined using photolithography except the gates and ohmic contacts which were defined using electron beam lithography (EBL) to ensure precision. The fabricated two finger HEMT RF device structure shown in Figure 6.2 (e) has gate to drain and gate to source spacings of 2 µm and 1 µm respectively with a gate width W_G of 2×50 µm. The fabrication processes are illustrated in Figure 6.2.

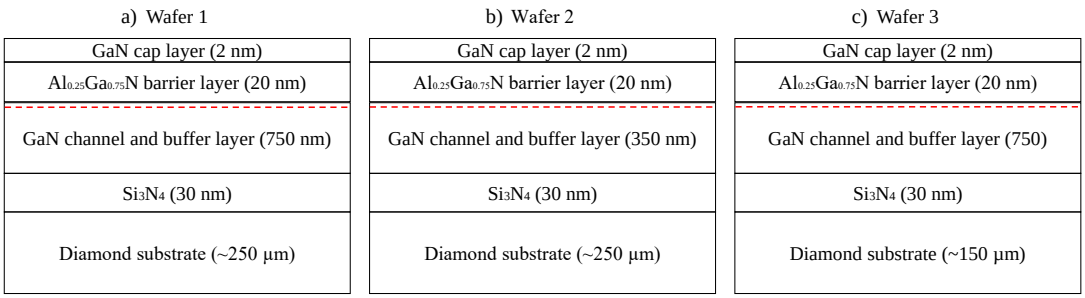


Figure 6.1 Epilayer structures of GaN on diamond with I. a) wafer 1 and b) wafer 2 identical substrate diamond thickness but different channel and buffer layer thickness, II. a) wafer 1 and c) wafer 3 identical channel and buffer layer thickness but different substrate diamond thickness, III. b) wafer 2 and c) wafer 3 different substrate diamond and channel and buffer layer thickness.

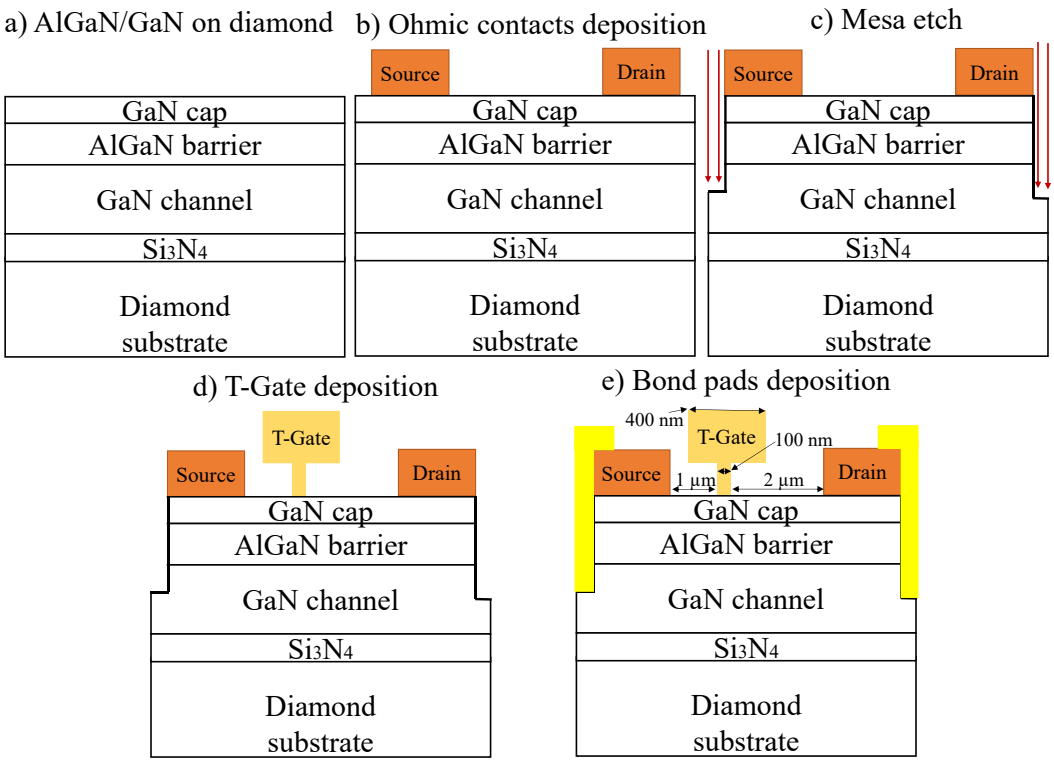


Figure 6.2 Schematic views of the process flow for fabrication flow of AlGaN/GaN HEMT on CVD diamond using two finger T-gate technology. (a) Cleaned wafer, (b) Deposition of Ti/Al/Mo/Au metal stack for the ohmic contacts, (c) Photolithography to expose deep mesa-etch pattern, (d) T-gate formation, (e) Bond pads contacts deposition.

6.3 Device Measurements and Characterisation

DC and RF measurements were carried out using Keysight's B1500A Semiconductor Device Analyser and E8361A 10 MHz – 67 GHz VNA network analyser, respectively. The VNA network analyser was integrated with N5260-60003 67 GHz - 110 GHz wave guide module to extend frequency measurement to 110 GHz. A comparable contact resistance of the three wafers of 0.6 Ω.mm was evaluated using transmission line structure (TLM) as shown in Figure 6.3. The output current characteristics were measured by sweeping the gate voltages from -6 V to 0 V at the step of 1 V and drain voltages from 0 V to +60 V. Measuring the drain voltage up to 60 V enables the characterisation of GaN devices for high-power amplifier applications. In high-power PA (power amplifier) designs, GaN devices are expected to deliver significant power output levels while maintaining mm-wave operation, gain, and efficiency at optimal performance. By measuring the devices

at high drain voltages, such as 60 V, their power handling capabilities can be evaluated, ensuring they can provide the required power output levels without compromising performance.

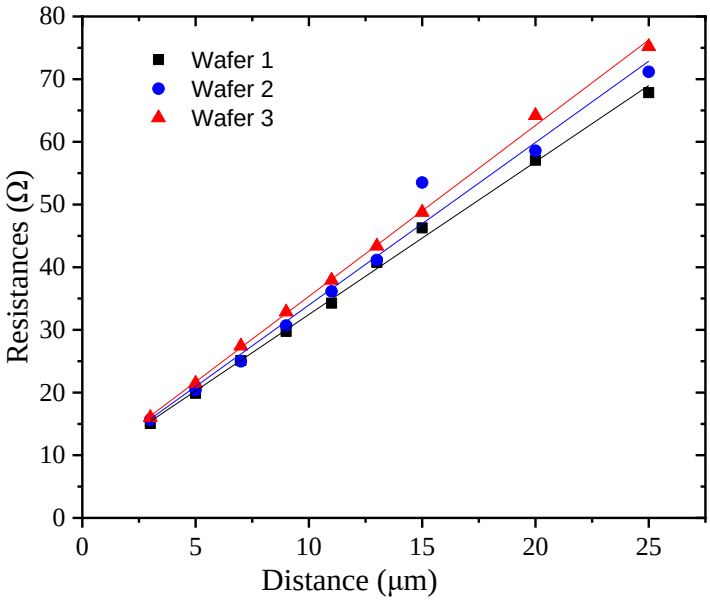


Figure 6.3 Comparison of the TLM measurement results for wafer 1, wafer 2, and wafer3.

6.4 Results and Discussion

6.4.1 Effect of GaN Buffer/Channel Thickness:

This section demonstrates analyses a comparison between the DC and RF results of two AlGaN/GaN HEMTs on identical CVD diamond wafers differing in the thickness of their buffer-channel layers. The main purpose of this comparison is to investigate the impact of the buffer-channel layer thickness on heat extraction and self-heating effects while subjected to high operating bias of up to 60 V. In Section 3.5.2 in Chapter 3, Figure 6.7 and Figure 6.11 presents the cut-off frequencies of the devices, which were measured at the drain voltage corresponding to the maximum output current (V_{DS} = 20 V for all devices). Additionally, the gate bias used for these measurements was set to the value that yielded the maximum transconductance (-2.5 V for all devices). The purpose of these measurements and the resulting plot in Figure 6.7 and Figure 6.11 is to

assess the cut-off frequencies of the devices under specific operating conditions. The cut-off frequency is a critical parameter that determines the device's high-frequency performance and bandwidth. By measuring the devices at the drain voltage associated with the maximum output current and the gate bias resulting in the maximum transconductance, the characterisation provides insights into the devices' high-frequency response under optimal operating conditions. This information helps evaluate the devices' suitability for high-frequency applications and aids in determining their potential performance limitations.

6.4.1.1 DC Performance

The measured output, transfer characteristics, and leakage current of the fabricated devices are shown in the Figure 6.4, Figure 6.5, and Figure 6.6 respectively. As seen in Figure 6.4, the 100 nm T-shape gate HEMT shows a maximum drain current saturation of 591 mA/mm, 525 mA/mm obtained under DC biases of 60 V and V_{GS} of 0 V for wafers 1, 2 respectively. The drain current drops from the knee voltage to the maximum drain bias by 0.4%, 0.13% for wafers 1, 2 respectively. This indicates efficient removal of heat channel and lesser influence of the TBR in the heat transport to the diamond substrate. However, at V_{DS} = 30 V, the I_{DS} drop for the two wafers is 9.6%, 7.6%, indicating the presence of self-heating at higher voltages which is lesser in Wafer 2 with thinner buffer layer of 350 µm due to the closer proximity of the buffer to the diamond substrate than in wafers 1.

The lower drain current in wafer 2 could be attributed to the higher threading dislocations due to lower thickness of the GaN buffer [140]. The cause of the self-heating at higher voltages can be linked to the presence of Si_3N_4 interlayer in the wafers which can significantly affect an efficient heat transport from the AlGaN/GaN channel to the substrate due to the existence of thermal barrier resistance caused by the film mismatch and surface roughness [132]. As the bias voltages go higher and higher, more heat is generated due to increasing power dissipation and the increasing influence of TBR results in the rising temperature around the junction affecting the devices' performance. Although the TBR for GaN on diamond is far lower than in GaN on silicon carbide or silicon [141], a

proper optimisation of the Si_3N_4 film can further improve in the thermal performance of the devices. A reduction in the mismatch and surface roughness was reported to be achieved with a suitable selection of the thickness of Si_3N_4 film [141, 142].

In Figure 6.5, the transconductance values are depicted as 217 mS/mm for wafer 1 and 181 mS/mm for Wafer 2. Notably, wafer 2 exhibits a lower transconductance, likely attributed to a prevalence of high threading dislocations within the thin buffer layer, potentially leading to a degradation of device characteristics. Moving on to Figure 6.6, the measured gate leakage currents at V_{GS} = -10 V, are presented as 4.41 µA/mm for wafer 1 and 193.33 µA/mm for wafer 2. Evidently, wafer 2 displays a higher leakage current, which can similarly be ascribed to the increased presence of threading dislocations within the thin buffer layer.

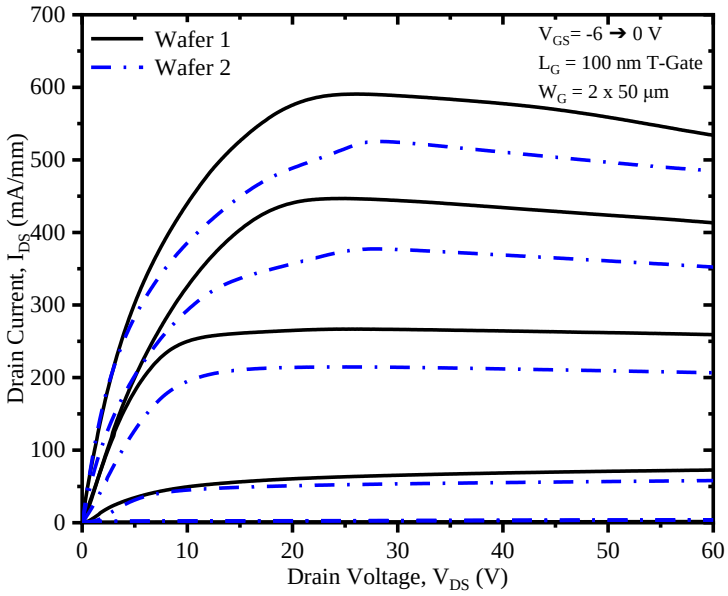


Figure 6.4 I_{DS}-V_{DS} characteristics of 2 x 50 µm wide devices at V_{GS} = 0 V to – 6 V and V_{DS} up to 60 V of AlGaN/GaN HEMT on CVD diamond.

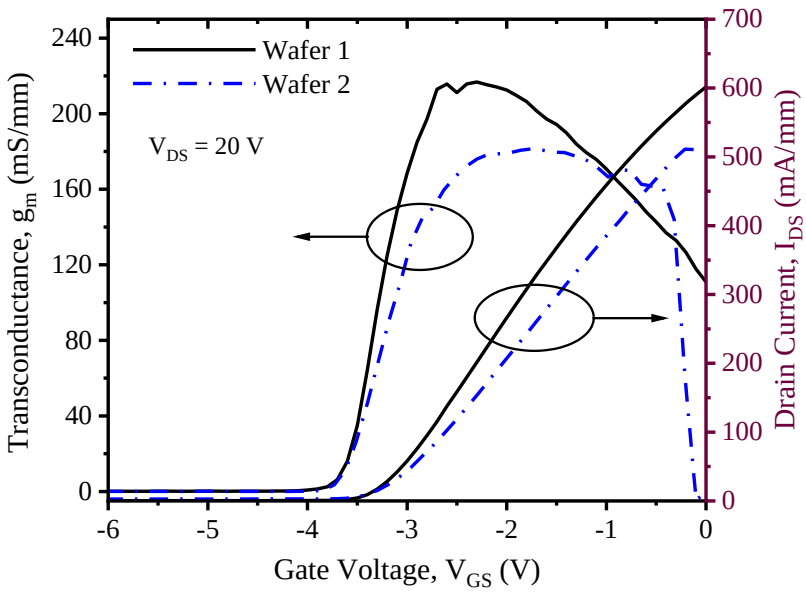


Figure 6.5 Measured transfer characteristics at a drain-to-source voltage, V_{DS} = 20 V.

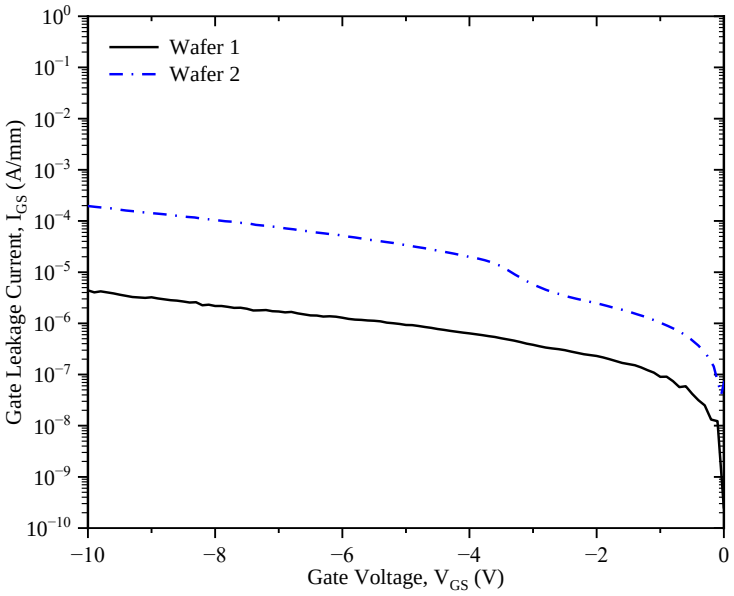


Figure 6.6 Gate leakage current for Wafer 1 and Wafer 2 at V_{DS} = 0 V.

6.4.1.2 RF Performance

The cut-off frequencies obtained for Wafers 1, 2 are as shown in Figure 6.7. Wafer 1 demonstrated impressive power density, reaching up to 32.04 W/mm at V_{GS} = 0 V and V_{DS} = 60 V (3.24 W/mm V_{GS} = 0 V and V_{DS} = 20 V, the points of biasing from which the RF measurements were obtained). Additionally, a high cut-off and maximum frequencies of 90 GHz and 128 GHz, respectively were obtained. These

results indicate the high-performance characteristics of the devices fabricated on wafer 1, showcasing their potential for applications requiring high RF-power and high-frequency capabilities.

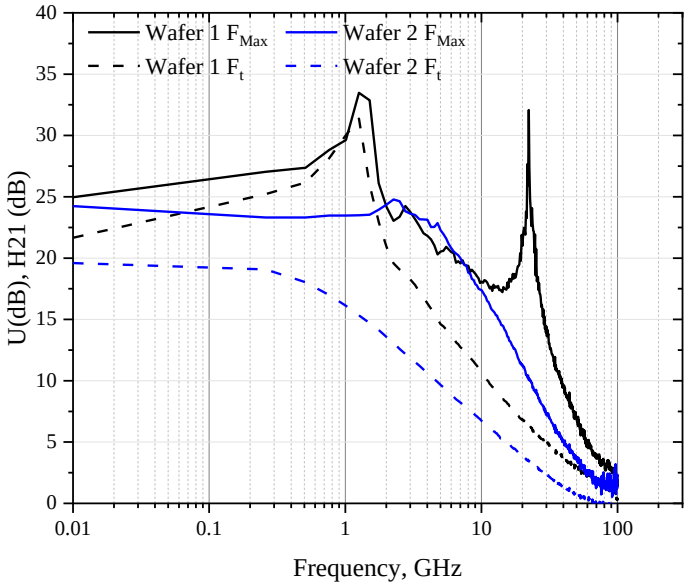


Figure 6.7 Measured H_{21} and Maximum signal gain for 2 x 50 µm device sizes for wafer 1 and wafer 2.

6.4.2 Effect of The Thickness of CVD Diamond Substrate

Similarly in this section, a comparison of the DC and RF results of two identical AlGaN/GaN HEMTs on varied thickness of CVD diamond substrates. The primary objective here is to assess the device performance with varying thickness of the channel/buffer layer on the diamond substrate on DC and RF performances.

6.4.2.1 DC Performance

Based on the experimental results obtained, wafer1 with thicker substrate layer was found to exhibit better DC characteristics. The measured results obtained from the 100nm T-shape gate HEMT fabricated for wafer 1 and wafer 3 is shown in Figure 6.8 presenting a maximum drain current saturation of 591 mA/mm and 518 mA/mm obtained under a high DC bias of 60 V and V_{GS} of 0 V for wafers 1, and 3 respectively. The drain current drops from the knee voltage to the maximum

drain bias by 0.4% and 0.33% for wafers 1 and 3 respectively. As the bias voltage increases from V_{DS} = 30 V to 60V, the I_{DS} drop in wafer 1 remains higher than wafer 3 with 9.6% and 9.1% respectively. Although the difference is not much, however, it is an indication that effective heat dissipation property is more on the wafer with thinner substrate. That may be associated with Lower drain current in the wafer with the thinner substrate. The threshold voltages of -3.7 V and -3.18 V were also obtained from wafer1 and wafer3 respectively.

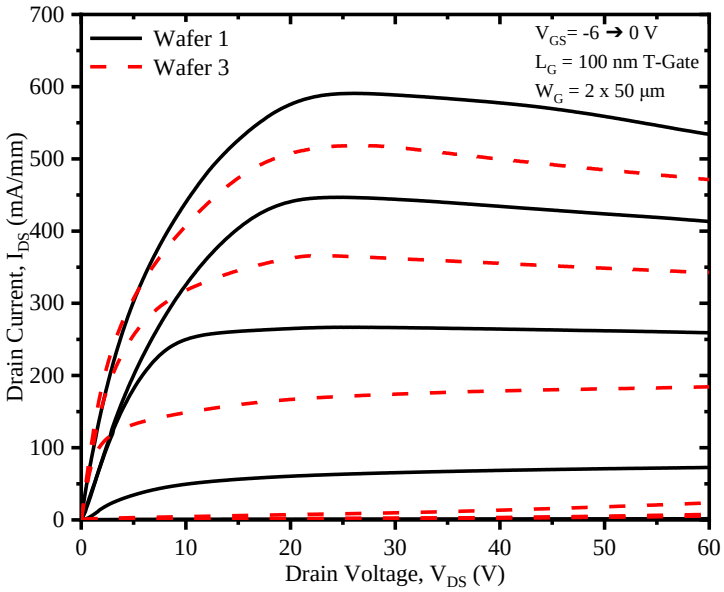


Figure 6.8 I_{DS}-V_{DS} characteristics of 2 x 50 µm wide devices at V_{GS} = 0 V to -6V and V_{DS} up to 60 V of AlGaN/GaN HEMT on CVD diamond.

Figure 6.9 and Figure 6.10 are the results obtained**Error! Reference source not found.** for the leakages and transconductances respectively, for wafers 1 and 3. The transconductance for wafer 1 and wafer 3 were 217 mS/mm 199 mS/mm respectively. Higer transconductance in wafer1 could be linked to its higher drain current. Low leakage current of 4.41 µA/mm was obtained from wafer 1, 10 times lower than the leakage current of 411.31 µA/mm from wafer 3 at V_{GS} = - 10 V.

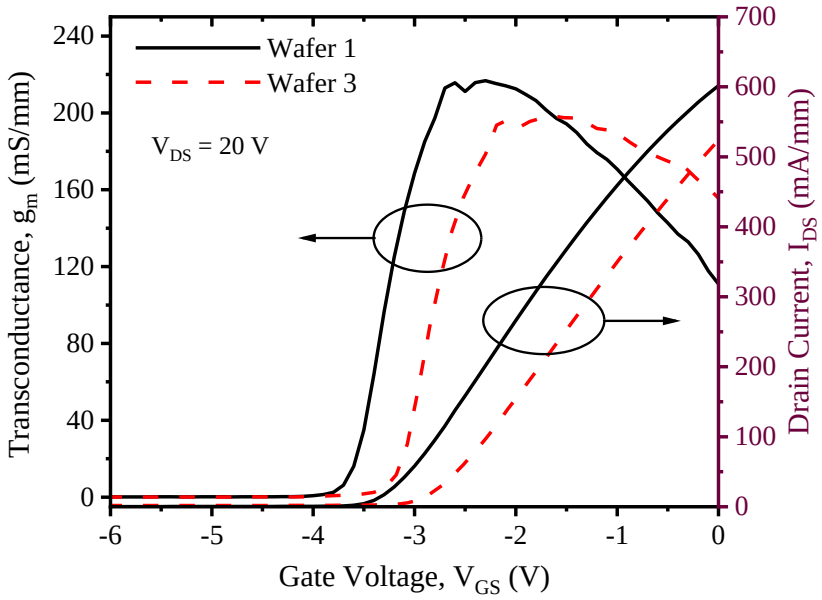


Figure 6.9 Measured transfer characteristics at a drain-to-source voltage, V_{DS} = 20 V.

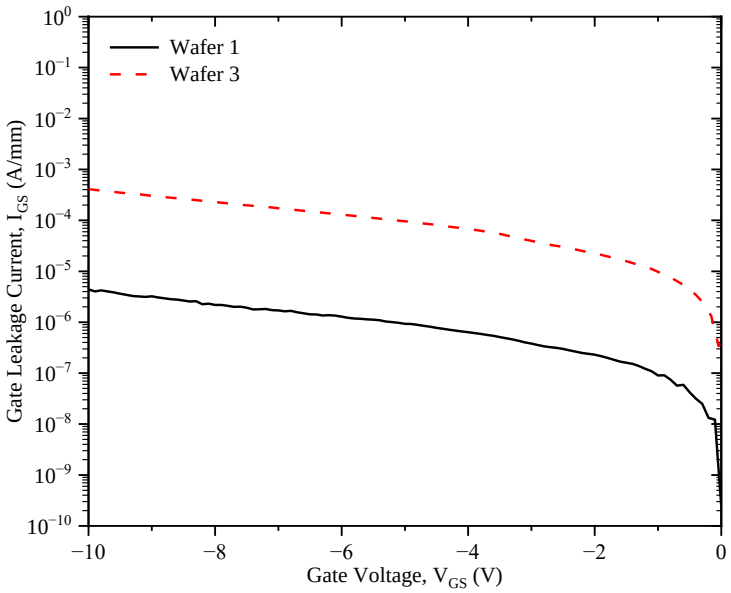


Figure 6.10 Gate leakage current for wafer 1 and wafer 3 at V_{DS} = 0 V.

6.4.2.2 RF Performance

The cut-off frequencies obtained for Wafers 1 and 3 are as shown in Figure 6.11. Higher cut-off and maximum frequencies of 90Ghz and 128GHz respectively were obtained from wafer 1. Similarly, the fmax and ft for wafer 3 were 46GHz and 119GHz as shown in the figure. The DC and RF results from the experimental measurements are summarised in Table 6.1.

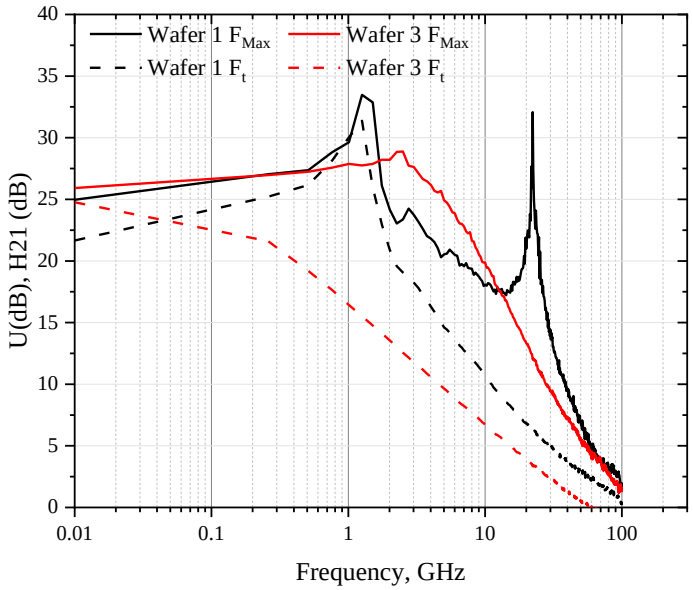


Figure 6.11 Measured H_{21} and Maximum signal gain for 2x50µm device sizes.

Table 6.1 A complete comparison for all the three wafers, including DC and RF measurement results. Extrapolated f_t and f_{Max} values from H_{21} and unilateral gain (U) measurements, respectively. Bond pad parasitic were de-embedded. Extrapolated contact resistance (R_c) and sheet resistance (R_{sh}) from TLM.

Parameters/wafers	Wafer 1	Wafer 2	Wafer 3
I_{DS_max} [mA/mm]	591	525	518
Reduction of I_{DS} @ V_{DS} = 30V (%)	0.4	0.13	0.33
Reduction of I_{DS} @ V_{DS} = 60V (%)	9.6	7.6	9.1
V_{th} (V) @ I_{DS} = 1 mA/mm	- 3.70	- 3.73	- 3.18
g_m [mS/mm]	217	181	199
f_{max} [GHz]	128	115	119
f_t [GHz]	90	44	46
R_c [Ω.mm]	0.61	0.60	0.60
R_{sh} [Ω/Sq]	352	360	393
Gate leakage current [µA/mm] @ V_{GS} = -10 V	4.41	193.33	411.31

6.5 Summary

Efficient heat extraction technology is essential to achieve optimal performance in GaN devices intended for high-power, high-frequency applications. The findings detailed in this chapter illustrate the potential of GaN/diamond structures to fulfil these application demands. They demonstrate effective dissipation of heat from GaN/CVD-diamond devices, with the outcome significantly influenced by the thickness of the GaN buffer. This factor necessitates optimisation efforts to determine the ideal values for specific applications. While self-heating becomes more pronounced at elevated drain-source voltages, careful optimisation of the buffer thickness and substrate selection proves instrumental in mitigating this effect.

In the context of this study, we observed noteworthy reductions of 9.6%, 9.1%, and 7.6% across three distinct wafers incorporating AlGaN/GaN HEMTs on CVD-diamond substrates. These wafers were subject to variations in buffer and substrate thickness and were subjected to testing under specific biasing conditions where VDS was maintained at 60 V and VGS at 0 V. These outcomes hold considerable promise, particularly when juxtaposed against findings from previously published research. To illustrate, when compared to AlGaN/GaN HEMTs on sapphire which exhibited an 18.8% reduction only under the biasing condition of VDS = 20 V [143], we also identified a reduction of 33% for AlGaN/GaN HEMTs on silicon only under the condition of VDS = 20 V [144]. Similarly, an estimated 28% reduction was observed for AlGaN/GaN HEMTs on SiC when biased up to VDS = 60 V [145]. Additionally, we documented a reduction of 17.7% for AlGaN/GaN HEMTs on CVD-diamond at a VDS value of 55 V [144]. These findings underscore the potential advantages inherent in the utilization of GaN/diamond structures for the purpose of augmenting thermal performance in applications characterized by elevated power levels and high frequencies.

Chapter 7

Conclusions and Future Work

A comprehensive review has been conducted to identify the major shortcomings of gallium nitride (GaN) material and recognise its significant role in high-power and high-frequency applications. Based on these findings as illustrated in Table 7.1, our key contributions and achievements in improving the power and frequency performance of GaN High Electron Mobility Transistors (HEMTs) are outlined in the following sections.

7.1 Fabrication of T-gate

To achieve high-frequency performance in GaN HEMTs, compact device size is crucial. Reducing the gate length to sub-100 nm is necessary, but it results in high gate resistance, which impacts the maximum cut-off frequency of the device. To address this challenge, a T-shaped gate structure is commonly used to reduce the gate resistance. However, the mechanical instability of sub-100 nm T-gates necessitates the use of a dielectric material for mechanical support. Unfortunately, the dielectric layer introduces unwanted parasitic capacitances that affect device performance. Our project introduces a new technique for fabricating a robust and stable T-shaped gate structure at sub-100 nm dimensions

without the need for a supportive dielectric, overcoming the limitations of conventional approaches.

7.2 Heavily Doped GaN Cap Layer

In this work, RF and gate wrap-around devices were fabricated on an AlN/GaN-on-sapphire substrate to demonstrate a novel technique for achieving low ohmic contact resistance using a heavily doped GaN cap layer without the need for regrowth. By depositing a Ti/Al/Ni/Au stack on the heavily doped cap layer, we achieved a remarkably low ohmic contact resistance of 0.132 Ω-mm. RF devices utilising this ohmic contact exhibited excellent cut-off and maximum frequencies (f_t and f_{max}) of 73 GHz and 78 GHz, respectively.

7.3 AlGaN/GaN on CVD Diamond HEMT

Efficient heat extraction is crucial for the frequency performance of RF GaN HEMT devices. Conventional substrates used for GaN devices have low thermal conductivity, leading to inadequate heat dissipation and degradation of DC and RF performance. In this project, we demonstrated the efficient heat extraction capabilities of GaN on diamond substrates. By employing GaN on CVD diamond substrates, we achieved a high-power density of up to 32.04 W/mm at V_{GS} = 0 V, V_{DS} = 60 V and remarkable cut-off and maximum frequencies of 90 GHz and 128 GHz respectively, showcasing the potential for enhanced device performance.

Through these advancements in T-gate fabrication, heavily n-doped GaN cap layers, and the use of GaN on CVD diamond substrates, our work significantly contributes to improving the power and frequency performance of GaN HEMTs. These achievements offer promising prospects for the deployment of GaN devices in various high-power and high-frequency applications, paving the way for enhanced performance and functionality in the field of advanced electronics.

Table 7.1 Comparison of this PhD works with the State Of the Art of GaN/HEMTs in high frequency.

L_g [nm]	R_C [Ω.mm]	I_{Dmax} [A/mm]	Gm [S/mm]	f_t [GHz]	f_{MAX} [GHz]	Ref	year
100	0.61	591	0.217	91	128	This work AlGaN/GaN on CVD diamond	2023
100	0.13	988	0.193	73	78	This work AlN/GaN on Sapphire	2023
50	0.1	1.65	0.553	170	347	[82]	2023
50	0.43	1.6	0.415	125	270	[83]	2021
100	0.16	1.85	0.525	88	204	[26]	2020
40	0.13	2.3	0.6	161	70	[84]	2019
110	0.45	1.2	0.4	63	300	[32]	2019
90	0.25	1.2	0.461	98	322	[73]	2018
40	-	1.5	-	140	280	[85]	2017
60	-	1.65	0.65	183	191	[86]	2017
90	0.32	1.25	0.33	113	160	[33]	2017
20	-	3	1.36	454	444	[24]	2015
27	0.1	2	1.0	302	301	[87]	2013
40	0.27	1.8	0.77	230	300	[88]	2013
80	0.09	1.7	-	148	351	[89]	2012
20	0.101	4	1.0	342	518	[23]	2012
60	0.025	2.77	1.105	260	20	[75]	2012

7.4 Future work

7.4.1 Improving Cut-off frequencies in AlN/GaN HEMT with Heavily n-Doped GaN Cap Layer

To enhance the power and frequency performance of AlN/GaN HEMTs with heavily doped GaN capped layer, scaling down the devices to a 50 nm gate length could

be implemented. The barrier is capable of withstanding the shorter gate length, allowing for improved performance. This reduction in gate length helps increase the cut-off frequency and maximum frequency, enabling higher frequency operation. Additionally, reducing the gap size between the source and drain regions (also known as channel length) could be employed to further enhance the operation frequency due to the reduced transit time for charge carriers across the channel.

By implementing these strategies of scaling down the gate length for the heavily doped cap layer and reducing the gap size between source and drain, the power and frequency performances of GaN HEMTs can be significantly enhanced. These advancements contribute to the realisation of higher-speed and higher-frequency devices, enabling their application in various high-performance electronic systems and communication technologies.

7.4.2 Improving Device Performance in AlGaN/GaN HEMT on CVD Diamond

Devices on all three wafers of AlGaN/GaN HEMTs on CVD diamond showed a high knee voltage, primarily due to the high contact resistance and surface traps. To mitigate this issue, several potential solutions could be explored:

1- Passivate the devices using 100 nm Si_3N_4 to reduce the strain relaxation, reduce gate leakage currents and improve Ohmic contacts resistances [146].
2- Etching a portion of the contact pads down to the channel layer in horizontal lines: This approach involves selectively etching the contact pads to reduce the contact resistance [72, 147, 148]. By creating vertical gaps in the contact pads, the resistance can be lowered, leading to improved device performance. This method is relatively cost-effective and does not require regrowth.

3- Growing new wafers with a heavily doped GaN cap layer: Another option is to fabricate new wafers with a heavily doped GaN cap layer. This highly

doped layer helps to reduce the contact resistance and enhances device characteristics as discussed in Chapter 5. By integrating this layer into the fabrication process, the performance of the HEMTs can be improved. This method is cost-effective and can be applied during the wafer growth stage.

4- Combination of etching and growing: Alternatively, a combination of the aforementioned approaches can be employed. It could involve growing a heavily doped GaN cap layer, followed by partial etching of the contact pads. This combined approach further reduces the contact resistance and optimises device performance.

It is important to consider that fully etching the ohmic contact regions and regrowing them with a heavily doped GaN cap layer is another potential method to address the high contact resistance issue. However, it is worth noting that this approach tends to be more expensive compared to the previously mentioned options. The cost is associated with the additional steps involved in the complete etching and regrowth process. Therefore, the decision to pursue this method should take into account the cost-effectiveness and the specific requirements of the application.

The choice of which approach to pursue depends on factors such as cost-effectiveness, feasibility, and the specific requirements of the application. Each method has its advantages and considerations, and careful evaluation is necessary to determine the most suitable solution for improving the performance of AlGaN/GaN HEMTs on CVD diamond wafers.

Appendix A

GaN HEMT Fabrication Processes using Photolithography

- *Sample cleaning*
  - Five minutes in acetone using ultrasonic bath.
  - Five minutes in Isopropyl Alcohol (IPA) using ultrasonic bath.
  - Blow dry using N_2.

- *Ohmic contact deposition*
  - Spin LOR 10 A at 6000 rpm for 30 seconds.
  - Soft bake at 150 ºC for two minutes using hotplate.
  - Spin S1818 at 4000 rpm for 30 seconds.
  - Soft bake at 115ºC for three minutes using hotplate.
  - Expose using MA6 mask aligner, for 6 seconds using hard contact.
  - Develop the exposed area in MF319 developer for 2.30 minutes.
  - Rinse in reverse osmosis (RO) water for 60 seconds.
  - Blow dry with N_2.
  - O_2 ash at 110 W for 2 minute using Plasma Ash.
  - Metallise using Plassys evaporation with metal stack: Ti/Al/Ni/Au 30/180/40/100 nm.
  - Lift-off using 1165 resist stripper in the hot water bath for 2 hours, pipette clean.
  - Rinse with water.
  - Blow dry with N_2.
  - Anneal using RTA at 800 °C in N2 environment for 30 seconds.

- *Mesa isolation*
  - Spin S1818 at 4000rpm for 30 seconds.
  - Bake at 115ºC for 3 minutes.
  - Expose in the MA6 using hard contact for 6 seconds.
  - Develop using MF319 for 2.30 minutes.
  - Rinse with RO water for 60 seconds.
  - Blow dry with N2.
  - Use ICP180 with Cl/Ar 30/15 RF/ICP 75 W/750 W, 4 mTorr for 50 seconds etch.
  - Remove remaining resist using 1165 stripper.
  - Dip in RO water.
  - Blow dry with N_2.

- *Gate recess*
  - Spin S1805 at 4000 rpm for 30 seconds.
  - Soft bake at 115 ºC for 3 minutes.
  - Expose using MA6 tool for 2.3 seconds, hard contact.
  - Use RIE 80+ with SF_6/O_2 20/20 sccm, 70 W power, and 50 mTorr etch for 120 seconds.
  - Remove resist in warm acetone for 2 hours, pipette clean.
  - Dip in IPA.
  - Blow dry with N_2.

- *Gate contact deposition*
  - Spin LOR 3 A at 4000 rpm for 30 seconds.
  - Soft bake at 150 ºC for two minutes using hotplate.
  - Spin S1805 at 4000 rpm for 30 seconds.
  - Soft bake at 115ºC for three minutes using hotplate.
  - Expose using MA6 mask aligner, for 2.3 seconds using hard contact.
  - Develop the exposed area in MF319 developer for 2.30 minutes.
  - Rinse in reverse osmosis (RO) water for 60 seconds.
  - Blow dry with N_2.
  - O_2 ash at 110 W for 1 minute using Plasma Ash.

- Metallise using Plassys evaporation with metal stack: Ni/Au 20/400 nm.
- Lift-off using 1165 resist stripper in the hot water bath for 2 hours, pipette clean.
- Rinse with water.
- Blow dry with N_2.

➢ *Bond pad deposition*

- Spin LOR 10 A at 6000 rpm for 30 seconds.
- Soft bake at 150 ºC for two minutes using hotplate.
- Spin S1818 at 4000 rpm for 30 seconds.
- Soft bake at 115ºC for three minutes using hotplate.
- Expose using MA6 mask aligner, for 6 seconds using hard contact.
- Develop the exposed area in MF319 developer for 2.30 minutes.
- Rinse in reverse osmosis (RO) water for 60 seconds.
- Blow dry with N_2.
- O_2 ash at 110 W for 2 minute using Plasma Ash.
- Metallise using Plassys evaporation with metal stack: Ti/ Au 20/400 nm.
- Lift-off using 1165 resist stripper in the hot water bath for 2 hours, pipette clean.
- Rinse with water.
- Blow dry with N_2.

➢ *Ohmic contact pads opening (Si3N4 etching)*

- Spin S1805 at 4000 rpm for 30 seconds.
- Soft bake at 115 ºC for 3 minutes.
- Expose using MA6 tool for 2.3 seconds, hard contact.
- Use RIE 80+ with CHF_3/Ar 25/25 sccm, 100 W power, and 30 mTorr etch for 60 seconds.
- Remove resist in warm acetone for 2 hours, pipette clean.
- Dip in IPA.
- Blow dry with N_2.

- *Ohmic contact pads opening (SiO2 etching)*
  - Spin S1805 at 4000 rpm for 30 seconds.
  - Soft bake at 115 ºC for 3 minutes.
  - Expose using MA6 tool for 2.3 seconds, hard contact.
  - Use RIE 80+ with CHF_3/Ar 25/25 sccm, 50 W power, and 30 mTorr etch for 60 seconds.
  - Remove resist in warm acetone for 2 hours, pipette clean.
  - Dip in IPA.
  - Blow dry with N_2.

- *Ohmic contact pads opening (HfO2 etching)*
  - Spin S1805 at 4000 rpm for 30 seconds.
  - Soft bake at 115 ºC for 3 minutes.
  - Expose using MA6 tool for 2.3 seconds, hard contact.
  - Use ICP 300 Cobra with ICP/RF (1250/25 W), 3 mTorr, 10 sccm BCl_3, 10 sccm Cl_2, He = 10 Torr for 40 seconds.
  - Remove resist in warm acetone for 2 hours, pipette clean.
  - Dip in IPA.
  - Blow dry with N_2.

- *Ohmic contact pads opening (Al2O3 etching)*
  - Spin S1805 at 4000 rpm for 30 seconds.
  - Soft bake at 115 ºC for 3 minutes.
  - Expose using MA6 tool for 2.3 seconds, hard contact.
  - Use ICP180 with 30 sccm BCl_3, 600 W ICP power, He= 7 Torr, and 80 mTorr etch for 60 seconds.
  - Remove resist in warm acetone for 2 hours, pipette clean.
  - Dip in IPA.
  - Blow dry with N_2.

Fabrication using E-Beam Lithography

- *Sample cleaning*
  - Five minutes in acetone using ultrasonic bath.
  - Five minutes in Isopropyl Alcohol (IPA) using ultrasonic bath.
  - Blow dry using N_2.

- *2) E-beam markers*
  - Spin 15% PMMA at 4000rpm for 60 seconds.
  - Soft bake at 180ºC for 5 minutes.
  - Spin 2% PMMA at 4000 rpm for 60 seconds.
  - Soft bake at 180ºC for 5 minutes.
  - Expose using EBPG with dose of 900, with current 32 nA, resolution of 25.
  - Develop in IPA:MIBK 2.5:1 for 45 seconds at 23 °C.
  - Dip in IPA for 30 seconds.
  - Blow dry with N_2.
  - Metallise Ti/Pl 20/100 nm.
  - Lift-off in warm acetone for 2 hours, pipette clean.
  - Dip in IPA.
  - Blow dry with N_2.

- *3) Ohmic contact formation*
  - Spin 15% PMMA at 4000rpm for 60 seconds.
  - Soft bake at 180ºC for 5 minutes.
  - Spin 2% PMMA at 4000 rpm for 60 seconds.
  - Soft bake at 180ºC for 5 minutes.
  - Expose using EBPG with dose of 900, with current 32 nA, resolution of 25.
  - Develop in IPA:MIBK 2.5:1 for 45 seconds at 23 °C.
  - Dip in IPA for 30 seconds.
  - Blow dry with N2.
  - Metallise Ti/Al/Ni/Au 30/180/40/100nm.
  - Lift-off in warm acetone for 2 hours, pipette clean.
  - Dip in IPA for 5 minutes.

- Blow dry with N_2.
- Anneal at 800 °C in N_2 environment for 30 seconds.

- *4) Mesa isolation*
  - Spin 15% PMMA at 4000rpm for 60 seconds.
  - Soft bake at 180 ºC for 5 minutes.
  - Expose in EBPG tool with dose of 900, beam current of 64 nA and resolution of 25.
  - Use ICP180 with Cl/Ar 30/15 RF/ICP 75 W/750 W, 4 mTorr for 50 seconds etch.
  - Remove resist in warm acetone for 2 hours, pipette clean.
  - Dip in IPA.
  - Blow dry with N_2.

- *5) Gate recess*
  - Spin 15% PMMA at 4000rpm for 60 seconds.
  - Soft bake at 180 ºC for 5 minutes.
  - Expose in EBPG tool with dose of 900, beam current of 64 nA and resolution of 25.
  - Use RIE 80+ with SF_6/O_2 20/20 sccm, 70 W power, and 50 mTorr etch for 120 seconds.
  - Remove resist in warm acetone for 2 hours, pipette clean.
  - Dip in IPA.
  - Blow dry with N_2.

- *6) T-Gate fabrication*
  - Spin 2% PMMA at 4000rpm for 60 seconds.
  - Soft bake at 180 ºC for 5 minutes.
  - Spin 2% PMMA at 4000rpm for 60 seconds.
  - Soft bake at 180 ºC for 5 minutes.
  - Spin LOR 3 A at 4000 rpm for 30 seconds.
  - Soft bake at 150 ºC for 2 minutes.
  - Spin CSAR at 2000rpm for 60 seconds.
  - Soft bake at 150 ºC for 2 minutes.

- Expose using EBPG tool with dose of 800, beam current of 4 nA, resolution of 4.
- Develop CSAR in amyl-acetate at 23 °C for 30 seconds.
- Dip in IPA for 30 seconds.
- Blow dry with N_2.
- Develop LOR 3A in CD-26 developer for 20 seconds.
- Rinse with RO water for 5 minutes.
- Blow dry with N_2.
- Develop with IPA:MIBK 3:1 for 30 seconds at 23 ºC.
- Dip in IPA for 30 seconds.
- Blow dry with N_2.
- Ash for 1 minute in plasma Asher.
- Metallise Ni/Au 20/300 nm.
- Lift-off in warm acetone for 2 hours, pipette clean.
- Dip in IPA for 5 minutes.

➢ *7) Bond pad metallisation*

- Spin 15% PMMA at 4000rpm for 60 seconds.
- Soft bake at 180 ºC for 5 minutes.
- Spin 2% PMMA at 4000 rpm for 60 seconds.
- Soft bake at 180 ºC for 5 minutes.
- Expose using EBPG with dose of 900, with current 32 nA, resolution of 25.
- Develop in IPA:MIBK 2.5:1 for 45 seconds at 23 °C.
- Dip in IPA for 30 seconds.
- Blow dry with N2.
- Metallise Ti/Au 20/400 nm.
- Lift-off in warm acetone for 2 hours, pipette clean.
- Dip in IPA for 5 minutes.
- Blow dry with N_2.

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