Advanced GaN HEMT Technology for Millimetre-wave Amplifiers

by

Aniket Dhongde

A thesis submitted in fulfilment for the degree of
Doctor of Philosophy

in the

Electronics and Nanoscale Engineering Division of

School of Engineering

The thesis is dedicated to my family and Dr. Babasaheb Ambedkar, who was a remarkable social reformer and the chief architect of the Indian Constitution.

Abstract

Gallium Nitride (GaN)-based High-Electron-Mobility Transistor (HEMT) technology is a breakthrough innovation in the semiconductor industry, offering high-frequency and high-power performance capabilities. GaN HEMTs are widely used in power electronics, wireless communication systems, and radar applications over the past two decades.

The key advantages of GaN HEMTs to produce heterojunctions to larger bandgap materials Aluminium Gallium Nitride (AlGaN) and the heterostructure results in the formation of the 2- dimensional electron gas (2DEG) which exhibits high electron mobilities of upto 2000 $\mathrm{cm}^2/\mathrm{V.s}$ and high saturation velocity of 2×10^7 cm/s, resulting in high switching speeds and power densities. Due to its wide bandgap of 3.4 eV, it also allows exceptionally high breakdown fields of 3.3 MV/cm. In this thesis, the focus is on the major challenges in the development of GaN HEMT technology including achieving a low resistance ohmic contact, reducing self-heating, and improving device high frequency performance.

Due to the wide bandgap of III-nitride semiconductors, achieving low-resistance Ohmic contact resistance is difficult. Recessing the Ohmic region prior to metallization is a typical approach to lowering the contact resistance. The contact resistance is often minimised by optimising factors such as recess depth, anneal temperature, and metal stack design. In this work, the three approaches involving the recessing of the ohmic region were evaluated. The Ohmic contact area was recessed in patterns similar to a chess board, vertical recessed stripes, and horizontal recessed strips. The two different recess etch depths, shallow and deep etch depths of 9 nm and 30 nm, respectively, were investigate. The lowest contact resistance of 0.32 Ω.mm (compared to 0.59 Ω.mm for a conventional non-recessed Ohmic contact) was observed for a deep horizontal patterned structure. The results also indicate that a highly reproducible process.

The other major issue to address was to reduce the impact of device self-heating by effective heat distribution and dissipation. A novel thermal management technique was proposed, and the preliminary results are promising. It exploits the very thin epitaxial layer stack of a buffer-less GaN-on-SiC HEMT structure. III-V nitride material is etched and removed from around the active device area and the Au bond pad electrodes sit directly on the SiC substrate, providing a route for

thermal dissipation from the active device to the substrate. This approach was demonstrated to reduce device self-heating and to improve the current density of the device.

We fabricated and compared the performance of devices fabricated on the buffer-free and conventional GaN HEMTs. For identically sized 2-μm gate long, two-finger 2 × 50 μm gate width device with a gate to drain spacing of 3 μm, the conventional devices broke down at 186 V while for the buffer-free structure, it was over 200 V (above the measurement capability of our equipment). The maximum drain current density of ~631 mA/mm and ~ 686 mA/mm biased at V_{GS} = 1 V for the two-finger 2 × 50 μm gate wide for buffer free and conventional GaN structure, respectively. The buffer free and conventional GaN structure devices were measured to determine their maximum cut-off frequency (f_T) and maximum oscillation frequency (f_{max}) when biased at V_{DS} = 15V. The lower gate leakage currents were observed for the fabricated buffer-free AlGaN/GaN HEMT device as compared to conventional GaN HEMTs 197μA and 260μA, respectively. Also, the buffer free device, which had two fingers each measuring 2x200 μm, yielded measurements of 4.6 GHz for f_T and 9.8 GHz for f_{max}. The conventional GaN device, also with two fingers each measuring 2x200 μm, was tested and resulted in measurements of 6.3 GHz for f_T and 14.7 GHz for fmax. These results demonstrate the high quality of the buffer-free GaN heterostructure despite the absence of thick transition layers as currently used in the conventional GaN HEMTs. This indicates that the "buffer-free" design has the potential to be useful for millimetre wave applications in the future.

This thesis also describes the fabrication and characterisation of a 100 nm footprint Ni/Au-based T-gate HEMT, 2x25 μm gate width, 1.5 μm drain source spacing, 100nm Si_3N_4 passivation layer thickness and device exhibit quite high peak currents of 805mA/mm and peak transconductance value of 246 mS/mm due to the low thermal boundary resistance on this buffer free epilayer wafer. The breakdown voltage was measured 47 Volts. Yielding a cut-off frequency f_T of 87 GHz and maximum oscillation frequency f_{max} of 143 GHz. We have developed a method for fabricating a T-shaped gate for sub 100nm gate foot length. The 100 nm length results in robustness, repeatable and has a high yield. Our findings indicate that this gate design could be beneficial for AlGaN/GaN buffer-free HEMTs used in millimetre wave frequency applications.

Acknowledgements

First of all, I must express my sincere thanks to my supervisor, Dr Edward Wasige, who introduced me to the complex and beautiful world of semiconductors material. Now, I am more in love with semiconductor devices. This work could not have been initiated and completed in a short time without the constant support, encouragement, guidance, and selfless dedication from my supervisor. I am lucky to have you. I feel incredibly pleased and honoured to express my deep gratitude and indebtedness to Dr Chong li, who has helped me comprehensively understand high frequency device optimization and guidance. Thank you so much. The government of Maharashtra, India, funded the research outcome presented in this thesis. I sincerely thank the government of Maharashtra for providing financial support.

I would like to thank the James Watt Nanofabrication Centre (JWNC) staff for maintaining the facility in excellent condition, for instructing and guiding me as I used different fabrication equipment, and for the daily conversation.

Thanks to Dr Maira Elksne and Dr Sanna Taking for all the help in the cleanroom and outside, encouragement, fruitful discussion. Big thanks to Dr Afesomeh Ofiare for his continuous help with discussions, RF measurement system set up and all the help with measurements.

I would like to thank my group mates, office mates, lab mates and friends for encouragement, support, discussions, dinners, hugs and lunchtime fun. Big thanks to my friends Dr. Takshak Shande, Sachin Bahade, Kaivan Karami and Dr. Abdullah Al-Khalidi, for all the encouraging postcards that came from all around the world. Special thanks to Tania, Maira and Swagata for being there for me and of course, for all those sweets and chats.

Personally, this journey would not have been possible without my wife Shikha’s generous love and support. Words are not enough to express it. And the biggest thanks to my little beautiful daughter Xiyana for choosing me to be her father and bringing us all the joy. Finally, I must thank my beloved parents, sister Neha and Samiksha, for their selfless love and motivation.

I am very thankful to every single person who has helped me through this journey.

List of publications

- Dhongde, A. Ofiare, A., Karami, K. and Wasige, E. (2023) Buffer-Free GaN-on-SiC HEMTs with Bond Pad Heat Sinks. UK Semiconductors 2023, Sheffield, UK, 12-13 July 2023.
- Dhongde, A., Taking, S., , Karami, K. , Elksne, M. , Dwidar, M., Al-Khalidi, A. and Wasige, E. (2022) DC and RF Characteristics of Buffer-Free AlGaN/GaN HEMT and MIS-HEMTs Using Si_3N_4 Passivated Mesa-Sidewall. In: International Conference on Electronic and Photonic Integrated Circuits (EPIC- 2022), Andhra Pradesh, India, 15-17 Dec 2022.
- Dhongde, A., Elksne, M. , Karami, K. and Wasige, E. (2022) Comparative Study of AlGaN/GaN HEMTs with and without the Buffer on SiC Substrates. UK Semiconductors 2022, Sheffield, UK, 6-7 July 2022.
- Dhongde, A., Taking, S., Elksne, M. , Ofiare, A., Karami, K. , Dwidar, M., Al-Khalidi, A. and Wasige, E. (2022) High Performance of AlGaN/GaN HEMTs using Buffer-Free GaN on SiC Structure. 45th WOCSDICE - Workshop on Compound Semiconductor Devices and Integrated Circuits, Ponta Delgada (São Miguel island – Azores), Portugal, 3-6 May 2022.
- Dhongde, A., Taking, S., Elksne, M. , Samanta, S. , Ofiare, A., Karami, K. , Al-Khalidi, A. and Wasige, E. (2021) The role of selective pattern etching to improve the Ohmic contact resistance and device performance of AlGaN/GaN HEMTs. *International Journal of Nanoelectronics and Materials*, 14, pp. 21-28.
- Karami, K. , Dhongde, A., Cheng, H., Reynolds, P. M. , Thoms, S. , Reddy, B. A., Ritter, D., Li, C. and Wasige, E. (2022) "Robust sub-100 nm T-gate fabrication process using multi-step development.", MNE EUROSENSORS 2022, Leuven, Belgium, 19-23 September 2022.
- Cheng, H., Dhongde, A., Karami, K. , Reynolds, P. , Thoms, S. , Wasige, E. and Li, C. (2022) Reliable T-gate Process for THz HEMTs. UK Semiconductors 2022, Sheffield, UK, 6-7 July 2022.
- Karami, K. , Taking, S., Ofiare, A., Elksne, M. , Dhongde, A., Al-Khalidi, A. and Wasige, E. (2022) Investigation of Al_2O_3, Si_3N_4 and SiO_2 Used for Surface

Passivation and Gate Dielectric on AlGaN/GaN Metal-Oxide-Semiconductor High Electron Mobility Transistors. WOCSDICE EXMATEC 2022, Ponta Delgada (São Miguel island–Azores), 3-6 May 2022.

- Karami, K. , Hassan, S., Taking, S., Ofiare, A., Dhongde, A., Al-Khalidi, A. and Wasige, E. (2023) Comparative Study of Al_2O_3 and HfO_2 as gate dielectric on AlGaN/GaN MOSHEMTs. *International Journal of Electronics and Communication Engineering*, 17(2), pp. 47-50.
- Ofiare, A., Taking, S., Karami, K. , Dhongde, A., Al-Khalidi, A. and Wasige, E. (2021) Investigation of plasma induced etch damage/changes in AlGaN/GaN HEMTs. *International Journal of Nanoelectronics and Materials*, 14, pp. 29-36.
- Karami, K. , Taking, S., Dhongde, A., Ofiare, A., Al-Khalidi, A. and Wasige, E. (2021) Heavily doped n++ GaN cap layer AlN/GaN metal oxide semiconductor high electron mobility transistor. *International Journal of Nanoelectronics and Materials*, 14, pp. 45-51.
- Karami, K. , Taking, S., Ofiare, A., Dhongde, A., Al-Khalidi, A. and Wasige, E. (2021) High performance of n++GaN/AlN/GaN high electron mobility transistor. 44th Workshop on Compound Semiconductor Devices and Integrated Circuits held in Europe (WOCSDICE), Bristol, UK, 14-17 June 2021.

Table of Contents

Abstract i
Acknowledgements iii
List of publications iv
List of Figures ix
List of Table xv
Definitions xviii
1 Introduction 2
1.1 Overview 2
1.2 GaN Applications 5
1.3 Research challenges 5
1.3.1 Ohmic contacts to AlGaN/GaN HEMTs 5
1.3.2 Self-heating 7
1.3.3 Thermal Boundary Resistance 8
1.4 Research aim 9
1.5 Thesis structure 9
2 GaN HEMT Basic Theory 12
2.1 Introduction 12
2.2 III-Nitride crystal structure 12
2.3 Polarization in III-N semiconductors 13
2.3.1 Spontaneous Polarization 13
2.3.2 Piezoelectric Polarization 14
2.3.3 2-Dimension electron gas (2DEG) formation 15
2.4 GaN HEMT device structure 17
2.4.1 Substrate 17
2.5 GaN-based HEMT epitaxial layer structure 19
2.6 Depletion mode GaN HEMT device: operation principle 20
2.7 Enhancement mode GaN HEMTs 24
2.8 HEMT RF Behaviour 25
2.8.1 Small signal Equivalent Circuit Model 28
2.9 Summary 29
3 GaN HEMT Device Fabrication Techniques 31

3.1 Introduction 31
3.2 Epitaxial material growth 31
3.2.1 Metal Organic Chemical Vapor Deposition 31
3.2.2 Molecular beam epitaxy (MBE) 33
3.3 Lithography 34
3.3.1 Photolithography 34
3.3.2 Electron beam lithography 35
3.3.3 Photoresists 37
3.4 Metallization 38
3.4.1 Electron beam metal evaporation 39
3.5 Annealing 40
3.6 Etching 41
3.6.1 Wet etching 41
3.6.2 Dry etching 41
3.7 Dielectric material deposition 42
3.8 T-gate fabrication 42
3.9 HEMT fabrication process flow 45
3.9.1 Mask plate design 45
3.9.2 Mesa isolation 47
3.9.3 DC and RF devices 49
3.9.4 Gate metallisation 50
3.9.5 Bondpad metallisation 50
3.10 Summary 50
4 Ohmic Contacts in GaN HEMTs 52
4.1 Introduction 52
4.2 Metal-semiconductor Contact 52
4.2.1 Schottky Gate contact 55
4.2.2 Ohmic contact formation 55
4.3 Transmission line model 56
4.3.1 Linear Transmission Line Model (LTLM) 56
4.3.2 Circular Transmission Line Model (CTLM) 58
4.4 Literature review on GaN based Ohmic contacts 59

4.5 Fabrication and evaluation of patterned Ohmic contacts 61
4.5.1 Patterned TLMs and device fabrication. 61
4.5.2 Experimental results and discussion 64
4.6 Conclusion 67
5 Comparative study of buffer thickness in AlGaN/GaN HEMTs on SiC substrates 69
5.1 Introduction 69
5.1.1 Buffer-free GaN heterostructure 71
5.2 Experimental results 72
5.2.1 Device structure and fabrication 72
5.2.2 Result and discussion 74
5.3 Conventional and buffer-free MOCVD-grown GaN HEMTs 80
5.3.1 Device measurement results 81
5.4 Conclusion 84
6 Thermally Efficient GaN HEMT Devices 86
6.1 Introduction 86
6.2 Thermal management of GaN HEMTs 86
6.3 Review of thermal management techniques for GaN HEMTs 89
6.4 Proposed thermally efficient GaN-on-SiC HEMT device 92
6.4.1 Experimental results 94
6.4.2 Mesa-passivated thermally-efficient GaN MIS-HEMTs 99
6.5 Conclusion 106
7 High Frequency GaN HEMT Devices 108
7.1 Introduction 108
7.2 State of the art 108
7.3 GaN HEMT devices with T-gates 114
7.3.1 The importance and fabrication of T-gates 114
7.3.2 RF measurements 119
7.4 Summary 120
8 Conclusions and Future work 122
8.1 Conclusion 122
8.1.1 Ohmic contacts to AlGaN/GaN HEMTs 122
8.1.2 Thermal management on AlGaN/GaN HEMTs 122

8.1.3 T-Gate fabrication 123
8.2 Future work 123
8.2.1 Proposed GaN/diamond-on-SiC 123
8.2.2 Proposed buffer-free AlN/GaN HEMT structure 124
Appendix A 125
References 130

List of Figures

Figure 1.1: A summary of the important properties of Si and GaN. 3
Figure 1.2: Cross section of typical GaN HEMT device 4
Figure 1.3 : Applications of GaN technology. 5
Figure 1.4: Ohmic contacts for AlGaN/GaN HEMTs (a) planar Ohmic contact (b) recess Ohmic contact (c) patterned Ohmic contact (d) regrown Ohmic contact. 6
Figure 1.5: Illustration of the standard AlGaN/GaN HEMT the channel heat source and TBR. 8
Figure 2.1: Hexagonal Wurtzite structure. 13
Figure 2.2: Crystal structure of wurtzite Ga (Al) face GaN b) Ga-face strained AlGaN/GaN heterostructures: Polarization-induced sheet charge and direction of spontaneous and piezoelectric polarisation [57]. 14
Figure 2.3: Illustration of how AlGaN is strained during the formation of 2DEG on GaN. 15
Figure 2.4: AlGaN/GaN energy band diagram illustrating the impacts of PSP and PPE on the conduction band [60]. 16
Figure 2.5: AlxGa1-xN/GaN heterostructure's band structure demonstrating 2DEG development at the heterojunction as a result of quantum well formation [60]. 16
Figure 2.6: Cross section of HEMT device structure. 17
Figure 2.7: Illustration of a HEMT operation principle and biasing (a) ON-state and (b) OFF-state with an AlGaN/GaN heterostructure and Si_3N_4 passivation. 21
Figure 2.8: Gate voltage effects on the energy band structure: a) $V_{GS} > V_{TH}$ and b) $V_{GS} < V_{TH}$. 22
Figure 2.9: Output DC- IV characteristic of a typical GaN HEMT. 23

Figure 2.10 Illustration of the three types of e-mode GaN HEMTs a) with p doped layer under the gate, b) deep recessed gate with insulator under the gate and c) fluoride treated region under the gate [76]. 24

Figure 2.11: Diagram of the two-port idea for device characterisation. 25

Figure 2.12: Micrograph of a fabricated GaN HEMT with landed RF ground-signal-ground probes on device RF ports. 26

Figure 2.13: Small-signal equivalent circuit model of HEMT. 28

Figure 3.1: Schematic illustrations (a) MOCVD growth chamber (b) In the hot-wall MOCVD growth chamber setup, the substrate is placed in the hot zone. Before entering the growth chamber, all precursors (TMAl/TMGa+NH3) and carrier gases (H2/N2) are mixed together 32

Figure 3.2: Schematic illustration of an MBE growth chamber. 34

Figure 3.3: Photo of the Karl Suss Mask Aligner (MA6). 35

Figure 3.4: Photo of the electron beam lithography tool Raith EBPG5200 HS. 36

Figure 3.5: Schematic illustration of the column of an electron beam lithography tool. 36

Figure 3.6: Positive photoresist spinning, exposure and development. 37

Figure 3.7: The metal lift-off process flow using (a) a single layer photoresist (b) a bi-layer od photoresist (c) a tri-layer of photoresist. 38

Figure 3.8: Image of the Plassys IV metal evaporation tool. 40

Figure 3.9: Photo of the Jipelec JetFirst 200 rapid thermal annealing (RTA) machine. 41

Figure 3.10: Schematic of the process flow for the fabrication of T shape gate using tri-layer (a) and (b) exposed gate region. 44

Figure 3.11: The measured beam spread effect by forward scattering in the top CSAR (a) and PMMA-950K (b) at 100 keV. The layer structure is 120 and 250 nm thick PMMA and CSAR, respectively. 45

Figure 3.12: SEM images of the developed three-layer photoresist profile of the T gate (a), the T-gate, image after metallization on SiC (b) and T-gate in between source and drain on SiC substrate (c). 45

Figure 3.13: Schematic views of the process flow for to substrate fabrication in AlGaN/GaN HEMT device processing steps (a)Clean wafer; markers (b) Photolithography and deep mesa-etch pattern using BCl_3/Cl_2 plasma (c) Deposition of Ti/Al/Ni/Au metal stack Ohmic contacts (d) Ni/Au based gate metallization (e) Bond pads contacts (f) Device passivation using 100nm Si_3N_4. 46

Figure 3.14: Screenshot of layout of a design in L-edit. 47

Figure 3.15: Layout design of a DC device. 49

Figure 3.16: Layout of fabricated design of a RF device. 49

Figure 4.1: Energy band diagram for a metal (n-type) semiconductor contact in thermal equilibrium. 53

Figure 4.2: The three types of carrier transport mechanism at metal and semiconductor, a) thermionic emission, b) Field emission and c) Thermionic field emission [101]. 54

Figure 4.3: IV characteristics for a Schottky gate contact 55

Figure 4.4: IV characteristics for a Ohmic contact. 55

Figure 4.5: (a) A semiconductor material with Ohmic contact pads for LTLM characterization (b) LTLM on after annealed. 57

Figure 4.6: An illustration of a plot of total resistance measurements versus various gap spacing. 58

Figure 4.7: Current flow in LTLM structures (a) non-isolated and (b) isolated. 58

Figure 4.8: Illustration of Reeves concentric circular contacts. 59

Figure 4.9: Top-view illustrations of the patterned surface of Ohmic contact using (a) conventional or planar (b) chess pattern etch (c) vertical pattern etch, and (d) horizontal pattern etch of AlGaN/GaN HEMT structures. 62

Figure 4.10: The cross-section schematic illustration of the fabricated AlGaN/GaN HEMT structures with (a) shallow (~ 9 nm of etch depth) (b) deep (~ 30 nm of etch depth) Ohmic recess etching. 62

Figure 4.11: The single etches chess pattern area 63

Figure 4.12: Measured contact resistances, R_C, of (a) shallow and (b) deep Ohmic recess etching on 4 different TLM pattern structures. 65

Figure 4.13. The cross-section schematic illustration of (a) shallow patterned etching (b) deep patterned etching (c) conventional or planar structure of Ohmic metal contact to AlGaN/GaN HEMT structures. 65

Figure 4.14: The measured output characteristics of the fabricated AlGaN/GaN HEMTs with a (a) shallow (b) deep patterned etching of 4 different TLM structure. 66

Figure 4.15. The measured transconductance of the fabricated AlGaN/GaN HEMTs with (a) shallow Ohmic recess etching (b) deep Ohmic recess etching with 4 different TLM pattern structures. 66

Figure 4.16: The gate leakage current characteristics of the fabricated AlGaN/GaN HEMTs with a (a) shallow Ohmic recess etching (b) deep Ohmic recess etching with 4 different TLM pattern structures. 67

Figure 5.1: A conventional AlGaN/GaN heterostructure with a significant C or Fe doping in the buffer layer. 71

Figure 5.2: A buffer-less AlGaN/GaN heterostructure. 72

Figure 5.3: Epitaxial wafer structure of fabricated AlGaN/GaN heterostructure devices using (a) a thick GaN layer and (b) a buffer-free (c) Micrograph of fabricated 200µm wide device. 74

Figure 5.4: Measured contact resistance versus gap spacing of thick GaN buffer and buffer-free GaN wafers. 75

Figure 5.5: The I_{DS}-V_{DS} characteristics for 50 and 200 µm wide devices on buffer-free GaN wafer. 75

Figure 5.6: The I_{DS}-V_{DS} characteristics for 50 and 200 µm wide devices on thick- GaN buffer wafer. 76

Figure 5.7: The I_{DS}-V_{DS} characteristics of 2 x 50 µm wide devices at V_{GS} = 0V to -5V and V_{DS} up to 40V on buffer free wafer and thick GaN buffer wafer. 76

Figure 5.8: Measured transfer characteristics of (a) buffer-free (b) thick GaN buffer devices biased at V_{DS} = 5 V. 77

Figure 5.9: Measured gate leakage currents of (a) buffer-free (b) thick GaN buffer devices with a 2-µm gate long, two-finger 2 x 50 µm wide biased at V_{DS} = 0 V 78

Figure 5.10: Measured off-state breakdown voltage of (a) buffer-free (b) thick GaN buffer devices with a 2- µm gate long, two-finger 2 x 50 µm wide biased at V_{GS} = -10 V 78

Figure 5.11: Measured H21 and Maximum signal gain for 2x200µm device sizes for buffer and buffer free devices. 79

Figure 5.12: Standard GaN-on-SiC epitaxial layer wafer structures for comparison in terms of the device thermal performance. 80

Figure 5.13: Micrograph of the fabricated 2×50 µm wide device with gate-length of 2 µm. 81

Figure 5.14: I_{DS}-V_{DS} characteristics for 50 µm wide devices on Wafer 1 (commercial) and 2 (buffer-free from SweGaN). 82

Figure 5.15: Transconductance (g_m) characteristics of the wafer 1 (commercial) and wafer 2 (buffer free) devices. 82

Figure 5.16: Gate leakage comparison of devices on wafer 1 (commercial) and wafer 2 (buffer free) devices. 83

Figure 5.17: Breakdown characteristics of wafer 1 (commercial) and wafer 2 (buffer free) devices. 84

Figure 6.1: A picture of a standard AlGaN/GaN HEMT with a three-arrow pointing from the channel to the substrate to show how heat flows. Also given are the thermal conductivities of the most common epi-layers and substrates. 87

Figure 6.2: The simulation on the effect of GaN buffer layer thickness on the thermal resistance for different substrate material [160]. 88

Figure 6.3: Thermal management options illustrated schematically utilising diamond heat extractor using liquid cooling [167] 89

Figure 6.4: A simulated comparison of heat source spacing distance dependence on temperature rise between GaN on GaN and GaN on SiC at different values of n × Wgu (left figure) and simulated structure with heat source placed on top of GaN epitaxial layer[169]. 90

Figure 6.5: Distributed gates design [172]. 91

Figure 6.6: Diamond heat extractor using liquid cooling [174]. 91

Figure 6.7:Backside Silicon etched and filling micro-trench with copper electroplating [175]. ... 92

Figure 6.8: Layout of the new device with bond pads as heat sink. 92

Figure 6.9: 3D- illustration GaN-based HEMT structure with bond-pads on SiC substrate as heat sinks..... 93

Figure 6.10: Cross-section of a GaN-based HEMT structure with bond-pads on SiC substrate. .. 93

Figure 6.11: Schematic views of the process flow for mesa etch up to substrate fabrication in AlGaN/GaN HEMT device processing steps (a) Clean wafer (b) Photo-lithography to expose deep mesa-etch pattern using BCl_3/Cl_2 plasma (c) Removal of photoresist and cleaning after 326nm nitride mesa deep etching (d) Deposition of Ti/Al/Mo/Au metal stack Ohmic contacts (e) Ni/Au based gate metallization (f) Bond pads contacts – showing how the bond pad contact will be acting as a heat sink for the device (g) Device passivation using deposition of 100nm Si_3N_4..... 94

Figure 6.12: The etch depth of 341nm nitride material around the active device area using the the BCl_3/Cl_2 gases using the DektakXT tool. 95

Figure 6.13: Epitaxial wafer structure of fabricated AlGaN/GaN heterostructure devices (a) Standard mesa HEMT and (b) Deep mesa etch upto substrate HEMT (c) SEM image of deep etched showing Ohmic metals, GaN epilayer and SiC substrate. 96

Figure 6.14: The I_{DS}-V_{DS} characteristics of 2 × 50 µm wide devices at V_{GS} = 0V to -5V and V_{DS} up to 15V on device 1 (left side in blue colour) and device 2 (right side in green colour). 96

Figure 6.15: The I_{DS}-V_{DS} characteristics of 2 × 50 µm wide devices at V_{GS} = 0V to -5V and V_{DS} up to 40V on device 1 (left side in blue colour) and device 2 (right side in green colour). 97

Figure 6.16: The I_{DS}-V_{DS} characteristics of 2 x 50 µm wide devices at V_{GS} = 0V to -5V and V_{DS} up to 15 V (left side graph) and 40V (right side graph) on Wafer 2 97

Figure 6.17: Schematic views of the process flow for mesa etch up to substrate fabrication in AlGaN/GaN MIS-HEMT device processing steps (a) Clean wafer (b) Photo-lithography to expose deep mesa-etch pattern using BCl_3/Cl_2 plasma (c) Removal of photoresist and cleaning after 326nm nitride mesa deep etching (d) Deposition of Ti/Al/Mo/Au metal stack Ohmic contacts (e) Deposition of 10nm Si_3N_4 dielectric layer to protect mesa sidewall – this step is omitted for the HEMT device (f) Ni/Au based gate metallization (g) Bond pads contacts – showing how the bond pad contact will be acting as a heat sink for the device (h) Device passivation using deposition of 100nm Si_3N_4. 99

Figure 6.18: Epitaxial wafer structure of fabricated AlGaN/GaN heterostructure devices (a) HEMT and (b) MIS-HEMT with 10nm Si_3N_4 (c) Micrograph of fabricated 200µm wide device. 100

Figure 6.19: The I_{DS}-V_{DS} characteristics of 2 × 200 µm wide devices at V_{GS} = 1V to -8V of AlGaN/GaN HEMT and Si_3N_4 MIS-HEMT. 101

Figure 6.20: The I_{DS}-V_{DS} characteristics of 2 x 200 µm wide devices at VGS = 1V to -8V and V_{DS} up to 40V of AlGaN/GaN HEMT and Si_3N_4 MIS-HEMT. 102

Figure 6.21: Measured transfer characteristics of HEMT and MIS-HEMT devices biased at V_{DS} = 7 V. 103

Figure 6.22: Measured gate leakage currents for the AlGaN/GaN HEMT and Si_3N_4 MIS-HEMT with same device dimensions. 103

Figure 6.23 Measured off-state breakdown voltage of HEMT and MIS-HEMT devices biased at V_{GS} = - 10 V. 104

Figure 6.24: Measured H21 and Maximum signal gain for 2x200µm device sizes for HEMT and MIS-HEMT devices. 105

Figure 7.1: An illustration of the conduction band profile for (a) long-channel HEMT and (b) short-channel HEMT at two different drain biases at the AlGaN/GaN interface. (c) An illustration of the transfer properties for an AlGaN/GaN HEMT with Lg = 50 nm at various drain voltages [17]. .. 111

Figure 7.2: Cross-sectional view of T-shaped gate module and associated parasitic capacitance. 115

Figure 7.3: T-gates were fabricated using metal lift-off process using multiple layers. 115

Figure 7.4: Illustration of the epitaxial structure used for T-gate device fabrication 116

Figure 7.5: SEM images of a fabricated T-gates a) 100nm T-gate b) gates between Ohmic metals & c) 200nm T-gate 116

Figure 7.6:T-gate device geometries for a) Device A with 100 nm gate and b) Device B 200 nm gate length. 117

Figure 7.7: DC-IV measurements of 100nm T-gate device and 200 nm T-gate device. 117

Figure 7.8: Measured a) transconductance and transfer characteristics of 100 nm and 200 nm T-gate devices at V_D = 9V. 118

Figure 7.9: Gate leakage currents of 100 and 200 nm T-gate devices at V_D = 0V. 118

Figure 7.10: Measured lateral off-state breakdown voltage of 100 nm and 200 nm devices biased at V_{GS} = - 12 V. 119

Figure 7.11: Masons unilateral power gain U, current gain H_{21} and extrapolated f_T and f_{MAX} for 100 nm T-gate device and 200 nm T-gate device. 119

Figure 7.12:Cut-off frequencies of devices fabricated during this project with standard and T-gate geometries. 120

Figure 8.1: Cross-sectional schematic of horizontal patterned Ohmic HEMTs on SiC substrate. 122

Figure 8.2: SEM micrographs of different gate length of fabricated gates. 123

Figure 8.3: GaN HEMT proposed model (a) Mesa etch SiC substrate (b) integrated diamond heat sink. 124

Figure 8.4: Proposed epilayer AlN/GaN structure 124

List of Table

Table 1-1: A comparison of the material properties of GaN and other competitors in the semiconductor industry. 3

Table 2-1: Structural parameters of common nitrides semiconductors 12

Table 2-2: Characteristics of widely used substrates for the growth of GaN HEMTs. 18

Table 3-1: Resists used in this research work for various applications. 38

Table 3-2: Different gases used in this SiNx and GaN material etching work. 48

Table 4-1: Gaps and their corresponding correction factor 59

Table 4-2 State-of-the-art Ohmic contacts to AlGaN/GaN 60

Table 5-1: As-grown material properties for both heterostructures both wafers measured by manufacturers. 73

Table 5-2 :Extrapolated f_T and f_{MAX} values from S-parameter measurements of buffer free and thick buffer devices at V_{DS} = 15 V. 79

Table 5-3: Manufacturers evaluated the 2DEG mobility, density, and average sheet resistances for both wafers. 81

Table 6-1: Extrapolated f_T and f_{MAX} values from S-parameter measurements of HEMT and MIS-HEMT devices at V_{DS}=15V 105

Table 7-1: Recent research progress in GaN-based HEMTs for high power high frequency RF applications 112

Author's declaration

Statement of Originality to Accompany Thesis Submission

Name: Aniket Dhongde

Registration Number:

I certify that the thesis I have submitted here for the University of Glasgow's PhD examination is entirely my own work, with the exception of any places where I have made it clear that it is the work of others (in which case the extent of any work done jointly by me and any other person is made clear in it), and that it has not been edited by a third party in excess of what is allowed by the university's PGR Code of Practice.

I certify that no work from a successfully submitted thesis for another degree is included in this thesis.

I certify that the University of Glasgow's Code of Good Practice in Research was followed in the produce of this thesis.

I understand that the examination may be delayed pending the results of any investigations into any issues highlighted regarding proper research practise based on a review of the thesis.

Signature:

Date ……5/05/2023……...

Definitions

2DEG	2-Dimensional electron gas
Al	Aluminium
Au	Gold
AlGaN	Aluminium gallium nitride
AlN	Aluminium nitride
Ar	Argon
BCl_3	Boron trichloride
Cl_2	Chlorine
CPW	Coplanar waveguide
CV	Continuous wave
CVD	Chemical vapour deposition
DC	Direct current
e-beam	Electron beam
f_{MAX}	Maximum oscillation frequency
f_T	Current gain cut-off frequency
GaN	Gallium nitride
GHz	Gigahertz
g_m	transconductance
HEMT	High electron mobility transistor
IV	Current voltage
ICP	Inductively coupled plasma
JWNC	James Watt Nanofabrication Centre
L_G	Gate length
MIBK	Methyl isobutyl ketone
MMIC	Monolithic microwave integrated circuit
MBE	Molecular beam epitaxy
MOCVD	Metal organic chemical vapour deposition
N_2	Nitrogen
Ni	Nickel
P_{PE}	Piezoelectric polarisation
P_{SP}	Spontaneous polarization

PAE	Power added efficiency
PECVD	Plasma enhanced chemical vapour deposition
PMMA	Poly methyl methacrylate
q	Electron charge
RO	Reverse osmosis
RIE	Reactive ion etching
R_c	Ohmic contact resistance
R_{sh}	Sheet resistance
RF	Radio frequency
RTA	Rapid thermal annealing
SEM	Scanning electron microscope
SiC	Silicon carbide
$SiCl_4$	Silicon tetrachloride
Si	Silicon
SiN_x	Silicon nitride
TiN	Titanium nitride
Ti	Titanium
TBR	Thermal boundary resistance
V_{BR}	Breakdown voltage
V_{DS}	Drain-source voltage
v_{eff}	Effective electron velocity
v_{sat}	Saturated electron velocity
V_{GS}	Gate-source velocity
V_P	Pinch off voltage
V_T	Threshold voltage
W_g	Gate width
ε_0	Vacuum permittivity
ε_r	Relative permittivity
Γ	Reflection coefficient
LOR	Lift-off resist
MMIC	Monolithic Microwave Integrated Circuit
κ	Thermal conductivity
μ_n	Electron mobility

Chapter 1

Introduction

1 Introduction

1.1 Overview

The use of wireless communications has increased exponentially over the last few years, so attention has been focused on developing wireless communication technologies operating in the millimetre-wave band to exploit the higher bandwidth available at the higher frequencies. As the demand for sixth generation (6G) wireless technology continues to increase, it is anticipated that it will operate in a frequency range above 100 GHz, with the potential for higher data rates and extended transmission distances. For efficient signal transmission, advanced power amplifier technology is required to achieve these goals. This involves the development of high-power amplifiers that can operate at millimetre-wave frequencies and deliver high output power while maintaining high levels of efficiency and reliability. These developments are essential for realising the full potential of 6G technology and enabling futuristic applications such as AI-powered wireless communications, robotics, and mobile communications, among others [1][2].

In the last few decades, gallium nitride (GaN) based semiconductor technology has witnessed significant advancement. The idea of a high electron mobility transistor (HEMT) was introduced in 1980 [3]. The innovation of this structure is that two materials of different bandgaps are built-in into the device structure to form a channel as opposed to the structure of an inversion layer device [4]. The group III and the group V elements can combine to create several compound semiconductors like gallium nitride (GaN), gallium arsenide (GaAs), indium phosphate (InP) and others. So, III-nitride semiconductors such as GaN have gained significant attention in accommodating this need due to their superior material properties.

Table 1-1 shows the material properties for GaN based devices compared with the Si, GaAs, AlN and InP for radio frequency (RF) applications. Some key properties are discussed next:

High breakdown field: Because of the large GaN bandgap (3.4 eV), the GaN material has a high breakdown field. GaN's high breakdown field strength enables RF GaN devices to work at higher voltages and powers than Si, InP and GaAs semiconductors. Because of this, RF GaN technology is ideal for high-power and high-frequency applications, like power amplifiers for base stations and radar systems, where high voltage and power-handling capabilities are essential [5].

High saturation velocity: Electrons in the GaN channel have a high saturation velocity at very high electric field. So, GaN devices can give higher current density. This in combination with the high operation voltages make GaN a high power density technology [6].

Excellent thermal properties: The thermal properties of GaN HEMT grown on silicon carbide (SiC) are improved because of SiC has a high thermal conductivity (4 W/cm K). Also, the lattice mismatch between the two is low and so it is easy to grow GaN on SiC. It means that GaN on SiC devices do not get as hot as GaAs or InP at same power dissipation. Therefore, there is no need to use extra heat sink and cooling system for cooling the devices [7]. Also, as noted above, because of its wide bandgap, GaN has a high breakdown field and therefore can operate at high voltages. The combination of high electron mobility and saturation velocity in devices enables to function at high frequencies and handle large drain currents, which enables the realization of RF power amplification devices [7][8].

Compared to devices made from other materials, GaN based material devices exhibit impressive characteristics and exceptional potential and performance in terms of operating at high power, high frequency, and high voltage levels in the microwave and millimetre wave range. So, GaN-based HEMT is considered as best candidate for device technology for high-power and high-speed applications.

Table 1-1: A comparison of the material properties of GaN and other competitors in the semiconductor industry.

Parameters and units	Si	GaAs	InP	Diamond	GaN	AlN	SiC
Energy bandgap, (eV)	1.12	1.43	1.34	5.5	3.44	6.2	3.26
Relative dielectric constant, (ε_r)	11.9	12.5	12.4	5.5	9.5	8.5	9.7
Thermal conductivity, (W/cm K)	1.5	0.54	0.67	10-20	1.3	1.8-5.5	4
Breakdown electric field, (MV/cm)	0.3	0.4	0.45	10	3.3	11	3
Saturated electron velocity, (10^7cm/s)	1	1	1	1.5	2.5	-	2
Electron mobility, μ (cm^2/Vs)	1500	8500	5400	1800	900	300	700
Lattice constant(A')	5.43	5.65	5.86	3.56	3.19	3.11	3.08

Figure 1.1 shows how III-nitride materials are much better than traditional semiconductors in several device parameters [10].

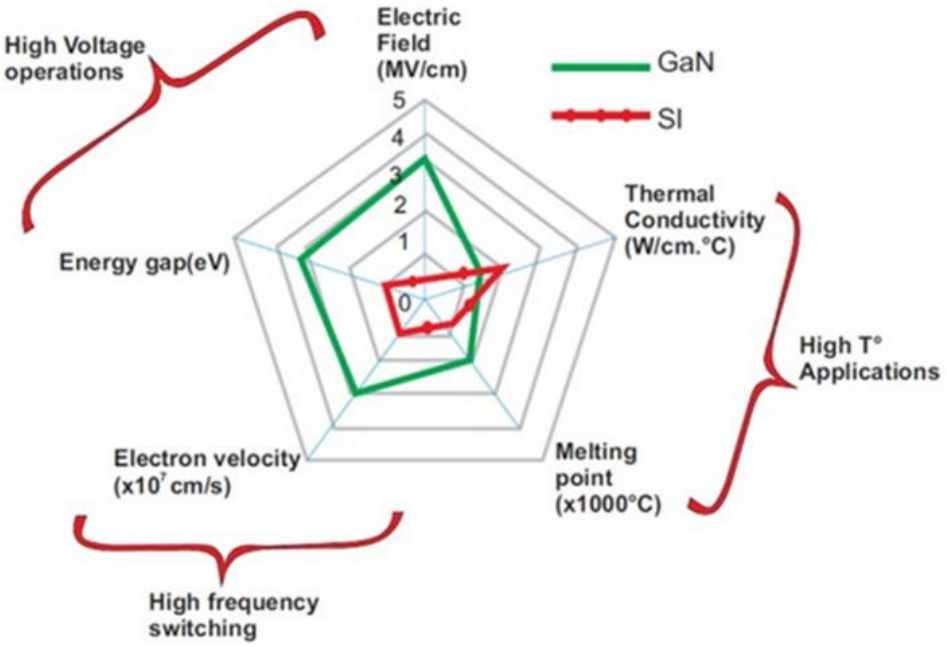


Figure 1.1: A summary of the important properties of Si and GaN.

GaN HEMT has the benefit of a heterojunction, which is created at the interface of aluminium gallium nitride (AlGaN) and gallium nitride (GaN), resulting in a 2-dimensional electron gas (2DEG) channel. Figure 1.2 shows the cross section of typical GaN HEMT device.

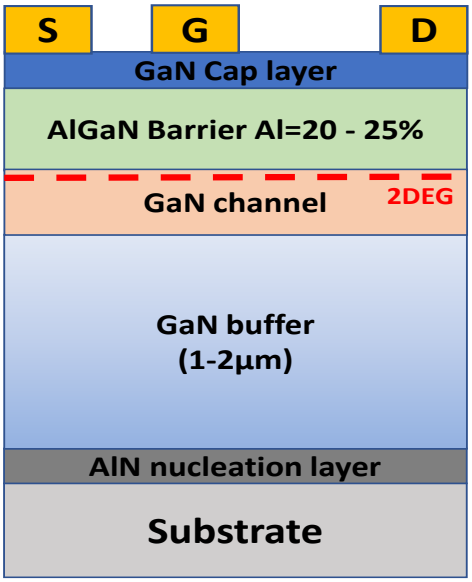


Figure 1.2: Cross section of typical GaN HEMT device

AlGaN/GaN heterostructure field-effect transistors have demonstrated state-of-the-art performance in terms of power density (8.7 W/mm), current gain cut off frequency, f_t (74 GHz), and power gain cut-off frequency or known as maximum oscillation frequency, f_{max} (140 GHz) [11]. Other heterostructures for the GaN material system include AlN/GaN [12], AlInN/GaN [13] and AlInGaN/GaN [14] in which the AlGaN barrier layer is replaced by aluminium nitride (AlN), aluminium indium nitride (AlInN) and aluminium indium gallium nitride (AlInGaN), respectively. These other heterostructures provide higher two-dimension electron gas (2DEG) carrier densities and also allow for the gate length downscaling (because they are thinner compared to an AlGaN barrier which is typically 20-25nm thick) to achieve even higher frequencies of operation [15] [16].

GaAs and InP have been widely used for W-band power amplifier technology but have a limitation in terms of output power density due to the small bandgap energy (1.43 eV for GaAs and 1.34 eV for InP) and poor thermal conductivity (0.54 W/cm K for GaAs and 0.67 W/cm K for InP). GaN HEMT technology has established improvements in W-band MMIC (monolithic microwave integrated circuit) RF (radio frequency) output power, power added efficiency and MMIC power density (MMIC output power relative to MMIC area) that can be obtained over the GaAs and InP semiconductor technology [17]. For example, a W-band GaAs MMIC output power of 0.5W was recently reported at 92 GHz with 12% PAE (power added efficiency) [18]. Another W-band InP MMIC design was reported with an output power of 0.15W at 95 GHz with 6% PAE [19]. The highest output power of power amplifier (PA) was 5.5 W/mm available 100nm GaN HEMT based on T-gate technology (f_t= 156 GHz, f_{max}= 308, PAE = 48%) [20].

1.2 GaN Applications

The III-nitrides device applications are shown in Figure 1.3 and include high-frequency MMICs, high-power RF, automotive, DC converters, LEDs, radars, base-stations, ultra-wideband communication, space applications, military, sensors for harsh environments, and biological sensors [21] [22] [23] [24] [25] [26] [27].

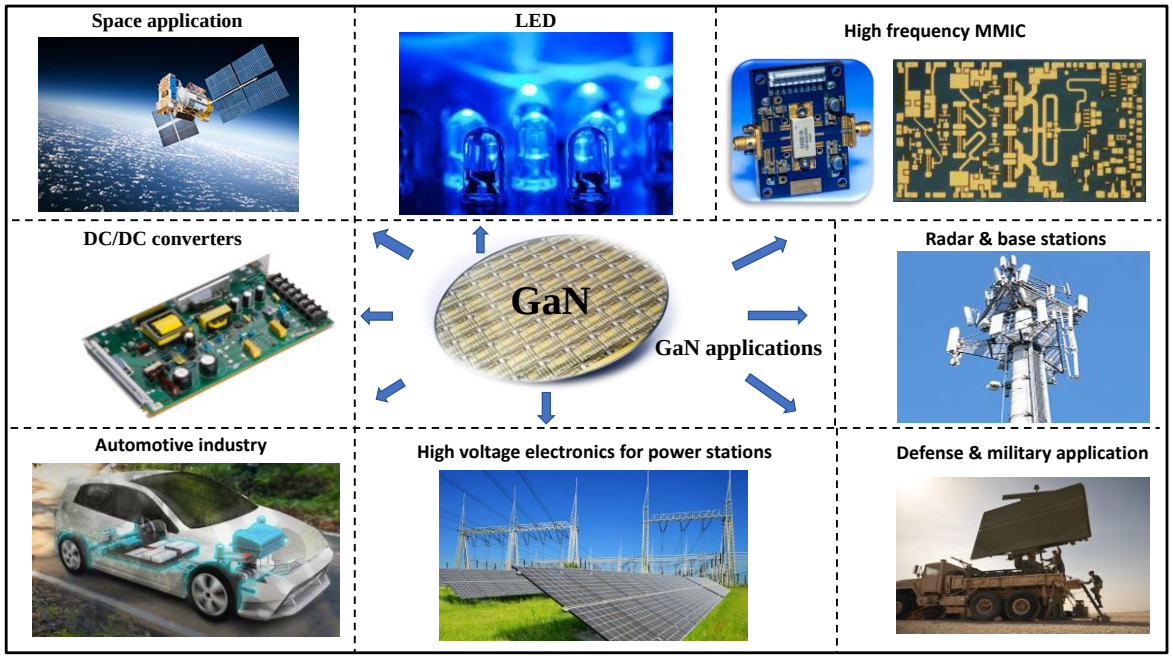


Figure 1.3 : Applications of GaN technology.

1.3 Research challenges

Despite all the advantages of GaN HEMTs there is still some important issues that need to be overcome to further increase the performance of GaN HEMT in various aspects. The main issues of GaN HEMT devices include (high) device contact resistance, poor thermal management in devices [28][29] and the design of the epi-layer structure some key design challenges are include managing strain, minimising defect density, reducing surface roughness, achieving the desired carrier concentration, and managing heat generation during operation [30].

1.3.1 Ohmic contacts to AlGaN/GaN HEMTs

Achieving low contact resistance (R_c) is highly desirable as that decreases the total on-resistance and reduces the power dissipation in the ohmic contacts, and so increases current density of the device. Reduced R_c also results in increased device bandwidth. It is however very challenging to achieve very low-resistive ohmic contacts to III-nitride semiconductors because of their wide bandgap [31]. This is particularly difficult for AlGaN barrier HEMTs since AlGaN has a wide band gap between 3.4 eV (GaN) and 6.2 eV (AlN). Nonetheless, it has been shown that Ohmic contacts made with the AlGaN/GaN heterostructure have a satisfactory contact resistance in the range of 0.2 to 0.8 Ω mm. Temperature and annealing time are critical parameters to consider while optimizing contact resistance.

Planar contact is the standard and simplest method to fabricate Ohmic contacts on GaN HEMTs. In planar contacts, the separation between ohmic metal stack on GaN cap and 2DEG (interface of barrier layer and buffer layer) is around (20-25nm) and makes it difficult to obtain low contact resistance < 0.8 Ω.mm. Therefore, different approaches of recessed Ohmic contacts have been investigated in the literature. Figure 1.4 shows the different contact on GaN HEMTs (a) planar Ohmic contact (b) recess Ohmic contact (c) patterned Ohmic contact (d) regrown Ohmic contact.

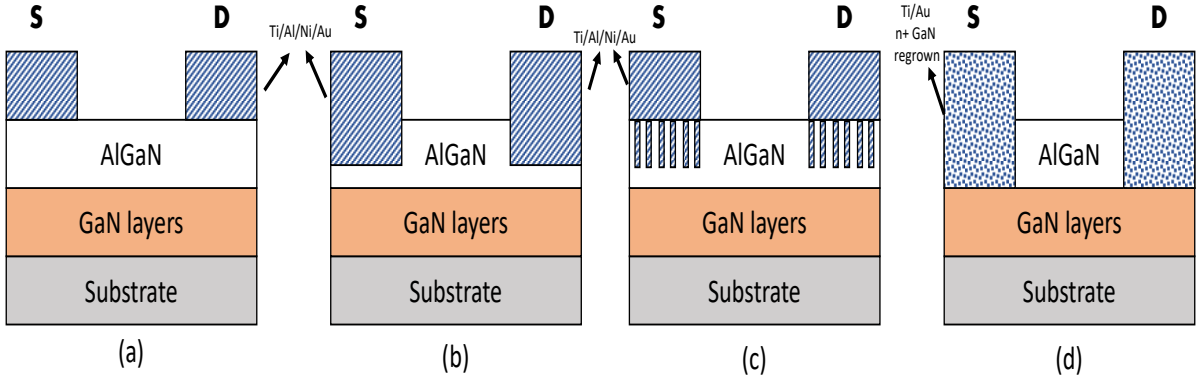


Figure 1.4: Ohmic contacts for AlGaN/GaN HEMTs (a) planar Ohmic contact (b) recess Ohmic contact (c) patterned Ohmic contact (d) regrown Ohmic contact.

A common method to reduce the contact resistance is to recess the Ohmic (source/drain) area and then metallize it. In the minimization of contact resistance, the key parameters are recess depth, annealing temperature and the metal stack used. The recessed depth approach can be divided into three ways; the first one is etching the barrier layer few up to nanometres above the 2DEG, the second one is etching the barrier layer up-to the 2DEG, and lastly etching the barrier layer below the 2DEG. Low contact resistance of 0.35 Ω.mm has been obtained using this approach [32].

In the regrown Ohmic contacts, the Ohmic contact areas are recessed by etching away the AlGaN barrier layer and part of the channel layer and growing highly doped (with silicon) GaN in the area. The n+ GaN ohmic layer is in direct contact with the 2DEG channel, and so this approach produces very low < 0.2 Ω.mm contact resistance because there are no barriers for electrons to transfer from contacts to channel. Therefore, it reduces the access resistance in the channel which is convenient to achieve the high frequency [33]. Also, there is no need to anneal the contacts. The selective regrowth by ammonia-source molecular beam epitaxy (MBE) below 800°C with highly doped silicon (> 5×10^{19} cm^{-3}) n+ GaN using SiO_2 mask, followed by Ti/Au metal stack deposition but not annealing [34] is a very complicated process as well as very costly because of the extra fabrication steps [35]. Another possible drawback of this approach is the potential to degrade the 2DEG density and mobility due to the etching of barrier layer.

In this project, we fabricated and measured AlGaN/GaN HEMT devices using 3 different patterned Ohmic contact recess patterns. The types of Ohmic contact patterns used were chess, horizontal, and vertical. A device with a conventional Ohmic contact was also fabricated for comparison. Two etching depths were used were ~9 nm and ~30 nm resulting in trenches above and below the 2DEG channel, respectively. A low Ohmic contact resistance of 0.32 Ω.mm was demonstrated, as will be described in chapter 4.

1.3.2 Self-heating

Due to the high 2DEG density and high electron mobility, GaN HEMT saturation currents can reach up to 2–3 A/mm [36] [37]. At such high currents and at higher biasing voltage, electrons in 2DEG scatter in collisions with the crystal lattice and transfer the energy to it to cause increases the channel temperature. Even though GaN is more thermally stable than silicon (Si), the heating decreases the mobility of electrons in 2DEG, reducing current and making it difficult to operate GaN HEMTs for a longer period of time [38][39].

Self-heating in GaN HEMTs can have several impacts on the performance and reliability of the device, including:

Increased channel resistance: AlGaN/GaN HEMTs generate a strong electric field near the drain-side gate edge during typical device operation, which causes electrons to accelerate significantly and accumulate significant energy. Since the electron temperature is high with such energy, the crystal lattice is bombarded by electrons and can raise the resistance of the channel as a result, thus the electrons disperse from the 2DEG and impart their energy to the crystal lattice, raising the temperature of the lattice. As a result, the performance of the AlGaN/GaN HEMT is decreased due to an increase in the carrier scattering and a reduction in the carrier mobility [40].

Device degradation: Self-heating can cause changes in the electrical and optical properties of the GaN material, leading to a degradation in the device performance and reliability. For example, self-heating can cause changes in the bandgap, leading to an increase in the leakage current and a reduction in the breakdown voltage [41].

Increased junction temperature: The increase in the temperature of the junction can reduce the reliability of the device, leading to a reduction in the lifetime of the device. The junction temperature can increase due to the heat generated by the current flowing through the device and the lack of efficient heat dissipation [42].

To mitigate the effects of self-heating in GaN HEMTs, several strategies can be employed, including:

Using high thermal conductivity substrate: The use of high thermal conductivity substrate can help to dissipate the heat generated by the device, reducing the effects of self-heating. For example, the use of materials such as diamond or silicon carbide (SiC) can improve the thermal conductivity of the device. Thermal management of GaN RF devices is often provided by high thermal conductivity substrates, primarily SiC with a thermal conductivity, k, of 4 W/cm K.

High power density GaN devices are usually realised on SiC substrates because of their high thermal conductivity (400 W/mK) as compared to Sapphire (35 W/mK) and silicon (150 W/mK). The limitation to efficient heat extraction in GaN HEMTs grown on SiC is the thermal boundary resistance (TBR) between the GaN buffer layer and the SiC substrate. The two common growth techniques are MOCVD and MBE (molecular beam epitaxy), and these provide wafers with different thickness and quality of the nucleation layer. The typical TBR in the GaN causes higher channel temperature in the transistor.

Recent GaN research has focused on replacing the SiC substrate with nano-crystalline diamond (NCD), which has a thermal conductivity of 2000 W/mK, which is 5 times greater than SiC [43] [44].

Implementing cooling systems: The implementation of liquid cooling systems [45] or a heat sink [46] and effective thermal packaging [47], can help to dissipate the heat generated by the device, reducing the effects of self-heating.

In this thesis, two approaches designed to reduce the self-heating in GaN-on-SiC HEMTs are examined.

- In one approach, a comparative study is carried out on the performance of devices fabricated on two GaN-on-SiC wafers, both the grown by a new growth technique, the so-called hot-wall MOCVD (Metal-Organic Chemical Vapour Deposition) by SweGaN, a Swedish manufacturer of custom-made epitaxial wafers. Using this technique, the AlN nucleation is said to be of higher quality and better thermal conductivity and the buffer in the conventional structure can be omitted. Therefore, one wafer with a standard GaN buffer layer and second wafer without the buffer layer, i.e. buffer-less will be studied. The fabrication, measurements, and analysis of device performance of devices from these wafer structures will be discussed in more detail in chapter 5.
- In another approach, the buffer-less epitaxial layer structure grown by the so-called hot-wall MOCVD technique is assessed in comparison with conventionally grown material, i.e. which uses conventional MOCVD. We will, therefore, do a comparative study of GaN-on-SiC devices from SweGaN and NTT manufacturers to quantify their quality in terms of device performance. The results of this approach are described and discussed in more detail in chapter 5.

1.3.3 Thermal Boundary Resistance

The heat flowing from one material to the another has to face thermal resistance at the interface. This resistance, which opposes heat flow, is referred as thermal boundary resistance (TBR). Electrical equivalent circuit is one method for modelling heat transfer at the interface. In this corresponding electrical circuit, TBR may be compared to an electrical resistance. As resistance in an electrical circuit opposes the passage of current, TBR hinders the transfer of heat from one material to another. This resistance can cause heat to accumulate in the region where it is created.

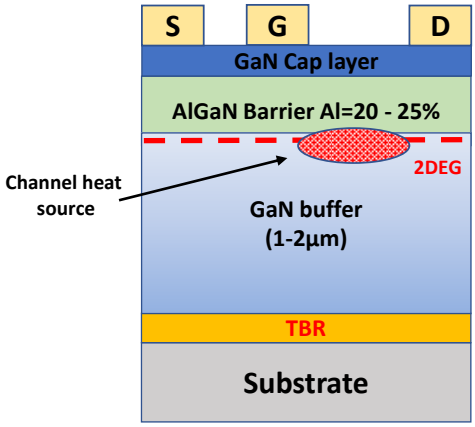


Figure 1.5: Illustration of the standard AlGaN/GaN HEMT the channel heat source and TBR.

As already noted, SiC substrates are commonly used to realise GaN devices [48]. The lattice mismatch between GaN buffer and substrate can lead to mechanical stress and deformation at the interface, reducing the device performance and reliability [49]. An AlN nucleation layer is important when GaN is grown on a foreign substrate to reduce the lattice mismatch between the GaN and the substrate, hence this layer cannot be neglected and this layer results in a TBR [50]. Figure 1.5 illustrates the channel heat source and the TBR in AlGaN/GaN epilayers.

In this project, we propose a thermal pathway around the TBR created by the AlN nucleation layer. The approach relies on front side processing in order to remove all nitride material surrounding the active device, allowing the device electrodes to sit on the SiC substrate and operate as heat sinks. This method will be explained and discussed in chapter 6.

1.4 Research aim

This project seeks to develop high frequency and thermally efficient GaN HEMT radio frequency (RF) electronic devices grown on the high thermal conductivity SiC substrates. The new devices should enable uncompromised amplifier design that can reduce component count and reduce the amplifier footprint by leveraging the high-power density into smaller more broadband circuitry. The project therefore has the following main objectives:

- Design, fabrication and characterization of Ohmic patterned recess etch GaN-based HEMT devices to reduce the contact resistance.
- Design, fabrication, characterization of GaN HEMTs with novel buffer-less epi-structure and comparison with conventional epitaxial designs.
- Design, fabrication and characterization of proposed thermally efficient GaN-on-SiC HEMT device.
- Design, fabrication and characterization of high frequency GaN HEMT devices employing a new T-gate process.

1.5 Thesis structure

This thesis is divided into 8 chapters. This chapter (Chapter 1) gives an overview of the AlGaN/GaN technology, its applications and highlights the material advantages over competing technologies. The research challenges and objectives including a summary of achievement are also described here.

Chapter 2 describes the theory of the GaN HEMT device starting from the basic transistor structure, piezoelectric and spontaneous polarization in GaN, and microwave and RF behaviour including scattering parameter measurements.

Chapter 3 describes standard fabrication techniques used for GaN HEMTs available at the James Watt Nanofabrication Centre (JWNC), University of Glasgow. It starts with descriptions of material growth, different metallization techniques followed by device layout design and plasma processing involved in GaN HEMT fabrication.

Chapter 4 describes the Ohmic contact formation to its operation principle and an experimental study to reduce the contact resistance by using the 4 different Ohmic patterns fabricated on shallow and deep etched patterns on AlGaN/GaN HEMT structures. It provides literature review on recent progress on

AlGaN/GaN HEMTs Ohmic contacts. The results and benefits of fabricated patterned devices on this wafer are described.

Chapter 5 describes the comparative study of buffer-free and conventional GaN-on-SiC HEMTs, where both wafers were grown by hot-wall MOCVD, and also for the case where the conventional (cold-wall) and hot-wall grown buffer-free GaN HEMTs were compared and discusses the achieved device performances.

Chapter 6 describes an experimental study of a developed novel thermal management technique based around removing all the nitride material around the active device so that the device electrodes sit on the SiC substrate and act as heat sink. Development process and fabricated device measurement results are presented. The chapter also describes thermally efficient MIS-HEMT devices.

Chapter 7 presents the literature review on recent research progress in GaN-based HEMTs for high frequency applications and describes results from the fabricated 100nm and 200nm T-gate long devices on buffer-free GaN HEMTs.

Chapter 8 provides a summary of the work done during this project and suggestions for future work.

Chapter 2

GaN HEMT Basic Theory

2 GaN HEMT Basic Theory

2.1 Introduction

This chapter provides an overview of the AlGaN/GaN-based HEMT device basics. First, the polarisation induced charges in GaN are described including the role of the crystal structure and then the properties of this semiconductor. The AlGaN/GaN HEMT's heterojunction quantum well, in which a 2-dimensional electron gas (2DEG) forms, is described. The material growth as well as common substrate options, and device structure and operation are discussed.

2.2 III-Nitride crystal structure

The group III nitride-based semiconductor materials (GaN, AlGaN, AlN, InN) have either a wurtzite (α-phase) or a zinc-blende (β-phase) crystal structure. The GaN wurtzite crystal, shown in Figure 2.1, has a stable hexagonal shape but lacks inversion symmetry and is not centrosymmetric. Due of the wide bandgap of 3.4 eV compared to the zinc-blende structure of 3.2 eV, this structure has strong bonding between Ga and N. When used in HEMTs, GaN is most frequently found in its wurtzite crystal form with [0001] orientation. This crystal structure's high heat resistance is made possible by the fact that it is thermodynamically stable. The crystal structure of zinc-blende is a face-centered, meta-stable cubic crystal structure. More typical III-V semiconductors have this structure (e.g. GaAs, InP, and InSb) [51][52][53].

GaN has a hexagonal lattice with four atoms per unit cell as its wurtzite structure [54]. As shown in Figure 2.1, the wurtzite structure is defined by three lattice constants: a, c, and u. The side length of the hexagonal wurtzite structure is represented by a, the cell height by c, and the III-N bond length by u. The value of the dimensionless parameter u is specified by the ratio of c. The ratio of these characteristics for an ideal wurtzite structure is u/c = 3/8 = 0.375 and c/a = $\sqrt{8/3}$ = 1.633. The arrows on the hexagonal structure of wurtzite indicate <111> directions. In Table 2-1, the structural properties of common III-N wurtzite semiconductors are listed [55].

Table 2-1: Structural parameters of common nitrides semiconductors

Parameter	AlN	InN	GaN
a (A°)	3.108	3.580	3.197
c/a	1.6033	1.6180	1.6297
$(u-u_{ideal}) \times 10^{-3}$	6.4	3.7	1.9

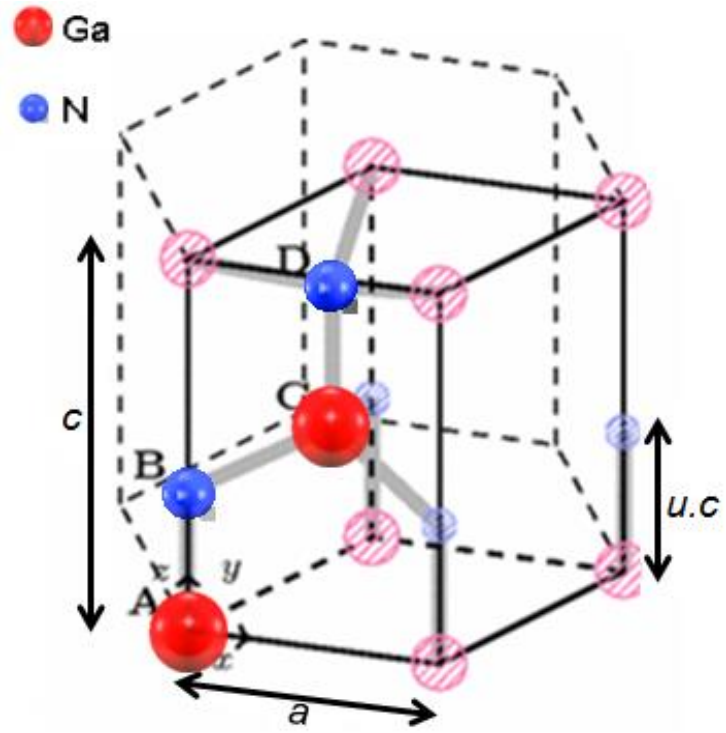


Figure 2.1: Hexagonal Wurtzite structure.

2.3 Polarization in III-N semiconductors

A heterostructure is a connection between two distinct materials. The two materials differ in bandgap energies and different band structures. The resultant hetero-junction band structure plays a crucial role in dictating the device's functionality. Furthermore, the band diagrams of III-N semiconductors are heavily influenced by the difference in polarisation of the materials and the resultant charges confined at the interface. The spontaneous and piezoelectric polarisations are a primary feature of AlGaN/GaN HEMTs that is enhanced by its wurtzite structure.

2.3.1 Spontaneous Polarization

The causes of spontaneous polarisation (P_{SP}) in GaN include the difference in electronegativity between Ga (1.81) and N (3.04) and the absence of inversion symmetry along the pyroelectric axis (c-axis) of the wurtzite structure. Positive sheet charge on one face and negative sheet charge on the other relative to the crystal direction cause spontaneous polarisation to occur at the faces of wurtzite crystals, so the [0001] crystal direction is used. The difference in the electronegativity of the Ga and N atoms, which results in the Ga-N bond exhibiting mixed ionic and covalent bonds, is what leads to the opposite sheet charge. Hence, the GaN compound is subjected to an electric dipole moment, a measure of polarity in a compound. Since there is no external field present when this polarisation phenomenon happens, it is known as spontaneous polarisation (P_{SP}) [56].

When GaN is grown along the c-plane, it spontaneously polarises, resulting in powerful electric fields of 3 MV/cm [57]. The following equation may be used to compute the spontaneous polarisation of an AlGaN/GaN and AlN/GaN structure [57].

$$P_{SP},Al_xGa_{1-x}N/GaN\ (x) = (-0.052 * x - 0.029)\ Cm^{-2} \qquad (2.1)$$

where x is the aluminium mole fraction in the AlGaN layer and P_{SP} is spontaneous polarisation. P_{SP} (0.25) = -0.042 Cm^{-2} for a typical AlGaN layer with a 25% Al content, while P_{SP} (1) = - 0.081 Cm^{-2} for a binary AlN layer with a 100% Al content. This reveals that the spontaneous polarisation charge is nearly doubled when the Al content of the barrier is increased to 100%. The GaN/AlGaN interface's crystal structure is depicted in Figure 2.2(a), and the layer structure's polarisation is shown in Figure 2.2(b), where P_{SP} refers for spontaneous polarisation and P_{PE} for piezoelectric polarisation.

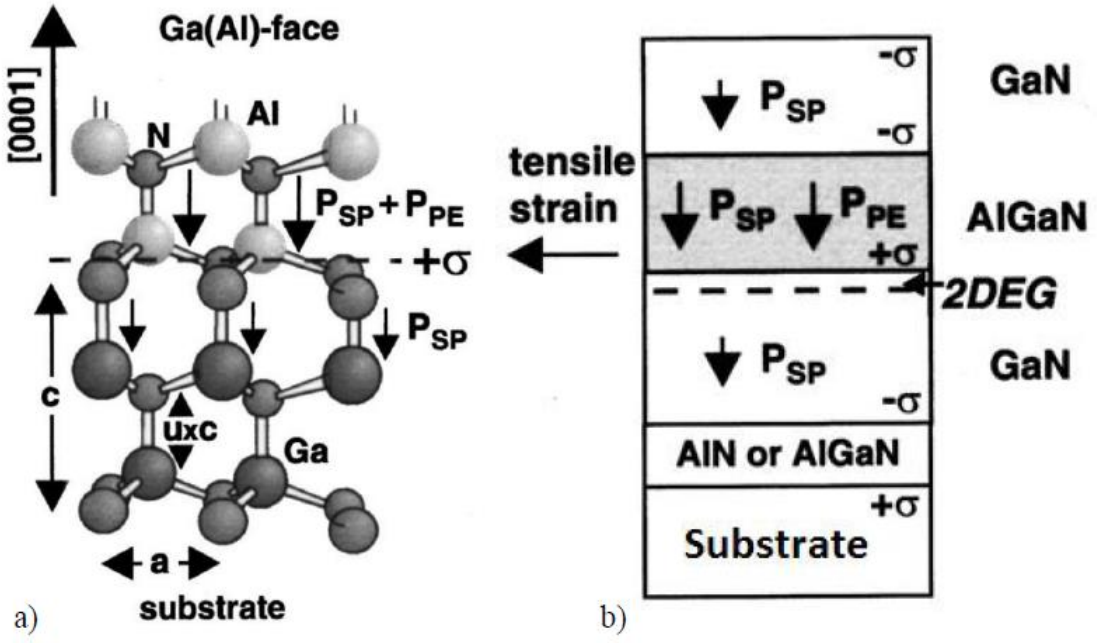


Figure 2.2: Crystal structure of wurtzite Ga (Al) face GaN b) Ga-face strained AlGaN/GaN heterostructures: Polarization-induced sheet charge and direction of spontaneous and piezoelectric polarisation [57].

2.3.2 Piezoelectric Polarization

When a material is put under mechanical stress, piezoelectric polarisation (P_{PE}) is brought about. Mechanical stress is a result of the material's elastic behaviour, which is controlled by its elastic stiffness constant, a measure of the material's "hardness." As a result, when piezoelectric polarisation is generated, charge in induced in the crystal structure of a material. When the AlGaN layer is compressively strained, the piezoelectric polarisation is positive; when it is in tensile stress, it is negative.

The piezoelectric polarisation is computed as follows:

$$P_{PE} = 2.\frac{a-a_0}{a_0}\left(\varepsilon_{13} - \varepsilon_{33}.\frac{C_{13}}{C_{33}}\right) \qquad (2.2)$$

where ε_{13} and ε_{33} are the piezoelectric coefficients, and C_{13} and C_{33} are the elastic constants.
The total spontaneous and piezoelectric polarisation gives the electrical polarisation effects in a material:

$$P = P_{SP} \pm P_{PE} \quad (2.3)$$

2.3.3 2-Dimension electron gas (2DEG) formation

Devices based on AlGaN/GaN possess a 2-dimensional electron gas (2DEG) channel. The formation of a heterojunction causes strain, which causes piezoelectric polarization inside the strained material. A high density 2DEG channel, which will be discussed in the next sections, is mostly formed as a result of this piezoelectric polarization.

AlGaN and GaN have different lattice constants, therefore growing a thin layer of AlGaN on top of GaN would result in mechanical strain within the AlGaN layer, as shown in Figure 2.3. Mechanical stress results from the material's elastic behavior. The alignment of AlGaN with GaN causes strain in both the x and y directions (biaxial strain) in the AlGaN layer. AlGaN's tensile strain (s) raises its lattice constant and aligns its atoms with those of GaN to form a heterojunction [58] [59].

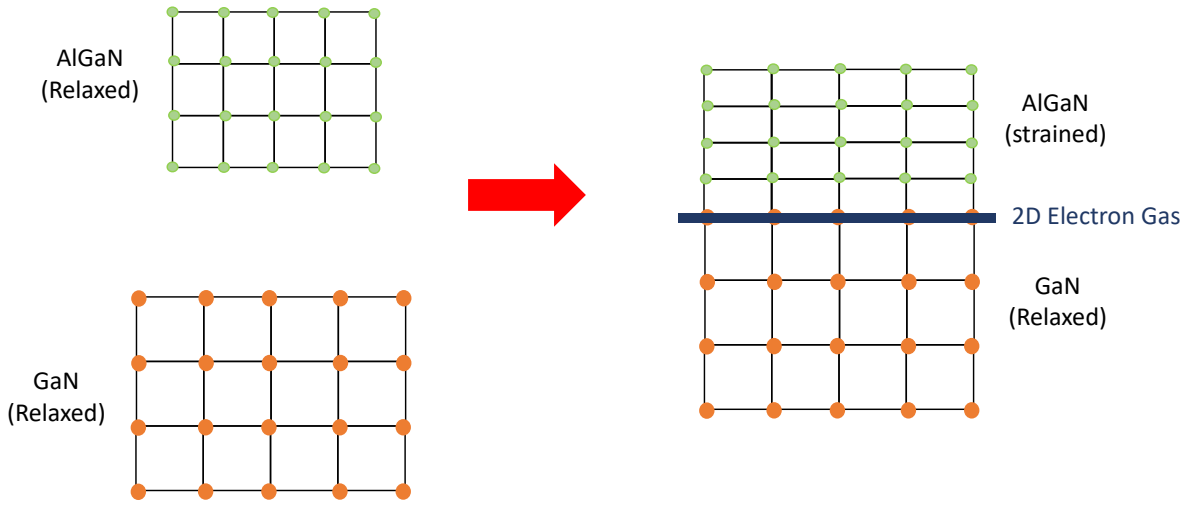


Figure 2.3: Illustration of how AlGaN is strained during the formation of 2DEG on GaN.

$$\Delta \equiv \frac{|\alpha_{AlGaN} - \alpha_{GaN}|}{\alpha_{AlGaN}} \quad (2.4)$$

$$\varepsilon_s = \Delta.(1 - r) \quad (2.5)$$

Where, Δ is lattice mismatch and r is the amount of strain relaxation and ε_s is tensile strain.

The discontinuity of the polarization (P_{PE} and P_{SP}) at the interface of AlGaN/GaN is the origin of quantum well creation. The importance of P_{PE} and P_{SP} on energy band in AlGaN/GaN HEMTs is shown in Figure 2.4, AlGaN/GaN energy band diagram illustrating the impacts of P_{SP} and P_{PE} on the conduction band [60]. A 2DEG exhibits a sheet carrier concentration of $6 \times 10^{12}\ \mathrm{cm}^{-2}$ for an aluminium content of 15% in a standard AlGaN/GaN HEMT. When the aluminium percentage is raised to 31%, the sheet carrier concentration may be enhanced to $2 \times 10^{13}\ \mathrm{cm}^{-2}$. A maximum sheet carrier concentration of $6 \times 10^{13}\ \mathrm{cm}^{-2}$ may be attained for the 100% Al binary AlN barrier [61]. As a result, devices with an AlN barrier are capable of producing up to three times as much power as traditional AlGaN/GaN HEMTs.

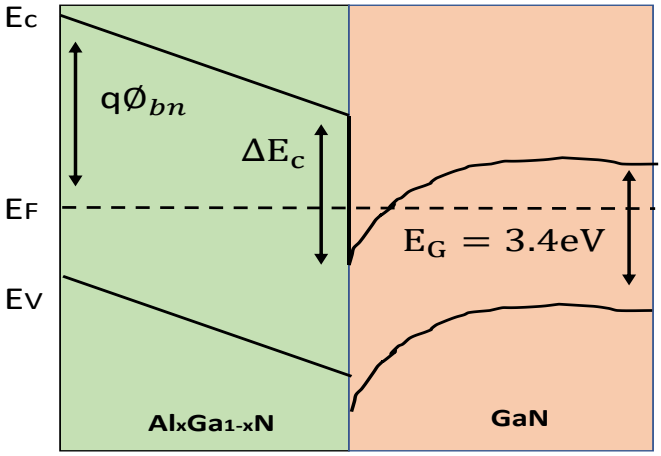


Figure 2.4: AlGaN/GaN energy band diagram illustrating the impacts of PSP and PPE on the conduction band [60].

A typical GaN HEMT's band diagram is shown in Figure 2.5. A 2DEG is created at the AlGaN/GaN interface, where $\Delta E_c$is the conduction band offset and $\emptyset_{bn}$is the Schottky barrier of the gate contact. ΔE_F is the Fermi level with respect to the GaN conduction band edge energy and q is the electron charge (1.6×10^{-19}).

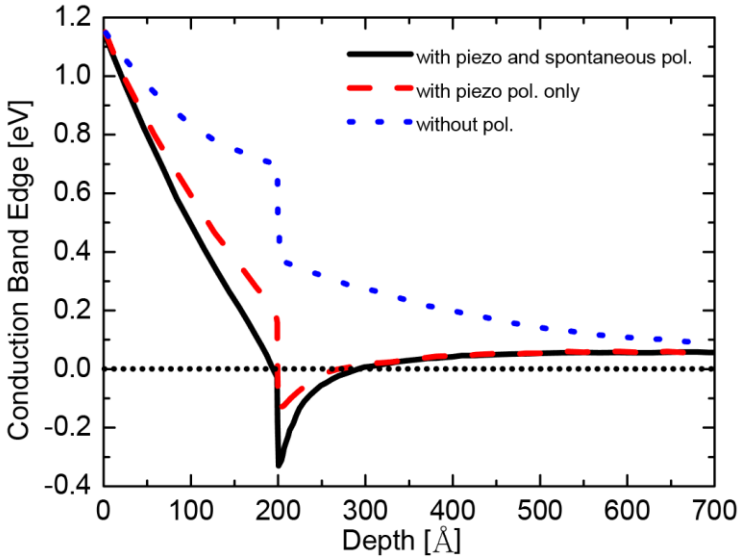


Figure 2.5: AlxGa1-xN/GaN heterostructure's band structure demonstrating 2DEG development at the heterojunction as a result of quantum well formation [60].

2.4 GaN HEMT device structure

Figure 2.6 shows the cross-section of the AlGaN/GaN HEMT structure. In this device, either molecular beam epitaxy (MBE) or metal organic chemical vapour deposition (MOCVD) is used to grow the semiconductor layers onto a substrate (such as Si, SiC, and Al_2O_3). After the nucleation layer, a thick layer of GaN (between 2 and 3 µm) is grown prior a thin layer of $Al_xGa_{1-x}N$ (about 20 nm). $Al_xGa_{1-x}N$ typically has an aluminium content percentage (x) of up to 0.40. Higher Al concentrations in this fundamental structure will cause the AlGaN layer to relax, lowering the material's strain and, consequently, the density of the 2DEG. This structure can be modified with more layers to improve the device's performance. We first discuss the substrate.

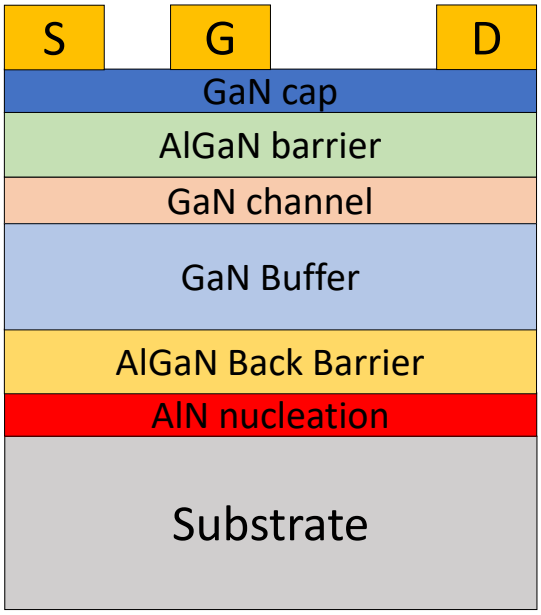


Figure 2.6: Cross section of HEMT device structure.

2.4.1 Substrate

The performance of the device that is grown on top of the substrate may be significantly improved by selecting the proper substrate. Due to the lack of native GaN substrates until recently, GaN is often grown on a foreign substrate. Many substrate alternatives include silicon, sapphire, silicon carbide (SiC), and chemical vapour deposited (CVD) diamond for the growth of GaN epitaxial layers. The criteria that affect the feasibility of the selected substrate are: (i) Available sizes (ii) the resistivity; (iii) the thermal conductivity; (iv) the lattice mismatch at the buffer/substrate interface; (v) the density of dislocations; (vi) the cost per unit area; and (vii) electrical isolation and cost. Table 2-2 provides a list of the most prominent substrate types for GaN epi-layer development and each substrate's fundamental properties.

Table 2-2: Characteristics of widely used substrates for the growth of GaN HEMTs.

Property/Substrate	GaN	SiC	Silicon	Sapphire	CVD Diamond
Mismatch to GaN (%)	0	3.1	17	13.9	11.9
Lattice constant (°A)	3.189	3.08	5.43	2.75	3.567
Thermal conductivity (W/m.K)	130	400	150	35	2000
Isolation (Ω.cm)	10^9	10^{11}	10^4	10^{16}	10^{16}
CTE (1 / 10^6K)	5.59	4.2	3.59	7.5	0.8
Defect density (cm^{-2})	10^3	5×10^8	10^9	8×10^8	-
Wafer sizes (inch)	2	6	12	6	4

2.4.1.1 Silicon

The most significant semiconductor and substrate material is silicon due to its economic significance and volume of use. Therefore, silicon as a substrate material is preferred, mostly for reasons of cost effectiveness. Silicon wafers are attractive because they can be purchased in diameters as big as 12 inches and are compatible with the current CMOS industry, making them affordable for use in commercial power and RF applications. But because Si has a small bandgap, it has a high concentration of intrinsic carriers, which makes it have a low resistivity. The thermal conductivity of Si (150 W/mK) is higher than that of sapphire and equivalent to that of bulk GaN, although it is still lower than that of SiC (400 W/mK). However, there are a few problems connected with GaN development on silicon, such as a 17% lattice mismatch to GaN and a 56% coefficient of thermal expansion (CTE) mismatch [61]. This makes growing GaN on silicon more difficult, with the grown epi-layers having the greatest defect concentrations of the wafer choices. Transition layers are required in addition of the nucleation layer to compensate for mismatches, making the epi-structure challenging to grow. Additionally, silicon has a worse electrical isolation than SiC (10^4 cm vs. 10^{11} cm), which results in lossy high-frequency RF transmission lines manufactured from silicon wafers.

2.4.1.2 Sapphire

Sapphire (Al_2O_3) is a promising material because of the low cost of 4-6 inch diameter substrates. Due to its low cost, excellent thermal stability, and high electrical resistivity, sapphire (Al_2O_3) has typically been used for GaN development in solid-state lighting applications. However, sapphire is less suited for high power HEMTs because to its poor thermal conductivity (35 W/mK)) and substantial lattice mismatch (13.9%) with GaN. In comparison to GaN epi-layers grown on silicon, GaN epilayer grown on sapphire have lower defect concentrations [62].

2.4.1.3 Silicon Carbide (SiC)

These substrates are more costly to produce than other materials. Due to its superior thermal conductivity (400 W/mK) and the low 3.1% lattice mismatch between SiC and GaN, it is the most desirable substrate. SiC is the most widely utilized substrate available on the market AlGaN/GaN HEMTs for RF applications. As AlGaN/GaN HEMTs disperse heat more effectively than other conventional substrates, this is especially helpful for high-power applications [63].

2.4.1.4 GaN substrate

GaN substrates are just recently accessible in n-conducting and semi-insulating forms with diameters suitable for electronic device fabrication, i.e., 2-inch size. The benefit of a native GaN wafer is that there is no lattice mismatch to GaN epi-layers, allowing for low defect density epitaxial layers. Also, the nucleation layer between the GaN buffer growth on the GaN substrate is not required, which removes the additional thermal boundary resistance between them. This is a significant improvement above the defect density of 10^8-10^9 cm^{-2} seen in GaN grown on foreign substrates. The availability of freestanding GaN substrates is crucial for GaN-based laser diodes since there performance is highly dependent on defect density [35] [64].

2.4.1.5 CVD Diamond

The chemical vapour deposition (CVD) technique is one of the most common and commercially feasible technique of diamond synthesis. Among the substrate options, CVD diamond has the maximum thermal conductivity of 2000 W/mK. It can help minimize the channel temperature of GaN HEMTs when employed as a substrate. However, the thermal and lattice mismatch between diamond and GaN is large (11.9%), making it difficult to grow GaN on diamond and limiting its benefit. A novel method for realizing GaN on diamond is to first grow GaN on a foreign substrate, usually silicon. The GaN epitaxial structure is then atomically bonded to a diamond substrate and then the foreign substrate is later removed from the back. GaN on diamond devices has been made possible by this method, and they could produce three times the power densities of GaN on SiC. Diamond is however the most expensive of the available wafer types [65] [66].

2.5 GaN-based HEMT epitaxial layer structure

The role of each epitaxial layer in the GaN HEMT structure is explained below:

2.5.1.1 Nucleation layer

Growth of GaN HEMT epitaxial layers on a foreign substrate starts with a thin layer of AlN, typically 20–200 nm thick. This layer initiates the growth process and minimizes the substrate's and buffer layer's lattice mismatch.

2.5.1.2 Back barrier layer

The back barrier layer is a thin layer of high bandgap material, such as aluminum gallium nitride (AlGaN), that is added to the back of the GaN layer. A thick and low Al concentration ($x < 0.15$) $Al_xGa_{1-x}N$ layer (1 to 2 µm) can be utilized. It helps to reduce leakage current in the buffer layer. The back barrier layer also helps to increase the breakdown voltage. Additionally, it can enhance the confinement of the electrons in the channel region, which increases the breakdown voltage [67] .

2.5.1.3 Buffer layer

The band gap of the GaN channel layer is smaller (3.4 eV) than that of the barrier layer (4 eV for AlGaN with 25% Al content). The 2DEG is formed by the difference in band gap energy between the GaN channel and the barrier layer. Typically, the thickness of buffer layer is GaN (2 to 3 µm) is employed to ensure strain relaxation. Higher resistivity is required in the buffer layer to increase electron confinement and

lower vertical leakage currents. C and Fe are the two acceptors that are most frequently used in doping the buffer in GaN HEMT heterostructures [68][69] .

2.5.1.4 Spacer layer

A 1-2nm thin AlN spacer layer is grown on top of the GaN buffer or channel layer. This helps to reduce the amount of strain and defects in the device layers, which can affect device performance and reliability. In addition to its lattice-matching properties, the AlN spacer layer also provides electrical isolation between the different layers of the device, which is important for reducing leakage currents and improving device efficiency. The spacer layer also reduce the scattering of moving electrons in the 2DEG channel by the alloy (AlGaN) and improves the concentration of carriers in the 2DEG. However, this layer stops the best Ohmic contacts from forming, which lowers the source/drain access resistance [70] .

2.5.1.5 Barrier layer

An AlGaN (aluminum gallium nitride) barrier layer is a thin layer of AlGaN (10-25nm). The AlGaN barrier layer is typically grown on top of the GaN channel layer in a HEMT structure. The primary function of the AlGaN barrier layer in a HEMT structure is to control the electron density and mobility in the 2DEG channel. The AlGaN barrier layer has a wider bandgap than the GaN channel layer. The electron density in the 2DEG channel increases with the bandgap size. The composition of the AlGaN barrier layer can be adjusted by varying the aluminum and gallium content, which affects the bandgap and other properties of the layer. For example, a higher aluminum content in the AlGaN barrier layer can increase the potential barrier and reduce leakage current but may also reduce the electron mobility in the device. The most popular barrier layer are AlGaN [71] and AlN [72] [73].

2.5.1.6 Cap layer

A very thin typical GaN layer (1 to 2 nm) is grown on top of the barrier layer to complete the epitaxial structure. It offers several advantages, such as blocking the barrier from relaxing, which decreases the gate leakage current as it raises the barrier height. It also offers surface passivation, which minimizes oxidation and enhances the density of 2DEG [74]. The GaN cap also has low bandgap energy and helps to reduce the Ohmic contact resistance [75].

2.6 Depletion mode GaN HEMT device: operation principle

The AlGaN/GaN HEMT has three terminals (source, gate, and drain), with the source and drain terminals being Ohmic contacts and the gate terminal having a Schottky contact. The gate terminal is usually positioned closer to the source side in order to lower the strong electric fields between the drain and the gate that develop at high drain voltages. This raises the HEMTs' lateral breakdown voltage and

lowers internal self-heating. Figure 2.7 (a) and (b) depict the cross-section of an AlGaN/GaN HEMT and its functioning under ON-state and OFF-state situations, respectively.

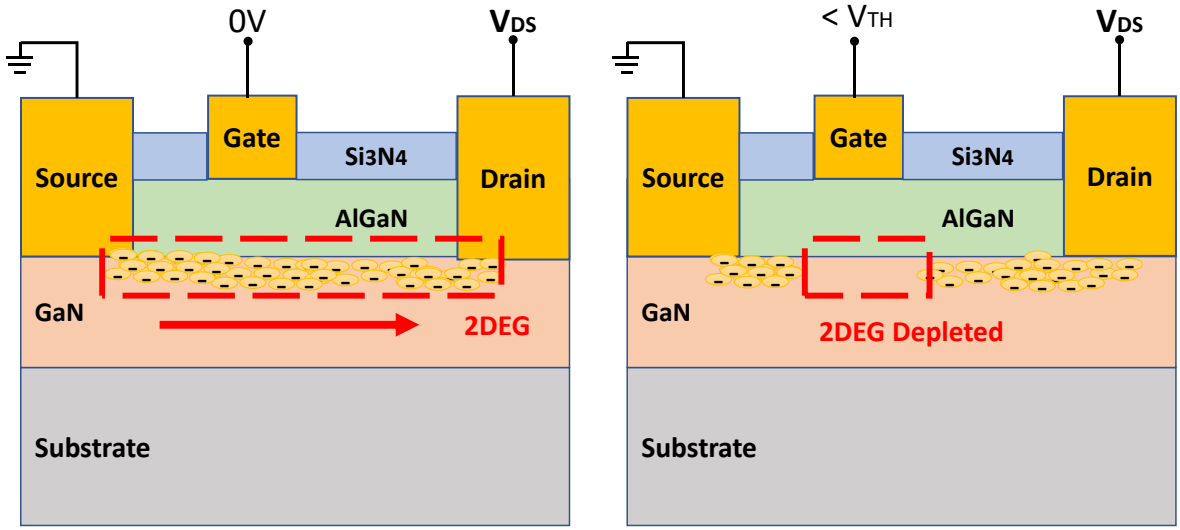


Figure 2.7: Illustration of a HEMT operation principle and biasing (a) ON-state and (b) OFF-state with an AlGaN/GaN heterostructure and Si_3N_4 passivation.

Due to the polarisation effect in the GaN HEMT structure, the device operates in the depletion mode or as a normally-on transistor. Giving a negative bias on the gate makes the 2DEG channel to deplete (in proportion to the applied voltage). The (gate) threshold voltage, V_{TH}, is the bias that just empties the channel of electrons so that no current can flow between the source and drain contacts and the device is turned off. For increasing gate bias above V_{TH}, the electron density in the 2DEG also increases and current can flow between the source and the drain if a bias voltage is applied between them. For a Schottky gate, there is a limit of +1 V after which it turns on, starts conducting, and no longer controls the 2DEG concentration or the drain source current. When the channel is completely depleted, the sheet carrier density can range from a maximum of n_{s0} to a minimum of zero, depending on how the gate bias is set. The devices utilized in this thesis are depletion mode or normally-ON, and the 2DEG is formed without supplying a voltage to the gate terminal (V_{GS}). V_{GS}, which controls the 2DEG sheet density in the channel, regulates the transition from ON-state ($V_{GS} > V_{TH}$) to OFF-state ($V_{GS} < V_{TH}$). In the OFF-state condition, when V_{GS} is less than V_{TH}, the 2DEG will deplete and thus block current flow through the device.

Figure 2.8 depicts the vertical conduction band edge profile at the middle gate of an AlGaN/GaN HEMT in the (a) ON-state and (b) OFF-state. V_{GS} has an impact on how close together the conduction band edge and the Fermi level (EF) are. When positive, this reduces the conduction band energy in relation to EF and increases the 2DEG. By using $V_{GS} < V_{TH}$, the conduction band energy must be increased above EF to close the channel.

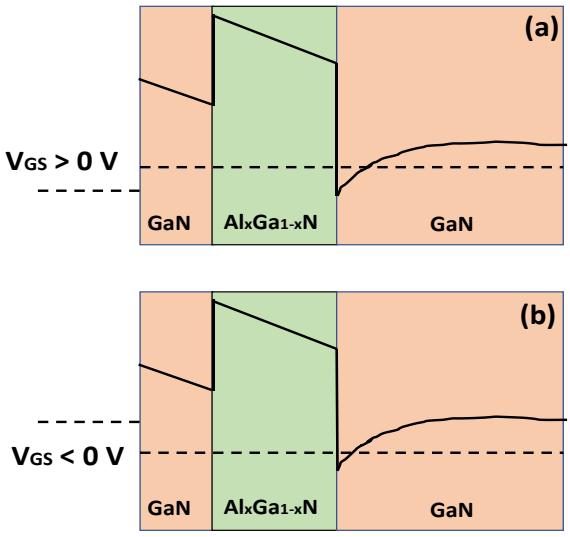


Figure 2.8: Gate voltage effects on the energy band structure: a) $V_{GS} > V_{TH}$ and b) $V_{GS} < V_{TH}$.

A HEMT's primary function is to switch electronic signals or to amplify them (either alone or as a component of a larger amplifier circuit). Current flowing between the source and drain can be calculated in the planar area by measuring the charge in the channel and the time it takes for that charge to cross the channel in response to an applied voltage (electric field). The following equation provides the drain-source current [10]:

$$I_{DS} = \frac{qn_s L_{DS} W_G}{\frac{L_{DS}}{v_{eff}}} \tag{2.6}$$

$$= qn_s v_{eff} W_G \tag{2.7}$$

where v_{eff} is the effective velocity of the electrons in the channel, q is the electron charge, n_s is the sheet carrier concentration, and W_G is the gate width. The applied electric field, E, and the mobility of the electrons in the channel, μ_n, can be used to calculate the electrons velocity, which can be written as follows:

$$v_{eff} = \mu_n E = \mu_n \frac{V_{DS}}{L_{DS}} \tag{2.8}$$

where, L_{DS} is the separation between the drain and source Ohmic contacts and V_{DS} is the voltage applied between those two contacts.

The gate metal and 2DEG channel can be regarded as a capacitor which means that n_s can be written as:

$$n_s = \frac{\epsilon_{AlGaN}}{q(d_{AlGaN} + \Delta d)} (V_G - V_T) \quad (2.9)$$

where d_{AlGaN} is the thickness of the AlGaN barrier layer, V_G is the gate bias voltage, and Δd is the effective distance of the 2DEG from the heterointerface.

The typical current voltage (I-V) characteristic of a GaN HEMT is illustrated in Figure 2.9. When the gate voltage exceeds the threshold voltage, the drain current grows linearly at first and then saturates as the drain bias voltage increases. Increasing the gate voltage causes more electrons to accumulate in the 2DEG channel and so increasing the drain current with applied V_{DS}.

The transconductance of the device can be defined as follows:

$$g_m = \frac{\delta I_{DS}}{\delta V_G} \quad (2.10)$$

where δI_{DS} is change in drain current and δV_G is change in gate voltage.

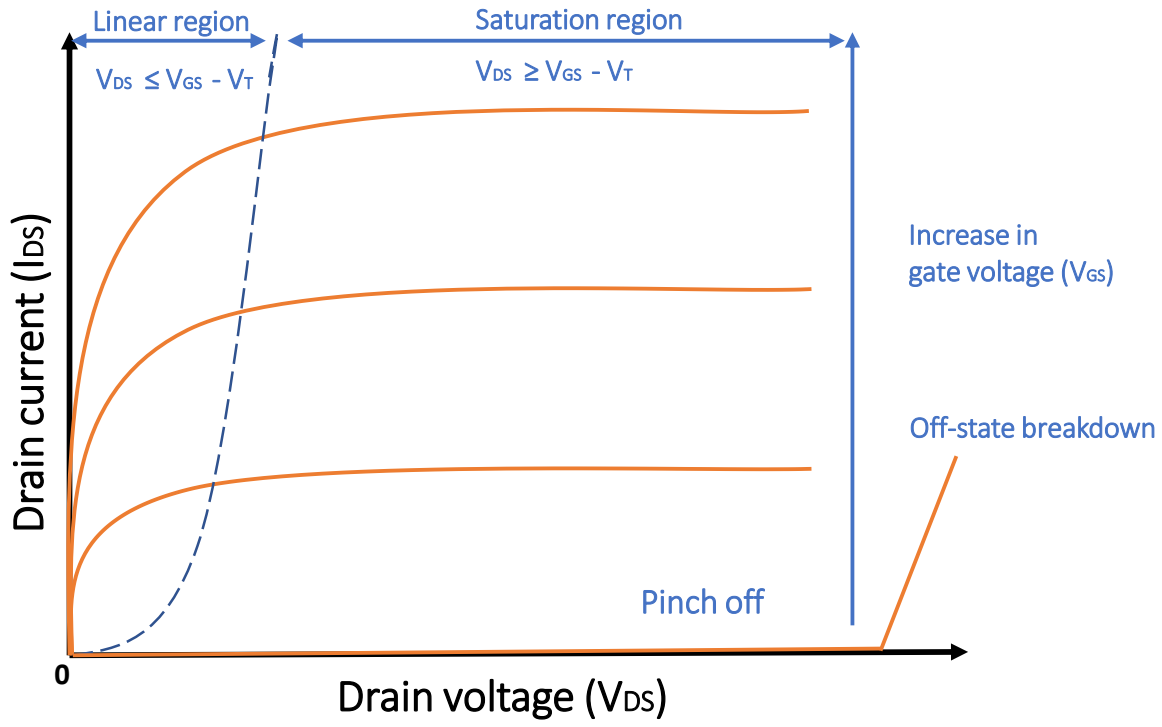


Figure 2.9: Output DC- IV characteristic of a typical GaN HEMT.

2.7 Enhancement mode GaN HEMTs

Opportunities for enhancing both RF GaN devices and power GaN devices extend beyond addressing self-heating and current collapse issues. In the realm of power GaN technology, additional challenges exist, including the inherent depletion mode or normally-On behaviour of AlGaN/GaN based devices. It's important to note that this concern pertains exclusively to power devices, as normally-On device operation is favoured in radio frequency (RF) applications.

In power devices, achieving a Normally-Off behaviour, also referred to as enhancement or e-mode operation, is highly desirable. This characteristic is crucial for safety reasons, ensuring fail-safe circuits that cut off the high voltage supply unless prompted by the gate control voltage. Furthermore, Normally-Off behaviour significantly enhances performance by minimizing leakage current, simplifying circuit layout, bolstering device stability, and improving efficiency. The advantage lies in the fact that e-mode devices don't require additional power to deactivate. When the gate voltage is zero, a Normally-Off GaN HEMT has an intentional p-type doping layer in its AlGaN barrier, resulting in a depletion area. A positive gate voltage attracts holes to the surface, resulting in the formation of an accumulation layer and a conducting channel that allows current to pass. When the gate voltage is removed, the accumulation layer is depleted, and the device is turned off.

Various strategies have been explored to attain e-mode devices, as depicted in Figure 2.10. These range from to diverse iterations involving p-type layers a top GaN HEMTs [76] [77], deep gate recessing [78], and adaptations involving gate oxide, known as MIS-HEMTs and the original 'fluoride gate' HEMTs [79], where fluoride ions were implanted beneath the gate, An alternative approach involves employing TiN gate structures, which have demonstrated remarkably low leakage currents.

In summary, there is substantial room for improvement in both RF GaN and power GaN devices. While challenges like self-heating and current collapse are recognized, the normally-On behaviour of power devices and the quest for Normally-Off behaviour, especially in power applications, are pivotal concerns. Diverse methods have been pursued to achieve this, ranging from fluoride-based techniques to novel gate structures like TiN, all with the goal of enhancing device functionality and efficiency.

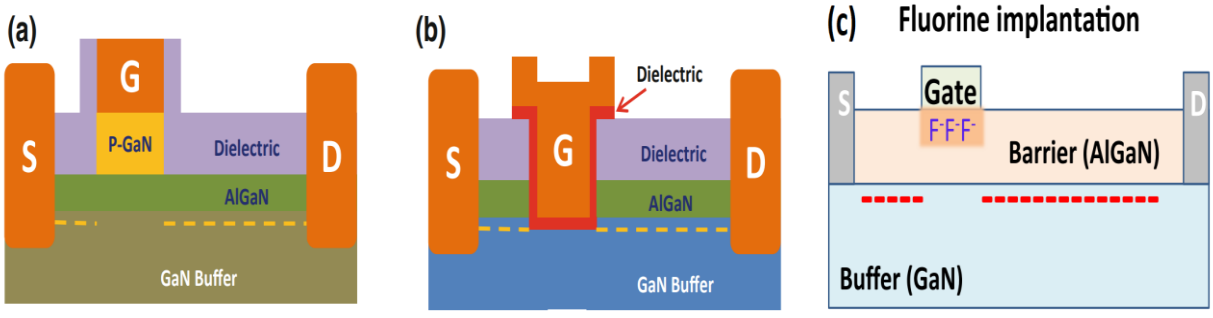


Figure 2.10 Illustration of the three types of e-mode GaN HEMTs a) with p doped layer under the gate, b) deep recessed gate with insulator under the gate and c) fluoride treated region under the gate [76].

2.8 HEMT RF Behaviour

The evaluation of the HEMTs' small-signal characteristics is typically done by measuring the scattering parameters (S-parameters) at the input and output end terminals. The input port corresponds to the gate source in the case where the HEMT is driven in the common source mode configuration, while the output end corresponds to the drain source. Figure 2.11 shows the two-port network S-parameters.

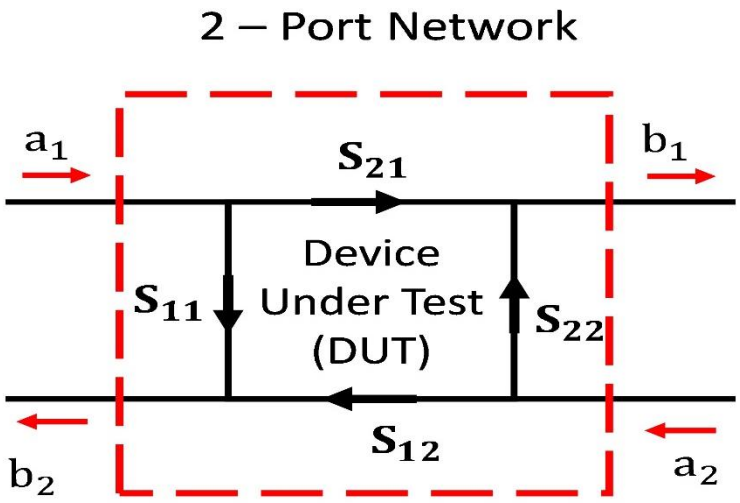


Figure 2.11: Diagram of the two-port idea for device characterisation.

Equation 2-11 shows the relationship between the input and output power waves of the two-port component.

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \end{bmatrix} \qquad (2.11)$$

The reflection coefficients are denoted by S_{11} and S_{22}. The transmission coefficients are denoted by S_{12} and S_{21}. S-parameters are usually measured over a wide frequency range in order to be able to fully characterize the devices. A vector network analyser (VNA) is used to measure the scattering or S-parameters of the transistor at any given bias point. The S-parameters may be used to calculate the input and output impedance of a transistor under any loading conditions. They are specifically used for the design of input and output matching networks. For these measurements, the reference impedance is generally 50 Ω. Prior to use, the VNA must be calibrated so that the reference measurement points are at the probe tips that make contact with the transistor pads (see Figure 2.12). The S-parameter can be used to calculate the H-parameter which then can be used to obtain f_T. Based on the measured S-parameters, the following figures of merit can be computed:

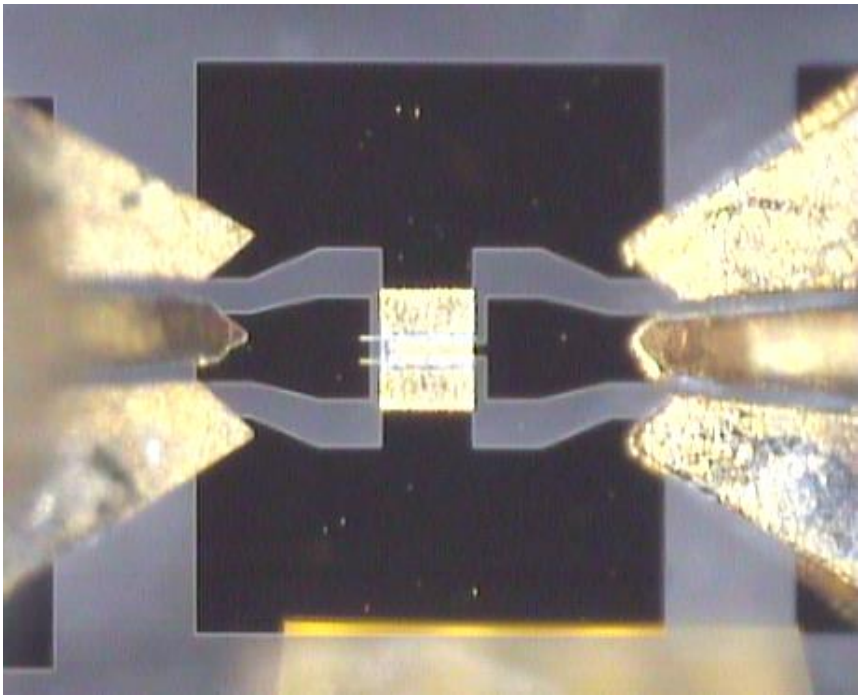


Figure 2.12: Micrograph of a fabricated GaN HEMT with landed RF ground-signal-ground probes on device RF ports.

- **Current gain cut-off frequency f_{T}**

The frequency at which the current gain $\frac{\mathrm{I_{out}}}{\mathrm{I_{In}}} = \frac{\mathrm{I_d}}{\mathrm{I_g}}$ falls to unity is called f_{T}.

$$f_{\mathrm{T}}: h_{21}(f_{\mathrm{T}}) = 1 \tag{2.12}$$

$$h_{21} = \frac{-2S_{21}}{(1 - S_{21})(1 + S_{22}) + S_{12}S_{21}} \tag{2.13}$$

- **Maximum frequency of oscillation f_{max}**

The point at which the power gain (G_p) of the device reaches unity is commonly referred to as f_{MAX}. The parameter G_p is defined as the ratio of the power delivered to the load to the power input to the HEMT. This value is determined by multiplying the gains in current and voltage ($G_p = G_i . G_v$). The computation of f_{MAX} is a more complex process. Prior to obtaining f_{MAX}, it is necessary to acquire the First Maximum Stable Gain (MSG) and Maximum Available Gain (MAG). The region denoted as MSG is characterized by values of stability factor (K) that are less than 1, while the region referred to as MAG is associated with values of K that are greater than 1. Rollet's stability factor is represented by the symbol K. A system is

considered conditionally stable if its K-factor exceeds one. In such cases, designers must employ a more rigorous procedure in amplifier design to ensure its stability. Conversely, if the K-factor is less than one, the system is deemed unconditionally stable, and amplify design is straightforward in this case [80].

$$f_{\mathrm{MAX}}: G_{\mathrm{P}}(f_{\mathrm{MAX}}) = 1 \tag{2.14}$$

$$G_{\mathrm{P}} = \frac{\left|\frac{S_{21}}{S_{12}} - 1\right|^2}{2\left[K\left|\frac{S_{21}}{S_{12}}\right| - Re\left(\frac{S_{21}}{S_{12}}\right)\right]} \tag{2.15}$$

MSG: $$\frac{|S_{21}|}{|S_{12}|} \tag{2.16}$$

MAG: $$\frac{S_{21}}{S_{12}}\left[K + (K^2 - 1)^{\frac{1}{2}}\right] \tag{2.17}$$

where K is called the stability factor which determines the stability of the devices, and expressed as:

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} \tag{2.18}$$

where $\Delta = S_{11}S_{22} - S_{12}S_{21}$. An unconditionally stable HEMT must meet the requirement of K > 1 and $|\Delta| < 1$.

2.8.1 Small signal Equivalent Circuit Model

In designing monolithic microwave integrated circuits (MMIC), the equivalent circuit model of the device is crucial [81]. This is a representation of the device's electrical properties, with each circuit element describing the electrical properties of a particular area of the device. The values of the circuit element based on S-parameters that were observed at a specific bias point, (V_{DS}, V_{GS}). Figure 2.13 depicts the intrinsic and external region of the small-signal equivalent circuit equivalent circuit model that captures the electrical characteristics of the HEMT physical structure at mm-wave frequencies [82]. The intrinsic elements of a transistor show how it works, whereas the extrinsic elements of a device represent its parasitic elements. The efficacy of RF devices is significantly impacted by the parasitic elements, which are primarily determined by the device geometry and layout design.

Gate-source capacitance (C_{gs}) and gate-drain capacitance (C_{gd}) are two elements that model the charge in the depletion region beneath the gate and towards the source and drain sides, respectively. C_{gd} affects the transistor's high-frequency performance and can lead to unwanted Miller effect, reducing the device's

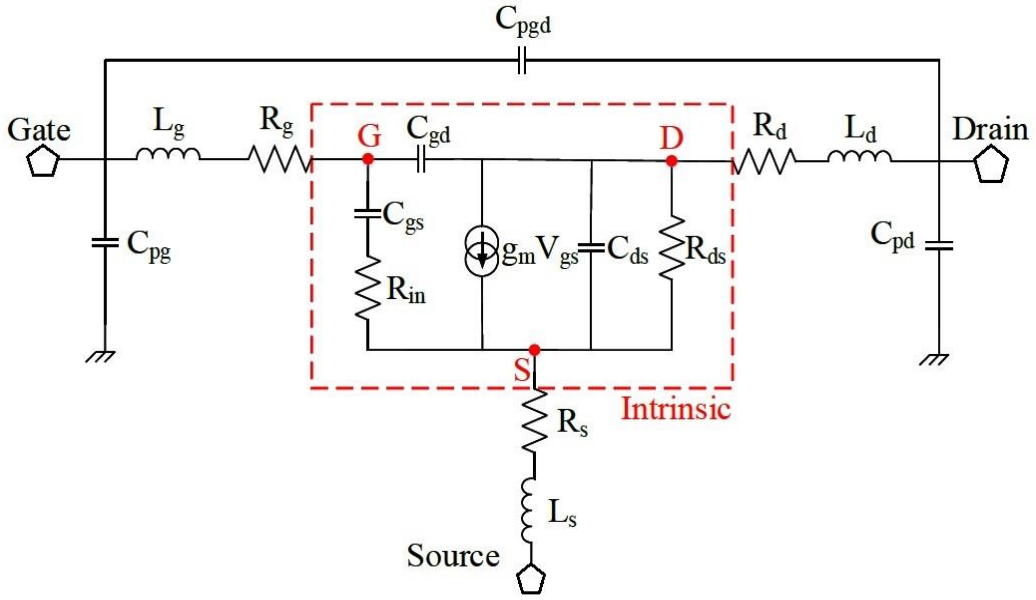


Figure 2.13: Small-signal equivalent circuit model of HEMT.

bandwidth and potentially causing stability issues in amplifier designs. The charging resistance is the input resistance (R_{in}). The current generator g_mV_{gs} provides information about transistor gain. Source drain resistance, R_{ds}, is used to indicate the device's finite output resistance. It is a linear parameter that is largely used in DC and low-frequency small-signal analysis. The series parasitic source resistance (R_s) and drain resistance (R_d) account for the source/drain Ohmic contacts and bulk resistance preceding the active channel [83]. Equation 2.19 can be used to determine the gate resistance (R_g), which results from the metallization resistance of the Schottky contact.

$$R_g = \frac{\rho W_G}{3n^2 h_G L_G} \tag{2.19}$$

where is the ρ resistivity of the gate metal. The gate length, breadth, and height are L_G, W_G, and h_G, accordingly.

Output conductance (g_{ds}) is the ratio of the output current to the output voltage, and it represents the loss in the device. A lower output conductance means less loss, which is also desirable for high frequency operation. Gate capacitance (C_{gs}), This is the capacitance between the gate and the source, and it represents the amount of charge that needs to be accumulated on the gate to turn on the device. A lower gate capacitance means faster switching, which is desirable for high frequency operation. Source capacitance (C_{gd}), This is the capacitance between the gate and the drain, and it represents the amount of charge that is stored in the channel when the device is turned on. A lower source capacitance means less charge storage, which is also desirable for high frequency operations [84].

The gate, source, and drain parasitic inductances, respectively, model the metal contact pads. The parasitic capacitances C_{pg}, C_{pg}, and C_{pgd} in the HEMT reflect the electrical field variations between the metal contacts. These capacitances are also primarily considered in the small-signal region and are linear parameters. These capacitances are geometrically dependent on the design layout of the transistor. While the internal resistance and capacitances are linear parameters in small-signal analysis, it's important to remember that GaN HEMTs can exhibit non-linear behavior under large-signal and high-frequency conditions. When analyzing the transistor's performance in those regions, additional non-linear parameters, such as third-order intercept point (IP_3), output power compression (P_1dB), and intermodulation distortion (IMD), become important for understanding the device's linearity and distortion characteristics [85].

The definitions of f_T and f_{MAX} in Section 2.7 can also be used to compute f_T and f_{MAX} as a function of the values of the parasitic elements shown in Figure 2.12 [86].

$$f_t = \frac{g_m}{2\pi(c_{gs} + c_{gd})\left(1 + \frac{R_s + R_d}{R_{ds}}\right) + g_m C_{gd}(R_s + R_d)} \tag{2.20}$$

$$f_{max} = \frac{f_t}{2\sqrt{\left(\frac{R_g + R_{in+}R_s}{R_{ds}}\right) + 2\pi f_t R_g C_{gd}}} \tag{2.21}$$

2.9 Summary

This chapter provided the fundamentals of GaN HEMT theory, from basic physics through substrate alternatives, epi-layer growth, and design. The spontaneous and piezoelectric polarisations have been discussed, as well as their function in the formation of the 2DEG channel. The HEMT structure operates in depletion mode. The advantage of GaN HEMTs originates from its ability to create heterostructures to larger band gap materials, resulting in 2DEG channels with high electron densities and mobilities. This chapter also discussed the substrate selection. Because native GaN substrates were not accessible until recently, GaN is grown on foreign substrates, the most common of which being SiC, silicon, and sapphire. SiC is the costliest material, yet it has the least lattice misfit and the highest thermal conductivity and so is the choice substrate for high power and high frequency applications.

Chapter 3

GaN HEMT Device Fabrication Techniques

3 GaN HEMT Device Fabrication Techniques

3.1 Introduction

This chapter describes the processing techniques for the fabrication of AlGaN/GaN HEMTs on GaN-on-SiC substrates. The different processes include sample preparation, lithography, metallization, etching, mesa isolation and dielectric layer deposition. All the processing is performed in the James Watt Nanofabrication Centre (JWNC), University of Glasgow. Although epitaxial growth of wafers occurs outside of the University of Glasgow, a brief introduction to the common processes is provided.

3.2 Epitaxial material growth

Epitaxy is a process of growing a crystalline material on top of a substrate with a matching crystal structure. The growth conditions such as temperature, pressure, gas flow rate, and precursor concentration are carefully controlled to achieve the desired crystal quality and thickness. These conditions depend on the specific material being grown and the desired application of the final growth material. The most commonly used techniques for GaN epitaxial growth are metal-organic chemical vapor deposition (MOCVD) [87] [88] and molecular beam epitaxy (MBE) [89][90]. MOCVD is a popular method because it allows for the growth of high-quality epitaxial layers and multiple wafer growth at a same time with good control over the growth rate and composition [91]. MBE, on the other hand, is a more expensive technique but allows for very precise control over the layer thickness and doping. All the wafers used in this thesis were commercially grown by MOCVD growth technique.

3.2.1 Metal Organic Chemical Vapor Deposition

The growth method known as metal organic chemical vapour deposition (MOCVD) uses a dynamic flow in which gaseous reactants move over a heated substrate and chemically react to generate a semiconductor layer. Due to its cheap cost in comparison to other methods MOCVD is the most widely used growth technique in the GaN industry. The average MOCVD growth rates are 1-2 µm/hr, which is roughly twice as rapid as MBE growth. The MOCVD growth temperature is often greater than 1000°C [92][87].

- Reactor setup: The MOCVD reactor consists of a gas inlet system, a substrate holder, a temperature control system, and a gas exhaust system. The reactor is typically operated at a high temperature (700-1100°C) and a low pressure (50-1000 mbar).
- Precursor gases: The precursor gases used for GaN growth in MOCVD are typically trimethylgallium (TMGa), ammonia (NH3), and optionally a dopant gas such as silane (SiH_4) or bis(cyclopentadienyl) magnesium (Cp_2Mg).
- Pre-growth preparation: Before growth, the substrate is cleaned using a sequence of chemical treatments to remove any impurities and ensure a clean surface. The substrate is then loaded into the reactor.
- Buffer layer growth: A thin buffer layer of AlN is typically grown on the substrate before the GaN layer to improve the crystal quality and reduce dislocations. The AlN layer is grown by introducing TMAl and NH3 precursor gases into the reactor.
- GaN epitaxial growth: Once the buffer layer is grown, the reactor is heated to the desired temperature, and the TMGa and NH3 precursor gases are introduced into the reactor in a

controlled manner. The precursor gases react on the substrate surface, causing the GaN layer to grow.

- Doping: During GaN growth, a small amount of dopant gas, such as SiH4 or Cp2Mg, can be introduced to the reactor to alter the electronic properties of the GaN layer.
- Post-growth annealing: After GaN growth, the sample is annealed in situ in the reactor to improve crystal quality and reduce dislocations.

This chemical reaction equation describes a typical gas reaction of GaN growth:

$$TMG + NH_3 \rightarrow GaN + 3CH_4$$

where, TMG is trimethyl gallium, NH_3 is ammonia and CH_4 is methane.
Figure 3.1 shows the MOCVD growth system [93].

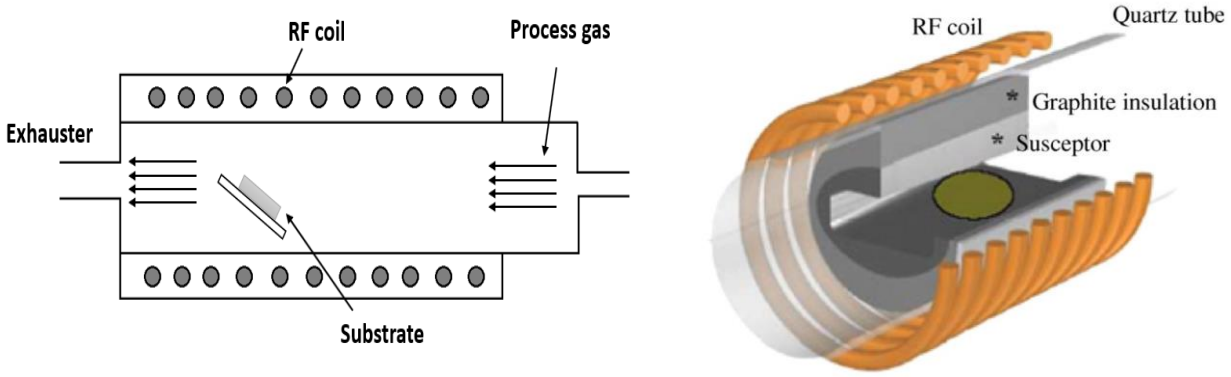


Figure 3.1: Schematic illustrations (a) MOCVD growth chamber (b) In the hot-wall MOCVD growth chamber setup, the substrate is placed in the hot zone. Before entering the growth chamber, all precursors (TMAl/TMGa+NH3) and carrier gases (H2/N2) are mixed together

Improving the growth conditions of the nucleation layer can result in higher quality GaN epitaxial layers. Better electrical and thermal properties would result from higher quality epitaxial layers. Only the wafer carrier, known as a susceptor, is heated to the appropriate growth temperature during the standard cold-wall MOCVD growth process, so no gas reaction occurs before reaching the hot wafer surface. As a result, there are significant temperature variations throughout the growth chamber, particularly in the vertical but also in the horizontal direction. Temperature gradients influence the uniformity of growth rate, doping, and composition. However, in a hot-wall MOCVD growth process, the entire chamber is heated, resulting in superior growth process uniformity due to the low temperature gradients in the chamber. Before entering the hot zone, the gases (H_2/N_2) and precursors (TMAl/TMGa+NH_3) are combined. The processing gases are driven through a hollow-shaped, RF-induction heated graphite susceptor enclosed by an insulator, as illustrated in Figure 3.1, which is a schematic view of the hot-wall MOCVD system. The vertical temperature gradient in the hot-wall MOCVD SiC growth chamber is an order of magnitude less in this design than in the standard cold-wall MOCVD chamber.

3.2.2 Molecular beam epitaxy (MBE)

Molecular Beam Epitaxy (MBE) is a technique used to grow thin films of materials on a substrate with atomic precision. The process involves the use of high-vacuum chambers and molecular beams of the desired material, which are directed towards the substrate surface where they react to form a thin film [94]. The typical growth temperature is 700°C which is lower than the MOCVD growth temperature. The growth rates for GaN material in an MBE system are typically approximately 0.5-1 µm/hr, which is slower than the growth rates achieved using MOCVD. As a result, the MBE approach is more costly. Since MBE is a high-quality material that can be utilized in tests to demonstrate proof of concept, its primary application is in the field of research [95]. The basic MBE system consist of following parts:

- Preparation of substrate: The substrate on which the film will be deposited is first cleaned and prepared by techniques such as chemical etching or annealing to remove any impurities and create a smooth surface. The substrate is then loaded into the MBE chamber.
- Introduction of source materials: The source materials for the desired film are loaded into crucibles or effusion cells, which are heated using resistive heaters or electron beams to create molecular beams of the desired material.
- Formation of molecular beam: The heated material evaporates from the surface of the crucible or effusion cell, and the resulting vapor molecules travel in a straight line towards the substrate surface. The molecular beam is collimated using a series of apertures or slits to ensure that the molecules travel in a straight line towards the substrate.
- Deposition on substrate: The molecular beams of the source materials are directed towards the substrate surface, where they react to form a thin film. The deposition rate and thickness of the film can be controlled by adjusting the temperature and flux of the molecular beams. The substrate is typically rotated during deposition to ensure uniform thickness across the surface.
- In-situ monitoring: During deposition, the properties of the growing film can be monitored using techniques such as Reflection High Energy Electron Diffraction (RHEED) or Laser Reflectometry. RHEED involves directing a beam of high-energy electrons towards the substrate surface and measuring the intensity and pattern of the reflected electrons to determine the crystal structure and growth rate of the film. Laser reflectometry measures the thickness of the film by detecting changes in the intensity of a laser beam reflected off the surface [96].
- Post-growth annealing: After deposition, the film may be annealed at high temperature in the MBE chamber or in a separate furnace to improve the crystalline quality and remove any defects or impurities.

Figure 3.2 shows the MBE growth system [97].

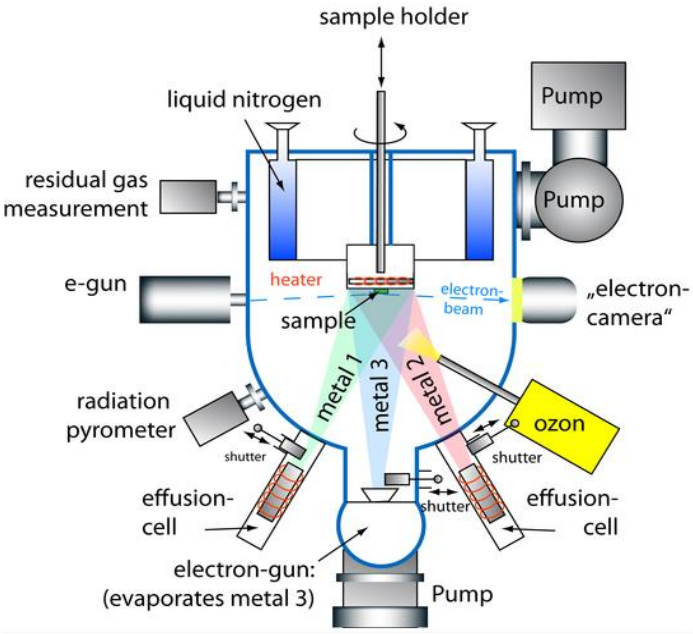


Figure 3.2: Schematic illustration of an MBE growth chamber.

3.3 Lithography

The process of lithography, which involves transferring patterns on the substrate, is an essential part of the production process for electronic devices. The fabrication of semiconductor devices involves nanoscale and microscale sizes. Optical lithography and e-beam lithography are the two primary forms of lithography. Photolithography is a reasonably quick procedure that has an alignment precision of 1 µm. E-beam lithography, on the other hand, has an alignment precision of 0.5 nm, it may be used to make submicron features that are as small as 1 nm. However, the process is rather slow, costly, and complicated, and it involves a lot of different processing stages.

3.3.1 Photolithography

The most popular method of producing semiconductor devices is photolithography, commonly referred to as optical lithography, since it can satisfy consumer demands for high throughput and small feature sizes. The hard chrome mask is used for photolithography to pattern transfer. A hard chrome mask is usually manufactured using electron beam lithography. The James Watt Nanofabrication Center (JWNC) uses a Karl Suss MA6 mask aligner with a minimum feature size of 1 µm for photolithography procedures. In order to fulfil market demand, optical lithography's fast throughput lowers the cost per unit of manufactured devices. Since photolithography is more affordable and quicker than electron-beam lithography, it was used for all process optimization work on this project. With photolithography, a wafer coated in photoresist is exposed using ultraviolet (UV) light. Figure 3.3 shows the Karl Suss mask aligner 6.

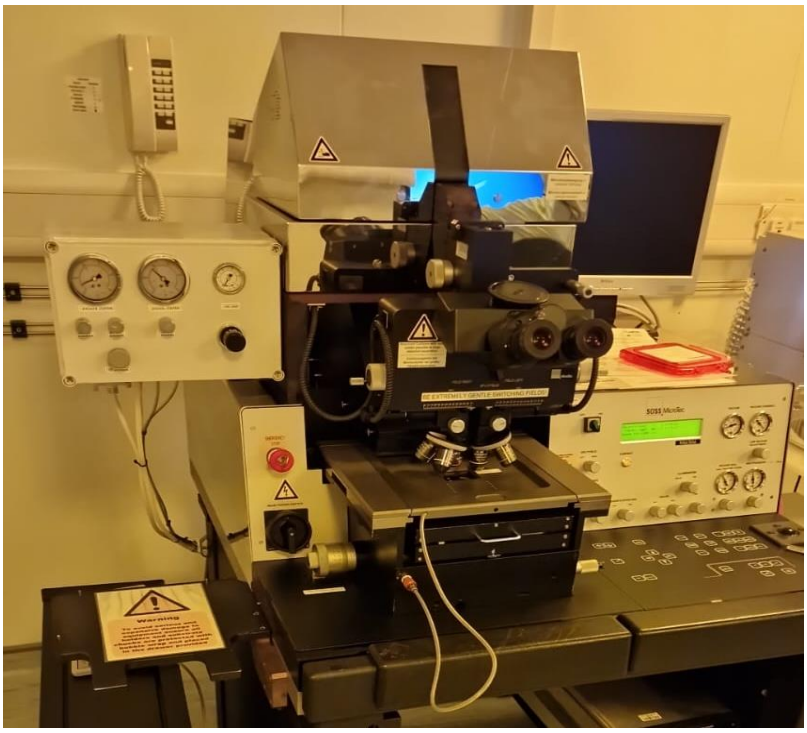


Figure 3.3: Photo of the Karl Suss Mask Aligner (MA6).

3.3.2 Electron beam lithography

Patterns are transferred onto the substrate via the method of electron beam lithography using e-beam resists, which are polymers. By transferring the pattern to the e-beam lithography tool and moving the electron gun over the wafer, electron beam lithography provides submicron pattern transfer directly to the wafer without the use of a mask plate. The ability to choose several exposure levels during a single exposure is another benefit of e-beam lithography. As a result, different dosages can be chosen for various patterned areas of the sample, such as the sample's corners, where the resist coatings are often thicker. The energy distribution arising from primary and dispersed electrons can be represented as a combination of Gaussian distributions using the 3-D Proximity Effect correction approach. In electron beam lithography (EBL), the proximity effect arises from interactions between primary beam electrons, resist, and substrate. This widens the exposure dose distribution beyond the scanned pattern, causing blurring but also enabling unique feature creation. EBL's proximity effect offers advantages like high aspect ratios (up to 100:1) by leveraging scattered electrons from sidewalls to enhance exposure at pattern bottoms. Moreover, it allows for small feature sizes (<10 nanometers) by similarly utilizing sidewall-scattered electrons, enabling capabilities beyond conventional lithography [98]. These distributions combine to generate the proximity function, which aids in determining the proper foot and head doses required to accomplish the desired structure. This method is especially useful in high-density areas, such as gate feeds, or when the gate pitch is tiny. These inputs, along with the correction procedure, were used to simulate the resist cross-section post-development using the GenIsys LAB modelling software. Additionally, this method offers great

alignment precision of 0.5 nm, ultra-high resolution, and precisely regulated operation. The main problem with electron beam lithography is that it can take a few hours to draw a pattern that could be exposed in a few seconds with photolithography. Still, electron-beam lithography is still used in a lot of places where research is done. This is because the design files are digital, and CAD software makes it easy to change designs. With optical lithography, on the other hand, a hard mask has to be made every time the design needs to be changed. In this work, the Raith EBPG5200 HS e-beam tool was used. Figures 3.4 and 3.5 depicts the component of the instrument that generates the electron beam for pattern exposing/writing.

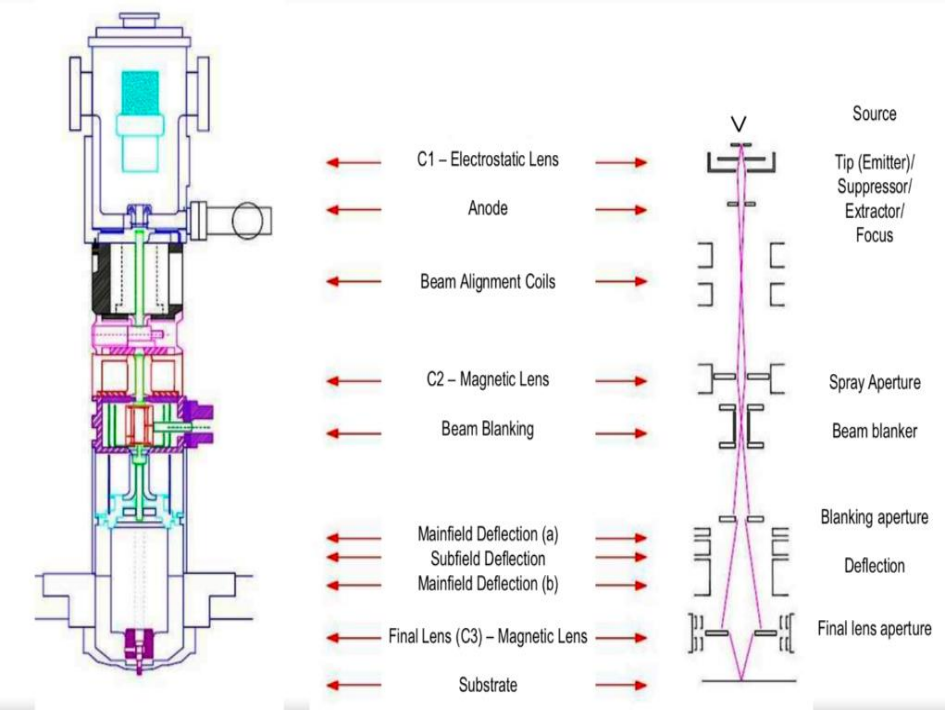


Figure 3.5: Schematic illustration of the column of an electron beam lithography tool.

Figure 3.4: Photo of the electron beam lithography tool Raith EBPG5200 HS.

3.3.3 Photoresists

A polymer that is sensitive to ultraviolet (UV) light is called photoresist. Spinning is used to apply it evenly to the wafer surface. Acceleration, spin speed, and time controls can be used to modify the resist's thickness. Positive and negative photoresists are both available. Positive photoresists clear during the development stage because the polymer bonds in the radiation-exposed areas breaks. As a result, during the development stage, the exposed parts dissolve away while the unexposed areas remain intact. Figure 3.6 serves as an example of the exposure and development of positive photoresist.

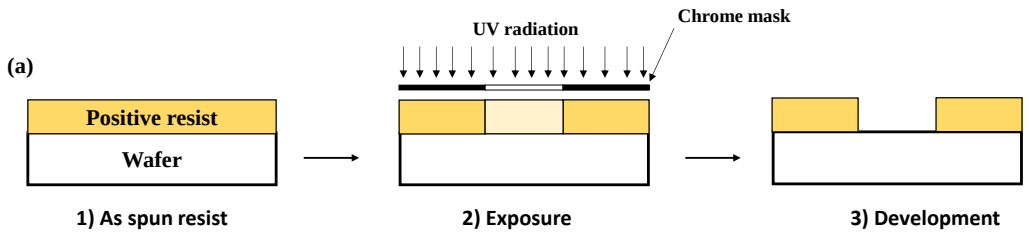


Figure 3.6: Positive photoresist spinning, exposure and development.

Using a lift-off procedure is one method for creating a metal pattern on a semiconductor surface. It is a method that makes use of photoresist, and windows are opened in the photoresist at the locations where the presence of metal is needed. Using UV exposure, the windows are opened. The exposed semiconductor regions and the photo-resist surface are subsequently blanketed with metal during the subsequent deposition process. The metal covering the photoresist is removed once it has been dissolved using a solvent like acetone. The metal that was deposited in the exposed windows remains on the semiconductor surface. In order for the lift-off procedure to be successful, the photoresist must have an undercut that separates the metal on its surface from the metal on the semiconductor. A lift-off method in photolithography can utilise a single layer photoresist (S1818 or S1805). This is exposed to a developer (MF319 developer) before the UV exposure stage to harden the surface and make it less sensitive to the developer solution. This causes the lowest part of the resist to develop more quickly. The single layer resist lift-off procedure is shown in Figure 3.7 (a).

Another way to get the undercut profile is to use a combination of two different photoresists. For this project, LOR10A and S1818 photoresists were used together. A bilayer photoresist process flow is shown in Figure 3.7 (b). The photoresist has an undercut profile so the resist stripper may access the resist under the metal and remove it together with the excess metal. Similarly, to get these undercut profiles in electron-beam resists, a tri-layer is used in which the lower resist layer has a lower molecular weight than the upper layer. This makes the lower layer more sensitive to radiation, so it gets developed faster than the upper layer. The tri layer resist lift-off procedure is shown in Figure 3.7 (c).

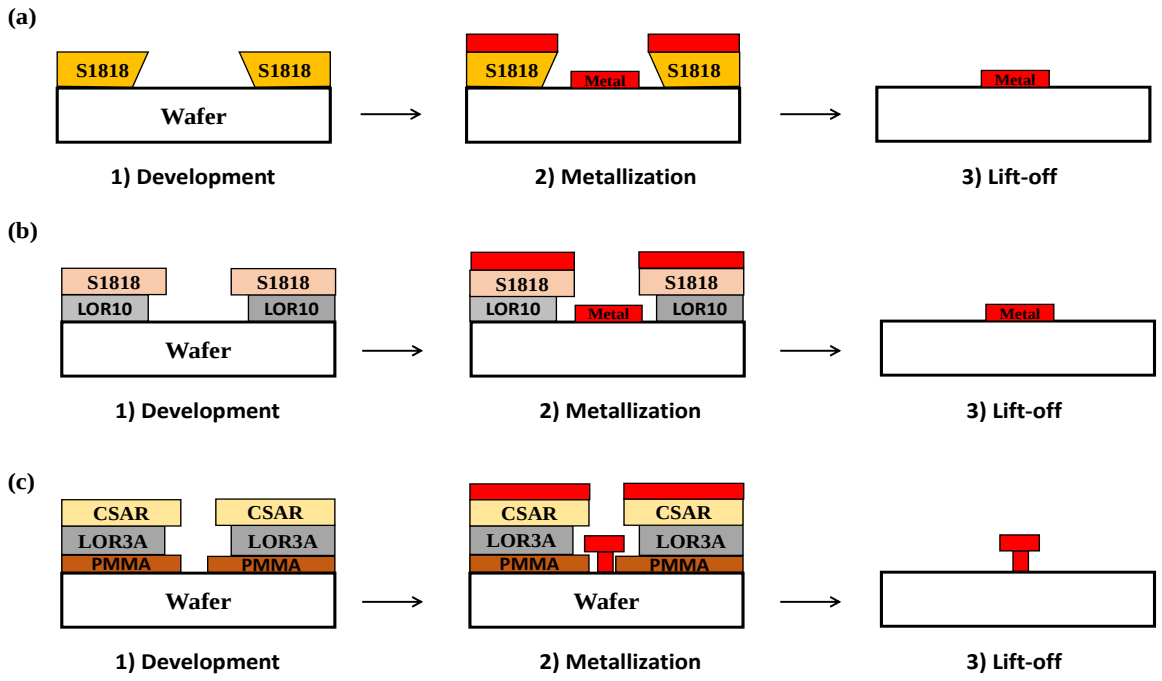


Figure 3.7: The metal lift-off process flow using (a) a single layer photoresist (b) a bi-layer od photoresist (c) a tri-layer of photoresist.

Various types of resists were used for the fabrication in this research, and these are outlined in Table 3- 1.

Table 3-1: Resists used in this research work for various applications.

Resist	Type	Application
PMMA	Positive	E-beam lithography
S1805/S1818	Positive	Dry etch mask
CSAR	Positive	Multilayer system for T-gates
LOR	Positive	Undercut for T-gates (better lift-off)

3.4 Metallization

Metal is required for making the electrical connections from semiconductors to the outside world, and so establishing metal contacts to semiconductors is a crucial step in the construction of devices. Metal may

be deposited on semiconductor surfaces using a number of different methods. Electroplating, sputtering, and electron beam evaporation. In this research, electron beam evaporation method used.

3.4.1 Electron beam metal evaporation

An electron beam metal evaporator is a type of vacuum deposition system that uses an electron beam to vaporize a metal source material and deposit a thin metal film onto a substrate. This metal crucible is water-cooled such that only the surface where the electron beam is focused evaporates. The system typically consists of a vacuum chamber, an electron beam gun, a metal source, and a substrate holder. Plassys MEB 550S (also known as Plassys II) and Plassys MEB 450 (further referred as Plassys IV) are the tools utilised in this research work for metal evaporation. A picture of Plassys IV is shown in Figure 3.8. Details of the electron beam metal evaporator tool are as follows:

- Electron beam gun: The electron beam gun is the key component of the evaporator. It generates an electron beam that is used to vaporize the metal source material. The gun typically consists of a cathode, an anode, and a magnetic focusing system that directs the electron beam towards the metal source.
- Metal source: The metal source is typically a rod or pellet of the metal to be evaporated. The source material should be of high purity and should be compatible with the electron beam gun. Commonly used metals include aluminium, nickel, molybdenum, copper, gold, silver, and titanium.
- Vacuum chamber: The evaporator operates in a high vacuum environment to prevent the metal from reacting with any gases or contaminants. High vacuum conditions enable for improved step coverage, which means the metal may coat vertical and non-planar surfaces more efficiently, resulting in more uniform and conformal deposition. The vacuum is in the range 10^{-6} to 10^{-8} Torr. The mean free path of an atom of metal in a vacuum chamber is the average distance it can travel before colliding with another particle or surface. When metal is deposited in a vacuum chamber, the chamber's high pressure reduces the likelihood of collisions between metal atoms and gas molecules. The vacuum chamber is typically made of stainless steel or other materials that are resistant to corrosion and can withstand the high vacuum.
- Substrate holder: The substrate holder holds the substrate to be coated and is typically made of a material that is compatible with the deposition process. The holder may be heated to promote adhesion between the metal film and the substrate.
- Deposition rate: The rate at which the metal source is evaporated can be controlled by adjusting the current supplied to the electron beam gun. The deposition rate is typically measured in nanometres per second (nm/s) and can be controlled to produce metal films of different thicknesses. The typical metal deposition rates 0.3 – 0.5 nm/s.
- Uniformity: The uniformity of the deposited metal film is critical for many applications. To ensure uniform deposition, the substrate holder may be rotated or moved during the deposition process, and the metal source may be moved or rotated to ensure that it is evenly evaporated.
- Monitoring and control: The evaporator may include monitoring and control systems to ensure that the deposition process is performed accurately and reproducibly. During the deposition, metal thickness is monitored using feedback of the oscillation frequency from a quartz crystal, which is inside the chamber.

An additional feature of Plassys IV is an internal argon (Ar) source concealed behind a second shutter that enables in-situ Ar surface treatment prior to metallization. Ar surface pre-treatment was employed in this research before Ohmic metal deposition because it removes the native oxides, effectively leaving the surface free of oxides that naturally develop.

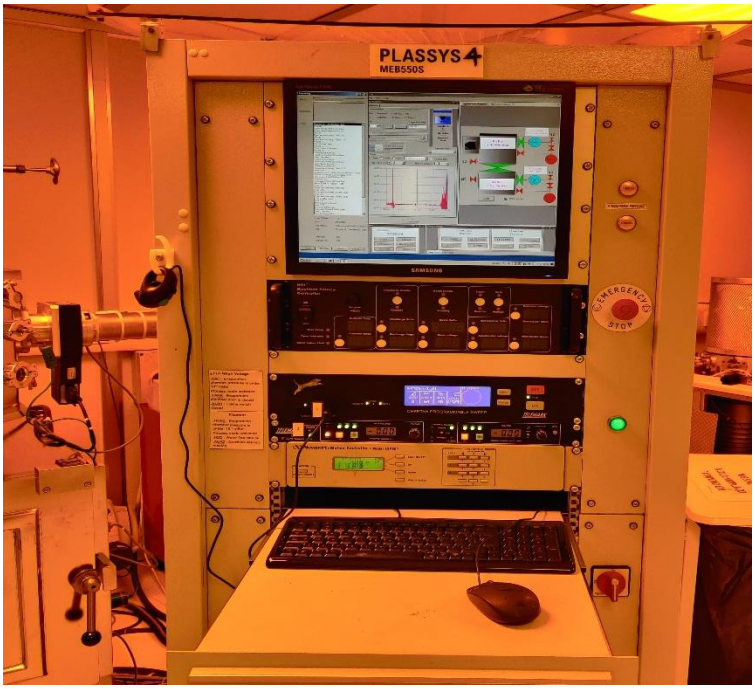


Figure 3.8: Image of the Plassys IV metal evaporation tool.

3.5 Annealing

Rapid thermal annealing (RTA) is a process of heating a material to a high temperature for a short period of time, typically on the order of seconds to a few minutes. The heating is done using intense pulses of light or radiation, such as a flash lamp or a laser, rather than a conventional furnace. RTA is used in semiconductor manufacturing to modify the properties of materials such as silicon, germanium, and III-V compound semiconductors. This can be done is a chamber filled with a gas such as nitrogen (N_2) or forming gas (H_2N_2). The conventional Ohmic contacts metals layers Ti/Al/Ni/Au or Ti/Al/Mo/Au are usually step annealed at 750°C - 950° C in N_2 environment for 30 – 40 seconds. It forms the TiN allow below the contacts to ensure the electron's flow through the contacts into 2DEG. Ti/Al/Mo/Au is better for ohmic contact than Ti/Al/Ni/Au in GaN HEMTs because Mo has a higher melting point than Ni, which prevents Au from diffusing into the Al layer and forming a high-resistance barrier. Mo also has a lower work function than Ni, which helps to lower the Schottky barrier at the GaN/metal interface and create a lower-resistance ohmic contact. In this thesis, we have both the metal stacks. We use the step JetFirst 200 rapid thermal annealing (RTA) illustrate in the figure 3.9.

Figure 3.9: Photo of the Jipelec JetFirst 200 rapid thermal annealing (RTA) machine.

3.6 Etching

Etching is a process that involves selectively removing material such as metal, dielectric or semiconductor material from a wafer substrate using an etchant. The etching process can be used to create patterns (mesa isolation), vias structures (through wafer), or features on the surface of the GaN substrate, which can be used in various applications such as in the semiconductor industry for creating electronic devices. It is important to make sure the photoresist mask is suitably thick and can withstand the etching conditions since the etching solution or gas affects both the resists and the wafer. Etch masks that can be used include metals, dielectrics, polyimide, e-beam replicas, and other materials. There are several methods for etching GaN, including wet etching and dry etching. Wet etching involves immersing the GaN substrate in a solution of chemical etchants, while dry etching uses a plasma to remove the material.

3.6.1 Wet etching

Wet etching is a process of selectively removing material from a substrate using a chemical solution or etchant. The etching rate and selectivity can be controlled by varying the concentration of the etchant solution, the temperature, and the immersion time. The etching rate is the rate at which the material is removed from the substrate, while the selectivity is the ratio of the etching rate between the GaN material, and any other materials present on the substrate. Wet etching is a relatively simple and inexpensive process, but it can be difficult to achieve high precision and uniformity. The wet process occurs both vertical and lateral direction. So, very limited control on the lateral etching and sidewall profile [99]. Additionally, wet etching can introduce surface damage to the substrate, which can affect the performance of devices. Ga-faced GaN has high chemical stability which makes it highly resistive to wet etching. Hence, dry etching was utilised throughout the research work.

3.6.2 Dry etching

Dry etching of GaN involves the use of plasma to selectively remove material from a GaN substrate. Plasma is a high-energy state of matter that can break down molecules and atoms in the gas phase, creating

reactive species that can react with the nitride material and etch it. The plasma is generated by applying a high-frequency electrical field to a gas mixture. The gas mixture typically contains a reactive gas, such as chlorine or fluorine, and an inert gas, such as argon or helium. The reactive gas dissociates in the plasma to form reactive species that can react with the GaN etching material. The plasma is directed towards the substrate, where it selectively etches the material layer of different material composition. The reactive species in the plasma react with the GaN material, forming volatile by-products that are removed from the substrate. The etch process is more vertical in this process. In this research work, dry etching of GaN was performed using two techniques: Inductively Coupled Plasma (ICP) and Reactive Ion Etching (RIE). Both techniques use plasma to selectively remove material from the GaN substrate, but they differ in the way the plasma is generated and the chemistry of the plasma process. The RIE with fluorine-based chemistry such as SF_6/N_2 [100] and ICP has chlorine-based chemistry BCl_3/Cl_2 [101]or Cl_2/Ar [102]. The primary distinction between them is that although ICP contains both DC and RF generators, RIE only has one RF generator. GaN based isolation is typically obtained by etching down the epi-layers up to the GaN buffer layer, typically a depth of around 200nm.

3.7 Dielectric material deposition

Dielectric materials may also be deposited on a wafer during the processing of GaN devices. Dielectric materials can be deposited on GaN wafer using various techniques, such as physical vapor deposition (PVD), plasma enhanced chemical vapor deposition (PECVD) and atomic layer deposition (ALD). PECVD is a technique for depositing thin films of silicon nitride or silicon dioxide on substrates using plasma-enhanced chemical reactions. The process involves introducing a mixture of precursor gases, typically silane (SiH_4) and ammonia (NH_3) for SiNx, into a vacuum chamber containing the substrate to be coated. The gases are then ionized by a low-power plasma discharge, which produces free radicals and ions that react with the surface on the substrate to form a thin film of silicon nitride. There is a PECVD tool that can deposit a few microns of SiNx layer in JWNC. This tool normally runs at a temperature of 300°C. Another alternative is a deposition tool called an inductively coupled plasma CVD (ICP 380), which could be used to deposit a thin coating of SiNx at the room temperature [103] [104]. In this research work, silicon nitride (SiNx) was deposited as a passivation layer to protect the GaN surface following the fabrication of the device.

3.8 T-gate fabrication

High-quality lithography requires excellent resists. There have been various reasons that have contributed to developments in optical lithography throughout the years. The main ones are decreasing exposure radiation wavelength, higher optics, and improved resist. The critical component of HEMT is the nanoscale T-shaped gate, whose gate foot defines the device's frequency regime and for which advanced nanolithography techniques is required.

The T-gate fabrication method consists of two major steps. The first is to design T-shape profiles in resists using the electron beam lithography (EBL) tool, and the second is to transfer the resist profile into gate metals using metallization and lift-off. The basic concept behind creating T-shaped profiles in a bilayer of resists using EBL is based on the difference in electron-beam sensitivity between the two resist layers, with the top resist layer being more sensitive than the lower. After development, the top layer with more

sensitivity creates the larger head of the T-shaped gate, while the lower layer with lesser sensitivity forms the narrower foot. Because this profile is the inverse of the undercut necessary for lift-off, extra precautions are usually taken to achieve a sufficient undercut in the top resist layer [105].

Recent developments in modelling resist development were used to design the process, in which each resist is developed separately to optimize the resulting structure. Initially, the CSAR and PMMA resists were defined separately by writing dosage wedges consisting of 200 x 500 µm rectangles scattered out at 400 µm period. After development, the residual resist thickness was measured using a single profilometer scan. The contrast data from these scans, along with the electron point spread function for the resist stack and material system, were loaded into the BEAMER software [106]. This allowed it to do 3-D Proximity Effect correction, the actual energy distribution given by the primary and scattered electrons can be approximated as the weighted sum of several Gaussian distributions, which, in principle constitute the proximity function and compute the appropriate foot and head doses in order to achieve the required structure. This is especially beneficial in high-density regions, such as gate feeds, or when the gate pitch is tiny. These inputs, in addition to the correction, were utilized to model the resist cross-section after development using the GenIsys LAB modelling software [98]. The proximity correction file is developed by research group. T-gate structures with head lengths of 500 nm and foot lengths between 50 and 100 nm made up the base pattern. A single cleave could be used to segment all the gates in the whole pattern, which was a linear repetition of the basic pattern printed at various dosages [107]. The clearing doses of CSAR and PMMA resists were identified from the dose test measurements to be 180 µC/cm2 and 480 µC/cm2 respectively .

In this research study, a CSAR/LOR/PMMA resist stack for using single-step EBL T-gate fabrication was developed, resulting in a reliable T-gate manufacturing method (CSAR is All resist GmbH AR-P 6200 series resist; LOR is Kayaku Lift-off Resist; PMMA is poly (methyl Methacrylate)). Independent development steps are required for the CSAR and PMMA layers. The LOR splitting layer separates the head and foot developments and also offers a controlled undercut. Using BEAMER software, 3D proximity correction was performed. The process flow for the fabrication of T-gate is shown in Figure 3.10 (a) and exposed dose gate region in Figure 3.10 (b). Figure 3.11 shows the (a) CSAR and (b) PMMA photoresist thickness determines the amount of resist material available to be patterned, while the electron beam dose intensity determines the amount of energy delivered to the resist to expose or clear it.

The substrates used were made of a thick (3 µm) and thin (0.35 µm) buffer GaN-on SiC structure. The 100nm PMMA (950k), 300nm LOR-3A, and 250nm CSAR were used to make multilayer resist stacks. For the PMMA, the required soft bake temperature on the hotplate were 5 minutes at 180 °C and 2 minutes at 150 °C after each of the other two layers. After exposure to an electron beam with a Raith 100 kV EBPG 5200 EBL tool, the three resist layers were developed in three separate steps. This enabled each layer to be developed independently, giving fine control over their relative sensitivities. CSAR was developed by dipping a sample in a bath of amyl acetate at 23 °C for 30 seconds, then rinsing it for 30 seconds in a bath of isopropyl alcohol (IPA), and then drying it with a N_2 blow dryer. LOR-3A is not sensitive to electrons, but it can be removed with TMAH. In this case, CD-26 is used for 25 seconds, followed by two 30-second rinse steps in RO water baths. IPA: MIBK 3:1 was used at 23 °C for 30 seconds to develop the PMMA. This was followed by a rinse with IPA and a N_2 blow dry. Later, Ni/Au metal stacks are deposited by e-beam

evaporation to form the Schottky gate contact. The dose test measurements for T-gate revealed that the clearing doses for T-gate in CSAR (wings) and PMMA (foot) resists are determined to be 180 µC/cm² and 480 µC/cm², respectively.

The fabrication flow for 2-finger devices was then combined with this T-gate fabrication technique. Figures 3-12 (a), (b), and (c) illustrate, respectively, the scanning electron microscopy (SEM) of T-gate development resists profile utilising three layers of photoresists, after metallization robust T-gate of sub-nanometre in size, and T-gate Schottky contact between the source and drain ohmic contacts. When an Ohmic contact is heated to 800 degrees, the surface may become uneven due to various factors. Thermal expansion of the material can cause different regions of the contact to expand at different rates, resulting in surface height variations. The material's non-uniform composition or microstructure can also contribute to differential thermal expansion, leading to surface irregularities. Additionally, surface tension forces at elevated temperatures can cause the molten metal to form irregular shapes and patterns. High temperatures can induce atomic diffusion and recrystallization, leading to changes in grain boundaries and crystal orientation, which in turn can cause surface roughness. Impurities or inclusions in the Ohmic contact material can result in localized differences in melting and solidification temperatures, leading to uneven surface features.

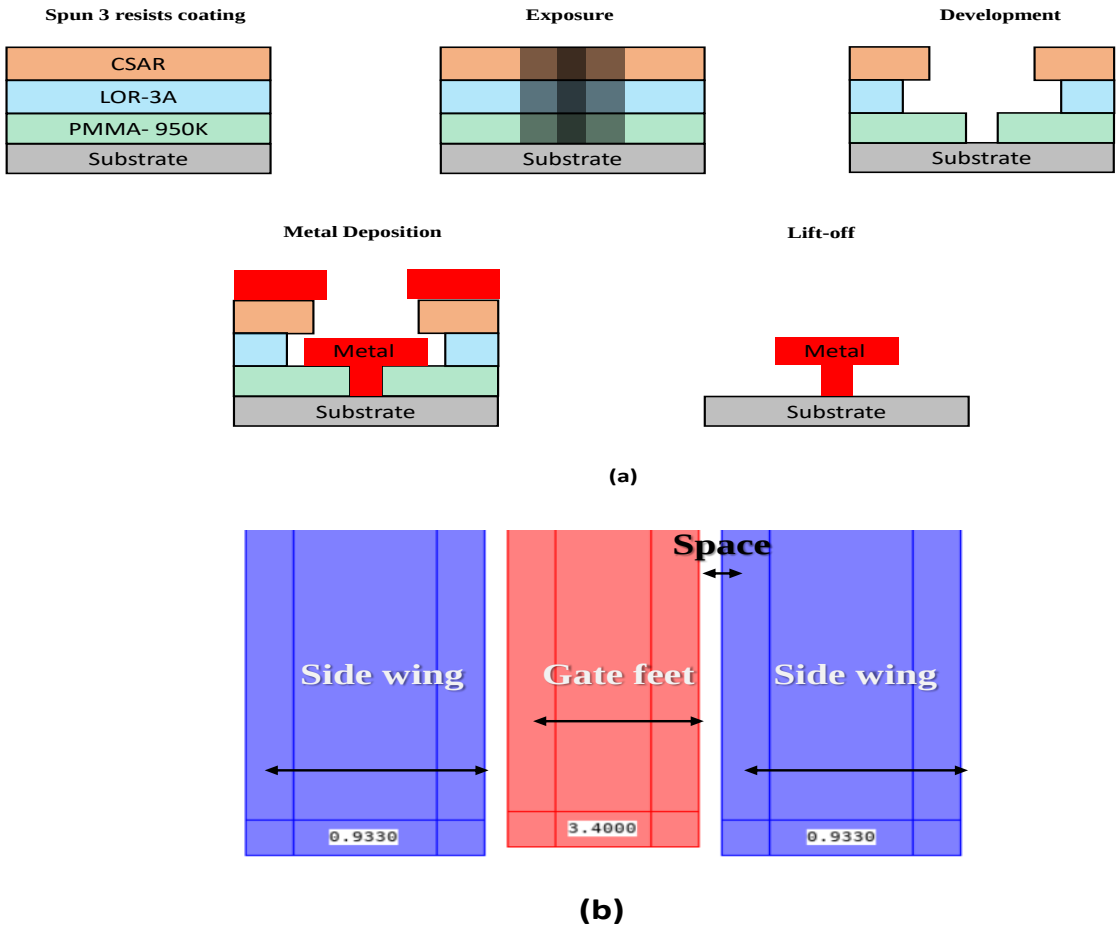


Figure 3.10: Schematic of the process flow for the fabrication of T shape gate using tri-layer (a) and (b) exposed gate region.

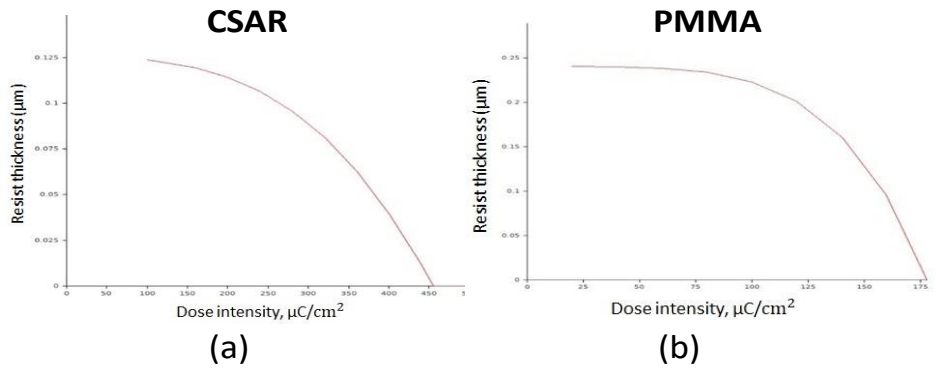


Figure 3.11: The measured beam spread effect by forward scattering in the top CSAR (a) and PMMA-950K (b) at 100 keV. The layer structure is 120 and 250 nm thick PMMA and CSAR, respectively.

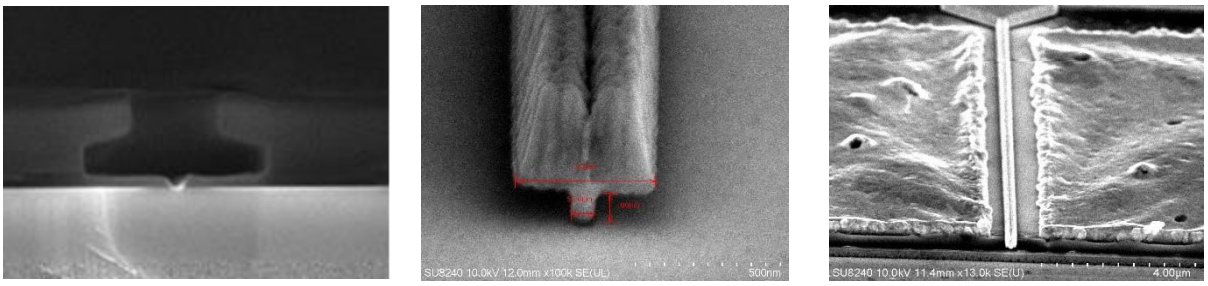


Figure 3.12: SEM images of the developed three-layer photoresist profile of the T gate (a), the T-gate, image after metallization on SiC (b) and T-gate in between source and drain on SiC substrate (c).

3.9 HEMT fabrication process flow

This section details the fabrication flow for the GaN HEMTs device used in this research. GaN HEMTs can then be made using the fabrication steps described including etching, metal deposition, and lift-off procedures. The fabrication method of dry etching had been developed by a University of Glasgow research groups and implemented in this study. The primary processes in GaN HEMT production are depicted in Figure 3.13. are mesa isolation, gate and bondpad metallisation. In Appendix A, specific details of each step are described.

3.9.1 Mask plate design

In this research work, optical lithography (Mask Aligner MA6) tool and electron beam lithography (Raith EBPG 5200 HS) tools were both used in the device processing. Computer aided design software, such as L-edit, one of the software products available from Tanner EDA, was used to create a design for a device before it was fabricated. Quartz mask plates with chromium on one side are manufactured using the

designs prepared in L-edit. On the other hand, an EBL tool receives the design files and uses them to pattern and etch the chrome so that it accurately reflects the original designs. Figure 3.14 shows a typical layout of a design in L-edit.

To study the impact of device geometry on performance, a typical mask is designed with a number of device geometries. Also, the mask has test components like CTLM (circular transmission line method), LTLM (linear transmission line method) and diodes that allow users to evaluate the quality of the Ohmic contact resistance and gate contact after each fabrication run.

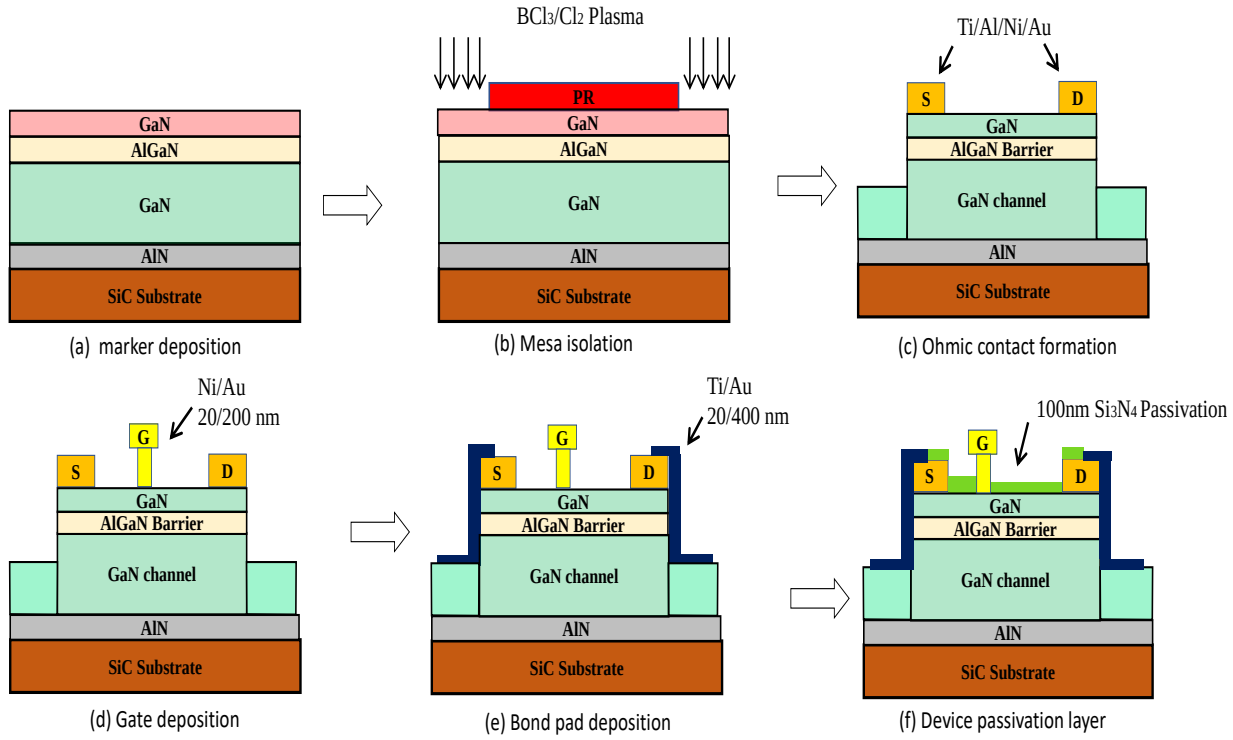


Figure 3.13: Schematic views of the process flow for to substrate fabrication in AlGaN/GaN HEMT device processing steps (a)Clean wafer; markers (b) Photolithography and deep mesa-etch pattern using BCl_3/Cl_2 plasma (c) Deposition of Ti/Al/Ni/Au metal stack Ohmic contacts (d) Ni/Au based gate metallization (e) Bond pads contacts (f) Device passivation using 100nm Si_3N_4.

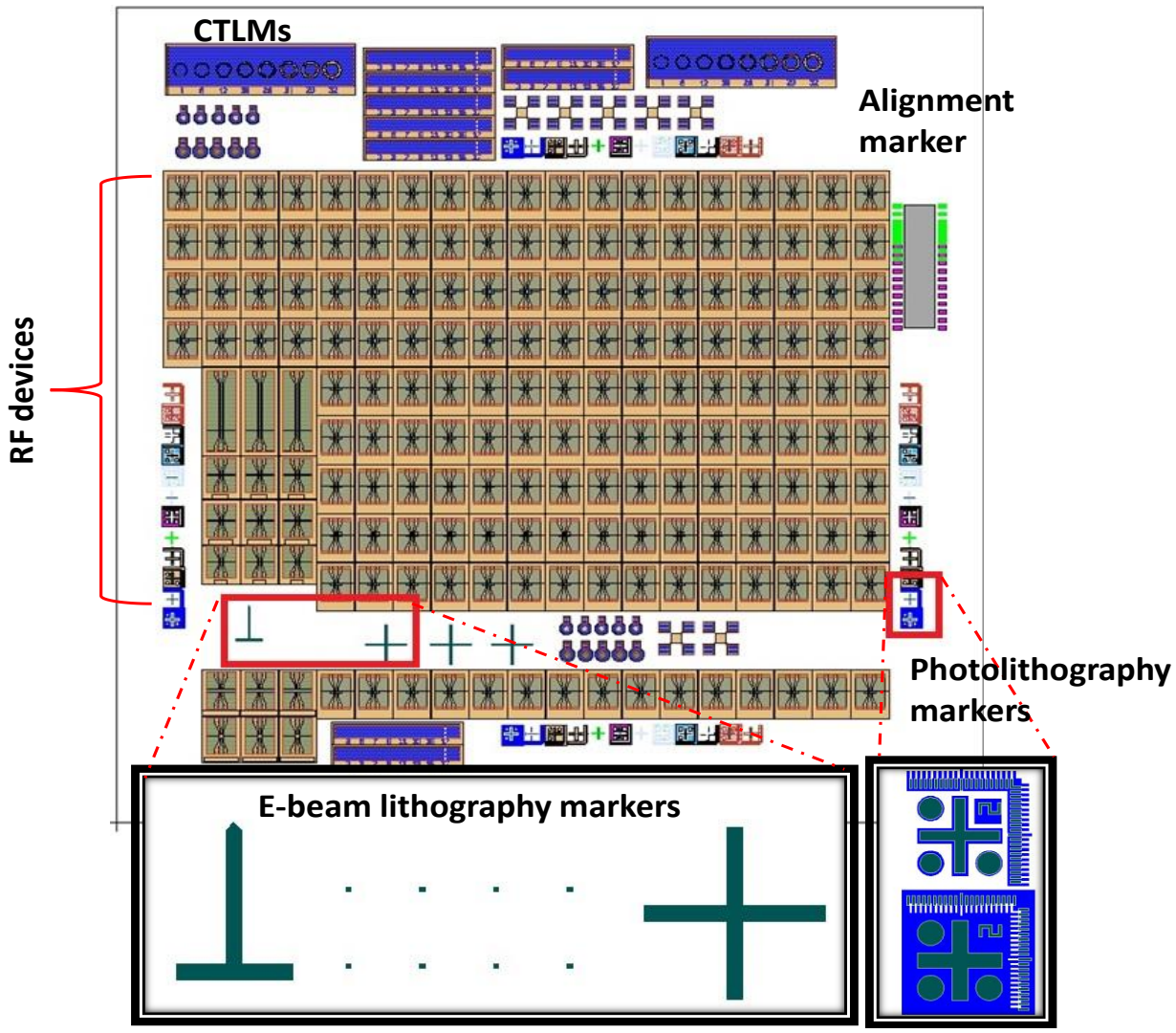


Figure 3.14: Screenshot of layout of a design in L-edit.

3.9.2 Mesa isolation

Mesa isolation is required to electrically isolate neighbouring devices on the sample material. An etch down to the semi-insulating (or buffer) GaN is necessary when considering AlGaN/GaN HEMT material (100–200 nm etch). Device isolation is only necessary for RF devices. Etching the GaN can be done in JWNC using either the RIE or ICP 180 dry etching recipes. In this work, a dry etching process is used to remove all active layers including the GaN cap layer, AlGaN barrier layer and part of the GaN buffer layer as shown in Figure 3.13 (b). Photoresist S1818 is the thick resist used as a mask for the etching with the (Inductively coupled plasma) ICP 180 dry etch tool. The gases were set to 30/15 sccm for the Cl_2/Ar at pressure 4mTorr, and the RF power and ICP DC power are 75W and 750W, respectively. The outcome was a 250-260 nm etch into the GaN buffer layer after a 1 minute. Alternatively, 80+RIE (reactive ion etching) with (chlorine and Argon) Cl_2/Ar gas was used for etching. This produces a controllable and repeatable etch rate of 260 nm/min.

3.9.2.1 Shallow Etching

Shallow etching is a critical process step in the fabrication of gallium nitride (GaN) devices. Shallow etching involves selectively removing a thin layer of GaN from the surface of the HEMT structure. The key challenge in shallow etching of GaN HEMTs is to remove the GaN without damaging the underlying device layers. The etching process must be carefully optimized to ensure that only a thin layer of GaN is removed, and the critical device layers, such as the gate and barrier layers, are not affected. Shallow etching is used for the gate Schottky contacts to etch the AlGaN barrier layer. The shallow etching is much difficult than the mesa etching. Its needs very high accuracy to reach up to 10-15 nm of the barrier layer. Therefore, various factors can affect the shallow etching process, including the gas mixture, etching time, temperature, and pressure. The etching parameters must be precisely controlled to achieve a uniform and reproducible etch profile across the wafer. The gases are used Cl_2 and BCl_3 at a rate of 10 sccm and 5 sccm respectively. For the low damage etching, RF and DC power considered carefully. The RF power is 15W and the DC power is 100W at the chamber pressure of 20mTorr at 20°C for 3 minutes. In this time, 16nm of AlGaN layer is etched, so the etching rate is 5nm/minute.

The silicon nitride (SiNx) passivation layer for dry etching, 80+RIE used for to achieve the more precise etching rate The gases are used SF_6/N_2 at the rate of 25/50 sccm. The RF power was 20W at the chamber pressure of 15 mTorr at room temperature. The optimised SiNx etching rate is 8-9nm per minute.

Table 3- 2 shows the different gases used for the SiNx and GaN material etching work with their etch rates.

Table 3-2: Different gases used in this SiNx and GaN material etching work.

Gases	Flow rate (sccm)	ICP/RF power (W)	Pressure (mTorr)	Temperature (°C)	Etch rate	Target material	Developed by
Cl_2 /BCl_3	25/15	100/13	20	30	70nm/min	For GaN	UofG Research group
Cl_2 /BCl_3	10/5	100/15	20	20	5nm/min	For GaN	Myself
$SiCl_4/SF_6$/Ar	10/3.5/10	100	20	20	20nm/min	SiN	UofG Research group
Cl_2/Ar	30/15	750/75	4	25	250 nm/min	For GaN	Myself
SF_6 /N_2	25/50	20	15	25	8-9nm/min	SiN	UofG Research group

3.9.3 DC and RF devices

Figure 3.15 depicts the gate wrap-around DC device layout. It is essential for process development because it only requires two lithography processes, allowing for more iterations than RF device layout. Since the gate encloses (wraps around) the drain region, a mesa isolation etch step is not required. The gate wrap around DC device has a gate with of 60 µm, a source to drain distance of 12 µm, a gate length of 3 µm, and gate to drain distance of 5 µm.

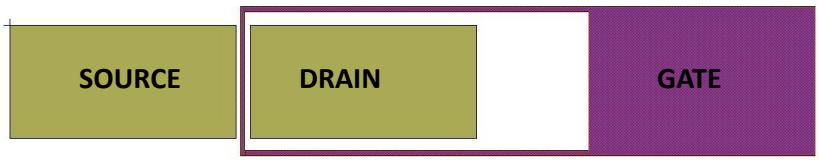


Figure 3.15: Layout design of a DC device.

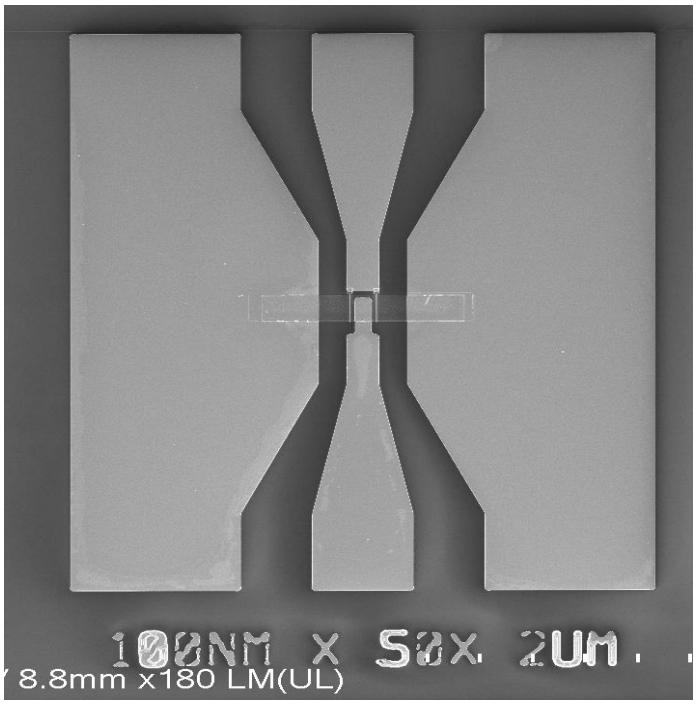


Figure 3.16: Layout of fabricated design of a RF device.

A typical RF device design layout shown in Figure 3.16. The RF devices have different gate lengths (50 nm to 200 nm) and gate width (12.5 µm to 50 µm). The RF layout design fabrication process required 4 lithography steps. It's a combination of e-beam lithography and photolithography. To enable testing of HEMT devices, contact pads are necessary to establish connections with external circuits. These pads utilise a ground-signal-ground configuration with coplanar waveguide (CPW) to ensure the integrity of RF signals, with their characteristic impedance adjusted to match that of the measurement system (50 Ω) by adjusting the signal-line width and signal-ground separation. However, adding contact pads can increase capacitance in HEMT devices at microwave frequencies, significantly affecting their performance. Therefore, in this study, the layout of the input and output feeds was designed to accommodate a

minimum RF probe tip pitch of 50 µm and the RF probing required for skating distances, with a minimum skating distance of 25 µm used as a rule of thumb. A 50 µm-pitch Pico probes were used to probe the CPW-transition parts located at left side of wafer, fabricated transmission lines and passive components. The samples were placed on a thick quartz spacer to eliminate any possible parasitic substrate modes caused by the metal chuck.

3.9.4 Gate metallisation

T-gate metallisation was defined by using the tri-layer of PMMA, LOR3A and CSAR e-beam and LOR10A and S1805 photoresists. The Ni/Au metal stack is used with thickness of 20/300nm respectively.

3.9.5 Bondpad metallisation

Only RF devices require bond pad metallization, and the metal stack used is Ti/Au with thicknesses of 20/400 nm, respectively.

3.10 Summary

This chapter has given an overview of how AlGaN/GaN HEMTs that have been produced throughout the course of this research. It briefly explains the processing methods, including lithography, metallization including a description of epitaxial growth. Details of the fabrication procedures for both DC and RF devices were provided.

Chapter 4
Ohmic Contacts in GaN HEMTs

4 Ohmic Contacts in GaN HEMTs

4.1 Introduction

Ohmic contacts have a significant impact on the performance of GaN HEMTs. Achieving low Ohmic contact resistance would increase current densities, lower the overall On-resistance, and reduce power dissipation in the Ohmic contacts, and so it is very desirable. To minimise the Ohmic contact resistance, either the barrier thickness or the barrier height at the metal-semiconductor interface can be reduced.

This chapter begins with a description of the theory of the metal-semiconductor interface and transmission line model, followed by a review of the existing research on Ohmic contacts made on AlGaN barrier HEMT devices. The optimisation work on recessed Ohmics on AlGaN/GaN material done in this project will be presented.

4.2 Metal-semiconductor Contact

A crucial component of all electrical devices are the contacts between metal and semiconductor. There are two different categories of metal-semiconductor junctions. One is a Schottky contact that functions as a rectifying diode. The other is an Ohmic contact a linear current voltage (I-V) characteristic. The Schottky barrier is usually created when a metal comes into contact with an undoped or lightly doped semiconductor. On the other hand, if a metal contacts a heavily doped semiconductor and is subjected to a thermal process, Ohmic contacts can be formed. In Ohmic connections, a low contact resistance (R_c) is essential. However, because of their wide bandgap, it is difficult to form good Ohmic contacts on III-nitride semiconductors like (Al)GaN.

Ohmic contacts exhibit a linear behaviour due to the emission of electrons from the metal into the semiconductor. This process is governed by the barrier width and magnitude, which is the difference between the conduction band at the interface and the Fermi level. When the barrier height is small, electrons can more easily cross it, leading to a lower resistance for Ohmic contacts. The height of the barrier is determined by the bandgap, where a lower bandgap results in a lower barrier height. The barrier width, on the other hand, depends on the doping level of the semiconductor. Figure 4.1 depicts the band diagram of a metal in contact with an n-type semiconductor. When there is no bias applied across the junction, the Fermi level (E_F) should be flat [58] . As a result, the energy bands bend, creating a depletion zone of width W. The Schottky barrier height, $q\emptyset_b$, is a barrier to electrons. $q\emptyset_b$, depends on the metal work function, $q\emptyset_m$, and electron affinity, $q\chi$, of the semiconductor, and its height determines the ease with which electrons can cross it. A discontinuity between the conduction bands of the metal and semiconductor is caused by band bending and is referred to as an energy barrier or Schottky barrier. The ideal Schottky barrier height can be calculated by:

$$q\emptyset_b = q\emptyset_m - q\chi \qquad (4.1)$$

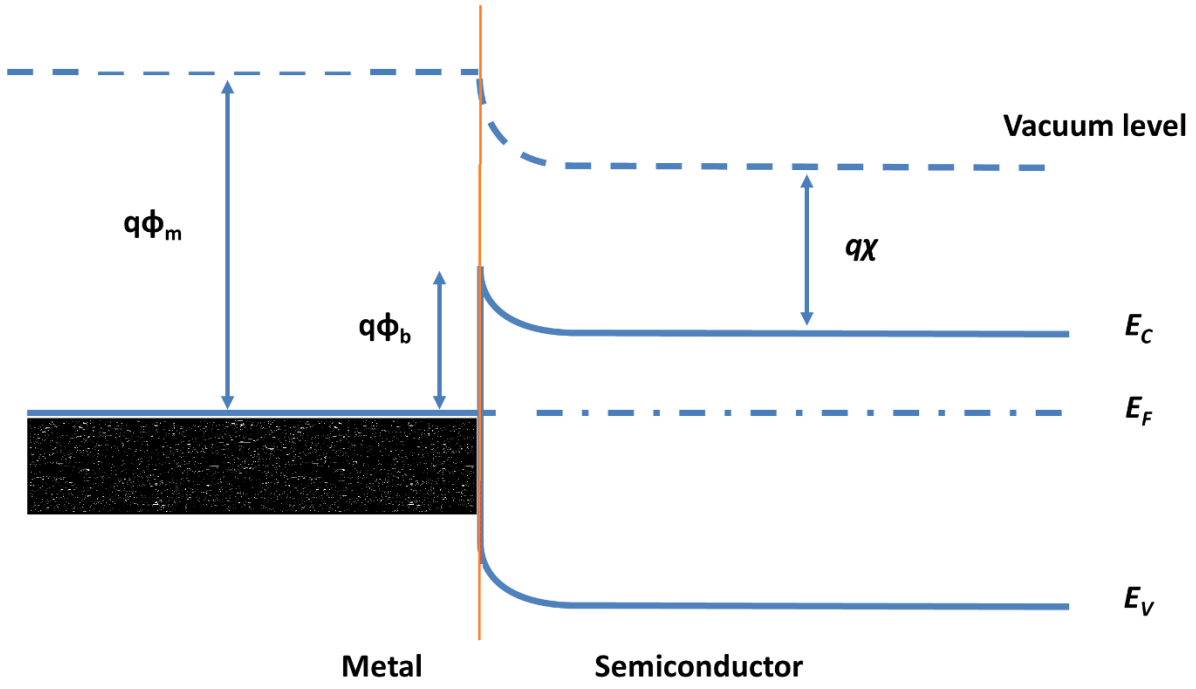


Figure 4.1: Energy band diagram for a metal (n-type) semiconductor contact in thermal equilibrium.

As illustrated in Figure 4.2, there are three main ways by which electrons can transit through the metal-semiconductor interface: thermionic emission, field emission, and thermionic field emission [108]. These are described briefly below:

1. Thermionic emission (TE) – Thermionic emission at the metal-semiconductor interface refers to the process where electrons escape from the metal and cross the Schottky barrier into the semiconductor due to thermal energy. When the metal is heated, the electrons gain enough energy to overcome the barrier, and they diffuse towards the semiconductor side. The ability of electrons to cross the Schottky barrier through thermionic emission is dependent on several factors, including the barrier height, temperature, and doping level of the semiconductor. Thermionic emission is a significant mechanism for current flow in Schottky contacts. For this contact, the doping concentration N_d of the semiconductor is typically below than $10^{17}/cm^3$.

2. Field emission (FE) – Field emission at the metal-semiconductor interface refers to the process where electrons escape from the metal and tunnel through the Schottky barrier into the semiconductor due to the application of an electric field. When a voltage is applied to the metal-semiconductor junction, an electric field is created that can cause the electrons to tunnel through the barrier. The ability of electrons to tunnel through the Schottky barrier via field emission is dependent on several factors, including the barrier height, the electric field strength, and the doping level of the semiconductor. If the doping concentration N_d of the semiconductor is more than $10^{19}/cm^3$, field emission occurs. Due to field emission, Ohmic contacts have linear transmission properties. The size and width of the barrier control field

emission. By increasing the GaN semiconductor's doping, the barrier's width can be minimized and reduces the Ohmic contact resistance. Lower Ohmic contact resistance results from easy electron transport across the barrier when the bandgap decreases.

3. Thermionic field emission (TFE) - A thermionic field emission (TFE) metal-semiconductor interface is a type of electron emitter that utilizes the combination of thermionic emission and field emission mechanisms to achieve high emission currents. In this interface, a metal with a high work function is in close contact with a semiconductor material with a low electron affinity, creating a potential barrier at their interface. A sharp electrode is usually placed near the interface to concentrate the electric field, leading to the enhancement of the emission of electrons. Under a high electric field, electrons in the semiconductor gain enough energy to overcome the barrier and escape into the metal through the thermionic emission process. Additionally, electrons can tunnel through the barrier at the interface via the field emission process, leading to a higher emission current.

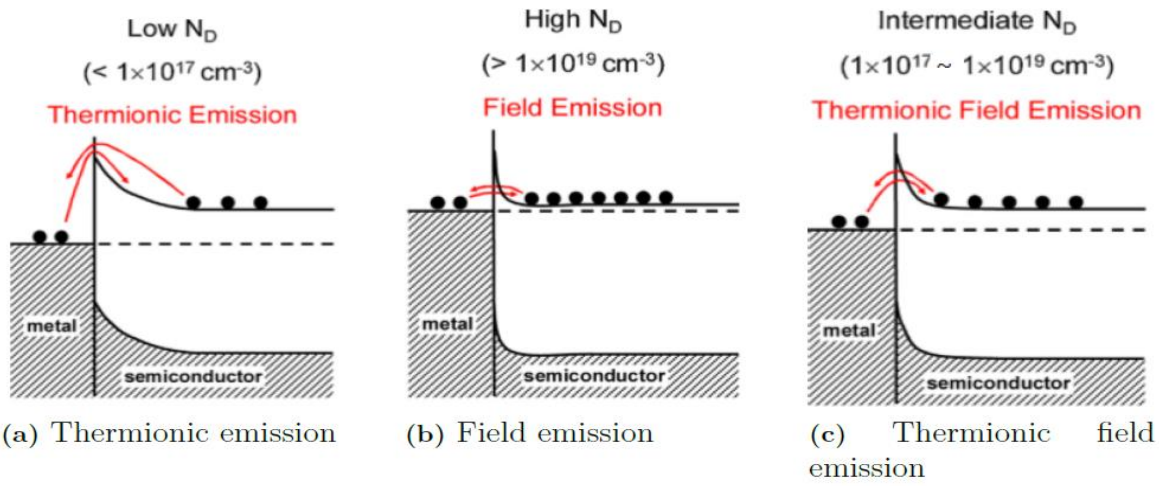


Figure 4.2: The three types of carrier transport mechanism at metal and semiconductor, a) thermionic emission, b) Field emission and c) Thermionic field emission [101].

The quality of Ohmic contacts play a crucial role in determining the device's performance. Lower contact resistance is essential for efficient carrier injection and extraction, which improves the device's overall efficiency and maximum output power. Additionally, higher series resistance introduced by Ohmic contacts can limit the device's transconductance, affecting its high-frequency performance and maximum oscillation frequency (f_{max}) and cut-off frequency (f_T). The presence of Ohmic contacts also introduces parasitic capacitance and inductance, which negatively impact the high-frequency response, reducing the device's bandwidth at mm-wave frequencies. Carrier transport properties influenced by Ohmic contacts can cause transit time delays, limiting the device's maximum operating frequency and switching speed. The thermal characteristics of Ohmic contacts are critical to dissipate heat efficiently at high frequencies, as excessive heat generation can lead to thermal instability and degrade device performance. Finally, Ohmic contact materials being carefully selected to match the GaN semiconductor material used in the

HEMT structure. By carefully optimizing Ohmic contacts through material selection and fabrication, designers can improve the frequency response of GaN HEMTs, especially in mm-wave applications.

4.2.1 Schottky Gate contact

For AlGaN/GaN-based devices, Schottky contacts are employed as the gate terminal. Figure 4.3 illustrates the IV characteristics of a Schottky contact. This contact regulates the density of 2DEG in AlGaN/GaN HEMTs. The 2DEG carrier density at the AlGaN/GaN interface is varied when the gate is biased. The high barrier height of a Schottky contact is desirable to reduce the current flowing from the semiconductor into the gate metal which is referred to as gate leakage current. Ni, Au, and Pt are three materials with high work functions that are often used in Schottky contacts. The work function of these materials is 5.15 eV, 5.10 eV, and 5.65 eV, in that order. In this case, Pt has the highest work function, but it is not used as much in AlGaN/GaN-based devices because it doesn't stick well to GaN. So, Ni is commonly used, followed by a layer of Au to keep it from oxidising and to reduce the contact resistance [109] [110].

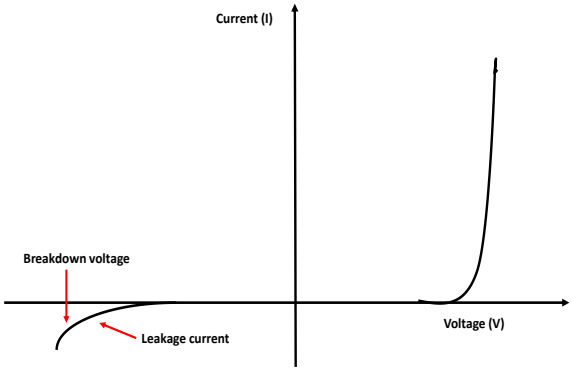


Figure 4.3: IV characteristics for a Schottky gate contact

4.2.2 Ohmic contact formation

The Ohmic contact (source/drain terminals) controls the flow of current through an AlGaN/GaN HEMT. Figure 4.4 illustrates the IV characteristics of a Ohmic contact.

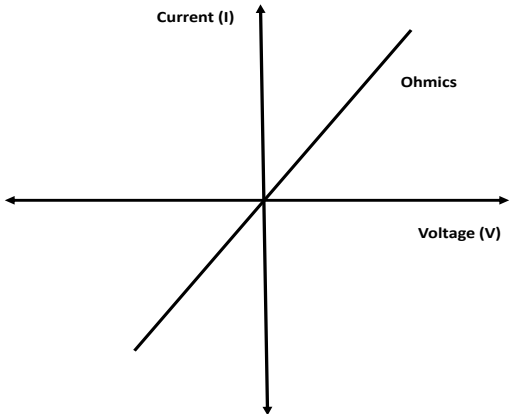


Figure 4.4: IV characteristics for a Ohmic contact.

Ohmic contacts on GaN are often created using rapid thermal annealing (RTA) at high temperatures between 750 and 900 °C and contain multiple metal layers, each having its own function in optimising the Ohmic behaviour of the contacts. The most common way to explain the low R_c is the formation of TiN. During the annealing, AlGaN loses its nitrogen atoms to make TiN. N-vacancies in the barrier layer act as n-dopants. So, the barrier layer becomes heavily doped, which raises the chance of tunnelling and lowers the R_c [111]. It has been shown that the metal stack of Ti/Al/Ni/Au provides good Ohmic behaviour for AlGaN/GaN devices, with excellent Ohmic contact resistances of about 0.2– 1.0 Ω-mm [112].
The following are typical metal schemes used for Ohmic contact layers, from bottom to top, and their functions:

- **Titanium (Ti):** A smooth metal/semiconductor interface is achieved by annealing at a high temperature for a brief period of time to keep the reaction of Ti with only the AlGaN barrier and prevent it from reacting with the GaN buffer layer. In the process, Ti forms an alloy with the nitrogen (N) in the AlGaN barrier layer. Nitrogen vacancies also created and as a result the AlGaN barrier beneath the contact becomes heavily doped with donor atoms. Therefore, electrons can easily tunnel through to the 2DEG from the contact owing to the low potential barrier between the two.
- **Aluminium (Al):** Al_3Ti alloy is created through the bonding of Al and Ti. This alloy helps to increase the conductivity of the contact by reducing oxidation of the Ti layer.
- **Nickel (Ni), Platinum (Pt), Molybdenum (Mo) or Titanium (Ti):** is the diffusion barrier between the top gold layer and the bottom Al layer to avoid the production of a highly resistant alloy called purple plague [113][114].
- **Gold (Au):** Au is used in the metallization of the Ohmic contact because it is a highly conductive material. When annealed at high temperatures, Au reduces the oxidation of the Ti and Al layers of the contact, further increasing the conductivity of the contact [114].

To realise (non-annealed) low Ohmic contact resistances, GaN is usually highly doped with silicon at doping densities of up to 1×10^{20} cm^{-3} [115].

4.3 Transmission line model

The performance and quality of Ohmic contacts are evaluated using the Transfer Length Method (TLM), sometimes referred to as the Transmission Line Model. Reeves and Harrison introduced this method, and a detailed analysis is published in reference [116]. These measurements are often performed using either linear TLM structures or circular TLM structures.

4.3.1 Linear Transmission Line Model (LTLM)

The model, shown in Figure 4.5 (a), (b), consists of a sequence of the same Ohmic contacts spaced apart by variable gap lengths, L_x. The increase in semiconductor series resistance is correlated with the increase in gap separation. The LTLM structure require mesa etching to isolate it and eliminate fringing fields (to be explained in next sub-section). In a TLM pattern, current travels from one contact to the next through the semiconductor material and then to a second metal contact through resistances R_c, R_{sh}, and R_c again and

follows the path of least resistance. Here, R_C is the contact resistance, R_{sh} is sheet resistance. Using a four-probe measurement system, which applies current through one pair of probes while measuring voltage with the other pair, it is possible to measure the total resistance between consecutive pairs of pads. As illustrated in Figure 4.6, the total resistance is plotted versus the pad spacing. The total resistance R_T of a metal semiconductor contact is the sum of the resistances encountered, which is calculated as follows:

$$R_T = 2R_c + R_{ch} = 2R_c + \frac{R_{sh}L}{W} \qquad (4.2)$$

Here, L is the spacing distance between the two contacts, W is the contact width contact and R_{ch} is the channel resistance.

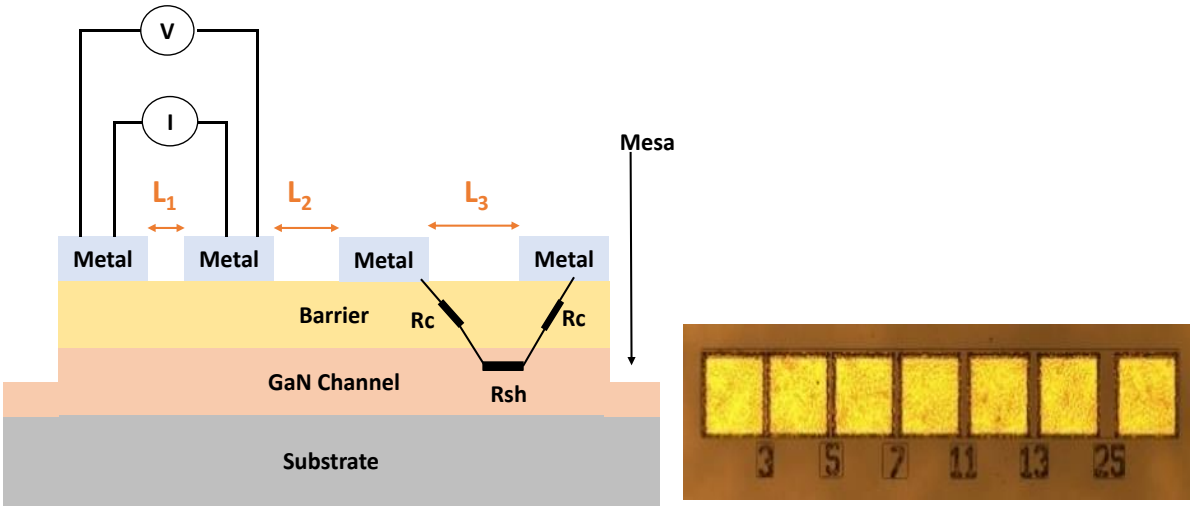


Figure 4.5: (a) A semiconductor material with Ohmic contact pads for LTLM characterization (b) LTLM on after annealed.

The contact resistance, $2R_c$, is obtained from the intercept with the y-axis. The normalised contact resistance, R_c (Ω.mm) is obtained by multiplying R_c by W, the width of metal contact. The transfer length, L_T, for semiconductors in general, which is the average distance over which electrons flow into or out of the semiconductor at the edge of the contact. It can be calculated from the intercept with the x-axis as follows:

$$L_X = 2L_T \qquad (4.3)$$

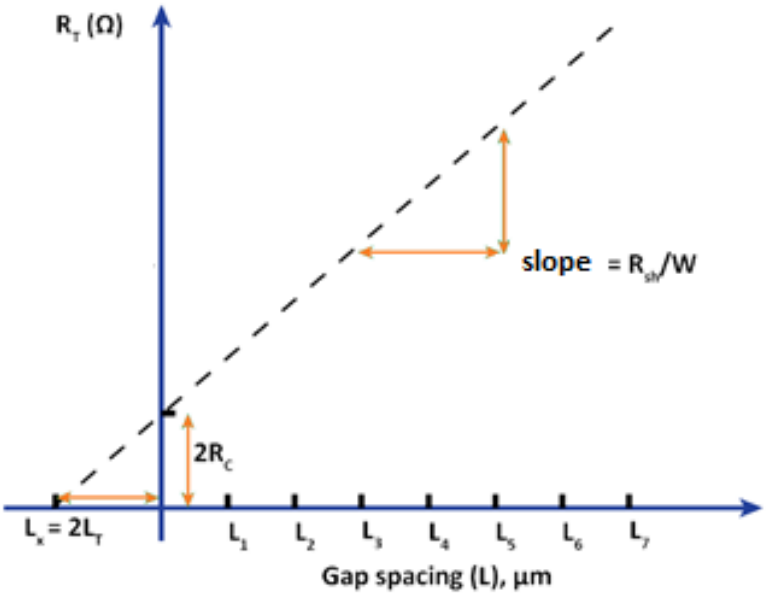


Figure 4.6: An illustration of a plot of total resistance measurements versus various gap spacing.

4.3.2 Circular Transmission Line Model (CTLM)

The CTLM technique is frequently used to measures the characteristics of Ohmic contacts. The problem of fringing fields can be simply solved with CTLM structures. The importance of mesa isolation depends on its ability to limit current in the channel and avoid fringe currents. The confinement of the current results in a more accurate estimation of the R_C and R_{sh} values. This is shown in Figure 4.7, which depicts the electric fields for isolated and non-isolated mesa pads. Mesa isolation of the LTLM structure prevents any unwanted current flow, resulting in more accurate measurements. In contrast to the two lithography stages needed for LTLM structures, the CTLM method only needs one. A gap separates pairs of two metallic contact locations in the test structure: an inner circle and an outer ring. The entire test structure comprises a collection of contacts with varied gap lengths, spanning from a few µm to tens of µm [117].

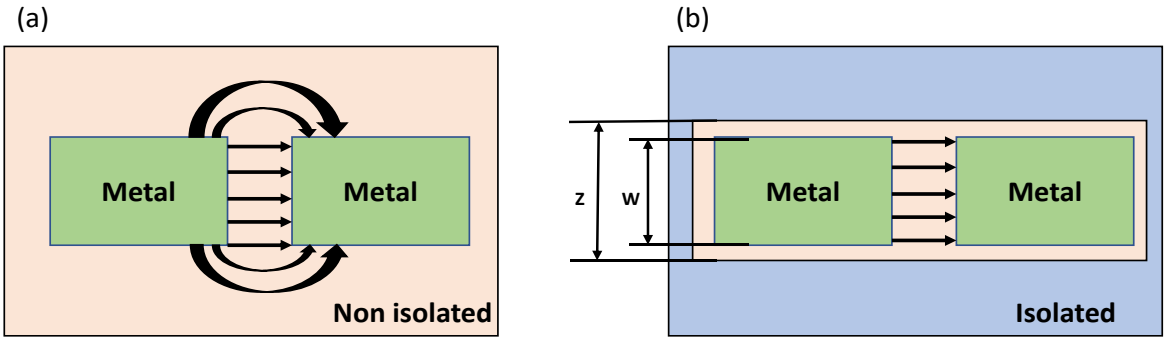


Figure 4.7: Current flow in LTLM structures (a) non-isolated and (b) isolated.

This structure is frequently used mostly for two reasons. First, due to the circular design, there is only one path for the current to pass between the metal contacts of the inner circle and the outside ring as shown in Figure 4.8, i.e. there are no fringing fields and therefore no requirement for mesa isolation. Secondly, the issue with the isolation size being different from the contact size may be avoided because isolation is not required.

Figure 4.8: Illustration of Reeves concentric circular contacts.

The technique used to extract the contact resistance from the LTLM structures is the same one used to extract the contact resistance from the CTLM structures. One exception is the necessity to apply a correction factor to data measured using CTLM structures because the inner circle's circumference is not equal to the outer circle's circumference and a correction factor is thus required to provide a linear fit. The correction factor is determined as follows, depending on the gap size [118] :

$$C = \frac{R_1}{s}\ln\frac{R_1 + s}{R_1} \qquad (4.4)$$

where s is the gap spacing and R_1 is the inner circle's radius. Table 4.1 lists the correction factors vs gap spacing for R_1 = 100 µm.

Table 4-1: Gaps and their corresponding correction factor

Gap spacing (µm)	4	8	12	16	20	24	32	40	48
Correction factor (C)	0.98	0.96	0.94	0.92	0.91	0.90	0.87	0.84	0.82

4.4 Literature review on GaN based Ohmic contacts

Generally, the formation of TiN on the AlGaN/GaN for the Ohmic contacts the Ti/Al built contacts is annealed at very high temperature [119] the contact resistance reduces with reducing the Ti/Al ratio, reaching a smallest at a ratio of 0.15 alloy at 900°C [120]. The formation of N vacancies in GaN leads in electrically active donors, which lower the barrier width and make electron tunnelling easier. This approach, however, is ineffective for AlGaN because the enthalpy of formation for GaN (-110.9 KJ/mol),

TiN (-265.5 KJ/mol), and AlN (-318.1 KJ/mol) all release a significant amount of energy during contact formation. Because the bonding in AlN is stronger than in TiN, Al_3Ti is formed, leaving AlGaN unchanged. As a result of the high Ohmic contact resistance, different metallization methods for GaN and AlGaN are required[121] [122]. The Ohmic contacts designed by using a metal stack of Ti/Al/Ni/Au (30/180/40/100nm) and annealed at 830℃ in N_2 atmosphere on 30 seconds time period for AlGaN/GaN devices provided the best reported low Ohmic contact resistance which is 0.1 Ω-mm [123]. Low contact resistance and very smooth surface morphology are the crucial parameters for the device-optimized by using the metal stack Ta/Al/Ta has got a contact resistance is 0.77 Ω·mm [124].

Non-annealed Ohmic contacts are now also widely used in current research. They are obtained by etching the Ohmic contact regions and regrowing with highly n-doped GaN. As discussed earlier, lower bandgap of GaN and the high doping helps to reduce the barrier height and thickness of the metal-semiconductor junction. Typically MBE (molecular beam epitaxy) is mostly used for regrowing Ohmic contacts on HEMTs [125]. The obtained low ohmic contact resistances extracted from TLM measurements are 0.12 Ω-mm [126], 0.2 Ω-mm [127] and 0.11 Ω-mm [128]. Table 4-2 below shows the literature review on AlGaN/GaN based Ohmic contacts.

Table 4-2 State-of-the-art Ohmic contacts to AlGaN/GaN

Ohmic metal layers (nm)	**Barrier layer thickness d_{AlGaN} (nm)**	**Aluminium concentration X_{Al} (%)**	**Annealing Condition**	**Ohmic contact resistance. (Ω.mm)**	**References and Regrown (Y/N)**
Ti/Al/Ni/Au (NA)	24nm	30%	850 °C for 30 s	0.12	[126], 2018, N
Ta/Al/Ti (10/300/20)	12nm	25%	550 °C for 60 s	0.4	[129], 2019, N
Ti/Al/Ni/Au (15/60/30/50)	20nm	20%	850 °C for 30 s	1.3	[130], 2018, N
Ti/Al/Ni/Au (NA)	20nm	25%	800 °C for 30 s	0.85	[131], 2018, Y
Ti/Al/Ni/Au (20/120/65/55)	23nm	25%	840 °C for 35 s	0.4	[132], 2016, N
Ti/Al/Ni/Au (60/180/83/68)	20nm	25%	850 °C for 60 s	0.8	[133], 2018, N
Ti/Al/Ni/Au (10/200/40/100)	25nm	32%	870 °C for 30 s	0.39	[134], 2018, N
Ti/Al/Ni/Au (25/140/40/50)	25nm	30%	830 °C for 30 s	0.67	[123], 2019, N
Ti/Au/Al/Ni/Au (25/20/120/40/50)	25nm	30%	830 °C for 30 s	0.5	[123], 2019, N
Ti/Al/Ti/TiN (20/100/20/60)	20nm	25%	550 °C for 90 s	0.21	[135], 2019, N
Ti/Al/Ti/Au (20/110/40/50)	21nm	26%	800 °C for 30 s	0.7	[136], 2018, N
Ti/Al/Ni/Au (20/110/40/50)	21nm	26%	800 °C for 30 s	1.3	[136], 2018, N
Ti/Al/W (20/100/30)	21nm	26%	830 °C for 45 s	0.45	[136], 2018, N
Ti/Al/Mo/Au (15/60/60/35)	25nm	26%	850 °C for 30 s	0.3	[35], 2018, Y

Ti/Al/Mo/Au (15/60/60/35)	25nm	26%	850 °C for 30 s	0.8	[35], 2018, N
Ti/Al/Ni/Au (20/100/40/50)	20nm	26%	870 °C for 20 s	0.3	[137], 2016, Y
Ta/Si/Ti/Al/Ni/Ta (5/5/20/120/40/30)	18nm	26%	850 °C for 30 s	0.22	[138], 2013, N
Ti/Al/Ni/TiN (20/60/10/80)	19nm	23%	900 °C for 30 s	1.1	[139], 2020, N
Ti/Al/Ni/Au (20/120/30/50)	21	25%	850 °C for 45 s	0.37	[140], 2022, N
Ti/Al/Ni/W (50/250/50/30)	21	25%	550 °C for 60 s	0.51	[140], 2022, N
Ti/Al/Ni/Au (20/120/40/50)	5	65%	850 °C for 30 s	0.17	[141], 2022, N
Ti/Al/Ni/Au (20/120/40/50)	20	22%	630 °C for 600 s	0.078	[142], 2022, N
Ti/Al/Mo/Au (15/60/35/50)	**21**	**25%**	**800 °C for 30 s**	**0.32**	**This work, N**

4.5 Fabrication and evaluation of patterned Ohmic contacts

In this project, we processed and characterized three (3) different patterned Ohmic contact structures (chess, vertical and horizontal) employing both shallow (~ 9 nm of etch depth) and deep (~ 30 nm of etch depth) Ohmic recess etching and analysed these using the transfer length method (TLM). Conventional or planar Ohmic contact structure was also fabricated for comparison. GaN HEMT devices were also processed and characterized to evaluate their performance.

4.5.1 Patterned TLMs and device fabrication.

The epitaxial layer structure used in this work was grown by Cambridge University, UK, using metal-organic chemical vapour deposition (MOCVD) on a 1-mm thick high-resistivity (HR) silicon substrate. The wafer structure consists of (from top to bottom), a 2-nm GaN cap layer, 21-nm $Al_{0.25}Ga_{0.75}N$ barrier layer, 1-nm AlN exclusion or spacer layer, 200-nm GaN channel layer, 850-nm GaN and 1.7-µm AlGaN buffer layers, and 250-nm AlN nucleation layer. Two samples were prepared and processed for Ohmic recess etching. The first sample was used for shallow etching (etch depth of 9 nm) above the 2DEG channel, and the second sample was used for deep etching (etch depth of 30 nm) below the 2DEG channel. Both samples have the conventional or planar (no pattern) and different TLM pattern structures (chess, vertical and horizontal) as shown in Figure 4.9. The device structure corresponding to each of these different TLM patterns was also included to evaluate the device performance. The conventional or planar structure no etching process is done. The wrap-around gate design (where the gate encircles the drain contact) structure was used for device evaluation. The horizontal patterned structure of ohmic contacts is preferred due to its potential to improve high-frequency performance by reducing contact resistance. Contact

resistance at the metal-semiconductor interface, caused by phenomena such as thermionic emission, tunnelling, and surface diffraction, is a limiting factor. This design decreases contact resistance by increasing contact area with vertical and chess patterns and by providing multiple electron pathways. In addition, its rough surface aides in electron scattering, reducing its susceptibility to surface scattering. Due to its capacity to reduce contact resistance, this horizontal patterned structure is anticipated to excel in high-frequency applications [32]. The cross-section schematic illustration of the fabricated AlGaN/GaN HEMT devices with a shallow and deep Ohmic recess etching are shown in Figures 4.10 (a) and 4.10 (b), respectively.

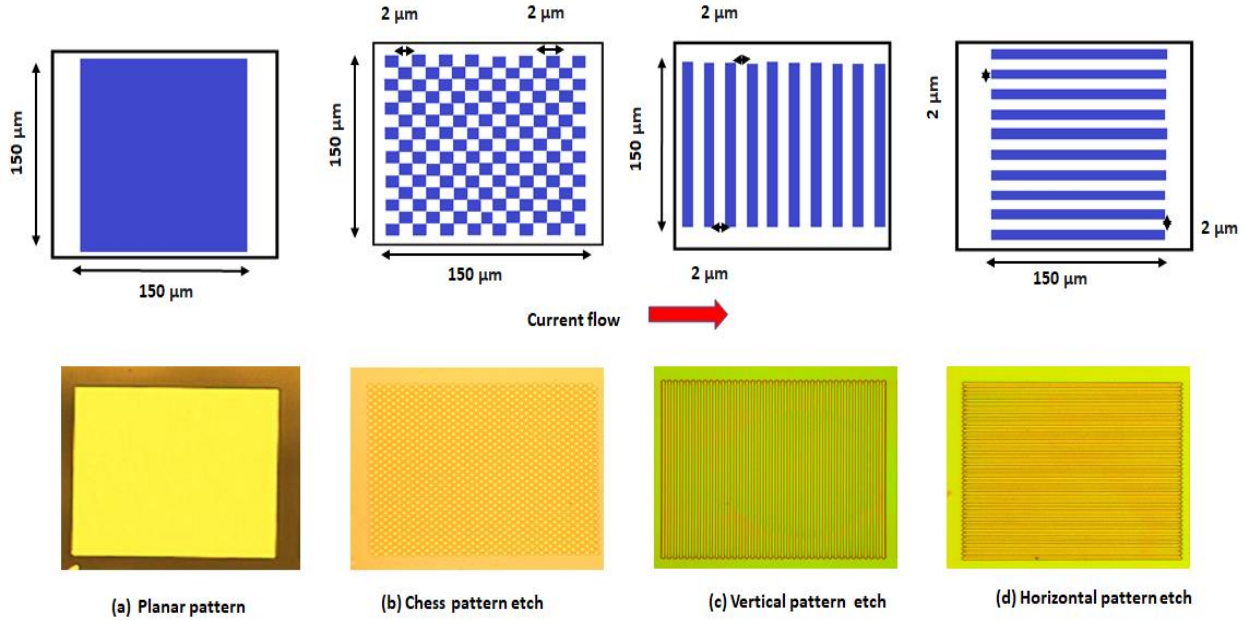


Figure 4.9: Top-view illustrations of the patterned surface of Ohmic contact using (a) conventional or planar (b) chess pattern etch (c) vertical pattern etch, and (d) horizontal pattern etch of AlGaN/GaN HEMT structures.

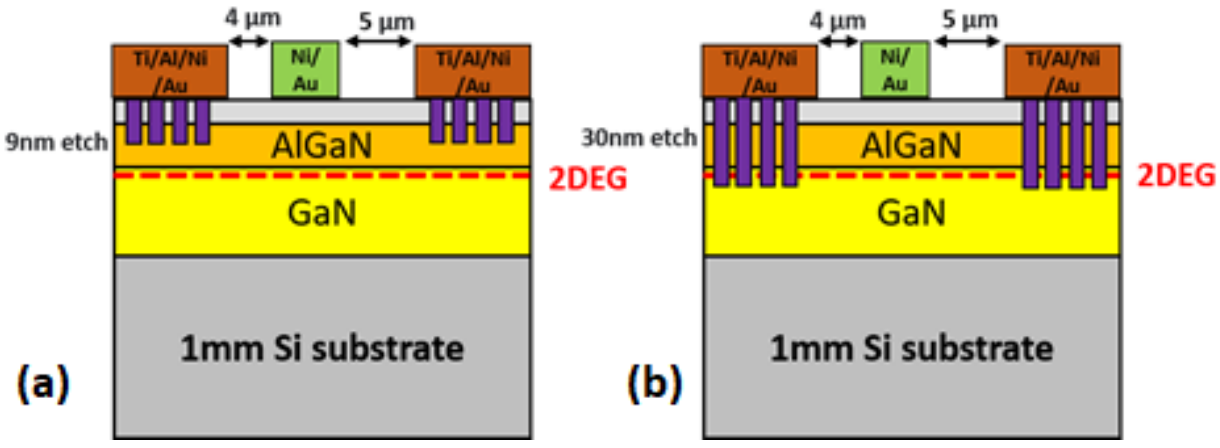


Figure 4.10: The cross-section schematic illustration of the fabricated AlGaN/GaN HEMT structures with (a) shallow (~ 9 nm of etch depth) (b) deep (~ 30 nm of etch depth) Ohmic recess etching.

The RIE delayed effect, also known as aspect ratio dependent etching (ARDE), occurs during reactive ion etching (RIE). As a result, the etching depth of a smaller trench is less than that of a larger trench. This is due to the depletion of etching ions and radicals as they travel through the trench, resulting in a diminished etch rate at the trench's bottom. Several methods exist for mitigating the RIE latency effect, including the use of high-density plasmas, the addition of inert gases to the plasma, and the application of a substrate bias [143]. In Figure 4.11 showed the sidewall area of single chess pattern in the Ohmic region. The formula for calculating the sidewall of chess square pattern:

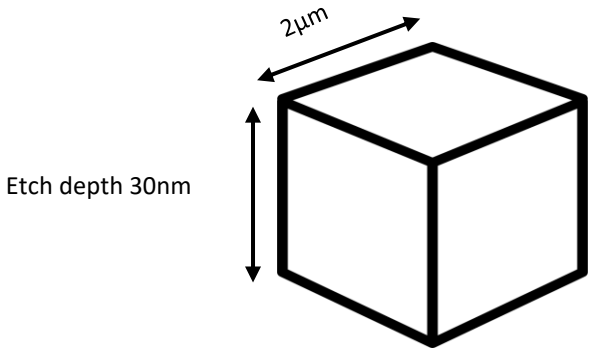


Figure 4.11: The single etches chess pattern area

$$\text{Total area} = \quad (L^2 + (L + etch\ depth \times 4)\mu m^2 \qquad (4.5)$$

Where, the L is length of etch area and etch depth is etch of AlGaN barrier layer (30nm).The analysis of sidewall characteristics in Ohmic etching, considering Planer pattern (22500 μm^2), Chess pattern (23,265 μm^2), Vertical pattern (23,850 μm^2), and Horizontal patterns (23,850 μm^2) revealed that the chess pattern exhibited slightly more surface area than the horizontal pattern. However, it was observed that the horizontal pattern demonstrated superior contact resistance compared to the other patterns.

Several factors could explain this phenomenon. Firstly, the horizontal pattern might have generated a greater number of sidewall regions on the AlGaN surface during the etching process. This increased the contact area for the Ohmic metal, facilitating a stronger tunnelling current between the Ohmic metal and the AlGaN barrier, consequently reducing contact resistance [32].

Secondly, the horizontal pattern may have been better aligned with the lateral current flow within the 2DEG. This alignment likely improved the tunnelling current and further contributed to the reduction in contact resistance [144].

Lastly, it's possible that the horizontal pattern exhibited greater uniformity in comparison to the chess pattern. This enhanced uniformity would have played a role in minimizing contact resistance.

In summary, based on the sidewall calculations and contact resistance measurements, it can be concluded that the horizontal pattern is the most favourable choice for Ohmic etching in GaN devices.

The fabrication starts with the mesa isolation using the Cl_2/Ar gases and the etched depth of 260 nm was measured. For the TLM pattern structure, the etching was done using inductively coupled plasma (ICP) 180 tool with the following recipes: chamber pressure of 20 mTorr, mixture of BCl_3 and Cl_2 gases with flow rates of 5/10 sccm, and ICP DC and RF power of 100 and 13 Watts, respectively. The two etching depths of ~ 9 nm and ~ 30 nm were compared for shallow and deep Ohmic recess etching, respectively. Prior to Ohmic metal deposition, an in-situ argon (Ar) etch for 30 seconds was applied to remove native oxide on the sample surface. A metal stack of Ti/Al/Ni/Au (30/180/40/100 nm) was deposited using E-beam evaporator, followed by a rapid thermal annealing (RTA) at 800°C for 30 seconds in N_2 environment. Finally, Schottky metal stack of Ni/Au (20/200 nm) was deposited for the gate contact. The fabrication was done by a combination of photolithography and electron beam lithography (E- beam) processing. E-beam lithography was used to get precise sizes of the TLM pattern structures which consist of the smallest pattern size of 2 µm as shown in Figures 4-8b, 4-8c and 4-8d. The width of the TLM structure is 150 µm with the gap spacings, L, of 5, 7, 9, 11 and 13 µm. The device dimensions used are as follows: gate width (W_G) of 60 µm, gate length (L_G) of 3 µm, drain to source distance (L_{DS}) of 12 µm, gate to drain (L_{GD}) of 5 µm and gate to source (L_{GS}) of 4 µm.

4.5.2 Experimental results and discussion

4.5.2.1 TLM measurements

Figure 4.12 shows the measured contact resistances, R_C, of a shallow (~9 nm of etch depth) and deep (~ 30 nm of etch depth) Ohmic recess etching on 3 different TLM patterned structures along with the conventional TLM structure. The cross-section schematic illustration of TLM patterned etching structures for a shallow and deep Ohmic recess are shown in Figures 4.13 (a) and 4.13 (b), respectively. The conventional or planar structure (no etching process is done) on both samples showed the same (0.59 Ω-mm) Ohmic contact resistance. The measured contacts resistances of TLM patterned structures show lower contact resistance both for shallow (0.46 Ω-mm) and deep (0.32 Ω-mm) Ohmic recess compared to the conventional (0.59 Ω-mm) TLM structure. We attribute to the uneven AlGaN barrier layer thickness underneath the Ohmic metal contacts. The formation of sidewall area on AlGaN surface during the patterned etching process provides better contact of Ohmic metal resulting in more tunnelling current between Ohmic metal and the AlGaN barrier thus, reducing the contact resistance [144]. As for the conventional TLM structure (see Figure 4.13 (c)), the Ohmic metal sits on the even (planar) AlGaN layer without the sidewall area and no ohmic recess etching resulting in higher contact resistance.

Further reduction of contact resistance for all 3 patterned etching structures was observed with a deep Ohmic recess (~ 30 nm of etch depth) due to the close contact between Ohmic metal and the 2DEG as shown in Figure 4.13 (b). The lowest contact resistance of 0.32 Ω.mm was observed for a deep horizontal patterned structure. These results are in good agreement with the obtained results from the previous published works in [32] where a deep ohmic recess etching (below the 2DEG) was performed prior to Ohmic metal deposition. The horizontal patterned structure provides the lowest contact resistance due to the removal of AlGaN barrier layer (patterned etching) and it is in parallel with the lateral current of the 2DEG (see Figure 4.9 d) resulting in better tunnelling current compared to the vertical (see Figure 4.9 (c)) and chess patterns (see Figure 4.9 (b)) where the patterned etching is perpendicular to the lateral current of 2DEG resulting higher contact resistances. It was also observed that the measured contact resistance of

chess patterned etching is higher than the conventional TLM structure for a shallow Ohmic recess. The reason for this is not clear and needs further investigation.

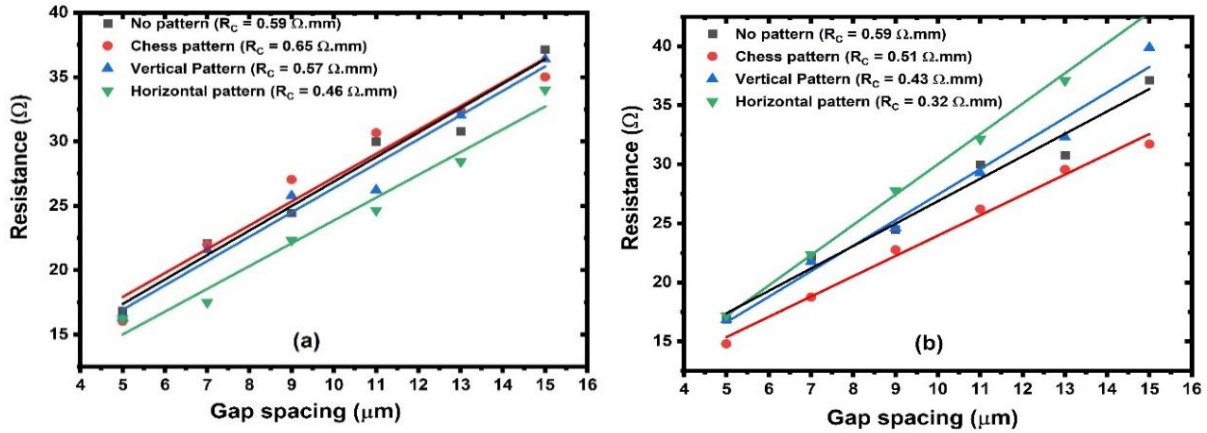


Figure 4.12: Measured contact resistances, R_C, of (a) shallow and (b) deep Ohmic recess etching on 4 different TLM pattern structures.

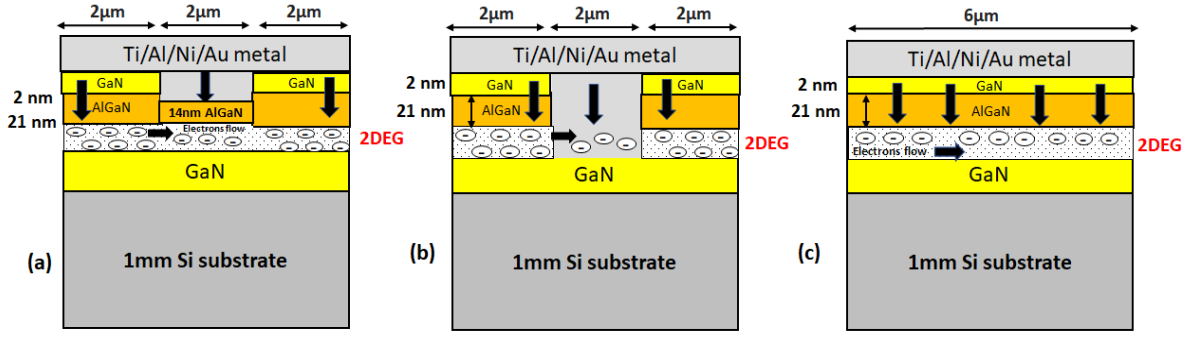


Figure 4.13. The cross-section schematic illustration of (a) shallow patterned etching (b) deep patterned etching (c) conventional or planar structure of Ohmic metal contact to AlGaN/GaN HEMT structures.

4.5.2.2 Device characterization

All fabricated devices were measured using the Keysight Agilent's B1500A semiconductor device analyser at room temperature. Figure 4.14 shows the measured output characteristics of the fabricated AlGaN/GaN HEMTs with a shallow (~ 9 nm etch depth) and deep (~ 30 nm etch depth) Ohmic recess etching of 3 different patterned Ohmic contacts and conventional or planar contact. The device with a conventional Ohmic contact on both samples exhibit a maximum saturation drain current of 970 mA/mm and 972 mA/mm. Note that there is no Ohmic recess etching for the device with a conventional Ohmic contact. As expected, the device with a horizontal patterned Ohmic contact shows higher maximum saturation drain current compared to other devices for both etching depths where the highest maximum saturation drain current of 1285 mA/mm was observed for a deep Ohmic recess. No obvious difference of maximum saturation drain current between devices with a vertical patterned and conventional Ohmic contacts while

the devices with a chess patterned Ohmic contacts show lower maximum saturation drain current both for shallow and deep Ohmic recess. The same trend was observed for the measured maximum transconductance of the fabricated devices. These results are in agreement with the measured contact resistances as observed in Figure 4.12.

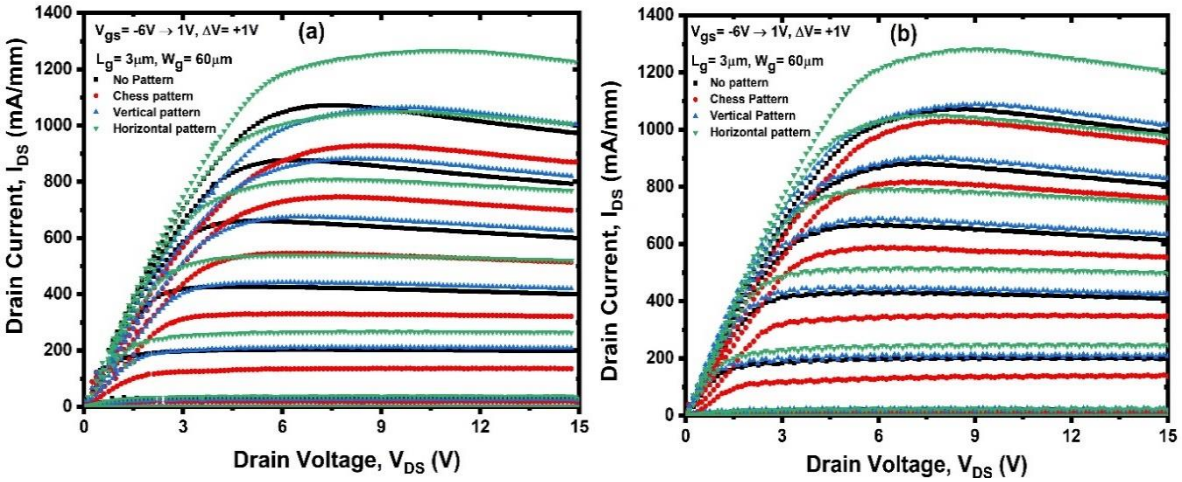


Figure 4.14: The measured output characteristics of the fabricated AlGaN/GaN HEMTs with a (a) shallow (b) deep patterned etching of 4 different TLM structure.

The transconductance characteristics of the fabricated AlGaN/GaN HEMTs measured at drain-to-source voltage, V_{ds} = 7 V are shown in Figure 4.15. The highest maximum transconductance was observed on the device with a horizontal patterned Ohmic contact which gives values of 284 mS/mm and 296 mS/mm for a shallow and deep Ohmic recess respectively. No obvious difference of maximum transconductance between devices with a vertical patterned Ohmic contact and conventional Ohmic contact structures while the device with a chess patterned Ohmic contact shows a lower maximum transconductance for both a shallow and deep Ohmic recess. The measured threshold voltage, V_{th} of - 4.1 V was observed and this value is consistent for all devices for a deep Ohmic recess. However, there is a shift toward the negative direction of the measured threshold voltage for devices with a horizontal and vertical patterned Ohmic contacts. This behaviour needs to be further investigated.

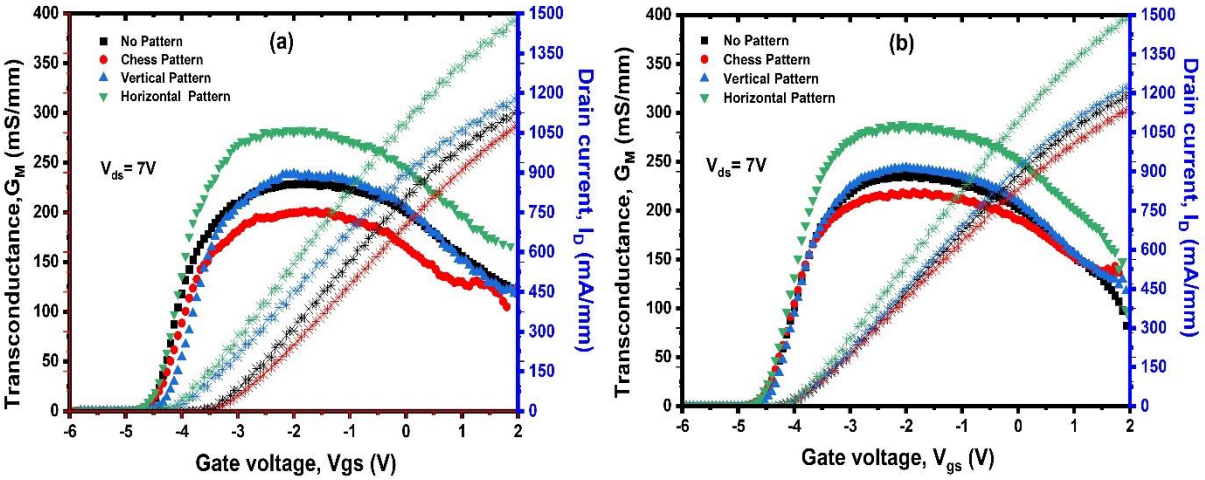


Figure 4.15. The measured transconductance of the fabricated AlGaN/GaN HEMTs with (a) shallow Ohmic recess etching (b) deep Ohmic recess etching with 4 different TLM pattern structures.

All devices exhibit lower gate leakage currents for a deep patterned Ohmic recess etch (compared to a shallow patterned Ohmic recess etch), where the lowest value is observed on the device with a horizontal patterned Ohmic contact as shown in Figure 4.16. These results corroborate the highest maximum saturation drain current and transconductance observed for this device. However, higher gate leakage currents were observed for devices with a shallow patterned Ohmic contacts compared to the device with a conventional Ohmic contact. The reason for this is not clear and needs further investigation.

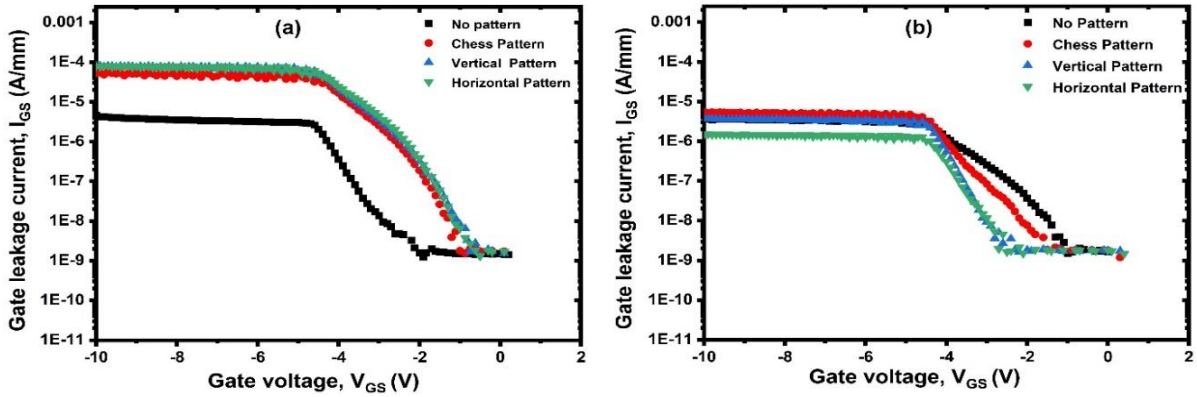


Figure 4.16: The gate leakage current characteristics of the fabricated AlGaN/GaN HEMTs with a (a) shallow Ohmic recess etching (b) deep Ohmic recess etching with 4 different TLM pattern structures.

4.6 Conclusion

This chapter provided an overview of GaN Ohmic contact technology as well as the fundamental metal-semiconductor interface theory. In this project, we have successfully fabricated and measured AlGaN/GaN HEMT devices using 3 different patterned Ohmic contact structures. The types of Ohmic contact patterns used were horizontal, vertical and chess. A device with a conventional Ohmic contact was also fabricated for comparison. Two etching depths were used were ~ 9 nm and ~ 30 nm resulting trenches above and below the 2DEG channel, respectively. The lowest contact resistance of 0.32 Ω.mm was observed for a deep horizontal patterned structure. The fabricated device with this structure also demonstrated the highest maximum saturation drain current of 1285 mA/mm, maximum transconductance of 296 mS/mm and gate leakage current of 1.5µA/mm which is better compared to other fabricated devices. We found that the uneven AlGaN layer thickness underneath the Ohmic metal contacts is responsible for reducing the Ohmic contact resistance. The formation of sidewall area on AlGaN surface during the patterned etching process provides better contact of Ohmic metal resulting in more tunnelling current between the Ohmic metal and AlGaN barrier thus reducing the contact resistance.

Chapter 5
GaN Buffer Thickness Study

5 Comparative study of buffer thickness in AlGaN/GaN HEMTs on SiC substrates

5.1 Introduction

Silicon carbide (SiC) is the substrate of choice for high-power RF applications due to its exceptional thermal conductivity, which greatly enhances device performance. To overcome lattice mismatch and reduce dislocation density in Gallium Nitride-on-SiC (GaN-on-SiC) structures, a specific growth strategy is employed. This involves the initial growth of an aluminium gallium nitride (AlN) nucleation layer (NL) with deliberately reduced crystalline quality. Subsequently, a GaN buffer layer, several micro-meters thick, is grown, and it is doped with deep acceptors such as iron (Fe) or carbon (C). These acceptors serve to compensate for any residual doping effects in the n-type GaN layer.[145] [146]. Silicon and oxygen impurities are the two prime shallow donor in GaN [147][148]. It's worth noting that silicon and oxygen impurities are the primary shallow donors in GaN. They introduce donor states, which increase the concentration of electron carriers while simultaneously lowering the resistivity of the buffer layer. However, this approach has some drawbacks. It degrades the overall thermal resistance of the structure, which diminishes the advantage of using a SiC substrate as an effective heatsink [149]. Furthermore, the introduction of acceptor-type impurities in a thick GaN buffer creates deep charge trapping area. These area have adverse effects, including an increase in low-frequency noise and the promotion of current collapse effects in High Electron Mobility Transistors (HEMTs) [150].

In the realm of Gallium Nitride-based High Electron Mobility Transistor (HEMT) heterostructures, the quality of GaN buffers holds immense importance. These buffers need to exhibit high resistance characteristics to achieve exceptional device isolation and to enhance the Radio Frequency (RF) performance of GaN-based HEMTs. The design of these buffers plays a pivotal role in shaping the epitaxial layer structure and the overall fabrication of AlGaN/GaN HEMT devices. When GaN buffers fail to maintain high resistance properties, several issues can arise. One critical concern is the inadequate confinement of electrons and the exacerbation of the Short Channel Effect (SCE). A "leaky" buffer hinders the attainment of high operating frequencies, thereby negatively impacting the device's performance. This can manifest as an increase in off-state leakage current, dielectric breakdown, or sudden spikes in current due to unintended additional leakage paths within the III-nitride heterostructure [151]. In addition, the quality of the heterostructure and the dielectric layers deposited on the buffer have a significant impact on electron trapping phenomena. These trapping-related effects can negatively impact the device's dynamic performance.

In the heterostructure interfaces, the buffer layer, or on the surface of III-nitride materials, electrons can enter acceptor-like states when subjected to off-state stress conditions. These electron traps may exhibit a slower release time compared to when transitioning from an off state to an on state[152].

To mitigate and eliminate these adverse effects, it becomes imperative to finely optimize both the growth process of GaN materials and the parameters involved in the fabrication of the device. This optimization effort is crucial for maintaining the desired electron population in the 2DEG during device operation, thereby ensuring the desired on-state current and overall device performance.

In some designs, an AlGaN back barrier layer replaces the buffer layer. The back barrier refers to a thin high bandgap layer of material that is grown between the substrate and the channel layer. The purpose of the AlGaN back barrier is to improve the electrical performance of the device by reducing the number of electrons that are trapped at the interface between the GaN channel and the substrate. The AlGaN back barrier has a wider band-gap compared to the conventional GaN buffer layer and it improves 2DEG confinement in the channel and breakdown voltage of the GaN HEMT [67]. The motivation of using the Buffer free GaN HEMTs due to the following reasons[153][154][155]:

- GaN HEMTs without a buffer are more efficient because they lose less power during transition.
- They are appropriate for high-frequency applications because they can switch faster than conventional FETs.
- They are less susceptible to noise, which increases their dependability in congested environments.
- They can be made smaller than conventional FETs, making them suitable for applications with limited space and portability.
- They are utilised in numerous applications, such as power amplifiers, RF converters, switching power supplies, and high-speed circuits.

This chapter discusses the two primary buffer design options outlined previously, i.e. conventional buffer design, and buffer-free HEMT heterostructure. Buffer-free GaN HEMTs have several advantages over standard GaN HEMTs with a buffer layer:

Lower trapping: The buffer layer in standard GaN HEMTs can trap electrons, which can reduce the device's performance. Buffer-free GaN HEMTs have a lower trapping rate, which can lead to higher output power and efficiency.

Better carrier confinement: The buffer layer in standard GaN HEMTs can also scatter electrons, which can reduce the device's frequency response. Buffer-free GaN HEMTs have better carrier confinement, which can lead to higher operating frequencies [153].

Lower thermal resistance: The buffer layer in standard GaN HEMTs can act as a thermal barrier, which can make it difficult to dissipate heat from the device. Buffer-free GaN HEMTs have lower thermal resistance, which can lead to better thermal management and improved reliability [156] .

Overall, buffer-free GaN HEMTs offer a number of advantages over standard GaN HEMTs with a buffer layer. These advantages can lead to higher performance, higher frequency response, and improved reliability. The conventional structure is shown Figure 5.1 and comprises: (1) an AlN nucleation layer, (2) a thick C or Fe-doped GaN buffer layer, (3) a UID-GaN layer, (4) an AlGaN barrier layer, and (5) GaN cap layer.

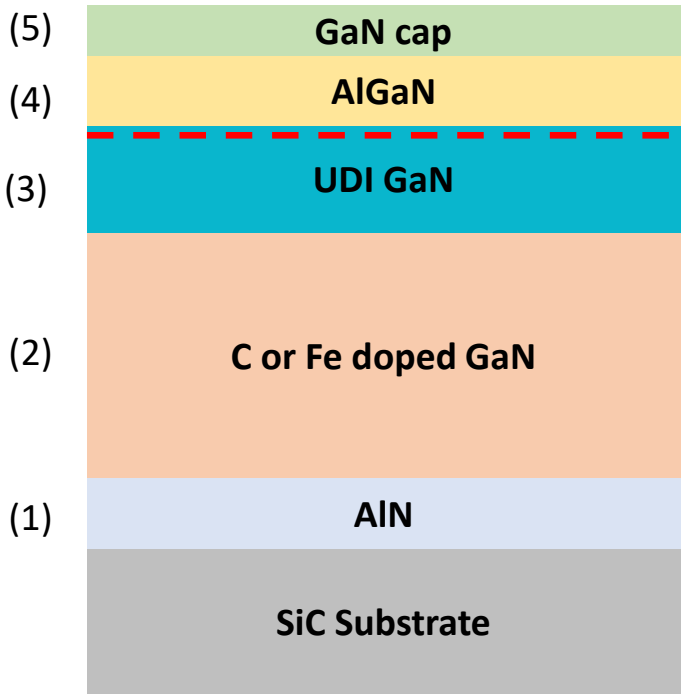


Figure 5.1: A conventional AlGaN/GaN heterostructure with a significant C or Fe doping in the buffer layer.

5.1.1 Buffer-free GaN heterostructure

AlGaN/GaN based HEMTs commonly use a thick GaN buffer of approximately ~ 2 micrometres to attain good crystalline quality close to the 2DEG and better device performance. However, achieving the same level of crystalline quality with a thinner GaN buffer offers numerous advantages. Thick-GaN buffers increase the bow of the structure, resulting in reduced device yield during fabrication, whereas thin-GaN buffers minimise the bow [157] [158]. In addition, during device operation, heat dissipation is a significant concern, and a thin-GaN buffer significantly reduces the total thermal resistance, resulting in a lower device channel temperature. In order to decrease leakage currents, improve breakdown voltages, and minimize short-channel effects, the buffer needs to be extremely insulating.

Recently, a new technique based on buffer-free epitaxy was reported. A buffer-less AlGaN/GaN heterostructure is shown in Figure 5.2 and comprises: (1) an AlN nucleation layer, (2) a UID-GaN layer, (3) an AlGaN barrier layer, and (4) GaN cap layer. Several advantages are expected using this new concept of epitaxial layers. A thin-GaN buffer significantly reduces the total thermal resistance, resulting the reduction of the device self-heating since the heat generated in the thin GaN channel would dissipate more efficiently into the substrate, less charge trapping effects since the thin GaN layer is unintentionally doped and the thin AlN nucleation layer could effectively serve as a back barrier layer to enhance the carrier confinement in the channel for high-frequency applications [159]. Moreover, the use of thin-GaN (~250 nm) reduces material consumption significantly (~ 80%). To date, few works have been reported using the buffer-free GaN heterostructure where the demonstrated devices were comparable with the devices fabricated on the conventional heterostructure employing a thick GaN buffer layer [156] [160] [161].

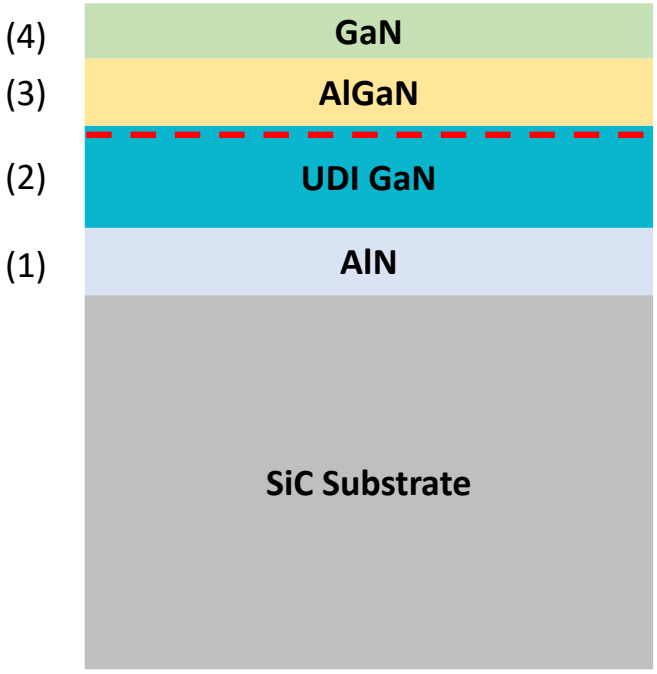


Figure 5.2: A buffer-less AlGaN/GaN heterostructure.

5.2 Experimental results

5.2.1 Device structure and fabrication

The epitaxial structures used in this work were grown by SweGaN commercial wafer suppliers, using hot wall metal oxide chemical vapour deposition (MOCVD) on a semi-insulating SiC substrate. The main difference between the wafers is the GaN buffer and AlN nucleation layer thickness. The structure of Wafer 1 consists of (from top to bottom) a 1 nm GaN cap layer, 16 nm thick AlGaN barrier with 31% Al content, a Fe doped - 1.6 µm GaN channel layer and low thermal boundary resistance 35nm AlN nucleation layer, while wafer 2 has a 2 nm GaN cap, a thinner 14 nm AlGaN barrier with 30% Al content, a 1 nm AlN spacer

layer, and an ultra-thin 250nm unintentionally doped (UID) GaN channel layer and very low thermal boundary resistance [162] and high quality 60nm AlN nucleation layer.

Details of the material properties for both heterostructures are enumerated in the Table 5-1. Wafer 1 exhibits lower average sheet resistance and higher 2DEG mobility and density due to the higher Al concentration in the AlGaN barrier layer and also due to the AlN spacer layer which increase the polarization effects at the quantum well. Wafer 2 shows that the 2DEG transport properties were not compromised when significantly reducing the GaN channel layer thickness.

Table 5-1: As-grown material properties for both heterostructures both wafers measured by manufacturers.

Material properties	Thick buffer wafer	Buffer-free wafer
2DEG	$1.2 \times 10^{13} cm^{-2}$	$1 \times 10^{13} cm^{-2}$
Mobility	>1900 cm^2/Vs	>2000 cm^2/Vs
Sheet resistance	~ 270 Ω/Sq	~ 330 Ω/Sq

Device fabrication started with the Ohmic metal contacts formed by the evaporation of Ti/Al/Ni/Au (30/180/40/100nm), followed by a lift-off process, then rapid thermal annealing at 800 °C for 30 secs. Next, mesa isolation was performed using the inductively coupled plasma (ICP180) with Cl_2/Ar gases at 30/15 sccm, RF/DC power of 75/750 W, and pressure of 4 mTorr, to achieve an etch depth of 100 nm. The gate metal contacts were formed by evaporation of Ni/Au (20/200 nm), followed by evaporation of bond pad metal contacts of Ti/Au (20/400 nm). A blanket deposition of 100 nm of Si_3N_4 grown using plasma-enhanced chemical vapour deposition (PECVD) at 300 °C was used for surface passivation. Finally, the Si_3N_4 layer in the Ohmic and gate regions was etched using SF_6/N_2 to allow probed access for device measurements. The details of the device optimization process can be found in [163] [164].
All fabrication steps were defined using photolithography. DC and RF measurements were made at room temperature using Keysight's B1500A Semiconductor Device Analyzer and E8361A PNA Network Analyzer, respectively. The epitaxial wafer diagram of the fabricated devices using a thick GaN layer and a buffer-free is illustrated in Figures 5.3(a) and 5.3(b) respectively. Figure 5.3(c) shows the micrograph of the fabricated 200 µm wide device. Device dimensions used in this work are as follows: gate length, L_G = 2 µm, gate-to-source distance, L_{GS} = 2 µm, gate-to-drain distance, L_{GD} = 3 µm and gate widths of 2 × 50 µm and 2 × 200 µm.

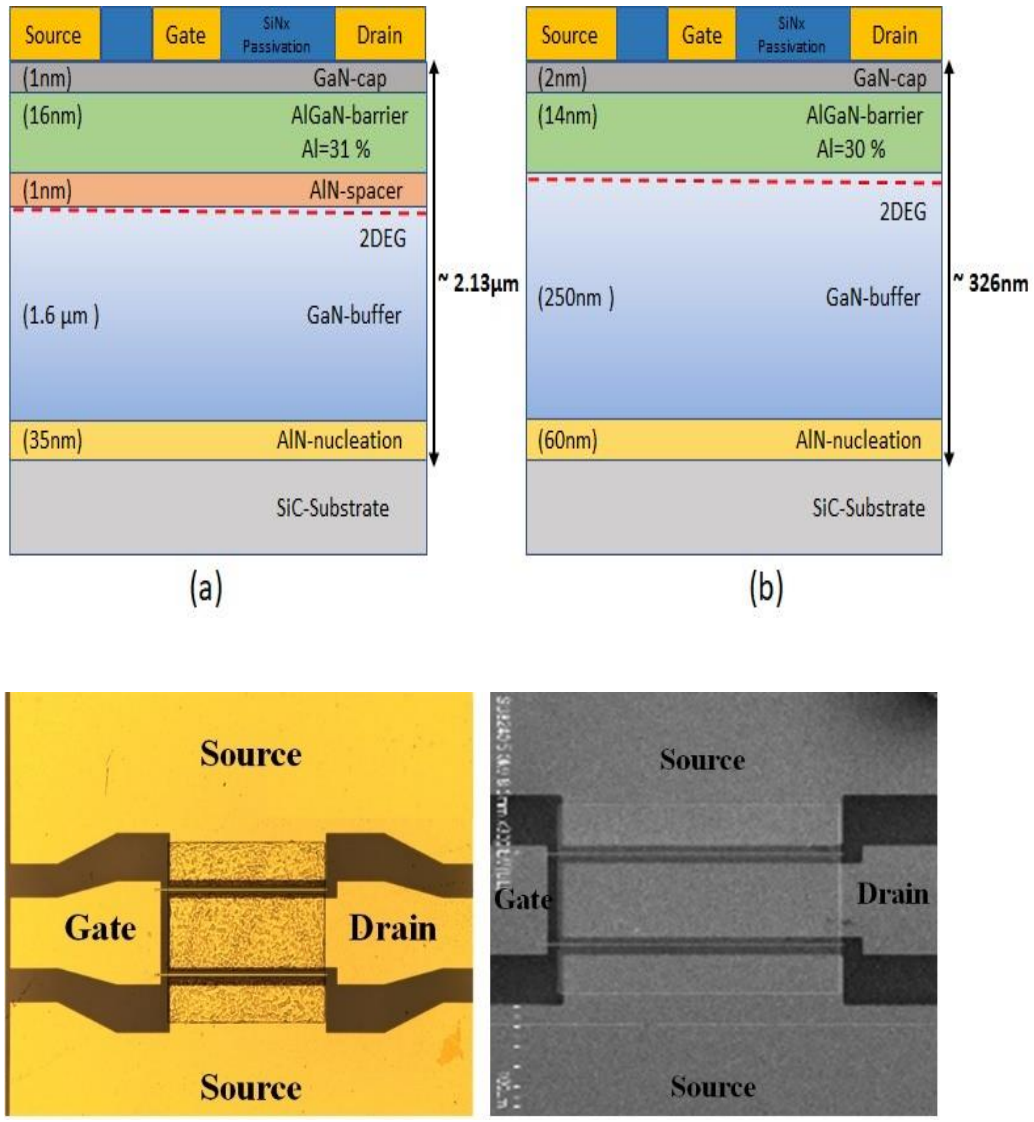


Figure 5.3: Epitaxial wafer structure of fabricated AlGaN/GaN heterostructure devices using (a) a thick GaN layer and (b) a buffer-free (c) Micrograph of fabricated 200µm wide device.

5.2.2 Result and discussion

To evaluate the contact resistance, R_C, for both heterostructures the circular transmission line model (CTLM) structure was fabricated on both epitaxial layer structures. Figure 5.4 shows the comparison between the buffer-free and the thick GaN buffer Ohmic contact measurements. No significance difference is observed in the measured contact resistance between these two samples. The extracted contact resistance values of 0.65 Ω.mm and 0.59 Ω.mm µm for the buffer-free and the thick GaN buffer Ohmic contact structures, respectively.

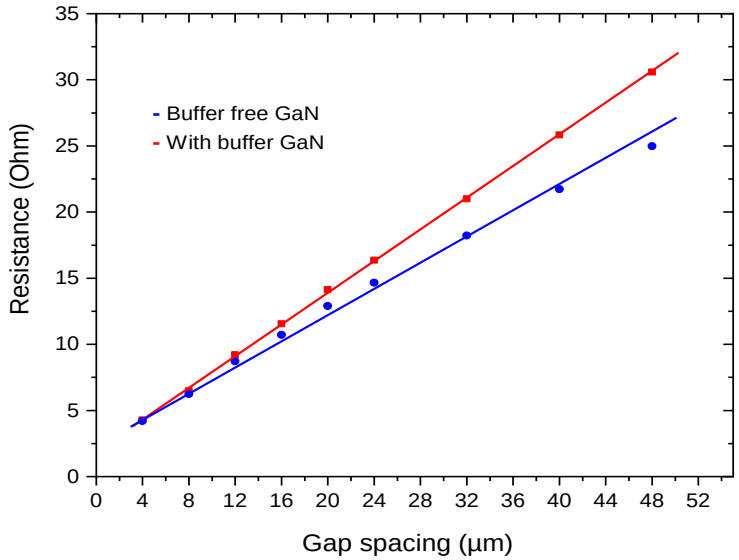


Figure 5.4: Measured contact resistance versus gap spacing of thick GaN buffer and buffer-free GaN wafers.

The fabricated buffer-free AlGaN/GaN HEMT devices with a 2-µm gate long, two-finger 2 × 50 µm and 2 × 200 µm gate widths demonstrate a maximum drain current density of ~631 mA/mm and ~ 462 mA/mm biased at V_{GS} = 1 V respectively. In comparison, the fabricated thick buffer AlGaN/GaN HEMT devices with a 2-µm gate long, two-finger 2 × 50 µm and 2 × 200 µm gate widths demonstrate a maximum drain current density of ~ 686 mA/mm and ~ 512 mA/mm biased at V_{GS} = 1 V respectively, as shown in Figure 5.5 and Figure 5.6.

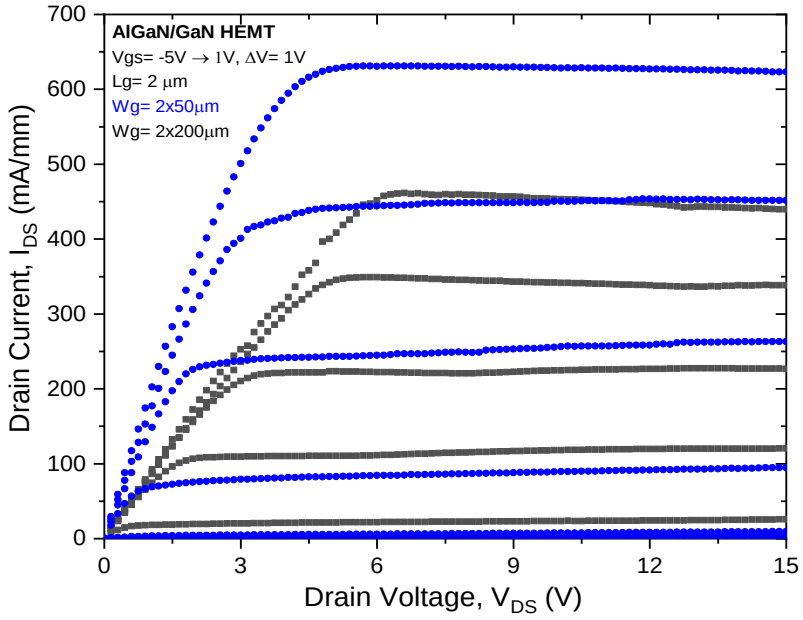


Figure 5.5: The I_{DS}-V_{DS} characteristics for 50 and 200 µm wide devices on buffer-free GaN wafer.

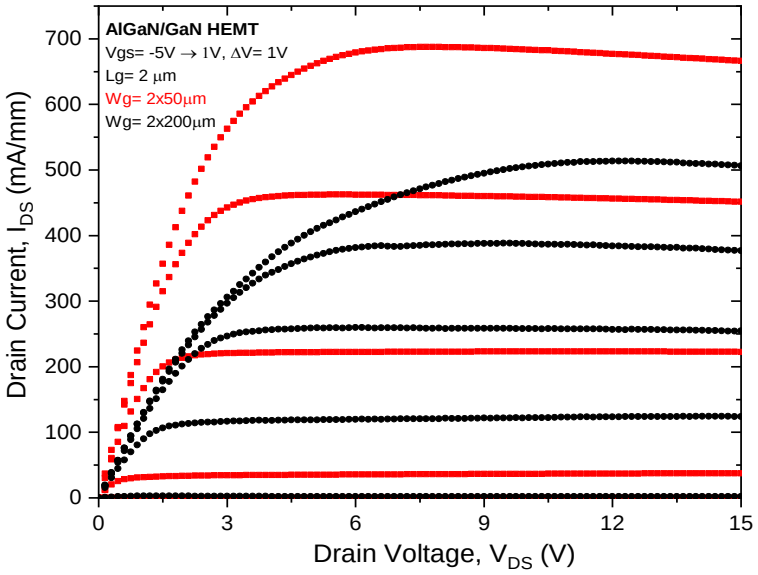


Figure 5.6: The I_{DS}-V_{DS} characteristics for 50 and 200 µm wide devices on thick- GaN buffer wafer.

Again, there is no significance difference is observed in the measured maximum current density, $I_{DS\,(max)}$, and maximum peak transconductance, $g_{m(max)}$, between these two samples.

Figure 5.7 showed measured DC-IV up to the higher drain bias voltage V_{ds} = 40V and V_{gs} at 0V for thick buffer wafer and buffer free wafer. They showed negligible self-heating effect in both wafers.

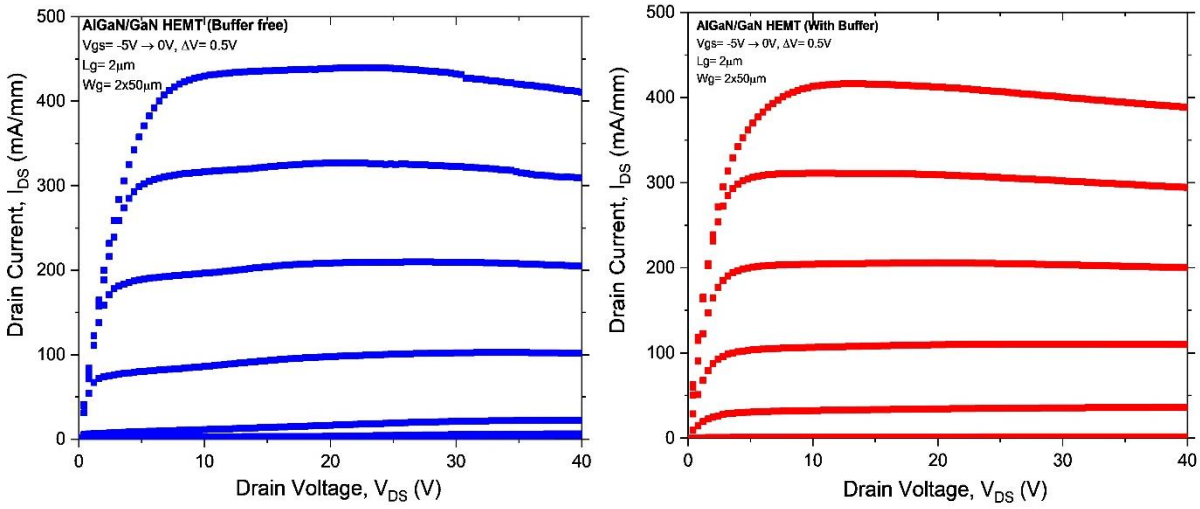


Figure 5.7: The I_{DS}-V_{DS} characteristics of 2 x 50 µm wide devices at V_{GS} = 0V to -5V and V_{DS} up to 40V on buffer free wafer and thick GaN buffer wafer.

These results indicate that the measured output characteristics of buffer-free AlGaN/GaN HEMT devices are comparable with the thick buffer AlGaN/GaN HEMT devices. In addition, the obtained results show an expected higher $I_{DS(max)}$ and $g_{m(max)}$ compared to the previous published work using the similar buffer-free

AlGaN/GaN heterostructure with device gate length of 5 µm [165]. The slightly higher currents in the thick buffer design are attributed to the higher 2DEG concentration, see Table 5-1.

The maximum peak transconductance, $g_{m(max)}$, of ~ 181.7 mS/mm and ~ 202 mS/mm biased at the V_{DS} = 5 V for buffer-free and thick buffer AlGaN/GaN HEMT devices with a 2-µm gate long, two-finger 2 × 50 µm gate width, respectively. The measured threshold voltage, V_{TH}, of – 2.6 V and – 3.6 V (extracted value of gate-to-source voltage, V_{GS} at I_{DS} = 1 mA/mm) were obtained for buffer-free and thick buffer AlGaN/GaN HEMT devices with a 2-µm gate long, two-finger 2 × 50 µm gate width, respectively, as shown in Figure 5.8. There is a shift to a more positive value of the measured threshold voltage for buffer-free AlGaN/GaN HEMT device compared to the thick buffer device due to the usage of thinner AlGaN barrier layer (14 nm of AlGaN).

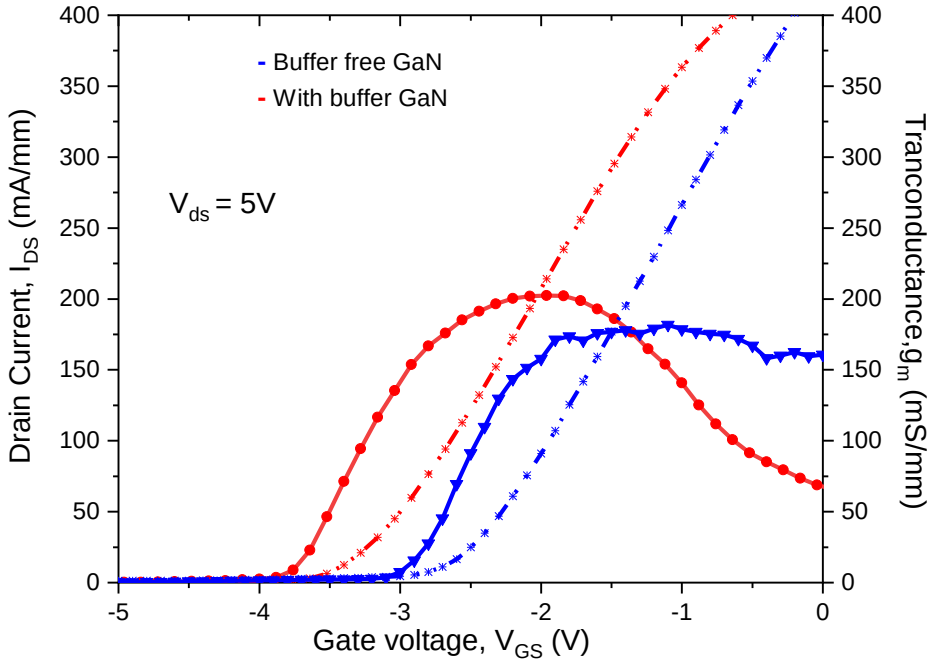


Figure 5.8: Measured transfer characteristics of (a) buffer-free (b) thick GaN buffer devices biased at V_{DS} = 5 V.

Lower gate leakage currents were observed for the fabricated buffer-free AlGaN/GaN HEMT device with a 2-µm gate long, two-finger 2 × 50 µm gate width as compared to the thick GaN buffer AlGaN/GaN HEMT device as shown in Figure 5.9. The higher gate leakage current for with buffer GaN is attributed to the electron trapping in the thick buffer layer. So, it can be concluded that the hot-wall MOCVD growth process for buffer free GaN is beneficial for improving the device performance. Note that gate leakage could be reduced also by improving the mesa isolation process.

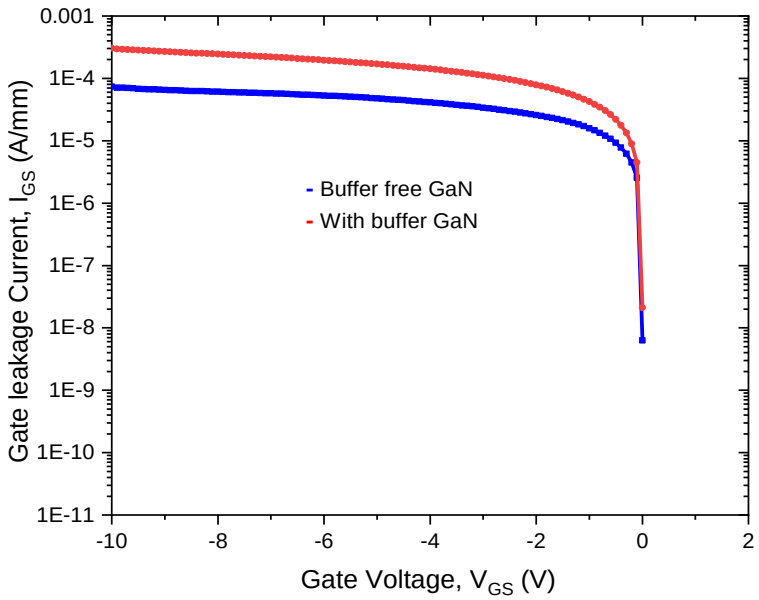


Figure 5.9: Measured gate leakage currents of (a) buffer-free (b) thick GaN buffer devices with a 2-µm gate long, two-finger 2 x 50 µm wide biased at V_{DS} = 0 V

The measured off-state breakdown voltage, V_{BR}, for fabricated buffer-free AlGaN/GaN HEMT device with a 2-µm gate long, two-finger 2 × 50 µm gate width exceeds the maximum compliance of the measurement set up of 200 V as compared to the thick GaN buffer AlGaN/GaN HEMT device with the V_{BR} of 186 V as shown in Figure 5.10.

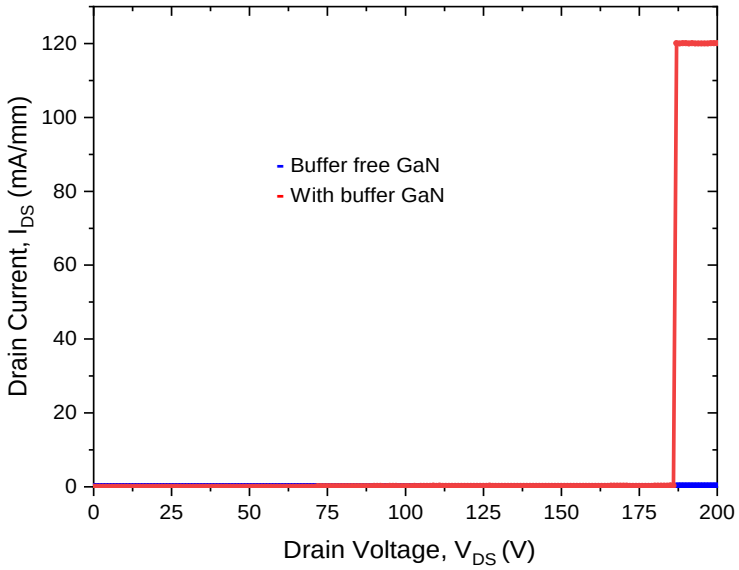


Figure 5.10: Measured off-state breakdown voltage of (a) buffer-free (b) thick GaN buffer devices with a 2- µm gate long, two-finger 2 x 50 µm wide biased at V_{GS} = -10 V

S-parameter measurements were done on both the wafer devices biased at V_{GS} = -2 V corresponding to peak transconductance. The RF performance measured on buffer-free and thick buffer small signal of the device were shown in Figure 5.11. In the buffer-free devices, the measured maximum cut-off frequency, f_T, and maximum oscillation frequency, f_{max}, of 4.6 GHz and 9.8 GHz were obtained for a two-finger 2 × 200 µm device biased at V_{DS} = 15 V. For the thick buffer design, a two-finger, 2 × 200 m device biased at V_{DS} = 15 V was found to have a f_T and f_{max} of 6.3 GHz and 14.7 GHz, respectively. The difference in frequency performance was attributed to the higher internal parasitics of the buffer-free devices.

The internal parasitics of a device are the electrical components that are not intentionally designed into the device but are present due to the manufacturing process. These parasitics can include capacitances, inductances, and resistances [166] [167]. In the case of buffer-free GaN HEMTs, the higher internal parasitics are due to the lack of a buffer layer. The parasitic effects of the bond pads were not de-embedded. Extrapolated cut off frequencies (f_T) and maximum oscillating frequencies (f_{MAX}) are provided in Table 5-2.

Table 5-2 :Extrapolated f_T and f_{MAX} values from S-parameter measurements of buffer free and thick buffer devices at V_{DS} = 15 V.

Wafer	Device size	F_T (GHz)	F_{MAX} (GHz)
		V_{DS} = 15V	V_{DS} = 15V
Buffer free GaN	2x200 µm	4.6	9.8
Thick Buffer	2x200 µm	6.3	14.7

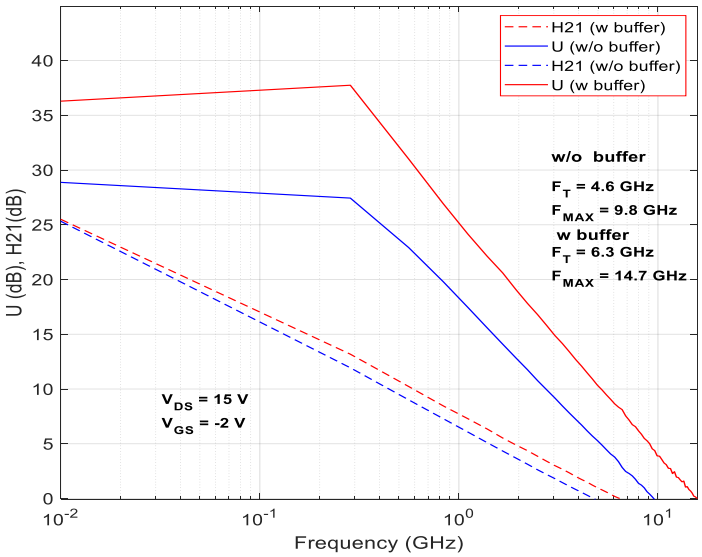


Figure 5.11: Measured H21 and Maximum signal gain for 2x200µm device sizes for buffer and buffer free devices.

5.3 Conventional and buffer-free MOCVD-grown GaN HEMTs

In this section, we investigated the thermal performance of two standard GaN HEMT epitaxial structures grown by metal organic chemical vapour deposition (MOCVD) on high thermal conductivity 4H-SiC wafers supplied from two commercial wafer vendors, supplier A (wafer 1) and SweGaN (wafer 2). The AlN layer growth conditions of the MOCVD methods, which result in different nucleation layer quality and required thicknesses, and the presence/absence of a buffer layer are the primary differences between the wafers. The wafer 2 grown was by hot wall MOCVD method. The epilayer structure of wafer 1 had 2 nm GaN cap, 20 nm of thickness of AlGaN barrier layer with 25% Al concentration and thick 1.8 µm of C-doped GaN buffer with 200nm GaN channel layer. Wafer 2 had a 2 nm GaN cap layer, 14 nm of thin layer of AlGaN barrier layer with 30% of Al concentration and 250 nm of undoped GaN channel layer. The epitaxial layer structures of both wafers are shown in Figure 5.12. In comparison to Wafer 1, which was grown using a standard growth procedure and contains an AlN nucleation layer that is 200 nm thick, Wafer 2 was claimed to have ultra-low thermal boundary resistance due to an optimised wafer growth process employing the hot-wall MOCVD growth technology and used of only 60nm AlN thin nucleation layer.

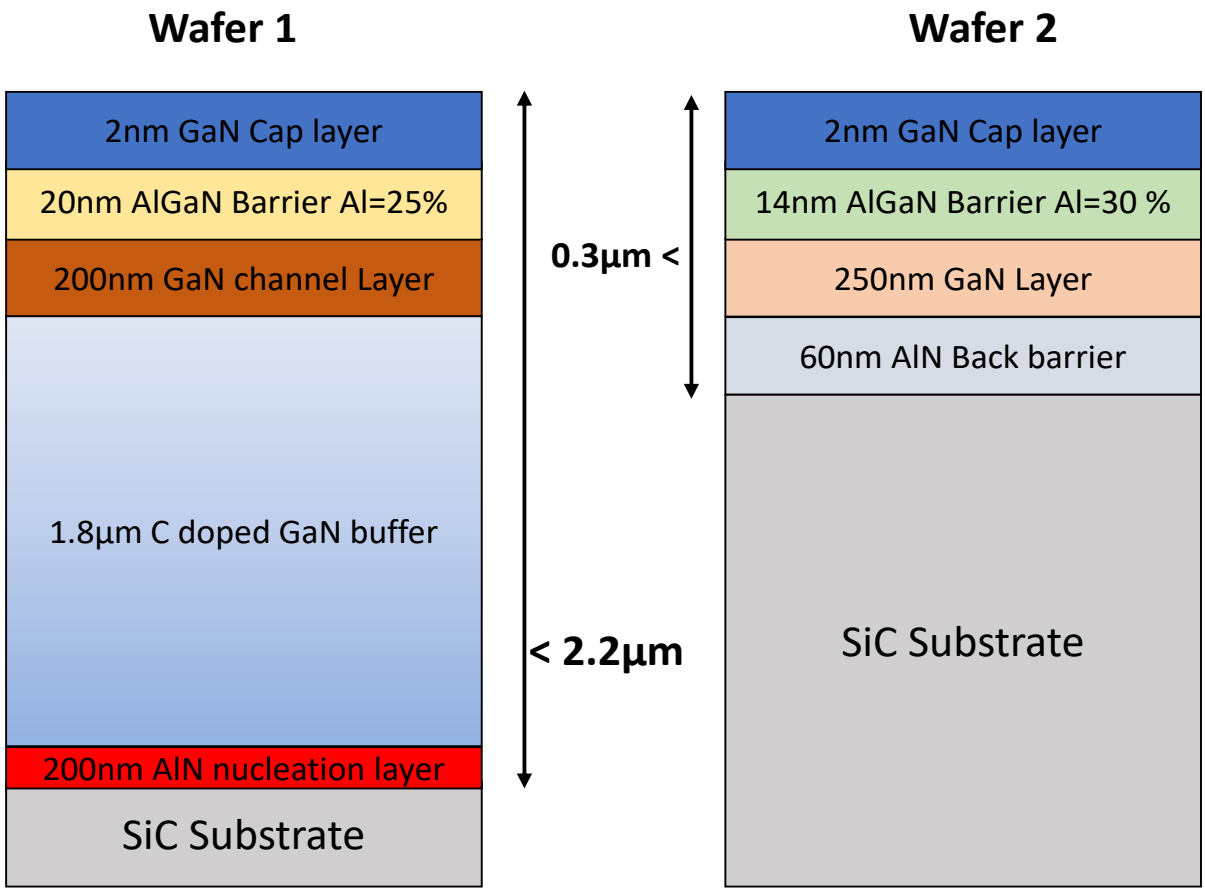


Figure 5.12: Standard GaN-on-SiC epitaxial layer wafer structures for comparison in terms of the device thermal performance.

Table 5.3 showed the manufacturers' average sheet resistivity, 2DEG mobility and density. Because of the greater Al concentration in the AlGaN barrier layer and the AlN spacer layer, Wafer 2 has lower average sheet resistance and higher 2DEG mobility and density.

Table 5-3: Manufacturers evaluated the 2DEG mobility, density, and average sheet resistances for both wafers.

	Wafer 1 (commercial)	**Wafer 2 (buffer free)**
2DEG mobility, μ_e	1400 cm^2/Vs	2000 cm^2/Vs
2DEG density, n_s	$1 \times 10^{13}\ cm^{-2}$	$1 \times 10^{13}\ cm^{-2}$
Average sheet resistance	406 Ω/□	330 Ω/□

5.3.1 Device measurement results

To assess the thermal performance of the devices, two finger devices were concurrently fabricated on each wafer, each having a gate length of 2 µm and gate width of 50 µm. All the fabrication of the devices was done by using photolithography as described in chapter 4 Section 4.5.1. In Figure 5.13, a micrograph of the manufactured device that is 2 × 50 µm wide is depicted. Ohmic contact resistances were extracted from transmission line method (TLM) tests for wafers 1 and 2 as 0.58 mm and 0.6 mm, respectively.

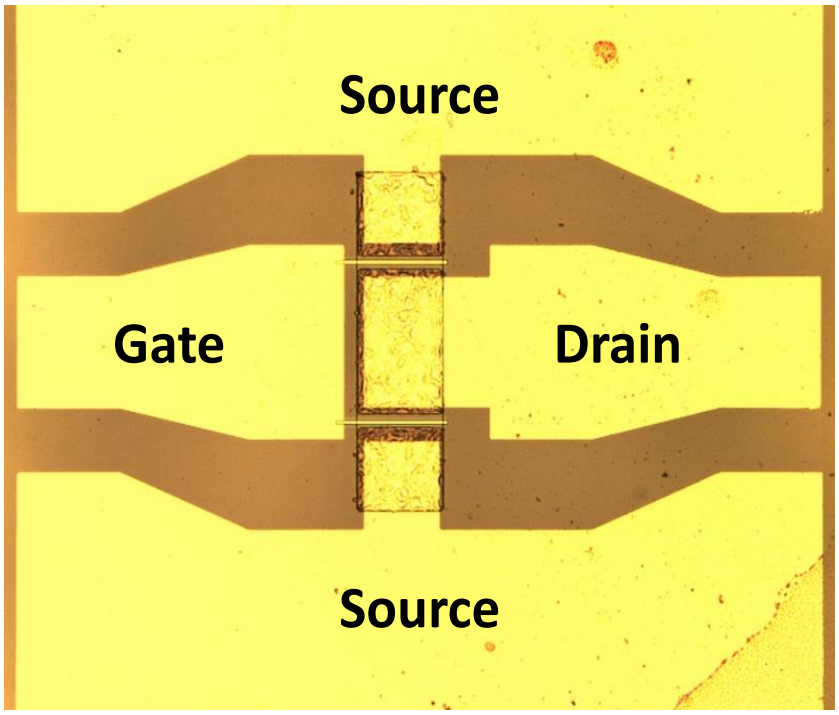


Figure 5.13: Micrograph of the fabricated 2×50 µm wide device with gate-length of 2 µm.

DC-IV measurements were done on a 2 × 50 µm wide device and are shown in Figure 5.14. Wafers 1 and 2 exhibit a maximum drain current density of 455 mA/mm and 712 mA/mm at a gate voltage of 1V, respectively.

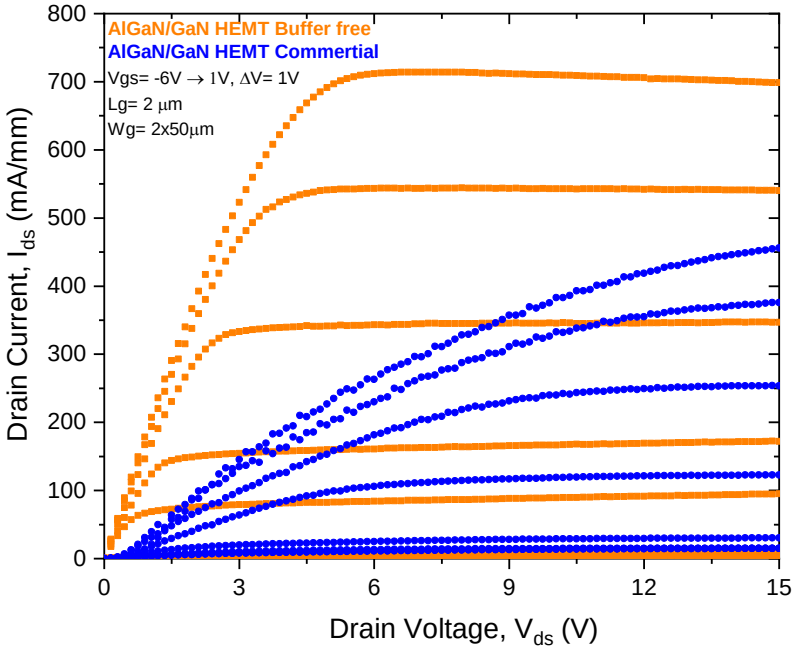


Figure 5.14: I_{DS}-V_{DS} characteristics for 50 µm wide devices on Wafer 1 (commercial) and 2 (buffer-free from SweGaN).

Figure 5.15 depicts the transconductance of two devices, each 50 µm in width, from both wafers. The transconductance of Wafer 2 is larger than that of Wafer 1 and the peak transconductances of the devices on wafers 1 and 2 are 81 mS/mm and 187 mS/mm, respectively.

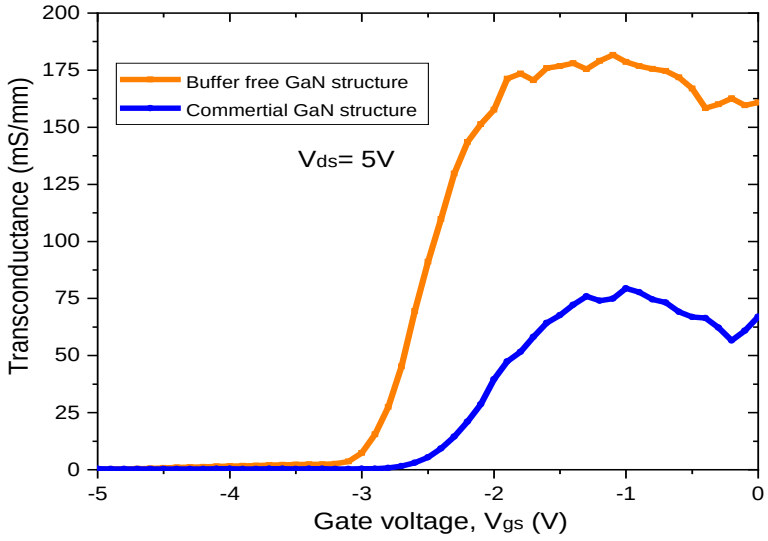


Figure 5.15: Transconductance (g_m) characteristics of the wafer 1 (commercial) and wafer 2 (buffer free) devices.

Figure 5.16 depicts the gate leakage currents of the two devices up to a gate voltage of -10 V. The leakage current for the devices on Wafers 1 and 2 is 2.1 x 10^{-4} A/mm and 4.6 x 10^{-4} A/mm at V_{GS} of -10V, respectively. Devices on Wafer 1 have greater gate leakage current possibly due to the thick barrier layer and thick buffer layers and the trap associated with these regions. Wafer 2, featuring a thin barrier layer and buffer-less structure, exhibits lower gate leakage compared to Wafer 1. Note that in general, improving the mesa isolation technique would also help lower the gate leakage current of the devices.

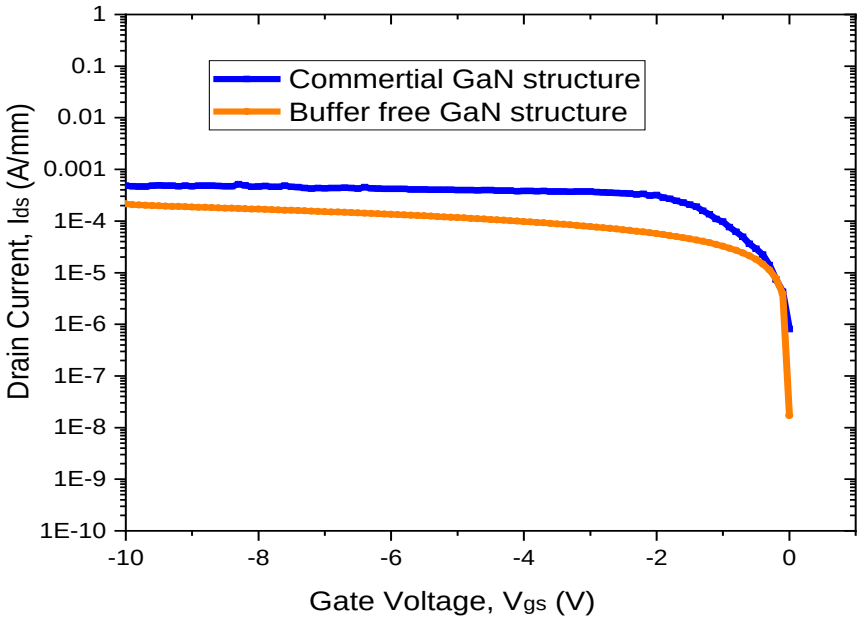


Figure 5.16: Gate leakage comparison of devices on wafer 1 (commercial) and wafer 2 (buffer free) devices.

The off-state three-terminal drain-source breakdown characteristics of the fabricated HEMTs from Wafers 1 and 2 were measured in order to analyse the breakdown behaviour and the findings are given in Figure 5.17. The devices were biased at gate voltage V_{GS} of -10V. The drain voltage at a gate current of 1mA/mm is defined as the breakdown voltage, V_{BR}, and it is consistent with the rapidly rising currents caused on by avalanche breakdown. The breakdown voltage of Wafer 1 was 189 V and Wafer 2 was over 200 V. This result on Wafer 2 further shows the high quality of the epitaxial layer structure. The measured results described above show the potential of this “buffer-free” structure for future microwave and millimetre-wave applications.

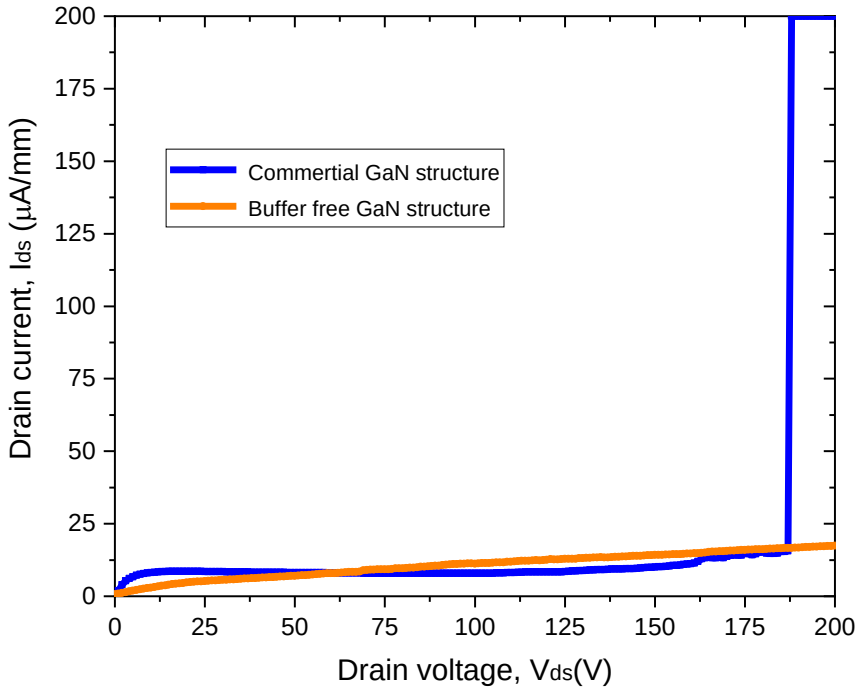


Figure 5.17: Breakdown characteristics of wafer 1 (commercial) and wafer 2 (buffer free) devices.

5.4 Conclusion

We have described a comparative experimental study of conventional (with buffer layer) and new buffer-free GaN HEMTs for microwave applications in terms of DC and S-parameter measurement. The DC and small-signal performances of the buffer-free GaN devices are comparable with the devices fabricated on the conventional heterostructure employing a thick GaN buffer layer. Also, the electrical performance of a novel "buffer-free" GaN HEMT was assessed. Compared to the commercial designs, the buffer-free devices exhibited lower gate leakage current (203 μA/mm) and improved the off-state breakdown voltages, above 200 V for 2 × 50 μm wide devices. The buffer-less devices also showed higher current density 712 mA/mm as compared to commercial wafer. These results demonstrate the high quality of the buffer-free GaN heterostructure despite the absence of thick transition layers as currently used in the conventional GaN HEMTs.

Chapter 6
Thermally Efficient GaN HEMT Devices

6 Thermally Efficient GaN HEMT Devices

6.1 Introduction

AlGaN/GaN HEMTs have been widely studied for high-power and high-frequency applications. It is crucial to remove the heat generated by power loss in a device when using a high-power density technology like GaN-on-SiC. Saturated drain currents, transconductance, gain of device, and output power are all drastically decreased when the junction temperature rises if effective heat extraction procedures are not used. One of the biggest obstacles facing modern GaN HEMT technology is thermal management. This is about extracting heat from the device and reducing the amount of heat that the device generates.

A major goal of this research was to investigate and develop novel approaches to the thermal management of GaN based devices. In this section, will discuss the role and effect of the nucleation layer between the substrate and GaN layer thickness, choice of substrate materials, and provide a literature review on thermal management techniques. We will describe an experimental comparative study on two different growths of GaN-on-SiC devices with different AlN nucleation layer thicknesses, and a novel method of heat extraction from the device where the nitride material around the device is removed to expose the SiC substrate on which the device bond-pads are deposited, and so the substrate acts as a heat sink.

6.2 Thermal management of GaN HEMTs

It has been shown that the DC biassing point primarily controls device heating, making changes in temperature and its distribution independent of the RF signal. For high RF power applications, good thermal management is crucial to decrease channel temperature and self-heating effect, which ensures output power performances for GaN-based HEMT [168].

As discussed earlier in chapter 2 section 2.4.1, GaN HEMTs are grown mostly on three popular substrate types: silicon, sapphire, and silicon carbide (SiC). Sapphire's thermal conductivity is 35 W/mK, for Si is 150 W/mK, for SiC 400 W/mK, and for diamond 2000 W/mK. Figure 6.1 illustrates the standard AlGaN/GaN HEMT with three arrows showing how heat flows from the channel layer to the substrate. Heat transport across the AlGaN/GaN interface, nucleation layer, and substrate interfaces plays a significant influence in defining the overall GaN HEMT performance. As a result of the scattering of thermal energy carriers (electrons and phonons), a thermal boundary resistance (TBR) appears between the different materials, and a temperature discontinuity occurs across the interface. The thermal resistance is calculated by dividing the maximum temperature rise by the power dissipated by the device. Also given are the thermal conductivities of the most common epi-layers and substrates [169].

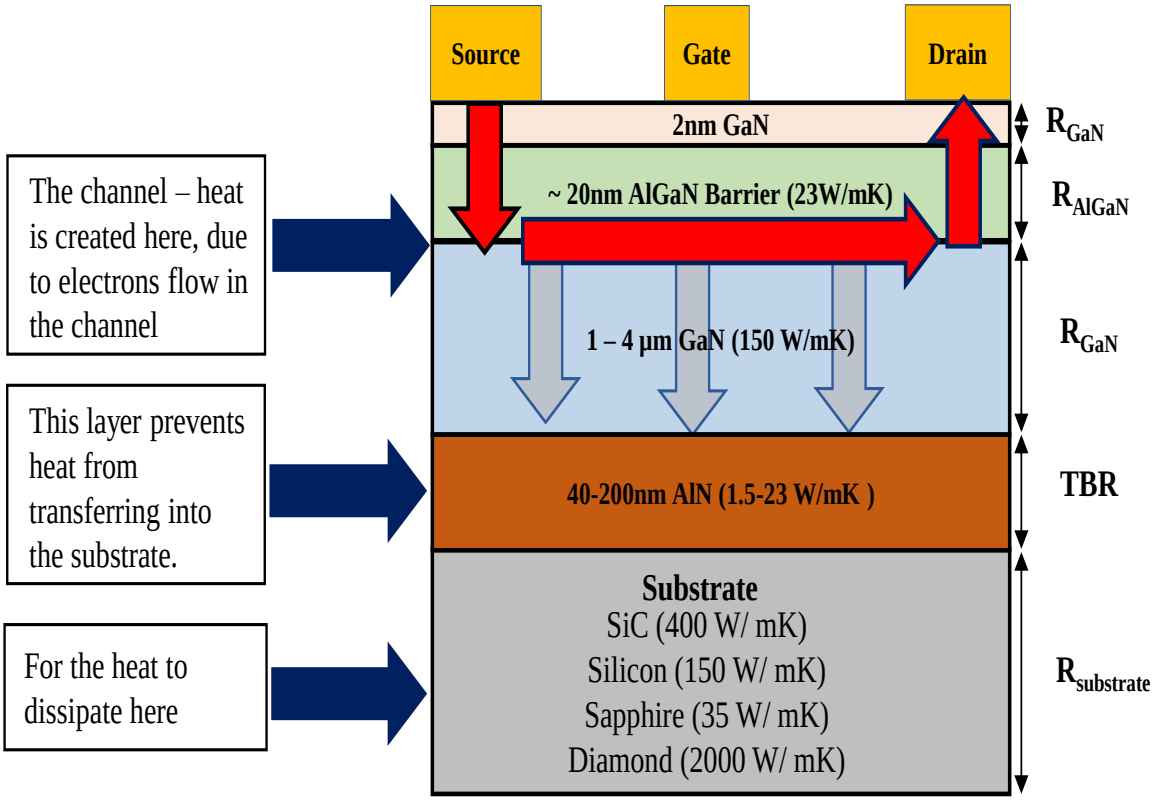


Figure 6.1: A picture of a standard AlGaN/GaN HEMT with a three-arrow pointing from the channel to the substrate to show how heat flows. Also given are the thermal conductivities of the most common epi-layers and substrates.

When the device is working, heat is produced at the AlGaN/GaN material interface in the 2-dimensional electron gas (2DEG) channel of the device. For GaN HEMTs, the TBR is the resistance to heat flow between the AlN nucleation layer and the substrate material on which it is grown [50] [170]. The nucleation layer is used to minimise the lattice mismatch between the GaN and the substrate when it is grown on a non-native substrate [171]. The TBR of the AlN nucleation layer is therefore an important parameter to consider in the design of GaN HEMTs. It can be affected by several factors, including the thickness and crystal quality of the layer, as well as the quality of the interface between the nucleation layer and the substrate. Generally, a thinner and higher quality nucleation layer will have a lower TBR than a thicker or lower quality layer [172]. Nonetheless, the nucleation layer's low thermal conductivity varies from 1.5 to 23 W/mK, which is two orders of magnitude lower than that of single crystal AlN [173] [174].

A recent investigation has highlighted TBR as the source of as much as 50% of the thermal resistance in the device [50]. Thermal analyses of GaN/substrate stacks show the significance of the thermal conductivity's temperature dependence. The effective size of the heat source grows as the GaN layer's temperature rises, reducing the thermal conductivity of GaN. In Figure 6.2 the simulation on the effect of GaN buffer layer thickness on the thermal resistance for different substrate materials is shown. The ideal

GaN layer thickness is reduced as a result, being lower than the value anticipated by the temperature independent thermal conductivity [175].

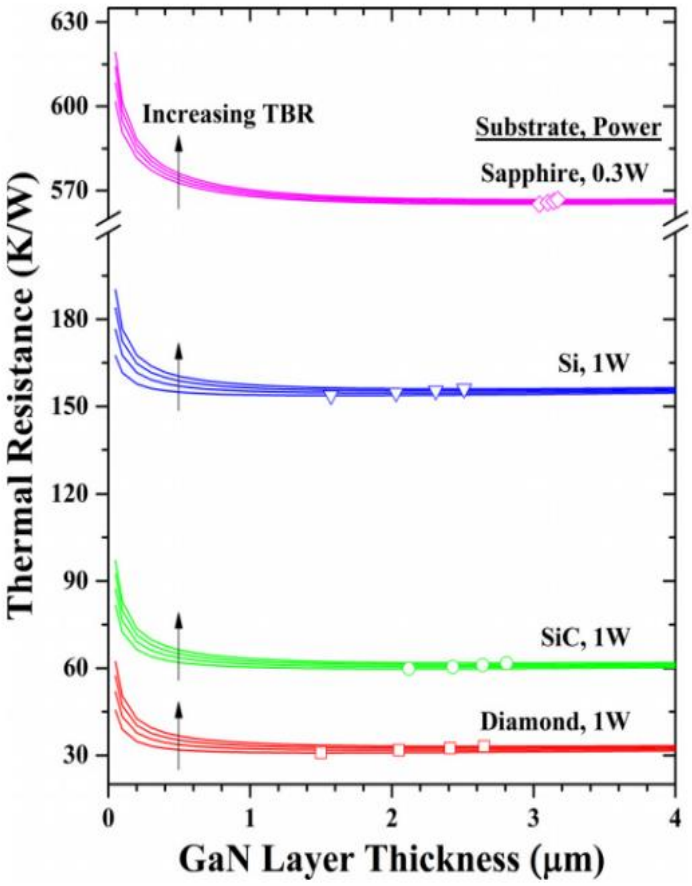


Figure 6.2: The simulation on the effect of GaN buffer layer thickness on the thermal resistance for different substrate material [160].

6.3 Review of thermal management techniques for GaN HEMTs

GaN devices can operate at high frequencies and can handle high power densities. However, as power densities reach around 30 W/mm, thermal management becomes critical for their reliability and performance [176]. Even though a lot of work has been done on thermal management of GaN devices in the past few years, the thermal limitation of the TBR is still the biggest problem for GaN technology. Here, we summarise some thermal management techniques used in GaN HEMTs:

Thermally conductive substrate: SiC is the chosen substrate for high power RF applications because of the high thermal conductivity of the substrate.

Heat sinks: Heat sinks are passive cooling devices that transfer heat away from the GaN HEMT and dissipate it to the environment. They are commonly used in electronic devices and are effective in cooling GaN HEMTs. Water-cooled serpentine rectangular mini-channel heat sinks were used in an experiment to see how well they work for controlling the temperature of GaN devices [177] [178].

Liquid cooling: Active cooling techniques, such as fans or liquid cooling, are used to cool GaN HEMTs when passive cooling is insufficient. Active cooling is more effective than passive cooling and is used when high power densities are expected. It transfers heat from the GaN device to the backside of the diamond substrate, where it is then transferred to a metal heat sink or a microfluidics assembly [179] [180], see Figure 6.3.

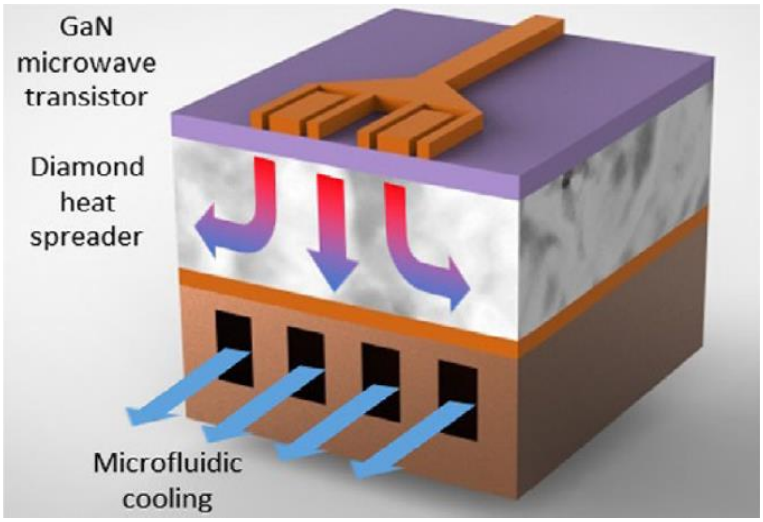


Figure 6.3: Thermal management options illustrated schematically utilising diamond heat extractor using liquid cooling [167]

Diamond substrate: In its purest form, diamond, the bulk material with the highest known thermal conductivity (Tc), reaches values well above 40,000W/mK at low temperatures and more than 2000 W/mK at room temperature; these values are roughly 6 times higher compared to the most advanced SiC substrates used for GaN devices. Due to its extremely high thermal conductivity, diamond is the best heat extraction medium for a GaN HEMT [181].

Thinning the substrate: Thinning the (SiC) substrate beneath the GaN HEMT reduces the thermal resistance between the device and the heat sink. This technique is effective in reducing the operating temperature of the device. Using thermal simulation, the authors [182] observed an improvement in the thermal management of RF GaN-on-GaN HEMTs. The temperature rise was found to be minimum at the substrate thickness of 100µm as showing in Figure 6.4.

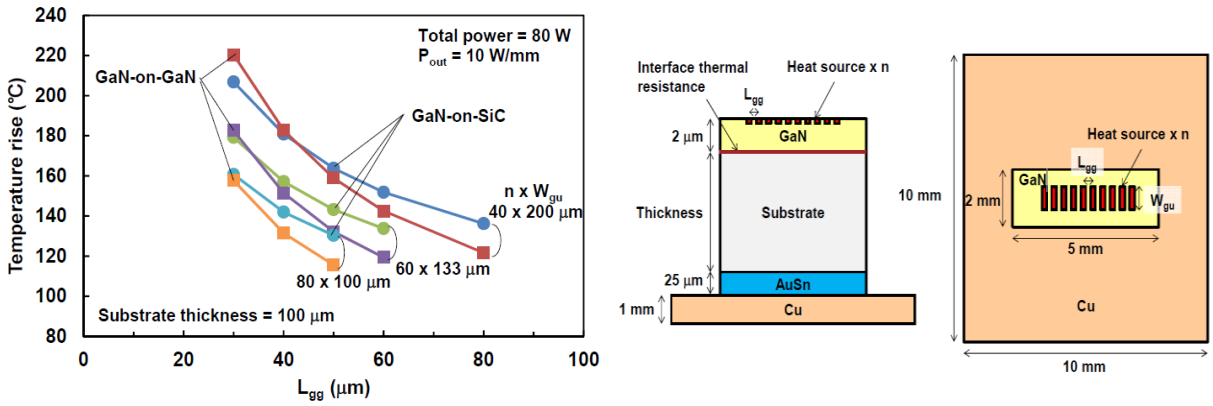


Figure 6.4: A simulated comparison of heat source spacing distance dependence on temperature rise between GaN on GaN and GaN on SiC at different values of n × Wgu (left figure) and simulated structure with heat source placed on top of GaN epitaxial layer[169].

Distributed gate designs: In this process, using a SiC / Si substrate, AlGaN/GaN HEMTs with a planar dispersed channel were formed. The region between the ohmic contacts was split into conductive and nonconductive areas using a typical ion implantation isolation procedure or oxygen plasma treatment technique. The fabricated multi-finger distribution channel devices showed a drop in channel temperature by at least 20°C [183] [184] [185], see Figure 6.5.

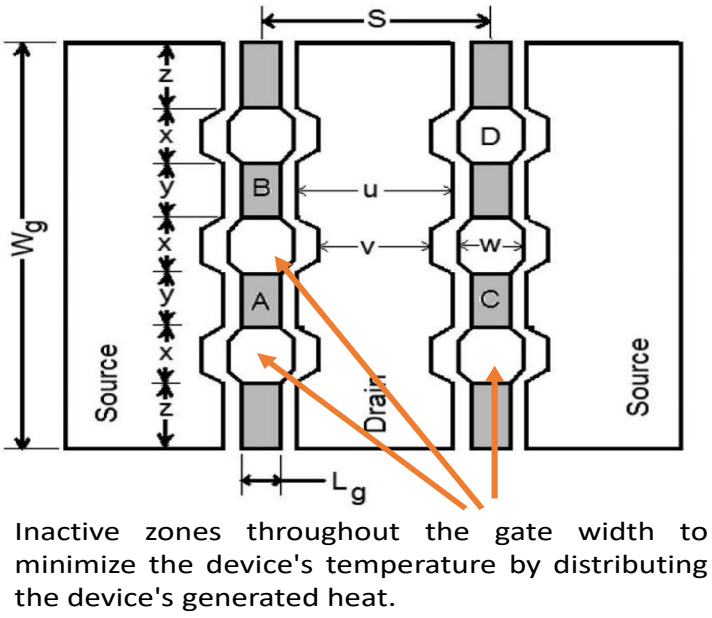


Figure 6.5: Distributed gates design [172].

Diamond heat spreader: A GaN-on-Si device with a diamond heat spreader was proposed, analysed, and compared to standard GaN-on-Si and -SiC devices. Simulation results show improvements in g_m and f_T by 14% and 17%, respectively, with respect to the conventional GaN-on-Si [186] [187]. The diamond heat spreader approach is illustrated in Figure 6.6.

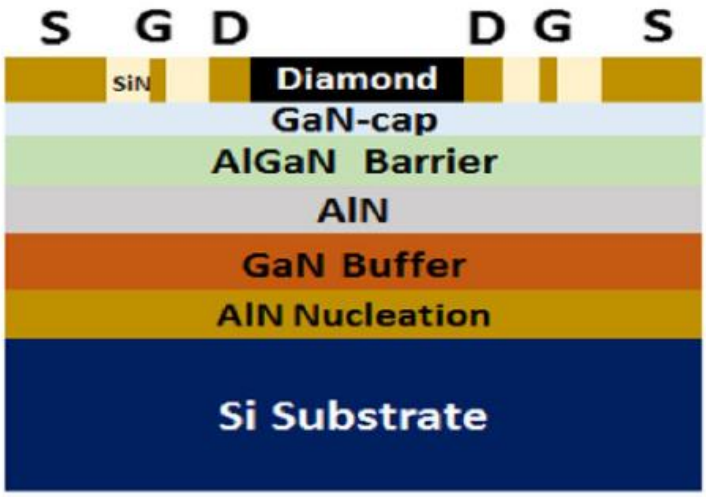


Figure 6.6: Diamond heat extractor using liquid cooling [174].

Copper filled micro-trench: The author [188] described a micro-trench structure that was fabricated on a silicon substrate for an AlGaN/GaN high electron mobility transistor (HEMT) via deep reactive ion etching and thereafter filled with high thermal conductivity material copper through electroplating. Due to efficient heat dissipation, the saturation drain current was increased by around 17%. Figure 6.7 shows backside silicon etched with micro-trench with copper.

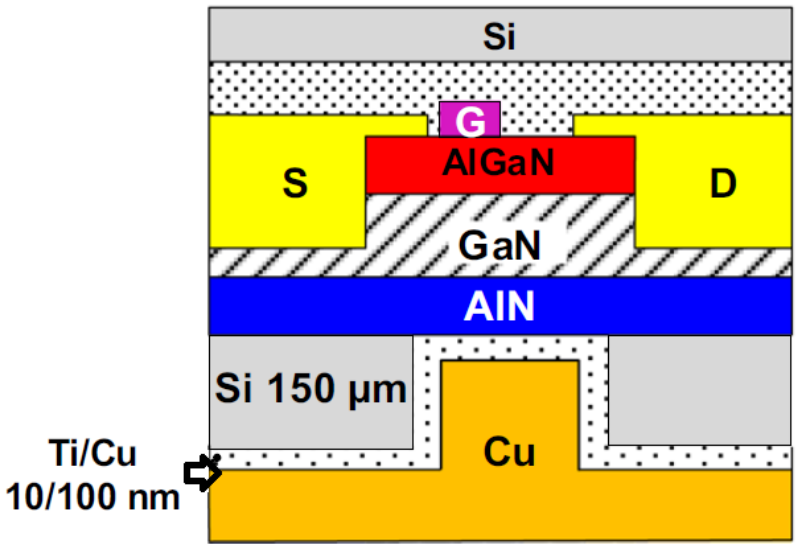


Figure 6.7:Backside Silicon etched and filling micro-trench with copper electroplating [175].

6.4 Proposed thermally efficient GaN-on-SiC HEMT device

Here, we propose a low thermal resistance path that connects directly to the high thermal conductivity SiC substrate and is only a few microns away from the 2DEG channel (heat source) as a method to remove heat that has been generated in the device. Figure 6.8 illustrates a schematic cross-section of the proposed device structure, while Figure 6.9 shows 3D illustration of GaN-based HEMT structure with bond-pads on SiC substrate. Figure 6.10 shows the top view of the new RF device layout. We will remove all nitride

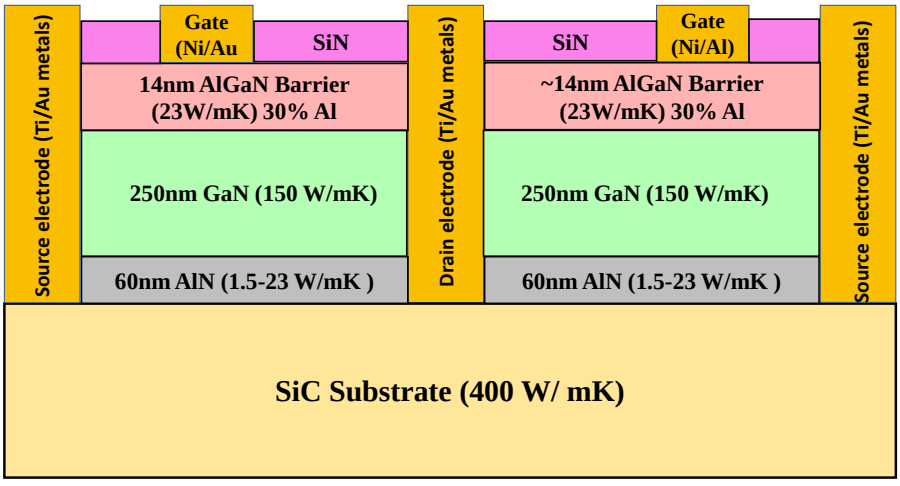


Figure 6.8: Layout of the new device with bond pads as heat sink.

material surrounding the active device region, allowing the device electrodes to sit on the SiC substrate and function as heat sinks.

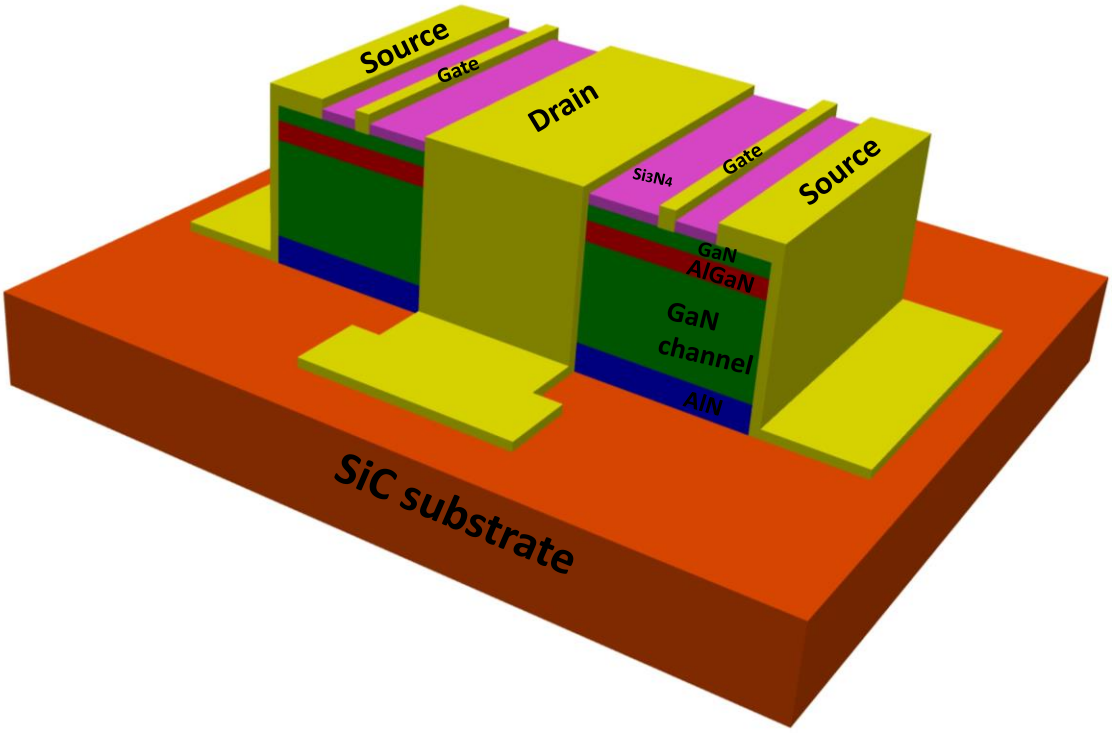


Figure 6.9: 3D- illustration GaN-based HEMT structure with bond-pads on SiC substrate as heat sinks.

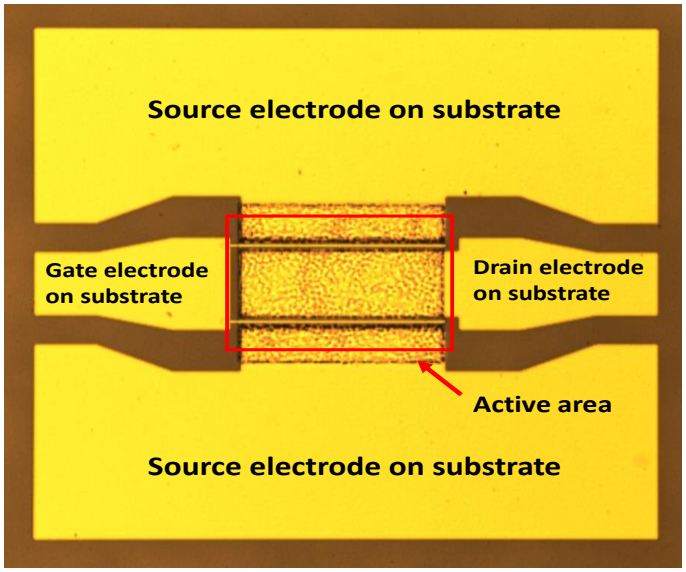


Figure 6.10: Cross-section of a GaN-based HEMT structure with bond-pads on SiC substrate.

6.4.1 Experimental results

The proposed technique makes use of a deep mesa-etch up to the SiC substrate layer by using the BCl_3/Cl_2 dry etch gases. In this section, we provide specifics on device processing methods and electrical properties of the devices. The buffer-free SweGaN wafer with a total epitaxial layer thickness of only 326 nm was utilised in this study.

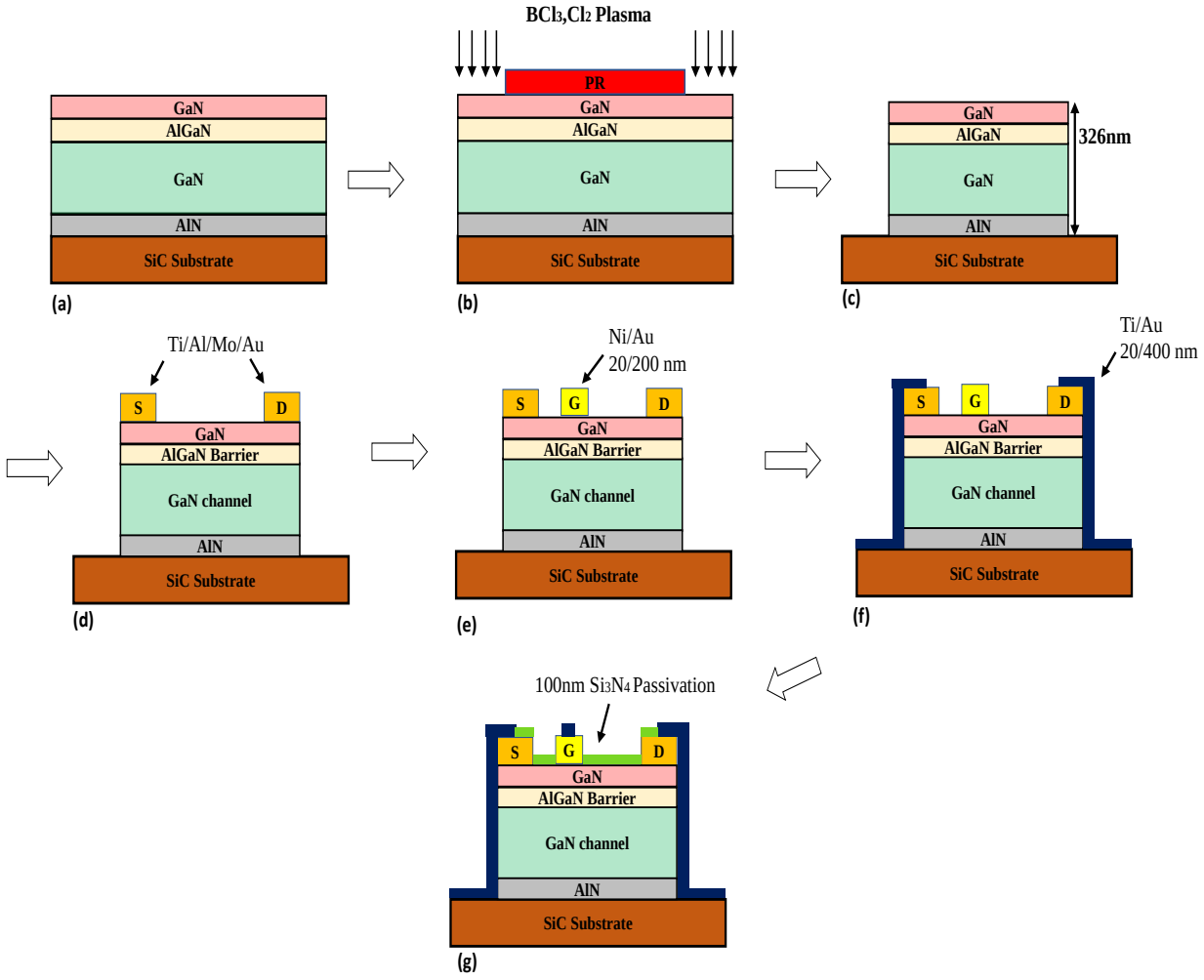


Figure 6.11: **Schematic views of the process flow for mesa etch up to substrate fabrication in AlGaN/GaN HEMT device processing steps (a) Clean wafer (b) Photo-lithography to expose deep mesa-etch pattern using BCl_3/Cl_2 plasma (c) Removal of photoresist and cleaning after 326nm nitride mesa deep etching (d) Deposition of Ti/Al/Mo/Au metal stack Ohmic contacts (e) Ni/Au based gate metallization (f) Bond pads contacts – showing how the bond pad contact will be acting as a heat sink for the device (g) Device passivation using deposition of 100nm Si_3N_4.**

The fabrication process is illustrated in Figure 6.11. It began with mesa isolation, the dry etching a depth of 326 nm of the nitride layers up to the SiC substrate. This was done using inductively coupled plasma (ICP180) with BCl_3/Cl_2 gases at 5/10 sccm, RF/DC power of 25/250 W, pressure of 20 mTorr, which resulted in an etch rate of 7.5 nm/min. This was followed by the evaporation of Ti/Al/Mo/Au (15/60/35/50nm)

metal stack to form the Ohmic metal contacts, followed by a lifted off process, then rapid thermal annealing procedure at 800 °C for 30 seconds. Thereafter, the gate metal contacts were formed by evaporation of Ni/Au (20/200 nm) and followed by the evaporation of bond pad metal contacts Ti/Au (20/400 nm). For final surface passivation, a Si_3N_4 coating of 100 nm deposited by plasma-enhanced chemical vapour deposition (PECVD) at 300 °C was done. Lastly, to allow probing access for device measurements, the Si_3N_4 layer in the Ohmic and gate areas was etched using reactive ion etching (RIE 80+) tool using SF_6/N_2 gases with RF power 50 W and pressure 100 mTorr. The etch rate was 25nm/min. Photolithography was used to define all fabrication processes. Figure 6.12 is a profile measurement using Dektak after the mesa-isolation step and shows a ~341nm mesa etch depth up to the substrate. All the nitride layers were completely etched using the BCl_3/Cl_2 gases (device 2). Standard devices in which the mesa depth is only 100 nm (device 1) were also fabricated for comparison.

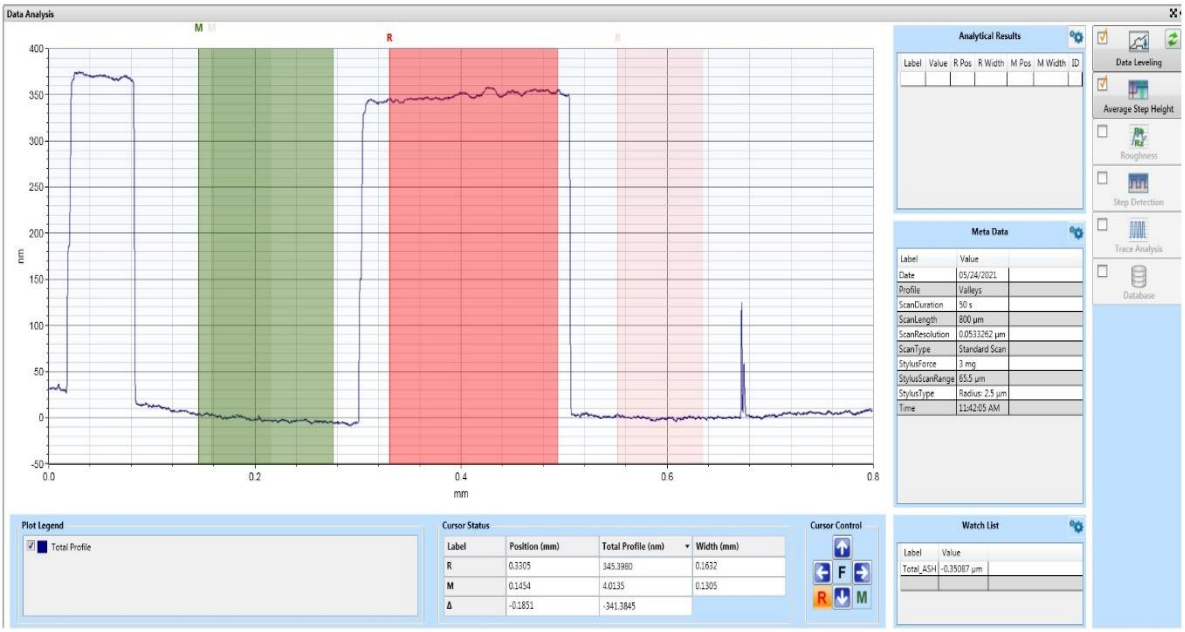


Figure 6.12: The etch depth of 341nm nitride material around the active device area using the the BCl_3/Cl_2 gases using the DektakXT tool.

The fabricated devices were 2-finger HEMTs with a gate length, L_G = 2 µm, gate-to-source distance, L_{GS} = 2 µm, gate-to-drain distance, L_{GD} = 3 µm, and gate widths of 2 × 50 µm. Ohmic contact resistances were extracted from circular transmission line model (CTLM) measurements to be 0.63 Ω·mm and 0.65 Ω.mm for devices 1 and 2, respectively. The fabricated devices standard (~200 nm) mesa etch and deep (~326 nm) up to substrate mesa etch, and SEM image of device 2 are shown in Figure 6.13.

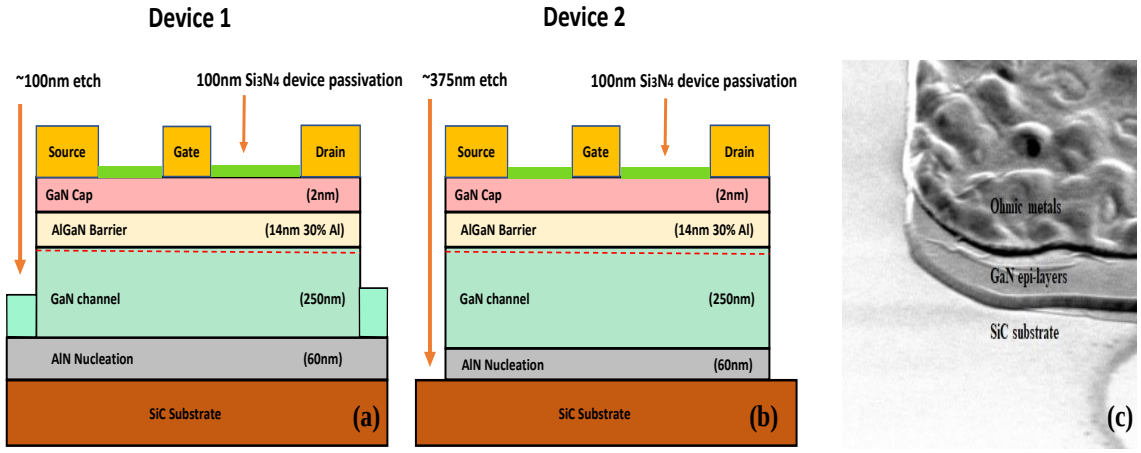


Figure 6.13: Epitaxial wafer structure of fabricated AlGaN/GaN heterostructure devices (a) Standard mesa HEMT and (b) Deep mesa etch upto substrate HEMT (c) SEM image of deep etched showing Ohmic metals, GaN epilayer and SiC substrate.

DC-IV measurements were done using the Keysight B1500A Semiconductor Device Analyzer at room temperature on 2 × 50 µm wide devices. The output characteristics are shown in Figure 6.14. The maximum saturated output currents for devices 1 and 2 were 0.46 A/mm and 0.24 A/mm, respectively. Device 2 showed just 50% of current compared to device 1 at V_{gs} = 0V. It is unclear why this is so.

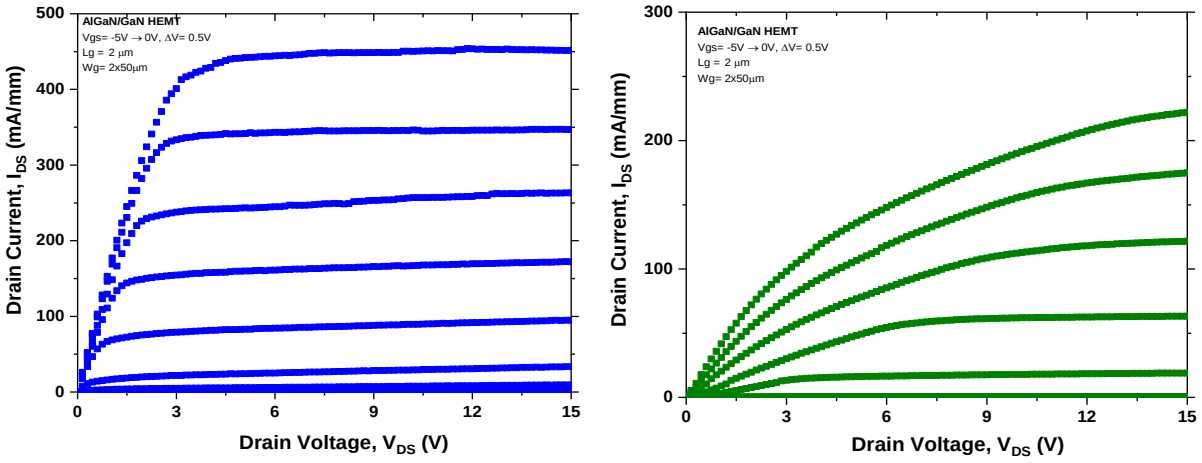


Figure 6.14: The I_{DS}-V_{DS} characteristics of 2 × 50 µm wide devices at V_{GS} = 0V to -5V and V_{DS} up to 15V on device 1 (left side in blue colour) and device 2 (right side in green colour).

Figure 6.15 shows the output characteristics of the devices to V_{DS} = 40 V. The saturated output currents at V_{GS} = 0 V for devices 0.42 A/mm and 0.24 A/mm which corresponds to dissipated DC powers levels of 16.8 W/mm and 8.8 W at 40 V drain voltage, on device 1 and device 2, respectively.

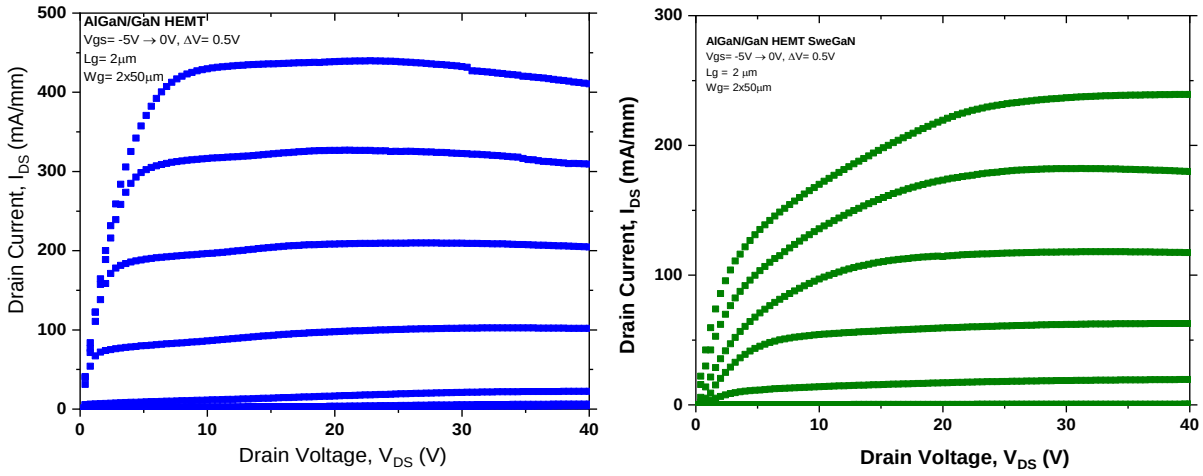


Figure 6.15: The I_{DS}-V_{DS} characteristics of 2 × 50 µm wide devices at V_{GS} = 0V to -5V and V_{DS} up to 40V on device 1 (left side in blue colour) and device 2 (right side in green colour).

More research is needed to determine why the current drops for device 2 (mesa isolation up to the substrate). We checked whether the SiC substrate was conducting or not after removal of nitride material surrounding the active device region. However, the results of the measurement revealed that the SiC substrate is not conducting. We also annealed device 2 at 400°C for 10 minutes in a N_2 atmosphere to mitigate against the damage during mesa etching. Figure 6.16 shows the IV characteristics of 2 × 50 µm wide device after annealing. The devices demonstrated excellent transistor IV characteristics and no sign of heating effect at increased drain bias voltage. However, the maximum output current was reduced to 50 mA/mm at V_{GS} = 0 V. The maximum output current of the device was reduced almost 2 times from the

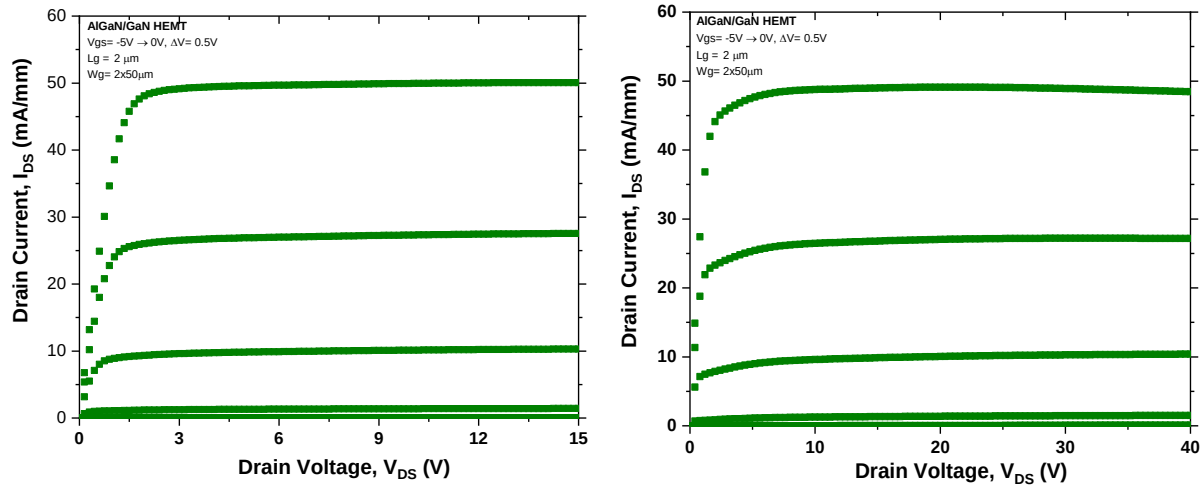


Figure 6.16: The I_{DS}-V_{DS} characteristics of 2 x 50 µm wide devices at V_{GS} = 0V to -5V and V_{DS} up to 15 V (left side graph) and 40V (right side graph) on Wafer 2

standard devices. The reason for this was not clear, but we suspected that it may be due to leakage currents. Leakage currents are currents that flow through the device even when there is no applied voltage [189]. These currents can be caused by defects in the semiconductor material or by the ohmic contacts. We investigated the possibility of leakage currents by measuring the current-voltage characteristics of the device. We found that the leakage currents were indeed increased in the device with the reduced maximum output current [190]. This confirmed our suspicion that the reduced maximum output current was due to leakage currents and so investigated a fully passivated mesa structure which is described next. Extending the metallization in bondpad to the level of the substrate can improve the performance of mm-wave circuits by reducing the parasitic inductance of the bondpad. The parasitic inductance is caused by the capacitance between the bondpad and the substrate. When the metallization is extended to the level of the substrate, the capacitance is reduced, which in turn reduces the parasitic inductance. This can lead to improved signal integrity and reduced signal loss at mm-wave frequencies [191].

The parasitic inductance of a bondpad is caused by the capacitance between the bondpad and the substrate. The capacitance is proportional to the area of the bondpad and the distance between the bondpad and the substrate. When the metallization is extended to the level of the substrate, the area of the bondpad is increased, which reduces the capacitance. The distance between the bondpad and the substrate is also reduced, which further reduces the capacitance. The reduction in parasitic inductance can lead to improved signal integrity and reduced signal loss at mm-wave frequencies. This is because the parasitic inductance limits the bandwidth of the circuit and causes signal attenuation. By reducing the parasitic inductance, the bandwidth of the circuit can be increased, and the signal attenuation can be reduced [192].

In addition to reducing parasitic inductance, extending the metallization in bondpad can also improve the heat dissipation from the circuit. This is because the extended metallization provides a larger surface area for heat dissipation. This can be important for mm-wave circuits, which can generate a lot of heat. Overall, extending the metallization in bondpad can be a beneficial technique for improving the performance of mm-wave circuits.

6.4.2 Mesa-passivated thermally-efficient GaN MIS-HEMTs

In this experiment, we fabricated mesa-passivated metal-insulator-semiconductor (MIS)-HEMT devices, in which all the nitride material around the active devices is removed and the transistor electrodes are deposited on the SiC substrate. Si_3N_4 dielectric was also used to protect the mesa side wall of the device after the mesa isolation to the substrate. The fabrication process for MIS-HEMT is illustrated in Figure 6.17.

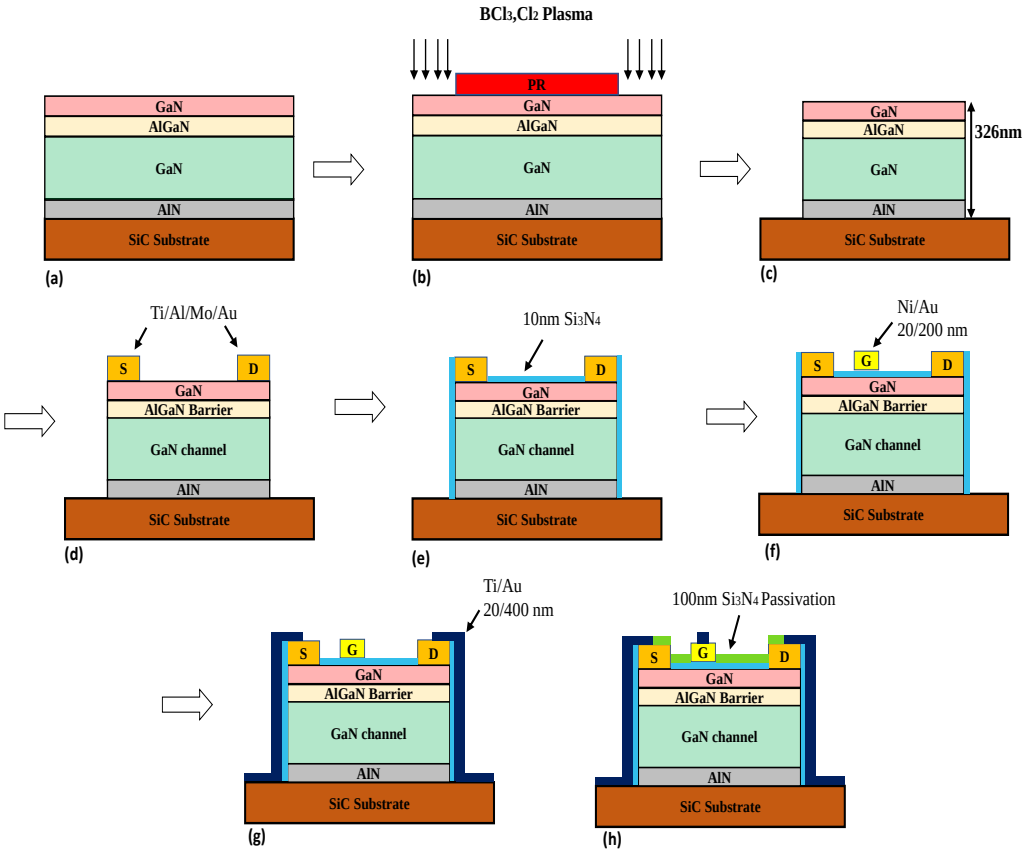


Figure 6.17: Schematic views of the process flow for mesa etch up to substrate fabrication in AlGaN/GaN MIS-HEMT device processing steps (a) Clean wafer (b) Photo-lithography to expose deep mesa-etch pattern using BCl_3/Cl_2 plasma (c) Removal of photoresist and cleaning after 326nm nitride mesa deep etching (d) Deposition of Ti/Al/Mo/Au metal stack Ohmic contacts (e) Deposition of 10nm Si_3N_4 dielectric layer to protect mesa sidewall – this step is omitted for the HEMT device (f) Ni/Au based gate metallization (g) Bond pads contacts – showing how the bond pad contact will be acting as a heat sink for the device (h) Device passivation using deposition of 100nm Si_3N_4.

The proposed technique makes use of a deep mesa-etch up to the SiC substrate layer by using the BCl_3/Cl_2 dry etch gases, followed by the deposition of 10 nm of Si_3N_4 using PECVD at 300 °C. The buffer-free GaN wafer was utilised in this study. Figure 6.18 MIS-HEMT device alongside a standard (~200 nm mesa etch) HEMT for comparison, and top view of SEM image of 200 µm device.

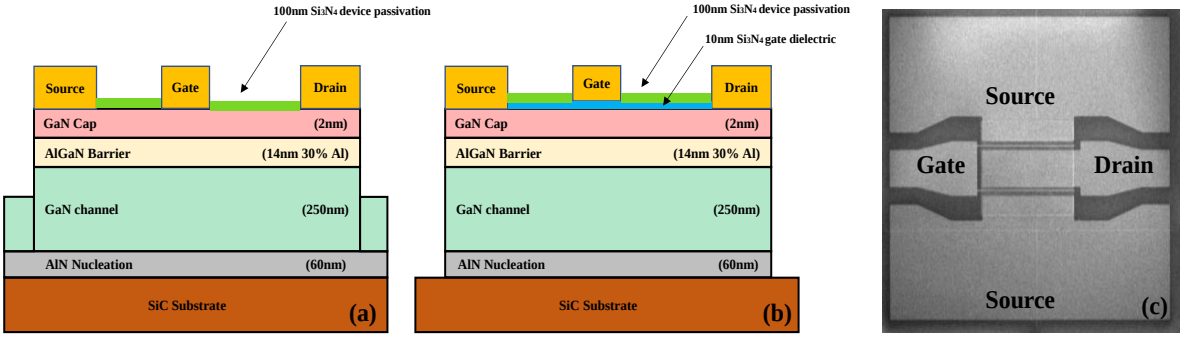


Figure 6.18: Epitaxial wafer structure of fabricated AlGaN/GaN heterostructure devices (a) HEMT and (b) MIS-HEMT with 10nm Si_3N_4 (c) Micrograph of fabricated 200µm wide device.

The fabrication of the device began with mesa isolation, dry etching a depth of 326 nm of the nitride layers up to the SiC substrate. This was done using inductively coupled plasma (ICP180) with BCl_3/Cl_2 gases at 5/10 sccm, RF/DC power of 25/250 W, pressure of 20 mTorr, which resulted in an etch rate of 7.5 nm/min. Then, evaporation of Ti/Al/Mo/Au (15/60/35/50nm) to form the Ohmic metal contacts, followed by a lifted off process, then rapid thermal annealing procedure at 800 °C for 30 seconds. As the gate dielectric and to passivate the mesa side walls, a blanket deposition of a thin layer of Si_3N_4 measuring 10 nm was carried out using plasma-enhanced chemical vapour deposition (PECVD) at 300 °C. Then gate metal contacts were formed by evaporation of Ni/Au (20/200 nm). To deposit the bond pads metals on SIC substrate, the 10nm Si_3N_4 layer was etched from the bond pad regions using reactive ion etching (RIE 80+) tool using SF_6/N_2 gases, followed by the evaporation of bond pad metal contacts Ti/Au (20/400 nm). For final surface passivation, a Si_3N_4 coating of 100 nm deposited by plasma-enhanced chemical vapour deposition (PECVD) at 300 °C. Lastly, to allow probing access for device measurements, the Si_3N_4 layer in the Ohmic and gate areas was etched using reactive ion etching (RIE 80+) tool using SF_6/N_2 gases with RF power 50 W and pressure 100 mTorr. The etch rate was 25nm/min. Photolithography was used to define all fabrication process steps.

Using the Keysight B1500A Semiconductor Device Analyzer and E8361A PNA Network Analyzer for measurements of DC and RF were performed at room temperature, respectively. The gate length, L_G = 2 µm, gate-to-source distance, L_{GS} = 2 µm, gate-to-drain distance, L_{GD} = 3 µm, and gate widths of 2 × 200 µm are the device dimensions employed in this study.

In both samples, circular transmission line model (CTLM) test structures were used to analyse the contact resistance, R_C, and the values were 0.65 Ω.mm and 0.59 Ω.mm, respectively. Figure 6.19 depicts the output current-voltage (I-V) characteristics of both the fabricated devices. At V_{GS} = 1, the Schottky-gate device's maximum drain current is 460 mA/mm, while the MIS-HEMT devices maximum drain currents are 728 mA/mm. The transistor's on- resistance decreases to 6.67 Ω.mm compared to 11.55 Ω.mm measured for the HEMT. Further, the HEMTs and MIS-HEMTs were completely pinch-off at a gate voltage of -2.6V and - 6.5V, respectively.

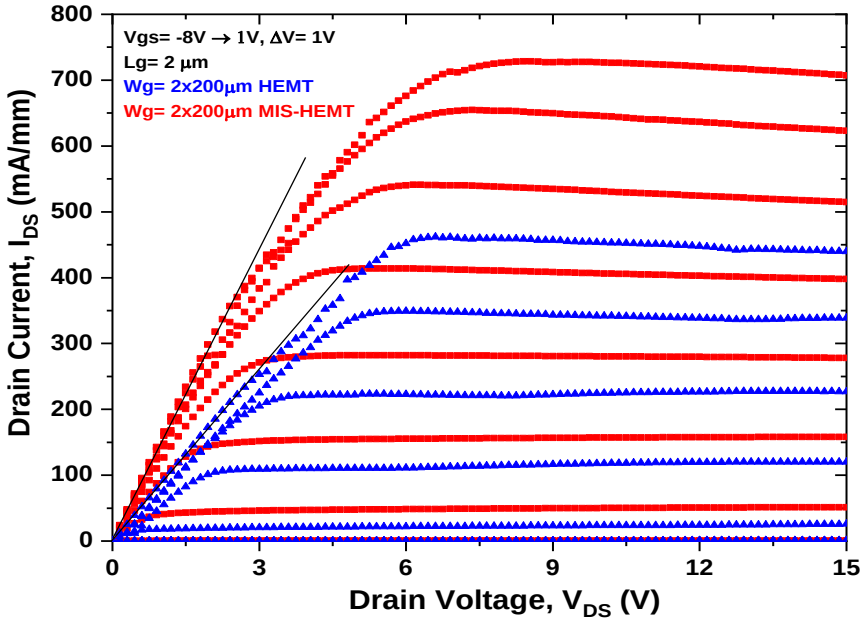


Figure 6.19: The I_{DS}-V_{DS} characteristics of 2 × 200 μm wide devices at V_{GS} = 1V to -8V of AlGaN/GaN HEMT and Si_3N_4 MIS-HEMT.

Figure 6.20 shows IV characteristics to V_{DS} = 40 V. Self-heating effect is evident in both the HEMT and MIS-HEMT devices, with 20.5% and 18.9% drop in the maximum drain current drop observed at higher V_{DS} drain voltage, respectively.

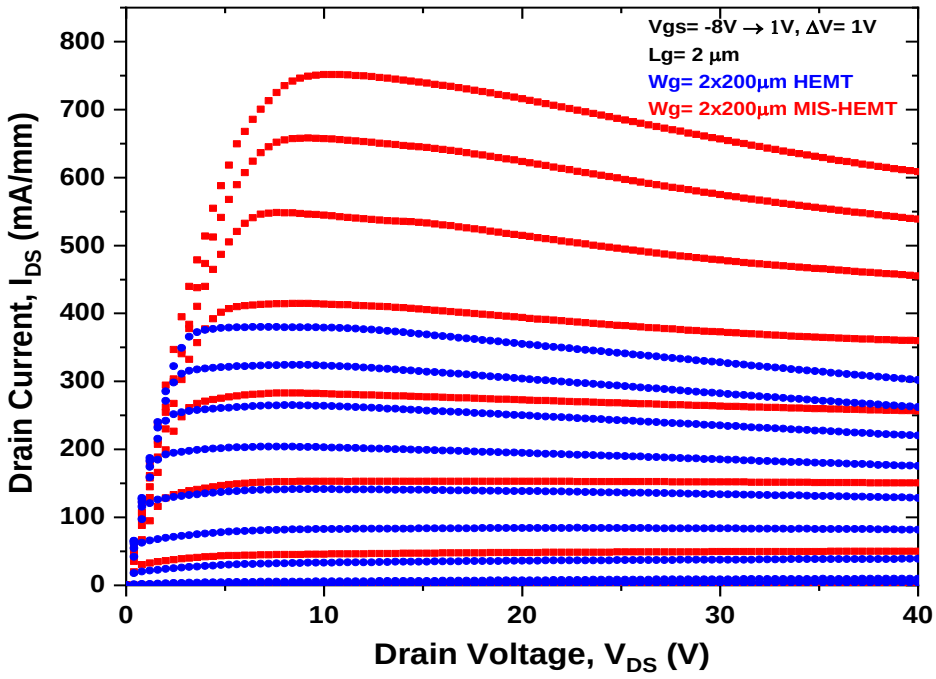


Figure 6.20: The I_{DS}-V_{DS} characteristics of 2 x 200 µm wide devices at VGS = 1V to -8V and V_{DS} up to 40V of AlGaN/GaN HEMT and Si_3N_4 MIS-HEMT.

These results show that the MIS-HEMTs can handle higher current compared to HEMTs. The drain current is also larger for MIS-HEMT at the same gate bias. As a result of this distinction, the channel depletion in a MIS-HEMT is less than that in a HEMT for a same gate voltage. The measured threshold voltage, V_{TH}, of – 2.6 V and – 6.5 V (extracted value of gate-to-source voltage, V_{GS} at I_{DS} = 1 mA/mm) were obtained for HEMT and MIS-HEMT devices as shown in Figure 6.21. The presence of an additional thin 10nm of Si_3N_4 layer in MIS-HEMTs results in a slight transconductance increase from 104.28 to 118.64 mS/mm in MIS-HEMTs compared to HEMTs, which is consistent with a further separation between the control gate and the 2-DEG channel. Moreover, the improvement in g_m, maximum of MIS- HEMT is 12.2 % in comparison to that of HEMT because of the higher drain currents.

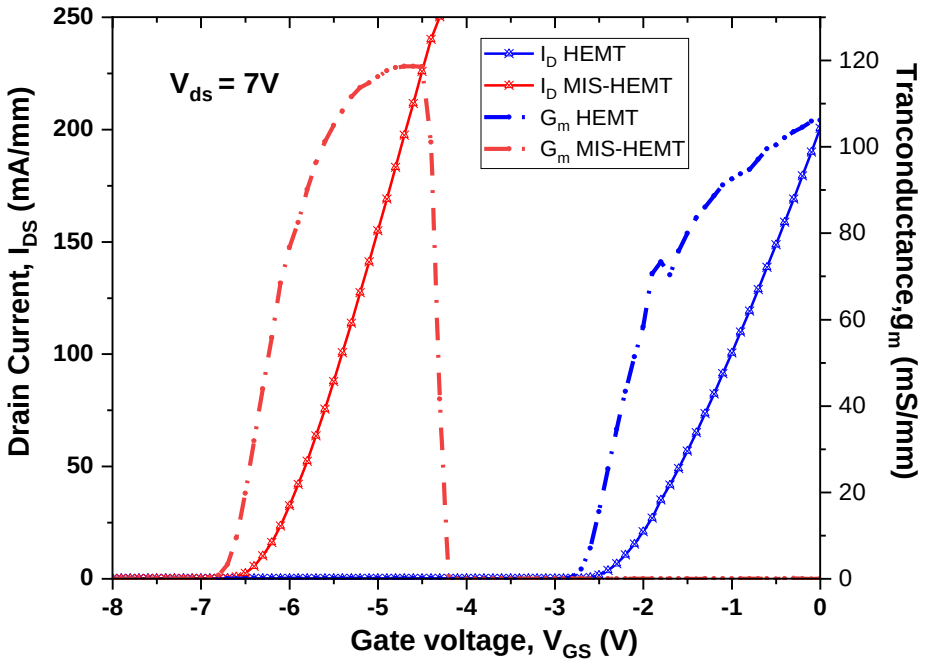


Figure 6.21: Measured transfer characteristics of HEMT and MIS-HEMT devices biased at V_{DS} = 7 V.

In Figure 6.22, a comparison of the gate leakage performance of devices with the same dimensions is shown. The leakage current of MIS-HEMTs is found to be significantly lower than that of Schottky gate HEMT. Nearly 10 orders of magnitude less gate leakage current density exists in MIS-HEMT than in HEMT. This is attributed to the large band offsets in the Si_3N_4/HEMT and the high quality of both the PECVD Si_3N_4 dielectric and the Si_3N_4/HEMT interface as well as the additional 100nm Si_3N_4 passivation layer for the low

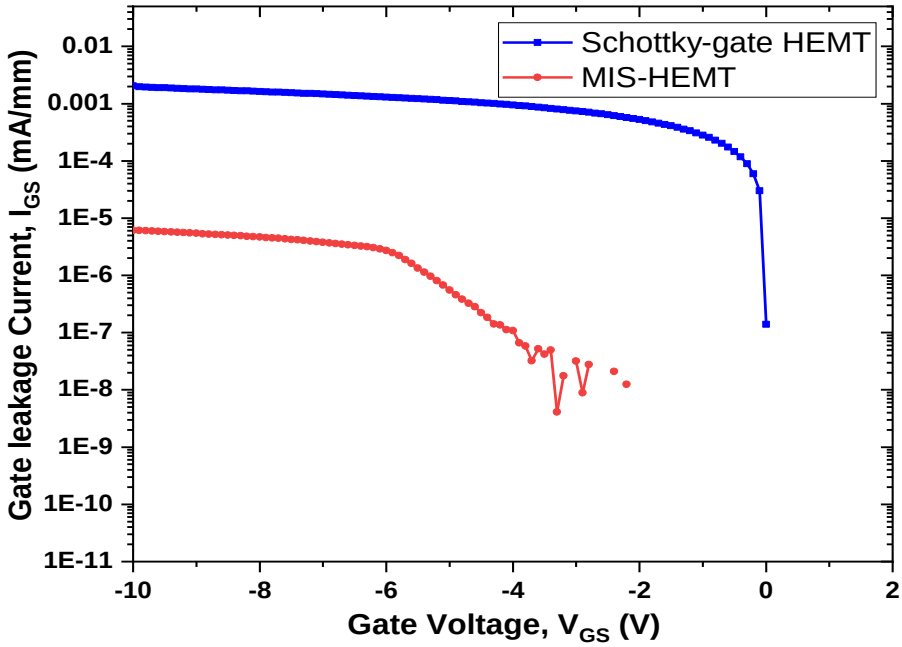


Figure 6.22: Measured gate leakage currents for the AlGaN/GaN HEMT and Si_3N_4 MIS-HEMT with same device dimensions.

gate leakage current. These results show that the Si_3N_4 dielectric thin film can act as an efficient gate insulator.

The Si_3N_4 MIS-HEMT and HEMT's off-state three-terminal drain-source breakdown characteristics were tested and the results are shown in Figure 6.23. The devices were biased in off-state with a gate voltage V_{GS} of - 10V. The breakdown voltage V_{BR}, which corresponds to the rapidly increasing currents caused by avalanche breakdown, is the drain voltage at a gate current of 1 mA/mm. The Si_3N_4 MIS-HEMT has a higher breakdown voltage than the conventional HEMT. The high breakdown voltage is related to the use of the Si_3N_4 gate dielectric to reduce leakage current.

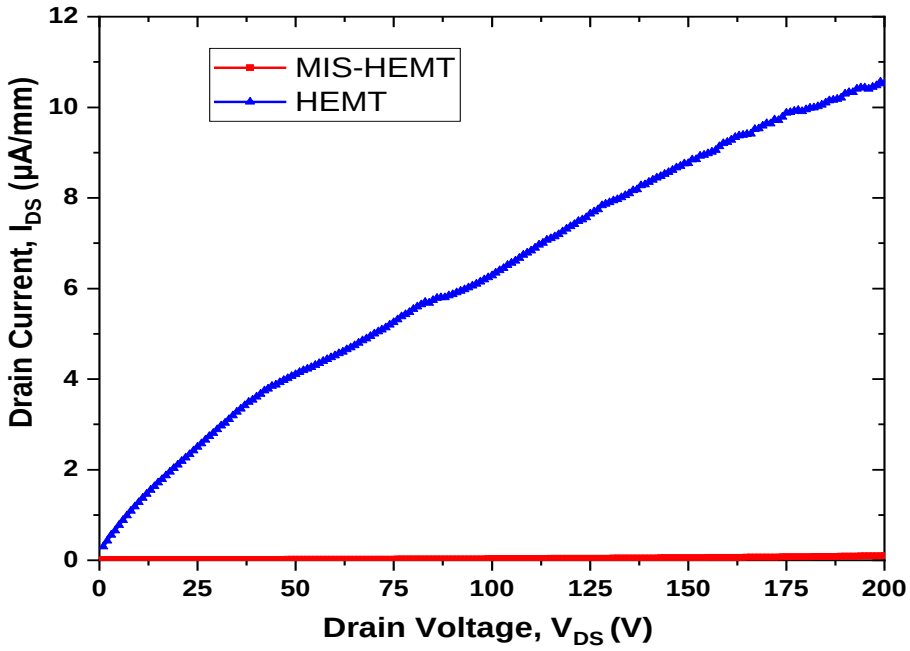


Figure 6.23 Measured off-state breakdown voltage of HEMT and MIS-HEMT devices biased at V_{GS} = - 10 V.

Using a vector network analyzer (VNA), the device's scattering or S-parameters were measured. S-parameters measure the transmission and reflection of a travelling wave and may be used to define two port networks, such as transistors or transistor amplifiers. The current gain cut-off frequency f_T may be calculated by converting measured S-parameters to hybrid parameters (h-parameters). The current gain is represented by the forward-transmission hybrid or h-parameter h21. Mason's unilateral power gain, U = 1, is used to determine the maximum oscillation frequency, f_{MAX}. The details of transistor cut-off frequencies in chapter 2 section 2.7. For both HEMT and MIS-HEMT devices biased at V_{GS} = -2.6 V and -5 V, which correspond to peak transconductance, respectively, S- parameter measurements were made. Figure 6.24. displays the RF performance of the HEMT and MIS-HEMTs from the small signal measurements (S-parameters). The maximum measured cut-off frequency, f_T, and the highest oscillation frequency, f_{MAX}, for the HEMT device were V_{DS} = 15 V at 4.7 GHz and 9.4 GHz, respectively. In MIS-HEMT, it was found that a two-finger, 2 × 200 µm device biased at V_{DS} = 15 V had maximum cut-off and oscillation frequencies of 6.3 GHz and 15.8 GHz, respectively. The bond pads' parasitic effects were not de-embedded. Table 6-1 provides maximum oscillation frequencies (f_{max}) and extrapolated cutoff frequencies (f_T).

Table 6-1: Extrapolated f_T and f_{MAX} values from S-parameter measurements of HEMT and MIS-HEMT devices at V_{DS}=15V

Wafer	Device size	F_T (GHz)	Fmax (GHz)
		V_{DS} = 15V	V_{DS} = 15V
HEMT	2×200 µm	4.7	9.4
MIS-HEMT	2×200 µm	6.33	15.68

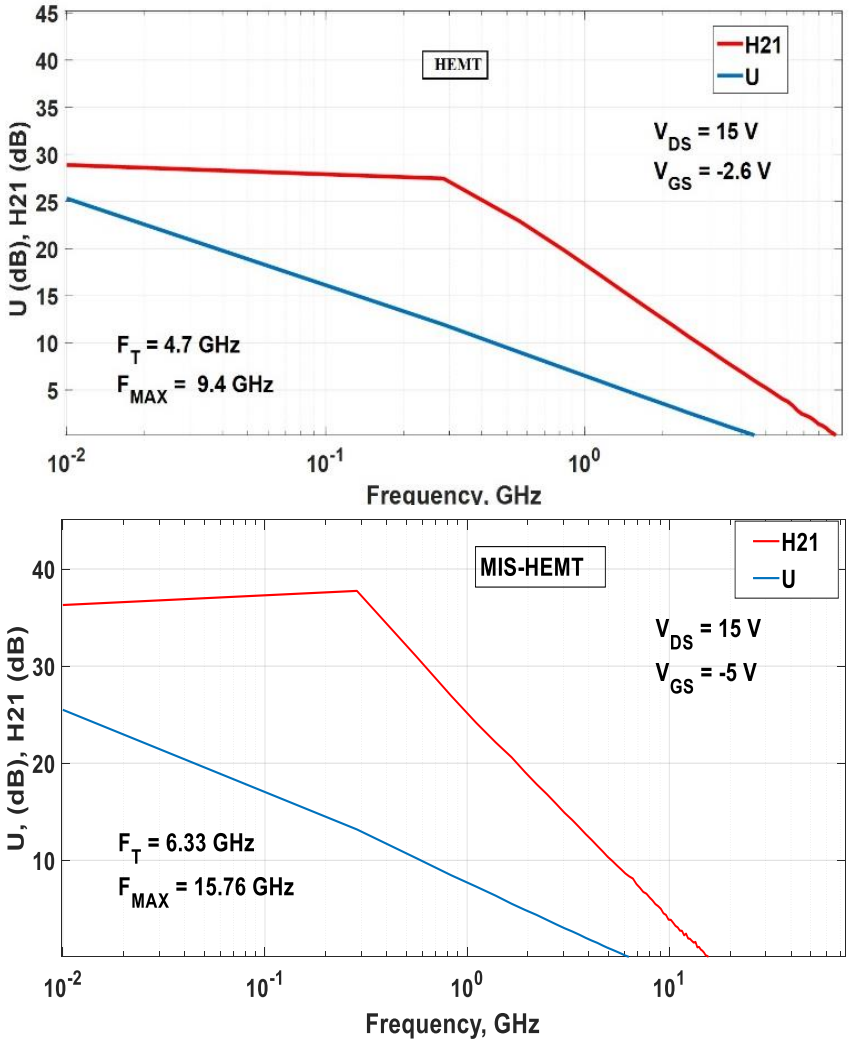


Figure 6.24: Measured H21 and Maximum signal gain for 2x200µm device sizes for HEMT and MIS-HEMT devices.

6.5 Conclusion

A new method for extracting heat in GaN-on-SiC HEMT devices was proposed and demonstrated. The method involves removing nitride materials from around the active part of the device and replacing this with metal electrodes to dissipate/route the heat to the SiC substrate, resulting in less self-heating and better current density. The approach exploits the thin epitaxial stack for the buffer-free device structure. Overall, this new buffer-free epitaxial approach has great potential for producing high performance GaN HEMTs for high-power and high-frequency applications.

Chapter 7
High Frequency GaN HEMT Devices

7 High Frequency GaN HEMT Devices

7.1 Introduction

The constant drive for higher power levels and high frequencies have seen major developments in GaN HEMT technology. HEMTs can be used in circuits that operate up to a quarter of the device unity power gain cut-off frequency, f_{MAX}. The highest reported current gain cut-off frequency, f_T, and f_{MAX} for AlGaN/GaN HEMTs so far is 454/444 GHz [193], and so the technology can support circuit design up to over 100 GHz. One of the most efficient methods of how to achieve higher operating frequencies is to use T-shaped gate with small gate lengths, for example 100nm [194] because it allows to reduces the gate parasitic capacitance and also reduces the gate resistance to allow for higher frequency operation and output power. In this chapter the design and fabrication of T-shaped gates will be discussed.

7.2 State of the art

The outstanding material properties of nitride semiconductors in combination with novel fabrication technologies allow fast development in the high-frequency performance of GaN HEMTs. High-speed FETs need the precision of a vertical epitaxial scaling as well as lateral device scaling. The technology advancement on GaN HEMT devices is gate length scaling, regrown ohmic contacts, scaling GaN HEMT device geometry and epilayer structure for GaN device. The GaN HEMT T-gate technology has several advantages than the planar gate for achieving high frequency. The T-shaped gate geometry reduces the parasitic capacitance due to the narrow footprint and lower gate resistance due to the larger head allowing cut-off frequency above 300 GHz. Using regrown ohmic contacts and a self-aligned gate process, GaN HEMTs have reached the f_t above 450 GHz [31].

The characteristics and performance of state-of-the-art performance of RF (W-band) GaN HEMT devices are shown in Table 7-1. It provides the recent research development in GaN-based HEMTs with ultrashort effective gate length (20-200 nm) for high frequency, high power RF applications from year 2010 to 2023.

1) The best performance using AlN/GaN/AlGaN double heterojunction with regrown n+ GaN ohmic layer which is not alloyed and high electron density (n_s)$1.2 \times 10^{13} cm^{-2}$ was achieved. They used ultra-thin barrier layer of AlN 3.5nm with highly scaled design structure, source to drain spacing was 100nm. The lowest contact resistance achieved (R_c) is 0.26 Ωmm. They reduced gate capacitance to achieve the record a cut-off frequency f_t of 454 GHz and an oscillation frequency f_{max} of 444 GHz with a gate length of 20nm and 50nm gate to source distance using the self-aligned gate approach on SiC substrate [33].

2) The first time deeply scaled self-aligned gate method with heavily doped n+ GaN source to drain direct contacts with the 2DEG near the gate results improvement in DC and RF characteristics. The gate length was used 20nm, and source to drain distance is 100nm. The lowest R_{on}(0.026Ωmm) resistance was achieved. Highest current density and transconductance (g_m) 4 A/mm and 2.25 S/mm was measured [31].

3) By shrinking the gate length to 30nm InAlN/GaN HEMTs on a SiC substrate, a record f_t at the time of 245 GHz was achieved by applying oxygen plasma treatment on InAlN, but the f_{max} of 13GHz

was poor because of high gate resistance of the rectangular gate [195]. In the same year, Lee *et al* improved the cut-off frequency f_t by 300 GHz by applying the InGaN back barrier [196].

4) Y. Yue *et al.* demonstrated InAlN/AlN/GaN HEMT on SiC substrate without dielectric passivation. They used rectangular 30nm gate, and regrown ohmic contacts and achieved high f_t of 370 GHz by minimizing parasitic effects [125].

5) Y. Yue *et al* pushed the cut-off frequency f_t 400 GHz by scaling gate length down to 30-nm rectangular gate. The epi-layer structure used InAlN/AlN/GaN/SiC HEMTs with a scaled source drain distance of 270 nm. However, the achieved $f_{max}$was only 33 GHz because of the very high gate resistance. They reduced total time delay by reducing the short channel effect by maintaining aspect ratio [197].

6) Ultra-thin InAlN/GaN devices were fabricated by scaling lateral dimensions to 600 nm between source to drain contacts. Heavily doped n+ GaN was regrown by MOCVD, and the Si doping concentration was $8 \times 10^{19} cm^{-3}$. Total resistance was calculated at 0.16 Ω.mm has a 40-nm T-gate. The device was passivated by the SiN with a thickness of 50 nm [198].

7) A record performance value of f_t of 220 GHz, f_{max} of 400 GHz was reported by Shinohara *et al.* The vertical scaling in AlN/GaN/AlGaN double heterojunction HEMT structure by thinning the top barrier minimized gate to channel distance. Reduction of access resistance was achieved using MBE regrown technology of n+ GaN Ohmic contacts, including 40-nm T-gate devices [199].

8) The Lin *et al* reported values of f_t of 183 GHz and f_{max} of 191 GHz by employing damage-free NBE (neutral beam etch) for gate recess in which 15 nm barrier layer was etched from a total barrier thickness was 20nm and 60nm of gate. The Al_2O_3/AlGaN/GaN MOSHEMT device was fabricated using Al_2O_3 as a dielectric layer (4nm). The device demonstrated a maximum output power density of 2.7 W/mm [200].

9) M. Diego *et al* demonstrated GaN-on-Silicon GaN HEMTs using recess T-gate 75nm technology showing maximum transconductance of 540mS/mm and cut-off frequencies as high as f_t /f_{max} = 152/149 GHz. The spacing between source to drain was 1 µm and measured maximum output power of 2W/mm using load pull measurement at 40 GHz [201].

10) An optimized AlGaN/GaN HEMT using T-gate 90nm length with N_2O plasma treatment in the gate region to form oxide layer which reduces the gate leakage current and improves breakdown voltage of 80V. The maximum drain current of 1200mA/mm and maximum transconductance of 461mS/mm, the small signal measurement was f_t /f_{max} = 98/332 GHz was achieved [202].

11) The Mi *et al* proposed a 20 nm in-situ SiN layer formed by MOCVD on the top of 6 nm-thick AlGaN barrier. The in-suit SiN layer is thick enough and acts as a passivation layer to reduce current collapse. Fluorine based etching is used to self-terminate after removing SiN, leaving the AlGaN barrier in the gate region. The device showed a drain current of 1022 mA/mm, a peak transconductance of 459mS/mm, and an f_{max} = 248 GHz by using the 100nm T-gate [203].

It is clear from the review that to enhance device performance, both in terms of raising the operating frequency and in terms of lowering the power wasted owing to the channel resistance, involves downscaling the gate length of GaN HEMTs and reducing the distance between the source and drain contacts. L_g reduction affects the current gain cut-off frequency (f_T) and the maximum power-gain cut-off frequency (f_{max}) in HEMTs built for microwave applications through the expressions:

$$f_T = \frac{v_{sat}}{2\pi L_g} = \frac{g_m}{2\pi(\ C_{gd} + \ C_{gs})} \tag{7.1}$$

$$f_{max} = \frac{f_T}{2\sqrt{(R_i + R_s + \ R_g)/R_{ds} + \ (2\pi f_T)R_g C_{gd}}} \tag{7.2}$$

where $v_{sat}$is the electron saturation velocity, g_m is the transconductance. Gate-source capacitance (C_{gs}) and gate-drain capacitance (C_{gd}) reflect the charge in the depletion region beneath the gate towards the source and drain sides, respectively. The R_i, R_s, R_g ,R_{ds} are the gate charging, source, gate, and output resistances respectively [204]. For getting higher f_t and so f_{max} due to the relationship with the gate length L_g, for getting the higher frequency need to maintain the high aspect ratio between the gate length and the 2DEG channel distance. When the length of the gate is reduced to less than 100 nm, short channel effect (SCE) become evident. These effects reduce the potential barrier formed beneath the gate in the off-state when V_{ds} is applied [205]. Typically, the energy barrier height reduction at the source side of the gate in a long-channel HEMT is negligible (Figure 7.1a), resulting in a small drain-source leakage current. Figure 7.1b demonstrates that when the gate length is sufficiently short, the voltage applied to the drain contact can affect the barrier height on the source side of the gate. In turn, thermal excitations allow electrons to overcome the energy barrier, resulting in an increase in drain-source leakage current. This manifests as a negative shift of threshold voltage V_{th} in the transfer characteristics of the device (Figure 7.1c), which is known as Drain induced barrier lowering (DIBL). Due to SCEs, the inability of the gate to modulate the electron concentration channel reduces g_m, which in turn reduces f_T and f_{max} (Equation 7.1 and 7.2) [206]. In addition, as the V_{ds}-dependence of V_{th} increases, R_{ds} decreases, resulting in a decrease in f_{max}. So, the short-channel effects can be reduced by having aspect ratios above 15 [207]. Reducing the gate length is an important parameter for increasing high-frequency performance; however, it is tougher to fabricate very-short gate length devices.

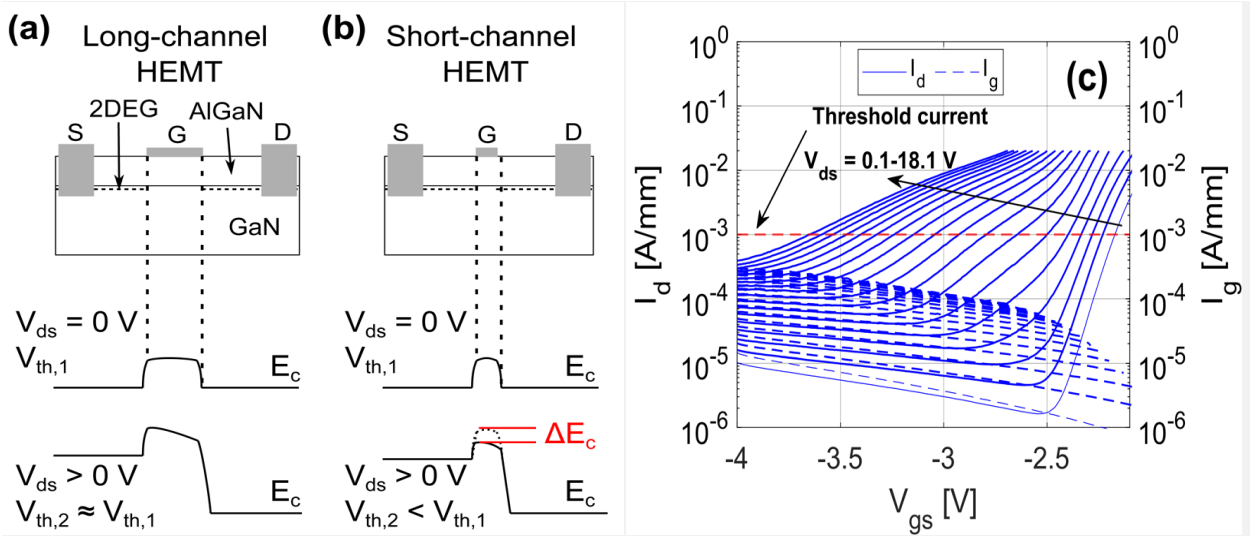


Figure 7.1: An illustration of the conduction band profile for (a) long-channel HEMT and (b) short-channel HEMT at two different drain biases at the AlGaN/GaN interface. (c) An illustration of the transfer properties for an AlGaN/GaN HEMT with Lg = 50 nm at various drain voltages [17].

Table 7-1: Recent research progress in GaN-based HEMTs for high power high frequency RF applications

L_g (nm)	I_d (A/mm)	g_m (S/mm)	R_c (Ω.mm)	R_{on} (Ω.mm)	L_{sd} (µm)	f_t (GHz)	f_{max} (GHz)	P_{out} (W/mm)	Substrate	References
20	4	2.25	0.026	0.23	0.3	342	518	-	SiC	[31], 2012
20	3	1.34	-	0.26	0.05	454	444	-	SiC	[33], 2015
20	2	1		0.3	0.14	301	302	-	SiC	[208], 2013
30	1.57	0.509	0.60	-	1.3	245	13	-	SiC	[195], 2011
30	1.8	0.520	-	1.2	1	300	33	-	SiC	[196], 2011
30	1.5	0.650	0.08	0.54	0.86	370	30	-	SiC	[125], 2012
30	1.9	0.653	0.16	-	0.27	400	33	-	SiC	[197], 2013
40	1.82	0.965	0.03	0.13	0.60	140	405	-	SiC	[198], 2018
40	1.61	0.723	0.03	0.81	1	220	400	-	SiC	[199], 2010
50	2.1	0.800	-	0.3	0.11	221	290	-	SiC	[209], 2017
50	0.9	0.466	0.1	-	1.1	170	363	-	SiC	[71], 2020
50	3.6	0.6	-	0.15	0.8	123	233	3	SiC	[72], 2020
50	1.6	0.415	0.43	-	1	125	270	-	Si	[210], 2021
55	2.8	0.660	0.07	0.6	0.175	250	204	-	Si	[36], 2020
60	2.1	0.800	-	0.3	0.11	210	55	-	SiC	[209], 2017
60	1.65	0.653	-	1.29	1.8	183	191	2.7	SiC	[199], 2017
60	1.53	0.764	-	0.24	0.60	149	263	-	SiC	[211], 2016
70	1.65	0.382	0.32	-	2	162	176	-	SiC	[212], 2011
75	1.05	0.540	0.40	-	1	152	149	2	Si	[201], 2016
75	0.8	0.418	0.46	-	1	170	210	-	SiC	[213], 2013
80	1.1	0.800	0.20	-	3	114	230	1.25	SiC	[214], 2014
80	-	0.388	0.14	0.9	2	176	70	-	Si	[215], 2015
80	1.7	0.387	0.09	0.42	0.25	149	351	-	SiC	[216], 2012

90	1.25	0.345	0.32	1.4	2.3	113	160	4.18	SiC	[217], 2017
90	1.2	0.461	0.25	-	2.5	98	332	-	SiC	[202], 2018
90	0.98	0.530	-	1	1	95	200	-	SiC	[218], 2018
100	1.75	0.530	0.39	-	1	103	162	-	Si	[219], 2011
100	1.65	0.800	0.20	-	3	80	200	-	SiC	[214], 2014
100	1.13	0.550	0.12	-	1.5	115	150	-	Si	[220], 2013
100	1.2	0.330	0.40	-	-	87	112	-	SiC	[221], 2015
100	1.02	0.459	0.40	-	2	90	248	-	Sapphire	[203], 2020
100	**0.80**	**0.24**	**0.65**	**4.7**	**1.5**	**87**	**143**	**-**	**SiC**	**This work**
150	1.4	0.439	0.3	-	2.4	104	205	5.1	Si	[222], 2020
160	1.19	0.354	0.62	-	2.8	79	113.8	-	SiC	[223], 2010
160	2	0.606	0.4	-	1.3	85	103	-	Si	[224], 2011
170	0.59	0.39	0.35		3.5	50	149	-	SiC	[225], 2016
200	1.2	0.390	0.27	-	2.5	40	146	-	SiC	[226], 2016
200	1.096	0.415	0.6	-	3.6	69	110	-	SiC	[227], 2017
200	1.20	0.422	-	-	2.4	81	194	5.1	SiC	[228], 2018
200	0.908	0.210	0.4	3.6	5	55	-	4.58	SiC	[229], 2020
200	0.882	0.217	0.43	-	3.8	38	135	4.6	SiC	[230], 2020
200	**0.78**	**0.18**	**0.65**	**4**	**1.5**	**69**	**121**	**-**	**SiC**	**This work**

7.3 GaN HEMT devices with T-gates

7.3.1 The importance and fabrication of T-gates

The smaller gate length that has to be designed for AlGaN/ GaN HEMT depends on the epitaxial layer structure. An aspect ratio (L_g/d- gate length/ distance to the channel) above 15 is necessary to avoid short channel effects which occur when the channel length is the same order of magnitude as the depletion layer widths of the source and drain junction. Two physical phenomena are attributed to short channel effects. Firstly, the modification of the threshold voltage due to shorter channel length and secondly the limitation on electron drift characteristics in the channel.

Short channel effects can be distinguished into 5 separate effects: surface scattering as the length of the channel becomes shorter the lateral electric field of drain-source voltage becomes stronger, to compensate this electric field induced by the gate voltage increases proportionally attracting the electrons to surface [231] , hot carrier injection, (shorted depletion regions have shorter distance between different potential leading to higher electric field, giving electrons high energy and they get trapped within the device) [232], velocity saturation is above the critical electric field at which the electron speed saturates [233], drain induced barrier lowering (DIBL) can be caused by a high leakage current through the buffer underneath the depleted gate region (punch-through) rather than at the AlGaN/GaN interface. Therefore, it is crucial to raise the buffer layer's resistivity such that the electron distribution is confined to a small area at the III-nitride interface. Another strategy is to add a back-barrier with a wider bandgap (such as AlGaN) to the quantum well to increase electron confinement. Improved gate control made possible by high electron confinement substantially lowers DIBL [234][235]. High Al concentration AlGaN barriers, AlN spacer layers, AlN barriers and/or gate recess can be used to minimise the distance from the gate to channel allowing one to use smaller gate lengths or thinner barrier layer. These strategies can be combined with use of a T-gate geometry to increase the device f_T and f_{MAX} for a certain epilayer structure since it reduces the gate resistance by having a smaller gate-length while keeping the total cross-sectional area large. Moreover, shorter gate lengths result in lower intrinsic gate capacitances (capacitance between the bottom of the gate and the channel). However, the gate head then adds extrinsic capacitances, namely:

- Parallel plate capacitance between the T-gate and surrounding electrodes.
- Fringing capacitance between the gate stem and the access regions.

As the gate length for T-gate structure reduces parasitic components of the capacitance become relatively high and become dominant for the gate capacitance [236]. The head of the T-gate also acts as a field plate above the channel on the drain side reducing the peak electric field within the device. The source/drain contact resistance, which often makes up the majority of the device's extrinsic resistance, can be reduced to further boost performance. Hence, it is necessary to lower the contact resistance from 0.6 Ω.mm to less than 0.1 Ω.mm in order to minimize this loss.
In order to achieve smooth edge roughness and, thus, to permit the further decrease of source-drain distance for high frequency operations, low-temperature annealing temperatures (600°C) are also necessary. For instance, despite the extra expense and challenging fabrication procedure, regrown Ohmics, or recess ohmic connections must be included into the current MMIC manufacturing method. Additional parasitic capacitances between the gate-source pads and gate-drain pads should be taken into consideration because lateral source-drain scaling is preferred to suppress drain delay and velocity

enhancements at frequencies above W-band. By making the T-gate foot (Hg) taller and employing air as a dielectric to provide minimal parasitic capacitances, parasitic capacitances can be avoided.

Figure 7.2 shows a schematic cross-sectional view of the T-gate technique and an overview of the device and associated parasitic capacitance.

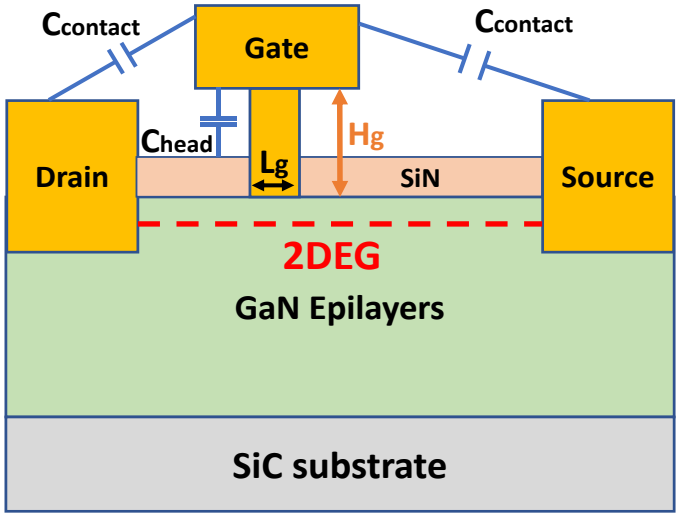


Figure 7.2: Cross-sectional view of T-shaped gate module and associated parasitic capacitance.

In this project we developed a novel recipe for T-gate fabrication. The details of the T-gate development process described in Chapter 3. Electron beam lithography was used to define T-gate structures in a single lithography step. T- gates were fabricated using a metal lift-off process having multiple layers of PMMA, LOR 3A and CSAR e-beam resists as shown in Figure 7.3. The key to obtain 3D gate features is to apply different beam energies to the gate head and gate foot during e-beam exposure. The resist layer stack consisted of 100 nm thick 2041 series PMMA, followed by 300 nm thick LOR 3A followed by 200 nm thick CSAR resist followed by 10 nm Al layer. As mentioned before, series 2010 PMMA has lower molecular weight and therefore it develops slightly faster than CSAR. The LOR3A layer between the two layers of PMMA and CSAR was used as a development stop layer for the gate head and the top Al layer was used as a discharge layer for the e-beam exposure to avoid charging effects on the sample during the exposure process [105].

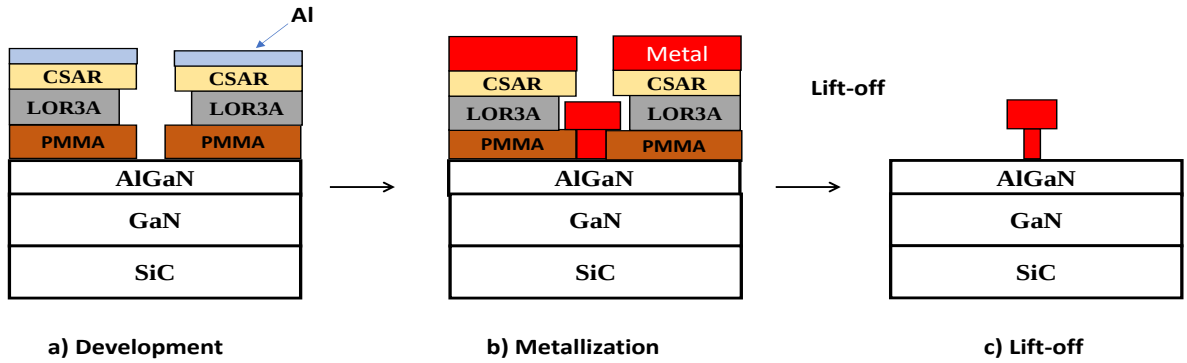


Figure 7.3: T-gates were fabricated using metal lift-off process using multiple layers.

The T-gate fabrication process was incorporated into the device flow used in previous fabrications (full fabrication details can be found in the Appendix A) on a wafer with the epitaxial structure shown in Fig. 7.4. Two finger devices with a gate pitch of 15 µm and different geometry T-gates were successfully fabricated: 100 nm and 200 nm symmetric T-gate devices. Close-up SEM images of fabricated T-gates are shown in Fig. 7.5 for a 100nm gate with a gate head of 500 nm and a 200 nm gate with a gate head of 500 nm.

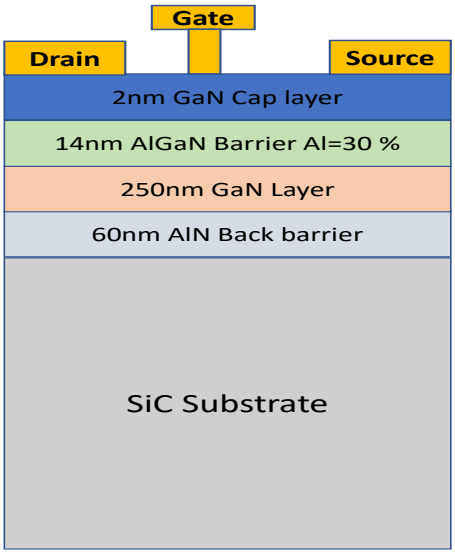
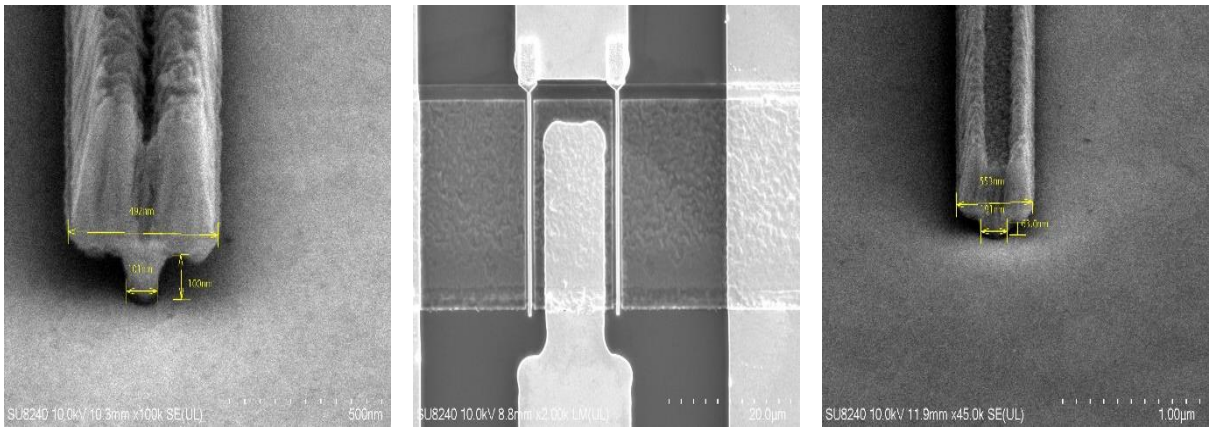


Figure 7.4: Illustration of the epitaxial structure used for T-gate device fabrication.



a) b) c)

Figure 7.5: SEM images of a fabricated T-gates a) 100nm T-gate b) gates between Ohmic metals & c) 200nm T-gate.

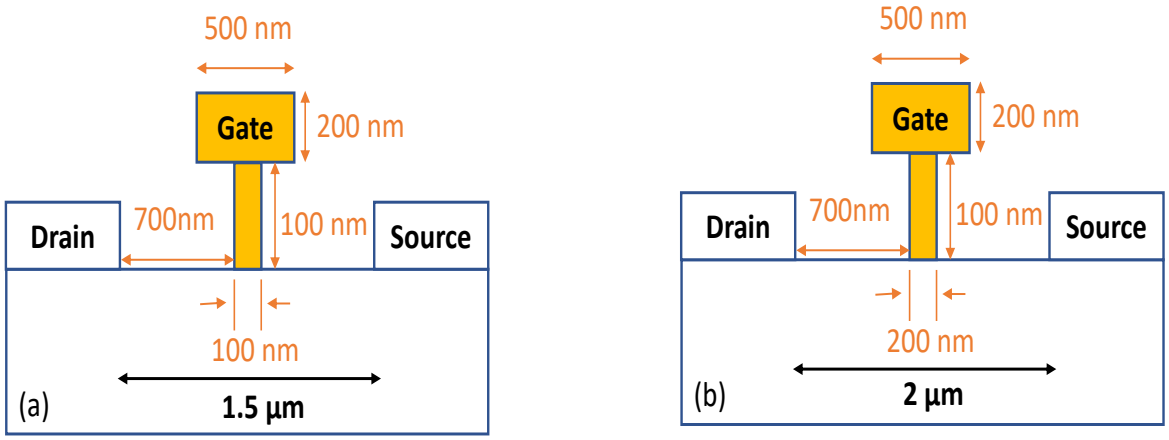


Figure 7.6:T-gate device geometries for a) Device A with 100 nm gate and b) Device B 200 nm gate length.

The T-gate device geometry of 100nm and 200nm as shown in fig. 7.6.

Two 2×25 µm devices with T-gates of gate lengths of 100 nm and 200nm were fabricated at the same time on the GaN-on-SiC wafer grown by hot-wall MOCVD described in chapter 5 following the fabrication steps described in Appendix A. A shallow ~200 nm deep mesa for device isolation was used. Both devices were passivated with 100 nm thick ICP SiN_x film. Ohmic contact resistances extracted from TLM measurements were found to be 0.65 Ω·mm. Device output characteristics were measured on both T-gate devices and are shown Fig.7.7. Both devices exhibit quite high peak currents of 805mA/mm and 785 mA/mm. We attribute this to the low thermal boundary resistance on this wafer.

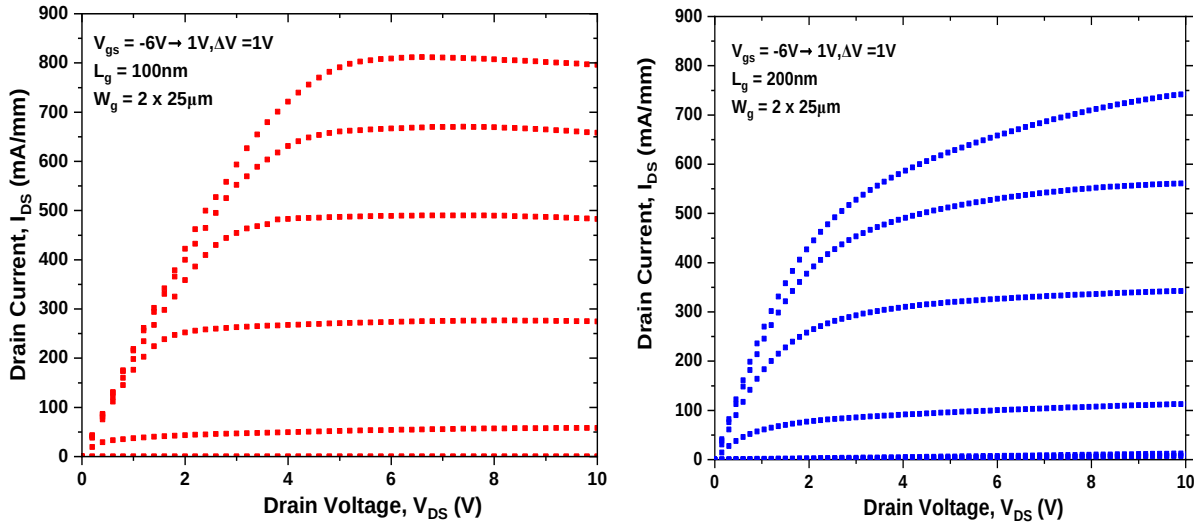


Figure 7.7: DC-IV measurements of 100nm T-gate device and 200 nm T-gate device.

Transconductance and tranfer characteristics of both devices are shown in Fig.7.8. Here, we can see that both devices exhibit similar peak tranconductance values of 246 mS/mm and 181 mS/mm at V_D = 9 V for devices with gatelegths of 100 nm and 200 nm, respectively. The threshold voltage V_{TH} of both the devices found to be -2.4 V.

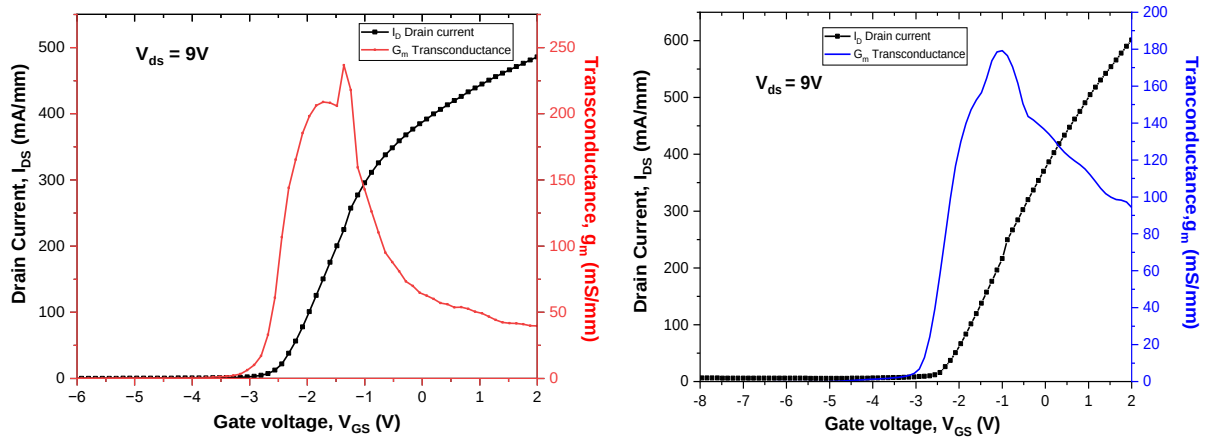


Figure 7.8: Measured a) transconductance and transfer characteristics of 100 nm and 200 nm T-gate devices at V_D = 9V.

Gate leakage currents of both devices were also measured and are shown in Fig. 7.9. Both devices exhibit gate leakage currents in the order of 100 µA/mm which is quite high. The higher gate leakage current for devices is attributed to the thinner barrier layer and higher current density in the channel. Other than gate leakage currents, all other measured device parameters are better on this GaN buffer free wafer, so it is concluded that the hot-wall MOCVD growth process is beneficial for improving the device performance. Leakage currents could be reduced by post gate annealing [237], using Pt based gates [238] or employing gate dielectric [239].

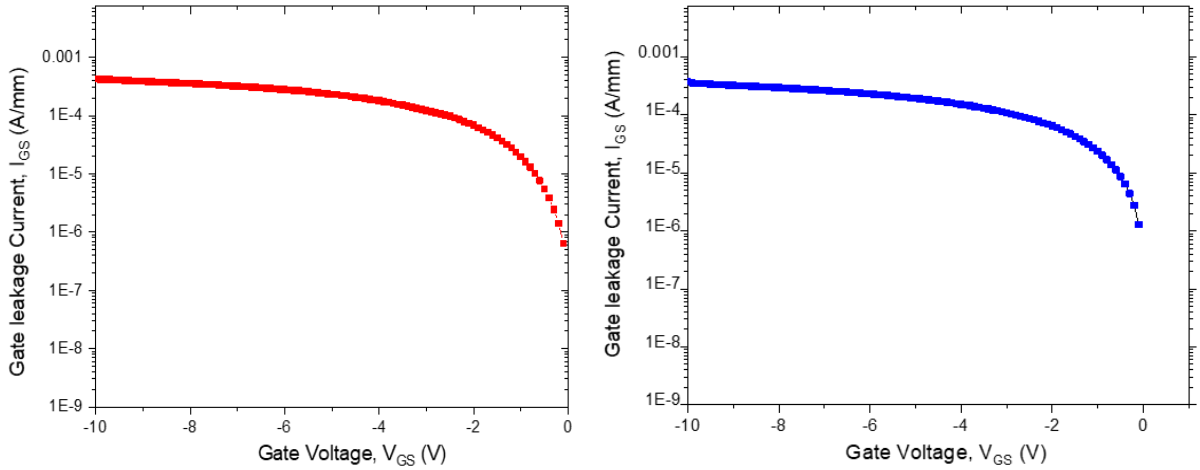


Figure 7.9: Gate leakage currents of 100 and 200 nm T-gate devices at V_D = 0V.

The off-state three-terminal drain-source breakdown characteristics were tested, and the results are shown in Figure 7.10. The devices were biased with a gate voltage V_{GS} of - 12V. The breakdown voltage, V_{BR}, which corresponds to the rapidly increasing currents caused by avalanche breakdown, is the drain voltage at a gate current of 1 mA/mm. The measured critical field breakdown voltage of the 0.1 and 0.2 µm T-gate HEMT devices are 0.31 MV/cm and 0.34 MV/cm, respectively. Due to the limited dimensions of the gate length and the gate-to-drain spacing, the linear relationship between the breakdown voltage and the gate length indicates that the breakdown occurred horizontally.

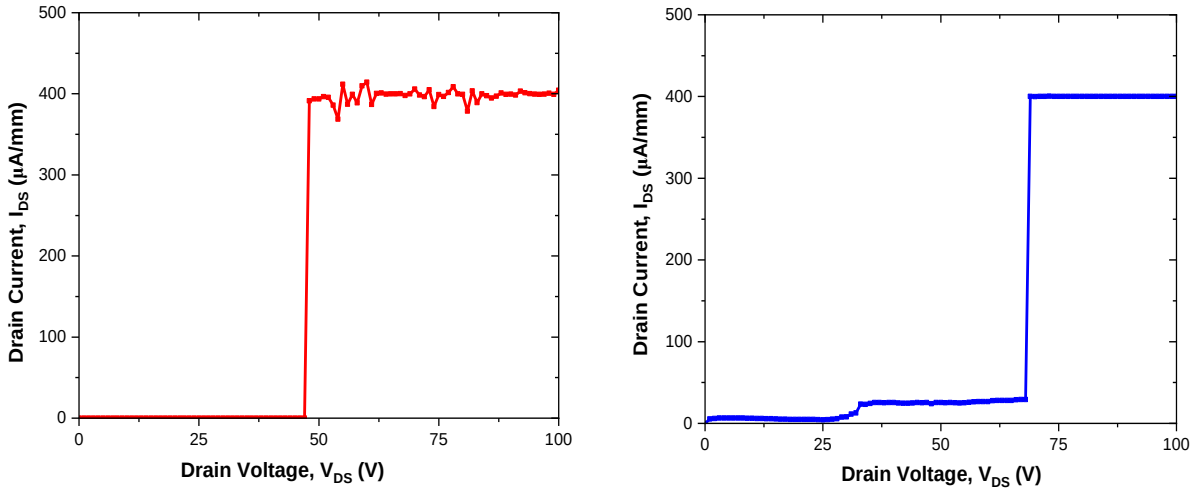


Figure 7.10: Measured lateral off-state breakdown voltage of 100 nm and 200 nm devices biased at V_{GS} = -12 V.

7.3.2 RF measurements

The maximum gain a transistor is capable of delivering at certain drain voltage is at the peak of transconductance for each drain voltage. S-parameters for fabricated devices were measured at V_D = 10 V and V_G = -1.4 V and calculated the values for maximum small signal gain U and hybrid parameter h21 at each frequency. Fig.7.11 shows the current gain, h21, Mason's unilateral power gain, U, and extrapolated f_T and f_{MAX} for both devices. f_T and f_{MAX} are found to be 87/143 GHz and 69/121 GHz for 100 nm and 200 nm gatelength devices, respectively. 200 nm T-gate device exhibits lower gain and cut-off frequency which is attributed to larger source-drain separation.

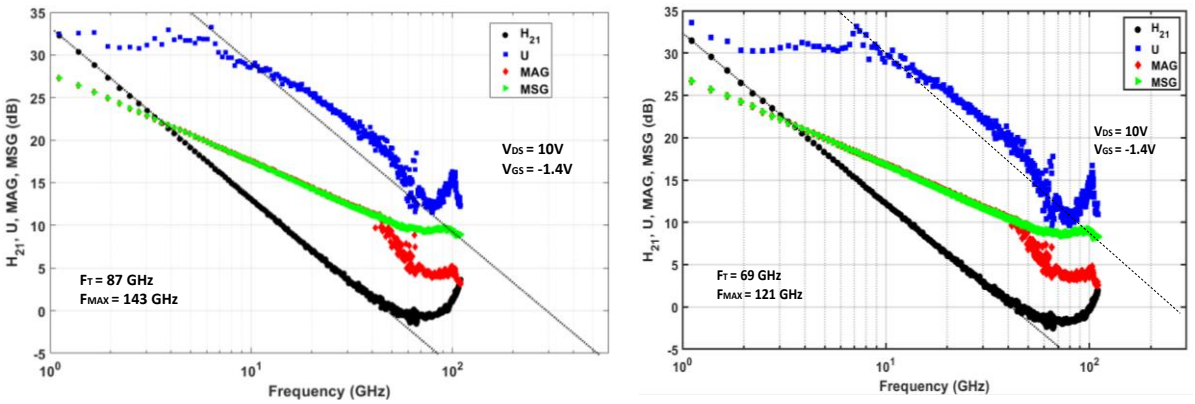


Figure 7.11: Masons unilateral power gain U, current gain H_{21} and extrapolated f_T and f_{MAX} for 100 nm T-gate device and 200 nm T-gate device.

Due to the more evenly distributed electric field devices, T-gate structures were expected to have highet f_T and f_{MAX} than standard gate devices structures. Comparison of cut-off frequencies of 2 finger

devices (pad parasitics included) with different gateleghts for both standard and T-gate geometries fabricated during this project is given in Fig. 7.12. Here, one can see a clear trend of an exponential increase in f_T with reducing gate length. The fabricated T-gate structures follow this trend but do not exhibit cut-off frequencies above the trendline.

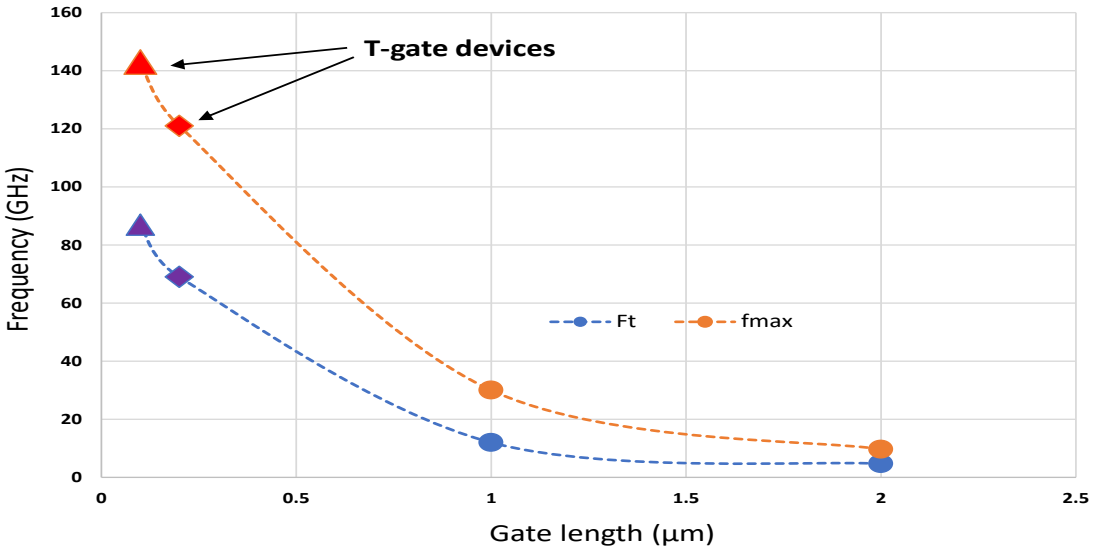


Figure 7.12:Cut-off frequencies of devices fabricated during this project with standard and T-gate geometries.

7.4 Summary

In this chapter, the design, fabrication and characterisation of devices with 100 nm and 200 nm T-gate structures was described and discussed. The main benefit of using T-gate structures is the more uniform electric field compared to standard gate structure. It is concluded that T- gate with larger gate head and small gate length leads to higher gain. However, the fabricated devices exhibit high leakage currents which led to similar cut-off frequencies achievable with a standard gate structure. Reducing the leakage currents would provide even higher cut-off frequencies and achieve the full benefits of employing a T-gate structure.

Chapter 8
Conclusion and future work

8 Conclusions and Future work

GaN HEMTs are extremely promising for future RF and power applications because of their exceptional features, such as high 2DEG sheet carrier density, mobility, and high breakdown fields. Three important areas of AlGaN/GaN technology have benefited from the work done in this project: improved Ohmic contacts, greater understanding of buffer free devices, thermal management for the devices, and T-gate technology for high frequency devices. This chapter provides a summary of the major accomplishments and the prospects for the future.

8.1 Conclusion

8.1.1 Ohmic contacts to AlGaN/GaN HEMTs

A new method for reducing contact resistance in AlGaN/GaN HEMTs has been presented in this thesis. We found that the uneven AlGaN layer thickness underneath the Ohmic metal contacts is responsible for reducing the Ohmic contact resistance. The formation of sidewall area on AlGaN surface during the patterned etching process provides better contact of Ohmic metal resulting in more tunnelling current between the Ohmic metal and AlGaN barrier thus reducing the contact resistance. Experiments showed that this technology works and is repeatable. The lowest contact resistance of 0.32 Ω.mm was observed for a deep (~30 nm) horizontal patterned structure. The fabricated device with this structure also demonstrated the highest maximum saturation drain current of 1285 mA/mm, maximum transconductance of 296 mS/mm and gate leakage current of 1.5µA/mm which is better compared to other fabricated devices. This new approach offers a promising future technique for low resistance contact formation on AlGaN/GaN HEMTs. Figure 8.1 depicts the cross-sectional schematic of horizontal pattern etch on Ohmic region in SiC substrate.

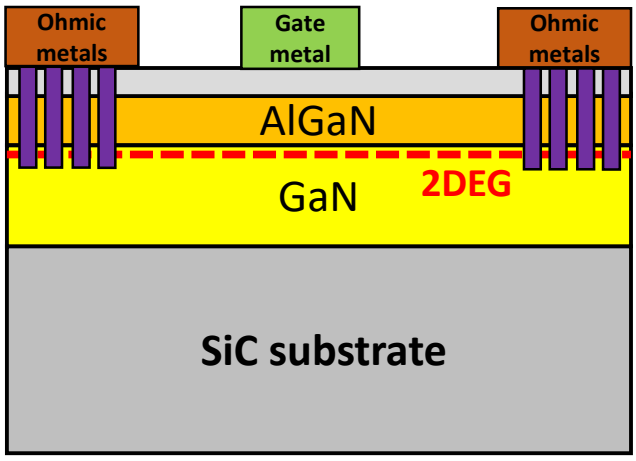


Figure 8.1: Cross-sectional schematic of horizontal patterned Ohmic HEMTs on SiC substrate.

8.1.2 Thermal management on AlGaN/GaN HEMTs

A novel approach to thermal management of GaN based devices was demonstrated. The method relies on the use of dry etching methods to remove the inactive GaN epi-layers around the device active area from the top side. The heat created at the 2DEG channel may be efficiently transferred to the SiC substrate by bond pads (Ti/Au) high thermally conductive metal. This allows device to operate at higher power densities and also reduces cooling requirements. The approach exploits the thin epitaxial stack

for the buffer-free device structure. The MIS-HEMT device made using this approach the side walls of mesa etch was covered with thin layer of Silicon Nitride which improved the leakage current and current density. Overall, this new buffer-free epitaxial approach has great potential for producing high performance GaN HEMTs for high-power and high-frequency applications.

8.1.3 T-Gate fabrication

In general, the RF performance of a high-speed device, such as a HEMT, is closely related to the quality of the substrate material, the device layer structure, the electronic property of the conducting channel and the effective channel length related to the foot-width of the T shape gate, the Ohmic contact resistance of the source and the drain contacts, and the device structure layout, such as the source-drain distance, and so on. Among all these considerations, nanoscale T shape gates play a critical role in setting a HEMT's current cut-off frequency (f_T). Decreasing the T shape gate's foot-width raises the operating frequency f_T [240]. Generally speaking, designing robust T-gate shaped structures is still challenging. T-shape gate fabrication consists of two major processes. The first is to use lithography to create T-shape profiles in resists, and the second is to use metallization and lift off to transfer the resist pattern into metallic gates. We developed and demonstrated the new fabrication process of sub-100nm T-gate structures using a single electron beam lithography exposure and a tri-layer resist stack - PMMA/LOR/CSAR Figure 8.2 shows the T-gate process developed using 3-layer resist process.

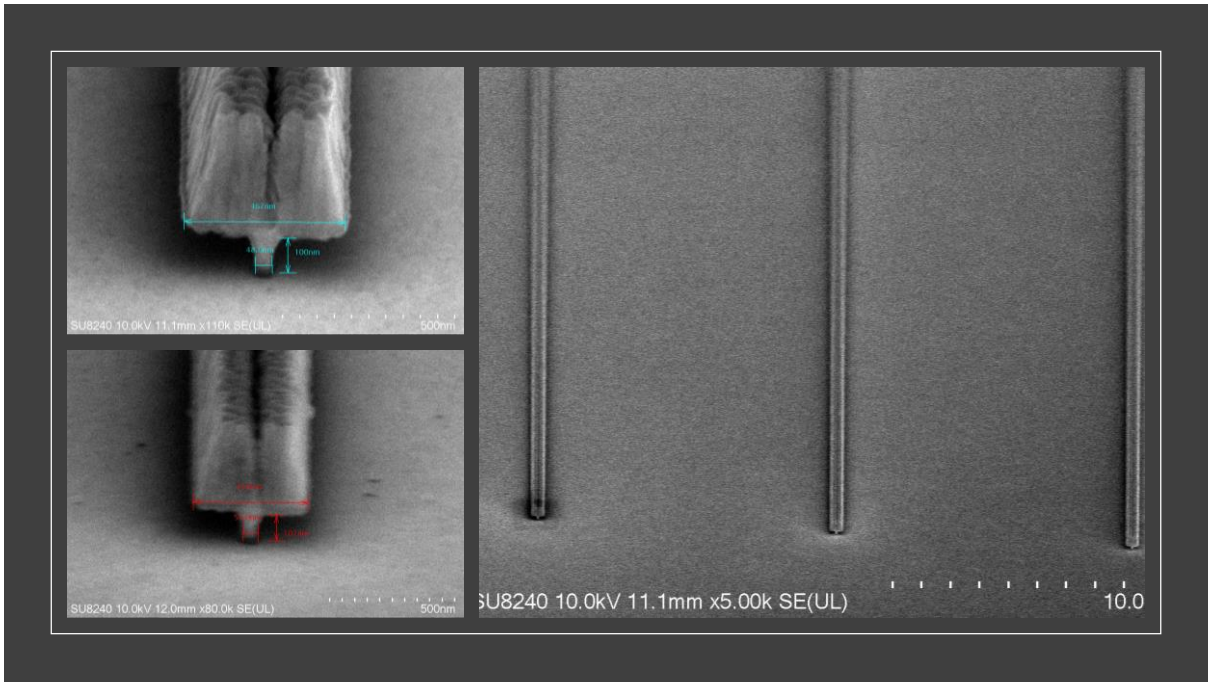


Figure 8.2: SEM micrographs of different gate length of fabricated gates.

8.2 Future work

8.2.1 Proposed GaN/diamond-on-SiC

GaN-on-Diamond devices have already demonstrated three times greater power densities than GaN-on-SiC devices [241]. This is due to diamond's greater heat conductivity when compared to SiC [242]. However, because to the lattice mismatch between diamonds and III-Nitride materials, developing good quality GaN-on-diamonds is problematic. As a result, filling the diamond around the active area

processing on GaN-on-SiC technology is proposed to combine the moderate-cost advantage of GaN-on-SiC with the high heat conductivity of diamond. Figure 8.3 shows proposed GaN on SiC with integrated diamond model.

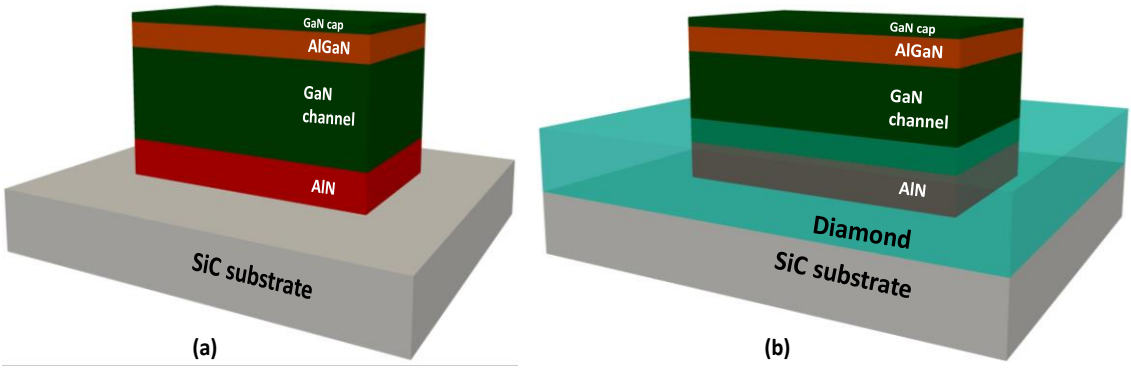


Figure 8.3: GaN HEMT proposed model (a) Mesa etch SiC substrate (b) integrated diamond heat sink.

8.2.2 Proposed buffer-free AlN/GaN HEMT structure

Ultrashort gate lengths (≤ 100 nm) are necessary to increase the speed (cut-off frequency) of GaN-on-SiC devices, as shown in Table 7.1. A high aspect ratio and 2DEG density may be achieved by using an ultrathin AlN barrier (≤ 5 nm) in place of AlGaN [72]. Figure 8.4 depicts a novel material structure. According to the study [243], the innovative idea of employing a total GaN layer thickness of 250 nm without a buffer layer. Device results in this thesis show that "buffer-free" material can outperform traditional materials at the device level. A thin undoped GaN channel layer sandwiched between an AlN barrier layer and a low TBR AlN nucleation layer that functions as a sandwich-like double heterostructure and provides adequate 2DEG confinement with significantly fewer trapping effects than traditional Fe- and C-doped buffer containing epi-structures. Also, in general, forming excellent Ohmic contact to AlN/GaN-based devices is difficult due to the use of a barrier layer with a large bandgap AlN (6.2 eV) as opposed to traditional AlGaN/GaN-based devices. The horizontal patterned recess Ohmic contact technology can be used to reduce the contact resistance as described in section 8.1. Figure 8.4 shows the proposed epilayer AlN/GaN on SiC structure.

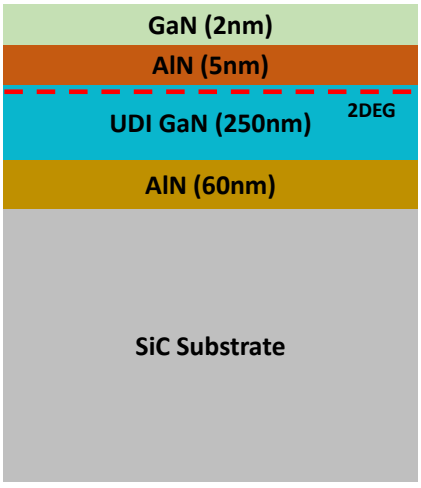


Figure 8.4: Proposed epilayer AlN/GaN structure

Appendix A

RF device fabrication using photolithography.

1) **Sample cleaning**

- Dip in Acetone for 5 minutes using ultrasonic bath
- Dip in Methanol for 5 minutes using ultrasonic bath
- Dip in Isopropyl Alcohol (IPA) for 5 minutes using ultrasonic bath
- Blow dry using N_2

2) Ohmic contact deposition

- Spin LOR 10A at 6000rpm for 30seconds
- Bake at 150ºC for 2 minutes
- Spin S1805 at 4000 rpm for 30seconds
- Bake at 115ºC 3 for minutes
- Expose in the MA6 mask aligner using hard contact for 2.4 seconds
- Develop using MF319 for 2 minutes
- Rinse in Reverse Osmosis (RO) water
- Blow dry with N_2
- Oxygen ash at 110W for 1 minute
- De-oxidise in $3H_2O$:HCl for 1 min
- Use Ar gun for 30 seconds in the Plassys IV
- Metalize Ti/Al/Ni/Au 30/180/40/100nm
- Lift-off using 1165 resist stripper in the hot water bath for 15 minutes, pipette clean
- Rinse with water
- Blow dry with N_2
- Anneal the sample in N_2 environment at 800°C for 30 seconds

3) Mesa isolation

- Spin S1818 at 4000rpm for 30 seconds
- Bake at 115ºC for 2 minutes
- Expose in the MA6 using hard contact for 6 seconds
- Develop using MF319 for 75 seconds
- Rinse with RO water
- Blow dry with N2
- ICP 180 with Cl2/Ar gases with 30/15sccm and RF/ICP power of 750/75W at 4mT for 1minutes
- Remove resist using Acetone
- Dip in IPA
- Blow dry with N_2

4) Gate contact deposition

- Spin LOR 3A at 6000rpm for 30seconds
- Bake at 150ºC for 2 minutes

- Spin S1805 at 4000 rpm for 30seconds
- Bake at 115ºC 3 for minutes
- Expose in the MA6 mask aligner using hard contact for 2.4 seconds
- Develop using MF319 for 2 minutes
- Rinse in RO water
- Blow dry with N_2
- Oxygen ash at 110W for 1 minute
- Metalize Ni/Au 20/200nm
- Lift-off using 1165 resist stripper in the hot water bath for 15 minutes, pipette clean
- Rinse with RO water
- Blow dry with N_2

5) Bond pad deposition

- Spin LOR 10A at 6000rpm for 30seconds
- Bake at 150ºC for 2 minutes
- Spin S1805 at 4000 rpm for 30seconds
- Bake at 115ºC for 3 minutes
- Expose in the MA6 mask aligner using hard contact for 2.4 seconds
- Develop using MF319 for 2 minutes
- Rinse in RO water
- Blow dry with N_2
- Oxygen ash at 110W for 1 minute
- Metalize Ni/Au 20/400nm
- Lift-off using 1165 resist stripper in the hot water bath for 15 minutes, pipette clean
- Rinse with RO water
- Blow dry with N_2

6) Surface passivation

- Deposit 100nm of Si3N4 using ICP 180 PECVD Deposition tool

7) Passivation etches

- RIE 80+ tool with SF_6/N_2 gases with 50/25sccm and RF power of 50W at 100mT for 5minutes

RF device fabrication using E-beam lithography

1) **Sample cleaning**

- Dip in Acetone for 5 minutes using ultrasonic bath
- Dip in Methanol for 5 minutes using ultrasonic bath
- Dip in Isopropyl Alcohol (IPA) for 5 minutes using ultrasonic bath
- Blow dry using N2

2) E-beam markers

- Spin 12% 2010 PMMA at 4000rpm for 60 seconds
- Bake at 180ºC for 3 min

- Spin 4% 2041 at 4000 rpm for 60 seconds
- Bake at 155ºC for 2 minutes
- Metallize with 10nm Al layer (Plassys 2 or 4)
- Expose at EBPG for markers
- Develop in CD-26 for 1min
- Dip in RO water for 1min
- Develop in MIBK: IPA 2.5:1 for 60 seconds at 23ºC
- Dip in IPA
- Blow dry with N_2
- Metalize Ti/Pt 20/80nm
- Lift-off in warm acetone for 15min, pipette clean
- Dip in IPA
- Check under microscope all the square markers

3) Ohmic contact formation

- Spin 12% 2010 PMMA at 4000rpm for 60 seconds
- Bake at 180ºC for 3 min
- Spin 4% 2041 at 4000 rpm for 60 seconds
- Bake at 155ºC for 2 minutes
- Metallize with 10nm Al layer (Plassys 2 or 4)
- Expose at EBPG for Ohmics patterns
- Develop in CD-26 for 1min
- Dip in RO water for 1min
- Develop in MIBK: IPA 2.5:1 for 60 seconds at 23ºC
- Dip in IPA
- Blow dry with N2
- Ash 110W for 1 min
- Deoxidized in HCl 1:3 RO water for 1 minute
- Rinse in RO water
- Blow dry with N2
- Use Ar gun in Plassys IV for 30 seconds
- Metalize Ti/Al/Mo/Au 15/60/35/50nm
- Metalize Ti/Pt 20/80nm
- Lift-off in warm acetone for 15min, pipette clean
- Dip in IPA
- Anneal at 800ºC for 30 seconds
- Check under microscope all the Ohmic patterns

3) Mesa isolation

- Spin 12% 2010 PMMA at 4000rpm for 60 seconds
- Bake at 180ºC for 3 min
- Spin 4% 2041 at 4000 rpm for 60 seconds
- Bake at 155ºC for 2 minutes
- Metallize with 10nm Al layer (Plassys 2 or 4)
- Expose at EBPG for mesa isolation
- Develop in CD-26 for 1min
- Din in RO water for 1min
- Develop in MIBK: IPA 2.5:1 for 60 seconds at 23ºC
- Dip in IPA

- Blow dry with N_2
- Submit sample for dry etch in ICP 180 (100nm etch)
  Step 1) Pre-condition for 15min
  Step 2) Tool: ICP 180
  Gases BCl_3/Cl_2 flow= 5/10sccm, RF and ICP power: 13/100 W,
  Pressure= 20mTorr, Etching time= 10 min
- Lift-off in warm acetone for 15min, pipette clean
- Dip in IPA
- Blow dry with N_2

4) T-Gates

- Spin 4% 2041 at 2000 rpm for 60 seconds (Recipe-8)
- Bake at 180ºC for 3 minutes
- Spin 4% 2041 at 2000 rpm for 60 seconds (Recipe-8)
- Bake at 180ºC for 3 minutes
- Spin LOR 3A at 6000 rpm for 30seconds (Recipe-1)
- Bake at 150ºC for 2 minutes
- Spin CSAR at 2000 rpm for 60seconds (Recipe-8)
- Bake at 150ºC for 2 minutes
- Expose at EBPG for T-Gate pattern
- Develop in CD-26 for 1min
- Din in RO water
- Blow dry with N_2
- Develop in amyl acetate for 30 seconds
- Dip in IPA for 30 seconds
- Blow dry with N_2
- Develop in CD-26 for 25 seconds
- Dip in RO for 30 seconds
- Blow dry with N_2
- Develop in MIBK: IPA 3:1 for 35 seconds at 23ºC
- Dip in IPA for 30 seconds
- Blow dry with N2
- Ash 80W for 1 min
- Metalize Ni/Au 20/300 nm
- Lift-off in warm acetone for 15min, clean very carefully
- Blow dry with hotplate

5) SiNx passivation

- Submit sample for blanket deposition of 100nm of SiNx (PECVD tool)

6) Bond pads

- Spin 12% 2010 PMMA at 4000rpm for 60 seconds
- Bake at 180ºC for 3 min
- Spin 4% 2041 at 4000 rpm for 60 seconds
- Bake at 155ºC for 2 minutes
- Metallize with 10nm Al layer (Plassys 2 or 4)
- Expose at EBPG for bond-pads pattern
- Develop in CD-26 for 1min

- Develop in MIBK: IPA 2.5:1 for 60 seconds at 23ºC
- Dip in IPA
- Blow dry with N2
- Ash 110W for 1 min
- Submit sample for dry etch RIE80+ (100nm etch)
- Recipe name: SF_6/N_2
- RF power 50 W, SF_6/N_2 50/25 sccm and pressure 100 mT
- Etching time: 5 Minute
- Metalize Ti/Au 20/400nm
- Dip in IPA for 30 seconds
- Blow dry with N_2
- Check under microscope

7) SiNx passivation

- Submit sample for blanket deposition of 100nm of Si_3N_4 (PECVD tool)

8) Passivation etches

- RIE 80+ tool with SF_6/N_2 gases with 50/25sccm and RF power of 50W at 100mT for 5minutes

References

[1] H. Tataria, M. Shafi, A. F. Molisch, M. Dohler, H. Sjoland, and F. Tufvesson, "6G Wireless Systems: Vision, Requirements, Challenges, Insights, and Opportunities," *Proc. IEEE*, vol. 109, no. 7, pp. 1166–1199, Jul. 2021, doi: 10.1109/JPROC.2021.3061701.

[2] Samsung Research, "6G: The Next Hyper Connected Experience for All.," *White Pap.*, pp. 1–44, 2020, [Online]. Available: https://research.samsung.com/next-generation-communications

[3] M. S. Adler, K. W. Owyang, B. Jayant Baliga, and R. A. Kokosa, "The Evolution of Power Device Technology," *IEEE Trans. Electron Devices*, vol. 31, no. 11, pp. 1570–1591, 1984, doi: 10.1109/T-ED.1984.21754.

[4] T. Mimura, S. Hiyamizu, T. Fujii, and K. Nanbu, "A New Field-Effect Transistor with Selectively Doped GaAs/n-Al x Ga 1- x As Heterojunctions," *Jpn. J. Appl. Phys.*, vol. 19, no. 5, pp. L225–L227, May 1980, doi: 10.1143/JJAP.19.L225.

[5] U. K. Mishra, Shen Likun, T. E. Kazior, and Yi-Feng Wu, "GaN-Based RF Power Devices and Amplifiers," *Proc. IEEE*, vol. 96, no. 2, pp. 287–305, Feb. 2008, doi: 10.1109/JPROC.2007.911060.

[6] U. V. Bhapkar and M. S. Shur, "Monte Carlo calculation of velocity-field characteristics of wurtzite GaN," *J. Appl. Phys.*, vol. 82, no. 4, pp. 1649–1655, 1997, doi: 10.1063/1.365963.

[7] J. Cho, E. Bozorg-Grayeli, D. H. Altman, M. Asheghi, and K. E. Goodson, "Low Thermal Resistances at GaN–SiC Interfaces for HEMT Technology," *IEEE Electron Device Lett.*, vol. 33, no. 3, pp. 378–380, Mar. 2012, doi: 10.1109/LED.2011.2181481.

[8] R. T. R. T. Kemerley, H. B. B. Wallace, and M. N. M. N. Yoder, "Impact of wide bandgap microwave devices on DoD systems," *Proc. IEEE*, vol. 90, no. 6, pp. 1059–1064, Jun. 2002, doi: 10.1109/JPROC.2002.1021570.

[9] A. S. A. Fletcher and D. Nirmal, "A survey of Gallium Nitride HEMT for RF and high power applications," *Superlattices Microstruct.*, vol. 109, pp. 519–537, 2017, doi: 10.1016/j.spmi.2017.05.042.

[10] B. Raphael, "A Novel AlGaN / GaN Based Enhancement Mode High Electron Transistor with Sub-critical Barrier Thickness," 2015.

[11] J.-L. Liu *et al.*, "8.7 W/mm output power density and 42% power-added-efficiency at 30 GHz for AlGaN/GaN HEMTs using Si-rich SiN passivation interlayer," *Appl. Phys. Lett.*, vol. 120, no. 5, p. 052101, Jan. 2022, doi: 10.1063/5.0080120.

[12] X. Luo *et al.*, "Scaling and high-frequency performance of AlN/GaN HEMTs," in *2011 IEEE International Symposium on Radio-Frequency Integration Technology*, Nov. 2011, pp. 209–212. doi: 10.1109/RFIT.2011.6141776.

[13] S. Sarkar, R. P. Khade, A. DasGupta, and N. DasGupta, "Effect of GaN cap layer on the performance of AlInN/GaN-based HEMTs," *Microelectron. Eng.*, vol. 258, no. December 2021, p. 111756, Apr. 2022, doi: 10.1016/j.mee.2022.111756.

[14] D. Biswas, H. Fujita, N. Torii, and T. Egawa, "Effect of In composition on electrical performance of AlInGaN/GaN-based metal-insulator-semiconductor high electron mobility transistors (MIS-HEMTs) on Si," *J. Appl. Phys.*, vol. 125, no. 22, p. 225707, Jun. 2019, doi: 10.1063/1.5098365.

[15] T. Satoh, K. Osawa, and A. Nitta, "GaN HEMT for Space Applications," in *2018 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS)*, Oct. 2018, pp. 136–139. doi: 10.1109/BCICTS.2018.8551070.

[16] T. N. T. Do *et al.*, "7–13 GHz MMIC GaN HEMT Voltage-Controlled-Oscillators (VCOs) for satellite applications," in *2017 12th European Microwave Integrated Circuits Conference (EuMIC)*, Oct. 2017, vol. 2017-Janua, pp. 220–223. doi: 10.23919/EuMIC.2017.8230699.

[17] E. Ture *et al.*, “First demonstration of W-band Tri-gate GaN-HEMT power amplifier MMIC with 30 dBm output power,” in *2017 IEEE MTT-S International Microwave Symposium (IMS)*, Jun. 2017, pp. 35–37. doi: 10.1109/MWSYM.2017.8058452.

[18] A. Barabi, N. Ross, A. Wolfman, O. Shaham, and E. Socher, “A +27 dBm Psat 27 dB Gain W-Band Power Amplifier in 0.1 µm GaAs,” *IEEE MTT-S Int. Microw. Symp. Dig.*, vol. 2018-June, pp. 1345–1347, 2018, doi: 10.1109/MWSYM.2018.8439854.

[19] R. Maurer, S. K. Kim, M. Urteaga, and M. J. W. Rodwell, “High-Linearity W-Band Amplifiers in 130 nm InP HBT Technology,” *Tech. Dig. - IEEE Compd. Semicond. Integr. Circuit Symp. CSIC*, vol. 2016-Novem, pp. 2–5, 2016, doi: 10.1109/CSICS.2016.7751042.

[20] J. S. Moon *et al.*, “Power Scaling of Graded-Channel GaN HEMTs with Mini-Field-Plate T-gate and 156 GHz fT,” *IEEE Electron Device Lett.*, vol. 42, no. 6, pp. 796–799, 2021, doi: 10.1109/LED.2021.3075926.

[21] B. N. Pushpakaran, A. S. Subburaj, and S. B. Bayne, “Commercial GaN-Based Power Electronic Systems: A Review,” *J. Electron. Mater.*, vol. 49, no. 11, pp. 6247–6262, Nov. 2020, doi: 10.1007/s11664-020-08397-z.

[22] K. Osawa, H. Yoshikoshi, A. Nitta, T. Tanaka, E. Mitani, and T. Satoh, “Over 74% efficiency, L-band 200W GaN-HEMT for space applications,” in *2016 46th European Microwave Conference (EuMC)*, Oct. 2016, pp. 397–400. doi: 10.1109/EuMC.2016.7824363.

[23] A. Hariya *et al.*, “Circuit Design Techniques for Reducing the Effects of Magnetic Flux on GaN-HEMTs in 5-MHz 100-W High Power-Density LLC Resonant DC–DC Converters,” *IEEE Trans. Power Electron.*, vol. 32, no. 8, pp. 5953–5963, Aug. 2017, doi: 10.1109/TPEL.2016.2616439.

[24] A. Dadgar, C. Hums, A. Diez, J. Bläsing, and A. Krost, “Growth of blue GaN LED structures on 150-mm Si(111),” *J. Cryst. Growth*, vol. 297, no. 2, pp. 279–282, Dec. 2006, doi: 10.1016/j.jcrysgro.2006.09.032.

[25] F. Iucolano and T. Boles, “GaN-on-Si HEMTs for wireless base stations,” *Mater. Sci. Semicond. Process.*, vol. 98, no. November 2018, pp. 100–105, Aug. 2019, doi: 10.1016/j.mssp.2019.03.032.

[26] C. Xie and A. Pavio, “Development of GaN HEMT based High Power High Efficiency Distributed Power Amplifier for Military Applications,” in *MILCOM 2007 - IEEE Military Communications Conference*, Oct. 2007, pp. 1–4. doi: 10.1109/MILCOM.2007.4455083.

[27] P. Europe, “semiconductor TODAY Power semiconductors News from IMS and PCIM Europe,” vol. 2935, 2018.

[28] Y.-K. Lin *et al.*, “A versatile low-resistance ohmic contact process with ohmic recess and low-temperature annealing for GaN HEMTs,” *Semicond. Sci. Technol.*, vol. 33, no. 9, p. 095019, Sep. 2018, doi: 10.1088/1361-6641/aad7a8.

[29] M. F. Abdullah, M. R. Mat Hussin, M. A. Ismail, and S. K. Wan Sabli, “Chip-level thermal management in GaN HEMT: Critical review on recent patents and inventions,” *Microelectron. Eng.*, vol. 273, no. November 2022, p. 111958, Mar. 2023, doi: 10.1016/j.mee.2023.111958.

[30] Z. Chen *et al.*, “A novel Si-rich SiN bilayer passivation with thin-barrier AlGaN/GaN HEMTs for high performance millimeter-wave applications,” *Chinese Phys. B*, vol. 31, no. 11, p. 117105, Nov. 2022, doi: 10.1088/1674-1056/ac81a6.

[31] K. Shinohara *et al.*, “Self-aligned-gate GaN-HEMTs with heavily-doped n+-GaN ohmic contacts to 2DEG,” in *2012 International Electron Devices Meeting*, Dec. 2012, pp. 27.2.1-27.2.4. doi: 10.1109/IEDM.2012.6479113.

[32] B. Benakaprasad, A. M. Eblabla, X. Li, K. G. Crawford, and K. Elgaid, “Optimization of Ohmic Contact for AlGaN/GaN HEMT on Low-Resistivity Silicon,” *IEEE Trans. Electron Devices*, vol. 67, no. 3, pp. 863–868, Mar. 2020, doi: 10.1109/TED.2020.2968186.

[33] Y. Tang *et al.*, “Ultrahigh-speed GaN high-electron-mobility transistors with fT/fmax of 454/444 GHz,” *IEEE Electron Device Lett.*, vol. 36, no. 6, pp. 549–551, Jun. 2015, doi: 10.1109/LED.2015.2421311.

[34] I. Abid *et al.*, "AlGaN Channel High Electron Mobility Transistors with Regrown Ohmic Contacts," *Electronics*, vol. 10, no. 6, p. 635, Mar. 2021, doi: 10.3390/electronics10060635.

[35] W. Wojtasiak *et al.*, "AlGaN/GaN High Electron Mobility Transistors on Semi-Insulating Ammono-GaN Substrates with Regrown Ohmic Contacts," *Micromachines*, vol. 9, no. 11, p. 546, Oct. 2018, doi: 10.3390/mi9110546.

[36] L. Li *et al.*, "GaN HEMTs on Si With Regrown Contacts and Cutoff/Maximum Oscillation Frequencies of 250/204 GHz," *IEEE Electron Device Lett.*, vol. 41, no. 5, pp. 689–692, May 2020, doi: 10.1109/LED.2020.2984727.

[37] T. Zimmermann *et al.*, "AlN/GaN Insulated-Gate HEMTs With 2.3 A/mm Output Current and 480 mS/mm Transconductance," *IEEE ELECTRON DEVICE Lett.*, vol. 29, no. 7, 2008, doi: 10.1109/LED.2008.923318.

[38] C. Wang *et al.*, "An Electrothermal Model for Empirical Large- Signal Modeling of AlGaN/GaN HEMTs Including Self-Heating and Ambient Temperature Effects," *IEEE Trans. Microw. Theory Tech.*, vol. 62, no. 12, pp. 2878–2887, Dec. 2014, doi: 10.1109/TMTT.2014.2364821.

[39] J. D. Albrecht, R. P. Wang, P. P. Ruden, M. Farahmand, and K. F. Brennan, "Electron transport characteristics of GaN for high temperature device modeling," *J. Appl. Phys.*, vol. 83, no. 9, pp. 4777–4781, May 1998, doi: 10.1063/1.367269.

[40] V. O. Turin and A. A. Balandin, "Electrothermal simulation of the self-heating effects in GaN-based field-effect transistors," *J. Appl. Phys.*, vol. 100, no. 5, p. 054501, Sep. 2006, doi: 10.1063/1.2336299.

[41] F. Yang, S. Dalcanale, M. Gajda, S. Karboyan, M. J. Uren, and M. Kuball, "The Impact of Hot Electrons and Self-Heating During Hard-Switching in AlGaN/GaN HEMTs," *IEEE Trans. Electron Devices*, vol. 67, no. 3, pp. 869–874, Mar. 2020, doi: 10.1109/TED.2020.2968212.

[42] V. Sodan, H. Oprins, S. Stoffels, M. Baelmans, and I. De Wolf, "Influence of Field-Plate Configuration on Power Dissipation and Temperature Profiles in AlGaN/GaN on Silicon HEMTs," *IEEE Trans. Electron Devices*, vol. 62, no. 8, pp. 2416–2422, Aug. 2015, doi: 10.1109/TED.2015.2439055.

[43] H. Guo, Y. Li, X. Yu, J. Zhou, and Y. Kong, "Thermal Performance Improvement of AlGaN/GaN HEMTs Using Nanocrystalline Diamond Capping Layers," *Micromachines*, vol. 13, no. 9, p. 1486, Sep. 2022, doi: 10.3390/mi13091486.

[44] L. Yates *et al.*, "Characterization of the Thermal Conductivity of CVD Diamond for GaN-on-Diamond Devices," in *2016 IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS)*, Oct. 2016, vol. 2016-Novem, pp. 1–4. doi: 10.1109/CSICS.2016.7751032.

[45] H. Zhang and Z. Guo, "Near-junction microfluidic cooling for GaN HEMT with capped diamond heat spreader," *Int. J. Heat Mass Transf.*, vol. 186, p. 122476, May 2022, doi: 10.1016/j.ijheatmasstransfer.2021.122476.

[46] A. F. Al-Neama, N. Kapur, J. Summers, and H. M. Thompson, "Thermal management of GaN HEMT devices using serpentine minichannel heat sinks," *Appl. Therm. Eng.*, vol. 140, pp. 622–636, Jul. 2018, doi: 10.1016/j.applthermaleng.2018.05.072.

[47] S. Cheng, P.-C. Chou, W.-H. Chieng, and E. Y. Chang, "Enhanced lateral heat dissipation packaging structure for GaN HEMTs on Si substrate," *Appl. Therm. Eng.*, vol. 51, no. 1–2, pp. 20–24, Mar. 2013, doi: 10.1016/j.applthermaleng.2012.08.009.

[48] J. Cho, Y. Li, D. H. Altman, W. E. Hoke, M. Asheghi, and K. E. Goodson, "Temperature dependent thermal resistances at GaN-substrate interfaces in GaN composite substrates," *Tech. Dig. - IEEE Compd. Semicond. Integr. Circuit Symp. CSIC*, no. c, pp. 12–15, 2012, doi: 10.1109/CSICS.2012.6340094.

[49] S. García, I. Íñiguez-de-la-Torre, J. Mateos, T. González, and S. Pérez, "Impact of substrate and thermal boundary resistance on the performance of AlGaN/GaN HEMTs analyzed by means of electro-thermal Monte Carlo simulations," *Semicond. Sci. Technol.*, vol. 31, no. 6, p. 065005, Jun. 2016, doi: 10.1088/0268-1242/31/6/065005.

[50] G. J. Riedel *et al.*, "Reducing Thermal Resistance of AlGaN/GaN Electronic Devices Using Novel Nucleation Layers," *IEEE Electron Device Lett.*, vol. 30, no. 2, pp. 103–106, Feb. 2009, doi: 10.1109/LED.2008.2010340.

[51] A. De and C. E. Pryor, "Predicted band structures of III-V semiconductors in the wurtzite phase," *Phys. Rev. B*, vol. 81, no. 15, p. 155210, Apr. 2010, doi: 10.1103/PhysRevB.81.155210.

[52] H. Okumura, S. Misawa, and S. Yoshida, "Epitaxial growth of cubic and hexagonal GaN on GaAs by gas-source molecular-beam epitaxy," *Appl. Phys. Lett.*, vol. 59, no. 9, pp. 1058–1060, Aug. 1991, doi: 10.1063/1.106344.

[53] C. Wilhelm, A. Larrue, X. Dai, D. Migas, and C. Soci, "Anisotropic photonic properties of III–V nanowires in the zinc-blende and wurtzite phase," *Nanoscale*, vol. 4, no. 5, p. 1446, 2012, doi: 10.1039/c2nr00045h.

[54] M. N. Fireman, H. Li, S. Keller, U. K. Mishra, and J. S. Speck, "Growth of N-polar GaN by ammonia molecular beam epitaxy," *J. Cryst. Growth*, vol. 481, pp. 65–70, Jan. 2018, doi: 10.1016/j.jcrysgro.2017.10.033.

[55] J. Pal, G. Tse, V. Haxha, M. A. Migliorato, and S. Tomić, "Importance of non linear piezoelectric effect in Wurtzite III-N semiconductors," *Opt. Quantum Electron.*, vol. 44, no. 3–5, pp. 195–203, Jun. 2012, doi: 10.1007/s11082-011-9518-z.

[56] F. Bernardini and V. Fiorentini, "Spontaneous versus Piezoelectric Polarization in III-V Nitrides: Conceptual Aspects and Practical Consequences," *Phys. status solidi*, vol. 216, no. 1, pp. 391–398, Nov. 1999, doi: 10.1002/(SICI)1521-3951(199911)216:1<391::AID-PSSB391>3.0.CO;2-K.

[57] O. Ambacher *et al.*, "Two dimensional electron gases induced by spontaneous and piezoelectric polarization in undoped and doped AlGaN/GaN heterostructures," *J. Appl. Phys.*, vol. 87, no. 1, pp. 334–344, 2000, doi: 10.1063/1.371866.

[58] S. M. Sze and K. K. Ng, *Physics of Semiconductor Devices*. Cham: Springer International Publishing, 2014. doi: 10.1007/978-3-319-03002-9.

[59] M. Azize and T. Palacios, "Effect of substrate-induced strain in the transport properties of AlGaN/GaN heterostructures," *J. Appl. Phys.*, vol. 108, no. 2, p. 023707, Jul. 2010, doi: 10.1063/1.3463150.

[60] C. Wood, *Polarization Effects in Semiconductors*. ab initio theory to device applications. Springer Science & Business Media; 2007., 2007.

[61] O. Ambacher, "Growth and applications of Group III-nitrides," *J. Phys. D. Appl. Phys.*, vol. 31, no. 20, pp. 2653–2710, Oct. 1998, doi: 10.1088/0022-3727/31/20/001.

[62] W. A. Melton and J. I. Pankove, "GaN growth on sapphire," *J. Cryst. Growth*, vol. 178, no. 1–2, pp. 168–173, Jun. 1997, doi: 10.1016/S0022-0248(97)00082-1.

[63] R. S. Pengelly, S. M. Wood, J. W. Milligan, S. T. Sheppard, and W. L. Pribble, "A Review of GaN on SiC High Electron-Mobility Power Transistors and MMICs," vol. 60, no. 6, pp. 1764–1783, 2012.

[64] T. J. Anderson *et al.*, "Effect of Reduced Extended Defect Density in MOCVD Grown AlGaN/GaN HEMTs on Native GaN Substrates," *IEEE Electron Device Lett.*, vol. 37, no. 1, pp. 28–30, 2016, doi: 10.1109/LED.2015.2502221.

[65] Q. Wu *et al.*, "Performance Comparison of GaN HEMTs on Diamond and SiC Substrates Based on Surface Potential Model," *ECS J. Solid State Sci. Technol.*, vol. 6, no. 12, pp. Q171–Q178, Dec. 2017, doi: 10.1149/2.0441712jss.

[66] G. Jessen *et al.*, "AlGaN/GaN HEMT on Diamond Technology Demonstration," in *2006 IEEE Compound Semiconductor Integrated Circuit Symposium*, Nov. 2006, pp. 271–274. doi: 10.1109/CSICS.2006.319952.

[67] C. Ren, H. Shen, Z. Li, T. Chen, B. Zhang, and T. Gao, "GaN HEMT with AlGaN back barrier for high power MMIC switch application," *J. Semicond.*, vol. 36, no. 1, p. 014008, Jan. 2015, doi: 10.1088/1674-4926/36/1/014008.

[68] P. Gamarra, C. Lacam, M. Tordjman, J. Splettstösser, B. Schauwecker, and M.-A. di Forte-Poisson, “Optimisation of a carbon doped buffer layer for AlGaN/GaN HEMT devices,” *J. Cryst. Growth*, vol. 414, pp. 232–236, Mar. 2015, doi: 10.1016/j.jcrysgro.2014.10.025.

[69] Y. C. Choi, L. F. Eastman, and M. Pophristic, “Effects of an Fe-doped GaN Buffer in AlGaN/GaN Power HEMTs on Si Substrate,” in *2006 European Solid-State Device Research Conference*, Sep. 2006, vol. 53, no. 12, pp. 282–285. doi: 10.1109/ESSDER.2006.307693.

[70] T.-S. Ko, D.-Y. Lin, C.-F. Lin, C.-W. Chang, J.-C. Zhang, and S.-J. Tu, “High-temperature carrier density and mobility enhancements in AlGaN/GaN HEMT using AlN spacer layer,” *J. Cryst. Growth*, vol. 464, no. December 2016, pp. 175–179, Apr. 2017, doi: 10.1016/j.jcrysgro.2016.12.023.

[71] J.-S. Moon *et al.*, “360 GHz f MAX Graded-Channel AlGaN/GaN HEMTs for mmW Low-Noise Applications,” *IEEE Electron Device Lett.*, vol. 41, no. 8, pp. 1173–1176, Aug. 2020, doi: 10.1109/LED.2020.3005337.

[72] A. Hickman *et al.*, “First RF Power Operation of AlN/GaN/AlN HEMTs With >3 A/mm and 3 W/mm at 10 GHz,” *IEEE J. Electron Devices Soc.*, vol. 9, no. October 2020, pp. 121–124, 2021, doi: 10.1109/JEDS.2020.3042050.

[73] B.-J. Godejohann *et al.*, “AlN/GaN HEMTs grown by MBE and MOCVD: Impact of Al distribution,” *Phys. status solidi*, vol. 254, no. 8, p. 1600715, Aug. 2017, doi: 10.1002/pssb.201600715.

[74] S. Heikman, S. Keller, Y. Wu, J. S. Speck, S. P. DenBaars, and U. K. Mishra, “Polarization effects in AlGaN/GaN and GaN/AlGaN/GaN heterostructures,” *J. Appl. Phys.*, vol. 93, no. 12, pp. 10114–10118, Jun. 2003, doi: 10.1063/1.1577222.

[75] M. E. Lin, Z. Ma, F. Y. Huang, Z. F. Fan, L. H. Allen, and H. Morkoç, “Low resistance ohmic contacts on wide band-gap GaN,” *Appl. Phys. Lett.*, vol. 64, no. 8, pp. 1003–1005, Feb. 1994, doi: 10.1063/1.111961.

[76] Z. Han *et al.*, “Investigating the Failure Mechanism of p-GaN Gate HEMTs under High Power Stress with a Transparent ITO Gate,” *Micromachines*, vol. 14, no. 5, p. 940, Apr. 2023, doi: 10.3390/mi14050940.

[77] M. Meneghini, G. Meneghesso, and E. Znoni, *Power GaN Devices*. Cham: Springer International Publishing, 2017. doi: 10.1007/978-3-319-43199-4.

[78] Y. Zhao *et al.*, “Effects of recess depths on performance of AlGaN/GaN power MIS-HEMTs on the Si substrates and threshold voltage model of different recess depths for the using HfO2 gate insulator,” *Solid. State. Electron.*, vol. 163, no. 2, p. 107649, Jan. 2020, doi: 10.1016/j.sse.2019.107649.

[79] N. Sun *et al.*, “Improving Gate Reliability of 6-In E-Mode GaN-Based MIS-HEMTs by Employing Mixed Oxygen and Fluorine Plasma Treatment,” *IEEE Trans. Electron Devices*, vol. 69, no. 1, pp. 82–87, Jan. 2022, doi: 10.1109/TED.2021.3131118.

[80] G. Gonzalez, *Microwave Transistor Amplifier Design*. New Jersey: Prentice-Hall, Inc., 1997.

[81] G. Crupi *et al.*, “Accurate Multibias Equivalent-Circuit Extraction for GaN HEMTs,” *IEEE Trans. Microw. Theory Tech.*, vol. 54, no. 10, pp. 3616–3622, Oct. 2006, doi: 10.1109/TMTT.2006.882403.

[82] Z. Zhao *et al.*, “A fast small signal modeling method for GaN HEMTs,” *Solid State Electron.*, vol. 175, no. December 2020, p. 107946, 2021, doi: 10.1016/j.sse.2020.107946.

[83] J. Kim, “A New GaN HEMT Small-Signal Model Considering Source via Effects for 5G Millimeter-Wave Power Amplifier Design,” *Appl. Sci.*, vol. 11, no. 19, p. 9120, Sep. 2021, doi: 10.3390/app11199120.

[84] M. Gassoumi, A. Helali, M. Gassoumi, C. Gaquiere, and H. Maaref, “High Frequency Analysis and Small-Signal Modeling of AlGaN/GaN HEMTs with SiO2/SiN Passivation,” *Silicon*, vol. 11, no. 1, pp. 557–562, Feb. 2019, doi: 10.1007/s12633-018-9767-6.

[85] M. Teng, H. Yue, C. Chi, and M. Xiaohua, “A new small-signal model for asymmetrical AlGaN/GaN HEMTs,” *J. Semicond.*, vol. 31, no. 6, p. 064002, Jun. 2010, doi: 10.1088/1674-4926/31/6/064002.

[86] L. He, B. Zhao, K. Ma, C. He, Z. Xie, and X. Long, “Design of 30 nm multi-finger gate GaN HEMT for high

frequency device," *Int. J. Electron.*, vol. 00, no. 00, pp. 1–15, 2023, doi: 10.1080/00207217.2023.2173810.

[87] S. Nakamura, Y. Harada, and M. Seno, "Novel metalorganic chemical vapor deposition system for GaN growth," *Appl. Phys. Lett.*, vol. 58, no. 18, pp. 2021–2023, May 1991, doi: 10.1063/1.105239.

[88] A. Sagar, R. M. Feenstra, C. K. Inoki, T. S. Kuan, and D. D. Koleske, "Combined MOCVD and MBE growth of GaN on porous SiC," *MRS Proc.*, vol. 798, no. 8, p. Y9.6, Feb. 2003, doi: 10.1557/PROC-798-Y9.6.

[89] T. D. Moustakas, T. Lei, and R. J. Molnar, "Growth of GaN by ECR-assisted MBE," *Phys. B Condens. Matter*, vol. 185, no. 1–4, pp. 36–49, Apr. 1993, doi: 10.1016/0921-4526(93)90213-P.

[90] T. . Moustakas *et al.*, "Growth and device applications of III-nitrides by MBE," *J. Cryst. Growth*, vol. 227–228, pp. 13–20, Jul. 2001, doi: 10.1016/S0022-0248(01)00625-X.

[91] H. Tokunaga, H. Tan, Y. Inaishi, T. Arai, A. Yamaguchi, and J. Hidaka, "Performance of multiwafer reactor GaN MOCVD system," *J. Cryst. Growth*, vol. 221, no. 1–4, pp. 616–621, Dec. 2000, doi: 10.1016/S0022-0248(00)00788-0.

[92] S. J. Heikman, "MOCVD Growth Technologies for Applications in AlGaN/GaN High Electron Mobility Transistors," no. September, 2002.

[93] A. Kakanakova-Georgieva, U. Forsberg, I. G. Ivanov, and E. Janzén, "Uniform hot-wall MOCVD epitaxial growth of 2inch AlGaN/GaN HEMT structures," *J. Cryst. Growth*, vol. 300, no. 1, pp. 100–103, Mar. 2007, doi: 10.1016/j.jcrysgro.2006.10.242.

[94] A. Thamm, O. Brandt, J. Hilsenbeck, R. Lossy, and K. H. Ploog, "Fabrication of device-related GaN/(Al,Ga)N heterostructures on SiC(0001) by reactive MBE," in *2000 IEEE International Symposium on Compound Semiconductors. Proceedings of the IEEE Twenty-Seventh International Symposium on Compound Semiconductors (Cat. No.00TH8498)*, pp. 455–460. doi: 10.1109/ISCS.2000.947198.

[95] N. G. Weimann *et al.*, "AlGaN/GaN HEMTs grown by molecular beam epitaxy on sapphire, SiC, and HVPE GaN templates," in *Proceedings. IEEE Lester Eastman Conference on High Performance Devices*, 2003, vol. 174, pp. 126–133. doi: 10.1109/LECHPD.2002.1146740.

[96] R. Held, D. E. Crawford, A. M. Johnston, A. M. Dabiran, and P. I. Cohen, "In situ control of gan growth by molecular beam epitaxy," *J. Electron. Mater.*, vol. 26, no. 3, pp. 272–280, Mar. 1997, doi: 10.1007/s11664-997-0163-z.

[97] F. Baiutti, G. Christiani, and G. Logvenov, "Towards precise defect control in layered oxide structures by using oxide molecular beam epitaxy," *Beilstein J. Nanotechnol.*, vol. 5, no. 1, pp. 596–602, May 2014, doi: 10.3762/bjnano.5.70.

[98] "BEAMER - GenISys GmbH." doi: 'LAB - GenISys GmbH'. https://www.genisys-gmbh.com/lab.html (accessed Oct. 24, 2022).

[99] D. Zhuang and J. H. Edgar, "Wet etching of GaN, AlN, and SiC: A review," *Mater. Sci. Eng. R Reports*, vol. 48, no. 1, pp. 1–46, 2005, doi: 10.1016/j.mser.2004.11.002.

[100] T. Sreenidhi, K. Baskar, A. DasGupta, and N. DasGupta, "Reactive ion etching of GaN in SF 6 + Ar and SF 6 + N 2 plasma," *Semicond. Sci. Technol.*, vol. 23, no. 12, p. 125019, Dec. 2008, doi: 10.1088/0268-1242/23/12/125019.

[101] K. Remashan, S. J. Chua, A. Ramam, S. Prakash, and W. Liu, "Inductively coupled plasma etching of GaN using BCl 3 /Cl 2 chemistry and photoluminescence studies of the etched samples," *Semicond. Sci. Technol.*, vol. 15, no. 4, pp. 386–389, Apr. 2000, doi: 10.1088/0268-1242/15/4/313.

[102] L. Jiang, N. O. V Plank, M. A. Blauw, R. Cheung, and E. van der Drift, "Dry etching of SiC in inductively coupled Cl 2 /Ar plasma," *J. Phys. D. Appl. Phys.*, vol. 37, no. 13, pp. 1809–1814, Jul. 2004, doi: 10.1088/0022-3727/37/13/012.

[103] M. Hua *et al.*, "GaN-Based Metal-Insulator-Semiconductor High-Electron-Mobility Transistors Using Low-Pressure Chemical Vapor Deposition SiN<italic>x</italic> as Gate Dielectric," *IEEE Electron Device Lett.*, vol. 36,

no. 5, pp. 448–450, May 2015, doi: 10.1109/LED.2015.2409878.

[104] V. K. Surana, S. Ganguly, and D. Saha, “Performance Improvement in AlGaN/GaN High-Electron-Mobility Transistors by Low-Temperature Inductively Coupled Plasma–Chemical Vapor Deposited SiN x as Gate Dielectric and Surface Passivation,” *Phys. status solidi*, vol. 219, no. 24, p. 2200509, Dec. 2022, doi: 10.1002/pssa.202200509.

[105] K. Karami, A. Dhongde, H. Cheng, P. M. Reynolds, S. Thoms, and E. Aditya, Bojja A., Ritter, D., Li, C. and Wasige, “Robust sub-100 nm T-gate fabrication process using multi-step development,” vol. 63, no. 10, pp. 3–4, 2016, doi: MNE EUROSENSORS 2022, Leuven, Belgium, 19-23 September 2022.

[106] N. Unal, D. Mahalu, O. Raslin, D. Ritter, C. Sambale, and U. Hofmann, “Third dimension of proximity effect correction (PEC),” *Microelectron. Eng.*, vol. 87, no. 5–8, pp. 940–942, May 2010, doi: 10.1016/j.mee.2009.12.002.

[107] H. Cheng, A. Dhongde, K. Karami, P. Reynolds, and S. Thoms, “Reliable T-gate Process for THz HEMTs,” *UK Semicond. 2022, Sheffield, UK*, no. July, pp. 6–7, 2022, doi: https://eprints.gla.ac.uk/274600/.

[108] G. Greco, F. Iucolano, and F. Roccaforte, “Ohmic contacts to Gallium Nitride materials,” *Appl. Surf. Sci.*, vol. 383, pp. 324–345, Oct. 2016, doi: 10.1016/j.apsusc.2016.04.016.

[109] “RELIABILITY CHARACTERISATION OF III-NITRIDES BASED DEVICES FOR TECHNOLOGY DEVELOPMENT,” no. December, 2018.

[110] S. Chakraborty and T.-W. Kim, “Comprehensive Schottky Barrier Height Behavior and Reliability Instability with Ni/Au and Pt/Ti/Pt/Au on AlGaN/GaN High-Electron-Mobility Transistors,” *Micromachines*, vol. 13, no. 1, p. 84, Jan. 2022, doi: 10.3390/mi13010084.

[111] M. Meer, A. Rawat, K. Takhar, S. Ganguly, and D. Saha, “Interface dynamics in ohmic contact optimization on AlGaN/GaN heterostructure by the formation of TiN,” *Microelectron. Eng.*, vol. 219, no. October 2019, p. 111144, Jan. 2020, doi: 10.1016/j.mee.2019.111144.

[112] A. Soltani *et al.*, “Development and analysis of low resistance ohmic contact to n-AlGaN/GaN HEMT,” *Diam. Relat. Mater.*, vol. 16, no. 2, pp. 262–266, Feb. 2007, doi: 10.1016/j.diamond.2006.06.022.

[113] N. Chaturvedi, U. Zeimer, J. Würfl, and G. Tränkle, “Mechanism of ohmic contact formation in AlGaN/GaN high electron mobility transistors,” *Semicond. Sci. Technol.*, vol. 21, no. 2, pp. 175–179, Feb. 2006, doi: 10.1088/0268-1242/21/2/014.

[114] A. Vertiatchikh, E. Kaminsky, J. Teetsov, and K. Robinson, “Structural properties of alloyed Ti/Al/Ti/Au and Ti/Al/Mo/Au ohmic contacts to AlGaN/GaN,” *Solid. State. Electron.*, vol. 50, no. 7–8, pp. 1425–1429, Jul. 2006, doi: 10.1016/j.sse.2006.07.003.

[115] Q. Z. Liu *et al.*, “Study of contact formation in AlGaN/GaN heterostructures,” *Appl. Phys. Lett.*, vol. 71, no. 12, pp. 1658–1660, Sep. 1997, doi: 10.1063/1.119786.

[116] G. K. Reeves and H. B. Harrison, “Obtaining the specific contact resistance from transmission line model measurements,” *IEEE Electron Device Lett.*, vol. 3, no. 5, pp. 111–113, May 1982, doi: 10.1109/EDL.1982.25502.

[117] A. Al-Khalidi, “Advanced Gallium Nitride Technology for Microwave Power Amplifiers,” 2015.

[118] A. Holland, Y. Pan, M. Alnassar, and S. Luong, “Circular test structures for determining the specific contact resistance of ohmic contacts,” *Facta Univ. - Ser. Electron. Energ.*, vol. 30, no. 3, pp. 313–326, 2017, doi: 10.2298/FUEE1703313H.

[119] B. Van Daele, G. Van Tendeloo, W. Ruythooren, J. Derluyn, M. R. Leys, and M. Germain, “The role of Al on Ohmic contact formation on n-type GaN and AlGaN⁄GaN,” *Appl. Phys. Lett.*, vol. 87, no. 6, p. 061905, Aug. 2005, doi: 10.1063/1.2008361.

[120] M. Y. A. Crespo, R. Fitch, J. Gillespie, N. Moser, G. Via, “Ti/Al/Ni/Au Ohmic Contacts on AlGaN/GaN HEMTs,” *Int. Conf. Compd. Semicond. Manuf. Technol.* , vol. Technical, 2003, Accessed: Apr. 04, 2019. [Online]. Available: https://csmantech.org/OldSite/Digests/2003/2003PDF/13-1.pdf

[121] T. Yoshida and T. Egawa, “Role of thin Ti layer in formation mechanism of low temperature-annealed Ti/Al-based ohmic contact on AlGaN/GaN heterostructure,” *Semicond. Sci. Technol.*, vol. 33, no. 7, p. 075006, Jul. 2018, doi: 10.1088/1361-6641/aac3c3.

[122] M. Vasilevska, “Thermally Efficient GaN HEMTs for High Performance Microwave Power Amplifiers,” no. May, 2017.

[123] Y. K. Yadav, B. B. Upadhyay, M. Meer, N. Bhardwaj, S. Ganguly, and D. Saha, “Ti/Au/Al/Ni/Au low contact resistance and sharp edge acuity for highly scalable AlGaN/GaN HEMTs,” *IEEE Electron Device Lett.*, vol. 40, no. 1, pp. 1–1, 2018, doi: 10.1109/LED.2018.2884155.

[124] H. Yazdani, S. Chevtchenko, F. Brunner, G. Tränkle, and J. Würfl, “Au-Free Ohmic Contact for GaN High-Electron-Mobility Transistors,” *Phys. status solidi*, vol. 219, no. 8, p. 2100802, Apr. 2022, doi: 10.1002/pssa.202100802.

[125] Y. Yue *et al.*, “InAlN/AlN/GaN HEMTs With Regrown Ohmic Contacts and f T of 370 GHz,” *IEEE ELECTRON DEVICE Lett.*, vol. 33, no. 7, 2012, doi: 10.1109/LED.2012.2196751.

[126] Y. Lu *et al.*, “High RF Performance AlGaN/GaN HEMT Fabricated by Recess-Arrayed Ohmic Contact Technology,” *IEEE Electron Device Lett.*, vol. 39, no. 6, pp. 811–814, Jun. 2018, doi: 10.1109/LED.2018.2828860.

[127] T. Huang, C. Liu, J. Bergsten, H. Jiang, K. M. Lau, and N. Rorsman, “Fabrication and improved performance of AlGaN/GaN HEMTs with regrown ohmic contacts and passivation-first process,” in *2016 Compound Semiconductor Week (CSW) [Includes 28th International Conference on Indium Phosphide & Related Materials (IPRM) & 43rd International Symposium on Compound Semiconductors (ISCS)*, Jun. 2016, vol. 60, pp. 1–2. doi: 10.1109/ICIPRM.2016.7528722.

[128] S. Ganguly *et al.*, “AlGaN/GaN HEMTs on Si by MBE with regrown contacts and fT = 153 GHz,” *Phys. Status Solidi Curr. Top. Solid State Phys.*, vol. 11, no. 3–4, pp. 887–889, Feb. 2014, doi: 10.1002/pssc.201300668.

[129] E. V Erofeev, I. V Fedin, V. V Fedina, and A. P. Fazleev, “Low-Temperature Ta/Al-Based Ohmic Contacts to AlGaN/GaN Heteroepitaxial Structures on Silicon Wafers,” *Semiconductors*, vol. 53, no. 2, pp. 237–240, Feb. 2019, doi: 10.1134/S1063782619020064.

[130] M. A. Awaah, I. Awaah, O. Akpa, U. Obahiagbon, and K. Aganah, “Analysis of the ‘Sheet’ Charge Concentration at the AlGaN/GaN Interface,” in *2018 IEEE PES/IAS PowerAfrica*, Jun. 2018, pp. 67–72. doi: 10.1109/PowerAfrica.2018.8521113.

[131] M. Hou, G. Xie, and K. Sheng, “Improved Device Performance in AlGaN/GaN HEMT by Forming Ohmic Contact With Laser Annealing,” *IEEE Electron Device Lett.*, vol. 39, no. 8, pp. 1137–1140, Aug. 2018, doi: 10.1109/LED.2018.2844951.

[132] Zhuo Liu *et al.*, “Mechanism of ohmic contact formation in AlGaN/GaN high electron mobility transistors using microwave annealing,” in *2016 13th IEEE International Conference on Solid-State and Integrated Circuit Technology (ICSICT)*, Oct. 2016, pp. 1050–1052. doi: 10.1109/ICSICT.2016.7998647.

[133] Z. Liu, D. Chen, L. Wan, and G. Li, “Micron-Scale Annealing for Ohmic Contact Formation Applied in GaN HEMT Gate-First Technology,” *IEEE Electron Device Lett.*, vol. 39, no. 12, pp. 1896–1899, Dec. 2018, doi: 10.1109/LED.2018.2877717.

[134] S. J. Duffy *et al.*, “Strain-Reduction Induced Rise in Channel Temperature at Ohmic Contacts of GaN HEMTs,” *IEEE Access*, vol. 6, pp. 42721–42728, 2018, doi: 10.1109/ACCESS.2018.2861323.

[135] J. Zhang *et al.*, “Ultralow-Contact-Resistance Au-Free Ohmic Contacts With Low Annealing Temperature on AlGaN/GaN Heterostructures,” *IEEE Electron Device Lett.*, vol. 39, no. 6, pp. 847–850, Jun. 2018, doi: 10.1109/LED.2018.2822659.

[136] W. Li *et al.*, “Au-based and Au-free ohmic contacts to AlGaN/GaN structures on silicon or Sapphire substrates,” in *2018 18th International Workshop on Junction Technology (IWJT)*, Mar. 2018, vol. 2018-Janua, pp. 1–4. doi: 10.1109/IWJT.2018.8330288.

[137] Bo Song *et al.*, "Ultralow-Leakage AlGaN/GaN High Electron Mobility Transistors on Si With Non-Alloyed Regrown Ohmic Contacts," *IEEE Electron Device Lett.*, vol. 37, no. 1, pp. 16–19, Jan. 2016, doi: 10.1109/LED.2015.2497252.

[138] Y. Li *et al.*, "Low-Contact-Resistance Non-Gold Ta/Si/Ti/Al/Ni/Ta Ohmic Contacts on Undoped AlGaN/GaN High-Electron-Mobility Transistors Grown on Silicon," *Appl. Phys. Express*, vol. 6, no. 11, p. 116501, Nov. 2013, doi: 10.7567/APEX.6.116501.

[139] X. Li, S. Gao, Q. Zhou, X. Liu, W. Hu, and H. Wang, "Fabrication and Performance of Ti/Al/Ni/TiN Au-Free Ohmic Contacts for Undoped AlGaN/GaN HEMT," *IEEE Trans. Electron Devices*, vol. 67, no. 5, pp. 1959–1964, May 2020, doi: 10.1109/TED.2020.2982665.

[140] S. Niranjan, A. Rao, R. Muralidharan, P. Sen, and D. N. Nath, "Performance Comparison of Au-Based and Au-Free AlGaN/GaN HEMT on Silicon," *IEEE Trans. Electron Devices*, vol. 69, no. 3, pp. 1014–1019, Mar. 2022, doi: 10.1109/TED.2021.3140193.

[141] H. Du *et al.*, "Low ohmic contact resistivity realized by in situ SiN x insertion for high Al-composition-AlGaN/GaN heterostructure," *Appl. Phys. Lett.*, vol. 121, no. 17, p. 172102, Oct. 2022, doi: 10.1063/5.0100329.

[142] O. Odabasi *et al.*, "Impact of the Low Temperature Ohmic Contact Process on DC and Forward Gate Bias Stress Operation of GaN HEMT Devices," *IEEE Electron Device Lett.*, vol. 43, no. 10, pp. 1609–1612, Oct. 2022, doi: 10.1109/LED.2022.3199569.

[143] N. Okamoto, K. Imanishi, T. Kikkawa, and N. Nara, "Influence of Negative Charging on High Rate SiC Etching for GaN HEMT MMICs," *Mater. Sci. Forum*, vol. 645–648, pp. 791–794, Apr. 2010, doi: 10.4028/www.scientific.net/MSF.645-648.791.

[144] Y. Takei *et al.*, "Reduction of contact resistance on AlGaN/GaN HEMT structures introducing uneven AlGaN layers," *Phys. status solidi*, vol. 212, no. 5, pp. 1104–1109, May 2015, doi: 10.1002/pssa.201431645.

[145] O. Axelsson *et al.*, "Application Relevant Evaluation of Trapping Effects in AlGaN/GaN HEMTs With Fe-Doped Buffer," *IEEE Trans. Electron Devices*, vol. 63, no. 1, pp. 326–332, Jan. 2016, doi: 10.1109/TED.2015.2499313.

[146] S. Kato, Y. Satoh, H. Sasaki, I. Masayuki, and S. Yoshida, "C-doped GaN buffer layers with high breakdown voltages for high-power operation AlGaN/GaN HFETs on 4-in Si substrates by MOVPE," *J. Cryst. Growth*, vol. 298, no. SPEC. ISS, pp. 831–834, Jan. 2007, doi: 10.1016/j.jcrysgro.2006.10.192.

[147] T. V. Malin *et al.*, "Undoped High-Resistance GaN Buffer Layer for AlGaN/GaN High-Electron-Mobility Transistors," *Tech. Phys. Lett.*, vol. 45, no. 8, pp. 761–764, Aug. 2019, doi: 10.1134/S1063785019080108.

[148] W. Götz, N. M. Johnson, C. Chen, H. Liu, C. Kuo, and W. Imler, "Activation energies of Si donors in GaN," *Appl. Phys. Lett.*, vol. 68, no. 22, pp. 3144–3146, 1996, doi: 10.1063/1.115805.

[149] J. Cho, E. Bozorg-Grayeli, D. H. Altman, M. Asheghi, and K. E. Goodson, "Low Thermal Resistances at GaN–SiC Interfaces for HEMT Technology," *IEEE Electron Device Lett.*, vol. 33, no. 3, pp. 378–380, Mar. 2012, doi: 10.1109/LED.2011.2181481.

[150] Z.-Q. Fang, B. Claflin, D. C. Look, D. S. Green, and R. Vetury, "Deep traps in AlGaN/GaN heterostructures studied by deep level transient spectroscopy: Effect of carbon concentration in GaN buffer layers," *J. Appl. Phys.*, vol. 108, no. 6, p. 063706, Sep. 2010, doi: 10.1063/1.3488610.

[151] P. Moens *et al.*, "Impact of buffer leakage on intrinsic reliability of 650V AlGaN/GaN HEMTs," in *2015 IEEE International Electron Devices Meeting (IEDM)*, Dec. 2015, vol. 2016-Febru, pp. 35.2.1-35.2.4. doi: 10.1109/IEDM.2015.7409831.

[152] S. C. Binari *et al.*, "Trapping effects and microwave power performance in AlGaN/GaN HEMTs," *IEEE Trans. Electron Devices*, vol. 48, no. 3, pp. 465–471, Mar. 2001, doi: 10.1109/16.906437.

[153] D.-Y. Chen *et al.*, "Impact of the Channel Thickness on Electron Confinement in MOCVD-Grown High

Breakdown Buffer-Free AlGaN/GaN Heterostructures," *Phys. status solidi*, Nov. 2022, doi: 10.1002/pssa.202200496.

[154] A. Gowrisankar *et al.*, "Compensation Dopant-Free GaN-on-Si HEMTs With a Polarization Engineered Buffer for RF Applications," *IEEE Trans. Electron Devices*, vol. 70, no. 4, pp. 1622–1627, Apr. 2023, doi: 10.1109/TED.2023.3244514.

[155] K. Harrouche, S. Venkatachalam, L. Ben-Hammou, F. Grandpierron, E. Okada, and F. Medjdoub, "Low Trapping Effects and High Electron Confinement in Short AlN/GaN-On-SiC HEMTs by Means of a Thin AlGaN Back Barrier," *Micromachines*, vol. 14, no. 2, p. 291, Jan. 2023, doi: 10.3390/mi14020291.

[156] D.-Y. Chen *et al.*, "Microwave Performance of 'Buffer-Free' GaN-on-SiC High Electron Mobility Transistors," *IEEE Electron Device Lett.*, vol. 41, no. 6, pp. 828–831, Jun. 2020, doi: 10.1109/LED.2020.2988074.

[157] M. Sakai, T. Egawa, M. Hao, and H. Ishikawa, "Effect of Various Interlayers on Epiwafer Bowing in AlGaN/GaN High-Electron-Mobility Transistor Structures," *Jpn. J. Appl. Phys.*, vol. 43, no. 12, pp. 8019–8023, Dec. 2004, doi: 10.1143/JJAP.43.8019.

[158] K. Narang *et al.*, "Suitability of thin-GaN for AlGaN/GaN HEMT material and device," *J. Mater. Sci.*, vol. 57, no. 10, pp. 5913–5923, Mar. 2022, doi: 10.1007/s10853-022-07017-x.

[159] and F. M. R. Pecheux, R. Kabouche, M. Zegaoui, J. T. Chen, O. Kordina, "GaN-based transistors using buffer-free heterostructures for next generation RF devices," *9th Wide Band Gap Semicond. Components Work.*, no. October, pp. 3–6, 2018, [Online]. Available: https://hal.science/hal-02356908/document

[160] J. Raychaudhuri *et al.*, "Study of 'Thin Buffer' GaN on SiC HEMT and Effect of Bulk Traps on it," *Silicon*, vol. 14, no. 18, pp. 12505–12512, Dec. 2022, doi: 10.1007/s12633-022-01951-w.

[161] J. Raychaudhuri, J. Mukherjee, S. Kumar, R. Bag, M. Mishra, and S. Ghosh, "Effect of different layer structures on the RF performance of GaN HEMT devices," *Semicond. Sci. Technol.*, vol. 36, no. 10, p. 105005, Oct. 2021, doi: 10.1088/1361-6641/ac1054.

[162] J. Lu *et al.*, "Transmorphic epitaxial growth of AlN nucleation layers on SiC substrates for high-breakdown thin GaN transistors," *Appl. Phys. Lett.*, vol. 115, no. 22, 2019, doi: 10.1063/1.5123374.

[163] A. Dhongde *et al.*, "High performance of AlGaN/GaN HEMTs using buffer-free GaN on SiC structure," 2022. doi: 45th WOCSDICE - Workshop on Compound Semiconductor Devices and Integrated Circuits, Ponta Delgada (São Miguel island – Azores), Portugal, 3-6 May 2022.

[164] A. Dhongde *et al.*, "The Role of Selective Pattern Etching to Improve the Ohmic Contact Resistance and Device Performance of AlGaN / GaN HEMTs," *Int. J. Nanoelectron. Mater.*, vol. 14, no. December, pp. 21–28, 2021, doi: International Journal of Nanoelectronics and Materials.

[165] J. Jorudas *et al.*, "AlGaN/GaN on SiC Devices without a GaN Buffer Layer: Electrical and Noise Characteristics," *Micromachines*, vol. 11, no. 12, p. 1131, Dec. 2020, doi: 10.3390/mi11121131.

[166] R. Khanna, W. Stanchina, and G. Reed, "Effects of parasitic capacitances on gallium nitride heterostructure power transistors," in *2012 IEEE Energy Conversion Congress and Exposition (ECCE)*, Sep. 2012, pp. 1489–1495. doi: 10.1109/ECCE.2012.6342638.

[167] B. Song *et al.*, "Effect of Fringing Capacitances on the RF Performance of GaN HEMTs With T-Gates," *IEEE Trans. Electron Devices*, vol. 61, no. 3, pp. 747–754, Mar. 2014, doi: 10.1109/TED.2014.2299810.

[168] S. Choi, E. R. Heller, D. Dorsey, R. Vetury, and S. Graham, "The Impact of Bias Conditions on Self-Heating in AlGaN/GaN HEMTs," *IEEE Trans. Electron Devices*, vol. 60, no. 1, pp. 159–162, Jan. 2013, doi: 10.1109/TED.2012.2224115.

[169] A. Manoi, J. W. Pomeroy, N. Killat, and M. Kuball, "Benchmarking of Thermal Boundary Resistance in AlGaN/GaN HEMTs on SiC Substrates: Implications of the Nucleation Layer Microstructure," *IEEE Electron Device Lett.*, vol. 31, no. 12, pp. 1395–1397, Dec. 2010, doi: 10.1109/LED.2010.2077730.

[170] L. Pan, X. Dong, Z. Li, W. Luo, and J. Ni, “Influence of the AlN nucleation layer on the properties of AlGaN/GaN heterostructure on Si (1 1 1) substrates,” *Appl. Surf. Sci.*, vol. 447, pp. 512–517, Jul. 2018, doi: 10.1016/j.apsusc.2018.04.001.

[171] K. Ranjan, S. Arulkumaran, G. I. Ng, and A. Sandupatla, “Investigation of Self-Heating Effect on DC and RF Performances in AlGaN/GaN HEMTs on CVD-Diamond,” *IEEE J. Electron Devices Soc.*, vol. 7, no. October, pp. 1264–1269, 2019, doi: 10.1109/JEDS.2019.2947564.

[172] J.-T. Chen *et al.*, “A GaN–SiC hybrid material for high-frequency and power electronics,” *Appl. Phys. Lett.*, vol. 113, no. 4, p. 041605, Jul. 2018, doi: 10.1063/1.5042049.

[173] C. Mion, J. F. Muth, E. A. Preble, and D. Hanser, “Thermal conductivity, dislocation density and GaN device design,” *Superlattices Microstruct.*, vol. 40, no. 4–6, pp. 338–342, Oct. 2006, doi: 10.1016/j.spmi.2006.07.017.

[174] S. R. Choi, D. Kim, S.-H. Choa, S.-H. Lee, and J.-K. Kim, “Thermal Conductivity of AlN and SiC Thin Films,” *Int. J. Thermophys.*, vol. 27, no. 3, pp. 896–905, May 2006, doi: 10.1007/s10765-006-0062-1.

[175] K. Park and C. Bayram, “Thermal resistance optimization of GaN/substrate stacks considering thermal boundary resistance and temperature-dependent thermal conductivity,” *Appl. Phys. Lett.*, vol. 109, no. 15, p. 151904, Oct. 2016, doi: 10.1063/1.4964711.

[176] Y. Zhang, K. H. Teo, and T. Palacios, “Beyond Thermal Management: Incorporating p-Diamond Back-Barriers and Cap Layers Into AlGaN/GaN HEMTs,” *IEEE Trans. Electron Devices*, vol. 63, no. 6, pp. 2340–2345, Jun. 2016, doi: 10.1109/TED.2016.2553136.

[177] A. F. Al-Neama, N. Kapur, J. Summers, and H. M. Thompson, “Thermal management of GaN HEMT devices using serpentine minichannel heat sinks,” *Appl. Therm. Eng.*, vol. 140, no. November 2017, pp. 622–636, Jul. 2018, doi: 10.1016/j.applthermaleng.2018.05.072.

[178] W. Tang, J. Li, J. Lu, K. Sheng, Z. Wu, and X. Li, “Thermal management of GaN HEMT devices using subcooled flow boiling in an embedded manifold microchannel heat sink,” *Appl. Therm. Eng.*, vol. 225, no. September 2022, p. 120174, May 2023, doi: 10.1016/j.applthermaleng.2023.120174.

[179] D. Francis and M. Kuball, “GaN-on-diamond materials and device technology: A review,” in *Thermal Management of Gallium Nitride Electronics*, Elsevier, 2022, pp. 295–331. doi: 10.1016/B978-0-12-821084-0.00006-8.

[180] Y. Won, J. Cho, D. Agonafer, M. Asheghi, and K. E. Goodson, “Cooling Limits for GaN HEMT Technology,” in *2013 IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS)*, Oct. 2013, pp. 1–5. doi: 10.1109/CSICS.2013.6659222.

[181] A. Jarndal, L. Arivazhagan, and D. Nirmal, “On the performance of GaN-on-Silicon, Silicon-Carbide, and Diamond substrates,” *Int. J. RF Microw. Comput. Eng.*, vol. 30, no. 6, pp. 1–10, Jun. 2020, doi: 10.1002/mmce.22196.

[182] N. Okamoto *et al.*, “Backside processing of RF GaN-on-GaN HEMTs considering thermal management,” *CS MANTECH 2019 - 2019 Int. Conf. Compd. Semicond. Manuf. Technol. Dig. Pap.*, 2019.

[183] M. Elksne, A. Al-Khalidi, and E. Wasige, “A Planar Distributed Channel AlGaN/GaN HEMT Technology,” *IEEE Trans. Electron Devices*, vol. 66, no. 5, pp. 2454–2458, May 2019, doi: 10.1109/TED.2019.2907152.

[184] J. Chen, J. Qin, X. Ma, and H. Wang, “Improved RF power performance of AlGaN/GaN HEMT on silicon with planar distributed channel,” *Solid. State. Electron.*, vol. 202, no. October 2022, p. 108619, 2023, doi: 10.1016/j.sse.2023.108619.

[185] A. M. Darwish, H. A. Hung, and A. A. Ibrahim, “AlGaN/GaN HEMT With Distributed Gate for Channel Temperature Reduction,” *IEEE Trans. Microw. Theory Tech.*, vol. 60, no. 4, pp. 1038–1043, Apr. 2012, doi: 10.1109/TMTT.2012.2185948.

[186] L. Arivazhagan, A. Jarndal, and D. Nirmal, “GaN HEMT on Si substrate with diamond heat spreader for high power applications,” *J. Comput. Electron.*, vol. 20, no. 2, pp. 873–882, Apr. 2021, doi:

10.1007/s10825-020-01646-8.

[187] R. Zhang, W. S. Zhao, W. Y. Yin, Z. G. Zhao, and H. J. Zhou, “Impacts of diamond heat spreader on the thermo-mechanical characteristics of high-power AlGaN/GaN HEMTs,” *Diam. Relat. Mater.*, vol. 52, pp. 25–31, Feb. 2015, doi: 10.1016/j.diamond.2014.12.001.

[188] S. K. Mohanty, Y.-Y. Chen, P.-H. Yeh, and R.-H. Horng, “Thermal Management of GaN-on-Si High Electron Mobility Transistor by Copper Filled Micro-Trench Structure.,” *Sci. Rep.*, vol. 9, no. 1, p. 19691, Dec. 2019, doi: 10.1038/s41598-019-56292-3.

[189] D. Marcon *et al.*, “Reliability Analysis of Permanent Degradations on AlGaN/GaN HEMTs,” *IEEE Trans. Electron Devices*, vol. 60, no. 10, pp. 3132–3141, Oct. 2013, doi: 10.1109/TED.2013.2273216.

[190] D. Marcon *et al.*, “Reliability of AlGaN/GaN HEMTs: Permanent leakage current increase and output current drop,” in *Proceedings of the 20th IEEE International Symposium on the Physical and Failure Analysis of Integrated Circuits (IPFA)*, Jul. 2013, pp. 249–254. doi: 10.1109/IPFA.2013.6599162.

[191] J. L. Lu, D. Chen, and L. Yushyna, “A high power-density and high efficiency insulated metal substrate based GaN HEMT power module,” in *2017 IEEE Energy Conversion Congress and Exposition (ECCE)*, Oct. 2017, vol. 2017-Janua, pp. 3654–3658. doi: 10.1109/ECCE.2017.8096647.

[192] B. Li, X. Yang, K. Wang, H. Zhu, L. Wang, and W. Chen, “A Compact Double-Sided Cooling 650V/30A GaN Power Module with Low Parasitic Parameters,” *IEEE Trans. Power Electron.*, vol. 37, no. 1, pp. 426–439, 2022, doi: 10.1109/TPEL.2021.3092367.

[193] Y. Tang *et al.*, “Ultrahigh-Speed GaN High-Electron-Mobility Transistors With fT/ fmax of 454/444 GHz,” *IEEE Electron Device Lett.*, vol. 36, no. 6, pp. 549–551, Jun. 2015, doi: 10.1109/LED.2015.2421311.

[194] J. W. Chung, Tae-Woo Kim, and T. Palacios, “Advanced gate technologies for state-of-the-art fT in AlGaN/GaN HEMTs,” in *2010 International Electron Devices Meeting*, Dec. 2010, pp. 30.2.1-30.2.4. doi: 10.1109/IEDM.2010.5703449.

[195] D. S. Lee *et al.*, “245-GHz InAlN/GaN HEMTs With Oxygen Plasma Treatment,” *IEEE Electron Device Lett.*, vol. 32, no. 6, pp. 755–757, Jun. 2011, doi: 10.1109/LED.2011.2132751.

[196] D. S. Lee, X. Gao, S. Guo, D. Kopp, P. Fay, and T. Palacios, “300-GHz InAlN/GaN HEMTs With InGaN Back Barrier,” *IEEE Electron Device Lett.*, vol. 32, no. 11, pp. 1525–1527, Nov. 2011, doi: 10.1109/LED.2011.2164613.

[197] Y. Yue *et al.*, “Ultrascaled InAlN / GaN High Electron Mobility Transistors with Cutoff Frequency of 400 GHz characteristics of the HEMTs were measured at both room,” *Japanese J. Appl. Phys.*, vol. 52, pp. 1–2, 2013.

[198] X.-C. Fu *et al.*, “High-frequency InAlN/GaN HFET with f max over 400 GHz,” *Electron. Lett.*, vol. 54, no. 12, pp. 783–785, Jun. 2018, doi: 10.1049/el.2018.0247.

[199] K. Shinohara *et al.*, “220GHz f<inf>T</inf> and 400GHz f<inf>max</inf> in 40-nm GaN DH-HEMTs with re-grown ohmic,” in *2010 International Electron Devices Meeting*, Dec. 2010, pp. 30.1.1-30.1.4. doi: 10.1109/IEDM.2010.5703448.

[200] Y.-K. Lin *et al.*, “High-Performance GaN MOSHEMTs Fabricated With ALD Al 2 O 3 Dielectric and NBE Gate Recess Technology for High Frequency Power Applications,” *IEEE Electron Device Lett.*, vol. 38, no. 6, pp. 771–774, Jun. 2017, doi: 10.1109/LED.2017.2696569.

[201] D. Marti, S. Tirelli, A. R. Alt, J. Roberts, and C. R. Bolognesi, “150-GHz Cutoff Frequencies and 2-W/mm Output Power at 40 GHz in a Millimeter-Wave AlGaN/GaN HEMT Technology on Silicon,” *IEEE Electron Device Lett.*, vol. 33, no. 10, pp. 1372–1374, Oct. 2012, doi: 10.1109/LED.2012.2204855.

[202] M. Mi *et al.*, “Improved f max and breakdown voltage in AlGaN/GaN HEMT with plasma treatment,” in *2018 1st Workshop on Wide Bandgap Power Devices and Applications in Asia (WiPDA Asia)*, May 2018, pp. 208–211. doi: 10.1109/WiPDAAsia.2018.8734554.

[203] M. Mi *et al.*, “In-situ SiN combined with etch-stop barrier structure for high-frequency AlGaN/GaN

HEMT," *Chinese Phys. B*, Feb. 2020, doi: 10.1088/1674-1056/ab7746.

[204] J. W. Chung, W. E. Hoke, E. M. Chumbes, and T. Palacios, "AlGaN/GaN HEMT With 300-GHz fmax," *IEEE Electron Device Lett.*, vol. 31, no. 3, pp. 195–197, Mar. 2010, doi: 10.1109/LED.2009.2038935.

[205] M. Allaei, M. Shalchian, and F. Jazaeri, "Modeling of Short-Channel Effects in GaN HEMTs," *IEEE Trans. Electron Devices*, vol. 67, no. 8, pp. 3088–3094, Aug. 2020, doi: 10.1109/TED.2020.3005122.

[206] B. Hult, "Design , Fabrication and Characterization of GaN HEMTs for Power Switching Applications," 2022.

[207] G. H. Jessen *et al.*, "Short-Channel Effect Limitations on High-Frequency Operation of AlGaN/GaN HEMTs for T-Gate Devices," *IEEE Trans. Electron Devices*, vol. 54, no. 10, pp. 2589–2597, Oct. 2007, doi: 10.1109/TED.2007.904476.

[208] M. L. Schuette *et al.*, "Gate-recessed integrated E/D GaN HEMT technology with f T /f max >300 GHz," *IEEE Electron Device Lett.*, vol. 34, no. 6, pp. 741–743, Jun. 2013, doi: 10.1109/LED.2013.2257657.

[209] P. Murugapandiyan, S. Ravimaran, and J. William, "Static and dynamic characteristics of L g 50 nm InAlN/AlN/GaN HEMT with AlGaN back-barrier for high power millimeter wave applications," *J. Sci. Adv. Mater. Devices*, vol. 2, no. 4, pp. 515–522, Dec. 2017, doi: 10.1016/j.jsamd.2017.08.004.

[210] P. Cui *et al.*, "InAlN/GaN HEMT on Si With fmax = 270 GHz," *IEEE Trans. Electron Devices*, vol. 68, no. 3, pp. 994–999, Mar. 2021, doi: 10.1109/TED.2021.3049316.

[211] H. Guo, Z. Feng, Y. Lv, Y. Fang, and X. Song, "High-frequency AlGaN/GaN HFETs with f T/f max of 149/263 GHz for D-band PA applications," *Electron. Lett.*, vol. 52, no. 15, pp. 1340–1342, Jul. 2016, doi: 10.1049/el.2016.1241.

[212] T. Han *et al.*, "70-nm-gated InAlN/GaN HEMTs grown on SiC substrate with f T / f max > 160 GHz," *J. Semicond.*, vol. 37, no. 2, p. 024007, Feb. 2016, doi: 10.1088/1674-4926/37/2/024007.

[213] D. M. Geum, S. H. Shin, M. S. Kim, and J. H. Jang, "75 nm T-shaped gate for In 0.17 Al 0.83 N/GaN HEMTs with minimal short-channel effect," *Electron. Lett.*, vol. 49, no. 24, pp. 1536–1537, Nov. 2013, doi: 10.1049/el.2013.2769.

[214] M. P. and X. G. B. P. Downey, D. J. Meyer, D. S. Katzer, J. A. Roussos, "SiNx /InAlN/AlN/GaN MIS-HEMTs With 10.8 THz·V," *IEEE Electron Device Lett.*, vol. 35, no. 5, pp. 527–529, 2014, doi: 10.1109/LED.2014.2313023.

[215] W. Jatal, U. Baumann, K. Tonisch, F. Schwierz, and J. Pezoldt, "High-Frequency Performance of GaN High-Electron Mobility Transistors on 3C-SiC/Si Substrates With Au-Free Ohmic Contacts," *IEEE Electron Device Lett.*, vol. 36, no. 2, pp. 123–125, Feb. 2015, doi: 10.1109/LED.2014.2379664.

[216] D. J. Denninghoff, S. Dasgupta, J. Lu, S. Keller, and U. K. Mishra, "Design of High-Aspect-Ratio T-Gates on N-Polar GaN/AlGaN MIS-HEMTs for High $f_{\max}$," *IEEE Electron Device Lett.*, vol. 33, no. 6, pp. 785–787, Jun. 2012, doi: 10.1109/LED.2012.2191134.

[217] H. Zhou *et al.*, "DC and RF Performance of AlGaN/GaN/SiC MOSHEMTs With Deep Sub-Micron T-Gates and Atomic Layer Epitaxy MgCaO as Gate Dielectric," *IEEE Electron Device Lett.*, vol. 38, no. 10, pp. 1409–1412, Oct. 2017, doi: 10.1109/LED.2017.2746338.

[218] J. S. Moon, R. Grabar, M. Antcliffe, H. Fung, Y. Tang, and H. Tai, "High-speed FP GaN HEMT with f T /f MAX of 95/200 GHz," *Electron. Lett.*, vol. 54, no. 10, pp. 657–659, May 2018, doi: 10.1049/el.2018.0417.

[219] F. Medjdoub, M. Zegaoui, and N. Rolland, "Beyond 100 GHz AlN/GaN HEMTs on silicon substrate," *Electron. Lett.*, vol. 47, no. 24, p. 1345, 2011, doi: 10.1049/el.2011.3166.

[220] D. Schwantuschke, P. Bruckner, R. Quay, M. Mikulla, and O. Ambacher, "High-Gain Millimeter-Wave AlGaN/GaN Transistors," *IEEE Trans. Electron Devices*, vol. 60, no. 10, pp. 3112–3118, Oct. 2013, doi: 10.1109/TED.2013.2272180.

[221] P. Xu *et al.*, "W-band GaN MMIC PA with 257 mW output power at 86.5 GHz," *J. Semicond.*, vol. 36, no.

8, p. 085009, Aug. 2015, doi: 10.1088/1674-4926/36/8/085009.

[222] Y. Zhang *et al.*, "Millimeter-Wave AlGaN/GaN HEMTs With 43.6% Power-Added-Efficiency at 40 GHz Fabricated by Atomic Layer Etching Gate Recess," *IEEE Electron Device Lett.*, vol. 41, no. 5, pp. 701–704, May 2020, doi: 10.1109/LED.2020.2984663.

[223] A. Crespo *et al.*, "High-Power Ka-Band Performance of AlInN/GaN HEMT With 9.8-nm-Thin Barrier," *IEEE Electron Device Lett.*, vol. 31, no. 1, pp. 2–4, Jan. 2010, doi: 10.1109/LED.2009.2034875.

[224] F. Medjdoub, N. Waldhoff, M. Zegaoui, B. Grimbert, N. Rolland, and P. A. Rolland, "Low-Noise Microwave Performance of AlN/GaN HEMTs Grown on Silicon Substrate," *IEEE Electron Device Lett.*, vol. 32, no. 9, pp. 1230–1232, Sep. 2011, doi: 10.1109/LED.2011.2161261.

[225] H. S. Yoon *et al.*, "Microwave Low-Noise performance of 0.17 µm Gate-Length AlGaN/GaN HEMTs on SiC With wide head Double-Deck T-Shaped gate," *IEEE Electron Device Lett.*, vol. 37, no. 11, pp. 1407–1410, Nov. 2016, doi: 10.1109/LED.2016.2612624.

[226] J. Bergsten *et al.*, "Performance enhancement of microwave gan hemts without an aln-exclusion layer using an optimized AlGaN/GaN interface growth process," *IEEE Trans. Electron Devices*, vol. 63, no. 1, pp. 333–338, Jan. 2016, doi: 10.1109/TED.2015.2501838.

[227] L. Yang *et al.*, "Enhanced gm and fT with High Johnson's Figure-of-Merit in Thin Barrier AlGaN/GaN HEMTs by TiN-Based Source Contact Ledge," *IEEE Electron Device Lett.*, vol. 38, no. 11, pp. 1563–1566, Nov. 2017, doi: 10.1109/LED.2017.2757523.

[228] Y. Zhang *et al.*, "High-Temperature-Recessed Millimeter-Wave AlGaN/GaN HEMTs with 42.8% Power-Added-Efficiency at 35 GHz," *IEEE Electron Device Lett.*, vol. 39, no. 5, pp. 727–730, May 2018, doi: 10.1109/LED.2018.2822259.

[229] Y. K. Yadav, B. B. Upadhyay, J. Jha, S. Ganguly, and D. Saha, "Impact of Relative Gate Position on DC and RF Characteristics of High Performance AlGaN/GaN HEMTs," *IEEE Trans. Electron Devices*, vol. 67, no. 10, pp. 4141–4146, Oct. 2020, doi: 10.1109/TED.2020.3019359.

[230] L. Yang *et al.*, "Analysis of DC, Channel Temperature, and RF Performance of in Situ SiN/AlGaN-Sandwich-Barrier/GaN/Al.GaN HEMTs," *IEEE Trans. Electron Devices*, vol. 67, no. 10, pp. 4147–4151, Oct. 2020, doi: 10.1109/TED.2020.3017136.

[231] G. Meneghesso *et al.*, "Surface-Related Drain Current Dispersion Effects in AlGaN–GaN HEMTs," *IEEE Trans. Electron Devices*, vol. 51, no. 10, pp. 1554–1561, Oct. 2004, doi: 10.1109/TED.2004.835025.

[232] I. Rossetto *et al.*, "Evidence of Hot-Electron Effects During Hard Switching of AlGaN/GaN HEMTs," *IEEE Trans. Electron Devices*, vol. 64, no. 9, pp. 3734–3739, Sep. 2017, doi: 10.1109/TED.2017.2728785.

[233] X. Chen, S. Boumaiza, and L. Wei, "Self-Heating and Equivalent Channel Temperature in Short Gate Length GaN HEMTs," *IEEE Trans. Electron Devices*, vol. 66, no. 9, pp. 3748–3755, Sep. 2019, doi: 10.1109/TED.2019.2926742.

[234] J. Li *et al.*, "An Improved Large Signal Model for 0 . 1 µ m AlGaN / GaN High Electron Mobility Transistors (HEMTs) Process and Its Applications in Practical Monolithic Microwave Integrated Circuit (MMIC) Design in W band," *Micromachines*, vol. 9(8), 396., 2018, doi: https://doi.org/10.3390/mi9080396.

[235] J. Luo *et al.*, "Effect of gate length on breakdown voltage in AlGaN/GaN high-electron-mobility transistor," *Chinese Phys. B*, vol. 25, no. 2, p. 027303, Feb. 2016, doi: 10.1088/1674-1056/25/2/027303.

[236] Y. Jia, Y. Xu, Z. Wen, Y. Wu, and Y. Guo, "Analytical Gate Capacitance Models for Large-Signal Compact Model of AlGaN/GaN HEMTs," *IEEE Trans. Electron Devices*, vol. 66, no. 1, pp. 357–363, Jan. 2019, doi: 10.1109/TED.2018.2881255.

[237] Y. S. Lin, Y. W. Lain, and S. S. H. Hsu, "AlGaN/GaN HEMTs with low leakage current and high on/off current ratio," *IEEE Electron Device Lett.*, vol. 31, no. 2, pp. 102–104, Feb. 2010, doi: 10.1109/LED.2009.2036576.

[238] K. Floros *et al.*, "Dual barrier InAlN/AlGaN/GaN-on-silicon high-electron-mobility transistors with Pt- and Ni-based gate stacks," *Phys. Status Solidi Appl. Mater. Sci.*, vol. 214, no. 8, Aug. 2017, doi:

10.1002/pssa.201600835.

[239] O. I. Saadat, J. W. Chung, E. L. Piner, and T. Palacios, “Gate-first AlGaN/GaN HEMT technology for high-frequency applications,” *IEEE Electron Device Lett.*, vol. 30, no. 12, pp. 1254–1256, Dec. 2009, doi: 10.1109/LED.2009.2032938.

[240] K. Shinohara *et al.*, “Scaling of GaN HEMTs and Schottky Diodes for Submillimeter-Wave MMIC Applications,” *IEEE Trans. Electron Devices*, vol. 60, no. 10, pp. 2982–2996, Oct. 2013, doi: 10.1109/TED.2013.2268160.

[241] D. Altman *et al.*, “Analysis and characterization of thermal transport in GaN HEMTs on Diamond substrates,” in *Fourteenth Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems (ITherm)*, May 2014, pp. 1199–1205. doi: 10.1109/ITHERM.2014.6892416.

[242] L. Sang, “Diamond as the heat spreader for the thermal dissipation of GaN-based electronic devices,” *Funct. Diam.*, vol. 1, no. 1, pp. 174–188, Jan. 2021, doi: 10.1080/26941112.2021.1980356.

[243] D.-Y. Chen *et al.*, “Microwave Performance of ‘Buffer-Free’ GaN-on-SiC High Electron Mobility Transistors,” *IEEE Electron Device Lett.*, vol. 41, no. 6, pp. 828–831, Jun. 2020, doi: 10.1109/LED.2020.2988074.