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Ultra-Thin Chip-based Printed Electronics for Emerging High-Performance Flexible Electronics

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Abstract

Flexible hybrid electronic (FHE) systems that signify the integration of printed electronics and conventional silicon (Si)-based CMOS technology, have gained tremendous interest in the past years owing to their newly discovered opportunities in wearables, soft robotics, ultra-thin displays, and healthcare devices, etc. These FHE systems are envisioned to cater to the demanding requisites of large-area electronics while maintaining high performance. Obtaining these characteristics exclusively through current Si technology or printed electronics however proves to be challenging. Achieving large-area electronics using Si technology alone is a demanding and high-cost task, and obtaining high performance with minimal data delays through printed electronics alone presents a substantial challenge. Nevertheless, the latter has unlocked pathways to resource-efficient and potentially environmentally sustainable routes for deploying electronics on diverse substrates. Consequently, the pragmatic approach involves the integration of devices fabricated through Si-CMOS technology and printed electronics into hybrid systems.

It is important to note that conventional Si-CMOS technology predominantly yields rigid devices. Therefore, the incorporation of thinning techniques to reduce wafer or chip thickness not only facilitates bendability but also ensures the preservation of flexibility within FHE systems. In this context, the concept of "flexible hybrid electronics (FHE)" or "heterogeneous integration," which combines ultra-thin chips (UTCs) with printed devices and interconnects, has garnered substantial interest. Despite advancements in each of these domains in recent years, substantial challenges persist in the effective integration of these technologies onto flexible substrates. Therefore, this thesis is devoted to addressing the enduring challenges associated with the development of ultra-thin integrated circuits (ICs) and their seamless integration with flexible foils, particularly in realising reliable interconnects using suitable techniques.

Firstly, the challenges associated with the development and handling of thin ICs are addressed. A novel two-step thinning process is devised, encompassing lapping with polymethyl methacrylate (PMMA) sacrificial technique and chemical etching using tetra-methyl-ammonium hydroxide (TMAH), enabling the attainment of UTCs with a thickness of up to 2 µm. The reliable and high-throughput lapping process is proven to be efficient and effective by showing stable device performance after thinning Si-based metal oxide semiconductor capacitors (MOSCAPs), aluminium nitride (AlN)-based pressure sensors and metal oxide semiconductor field effect transistors (MOSFETs) down to 35 µm with excellent flexibility. Si-based MOSFET UTCs have been used for all the following processes to enable FHE systems in this thesis to evaluate the reliability of the developed procedures. The challenges relating to physically bonding thin ICs have been addressed by adopting the direct transfer printing process. The electrical bonding between thin ICs and flexible foils is thoroughly studied and developed using high-resolution extrusion and electrohydrodynamic inkjet (EHD) printing. UTC-based MOSFET device performance is comprehensively evaluated at each fabrication step and eventually under bending, repeatedly confirming the reliability of every developed process step. The EHD printing system has also been adopted to realise high aspect ratio 3D pillars, opening opportunities to create out-of-plane high-density and high-performance electronics, demonstrated by fabricating photodetectors with excellent UV sensing and omnidirectional light-absorption ability. This thesis, which entails a comprehensive evaluation of each meticulously developed process, has not only affirmed the reliability and repeatability of these procedures but has also demonstrated their efficacy in the pursuit of realising high-density thin Si IC-based FHE systems. Through rigorous investigations, this research establishes a solid foundation for the implementation of these processes in practical applications.

List of Publications

Journal Publications:

1. **S. Ma**, A. S. Dahiya, and R. Dahiya, "Out-of-Plane Electronics on Flexible Substrates Using Inorganic Nanowires Grown on High-Aspect-Ratio Printed Gold Micropillars," *Advanced Materials*, p. 2210711, 2023, doi: https://doi.org/10.1002/adma.202210711.
2. A. Christou*, **S. Ma***, A. Zumeit, A. S. Dahiya, and R. Dahiya, "Printing of Nano to Chip Scale Structures for Flexible Hybrid Electronics," *Advanced Electronic Materials*, 2023, doi: 10.1002/aelm.202201116 (*Equal contribution).
3. **S. Ma**, A. S. Dahiya, A. Christou, L. D. Pamphilis, and R. Dahiya, "All-Printed ZnO Nanowire based High Performance Flexible Ultraviolet Photodetectors," *IEEE Journal on Flexible Electronics*, pp. 1-1, 2023, doi: 10.1109/JFLEX.2023.3243583.
4. **S. Ma**, Y. Kumaresan, A. S. Dahiya, and R. Dahiya, "Ultra-Thin Chips with Printed Interconnects on Flexible Foils," *Advanced Electronic Materials*, p. 2101029, 2021, doi: https://doi.org/10.1002/aelm.202101029.
5. **S. Ma**, Y. Kumaresan, A. S. Dahiya, L. Lorenzelli, and R. Dahiya, "Flexible Tactile Sensors using AlN and MOSFETs based Ultra-thin Chips," *IEEE Sensors Journal*, pp. 1-1, 2022, doi: 10.1109/JSEN.2022.3140651.
6. Y. Kumaresan*, **S. Ma***, and R. Dahiya, "PMMA Sacrificial Layer based Reliable Debonding of Ultra-Thin Chips after Lapping," *Microelectronic Engineering*, vol. 247, p. 111588, 2021, doi: https://doi.org/10.1016/j.mee.2021.111588 (* Equal contribution).
7. J. Neto, A. S. Dahiya, A. Zumeit, A. Christou, **S. Ma**, and R. Dahiya, "Printed n- and p-Channel Transistors using Silicon Nanoribbons Enduring Electrical, Thermal, and Mechanical Stress," *ACS Applied Materials & Interfaces*, vol. 15, no. 7, pp. 9618-9628, 2023, doi: 10.1021/acsami.2c20569.
8. L. D. Pamphilis, A. S. Dahiya, A. Christou, **S. Ma**, and R. Dahiya, "Patterned Assembly of Inorganic Semiconducting Nanowires using Lithography-free Technique," *IEEE Journal on Flexible Electronics*, pp. 1-1, 2022, doi: 10.1109/JFLEX.2022.3232079.
9. Y. Kumaresan, **S. Ma**, O. Ozioko, and R. Dahiya, "Soft Capacitive Pressure Sensor with Enhanced Sensitivity Assisted by ZnO NW Interlayers and Airgap," *IEEE Sensors Journal*, vol. 22, no. 5, pp. 3974-3982, 2022, doi: 10.1109/JSEN.2022.3143030.

Book Chapter:

1. **S. Ma**, F. Liu, and R. Dahiya, "Transistor-based Flexible Touch Sensors," in *Encyclopedia of Materials: Electronics*, A. S. M. A. Haseeb Ed. Oxford: Academic Press, 2023, pp. 1-13.

Conference Publications:

1. **S. Ma**, A. S. Dahiya, X. Karagiorgis, and R. Dahiya, "Ultra-Thin Chips for High-Performance Semi-Transparent Flexible Electronics," in *2023 IEEE International Conference on Flexible and Printable Sensors and Systems (FLEPS)*, 9-12 July 2023, pp. 1-4, doi: 10.1109/FLEPS57599.2023.10220424.
2. **S. Ma**, A. S. Dahiya, A. Christou, and R. Dahiya, "All-Printed ZnO Nanowire based High Performance Photodetectors," in *2022 IEEE International Conference on Flexible and Printable Sensors and Systems (FLEPS)*, 10-13 July 2022, pp. 1-4, doi: 10.1109/FLEPS53764.2022.9781570.
3. **S. Ma**, A. S. Dahiya, and R. Dahiya, "Direct Write 3D-Printed Interconnects for Heterogenous Integration of Ultra-Thin Chips," in *2022 IEEE International Conference on Flexible and Printable Sensors and Systems (FLEPS)*, 10-13 July 2022, pp. 1-4, doi: 10.1109/FLEPS53764.2022.9781596.
4. Y. Kumaresan, **S. Ma**, D. Shakthivel, and R. Dahiya, "AlN Ultra-Thin Chips based Flexible Piezoelectric Tactile Sensors," in *2021 IEEE International Conference on Flexible and Printable Sensors and Systems (FLEPS)*, 20-23 June 2021, pp. 1-4, doi: 10.1109/FLEPS51544.2021.9469763.

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Author's Declaration

I, Sihang Ma, declare that, except where explicit reference is made to the contribution of others, this thesis is the result of my own work and has not been submitted for any other degree at the University of Glasgow or any other institution.

Where others have provided a scientific and experimental contribution to the work presented in this thesis, a note is provided highlighting their contribution under the heading of the section in which that work is presented.

Glossary of Abbreviations

AJP	Aerosol Jet Printing
AM	Additive Manufacturing
CMOS	Complementary Metal-Oxide Semiconductor
CTE	Coefficient of Thermal Expansion
DIW	Direct Ink Write
EHD	Electrohydrodynamic
FHE	Flexible Hybrid Electronic
HT	Hydrothermal
IC	Integrated Circuit
LDW	Laser Direct Write
MEA	Micro Electrode Array
MOSFET	Metal-Oxide-Semiconductor Field Effect Transistor
NP	Nanoparticle
NW	Nanowire
PCB	Printed Circuit Board
PD	Photodetector
PDMS	Polydimethylsiloxane
PI	Polyimide
PMMA	Polymethyl Methacrylate
SEM	Scanning Electron Microscopy
Si	Silicon
SOI	Silicon-on-Insulator
TMAH	Tetra-Methyl-Ammonium Hydroxide
TSV	Through-Silicon Via
UTC	Ultra-Thin Chip
UV	Ultra-Violet
VIA	Vertical Interconnection Accesses
ZnO	Zinc Oxide

Chapter 1. Introduction

1.1 Background and Motivation

In an era of rapid technological advancement, the integration of flexible electronics is catalysing remarkable transformations in various aspects of human life. These next-generation electronics are not only reshaping innovation but also introducing novel applications that transcend traditional boundaries, offering potential uses in implantable and wearable systems, human-machine interactions, soft robotics, etc [1-3]. The realm of technological innovation continues to burgeon, notably exemplified by introducing printed electronics in recent years. The adoption of printing technologies furnishes a straightforward and cost-effective manufacturing route for large-area electronics with mass production. Printed electronics present fabrication attributes encompassing resource efficiency, owing to its additive nature, as well as innovative form factors such as lightweight, flexible, stretchable, soft, and degradable structures [4]. Notably, these characteristics allow independence from specific substrates, accommodating different flexible materials such as plastics, textiles, and paper [5].

However, the present applications of printed electronics cannot currently serve as a direct replacement for conventional silicon (Si)-based complementary metal-oxide semiconductor (CMOS) technology. This is primarily attributed to the modest performance, low integration density, and long switching times exhibited by fully printed devices and circuits [6]. The constrained device performance of printed electronics stems from two key factors: Firstly, commonly explored materials for fabricating flexible electronics involve organics, which inherently exhibit lower carrier mobility. Secondly, the high resolution of commercial printers (1 – 10 μm) is still considerably inadequate compared with the integration density achievable through conventional CMOS technology. Moreover, the chemical instability of the typically employed materials further restricts their applicability to lower-end uses. Many emerging and

futuristic applications such as the Internet of Things (IoTs), mobile healthcare, smart cities, and electronic skin (e-skin), etc. require rapid data processing and communication, which currently only Si-CMOS technology can achieve [7].

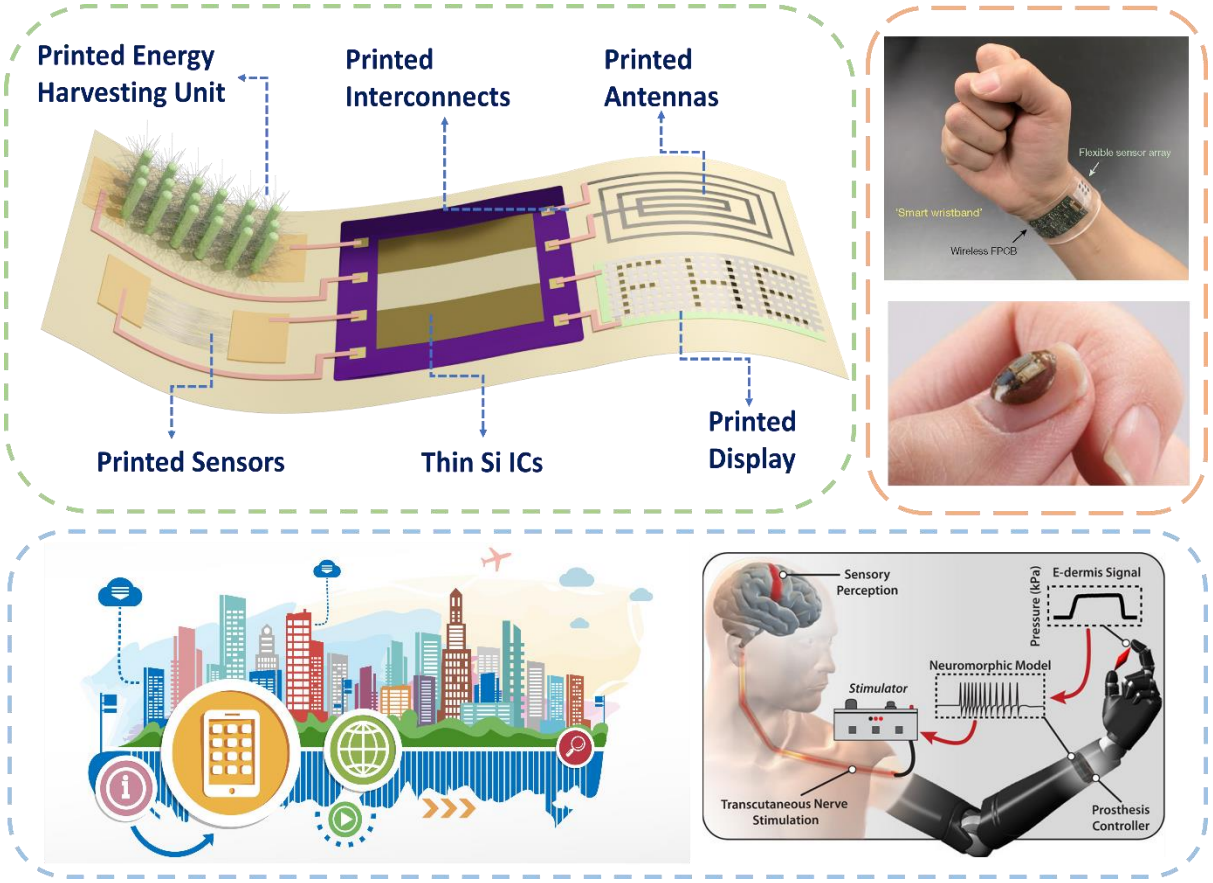

Figure 1-1. Schematic, current applications and future applications of flexible hybrid electronics.

Therefore, flexible hybrid electronics (FHEs) have emerged as an intermediate solution as they offer high-performance Si integrated circuits (ICs) and printed electronics on the same platform, surpassing the current limitations. There has been significant progress made in integrating rigid Si ICs on flexible substrates, however, rigid Si ICs established by standard CMOS process are prone to fracturing under bending, compromising the purpose of adopting flexible electronics. To address this concern and achieve Si-based high-performance FHEs, the advancement of Si thinning technology becomes imperative. Additionally, to realise FHEs, other integration factors and challenges are still yet to be overcome such as the handling of

ultrathin Si ICs, the physical bonding of thin Si ICs with flexible substrates, the electrical bonding to access ICs on thin Si chips/wafers as well as the integration and encapsulation of thin Si ICs with printed sensors. Therefore, this thesis is dedicated to advancing in high-performance FHEs.

1.2 Research Objectives

The aim of this thesis is to address long-standing challenges concerning the integration of ultra-thin flexible Si ICs on flexible substrates to meet the following objectives:

1) To advance the conventional CMOS technology to obtain ICs in flexible form factors.
2) To develop a new hybrid integration strategy for flexible ICs, particularly using the printing route to develop interconnects needed to access the circuits on flexible ICs.
3) To explore resource-efficient manufacturing of 3D micropillars and their potential use for steep interconnects.
4) To benchmark the state-of-the-art printing techniques for developed printed interconnects.

1.3 Thesis Structure

Following the introduction, this thesis is organised as follows:

Chapter 2 introduces the state-of-the-art technologies related to obtaining high-performance FHEs. The two main building blocks of realising FHE systems, the development of thin ICs and the interconnects needed to access devices and circuits on thin ICs, are discussed along with the operating mechanisms of existing technologies, feasibility, and challenges in terms of realising FHEs.

Chapter 3 presents the developed thinning technique used in this thesis, including mechanical and chemical thinning techniques. In particular, the mechanical backside lapping assisted with polymethyl methacrylate (PMMA) sacrificial technique is presented to obtain ultra-thin chips (UTCs). The reliability of the presented method has been confirmed repeatedly by showing negligible differences in device performance using chips having metal oxide semiconductor capacitors (MOSCAPs), aluminium nitride (AlN)-based pressure sensors and metal oxide semiconductor field effect transistors (MOSFETs). Additionally, combined with chemical etching, the thickness of UTCs can be further reduced.

Chapter 4 describes the process of forming interconnects to access MOSFET devices on UTCs from flexible substrates by adopting the extrusion-based high-resolution printing system with the capability of printing over UTCs' step height. This chapter includes the characterisation of printed interconnects on planar substrates as well as bonded with MOSFET devices. Device performance is evaluated before and after bonding by extrusion printing, as well as under 40 mm concave and convex bending. Further, a new approach of physically bonding UTCs on flexible substrates is presented using direct transfer printing. MOSFET devices are then evaluated before and after transfer printing as well as after forming interconnects by extrusion printing.

Chapter 5 introduces an alternative to extrusion printing to form interconnects by adopting electrohydrodynamic inkjet (EHD) printing with the capability of forming out-of-plane features. 3D micropillars with a high aspect ratio are presented with a detailed optimisation. New opportunities are discovered for the application of printed high-density 3D micro features. By combining additive manufacturing with the hydrothermal growth method, seedless synthesis of zinc oxide (ZnO) nanowires (NWs) on EHD printed high aspect ratio micro-electrode arrays is demonstrated via fabricating flexible photodetectors (PDs). Thorough studies are performed to evaluate the light sensing capabilities of the developed 3D structured

PDs including their omnidirectional sensing ability as well as mechanical stability under bending.

Chapter 6 further explores the possibility of adopting EHD printing to realise printed interconnects for UTCs on flexible foils. Attempts have been made to realise interconnects with a wire-bonding-like configuration. Challenges using EHD printing have been faced and explained. An efficient alternative approach has been developed to avoid all issues encountered previously by embedding UTCs in polyimide (PI), opening vias through lithography and printing vertical vias. Both EHD and extrusion printing are evaluated for this approach. Compatible inks for both systems are explored. Comprehensive studies are conducted to compare EHD and extrusion printing systems. MOSFET device performance on thin chips is assessed after each step, including via opening, via forming by printing, and under bending (40-, 30- and 20-mm concave and convex bending).

Chapter 7 summarises the key contributions of the thesis and provides suggestions for future work in this field.

1.4 Research Contributions

This thesis addresses the current challenges of delivering high-performance FHEs and provides novel processes developed with in-depth studies and optimisations to overcome these obstacles. The key contributions are summarised as follows:

1) An effective thinning method has been developed using the effective mechanical lapping assisted with the PMMA sacrificial technique to obtain Si chips with 35 µm thickness. The reliability of this optimised process has been confirmed by evaluating

chips with different devices. Further, this thesis presents an approach to realise thin chips ~2 µm thick by using chemical etching.

2) A reliable transferring approach to physically bond thin chips with flexible substrates by direct transfer printing has been established using the custom-made automated setup. MOSFET devices on thin chips are assessed before and after transfer printing, confirming the reliability of the developed process.
3) A resource-efficient method to form interconnects between thin chips and flexible substrates is developed by printing techniques. Extrusion and EHD printing systems are explored with detailed optimisations. Different configurations to integrate UTCs with printed interconnects are explored. Comprehensive studies are performed, including the comparison of both systems, electrical performance comparison of the effect on bonded MOSFET devices, and electrical performance stability of thin chips with printed interconnects under bending conditions. The transistor performance is investigated at each fabrication step.
4) New opportunities using EHD-printed 3D interconnects are explored by presenting a novel approach to realise out-of-plane flexible electronics. By combining additive manufacturing and the hydrothermal method, seedless synthesis of ZnO NWs on printed gold microelectrode arrays are formed, demonstrated as photodetectors. This hybrid approach leads to hierarchical light-sensitive NW-connected networks, showing favourable ultraviolet sensing. The 3D-configurated sensors exhibit excellent omnidirectional light absorption abilities and mechanical flexibility.

Chapter 2. State of the art

As suggested in Chapter 1.1, flexible hybrid electronic (FHE) systems that combine thin Si ICs and printed electronics have become the intermediate solution to achieve high-performance next-generation electronics with additional form factors (flexibility, stretchability and softness, etc.) for emerging applications. A comprehensive report titled 'Flexible Hybrid Electronics 2024-2034' was published by industry analysts from IDTechEx in July 2023. This report, based on years of monitoring the printed electronics sector and 40 in-depth interviews, predicts that FHE systems can be established across five distinct application fields (automotive, consumer goods, energy, healthcare/wellness, and infrastructure/buildings/industrial sectors), including 39 specific opportunities, such as skin temperature sensors and printed RFID tags. Through rigorous analysis, IDTechEx forecasts that the global demand for FHE circuits will achieve a value of approximately US$1.8 billion by 2034. This valuation could be even higher if factors such as infrastructure, software, and services are taken into consideration [8]. As a newly developed concept, there are many challenges to be addressed to realise FHEs, including the development and handling of thin Si ICs, realising interconnects using suitable techniques to access thin ICs, integrating thin ICs with printed sensors on flexible substrates and encapsulating of the entire system, etc. The primary goal of this thesis is to address the obstacles related to the two main building blocks in FHE systems, particularly the development of ultrathin ICs and interconnects that electrically bond thin ICs with flexible substrates.

This chapter introduces the state-of-the-art technologies associated with these two main building blocks for realising FHEs. The comprehensive research demonstrated in this chapter discusses the operating mechanisms of existing technologies, feasibility, and challenges regarding realising FHEs.

2.1 Development of Thin Si ICs

The growth of today's digital landscape has been significantly propelled by the reliable, batch-fabrication-capable, and well-established technology rooted in CMOS technology-based electronics. CMOS-based Si ICs that manage signal computation, communication as well as processing are one of the most important components in FHE systems and are often the only rigid integral parts. However, the rigid feature restricts the possibility of CMOS electronics being explored in emerging applications that require bendability/flexibility. The development of thin Si has therefore gained tremendous interest in recent years to achieve flexible high-performance CMOS electronics without compromising their functionality. Figure 2-1 presents the classification of different technologies for realising ultrathin Si, either based on silicon-on-insulator (SOI) wafers or bulk Si wafers.

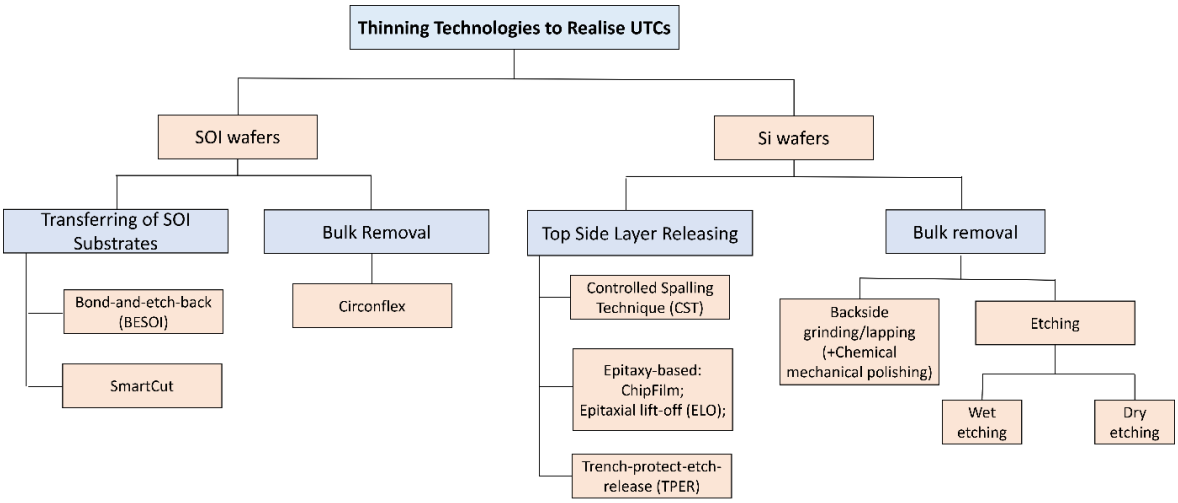

Figure 2-1. Classification of thinning technologies to realise UTCs.

2.1.1 SOI Wafer-based

In the case of using SOI wafers, electronic devices can be dielectrically separated from the Si substrate by creating a buried oxide (BOX) layer. Compared with conventional Si wafers, SOI wafers offer a higher resistance to latch-up, lower parasitic/junction capacitance and leakage

current, etc [9]. Ultrathin SOI wafers can be obtained by the transfer approach (bond-etch-back SOI (BESOI) or SmartCut) or bulk removal (Circonflex) [10, 11].

BESOI and SmartCut technologies both use BOX as the stopping point to obtain thin Si: (1) trenching the chip down to BOX then selectively removing the BOX; (2) attaching thin Si to a temporary wafer with the SOI side facing down, thinning the backside of the Si substrate until reaching BOX, followed by trenching the chip and releasing thin Si from the carrier wafer. BESOI involves bonding two wafers with an insulating layer in between and etching the backside of one of the wafers (Figure 2-2 (i)). The use of two wafers per production is costly, especially with one being wasted. In the case of SmartCut (Figure 2-2 (ii)), on the other hand, a recyclable handling wafer is used, and the thickness of the other wafer is reduced by splitting (high dose of hydrogen and subsequently high-temperature annealing) instead of etching [12]. However, the hydrogen implantation induces defects and increases the surface roughness. These two SOI-based technologies are also referred to as the device-last approach. The obtained ultrathin Si layer has often been used to fabricate devices by a selective removal of the BOX layer and selectively etching of the top layer for forming thin single crystal Si structures such as micro-/nanoribbons, then transferring printing them to flexible substrates for further device fabrication [13, 14].

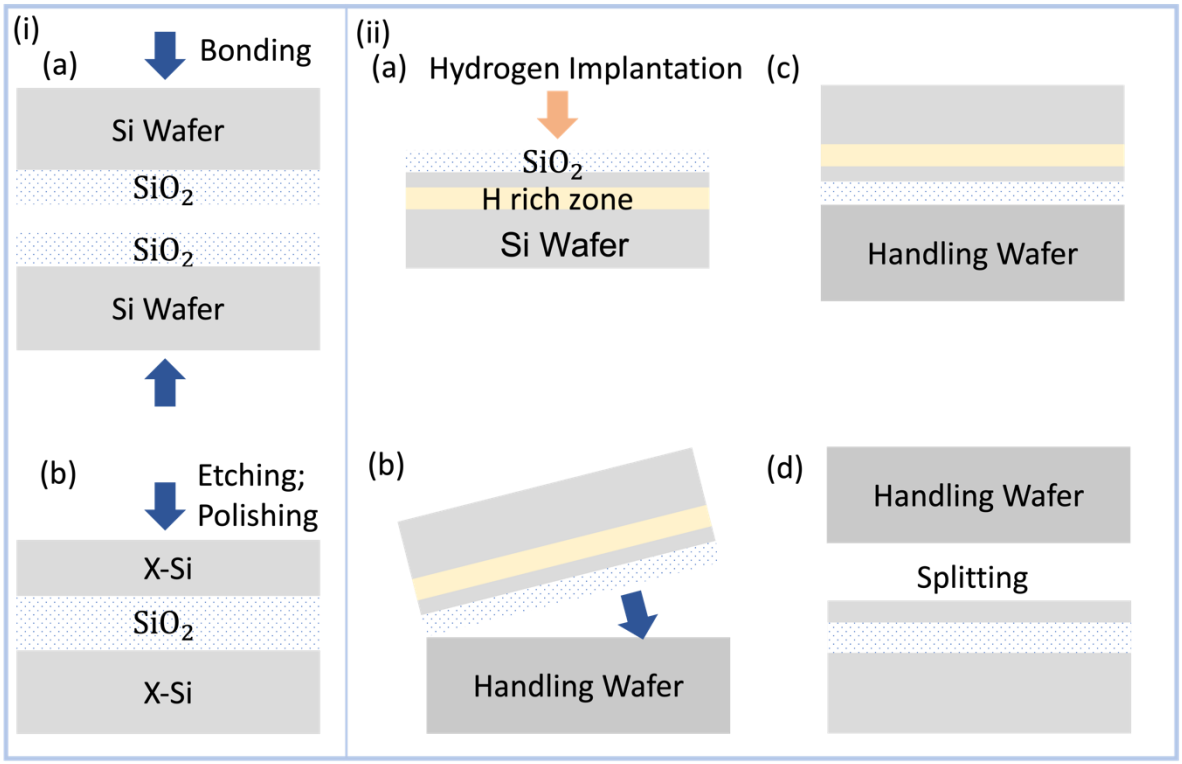

Figure 2-2. Schematic of SOI technology based on BOX removal (i) BESOI process; (ii) SmartCut® process.

Circonflex is a device-first approach (Figure 2-3). A polyimide film is used to cover the already fabricated devices on the SOI wafer, except the wafer edge, and a temporary glass carrier is attached to the sample with adhesive. Last, the bulk Si is selectively removed, and the ultrathin Si layer is released by trenching the wafer edges [15]. The merit of SOI technologies is that nanometre thickness is possible to achieve. However, multiple complex processes are inevitable, and the high manufacturing cost may hinder the further progress of such techniques for industrial-scale manufacturing. In addition, with thin thickness, the thermal conductivity of nanoscale Si is expected to be half of the undoped bulk Si, which could result in poor heat dissipation and require extra heat management [16]. Moreover, the dependence of mobility on temperature also needs to be taken into consideration, as higher temperature could lead to lower intrinsic mobility [17].

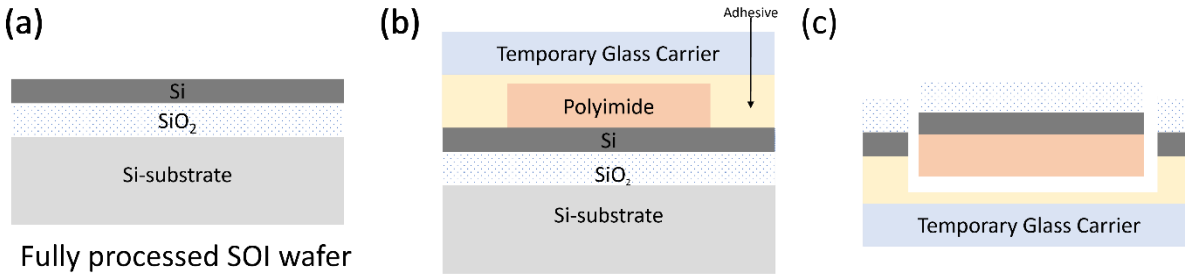

Figure 2-3. Schematic process of Circonflex technology.

2.1.2 Si Wafer-based

The bulk Si wafers offer a more cost-effective alternative to process in UTC technology (~$25 per 6-inch bulk Si wafer vs. ~$1000 per SOI wafer) [7]. Bulk Si-based thinning technologies are normally classified into two categories: (1) releasing the top layer; (2) removing the bulk Si from the backside. The controlled spalling technique (CST), also termed Slim-Cut, has been explored as one of the top layer releasing approaches. In this case, the top thin Si layer is achieved by inducing a fracture to propagate the crack in parallel to the wafer surface (Figure 2-4 (a)). To prevent the formation of cracks, a tensile stressor layer, such as nickel, is introduced in this technique. Owing to the induced upward shear force, the top thin Si layer can be removed from the bulk substrate. This method, although challenging, could achieve a controllable thickness of the desired top layer and fracture depth by taking advantage of the stressor layer material and/or thickness [18, 19]. UTCs can also be obtained using the trench-protect-etch-release (TPER) method (Figure 2-4 (b)). Firstly, deep reactive-ion-etching (DRIE) is used to form the deep trenches. A soft mask (photoresist) and hard mask (SiO_2) are used to protect the device side of the wafer, along with aluminium oxide (Al_2O_3) deposited by atomic layer deposition (ALD) to cover all other sides of the sample. Al_2O_3 on the backside of the wafer is etched using RIE and the wafer is subsequently etched using xenon difluoride (XeF_2), which leads to the formation of spheres merging with neighbouring spheres and therefore the release

of a top Si layer. In addition, the remaining bulk wafer can be re-used after polishing using chemical mechanical polishing (CMP), which reduces the overall process cost [20, 21]. Epitaxy-based top Si layer releasing is another approach that has been studied, such as Chipfilm technology and epitaxial lift-off (ELO). By introducing a sacrificial layer (e.g., a porous Si or epitaxially grown layer) between the bulk wafer and the top Si layer, the removal of the desired top layer can be realised either physically or chemically (Figure 2-4 (c)). The advantage of this technique is the precise control over the desired thickness of the top Si layer [22].

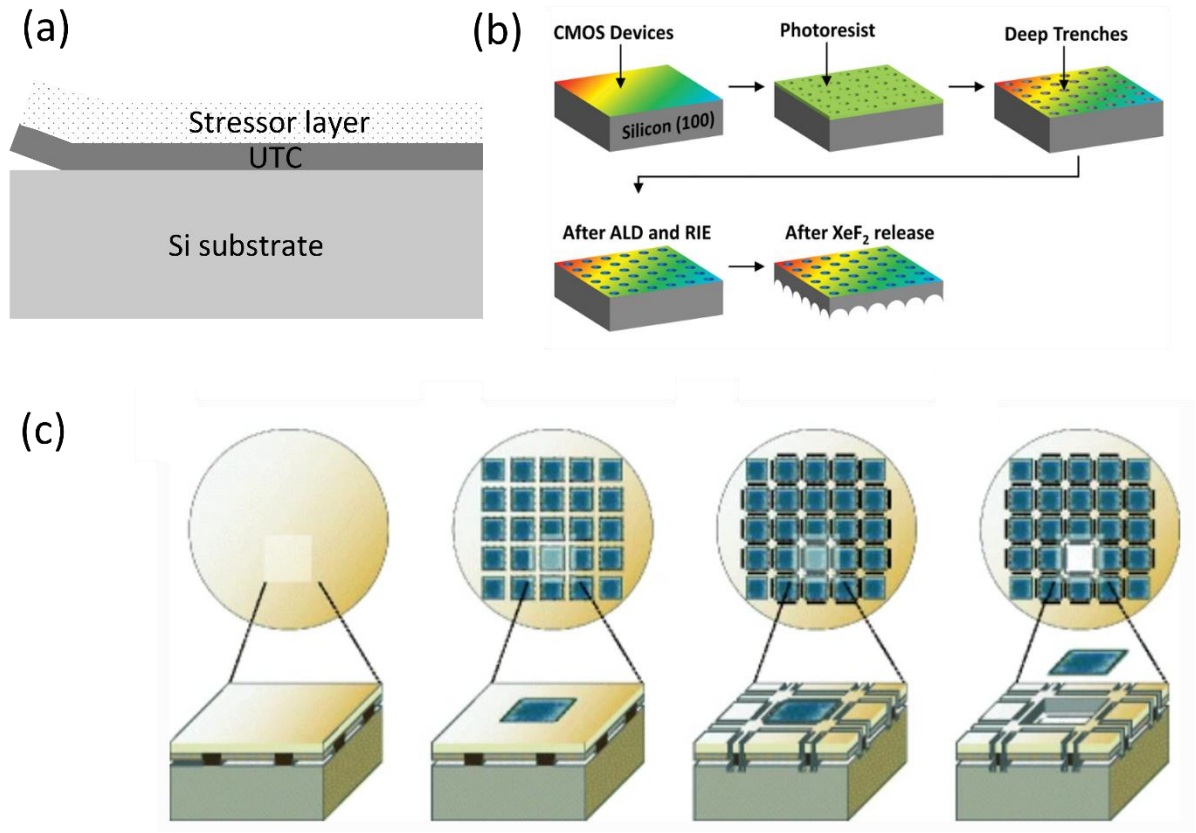

Figure 2-4. Schematic of UTC Si-based technology by releasing top layers: (a) Controlled Spalling Technique (CST); (b) Trench-protect-etch-release (TPER). Reprinted with permission from [20]. Copyright John Wiley & Sons; (c) ChipFilm technology. Reprinted with permission from [22]. Copyright Springer.

The other category of Si-UTC technology is focussed on removing the bulk substrate after the device fabrication on the front side, usually assisted with a protective layer for the top side,

including backside lapping/grinding [23], wet etching [24], dry etching [25], or a combination of all.

Backside lapping/grinding (Figure 2-5 (a) and (b)) is the most commonly used because of its higher throughput than the other techniques and good surface flatness of the desired thin chips [26]. Backside mechanical thinning is usually conducted with 2 steps: (1) Coarse thinning for a rapid removal rate; (2) Fine thinning for obtaining a smooth surface with a relatively slower etch rate. The main disadvantage is that high mechanical stress is induced in the Si crystal structure, potentially leading to wafer warpage or even breakage. Therefore, different stress-relief methods have been explored, such as etching (introduced below), dicing before grinding (DBG), or stealth dicing before grinding (SDBG). In the case of DBG, wafers are partially grooved before grinding. After grinding, the final thickness can be less than those realised by dicing after grinding (DAG) with a less chance of breakage. However, blade sawing and tape removal can both potentially induce wafer chipping. The potential issues created by mechanical interaction during DAG and DBG can be overcome by SDBG where a laser process is implemented internally [27]. SDBG can be conducted at a high speed by a completely dry process without giving rise to any debris pollution. The disadvantages of the SDBG process include that the wafer separation process is assisted by tape expansion, posing risks in surface cracks propagated from the stealth dicing layer [28]. A more cost-effective stress-relief method has been developed in this thesis and shown with comprehensive studies in Chapter 3.

Chemical mechanical polishing (CMP), also referred to as chemical mechanical polarisation, has also been used to improve the surface quality after the major removal of the bulk substrate (Figure 2-5 (c)). As during this process unwanted materials on an atomic scale can be removed by chemical etching for a desirable flatness, CMP can be a part of an integrated thinning process to reduce the non-flatness generated from previous procedures [29].

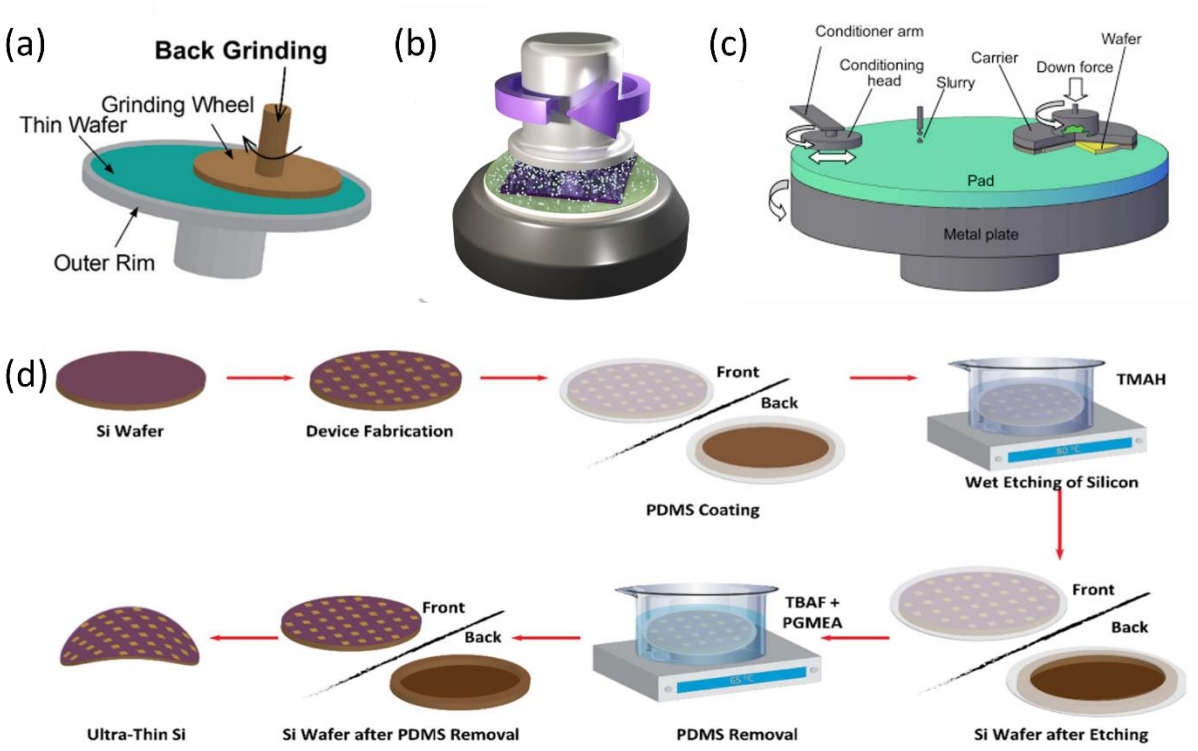

Figure 2-5. Schematic of Si-UTC technology for bulk removal: (a) Backside grinding [7]; (b) Backside lapping [30]; (c) Chemical mechanical polishing. Reprinted with permission from [29]. Copyright from ScienceDirect; (d) Wet chemical etching [31].

In addition to the previously mentioned mechanical-based processes, wet and dry etching can be further employed to reduce the wafer thickness. Wafers are less likely to be affected by crystalline defects and microcracks due to the absence of mechanical pressure on the wafer during wet/dry etching processes. In the case of wet etching, aqueous solution is employed to dissolve the Si substrate. For this, two kinds of solutions are used to provide isotropic or anisotropic results. Solutions containing nitric acid (HNO_3) or hydrofluoric acid (HF) can lead to isotropic etching, which is orientation-independent and can potentially cause under-etching [32]. The reaction of Si oxidisation by HNO_3 and dissolution by HF are shown as follows (Equation 2-1 and 2-2):

$$3Si + 4HNO_3 \rightarrow 3SiO_2 + 4NO + 2H_2O \qquad 2\text{-}1$$

$$SiO_2 + 6HF \rightarrow H_2SiF_6 + 2H_2O \qquad 2\text{-}2$$

Anisotropic wet etching usually involves etchants such as potassium hydroxide (KOH), ethylene diamine-pyrocatechol (EDP), or tetra methyl ammonium hydroxide (TMAH) [33]. The chemical reaction in anisotropic wet etching is separated into an oxidation reaction and a reduction reaction, and the simplified reaction can be expressed as Equation 2-3:

$$Si + 2OH^- + 2H_2O \rightarrow SiO_2(OH)_2^{--} + 2H_2\uparrow \qquad 2\text{-}3$$

Anisotropic etching often causes pyramid-shaped hillocks of the material surface, which can be prevented by adding IPA in the etchant to decrease the formation of hydrogen bubbles.

Dry etching is a thinning method run in a reactive ion atmosphere. Similar to wet etching, it is well known for not giving rise to edge chipping as mechanical pressure is not involved. It is also not likely to cause mask undercutting which has been observed in the isotropic wet etching process. There are various types of dry etching processes, including reactive ion etching (RIE), reactive ion beam etching (RIBE), ion beam etching (IBE), barrel etching and reactive sputter etching (RSE) [34]. RIE is the most common type of dry etching where it combines the anisotropic or directional ionic bombardment and isotropic reactions. U-grooves can be generated after dry etching without the sharp crack tip, giving rise to less stress concentration and better surface flatness. Due to the relatively lower etch rate using wet or dry etching, they are mostly used as a stress-relief thinning approach after the completion of the mechanical grinding/lapping. Table 2-1 summarises a comparison between different thinning technologies regarding their challenges.

Table 2-1. Comparison of different thinning technologies regarding their challenges.

Technologies	**Challenges**	**Ref.**
SOI Wafer based	1. Higher cost for SOI processing than Si wafers 2. Complexity and difficulties of fixing, transferring and supporting UTCs during the removal process of the remaining wafer	[9]
Controlled Spalling Technique (CST)	1. Extra tensile stress induced by the deposition of the stressor layer, potentially shifting the Si band structure, therefore changing the effective mass of carriers and carrier mobility 2. Difficulty of controlling the desired top layer thickness 3. Wafer warpage due to the tensile stress even after removing the stressor layer	[35, 36]
Epitaxy-based: Chipfilm Technology, Epitaxial lift-off (ELO)	Time consuming, low throughput and costly due to the use of epitaxy	[20]
Trench-Protect-Etch-Release (TPER)	The space available for device fabrication is reduced because of the creation of holes due to the trench formation	[20]
Backside grinding/lapping	High stress induced in the crystal structure; stress-relief methods often needed	[23]
Wet etching	Time consuming, mask undercutting for isotropic etching or hillock formation on the surface for anisotropic etching	[24]
Dry etching	High cost, low throughput	[37]

2.2 Bonding

In addition to successfully developing ultrathin Si ICs, the other crucial component in realising FHE systems is the interconnects. This section describes the existing interconnect technologies including their operation mechanism and suitability of being employed for thin Si IC-based

FHE systems. Conventional interconnect technologies that have been explored for UTC electrical bonding are firstly discussed, followed by the resource-efficient printing techniques (Figure 2-6).

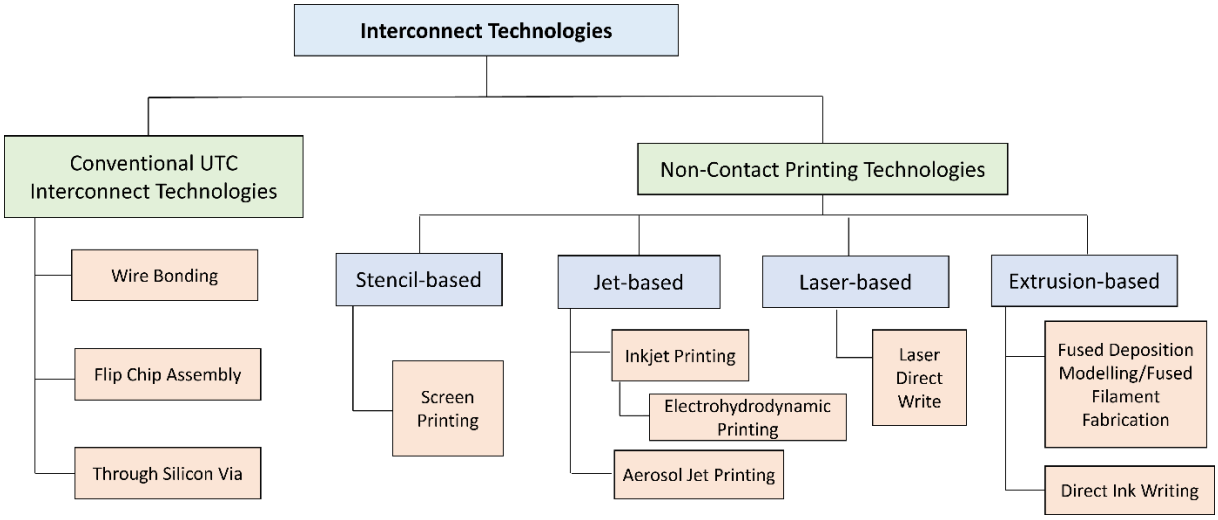

Figure 2-6. Classification of interconnect technologies.

2.2.1 Conventional UTC Interconnect Technologies

2.2.1.1 Wire bonding

Wire bonding is the most prevalent traditional packaging method due to its manufacturing flexibility, low cost and maturity [38]. Ninety percent of the first-level chip interconnects in the world are assembled through wire bonding [39, 40]. The bonding process starts with a process named die or chip attach where an organic adhesive, a low melting point glass, a eutectic alloy or the reflow of a metal alloy is used to adhere the backside of the chip to the substrate. Sequentially, capillary or wedge bonding tools, with tip sizes ranging from 12.5 to 500 µm diameter are employed to firmly attach wires to bond pads on the chip. There are three wire bonding methods including thermocompression bonding, ultrasonics bonding and thermosonic bonding [41].

Thermocompression and thermosonic bonding usually involve forming a ‘ball bond’ on the first bond pad on the chip with one end of the wire and a ‘wedge bond’ on the second pad with the other end of the wire on the package (Figure *2-7* (a)). The major factors in the thermocompression process are temperature, force or pressure and time. Firstly, it demands high temperature (usually ranging from 300-400°C) at the bonding interface between wires and pads, heated through either the capillary tool or the stage with a bonding force of 0.5-1.5N, depending on the wire materials [42]. Ultrasonic bonding produces a wedge-wedge bonding structure (Figure *2-7* (b)). In comparison with the ball bonding structure from thermocompression, ultrasonic bonding provides narrower bonds and lower wire loop heights, giving rise to finer pitches. It is performed at room temperature with ultrasonic energy and mechanical pressure (ranging from 0.35 to 0.6 N) [43]. Besides, the ultrasonic energy is generated through a transducer in a frequency range of 20-300 kHz [39]. Thermosonic bonding is a combination of thermocompression and ultrasonic bonding, using high temperature, ultrasonic energy and mechanical forces [44]. However, the temperature in this case is less than thermocompression, usually around 200 °C or even lower, resulting in less risk of intermetallic growth of bonding structures [45]. In addition, by integrating both temperature and ultrasonic energy at the interface between the pad and bond, the bond force needed is less than the other two techniques, usually ranging from 0.2 to 0.4 N [46]. To avoid device damage potentially caused by forces created through the bonding processes, bond pads are usually located at the peripheral or non-active region of the chip.

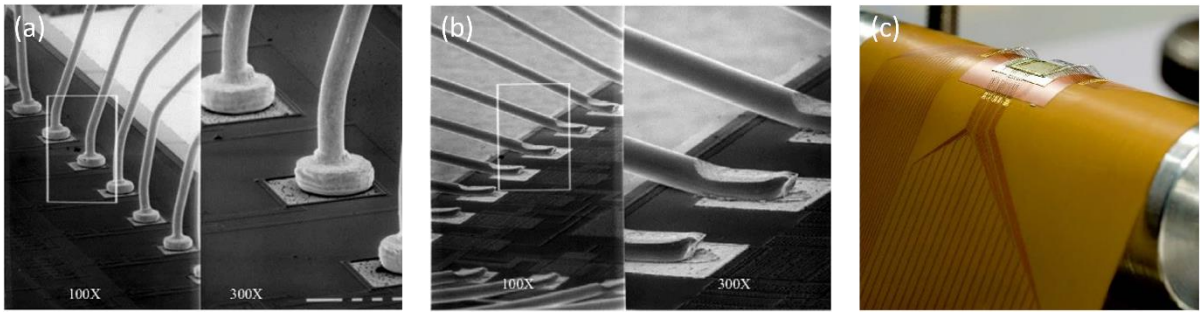

Figure 2-7. (a) Thermocompression or Thermosonic (Ball bonds); (b) Ultrasonic bonds [39] Copyright Springer; (c) Wire-bonded UTC on flexible substrates [47].

UTC bonding by conventional wire bonding has been adopted in a few studies (Figure *2-7* (c)) [48-50]. Nevertheless, despite the maturity of the wire bonding process, wires developed in this technique are known to present large minimum loop height (finest = 52 µm, commonly used = 130 – 200 µm) and therefore require a large footprint of the packaged systems [51]. This could hinder the progress of high-density FHE integration and packaging. Besides, in the case of adopting wire bonding on soft/flexible substrates, titanium-tungsten or titanium nitride layers are required to be placed between the bond pads and the flexible substrate to strengthen the adhesion. Titanium migration can lead to bonding issues and increased metallization hardness, requiring more aggressive bonding parameters for high-quality bonds, such as higher bonding temperatures (>180 °C) and high-temperature die attach (gold-silicon eutectic) [39]. Additionally, the inevitable involvement of mechanical pressure during the bonding process is required, it has been found that the compressive loading of rigid capillaries can cause the deformation of flexible substrates, leading to weak attachment at the interface between the bonding wires and the bonding pads [50].

2.2.1.2 Flip chip (FC) assembly

The original flip chip assembly, namely Controlled Collapse Chip Connection (C4), was developed by IBM in the 1960s. As suggested by its name, the chip is bonded to the substrate with its front side or device side facing down. By depositing conductive materials on the pads across the wafer surface, FC also enabled the first ‘Wafer-Level Packaging’ process [52]. Unlike wire bonding where the bond pads are required to be placed at the periphery side of the chip, the FC pads can be distributed over the whole surface of the chip/wafer, allowing a smaller form factor, less signal noise and higher density of Input/Output (I/O) counts, 10 times

higher than wire bonding (the number of I/O per unit area) [53]. As a result, FC technology offers better performance than wire bonding with reduced inductance, improved device speed and noise control. However, the finest inline pitch of FC-bonded interconnects achieved so far is only around 90μm, three times higher than wire bonding [54]. Besides, each interconnect built by FC costs 20 to 50 times more than the wire bonding counterpart ($ 0.0005 – 0.001 per interconnect with full automation by wire bonding, $ 0.01 – 0.05 per interconnect by FC) [39].

FC assembly can be conducted by different approaches, including solder reflow, thermocompression and thermosonic energy. Different FC assembly approaches for UTCs have been reported. For instance, 25μm-thick UTCs can be reflow-soldered on top of the polyimide substrate [55]. Alternatively, solder connections can be achieved through vias to reach the other side of the polyimide (PI) or liquid crystal polymer (LCP) substrates to minimise the thickness of the whole package (Figure 2-8 (a)). UTCs can also be thermocompression-laminated into LCP films without the need to use underfill (Figure 2-8 (b)) [56]. However, it has been found that the utilisation of underfill helps redistribute the thermal stress on the solder joints due to low mismatch in the coefficient of thermal expansion and improves the adhesion between the chip and substrate. It has been reported that underfill can expand the solder joint's fatigue life by 10 to 100 times [57]. Another utilisation of FC assembly is to be assisted by adopting anisotropic conductive adhesives (ACA), such as anisotropic conductive films (ACF) and anisotropic conductive pastes (ACP), as a low temperature (100 – 150 ˚C) fabrication alternative of the conventional solder involved processes (temperature required: 180 – 300 ˚C). A study showed that FC-bonded UTCs with ACP interconnects possessed less resistance but also lower bending cycles to failure than the ACF counterpart. It was concluded that the morphology of the conductive particles contributed to a lower contact resistance, however, the polymer-cored particles in ACF are more flexible [58]. A photograph of UTCs bonded by FC assembly on a flexible substrate is shown in Figure

2-8 (d) [55]. Despite the convenience of achieving both physical and electrical bonding with one step in FC assembly, challenges are posed by several factors, such as the difficulty to test (as the device sides are facing down after completing the assembly process), the high possibility of misaligning the pads on UTCs with pads on substrates due to the facing down configuration, and the difficulty in precisely controlling the adhesive distribution. Adhesive over-dispensing often occurs, leading to excessive spreading of the adhesive, flowing over the chip, and presenting a higher profile than UTCs. Controlled ACA dispensing has only been accomplished on the laboratory scale. This will further cause challenges in post-processing including integrating bonded UTCs with printed sensors in FHE systems. Issues related to controlled adhesive distribution have also been faced in this thesis and addressed in Chapter 4.3.

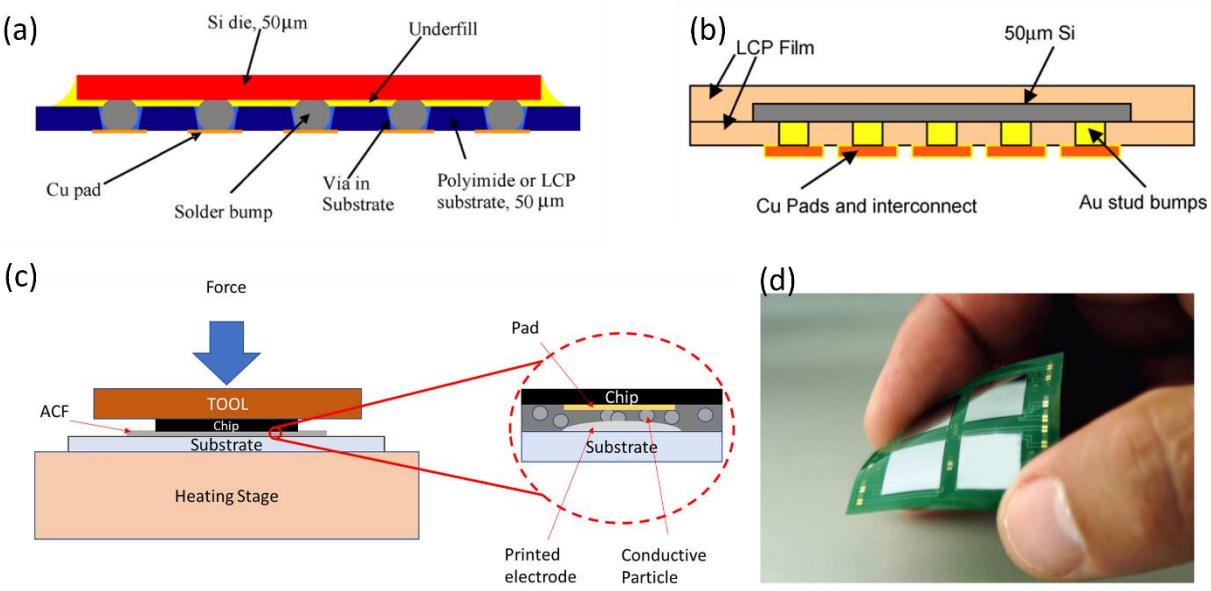

Figure 2-8. (a) FC laminated into LCP films; (b) thermocompression-laminated FC bonding without the use of underfill [56]; Copyright IEEE (c) Adhesive-based FC schematic [58]; Copyright Elsevier (d) Photograph of FC-bonded UTCs on the flexible substrate [55]; Copyright IEEE.

2.2.1.3 Through-Silicon Via (TSV)

Vertically connected electrical interconnects that are etched into silicon wafers can be achieved by through-silicon via (TSV) technology, usually for the application of UTC 3D integration as the more-than-Moore solution. TSV can be used for wafer-to-wafer bonding, die-to-die bonding and die-to-wafer bonding [59]. The advantages of TSV not only include shorter interconnect length, lower latency, capacitance and inductance but also enhanced energy efficiency, higher speed and number of interconnections [60, 61]. It can be categorised into three classifications: (1) simple-backside-connection where the back of the wafer is vertically connected without any die stacking; (2) 2.5D integration where TSVs are created in the interposer; (3) 3D integration where TSVs are formed in active dies, enabling die stacking. Different processes to manufacture TSVs are summarised in Figure 2-9 (a) – (d). The fabrication process includes forming the vias using deep reactive ion etching or laser drilling, followed by SiO_2 deposition, barrier and seed deposition, via filling by Cu plating, and Cu plating residue removal through chemical and mechanical polishing (CMP) [62].

Figure 2-9 (e) shows an example of a cross-section of 3D integrated thin chips using TSV and Figure 2-9 (f) is an example of a cross-section of an UTC (~15μm thickness) with TSV [33, 63]. Cu usually is needed during the process, whilst the mismatch between the coefficient of thermal expansion of Cu and Si can cause wafer warpage [62]. Heat dissipation-related issues have also posed a significant challenge, impeding the progress towards achieving high-volume production. To date, this process has only been conducted on rigid substrates or thin Si substrates. Difficulties relating to integrating this process on flexible foil would need to be further considered and addressed. Nevertheless, the complexity of the fabrication processes gives rise to low throughput and high cost [64].

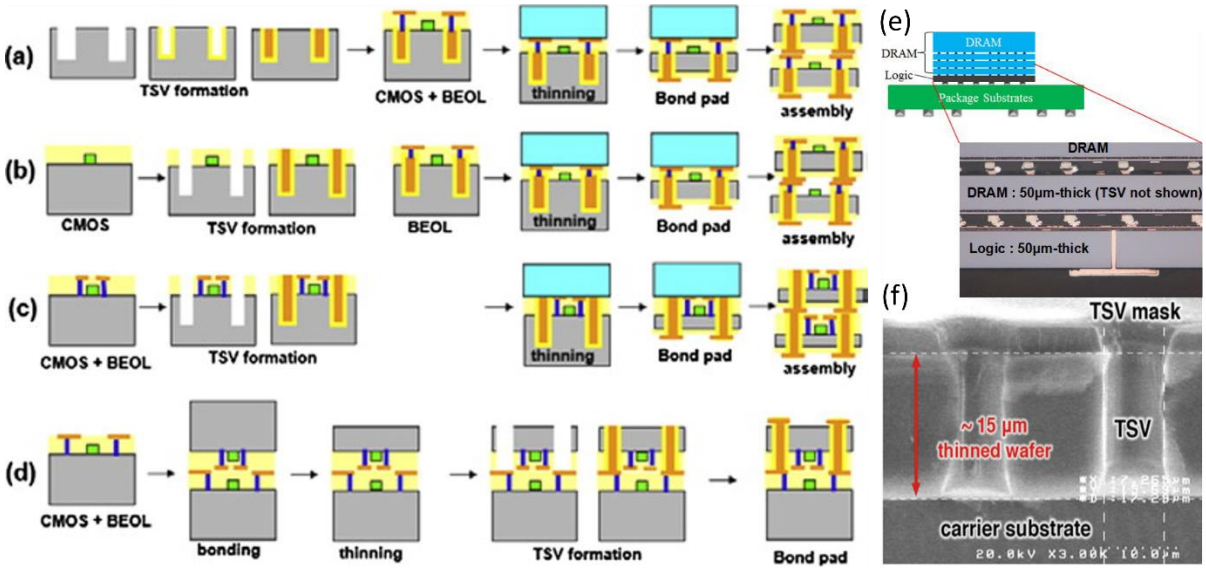

Figure 2-9. Schematic of different TSV process flow: (a) Frontside via-first; (b) Frontside via-middle; (c) Frontside via-last; (d) Backside via-last [61]; Copyright Elsevier (e) Cross section of 3D integrated thin DRAM and logic chips; [63] Copyright IEEE (f) UTC cross-section with TSV [33] Copyright Springer.

In conclusion, this section discussed the existing technologies used for UTC electrical bonding, including wire bonding, flip chip assembly and through-silicon via. Concerning the possibility of adopting these conventional interconnect technologies to enable flexible hybrid electronics, there are still limitations that cannot be neglected. The constraints associated with wire bonding include large minimum loop heights, increased footprint size, adhesion challenges on soft substrates, and the risk of substrate deformation due to mechanical pressure, all of which hinder high-density FHE integration and packaging. Although flip chip offers a smaller form factor, less signal noise, and higher density of Input/Output (I/O) counts, several challenges arise. Due to the downward-facing configuration, there are testing difficulties and high risks of misaligning the pads on UTCs with those on substrates. The complexity of precisely controlling the adhesion distribution also leads to challenges in FHE integration. Through-silicon via technology has yet to be discovered for UTC integration with flexible foils. There are still concerns to be addressed such as dissipating heat from stacked thin dies. The complexity and high cost of the fabrication process also impede the progress towards high-volume production.

2.2.2 Bonding by Printing

Considering the difficulties and complexities in the conventional UTC interconnect technologies, printing technologies, for selective and maskless deposition of functional materials on targeted substrates, have been taken into consideration for realising interconnects for UTCs. As a single-step additive approach, printing technologies are more straightforward, cost-effective, and resource-efficient than the conventional fabrication approach. Printing technologies can be classified into two categories, contact and non-contact printing. Contact printing technologies such as offset lithography, gravure printing and flexography have been commonly used, which however involve direct large area contact between the printing tool and the substrate. As mentioned above, UTCs exhibit physically fragile natures after the thickness has been reduced. Therefore, during post-processing, mechanical pressure acting on UTCs needs to be minimised. Thus, in this section, only non-contact printing technologies (including the ones in which only the printing tip is in microcontact with the substrate with negligible force) with controlled deposition are considered. Additionally, as semiconductor devices continue to undergo reductions in feature sizes while simultaneously enhancing their functionality, there is an increasing demand for the capacity to establish connections between smaller pads with ultra-fine pitch (<50 μm) and lower interconnect heights (<60 μm) [65]. A noteworthy aspect often subject to the comparison between printing and conventional fabrication is the achievable resolution. Therefore, it is crucial to acknowledge that some of the cutting-edge printing techniques have enabled significant advancements in facilitating nanoscale fabrication capabilities, such as pyroelectrodynamic printing, dielectrophoretic printing, Dip-pen nanolithography, projection microstereolithography, etc [66]. Considering the minimum pitch that can be achieved by conventional UTC interconnect technologies (summarised in Table 2-2), an ideal printing technique for this application should be comparable to the conventional counterparts and align with the future prediction. The adoption

of nanoscale printing technologies would lead to extremely low throughput. Therefore, amongst all printing systems, only the ones that meet the requirements abovementioned are discussed in this section, which are stencil-based, jet-based, laser-based and extrusion-based systems.

2.2.2.1 Screen printing

Screen printing can be used as both contact and off-contact printing technology and is the most adopted printing method in the industry due to its maturity, fast speed, simplicity, and large-scale productions. The printing process involves a mesh screen being moved by a squeegee with the ink being poured through the open areas of the mesh screen. As a result, the printed pattern is directly replicated from the designed meshes. The commonly selected ink/paste include gold, silver and carbon [67]. There are two types of screen-printing techniques, flat-bed screen printing and rotary screen printing respectively, both of which operate based on the same principle, as demonstrated in Figure 2-10 (a) and (b) [68]. Rotary screen printing is better suited for fully continuous processes owing to higher speed, improved edge definition and resolution compared with flat-bed screen printing.

Screen-printed interconnects have been widely explored. In the case of UTC bonding, it has been reported that 5μm-thick face-up and face-down piezoresistive UTCs attached on polyimide tapes can be fabricated with screen-printed silver ink with a measured resistivity of 2.03×10^{-5} Ω.cm. (Figure 2-10 (c)) [69]. Another application for UTC interconnects is to integrate UTCs onto screen-printed circuitry by placing UTCs facing up (Figure 2-10 (d)) or facing down through flip-chip bonding with conductive adhesives [58, 70]. Thus, the same limitations from flip chip assembly would arise in this case too, as mentioned in Chapter 2.2.1.2. The disadvantages of implementing screen printing include material waste such as

screen and stencil waste, ink waste and screen reclamation chemicals, and relatively poor resolution (50 – 100 µm) [71]. Other constraints in screen printing arise from its dependence on pre-determined stencils or screens, which can result in higher costs as only a limited number of designs can be accommodated per stencil.

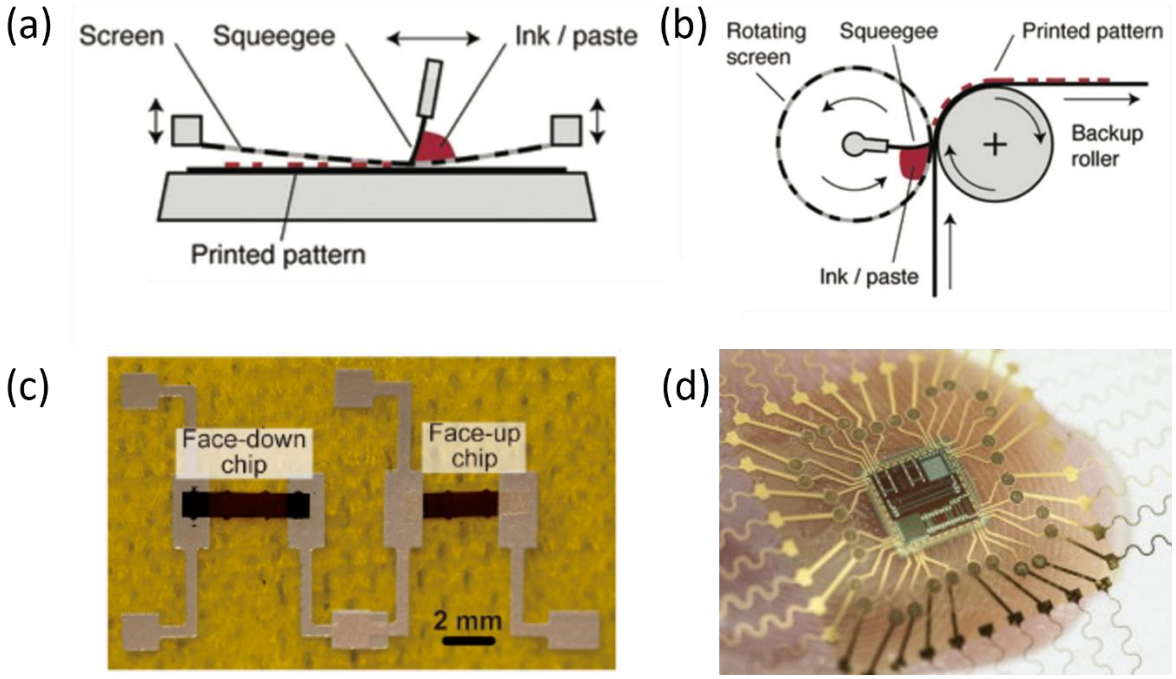

Figure 2-10 Schematics of screening printing technology: (a) flat-bed screen printing; (b) rotary screening printing [68] Copyright John Wiley & Sons; (c) 5µm-thick face-up and face-down UTCs with screen-printed interconnects [69] Copyright MDPI; (d) 20 µm-thick UTC with fan-out interconnection scheme on screen-printed circuitry [70] Copyright Elsevier .

2.2.2.2 Inkjet printing

Printing patterns can also be realised by inkjet printing through applying digital commands to deposit different functional inks through nozzles. The highest printing resolution ranges from 20 to 50 µm [72]. It is operated in two modes, Continuous Inkjet (CIJ) and Drop-On-Demand (DoD) respectively (Figure 2-11). CIJ is traditionally used for high-speed operation through its uniformly spaced and sized droplets (Figure 2-11 (a)). It generates a continuous flow of liquid droplets, with undesired droplets redirected by the electric field towards a collection area (a

gutter). Recycling of the unused ink can be conducted. However, in materials science applications, recycling it, after having been exposed to the environment, poses the risk of ink contamination. Therefore, CIJ printing can be considered a potentially wasteful process. On the contrary, DoD printing is more environmentally friendly and flexible with the process of generating droplets where needed. It is usually either thermally or piezoelectrically conducted (Figure 2-11 (b) and (c)) [73, 74]. The printed feature sizes can be manipulated by controlling the pressure pulse used to form droplets, which is one of the advantages of adopting digitally controlled printing systems without any mask requirements, unlike the conventional fabrication route and screen printing. Owing to the compatibility with group printheads, the maximum printing speed of inkjet printing can reach up to ~8000 mm/s [5]. The ink viscosity should ideally be less than 20 centipoise (cP) for inkjet printing to ensure a smooth droplet ejection without clogging the nozzles [75].

Interconnects between contact pads on bare dies have been realised through inkjet printing with the assistance of firstly forming a ramp using non-conductive adhesive to level the step height between the chip and substrate (Figure 2-11 (d)) [76]. Similar to the case introduced in Chapter 2.2.1.2 related to precisely controlling the adhesive dispense, the same challenges are expected to occur in this case, and will be explained and addressed in Chapter 4.3. In addition, one layer of printed lines does not show conductivity. The lowest resistance achieved is ~10 Ω and 130 Ω by gold and silver nanoparticle inks respectively after printing 50 μm-length interconnects with 5 layers [77]. Nevertheless, multi-layer printing leads to the risk of ink overflowing, resulting in short-circuiting between adjacent interconnects. Ink spreading is usually observed in this technology, negatively impacting on the resolution, the morphology of the printed patterns, integration degree and eventually the electrical stability of the printed electronics [78]. More specifically, inkjet-printed droplets can cause bulging, scalloping or even open lines as a result of the discrete drop nature [79]. Coffee ring effects are also commonly shown in inkjet-

printed patterns, which need additional processes to solve, such as reducing the rim evaporation [80].

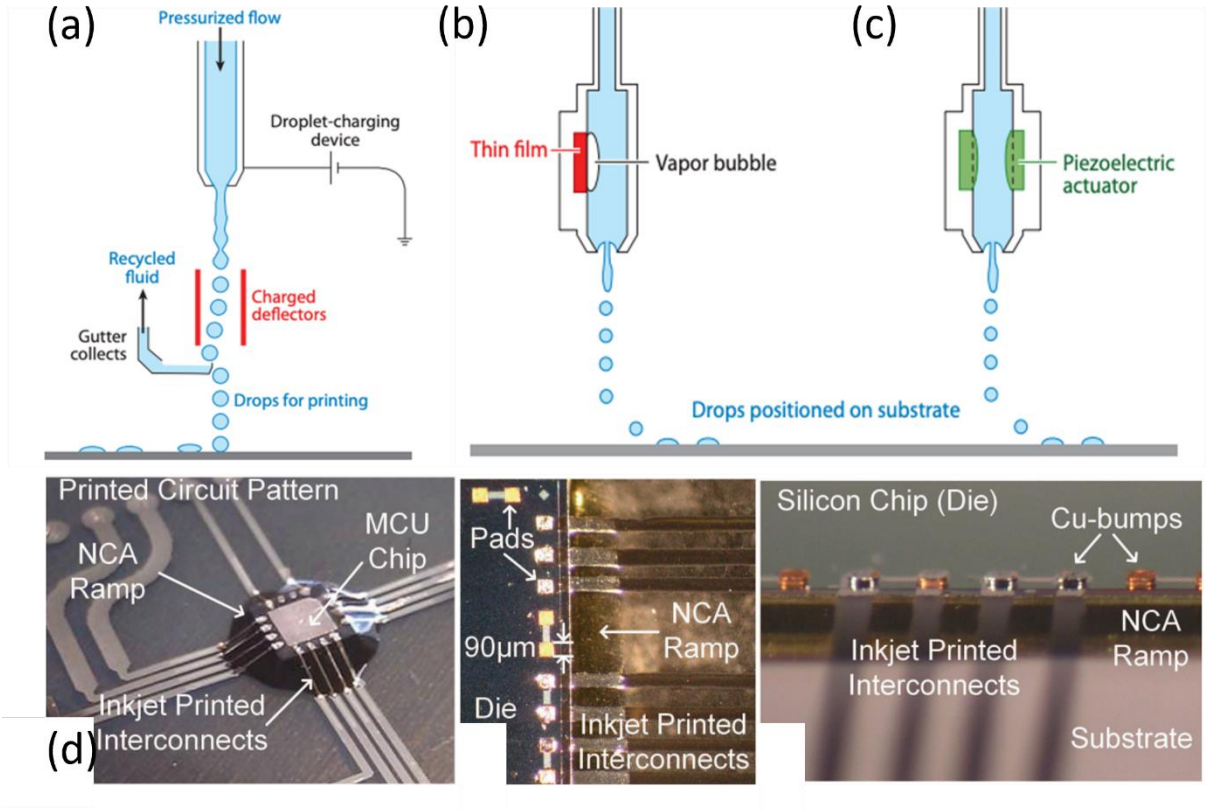

Figure 2-11. Illustration of inkjet printing technology: (a) Continuous inkjet; (b) Drop-on-Demond thermally conducted; (c) Drop-on-Demond piezoelectrically conducted [74] Copyright Annual Reviews; (d) Examples of inkjet-printed interconnects for packaged chip and bare die including the top view and side view [76].

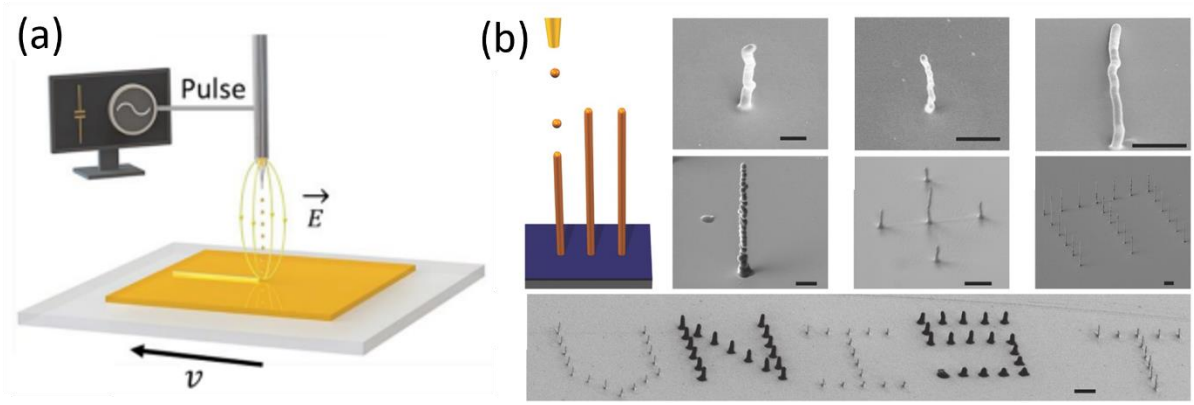

Figure 2-12. Electrohydrodynamic inkjet printing: (a) Schematic; (b) Pillar printing schematic and SEM images [81, 82] Copyright John Wiley & Sons.

2.2.2.2.1 Electrohydrodynamic

As mentioned above, one of the most critical challenges regarding using inkjet printing is the resolution limitation as inkjet printing often causes ink spreading. When aqueous fluids are deposited on metal and/or glass surfaces, the diameter of the dropped spot on the substrate generally becomes two to four times larger than that of the droplet [83]. Consequently, the minimum volume of droplets generated by conventional inkjet printing would not be precise for nanotechnology. The interconnect resolution plays a significant role in the UTC bonding and an ideal alternative using printing techniques should have comparable capabilities as conventional bonding technologies. The difficulty of realising more precise patterns with higher resolution has led to the invention of electrohydrodynamic inkjet (EHD or E-jet) printing which is derived from the conventional inkjet printing discussed above (Figure 2-12 (a)). Different from inkjet printing, EHD printing is operated through externally applied electrical fields instead of thermal or piezoelectric energies. The ink is firstly transferred from a reservoir to form a hemispherical meniscus at the nozzle tip. The electrical field is then applied by the voltage bias between the nozzle tip and the substrate, the surface charge of the ink accumulates, and a conical shape (also referred to as Taylor cone, first described by Sir Geoffrey Taylor) at the nozzle tip is subsequently formed. When the electrostatic stress exceeds the force at the cone tip with increasing applied voltage, droplets are generated [84]. Droplets with smaller diameters than the nozzle diameters can be achieved through EHD printing whereas the finest inkjet-printed droplet diameters (without considering ink spreading) are usually equal to the diameter of the nozzles [85].

The superfine inkjet (SIJ) printer, the newest novel EHD printer, has been developed by the National Institute of Advanced Industrial Science and Technology (AIST). Based on electrohydrodynamics, SIJ creates pressure to eject droplets through an oscillating electric field between the nozzle and the printing stage. In comparison with EHD printing, SIJ does not form

a Taylor cone that has limited process controllability [86]. More precise control and variety on printed patterns can be achieved as there are multiple printing parameters, such as voltage, bias voltage, frequency, stage moving speed, stage moving acceleration, etc. to assist in realising desired features (high resolution: 1-10 μm). The manipulation of a combination of printing parameters facilitates the construction of 3D printed features using low viscosity ink. This coordination ensures that the droplets have sufficient time for partial evaporation before the arrival of subsequent droplets. The ability of forming free-standing 3D features that make this system stand out amongst the others. In addition, there is no material waste during the printing process, which lowers the cost and negative environmental impact. Besides, a wide range of inks can be used in SIJ, such as silver and gold nanoparticles, carbon nanotubes, fluorescent dyes, electro-conductive polymers and functional ceramics [87]. Therefore, an EHD-based SIJ printer has been adopted in this thesis for achieving printed interconnects (Chapter 5 and Chapter 6).

2.2.2.3 Aerosol Jet Printing (AJP)

Similar to inkjet printing, aerosol jet printing (AJP) is also a digitally controlled deposition method compatible with functional inks and the finest aerosol jet printed resolution is 10μm [88]. AJP is classified into two different systems, ultrasonic and pneumatic atomisation (Figure 2-13 (a) and (b)). Ultrasonic atomisation supports lower viscous inks with 1-10 cP, whereas pneumatic atomisation tolerates higher viscosity, up to 1,000 cP [89]. More specifically, in terms of the operating mechanism, concentrated vapour is produced by the atomiser, based on either ultrasonic or pneumatic systems, after the nano-material ink has been inserted into it. Subsequently, the vapour is transferred to the deposition head by the atomiser (gas) flow passing through the atomiser, which is then concentrated further by the sheath flow within the

deposition head, leading to the formation of the co-axial annular flow. Lastly, the flow exits from the deposition head through the nozzle and deposits the ink onto the substrate [89, 90].

Ag interconnects for two rigid chips in the vertical integration on rigid printed circuit boards (PCBs) have been achieved by the AJP technique (Figure 2-13 (c)). This could be further investigated for transforming to flexible hybrid systems using flexible foils as substrates and ultrathin ICs. However, it was also found that printed interconnects would peel off from the Si/SiO_2 substrate and it worsens with the increasing number of printing layers. More studies regarding compatible printing materials are needed. Surface pre-treatment can be considered too. In this study, only 2 printing layers could be conducted on the PCB with mandatory surface treatment [91]. This could highly likely limit the desired resistance of the printed lines without the capabilities of vertical multi-layer printing using relatively low-viscosity inks.

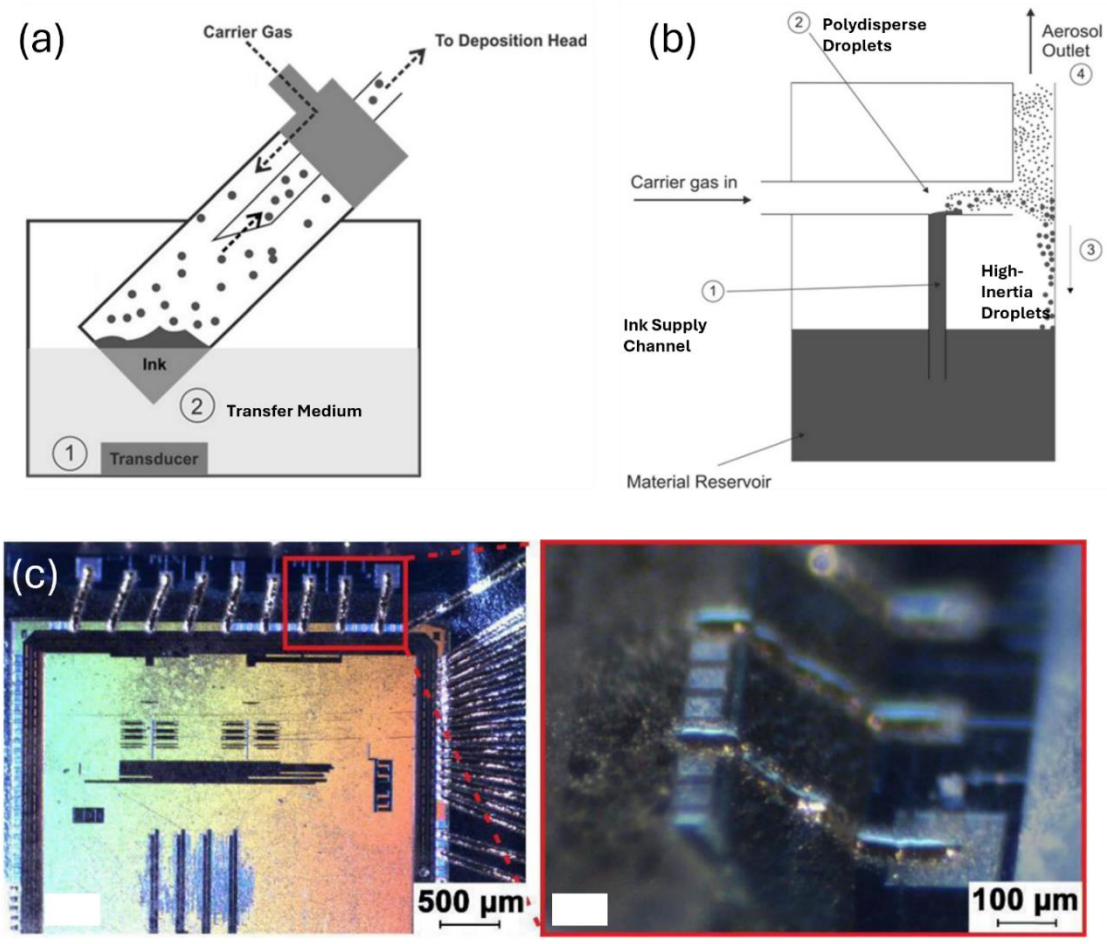

Figure 2-13. Schematics of AJP based on (a) Ultrasonic atomisation; (b) Pneumatic atomisation; [89] Copyright Springer (c) Printed electrical connections between chips and PCB [91] Copyright Elsevier.

2.2.2.4 Laser Direct Write (LDW)

Laser Direct Write, often also referred to as laser-induced forward transfer (LIFT), is another high-resolution computer-controlled printing technique. It can generate uniform and well-defined 2D and 3D structures with a resolution of 10 µm by depositing metals, semiconductors, polymers and ceramics through laser without any physical contact between the tool and the target substrate (Figure 2-14 (a)) [92, 93]. It is compatible with high-viscosity paste (~100 – 400,000 cP) and high solid content of the paste (> 80 wt.%) [94]. A transparent donor or sacrificial carrier substrate coated with the material of interest is required to be placed close to a receiving substrate. When the pulsed laser energy exceeds the threshold energy, the desired patterns from the donor substrate can be released or de-bonded by the pulsed laser. The propelled materials are subsequently placed on the acceptor or the receiving substrate through the laser decal transfer process [92]. The deposition of drops, lines and voxels can be achieved through LIFT [95].

3D structures such as micropillars (30 µm × 30 µm × 75 µm, aspect ratio 2.5) have been realised by vertically tacking 20 voxels (Figure 2-14 (b)). The ability to assemble micro-scale voxels has been used for creating high-resolution 3D interconnects. Although LDW has not been explored for UTC bonding applications, Cu bond pads on Si have been bonded by using Ag paste to form two circular voxels (radius = 4 µm, thickness = 1 µm) at the bottom and a bridging rectangular voxel (15 µm × 6 µm × 1 µm) on top with a resistance of ~37 Ω (Figure 2-14 (c)) [96]. Additional attention is required when printing metallic materials as the printing process involves melting the material, which easily leads to metal oxidation and poor adhesion between the deposited metal and substrate. Printing materials compatible with this technique is relatively limited. Low-viscosity inks are not recommended as debris can be easily

established, lowering the achievable resolution. Ceramics and inorganic materials are not suited due to irreversible phase changes and decomposition during melting and solidification [97].

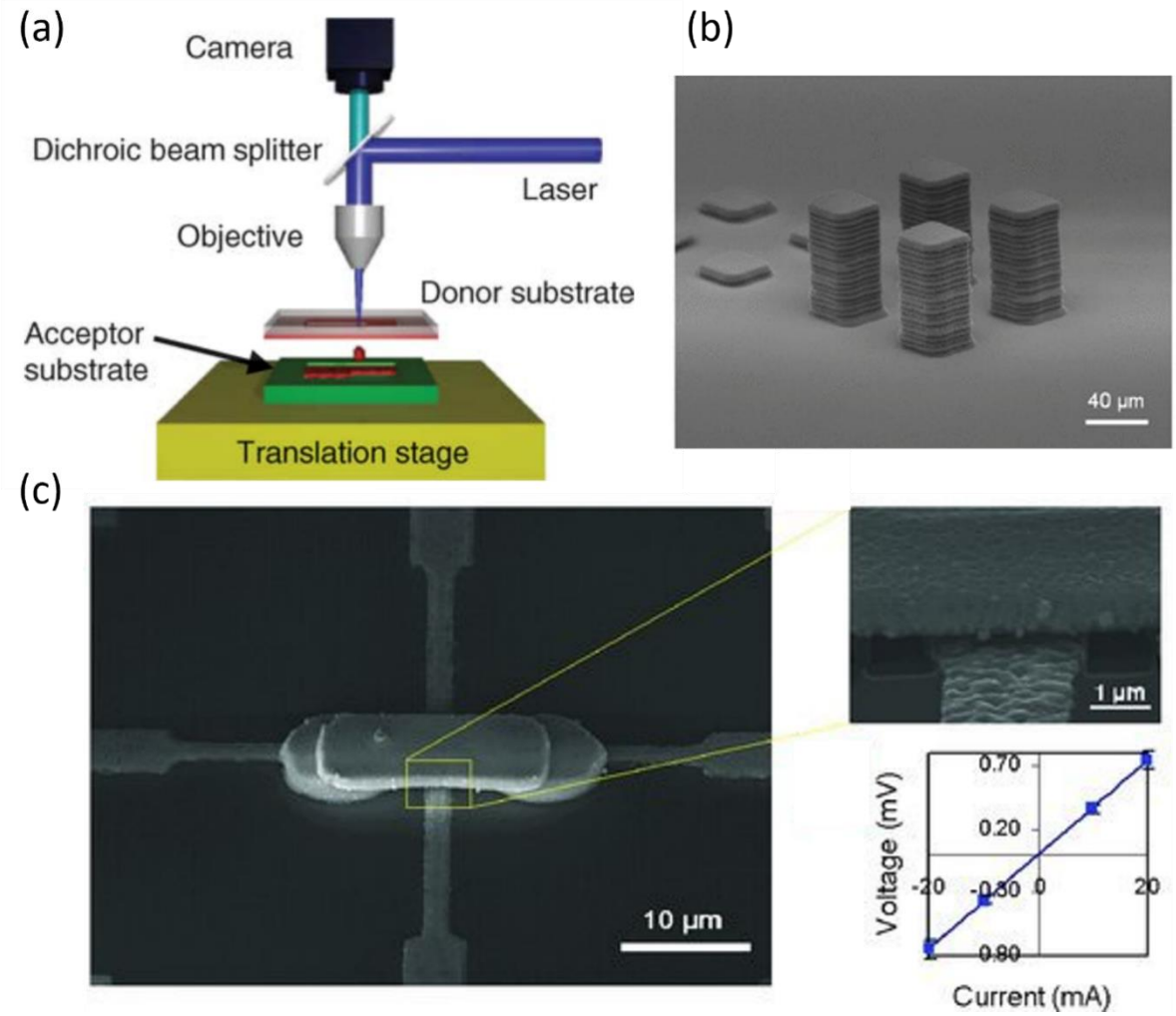

Figure 2-14. (a) Schematic of LDW [92]; Copyright Springer. (b) and (c) SEM of laser printed micro pillar arrays, interconnects bonding Cu electrodes, IV curve of the interconnect [96] Copyright John Wiley & Sons.

2.2.2.5 Extrusion Printing

Extrusion printing provides continuous ink/paste disposition through nozzles using pneumatic or mechanical forces with a computer-interfaced system [98]. The commonly used extrusion systems include fused deposition modelling (FDM), also known as fused filament fabrication (FFF), and direct ink writing (DIW). FDM/FFF generates 3D structures based on the melt

extrusion of thermoplastic filaments (that can solidify when cooled down after heating) made of polymeric materials or polymers with functional materials, such as polyvinyl alcohol (PVA), polylactic acid (PLA), PLA with graphene, etc. [99]. DIW refers to the extrusion of viscoplastic inks/pastes, which is more commonly used in smaller-scale fabrication such as printed sensing electronics, bioprinting, etc. [100]. To meet the requirements of UTC bonding, interconnects between the thinned chips and substrates are required to be highly conductive and robust with a 3D structure that covers the step height between contacts on the chips and substrates (equivalent to the sum of the thickness of UTCs and adhesives). In the case of other printing techniques discussed above, multiple printing passes are needed to suit such criteria. On the contrary, DIW is compatible with conductive ink/paste with high viscosity and yield stress without clogging the nozzles [101]. High viscous inks/pastes are more advantageous in printing, which is explained as follows: The preferable inks in all non-contact printing technologies are usually the ones with non-Newtonian rheological properties, which is explained as follows [102]: the ink's effective viscosity changes depending on the shear rate. During printing, when the ink reaches the nozzle tip and gets ejected from the nozzle, it experiences an increasing shear strain as the nozzle diameter becomes smaller towards the nozzle tip. Under the increasing shear rate, the ink becomes less viscous (shear-thinning behaviour), which can be expressed by the Herschel-Bulkley equation 2-4:

$$\tau = \tau_y + K\dot{\gamma}^n \qquad 2\text{-}4$$

where τ is the shear stress, τ_y stands for the yield stress, K is the viscosity parameter, $\dot{\gamma}$ is the shear rate and n is the shear thinning exponent or the flow index [103]. Besides, commonly used Au or Ag-based paste is highly thixotropic (time-dependent shear thinning property), which implies that it has the capability of recovering to its initial value of viscosity after printing [104, 105]. Furthermore, higher viscosity leads to more resistance to shear, less likely

causing ink spreading. Therefore, higher viscous inks are more beneficial for realising high aspect ratio structures.

Despite the lack of studies in interconnects printed by such system for UTC integration, it has been investigated that a single-pass printing can be achieved in extrusion printing for 3D Ag interconnects (line width = 15 µm and height = 13 µm) for silicon solar cells (Figure 2-15 (c)). [106]. The potential of the extrusion mechanism and compatibility with high-viscosity printing materials have prompted an investigation into its feasibility for application in UTC bonding, which has led to the discovery of a newly developed high-precision printer, XTPL Delta Printing System. It supports high-resolution printing (1 – 10 µm lines) and high viscosity paste (100,000 cP with a metal content of 82 wt.%). The suitability for UTC electrical bonding has been studied in Chapter 4 and Chapter 6 with different integration configurations.

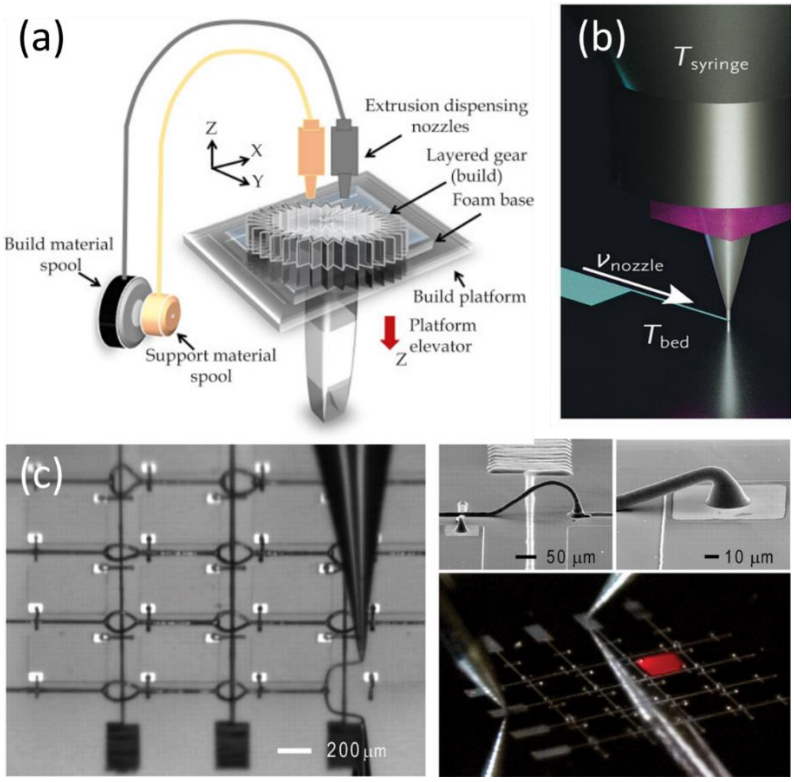

Figure 2-15. Schematic of extrusion-based printing (a) Fused deposition modelling or fused filament fabrication [107]; Copyright ScienceDirect (b) Direct ink writing [108]; Copyright John Wiley & Sons (c) Optical images of DIW-printed Ag interconnects [106] Copyright Science.

Table 2-2. Comparison of UTC interconnect technologies

Interconnect Technologies		Finest Pitch (µm)	Limitations for flexible Electronics	Ref.
Conventional Techniques	Wire Bonding	30	1. Mandatory bonding force and temperature, damaging flexible foils 2. High interconnect length and height, large footprint required 3. Limited I/O count (100 – 1000s) 4. Adhesion challenges on soft substrates	[39, 54]
	Flip Chip	90	1. Larger pitch 2. Poor alignment 3. 20-50 times most costly than wire bonding per interconnect 4. Difficulties in testing 5. Difficulty in precisely controlling the adhesive distribution	[39]
	Through Silicon Via	< 5	1. Wafer warpage due to CTE mismatch between Si and Cu 2. Low throughput and high cost	[25, 62]
Printing Techniques	Screen Printing	50 – 100	1. Lower resolution 2. Material waste	[71]
	Inkjet Printing	20 – 50	1. Ink spreading affecting the resolution, morphology of the printed patterns, integration degree and eventually the electrical stability of the printed electronics 2. Discrete drop nature causing droplet bulging, scalloping or even open circuit	[72, 109]

	Electrohydrodynamic	~1 – 10	1. Feasibility to be discovered, optimisation required	[110]
	Aerosol Jet Printing	< 10	1. Discontinuity in line morphology 2. Degraded performance due to overspray	[88, 91]
	Laser Direct Write	< 10	1. Limited printing materials	[93, 97]
	Extrusion Printing	~1 – 10	1. Feasibility to be discovered, optimisation required	[106]

2.3 Conclusion

This chapter introduced various technologies regarding the development of UTCs and interconnect technologies that could potentially electrically bridge the devices on UTCs and the flexible substrates. This chapter discussed the operating mechanism of each technology, their limitations, and the feasibility of being adopted for realising thin Si IC-based FHE systems.

To be more specific, two methods to obtain bendable ultra-thin Si were presented, SOI wafer-based and Si wafer-based. The Si wafer-based bulk removal approach was concluded to be more appealing due to simpler processes. However, amongst the bulk removal methods, stress relief processes such as etching are time consuming, and fast operational mechanical thinning inevitably introduces pressure onto thin chips. Issues related to this obstacle are solved by introducing a novel and cost-effective stress relief method for mechanical thinning, as well as adopting chemical etching after the mechanical process. Thorough studies are included in Chapter 3.

Next, the challenges of adopting conventional interconnect technologies for integrating UTCs and flexible substrates were discussed. The common challenges include the difficulties of integrating high-density interconnects between UTCs and flexible substrates due to the mechanical and temperature requirements, and the complexity of multi-step processes. One-step printing technologies were introduced to overcome the difficulties presented by the conventional counterparts as a simpler, greener, and more economical alternative. Chapter 4 to Chapter 6 provide in-depth investigations of printed interconnects for UTC bonding.

Overall, this chapter discussed the long-standing challenges and current limitations for integrating UTCs and interconnects on flexible foils. The following chapters will demonstrate the developed, optimised, and novel processes to realise ultrathin Si IC-based FHE systems.

Chapter 3. Development of Ultra-thin Silicon-based Chips

The content of this chapter was adapted from the following published papers written by the author from the research undertaken during this Ph.D. work:

- Y. Kumaresan*, **S. Ma***, and R. Dahiya, "PMMA Sacrificial Layer based Reliable Debonding of Ultra-Thin Chips after Lapping," *Microelectronic Engineering*, vol. 247, p. 111588, 2021, doi: https://doi.org/10.1016/j.mee.2021.111588 (* Equal contribution).
- **S. Ma**, Y. Kumaresan, A. S. Dahiya, L. Lorenzelli, and R. Dahiya, "Flexible Tactile Sensors using AlN and MOSFETs based Ultra-thin Chips," *IEEE Sensors Journal*, pp. 1-1, 2022, doi: 10.1109/JSEN.2022.3140651.
- **S. Ma**, Y. Kumaresan, A. S. Dahiya, and R. Dahiya, "Ultra-Thin Chips with Printed Interconnects on Flexible Foils," *Adv. Electron. Mater.*, p. 2101029, 2021, doi: https://doi.org/10.1002/aelm.202101029.
- **S. Ma**, A. S. Dahiya, X. Karagiorgis, and R. Dahiya, "Ultra-Thin Chips for High-Performance Semi-Transparent Flexible Electronics," in *2023 IEEE International Conference on Flexible and Printable Sensors and Systems (FLEPS)*, 9-12 July 2023, pp. 1-4, doi: 10.1109/FLEPS57599.2023.10220424.

3.1 Introduction

Flexible hybrid electronics (FHEs) have garnered significant interest in recent years due to their ability to integrate printed electronics with silicon (Si)-based CMOS technology. This hybrid approach holds promise in harnessing the strengths of both technologies to create electronic systems that offer advantages such as high-speed connectivity, low data latency, expanded functionality, adaptable physical forms, and cost-effective manufacturing. These attributes are pivotal as they serve as the foundation for the ongoing shift toward a highly interconnected world characterised by widespread digitisation across numerous applications. However, the Si ICs manufactured by conventional CMOS technology are rigid and brittle, limiting the possibilities of being adopted in free-form electronics. Therefore, the ultra-thin

chip (UTC) technology has emerged as a key solution in leveraging the well-established CMOS technology to transform rigid Si ICs into flexible forms, while preserving device performance.

As introduced in Chapter 2, comparing different thinning technologies including their advantages and disadvantages, back grinding/lapping stands out for high throughput and good surface flatness of the desired thin wafers/chips. In comparison with back grinding, back lapping employs loose abrasive slurry instead of fixed abrasive wheels, which provides a gentler thinning process [111]. As a result, it is more effective than grinding for removing wafer waviness and offers a more uniform surface. Additionally, the stress generated at the material's surface results in less sub-surface damage, owing to the reduced plate speeds and lower applied loads on wafers/chips compared to back-grinding processes. Nevertheless, there is still pressure that can be induced in the Si crystal structure, limiting the final achievable thickness. Chemical and dry etching methods cause fewer crystalline defects as there is no mechanical pressure involved. Both etching processes can reduce more thickness than mechanical thinning but are more time-consuming. Dry etching operation is also more costly [37].

As the throughput and UTC thickness have become a trade-off amongst the bulk removal thinning processes, herein in this chapter, the mechanical and chemical thinning processes are combined to explore the minimum achievable thickness of UTCs. Additionally, handling of UTCs (< 50 μm thick), particularly after thinning, is a challenging task as the excessive stress could lead to cracking. Such damage could be prevented by restricting the stresses to acceptable levels. Herein, this chapter presents a novel, reliable and cost-effective method based on a polymethylmethacrylate (PMMA) sacrificial layer. The reliability of the presented lapping with the PMMA layer method has been confirmed repeatedly by showing negligible differences in device performance using chips with metal oxide semiconductor capacitors (MOSCAPs), aluminium nitride (AlN) pressure sensors and metal oxide semiconductor field effect transistors (MOSFETs). The reasons of these devices being selected in this study include:

a) after studying dummy silicon dies, MOSCAPs were firstly chosen due to their simple and well-understood structure to evaluate whether thinning would affect devices based on any capacitor-involved features; b) AlN based pressure sensors were then used to study whether the developed thinning process would cause any impact on silicon chips with thin film-based sensors (More explanations regarding the device mechanism are included in Chapter 3.4.2); c) at last, MOSFETs are employed as they are the fundamental building blocks of modern ICs and they provide a more comprehensive understanding based on the device performance, including analysing key parameters such as threshold voltage, transconductance, mobility, etc. Subsequently, chemical etching is adopted to further reduce the thickness of UTCs using tetra-methyl-ammonium hydroxide (TMAH) assisted with a reliable protective layer, ProTEK (Brewer Science). The electrical characterisation conducted before and after the 2-step thinning process has confirmed the reliability of the thinning process by showing negligible differences in the device performance.

3.2 Mechanical Thinning Methods and Materials

This section focusses on the development of the high-throughput mechanical thinning technique via lapping. The thinning process conducted in this work involves four steps: (1) Sample preparation; (2) Attachment of the sample to a holder with wax substrates; (3) Backside lapping; and (4) UTC removal from the lapping holder substrate.

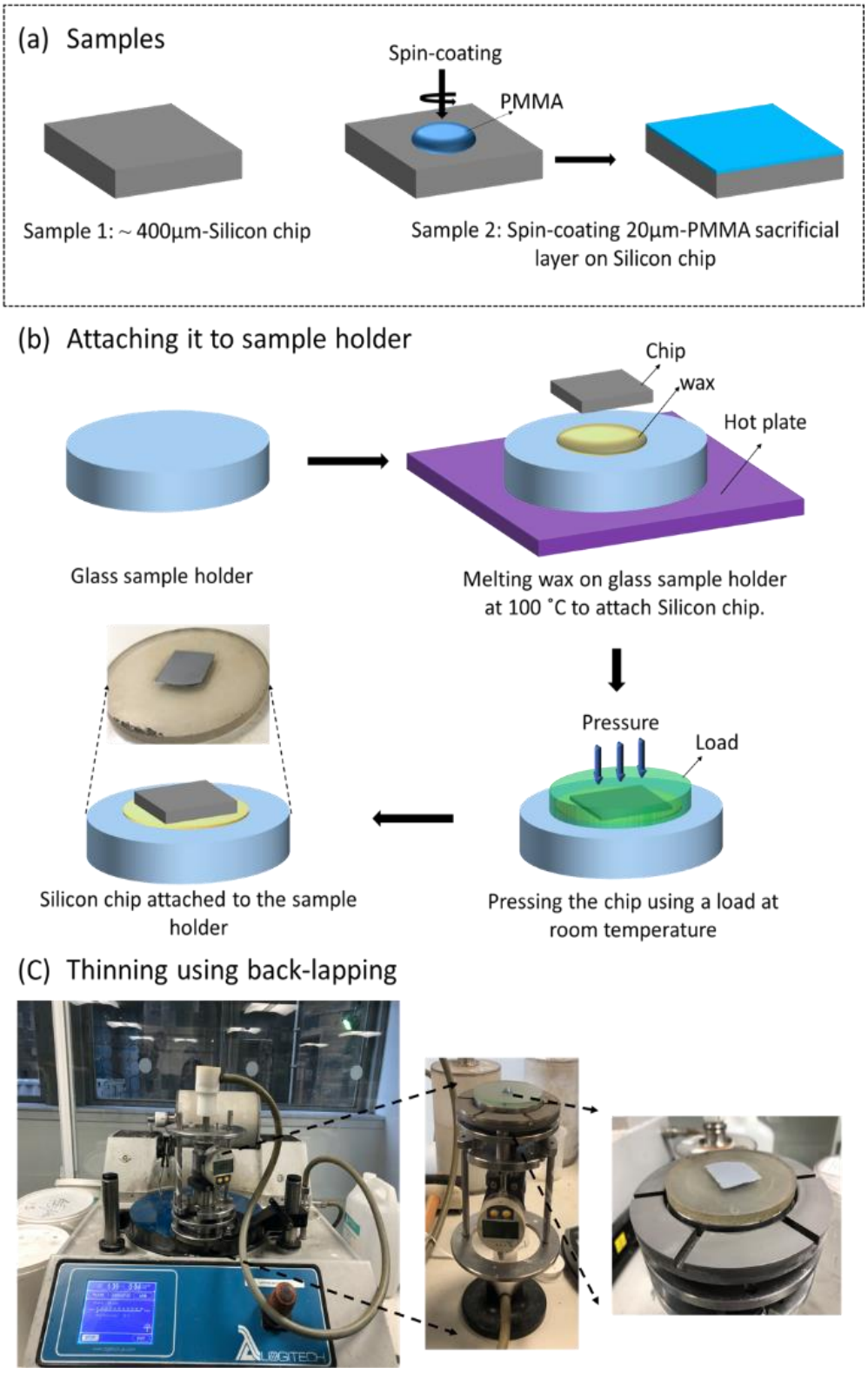

Figure 3-1. Schematic flow of the wafer/chip thinning process; (a) Sample preparation of sample 1 (the Si chip without any sacrificial layer) and sample 2 (the Si chip with the PMMA sacrificial layer); (b) Schematic flow of attaching the samples to the sample holder using wax; (c) Digital images of the backside thinning using a lapping machine, in which the sample on the sample holder is mounted on the jig (right corner).

Two Si dummy chips, each with a thickness, length, and width of ~400 µm, 2.5 cm and 2.5 cm respectively were used for the thinning process. As shown in Figure 3-1 (a), the pristine Si chip was considered as sample 1. Sample 2 was prepared by spin coating 15 wt% PMMA in anisole over the polished side (or on the device side for processed chips) at 1000 rpm to obtain a ~20 µm thick PMMA sacrificial layer. The PMMA layer acts as a sacrificial layer and serves the purpose of planarizing the sample as the manufactured wafers are usually not completely flat. After spin coating, sample 2 was baked on a hot plate at 100 ºC for 1 min.

Before initiating the backside lapping process, the two Si chips were attached to sample holders as chip carriers for thinning by placing the polished side (sample 1) or the PMMA side (sample 2) facing down using the quartz wax (Logitech), shown in Figure 3-1 (b), so that the exposed side of the chips (or the backside of the chips) would be the side being lapped. As the flatness/planarity of the UTCs is desired, tools that could potentially affect the flatness need to be checked for flatness using the planarity gauge before performing the thinning process, including tools that are in contact with the chips during thinning, such as the lapping plate and the glass holder. If the glass holder is not planar, then it needs to be lapped until the thickness variation becomes within 1 µm. If the lapping plate is not flat, a weighing block would be used to lap the plate. Next, attaching the chip on the glass holder via wax is needed to firmly hold the chip during lapping. Subsequently, the sample carriers with bonded chips were placed under the contact pressure equipment at room temperature for 30 min to ensure an even spreading of the wax and a solid bonding between the chip and the sample holder. After, the flatness of the wax distribution was observed by gauging the thickness of wax-bonded Si samples across various areas of their surface (for a 1 cm × 1 cm die, the thicknesses of each corner, midpoints of each corner, and the midpoint of the diagonals would be measured) using the contact profilometer.

The back lapping process was performed using a bench top PM5 Logitech precision lapping and polishing machine (Figure 3-1 (c)). Firstly, the glass sample holder was attached tightly to the lapping jig using vacuum. While lapping, a mixture of water and aluminium oxide (Al_2O_3) powder with the particle diameter of ~12 µm was utilised as the slurry to back thin the Si chip. The speed of the lapping plate was set to 25 rpm, and the thickness of the etched silicon was observed using the thickness monitor on the jig. The etch rate was determined by a combination of factors including the vertical force applied in the lapping jig onto the sample, the lapping plate rotational speed and the size of the alumina particles. In this work, the etch rate was measured to be ~10 µm/min.

After thinning, the sample was removed from the glass holder by placing it on a hot plate at 100 ºC to melt the wax. Once the wax was melted, the UTC was carefully detached from the glass sample holder (Figure 3-2). After this, the residual wax and PMMA were removed using acetone. After back-thinning, the critical challenge lies in the separation or removal of UTCs from the sample holder. Due to their fragile nature, the UTCs are prone to cracks and damages (Figure 3-2 (a)) and therefore the stress on the UTCs during the separation process needs to be carefully evaluated. In the industrial back-thinning process, UV tapes are used to encapsulate and protect the semiconductor devices on Si wafers from impurities and/or damage. The adhesion between Si wafers and UV tapes is controlled by irradiating UV light. After thinning, the removal of UV tapes from thin wafers is conducted by reducing the adhesion strength of these tapes through UV irradiation. However, these tapes are costly and therefore lead to a higher manufacturing cost of UTCs. For example, 2 ml of PMMA needed here would cost ~$ 0.1, which is much lower than the cost of UV tape for a 6-inch wafer (~$ 1). Recent reports also highlighted the issue regarding the increase in overall UTC manufacturing cost due to the adoption of UV tapes [112].An economical alternative way of thinning is to attach the bulk Si chip to the sample holder using a wax layer. However, after

thinning, the wax needs to be melted at 100 ºC to remove UTCs from the sample holder, during which it could result in a greater stress, eventually damaging the UTCs. As a result, the use of wax for chips with thicknesses below 100 μm has become challenging. This is also evident from the experiments related to sample 1, which was attached directly to the wax and then thinned down to about 35 μm thickness. Multiple cracks were developed during the removal process from the sample holder (Figure 3-2 (a)) due to the thermal stress from melting the wax and possibly residue stress induced by the lapping process.

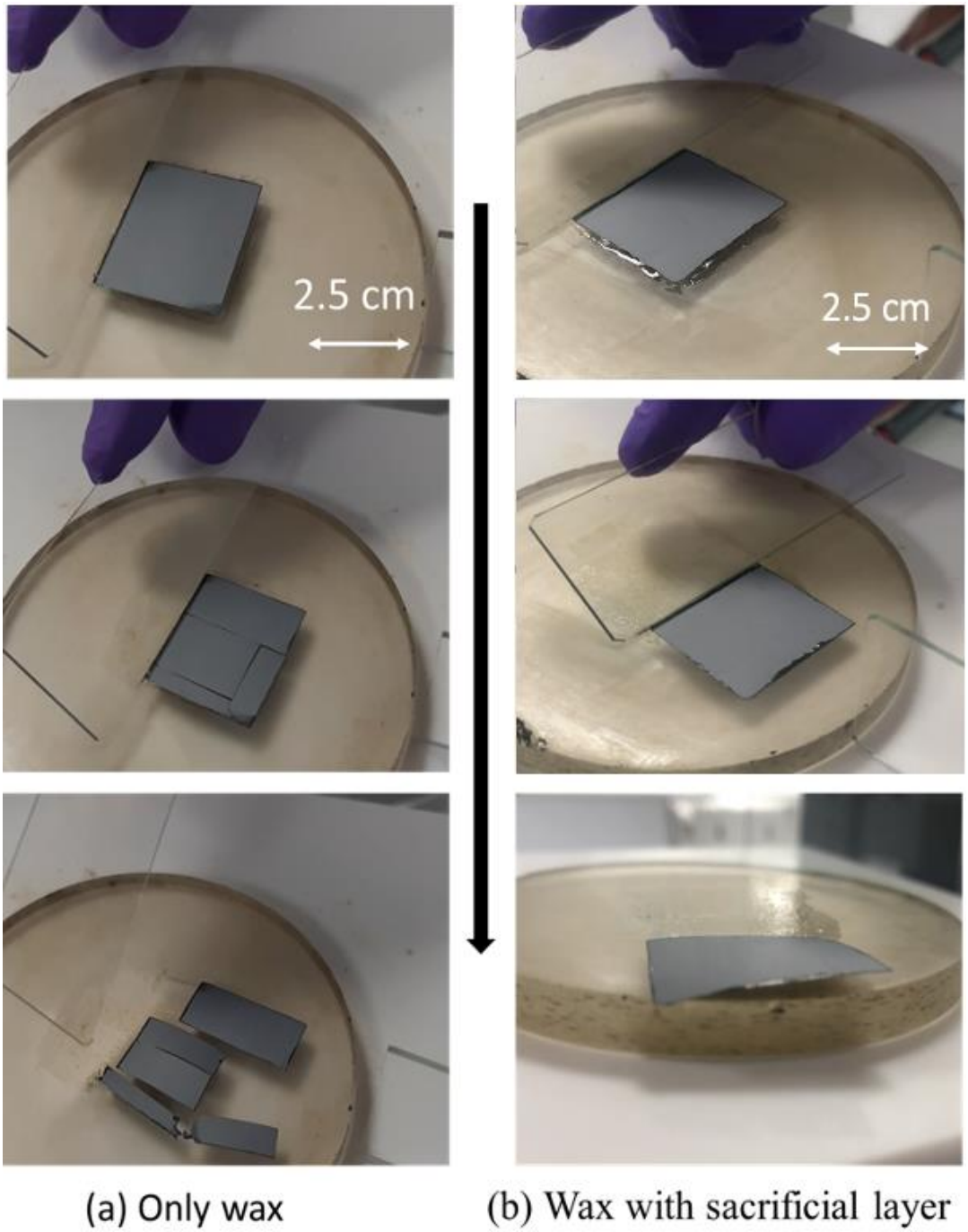

Figure 3-2 Image of UTCs during separation from the glass sample holder after lapping process; (a) Sample 1, silicon without sacrificial layer, and (b) sample 2, silicon with PMMA as a sacrificial layer.

The stress experienced during the separation of UTCs from the wax melting on the sample holder was investigated using COMSOL Multiphysics® (Figure 3-3). In the case of sample 1, the model was composed of the UTC with dimensions of 2.5 cm × 2.5 cm × 35 µm (length, width and height) placed directly above the wax with dimensions of 2.5 cm × 2.5 cm × 5µm

(length, width and height). With the temperature of 100 ºC applied to the model, the Von Mises stress of 2.58×10^6 N/m^2 was developed at the interface between the wax and the UTC. In addition, a thermal expansion of the chip was also observed (Figure 3-3 (a)). Therefore, introducing an additional layer to relieve the thermal stress at the interface between wax and the UTC has been explored.

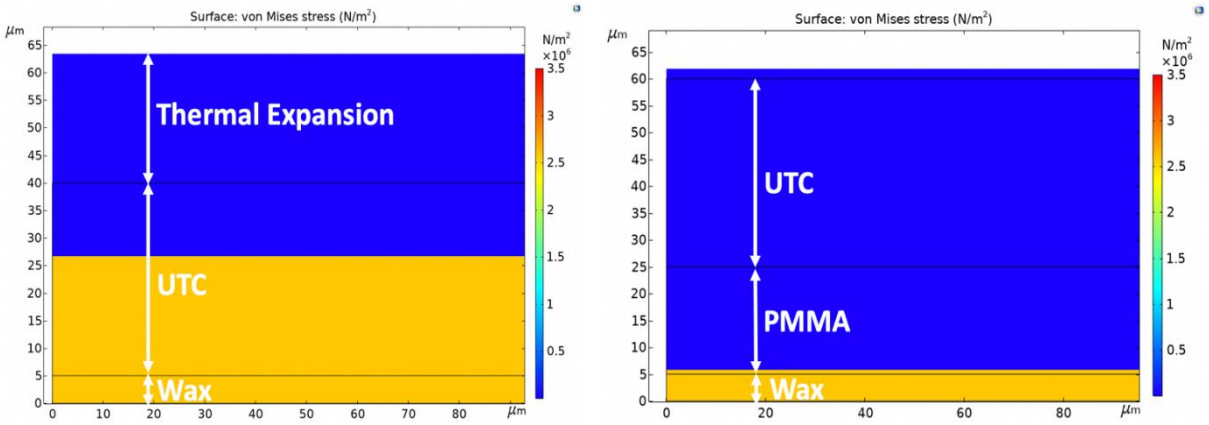

Figure 3-3. Simulation results obtained from COMSOL comparing the stress distribution of UTCs without and with a sacrificial layer, stating high stress level in the case of UTC directly bonded with wax and high warpage level indicated due to thermal stress; (a) UTC without any sacrificial layers; (b) UTC with PMMA as the sacrificial material.

Thermally insulating layers could be used to reduce the temperature-induced stress on UTCs during the separation process [113]. In this regard, sacrificial materials such as SU-8 photoresist, polyimide (PI), silicon dioxide (SiO_2), polycarbonate (PC) and PMMA were selected and simulated in COMSOL Multiphysics®. In the case of UTCs with a sacrificial layer, the model composed of an additional sacrificial layer with dimensions of 2.5 cm × 2.5 cm × 20 µm (length, width and height) placed in between the wax and the silicon chip (Figure 3-3 (b)). Accordingly, the Von Miss stress was predicted at 100 ºC for the selected sacrificial layer (Table 3-1).

Table 3-1. Sacrificial Materials Comparison.

Materials	SiO_2	SU-8	PI	PC	PMMA
Young's modulus	74GPa [114]	4.02GPa [115]	4.0GPa [116]	2.3GPa [117]	3.1GPa [118]
Removal Method	Wet/Dry Etching [119]	Wet/Dry Etching [120]	Dry Etching [121]	Dioxane [122]	Acetone [123]
Von Mises Stress (N/m^2)	2.85×10^6	4.08×10^4	1.45×10^4	2.77×10^4	7.86×10^2

Based on the simulation, the model with PMMA revealed the lowest stress amongst the selected sacrificial layer materials. Besides, a protective layer with lower stiffness and a relatively low Young's modulus (the ratio of the stress to the material and the resulting strain) is preferred. This is because when the melted wax starts to drag the polymer layer, the polymer chain with low Young's modulus has multiple degrees of freedom, guiding the polymer to deform at the wax interface without any significant changes at the UTC interface. In this regard, PC and PMMA have relatively lower Young's modulus [114, 116-118, 124]. However, PC is 30% more expensive than PMMA, potentially increasing the cost of the process [123]. Finally, the sacrificial layer needs to be removed after the removal of UTCs, and in this regard, an easy removal method is preferred. PC and PMMA can be simply dissolved in a chemical solution [122]. In conclusion, considering low Von Mises stress (materials experience plastic deformation when the Von Mises stress exceeds their yield strength), low Young's Modulus, easy removal method and low cost, PMMA stands out as the preferred sacrificial material. Compared with the UTC without any sacrificial layer, the

stress over the polished side of the chip is drastically reduced from 2.58×10^6 N/m^2 to only 786 N/m^2 with the use of PMMA as a sacrificial layer (Figure 3-3).

To prove the hypothesis, sample 2 (~35 µm-thick UTC after thinning assisted with a PMMA sacrificial layer) separation from the glass substrate was also conducted. In this case, a 20µm-thick PMMA layer was used as a thermal insulating sacrificial layer before bonding to the bulk chip. The thinned Si chip was successfully separated by using the glass slide, following similar steps as for sample 1 (Figure 3-2 (b)). A minor warping was also observed. Compared with sample 1 (Figure 3-2 (a)), it was evident that the PMMA layer protected the UTC during the separation process. The thickness of the PMMA layer also played a critical role in the successful separation of the UTCs. In is study, 20 µm-thick PMMA layers were used, but by increasing the thickness, it may be possible to further reduce the warping of UTCs caused by thermal stress. To achieve thicker PMMA, multiple spin coatings or a lower spin coating speed could be performed. Other factors during thinning could be manipulated to further reduce the warpage caused by the mechanical stress induced by thinning, such as a lower lapping plate rotation speed and/or a smaller slurry size. However, this minimal warpage observed does not affect future post-processing, which will be shown in the following chapters.

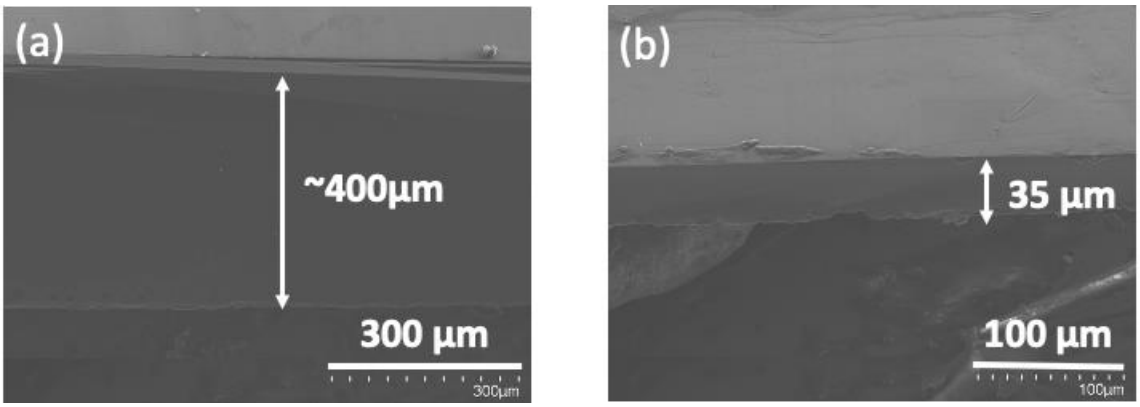

Figure 3-4. SEM images of silicon chips; (a) Silicon chip with original thickness of 400µm. (b) Thinned chip with a thickness of 35µm.

The thickness and surface morphology of UTCs were observed using the cross-sectional scanning electron microscope (SEM) of the bulk silicon chip and the UTC (Figure 3-4). It can be concluded from SEM images (Figure 3-4 (a)) that the thickness of the bulk silicon sample, ~400 µm, was reduced to 35±0.6 µm (Figure 3-4 (b)) after the successful thinning process. The flexibility of the UTCs was also investigated using 3D printed concave-shaped test rigs with a radius of curvature of 40 mm, 20 mm, and 10 mm (Figure 3-5 (a) – (c)). In the case of 40 mm and 20 mm bending, the UTCs could conform to the concave-shaped test rigs without any cracks (Figure 3-5 (d) and (e)). However, the UTC broke into multiple pieces when subjected to 10 mm bending radius as shown in Figure 3-5 (f). The strength of UTCs is dependent on the thinning techniques. For instance, UTCs developed by reactive ion etching, with thicknesses ranging from 15 to 20 µm, exhibit remarkable strength, reaching 2.34 GPa, allowing them to tolerate bending down to a minimum radius of 2.5 mm. In contrast, UTCs produced through grinding and polishing can be flexed to a minimum radius as wide as 33 mm [125]. In this case, standalone UTCs could tolerate up to 20 mm radius of bending. It can be concluded that, despite mechanical pressure involved in the thinning process, the PMMA sacrificial technique as a stress relief method helped reduce defects that could lead to residual stress. Nevertheless, 20 mm bending radius is adequate for many emerging applications in flexible electronics (the bending radii required for wearables used for human body parts, such as arms and legs, are 50 to 75 mm) [126].

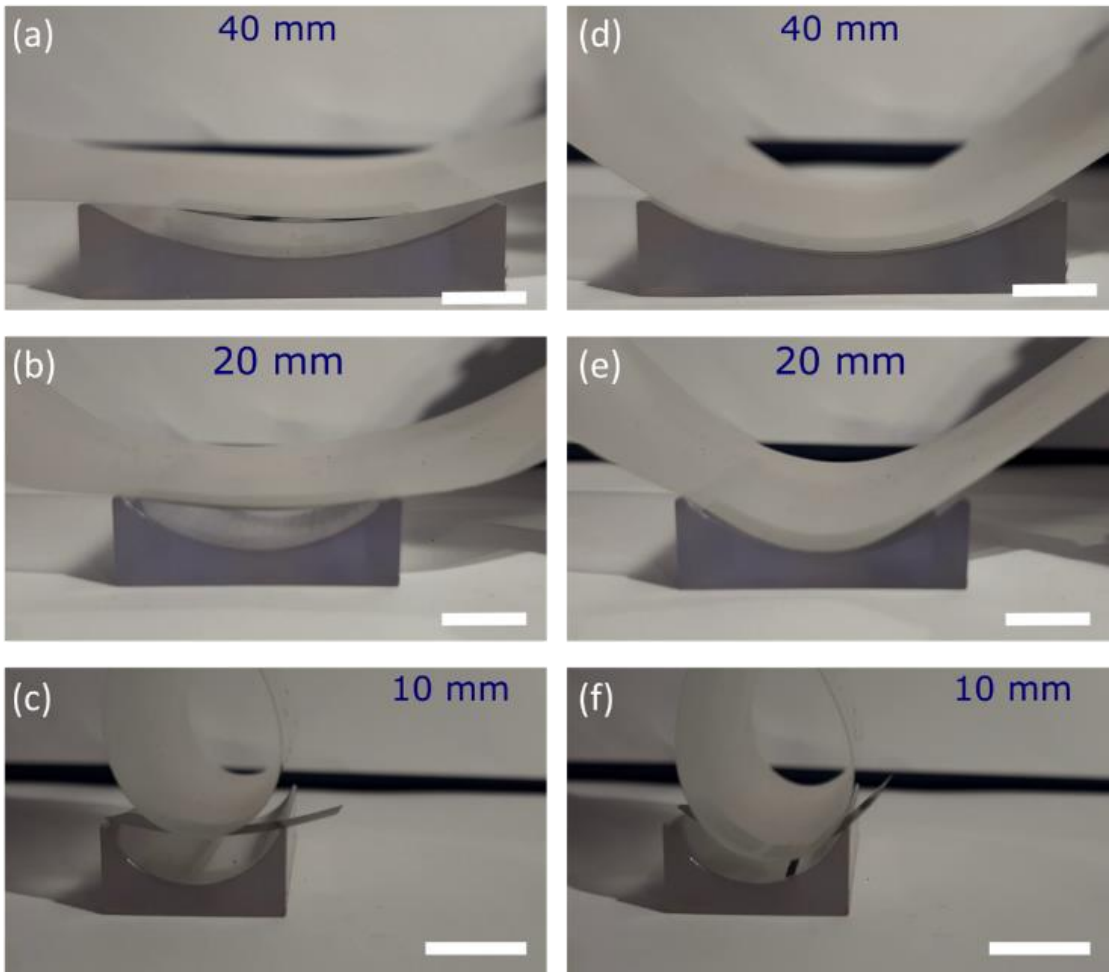

Figure 3-5. The bending tests: UTC placed flat on top of 3D printed bending test rig with bending radius without bending (a) 40mm; (b) 20mm; and (c) 10mm; and UTC showing flexibility under (d) 40mm and (e) 20mm bending radii; (f) UTC broken into pieces under 10mm bending radius. The scale bar is 10mm.

3.3 Chemical Etching Methods and Materials

As discussed above, the lapping process involves mechanical force, and the thinnest optimum thickness achievable by this process is concluded to be 35 µm. As discussed in Chapter 2.1.2, a stress-relief method such as wet or dry etching can be used to further reduce the UTC thickness. As dry etching operation is more costly and time-consuming than wet etching, wet etching is adopted in this work. During etching, a protective layer is required to cover the front side of UTCs to avoid device damage on the front side caused by the etchant. Before etching,

the protective layer needs to be spin-coated on UTCs to ensure uniformity and planarity. However, UTCs with 35 µm thickness tend to indent on the spin-coater once the vacuum is turned on, even with the smallest chuck. In that case, the spin-coated layer would not be uniform. Therefore, in this study, UTCs with 50 µm thickness were firstly obtained by the lapping assisted with the PMMA sacrificial technique, and subsequently chemical etching using tetra-methyl-ammonium hydroxide (TMAH) was used to explore the minimum achievable thickness (Figure 3-6 (a)). TMAH was selected in this work due to its excellent anisotropic etching characteristics.

Before chemical etching, ProTEK B3 primer (Brewer Science) was firstly spin-coated on the front side of UTCs (50 µm thickness) at 1500 rpm with 10,000 rpm/s acceleration for 60s. After soft-baking UTCs coated with the primer layer on a hot plate at 205 ˚C for 60 s, ProTEK B3 protective coating was spin-coated at 1000 rpm for 60 s with an acceleration of 5000 rpm/s. UTCs were then transferred to glass slide carriers and baked on a hot plate at 140 ˚C for 120 s, followed by 205 ˚C for 60 s (Figure 3-6 (b)). Next, chemical etching was conducted using 30 ml of 25 wt.% TMAH in a pre-heated water bath at 80 ˚C. At last, UTCs were removed from the glass carrier and ProTEK coating was dissolved in the ProTEK remover and DI water.

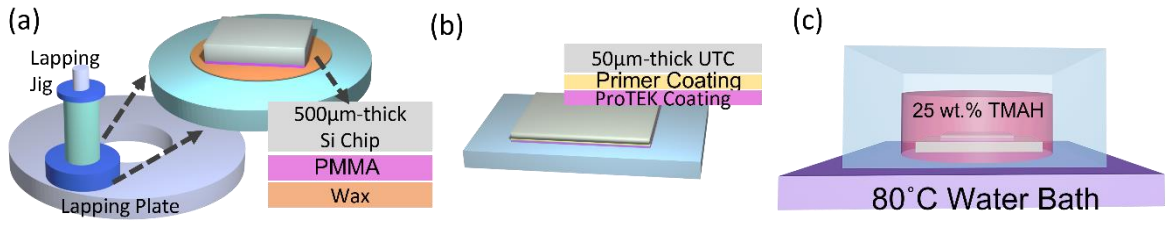

Figure 3-6. 2 step process schematics of realising UTCs: (a) Mechanical thinning by backside lapping; (b) Sample preparation for chemical etching; (c) Chemical etching using 25 wt.% TMAH.

Firstly, the thinning rate and the minimum achievable thickness of UTCs were explored. With the optimised mechanical lapping process, the thinning rate was ~10 µm/min to achieve 50

μm-thick UTCs. As can be seen in Figure 3-7 (a), the change in the UTC thickness at different etching times was recorded to investigate the chemical etch rate in this case. The obtained result shows an almost linear function with an etch rate of approximately 0.4 μm/min. After 120 min of chemical etching, the UTC thickness becomes ~2 μm (Figure 3-7 (c)). Overall, ~500 μm Si chips can be thinned down to ~2 μm within 3 hr by combining the mechanical lapping and chemical etching.

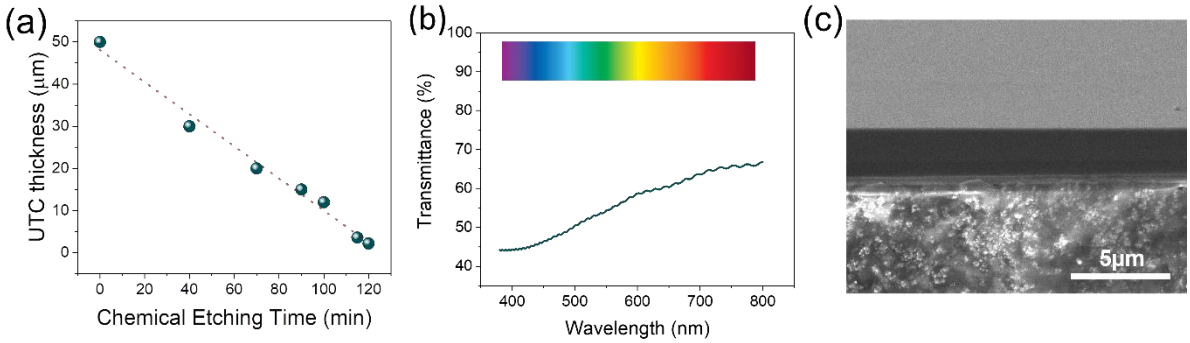

Figure 3-7. (a) Plot of UTC thickness after chemical etching for different periods of time; (b) Plot of ~2μm-thick UTC transmittance vs wavelength in the visible spectrum; (c) SEM image of UTC after thinning, ~2μm.

Because of the different absorption coefficients of Si under different wavelengths, Si becomes optically transparent with the reduction in its thickness. As the absorption coefficient of Si decreases towards the red region, the transmittance of Si increases accordingly. The spectroscopic study was carried out using Shimadzu UV2600 spectrophotometer. Figure 3-7 (b) shows the plot of UTC transmittance vs wavelength in the visible spectrum, indicating the transmittance ranging from 44% to 67%. Such property can be potentially used to monitor the thickness change of UTCs during chemical etching.

3.4 Device Evaluation after Thinning

To evaluate the effectiveness of the proposed thinning processes, processed Si chips were used to evaluate the device performance before and after thinning, including Si chips with metal-oxide-semiconductor capacitors (MOSCAPs), aluminium nitride (AlN)-based pressure

sensors, and metal-oxide-semiconductor field effect transistors (MOSFETs). Firstly, all three types of processed chips were studied to investigate the reliability of the developed mechanical thinning process. After, MOSFET chips were used for evaluating the 2-step thinning process.

3.4.1. MOSCAP

Firstly, the MOSCAPs were fabricated on a P-type Si/SiO_2 (490μm/300nm) substrate (Figure 3-8 (a) and (b)), which were designed and prepared by a former colleague, Dr. Yogeenth Kumerasan. The single chip (length = 2.5 cm, width = 2.5 cm, and thickness = ~490 μm) consisted of 8 × 5 arrays of MOSCAP devices (Figure 3-8 (c)). MOS capacitors are formed by sandwiching an insulator between a metal plate and a semiconductor. Applying voltages to the metal induces either positive (holes) or negative (electrons) charges on the semiconductor's surface. Oppositely charged charges gather on the metal plate, effectively creating a capacitor structure. To introduce bendability, the p-type substrate of the MOSCAP array was thinned down to ~35 μm through the back lapping process assisted with the PMMA sacrificial layer. Figure 3-8 (c) shows the array of MOSCAPs on a 40mm bending test rig and the cross-sectional SEM image of a single MOSCAP device displaying individual layers (metal, oxide, and semiconductor).

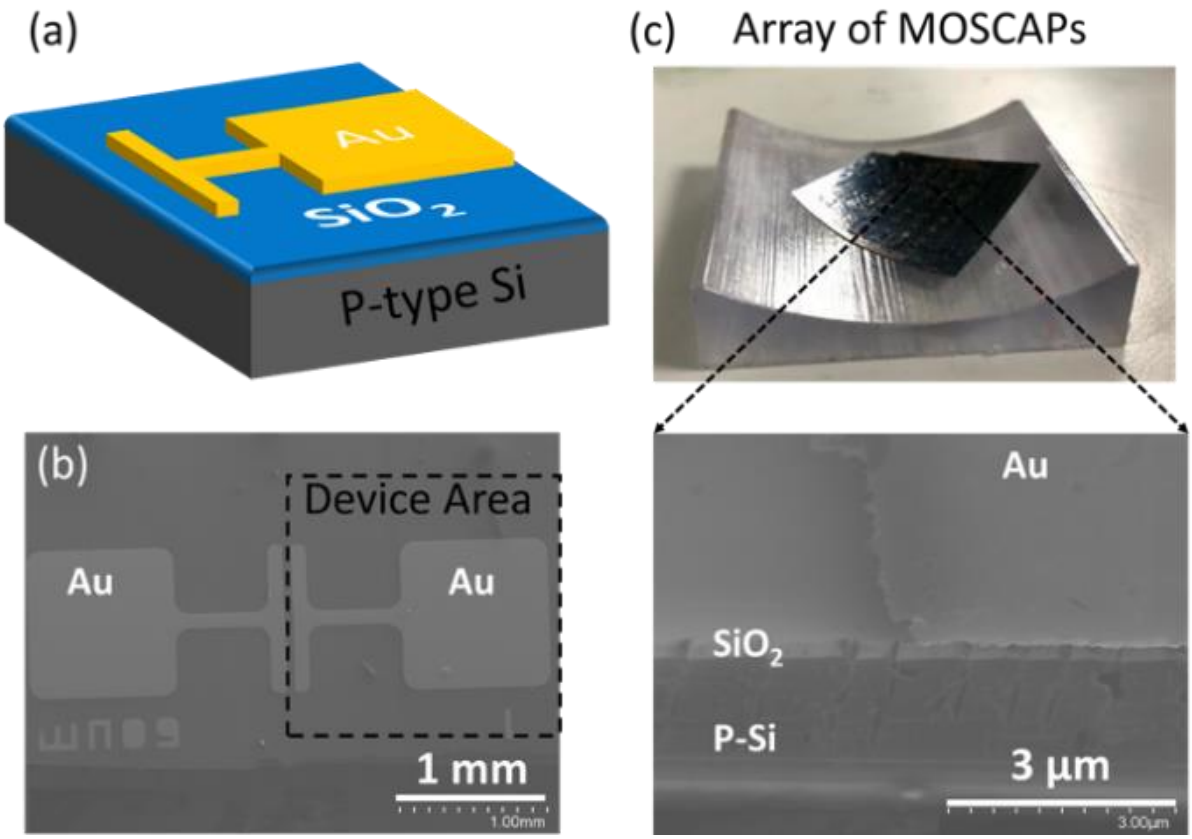

Figure 3-8. MOSCAPs thinning: (a) the schematic of MOSCAPs devices; (b) SEM image of the MOSCAPs before thinning; (c) Array of MOSCAPs after thinning.

To evaluate the effect of thinning on the MOSCAP device performance, the MOSCAP device was characterised before and after the thinning process (Figure 3-9). In addition, the flexibility of the MOSCAP device was evaluated by measuring the capacitance while the device was placed on a 40 mm bending test rig (Figure 3-9 (a) and (b)). The device demonstrated a stable capacitance value of 134 ± 10 pF (scan range from 0 to 2 V) under all three conditions, namely 1) before thinning, 2) after thinning and 3) under bending (Figure 3-9 (c)). From the capacitance-voltage characterisation (C-V plot), it is evident that the thinning process did not affect the device performance. Furthermore, the thinning of the MOSCAP chip introduced flexibility without any degradation in the device performance. In addition, a minimum device-to-device variation (< ± 10 pF) was observed, as shown in Figure 3-9 (d).

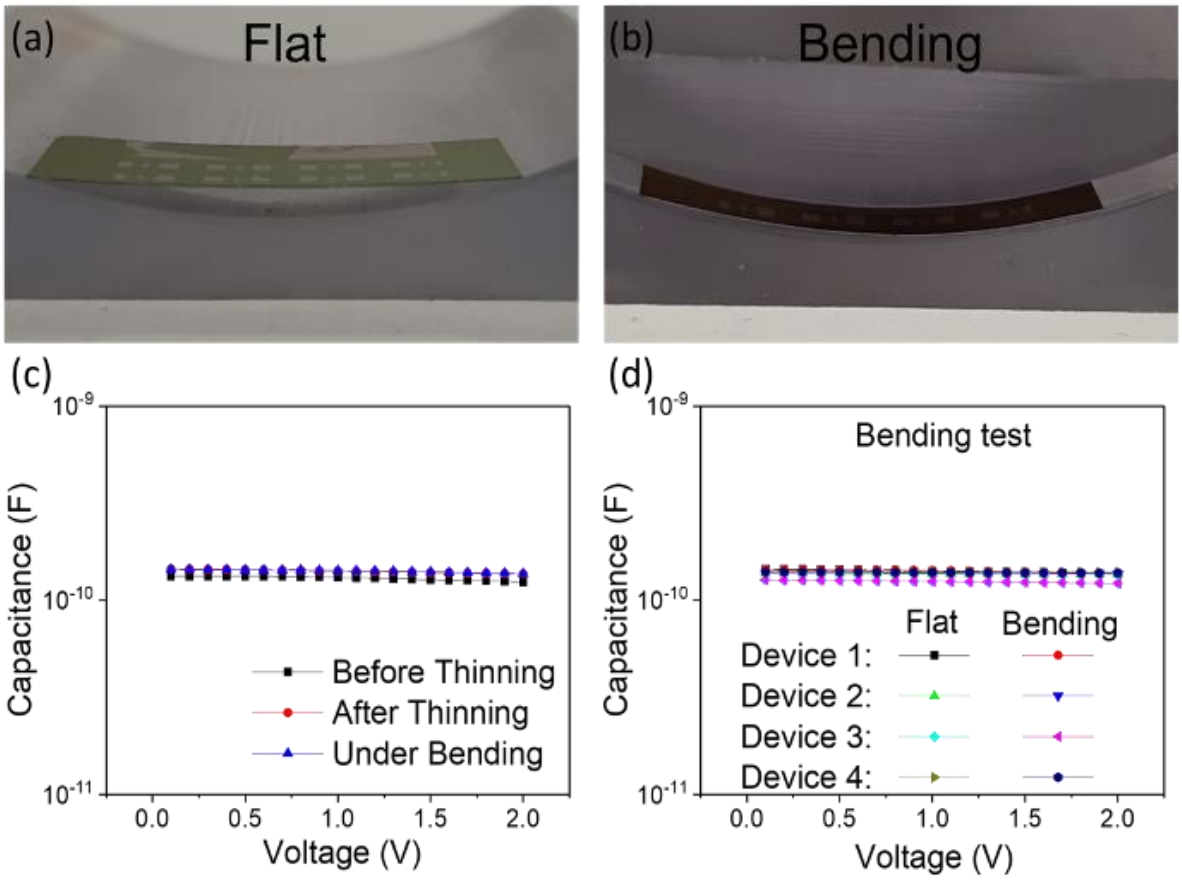

Figure 3-9. Processed chip with array of MOSCAPs device. The image of 8 x 2 array of MOSCAPs mounted on 3D printed bending tool under (a) flat and (b) 40mm bending state; (c) Comparison of C-V plot of MOSCAP device before and after thinning and under bending; (d) C-V measurement under flat and bending state for four devices.

3.4.2. AlN

In this section, processed Si chips with AlN-based piezoelectric pressure sensors were used to study the effect of thinning on devices composed of thin sensing films. Si-based AlN chips were provided by a collaborator. Chips with AlN pressure sensors were thinned down to 35 µm thickness using the lapping assisted with the PMMA sacrificial technique (Figure 3-10 and Figure 3-11 (a)) and the device performance was studied as follows:

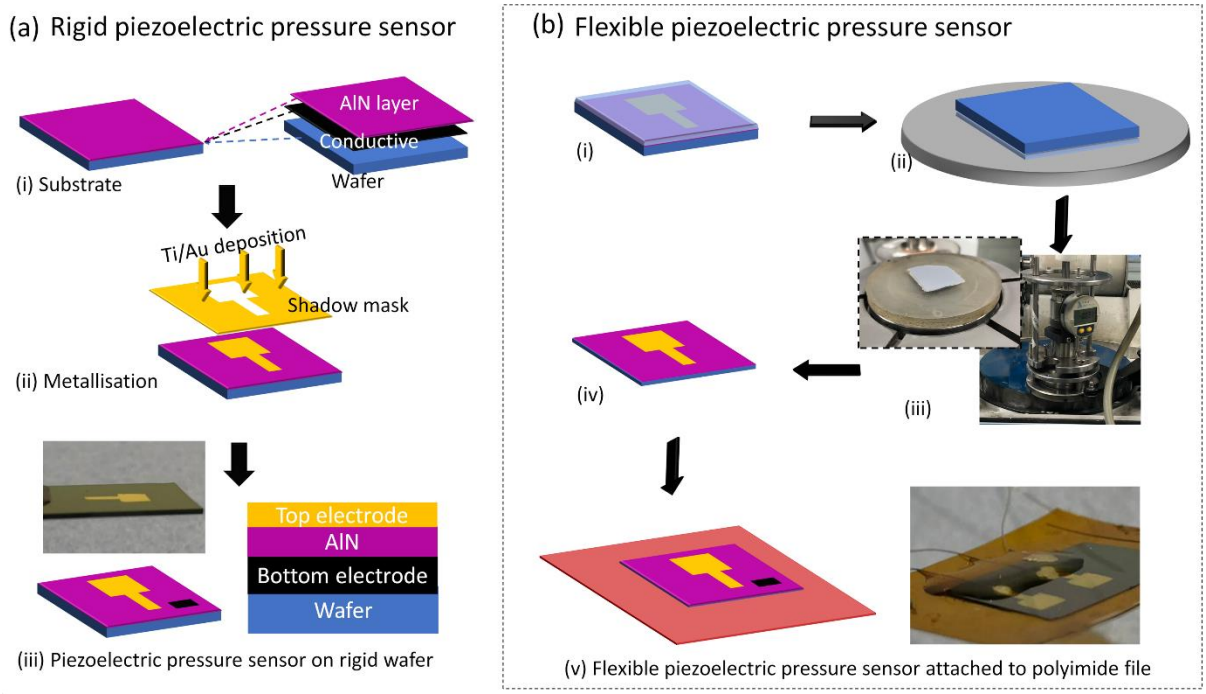

Figure 3-10. Schematic illustration of the fabrication of rigid and flexible piezoelectric pressure sensors.

AlN-based piezoelectric pressure sensors were characterised using a 1004 aluminium single-point low-capacity load cell with a linear motor controlled through a custom-made LabView programme (2018 Robotics v18.0f2, National Instruments, Texas, USA). The output piezopotential was measured by a digital multimeter (Agilent 34461A). The sensing performances of both bulk and UTC-based devices were evaluated and compared regarding the capacitance and sensing response. Given that the AlN pressure sensor shares the same structure as MOSCAPs (metal-insulator-metal), the initial stage of experimentation involved testing capacitance. The measurement of capacitance before and after thinning indicated similar values (Figure 3-11 (b)). Further, to evaluate the sensing response, an external force (0.1 N) was applied on both bulk and UTC-based AlN devices at 0.1 Hz and 0.5 Hz (Figure 3-11 (c) – (f)). The operational concept behind a piezoelectric pressure sensor relies on the transient generation of electric charge when subjected to an external mechanical stress. When a vertically compressive force is applied, an electric polarisation (potential) is induced in the AlN

sensing layer, owing to the relative displacement of the centres of the cations and anions in the AlN, resulting in a microscale dipole moment. Due to the generated electric field, charges accumulate at the top and bottom electrodes. While the pressure or force remains constant, free charges with opposite polarities are attracted to the surface (screening effect) and thus, a new equilibrium is reached. This leads to a rapid decrease in the piezo output, which eventually reaches zero. When the force is released, the piezoelectric polarisation disappears, giving rise to a negative peak (charges flow in backwards direction to achieve the new equilibrium). Consequently, the continuous application and release of compressive stress lead to the generation of alternating voltage. [127].

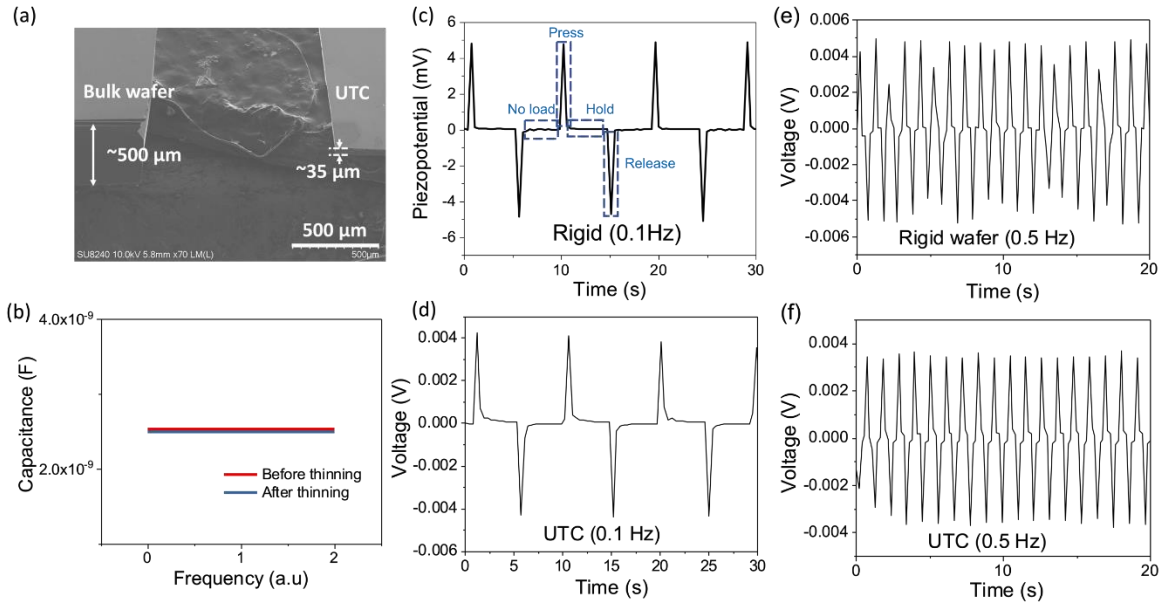

Figure 3-11. AlN-based piezoelectric pressure sensor characterisation: (a) SEM image showing the thickness comparison between the bulk and thinned chips; (b) Capacitance characterisation before and after thinning; (c) and (d) Bulk and ultra-thin AlN chip under 0.1N at 0.1Hz; (e) and (f) Bulk and ultra-thin AlN chip under 0.1N at 0.5Hz.

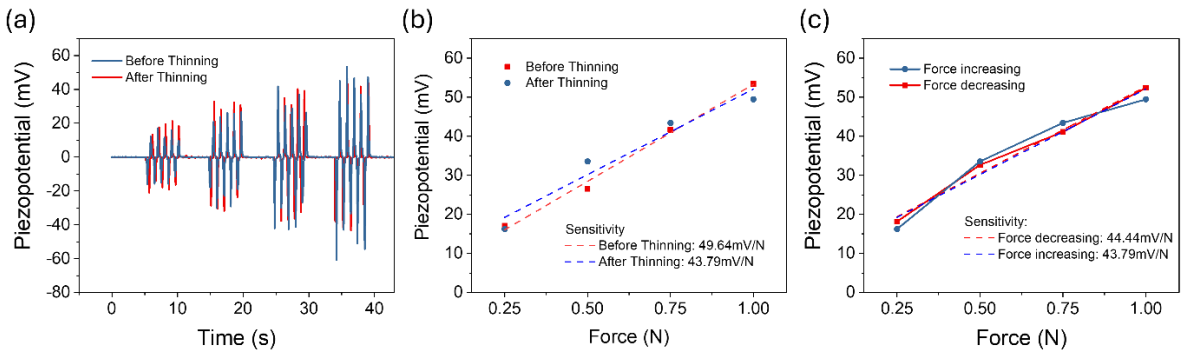

Figure 3-12. The response of AlN piezocapacitors for both bulk and thinned samples: (a) Under different applied forces; (b) Comparison of sensitivities; (c) Hysteresis test for UTC-based AlN piezocapacitor.

Next, a continuous force was applied to both bulk and UTC-based AlN devices at 0.5 Hz frequency and the force was increased from 0.25 N to 1 N with a step of 0.25 N, as shown in Figure 3-12 (a). The result revealed a repeatable, stable, and fast response (< 100 ms, extracted from Figure 3-12 (a)) before and after thinning. Meanwhile, as the applied force was increased, a rise in piezopotential was observed. It is well known that for piezoelectric devices the voltage generated is directly proportional to the applied stress, as expressed in Equation 3-1.

$$V = \frac{dFt}{\epsilon_r \epsilon_o A} \qquad 3\text{-}1$$

where V is piezopotential, d is piezoelectric coefficient, F is force, t is thickness, ϵ_r is relative permittivity, ϵ_o is vacuum permittivity and A is area. Therefore, it is expected that the output voltage will be pressure-sensitive [128]. The sensitivities of the bulk and UTC-based AlN pressure/touch sensors were extracted from Figure 3-12 (a). The results indicate a slight increase in sensitivity by ~3.7% after thinning, from 42.16 mV/N to 43.79 mV/N (Figure 3-12 (b)). Furthermore, compared with previous research on tactile sensors using AlN thin films, the sensitivity (how much pieozopential can be generated per newton of force applied) of UTC-based AlN is drastically improved by almost six times i.e., from 7.37 mV/N to 43.79 mV/N. A hysteresis test for UTC-based AlN piezocapacitors was conducted by increasing and decreasing the applied force (Figure 3-12 (c)). The sensitivity extracted showed a negligible difference

(1.46 %) between the increase of force and decrease. Finally, the effect of device performance under bending was studied. Figure 3-13 demonstrates the characterisation results of thinned devices under the planar condition and under 40 mm bending, showing negligible changes. The results under planar and bending conditions compared with bulk devices prove the reliability of the developed thinning technique for realising UTC-based AlN piezocapacitors with good robustness, reliability, and sensitivity.

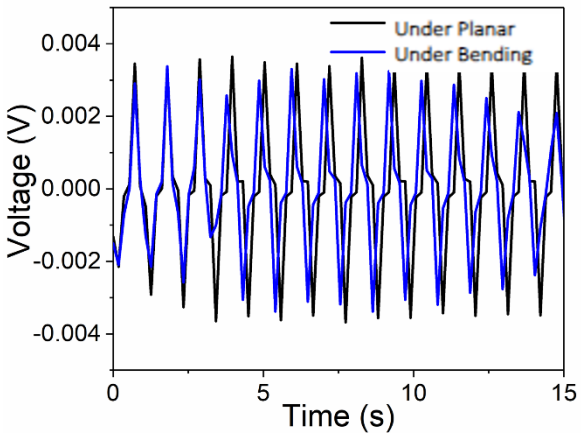

Figure 3-13. Performance comparison after thinning between under the planar condition and under bending.

3.4.3. MOSFET

To monitor the effect of chip thinning, in this section, chips with n channel MOSFET devices are used. Si chips with MOSFET devices were designed by a former colleague, Dr. Shoubhik Gupta, and fabricated by Fondazione Bruno Kessler, Italy. A n-MOSFET is usually a three-terminal device, consisting of a p-type semiconductor substrate with two n^+ regions, designated as the source and drain. The metal plate positioned on the oxide layer is referred to as the gate. After implementing lapping with the PMMA sacrificial material, 35 µm-thick Si-UTC with MOSFET devices were successfully developed (Figure 3-14).

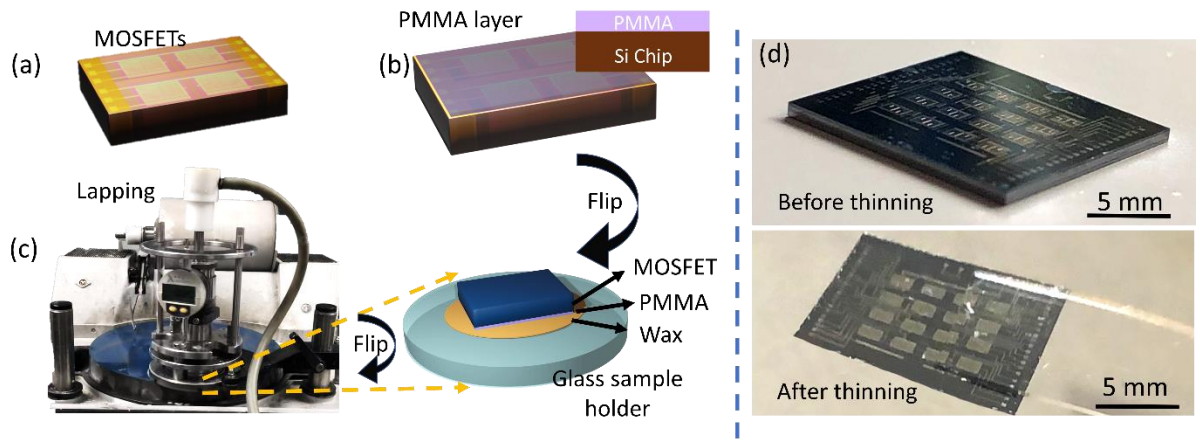

Figure 3-14. Schematic of realising ultra-thin Si-based MOSFET chips: (a)-(c) The developed and optimised lapping process assisted with PMMA sacrificial technique; (d) Optical images of the bulk MOSFET chip and UTC with MOSFET devices.

To monitor the device performance, the transfer and output characteristics of the MOSFET device were obtained before and after thinning using a Cascade Micro-tech Auto-guard probe station interfaced to a source measurement unit (B2912A, Keysight). To obtain the transfer (I_d – V_g) scans, the gate-source voltage (V_g) was swept from − 0.5 to + 1.75 V at drain bias (V_d) of 0.3 and 0.5 V (Figure 3-15 (a)). The family of output (I_d – V_d) scans were obtained by sweeping V_d from 0 to 1.75 V and V_g was incrementally stepped from 0 to 1.5 V with a step of 0.5 V after a full sweep of V_d (Figure 3-15 (b)). In the absence of a gate voltage, the source-to-drain electrodes represent two back-to-back p–n junctions. Consequently, the only current capable of flowing from the source to the drain is the reverse-leakage current. However, upon applying a positive bias to the gate, the MOS structure undergoes inversion, leading to the formation of a surface inversion layer (or channel) between the two n+ regions. Subsequently, the source and drain become linked by a conducting surface n-channel, enabling the passage of a substantial current. This channel's conductance can be adjusted by altering the gate voltage. From the output and transfer data, increasing V_g towards more positive values resulted in an increase of the drain current (I_d). This is typical of an n-channel MOSFET operation. Notably, the low-V_d region in the output scans ($V_d \leq \sim 0.1$ V) shows a linear dependence of I_d with

increasing V_d without any inflection point. When a small drain voltage is introduced, electrons will traverse from the source to the drain (resulting in a current flow from drain to source) via the conducting channel. Consequently, the channel acts as a resistor, with the drain current being directly proportional to the drain voltage. This behaviour of the device is typical of a MOSFET operating in the linear regime. As the drain voltage increases, it eventually attains V_{Dsat}, at which the thickness of the inversion layer reaches to zero, referred to as the pinch-off point. Beyond the pinch-off point, the drain current sustains a consistent level. This phase characterizes the saturation region. A clear I_d saturation with an increasing V_d was observed, showing excellent gate control over the semiconducting channel. The device characterisation before and after thinning presents negligible changes, as can be seen in Figure 3-15 (a) and (b). A quantitative comparison for key MOSFET performance parameters such as mobility, current on/off ratio, etc. is also made for before and after chip thinning and discussed and summarised in Table 4-2 in Section 4.2.3.

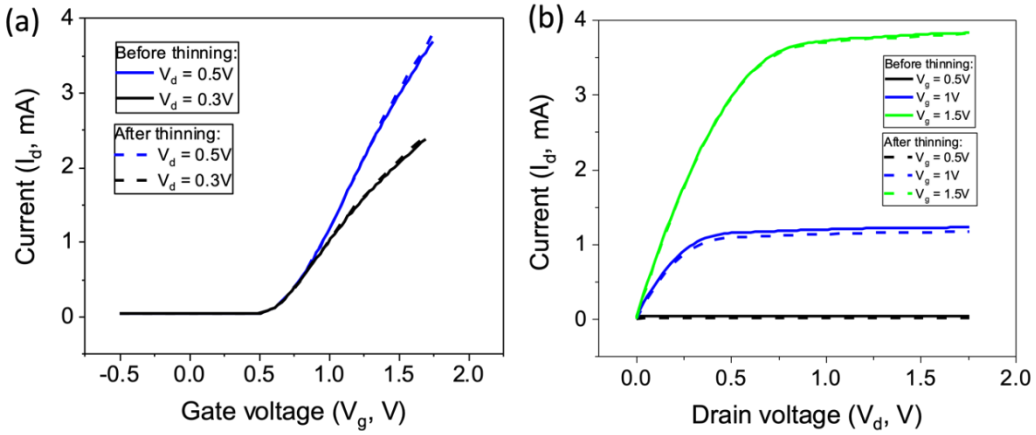

Figure 3-15. Device characterisation results: (a) Transfer function before and after thinning (down to 35 µm); (b) Output function before and after thinning.

Further, threshold voltage (V_{th}) and subthreshold swing (SS) values were extracted from the transfer curve (Figure 3-15 (a)). Firstly, V_{th} was extracted using the linear extrapolation method. For this, the linear extrapolation of $I_d - V_g$ intercepting the $I_d = 0$ axis gives the V_{th}

value. The SS values were extracted using the logarithmic transfer curve plot, based on Equation 3-2:

$$SS = \frac{\partial(logI_{ds})^{-1}}{\partial V_{gs}} \qquad 3\text{-}2$$

The difference in the device field-effect mobility (μ_{FE}) before and after thinning was also studied by firstly obtaining the transconductance (g_m), according to Equation 3-3 shown below:

$$g_m = \frac{\partial I_d}{\partial V_g} | V_d = constant \qquad 3\text{-}3$$

The extracted parameter was then used to calculate the field-effect mobility (μ_{EF}) using Equation 3-4 where W and L are the channel width and length (L is the distance between the two metallurgical n^+-p regions) respectively and C_{ox} stands for the oxide capacitance (W/L = 2000 µm/12 µm, thickness of SiO_2 = 50 nm in this work).

$$\mu_{FE} = \frac{g_m}{C_{ox}(\frac{W}{L})V_d} \qquad 3\text{-}4$$

The mobility and threshold voltage before and after thinning remain unchanged, 780 cm^2/Vs and 0.6 V respectively, showing that the lapping with PMMA sacrificial technique is reliable for UTC thinning and does not affect the device performance. Also, other important MOSFET performance-defining parameters stay constant, as shown in Table 4-2 in the next chapter, along with results after interconnect printing and under bending.

After confirming the reliability of the developed mechanical lapping process, the 2-step process combining both mechanical and chemical thinning was adopted to realise 20 µm-thick UTCs with MOSFET devices. MOSFET devices were electrically characterised before and after the two-step thinning process under ambient environment to investigate the effect of the thinning process on the device performance Figure 3-16. Table 3-2 shows the extracted key parameters of the MOSFET device before and after the 2-step thinning process, indicating insignificant

differences, and confirming the reliability of the proposed process. In this study, ~20 µm-thick UTC-based MOSFET devices are evaluated as it becomes more difficult to handle freestanding UTCs with a thinner thickness. Direct roll transfer printing could be explored to integrate UTCs with < 20 µm thickness onto flexible substrates [129].

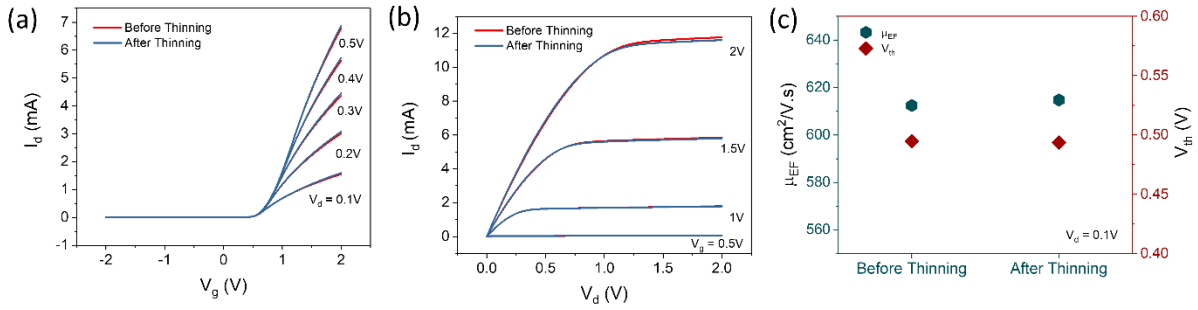

Figure 3-16. MOSFET electrical characterisation before and after thinning: (a) Transfer characteristics; (b) Output characteristics; (c) Extracted peak mobility (μ_{EF}) and threshold voltage (V_{th}) from transfer function at V_d = 0.1V.

Table 3-2. MOSFET Key Parameters Comparison

Condition	**V_{th} (V)**	**g_m (mS)**	**μ_{FE} (cm^2/V.s)**	**SS (mV/dec)**
Before thinning	0.49	1.56	612.43	242.35
After thinning	0.49	1.57	614.75	252.19
% change	0	0.64	0.38	4.06

3.5 Conclusions

This chapter presented the developed thinning process including mechanical and chemical techniques. Firstly, the PMMA sacrificial technique was introduced as a part of the mechanical lapping process to assist a simple and economical method for the removal of thinned silicon chips without causing any damage. The thinning and debonding processes of

UTCs with and without the sacrificial layer were compared through both experiments and COMSOL simulations. The PMMA layer protected the active device region from impurities or damage during thinning and transferring processes. Additionally, the use of the PMMA layer resulted in four orders of magnitude lower stress on UTCs during the UTC removal process after thinning. It revealed a stress-free method for the handling and transferring of UTCs without breakage. The distinctive features of the presented method are high reliability and cost-effectiveness (an order of magnitude cheaper) in comparison with conventional methods that use UV curable tapes. UTCs with approximately 35 µm thickness were successfully obtained by using the presented method. This fabrication approach takes advantage of PMMA's mechanical properties. Due to the simplicity of the method, there is promising potential for the presented approach to be employed in the large-scale manufacturing of UTCs. Furthermore, the processed Si chips with different devices including MOSCAPs, AlN-based piezoelectric pressure sensing and MOSFETs were thinned down to 35 µm thickness and demonstrated stable performances before and after thinning processes with enhanced flexibility.

Further, an efficient two-step thinning process by combining mechanical lapping and chemical etching was presented to realise semi-transparent (44% to 67% transmittance under visible spectrum) UTCs with ~2 µm thickness within 3 hr. UTC-based MOSFET devices with 20 µm thickness were evaluated before and after the optimised 2-step thinning process, revealing negligible differences in the device performance, and confirming the reliability of the process. The assessment of MOSFET devices based on ~20 µm-thick UTCs was conducted due to the increasing challenge of handling thinner freestanding UTCs. The possibility of employing direct roll transfer printing can be considered to integrate UTCs with a thickness of less than 20 µm onto flexible substrates.

As 35 μm-thick UTCs developed by the reliable and high-throughput lapping with the PMMA sacrificial technique have presented stable device performance and excellent flexibility (up to 20 mm bending curvatures), samples in the following chapters are all processed using this procedure.

Chapter 4. Printed Interconnects for FHE Systems

The content in this chapter was adapted from the followings:

- **S. Ma**, Y. Kumaresan, A. S. Dahiya, and R. Dahiya, "Ultra-Thin Chips with Printed Interconnects on Flexible Foils," *Adv. Electron. Mater.*, p. 2101029, 2021, doi: https://doi.org/10.1002/aelm.202101029.
- A. Christou*, **S. Ma***, A. Zumeit, A. S. Dahiya, and R. Dahiya, "Printing of Nano to Chip Scale Structures for Flexible Hybrid Electronics," *Adv. Electron. Mater.*, 2023, doi: 10.1002/aelm.202201116. (* Equal contribution: A. Chritou performed the direct transfer printing process and the cyclic bending. I conducted the chip thinning, substrate preparation, device characterisation and interconnect printing.)

4.1 Introduction

Following the introduction of flexible hybrid electronics (FHEs) in Chapter 1 and Chapter 2, and the development of the novel, effective thinning technique to realise ultra-thin chips (UTCs) in Chapter 3, reliable interconnects are another important element to the realisation of hybrid high-performance flexible electronic systems.

As discussed in Chapter 2, due to considerable differences in mechanical and thermal requirements, it is challenging to adopt conventional interconnect technologies to robustly connect the UTCs on flexible substrates with other printed devices. Conventional wire bonding approaches including thermocompression, thermosonic and ultrasonic bonding introduce mechanical force (ranging from 0.2 to 1.5 N) during bonding processes [42, 43, 46]. Besides, thermocompression and thermosonic bonding processes require high temperatures, 200 – 400 °C, whereas most of the polymeric flexible substrates become unstable at such high temperatures, leading to poor adhesion between the bond pad and the substrate and substrate deformation [39, 45]. Other traditional UTC interconnect technologies such as Flip Chip (FC) assembly and Through Silicon Via (TSV) have also been explored [25, 130, 131]. Their

common technological drawbacks involve the complexity and cost of the manufacturing process as well as challenges in testing. Considering these difficulties, the printing route is considered here for gaining access to UTCs. With printing technologies, it is possible to deposit conductive materials for electrical connections at lower temperatures. As a single-step additive approach, printing technologies are more straightforward and cost-effective than the conventional UTC interconnect techniques.

Driven by these motivations, this chapter presents a non-contact printing approach to realise reliable interconnects for FHE systems. Unlike contact-based printing methods such as offset lithography, gravure printing and flexography, the presented approach does not involve direct contact between the printing tool and the substrate, ensuring the prevention of any mechanical stress on the fragile UTCs [72]. Table 2-2 in Chapter 2.2 discussed the limitations of existing non-contact printing technologies including screen printing, inkjet printing, electrohydrodynamic (EHD) inkjet printing, aerosol jet printing (AJP), laser direct write (LDW) and extrusion printing. In the case of integrating and electrically accessing UTCs on flexible foils, the UTC thickness needs to be considered for the interconnects to be printed over its step height. Considering the challenges in electrically covering the step height as well as other technological limitations summarised in Table 2-2, the extrusion-based printing system therefore stands out as a potentially ideal technique for this application. Due to the printing mechanism and the compatibility with high-viscosity printing materials, conformal structures covering the thin chip's step height can be achieved by one-pass printing through the extrusion printing system (Table 4-1).

Table 4-1. Comparison between non-contact printing technologies for UTC interconnect.

Technologies	**Printing Resolution (µm)**	**Printing Directions**	**Number of Printing Layers to Cover a Step Height of >30 µm**	**Ref.**
Screen Printing	50 – 100	Horizontal	N/A	[72]
Inkjet Printing	20 – 50	Horizontal and Vertical	~20 – 100 layers (Line thickness = ~0.3 – 1.5 µm)	[78, 109, 132-134]
Electrohydrodynamic (EHD) Printing	1 – 10	Horizontal and Vertical	~40 layers (Droplet thickness = ~0.75 µm)	[135]
Aerosol Jet Printing (AJP)	< 10	Horizontal and Vertical	6-15 layers (Line thickness = ~2 – 5 µm)	[88, 89, 136, 137]
Laser Direct Write (LDW)	< 10	Horizontal and Vertical	35 layers (Voxel thickness = 1 µm)	[71, 93, 96]
Extrusion Printing	1 – 10	Horizontal and Vertical	1 layer	This work

Therefore, in this chapter, a new approach is introduced to realise interconnects for accessing devices on thin Si ICs by adopting the single-step extrusion printing technique. The high-viscosity silver (Ag) conductive paste (> 100,000 cP, 82 wt.% of metal), extruded from a high-resolution printer (1 – 10 µm line width), is used here to connect the Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) on UTCs (35 ± 0.6 µm thick) with the extended pads on flexible printed circuit boards (PCBs). The performance of extrusion printed interconnects is studied and evaluated along with the performance of transistors on thin Si chips. UTCs with MOSFET devices are developed using the high-throughput mechanical thinning technique presented in Chapter 3.2. The electrical characterisation is conducted after

interconnect printing and under bending. Further, a new approach for physically bonding UTCs is demonstrated by using direct transfer printing.

4.2 Electrical Bonding by Extrusion Printing

4.2.1 Materials and Methods

The electrical interconnects in this work were formed using a high-resolution extrusion printer (Delta printer by XTPL). Firstly, the nozzle opening size and ink material were selected considering the resolution and conductivity of the printed structures. The available nozzle opening sizes were 1.5, 3.5 and 5 µm diameters, which could directly affect the printing resolution and throughput. An approximately 1 µm feature size can be achieved as the highest resolution for this extrusion printing system. However, in the case of adopting printing techniques for UTC bonding, robustness and conductivity also need to be taken into consideration. To meet such criteria, interconnects with relatively larger features are required to lower the resistance and increase the fabrication throughput. It is easier to achieve this with a bigger nozzle size, and hence nozzles with the 5 µm opening size were selected in this work. The choice of ink also plays a significant part in the performance of the bonding structure as low-viscosity inks tend to spread on the substrate and lead to unstable electrical performance or even short-circuiting of pads. For UTC bonding, uniform and continuous printed conductive tracks are needed to connect the MOSFET chip with flexible substrates. As there is a step of 35 ± 0.6 µm between the chip and PCB, inks with a high viscosity are preferred. Accordingly, silver (Ag) nano-paste (XTPL CL85) with spherical Ag nanoparticles (35 – 50 nm diameter, 82 wt.% of metal, viscosity above 100,000 cP, measured at room temperature with a shear rate of 0.2 s^{-1}) was used. Ag as the chip bonding material has been widely explored because of its inherent properties such as high electrical conductivity, high thermal conductivity and high

melting point [138]. The metal content of CL85 is more than that of commercially available inks by 20 wt% (NPS-J from Harima, metal content: 62 – 67 %) [139]. As introduced in Chapter 2.2.2.5, considering the rheology for different ink/paste for DIW printing technologies, they usually exhibit non-Newtonian behaviour, which means that their effective viscosity does not remain constant and depends on the shear rate. In this case, the viscosity decreases as the nozzle diameter becomes smaller towards the tip and the shear rate increases under the influence of shear thinning. Therefore, the effective viscosity at the nozzle tip is orders of magnitude smaller. However, as commonly used Au or Ag-based paste is highly thixotropic, the viscosity of the ink or paste deposited on the substrate after printing can return to the initial viscous state. As a result, despite the wettability of the substrate, it is easier to achieve continuous electrical connections with a high aspect ratio using high-viscosity printing materials.

Regarding operating the system, the nozzle and sample need to be firstly placed in the designated positions, i.e., the ink cartridge and the printing stage, and the nozzle needs to be loaded with ink/paste. The printing angle between the nozzle and substrate was set to be at 55°. There are two important printing parameters adopted in this system, printing velocity and pressure respectively. The values applied for these parameters are highly dependent on the ink/paste properties, particularly their viscosity. For example, the Ag paste adopted in this work exhibits high viscosity (over 100,000 cP) and therefore relatively high pressure (7 bar) and low velocity (0.07 mm/s) are required to ensure continuous and conductive printed lines. In the case of using an inkjet printing compatible ink which usually exhibit low viscosity (less than 20 cP), such as nanosilica/epoxy ink used later in this chapter, a much lower pressure is adequate (3 bar). In all cases, with the increase of pressure and/or decrease of velocity, there would be more printing material. Therefore, the printing parameters can be manipulated for different intended structures.

4.2.2 Evaluation of Interconnects Formed by Extrusion Printing

The printed interconnects were firstly investigated on a planar spin-on polyimide (PI) substrate. More information of the selected PI is included in Chapter 4.3. Lines with varying lengths (20 – 1500 µm) were printed with different numbers of layers (1, 2, 3, 5 and 10 layers), as shown in Figure 4-1 (a). The geometric measurements were conducted using the contact profilometer, showing the thickness and width of lines formed with different numbers of printing layers (Figure 4-1 (b) and (c)). The resistance of all printed lines was also measured by probing the contact electrodes printed at both ends of the printed lines, indicating that it increases with the increase of line length, and decreases with the increment of the printed layers for the same length.

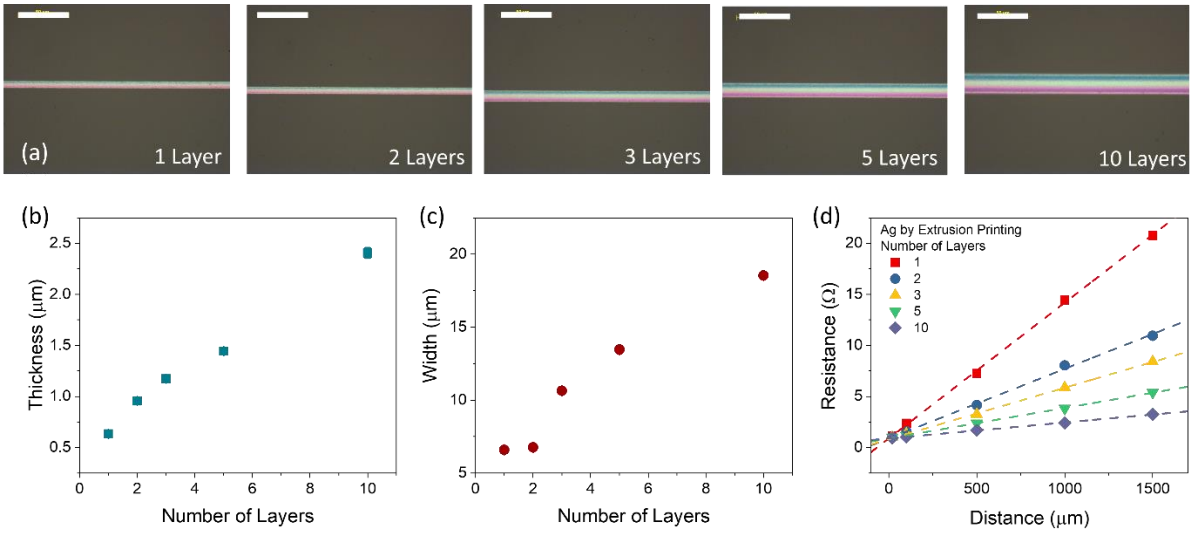

Figure 4-1. Interconnects formed by extrusion printing system: (a) Optical images of printed interconnects with different number of layers (1, 2, 3, 5 and 10), scale bar = 50 µm; (b) Thickness of printed interconnects vs. numbers of layers; (c) Width of printed interconnects vs. numbers of layers; (d) Measured resistance vs. interconnect lengths with different numbers of layers.

4.2.3 Evaluation of Device Performance after Bonding by Extrusion Printing

In this work, after obtaining 35 µm-thick UTCs with MOSFET devices using the mechanical lapping assisted with the PMMA sacrificial technique introduced in Chapter 3.2, UTCs were

then transferred and attached to a flexible printed circuit board (PCB) via a small amount of low-stress adhesive, EpoTEK 301-2 (Figure 4-2 (a)). Subsequently, high-resolution extrusion printing was adopted to realise the interconnects to access devices on UTCs. There was a step height (equivalent to the chip thickness + adhesive thickness) between the pads on the chip and the substrate. When printing the planar structures on chips and substrates, the printing parameters were set as 7 bar pressure and 0.07 mm/s velocity. However, when covering the step height, the nozzle needed to be shifted gradually along the Z-axis, and a much lower velocity was required (~0.01 mm/s). After printing, the printed structures were annealed at 150 °C for 15 min.

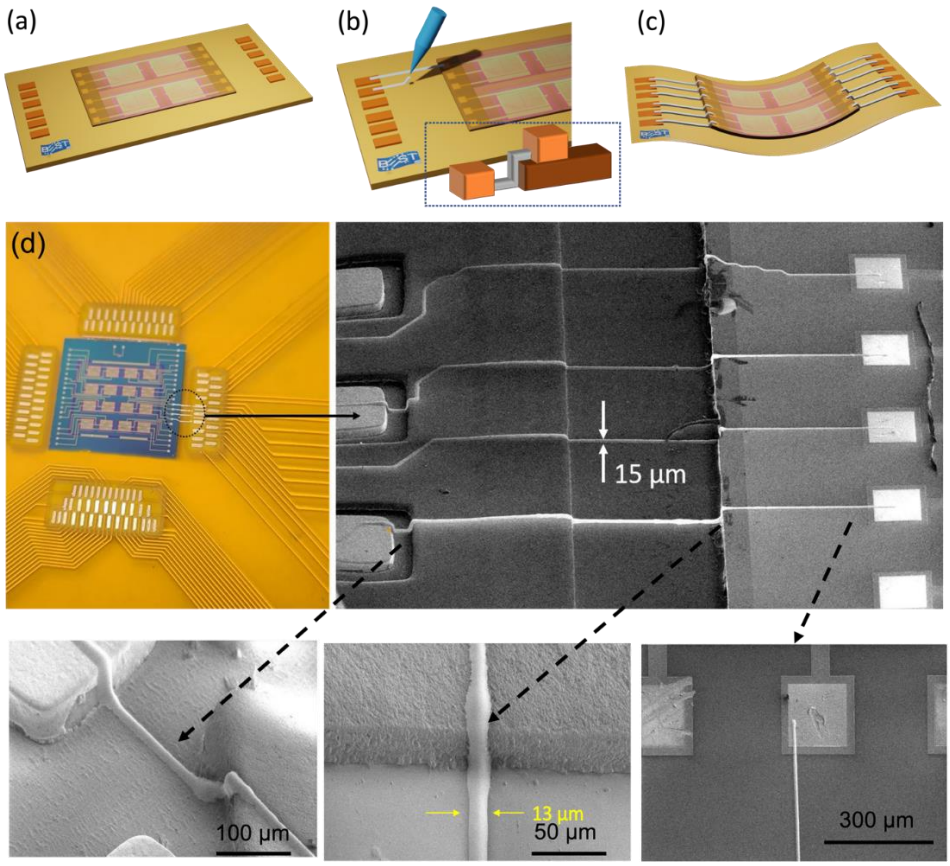

Figure 4-2. Schematic of realising printed interconnects for UTC electrical bonding on flexible PCB: (a) Thinned chip attached on flexible PCB; (b) Interconnects between the devices on the UTC and flexible PCB realised by extrusion printing of high-viscosity nano paste with a cross section scheme (inset); (c) Scheme of the realised flexible ultra-thin MOSFET chip; (d) Optical and SEM images of ultra-thin MOSFET chip attached on the flexible PCB with printed interconnects.

Next, the electrical characterisation was conducted using a Cascade Micro-tech Auto-guard probe station interfaced to a source measurement unit (B2912A, Keysight) under similar conditions as devices after thinning (discussed in Chapter 3.4.3). The transfer (Figure 4-3 (a)) and output (Figure 4-3 (b)) scans recorded to present the MOSFET device performance after thinning (before interconnect printing, electrical probes placed on the UTC) and after interconnect printing (electrical probes placed on the peripheral or extended contact pads on the flexible PCB). The key parameters including peak mobility (μ_{EF}), threshold voltage (V_{th}) and subthreshold swing (SS) were extracted using the same steps presented in Chapter 3.4.3. The extracted mobility values before and after bonding are shown in Figure 4-3 (c).

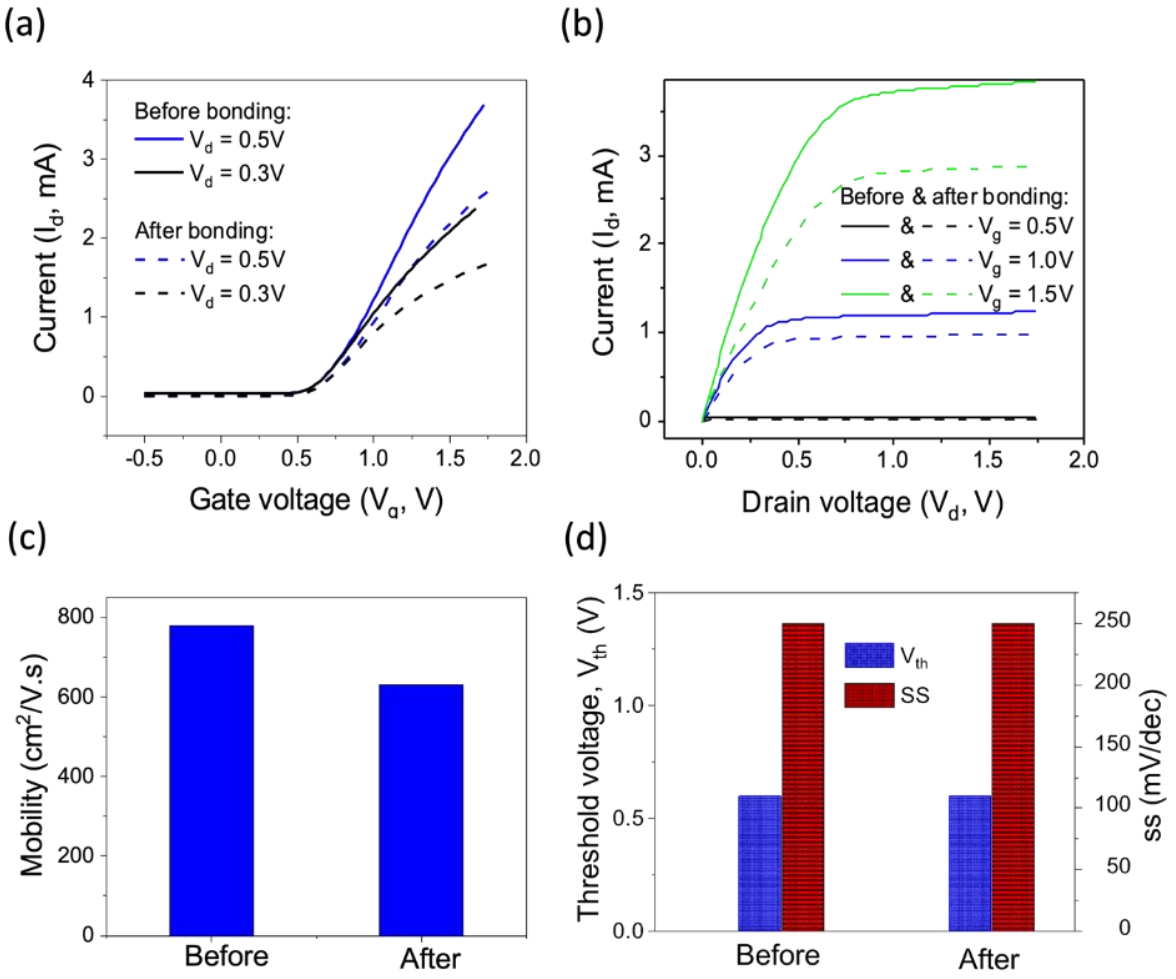

Figure 4-3. Device characterisation before and after bonding by printing: (a) Transfer functions; (b) Output functions; (c) Mobility; (d) Threshold and subthreshold voltages.

Compared with the characterisation results after thinning, the device performance demonstrated a minor decrease in drain current (transconductance) which resulted in the reduction of carrier mobility ($\mu_{FE} \approx 630 cm^2/Vs$ after bonding) although other device parameters such as V_{th} and SS. remained unchanged (Figure 4-3 (d)). The decrease in mobility after printing the interconnects is explained as follows:

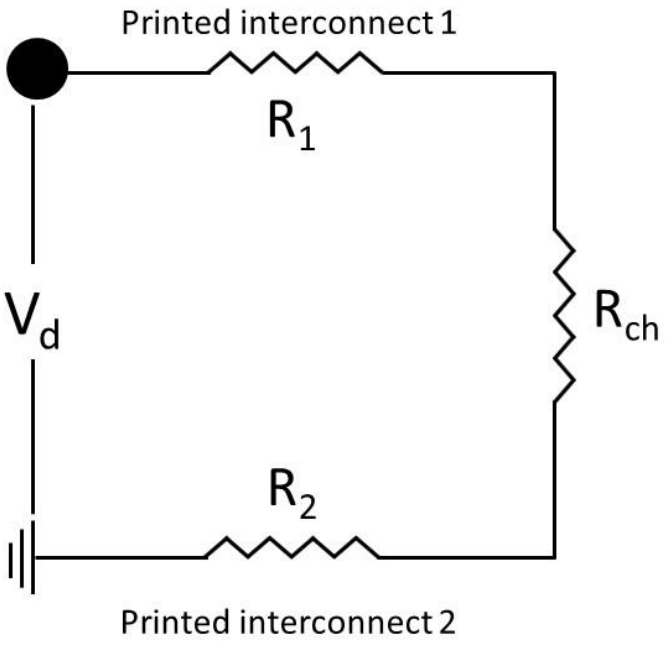

Figure 4-4. An equivalent circuit for bonded MOSFET device.

Table 4-2. Parameters for interconnect analysis

Applied drain bias	**R_{ch} (fully accumulated channel)**	**R_1**	**R_2**	**Effective V_d across channel**	**Mobility (extracted from the measure curves)**	**Mobility (theoretical, using effective V_d)**
0.3	350 Ω	~30 Ω	~30 Ω	~0.25	630 cm^2/Vs	780 cm^2/Vs

An equivalent circuit for a bonded MOSFET device is shown in Figure 4-4. Two additional resistances (R_1 and R_2) connected in series are added to the MOSFET channel after printing interconnects. The value of these extra resistors plays a significant role in defining the transconductance of the device and thus, the field effect mobility. Accordingly, the electrical characterisation of the printed structure was first evaluated. The resistivity of the Ag nano paste was found to be approximately $4.2 \times 10^{-8}\ \Omega m$, equivalent to the conductivity of 40 % bulk Ag, revealing the high conductivity in comparison with other interconnect materials such as Cu/low-k, carbon nanotube (CNT) and graphene nanoribbon (GNR) [140]. Nevertheless, the additional resistance (~30 Ω each) in series leads to a small voltage drop across them and thus reduces the effective drain bias across the MOSFET channel. Based on the measured resistance of printed bonding lines, the voltage drops on each resistor load were theoretically calculated when connected in series and summarised in Table 4-2. Accordingly, such a decrease in mobility could potentially originate from the additional resistance between the chip pads to the PCB pads generated by the printed structures.

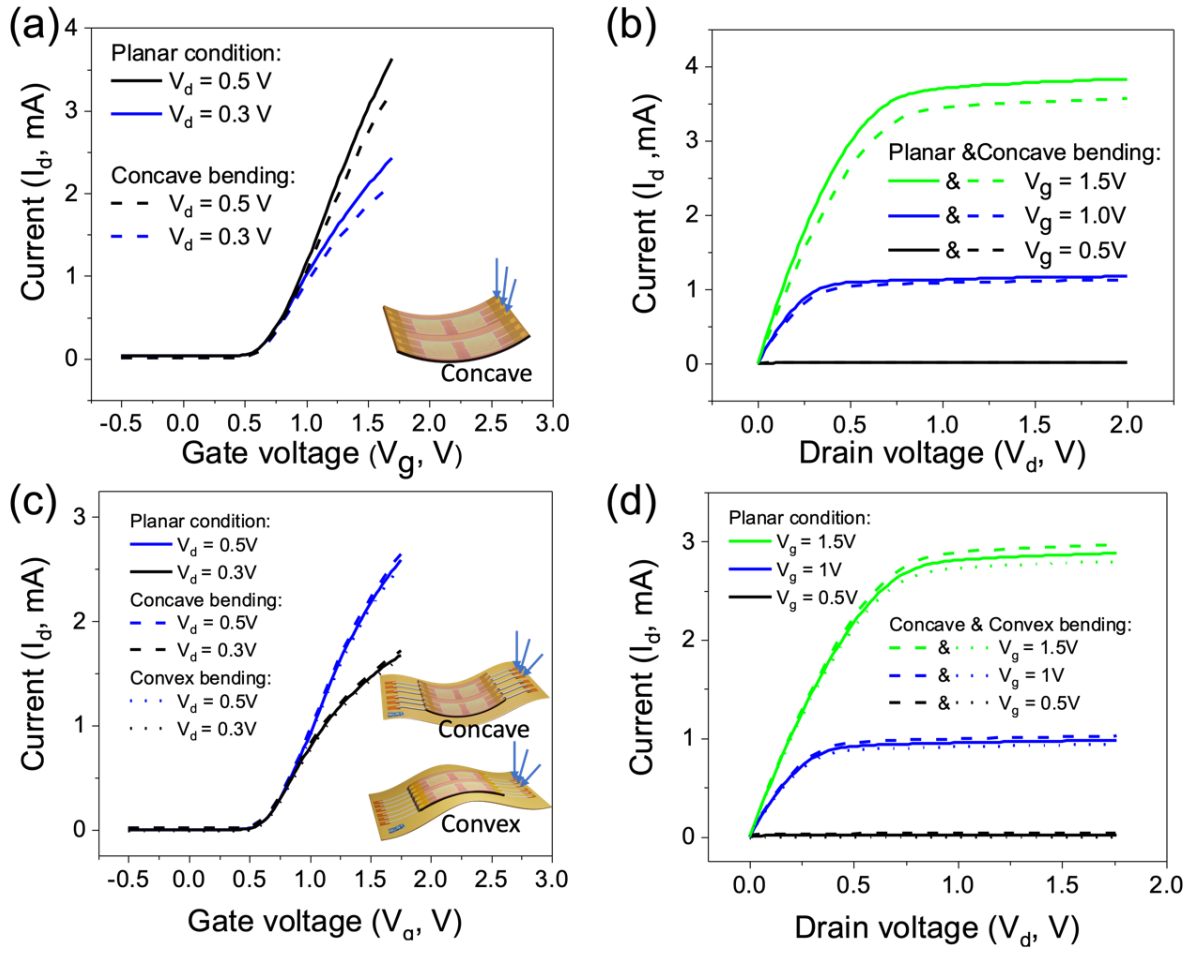

Figure 4-5. Device characterisation after bonding by printing under planer and bending conditions for (a) and (b) after thinning; (c) and (d) after printing by bonding.

Table 4-3. Comparison of MOSFET key parameters under different conditions.

Condition	**Peak Mobility, μ_{EF} (cm^2/Vs)**	**Peak transconductance, g_m (mS)**	**V_{th} (V)**	**SS (mV/dec)**	**Current On/off ratio**
Before thinning	780	2.6	0.6	~125	$>10^4$
After thinning	780	2.6	0.6	~125	$>10^4$
After bonding	630	2.1	0.6	~125	$>10^4$

Bending after thinning	750	2.5	0.6	~125	$>10^4$
Bending after bonding	630	2.1	0.6	~125	$>10^4$

In addition, the bendability of the UTC-based MOSFET was studied by placing the thinned chip on a 3D-printed concave test rig with a radius curvature of 40mm where the thinned MOSFET experienced compressive uniaxial bending stress. Firstly, the bending effect was studied and compared under planar and bending after thinning of chips. In this case, the characterisation was carried out directly on the chip pads. As can be seen from the characterisation results shown in Figure 4-5 (a) and (b), a slight decrease in the drain current, I_d, was observed under the compressive stress. The extracted mobility under bending after thinning (750 cm^2/Vs) is 30 cm^2/Vs lower than under the planer condition (780 cm^2/Vs) without the V_T being shifted. The bending tests were then conducted after forming interconnects under similar conditions. Carrier mobility ($\mu_{FE} \approx 630$ cm^2/Vs) and threshold voltage ($V_T = 0.6$ V), along with other parameters remained unchanged under planar and bending conditions after printing the interconnects, as summarised in Table 4-3. More discussions regarding electrical performance under bending are included in Chapter 6.3.3.

4.3 Physical Bonding by Direct Transfer Printing

The fabrication approach presented above in Chapter 4.2 has led to successful electrical bonding between UTCs and flexible PCBs. However, a minor challenge still existed during the process of transferring UTCs after thinning to flexible PCBs, prior to interconnect printing. This process requires a manual deposition of the low-stress adhesive. The same issues were also found in literature studies introduced in Chapters 2.2.1.2 and 2.2.2.2. Such a manually

conducted process may not be repeatable, often resulting in excessive or inadequate deposition. An excessive amount of adhesive could lead to overflowing of the glue, potentially covering the electrical contact pads on UTCs and an inadequate amount could cause unfirm attachment between UTCs and substrates. The amount of manually deposited adhesive is challenging to be kept constant, or optimisation would be required for chips with different dimensions. In addition, handling UTCs and transferring them to the designated place manually poses the risk of dropping and/or misplacing.

This section addresses the challenges in transferring and physically bonding UTCs onto flexible substrates. As conventional pick-and-place technique involves the use of a vacuum, which can highly likely damage the thinned chips because of their fragile nature. Other pick and place processes and materials for handling and bonding UTCs have thus been explored, such as transferring using tapes or elastomeric stamps such as polydimethylsiloxane (PDMS) owing to their flexible and conformable features. Despite the process being commonly explored, an intermediate handling material is inevitably required, and the delamination of such materials can lead to risks of damaging thin chips. These challenges could be effectively mitigated by employing the 'direct transfer printing' method, which has been proven to successfully integrate laterally aligned nanoscale and microscale structures with a remarkable transfer yield of 95% [129, 141]. Therefore, a direct transfer printing technique, as a single-step approach without the need to adopt an intermediate material, has been adopted to transfer UTCs onto flexible substrates using a custom-made setup, as a collaboration with my colleague, Adamos Christou [142].

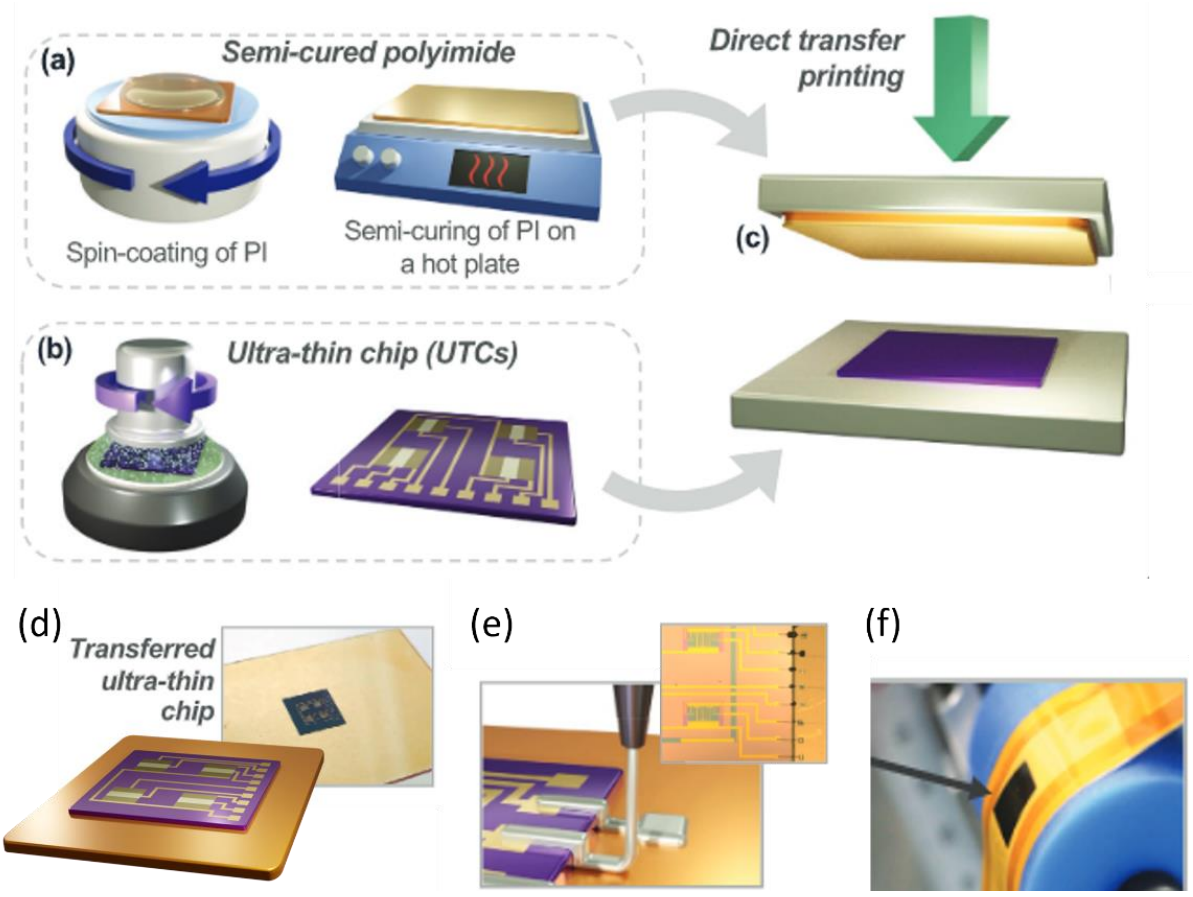

Figure 4-6 Schematic representation of the experimental steps followed to integrate UTCs onto flexible substrates to enable FHE system: a) preparation of receiver semi-cured PI substrate; b) realising the ultra-thin MOSFET chip (UTCs); c) direct transfer printing of UTCs; d) printed UTCs; e) DIW to print interconnects to access UTCs. The figure panel e also shows optical images of UTCs with printed interconnects. (f) bended UTC after encapsulation. {Figures used with permission from A. Christou}

Figure 4-6 shows a schematic representation of the experimental steps followed to integrate UTCs onto flexible substrates, including thinning, direct transfer printing, interconnect printing by extrusion system and bending test to confirm the flexibility and reliability of the bonded UTCs.

Firstly, a destination substrate material needs to be selected and suitable for potential uses in FHE systems. Ideally, the target substrate should be: 1) flexible, lightweight, and manufacturable; 2) chemically inert, as the subsequent processes may involve chemicals; 3) non-toxic, for potential applications in wearables and implantable systems; 4) thermally

conductive, to assist heat dissipation; 5) electrically insulating, to ensure firm isolation between Si processing modules and other printed devices; 6) similar coefficient of thermal expansion to Si (CTE_{Si} = 3.2 ppm/°C), ensuring materials' stability in the following processes. Commonly explored destination substrates for flexible electronics include polymeric, glass foils, paper, and fabric substrates. Considering that in the device-first approach, there are subsequent fabrication steps that have requirements for temperature tolerance and electrical insulation, only polymeric substrates have been taken into account. Thin polymer-based plastic sheets such as polyethylene terephthalate (PET), polyethylene naphthalat (PEN), polydimethylsiloxane (PDMS) and polyimide (PI) are widely used. PI especially stands out amongst the rest due to higher glass transition temperature (up to 400 ºC) and lower CTE (as low as 3 ppm/°C, matching with that of Si).

In this work, destination substrates are prepared as follows: Glass substrates are used to function as temporary carriers with good planar surfaces for all development processes. Glass substrates are firstly thoroughly cleaned by dipping in acetone, IPA, and DI water baths with gentle agitation in the ultrasonic bath and followed by nitrogen stream to dry. After the use of cleaning agents, argon plasma is adopted as the last cleaning step to remove any residual contaminants and activate the surface for better adhesion. Next, PI substrates are obtained by spin-coating two layers of PI (PI2611 from HD Microsystems) on rigid glass substrates. A semi-cured layer of PI is obtained to serve as an adhesive layer, prior to transfer printing by heating the PI at 90°C for 3.5min. In the present case, semi-cured PI acts as a substrate as well as an adhesion layer. It is also to be noted that PI2611 for these experiments has been specifically selected, which has a coefficient of thermal expansion (CTE) very close to the CTE of silicon (CTE_{PI} = 3 ppm/°C, CTE_{Si} = 3.2 ppm/°C) to prevent chip damage/delamination during annealing from interfacial thermal stress generation [64, 143]. By employing this process followed by the direct transfer printing technique to physically integrate UTCs on

flexible foils, the adhesive-related issues previously discussed can be resolved. The replacement of glue-based adhesive with spin-coated semi-cured PI eliminates the risks of over- or under-dispensing of the adhesive, ensuring a uniform and planar substrate for UTCs. More details are discussed in Adamos Christou's thesis, including the advantages of employing semi-cured PI, thorough details of the transfer printing step, optimisation, the impact of transfer printing on UTC-based MOSFETs (electrical behaviour before and after transfer printing of 14 devices from 3 UTCs) and cyclic bending tests of embedded UTCs. The key findings showed that the difference of the device performance before and after transfer printing was within an acceptable range. The cyclic bending tests of embedded UTCs were performed under bending, ranging from 0 to 100 cycles at a various of bending radii (40 mm, 30 mm, and 20 mm). UTCs were undamaged after the tests. This series of studies proved the reliability of the proposed direct transfer printing method.

After transfer printing, devices on UTCs were electrically bonded by the optimised extrusion printing system. The dielectric structures were firstly realised covering the step heights by using nanosilica/epoxy to prevent interconnect short-circuiting. After annealing the dielectric layer at 100 °C for 30 min, Ag nano-paste was used to form the conductive tracks (Figure 4-7). It is to be noted that in Chapter 4.2, dielectric ink was not applied as the excessive epoxy-based adhesive had already served as an insulating layer. The device was even evaluated from the extended printed pads. The electrical performance suggested a similar trend as the work carried out in Chapter 4.2.3 (only a minor degradation in mobility with other extracted parameters remaining unchanged).

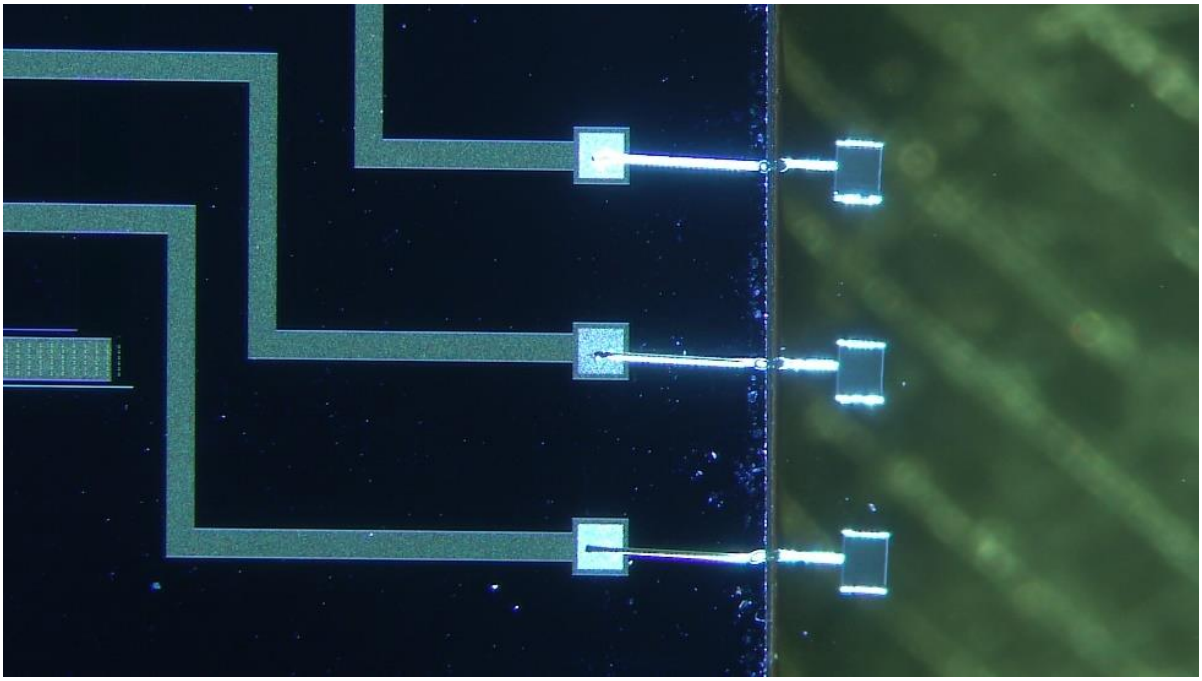

Figure 4-7. Optical image of electrically bonded UTC with printed dielectric layer and conductive interconnects after transfer printing.

4.4 Conclusion

A one-step interconnect forming technology via non-contact printing was demonstrated in this chapter. To elucidate the efficacy of the printing technology for interconnects, conductive tracks were realised to integrate the UTC on the flexible PCB. The UTC was safely electrically bonded using the high-precision extrusion printing system, causing no damage to the thinned chip. This was confirmed by detailed electrical measurements of the MOSFETs after the realisation of printed interconnects. A slight degradation in the device mobility (from 780 cm^2/Vs to 630 cm^2/Vs) was observed after bonding which was attributed to the extra resistances added due to printed lines. Nevertheless, the mobility is still high enough for obtaining high-performance hybrid systems. Such minor performance degradation by printed lines can be prevented by using conductive pastes with lower resistivity. More research will be needed to this end. Finally, mechanical and electrical robustness of both MOSFET and interconnects

were tested under bending conditions (40 mm). The electrical measurements showed excellent stability for both interconnects and MOSFET devices. Further, direct transfer printing was performed to transfer and physically bond UTCs onto flexible substrates using a semi-automated setup. By adopting semi-cured PI serving as part of the substrate and the adhesion layer, the long-standing adhesive distribution issue was successfully eliminated. The reliability of the proposed direct transfer printing method was confirmed by showing stable MOSFET behaviours before and after the process and intact embedded UTCs after cyclic bending tests (more details can be referred to in Adamos Christou's thesis). The presented fabrication route will open new avenues to further progress in the FHE field and meet the high-performance requirements of a wide range of applications.

During this study, it was discovered that only conformal printing could be achieved by the extrusion printing system. Due to the printing material's high viscosity and the system's extruding mechanism, it cannot support freestanding structures with a high aspect ratio. Hence, the printed interconnects were achieved by printing directly on top of the printed dielectric layer. If the printed structure could be constructed similarly to conventional wire bonding, then the printing of the dielectric layer could have been omitted. Therefore, a different printing technique has been taken into consideration to explore the possibility of building printed wire-bonding-like, freestanding, out-of-plane features, which is discussed in the next two chapters.

Chapter 5. Printing of Vertical and High Aspect Ratio Interconnects for Out-of-Plane Electronics

The content in this chapter was adopted from this paper:

- **S. Ma**, A. S. Dahiya, and R. Dahiya, "Out-of-Plane Electronics on Flexible Substrates Using Inorganic Nanowires Grown on High-Aspect-Ratio Printed Gold Micropillars," *Advanced Materials*, p. 2210711, 2023, doi: https://doi.org/10.1002/adma.202210711.

5.1 Introduction

As mentioned above in Chapter 4.4, a printing technique with the capability of forming freestanding features with a high aspect ratio would be a simpler alternative to extrusion printing without the need to form dielectric layers prior to interconnect printing. However, most of the existing additive manufacturing (AM) techniques offer a poor resolution and it is challenging to obtain out-of-plane structures (e.g. micro/nanopillars) with diameters less than 50 µm [4]. Despite the capability of achieving high-resolution printed interconnects by the extrusion printing system introduced in Chapter 4, several determinants serve as underlying challenges that could impede its application in the fabrication of freeform out-of-plane structures. As usually high-viscosity inks/pastes are adopted in extrusion printing (such as >100,000 cP used in Chapter 4), the challenges can occur in these ways: (1) Extruding highly viscous inks with high yield strength requires more pressure, which can lead to challenges in maintaining consistent extrusion rates and material flow. This can further negatively influence the accuracy and quality of the printed structure, especially in intricate or fine-detailed designs such as pillars. (2) Printing out-of-plane structures, such as arches, or in the case of forming a wire-bonding-like interconnect for UTCs, often involves printing hollow structures or layers that are not fully supported by any layers below. This can lead to issues with sagging or collapsing of the printed material because of gravity, especially when using viscous materials

that might not have sufficient initial strength to hold their shape. The solution to these can be adopting a sacrificial supporting structure prior to printing using extrusion systems for a more controlled environment/base, however, this adds more fabrication steps and complexity, and a successful removal can be potentially challenging too [144]. In this regard, the high-resolution jet-based printing technique has shown good potential. For instance, aerosol jet printing has been used to produce micropillar electrode arrays (MEAs) for photosynthetic applications [145]. The aerosol jet printing with a resolution of 10 – 15 μm can provide out-of-plane structures with a larger height (> 500 μm) but fails to deliver the same with a high aspect ratio. High aspect ratio 3D structures are needed to achieve high-density device integration. In this regard, the drop-on-demand (DoD), electrohydrodynamic (EHD)-based jet printing has garnered significant attention. The method involves the dropwise dispensing of nanoparticle-laden ink from a scanning nozzle [135, 146-149]. Such printing systems are usually computer-interfaced, and they enable mask-less fabrication, allowing greater flexibility for building out-of-plane self-supporting structures such as micro- and nanoscale pillars. High-resolution EHD printing systems have therefore been explored for achieving 3D structures, however, the choice of printing materials is mainly limited to forming metallic structures with a small aspect ratio.

Before obtaining printed wire-bonding-like interconnects which consist of a pair of tilted and connected pillars on different planes due to the UTC step height, pillar printing is firstly explored. Hence, in this chapter, the optimisation of EHD printing is firstly thoroughly studied, in terms of applied voltage, frequency, stage speed, and nozzle-to-substrate distance, to obtain directly printed high aspect ratio (ultra-long with short diameters) metallic micropillars. The optimised EHD process has allowed printing libraries of Au MEAs with different heights, diameters, and pitches. Maximum micropillars, height of ~196μm with an aspect ratio of ~52, have been achieved.

The capability of printing high-density out-of-plane structures by the EHD system has also led to the exploration of transforming the current planar integration of electronic devices into 3D or out-of-plane configurations, creating attractive new opportunities for the advancement of this exciting field into diverse ranges of applications such as drug delivery, tissue engineering, surface engineering, optoelectronics, energy conversion and storage, etc [150-159]. For instance, hemispherical silicon nanorod photodiode arrays have been used to extract the angular information of light in a 3D space to enable imaging systems with a wide field of view, miniaturised design and deep depth of field [160]. The additional attributes of out-of-plane configurations endow to flexible electronic system with an enhanced sensing surface area, large stretchability, and high device integration density [161, 162]. Owing to such features, the out-of-plane structures such as micro/nanopillars, nanowires (NWs), scaffolds, etc. have attracted attention [82, 163]. Table 5-1 shows EHD printed out-of-plane structures and a comparison regarding the aspect ratio, length, type of inks, substrates, and applications developed.

Table 5-1. Comparison of EHD-based jet printed nano to microscale pillars.

Diameter	**Height**	**Aspect Ratio**	**Ink**	**Substrate**	**Application**	**Ref.**
12µm	100µm	8	wax	N/A	-	[164]
~200µm	0.7-1.8mm	3.5-9	Molten metal (32.5% Bismuth, 51% Indium, 16.5% Tin)	PDMS, Glass	Interconnects	[165]
1.4µm	66µm	50	Ag	Plastic, flexible	Interconnects	[82]
20µm	120µm	6	Ag	N/A	-	[166]
-	-	35	Ag	Si wafer and glass coverslip	Touch sensor and air flow-rate sensor	[147]

170nm - Cu	65µm - Cu	400 - Cu	Ag, Cu, Ag-Cu	Glass slides and Si wafers	-	[167]
3µm	75µm	25	Au	Rigid glass slide & MEA	Cellular activity monitoring	[135]
50nm	850nm	17	Au	Glass	Plasmonics	[168]
3.74µm	196µm	52.47	Au	Flexible polyimide	Out-of-plane ZnO nanostructure-based Photodetectors	This work

Herein, this chapter also presents a novel fabrication route to obtain out-of-plane hierarchical functional (light-sensitive) nanoarchitectures comprising of DoD-based EHD printed high-aspect ratio conductive micropillars, followed by seedless growth of zinc oxide (ZnO) nanowires (NWs) on as-printed micropillars using low temperature hydrothermal (HT) growth method [169-173]. To the best of our knowledge, this is the first study where a seedless HT growth of ZnO NWs is carried out on printed 3D Au micropillars. As a proof of concept, these light sensitive hierarchical structures have been used to obtain out-of-plane 3D flexible ultraviolet (UV) photodetectors (PDs). Further, compared to 2D layouts, the fabricated 3D PDs have shown better sensitivity and an excellent omnidirectional light absorption ability. The developed PDs maintain high photocurrents over wide light incident angles (±90°), which is needed to enable broadband omnidirectional UV light detection. The 3D PDs have also been evaluated under both concave and convex bending conditions and demonstrated excellent mechanical flexibility as well as negligible changes in device performance under mechanical loadings. The presented hierarchical 3D connected NW network shows the potential to enhance the energy harvesting efficiency of solar cells and artificial photosynthesis process by light scattering enhancement and trapping [145, 174, 175].

5.2 Optimisation of EHD-Printed Freeform Structures

The EHD-based jet printing is an AM technique that can print metal and/or functional nanoparticle inks with high design flexibility and resolution via a contactless direct write approach. In this chapter, the EHD-based super inkjet (SIJ) printer is employed (resolution: 1-10 µm), as shown schematically in Figure 5-2. During printing, the nozzle is positioned a few microns (20-40 µm) above a motorised stage on which the substrate is placed. As per the EHD mechanism, the computer-interfaced system generates force to eject droplets through an oscillating electric field between the nozzle and the printing stage, controlled by the voltage applied. It is to be noted that in comparison with conventional EHD printing, SIJ does not form a Taylor cone that limits the process controllability [86]. As a result, SIJ has precise control over the volume of the ink droplet. The minimum volume of ink droplets is < 1 femtolitre (fL) i.e., 1,000 times smaller than that of a conventional inkjet printer (volume = 2 picolitre (pL), or diameter = 16µm) [134, 176]. Further, the volume of the droplet and/or the printing resolution can be changed or optimised by varying the applied frequency, the stage speed, and the distance between the nozzle tip and the substrate. For example, the printing frequency becomes critical for the construction of micropillars when the ejected droplets are required to be vertically stacked. Frequency is important because it controls the time interval between the consecutive droplets. For the pillar formation, each incoming droplet needs to be viscous enough to avoid spreading (i.e., most of the solvent must evaporate before arriving on the pillar/substrate). The optimised frequency needs to provide enough time for the previous droplet to dry and hence maintain its shape. Therefore, the optimisation of each printing parameter is critical for a sequence of droplet deposition and liquid vaporisation to achieve a high aspect ratio and uniform out-of-plane micropillars.

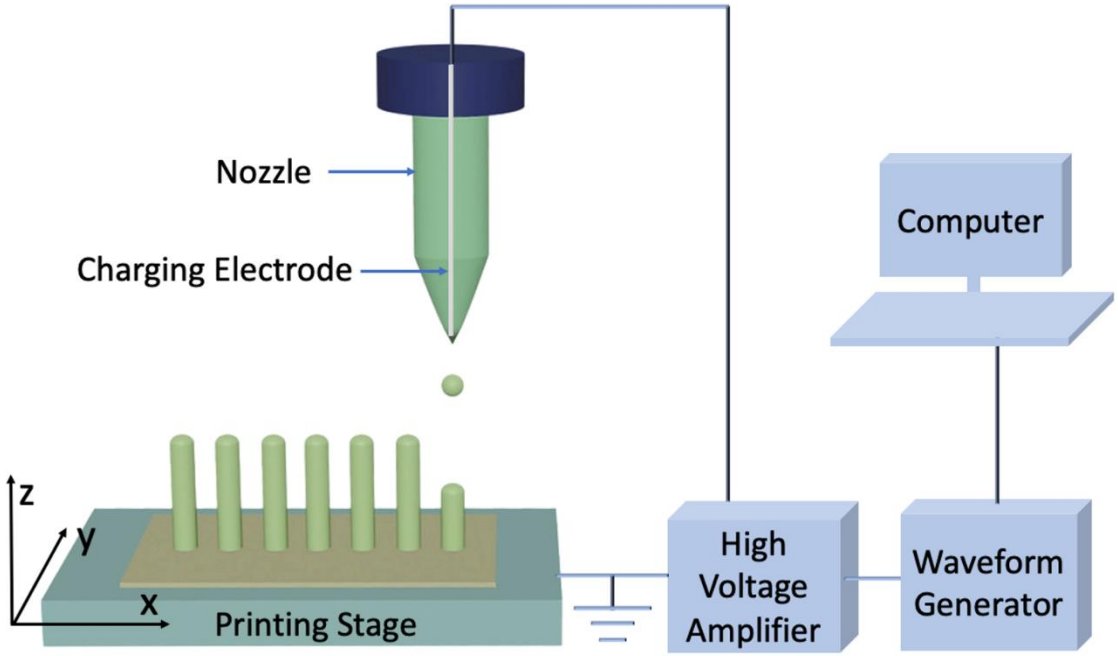

Figure 5-1. EHD pillar printing schematic.

In this work, printed micropillars were obtained using super fine nozzles (1 – 3 µm diameter opening size) with gold nanoparticle (Au NP) ink under ambient and controlled conditions (room temperature between 20 – 23 °C, relative humidity (RH): ~40 %). The optimisation process is as follows: One of the most critical printing parameters is the applied voltage, which directly determines the electric field strength needed to eject the droplet from the nozzle. Primarily, the applied voltage needs to be large enough to eject droplets. A higher electric field leads to a higher jetting speed and higher volume of the jetted ink per droplet, therefore leading to larger printed features. Further, a higher jetting speed results in a shorter flight time of the ejected droplets, providing less time to evaporate the ink solvent and thus, poor control over the micropillar's diameter. Besides, higher voltages could lead to ink spreading at the bottom of the pillar, potentially short-circuiting the adjacent pillars. Figure 5-2 show the influence of the change in applied voltage on the diameter of micropillars. The data shows a direct proportional relationship between the applied voltage and the diameter of micropillars. Other important printing parameters are the stage speed, frequency of applied voltage and the nozzle

to substrate distance. To construct MEAs, it is important to control the stage speed as it can affect the desired pillar spacing. A lower printing speed is more suited to achieving MEAs with smaller pitches as it provides a longer flight time and hence allows the solvent to dry before the subsequent droplet reaches on top of the previous one. Likewise, the frequency of the applied voltage is directly related to the liquid vaporisation rate. The optimised printing frequency and speed used in this work to construct MEAs were 20 Hz and 1 mm/s, respectively. It is to be noted that the printing acceleration was fixed to 10 mm/s^2. The nozzle-to-substrate distance was optimised to be ~20 µm for a stable printing.

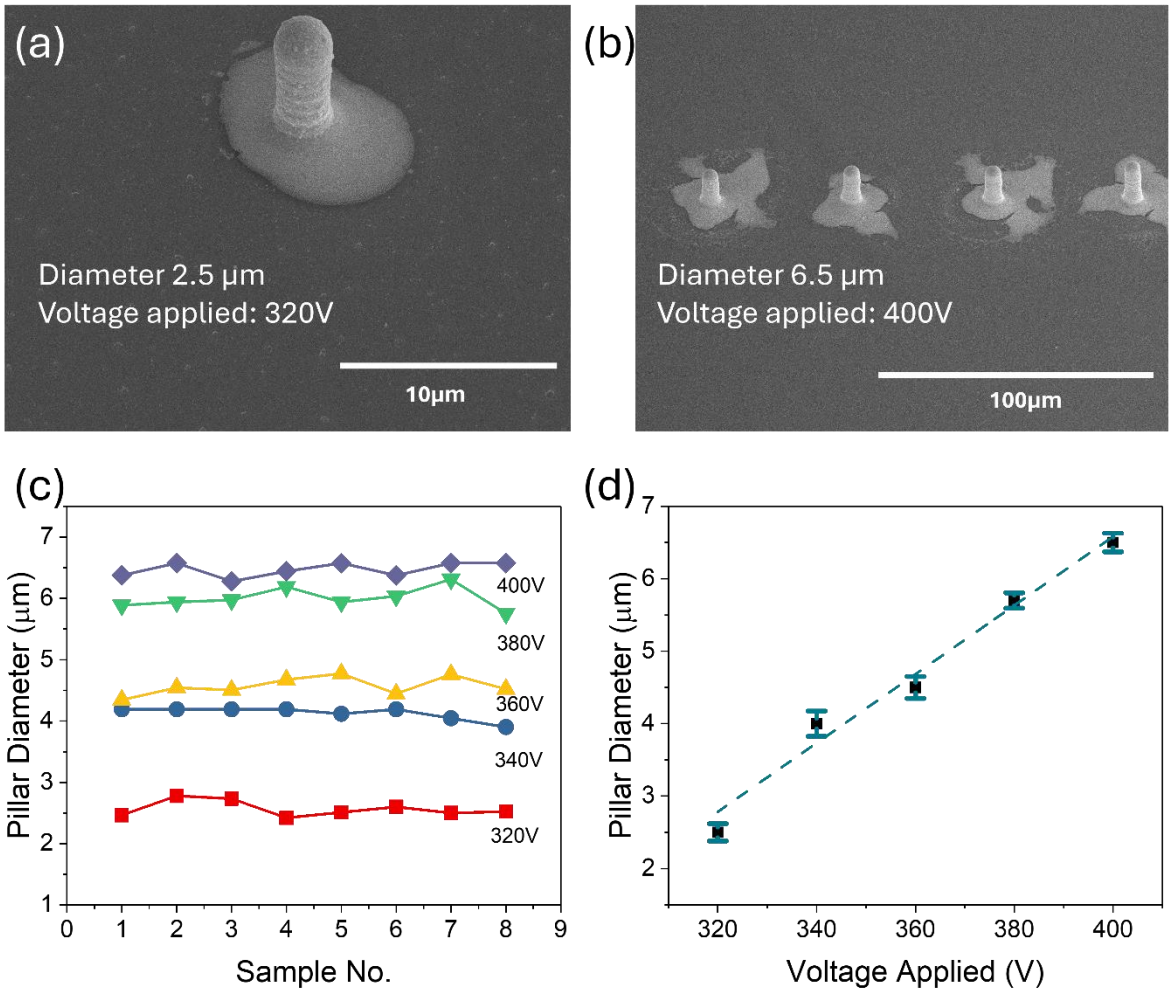

Figure 5-2. (a) SEM image of a pillar with 2.5µm diameter achieved by applying 320V; (b) SEM image of pillars with 6.5µm diameter achieved by applying 400V; (c) Influence of applied voltage on pillar diameter, characterised for 8 samples to obtain statistical data; (d) The change of pillar diameter as a function of the applied voltage.

Next, the change in the micropillar height with respect to the number of droplets was recorded. It was observed that the micropillar started to appear after five droplets (Figure 5-3 (a), a pillar formed by 10 droplets). Figure 5-3 (b) depicts the SEM image of five rows of printed micropillars obtained with different numbers of droplets (10 – 50 droplets from the bottom to the top in the image). Figure 5-3 (c) and (d) show the plots of measured micropillar heights with an increasing number of droplets applied (from 10 to 50).

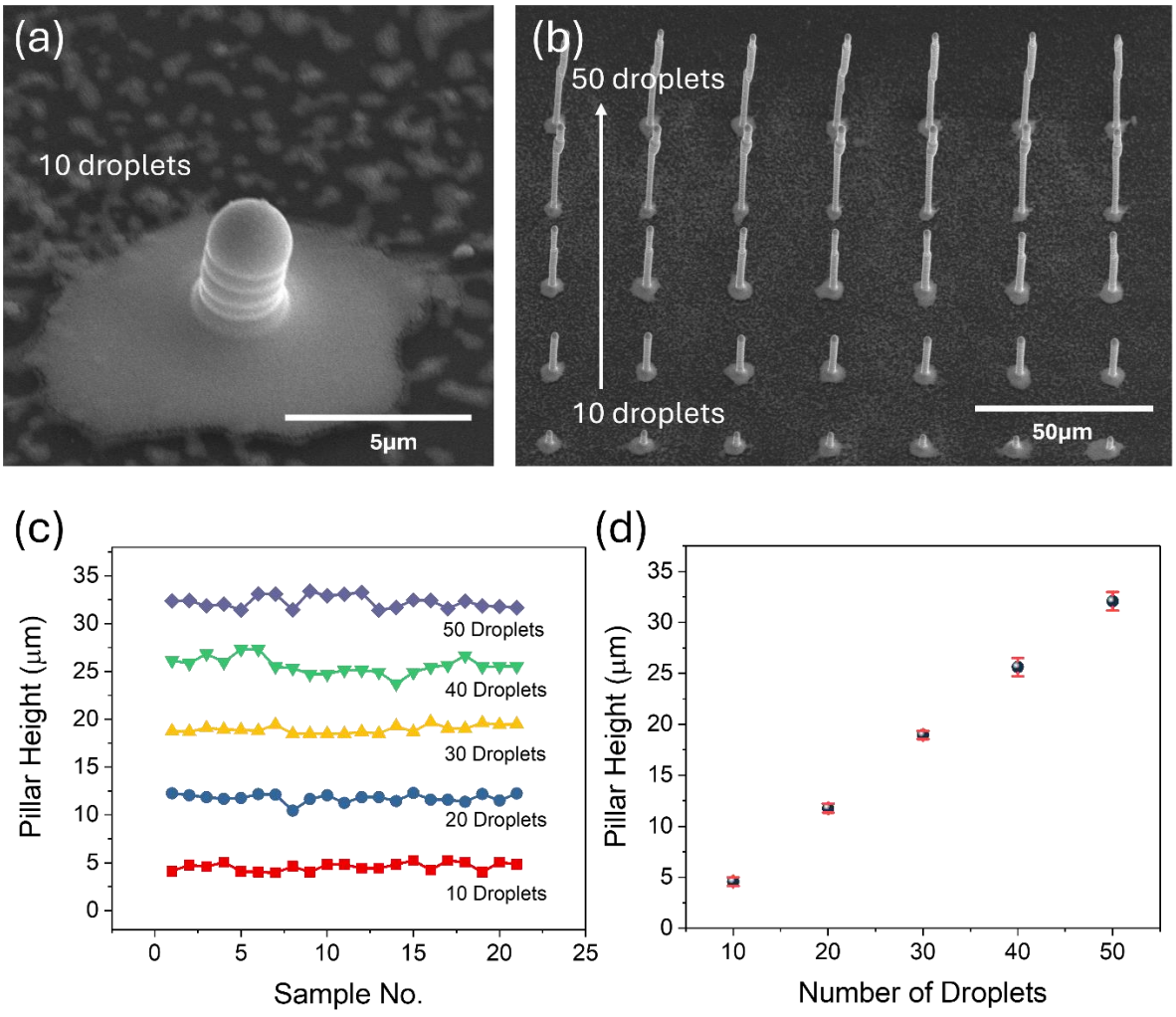

Figure 5-3. (a) SEM image of a micropillar formed with 10 Au droplets; (b) SEM image of a micropillar electrode array (MEA) with 25µm spacing. Micropillars in each row are formed with different number of droplets (10 to 50 Au droplets from bottom to top); (c) Pillar height as a function of Au droplets, characterised for 21 samples to 3 obtain statistical data; (d) The change of pillar height as a function of the numbers of droplets;

After the pillar 'base' is built, the average pillar growth rate is ~0.5 µm per droplet. To avoid nozzle clogging and to ensure uniform growth of micropillars, the nozzle distance from the substrate was increased during printing in such a way that there was some distance between the micropillar tip and the nozzle. For this, the nozzle was moved up along the z-axis by 10 µm for every 20 droplets (corresponding to ~0.5 µm per droplet). After printing, the micropillars were annealed at 250 °C for 2 h to cure the ink. Using the above-mentioned optimised parameters, in the case of MEA printing, taking the stage movement into account, a micropillar printed through 50 droplets (~22.5 µm) can be generated in approximately 5 – 6 s. Figure 5-4 (a) shows the SEM image of MEAs resulting from the optimised printing parameters with the state-of-the-art aspect ratio (height = 196 µm, diameter = 3.74 µm, aspect ratio = 52.47). (Note: the SEM images are taken with the sample held at 45°. Hence, the actual pillar height = pillar height in SEM images $\times \frac{1}{\sin(45°)}$). Figure 5-4 (c) shows a tilted micropillar obtained by moving the printing stage along the x-axis. This can be achieved owing to the autofocussing effect. During printing, the top of the pillar can serve as a charged electrode, which can generate electric field gradients and attract the approaching droplets towards the already printed structure instead of the substrate. An array of tilted pillars formed with different numbers of droplets is shown in Figure 5-4 (b). Subsequently, free-standing arch-shaped structures were realised by controlling the direction of the substrate movement (Figure 5-4 (d) and (e)). The demonstrated capability to achieve different shapes of high-resolution, freestanding out-of-plane structures reflects the versatility of the presented printing approach, which can also assist in the development of new solutions for 3D interconnects, vias, extracting light's angular information in 3D space and so on.

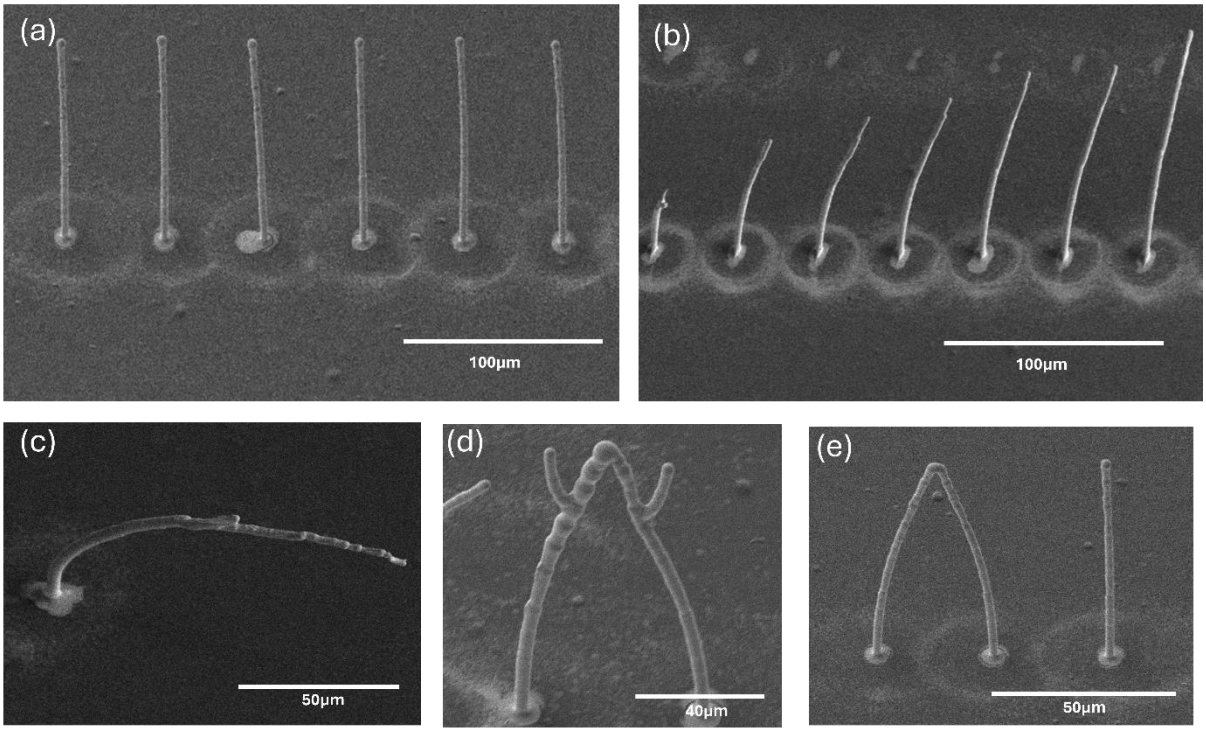

Figure 5-4. SEM images of (a) linear array of high-aspect-ratio micropillars; (b) single row of the tilted MEAs with different number of droplets; (c) one tilted pillar; (d) utilisation of two tilted micropillars to form an arch for three-dimensional interconnects and out of plane vias; (e) an arch-shaped pillar with a vertical pillar.

5.3 Out-of-Plane Electronics

5.3.1. Methods and Materials

The printed MEAs were used to realise a 3D hierarchical light-sensitive NW network for omnidirectional light harvesting. For this, a seedless hydrothermal (HT) growth approach was used to grow out-of-plane ZnO NWs on the printed MEAs. The growth was conducted by a former colleague, Dr. Abhishek Singh Dahiya. The HT approach was adopted for the synthesis of ZnO NWs on printed Au MEAs using a growth solution containing 1:1 ratio of 100 mM zinc nitrate hexahydrate ($Zn(NO_3)_2$, $6H_2O$, 98 %, Sigma-Aldrich), and 100 mM hexamethylenetetramine (HMTA, Sigma-Aldrich). 1 ml of a 40 mM ammonium hydroxide (NH_4OH, Sigma-Aldrich) solution was also added into the growth solution. During the NW

growth, the substrates were immersed facing down in a Teflon flask with growth solution, sealed inside a stainless-steel autoclave reactor, and placed in a preheated convection oven at 95 °C and left inside for 15 h. The autoclave is then taken out from the oven and allowed to cool down naturally.

5.3.2. Evaluation of the Device Configuration

To validate the omnidirectional light detection, the ultraviolet (UV) photodetectors (PDs) were realised on flexible polyimide (PI) substrates using the 3D hierarchical NW network. First, the pillar pitch was optimised to present the best UV sensing performance. For this, Au contact electrodes with 100 µm channel length were first printed. Then, one row of micropillars was printed in between the printed contact electrodes. It is to be noted that the device contact electrodes were connected to the ZnO NWs through micropillars on the electrodes. Pillar arrays with three different pitches (10, 15 and 20 µm) were fabricated to explore the effect of 3D micropillar pitches on the PD performance (Figure 5-5). Next, ZnO NWs were hydrothermally grown (Chapter 5.3.1).

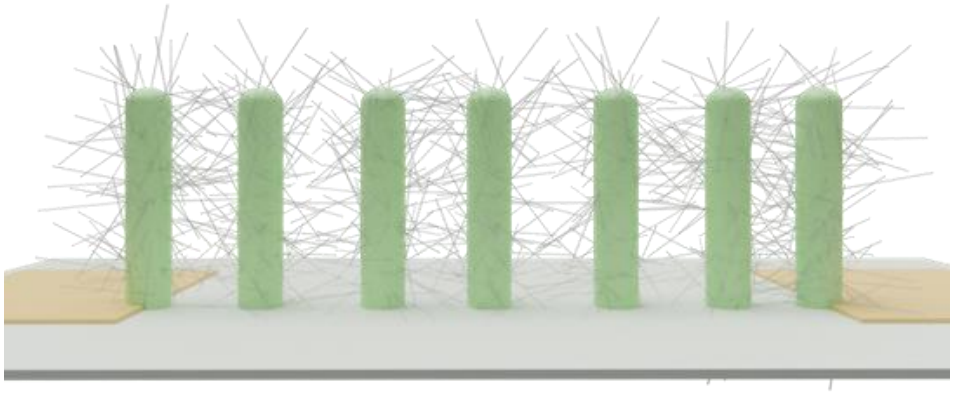

Figure 5-5. Schematic of as-fabricated PD.

The electrical characterisations of as-fabricated PDs were performed using a UV light-emitting diode (365 nm) under ambient conditions. To have the statistical data, five devices for each pillar pitch were characterised under similar conditions: 1 µW/cm^2 light illumination and 1 V

bias voltage. The obtained experimental results are shown in Figure 5-6. Figure 5-7 (a) – (c) depict the time-domain photo response of fabricated PDs with different pillar pitches at 1 V bias under varying illumination intensities from 0.5 to 2.5 μW/cm^2 with a step of 0.5 μW/cm^2.

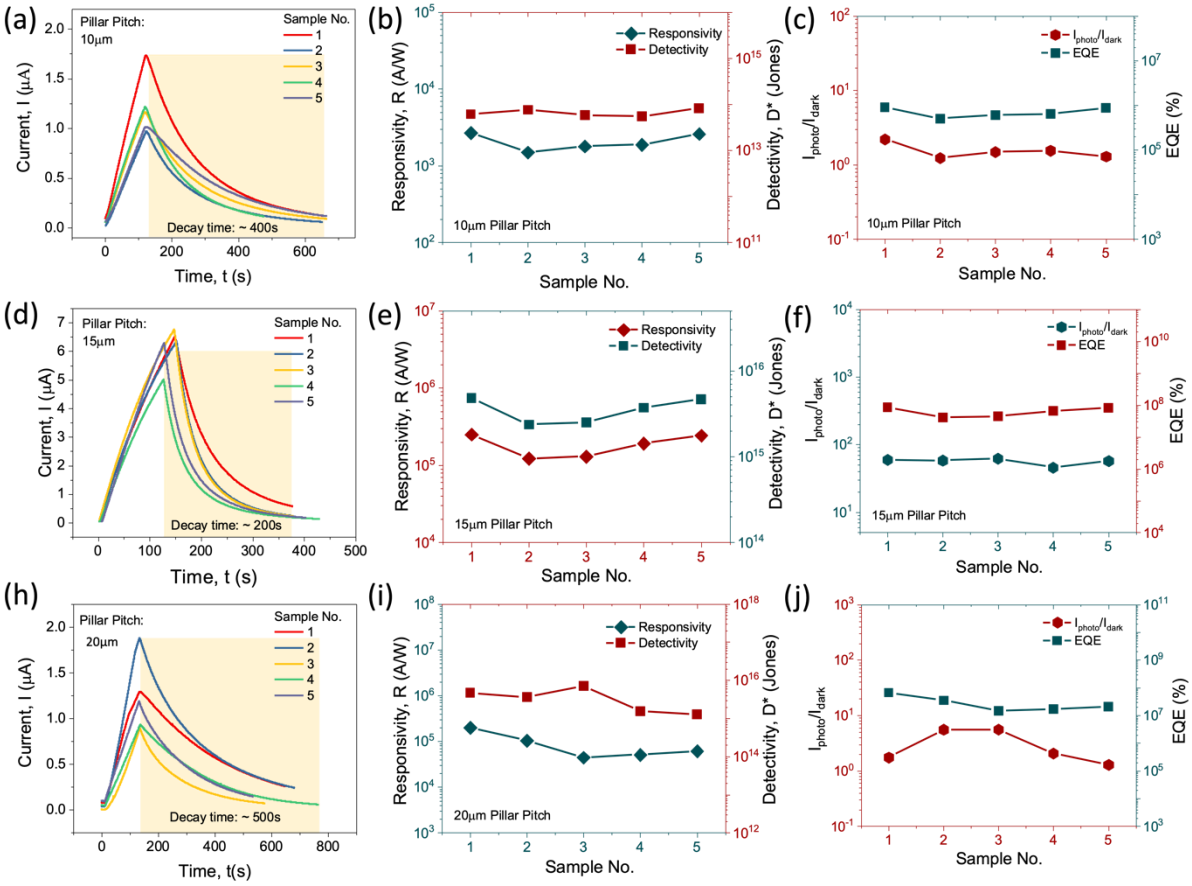

Figure 5-6. Photo response characterisation for 5 samples including time domain response, extracted parameters (responsivity, detectivity, I_{photo}/I_{dark} and EQE) for devices structured with different pillar pitches under 1 μW/cm^2 light intensity and 1V bias voltage: (a)-(c) 10 μm pillar pitch; (d)-(f) 15 μm pillar pitch; (h)-(j) 20 μm pillar pitch.

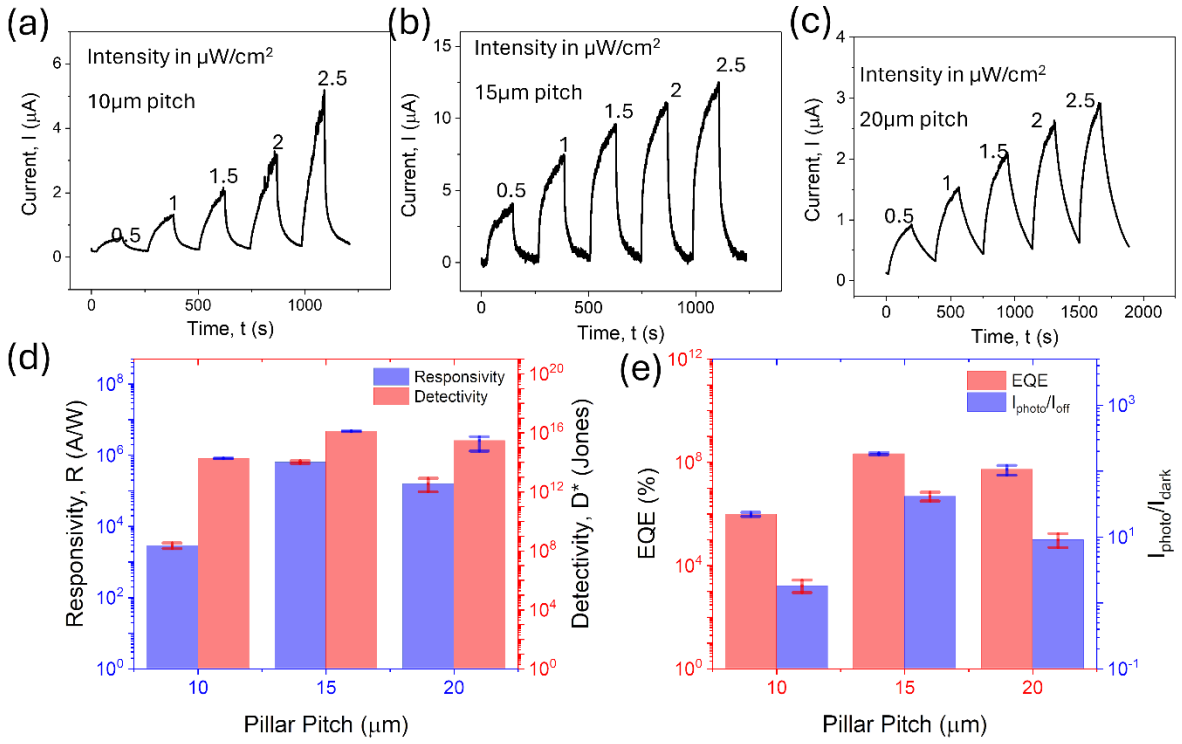

Figure 5-7. Time-domain photo response of fabricated out of plane PDs at 1V bias under increased illumination intensities from 0.5 to 2.5 μW/cm² with a step of 0.5 μW/cm² and different pillar pitches: (a) 10 μm pillar pitch; (b) 15 μm pillar pitch; (c) 20 μm pillar pitch; Extracted parameters: (d) Responsivity and detectivity; (e) Extracted EQE and I_{photo}/I_{dark}.

In all the cases, the photocurrent increased with the increment of incident UV light intensities, because of higher electron-hole pair generation. Further, key parameters including responsivity (R), specific detectivity (D^*), external quantum efficiency (EQE) and I_{photo}/I_{dark} ratio were extracted from the photo response curves at different light intensities (Figure 5-8). Responsivity (R) was calculated to study the photocurrent response to the incident light using this expression (Equation 5-1):

$$R = \frac{(I_{photo} - I_{dark})}{(P_{in} \times S)} \qquad 5\text{-}1$$

where I_{photo} stands for the current under UV light, I_{dark} is the current under the dark condition, P_{in} is the incident light power per unit area (from 0.5 to 2.5 μW/cm²), S is the effective sensing area of the device (channel length = 100 μm, channel width = 13 μm including the pillar diameter and NW length, $S = 1.3 \times 10^{-5}$ cm²).

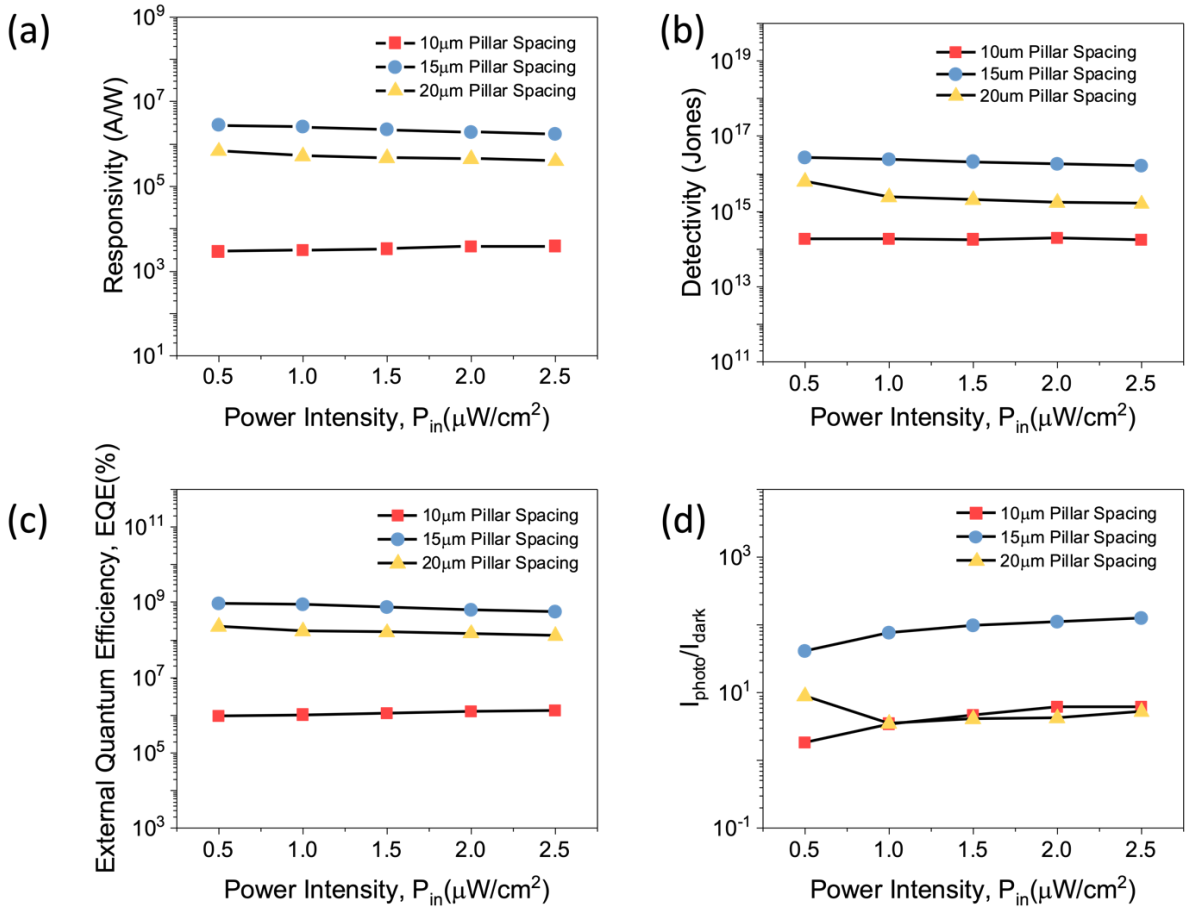

Figure 5-8. Comparison of PD light detection performance for MEAs with different micropillar's pitch and under different incident light intensities from 0.5 to 2.5 µW/cm2: (a) Responsivity; (b) Detectivity; (C) EQE and (d) I_{photo}/I_{dark}.

The specific detectivity (D^*) was obtained to study the device's capability of detecting the smallest signals using Equation 5-2:

$$D^* = \frac{R}{\sqrt{2eJ_{dark}}} \qquad 5\text{-}2$$

where e is the elementary charge and J_{dark} is the current density during the dark condition. Next, EQE was derived to assess the optical properties using Equation 5-3 [177]:

$$EQE = \frac{R \times hc}{e\lambda} \times 100 \qquad 5\text{-}3$$

where c represents the velocity of light and λ is the wavelength of incident light. Finally, the photocurrent on/off ratio was extracted for PDs with 10, 15 and 20 µm micropillar pitches. Extracted parameters are shown in Figure 5-7 (d) and (e) to compare between three different

configurations. The 15 µm spaced micropillar-based PDs showed the best performance among these samples, exhibiting R = 6.31×10^5 A/W (Figure 5-7 (d)), D* = 1.27×10^{16} Jones (Figure 5-7 (d)), EQE = 2.11×10^8 % (Figure 5-7 (e)) and I_{photo}/I_{dark} = 41 (Figure 5-7 (e)) at the light intensity of 1 µW/cm^2 and 1 V bias. It is to be noted that the sensing channel length and applied bias voltage were fixed for all the samples. The experimentally obtained results can be explained using the following hypothesis: The sensing mechanism is described using an energy band diagram schematic shown in Figure 5-9.

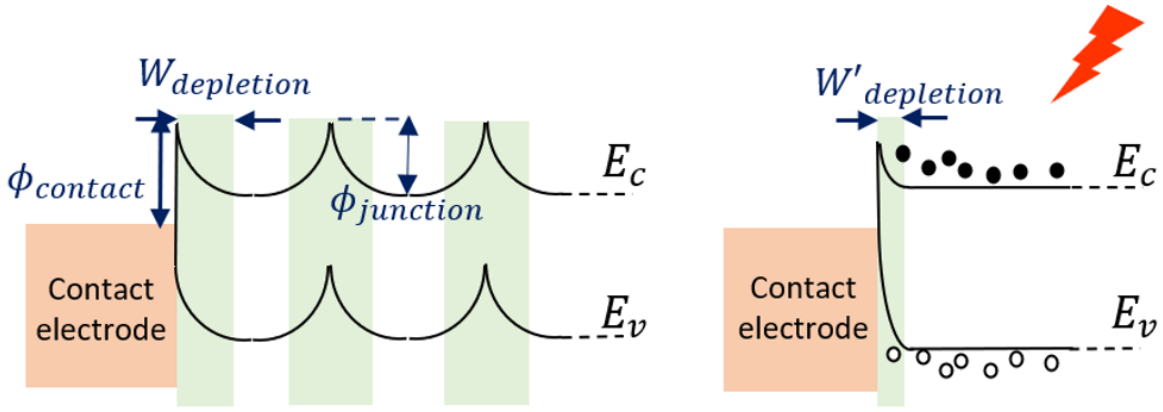

Figure 5-9. Schematic of as-fabricated PD energy band diagram under dark and UV conditions showing the sensing mechanism.

Under no UV light illumination, oxygen molecules exist on the NW surface, forming an electron depletion layer on the NW surface. The near-surface depletion layer results in an upward band bending and therefore forming energy barriers at the metal-semiconductor (MS) interfaces. In all device cases (i.e., PDs with 10, 15 and 20 µm micropillar pitches), devices structured by the row of pillars in series and grown NWs on them form countless NW-NW junctions between the sensing channels. Each NW-NW junction can be represented with a potential energy barrier encountered by the charge carriers under a fixed voltage bias. Under UV illumination, a large number of electron-hole pairs are formed, with electrons being excited to the conduction band and leaving behind holes in the valence band. Furthermore, the generated holes react with the adsorbed oxygen ions on the surface, resulting in the desorption

of oxygen molecules and the release of free electrons. Both events lead to a decrease in the depletion width (W'depletion shown in Figure 5-9) at the MS interface and NW-NW junctions.

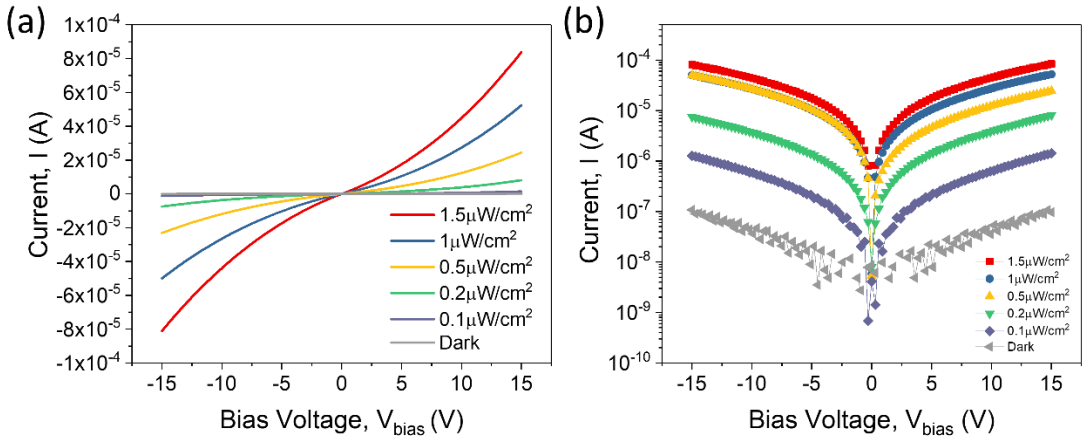

Figure 5-10. Device I-V characteristics under dark and different illumination intensities: (a) Linear scale; (b) Log scale.

Likewise, the barriers become transparent to the incoming free charge carriers, leading to an exponential increase in the device current. With the fixed channel length for all cases (100 µm channel length for PDs with 10, 15 and 20 µm micropillar pitches), there is a larger number of pillars in the sensing channel for devices with 10 µm spaced micropillars. The larger number of pillars in these devices provides more nucleation sites for the growth of NWs, leading to a greater number of NW-NW junctions. This also results in extra energy barriers and reduced dark current. Conversely, devices with 20 µm pillar pitches possess fewer NW-NW junctions, causing electrons to travel in fewer barriers and therefore leading to a higher dark current and longer recovery time. In addition, using the above-mentioned HT ZnO NWs growth method, the NW length is ~5 µm. Considering the micropillar diameter (~3 µm), devices with 15 µm pillar spacing allow a more suitable space for the NW growth, resulting in the most desirable scenario to achieve an optimal high sensing performance. The I-V characteristics (both in linear and log scales) for the 15 µm pillar pitch device, under dark and UV illumination, are shown in Figure 5-10. Schottky barriers were expected to be formed at the metal (Au) and

semiconductor (ZnO interface ($\Phi_{m(Au)}$ = ~5.1 eV, $\chi_{s(ZnO)}$ = ~4.5 eV, leading to a potential barrier height of ~0.6 eV). A symmetrical rectifying behaviour was observed under the dark condition with low current, and an almost linear shape (near-ohmic) I-V curves were obtained under UV illumination due to the reduction in energy barriers.

5.3.3. Evaluation of the Optimised Out-Of-Plane Electronics

Next, MEAs with 3-row micropillar-based PDs were fabricated using the same bottom-up method and the micropillar centre-to-centre distance was kept at 15 µm. Figure 5-11 demonstrates the schematics and SEM images of printed contact electrodes and micropillars (Figure 5-11 (a)), PDs after growing ZnO NWs (Figure 5-11 (b) and (c)), as well as the electrical characterisation results (Figure 5-11 (d) to (e) and Figure 5-12). In this configuration, the sensing area was increased by approximately three times, from 1.3×10^{-5} cm^2 to 4.4×10^{-5} cm^2 (channel width increased from 13 µm to 44 µm with the same channel length: 100 µm). Electrical characterisations were conducted at 0.1 V bias. Interestingly, even with 10 times smaller applied bias voltage, the device detectivity showed an increment of 2 orders whereas I_{photo}/I_{dark} ratio showed 3 orders of enhancement as compared to the results shown in Figure 5-7.

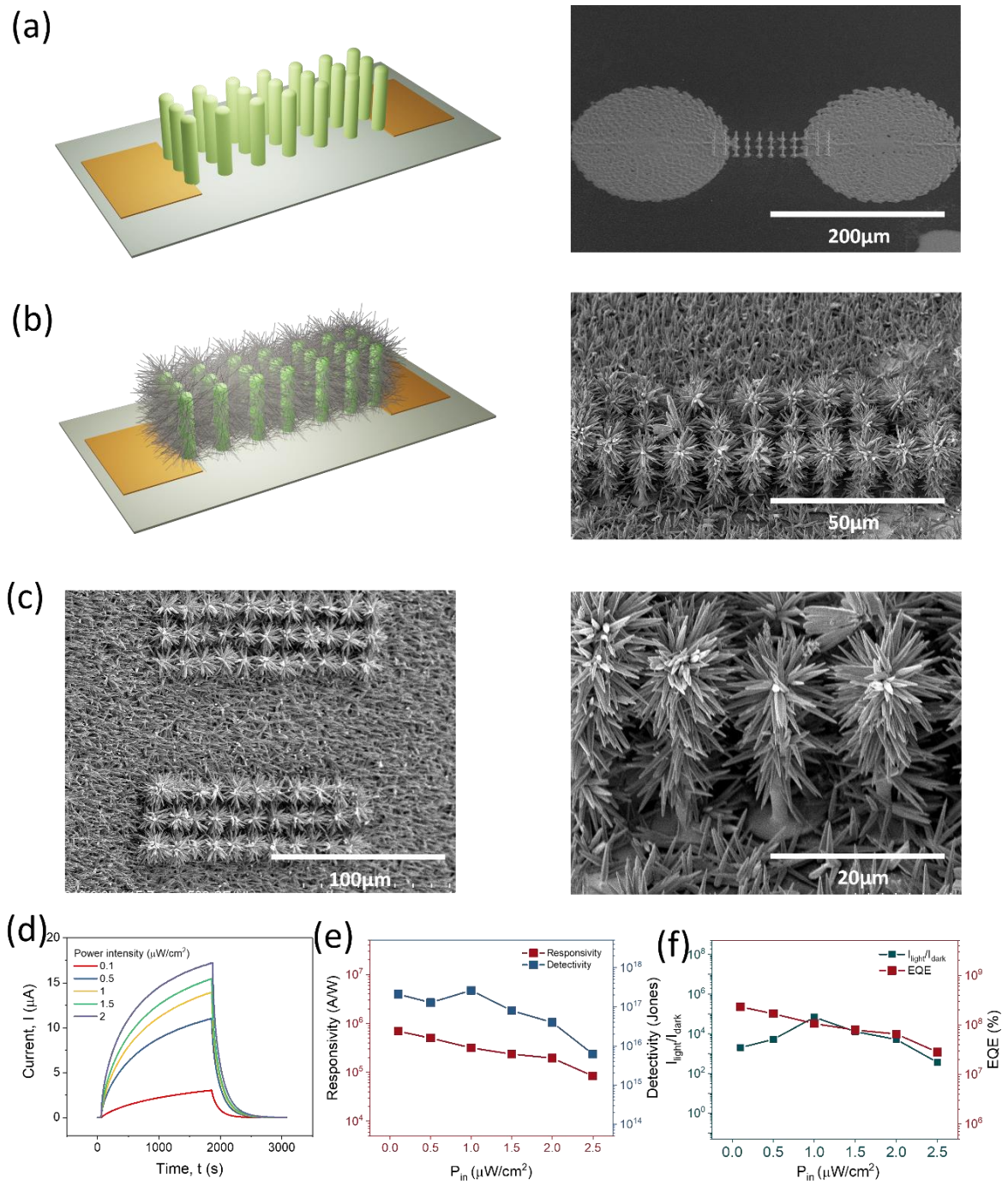

Figure 5-11. (a) Schematic and SEM image of printed micropillars and contact electrodes; (b) Schematic and SEM images of fabricated out-of-plane PDs after growing ZnO NWs on printed micropillars; (c)SEM images of top and tilted side views of printed pillars and contact electrodes; Device characterisation including (d) time-domain photo response, extracted values:(e) responsivity and detectivity: (f)I_{light}/I_{dark} and EQE under different light illumination from 0.1 to 2.5 µW/cm^2.

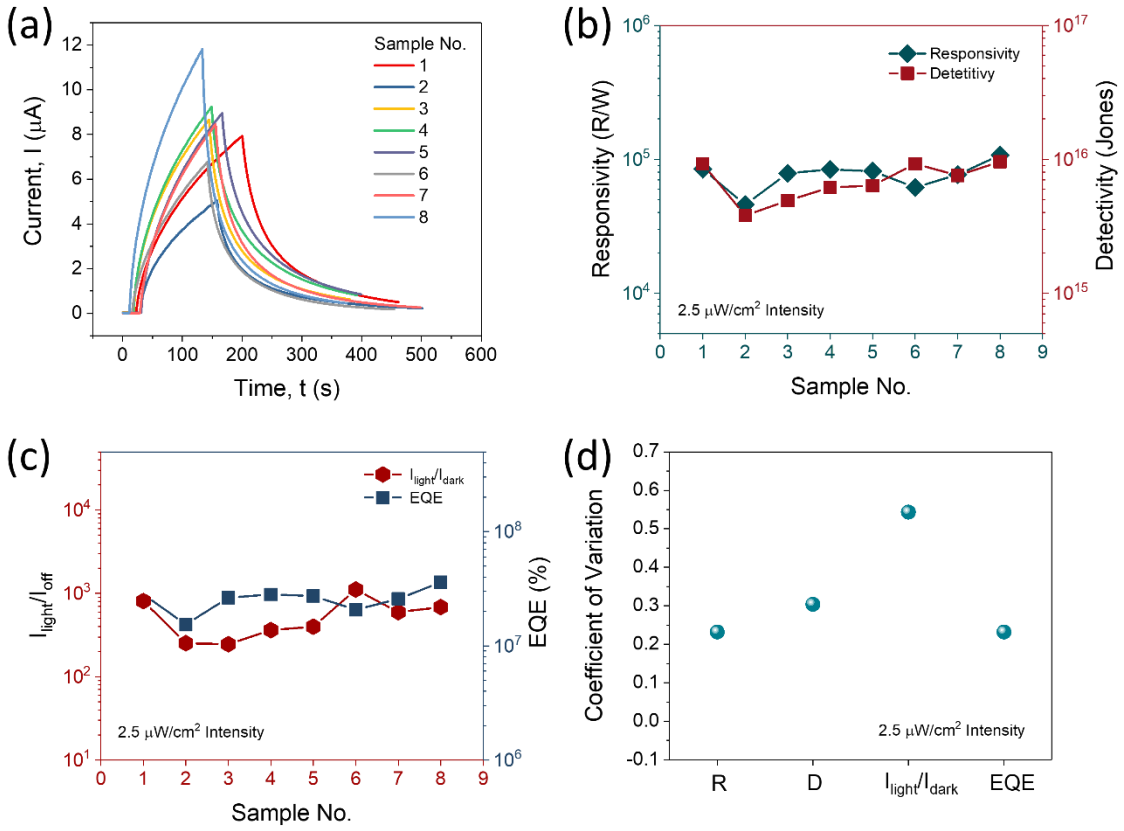

Figure 5-12. Electrical measurements for 8 samples from 3-rows of pillars under 2.5μW/cm² light intensity and 0.1V bias voltage: (a) time domain photo response; Extracted values: (b) Responsivity and detectivity, (c) I_{light}/I_{dark} and EQE; (d) Coefficient of variation for each extracted value.

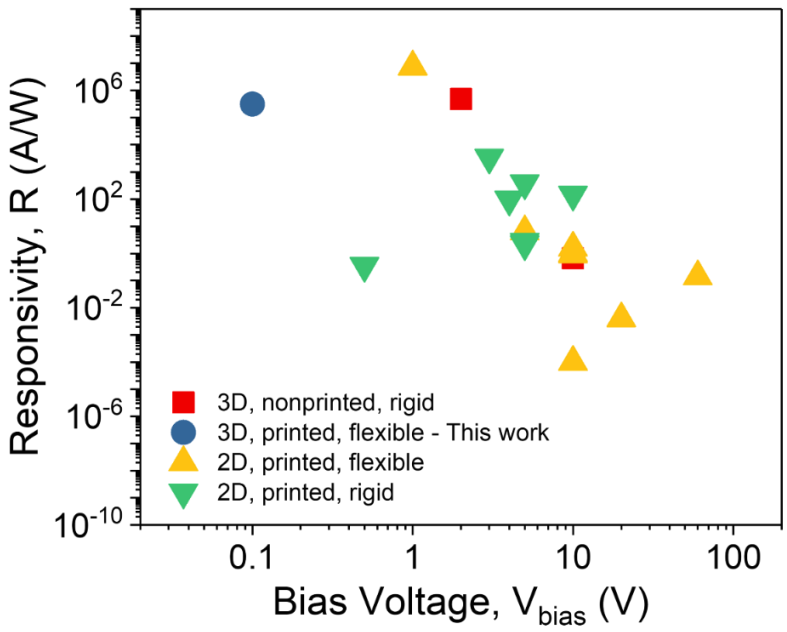

Figure 5-13. Responsivity comparison between this work and other 3D configuration and 2D printed PDs reported in literature.

The out-of-plane ZnO NW-based PD performance was compared with the other state-of-the-art 3D UV PDs and 2D printed PDs and the results are presented in Figure 5-13 and summarised in Table 5-2. So far, the reported 3D PDs have been obtained by hydrothermally grown ZnO NWs on crystalline 3C-SiC or spin-coating ZnO quantum dots (QDs) on Au nanostructure/anodic aluminium oxide (AAO) matrix. They have been fabricated only on rigid substrates through multiple lithography and etching steps [178, 179]. The 2D printed PDs have been recently studied using inkjet, screen, gravure printing [180-194]. Noticeably, most of the flexible 2D printed PDs exhibit relatively lower responsivity and require a higher bias voltage. As the only flexible PD with 3D printed or out-of-plane architectures, this work presents one of the best photo-responsive performances, exhibiting responsivity (3.16×10^5 A/W), detectivity (2.62×10^{17} Jones) and EQE (1.06×10^8 %) using low bias voltage (0.1 V) under low light intensity (1 μW/cm^2). This is attributed to the high aspect ratio micropillars that have provided the 'base' for NWs and allowed the creation of countless NW-NW junctions in a 3D space. The numerous energy barriers existing in the sensing channel for free charge carriers result in the reduction of dark current and a large change in device current under UV light illumination.

Table 5-2. The 3D printed flexible PDs performance comparison with the state-of-the-art PDs fabricated in 3D and 2D configurations.

2D/ 3D	**R (A/W)**	**D* (Jones)**	**I_{photo}/I_{dark}**	**EQE (%)**	**Printed**	**Flexible**	**Materials**	**P_{in} (μW/cm^2)**	**V_{bias} (V)**	**Ref.**
3D	3.16×10^5	2.62×10^{17}	6.95×10^4	1.06×10^8	EHD	yes	Au/ZnO	1	0.1	This work
3D	0.66	N/A	N/A	225	NO	no	Au/ZnO	6900	10	[179]
3D	4.8×10^5	N/A	187.8	1.69×10^8	NO	no	SiC/ZnO	2.61	2	[178]

2D	$\sim 10^{-4}$	8.14×10^{8}	13.4	N/A	Screen Printing	yes	ZnO	3800	10	[180]
2D	7.5×10^{6}	3.3×10^{17}	10^{6}	N/A	Inkjet	yes	ZnO	9.1	1	[181]
2D	6.4	N/A	10^{3}	N/A	Inkjet	yes	ZnO/TPU	1000	5	[182]
2D	2.2	2.00×10^{11}	10^{3}	N/A	Inkjet	no	ZnO	2.2	5	[183]
2D	0.004	1.45×10^{10}	N/A	N/A	Inkjet	yes	ZnO/Ag	715	20	[184]
2D	0.14	N/A	10^{-3}	N/A	Inkjet	yes	ZnO	500	60	[185]
2D	2.7	N/A	3538	N/A	Inkjet	no	WO_3	0.27	5	[186]
2D	148	N/A	N/A	N/A	Screen Printing	no	ZnO	1000	10	[187]
2D	0.35	N/A	N/A	N/A	Inkjet	no	ZnO	1000	0.5	[188]
2D	383.6	N/A	2470	N/A	Inkjet	no	ZnO	520	5	[189]
2D	1.01	N/A	N/A	N/A	Gravure printing	yes	ZnO	127	10	[190]
2D	0.92	6.19×10^{11}	5.60×10^{2}	N/A	Gravure	yes	PBDTT-*ff*Qx/PCBM	N/A	10	[191]
2D	3386	N/A	N/A	1.20×10^{4}	Inkjet	no	ZnO	50	3	[192]
2D	1.62	7.77×10^{12}	1.83×10^{4}	N/A	Gravure	yes	Perovskite	N/A	10	[193]
2D	97.5	N/A	N/A	35580	Inkjet	no	ZnO	N/A	4	[194]

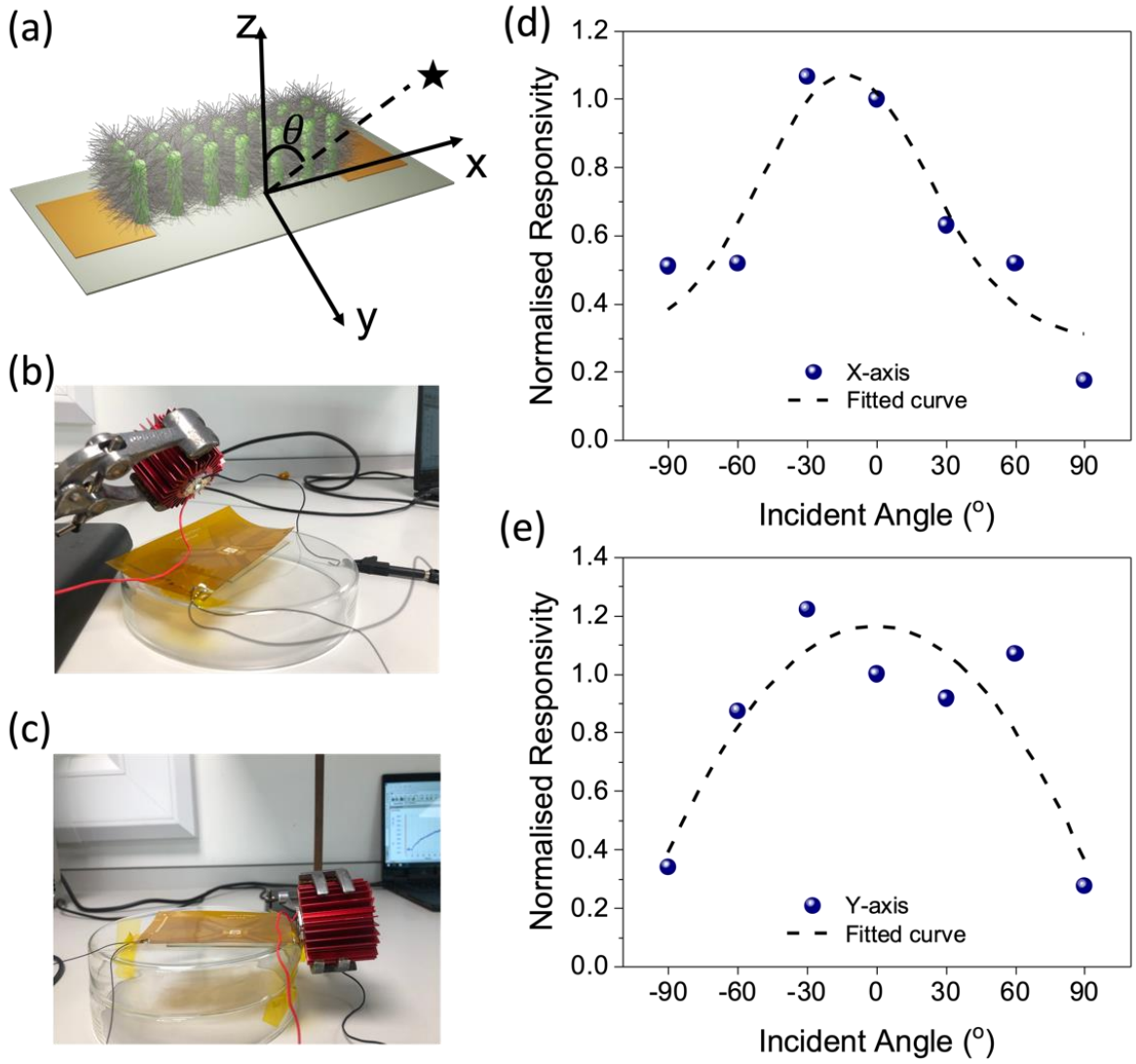

Figure 5-14. Wide angle sensing measurements: (a) Schematic of the wide-angle sensing measurement, showing the light source set at an angle along x and y-axis; Photographs of the measurement set-up: (b) Incident angle at -30o along y-axis; (c) Incident angle at +90o along x-axis; Normalised responsivity extracted from angular response: (d) along x-axis; (e) along y-axis.

The omnidirectional light harvesting capability of the 3D PDs was shown by recording their angle-dependent optical response. The wide-angle photo response was recorded with the light source positioned at the normal position, ± 30º, ± 60º and ± 90º along the x and y-axis. Figure 5-14 (a) presents the schematic of the experimental setup, and Figure 5-14 (b) and (c) show the photographs of the measurement setup. Figure 5-14 (d) and (e) depict the extracted normalised responsivity for all angles and fitted curves. The fitted curves demonstrate a symmetrical function for results obtained along both axes. Interestingly, in comparison with the response at

the 0º light source position (when the UV source is in parallel with the device), the device responsivity tends to decrease with the incident angle increases for both axes. The observed variation in responsivity at different incident angles is caused by the change in the refractive index profile [195]. Most importantly, the PDs' responsivity remained high (~20 % of the responsivity at normal position), despite the variation, even in extreme cases of under ± 90º light illumination, thus showing a strong capability of absorbing and detecting omnidirectional light sources over a broad incident angle due to the arrays of hierarchical structures, increased sensing areas as well as enhanced light-NW interaction [196]. Such excellent light absorption and omnidirectional detection capabilities present an advanced functionality compared with traditional 2D devices and can be advantageous for the development of 3D smart optoelectronic, efficient solar cells, artificial photosynthesis and artificial intelligent systems. For example, the out-of-plane NW network on the flexible solar cells offers unique advantages in terms of strong light capture and harvest, even in extreme cases of ± 90º light illumination, and thus could offer the opportunity to improve their conversion efficiency [197]. The one-dimensional (1D) semiconductor NWs, with direct wire paths for charge transport and high surface area for light harvest, are emerging as promising candidates for building photovoltaic (PV) cells. In fact, ZnO NWs have also been adopted in dye-sensitized solar cells (DSSCs) and the out-of-plane presence of such NWs, as shown here, will further advance the research in this area [196].

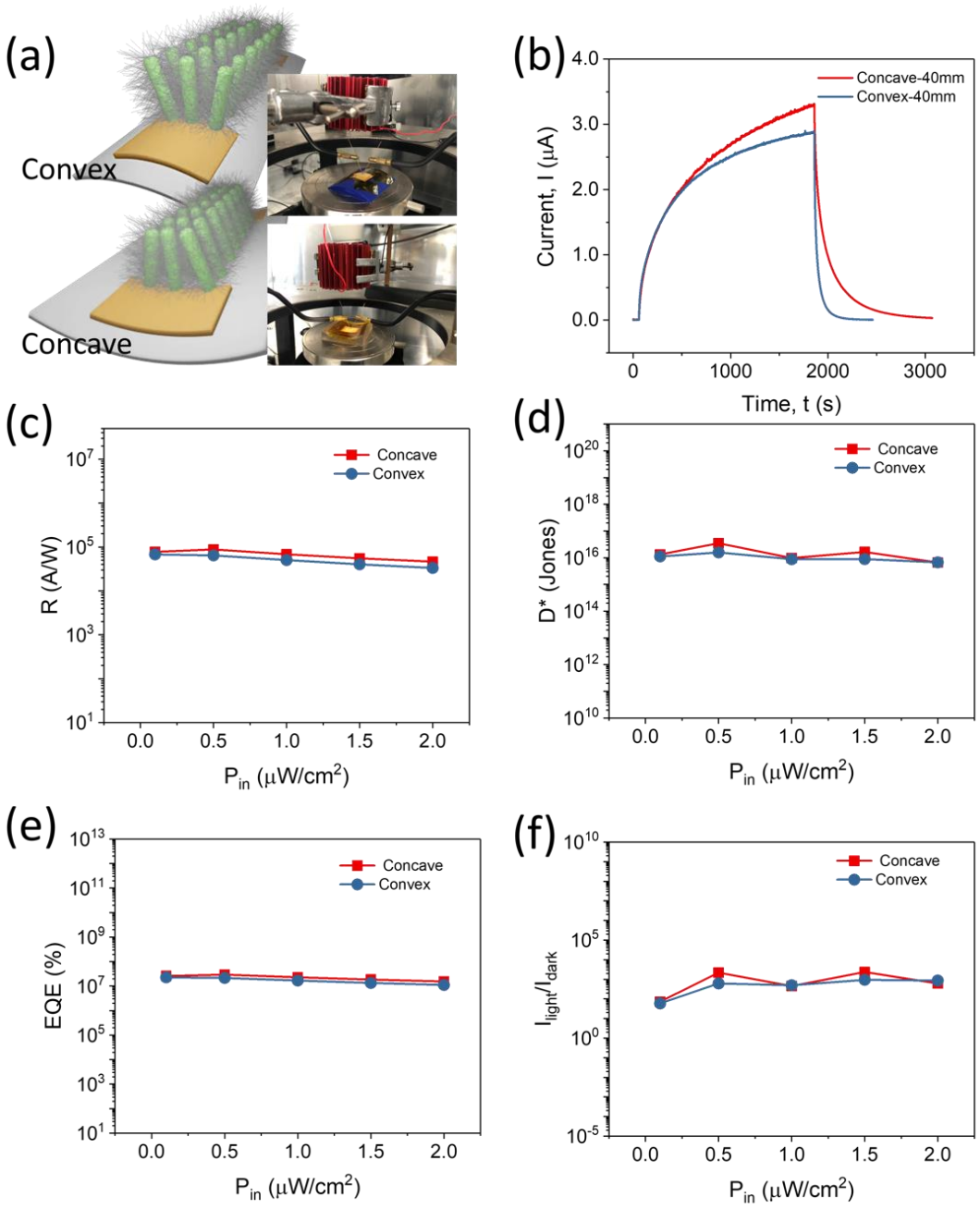

Figure 5-15. Photoresponse under 40 mm concave and convex bending conditions. (a) Schematic and the experimental arrangement during electrical measurements. (b) Time-domain photoresponse curves recorded at 0.1 Vbias and 1 μW cm^{-2} light illumination. Extracted parameters for both bending conditions including: (c) R; (d) D; (e) EQE; and (f) I_{photo}/I_{dark}.*

Next, similar electrical characterisations were conducted under bending conditions (40 mm radius curvature). With the sample mounted on 3D printed concave and convex bending tools (Figure 5-15 (a)), the photo response was studied under different light intensities, from 0.1 to 2.0 μW/cm^2. Figure 5-15 (b) shows the time-domain photo response curves set at 0.1 V_{bias} and

1 μW/cm^2 light illumination under concave and convex conditions. It is apparent that devices under the convex condition presented a slightly lower photocurrent but faster response/recovery time. The minor decrease in photocurrent is owing to the slight increase in the sensing area (channel width reduced from 44 to 48 μm with the fixed 100 μm channel length). Moreover, the response/recovery time dramatically decreased owing to more spaced-out NWs and potentially smoother carrier transport pathways. Further, devices under both bending (concave and convex) conditions with strains applied perpendicular to the sensing channel were also investigated (Figure 5-16). The response/recovery time showed a similar trend as the case of the strain parallel to the sensing channel. However, the change in the photocurrent was negligible when compared to the devices under the parallel strain. This was possibly because when the strain was applied perpendicular to the channel, the sensing area remained approximately unchanged for planar, concave, and convex conditions, leading to a negligible change in the device performance under both concave and convex conditions. Nevertheless, all parameters extracted (R, D*, EQE, I_{photo}/I_{dark}) under different bending and strain conditions revealed a stable performance and insignificant difference.

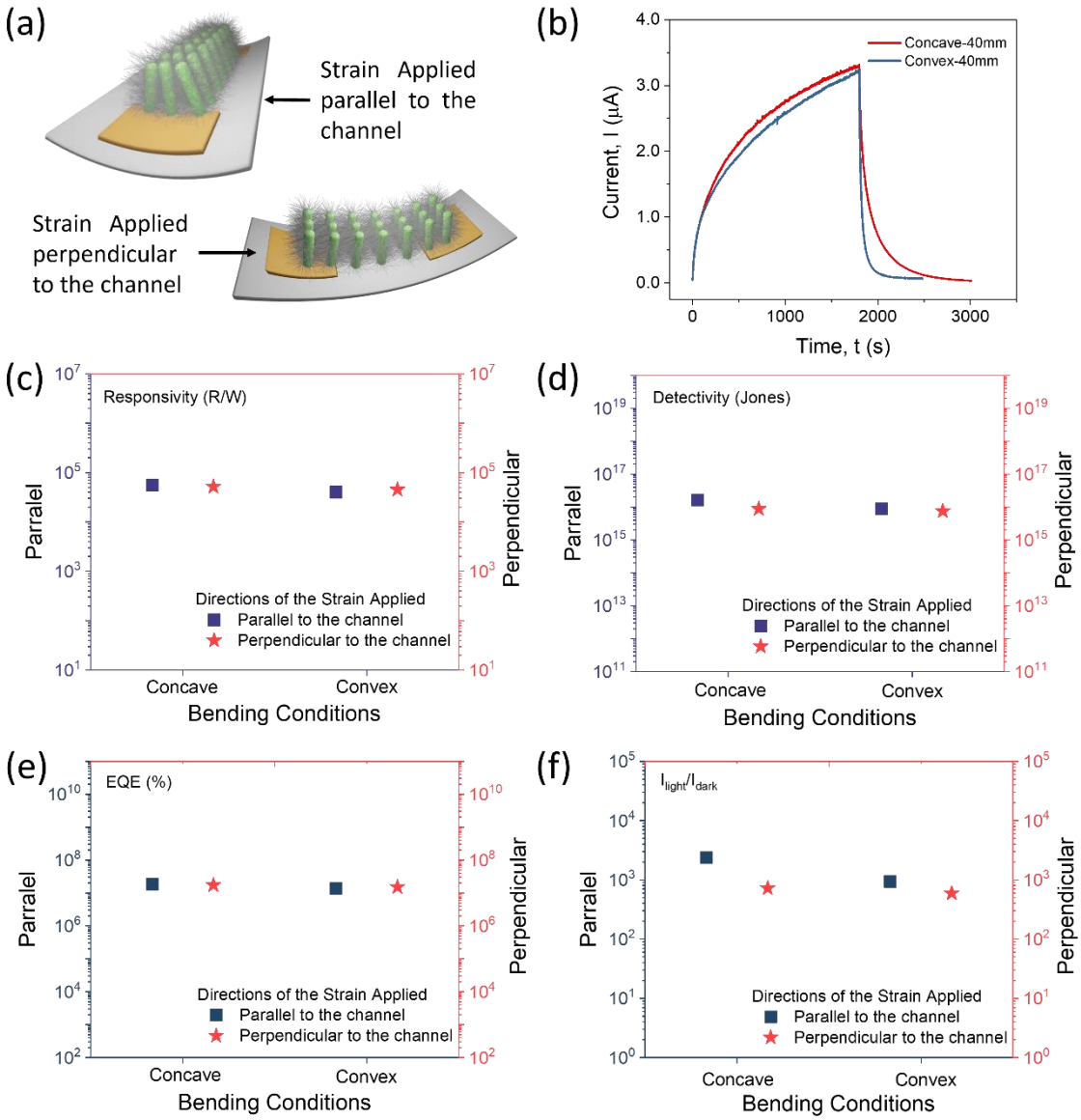

Figure 5-16. PD characterisation under different bending conditions: (a) Schematic of the concave case for two different bending setups including applying the strain parallel and perpendicular to the device sensing channel; (b) Time-domain curve of the device with strains perpendicular to the channel under concave and convex bending conditions; Comparison of extracted values of devices with both strain conditions under concave and convex bending: (c) Responsivity; (d) Detectivity; (d) EQE; (f) I_{light}/I_{dark}.

5.4 Conclusion

In accordance with the motivation to create wire-bonding-like interconnects through EHD printing, the fabrication of high aspect ratio Au-based micropillar electrode arrays (MEAs) on

flexible substrates was successfully achieved. The developed method could be used to obtain different shapes of multi-length-scale out-of-plane architectures with different spacings. The presented printing approach was versatile, which could lead to new opportunities for applications such as high-resolution interconnects for heterogeneous integration or the out-of-plane NW network coating to trap or soak the light. Therefore, this chapter also showed the developed, novel 3D hierarchical functional architecture through growing out-of-the-plane NW networks by employing seedless hydrothermal synthesis. This was expected to enhance the light scattering events and thus, lead to a higher trapping of the incident omnidirectional light (to enhance the light flux). Therefore, the method could be employed to enhance the energy harvesting efficiency of solar cells and artificial photosynthesis processes. To demonstrate this, the fabricated hierarchical architectures were employed to fabricate 3D flexible UV PDs. The 3D PDs, formed with the optimised micropillar spacing, showed one of the best photo-responsive performances, including detectivity (2.62×10^{17} Jones), responsivity (3.16×10^{5} A/W) and EQE (1.06×10^{8} %) at low bias voltage (0.1 V) and light intensity (1 μW/cm^2). The fabricated 3D PDs' sensing performance was tested over wide light incident angles (± 90°). The photocurrent ratios at an incident angle to normal incidence were extracted and exhibited good omnidirectional light absorption ability. Furthermore, the 3D PDs were tested under both concave and convex bending conditions and demonstrated excellent mechanical flexibility with negligible changes in performance. The presented study demonstrates the potential of high-resolution EHD-based jet printing towards 3D conductive and functional structure fabrication and opens new directions for high-performance flexible electronics.

Chapter 6. Interconnects Based on High-Resolution Printing Techniques for 3D Integrated Flexible Electronics

6.1 Introduction

As discussed in Chapter 5.1, electrohydrodynamic (EHD) printing was introduced to explore the possibility of forming printed wire-bonding-like interconnects. Following successfully achieving printed high aspect ratio micropillars, attempts to print wire-bonding-like interconnects have been undertaken and several challenges have been faced. More details are explained in the following section. Therefore, a new configuration for UTC bonding on flexible foils has been discovered and is compatible with both extrusion and EHD-based printing systems.

In this chapter, a method to form vertical interconnects for enabling high-density FHE is proposed using high-resolution EHD- and extrusion-based direct-ink writing (DIW) printers. Further, comprehensive studies are performed to: (i) compare and benchmark the printing speed and throughput of both printers, (ii) perform the electrical performance comparison of vertically bonded transistors on ultra-thin chips (UTCs), and (iii) evaluate the electrical performance stability of FHE system (interconnects and bonded UTCs) under mechanical bending conditions. To begin the process of enabling FHE, UTCs are realised by thinning the backside of the Si chips via the reliable lapping process assisted with the poly(methyl methacrylate) (PMMA) sacrificial technique introduced in Chapter 3.2 [23]. Thereafter, UTCs are transfer printed onto flexible polyimide (PI) substrate using the custom-developed direct printing technique discussed in Chapter 4.3 [30, 129, 198]. Subsequently, the transfer-printed UTCs on flexible substrates are embedded in PI by spin-coating a top encapsulation layer. Embedding UTCs in foil is advantageous as it: i) protects devices from the ambient atmosphere, (ii) provides mechanical support for UTC handling due to their fragile nature, (iii) helps to

accommodate stress, such as bending-induced stress, ensuring that UTCs endure larger stress without breakage, and (iv) prevent toxicity caused by material erosion such as aluminium, silicon dioxide, etc., especially for human implantable applications [49]. After embedding, the vertical interconnection accesses (VIAs) are achieved by following conventional photolithography and plasma etching steps to expose the contact electrodes of the devices on UTCs. Finally, conductive nanoparticle-based ink and paste are filled in VIAs using high-resolution printing systems to form vertical interconnects, accessing the devices in embedded UTCs. The performance of Metal-Oxide-Semiconductor Field Effect Transistors (MOSFETs) devices in embedded UTCs with printed vertical interconnects is comprehensively investigated at each fabrication step. The FHE system which includes vertical interconnects and transistors is also studied under concave and convex bending conditions.

6.2 Challenges in the Planar Integration

The possibility of adopting EHD printing for forming interconnects with UTCs in the planar configuration (wire-bonding-like) was firstly explored. As only low-viscosity inks are compatible with EHD printing, forming out-of-plane structures on two different planes is difficult to achieve, especially in the case of printing interconnects with UTCs including covering the step height, unlike the case of forming conformal structures covering the chip step height using extrusion printing (Chapter 4). Hence, UTC interconnects in the planar configuration (wire-bonding-like) on flexible substrates can potentially be conducted in two different ways: (1) Firstly forming a ramp structure by the side of UTCs, subsequently printing conductive lines on top of the dielectric ramp structure; or (2) Taking advantage of the capability of printing high aspect ratio out-of-plane structures, printing tracks on UTCs and flexible substrates, as well as bridging the conductive lines from two different planes in the

form of an arch shape, covering the step height (= UTC thickness, 35 µm in this work). The method (1) involves the formation of the ramp structure, which, if using the printing route, would prolong the process significantly. If not using the additive manufacturing route, the ramp structure could be created by placing chips on the non-conductive adhesive (NCA) after dispensing the NCA [76]. However, this process could easily cause uneven structures of the NCA ramp, control over the NCA dispensing amount as well as the placement of UTCs needs to be extremely accurate, as any misalignment could lead to uneven NCA and thus ununiform conductive tracks, ununiform resistance of the interconnects and eventually poor device performance. Therefore, in this section, method (2) was explored for realising EHD-printed UTC interconnects. Despite successfully achieving out-of-plane micropillar structures with the highest aspect ratio, printing structures involving bridge-like arches stemming from two different planes is extremely difficult. The challenges faced are summarised as follows:

1) After the thorough optimisation for obtaining high aspect ratio micropillars (Chapter 5.2), freeform arch printing on the same plane (substrate) was subsequently explored. Figure 6-1 (a) demonstrates the attempted arch arrays by printing one side of the arch shape first, followed by the other half of the arch. The half arch on the left-hand side in Figure 6-1 (a) was formed by normal, vertical pillar printing then tilted pillar on top by moving the substrate stage 0.5µm per two droplets. However, the opposite half of the arch on the right-hand side was challenging to print. The issue lies in the effect of the electric field. While the other half was being printed, the left-hand side tilted pillars would constantly move, bend, and contact the nozzle, which disturbed the printing for the other half of the arch. One of the solutions was to anneal the sample after printing for one side. Alternatively, to avoid time-consuming and multiple annealing, arch shapes were achieved by printing both sides at the same time by moving the substrate stage in alternate directions. Figure 6-1 (b) shows the successfully printed arch using the alternative method.

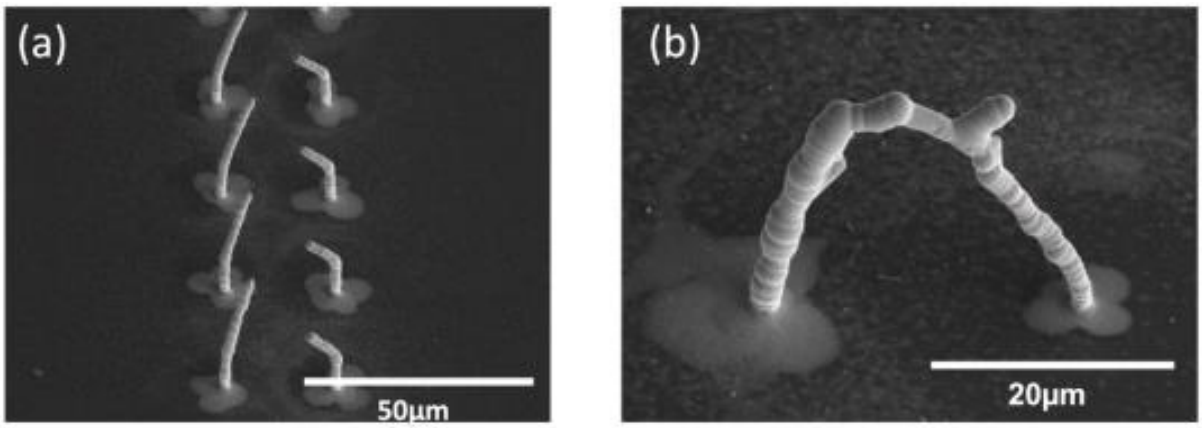

Figure 6-1. SEM images of attempted arch array printing.

2) After successfully obtaining printed arches on the same plane, interconnect printing was then explored with UTCs on flexible substrates involving arch printing on two different planes, as the motivation was to omit the step of dielectric printing and form directly out-of-plane wire-bonding-like interconnects. Attempts were undertaken and it was found that it was extremely challenging to connect the tilted pillars built on different planes (from the flexible substrate and the UTC), and there was severe ink spreading on the side of UTC, which could lead to interconnect short-circuiting through the doped Si-UTC substrate (Figure 6-2 (a)).

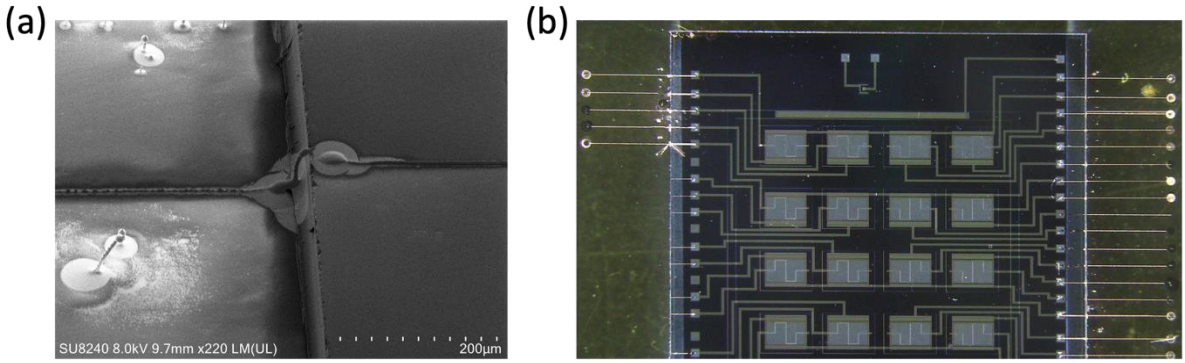

Figure 6-2. (a) SEM images of UTC interconnects formed by EHD printing without dielectric layer; (b) Optical image of EHD bonded UTC after depositing dielectric layer.

3) To address the challenge mentioned in point 2, creating the dielectric layer before interconnect printing became unavoidable. In the case of interconnects by extrusion printing, conductive tracks were formed after dielectric ink printing (nanosilica/epoxy) to avoid interconnects short-circuiting from the highly doped Si substrate. Because of the high viscosity

of the extrusion printing paste, interconnects can be successfully conformally constructed on the dielectric surface without ink spreading, and the dielectric layer was only required to be printed where needed. However, even in the case of extrusion printing, when printing dielectric layers, the same as the conductive tracks, nozzles must be adjusted manually along the Z-axis to print over the UTC step height. This process often causes the ununiform formation of the printed structures. In this case of EHD printing, despite the capability of freely adjusting nozzles, printing over an ununiform surface is highly challenging. Therefore, 1 μm-thick silicon nitride (Si_3N_4) was deposited using ICP380 to form a uniform dielectric layer before interconnects were printed (Figure 6-2 (b)). However, printing over the UTC step height was still problematic, causing severe ink spreading at the edge of the chip and interconnect discontinuation in some cases.

4) Despite some interconnects successfully formed, high resistance with a large standard deviation (SD) was observed (Figure 6-3). This could be because of the irregularities of the printed structures.

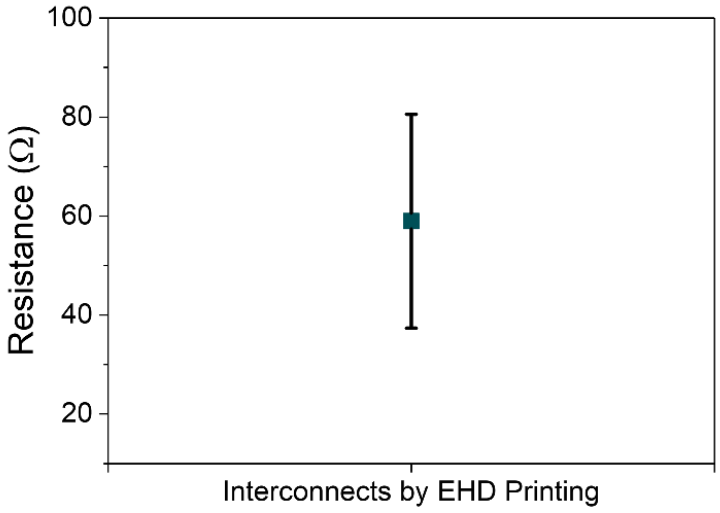

Figure 6-3. Interconnect resistance measured with SD.

6.3 UTC Vertical Integration with Extended Pads

To address all the challenges mentioned above (Chapter 6.2), a new approach has been developed by firstly packaging UTCs, followed by via opening and lastly interconnect printing.

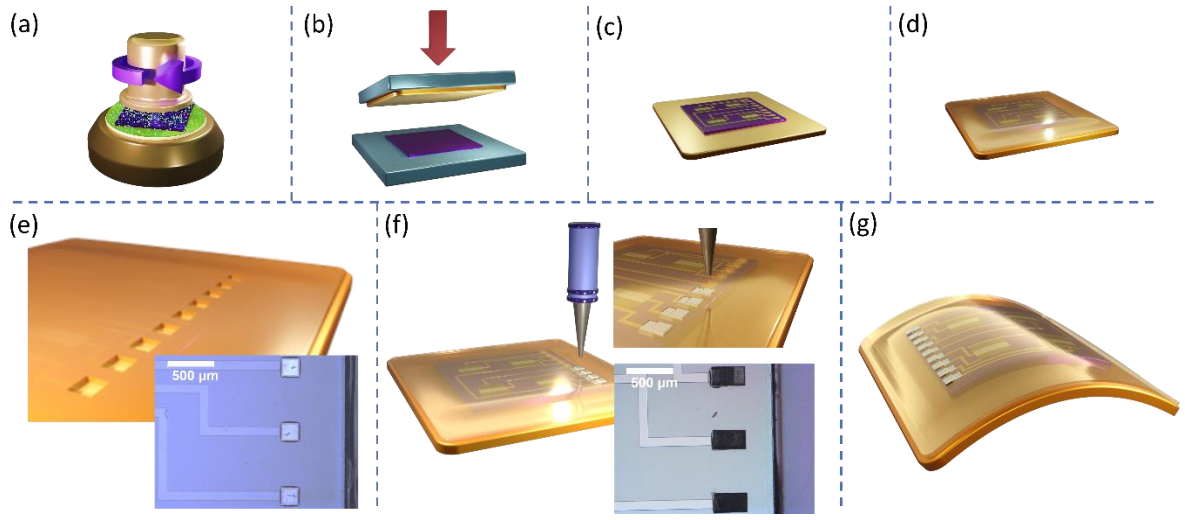

Figure 6-4 Schematics of realising packaged UTCs with printed vias to enable FHE: (a) Chip thinning through lapping with PMMA sacrificial technique; (b) Direct transfer printing of UTCs; (c) Transferred UTCs on flexible substrates; (d) Packaged UTCs; (e) Via opening of the packaged UTCs; (f) Via printing by EHD and Extrusion printing systems; (g) Packaged UTCs with printed vias under bending.

6.3.1. Thinning, Transferring and Packaging of UTCs

Figure 6-4 presents schematic process steps of the optimised UTC fabrication, transferring, packaging, and interconnect printing. Firstly, ultra-thin Si-based metal oxide semiconductor field effect transistor (MOSFET) chips with ~35 µm thickness were fabricated using the developed, reliable backside lapping assisted with the poly (methyl methacrylate) (PMMA) sacrificial technique (Figure 6-4 (a)). The details of the process can be found in Chapter 3. Next, the direct transfer printing approach was adopted using the custom-made setup to transfer and integrate UTCs onto flexible polyimide (PI) substrates (Figure 6-4 (b)). More details regarding the transfer printing process were included in Chapter 4.3 [30]. Lastly, UTCs were encapsulated by spin-coating a thin PI layer (Figure 6-4 (c) and (d)). PI was particularly chosen as the insulating material for UTC packaging due to its excellent properties such as superior

dielectric properties, and favourable chemical, mechanical as well as thermal stability. PI2611 (HD Microsystems) has been specifically selected in this work as its thermal expansion coefficient is close to that of Si to prevent the chip from damaging and/or to avoid delamination of Si chips due to thermal stress generated at the interfaces during annealing.

6.3.2. Realisation of Vertical Interconnects

After chip packaging, contact electrodes of MOSFET devices need to be exposed. As PI2611 is not photo-definable, laser-based techniques (frequency tripled neodymium-doped yttrium aluminium garnet (Nd-YAG) laser and CO_2 based laser) [143] and plasma (inductively coupled plasma (ICP) [199] and reactive-ion etching (RIE)) techniques have been explored for PI selective removal. Nd-YAG laser is known to be challenging for controlling the stopping point. Due to the higher power in the centre of the Gaussian beam in the YAG laser, it can easily cause damage in the centre of the contact electrode with poor edge quality [200]. The alternative to the Gaussian beam is using a shaped beam. However, it presents poor repeatability. YAG laser technologies have also been found to have limited minimum achievable diameters of VIAs (~35 – 50 µm) [143, 201]. It has been observed that a CO_2 laser is a more effective solution than the YAG-laser as some of the embedded metal layers, such as aluminium, can serve as a stopping point. This is because these metals reflect infrared and the CO_2 laser is operated in the infrared spectrum [202]. The CO_2 laser is usually adopted with an etch mask for a finer VIA pitch. However, the PI residue is often found on the contact electrode owing to the locally absorbed heat preventing the thin PI residue layer from reaching the melting and evaporation temperature. Hence an extra excimer laser clean step is inevitable in this case [143]. ICP etching is another commonly used technique for micro-VIA formation [203]. Despite the high precision and aspect ratio that can be achieved, hard masks are mandatory, adding more cost and additional processes. As the PI specifically selected for this

work, PI2611, is not photosensitive, RIE etching has been adopted to achieve the residue-free micro-VIA opening after photolithography (Figure 6-4 (e)).

Firstly, the packaged sample was spin-coated by an adhesion promoter, hexamethyldisilazane (HDMS), at 4000 rpm for 5 s, followed by soft-baking at 115 ºC for 1 min. The sample was then spin-coated by a viscous photoresist, AZ4562, at 2000 rpm for 30 s. The viscous photoresist was selected to ensure good protection of the packaged UTC during the PI etching process. The sample was then kept at room temperature for 15 min to allow most of the solvent to evaporate. This was to prevent the resist surface from drying fast and causing the trapped solvent to form bubbles and lift the resist film. After, the sample was soft-baked at 100 ºC for 50 s. Subsequently, via openings, 200 µm × 200 µm (same dimension as the MOSFET electrodes), were defined using the SUSS Mask Aligner MA6 with a constant intensity of 7.2 mW/cm^2 for an exposure time of 21 s. After, the exposed resist was developed using dilute AZ400K (1:4 with RO water) and the post-bake following the development was conducted at 115 ºC for 50 s. After photolithography, photo-defined electrical pads were exposed through RIE (5/95 sccm CF_4/O_2, 200 W, 20 mT for ~15 min). At last, the photoresist was removed by dipping in an acetone bath. Figure 6-5 shows the contact profile of the micro VIAs after dry etch.

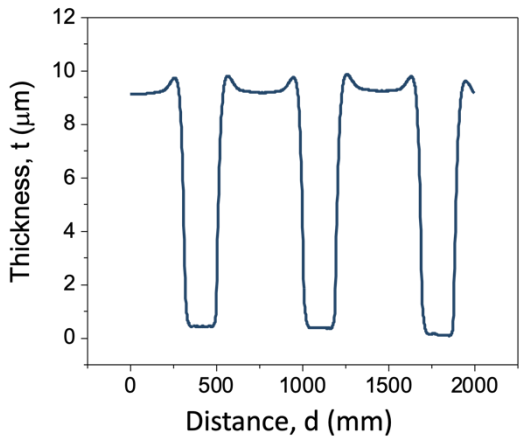

Figure 6-5. Contact profile of packaged UTCs after dry etch.

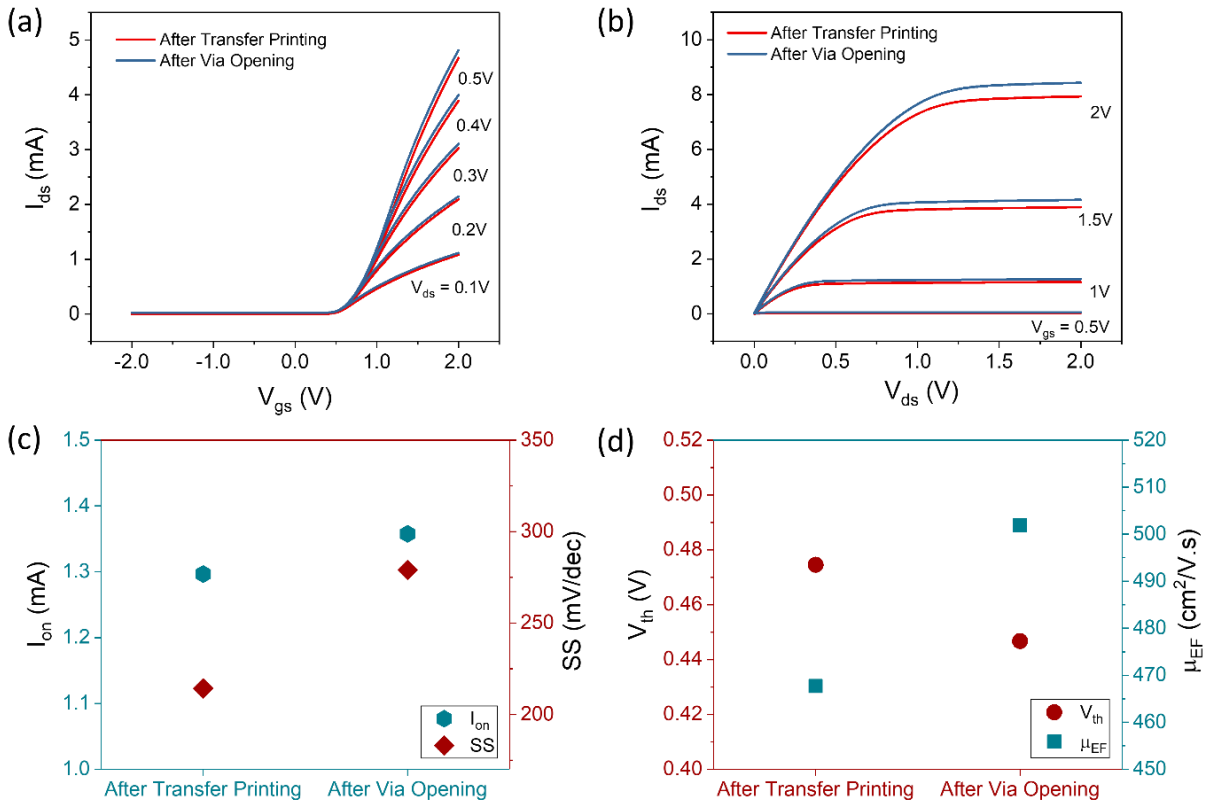

Figure 6-6. MOSFET device characterisation before and after via opening: (a) Transfer characteristics; (b) Output Characteristics; Extracted parameters at V_{ds} = 0.1 V (c) I_{on} and SS; (d) V_{th} and μ_{EF}.

The reliability of the optimised thinning and transfer printing processes has been confirmed in the previous Chapters (Chapter 3 and Chapter 4). In this chapter, the effect of the VIA-opening process was firstly evaluated by investigating the n-channel MOSFET device performance before and after VIA-opening. Figure 6-6 (a) presents the transfer characteristics (I_{ds} – V_{gs}) during the sweep of the gate-source voltage (V_{gs}) from -2 to 2 V at different drain voltages (V_{ds}) from 0.1 to 0.5 V with a step of 0.1 V. Figure 6-6 (b) shows the output characteristics (I_{ds} – V_{ds}) during the sweep of V_{ds} from 0 to 2 V at different V_{gs} from 0.5 to 2 V with a step of 0.5 V. Both transfer and output curves demonstrated the typical n-channel MOSFET behaviours with excellent gate control over the semiconducting channel. To further investigate the influence of the micro-VIA opening process on the device performance, key parameters were

extracted using the transfer scans performed at V_{ds} = 0.1 V before and after chip packaging and VIA opening, including device on-current (I_{on}), threshold voltage (V_{th}), subthreshold swing (SS) and the peak field-effect mobility (μ_{EF}). The I_{on} was obtained from the transfer curve at V_{gs} = 2V and V_{th} was accessed from the linear region of the transfer characteristic using the linear extrapolation method to select the intercept value at I_{ds} = 0. Next, SS was extracted using Equation 3-2. At last, μ_{EF} was obtained using Equation 3-4 after extracting transconductance (g_m) using Equation 3-3. I_{on} and μ_{EF} both revealed a slight increase after VIA opening. The I_{on} increased from 1.30 to 1.36 A and μ_{EF} from ~467 to ~501 cm^2/V.s. It is known that when exposing the bonding pads to ambient air, a layer of organic hydrocarbon and/or, for reactive metals such as aluminium (Al), a thin layer of metal oxide will form on the surface. Conventionally, to achieve reliable interconnects and chip packaging, the surface of all the internal interfaces must be cleaned to ensure good adhesion. It could be assumed that the electrical pads, Ti/Al:Si (60/600nm), had a thin native oxide layer on top which could be the reason for showing poorer performance (as it would add an extra resistance in series) before processing. During the dry etch process for VIA opening of the packaged UTCs, the native oxide layer was then removed, which consequently decreased the contact resistance of the electrical pads. Therefore, I_{on} and μ_{EF} showed a slightly improved value. However, the shift in V_{th} and SS indicated that long plasma exposure had possibly caused the generation of minor defects in the gate oxide. Under the plasma ambience, electrodes constantly collected ions and electrons. Such steady-state voltage could lead to electrical stress on the MOS devices, giving rise to charge trapping in the oxide and interface traps at the SiO_2-Si interface, potentially weakening the oxide layer [204]. Figure 6-7 shows the percentage (%) change in key parameters after VIA-opening for 15 devices from 5 different chips.

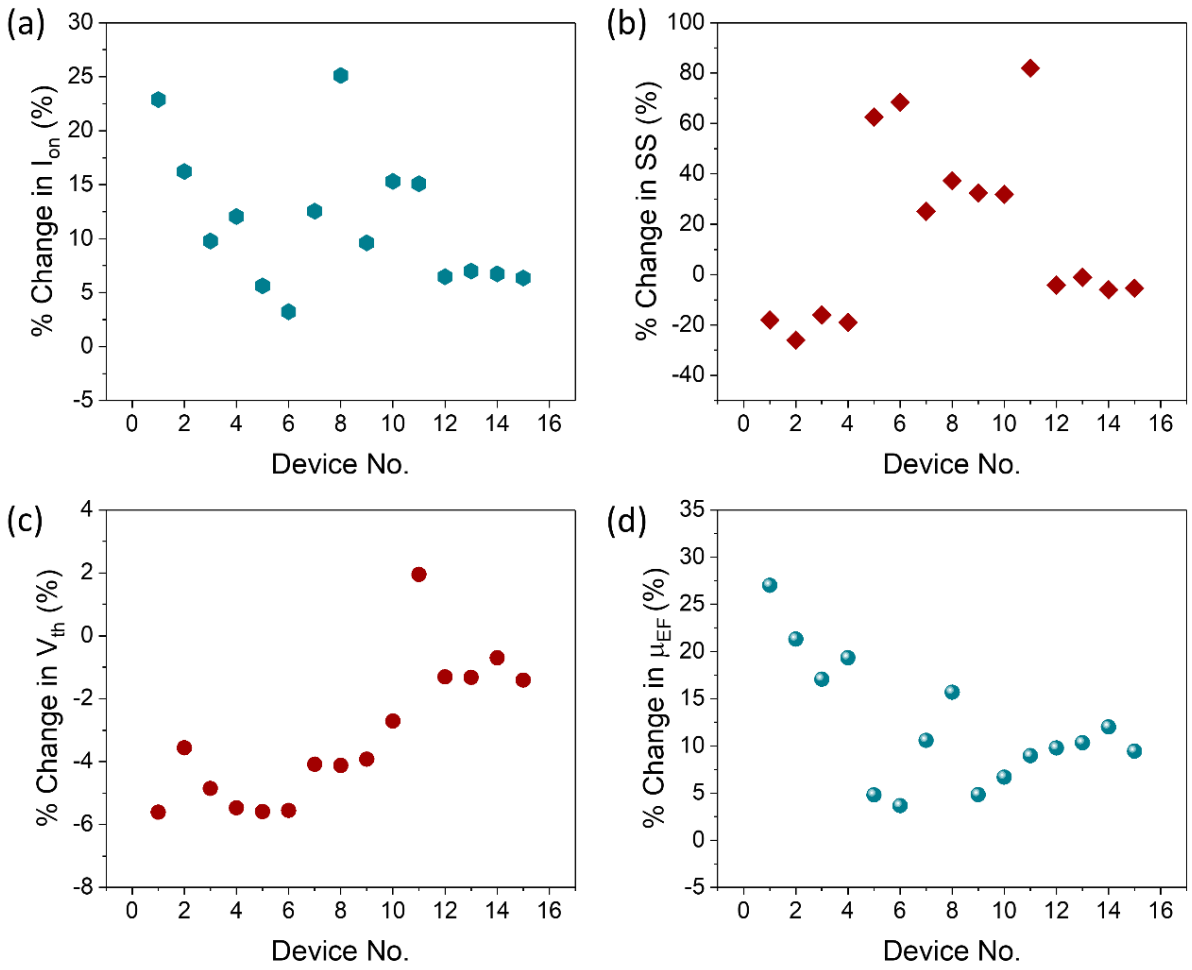

Figure 6-7. % Change in extracted parameters of 15 devices from 5 different chips between the original MOSFET performance and after via opening (including after thinning, transferring, packaging): (a) I_{on}; (b) SS; (c) V_{th}; (d) μ_{EF}.

6.3.3. Evaluations of Printed Interconnects

After realising micro-VIAs, high-resolution extrusion and electrohydrodynamic inkjet (EHD) printing systems were explored to investigate the suitability of forming printed interconnects for packaged UTCs. A series of experiments were conducted for the performance evaluation and benchmarking of these high-resolution printers in forming vertical interconnects. Firstly, lines with varying lengths, ranging from 20 to 1500 µm were printed with different numbers of layers (from 1 to 10 layers) on a flexible PI film using silver (Ag) inks for both systems (Ag nanoparticle ink for EHD system, Ag nano paste for the extrusion system as presented in

Chapter 4.2.2). Figure 6-8 (a) and (b) indicate that the measured resistance increases with the increment of the printed line length for the same number of printed layers. Meanwhile, the resistance decreases with the increment of the printed layers for the same printed distance. Figure 6-8 (c) and (d) present the geometric measurements for all printed lines, showing the thickness and width of lines with different numbers of layers. As the printing substrate had experienced the same plasma pre-treatment, the surface energy remained the same for both studies. It can be concluded that the difference in results is attributed to the ink properties. It is expected that printed lines formed by Ag nano paste present a larger thickness than the metallic nanoparticle inks as the paste contains a higher metal content and has significantly higher viscosity. Interconnects printed by Ag NP ink suggest a lower contact angle with more ink spreading. This could be also because of the difference in their ink/paste's viscosity. Studies have suggested that inkjet printing is compatible with low-viscosity inks which present Newtonian behaviour and the ink/paste adopted for extrusion printing is the opposite [205]. However, higher aspect ratio interconnects can be achieved with the EHD printing system by tuning the printing parameters. Nevertheless, in this case, a lower resistance is more important.

The optimal printing speed was also studied to evaluate both printing systems. For both systems, as can be seen from Table 6-1, the printing speed and/or printing parameters for a desired resistance become a trade-off. The faster the printing speed, the higher the resistance of the printed interconnects with the same printing parameter applied. In terms of printing parameters, a higher pressure with the extrusion system can achieve a lower resistance with the same printing speed. The same also applies for the EHD system with the voltage set. It may appear that EHD printing for each layer is faster than extrusion printing, however, because of the higher metal content and viscosity of the nano-paste compatible with the extrusion system, fewer printing layers are adequate for extrusion printing. For instance, 3 layers of extrusion printing for obtaining 1000 μm length lines showed approximately the same resistance as 10

layers of EHD printing, as can be seen from Figure 6-8 (a) and (b) using the parameters set in this work. However, as printing parameters for both systems can be manipulated to achieve the desired resistance of interconnects, both systems present the capability for providing similar throughput.

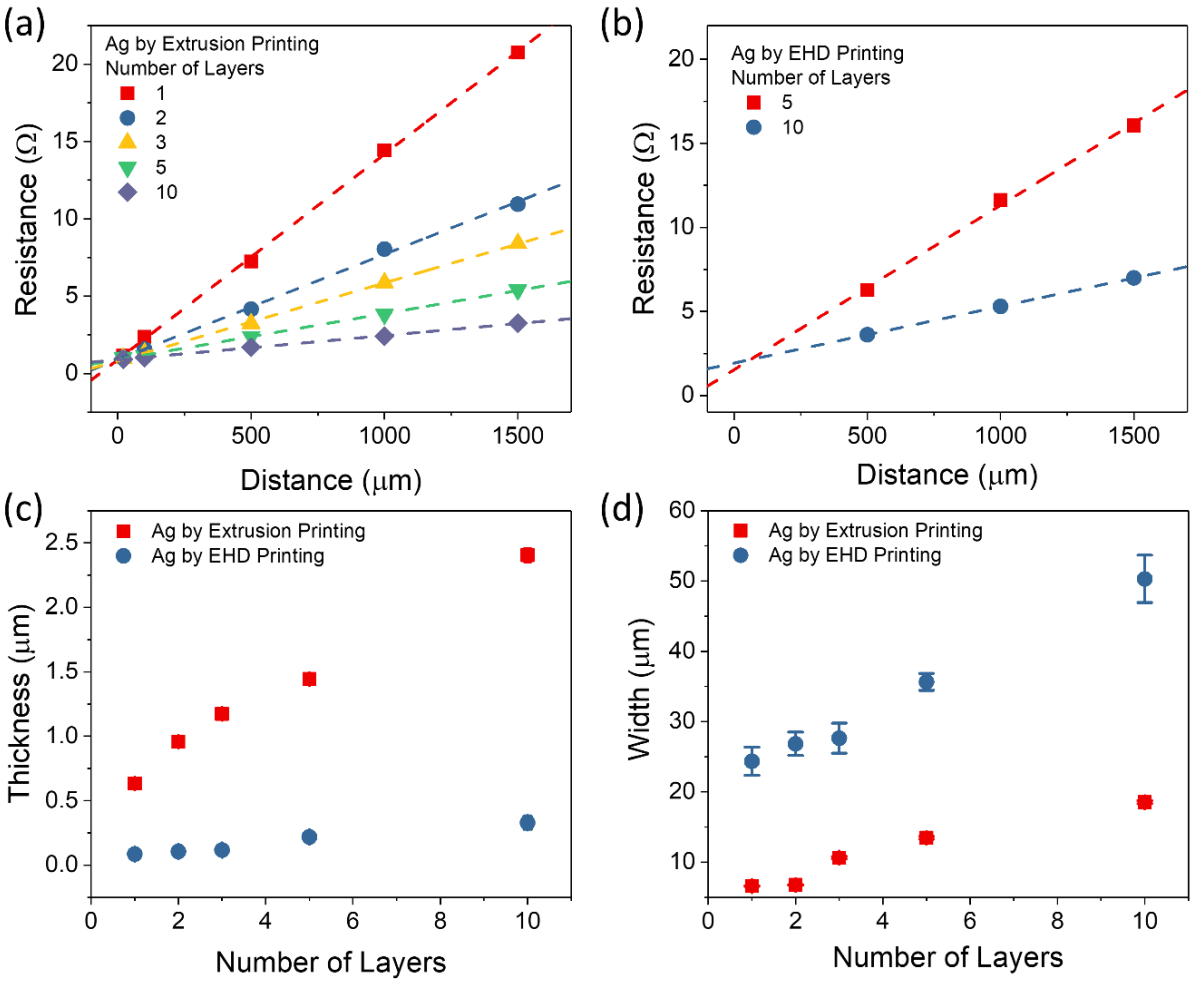

Figure 6-8. Ag Interconnect geometries by extrusion and EHD printing with different number of layers (a) Thickness; (b) Width; Resistance vs. Ag interconnect lengths with different numbers of layers by (c) Extrusion printing; (d) EHD printing.

Table 6-1. Printing parameters and throughput studies for EHD and extrusion systems.

Printing Mechanism	Printing Speed (mm/s)	Printing Parameter	Time Spent for Printing 1000um-Length Interconnects (s)	Interconnect Resistance (Ω)
EHD	0.4	Voltage = 275V	28.196 (10 layers)	5.3
Extrusion	0.07	Pressure = 6.5 Bar	14.951 (1 layer)	14.43426
Extrusion	0.07	Pressure = 6.5 Bar	154.366 (10 layers)	2.40214
Extrusion	0.4	Pressure = 6.5 Bar	36.461 (10 layers)	14.487
Extrusion	1	Pressure = 6.5 Bar	22.061 (10 layers)	25.55
Extrusion	1	Pressure = 8 Bar	22.061 (10 layers)	17.87
Extrusion	1.5	Pressure = 6.5 Bar	18.461 (10 layers)	51.57
Extrusion	2	Pressure = 8.5 Bar	17.561 (10 layers)	47.04

Both systems therefore were explored for realising electrical vias for packaged UTCs. Interconnects were formed by printing Ag ink with the EHD system and Ag paste with the extrusion system from the exposed electrodes to the top PI of the packaged UTC including covering the step height (= the thickness of the top PI) of 4 µm. Accordingly, the MOSFET devices were evaluated with these printed vias (Figure 6-9). Figure 6-10 presents the measured resistance of all printed vias, showing low and consistent values for both systems (less than 2 Ω). It is clear that the standard deviation of the measured resistance in this newly developed approach is drastically less than the previous approach as mentioned in Chapter 6.2. Figure 6-11 shows 4 device performances with printed vias by each printing system. It was expected that I_{on} showed a minor degradation after forming the printed vias due to the added resistance of interconnects, which decreased μ_{EF}, as discussed in Chapter 4.2.3.

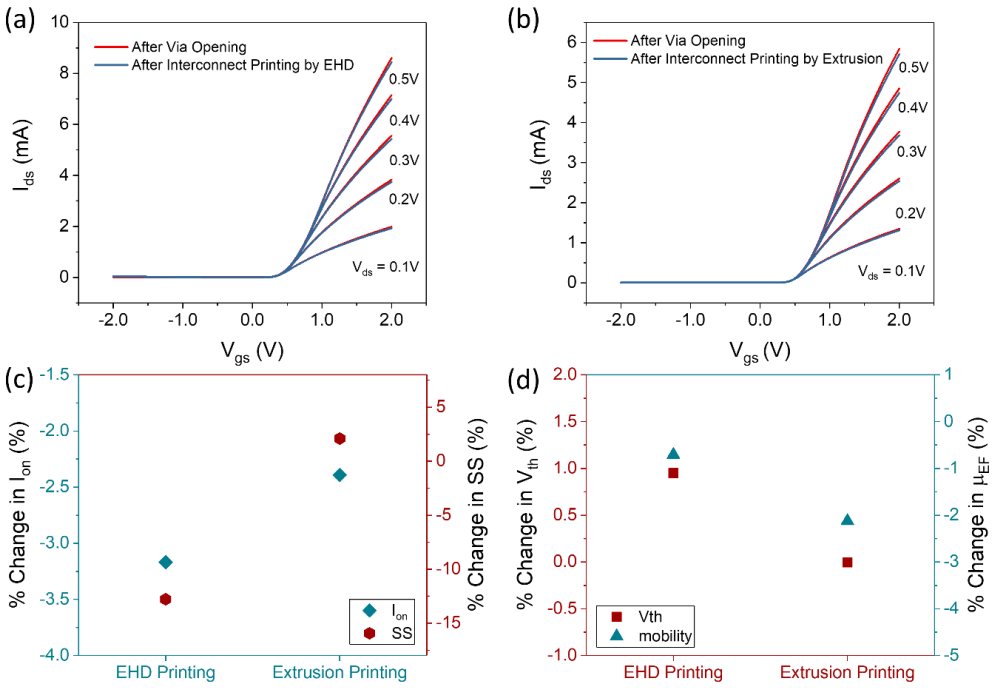

Figure 6-9. MOSFET device performance before and after via printing using Ag ink by EHD and extrusion printing systems: (a) Transfer characteristics for devices with vias formed by EHD printing; (b) Transfer characteristics for devices with vias formed by extrusion printing; Extracted parameters at V_{ds} = 0.1V: (c) I_{on} and SS; (d) V_{th} and μ_{EF}.

Devices with EHD printed vias presented a marginally larger variation in I_{on} and μ_{EF}. This could be due to the interface difference between the Ti/Al pad and the printed structures. As discussed before and shown in Figure 6-8, a larger standard deviation was observed for lines printed with Ag nanoparticle ink because of the smaller nanoparticle size, lower viscosity, and less metal content. The larger variation in V_{th} and SS for EHD samples could be attributed to the thermal stress from a slightly longer curing time for Ag nanoparticle ink (1 – 2 hrs, 15 – 30 mins for extrusion printed structures), in addition to the previous defects caused by long time plasma for via opening (sample 1 – 4 in Figure 6-11 are the same samples (No. 1 to No. 4) in Figure 6-7). Nevertheless, Figure 6-12 summarises the % change in extracted parameters between the original device performance (before thinning, transfer printing, packaging, dry etch) and after vias realised by EHD and extrusion printing, indicating an overall minor change in all devices and confirming the reliability of the entire integration process.

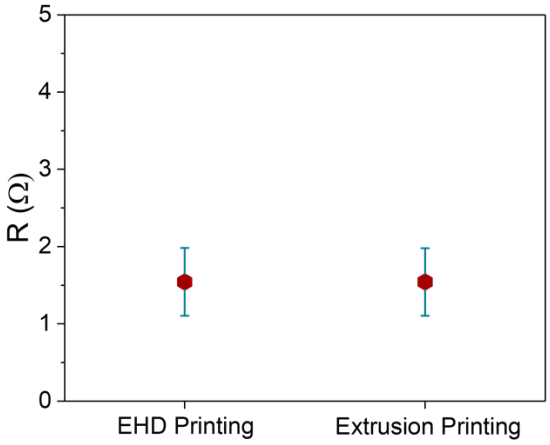

Figure 6-10. Resistance of the printed vias on packaged UTCs.

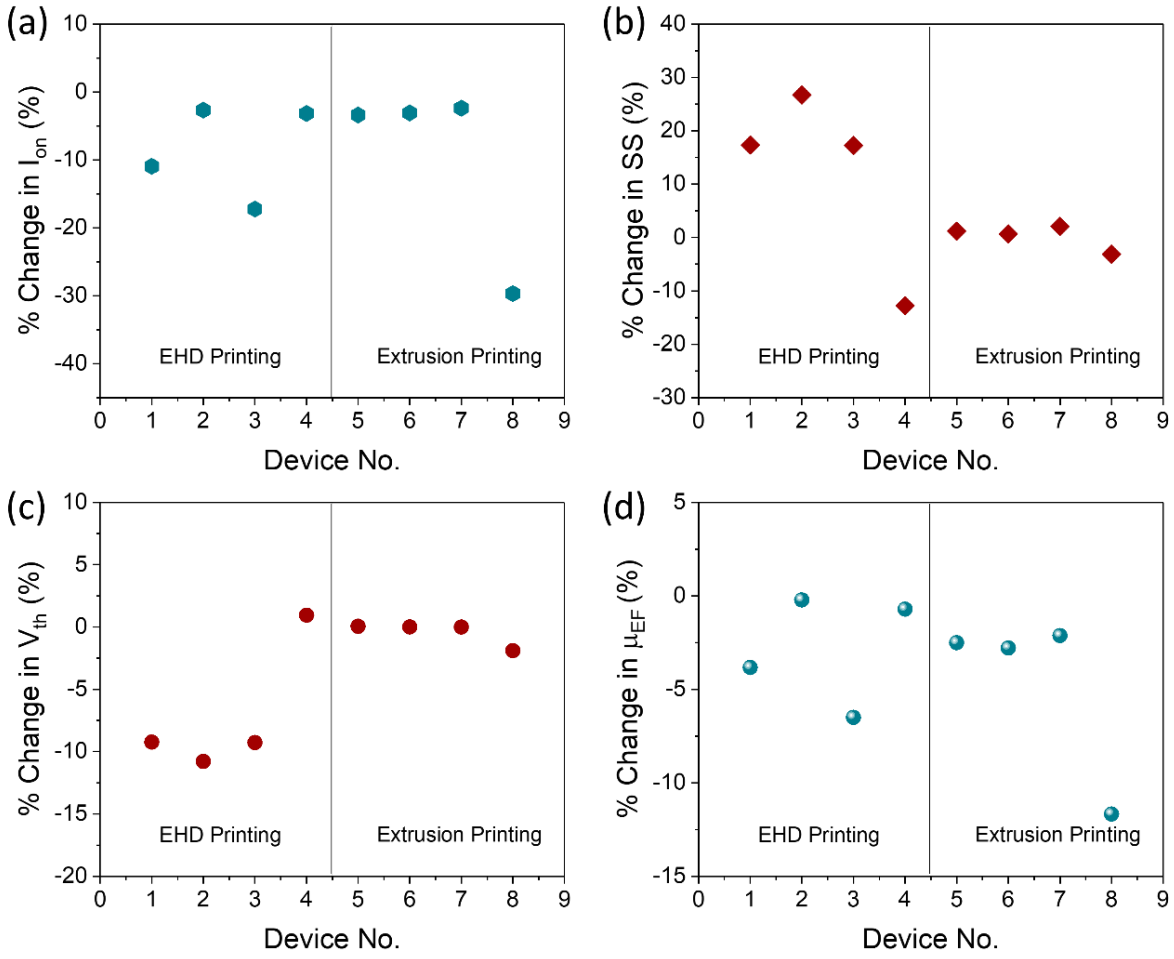

Figure 6-11. % Change in extracted parameters of packaged UTCs before and after vias realised by EHD and extrusion printing: (a) I_{on}; (b) SS; (c) V_{th}; (d) μ_{EF}.

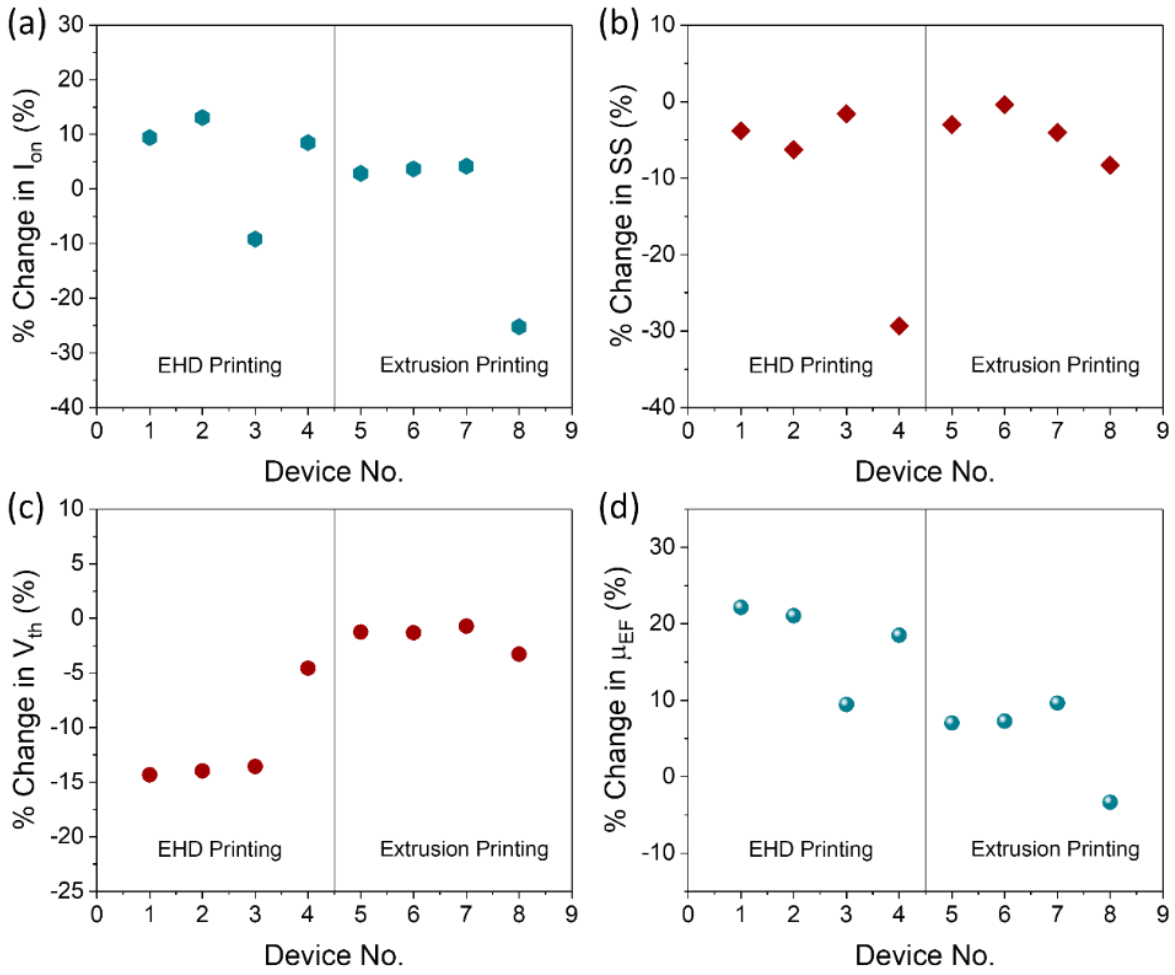

Figure 6-12. % Change in extracted parameters of packaged UTCs between the original performance and after vias realised by EHD and extrusion printing: (a) I_{on}; (b) SS; (c) V_{th}; (d) μ_{EF}.

Further, the device performance was evaluated under static uniaxial concave and convex bending conditions from 40 to 20 mm radii of curvature by attaching the devices to 3D printed tools. Figure 6-13 depicts the transfer characteristics and key parameters for all cases. It was observed that the shift in parameters such as I_{on} and μ_{EF} became larger as the bending radius decreased. The reason for this is explained as follows: The strain (ε) in the location of y of a multi-layered system (embedded UTCs in PI in this case) is expressed as Equation 6-1, consisting of a uniform strain component generated by thermal residual stress and a bending-induced strain [206, 207].

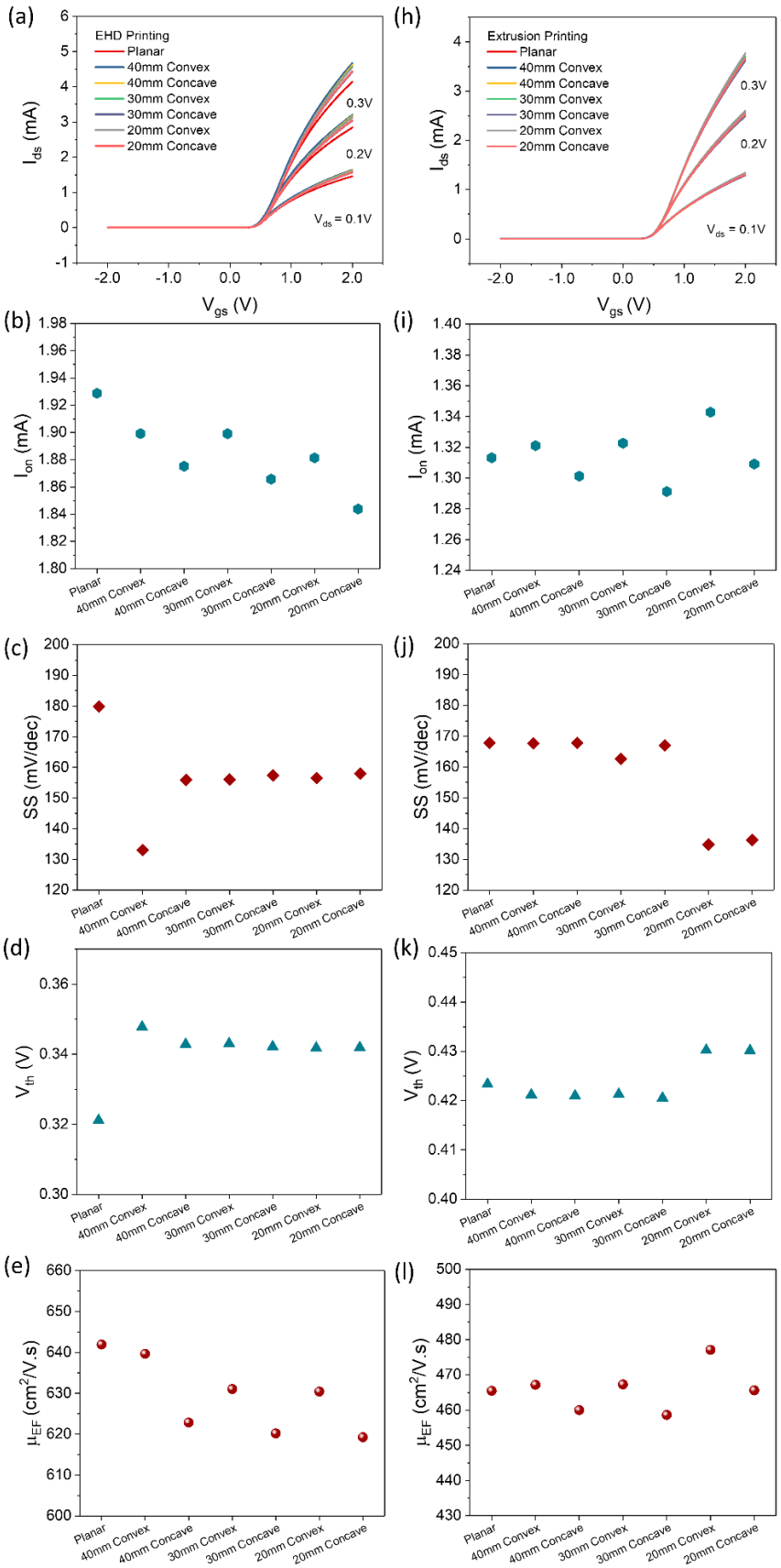

Figure 6-13. Transfer characteristics and extracted parameters under planar and bending conditions for devices with printed vias formed by (a-e) EHD system; (h-k) Extrusion system.

$$\varepsilon = c + \frac{y - t_b}{R} (0 \le y \le yn) \qquad 6\text{-}1$$

$$t_b = \frac{\sum_{i=1}^{n} E_i \times t_i \times (2 \times h_{i-1} + t_i)}{2 \times \sum_{i=1}^{n} E_i \times t_i} \qquad 6\text{-}2$$

where c is the uniform strain component, y is the location where strain is required for calculation, t_b is the location of bending axis, R is the bending radius, E_i is the Young's modulus of the i's material, t_i is the thickness of the i's layer, h_i is the height of the location of the i's layer (the sum of thickness from layer 0 to layer i). In this case, as the embedding material, PI, is carefully selected to match Si's CTE and the printed interconnects occupy very little space of the multi-layered system (the area of printed interconnects < $\frac{1}{125}$ of the UTC), the thermal residue stress has been neglected. Hence Equation 6-1 indicates that the strain is highly dependent on the bending, and it increases with the reduction of bending radius. It is to be noted that this is because mechanical stress can alter MOS devices' electrical properties by reshaping the semiconductor band structure and carrier transport properties [26, 208, 209]. The external strain reshapes the Si band structure by altering the band structure. There are six degenerate valleys, Δ_6. The uniaxial strain splits the conduction band into two sub-bands, Δ_2 and Δ_4. Under convex bending (tensile strain), electron repopulation occurs as more electrons move into the lowest energy sub-band Δ_2. Besides, the strain shifts band edge energies according to the deformation potential theory, indicating that the band edge shift caused by strain is proportional to the strain tensor (Equation 6-3) [210].

$$\Delta E = \sum_{ij} \Xi_{ij} \varepsilon_{ij} \qquad 6\text{-}3$$

where Ξ is the deformation potentials. Such a shift in the energy spectrum therefore impacts the carrier transport properties as the electron repopulation affects the conductivity effective mass (m*) and the momentum relaxation time (τ). In the case of convex bending with tensile stress, the electron repopulation leads to a decrease in the conductivity effective mass. The

concave condition presents the opposite. Devices under convex bending therefore exhibit higher mobility than the concave counterparts (Equation 6-4, Figure 6-13) [211].

$$\mu = \frac{|\vec{v}|}{|\vec{E}|} = \frac{q \times \tau}{m^* \times m_0} \qquad 6\text{-}4$$

where $\frac{|\vec{v}|}{|\vec{E}|}$ is the ratio between the constant average velocity and the electric field applied. q is the electron charge and m_0 is the free electron rest mass ($m_0 = 9.11 \times 10^{-31}$ kg). Additionally, MOSFET devices experience strain at the channel, leading to an additional shift of the energy levels and impacting the mobility due to the electric confinement and the Si/SiO_2 interface scattering. It then leads to the variation of all key parameters including I_{ds}, SS and V_{th} (Equation 6-5) [24].

$$\frac{\Delta\mu}{\mu} + \frac{\Delta C_{ox}}{C_{ox}} = \frac{\Delta I_{ds}}{I_{ds}} = \Pi \times \sigma \qquad 6\text{-}5$$

where Π is the piezoresistive coefficient and σ is the external stress. The devices with printed interconnects by both printing systems present the same trend: a higher I_{on} and μ_{EF} under convex bending than concave bending, which is consistent with the theoretical reasons explained above and other reported studies [24, 129, 212, 213]. Figure 6-14 shows the resistance change of the printed interconnects under bending, indicating minor variations with the external stress applied. Therefore, it can be concluded that the device performance variation under bending is mainly attributed to the UTC-based MOSFETs with negligible contributions from the printed interconnects.

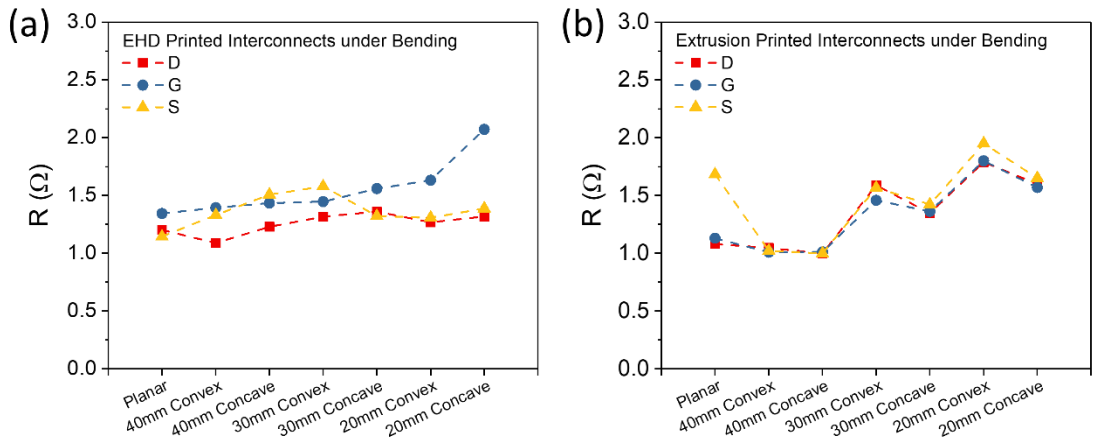

Figure 6-14. Resistance of interconnects under bending printed by (a) EHD system; (b) Extrusion system.

The quantitative and qualitative studies presented so far on the device performance with printed interconnects formed by both printing systems with different operating mechanisms can confirm the suitability of both systems being applicable in this area. Further, the same fabrication steps were used to evaluate the device performance with a different printing ink. Gold (Au) nanoparticle ink has been selected which is compatible with EHD printing system. Studies regarding the electrical resistance measurement and geometries of the printed 2D interconnects were repeated for Au-printed interconnects (Figure 6-15). The Au-printed interconnects presented the same trend as the studies on Ag. However, compared with the Ag features printed by EHD, the width of the printed features was significantly reduced. For example, for 10 printing layers, Au lines were ~20 µm and Ag lines were ~50 µm width. The measured resistance of Au interconnects was higher than the Ag counterparts. This could be because: (1) Ag is inherently more conductive than Au (after curing, Ag NP ink resistivity = 1.6 µΩ•cm, Au NP ink resistivity = 8 µΩ•cm used in this work). (2) When printing these Au and Ag lines using EHD, the same printing parameters were used (same voltage applied, frequency and printing speed). With the same voltage/electric field applied, the conductive particles in the ink experience a force proportional to the charge and electric field strength. Due

to the higher conductivity of Ag ink, it could result in a stronger response to the electric field, leading to increased ink movement and eventually causing more material deposited and lower resistance measured. This could also explain the larger width of the Ag printed features. Nevertheless, it is to be noted that the printing parameters can be manipulated to obtain the desired feature size and improve the measured resistance.

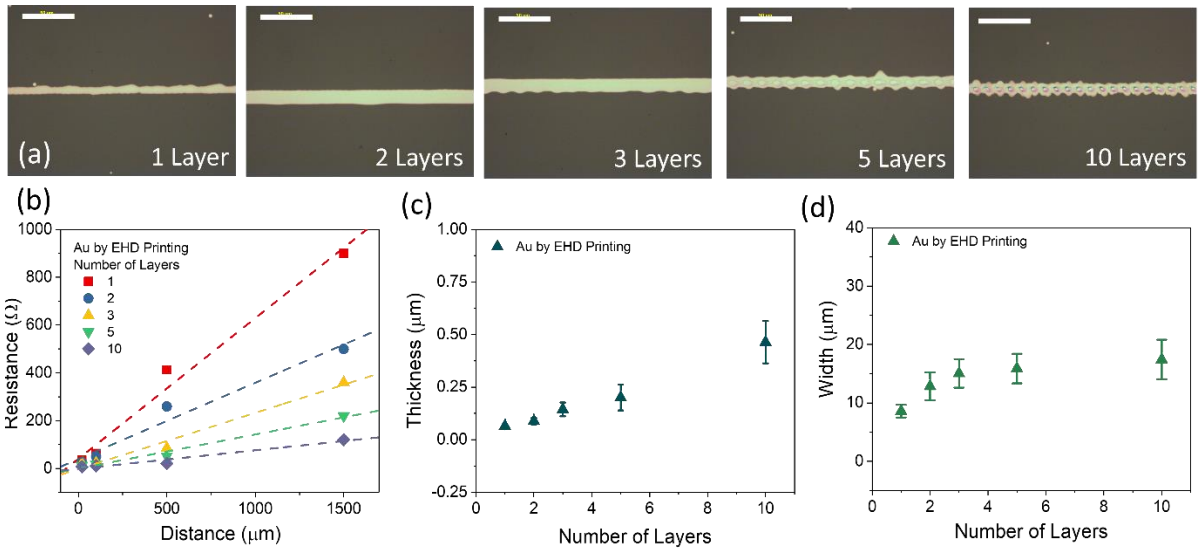

Figure 6-15. Au Interconnect geometries by EHD printing with different number of layers (a) Resistance vs. Au interconnect lengths; (b) Thickness; (c) Width.

Next, the UTC-based MOSFET device performance was investigated after thinning, transfer printing, via opening and via realising by EHD Au ink. Figure 6-16 (a) – (c) show the transfer characteristics for the original device performance and the performance after via realising recorded under the same condition as studies discussed above and extracted parameters including I_{on}, V_{th}, SS and peak μ_{EF}. Figure 6-16 (d) – (i) present the transfer curves and extracted parameters under planar and bending conditions. Overall, devices demonstrated similar performance under all conditions.

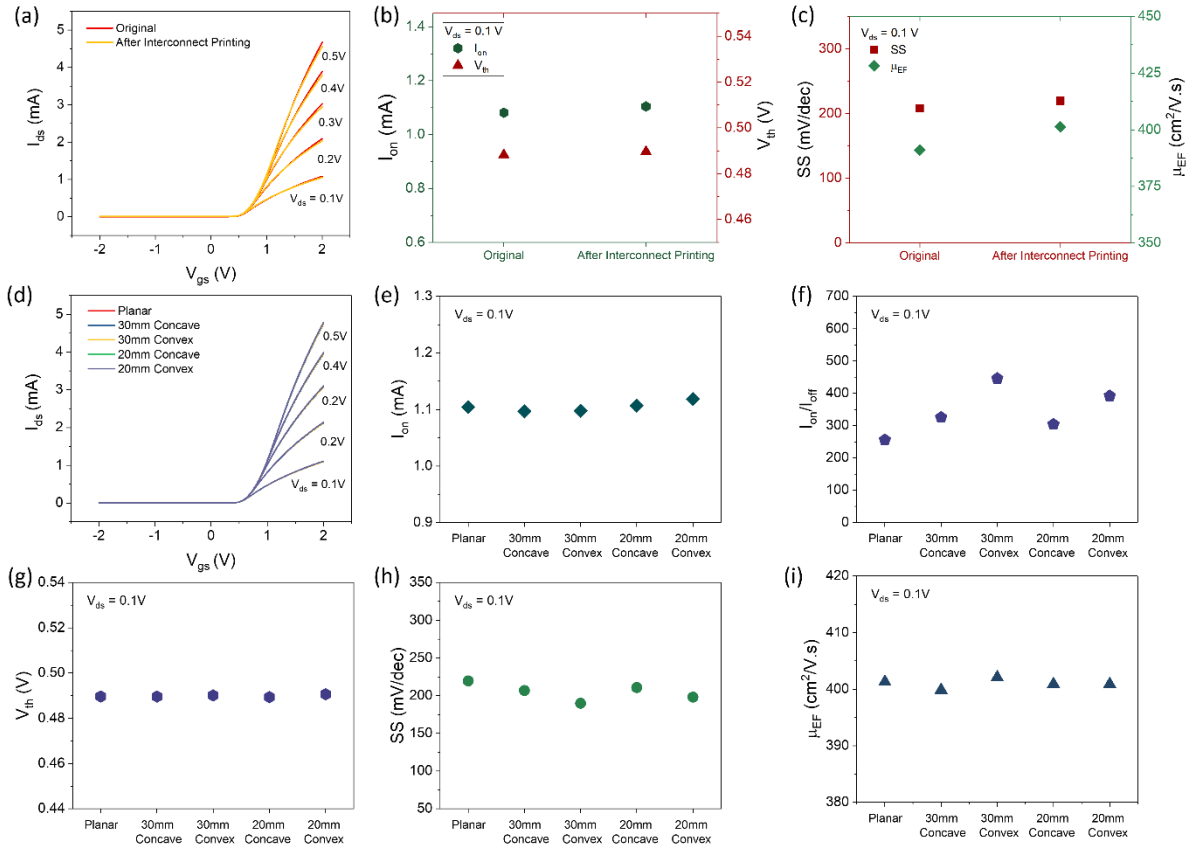

Figure 6-16. MOSFET device original performance and performance after vias realised using Au ink by the EHD printing system: (a) Transfer characteristics; Extracted parameters at V_{ds} = 0.1V: (b) I_{on} and SS; (c) V_{th} and μ_{EF}; Device performance under bending: (d) Transfer characteristics; (e) I_{on}; (f) I_{on}/I_{off}; (g) V_{th}; (h) SS; (i) μ_{EF}.

Further, devices with printed interconnects were evaluated again after printing was complete, and the devices were stored under ambient conditions for two months to investigate the effect of aging (Figure 6-17). Devices with Au interconnects presented no degradation after two months of storage (Figure 6-17 (a)). However, the ones bonded with Ag tracks showed severe degradation in their performance (Figure 6-17 (b) and (c)). Such a decline in the performance is expected as Ag is known to easily oxidise under ambient conditions with exposure to air and moisture. The oxidation leads to the formation of a silver oxide layer on the surface of the interconnects, leaving a detrimental effect on the electrical conductivity and therefore the device overall performance. Au, on the other hand as a noble material, is less reactive to environmental factors that cause oxidation. Hence, devices with Au-printed interconnects

present a steady performance even over an extended period. To prevent silver oxidation from occurring, protective coatings can be applied to encapsulate the printed interconnects. Nevertheless, printed interconnects should be encapsulated in FHE systems, regardless of the printing materials. Encapsulation can prevent printed structures from oxidising as mentioned above. It can also shield them from other environmental factors (contaminants, water, etc.) and mechanical damage. For FHEs used in implantable systems, encapsulations made of biocompatible materials can prevent direct contact between the bodily fluids and the printed structures which may induce adverse reactions to the surrounding tissues.

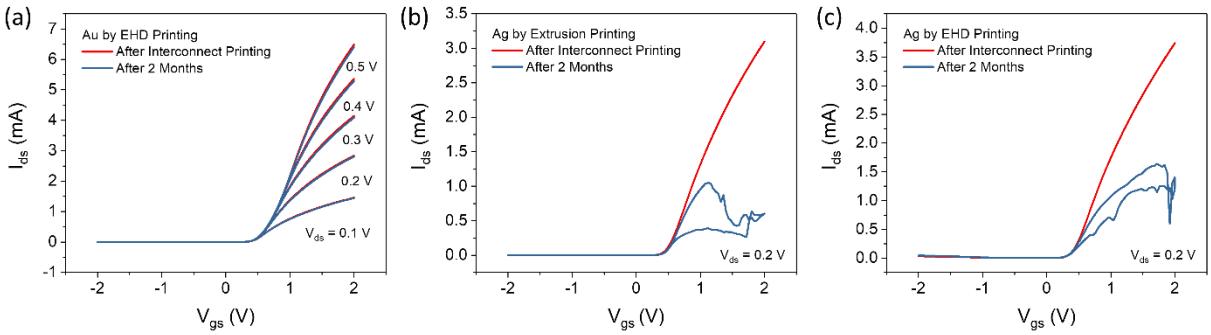

Figure 6-17. Transfer characteristics of UTC-MOSFET with printed interconnects recorded for aging studies including the performance after printing and after 2 months: (a) Au interconnects by EHD printing; (b) Ag by extrusion printing; (c) Ag by EHD printing.

6.4 Conclusion

In summary, after facing and evaluating the challenges of attempting to form wire-bonding-like interconnects in the planar configuration through EHD printing, the presented work in this chapter showed a new optimised approach to enable printed vertical interconnects to potentially construct 3D integrated FHE systems. High-resolution printing systems, EHD- and extrusion-based, were used to achieve printed vertical VIAs using Ag ink/paste with comprehensive studies on the electrical performance as well as the throughput of these systems. The electrical performance of the MOSFET devices on UTCs with printed VIAs was investigated at every

fabrication step including VIA opening and interconnect printing. Multiple devices were evaluated at each step to confirm the reliability and repeatability of the proposed process. Moreover, aging studies were conducted for devices with Ag- and Au-printed interconnects, and the importance of encapsulation was highlighted. Further, the robustness of the developed FHE was verified by performing electrical measurements under mechanical bending with different radii of curvature (40, 30 and 20mm), showing excellent stability under compressive and tensile strain. The proposed fabrication approach lays the foundation to develop high-performance and high-density UTC-based FHE systems.

Chapter 7. Conclusion and Future Perspectives

7.1 Conclusion

Flexible Hybrid Electronic (FHE) systems combine the strengths of traditional CMOS technology, known for high performance, with the advantages of printed electronics, including flexibility and cost-effectiveness. This integration yields flexible electronics that are both high-performing and adaptable, making them suitable for emerging applications such as wearables and IoT devices as the immediate solution. To explore the possibility of exploring this route of study, firstly, an in-depth literature review was conducted, particularly on the development of thin Si ICs and integrating them with interconnects on flexible substrates (Chapter 2). Existing technologies were introduced regarding realising thin Si ICs and forming interconnects for UTCs. The limitations associated with existing technologies were discussed along with their feasibility in integrating thin Si ICs with interconnects on flexible substrates for FHE systems. This thesis was therefore dedicated to advancing the research in this field by overcoming the long-standing challenges. The significant research outcomes are summarised below:

An effective two-step thinning process was developed to overcome the challenges in obtaining and handling UTCs. The lapping process assisted with the PMMA sacrificial technique and chemical etching using TMAH were presented (Chapter 3). The novel utilisation of PMMA, as a sacrificial layer and a cost-effective alternative (1 order of magnitude cheaper) to UV tapes adopted in the industry, led to 4 orders of magnitude lower stress on UTCs during the UTC debonding process after lapping. As a result, 35 µm-thick UTCs were successfully obtained through the fast-operation lapping process. Combining chemical etching, the minimum achievable thickness of Si-based chips could reach up to 2 µm with semi-transparency (44% to 67% transmittance under the visible spectrum). Further, to evaluate the reliability, processed chips with MOSCAPs, AlN-based pressure sensors and MOSFETs were thinned down to 35

μm thickness using lapping assisted with the PMMA sacrificial technique. All devices presented stable performance with insignificant change after thinning. Due to the handling difficulties of standalone UTCs with less than 20 μm thickness, the 2-step thinning process was adopted to evaluate MOSFET chips with 20 μm thickness. Devices revealed negligible differences in the performance after lapping and chemical etching. Nevertheless, it was discovered that 35 μm thick-UTCs developed by lapping with PMMA could withstand up to 20 mm bending radius and this is adequate for many emerging applications in wearables, soft robots, etc.

Following successfully obtaining UTCs with 35 μm thickness, they were subsequently transferred onto flexible substrates, and interconnects were needed to access the devices on thin Si ICs as a crucial part of realising FHE systems. As it was challenging to use conventional interconnect technologies due to considerable differences in mechanical and thermal requirements, the high-resolution extrusion printing system was used to form conformal interconnects, as a novel, simpler and cost-effective alternative (Chapter 4). The highly viscous Ag nano paste used in this work could form conductive tracks covering the step height of thin chips (equivalent to their thickness, 35 μm). UTC-based MOSFET devices were evaluated before and after interconnect printing. It was observed that the device mobility experienced a minor reduction from 780 cm^2/Vs to 630 cm^2/Vs, which was attributed to the added resistance owing to the printed lines. Further, MOSFET-UTCs with printed interconnects were tested under 40mm bending and showed negligible changes in the device performance. During this process, UTCs were initially transferred and bonded using low-stress epoxy-based adhesive (EpoTEK). However, it was proved to be challenging. Therefore, the direct transfer printing method, a collaborative work with Adamos Christou, was adopted to address issues related to the physical bonding between UTCs and flexible foils. It was conducted through a custom-made setup, and semi-cured PI was employed as the adhesive for the UTC bonding agent. 14

MOSFET devices from three different UTCs were assessed by conducting the electrical characterisation before and after transfer printing, showing negligible variation and proving the efficacy of the process. Cyclic bending tests at 40, 30, 20 mm radii were also performed, confirming the excellent interfacial behaviour between the UTC and flexible substrate.

As the conformal extrusion printed interconnects required an insulating dielectric layer, electrohydrodynamic inkjet (EHD) printing was selected to explore the potential of directly forming out-of-plane wire-bonding-like interconnects to omit the dielectric printing step. 3D pillars were then firstly investigated in Chapter 5. After thorough optimisation, libraries of Au micropillar electrode arrays (MEAs) reaching a maximum height of 196 µm and a maximum aspect ratio of 52 were successfully realised (the highest aspect ratio metallic micropillar reported using EHD printing). This resource-efficient fabrication approach then led to the exploration of creating high-density out-of-plane or 3D electronics on flexible substrates as an interesting direction that could enable novel solutions such as solar cells and artificial photosynthesis for efficient energy harvesting. Further, by combining additive manufacturing (AM) with the hydrothermal growth method, seedless synthesis of zinc oxide (ZnO) nanowires (NWs) on the printed Au MEAs was demonstrated. The developed hybrid approach led to hierarchical light-sensitive NW-connected networks exhibiting favourable UV sensing as demonstrated via fabricating flexible photodetectors (PDs), including detectivity (2.62×10^{17} Jones), responsivity (3.16×10^{5} A/W) and EQE (1.06×10^{8} %) at low bias voltage (0.1 V) and light intensity (1 µW/cm^2). The 3D PDs exhibited an excellent omnidirectional light-absorption ability and thus, maintained high photocurrents over wide light incidence angles (± 90°). Lastly, the PDs were tested under both concave and convex bending at 40 mm, showing excellent mechanical flexibility. This work showed the possibility of achieving 3D conductive and functional structure fabrication using EHD printing and introduced new pathways towards high-performance flexible electronics.

After successfully realising 3D micropillars, the out-of-plane wire-bonding-like structures were attempted to achieve using pillars as the base feature. However, it was found that this configuration was extremely challenging to obtain as explained in Chapter 6.2. Therefore, a method to form vertical interconnects using high-resolution EHD- and extrusion-based direct-ink write printing systems was developed (Chapter 6). First, vertical interconnection accesses (VIAs) were achieved by following conventional photolithography and plasma etching steps. This was followed by filling the VIAs with conductive Ag and Au nanoparticle-based ink/paste using printers accessing transistors on UTCs. Comprehensive studies were performed to: (i) compare and benchmark the printing speed and throughput of both printers, (ii) investigate the electrical performance of vertically connected MOSFETs in UTCs, and (iii) evaluate the electrical performance stability of FHE system (interconnects and UTCs) under mechanical bending conditions. The performance of transistor devices on embedded UTCs with printed vertical interconnects were comprehensively investigated at each fabrication step. In comparison with the original performance, MOSFET-UTCs showed insignificant variations after completing a series of processes including thinning, transfer printing, embedding and via opening, as well as interconnect printing. Devices with printed interconnects formed by different printing systems also presented similar performance. The significance of encapsulating printed interconnects was highlighted. Further, the robustness of the developed FHE was confirmed through electrical measurements conducted while subjecting it to mechanical bending at varying radii of curvature (40 mm, 30 mm, and 20 mm). The results exhibited exceptional stability even when exposed to both compressive and tensile strains. This work has therefore confirmed the reliability and repeatability of the developed process towards realising high-density thin Si IC-based FHE systems.

7.2 Future Perspectives

The process of integrating thin Si ICs with printed interconnects on flexible substrates has been successfully developed and demonstrated in this thesis. The presented series of developments lays the foundation to further advance high-performance and high-density UTC-based FHE systems. Future research can be directed into the following:

Handling fragile UTCs with less than 20 µm thickness:

Chemical etching was explored to further reduce UTC thickness as a stress relief method because there were limitations in the achievable thickness developed from the lapping process due to the mechanical pressure induced. However, it was noted that handling standalone UTCs with less than 20 µm thickness became extremely challenging owing to their fragile nature. The potential solution to address this problem is to evaluate the devices on UTCs after transferring onto flexible substrates by employing direct roll transfer printing as the thin chip could conform to the roll system for easy facilitation of the transferring process.

3D integrated and fully encapsulated UTC-based out-of-plane electronic applications:

Based on the progress made in Chapter 3 and Chapter 4, Chapter 6 demonstrated the fully developed and optimised process for realising bendable thin Si IC integrated with printed vertical interconnects, enabling high-density FHE. The work presented in Chapter 5 showed great promising results for constructing 3D structures via the printing route for realising flexible out-of-plane electronics. These optimised processes broadened horizons for integrating thin Si IC-based out-of-plane high-performance flexible hybrid electronics. Towards this, some preliminary studies were conducted. Out-of-plane NW-connected photo-sensors were fabricated on top of embedded ultrathin MOSFET-based UTCs and electrically connected with MOSFET devices with printed interconnects, allowing 3D high-density and high-performance active-matrix flexible sensory systems (Figure 7-1).

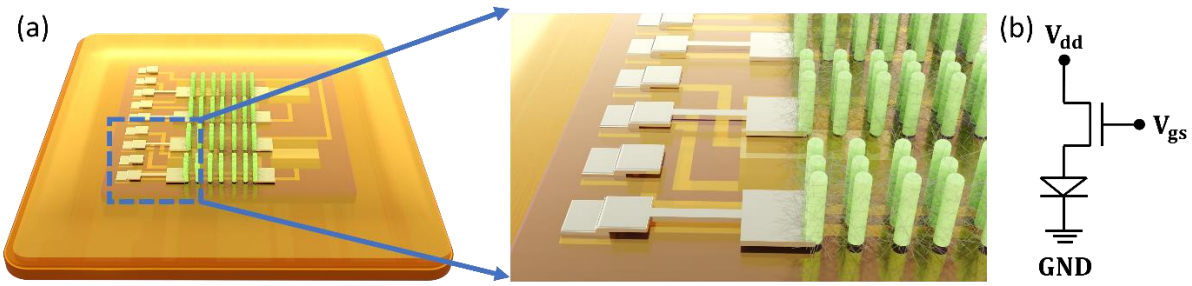

Figure 7-1. Out-of-plane NW-connected photosensor coupled with MOSFET-based UTC in the vertical integration: (a) Schematic; (b) Circuit equivalent schematic.

Figure 7-2 shows the electrical characterisation of an exemplary pixel of the out-of-plane UTC-based active matrix. Figure 7-2(a) and (b) depict the photoinduced transfer curves at V_{ds} = 0.5 V and V_{ds} = 1 V under dark conditions and different incident power intensities from 0.5 to 2.5 µW/cm^2 with a step of 0.5 µW/cm^2, showing a significant increase in the output current with the increase of the light intensity. However, the saturation of the output current at low gate voltage was observed due to the high resistance of the PD. This could be potentially resolved by reducing the PD channel length and/or building more rows of pillars to offer more sensing area as well as increasing electric routes in the channel. Nevertheless, in this case, with 100 µm channel length and 3 rows of pillars (same configuration presented in Chapter 5), photoinduced transfer curves at the same range of V_{gs} presented no output current saturation at V_{ds} = 2 V (Figure 7-2 (d)). It can be seen that without integrating with the transistor, the time domain UV curve shown in Figure 7-2 (c) reveals that the device takes longer to recover and the off current becomes significantly higher, whereas the integrated pixel in Figure 7-2 (d) remains constantly low off current before the transistor turns on. Extracted photo parameters are shown in Figure 7-2 (e) and (f).

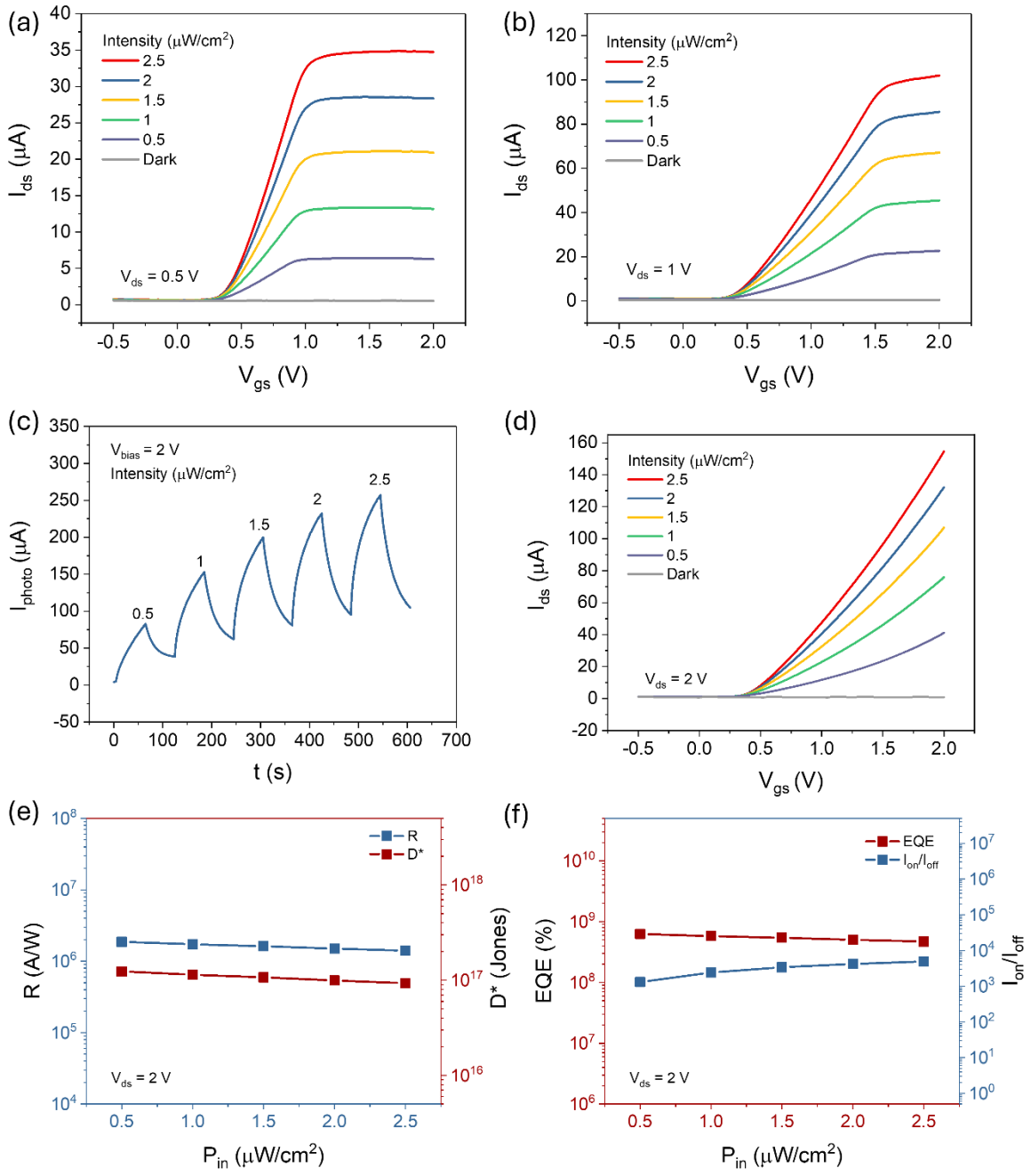

Figure 7-2. Electrical characterisation of an exemplary pixel of the active matrix: Photoinduced transfer curves of the pixel under dark condition and under different incident power intensities, from 0.5 to 2.5 μW/cm2 with bias voltage at (a) Vds = 0.5 V; (b) Vds = 1V; (c) time domain photo curve of the out-of-plane PD at Vbias = 2V; (d) photoinduced transfer curve of the pixel at Vds = 2 V; Extracted parameters: (e) R and D; (f) EQE and Ion/Ioff.*

The integrated pixel presents the advantages of integrating UV sensors with transistors, leading to a more controlled behaviour. Future studies can be focussed on encapsulating the out-of-plane sensors and vertical interconnects (as the importance was highlighted in Chapter 6.3.3)

potentially by drop-on-demand printing and fabricating large area sensory matrices with high uniformity. Besides, currently the out-of-plane sensors are fabricated by printing Au micropillars and hydrothermally growing NWs. The hydrothermal growth of NWs could be potentially replaced by directly printing out-of-plane sensing structures. For example, functional ink can be used to firstly print 2D features to connect electrical pads, followed by printing high-density pillars on top of the 2D routes to increase sensing area. By doing so, chemical waste created by hydrothermal growth would be eliminated. Nevertheless, the studies presented so far are adequate to prove the reliability of the developed process regarding realising high-performance and high-density thin Si IC-based flexible hybrid electronic systems for emerging applications.

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