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Heterointerface Control in III-V Nanowires Monolithically Integrated on Silicon

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Submitted in fulfilment of the requirements for the
Degree of Doctor of Philosophy

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Abstract

Integration of photonic integrated circuits (PICs) serving as interconnects on the silicon electronic platform is gaining momentum as computational requirements increase. Due to material compatibility, silicon-based photonic components remain the main choice for industrial integration. However, research focused on integrating III-V semiconductor-based photonic components has made great progress in tackling the problem of lattice mismatch, which has hindered the use of this material on silicon platforms so far.

A promising monolithic method for the integration of III-V components in CMOS wafers is template assisted selective epitaxy (TASE), which employs a silicon oxide (SiO_2) template to guide the metal-organic chemical vapor deposition (MOCVD) of III-V devices from a silicon seed defined in the device layer of a silicon on insulator (SOI) wafer. TASE enables high defect control but is still affected by a multifaceted growth front, which limits its compositional control and efficient integration of quantum confinement structures.

This work focuses on the monolithic growth of III-V nanowires from silicon, and, in particular, on the control of the morphology of the growth front and the sharpness of heterointerfaces as enablers for the creation of superlattices embedded in the nanowires. Stabilisation of a growth front consisting of a single $\{1\,1\,1\}_B$ facet was achieved on two SOI wafers with $(0\,0\,1)$ and $(1\,1\,0)$ device layer crystallographic orientations by exploiting the growth of InP with high precursor V / III ratios. With an overall growth yield of 92.55 % calculated on a sample of 15 840 growth sites on two $(1\,1\,0)$ chips, the method has proven to be very reliable even under laboratory conditions.

This method enabled the fabrication of InGaAs and InAs quantum wells in a InP matrix. Compositionally sharp heterointerfaces and perfect alignment of concentration profiles of the V and III group elements in the sub-10 nm layers were achieved by employing hold steps in the MOCVD recipe. The growth regime was estimated to be "layer-by-layer", with a very early stabilisation of a single $\{1\,1\,1\}_B$ facet as the growth front, as single crystals resulting from the merging of crystals grown from three nucleation sites were observed with the methodology used in this study. These merged crystals had a crystalline quality fully comparable to that of crystals grown from a single seed.

The growth rate homogeneity and highly predictable heterointerface positioning achieved in this work are expected to aid in the monolithic integration of photonic devices on the wafer scale. The integration of quantum well structures demonstrated in this thesis into the intrinsic

region of p - i - n photodiodes and their in-depth electrooptical characterisation are the natural next step in proving an improvement in the performance of TASE-based photodetectors. Such an improvement, in conjunction with recent progress on TASE based modulators and microdisk lasers, will enable a fully TASE-fabricated PIC.

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Acronyms

APB anti-phase boundary.

BRNC Binning and Rohrer Nanoscience Center.

DESIGN-EID Defect Simulation and Material Growth of III-V Nanostructures - European Industrial Doctorate Program.

DFT density functional theory.

ESR early stage researcher.

EU European Union.

FFT fast Fourier transform.

GMS Gatan Microscopy Suite.

IBM International Business Machines Corporation.

LED light-emitting diode.

PDK process design kit.

PIC photonic integrated circuit.

QW quantum well.

RTP rotational twin plane.

WP work package.

Elements, Chemicals, and Materials

As arsenic.

GaAs gallium arsenide.

GaSb gallium antimonide.

Ga gallium.

H_2O_2 peroxide.

H_2O water.

H_2SO_4 sulfuric acid.

HBr hydrobromic acid.

HF hydrofluoric acid.

InAs indium arsenide.

InGaAs indium-gallium arsenide.

InP indium phosphide.

In indium.

O oxygen.

Pt platinum.

P phosphorus.

Sb antimony.

SiO_2 silicon oxide.

Si silicon.

Sn tin.

W tungsten.

HSQ hydrogen silsesquioxane.

SOI silicon on insulator.

TBAs *tert*-butyl arsine.

TBP *tert*-butyl phosphine.

TESn tetraethyl tin.

TMAH tetramethylammonium hydroxide.

TMGa trimethyl gallium.

TMIn trimethyl indium.

TMSb trimethyl antimony.

Characterization and Fabrication Techniques

ADF annular dark field.

ALD atomic layer deposition.

ART aspect ratio trapping.

BF bright field.

CMOS complementary metal oxide semiconductor.

DF dark field.

DFL defect filter layer.

EBL electron beam lithography.

EDS energy dispersive X-Ray spectroscopy.

EELS electron energy loss spectroscopy.

FIB focused ion beam.

GPA geometric phase analysis.

HAADF high angle annular dark field.

ICP inductively-coupled plasma.

IMA interface misfit array.

LART lateral aspect ratio trapping.

MOCVD metal-organic chemical vapor deposition.

PECVD plasma-enhanced chemical vapour deposition.

RIE reactive ion etching.

SAG selective area growth.

SEM scanning electron microscopy.

SLS strained-layer superlattice.

SNOM scanning near-field optical microscopy.

STEM scanning transmission electron microscopy.

TASE template assisted selective epitaxy.

TEM transmission electron microscopy.

TERS tip-enhanced Raman spectroscopy.

VLS vapour-liquid-solid.

Acknowledgements

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I thank the Cleanroom Operations Team of the Binning and Rohrer Nanoscience Center for their help and support.

This thesis is the culmination of a process that started around new year 2020, when I first found out the DESIGN-EID project was recruiting. My interest in semiconductors was first sparked during my master's degree at the Università degli Studi di Padova by the semiconductor physics course held by Prof. Davide de Salvador and Prof. Enrico Napolitani. A big thank-you goes to Prof. Raffaella Signorini, for her training and supervision during my master thesis, which introduced me to the world of III-V semiconductors and optoelectronics.

This project started in a particularly difficult year, in 2020, with the onset of COVID grinding all international travel to a halt. As an Italian citizen, my country was one of the first in Europe to be hit by the pandemic and by the time I was selected, it was not clear when exactly I would be able to enjoy the mobility required by this EU project. I thank the team at IBM in Switzerland and the University of Glasgow for working hard to take advantage of the relaxation of quarantine measures that summer.

I want to thank Prof. Kirsten Moselund for leading the MIND team that I was lucky to join, her ability in creating a strong team bond was conductive to a wonderful work environment. A big thank-you goes to Nele Harnack for all the sorties exploring Switzerland during the first year of our PhD. Another thank-you goes to Markus Scherrer and Preksha Tiwari for showing me the ropes of the TASE process and cleanroom etiquette, despite some questionable choices of wafer holder at the spin coater. The company of the MIND PhD students (and friends) was one of the

personal highlights of my stay in Switzerland, whether at the lab or at the many outings in the alps, with a special mention to the Italy road trip.

I'm giving Ms. Marilyne Sousa her own paragraph as she stood out for her patience, kindness, trust, and attentive supervision during the entirety of my PhD. Marilyne always made me feel like I had an ally by my side, encouraging me in difficult moments and celebrating my achievements, no matter how little.

A special mention goes to the other ESRs in the DESIGN-EID project, Cristina Martinez Oliver and Christian Dam Vedel, for tolerating my breaking of the ESR naming convention with an "Enrico", patiently joining the (many) ESR-only meetings I organised, and overall being great to work with. A further acknowledgement goes to Cristina for her help during nanofabrication.

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I was fortunate enough to have many people share, if not all, at least pieces of this long, sometimes windy, road across Italy, Switzerland and Scotland, with me. Some of them were already mentioned, some other might not find a place here, but they all had a profound impact on my life, whether good or bad, in the last years. A huge thank-you goes to Audrey Liska, for her continued friendship and support, especially in times of hardship, and for the many adventures we shared meeting around Europe. Thank you to the old friends from Italy, Martina Marasi, Nico Ragazzo, and Gabriele Baldon, who shared a bit of my adventure in Switzerland, and Lorenzo Cazzola and Daniele Chilò who were always available for a spritz, a card game, and many laughs when I was back in Italy. A mention goes out to the "Fioi" group, which, while more and more scattered around Europe, still had great stories during our meetups. Another special mention goes out to the Scottish components of the "Mumble" group, for their linguistic and cultural tutoring, as well as the endless and (mostly) tasteful banter.

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Declaration

I declare that, except where explicit reference is made to the contribution of others, that this dissertation is the result of my own work and has not been submitted for any other degree at the University of Glasgow or any other institution.

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Publications

Journal articles

Enrico Brugnolotto et al. 'Growth of type I superlattice III-V heterostructure in horizontal nanowires enclosed in a silicon oxide template'. In: *Journal of Crystal Growth* 603 (Feb. 2023), p. 127015. ISSN: 00220248. DOI: 10.1016/j.jcrysgro.2022.127015. URL: https://linkinghub.elsevier.com/retrieve/pii/S0022024822004973

Enrico Brugnolotto et al. 'In-Plane III–V Nanowires on Si(1 1 0) with Quantum Wells by Selective Epitaxy in Templates'. In: *Crystal Growth and Design* 23 (11 Nov. 2023), pp. 8034–8042. ISSN: 1528-7483. DOI: 10.1021/acs.cgd.3c00806

Enrico Brugnolotto et al. 'Machine Learning based Nanowire Classification method based on Nanowire Array Scanning Electron Microscope Images [version 1; peer review: awaiting peer review]'. In: *Open Res Europe* (Mar. 2024). DOI: 10.12688/openreseurope.16696.1

Conference contributions

Enrico Brugnolotto et al. 'STEM analysis of Defects and Grain Boundaries in an InGaAs Microdisk'. In: Online: SwissNanoconvention 2021, 2021

Enrico Brugnolotto et al. 'Electron Microscopy and EDS analysis of InGaAs-InP Heterointerfaces in Horizontal Nanowires Grown with the TASE Process'. In: Online: E-MRS Spring Meeting 2022, 2022

Enrico Brugnolotto et al. 'Growth of type II superlattice III-V heterostructure in horizontal nanowires enclosed in a silicon oxide template'. In: Stuttgart, Germany: ICMOVPEXX, 2022

Enrico Brugnolotto et al. 'Application of TASE in the growth of InP/InGaAs in horizontal nanowires'. In: Glasgow, United Kingdom: SINANO, 2022

Enrico Brugnolotto et al. ‘STEM and EDS study of heterointerfaces in III-V nanowires’. In: Busan, Republic of Korea: IMC20, 2023

Preksha Tiwari et al. ‘InGaAs microdisk cavities monolithically integrated on Si with room temperature emission at 1530 nm’. In: IEEE, June 2021, pp. 1–1. ISBN: 978-1-6654-1876-8. DOI: 10.1109/CLEO/Europe-EQEC52157.2021.9541796. URL: https://ieeexplore.ieee.org/document/9541796/

Christian Dam Vedel et al. ‘Impact of different types of planar defects on current transport in Indium Phosphide (InP)’. in: *2021 Joint International EUROSOI Workshop and International Conference on Ultimate Integration on Silicon, EuroSOI-ULIS 2021* (860095 2021), pp. 1–5. DOI: 10.1109/EuroSOI-ULIS53016.2021.9560698

Markus Scherrer et al. ‘Heterojunctions in Integrated Hybrid III-V/Si Photonic Crystal Emitters’. In: Jeju, Republic of Korea: CSW 30, 2023

Markus Scherrer et al. ‘Monolithic Integration of Hybrid III-V/Si Photonic Devices’. In: San Jose, United States of America: CLEO 2023, 2023

Other

Enrico Brugnolotto. *SEM Images of Arrays of III-V Nanowires with Labelled Data*. 2023. DOI: 10.5281/zenodo.10204018

Enrico Brugnolotto and Preslav Alexandrov. *Image Classifier of Nanowire Arrays*. 2023. DOI: 10.5281/zenodo.10255657

Contributions to the Thesis

The tasks in black in the following flowcharts are those I performed. Tasks that other staff and researchers kindly carried out on my request and the key external input for the pooling method in the image preprocessing are highlighted in red. The rectangles represent multiple process steps, further explained in Section 2.4 for the initial nanofabrication process and in the experimental chapters for growth, characterisation, and data analysis. Rhomboids represent single process steps. The rounded boxes represent the flowcharts' start and end(s).

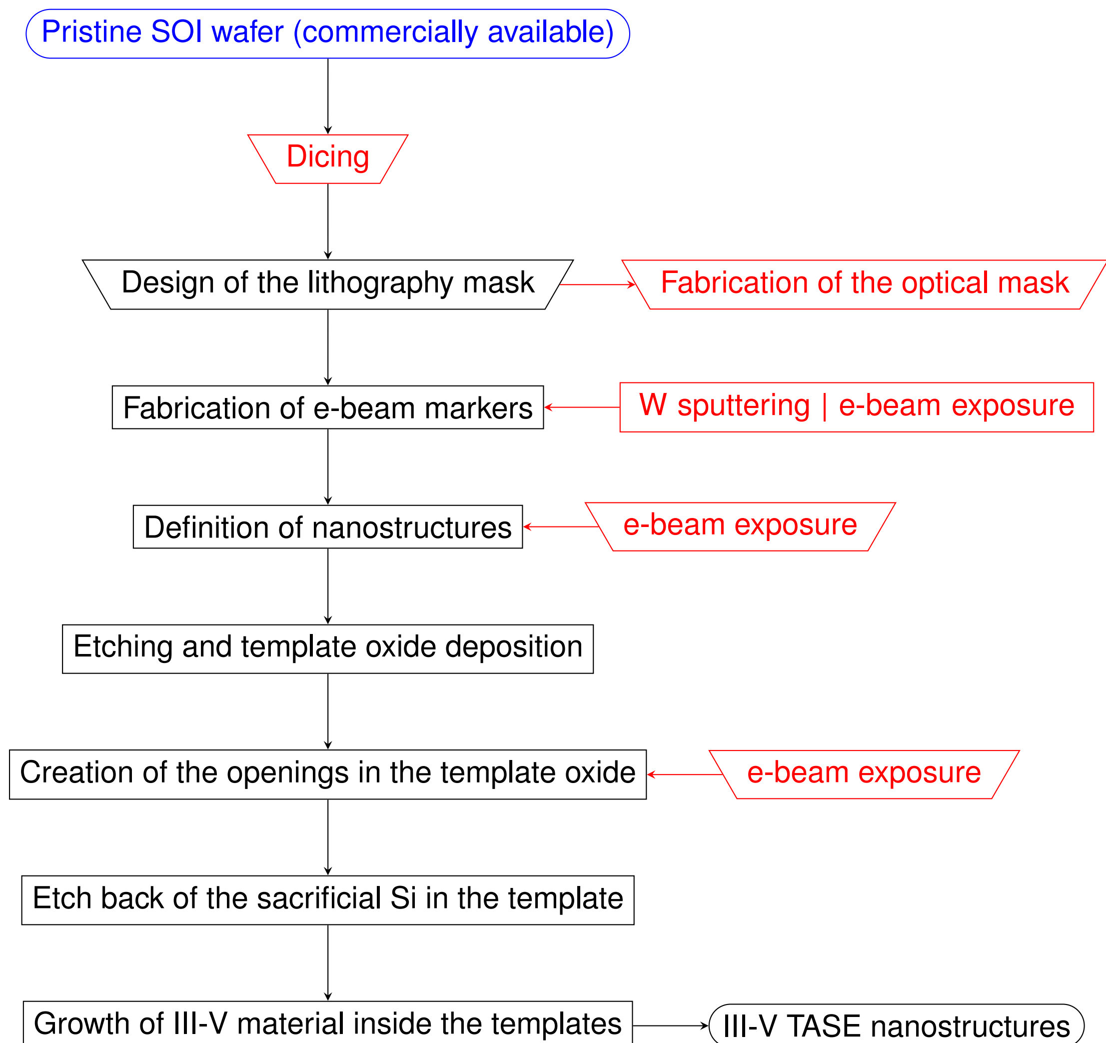


Figure 1: Nanofabrication flowchart.

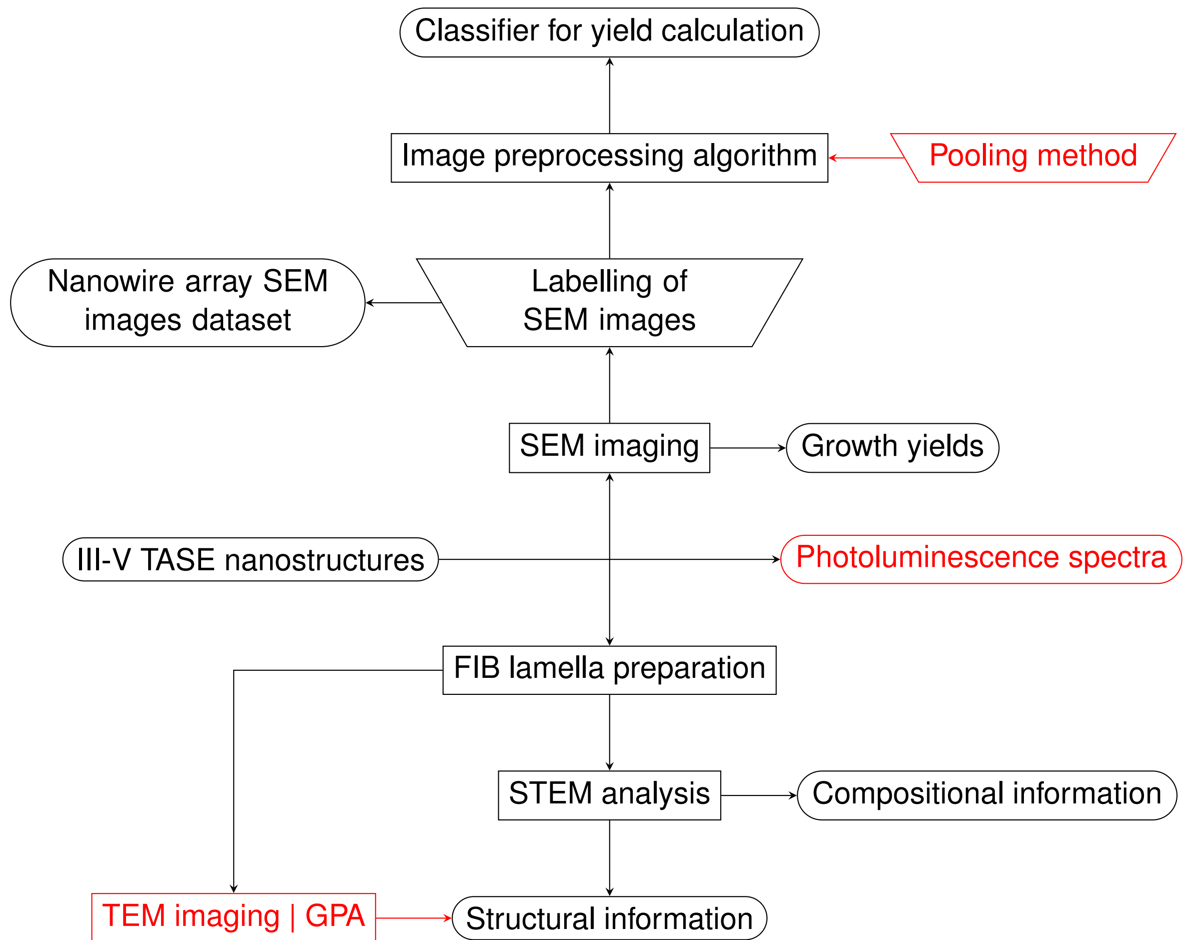


Figure 2: Characterisation flowchart.

Daniele Caimi operated the dicing tool and carried out tungsten sputtering. Diana Dávila Pineda fabricated the optical mask. Antonis Olziersky operated the electron beam lithography machine. Markus Scherrer carried out Photoluminescence measurements. Marilyne Sousa carried out geometric phase analysis (GPA). Preslav Alexandrov first proposed the pooling method. Michael Stiefel recorded TEM images of the merge wires.

Chapter 1

Introduction

Most of the world's telecommunication infrastructure has abandoned the electron and chosen the photon as its primary information-carrying particle for long-range information exchanges. Indeed, even at medium distances, the first world has seen the same transition occur, with fibre optic cables substituting copper wires up to many city homes' doorsteps [15, 16]. In the short distance, data centres have already begun the transition from copper to fibre optics to connect servers [17, 18], and continue to introduce technological developments to improve bandwidth on this optical support [19].

This trend continues towards the ultra-short distances of in-board and in-chip interconnects [20], where photonic integrated circuits (PICs) combine optical emitters and absorbers with waveguides directly on the surface of semiconductor chips, slowly but surely encroaching on what has traditionally been the electron's domain [21, 22, 23]. However, there still exists a point at which the maturity (and overwhelming budget superiority) of electronics requires the photonic data stream to be translated into an electric signal so that transistors can manipulate it in silicon-based complementary metal oxide semiconductor (CMOS) integrated circuits.

Research focussing on optically active elements at the interface between light-speed communication and electronic elaboration efficiency has been ongoing for decades, ever since the first concept of PIC was proposed at the end of the 1960s [24], through the development of silicon waveguides in the 1980s [25, 26]. Given the relatively simple material requirements of electronics compared to photonics, photonics gained popularity as a complementary interconnect technology only after the rapid diffusion and increasing bandwidth requirements of the Internet materialised and were followed soon after by the limits of Moore's law coming into sight [22, 27, 28]. Since then, photonics has begun to shape the myriad of devices on which we rely so much in modern society and has been proposed as a prime candidate for interconnecting quantum systems [29].

Silicon photonics is an emerging technology, but only in the sense that it has recently started to find its place in the manufacturing sector of the semiconductor industry. Since all of the materials involved are already being used in the CMOS process, the integration of new components

into the process design kit (PDK) of many foundries was straightforward [30, 31, 32]. However, the advantages of silicon photonics are much more related to the high maturity of silicon processing technology [32], which has been the backbone of the computing infrastructure of the world since the invention of the CMOS process, than to the actual material properties of this semiconductor. Silicon's electronic structure makes it an ill-suited material for light emission and adsorption, at least when it is not alloyed or otherwise modified.

On the other hand, III-V semiconductors have been the key material of solid-state light emission [33, 34] and sensing [35, 36] devices for the past three decades. The elements of group III and V are rarer and often toxic compared to the group IV element silicon, which is one of the most readily available on the planet. However, in what is a key difference, silicon has an indirect band gap [37], which enables the light-absorbing and emitting properties of III-V semiconductors, which have a direct band gap [38], to shine in comparison.

Today, industrial integration of III-V components on a silicon platform is mainly achieved through the transfer of active components from the lattice-matched substrate on which they grew [39, 40]. Research and development of this type of integration is ongoing and focussing more and more on pick-and-place methods [41] to maximise positioning accuracy, which is a key metric to reduce the footprint and energy efficiency of optical interconnects compared to their traditional metallic counterparts [42, 43]. In turn, this integration route allows the technologist to side-step the issue of lattice mismatch between silicon and III-V semiconductors.

The alternative approach is monolithic integration, which involves the direct growth of III-V material on a silicon-based substrate. This method reduces the positioning fluctuation to a few nanometres but leaves the researcher with a much larger problem to solve: that of lattice-mismatch-borne defects. Technological advancements such as selective area growth (SAG) and aspect ratio trapping (ART) [44, 45], together with the selection of the appropriate starting facet [46] have sought to minimise the occurrence of such defects. A very powerful evolution of all of these methods is template assisted selective epitaxy (TASE), a silicon on insulator (SOI) and metal-organic chemical vapor deposition (MOCVD) based and CMOS-compatible [47] monolithic integration method [48, 49]. Another advantage of TASE is that it allows for the control of defects in the resulting material [50, 51, 52].

Two key findings on which the present work is built were observed during the study of III-V growth in templates. The first is the high influence of the process temperature and V/III ratio loaded in the reactor on the facet-specific growth rates and, in turn, on the morphology of the resulting nanowire [53]. High V/III ratios in the growth of InAs were shown to favour the stabilisation of a $\{1\,1\,1\}_B$ facet, while low V/III ratios favour the stabilisation of $\{1\,1\,0\}$ facets, with intermediate values creating a multi-faceted configuration [54]. A second study showed how different facets enable different rates of III group element incorporation in ternary materials such as InGaAs, leading to internal composition gradients in TASE nanowires and microstructures [55].

Despite these two findings, the majority of studies related to TASE nanowires show structures containing multi-faceted growth fronts [50, 56, 57, 58, 59, 60] and the studies that showed single-facet stabilisation in templates dealt primarily with homoepitaxy [61]. Initially, this could be attributed to the desire to mimic the homoepitaxial result showing the stabilisation of a $\{1\,1\,0\}$ facet, as this has been shown to lead to defect-free crystals. However, due to the nature of the TASE fabrication process leading to MOCVD deposition, the selection of one or more $\{1\,1\,0\}$ facets has proven to be a stochastic process [50] and, over time, this research path was left to rest, at least at IBM Research Europe - Zurich, where TASE was first formulated.

This also resulted in little attention being paid to the second alternative, the study of growth with a single $\{1\,1\,1\}_B$-stabilised facet. In this thesis, I will attempt to highlight the advantages of this method for the fabrication of binary phosphide / ternary arsenide heterostructures in TASE nanowires, estimate their growth yield, and study how this method applies to more complex structures.

Structure of the thesis After this general introduction contextualising the research carried out in this project within the knowledge base and the funding objectives, Chapter 2 aims to dive deeper into the state-of-the-art and introduce concepts necessary to understand the techniques used in the fabrication and characterisation of heterostructured III-V TASE crystals and their material properties. It also explains the TASE process used to fabricate the samples shown in this thesis to the reader. Chapter 3 talks about the initial experiments and how they led to the formulation of the facet stabilisation method used throughout the thesis, while Chapter 4 explores the consequences of this growth regimen in the growth of III-V micro- and nanostructures in TASE templates. Finally, Chapter 5 aims to explore the growth yields that can be obtained with the facet stabilisation method and proposes an avenue for automatic yield assessment for future samples. The thesis concludes in Chapter 6 with an overview of the results and proposals for further avenues of study.

Appendix A gives an overview of the tools and facilities employed.

1.1 The DESIGN-EID consortium

The work described in this thesis was carried out within the framework of the "Defect Simulation and Material Growth of III-V Nanostructures - European Industrial Doctorate Program" (DESIGN-EID) project. The project was made possible thanks to funding from the European Union's HORIZON2020 programme through grant number 860095 [62].

DESIGN-EID brings together three institutions: the University of Glasgow, located in Glasgow, Scotland, as the leading institution and primary beneficiary of the EU funding; IBM Research Europe - Zurich, located in Rueschlikon, Switzerland, as the leading experimental partner; and Synopsys Quantum ATK, located in Copenhagen, Denmark, as the leading simulation

partner.

Aside from its training objectives, the project aimed to explore, characterise, simulate, and exploit defects in III-V semiconductors and the effect of growth conditions in their formation. To achieve these goals, four work packages (WP) were identified:

- WP1: Material Growth. This package encompassed crystal growth and characterisation on the nano- and microscale. In particular, crystalline and compositional studies were to be performed.
- WP2: Material Simulation. This package dealt with the simulation of the effect of crystalline defects and compositional gradients on the electronic and optical properties of the material. Another topic of interest was the simulation of the growth dynamics leading to defect formation.
- WP3: Device Fabrication. As the name suggests, the objective of this package was to employ the knowledge gained during the project to fabricate a device that could be used as an active photonic component.
- WP4: Device Simulation. This package encompasses the simulation effort to identify the best device structure and composition to achieve its intended role as an active photonic component.

Three early stage researchers (ESRs) were hired to achieve the consortium's objective, and each of them carried out a third of their doctoral studies at the University of Glasgow and spent the remaining time at one of the other two partner institutions. As ESR1, I spent the first two years of my doctoral studies at IBM Research Europe- Zurich, from September 2020 to the end of August 2022, mainly performing experimental work related to WP1. Finally, in the last year of my doctorate, I concentrated on data analysis and developing a machine-learning algorithm for classifying TASE-grown III-V nanowires from scanning electron microscopy (SEM) images.

Chapter 2

Literature review and methodology

If the reader asks a common person in the street what "electronics" means they will receive a variety of responses centred on computers, smartphones, television sets, and other everyday appliances. On the other hand, if the same interviewee demographic was asked about "photonics", some might mention light-emitting diodes (LEDs) and lasers, others might cite Star Trek or other science-fiction work. The term photonics has not found widespread understanding outside the semiconductor industry, despite these two technologies often being separated by around a decade and a half in the research and development stages.

The basic building block of modern electronics, the transistor, was invented in 1947 [63, 64]. Pointing to a direct equivalent in the history of photonics is not straightforward; however, the first solid-state light-emitting device was described just 15 years later in 1962 [65] and consisted of a gallium arsenide (GaAs) LED emitting in the infrared. Interest in solid-state lasing grew immediately after this discovery [66, 67] affirming the role of III-V semiconductors as solid-state light emitters. The next year, in 1963, Wanlass invented complementary metal oxide semiconductor (CMOS) technology [68] cementing integrated planar electronics as the main computational platform of the second half of the century. It took four years after this seminal invention for the idea of a photonic integrated circuit (PIC) to follow [24].

Therefore, while integrated electronics was entering its exponential phase, exemplified by Moore's law [69], formulated in the mid-1960s, the building blocks of photonics were just being discovered or still in a conceptual phase. This led to a difference in investment that, in turn, shaped the technological landscape of humanity. While commercial electron-based technologies were progressing through small-, medium- and large-scale integration, up until very large-scale, photon-based technology was mostly commercialised as bulk devices for, until the discovery of the blue LED in the early 1990s [34], highly specialised lighting applications, and solid-state lasers.

The 1990s saw a new revolution: the introduction and rapid diffusion of the Internet. This new technology exposed the limitations of the electron as an information-carrying particle: impedance losses and inductive currents can be sidestepped by choosing to transmit information

with pulses of light, as they are issues specific to electron-based technology. Furthermore, fibre optic cables can support a larger data stream compared to copper wires. The switch from metallic cables to optical supports was quickly implemented in the long-range communication infrastructure, going hand in hand with the employment of bulk emitters and absorbers at the two ends of the cable [33]. This change also stimulated interest in the use of this technology in integrated interconnects, which has been growing since the late 1980s [70].

The use of photons bypasses some important problems affecting electrical lines in integrated interconnects, such as the "aspect ratio limit" binding the maximum amount of bits per second to the shape of the interconnect [71], the dependence of clock timing on temperature, cross-talk between neighbouring interconnects, and the transition between high impedance electronic components and low impedance electronic interconnects, while simultaneously providing voltage isolation and enabling free space interconnects if required [72]. Most of these issues also have electrical solutions. Still, these solutions, in turn, increase the energy requirements and therefore the energy loss that occurs on the circuit board. As there is a limit to how much heat can be cost-effectively extracted from each singular chip, photonics becomes attractive from both an energy- and a cost-efficiency point of view [43], provided that the integration method allows such an efficiency.

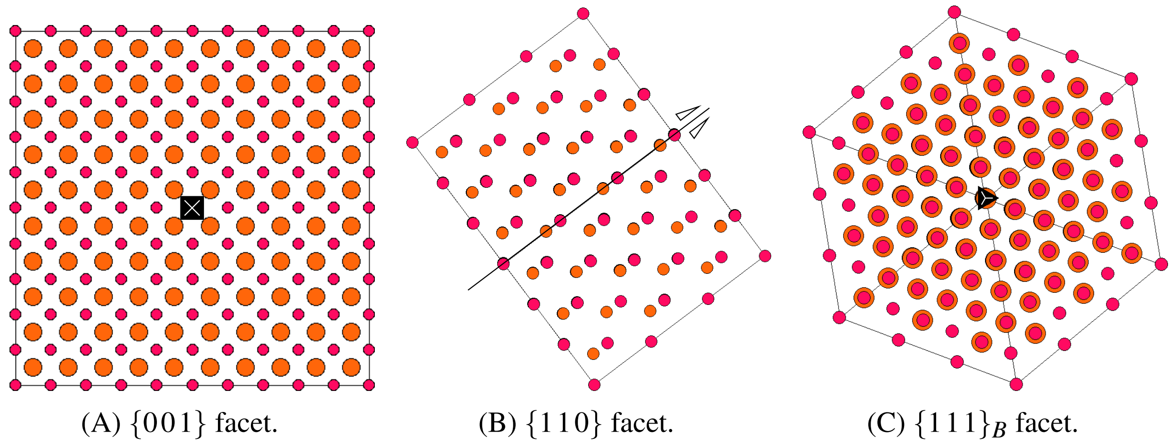
Indeed, integration is the key step in enabling photonics. The initial photonic circuits of the late 1980s and 1990s were realised directly on indium phosphide (InP) wafers from 2 inches to 4 inches in diameter. Despite their small size, InP wafers are expensive supports compared to the much larger 150 mm and 200 mm silicon supports their contemporary. Still, this spearhead technology managed to achieve very large scale integration density by the mid-2010s, after which it was surpassed by both silicon and III-V on silicon photonic integrated circuits [21, 22].

Therefore, an important objective for contemporary scientists working in the field of photonics is to perfect the integration of efficient III-V components on the (comparatively) cheap silicon substrate. The main issue to be addressed in integrating III-V semiconductors on silicon is the mismatch in the lattice parameter between these two materials, which causes a wide variety of defects in monolithic integration [46].

2.1 Properties of III-V materials

III-V semiconductors are compound semiconductors formed by the stoichiometric combination of elements from the III group (third group, or group thirteen in the modern nomenclature) and the V group (fifth group, or group fifteen) of the periodic table. In their simplest form, they are binary, consisting of one III group and one V group element, with some examples being InP and GaAs. Ternary and quaternary III-V materials such as $In_{1-x}Ga_xAs$ or $In_{1-x}Ga_xAs_{1-y}P_y$ contain three or four different elements, respectively.

Crystallographically, III-V materials are available at room temperature in crystals with the



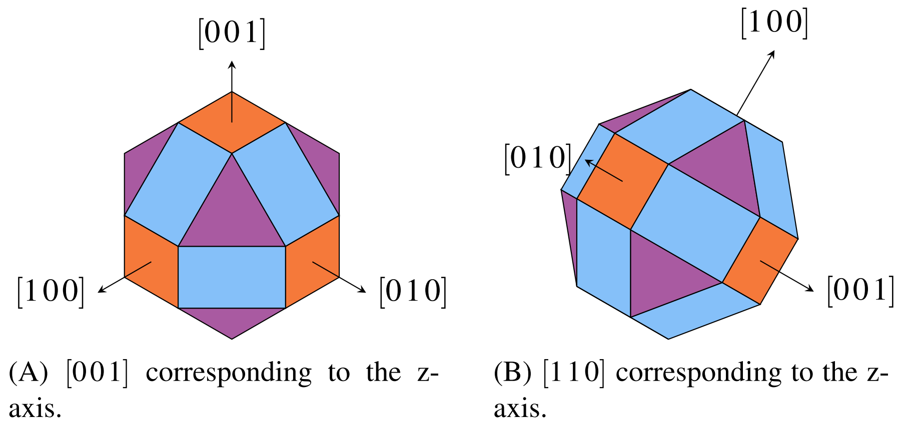
(A) $\{0\,0\,1\}$ facet. (B) $\{1\,1\,0\}$ facet. (C) $\{1\,1\,1\}_B$ facet.

Figure 2.1: 2D projections of the low-index facets in the F$\bar{4}$3m GaAs crystal with the basic symmetry elements highlighted. Gallium is represented in orange and As in pink; atomic radii are not to scale. (A) shows the 2D projection of the lattice along the $\{0\,0\,1\}$ direction, which coincides with the four-fold axis. (B) shows the 2D projection along the $\{1\,1\,0\}$ direction, contained in the mirror plane. (C) shows the 2D projection along the $\{1\,1\,1\}$ direction, coinciding with the three-fold axis.

symmetries of space group number 216 (F$\bar{4}$3m, or zincblende-like) or 186 (P6_3mc, or wurtzite-like) and are easily affected by polytypism when grown. Space group 216 is that of a cubic face-centred crystal, while space group 186 describes a hexagonal crystal. These two structures are closely related, as the addition of a two-fold axis alongside the three-fold axis of space group 216 results in a phase change to space group 186, transforming the affected $\langle 1\,1\,1 \rangle$ direction in the zincblende phase to the $\langle 0\,0\,0\,1 \rangle$ direction in the wurtzite phase [73]. $\{1\,1\,1\}$ facets can also be described according to which half of the AB stoichiometry of the III-V material is exposed. For example, in Figure 2.1(C) the top layer is entirely composed of V group atoms. This facet is called a $\{1\,1\,1\}_B$ facet, while a $\{1\,1\,1\}_A$ facet has III group atoms exposed.

Figure 2.1 shows the 2D projections of a GaAs F$\bar{4}$3m crystal along the low-index directions. These projections are useful for interpreting atomic-resolution microscopy images of III-V semiconductors. These computer-generated projections were created using CrystalKit, a dedicated software. They also highlight the main symmetry elements of the zincblende space group. The 2D projection in Figure 2.1(A) shows how a $\{0\,0\,1\}$ facet appears in the microscope. The symmetry element controlling its motif is a four-fold axis perpendicular to the projection plane. Similarly, Figure 2.1(B) shows how a $\{1\,1\,0\}$ facet appears in the microscope and the mirror plane dictating its symmetry. Finally, Figure 2.1(C) shows the lattice projected along the $\langle 1\,1\,1 \rangle$ direction. The symmetry of this projection is compatible with a three-fold axis coinciding with the $\langle 1\,1\,1 \rangle$ vector.

Although the orientation of the low index facets with respect to each other is difficult to properly convey in a 2D projection, Figure 2.2 shows how the three different facets, $\{0\,0\,1\}$ in orange, $\{1\,1\,0\}$ in light blue, and $\{1\,1\,1\}$ in purple, are orientated in a cubic crystal. The shapes of the polygons that make up the figure also give a hint as to what kind of symmetry element



(A) [0 0 1] corresponding to the z-axis.

(B) [1 1 0] corresponding to the z-axis.

Figure 2.2: Low index facet orientation in the F$\bar{4}$3m space group. The $\{0\,0\,1\}$, $\{1\,1\,0\}$, and $\{1\,1\,1\}$ facets are color-coded in orange, light blue, and purple, respectively. The two orientations shown in this Figure are with the vertical z-axis coinciding with the $[0\,0\,1]$ and $[1\,1\,0]$ directions in (A) and (B), respectively.

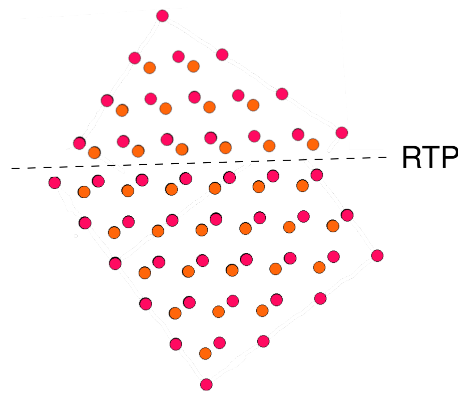
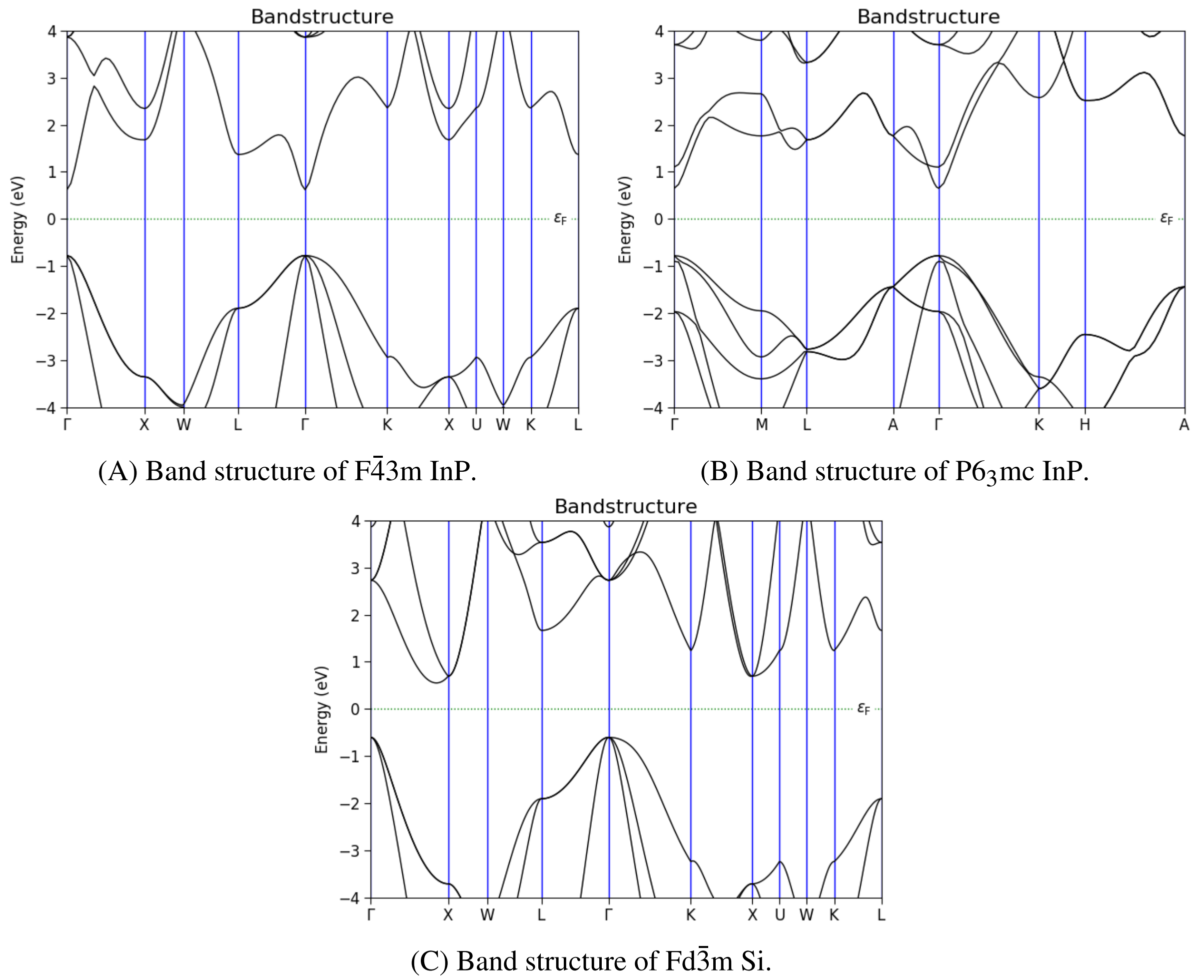


Figure 2.3: Drawing of a rotational twin plane (RTP), highlighted by a dashed line, corresponding to a $\{1\,1\,1\}$ plane in a GaAs F$\bar{4}$3m crystal.

is present in each facet. Figure 2.2(A) can also be used to understand the relationship between different planes in the cubic silicon crystal of the $(0\,0\,1)$ silicon on insulator (SOI) device layer used as growth substrate in Chapter 3. Similarly, Figure 2.2(B) illustrates the symmetry of the $(1\,1\,0)$ SOI device layer used in Chapters 4 and 5.

Figure 2.3 shows a drawing of a rotational twin plane (RTP) corresponding to a $\{1\,1\,1\}$ plane in a GaAs F$\bar{4}$3m crystal. Formation of this type of 2D defect is common in the growth of III-V crystals [74] and its density is very sensitive to changes in the growth environment [75, 76] due to its low formation energy. From a lattice symmetry point of view, the RTP is formed by adding a two-fold rotation axis to the $\{1\,1\,1\}$ direction of the crystal. The two atomic bilayers adjacent to the RTP can be considered a thin slice of wurtzite [77, 78].

Both atomic species and lattice symmetry affect the electronic properties of crystals. Bloch functions are the eigenfunctions of the Hamiltonian that describe a particle in a periodic potential [79], and pose the basis for understanding the behaviour of electrons in crystals. They are also periodic functions, and in reciprocal space they are used to describe the electronic band structure,



(A) Band structure of F$\bar{4}$3m InP.

(B) Band structure of P6_3mc InP.

(C) Band structure of Fd$\bar{3}$m Si.

Figure 2.4: Band structures of Si, and InP in its cubic and hexagonal phases, calculated with DFT. (A) and (B) show the band structures of zincblende and wurtzite InP. The Fermi energy (ε_F) defines the origin of the ordinate and is marked by a dotted line. (C) shows the band structure of Fd$\bar{3}$m Si. Images courtesy of Christian Dam Vedel.

resulting in plots such as those in Figure 2.4. The band structures in this figure were calculated, using density functional theory (DFT), and then plotted by Christian Dam Vedel. Energy is on the vertical axis, with its origin at the Fermi energy, which is the energetic midpoint between the last occupied state and the first unoccupied state, at 0 K (thermal zero). The horizontal axis shows wavevectors along certain high-symmetry directions in the unit cell of the reciprocal lattice: the Brillouin zone [80]. The energy of each of the states along the one-dimensional paths that link these points is then plotted. Therefore, in Figure 2.4, the states below the Fermi energy are part of the valence band and those above it are part of the conduction band.

The Γ point is the centre of the Brillouin zone and is very important for understanding photon-driven electronic transitions between bands. A material with the minimum of the conduction band and the maximum of the valence band at the Γ point is said to have a direct band gap. Conversely, a material that has a band structure with the minimum of the conduction band at a wavevector that is different from the wavevector of the maximum of the valence band is

said to have an indirect band gap. Due to momentum conservation rules, a single photon can only cause so-called centrezone transitions, which are transitions between states at the Γ point. Interband transitions outside of the centrezone require a third particle, usually a phonon, to mediate the transition, changing the type of interaction from two-particle to three-particle; which has a lower probability of occurring. Similarly, the radiative relaxation pathway is prevalent in direct band-gap semiconductors, while non-radiative relaxation paths are prevalent in indirect band-gap semiconductors.

Therefore, the band gap type greatly affects a semiconductor's light-emitting and -absorbing properties. III-V semiconductors have direct band gaps, as exemplified by those of the zincblende and wurtzite phases of indium phosphide shown in Figures 2.4(A) and 2.4(B), and are highly efficient light emitters and absorbers as a consequence. On the contrary, silicon has an indirect bandgap, as shown in Figure 2.4(C), making it an ill-suited material for light emission and absorption.

Tuning a semiconductor's band gap is key to the control of its absorption and emission wavelengths. Although binary III-Vs provide fixed starting points in both band gap and lattice constant, ternary and quaternary III-V compounds allow high-precision tuning of both properties [81]. For example, the materials chosen by the DESIGN-EID consortium were InP and $In_{0.53}Ga_{0.47}As$, because they are lattice-matched and therefore a lower density of defects is expected at their interface [82, 83, 84] and because InGaAs emits in the telecom range [85, 86].

2.2 III-V-on-Si integration routes

Various III-V synthesis methods are available [87]: the following is an overview of epitaxial growth methods focussing on the integration routes of III-V semiconductors on silicon, which can be divided into two broad categories: transfer and monolithic integration.

2.2.1 Transfer integration

Transfer integration refers to the indirect integration of III-V material grown on a different lattice-matched substrate on a silicon wafer.

The main advantage of these techniques is the absence of lattice mismatch as a source of defects during epitaxial growth. Furthermore, it allows the selection of the best-performing structures to be transferred onto the silicon substrate [88, 89]. Transfer integration does not have to compromise on the growth parameters or material systems to achieve CMOS compatibility (except for bonding temperature). Together, the various methods that fall under this definition form a mature technology well established in industry [39, 40, 89], and, as a result, benefit from years of industrial optimisation.

This type of integration requires the growth of III-V in a separate fabrication line that must maintain the high precision and cleanliness standard of the main CMOS silicon line, resulting

in a large capital investment. Furthermore, most classic transfer steps can result in a material with a more irregular geometry (wafer bow, surface roughness after etching), or presenting transfer-related defects [90], or require an extra bonding layer [91, 92, 93, 94], and do not allow nanometre precision in integration [41, 89]. However, the most advanced techniques that bypass most of these quality issues are too slow to provide a competitive transfer time for large, densely integrated 200 mm (or 300 mm) production wafers [41, 89].

2.2.2 Monolithic integration

Monolithic integration refers to direct integration by epitaxial growth of III-V semiconductors on a silicon substrate.

It naturally provides advantages such as extremely high spatial precision and accuracy for small device integration on wafer-scale substrates, which can be achieved in a shorter time frame compared to its transfer analogues [89, 95]. It has the potential to be a more economical alternative to heterogeneous integration. If the growth process can be integrated with current CMOS processes, its implementation in a CMOS line would eliminate the need to have a dedicated III-V fabrication facility running in parallel with a silicon-based plant, especially if the use of III-V electronics is envisioned at the same time as III-V photonics [89]. Thus, monolithic integration has the potential to reduce the capital cost required to integrate III-V photonics in different silicon-based devices [89, 91].

The main disadvantage of monolithic integration is the high lattice mismatch between silicon and most III-V materials [87]. The effect of this mismatch in the material is the formation of strain-relaxing defects at the silicon / III-V heterointerface [46, 96]: these defects have a very detrimental effect on the performance and lifetime of a device [97, 98], and act as scattering or recombination centres [99]. The polar nature of III-V atomic bonds compared to nonpolar Si-Si bonds means that anti-phase boundary (APBs) can be created during growth on silicon surfaces with monoatomic steps [46], and most known surface treatments to eliminate nucleation sites for these defects occur in temperature ranges that are incompatible with the CMOS process [100, 46, 42]. Furthermore, materials that are known to grow at a higher temperature, such as III – nitrides [101], and substances that could have detrimental effects on the passivating of silicon oxide (SiO_2) layers through their diffusion, such as gallium [42] which readily diffuses in silicon oxide [102], also pose temperature-related CMOS compatibility issues. Another key obstacle, especially related to the direct growth of micro- and nanostructures, is the stricter requirements for the reproducibility and reliability of the process.

There are many monolithic integration routes, and the most common categories are introduced in the following paragraphs.

Planar growth Direct planar growth of III-Vs on silicon (Figure 2.5(A)) is the simplest method of monolithic integration. It can be suitable for the growth of III-Vs with a lattice constant

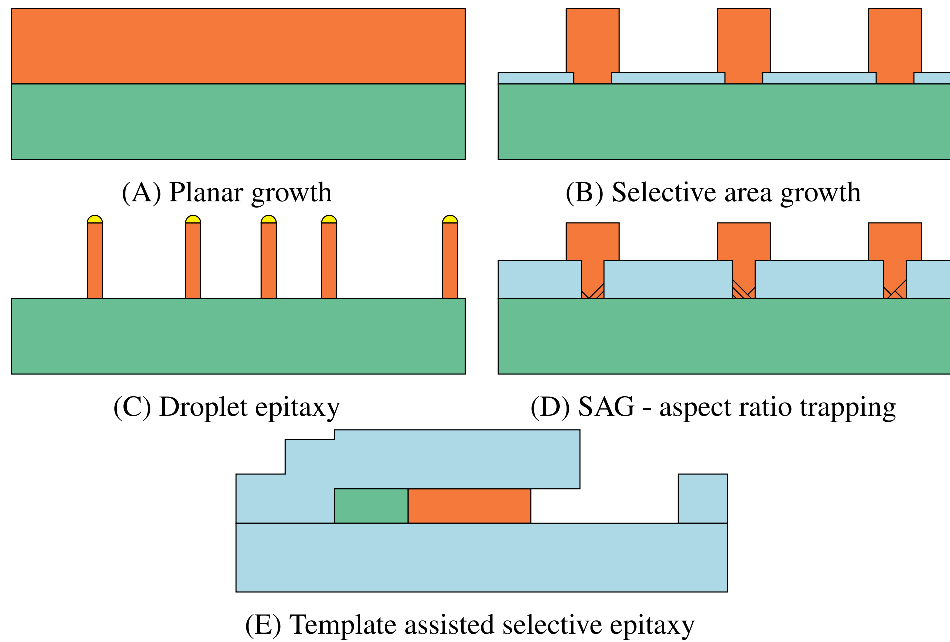


Figure 2.5: Types of III-V on Si monolithic integration methods. Si is shown in green, SiO_2 in blue, III-V semiconductor in orange, and metal catalyst in yellow. (A) shows an example of a planar III-V film growing from a Si substrate. (B) shows an example of SAG, where III-V semiconductor grows from small opening in a passivating layer. (C) shows a drawing of droplet epitaxy, where nanodroplets of a catalyst metal mediate nucleation and growth. (D) illustrates the mechanism by which defects, the black lines in the nucleation area of the III-V material, are trapped by sidewalls of passivating material. (E) shows a drawing of TASE, where III-V semiconductor grows horizontally in passivating material templates with high aspect ratio.

very close to that of silicon or for the self-assembled nucleation of nanoparticles in a Stranski-Krastanov growth mode, which can pose the basis for quantum dot fabrication [103, 104]. It, however, presents a few drawbacks related to the absence of a way to contain defects and the different material properties of the material stack [105]. It can lead to wafer bow or warp due to the mismatch of thermal coefficients between the various materials [106, 107], and materials with a high deviation from the silicon lattice parameter can require strain management layers of 1 µm or more to grow without defects [107, 108, 109]. Some techniques to lower the thickness of the semiconductor layer containing defects include the use of a strained-layer superlattice (SLS), a series of thin layers of highly mismatched material, which acts as a defect filter layer (DFL) halting the spread of threading dislocation by reflecting them back towards the substrate [46, 110, 111]. Similarly, an interface misfit array (IMA) has been shown to improve material quality, but is only available as a stress-reducing avenue between highly lattice-mismatched materials [112, 113].

Selective area growth (SAG) As shown in Figure 2.5(B), SAG consists in the growth of III-V material from silicon seeds located in openings in a horizontal mask of a material that does not promote nucleation, such as SiO_2. These holes can be defined with different methods, from

self-assembled masking to lithography. This type of growth results in nanostructures [108] such as nanowires, both of a single material and in core-shell configurations with very high position control [114]. Wafer bow and warp are not issues with SAG, since growth does not, unless promoted by accentuating lateral growth [115], end up forming a single material layer. However, in this technique, growth develops mainly in the vertical direction, and the presence of lateral growth can result in unwanted heterointerfaces.

Droplet epitaxy Droplet or vapour-liquid-solid (VLS) epitaxy consists in guiding the nucleation of III-V material by using a nano-droplet of a catalyst metal, such as gold, on the silicon substrate (Figure 2.5(C)). This technique also avoids wafer bow as it only results in the growth of nanowires [116]. Since VLS is dependent on the metallic droplet, the growth can be tuned to achieve high directionality and the incorporation of heterostructures with minimal or no unwanted side growth [117, 118]. This type of growth depends on the metal droplets and therefore on their self-assembled distribution on the substrate surface, which diminishes position control [118]. Similarly, the geometry of the resulting structures is limited to nanowires [116], and the reservoir effect in the catalyst droplet complicates the control of composition in ternary and quaternary III-V materials [119]. Nonetheless, this method allows for sophisticated growth studies such as in-situ TEM imaging [117, 120, 121], leading to the possible refinement of growth recipes to the point where phase control can be achieved [75, 118, 73].

Aspect ratio trapping (ART) ART refers to the confinement of defects to the seed region by sidewalls and other such barriers in a growth regimen mediated by a template. The basic idea is that, as most defects nucleate near the silicon / III-V interface and then propagate in directions that are often not parallel to the growth axis, they can be trapped in the region of the material closest to the seed by sidewalls that constrict the III-V crystal so that it grows in a cavity with a high aspect ratio, as shown in Figure 2.5(D).

SAG-ART has the mask selecting the seed areas increase in thickness to allow the trapping of defects. This technique also allows high position control of the III-V crystal, while accentuating control over the defects [56, 122]. However, typically SAG-ART employs large templates, which means that defects propagating in directions that lie in the plane of the side walls are not filtered by the ART mechanism [46]. Simultaneously, multiple nucleation points in large seed areas can result in coalescence-borne defects often not trapped by sidewalls [44].

Template assisted selective epitaxy (TASE) TASE can be seen as an evolution of the SAG-ART method as it also defines silicon seeds surrounded by SiO_2 and uses templates with high aspect ratio to guide growth, as shown in Figure 2.5(E). The main differences with SAG-ART are the size and complexity of the templates and the focus on planar growth. TASE enables the growth of various vertical and horizontal nanostructures while maintaining extremely accurate geometry and position control [123, 124, 49]. It also enables superior defect control, even

compared with ART: far from the growth interface, defects can be effectively limited to twin planes [52], which can also be eliminated in some cases [50]. In certain geometries, it also enables phase control [51].

On the other hand, it is the most complex method of those listed in terms of overall steps before III-V growth. Furthermore, since nanowires fill templates quickly, TASE can only grow core-shell structures in a microdisk format [124] and not in nanowire format. Like other techniques which employ a mask to control selectivity, unwanted nucleation on the masks, called parasitic growth, which results in parasitic crystals, can occur [125].

2.3 State of template assisted selective epitaxy

As shown in the previous section, TASE is one of the most advanced monolithic integration techniques; its implementation can be found in Section 2.4. The flexibility of TASE is demonstrated by the different ways research groups have used it.

2.3.1 Selection of nanofabrication process

A group at the University of California Santa Barbara used TASE to achieve high facet control in the homoepitaxial growth of III-V semiconductors [61, 53, 125]. Their growth approach mainly focusses on homoepitaxy of III-Vs on III-V substrates [61, 53, 125], which are more expensive compared to SOI. While growth dynamic studies from this group highlighting the role of low temperature and high V/III precursor ratios were instrumental in informing the growth parameters used in this thesis, a process based on SOI wafer was needed, as the growth findings of this project have the objective to further enable co-planar integration of active III-V components with silicon waveguides.

The group at the University of Hong Kong focussed on deposition in large templates [52, 57]. Sometimes the name lateral aspect ratio trapping (LART) is used to highlight the use of large templates to create in-plane structures inside templates [126]. This method increases the risk of multiple nucleations and limits the defect-trapping effect in the in-plane direction [52, 57, 127]. As the LART emitter fabrication methods used in the process adopted by this group are based on the etching of III-V LART platelets [126, 127], the resulting devices are located far from waveguides. Furthermore, the use of etching in the fabrication process further complicates optimisation at the wafer scale, as both the growth and following etching parameters need to be tuned in order to create working devices.

The Hong Kong University and IBM Research Europe - Zurich groups have been developing template-based methods to fully integrate planar PICs on a SOI platform [128]. This means a circuit made up of emitters, waveguides, and detectors. With the TASE method used in the Zurich group, silicon waveguides can be defined in the same lithography step as emitting and

absorbing structures, allowing for high design accuracy [60]. Emitters can be integrated in the form of microdisks [124, 9]. TASE microdisk devices, while demonstrating good performance, with evidence of lasing [124], suffer from the lower amount of gain material available with TASE compared with LART [127]. Alternatively, modulators can be made with TASE [129, 58] to substitute a dedicated emitter with the modulation of an existing light beam. Detectors can be made out of III-V *p*-*i*-*n* structures in nanowires and have demonstrated high performance [128, 60]. The advantage of the TASE process employed in the Zurich group is that it allows for close coupling with co-planar silicon waveguides, while avoiding the complications stemming from large seed areas. The growth study in this thesis supports the control of heterointerface in nanowire devices and, more specifically, the integration of quantum wells in *i* regions of *p*-*i*-*n* structures. Nanowire *p*-*i*-*n* detectors fabricated at IBM Research Europe - Zurich have shown similar performance as bulkier *p*-*i*-*n* detectors from the University of Hong Kong [128, 60, 59]. Therefore, considering the existing know-how in Zurich, where the experimental part of my PhD took place, the IBM TASE process was used in this work.

2.3.2 State of TASE at the beginning of the project

This project started with the backdrop of the device published by Wen et al. [60], shown in its structure in Figure 2.6. The BF-STEM image in Figure 2.6(A) shows the morphology of the nanowire. A $\{1\,1\,1\}$ silicon facet on the right of the image served as the nucleation surface from which the heterostructures nanowire grew. The selection of this particular facet in TASE is not casual. The aim is to avoid monoatomic steps on the seed surface that can lead to the formation of APBs [46]. Nickel-gold contacts are placed at the two *p* and *n* extremities of the doped III-V *p*-*i*-*n* diode. These contact areas were defined specifically for the wire in question.

Figure 2.6(B) shows a composition map of the device created from energy dispersive X-Ray spectroscopy (EDS) data. It can be seen that the internal structure of the nanowire contains multi-faceted heterointerfaces. This is exemplified by the first phosphide layer (counting from the silicon seed on the right of the image towards the end of the wire on the left) which presents a bottom $\{1\,1\,1\}$ facet and one visible $\{1\,1\,0\}$ facet at the top, which is indicative of an "arrowhead" morphology implying the presence of a second $\{1\,1\,0\}$ facet at the top [50, 54, 55].

The heterointerfaces act as a "snapshot" of the shape of the growth front when the precursors were switched during metal-organic chemical vapor deposition (MOCVD). The second phosphide layer exemplifies the first issue with a multi-faceted growth front: the layer thickness varies depending on the vertical position in the layer. The second issue is that the contacting of the device is complicated, as it becomes difficult to predict accurately where each layer begins and ends. Even in this situation where the contacts were specifically defined for this device, the contact on the first phosphide layer also touches the arsenide intrinsic layer because of the arrowhead shape of the heterointerface. Further, having facets of different types will result in different growth rates and therefore loss of thickness control for quantum confinement structures

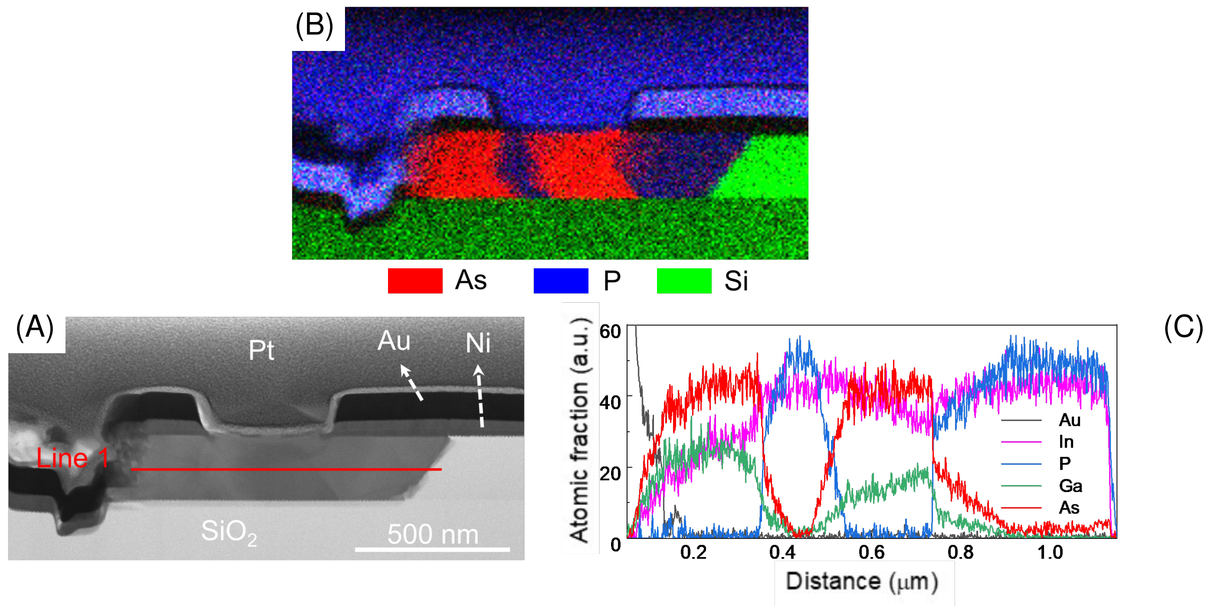


Figure 2.6: Structural and compositional analysis of a nanowire detector carried out by Wen *et al.* (A) shows a BF-STEM image of the nanowire detector. The Si seed is on the right, and the III-V wire grows out towards the left had side of the image, over the buried oxide layer. The Ni-Au contacts cover the *p* and *n* areas of the diode. (B) shows an EDS map highlighting Si, As, and P concentrations in the sample. Blue colouring on the metallic contacts is due to EDS peak overlap and is not indicative of P presence. (C) shows the composition profile along the wire length, as calculated from an EDS linescan along the path marked as "Line 1" in (A). This Figure was adapted from the work of Wen *et al.* [60] under the terms of the CC BY 4.0 licence [130].

such as quantum wells [52].

The third issue with a multi-faceted growth front is that, in ternary compounds, the integration of each III group element is dependent on the type of facet it is deposited onto [55], causing composition gradients within the wire itself with the potential to alter its absorption properties.

Composition gradients at the heterointerfaces are another issue that should be solved before fine structures such as superlattices can be accurately defined. As seen in Figure 2.6(C) these interface gradients can last hundreds of nanometres, if taken at face value. In reality, the complex geometry of the heterointerfaces also makes it impossible to determine exactly the size of these gradient areas.

Due to these observations, it becomes clear that the quality of devices built with the TASE process can continue to improve with the reliable integration of quantum wells in nanowires if defined heterointerfaces and constant thickness can be achieved. The potential of this technique for highly controlled quantum well integration in nanowires is given by the absence of side growth and the consequent elimination of core-shell architectures that could emerge in SAG, allowing for as good or better growth direction control as VLS techniques.

Stabilisation of a single $\{110\}$ facet has been achieved in homoepitaxy in SiO_2 templates, as shown by the integration of quantum wells [61]. Similarly, it has been found that it is pos-

sible to select the $\{1\,1\,1\}_B$ facet as a single growth front by changing the growth conditions, in homoepitaxy [53]. Selecting a $\{1\,1\,0\}$ growth front has been the preferred growth method given the high reduction in RTP formation in this growth regimen. However, stabilisation of a single $\{1\,1\,0\}$ growth facet from a $\{1\,1\,1\}$ silicon seed surface has been elusive [50].

As a result, this thesis focusses on stabilising a single $\{1\,1\,1\}_B$ facet as a growth front from a $\{1\,1\,1\}$ silicon seed surface inside a TASE template. The possibility of this stabilisation in TASE has already been shown in the literature [123, 54]. However, to my knowledge, no study on this growth regimen's reliability, yield, and possible applications has been published (aside from research that comprises part of this thesis in [1, 2]).

2.4 Implementation of the TASE process

The concept of TASE is relatively simple, consisting in the growth of III-V material in an enclosed SiO_2 template from a silicon seed [49, 48]. However, its experimental implementation to achieve a finished sample is lengthy. Thirty-five process steps (three of which are electron beam lithography (EBL) steps and one of which is an optical lithography step) involving 13 tools, four characterisation methods, and around 30 different chemicals are required to transform a silicon on insulator (SOI) wafer into a chip with III-V TASE-grown nanostructures ready for further study or contacting.

I used this fabrication process, starting from the pristine SOI wafer and ending with III-V structures ready for analysis, except for steps where otherwise stated. My main contributions to the TASE process involved optimising the MOCVD recipe and the design of the EBL masks.

2.4.1 Substrate and preprocessing

TASE uses the SOI wafer as its starting substrate: this is a $Si/SiO_2/Si$ wafer in which a thick silicon backplate supports a thin buried silicon oxide layer and an even thinner silicon device layer (Figure 2.8). Two different 8-inch wafers (Figure 2.7) were used in this work:

1. the $(0\,0\,1)$ wafer: Figure 2.8(A) shows the 2 µm thick buried oxide and 220 nm thick $\langle 0\,0\,1\rangle$ oriented silicon device layer. Figure 2.7(top) shows how this wafer was diced in four $6.5\,\text{cm} \times 6.5\,\text{cm}$ dices, plus edge pieces, and that there are no in-plane $\langle 1\,1\,1\rangle$ directions in this wafer.

2. the $(1\,1\,0)$ wafer: Figure 2.8(B) shows the 150 nm thick buried oxide and 70 nm thick $\langle 1\,1\,0\rangle$ oriented silicon device layer. Figure 2.7(bottom) shows how this wafer was diced in four $6\,\text{cm} \times 6\,\text{cm}$ dices, plus edge pieces.

The tool responsible carried out the dicing cuts at a wafer dicing machine. Every dice is designed to be further divided into nine identical $2\,\text{cm} \times 2\,\text{cm}$ smaller dice that, in turn, contain

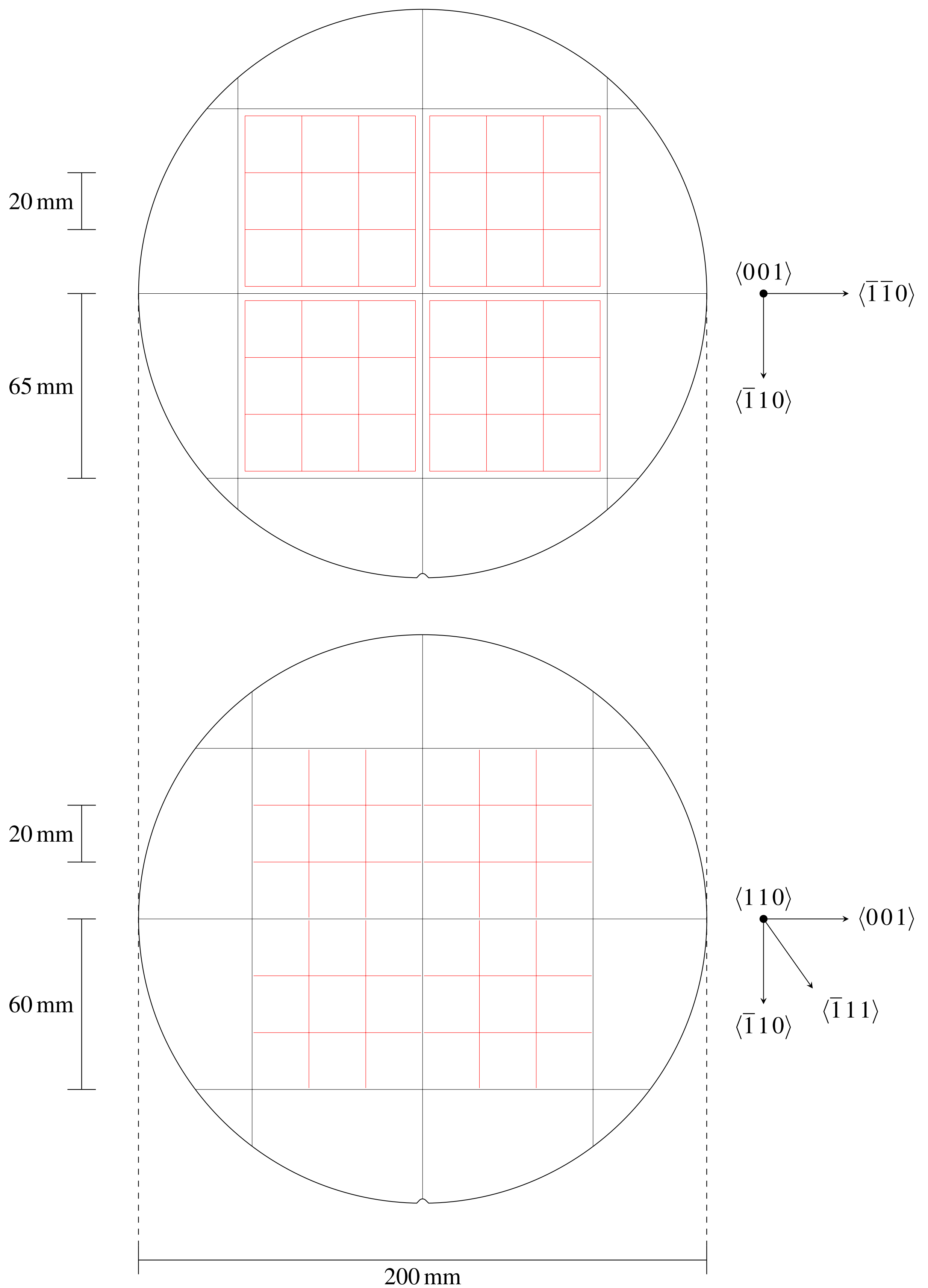


Figure 2.7: In-plane and perpendicular directions; and dimensions for the two SOI wafers employed in this thesis. 6.5 cm × 6.5 cm and 6 cm × 6 cm dicing is shown in black and the following 2 cm × 2 cm cuts in red.

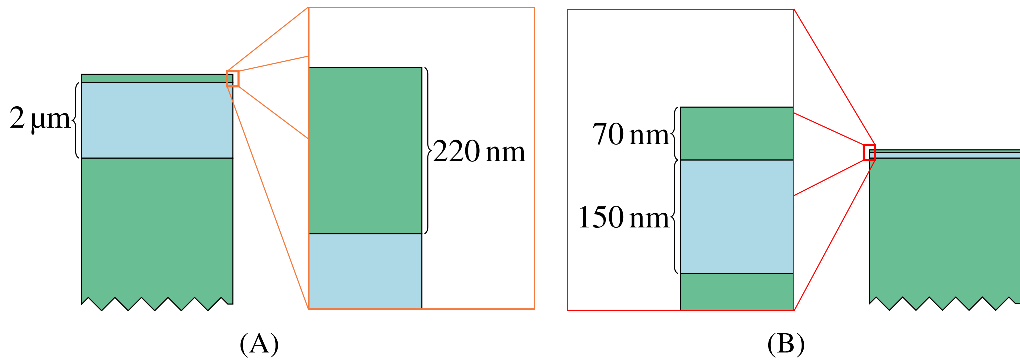


Figure 2.8: Drawing of the layer stack of the two SOI wafers showing different layer thicknesses, Si is represented in green and SiO_2 in light blue. The cross-section of the ⟨0 0 1⟩ wafer is shown in (A) with a magnified insert showing the 220 nm - thick Si device layer. The layer thicknesses in (B) are proportional to the ones in (A) highlighting how thin the SiO_2 (150 nm) and Si (70 nm) layers are in comparison.

the EBL write regions. This means that every large dice produces nine smaller sample dice that all include the same nanostructure designs but can be grown separately: this considers the possibility of error or damage to some of the smaller dice during processing. The first wafer was cut in 6.5 cm × 6.5 cm dice for ease of handling at the EBL machine. However, it was found that this presented issues with other tools at later steps. Therefore the dice dimensions were reduced to 6 cm × 6 cm for the second wafer. Figures 2.9, 2.10, and 2.11 show schematic drawings of the primary process steps as they appear when applied to the ⟨1 1 0⟩ wafer, but the process steps are the same on the ⟨0 0 1⟩ wafer.

The device layer defines the shape of the silicon seeds and III-V nanostructures. To do so, two lithography steps are needed, one defining the geometry of the wires and one opening the template oxide that encases them. The alignment between these two steps is critical. Much like the definition of the nanostructures themselves, it requires an accuracy of the order of the nanometre on a dice size of 2 cm. This resolution is only available with electron beam lithography (EBL) in a research environment. A third EBL step is introduced to ensure correct alignment. Markers that the EBL machine will use to determine the position of the sample with the necessary accuracy are defined in this process step. While I created the mask designs and provided the substrate ready for exposure, given its high degree of complexity, automation, and workload, the machine was loaded and operated by the tool responsible.

The creation of the alignment markers constitutes an important pre-processing step. A 10 nm thick SiO_2 protective layer is deposited on top of the device layer using plasma-enhanced chemical vapour deposition (PECVD) before sputtering a 100 nm tungsten (W) layer on top of the wafer (Figure 2.9(A)). The sputtering tool was operated by the responsible for the tool. Tungsten is used to achieve high contrast in the electron microscopy image that the EBL machine uses to orient itself on the sample. A negative photoresist is spun before submitting the wafer for the first EBL run. During this step, the EBL markers are defined in the resist, which, after

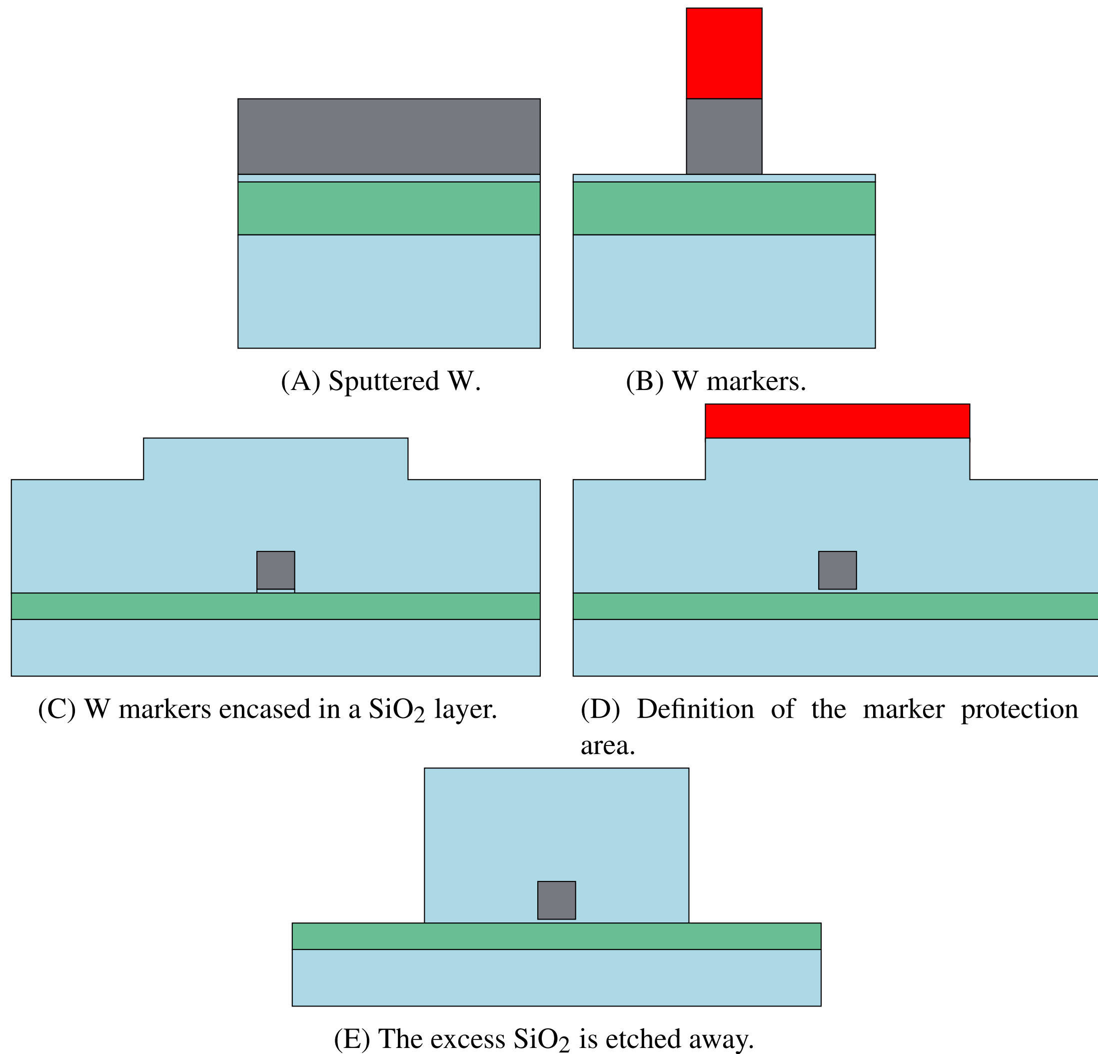
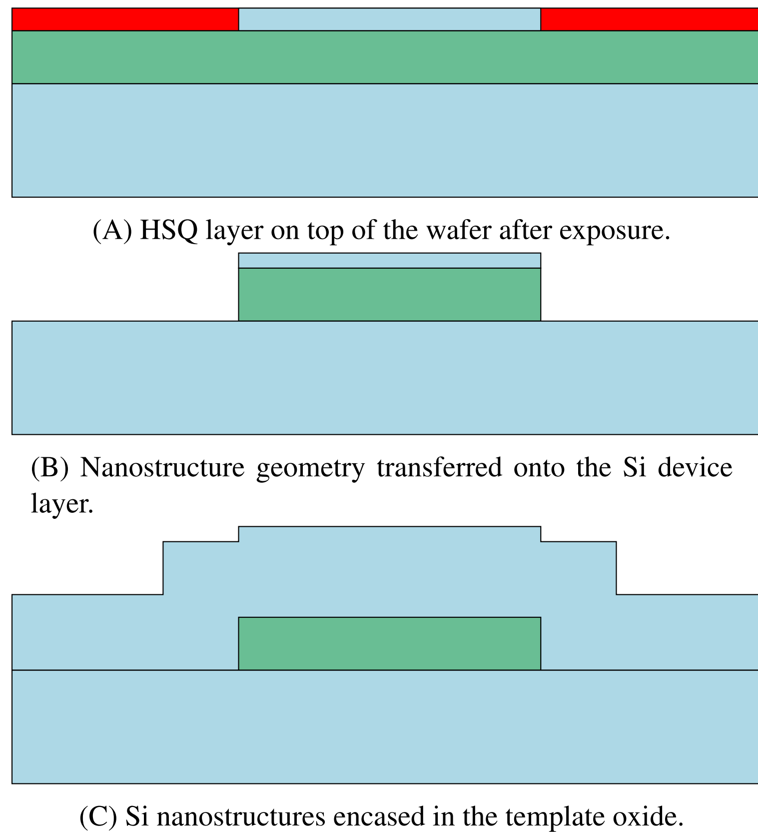


Figure 2.9: Drawings showing the fabrication process of the W markers and marker protection. The sputtered W layer (A) is first patterned (B) and then encased in 300 nm-thick SiO_2 layer (C). The marker protection area is defined through optical lithography (D), and then the excess SiO_2 is removed (E).

development, acts as a mask that protects only certain areas of the tungsten layer. Reactive ion etching (RIE) is used to remove the unprotected tungsten: this leaves well-defined markers on the wafer (Figure 2.9(B)).

The alignment markers are then protected from the next aggressive etching steps that follow in the TASE process by depositing a 300 nm thick silicon oxide layer on the entire wafer with PECVD. This protective layer is then annealed at 750 °C for 300 s to improve its resistance to etching (Figure 2.9(C)). This cover shields both the alignment markers and the device layer. However, the device layer must be accessible to define the nanostructures that will form the base of the TASE process. Optical lithography is used to pattern openings in a positive optical resist, leaving only the areas of the SiO_2 film above the tungsten markers masked (Figure 2.9(D)). After development, the silicon oxide layer can be removed in correspondence with these openings



(A) HSQ layer on top of the wafer after exposure.

(B) Nanostructure geometry transferred onto the Si device layer.

(C) Si nanostructures encased in the template oxide.

Figure 2.10: Drawings showing (A) the HSQ layer after exposure (red unexposed, blue exposed), (B) the nanostructures as defined in the device Si layer, and (C) the nanostructures encased in the template oxide.

using a diluted hydrofluoric acid (HF) solution (Figure 2.9(E)), uncovering most of the device silicon layer. Reflectometry can ascertain the presence and thickness of the device silicon layer, thereby evaluating the health of the wafer after the pre-processing steps.

This concludes the initial steps that prepare the wafer to go through the TASE process. In the following illustrations (Figures 2.10 and 2.11), the tungsten markers and their oxide protection are omitted as they will not be affected by the following process steps in a process-relevant manner. Still, they are not removed and are the basis for alignment in the next lithography steps.

2.4.2 Nanostructure definition and template deposition

The first step of the TASE process is to define the geometry of the seed and the nanostructure. An EBL mask is designed using mask design software, such as L-Edit, and has to be then transferred onto the device silicon layer: practically, this is accomplished using hydrogen silsesquioxane (HSQ) as a resist. This negative electron-sensitive resist allows for very high-precision pattern transfer through EBL. After development, HSQ leaves a thin layer of silicon oxide covering the area corresponding to the nanostructures that will be fabricated (Figure 2.10(A)). The unprotected device layer silicon is removed using hydrobromic acid (HBr)-based inductively-

coupled plasma (ICP) etching. The resulting silicon nanostructures reflect the geometry of both the silicon seed and the III-V wire that will be grown (Figure 2.10(B)).

The template silicon oxide is then deposited and encases the silicon nanostructures as illustrated in Figure 2.10(C). The template deposition step is particularly delicate as the template oxide must closely follow the geometry of the silicon nanostructures. Atomic layer deposition (ALD) enables this level of precision. With this method, the template oxide grows in steps: first, a complete layer of oxygen atoms is deposited, followed by an entire layer of silicon atoms, and so on. Although time-consuming, this growth allows the template oxide to closely follow the geometry of the silicon nanostructures and grow in an ordered manner, resulting in strong etch resistance.

2.4.3 Etch-back and growth

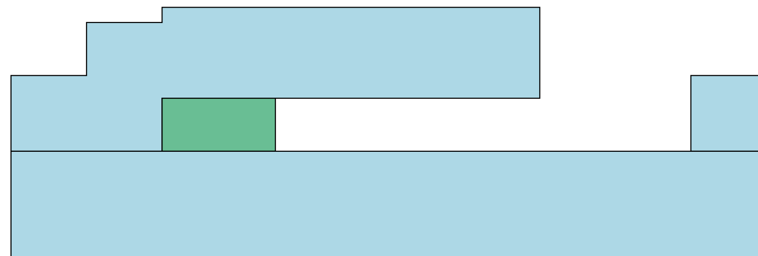
The last lithography step involves defining the opening areas in the template oxide through which the etch back and growth occur. Holes are defined in a positive resist layer (Figure 2.11(A)). After EBL exposure and development, RIE is used to etch the template oxide and the device silicon underneath through these holes, with good vertical selectivity (Figure 2.11(B)). After opening the template, each $6.5\,\mathrm{cm} \times 6.5\,\mathrm{cm}$ or $6\,\mathrm{cm} \times 6\,\mathrm{cm}$ dice is further cut into smaller $2\,\mathrm{cm} \times 2\,\mathrm{cm}$ dice that will then be etched back and grown singularly as described in the following paragraphs.

Excess silicon to be substituted with III-V material is removed using a $2.5\,\%_{\mathrm{V/V}}$ tetramethylammonium hydroxide (TMAH) / water (H_2O) solution heated at $80\,^{\circ}\mathrm{C}$. This solution has a reliable etch-back speed of $60\,\mathrm{nm\,min^{-1}}$. The etch back proceeds from the template openings to leave only the seed area inside an empty silicon oxide template where the III-V crystal will grow (Figure 2.11(C)). TMAH is specifically chosen because it has good selectivity to silicon, therefore leaving the SiO_2 template mostly unaffected. A small amount of template etching still takes place and must be considered when etching multiple micrometres of silicon by depositing a thicker template oxide in previous fabrication steps. Another advantage of TMAH etching is that it results in silicon seeds terminated by $\{1\,1\,1\}$ facets that avoid antiphase boundary formation during metal-organic chemical vapor deposition (MOCVD) [46]. After etching, the chip is ready for III-V material growth, pre-growth surface treatment steps include a dip in a 2:1 sulfuric acid (H_2SO_4) / peroxide (H_2O_2) solution to remove organic contaminants and a further $10\,\mathrm{s}$ dip in a diluted HF solution to remove the native oxide layer.

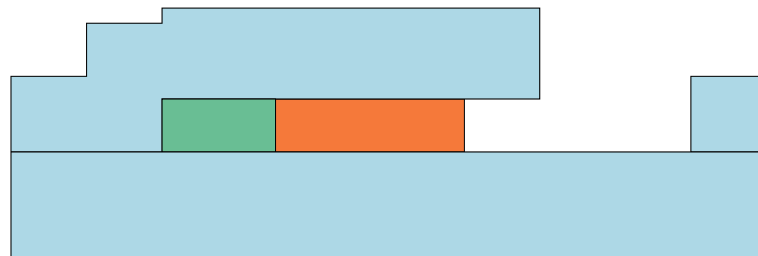
Before growth and in the chamber, the chip is also thermally treated at $750\,^{\circ}\mathrm{C}$ for $3\,\mathrm{min}$ in an As atmosphere to facilitate oxygen desorption from the silicon seed. The nucleation of the III-V material is selective to the silicon seeds. This means that the growth of the III-V nanostructures is limited to the areas defined in the previous lithography steps (Figure 2.11(D)). At the beginning of this project, the DESIGN-EID consortium chose to investigate the growth and properties of indium-gallium arsenide (InGaAs) / indium phosphide (InP) material systems.

(A) Openings patterned on a positive resist layer.

(B) Etch down of the template SiO_2 and device Si to reach the buried oxide layer.



(C) Etch back of the Si to create the seed.



(D) A III-V crystal (orange) was grown from the Si seed.

Figure 2.11: Drawings showing the last steps of the TASE process. A positive resist layer is patterned (A) and used as a mask for the RIE etch-down of holes in the template SiO_2, exposing a vertical and flat Si surface (B). TMAH etch-back (C) and MOCVD growth follow, creating a III-V nanostructure (orange) in the place previously occupied by Si (D).

Growth MOCVD growth took place in a showerhead type reactor, operating at a pressure of 60 Torr (0.08 bar). A rotating susceptor capable of holding up to three 2 in wafers was used to accommodate 2 cm × 2 cm chips containing the TASE structures. Two different lines were used for III and V precursors, which were stored in bubblers and transported to the reactor using a hydrogen flow. The precursors used in the growth of III-V material are:

- trimethyl indium (TMIn),
- trimethyl gallium (TMGa),
- *tert*-butyl arsine (TBAs),
- *tert*-butyl phosphine (TBP),
- trimethyl antimony (TMSb)

Before growth, a 10 s hydrofluoric acid (HF) dip was performed to remove native SiO_2 from the seed surfaces. A further oxygen desorption step was carried out in hydrogen atmosphere in the reactor by raising the susceptor temperature to 750 °C. The nucleation and growth of the III-V semiconductor was carried out at the temperature of 580 °C. Each sample employed a different precursor step sequence, and they are shown in the following experimental chapters, together with the V/III ratios loaded into the reactor. In general, low temperature growth coupled with high V/III ratios was chosen from the beginning as it was proven to aid in the stabilisation of growth fronts with a lower number of facets [53].

2.5 Characterisation of nano- and microstructures

The main difficulty in the characterisation of sub-micrometre structures is their small size. Even techniques instrumental in determining lattice properties, such as X-ray diffraction and Raman spectroscopy, struggle at this size.

Optical methods are limited in spot size by the diffraction limit and the deviation from the ideal behaviour of optical components. Still, optical techniques such as photoluminescence can provide important information on sub-micrometre structures in the correct conditions, as the right excitation wavelength can, for example, provide information on specific material layers with thicknesses well below the diffraction limit [85]. Some techniques to overcome the diffraction limit have been devised. Tip-enhanced Raman spectroscopy (TERS) is one of the techniques that exploit the tip-effect to enhance the electromagnetic field near a metallic tip of sub-micrometre sharpness [131]. While this method greatly increases the lateral resolution of Raman spectroscopy, it is also primarily a surface method, not well suited to analise III-V structures encased in 50 nm-thick SiO_2 templates. Another imaging method is scanning near-field optical microscopy (SNOM), in which a sharp metallic point and an optical fibre is used

to hyperfocus light to achieve nanometre-scale lateral resolution [132]. This method can be particularly powerful when damage from the electron beam of a SEM is feared or when imaging dielectric material, where sample charging can result in a distorted image. Given the absence of either of these issues in samples explored in this thesis, SEM, which reaches equivalent levels of resolution with more versatility in magnification choice, was used for imaging. Techniques that require additional process steps such as the deposition of metals and following etching of openings to create an optical mask are not time competitive and present fabrication risks. A better alternative to optical masks, if extensive optical analysis is planned, would be the inclusion of isolated single nanowire structures in the EBL mask during the fabrication stage.

Laboratory-sized X-ray equipment has a spot size of more than one centimetre. Therefore, crystallographic information cannot be accessed through X-ray methods unless extremely high-cost facility-size tools such as a synchrotron beamline are used.

Transmission electron microscopy (TEM) and its scanning version scanning transmission electron microscopy (STEM) allow atomic-resolution imaging of thin (sub 100 nm in thickness) slices of material. In this thesis, most nanostructure characterisation was carried out using a scanning transmission electron microscope. Due to the complex interactions between the high-energy (200 keV for the tool used in this work) electron beam and matter, a compositional as well as structural information can be extracted from the sample in a single measurement. In a STEM the electron beam spot size determines the resolution of spectrographic methods such as energy dispersive X-Ray spectroscopy (EDS) and electron energy loss spectroscopy (EELS), which can go down to atomic resolution [133].

The main spectrographic technique used in this thesis is EDS. The X-ray signal recorded in this technique is generated when, after the electron microscope's beam dislodges a core electron from an atom, an electron from the outer shell falls to fill the vacancy, emitting a photon. This photon can be collected by one (or more) X-ray spectrometers [134]. Since the cross-sections of each of the possible processes and the energy of the X-rays emitted are known for each element, it becomes possible to calculate relative elemental concentrations and therefore have access to the compositional information of the material [135].

The main disadvantages of STEM are that the microscopes required to achieve this level of resolution are very expensive, that sample preparation is destructive, and that the entire sample preparation process is very time-consuming. If and when a correlation between the geometry of the entire micro- or nanostructure and its internal morphology can be established, scanning electron microscopy (SEM) becomes a faster survey method that can acquire data over chip-sized surfaces in reasonable time frames. Automated SEM data collection combined with computer vision analysis, powered by machine learning, can speed up the yield calculation of nanostructures with critical features smaller than the diffraction limit that cannot be imaged with traditional optical microscopy [136, 137, 138].

Chapter 3

III-V growth in TASE samples

For over a decade, research on monolithic integration of III-V semiconductors has been conducted at IBM Research Europe - Zurich. The template assisted selective epitaxy (TASE) method was thought of and developed during this long research effort [48, 139]. TASE was then applied to integrate emitting and absorbing electronic elements, such as lasing microdisks and nanowire-based photodetectors. As I joined IBM, research on both of these device architectures was still ongoing, and, as I was familiarising myself with the tools necessary to conduct my research in the first months of my PhD, I had the opportunity to cooperate with other team members on their projects. Dr. Wen led one such project and aimed to create a single nanowire photodetector. In the end, the project achieved its goal, as seen in [60]. However, one particular aspect that still needed improvement if the single sample shown in the paper was to be reproducible was the control of the growth front morphology.

Controlling the morphology of the growth front is essential for several reasons. The first is that by ensuring a specific shape of the various heterolayers, the metal-to-semiconductor contact regions can be determined more accurately, aiding in further process steps. The second reason concerns the different integration rates of III group elements on different facets. This was already explored by researchers who showed a marked dependence of the atomic fraction of the III group element in InGaAs from the facet on which it was grown [55].

This chapter expands on the research published by my co-authors and me in [1]. The most common crystalline defects observed in STEM images of TASE grown structures will be discussed to complement this chapter's compositional and morphological introduction. An in-depth exposition of the nanowire design and growth recipes and their analysis, explaining the evolution of the methodology from a simple thick lateral heterostructure to a multi-quantum well architecture with single facet heterointerfaces, follows. When discussing the order of appearance of the wire's internal structure in this thesis, the reference point is set at the silicon (Si) seed interface, regardless of its position in the image.

3.1 Initial measurements on pre-existing samples

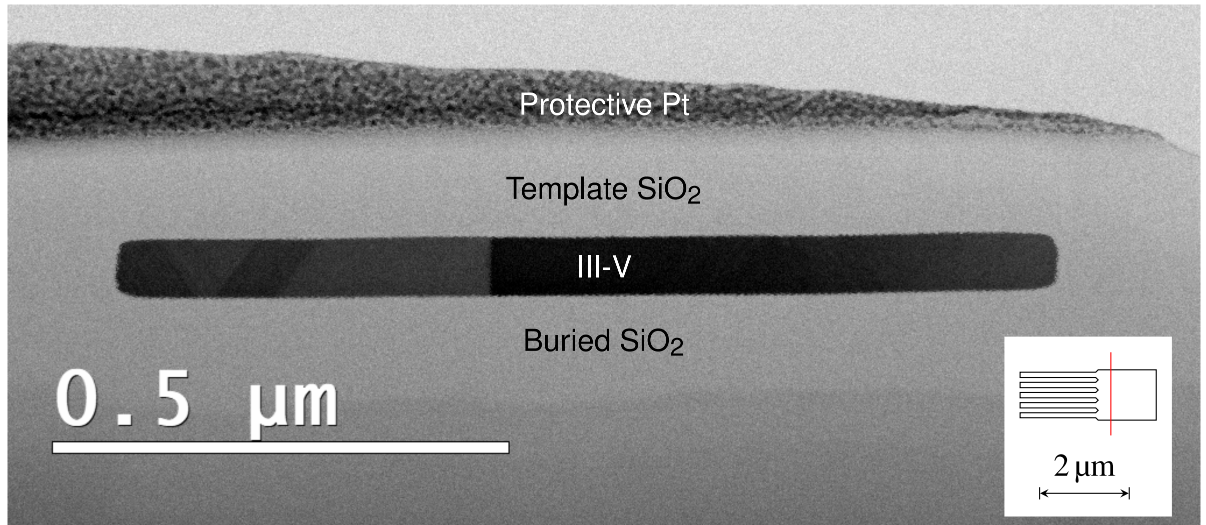
As the previous section shows, TASE has been developing for the last decade [140]. As such, when I started working on the project, an initial study was conducted to determine the crystalline quality of TASE-grown structures from other ongoing projects.

3.1.1 Defects in TASE samples

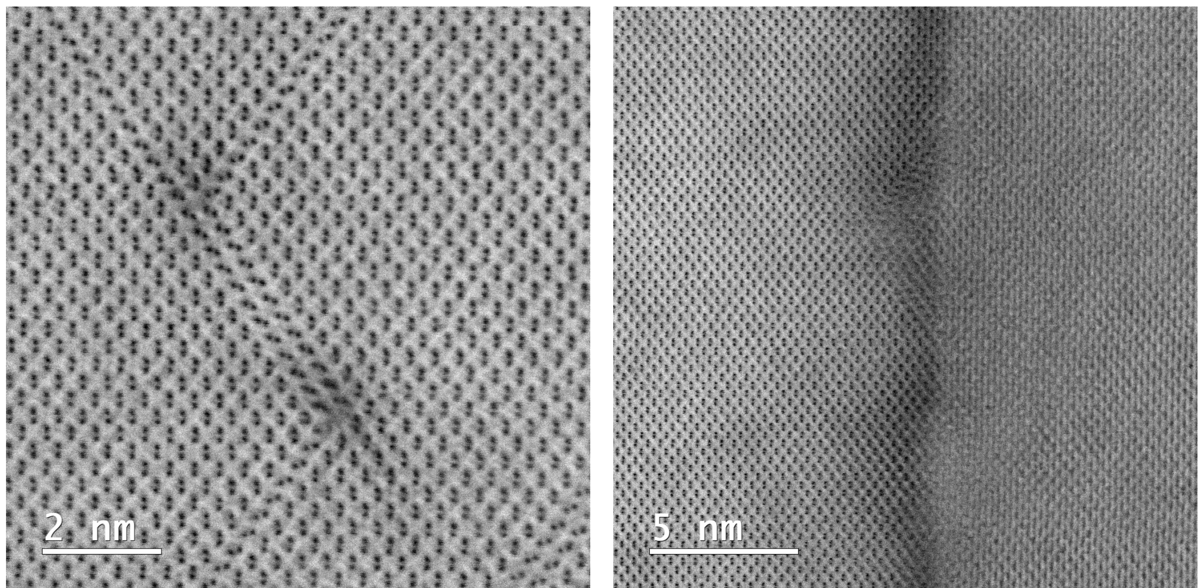
Rotational twin planes (RTPs) were found to be the most common crystalline defect from the characterisation conducted on TASE-grown samples throughout the project. A widespread presence of micro twins was found in all samples [1, 2], even those dating to before the start of the project [51]. Only one of the structures, created by merging different nanowires into a larger platelet, had dislocations (Figure 3.1(B)).

The sample in Figure 3.1 was grown by Svenja Mauthe before the beginning of my stay at IBM Research Europe - Zurich as part of her study on the controlled introduction of dislocation at the merging point of two growing crystals [139]. A cross-section of a structure deriving from one such experiment is shown in Figure 3.1(A). This lamella was cut in the area of the device where the wires had already merged. Two areas of the structure stand out particularly: on the left side of the image, a series of "v-shaped" parallel lines denote the presence of two-fold rotational twin plane (RTP)s in orthogonal $\{1\,1\,1\}$ planes. In this region, Figure 3.1(B) shows the two stair-rod dislocations forming where two twin planes intersect or when one is annihilated and the other changes direction. This type of defect was the subject of an in-depth study by Bologna et al. [133], but it will not make another appearance in any of the other scanning transmission electron microscopy (STEM) images recorded during my studies. However, it should be noted that the vast majority of cross-sections imaged from this point on were cut along the growth axis instead of perpendicularly to it as this one was. Figure 3.1(C) shows the interface between the light grey and dark grey segments that comprise the III-V crystal in Figure 3.1(A).

As made clear by the definition with which the atomic columns are visible on the left-hand side of Figure 3.1(C) the sample was orientated to achieve the channelling condition of the STEM electron beam in the corresponding crystal. The crystal's lattice on the right-hand side of the same image does not appear as clearly defined: a slight rotation at the time of nucleation might have happened for one of the two seeds pictured. Of course, since the platelet originated from five different seeds, an empirical assumption can be made about two of them prevailing over the other three. This hypothesis is further supported by the presence of RTPs on the leftmost portion of the crystalline slice in Figure 3.1(A). At the same time, the area to its immediate right does not show signs of RTPs, hinting at the possibility of growth developing in two different directions.



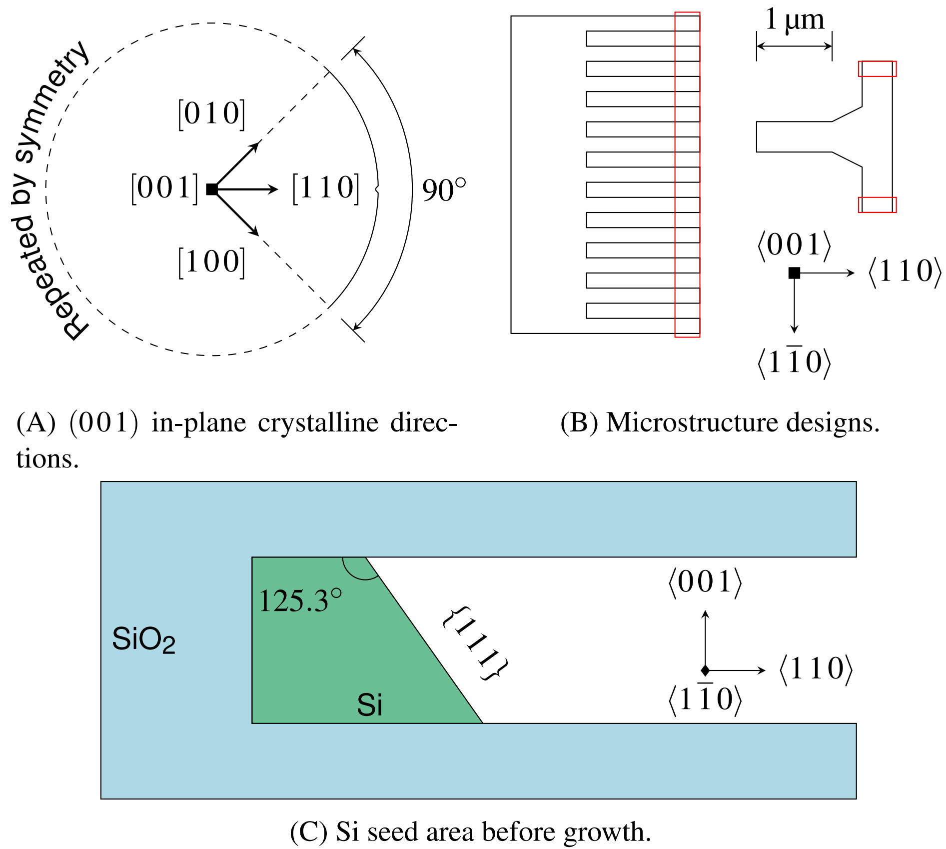
(A) Cross-section (cut marked in red in the insert showing the topd down view of the structure) of a multi-seeded coalesced III-V structure grown on Si.



(B) Detail of twin planes and dislocations.

(C) Detail of a grain boundary.

Figure 3.1: BF-STEM images of a cross-section of a TASE structure. (A) overview image of the entire platelet. Two regions can be identified in this image, with the leftmost area of the left section presenting an area with darker lines describing a "v" shape. These lines are caused by RTPs. (B) a pair of stair-rod dislocations [133] imaged in high-resolution. (C) high-resolution image of the area in which the two regions in (A) meet.



(A) $(0\,0\,1)$ in-plane crystalline directions.

(B) Microstructure designs.

(C) Si seed area before growth.

Figure 3.2: Wafer symmetry and microstructure design. (A) shows the in-plane low-index crystalline directions in a $(0\,0\,1)$ wafer, using a 90° arc centred around the notch that indicates the in-plane $[1\,1\,0]$ direction. The rest of the directions can be deduced by the symmetry defined by the four-fold axis perpendicular to the wafer plane. (B) illustrates two different microstructure designs, comb arrays and T-shaped structures, complemented by a scale bar and an in-plane orientation guide. The black designs were transferred to the device Si layer of the SOI wafer, while the red designs marked the position of the template openings. (C) is a drawing of the Si seed area showing its configuration after etch-back for a structure orientated along an in-plane $\langle 1\,1\,0 \rangle$ direction.

3.2 Fabrication on Si$(0\,0\,1)$ SOI

Nanofabrication was carried out with the TASE process (see Section 2.4 for details) and, together with the later sample characterisation, took place in highly controlled environments such as a cleanroom and noise-free lab (see Appendix A). Firstly, the shape of the ensemble of nucleation seed and nanostructure is transferred to the silicon device layer of the SOI wafer through a series of lithographic and etching steps. The template, composed of SiO_2, is then deposited on top of the resulting microstructures. Finally, the template is opened in one or more positions before the etch-back of the sacrificial silicon volume and the introduction of metal-organic chemical vapor deposition (MOCVD) grown III-V semiconductor in its place [49, 48].

Initial growth experiments focussed on nanowires, one of the simplest geometries. The relative simplicity of the nanowires allows for the study of the impact of even minor modifications

of the growth recipes on the final crystal, both in terms of structure and composition.

3.2.1 Template design considerations

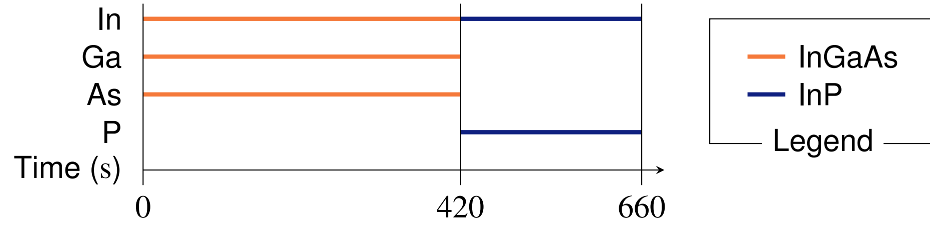
The orientation of the TASE template on the silicon $(0\,0\,1)$ surface, and therefore the crystalline direction along which the growth will take place, is the first key factor in determining the final shape of the crystal. In the silicon space group 227 [141], the $\langle 0\,0\,1 \rangle$ vector contains a four-fold axis, represented by a square dot in Figure 3.2(A). If we were to examine the possible in-plane directions within an arbitrary 90° angle, we would find them repeated three more times in the remaining in-plane 270° arc because of this symmetry element. Figure 3.2(A) shows this principle applied to the $(0\,0\,1)$ wafer used to fabricate the first samples. By drawing a 90° angle around the notch indicating the $[1\,1\,0]$ direction and highlighting the low-index in-plane directions, the two equivalent $[0\,1\,0]$ and $[1\,0\,0]$ directions define the edges of the arc. Although the cubic III-V semiconductor phase is zincblende (space group 216) [142, 143, 144, 145], equivalent symmetry considerations can be made, provided the polar nature of the compound is taken into account.

Most previous TASE nanowire growth experiments have used the $\langle 1\,1\,0 \rangle$ vector as the primary in-plane growth axis [61, 50, 74, 49]. Therefore, this direction was selected as a starting point to analyse the growth results. Figure 3.2(B) shows the two designs divided by colour in the two electron beam lithography (EBL) exposures during fabrication with scale and direction relative to the crystal. For the first design, the black pattern comprises a series of 11 nanowires and a back anchor in a comb-like structure. These, while maintaining a constant wire length, were designed in multiple wire widths ranging from 50 nm to 500 nm. In contrast, the second design is shaped as a capital "T" with a wire thickness ranging from 50 nm to 400 nm.

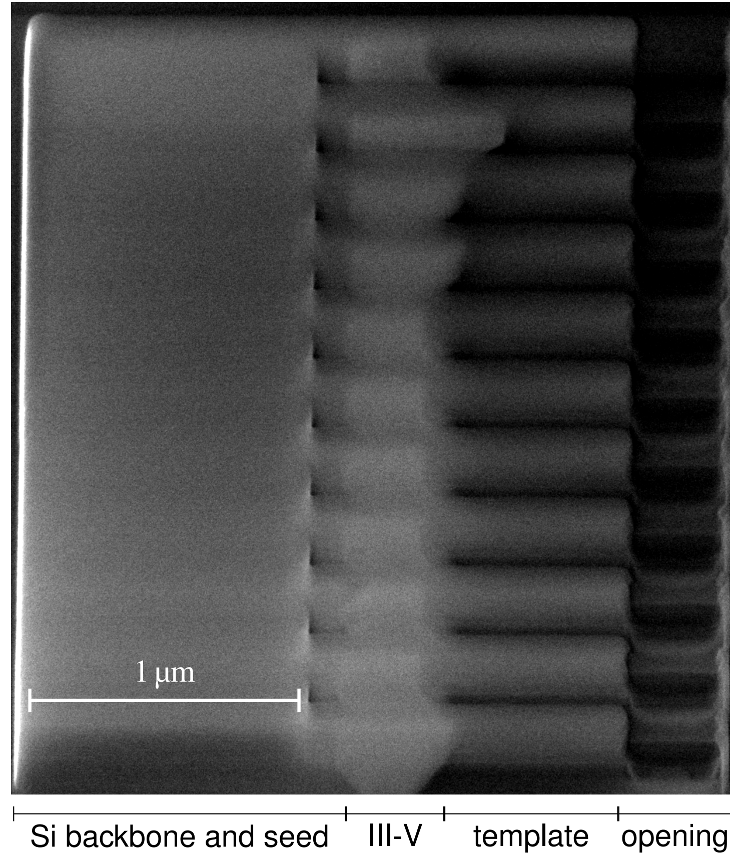
While the comb-like design is just meant to grow a group of nanowires close together to facilitate scanning electron microscopy (SEM) analysis, the T-shaped design was meant to test a theory reliant on the stabilisation of a single $\{1\,1\,0\}$ growth facet. If such a stabilisation was achieved in a layer by layer growth regimen it would mean that, past the initial nucleation region, only RTPs containing the growth direction would be able to propagate forward. At the T-junction, if only $\{1\,1\,0\}$ side facets were created, the resulting material in the two arms of the T would be defect-free. This early experimental idea didn't materialise as (as seen later in Figure 3.7(B)) the template length were too mismatched in this first experiment to provide the necessary etch back time to result in a single seed, and was not attempted again as experimental findings moved the focus towards the stabilisation of RTP-prone $\{1\,1\,1\}$ facets as growth fronts.

These designs are transferred onto the silicon layer by selectively etching the superfluous material around them. Subsequently, the resulting structures are encapsulated in a SiO_2 layer that forms the template. EBL is then used to define the area of the template to be opened (in red in Figure 3.2(B)).

Figure 3.2(C) shows the situation of the silicon seed of one of the nanowires after template



(A) Precursor sequence [1].



(B) 52° tilted image of III-V nanowires.

Figure 3.3: Growth of the first sample. (A) diagram representing the precursor sequence for a single-heterointerface III-V wire [1]. Each line represents an active flow of precursor into the reactor. The colour of the horizontal lines represents the target material. (B) shows a SEM image of an 11-nanowire array. The Si seed, III-V segment, empty template, and template opening are visible from left to right.

Table 3.1: V/III molar ratios injected in the reactor during each material deposition step [2].

Material	V/III ratio
InP	234
InGaAs	29

opening and etch-back of the microstructured silicon device layer. It is encased on all but one side by the oxide template and the buried oxide. It presents a surface composed of one (or, as seen experimentally, two, with one being larger than the other in most seed surfaces) $\{1\,1\,1\}$ facets because of the chemistry of the TMAH etch, which is slower on this densely-packed facet [146]. The acute angle that this type of facet forms with the template can easily result in unwanted effects, such as incomplete template filling in the seed area [129].

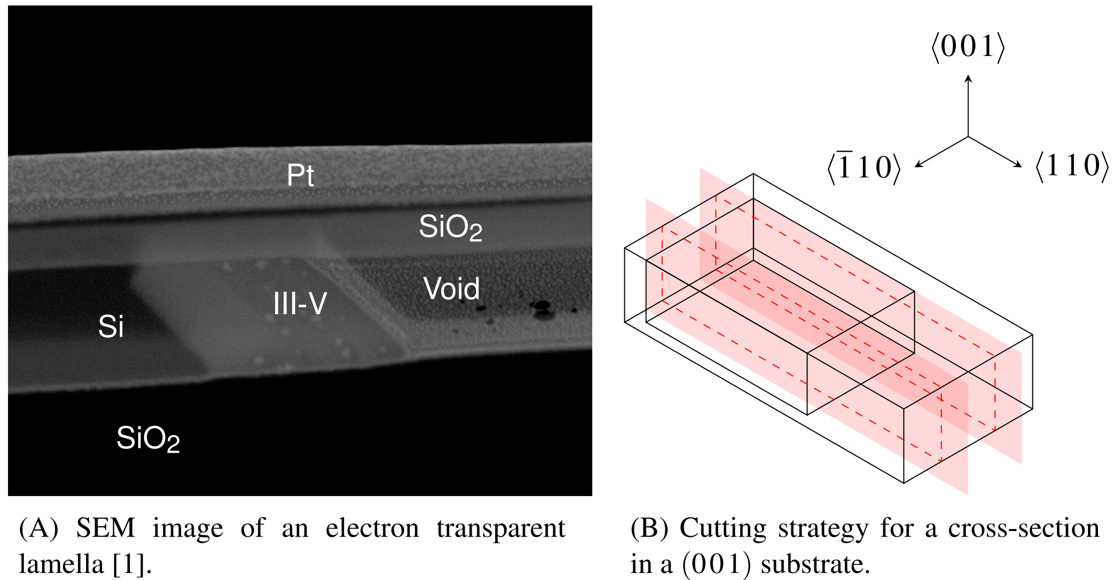
3.2.2 Simple precursor switching sequence

The second key factor in determining the shape of the growing crystal is the individual growth rate of each facet. Growth conditions, including temperature, precursor molar flow, III/V ratios, and chemical species, are the key to determining the low-index facet growth rate [54, 147].

After all the fabrication and pre-processing steps, the growth of III-V material occurs in an metal-organic chemical vapor deposition (MOCVD) reactor at 580 °C. The precursor sequence used for the first growth experiment is shown in Figure 3.3(A). In this image, the flow of a precursor into the reactor is represented by a horizontal line, and the colour of each line indicates the target material.

The objective of this growth run was to study the evolution of growth and evaluate the effects of the growth parameters on the morphology of the two material segments. Two different III-V segments were grown for this sample with the deposition times of 420 s and 240 s for the InGaAs and InP segments, respectively. Table 3.1 summarises the V/III molar ratios used. These were chosen according to those used in previous experiments to aid in recognising patterns that could be improved upon during growth without unexpectedly influencing parameters such as nucleation yield and growth rates.

The SEM image in Figure 3.3(B) shows a comb array with 11 nanowires after MOCVD growth. The structure segments are marked: on the right side of the image, the holes through which the precursors entered the templates are visible. The image was captured with the sample fixed on a stage that was tilted 52° with respect to the $\langle 0\,0\,1 \rangle$ direction in the device layer of the SOI device layer before FIB cutting. The shape of the end facet of each nanowire is visible due to the tilt, with most wires terminating with a $\{1\,1\,1\}_B$ facet. Only one of the wires, the second one from the top, appears to have a different end-facet. The third wire from the bottom presents an interesting (but not unique, as shown in [129]) situation where the growing crystal leaves the seed partially uncovered. Two $\{1\,1\,0\}$ facets form an arrowhead-like shape, indicating the presence of faster growth in the $\langle 1\,1\,1 \rangle$ direction compared to the $\langle 1\,1\,0 \rangle$ directions immediately after nucleation.



(A) SEM image of an electron transparent lamella [1].

(B) Cutting strategy for a cross-section in a (001) substrate.

Figure 3.4: FIB cut of a lamella from a $\langle 001 \rangle$ SOI wafer. (A) shows the SEM image of a thinned electron-trasparent lamella. The various materials are marked, and the structure is discernible. (B) shows how the cut is made within the context of the crystalline and growth directions. The red-shaded planes show that the cut was selected to expose the sides of the wire in correspondence to a $\{\bar{1}10\}$ plane, if the template axis was labelled as a $\langle 110 \rangle$ direction. (A) was adapted from the work of Brugnolotto *et al.* [1] under the terms of the CC BY 4.0 licence [130].

3.2.3 FIB lamella fabrication

A high-resolution analytical method is needed to analyse the type of structures shown in Figure 3.2(B). Indeed, their small size means that, for example, X-ray analysis with laboratory-sized tools is unfeasible. Instead, microscopy techniques are particularly powerful, with high-end transmission electron microscopy (TEM) or scanning transmission electron microscopy (STEM) able to resolve features up to atomic resolution and provide important structural information. However, an electron-transparent lamella is required to analyse material layers and investigate the morphology of internal heterointerfaces. Focused ion beam (FIB) tools can create these $<$100 nm thin semiconductor cross-sections. In this study, an FEI Helios NanoLab 450S was used.

Figure 3.4(A) shows how one lamella looks once FIB cutting is complete. This image is perfect for showcasing the various material portions of the sample while retaining a three-dimensional view, which is lost in the later STEM analysis. The silicon seed is visible on the left, followed by the III-V material layer, which appears brighter in the centre of the image. On the exposed surface of this layer, two areas can be characterised and distinguished by the presence of small indium droplets (on the right) and their absence (on the left). These indium droplets are commonly formed during the ion milling of indium phosphide at the FIB tool.

On the right side, the empty template is filled with a platinum lace-like structure consisting of a web of platinum nanoparticles appearing as dots in the "void" area in Figure 3.4(A). This

is essentially a very low-density platinum structure formed when the protection layer was deposited before the lamella was cut from the chip. During this process, a metal-organic platinum precursor is made to flow over the chip and broken up by the ion beam of the FIB. The resulting platinum atoms form a protective layer on top of the chip, however, a few enter the TASE cavity and are deposited on the sidewalls, creating this low-density structure.

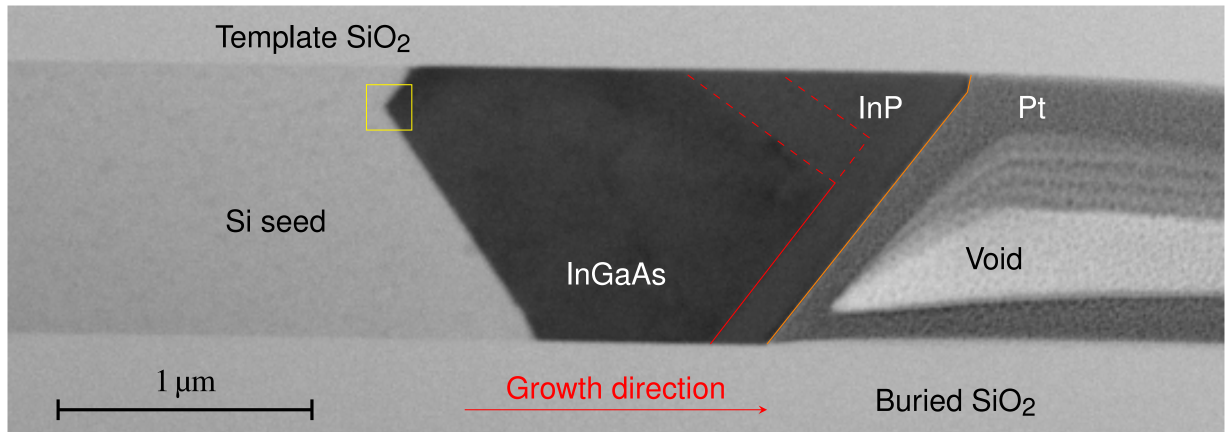
The upper and lower interfaces of the template are visible in this image, appearing as two ribbons or bands above and below the silicon / III-V / void structure. In particular, the upper interface is the most visible; they can be easily spotted by looking at the silicon region. What remains of the platinum protective layer is also noticeable as a bright region at the very top of the structure.

The objective of the cut strategy shown in Figure 3.4(B) is two-fold. The first aim is to provide a lamella that showcases both the seed and end facets to evaluate the evolution of the growth front, and the second is to have access to a low-index facet that can provide structural information on the quality of the lattice. For the zincblende phase, the second criterion is satisfied by $\{1\,1\,0\}$ facets [148]. In a $\{0\,0\,1\}$ SOI there is an in-plane $[\bar{1}\,1\,0]$ direction perpendicular to the $[1\,1\,0]$ direction along which the template is orientated. This means that a simple cross-section along the wire allows access to the maximum information about the nanowire.

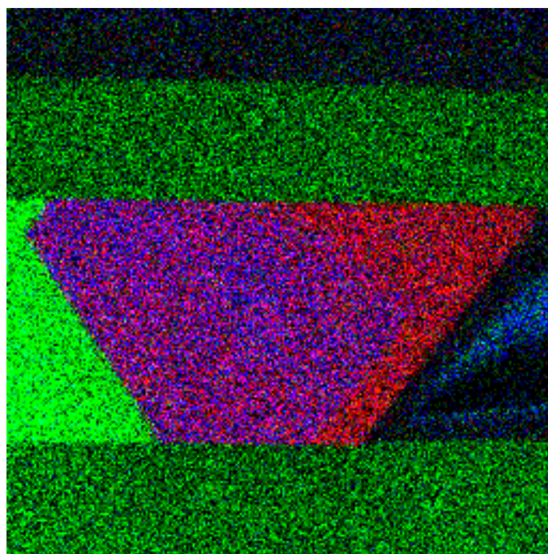
3.2.4 STEM analysis

The bottom-most wire of the array in Figure 3.3(B) was chosen for investigation. Once the FIB cut was complete, the resulting lamella was cleaned in an oxygen plasma for 30 s before being loaded in a JEOL ARM 200F scanning transmission electron microscope. Figure 3.5(A) shows an overview image of the lamella imaged with the bright field (BF) detector of the STEM. The difference in atomic number gives contrast to the image through what is known as Z-contrast: material composed of heavier atoms will appear darker in a BF image, and vice versa in an annular dark field (ADF) or high angle annular dark field (HAADF) image. Therefore, the darkest area of the sample is the InGaAs layer, as its III and V components have a high atomic number. InP appears a bit brighter given that the V group element, phosphorus, is light. The silicon and SiO_2 layers are very bright in comparison, as the small silicon and oxygen atoms allow the transmission of a higher portion of the beam. The contrast of the FIB-deposited platinum is modulated by its thickness and lower density. The red and orange lines in this figure highlight the two segments. The red line shows the limit of the InGaAs segment, with the top dashed lines signifying the presence of a facet tilted from the observation direction. The orange lines show the limit of the InP segment. The Z-contrast's compositional clues are confirmed by spectroscopic analysis in Figure 3.5(B) and Figure 3.5(C).

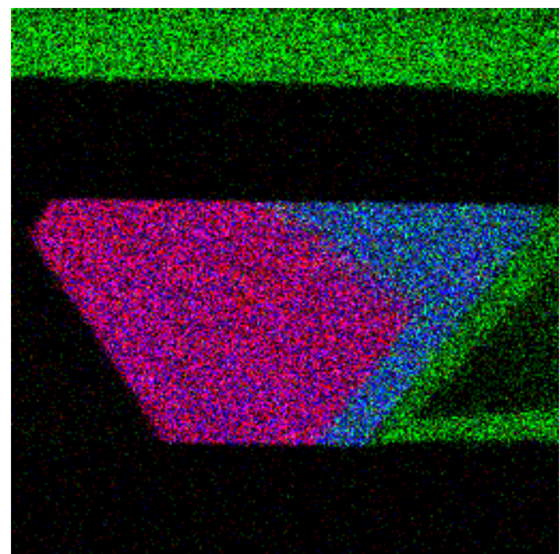
Spectroscopic analysis Figure 3.5(B) shows a low-resolution compositional map created with the energy dispersive X-Ray spectroscopy (EDS) data from the sample in Figure 3.5(A). The



(A) BF-STEM overview of a III-V nanowire cross-section.



(B) EDS map: red-In, green-Si, blue-Ga.



(C) EDS map: red-As, green-P/Pt, blue-In.

Figure 3.5: (A) overview of a III-V nanowire grown in a comb array. The wire grew from the Si seed on the left in the direction indicated by the red arrow. The red line highlights the shape of the InGaAs / InP heterointerface, and the orange line indicates the shape of the end facet of the wire. The dashed lines indicate the presence of a facet which does not contain the viewing direction in the InGaAs / InP heterointerface. The yellow square shows the position of Figure 3.6. (B) and (C) show the EDS composition maps of sample 1.

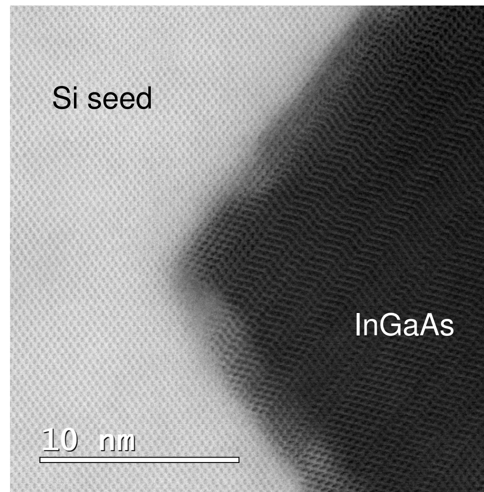


Figure 3.6: BF-STEM detail of the V-shaped Si / InGaAs interface between the seed, on the left, and the InGaAs nucleation layer, on the right.

map is colour-coded with each colour representing the intensity of an element-specific spectroscopic line processed to consider the cross-section of each transition. This creates the compositional map. Areas that appear more red have a higher indium concentration, those that appear green have a high silicon content, and those with a blue tinge contain gallium. The brightness of its colour carries information regarding the amount of each element present in each region. For example, the silicon signal is stronger in the seed area on the left of the image and fainter in the top and bottom SiO_2 template and buried oxide areas. Indium signal is present throughout the III-V area, as expected given the two InGaAs and InP layers. The gallium signal is mostly confined to the InGaAs layer, but a small blue tint can be noticed in correspondence with the outer platinum region inside the template on the right centre of the map. This is due to the FIB processing causing redeposition. Indeed, some green dots from the redeposited silicon can also be spotted in that map area. The absence of indium signal could be attributed to the tendency of this material to form droplets, as seen in Figure 3.4(A).

Another EDS map of the lamella in Figure 3.5(A) investigating the distribution of V group elements is shown in Figure 3.5(C). Here, arsenic appears in red, phosphorus in green, and indium in blue. The indium signal allows for the determination of the III-V area, as it is present in both InP and InGaAs. The arsenic signal defines the InGaAs area, and the green dots revealing the presence of phosphorus are also present in the remaining In-rich area. What appears, upon first examination, to be further phosphorus high concentration in the FIB-deposited platinum is also noticeable. However, this signal can be better explained by examining the energy at which the phosphorus K_α line is located. Indeed, the P K_α line at 2.013 keV is very close to the platinum M line, which falls at 2.048 keV. These two energies are too close for the two peaks to be distinguished when peak width and spectral resolution are taken into account, generating the "fake" phosphorus signal in the platinum layers.

Table 3.2: Growth rates for the first grown sample.

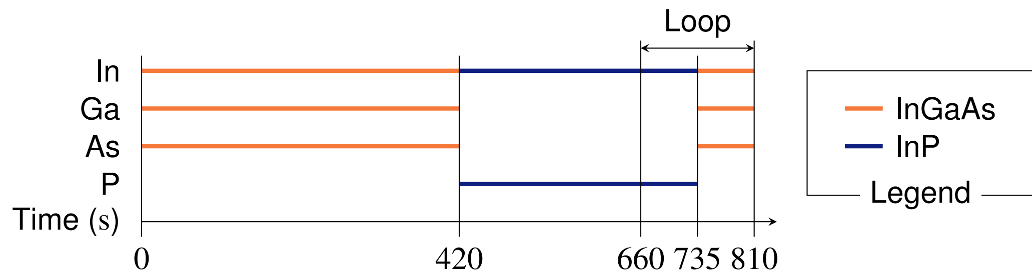
Layer	Growth rates ($nm\,min^{-1}$) $\langle 1\,1\,1 \rangle$	Longest distance	Shortest distance
InGaAs	46.5 ± 0.1	51.8 ± 0.2	20.0 ± 0.2
InP	9.1 ± 0.2	57.2 ± 0.8	9.1 ± 0.2

Heterointerfaces This sample presents three interfaces of interest: silicon/InGaAs, InGaAs/InP, and InP/empty template. Figure 3.6 shows the first interface at the "V" corner marked with a yellow square in Figure 3.5(A). Here, the epitaxial relation between the two lattices is visible. The surface of the silicon seed has some roughness, as made evident by the varying intensity of the InGaAs image in the first 6 III-As layers. Rotational twin planes parallel to the upper $\{1\,1\,1\}$ silicon facet are also visible in this high-resolution image. The shape of this first interface is defined by the TMAH etch-back before growth, but the next interface, between InGaAs and InP, is determined by the growth parameters in the reactor. Its shape is consistent with that seen in [129, 74, 54], with a lower $\{1\,1\,1\}$ facet (marked with a red full line) and an upper $\{1\,1\,0\}$ facet (traced on its expected position in a dashed red line), which is likely one of two. Interestingly, this $\{1\,1\,0\}$ facet disappears almost completely after the growth of the InP layer, leaving only a long $\{1\,1\,1\}$ facet and a smaller $\{1\,1\,0\}$ facet at the top. The $\{1\,1\,1\}$ facet is parallel to the RTPs and, therefore, the upper silicon interface. Looking back at the array of nanowires in Figure 3.3(B), the selection of which starting $\{1\,1\,1\}$ facet the end-facet is parallel to appears to be random.

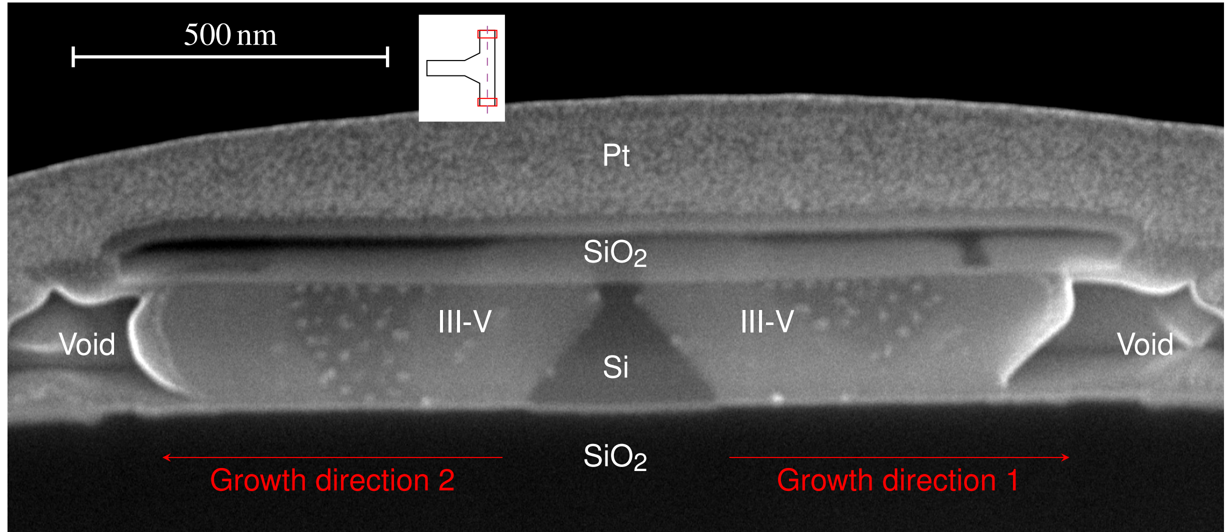
Growth rates An attempt to estimate the growth rate of InGaAs and InP can be made. However, multiple reference points can be taken to measure between them because the shape of the seed and end facet are complex. Three different measurements were made for each layer: $\langle 1\,1\,1 \rangle$, longest distance, and shortest distance; the first category means that the distance between the two parallel $\{1\,1\,1\}$ facets is measured to calculate the growth rate. For InP, the $\langle 1\,1\,1 \rangle$ and shortest distance growth rates coincide. For the $\langle 1\,1\,1 \rangle$ growth rates, the difference between InGaAs and InP is particularly high, and so is the difference between the longer distance and the $\langle 1\,1\,1 \rangle$ growth rates of InP. This suggests that the InP growth rate in the $\langle 1\,1\,0 \rangle$ direction is higher than that in the $\langle 1\,1\,1 \rangle$ direction.

3.3 Introduction of thin material layers

Regarding growth dynamics, the main finding from the sample in Figure 3.5 is the trend towards stabilisation of the $\{1\,1\,1\}$ growth front during InP growth. However, many optoelectronic devices rely on harnessing the properties of quantum confinement structures, and there is no one thin enough layer in sample 1 to constitute one. Therefore, an effort was made to introduce short



(A) Precursor sequence for sample 2 [1].



(B) SEM image of the lamella for sample 2.

Figure 3.7: Growth of the second sample. (A) is the diagram representing the modified precursor sequence introducing the looped segment for thin layer deposition [1]. Each line represents an active flow of precursor into the reactor. The colour of the horizontal lines represents the target material. (B) SEM image of the lamella during FIB thinning. The various material regions are labelled, including the Si seed, from which 2 III-V wires grew towards in opposite directions, highlighted by the red arrows underneath them. The vertical purple dashed line in the insert next to the scale bar shows where the cross-section was cut.

material deposition segments in the growth recipe and study how they modified and manifested in the final nanowire morphology and composition.

3.3.1 Growth recipe for the introduction of short material segments.

A further looped deposition segment was introduced at the end of the recipe in Figure 3.3(A) to study the growth of thin structures in the template. The resulting recipe is illustrated in Figure 3.7(A). The looped segment, executed twice without interruption, contains an InP and an InGaAs deposition step. The two short deposition steps are 75 s long. The growth temperature was kept constant at 580 °C, and the III-V ratios were unchanged from those in Table 3.1.

Figure 3.7(B) shows an SEM image of a lamella being cut from one of the T-shape devices shown in Figure 3.2(B). The image was taken during the last stage of FIB processing; two III-

V nanowires can be observed to have grown from a central silicon seed, filling the template almost entirely. The areas where the two "Void" labels are placed also mark the end of the upper template SiO_2 layer. The protective platinum layer and buried oxide layers are also visible. Lamella thinning from the back side was ongoing. As such, the farther template wall was still present. The InP regions for both wires are visible as being darker with brighter indium droplets.

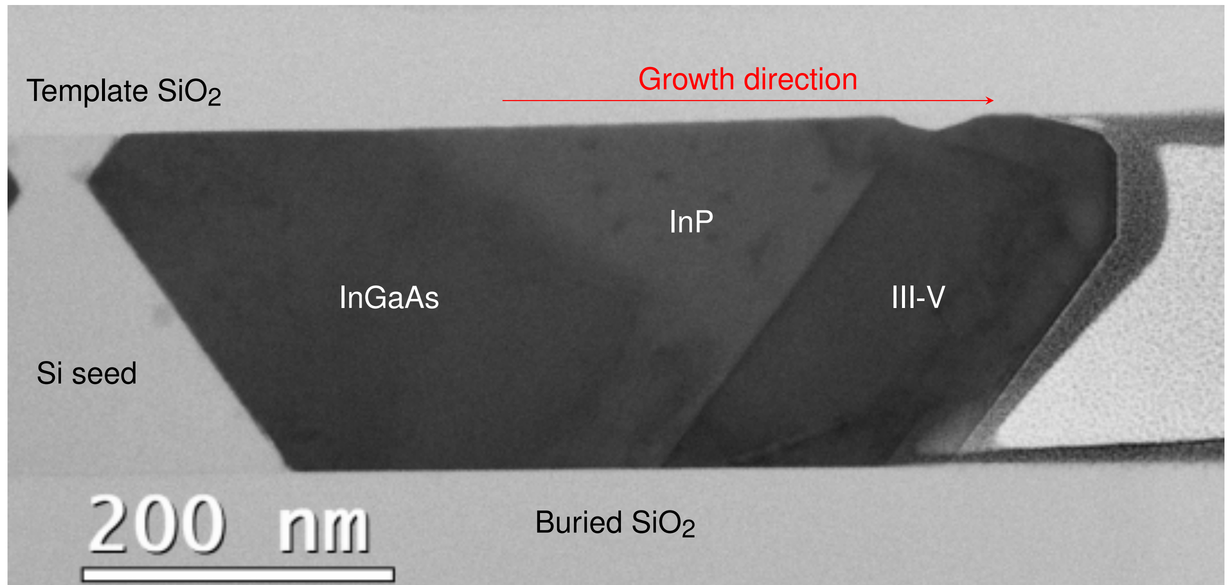
The shape of the silicon seed surfaces is very similar to those of the previous samples (Figures 3.4(A) and 3.5(A)) with the upper $\{1\,1\,1\}$ facet being the smaller of the two. This regularity in seed shape could be attributed to the fact that the templates in all three samples were opened during the same reactive ion etching (RIE) run, as they were processed simultaneously until the silicon etch back step right before growth. The two seed facets in Figure 3.7(B) formed when the TMAH etch back of the sacrificial silicon was stopped just before entering the "stem" of the T shape.

It is interesting to notice how the contrast of the III-V / upper SiO_2 layer contact interface is broken by a darker segment for the wire on the right. Even in correspondence of the void region seen in Figure 3.4(A), the interface appeared bright; this is likely due to the platinum deposited just before FIB cutting creating a contact interface. This darker region could result from a void formed during MOCVD growth inside the wire itself.

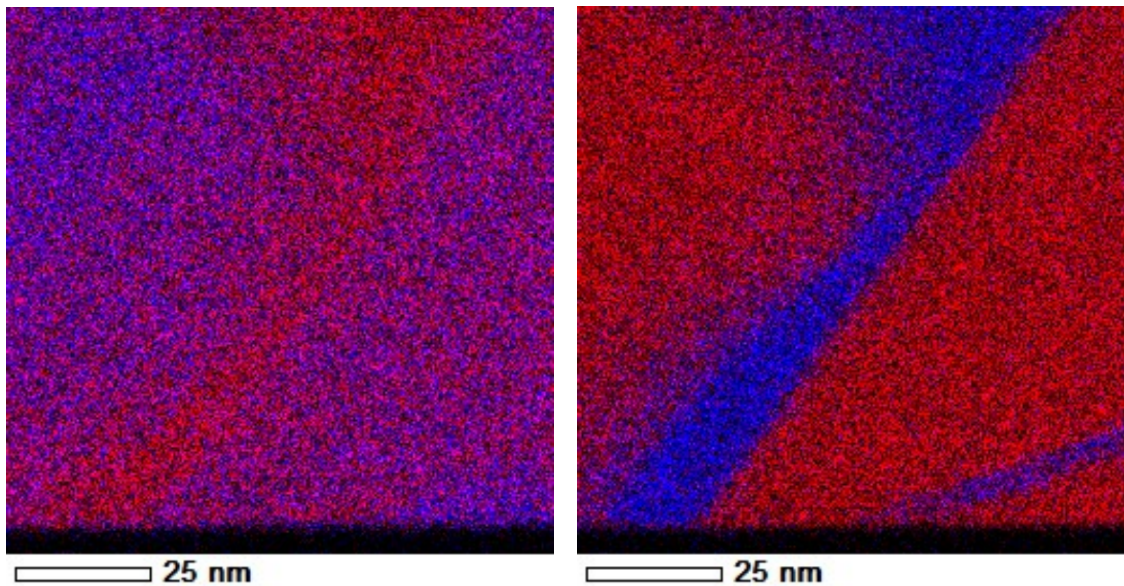
3.3.2 STEM analysis

The STEM analysis of the sample started with the recording of the overview image in Figure 3.8(A). It is a BF-STEM image showing the right wire visible in Figure 3.7(B). The silicon seed presents the previously discussed "V"-shaped interface composed of two $\{1\,1\,1\}$ facets, which are once more identifiable by the image contrast on the left side of the image. A brighter region within the dark III-V material segment coincides with the presence of InP. The evolution of the interfaces follows the trend that was highlighted in sample 1, with an initial InGaAs segment growing with a multi-faceted growth front exhibiting both $\{1\,1\,0\}$ and $\{1\,1\,1\}$ facets. The following InP layer grows quickly in the $\{1\,1\,0\}$ directions, and as such, the bottom $\{1\,1\,1\}$ facet is larger. However, in the following segment, thinner material layers can no longer be identified through channelling-driven differences in contrast.

Facet selection The presence of two top $\{1\,1\,0\}$ facets and the tendency of multiple facets of this family to form in this growth configuration is also reflected in the existing literature [49, 50, 54, 140]. The initial nucleation sees the formation of a multi-faceted InGaAs particle resting on the silicon seed surface. As it grows, both the difference in growth rates of the different facets and the template walls limit which facets establish a stable growth front. Looking at the $[1\,1\,0]$ growth axis in the cubic system, there are five energy-equivalent $\{1\,1\,0\}$ facets available, of which the first is perpendicular to the template orientation and the other four's defining vector is offset by $60°$ from the first one's. On the other hand, there are only two available $\{1\,1\,1\}$ facets at



(A) BF-STEM image of the right wire of sample 2 [1]. The growth direction is marked in red.



(B) EDS map: red-In, blue-Ga [1].

(C) EDS map: red-As, blue-P [1].

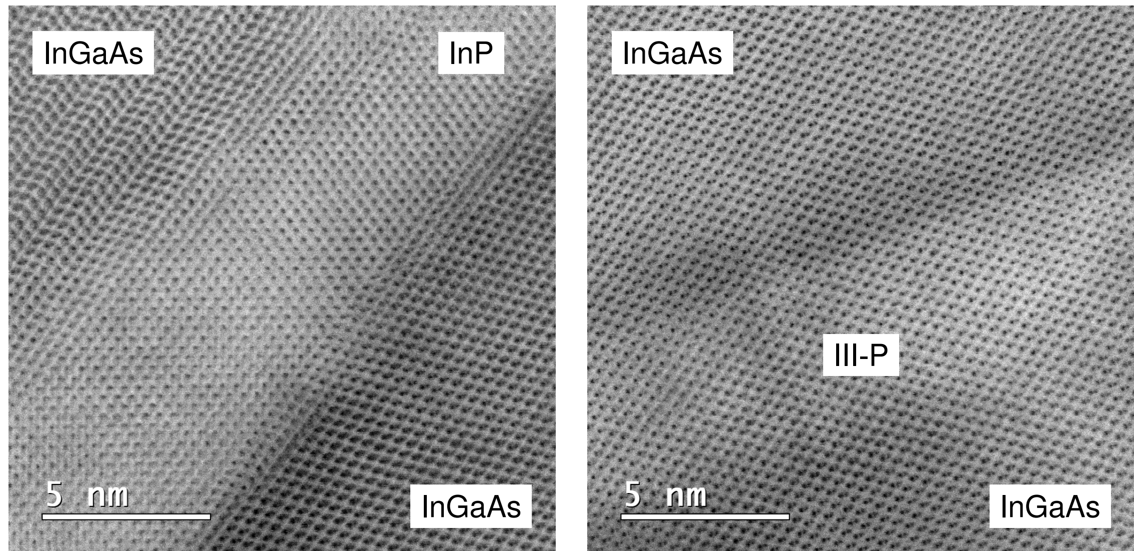
Figure 3.8: Microscopy images of the second sample. (A) shows a BF-STEM image of the lamella of sample 2, centred on the right wire. Various interfaces are visible, such as the Si/III-V interface and those between the two materials in the thick InP and InGaAs layers. Some other areas of interest are also present. (B) shows the III group element EDS map, and (C) the V group element EDS map, of the lamella shown in (A). This Figure was adapted from the work of Brugnolotto *et al.* [1] under the terms of the CC BY 4.0 licence [130].

35.3°, close to the template direction. Furthermore, in the zincblende system, the $\{1\,1\,1\}$ facets can be classified as $\{1\,1\,1\}_A$ and $\{1\,1\,1\}_B$ depending on whether only III or V atoms are exposed, respectively. The high V/III ratio loaded into the reactor during the InP deposition step selects the $\{1\,1\,1\}_B$ facet due to the marked prevalence of phosphorus in the reactor atmosphere. The same phosphorus saturation is likely to occur on the $\{1\,1\,0\}$ facets; however, the difference in the morphology of the facet means that growth is enhanced on this facet, leading to its annihilation.

An example of how the different growth rates for each facet family affect the shape of the crystal is seen in the InGaAs layer immediately after this central InP region. Here, growth appears to be relatively slow on $\{1\,1\,2\}$ facets, and a void region is created at the top of the wire. Looking at Figure 3.7(B), this information confirms the interpretation of the darker region spotted at the top of the right wire on the upper SiO_2 template wall. This allows a better understanding of the shape of this void region: its limits are mainly perpendicular to the template axis, except in the area closest to the far template wall, where it appears that the limit closest to the seed curves back.

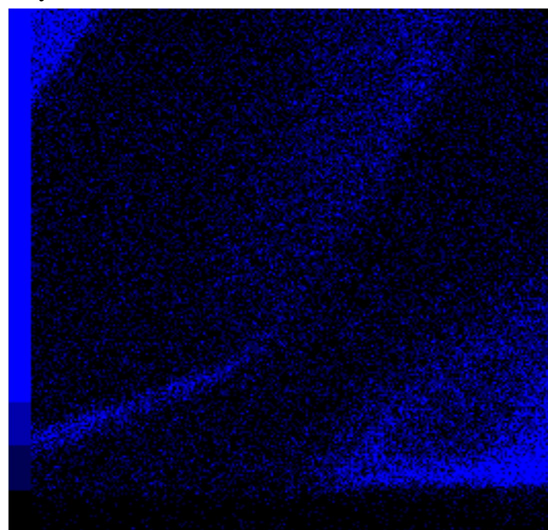
Initial spectroscopic analysis III and V group element EDS maps centred on the central InP segment are shown in Figure 3.8(B) and 3.8(C) respectively. Once again, the thick InP layer already identified through channelling contrast is immediately noticeable at the centre of the images. However, the V map in Figure 3.8(C) also shows an important clue to the location of one of the heterointerfaces in the thin layer segment at the end of the wire. A thin blue line is visible on the bottom right of this image, revealing the presence of phosphorus in this wire area. This phosphide layer originated from the 75 s long pulse in the looped segment of the recipe shown in Figure 3.7(A) and is well defined, without shading at the edges, which means that the growth front facet was perpendicular to the viewing direction. Despite this, no corresponding In-rich layer is found in Figure 3.8(B). This finding points to a difference in the relationship between precursor flow and elemental incorporation during material growth for the III and the V group elements when the growth occurs in templates.

High-resolution imaging Two high-resolution BF-STEM images of the phosphide segments identified in the spectroscopic analysis of the sample are presented in Figure 3.9(A) and 3.9(B). Figure 3.9(A) shows the layer resulting from the long InP deposition step sandwiched between two InGaAs segments. The two materials are easily distinguishable, as the III-As couples have similar sizes for both atoms. In contrast, the phosphorus atoms are much smaller and are almost invisible next to the indium atoms in the InP region. rotational twin planes are visible on the top left of the image, in the InGaAs layer. However, they are not visible after the InP layer in the next InGaAs layer. This, coupled with the presence of $\{1\,1\,2\}$ facet in the growth front, could indicate that something is affecting the growth of the wire after this point: precisely what cannot be analysed easily after the growth itself is complete. Therefore, it becomes prudent to avoid

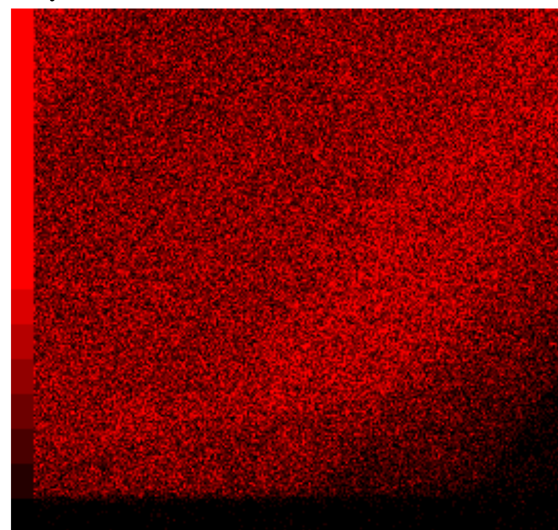


(A) High-Res BF-STEM image of the InP layer [1].

(B) High-Res BF-STEM image of the III-P layer.



(C) EDS map of the P concentration. In the bottom right, Pt signal affects this map.



(D) EDS map of the In concentration.

Figure 3.9: Analysis of the thin-layer region. (A) BF-STEM image of the lower part of the thick InP layer, where it is at its thinnest. (B) BF-STEM image of the thin phosphide interface at the bottom left of 3.8(A). (C) EDS composition map of phosphorus presence in the sample. (D) EDS composition map of indium presence in the sample. (A) and (B) were adapted from the work of Brugnolotto *et al.* [1] under the terms of the CC BY 4.0 licence [130].

drawing conclusions about the shape of the growth front morphology after this area. However, an analysis of how the III and V composition profiles interact is still possible, as this is related to the diffusion of the precursor in the template. Further, the thickness of the phosphide layer in Figure 3.9(B) is 6 nm, indicating the potential for thin heterostructures with well-defined composition gradients.

Further spectroscopic analysis The ending region of the wire was further analysed with EDS, resulting in the two images in Figure 3.9(C) and 3.9(D). They show the concentration profiles calculated from the signal intensity at the phosphorus K line and indium L line, respectively. As discussed during the analysis of the previous sample, the phosphorus K_α line is very close in energy to the platinum M line. Therefore, the high phosphorus signal visible on the bottom right of the image is interpretable as platinum presence.

This comparison aims to evaluate the growth of the InP segment based on how the indium and phosphorus concentrations line up in the sample. As is particularly evident from observing the top right corners of each EDS map, the area with high indium concentration is to the left of the one with high phosphorus concentration. This indicates a delay in III group element integration compared to the corresponding V group element integration step. This is likely due to a difference in diffusion between the two materials and will need to be solved if precise integration of thin III-V material layers is to be attempted.

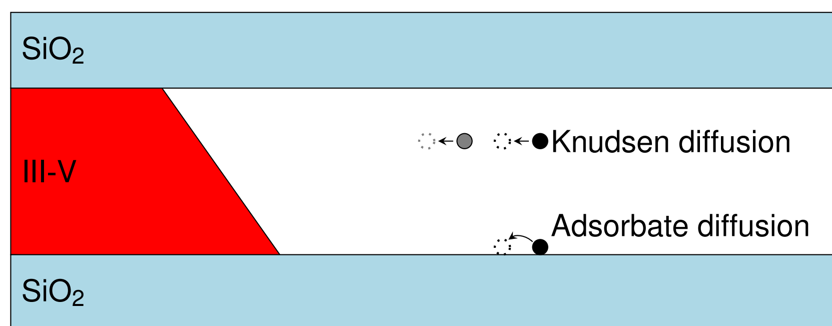
The complex layer morphology and, most importantly, the high composition intermixing between material layers make it impossible to calculate growth rates for this terminal area of the wire.

3.3.3 Correlation between growth dynamics and results

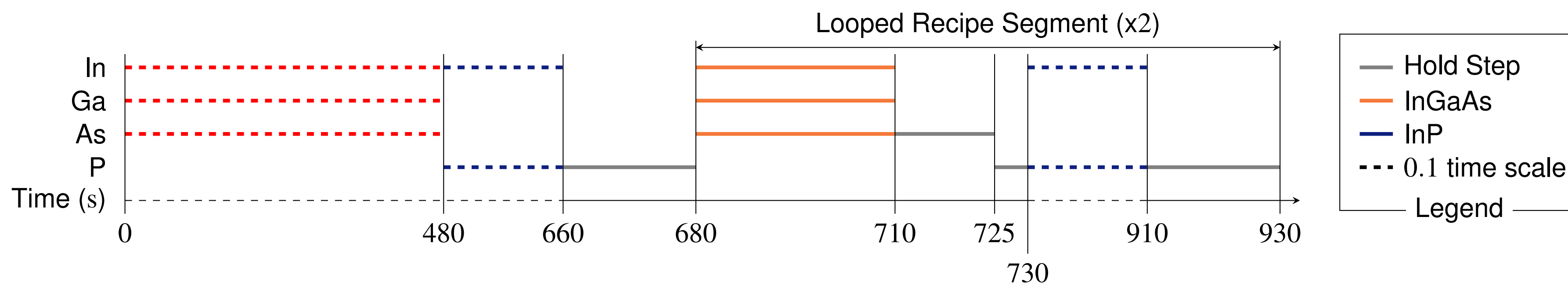
The stabilisation of the $\{1\,1\,1\}$ facet in high V/III ratio InP deposition makes this combination of material and facet the preferred one for the growth of thin heterostructures. The potential for thin heterolayers and quantum wells was highlighted by the 6 nm wide phosphide structures shown in the second sample. The thickness of the InP layer in Figure 3.9(A) can be misleading, as without the context given by the larger overview image in Figure 3.8(A), the information is lost that most of the material deposition occurs on the $\{1\,1\,0\}$ facets.

Still, both Figure 3.9(A) and Figure 3.9(B) show that for the V component of the semiconductor, it is possible to obtain <10 nm thick compositional structure. However, for the III group elements, short deposition pulses lead to heavy alloying and delay in integration. This indicates the presence of different diffusion mechanisms that affect the supply of reactant to the reaction interface (the growth front).

When the possible diffusive pathways available to the precursors are examined, it becomes clear that gas-phase diffusion is the first route available directly from the showerhead, through which precursors are introduced into the reactor. However, when the precursors land on the



(A) Diffusion mechanisms inside the SiO_2 interface. Bulk materials are labelled, with the two SiO_2 template layers above and below the III-V wire. The precursors are represented by black (III group element precursors) and grey (V group element precursors) circles. [1].



(B) Precursor sequence for sample 3 [1]. Each line represents an active flow of the corresponding precursor into the reactor. The colour of the horizontal lines represents the target material.

Figure 3.10: (A) Schematic representation of the diffusion avenues available inside the TASE template. (B) Modified MOCVD recipe based on the analysis of growth results.

wafer, the surface is non-reactive, unlike in planar growth, and the adsorbed precursors either desorb and continue diffusion through the gas phase or diffuse on the surface to reach the reaction interface. If the V precursors mainly desorb from the surfaces and primarily reach the reaction interface through gas-phase diffusion, and if the III precursors tend to diffuse as adsorbates on the surface, then this could be the diffusive mechanism difference that can explain the different sharpnesses in heterointerfaces. Additionally, if it is assumed that adsorbate diffusion is a slower mechanism than vapour phase diffusion, then this could also explain the integration delay of III group elements compared to their expected layer.

These two diffusion routes are illustrated in Figure 3.10(A). Given the small volume of the cavities, Knudsen vapour phase diffusion occurs inside the template. This diffusion regimen appears when the mean free path of the diffusing element is comparable to the size of the area within which it is diffusing. Simultaneously, the III group elements diffuse inside the template with the additional mechanism of adsorbate diffusion. This means that the III atoms can jump from equilibrium to equilibrium site on the surface of the template oxide until they reach the reaction interface. The effects of the different availability of these diffusion pathways to the various species are highlighted for short deposition pulses as the deposition time approaches the diffusion timescales [1].

3.4 Implementation of a revised switching sequence

To address the intermixing and integration delay issues identified in previous sections, several modifications were made to the MOCVD growth recipe, resulting in the revised step sequence shown in Figure 3.10(B). In this graphic, the segments drawn with dashed lines are represented with a 0.1 time scale to maintain a reasonable size for the picture. The main additions to the recipe are the "hold steps": moments at the end of each layer deposition segment when the flow of III precursors was halted, leaving only a V group element atmosphere in the background. The 5 s-long phosphorus hold step was introduced after the arsenic hold step and the InGaAs deposition step in the looped recipe segment to promote a change in the atmosphere inside the template for the following InP deposition step. The rationale for its introduction here but not in the previous arsenide-to-phosphide step is that the smaller size and weight of the phosphorus atom would give it a higher mobility and a lower chance to diffuse as an adsorbate compared to the bulkier, heavier arsenic atom.

A second modification affected the length of the material deposition segments, which was adjusted to consider the lower growth rate of InP compared with InGaAs. As the looped segment was repeated twice for the next growth run, this recipe will theoretically result in the correct barrier/well material layers alternating to create two InGaAs quantum wells in series in a InP matrix. The V/III ratios and the 580 °C growth temperature are kept constant to continue to benefit from the stabilisation of the single $\{1\,1\,1\}$ facet growth front that occurs during InP

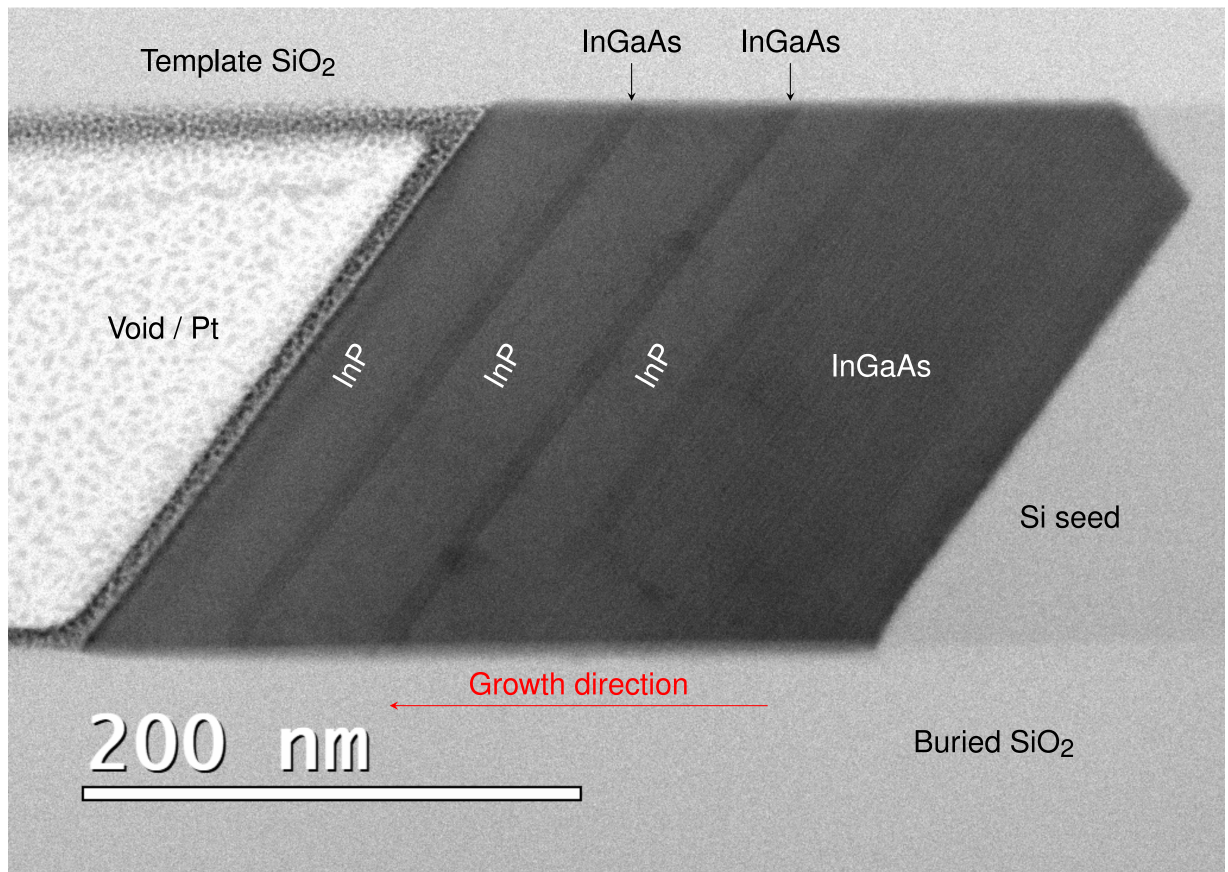


Figure 3.11: BF-STEM image of a semiconductor lamella cut from a nanowire comb array (see Figure 3.2(B)) in sample 3. The labelled material layers are already visible through channelling contrast. The wire grew from the Si seed on the right of the image, following the growth direction marked by the red arrow. An initial InGaAs nucleation layer gives way to an InP stabilisation layer followed by InGaAs quantum wells and InP barriers. This Figure was adapted from the work of Brugnolotto *et al.* [1] under the terms of the CC BY 4.0 licence [130].

deposition.

The SEM image of the sample during FIB processing for STEM analysis was already shown in Figure 3.4(A), where a hint of the finer structure is already visible by tracking the position of the indium droplets on the exposed InP lateral surfaces.

3.4.1 STEM analysis

The BF-STEM image in Figure 3.11 gives a better view of the material layers. The wire grew right-to-left from the silicon seed on the right of the image, which, once again, has the "V" shaped morphology observed in the two previous samples. Then, from right to left, the first dark area consists of an InGaAs layer, followed by a lighter InP layer and then by an alternating InGaAs and InP well-barrier quantum well structure. Compared to sample 2 (Figure 3.8(A)), here the thin heterolayers are immediately visible before EDS mapping, directly from the BF-STEM image.

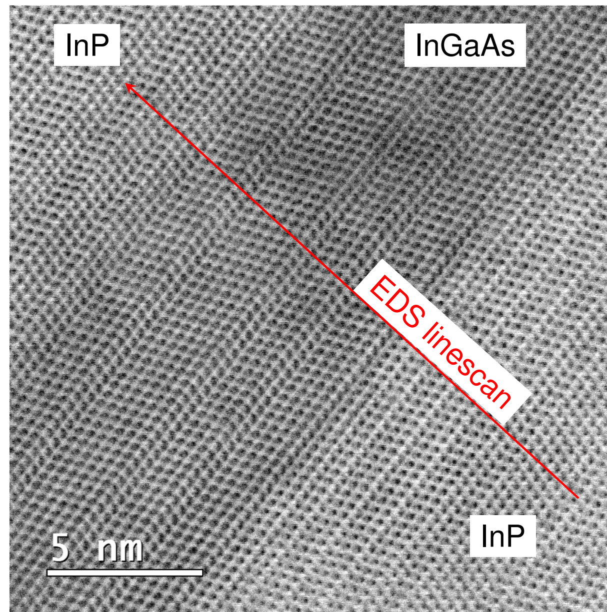
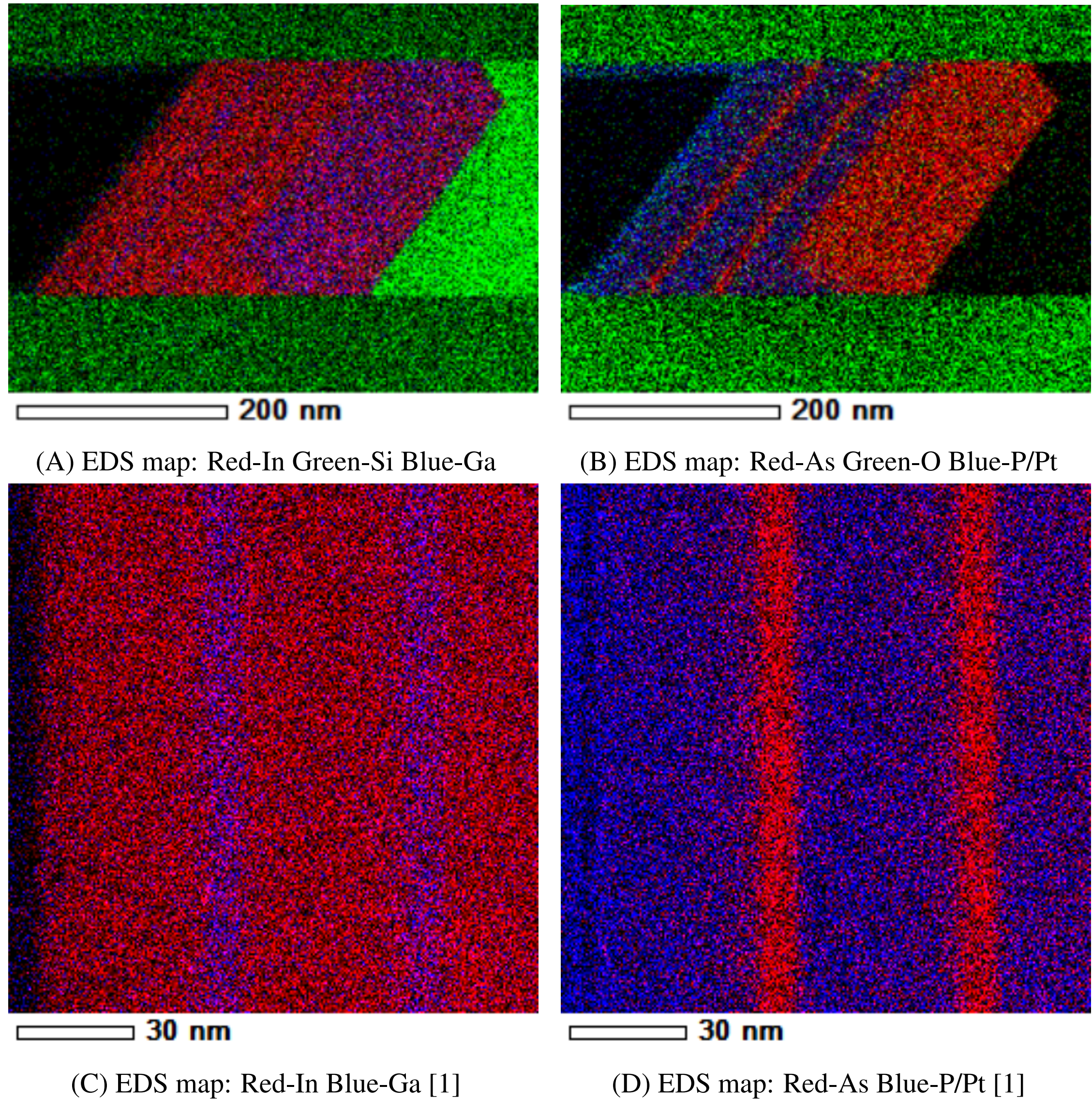


Figure 3.12: High-resolution BF-STEM image of the second quantum well region of sample 3. Material layers are labelled, and RTPs are visible throughout the image. The highlighted EDS linescan path shows the area sampled to create the composition profiles shown in Figure 3.14. This Figure was adapted from the work of Brugnolotto *et al.* [1] under the terms of the CC BY 4.0 licence [130].

Platinum is visible in the opening to the left of the III-V wire. The top and bottom of the image are occupied by the upper and lower SiO_2 template and buried oxide layers, respectively. The first InGaAs layer presents a multi-faceted growth front once again, with an upper $\{1\,1\,1\}$ facet and a $\{1\,1\,0\}$ region at the bottom. The following InP layer stabilises the $\{1\,1\,1\}$ facet up to the last few nanometres at the bottom of the wire, where a small $\{1\,1\,0\}$ facet survives, maintained through the next InGaAs layer which is, importantly, conformal to the previous InP segment when it comes to the morphology of the growth front. It is only in the second InP layer that a single $\{1\,1\,1\}$ facet is stabilised. However, it is clear that, given a sufficiently thick InP layer, growth front stabilisation will occur.

High-resolution imaging Lines parallel to the large $\{1\,1\,1\}$ seed facet are already visible in the overview image in Figure 3.11. These are the rotational twin planes already discussed in previous samples and are more easily identified in the high-resolution images in Figure 3.12, which shows the second quantum well (counting from the seed, therefore from right to left) of sample 3 (Figure 3.11). Once more, the size difference between the phosphorus and arsenic atoms creates the contrast in the image, and the arsenide layer appears darker.

Spectroscopic analysis The identification of the different material layers through channelling contrast is confirmed by the EDS maps in Figures 3.13(A) and 3.13(B), which provide spectroscopic data and composition information for the BF-STEM image in Figure 3.11. Fig-



(A) EDS map: Red-In Green-Si Blue-Ga
(B) EDS map: Red-As Green-O Blue-P/Pt
(C) EDS map: Red-In Blue-Ga [1]
(D) EDS map: Red-As Blue-P/Pt [1]

Figure 3.13: Spectroscopic information for sample 3. (A) and (B) are the III and V group element maps, with Si and O to visualise the position of the seed and template. (C) and (D) are III and V EDS maps focussing on the quantum well region of the sample. (C) and (D) were adapted from the work of Brugnolotto *et al.* [1] under the terms of the CC BY 4.0 licence [130].

ure 3.13(A), showing the indium, silicon, and gallium distribution in the sample, demonstrates how the composition gradients for the III and V components of the sample now match each other, once compared to Figure 3.13(B), which shows the distribution arsenic, oxygen, and phosphorus in the sample. This proves the efficacy of hold steps in preventing intermixing between the two III-V materials.

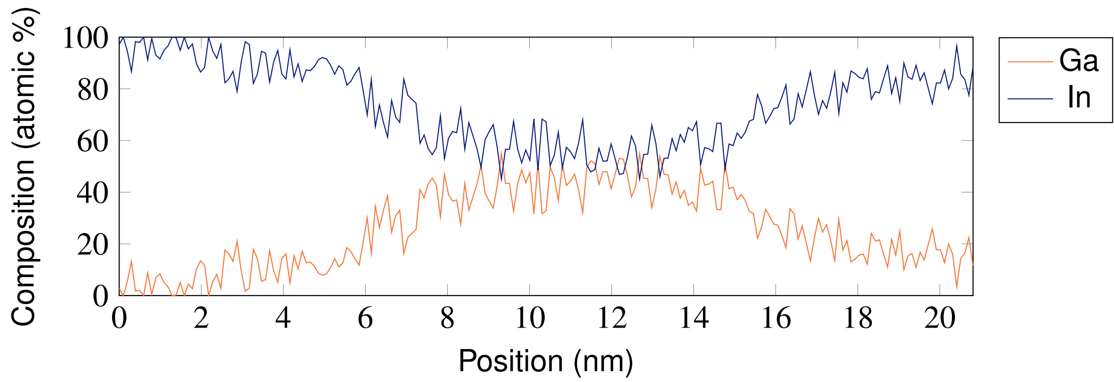
While providing a good overview of the sample composition, these two colour-coded maps lack information on the quantum wells area. Therefore, the higher resolution EDS maps in Figures 3.13(C) and 3.13(D) were recorded. The scanning angle of the STEM was changed to show the heterostructures going from top to bottom without tilt, while keeping the growth orientation from left to right. The noticeable difference in the presence of blue "phosphorus" signal on the left side of Figure 3.13(D) in an area where there is no III component in the corresponding map can be explained once again by the phosphorus K_α line being close in energy to the platinum M line.

The arsenide layers in the V map are confirmed to perfectly coincide with the Ga-rich regions. However, the V map also highlights an asymmetry in the composition of the areas immediately before and after an InGaAs quantum well, with the InP region after a well showing a higher arsenic signal than the InP region immediately before.

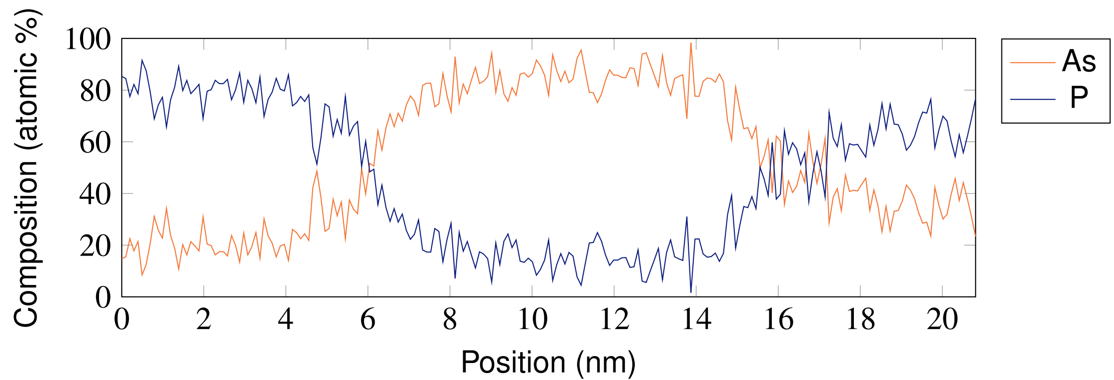
An EDS linescan was taken to quantify the composition gradient. With this methodology, the electron beam is moved point by point on a linear path instead of recording the spectra as the image is formed, as was done for the EDS maps presented so far. On each stop, a full EDS spectra is recorded; therefore, a complete compositional analysis with localised data is possible. A linescan limits the area that can be examined but, in doing so, also allows for more time to be dedicated to each measuring point, resulting in a better quantification of the sample's composition compared to the mapping method used so far.

The peak intensity of the gallium and indium L_α lines (at 1.098 keV and 3.286 keV) were elaborated by the Gatan Microscopy Suite (GMS) to extrapolate, taking into consideration the cross-section for both emission processes, the relative composition in percentage at each given survey point, resulting in the graph in Figure 3.14(A). The choice to use the L_α lines of these two materials was dictated by the lack of a calibration sample and the need to use the internal parameters of the GMS software. Therefore, it was decided that the use of the same kind of line, which results from the same electronic transition, would be likely to produce more reliable results than the use of two different lines, and, while usually the K_α lines would be the first choice, the In K_α line falls outside the spectral range of the EDS detector. Figure 3.14(B) was generated with the same methodology, but using the arsenic and phosphorus K_α line at 10.530 keV and 2.013 keV, respectively, as they are both within the detector's spectral range.

The two graphs in Figure 3.14 show that the resulting composition profiles are very noisy, revealing the limitations of EDS with 10 % noise fluctuations caused by the sum of the errors in the quantification of the atomic percentages of the two elements. Despite this, specific trends



(A) EDS linescan: III atomic percentage vs position [1].



(B) EDS linescan: V atomic percentage vs position [1].

Figure 3.14: EDS linescans for the (A) III group elements and (B) V group elements across the second quantum well of sample 3. The origin of the x-axis is situated before the well itself on the side of the Si seed, and higher position numbers (in nm) represent the scan moving along the $\{1\,1\,1\}$ vector perpendicular to the growth front away from the seed. The beam path is shown in Figure 3.12

can be observed, such as the presence of very little gallium in the area immediately before the InGaAs quantum well in Figure 3.14(A) hinting at the expected 100 % indium fraction for the InP layer. The transition area for the onset of the Ga-rich well is also around 2 nm in width, which translates to roughly 6 bi-atomic layers along the $\langle 1\,1\,1 \rangle$ direction. The InGaAs layer has a $In_{0.55}Ga_{0.45}As$ composition. Finally, in the InP layer following the InGaAs well, there is a background gallium concentration that slowly goes down to 10 % at the end of the scan region.

An analysis of the atomic percentages of V group elements in the InP barrier layers around the InGaAs well highlights a high arsenic background contamination. Indeed, even though before the well the arsenic atomic percentage is already around 20 %, right after the well and the transition area at the interface between the two materials, the lingering arsenic atomic fraction oscillates between 30 % and 40 %. In the well itself, the arsenic atomic percentage reaches 90 %. This confirms and quantifies the qualitative observation of a higher red "arsenic" concentration in Figure 3.13(D) immediately after the InGaAs wells. It is known that the second heterointerface of an InP-InGaAs-InP material stacking is not as well defined compared to the first. While this

Table 3.3: Growth rates for the third grown sample.

Layer	Growth rates (nm min^{-1}) $\langle 1\,1\,1\rangle$	Longest distance	Shortest distance
InGaAs nucleation	15.0 ± 0.2	18.3 ± 0.2	10.3 ± 0.4
InP stabilisation	9.9 ± 0.3	34.9 ± 0.8	11.7 ± 0.7
InGaAs well 1	18.5 ± 0.5	N.A.	N.A.
InP barrier 1	13.7 ± 0.2	N.A.	N.A.
InGaAs well 2	17 ± 1	N.A.	N.A.
InP barrier 2	13.9 ± 0.1	N.A.	N.A.

could be simply due to the reservoir effect caused by the template, which was to be avoided by the introduction of a short phosphorus pulse before the onset of the InP deposition step, it could also originate in decomposition mechanisms of the InGaAs known to occur in some planar deposition configurations [149]. However, if such layer degradation occurs, it is not as strong a process as observed in the literature, as the two heterointerfaces remain regular and parallel. A more detailed study of the phenomenon by changing the post-InGaAs step is required to shed light on this issue.

Growth metrics Table 3.3 shows the growth rates for the different material layers in the sample, measured the same way as for those in Table 3.2. The three ways of measuring growth rates were used for the first two layers: the InGaAs nucleation layer and the InP stabilisation layer (named after its role in stabilising a single $\{1\,1\,1\}$ facet as the growth front). As the single-facet growth front is established, the $\langle 1\,1\,1\rangle$ growth rates become the actual growth rate of the wire and, therefore, it is the only one given for the remaining four layers.

Having access to the information regarding the growth rates of each material in both a single- and multi-facet growth front allows us to analyse the effect of each growth configuration. Both the $\langle 1\,1\,1\rangle$ growth rates for the first InGaAs and InP layers are lower than those after the growth front is stabilised. While for the nucleation layer this is likely due to the need for the initial crystal to expand and fill the template, for the InP stabilisation layer this is mainly due to the rapid annihilation of the $\{1\,1\,0\}$ facet, as is made evident by the high "longest distance" growth rate, which is measured along the $\langle 1\,1\,0\rangle$ template axis at the bottom of the corresponding InP segment in Figure 3.11.

The growth rates differ significantly from those in Table 3.2 for the InGaAs layer. This could be due to the different morphology of the growth front, which has a much larger $\{1\,1\,1\}$ facet. For the InP layer, on the other hand, the growth rates remained somewhat comparable. The $\langle 1\,1\,1\rangle$ growth rate is higher, however, which could be explained by the smaller $\langle 1\,1\,0\rangle$ facet having to be filled after the InGaAs layer. This is also reflected in the lower growth rate for the $\langle 1\,1\,0\rangle$ template axis "long direction".

After the stabilisation layer, the growth rates of the two wells and those of the two barriers

are comparable and within each other's uncertainty interval.

3.5 Discussion and future developments

The main accomplishment in this chapter was the identification and exploitation of the high V/III ratio InP MOCVD growth conditions' effect on the stabilisation of the $\{1\,1\,1\}_B$ facet as the single growth front for the growing III-V nanowire. This avoids issues related to different incorporation rates of III group elements in ternary materials such as InGaAs [55] and creates compositionally uniform material layers. This is then united with the introduction of hold steps, which mitigate the effect of the adsorbate diffusion pathway, avoiding creating a reservoir effect for the III group-components, which are integrated into their design layer as expected and without delay.

The facet stabilisation method is expected to provide a solution or, at the very least, improve on all the issues identified in Figure 2.6. However, some critical problems remain. The first is related to the possibility of the stabilisation of either of 2 different $\{1\,1\,1\}$ facets. This negates the advantage gained in terms of contact positioning, as the selection of the $\{1\,1\,1\}$ facet remains a stochastic process. This is an unsolvable problem with the $[0\,0\,1]$ SOI wafer, as this substrate defines the crystalline orientation of the growing wire.

As the experiments described on this sample were being carried out, Markus F. Ritter was in the process of publishing a paper on hybrid TASE, a methodology through which part of the SiO_2 template is switched out for a superconducting material [123]. As a result of a collaboration on the STEM analysis of hybrid TASE samples, access to $[1\,1\,0]$ SOI wafers as a growth substrate was obtained for this project. This new crystalline orientation of the growth substrate means that there are in-plane $\langle 1\,1\,1 \rangle$ vectors at high angles with respect to each other, and prompted my interest in using these wafers as the substrate for the next steps of my research.

This new wafer had a silicon device layer thickness of 70 nm and a 150 nm-thick buried oxide layer, compared to the $[0\,0\,1]$ wafer employed so far for which the thicknesses were 220 nm and 2 µm, respectively. The new wafer, therefore, is less suited for optoelectronic and photonic applications but should still prove an ideal test bed for the study of MOCVD growth dynamics.

In particular, there are remaining questions on the reproducibility of the study, the yield of the growth stabilisation, the optical properties of the devices and the application of this facet stabilisation method to the integration of different III-V materials outside of the lattice-matched $In_{0.55}Ga_{0.45}As$ and InP material system [82, 83, 84] studied in this chapter.

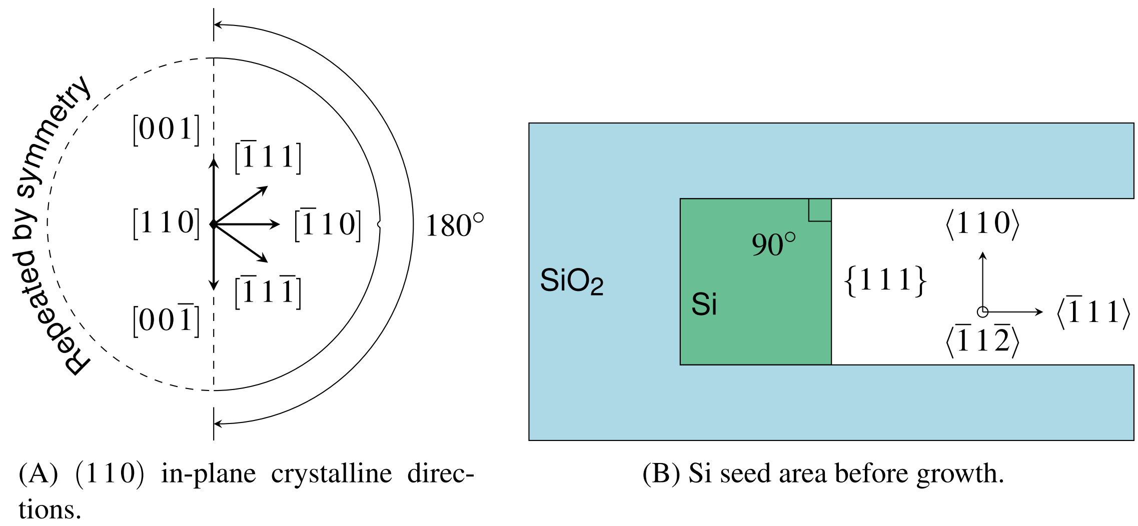
Chapter 4

Properties of TASE-grown nanowires

The critical growth mechanisms and single-facet $\{1\,1\,1\}_B$ growth front stabilisation method were explored and developed in Chapter 3. However, the lack of in-plane $\{1\,1\,1\}$ directions in the $(0\,0\,1)$ silicon on insulator (SOI) wafer on which growth was carried out complicates the analysis of growth results. The two possible $\{1\,1\,1\}$ facets are tilted and, therefore, yield calculations and device contacting become more complex. as the process through which one of the facets is selected for stabilisation is dependent on the shape and orientation of the nucleating crystal on the silicon seed.

This chapter expands on the research my coauthors and I published in [1, 2]. The first section provides an overview of the challenges related to fabrication on $\langle 1\,1\,0\rangle$ wafers and how the design of the template assisted selective epitaxy (TASE) structures and their characterization evolved from what was seen in the previous chapter. The first growth section compares the result of applying the same growth recipe developed on the $\langle 0\,0\,1\rangle$ SOI wafer to the new substrate. Further optimisation of material growth follows, and the characterisation of single-crystal TASE-grown III-V microstructure developing from multiple silicon seeds is shown.

A growth rate study linking the growth rates of indium phosphide (InP) and indium-gallium arsenide (InGaAs) to the position of each respective material layer in the template, expressed as its distance from the silicon seed, was carried out. The effects of growth in highly competitive environments on growth rates were explored. In the penultimate section, the materials investigated are expanded to indium arsenide (InAs), gallium arsenide (GaAs), and gallium antimonide (GaSb). The effect of the presence of these new and strained heterolayers on growth is explored. Finally, the impact of the introduction of tin (Sn) in dopant concentrations on the growth dynamics inside the TASE template is reported.



(A) $(1\,1\,0)$ in-plane crystalline directions.

(B) Si seed area before growth.

Figure 4.1: Crystalline orientations in the $(1\,1\,0)$ SOI wafer. (A) shows a schematic of the crystalline directions in the plane of the Si device layer, highlighting its mirror plane symmetry. (B) highlights the high-symmetry directions in the $\{1\,1\,2\}$ plane containing the chosen $\langle 1\,1\,1\rangle$ growth direction and the $[1\,1\,0]$ vector defining the wafer orientation. It highlights the vertical $\{1\,1\,1\}$ seed facet.

4.1 Fabrication on Si$(1\,1\,0)$ SOI

The fabrication of templates for nanowires and microstructures on the new $(1\,1\,0)$ substrate followed the same underlying methodology (see Section 2.4) implemented on the same tools (see Appendix A) that was used for the samples in Chapter 3. A series of lithography steps, including both electron beam lithography (EBL) and optical lithography; deposition steps, including atomic layer deposition (ALD) and plasma-enhanced chemical vapour deposition (PECVD); and etching steps, including reactive ion etching (RIE), inductively-coupled plasma (ICP) etching and tetramethylammonium hydroxide (TMAH) and hydrofluoric acid (HF) etching were employed to define the structures (seed and growth region) enclose them in the template SiO_2, open the template, and finally etch back the sacrificial silicon to expose the seed surface.

4.1.1 Template design considerations

An initial evaluation of the crystalline symmetry in the wafer plane is necessary to plan the orientation of the TASE templates on the wafer surface. Figure 4.1(A) shows the various in-plane crystalline directions in the top device layer of the $(1\,1\,0)$ SOI wafer employed in the fabrication of all future samples. Unlike its $(0\,0\,1)$ predecessor, which had a four-fold axis perpendicular to the wafer plane, this $(1\,1\,0)$ wafer has a mirror plane dictating the in-plane symmetry. Therefore, the wafer's notch becomes key to orienting the TASE structures with the desired crystalline directions.

Figure 4.1(B) shows a schematic cross-section of the TASE structure before growth with

colour-coded materials. The silicon seed presents a $\{1\,1\,1\}$ facet forming a 90° angle with all the template walls because of the TMAH etchant used to remove the sacrificial silicon; unlike the $\langle 0\,0\,1 \rangle$ wafer samples which formed 90° angles with the sidewalls (Figure 3.2(C)).

Figure 4.2 shows the evolution of the TASE structures from those in Figure 3.2. The comb structure of Figure 3.2(B) is perfect for scanning electron microscopy (SEM) analysis of multiple wires in a single image and the scanning transmission electron microscopy (STEM) survey of cross-section cuts perpendicular to the growth direction. However, cross-sections parallel to the growth direction only allow for the analysis of a single wire.

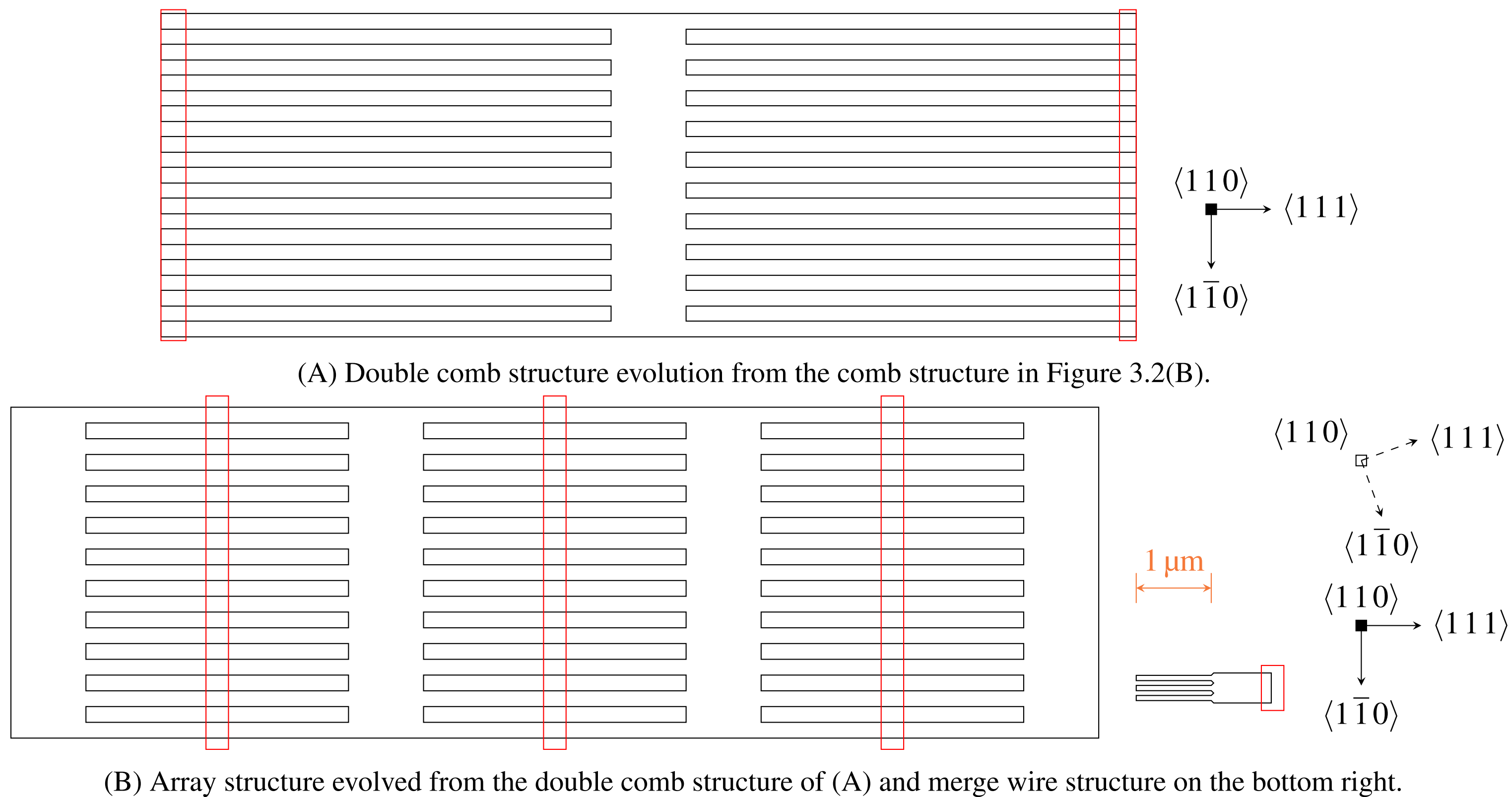
As the analysis of heterointerfaces stacked along the growth vector is the primary goal of this work, maximising the number of wires observable from seed to final interface in a single focused ion beam (FIB) cut is a key objective of the design phase. Taking inspiration from the "T-shaped" structure in Figure 3.2(B) the first evolution of the comb array is shown in Figure 4.2(A). A central rectangular silicon backbone anchors two rows of nanowires that extend from either side, with the templates being open at the very edges of the structure (in red in Figure 4.2(A)). The length of the nanowire growth area extends up to 7 µm for this design. These long channels (in relation to their 70 nm height) were designed to study the effect of growth in "deep" templates on resulting composition and growth rates. Unfortunately, in practice, the resulting structure could only be used with short etch-back segments. This was due to the thickness of the side walls in the final samples, which was insufficient to ensure structural integrity during TMAH etch-back, despite the selectivity of this etchant.

The difficulties encountered with the design in Figure 4.2(A) together with the possibility of having more STEM-observable nanowires per FIB cut led to the design of the array structure in Figure 4.2(B). This allows for the STEM analysis of 6 short nanowires up to 2 µm-long while keeping the overall length of the structure at 14.5 µm, and therefore comparable to that of the double-comb design (13 µm). There are 4 equidistant rectangular backbone anchors, with two marking the beginning and end of the structure. The templates are open between the anchors in three areas of the structures (in red in Figure 4.2(B)). Thus, once complete, one such array contains 66 growth sites.

Wire widths of 70 nm, 140 nm, 210 nm, and 280 nm were fabricated, the Figures 4.2(A) and 4.2(B) show the 210 nm designs.

To the bottom right of the array in Figure 4.2(B) there is a "merge wire" structure. In this structure, three nucleation wires with a design width of 70 nm all terminate in a single channel 400 nm wide. This structure was designed to study the merging regions between the three growing crystals to observe the defects that could form from the merging of two growing crystals. In the past, it was employed to demonstrate the introduction of dislocations in TASE microstructures [139].

Both structures in Figure 4.2(B) were grown aligned to the in-plane $\langle 1\,1\,1 \rangle$ direction but also 20° misaligned. In practice, this was done by aligning one set of structures to an in-plane $\langle 1\,1\,1 \rangle$



(A) Double comb structure evolution from the comb structure in Figure 3.2(B).

(B) Array structure evolved from the double comb structure of (A) and merge wire structure on the bottom right.

Figure 4.2: Microstructure designs for TASE growth. The structures transferred to the Si device layer are represented in black and the template opening regions in red. (A) shows the double comb structures grown on the first $[1\,1\,0]$ samples. These were always oriented to have the template axis coincide with the in-plane $\langle 1\,1\,1 \rangle$ directions. (B) shows the nanowire array structures used in later experiments on the $[1\,1\,0]$ SOIs and the "merge wire" structures. These types of structures were grown both aligned with the in-plane $[1\,1\,1]$ direction, as highlighted by the solid-line arrows, and 20° misaligned, as shown by the dashed arrows [2].

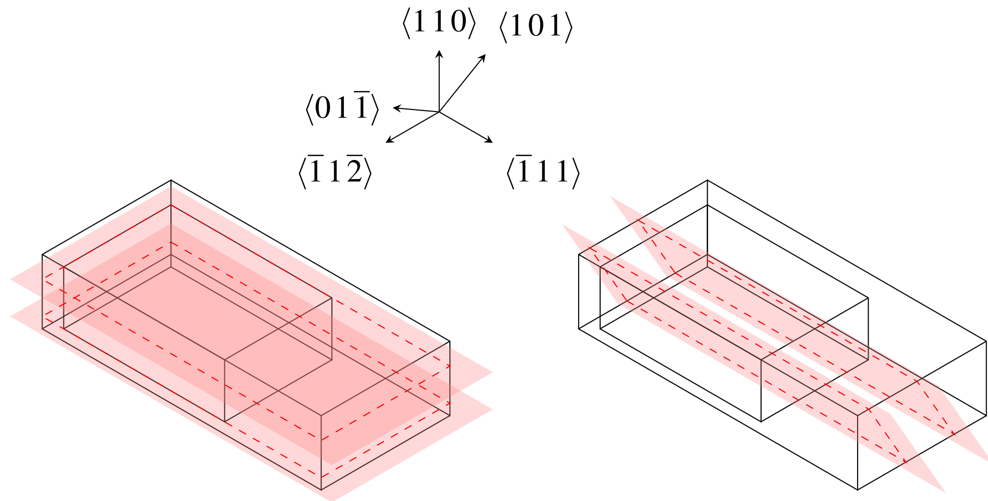


Figure 4.3: FIB cutting strategies to expose $\{110\}$ facets from a $[110]$-oriented substrate. The red-shaded planes show how the cut planes are selected to expose the sides of the wire in correspondence to $\{110\}$ facets if the template axis coincides with a $\langle 111\rangle$ direction. On the left is a plane-view cut and on the right a 30° cut.

direction and rotating each subsequent set by 90°. Selecting this specific 20° misalignment as a basis for analysis therefore has two advantages:

1. the resulting seed surfaces and projected growth fronts are at a significant angle with the template sidewalls
2. there is no need to keep track of the direction of the notch past the dicing stage which resulted in the initial 6 cm × 6 cm die.

4.1.2 FIB lamella fabrication

While a new $\langle 110\rangle$ wafer and $\langle 111\rangle$ template orientation were used for fabrication, the preference for an exposed $\{110\}$ facet for structural analysis with STEM remains unaltered due to this facet allowing easy recognition of a wide variety of crystalline defects [148]. However, the first difficulty is that, as highlighted in Figure 4.1(B), the in-plane crystalline direction perpendicular to the $\langle 111\rangle$ template axis is a $\langle 112\rangle$, making the simple cross-section cut used in the previous chapter (Figure 3.4(B)) unsuitable.

The most obvious $\langle 110\rangle$ direction perpendicular to the $\langle 111\rangle$ template axis is the one that defines the wafer orientation itself. As shown on the left of Figure 4.3, a plane-view cut would satisfy orientation requirements and allow for precise energy dispersive X-Ray spectroscopy (EDS) composition maps and an excellent overview of the evolution of the growth front. However, such a cut is much more complex and time-consuming than a cross-sectional cut. The amount of lamella that must be thinned to sub 100 nm thickness to ensure electron transparency increases from a few hundred nanometres to 1.5 µm in this configuration. A challenging target

to meet with the ion beam of the FIB that requires a high level of precision. This is particularly true when milling both sides of a target region composed of multiple material layers eroded at different rates.

A compromise can be found by cutting the sample with a 30° tilt in the stage resulting in the cutting planes drawn on the nanowire on the right in Figure 4.3. Referring to the direction legend in Figure 4.3, these expose the $(1\,0\,1)$ facet, part of the family of $\{1\,1\,0\}$ facets which all share the same symmetry in the zincblende phase (space group 216) [142, 143, 144, 145]. This "30° cut" allows an analysis of the evolution of the growth front comparable to the simple cross-section cut used in the previous chapter (Figure 3.4(B)). Still, tilt means that any material layers not perpendicular to the growth front will appear distorted, and, similarly, horizontal and tilted heterointerfaces will be shaded in EDS analysis. Therefore, a limited use of the regular 90° cross section was kept at the beginning for the experiments with the $\langle 1\,1\,0\rangle$ wafer.

4.2 Application of the growth recipe on the new substrate

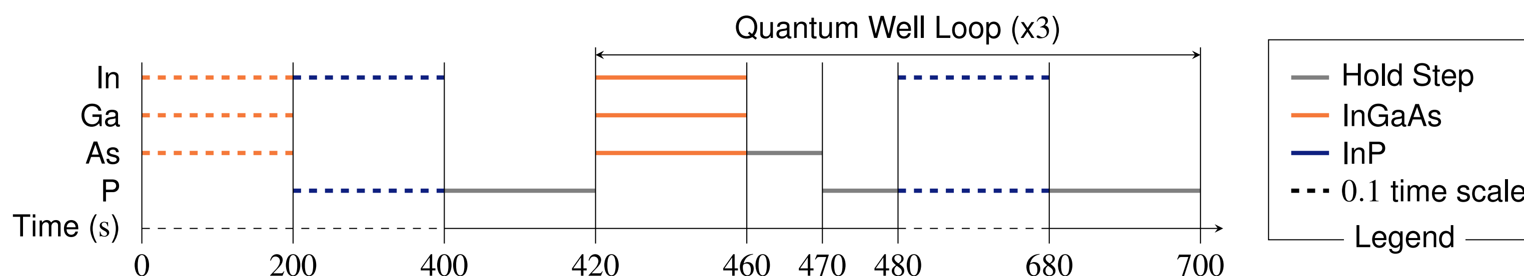
The recipe in Figure 4.4(A) was kept similar to that used in sample 3 (Figure 3.10(B)) for the initial experiment on the new $\langle 1\,1\,0\rangle$ substrate. It contains a looped segment for creating InGaAs quantum wells between InP barrier layers. The main adjustments concern the deposition times. The initial growth steps, were changed from 480 s and 180 s to 200 s for both InGaAs and InP, respectively. The deposition times for InGaAs quantum wells were lowered from 30 s to 20 s in anticipation of the smaller area of the growth front. Simultaneously, the duration of InP barrier steps was increased from 180 s to 200 s.

The most significant change concerned the post-InGaAs hold step. Here, As precursor flow step time was reduced from 15 s to 10 s and the following P precursor flow step time increased from 5 s to 10 s. This change was made to address the As profile seen in the InP layer of the sample 3 (Figure 3.14(B)). By reducing the As precursor flow time in the hold step it was hoped that the As contamination in the first nanometres of the InP layer would be reduced or, in the best case, eliminated in sample 4.

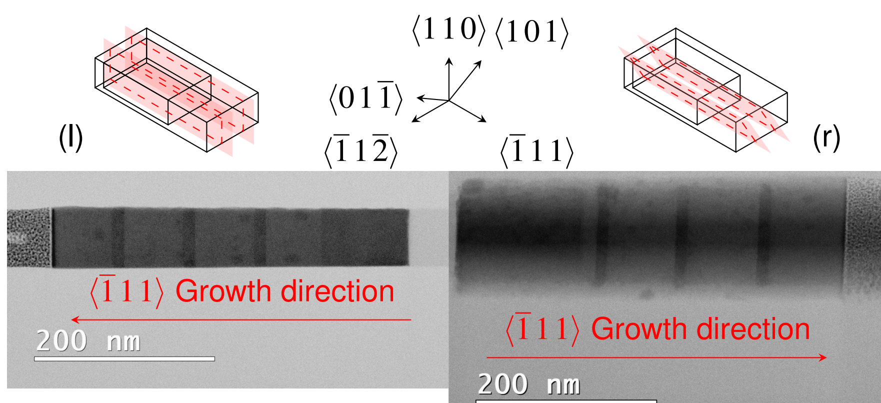
4.2.1 Structural analysis

Figure 4.4 shows BF-STEM images of two different wires from sample 4. The images on the left side of both Figure 4.4(B) and 4.4(C) show the wire cut with a standard cross-section used in the previous chapter and schematised in Figure 3.4(B). In comparison, on the right side of the same figures, the images of a lamella cut with the 30° cross-section illustrated on the right of Figure 4.3 are shown.

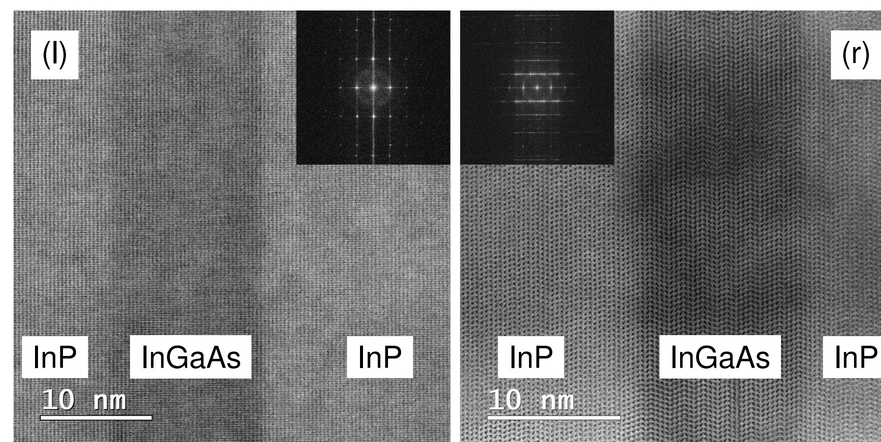
Both lamellae come from the same sample, with identical device layer thickness. However, Figure 4.4(B) highlights how the 30° cross-section appears larger because the viewing angle is



(A) Precursor sequence for sample 4 [1]. Each line represents an active flow of the corresponding precursor into the reactor. The colour of the horizontal lines represents the target material. The dashed lines are time-compressed 10 times. The quantum well growth loop was executed three times.



(B) BF-STEM overview images of two nanowires from sample 4. The wire on the left was cut with a regular cross-section, while the wire on the right was cut with a 30° cross-section, as shown by the 3D drawings. The direction guide only refers to the drawings.



(C) High-resolution BF-STEM images of the first quantum well for both wires in (B) with FFT inserts. Further FFT analysis is shown in Figure 4.5.

Figure 4.4: Precursor sequence and BF-STEM images of sample 4. The III-V material appears dark due to channelling contrast, with InGaAs being the darkest of the two III-V materials. (A) shows the precursor sequence. (B) shows overview images of the normal cross-section and 30° cross-section. (C) shows high-resolution images of the first quantum well for both wires in (B) with inserts showing the calculated FFTs. (B)(l) and (C)(l) were adapted from the work of Brugnolotto *et al.* [1] under the terms of the CC BY 4.0 licence [130].

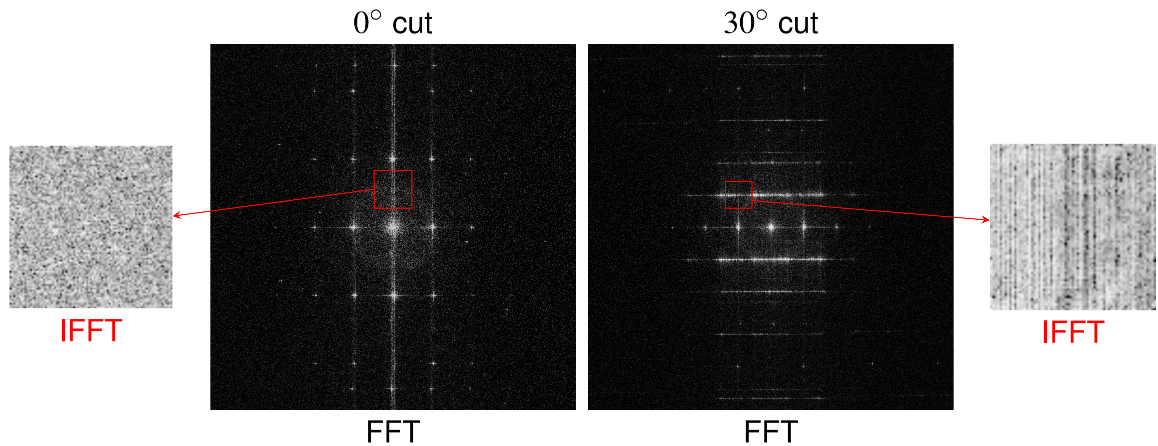


Figure 4.5: Detail of the FFTs of sample 4 seen in Figure 4.4(C) with inverse transforms. The two FFTs for the 0° and 30° cuts are at the centre of the image, with red squares showing the areas that were sampled for the inverse transforms. The inverse transforms are labelled IFFT and are located at the two sides of the FFTs. Arrows connect the sampled areas to the corresponding IFFTs.

not perpendicular to the heterointerfaces that lay in the wafer plane. This distortion becomes clear when one looks at the III-V / Si interfaces at the top and bottom of the nanowires. The well-defined lines in the standard cross-section become large regions in the 30° cross-section. In these regions, the III-V nanowire and the SiO_2 template appear superimposed, as they are one on top of the other in the path the electron beam takes through the lamella.

An evident advantage of the 30° cut in combination with the $\langle 1\,1\,0 \rangle$ wafer is that vertical $\{1\,1\,1\}$ heterointerfaces remain perpendicular to the viewing direction. As the recipe optimised in Chapter 3 stabilises this facet family, this new viewing angle does not affect the observer's ability to evaluate the sharpness of this type of interface from STEM measurements.

The comparison between the two wires at high resolution in Figure 4.4(C) also highlights the amount of structural information available when viewing a $\{1\,1\,0\}$ plane (on the right) compared to a $\{1\,1\,2\}$ plane (on the left). The presence of rotational twin planes (RTPs) is evident in the 30° cross-section both in the BF-STEM image and in its fast Fourier transform (FFT) in the insert. The RTPs have manifested as horizontal lines in the frequency domain. In contrast, both the $\{1\,1\,2\}$ BF-STEM image and its fast Fourier transform (FFT) do not contain any trace of this type of defect. This can be easily confirmed by carrying out an inverse FFT of a small portion of the initial FFT. Figure 4.5 shows the result of this operation for the vertical line in the FFT of the 0° cross-section on the left, and of the horizontal lines in the 30° cross-section on the right. It's clear to see that, while the former only contains intensity information, the latter shows the position of (at least some of) the RTPs in the original BF-STEM image.

Both wires grew from silicon seeds that in Figure 4.4(B) appear towards the centre of the image and grew out toward the margins. The initial InGaAs nucleation layer gives way to a lighter InP layer in both lamellae, however, the length of this layer appears different. This could

Table 4.1: Growth rates for each heterolayer in the two nanowires in Figure 4.4

material layer	growth rates (nm min^{-1}) 0° cross-section	30° cross-section
InGaAs nucleation	29.0 ± 0.2	42.4 ± 0.3
InP stabilisation	18.3 ± 0.1	4.7 ± 0.2
pre-wells layers	**23.7 ± 0.1**	**23.6 ± 0.3**
InGaAs well 1	39 ± 1	35 ± 2
InP barrier 1	19.7 ± 0.2	22.4 ± 0.1
InGaAs well 2	41 ± 1	38 ± 1
InP barrier 2	19.7 ± 0.2	23.6 ± 0.1
InGaAs well 3	43 ± 1	39.1 ± 0.9
InP barrier 3	20.0 ± 0.2	25.0 ± 0.1
wire total	**22.5 ± 0.2**	**24.4 ± 0.2**

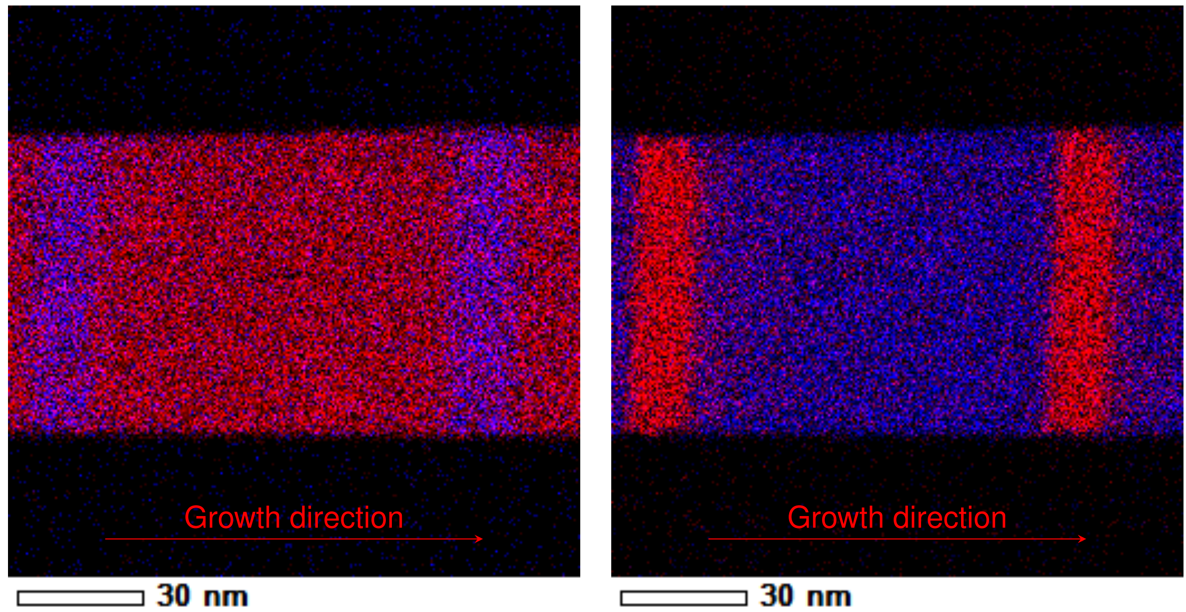
be due to a different shape of the InGaAs nucleus' growth front. A trace of the complexity of this interface is seen at the bottom of the first well of the 30° cross-section. The bottom of this heterostructure appears bent towards the seed, suggesting that the InP layer did not have enough time to grow to annihilate all the non-$\{1\,1\,1\}$ facets.

Growth rates The growth rates for each material layer in the wires of Figure 4.4 are summarised in Table 4.1. These values were calculated by taking seven repeated measurements of each layer thickness perpendicularly to each heterointerface and are therefore comparable to the $\{1\,1\,1\}$ growth rates of sample 3 (Table 3.3).

The discrepancy between the size of the InGaAs and InP pre-well layers noted in the BF-STEM images of the two wires from sample 4 is also reflected in their growth rates. The InGaAs growth rate for the nanowire observed with a 30° cross-section is (42.4 ± 0.3) nm min^{-1}: significantly higher than that of its counterpart in the nanowire observed under the standard cross-section which stands at (29.0 ± 0.2) nm min^{-1}. The InP growth rates, however, have an opposite trend, resulting at (4.7 ± 0.2) nm min^{-1} and (18.3 ± 0.1) nm min^{-1}, respectively.

Consequently, when examining the total growth rate of the nanowires before the first quantum well the two values are within each other's error at (23.6 ± 0.3) nm min^{-1} and (23.7 ± 0.1) nm min^{-1}, respectively. Since the amount of material introduced in the reactor was the same for both wires, this would support the theory that a complex growth front forms in one of the two wires and then is simplified to a single $\{1\,1\,1\}$ facet by the InP layer. In this scenario InP and InGaAs layers could be one behind the other in the path of the electron beam. Another option is that the "missing" InP could have been removed during the FIB thinning of the lamella. During this process, part of the nanowire's material is removed; therefore, the III-V semiconductor film seen in the STEM image is only a portion of the entire wire.

Both the InGaAs well and InP growth rates increase as the growth front approaches the opening of the template. This trend is not very pronounced for the InP layers of the nanowire



(A) III-element EDS map. Red In, blue Ga

(B) V-element EDS map. Red As, blue P

Figure 4.6: EDS maps of the quantum well region of the 0° cross-section in Figure 4.4(B). The seed is out of frame on the left of the images. This Figure was adapted from the work of Brugnolotto *et al.* [1] under the terms of the CC BY 4.0 licence [130].

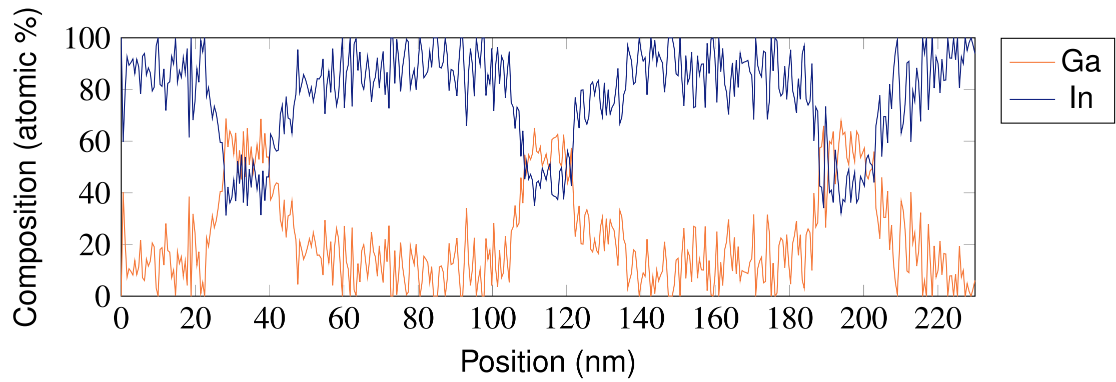
cut with the standard cross-section procedure but is more pronounced in the 30° cross-section sample. This results in a higher total growth rate for the latter nanowire, with nearly 2 nm min^{-1} of difference. This difference, which develops in the latter precursor-switching-rich part of the recipe when the growth front is nearer to the template opening, could indicate a limited competition between neighbouring nanowires or a precursor concentration gradient in the reactor in the moments immediately following the precursor switches.

4.2.2 Compositional analysis

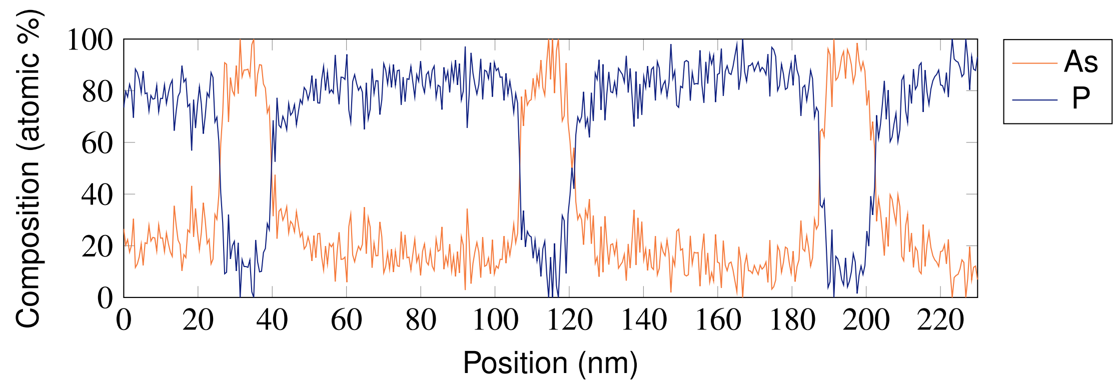
Figure 4.6 shows the EDS maps. The elements gallium and phosphorus are colour-coded in blue while indium and arsenic are colour-coded in red. Two InGaAs quantum wells are visible on both maps, showing the same nanowire area.

The III group element map shows how gallium is well-segregated into the InGaAs layers. However, a difference between the leading and trailing edges of the quantum wells is visible once more when examining the V group element map. Indeed, while the leading edge is sharp, a light red shading is present in the phosphorus region after the trailing edge. This indicates an arsenic contamination in the InP barrier layer. As the image is comparable to the one in Figure 3.13(D), the lengthening of the phosphorus flow step during the post InGaAs hold step had little impact on the resulting post-well composition profile.

Figure 4.7 shows the composition data calculated from the EDS linescan taken on the quantum well region of the 0° sample in Figure 4.4(B). The scan was taken from before the first quantum



(A) EDS linescan: III atomic percentage vs position.



(B) EDS linescan: V atomic percentage vs position.

Figure 4.7: EDS linescan compositional data (in percentage) for the (A) III group elements and (B) V group elements across all three quantum wells of the 0° sample seen in Figure 4.4(B). The origin of the x-axis is situated before the first well and is the closest point to the Si seed. Higher position numbers (in nm) represent the scan moving along the $\{1\,1\,1\}$ vector perpendicular to the growth front away from the seed.

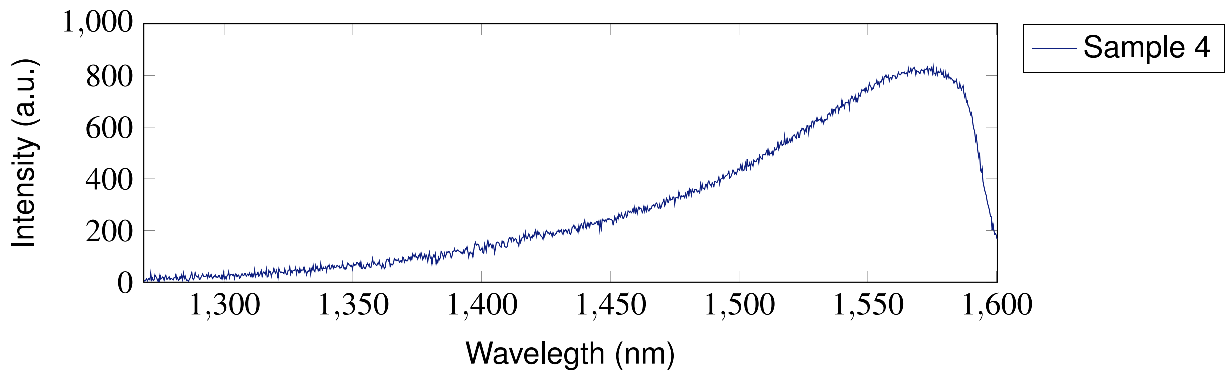


Figure 4.8: Photoluminescence spectrum of a nanowire from sample 4. The effect of the detector cut-off on the emission profile makes the individuation of the peak impossible. This spectrum was kindly recorded by Markus Scherrer.

well, closest to the silicon seed.

The III group element composition profile of Figure 4.7(A) was calculated using the L_α lines of indium and gallium. The graph is very noisy, with noise fluctuations reaching 20 %, but shows a composition close to $In_{0.4}Ga_{0.6}As$ in all three quantum wells. Similarly to the profile in Figure 3.14(A), it suggests the presence of a gallium composition gradient after the well itself.

The V group element composition profile of Figure 4.7(B) was calculated using the K_α lines of arsenic and phosphorus. This graph has noise fluctuations of about 10-15 %. An arsenic percentage composition close to 100 % is present in the InGaAs quantum well similarly to what was observed for sample 3 (Figure 3.14(B)). The As-rich region extends for 10-15 nm after the end of the InGaAs quantum well.

As the precursor flows were not altered from those of previous samples, the V / III ratios remain as in Table 3.1. The higher concentration of gallium in the quantum wells could therefore be caused by the change in the geometry of the template given by the difference in device layer thickness of the $\langle 1\,1\,0 \rangle$ SOI wafer.

4.2.3 Photoluminescence analysis

The photoluminescence spectrum in Figure 4.8 was recorded from one of the nanowires in sample 4. The operator selected a nanowire far from parasitic growths. The nanowire was excited with a 1 s-long laser pulse with a wavelength of 1000 nm while cooled to −200 K. This wavelength was selected as it is higher than the absorption wavelength of InP (920 nm [150]) but lower than that of $In_{0.53}Ga_{0.47}As$ (1650 nm [151]) to selectively excite the latter material.

As the focus size of a wave is limited by both the diffraction limit and the real (therefore imperfect) optics of the setup, the illumination spot used to excite the nanowire is larger than 500 nm and can be approximated at an order of magnitude of 1 μm [85]. As such, the spot size is much larger than that of even just one of the nanowires, let alone that of the single heterolayers.

One of the nanowires at the edge of one of the double comb structures shown in Figure 4.2(A) was chosen for measurement to minimise the influence of neighbouring wires as much as possible. The resulting spectrum of Figure 4.8 shows a wide emission range, with an emission profile extending over the detector cutoff. As the detector used to register the emission spectra is also based on InGaAs, the exact position of the peak cannot be clearly determined. However, as the emission appears to be broad, it is unlikely to be originating from the quantum wells.

The reason for this wide spectrum could lie in the large InGaAs nucleation layer, which still constitutes the bulk of InGaAs in the nanowire and grows before the facet stabilisation process mediated by the following InP layer. As such, it becomes important to minimise the length of this nucleation layer as much as possible if the photoluminescence spectrum of the InGaAs heterostructures is to be recorded.

4.3 Minimisation of nucleation layer thickness

After examining the photoluminescence results of sample 4 (Figure 4.8) the recipe was adjusted to minimise the effect of the InGaAs nucleation layer. Previous experience in the research group at IBM Research Europe - Zurich has shown that this layer, grown with a target composition of $In_{0.53}Ga_{0.47}As$, has a positive effect on the nucleation yield of III-Vs on silicon. However, once nucleation is achieved, it does not serve a further purpose in the experiments described in this chapter.

Given its possible negative impact on the photoluminescence analysis of the samples, a new metal-organic chemical vapor deposition (MOCVD) recipe was created, shown in Figure 4.9(A). The step time for the nucleation InGaAs layer was reduced to 30 s. The deposition time of the InP stabilisation layer was increased to 450 s to keep the InGaAs quantum wells far from the nucleation layer. This was also meant to ensure the stabilisation of the single-facet $\{1\,1\,1\}$ growth front, to avoid situations such as the one seen in the 30° cross-section of sample 4 (Figure 4.4(B)), where the first quantum well followed a multi-faceted growth front.

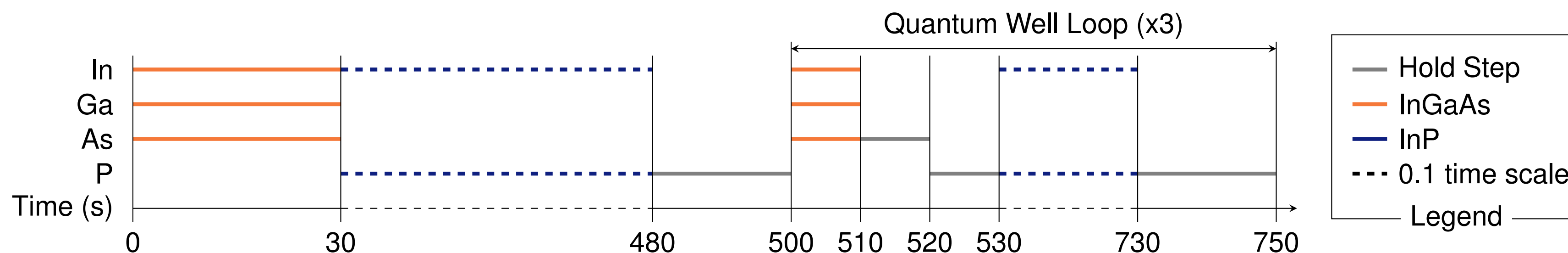
Part of one of the nanowire arrays designed in Figure 4.2(B) was imaged at a 52° angle with SEM. The resulting image is shown in Figure 4.9(B). The various elements of the TASE structures are visible. Various silicon seeds are anchored to each rectangular silicon backbone. The III-V semiconductor nanowires appear as the brighter segments after the seeds. The empty templates follow the III-V material, ending in the opening of the template visible in the centre of the image created by the inductively-coupled plasma (ICP) etching.

Already in Figure 4.9(B), the low competitiveness of the growth process is qualitatively inferable, as the length of the nanowires in the middle of the array is not noticeably different from that of the nanowires at the edges.

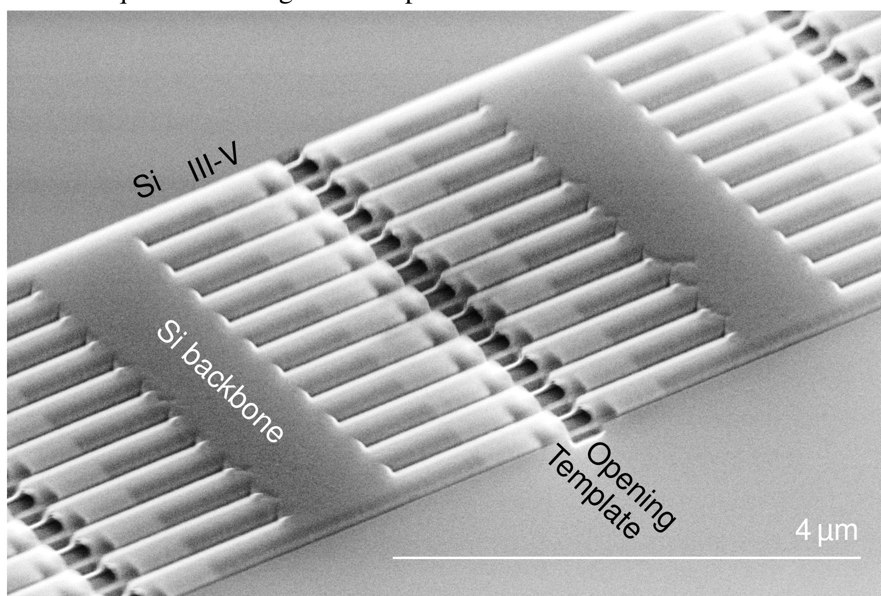
Figure 4.9(C) shows a BF-STEM image of a nanowire from sample 5. The silicon seed is on the left of the image. The variable thickness of the lamella, manifested by the decreasing height (from left to right) of the top platinum layer, leftover from FIB sample preparation, contributes to a progressive darkening of the InP stabilisation layer towards the seed. Furthermore, the absence of a hold step after the nucleation layer makes the heterointerface between the arsenide and phosphide layer more "blurred". These factors make the now thin InGaAs layer not immediately identifiable by channelling contrast, unlike in Figure 4.4(B).

All visible heterointerfaces, including the final facet of the nanowire exposed to the protective platinum on the right of the image, appear sharp in this image. The heterointerfaces also give the reader a snapshot of the growth front, which is composed of a single $\{1\,1\,1\}$ facet after the InP stabilisation layer.

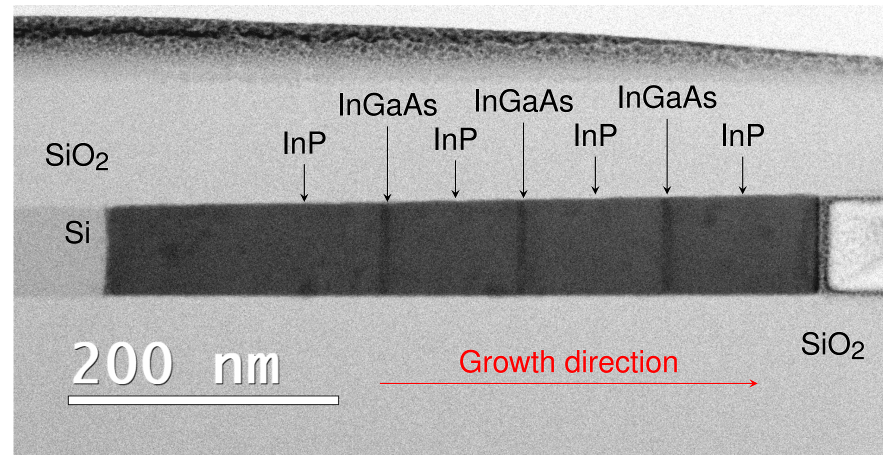
Growth rate The growth rate calculation methodology remains unchanged for this sample and consists of taking the average of 7 repeated measurements of layer thickness perpendicularly to each subsequent heterointerface. The error expresses the 95 % confidence interval around the



(A) Precursor sequence for sample 5 and for merge structures [2]. Each line represents an active flow of the corresponding precursor into the reactor. The colour of the horizontal lines represents the target material. The dashed lines are time-compressed 10 times. The quantum well growth loop was executed three times.



(B) SEM image of nanowire array made with the design in Figure 4.2(B).



(C) BF-STEM overview image of a nanowire from sample 5. The Si seed is on the left and the growth direction is highlited in red.

Figure 4.9: MOCVD recipe and growth results for sample 5. (A) shows the MOCVD precursor sequence. (B) shows an SEM image of an array of nanowires. The image was recorded with the stage tilted 52°. An in-plane $\langle 1\,1\,0 \rangle$ direction runs parallel to the bottom margin of the image. (C) shows a BF-STEM overview images of a nanowires. The Si seed is on the left of the III-V nanowire.

Table 4.2: Growth rates for the superlattice region of sample 5.

	InGaAs			InP		
material layer	well 1	well 2	well 3	barrier 1	barrier 2	barrier 3
growth rates (nm min^{-1})	43 ± 3	39 ± 2	44 ± 4	28.0 ± 0.2	30.2 ± 0.1	32.7 ± 0.2

growth rate value and it is assumed that the deposition time is error-free.

Table 4.2 summarises the growth rates for each material layer in the InGaAs-InP quantum well structure. The InGaAs growth rates remain similar to those calculated for sample 4, despite the halving of the InGaAs deposition time. On the contrary, InP growth rate is higher by between 7 nm min^{-1} and 10 nm min^{-1}, despite the fact that the InP deposition step time was not altered from the recipe used for sample 4 (Figure 4.4(A)).

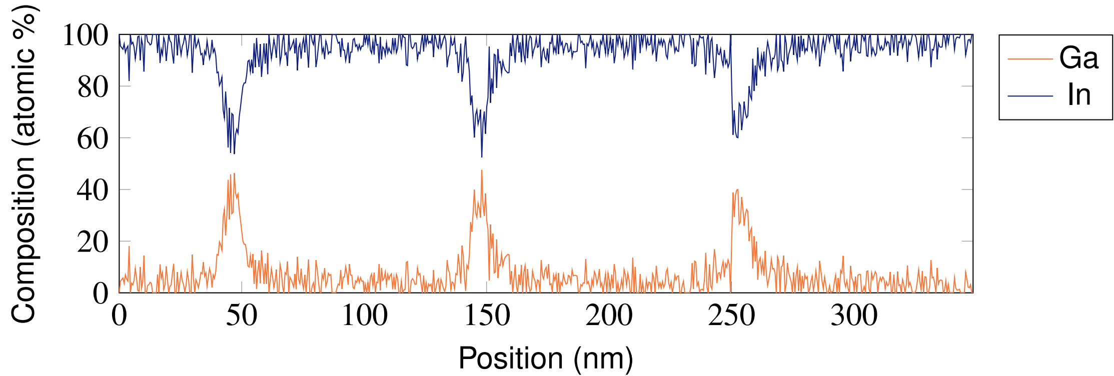
This discrepancy in growth rate evolution for the InP and InGaAs layers could indicate a small dependency of the growth rate on deposition time. This may be due to the time required to exchange the precursor molar fractions in the template becoming less and less negligible as the step time lowers.

EDS analysis An EDS linescan measurement was carried out across the InP-InGaAs quantum well region. After elaboration with the Gatan Microscopy Suite (GMS), the two composition profiles, one for III group elements, and the other for V group elements, are reported in Figure 4.10. The linescan was recorded starting from before the first quantum well and moved across the superlattice towards the end of the wire, stopping after the third quantum well.

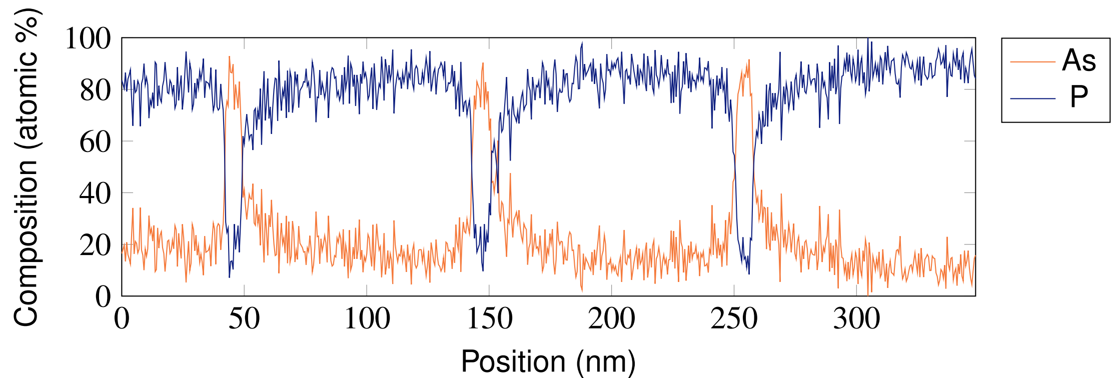
Figure 4.10(A) shows a graph of the concentration, in atomic percentage, of gallium and indium, calculated from the relative intensity of their respective L_α lines and their EDS cross-section. Unlike previous samples, the gallium contamination following the InGaAs quantum well is absent in the starting portion of the InP well. The lower overall concentration of gallium in the quantum well could, however, simply make a trailing gallium contamination too small to be noticeable above the 10 % noise level that affects the concentration measurement. The composition of the quantum well can be estimated at approximately $In_{0.4}Ga_{0.6}As$.

The atomic percentage concentrations of arsenic and phosphorus in Figure 4.10(B) were calculated from their respective K_α lines. The noise level is around 20 %. The presence of a post-InGaAs arsenic contamination in the InP barrier layer remains distinguishable from background noise. This is particularly evident when looking at the steepness of the arsenic peaks at each arsenide-phosphide interface. The leading interface is almost vertical while the trailing interface curves down more gently.

These repeated observations (Figures 3.14, 4.7, and 4.10) point to an InGaAs to InP heterointerface definition limitation inherent to the stacking of the material layers. Although the changes in the hold step following the InGaAs layer did not contribute to the interface definition, they did solve the III group element integration delay issue, as the arsenic and gallium profile



(A) EDS linescan: III atomic percentage vs position.



(B) EDS linescan: V atomic percentage vs position.

Figure 4.10: EDS compositional data for the (A) III group elements and (B) V group elements across all three quantum well of the sample seen in Figure 4.9(C). The origin of the x-axis is located before the first well on the side of the Si seed. As the position (in nm) grows along the x-axis, the beam moves along the $\langle 1\,1\,1 \rangle$ vector away from the seed.

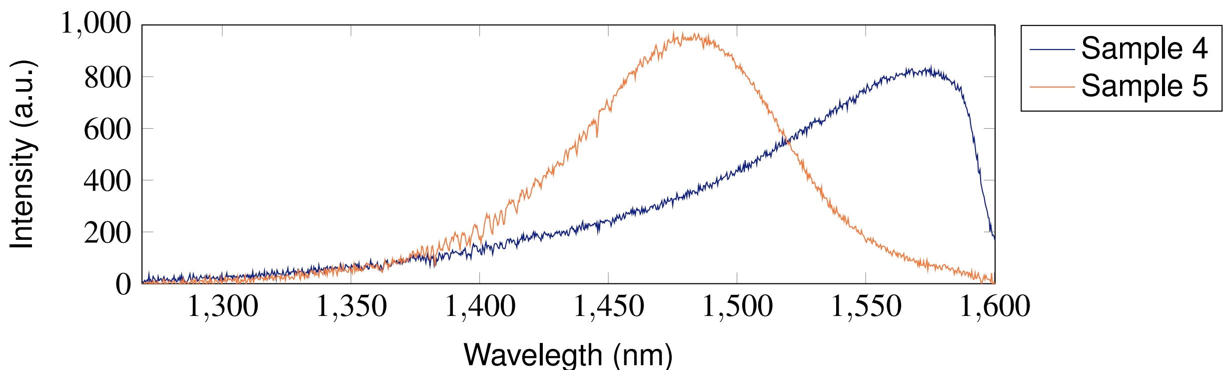
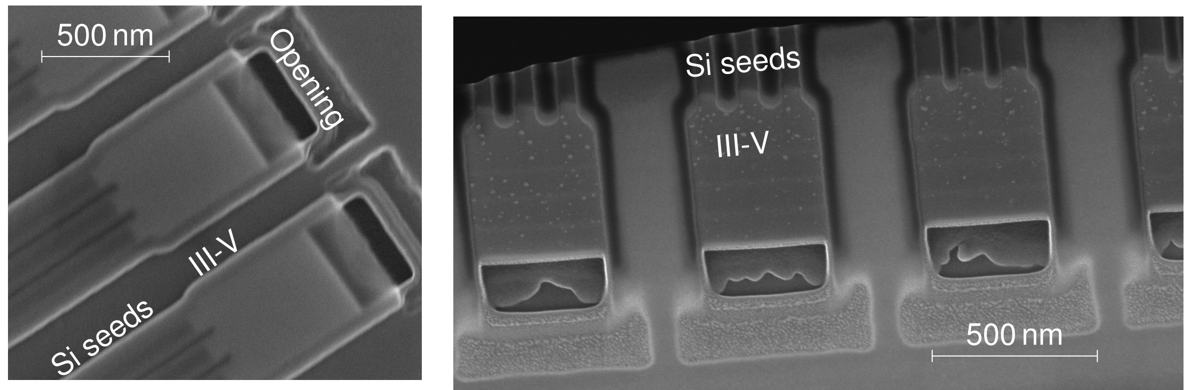


Figure 4.11: Photoluminescence spectra of two nanowires from samples 4 and 5. The emission profile of sample 5 appears narrower with a peak at lower wavelength compared to that of sample 4 These spectra were kindly recorded by Markus Scherrer.



(A) SEM image of merge structures before lamella cut-off.

(B) SEM image of a lamella containing merge structures during FIB plane-view thinning.

Figure 4.12: SEM image of merge structures taken (A) before and (B) during FIB lamella cut-out and thinning. The three Si seeds seen on the bottom left of (A) appear at the top of (B), which gives a point of view from below the wafer surface now that the lamella has been thinned and the buried SiO_2 sputtered away.

remain reliably synced in multiple growth runs.

Photoluminescence analysis Figure 4.11 compares a photoluminescence spectrum recorded for sample 5 with that recorded for sample 4 and shown in Figure 4.8. The measurement conditions were left largely unchanged. The main alterations affected the sample temperature, which was ∼100 K instead of ∼200 K, and the excitation wavelength, set at 1060 nm instead of 1000 nm. Therefore, despite the small change in wavelength, the material targeted for analysis remained InGaAs.

The emission peak of the quantum wells is found at a wavelength lower than that of the peak of sample 4. This could be due to the higher indium concentration seen in Figure 4.10(A), however, as the peak is much narrower for this sample, a quantum well effect could be present. Unfortunately, due to the noise level of the EDS composition profiles, it is difficult to solely attribute the spectral changes to either of these changes.

4.3.1 Merge structures

In addition to the nanowire arrays (Figure 4.9(B)), sample 5 contained the multi-seed structures shown in Figure 4.12.

This structure design was already used in the past at IBM Research Europe - Zurich. Indeed, Figure 3.1 showed the characterisation of a III-V TASE structure grown from 5 independent silicon seeds. This type of structure was patented with the claim of achieving spacially controlled introduction of dislocations in semiconductors [139]. I decided to include these structures on one of my samples to test the growth methodology developed in the previous sections in a challenging template geometry. Improvements in dislocation introduction reliability during growth

with the facet stabilisation method could have opened more research avenues in their exploitations in devices. On the other hand, absence of defects in this growth regimen would set the basis for the creation of large III-V platelets similar to those seen in lateral aspect ratio trapping (LART) [57, 52] with greatly reduced dislocation and grain boundary density.

These multi-seed structures were processed (template opening, sacrificial silicon etch-back, and MOCVD growth) at the same time as the arrays seen in the previous section. In these multi-seed structures, three seed regions are provided for III-V nucleation. The template design then forces the three growing crystals into a larger template area where they can come into contact with each other and merge. This type of structure is expected to introduce defects at the merging locations, even in the case of simultaneous nucleation on all three seeds [139].

Various avenues of stress relaxation in epitaxially grown III-V crystals induce alterations in their lattice, making the merging of two different crystals a prime defect-nucleating event [152]. The nucleation of defects is common even in situations where lattice rotations follow the symmetry rules of the crystals [153]. If a small (1° to 5°) tilt of the III-V crystalline axis from the $\langle 1\,1\,1 \rangle$ axis occurs to relax stress, as will be seen in sample 6 (Figure 4.16(B)) it is expected to lead to a similar defect-nucleating situation. In contrast, under optimised growth conditions, the merging of two different crystals can result in defect-free material [154], leading to improvements in the crystalline quality of large-area III-V semiconductor films [155].

Figure 4.12(A) shows the merge structures as they appear after MOCVD growth. In this top-down SEM image, the templates are orientated along an in-plane $\langle 1\,1\,1 \rangle$ direction and present a single $\{1\,1\,1\}$ end facet. The III-V material can be seen filling the areas corresponding to the three seeds without any noticeable voids.

The SEM image in Figure 4.12(B) shows the same structures already seen in Figure 4.12(A), this time in the final phases of FIB processing. The lamella was cut using the "plane view" technique (Figure 4.3 left) to access multiple structures simultaneously on a $\langle 1\,1\,0 \rangle$ viewing axis at the STEM. Three lighter lines are already visible in each structure with SEM at this magnification level likely corresponding to the InGaAs layers.

In Figure 4.13, each structure's three silicon seeds appear at the top of the lamella. The (comparatively) electron transparent SiO_2 template outlines each of the five III-V structures. The FIB thinning partially damaged the leftmost structure, as too much material was removed from the seed area at the top left most of the lamella. The varying thickness of the lamella can be inferred by the darkness of the platinum layer between the III-V structure. Despite the best efforts made during FIB lamella preparation, the lamella is slightly thicker towards the bottom of the image, but this does not affect the quality of the image in the structure area, at this magnification level.

The first three structures have 50 nm wide seed areas, while the two on the right have 70 nm wide seeds. This small structural difference does not result in any appreciable change in the final III-V crystals, which all follow the template shape. The three lines corresponding to the

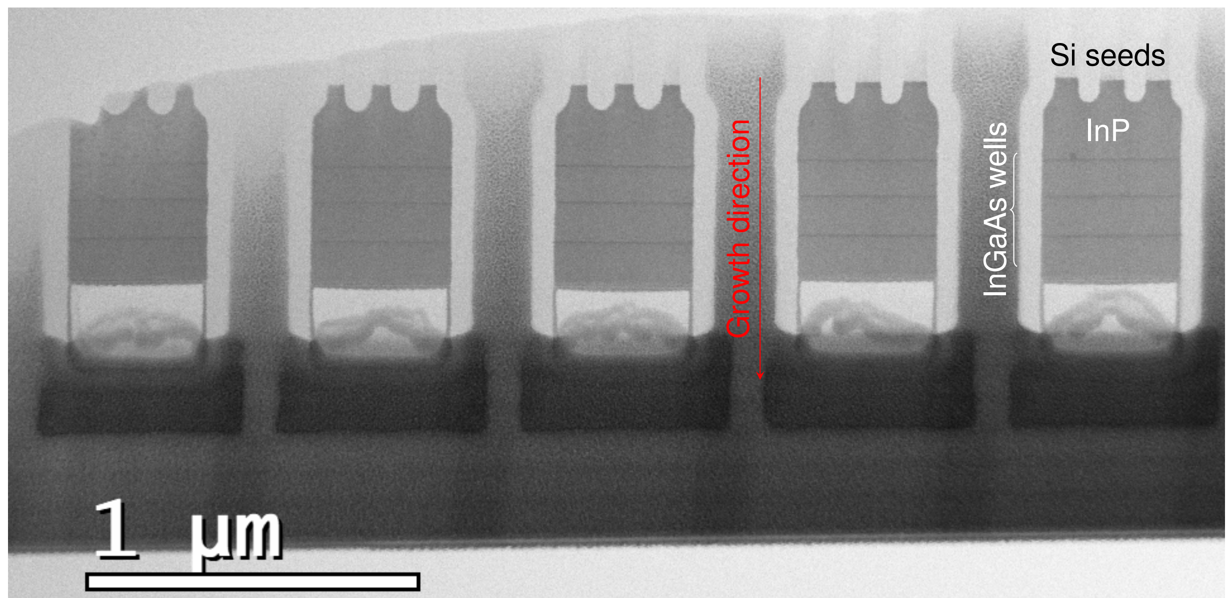


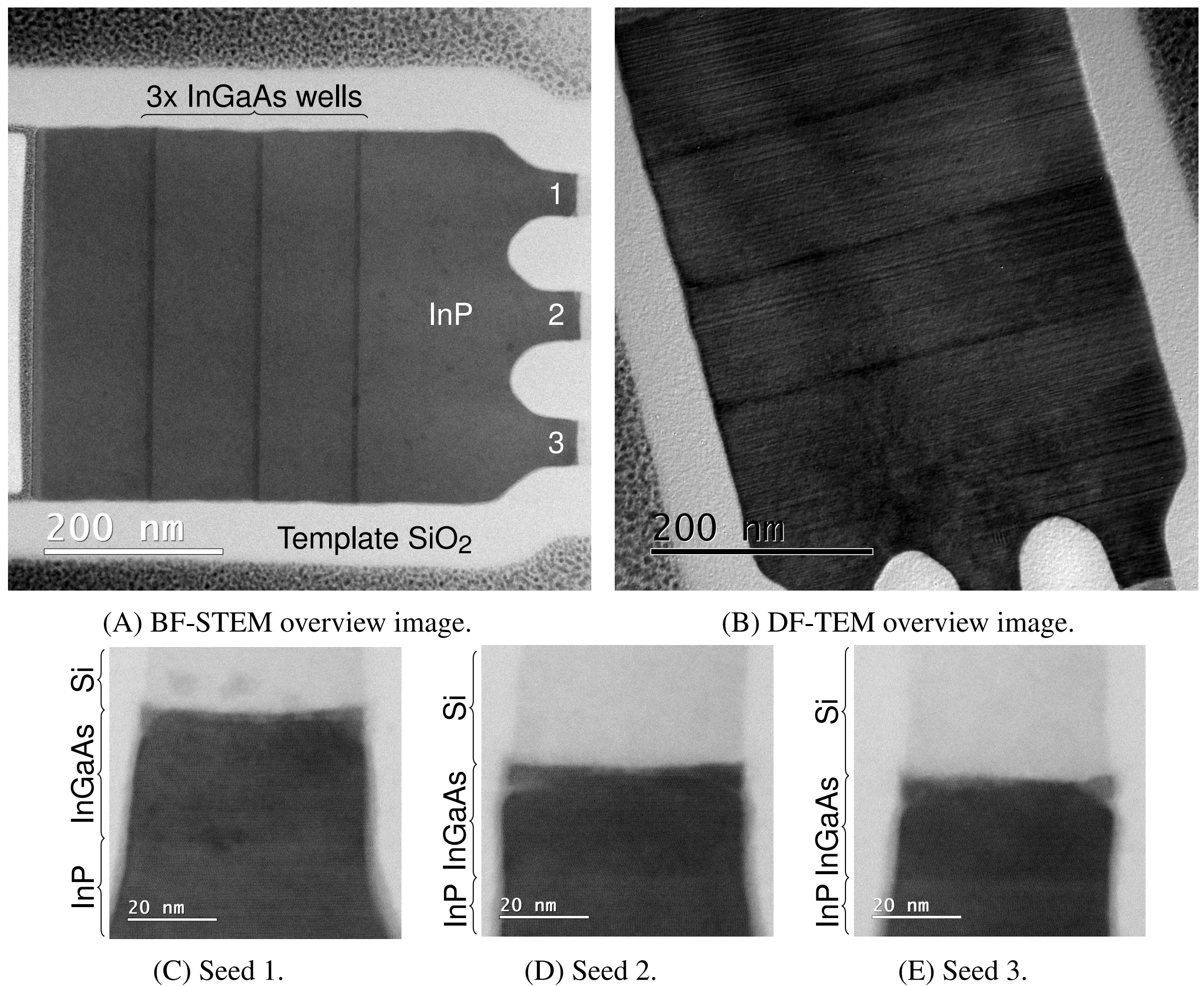
Figure 4.13: BF-STEM overview image of the lamella containing five merge structures. The right most structure has the important material layers labelled. The three structures on the left have seed widths of 50 nm and the two on the right of 70 nm. The InGaAs wells appear in the same position in all five structures, and all have heterointerfaces consisting of a single $\{1\,1\,1\}$ facet. This Figure was adapted from the work of Brugnolotto *et al.* [2] under the terms of the CC BY 4.0 licence [130].

arsenide layers are better visible in this BF-STEM image, and all appear at the same distance from the silicon seed.

The nucleation areas of this structure are shown in high-resolution BF-STEM images in Figures 4.14(C), 4.14(D), and 4.14(E). The silicon seed is visible at the top of the images. The Si / III-V interface is well defined, showing the epitaxial relationship between the two lattices. The crystal appears to have nucleated towards the centre of the silicon seed surface at all three nucleation sites. The InGaAs nucleation layer appears lighter in correspondence to the corners of the seed surface, likely due to a smaller amount of material in that area. As the crystal grows, it fills the 50 nm wide template within the first 25 atomic bilayers.

The presence of an initial InGaAs followed by the InP stabilisation layer within all three nucleation areas confirms that the simultaneous nucleation of three crystals has occurred for each structure. Once they have grown out of the SiO_2 separators, these three crystals must merge into one in the following template region. As seen in both Figures 4.14(A) and 4.14(B), the template is completely filled with III-V material, which has grown into the shape of the template. This excludes the formation of voids in this growth regime; however, the nucleation of point, line, and plane defects is still possible in the areas where the three crystals have come into contact with each other.

It is important to note that this occurs even though the thickness of the InGaAs layer is different in the three seed regions. Seed one has a InGaAs thickness of (28.3 ± 0.8) nm, seed



(A) BF-STEM overview image.

(B) DF-TEM overview image.

(C) Seed 1.

(D) Seed 2.

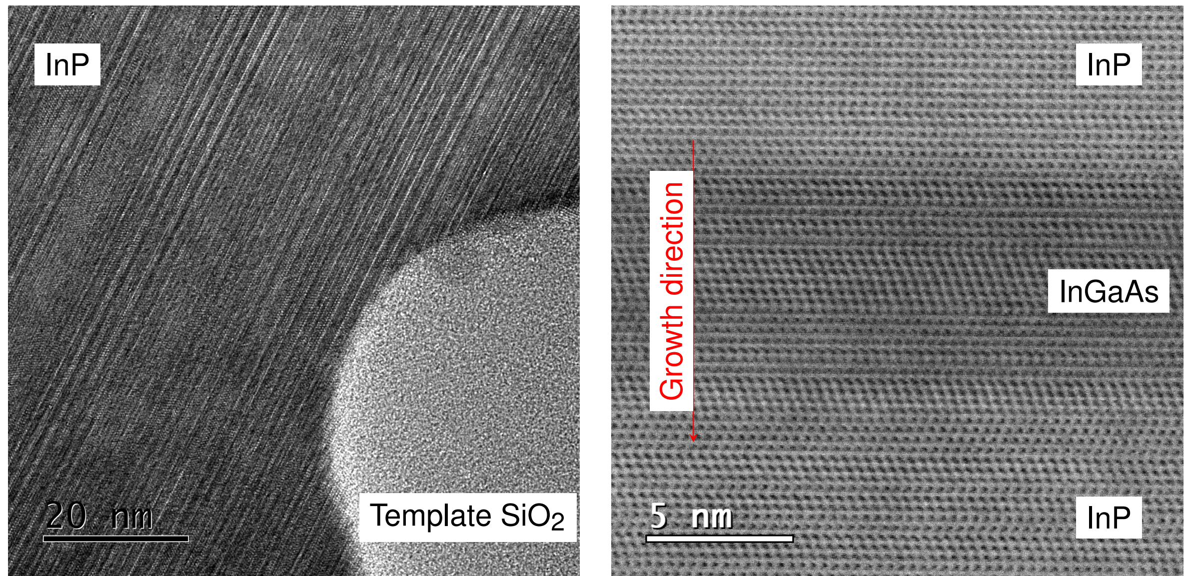
(E) Seed 3.

Figure 4.14: (A) BF-STEM and (B) DF-TEM overview images of a single merge structure. RTPs are more easily identifiable by the thin lines in (B), but no other defects can be spotted. (C), (D), and (E) are BF-STEM images of the nucleation areas 1, 2, and 3 as marked in (A); the Si seed, InGaAs nucleation, and InP stabilisation layers are marked. (B) was kindly recorded by Michael Stiefel. (A) was adapted from the work of Brugnolotto *et al.* [2] under the terms of the CC BY 4.0 licence [130].

two shows a (24.4 ± 0.3) nm thick InGaAs nucleation layer, and the third nucleation layer has a length of (23.1 ± 0.9) nm. All three numbers are the result of averaging seven repeated measurements, and their errors represent the 95 % confidence interval.

The presence of three heterolayers for each structure is reflected in the single-structure BF-STEM and dark field transmission electron microscopy (DF-TEM) overviews of Figures 4.14(A) and 4.14(B). The latter TEM image was recorded by Michael Stiefel, as was Figure 4.15(A). These three heterolayers are arsenide heterostructures, as shown by the contrast with the surrounding InP, delimited by two single-facet $\{1\,1\,1\}$ heterointerfaces. The similarity of these heterostructures to those seen in single nucleation nanowires, such as those in Figures 4.9(C) and 4.4(B), suggests that a highly ordered growth dynamic takes place in the template.

Figure 4.15(A) shows a magnified BF-TEM image of the area immediately after the SiO_2



(A) BF-TEM image of a candidate merging region.

(B) BF-STEM image of a quantum well [2].

Figure 4.15: High-resolution microscopy images for lattice analysis. (A) shows a DF-TEM image the region immediately after one of the SiO_2 spacers between the seed areas (visible in the bottom right of the image). (B) shows a high-resolution BF-TEM image of the first quantum well (counting from the nucleation areas) in the common part of the template. (A) was kindly recorded by Michael Stiefel. (B) was adapted from the work of Brugnolotto *et al.* [2] under the terms of the CC BY 4.0 licence [130].

spacer between the nucleation regions 2 and 3 as marked in Figure 4.14(A). These TEM images make structural information readily available highlighting 1D and 2D defects better than their STEM-generated counterparts. This is evident in Figure 4.15(A) by the presence of a series of lines tracing many of the $\{1\,1\,1\}$ planes in the III-V crystals. These lines are found in correspondence with RTPs, which have been a common defect in all samples grown with the $\{1\,1\,1\}$ growth front stabilisation method so far. The absence of other off-plane features in the image suggests the absence of other defects. However, a few defects could still be "hidden" because of the viewing angle.

A step-flow growth regimen can explain the absence of detectable defects on the merged regions between the three crystals [2]. Under these growth conditions, each InP atomic bilayer fills the width of the template before the next bilayer grows. This is the extreme result of the higher growth rates observed in $\langle 1\,1\,0\rangle$ directions. In such a regimen, even if a crystal reached the larger template portion with the advantage of a few bilayers over the other two, its growth would support and be supported by the lattice matched $\{1\,1\,1\}$ surfaces of the other two crystals. In this situation, as the leading crystal reaches the end of its individual seed area, diffusion of adsorbate atoms and precursors on the tightly packed $\{1\,1\,1\}$ surface would bring precursors toward neighbouring wires. In such a configuration, the growth of shorter wires could be enhanced by the additional supply of precursors from the lead wire, up to the point where the $\{1\,1\,1\}$ surface of

Table 4.3: Growth rates for the superlattice region of the sample containing merge structures.

	InGaAs			InP		
material layer	well 1	well 2	well 3	barrier 1	barrier 2	barrier 3
growth rates ($\mathrm{nm\,min^{-1}}$)	45 ± 3	48 ± 2	53 ± 3	30.5 ± 0.3	33.3 ± 0.3	37.7 ± 0.3

the shorter wire can function as a support for the lateral expansion of the leading wire. Another option is for the leading wire to simply spill over the spacer: this situation would see the formation of non-$\{1\,1\,1\}$ facets, which would quickly grow out, filling the neighbouring templates using the lattice-matched InP crystals as support.

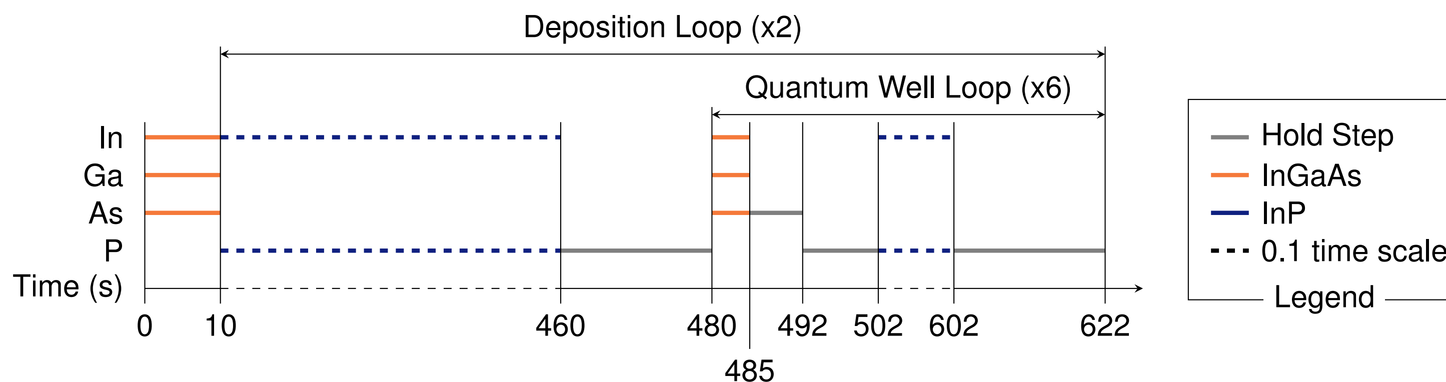
Once the single growth front is established, the growth of the crystal can continue under its step flow condition, creating the single-facet heterointerfaces seen in Figure 4.14(A). The high-resolution BF-STEM image in Figure 4.15(B) shows a section of the first InGaAs quantum well, counting from the nucleation areas toward the opening of the template. The RTPs highlighted in the BF-TEM image of Figure 4.15(A) are identifiable by the apparent change of orientation of the biatomic units visible in this atomic resolution image. The heterostructure itself appears well-defined, on par with those of previous single nucleation samples on the $\langle 1\,1\,0\rangle$ substrate shown in Figure 4.4(C).

Growth rate Table 4.3 shows the growth rates of each material layer starting at the first InGaAs quantum well for the merge structure shown in Figure 4.14(A). This III-V structure was grown in the same growth run as the wire in Figure 4.9(C), allowing a direct comparison to be drawn between these growth rates and those in Table 4.2. The growth rates for the superlattice layers of the merge structure are higher compared to their single-seed counterparts. This can be explained by the difference in the size of the template, which is 400 nm wide in the common section of the merge structure, while the nanowire in Figure 4.9(C) had a width of 210 nm. Growth rates increase as the heterolayers grow closer to the opening of the template.

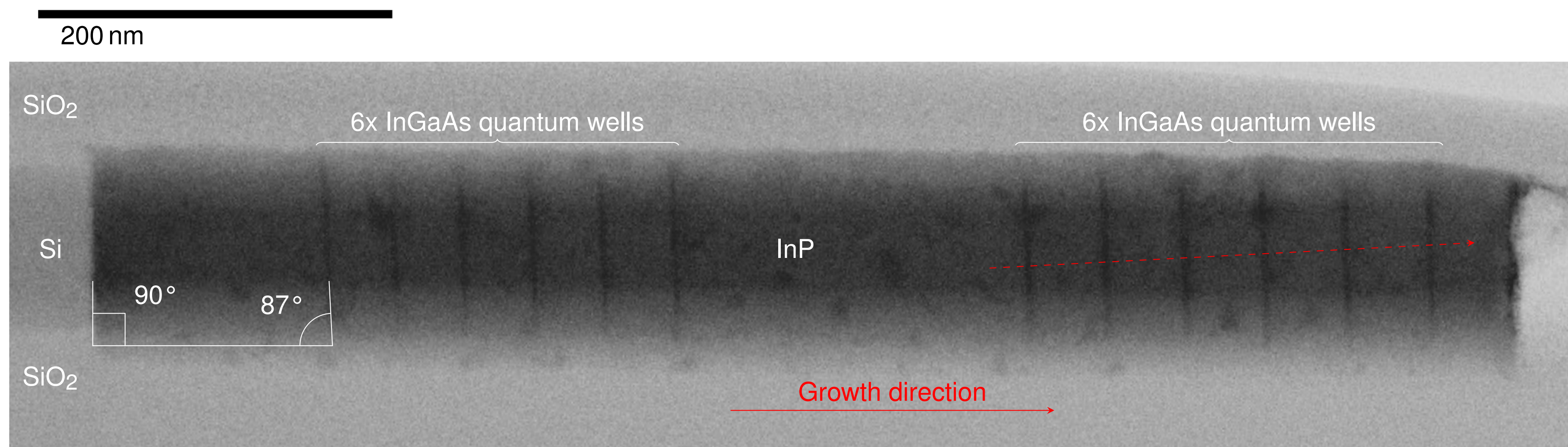
4.4 Growth of thin heterolayers

A modified growth recipe was built based on the results of sample 5. The main objectives were to create even thinner InGaAs quantum wells, which would give more information on the minimum thickness of the heterolayer achievable by MOCVD growth using the facet stabilisation method and a further decrease of the post-InGaAs arsenic hold step, to try to further mitigate the arsenic contamination in the InP region immediately after each quantum well.

The resulting recipe is shown in Figure 4.16(A). The InGaAs nucleation layer's deposition time was decreased from 30 s to 10 s. As there had been no nucleation issues with the 30 s deposition time in sample 5, a lower step time was tested for this sample to minimise the amount of InGaAs outside the quantum wells. The recipe segments and loops following the nucleation



(A) Precursor sequence for sample 6 [2]. Each line represents an active flow of the corresponding precursor into the reactor. The colour of the horizontal lines represents the target material. The dashed lines are time-compressed 10 times. The quantum well growth loop was executed six times.



(B) BF-STEM image of a nanowire grown with the recipe in (A) [2]. Each material layer is labelled, and a guide highlighting the lattice rotation is present. This Figure was adapted from the work of Brugnolotto *et al.* [2] under the terms of the CC BY 4.0 licence [130].

Figure 4.16: (A) MOCVD precursor sequence and (B) resulting nanowire for sample 6 with EDS linescan path marked by a red dashed arrow.

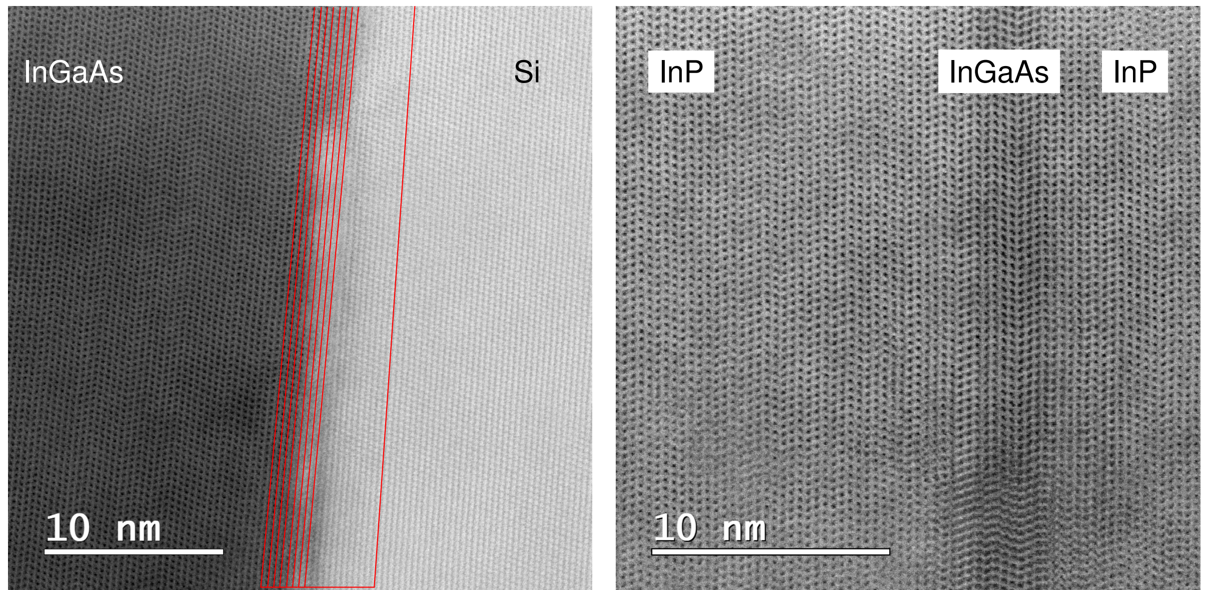
layer were run twice. The deposition of the InGaAs/InP superlattice took place after 450 s of InP growth. The step time for InGaAs was reduced from 10 s to 5 s, and the post-InGaAs arsenic hold step shortened from 10 s to 7 s. The deposition times of the barrier layers were also shortened from 200 s to 100 s. The number of repetitions of the quantum well loop was doubled from 3 to 6. The cumulative changes were meant to double the number of quantum wells present in the same length of nanowires that contained the superlattice in sample 5, while repeating the entire recipe twice was meant to result in a longer overall nanowire to highlight differences in growth rate based on the depth of each material layer in the template.

The 30° cross-section of a nanowire grown with this revised recipe is shown in the BF-STEM image in Figure 4.16(B). The angled view given by this tilted cross-section causes the shaded top and bottom interfaces of the III-V material region. The circular shades in the image are given by indium droplets, a common residue left over from FIB lamella preparation. The III-V material, appearing darker in the centre of the image, is sandwiched between the template oxide at the top and the buried oxide layer at the bottom. The silicon seed is visible on the left of the image, while the InGaAs nucleation layer is too thin to appear as more than a darker shade at the very beginning of the nanowire. Twelve vertical lines, darker compared to the InP making up the majority of the wire, are created by a change in channelling contrast given by the presence of arsenic atoms, which are larger than the phosphorus atoms that make up the majority of the V group atoms in the wire.

The seed surface consists of a single $\{1\,1\,1\}$ facet resulting from the selective etching of silicon carried out with TMAH before deposition. This surface forms a 90° angle with the wafer plane, but, as can be seen in the highlight in Figure 4.16(B), the first quantum well, and indeed all the others, are tilted 3° off the perpendicular to the wafer plane. A slight rotation of the growing lattice compared to the seed's lattice orientation can occur during epitaxy because it is a way for the growing crystal to compensate for some of the stress caused by lattice mismatch. Despite the 3° rotation, the stabilisation of the $\{1\,1\,1\}$ facet is achieved during the initial InP deposition and is maintained throughout the wire. The 12 quantum wells range in thickness from 3.7 nm to 4.3 nm.

High resolution analysis Figure 4.17 shows high resolution BF-STEM images of two heterostructures in the nanowire seen in Figure 4.16(B). Many RTPs are present in both images, confirming that this defect is the most common in III-V $_B$ growth on $\{1\,1\,1\}_B$ planes.

Figure 4.17(A) shows the heterointerface between the silicon seed and the InGaAs nucleation layer. 8 red lines were added parallel to the first visible continuous biatomic layer on the InGaAs side. A single red line was added to follow one of the Si $\{1\,1\,1\}$ facets. By comparing the distance between the lines at the top and bottom of the image, it is clear that the two lattices are already misaligned at the nucleation interface. This region is strained by the mismatch between two lattices, and the first few InGaAs atomic layers after the silicon seed surface are prone to



(A) BF-STEM image of the Si / III-V interface.

(B) BF-STEM image of the first InGaAs QW.

Figure 4.17: High-resolution BF-STEM images of (A) the nucleation area, showing the Si / InGaAs heterointerface. The red lines highlight the $\{1\,1\,1\}$ atomic planes in InGaAs and Si. As can be seen by comparing the distance between the lines following the atomic planes in InGaAs and in Si at the top and at the bottom of the image, there is a difference in alignment resulting in the rotation of the $\langle 1\,1\,1 \rangle$ axis highlighted in Figure 4.16(B). (B) shows the first quantum well in sample 6, various RTPs are visible.

nucleation for dislocations. The presence of this type of defect in the blurred area at the centre of the image can explain the varying distance between the two $\{1\,1\,1\}$ atomic planes in the InGaAs and silicon.

The first, counting from the silicon seed, InGaAs quantum well appears as the darker vertical stripe in Figure 4.17(B). The well is well-defined thanks to the channelling contrast between the light phosphorus atoms and the heavier As atoms, which denotes a good segregation of the two species in the respective layers. Comparing the InP layers at either side of the well, however, shows a darker shade on the right, in the InP area, which grew immediately after the InGaAs heterolayer. This suggests the presence of arsenic contamination after the well, as observed in all previous samples.

Growth rate Growth rates in the quantum well structure were calculated by averaging seven thickness measurements of each material layer along the $\langle 1\,1\,1 \rangle$ direction and dividing them by the deposition time, which is taken from the recipe and is assumed to be error-free. Figure 4.18 shows each growth rate as a function of the distance of the first heterointerface of the respective layer from the silicon seed. This metric is also calculated by averaging seven measurements and errors on the first heterointerface's position and the growth rates of each layer to express the 95 % confidence interval. All errors were plotted in Figure 4.18. However, the only error

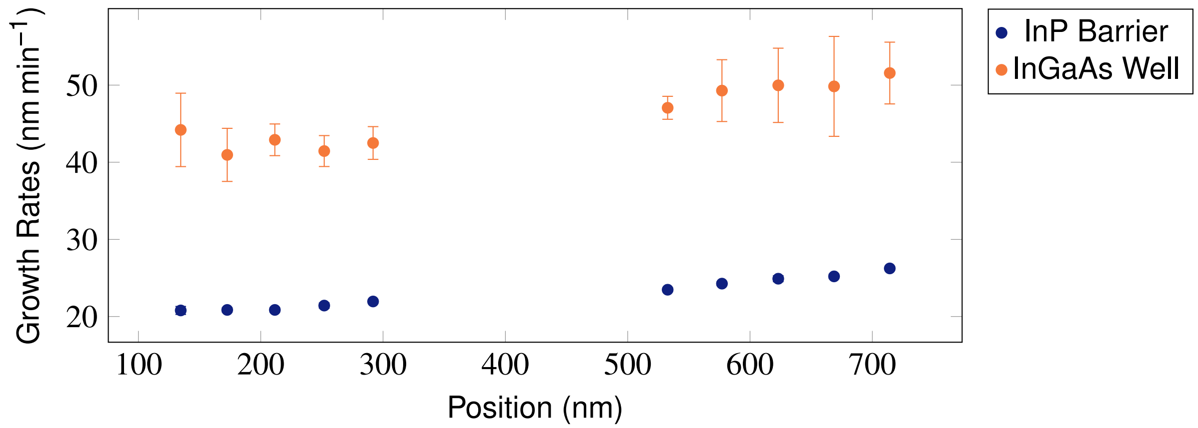
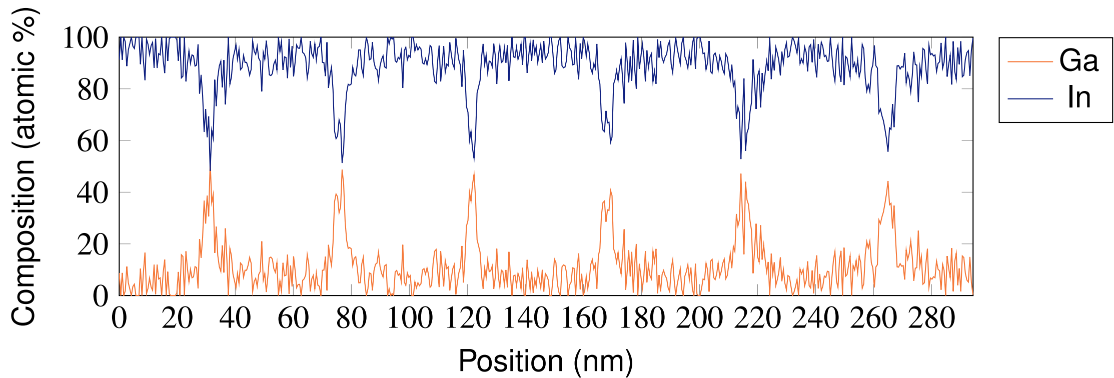
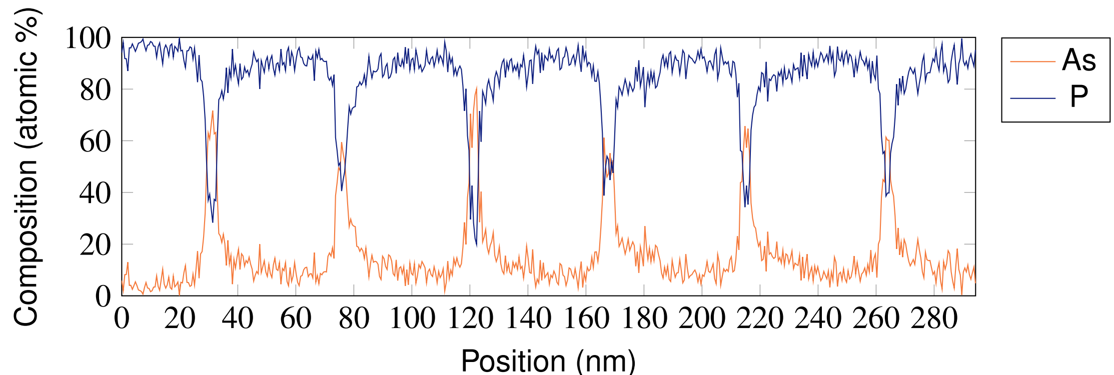


Figure 4.18: InGaAs and InP material layer growth rates as a function of their distance from the Si seed surface [2]. Both x and y error bars are present but smaller than the markers, except for those on the growth rate of InGaAs. This Figure was adapted from the work of Brugnolotto *et al.* [2] under the terms of the CC BY 4.0 licence [130].



(A) EDS linescan: III atomic percentage vs position.



(B) EDS linescan: V atomic percentage vs position.

Figure 4.19: EDS linescan compositional data (in percentage) for the (A) III group elements and (B) V group elements across the last 6 quantum wells of sample 6 (Figure 4.16(B)). The origin of the x-axis is situated before the first well and is the closest point to the Si seed. Higher position numbers (in nm) represent the scan moving along the $\{1\,1\,1\}$ vector perpendicular to the growth front away from the seed. This Figure was adapted from the work of Brugnolotto *et al.* [2] under the terms of the CC BY 4.0 licence [130].

bars that exceeded the size of the graph markers were those of the InGaAs quantum well growth rates.

Growth rates for InP layers start at $(20.8 \pm 0.5)\,\mathrm{nm\,min^{-1}}$ and end at $(26.2 \pm 0.2)\,\mathrm{nm\,min^{-1}}$, falling between those of samples 4 and 5. On the other hand, the growth rates of InGaAs quantum wells is higher than both those of samples 4 and 5 and ranges from $(41 \pm 3)\,\mathrm{nm\,min^{-1}}$ to $(52 \pm 4)\,\mathrm{nm\,min^{-1}}$. The increase in the growth rate values with the nearing of the growth front to the opening of the template confirms its dependence on the diffusion process of the precursors and adsorbates in the template [156]. Their lower thickness gives the higher error in the growth rates of the InGaAs layers.

EDS analysis An EDS linescan was carried out along the $\langle 1\,1\,1 \rangle$ vector which also defines the $\{1\,1\,1\}$ single-facet heterointerfaces, marked in red in Figure 4.16(B), to capture the variation in composition across the last 6 InGaAs quantum wells. Figure 4.19(A) shows the concentration profile of the III group element. The noise level is around 15 % and the calculated atomic percentage of gallium in the InGaAs layer ranges from 40 % to 50 %. These concentrations are in line with those seen in Figure 4.10(A) for sample 5.

Figure 4.19(B), however, shows a low arsenic concentration in the InGaAs layers. Its highest value is 80 % in well 9, while it oscillates between 50 % and 60 % in wells 7, 8, 10, 11, and 12. These concentration profiles depart from the very well-segregated V group elements shown in Figure 3.14(B), 4.7(B), and 4.10(B). This indicates that layers under 5 nm in thickness could be too thin to allow for a complete switch in composition from phosphorus to As. Other explanations involve probe size effects, which could be "smoothing" the composition profiles across the heterointerfaces, or a small angle in the lamella exposing both InGaAs and InP to the beam. However, comparing the V group element profiles with the III group element profiles, it appears unlikely that either of these instrument-related distortions could have played a major role. Indeed, the same effects would be expected to affect the concentration profile of the III group elements, lowering the gallium concentration as a result. The fact that this has not happened makes the possibility that the thickness of the transition layer is on the order of 2 nm more likely.

Arsenic contamination continues to be present in the InP layer immediately after the InGaAs quantum wells.

4.4.1 Growth in a competitive environment

As seen in the SEM image in Figure 4.9(B), competition between multiple nucleation points within a nanowire array does not result in a pronounced variation of growth rate within the nanowires.

Figure 4.20 shows a nanowire grown in an area of the wafer with many parasitic crystals. This can happen because of leftover contaminants on the wafer surface. In this case, the contam-

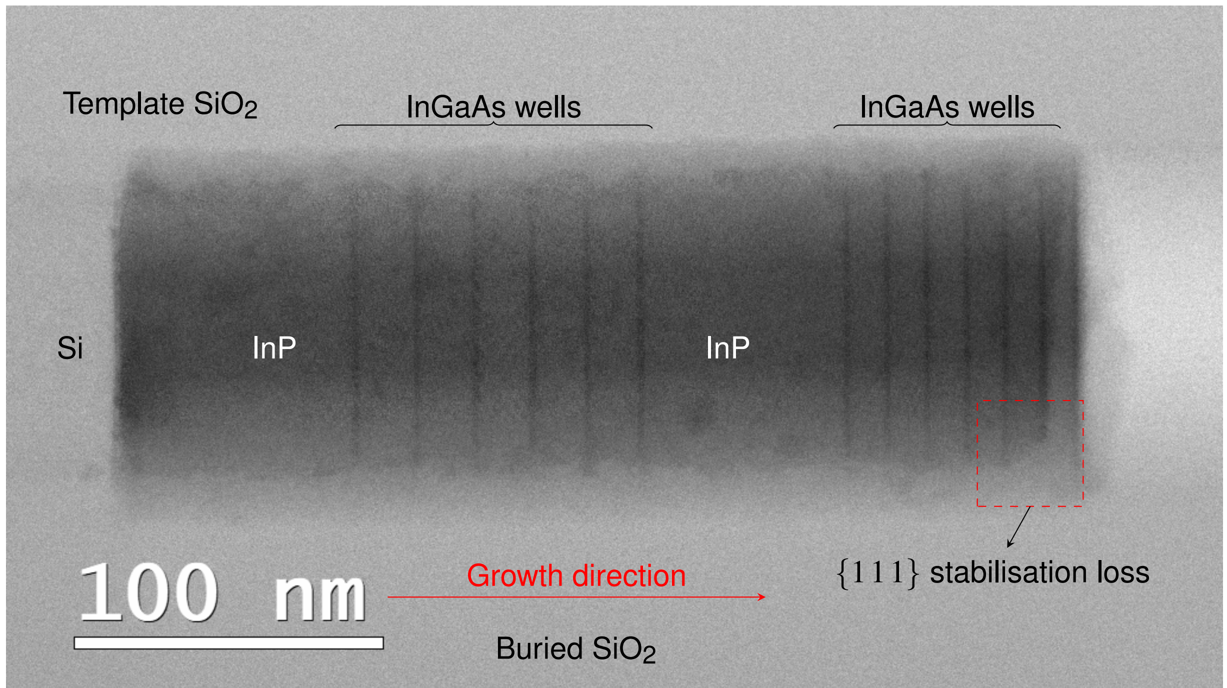


Figure 4.20: BF-STEM image of a nanowire from sample 6 grown in an area of the wafer with many parasitic nucleations. The wire grew from the Si seed on the left in the direction specified by the red arrow. Compared with the wire shown in Figure 4.16(B) all layers are thinner, resulting in a shorter wire. A loss stabilisation of the $\{1\,1\,1\}$ single-facet growth front occurs at the end of the wire, as revealed by the trace left by the InGaAs wells.

inants were likely deposited by vacuum-driven evaporation of a small droplet left on the surface of the chip after manipulation with wet tweezers. The contaminants act as additional nucleation centres for the III-V precursors. This is similar to the procedure used to create a self-assembled distribution of nanocrystals. The resulting 100 nm-wide crystals created a much more competitive growth environment compared to the rest of the chip that was unaffected by this issue and from which the wire in Figure 4.16(B) was cut.

As a result, the wire in Figure 4.20 is considerably shorter than the wire in Figure 4.16(B). The InGaAs nucleation step resulted in a nanocrystal visible by channelling contrast in the lower left portion of the Si / III-V interface. The 12 InGaAs quantum wells are still visible in the InP matrix and provide a snapshot of the evolution of the growth front. Counterintuitively, the growth rates of the various heterolayers appear to decrease as the wire grows towards the opening of the template, as demonstrated by the shorter InP segments in the last part of the wire.

As parasitic crystals grow, so does their ability to capture precursors. As a result of the template oxide restricting the gas phase diffusion of the precursors to a smaller solid angle and lengthening the surface diffusion distance the adsorbates have to travel to reach the growing nanowire, the precursor capturing power of the parasitic crystals increases more rapidly than that of the TASE nanowires. This competition mechanism explains the decrease in the growth rate of the nanowire. Further, the last InGaAs quantum well of the wire in Figure 4.20 is shorter

than the others, with a multi-facet growth front forming in the previous InP barrier layer. This indicates that the effective V / III ratios in the template are beginning to be affected by the competitivity of the parasitic crystals in precursor capture.

If the deposition of densely packed III-V structures is planned, the effect of this competition during MOCVD growth should be taken into account to ensure that the desired material properties are obtained.

4.5 Growth of strained heterolayers

All samples presented so far in this thesis targeted an $In_{0.53}Ga_{0.47}As$ composition in the arsenide layers, with varying degrees of success, as shown in each sample's EDS analysis. This composition is lattice-matched to the supporting InP barrier layer [82, 83, 84], therefore simplifying the growth process by confining any strain or stress to the initial material layers after nucleation.

Therefore, the introduction of a lattice mismatch in the quantum well heterointerface will alter the stress profile within the nanowire, introduce strain gradients at each interface, or potentially have both effects. In turn, this can lead to destabilisation of the $\{1\,1\,1\}$ single-facet growth front regimen created by the high V / III ratio InP layer. To verify whether or not this occurs, two experiments were carried out that broadened the scope of the materials under investigation to other arsenides and antimonides.

4.5.1 Arsenides

Two more binary materials, gallium arsenide (GaAs) and indium arsenide (InAs), can be grown without altering the precursor species introduced into the reactor from those used in previous experiments. Figure 4.21 shows the MOCVD recipe used in the growth of sample 7. This new recipe was derived from those used for samples 5 and 6 (Figures 4.9(A) and 4.16(A)). The initial InGaAs nucleation layer, with a target composition of $In_{0.53}Ga_{0.47}As$ was grown for 30 s, followed by the 450 s-long InP $\{1\,1\,1\}$ facet stabilisation step.

The superlattice deposition loop was expanded to include InAs and GaAs quantum wells. Both materials were deposited in 10 s-long steps, while the growth time of the third arsenide layer targeting the lattice matched $In_{0.53}Ga_{0.47}As$ was kept unchanged from sample 6 at 5 s. The three InP barrier layer deposition steps lasted 100 s. The growth loop sequence was InAs - InP - InGaAs - InP - GaAs - InP. The hold steps were kept unchanged from those of sample 6: the post-phosphide hold step consisted in a 20 s-long *tert*-butyl phosphine (TBP) single-precursor flow, while the post-arsenide hold step was kept as 7 s of pure *tert*-butyl arsine (TBAs) followed by 10 s of pure TBP. This quantum well deposition loop was repeated three times, resulting in nine quantum wells: three for each target arsenide compound.

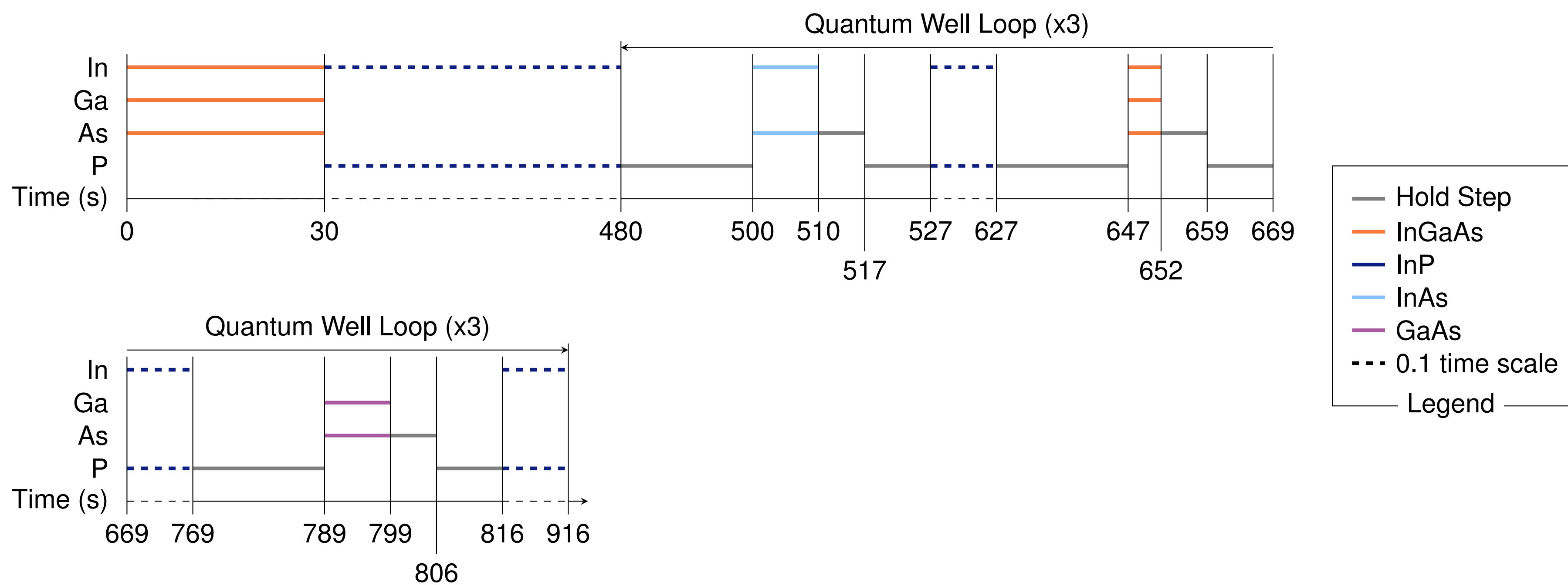


Figure 4.21: MOCVD precursor sequence for sample 7 [2]. Each line represents an active flow of the corresponding precursor into the reactor. The colour of the horizontal lines represents the target material. The dashed lines are time-compressed 10 times. The quantum well growth loop was executed three times.

Table 4.4: V/III ratios used in the MOCVD growth of sample 7 [2].

Material	InP	InAs	InGaAs	GaAs
V/III Ratio	234	186	29	34.4

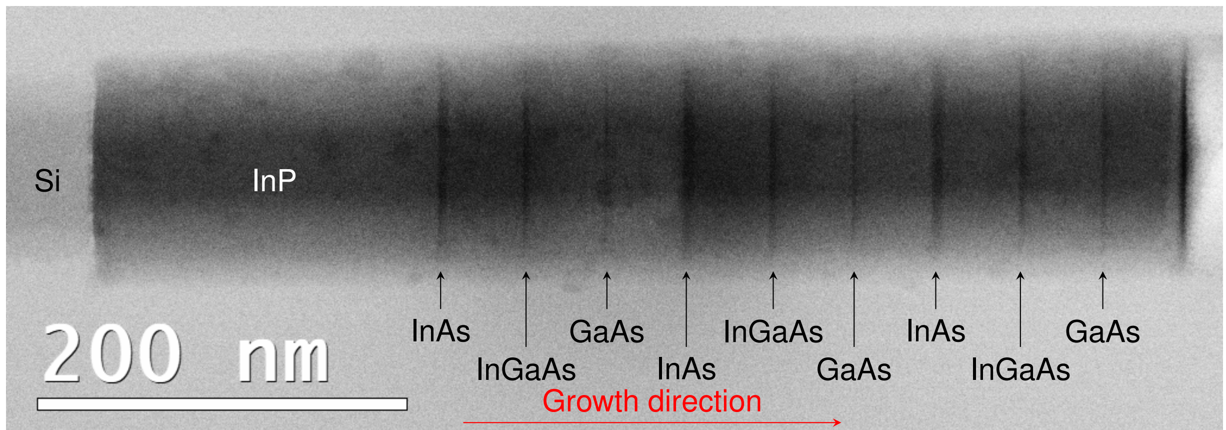


Figure 4.22: BF-STEM image of a nanowire from sample 7. The Si seed is on the left of the image, followed by the InGaAs nucleation layer and InP stabilisation layer. Of the 9 quantum wells, the thickest are composed of InAs, then the InGaAs quantum wells, and finally the GaAs quantum wells are the thinnest, assuming the intended material layers have been deposited. This Figure was adapted from the work of Brugnolotto *et al.* [2] under the terms of the CC BY 4.0 licence [130].

The V / III molar ratios loaded in the reactor in this growth run are summarised in Table 4.4. The precursor flows were kept unchanged from previous growth runs and, as such, the V / III ratios during the deposition of InP and InGaAs are unchanged from those seen in Table 3.1 at 234 and 29, respectively. The precursor flows were kept constant during deposition to avoid fluctuations in precursor molar flows given by the real hardware. As such, the V / III ratios for InAs and GaAs were dictated by the flows used to deposit InP and InGaAs. The V / III rates for these last two material deposition steps were 186 and 34.4, respectively.

The complexity of the precursor switches varies in the quantum well deposition loop. The simplest is the InP to InAs material switch, as only the V precursor changes. In the InGaAs deposition layer, there is a switch of V precursor, and both III precursors are used, while in the last GaAs layer, both V and III precursors are switched. When considering diffusion times, the InP to GaAs is the more complex of the material changes, as the potential of leftover precursors from the InP deposition step still being able to diffuse to the reaction interface can lead to the formation of a quaternary InGaAsP layer at the heterointerface, two elements away from the target material.

Figure 4.22 shows a BF-STEM image of a lamella cut with the 30° method out of a nanowire array grown with the recipe in Figure 4.21. The silicon seed is on the left of the image, and the nanowire grew toward the right. 3 groups of 3 quantum wells of different size are visible after the initial InP stabilisation layer.

The evolution of the growth front morphology during MOCVD growth is captured by the heterolayers embedded in the InP matrix. All arsenide layers form parallel lines and are enclosed by $\{1\,1\,1\}$ heterointerfaces. Any eventual strain introduced in the nanowire lattice does not destabilise the $\{1\,1\,1\}_B$ growth regimen.

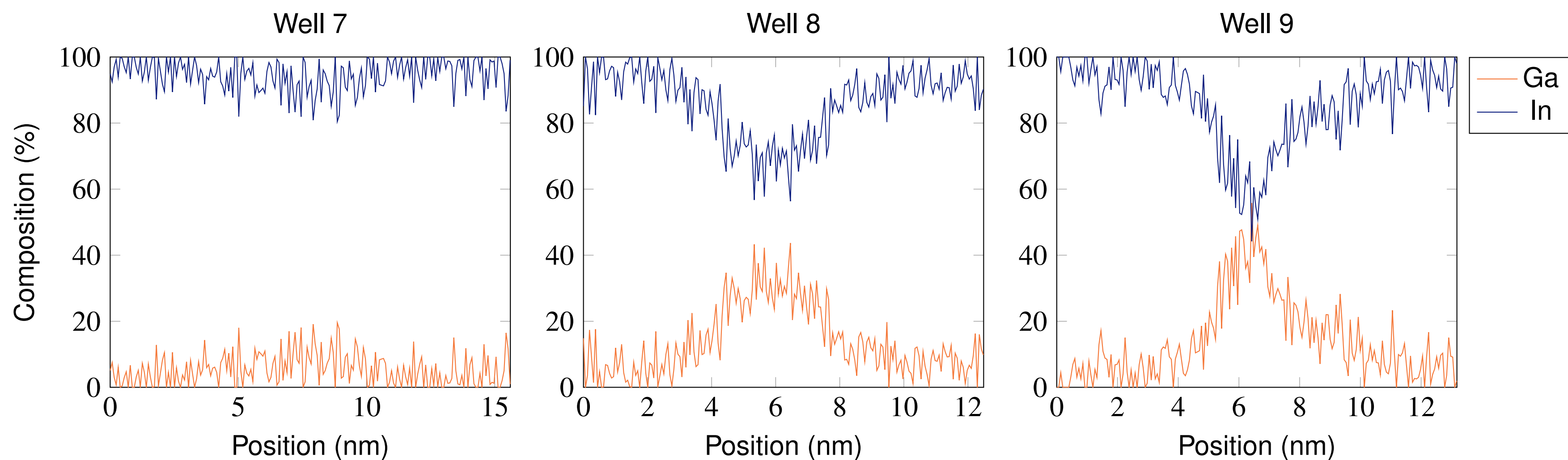
EDS analysis Figure 4.23 summarises the calculated concentration of III and V group elements as calculated from EDS linescans carried out across the quantum wells of sample 7, shown in Figure 4.22. The concentration profiles of each quantum well are coupled vertically: from left to right, the results of the 7th, 8th, and 9th quantum well are shown. As usual, the III group element concentration profiles are calculated from the relative intensity of the L_α lines of gallium and In, resulting in a 20 % noise level. Likewise, the V group element concentrations were derived from the relative intensity of the K_α lines of phosphorus and arsenic, and the resulting concentration profiles have a noise level of 15 %.

The InAs layer grew as expected with only a light phosphorus background remaining in the quantum well region. The following InGaAs layer is rich in indium when compared to the target composition of $In_{0.53}Ga_{0.47}As$, showing an indium atomic percentage value around 75 % instead. Similarly, the (planned) GaAs layer grew highly alloyed, with gallium representing less than 50 % of the atoms in the well.

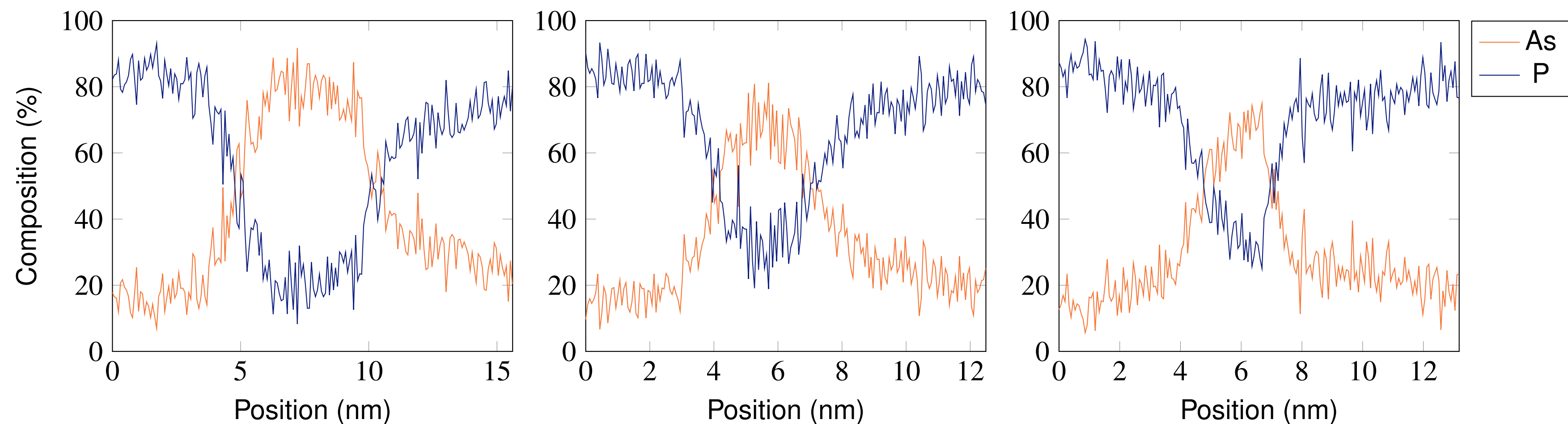
The high indium content is probably due to the high rate of incorporation of this species into ternary arsenides during $\{1\,1\,1\}$ growth [55]. The In/(In+Ga) ratio loaded into the reactor during InGaAs growth was 0.16 which is expected to lead to a $In_{0.5}Ga_{0.5}As$ composition [55]. In reality, the steepness of the function that links the molar fraction of trimethyl indium (TMIn) in the reactor with the molar fraction of indium in the resulting material is very high [55]. This means that fluctuations in precursor concentration within the template, due to different diffusion effects, can lead to very different growth results in terms of indium concentration. Similarly, even a small amount of indium being leftover in the template after the hold steps or diffusing into it from the surface of the chip has a very high impact on the final indium concentration in the material.

Therefore, the three arsenide materials are better identified as InAs, $In_{0.75}Ga_{0.35}As_{0.60}P_{0.40}$, and $In_{0.55}Ga_{0.45}As_{0.5}P_{0.5}$. Longer hold steps could solve the alloying issue in the layers of the last two materials [2].

The V group element composition graph for the 2 nm-wide well 9 tells an interesting story about finite heterointerfaces. Indeed, the arsenic composition profile is highly asymmetrical. The leading edge grows in the same half-bell shape seen in all previous composition profiles but decays much more abruptly in the trailing edge. This can be explained by the fact that the growth of the GaAs layer is cut short before the well composition stabilises. This finding allows for an even stronger argument for longer hold steps in future deposition recipes and gives an indication of the real size of each heterointerface under these growth conditions, which is larger

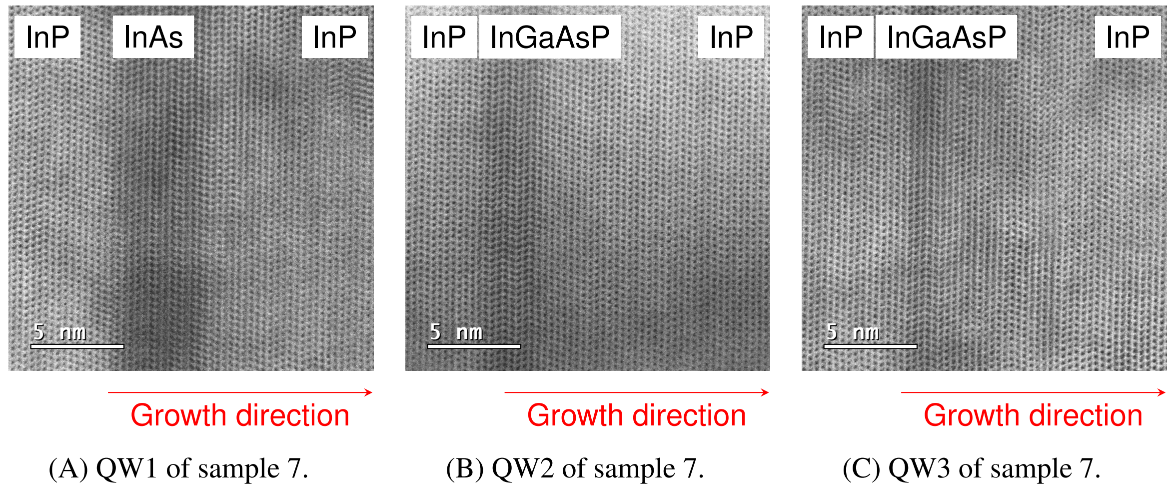


(A) Gallium and indium concentrations in atomic percentage across the 7th, 8th, and 9th quantum well of the wire in Figure 4.22 [2].



(B) Arsenic and phosphorus concentrations in atomic percentage across the 7th, 8th, and 9th quantum well of the wire in Figure 4.22 [2]

Figure 4.23: (A) III and (B) V concentration profiles across the 7th, 8th, and 9th quantum well of the nanowire in Figure 4.22. This Figure was adapted from the work of Brugnolotto *et al.* [2] under the terms of the CC BY 4.0 licence [130].



(A) QW1 of sample 7. (B) QW2 of sample 7. (C) QW3 of sample 7.

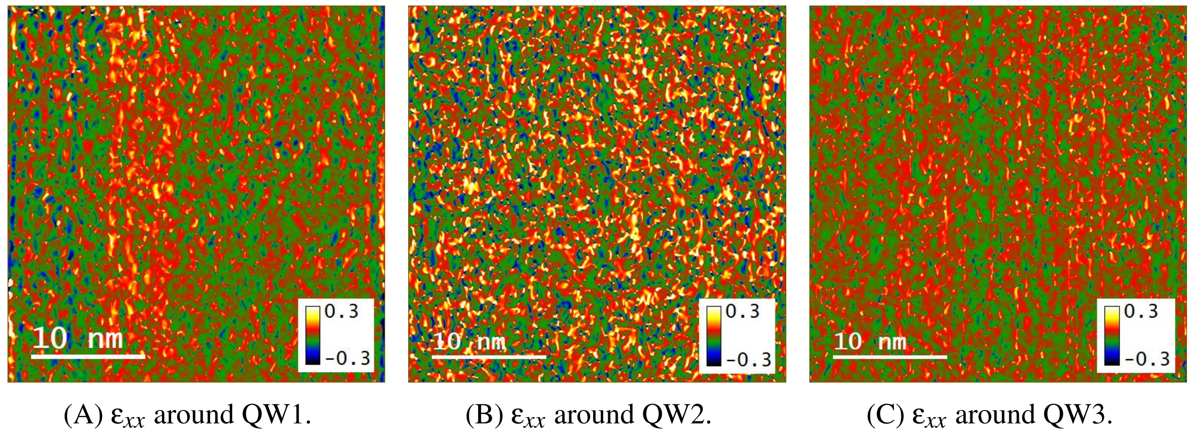
Figure 4.24: High-resolution BF-STEM images of the first three quantum wells of the nanowire pictured in Figure 4.22. (A) shows the first InAs quantum well, (B) shows the first $In_{0.75}Ga_{0.35}As_{0.60}P_{0.40}$ quantum well, and (C) shows the first $In_{0.55}Ga_{0.45}As_{0.50}P_{0.50}$ quantum well.

than 2 nm.

Structural analysis The BF-STEM images in Figure 4.24 show the first three quantum wells of sample 7 in atomic resolution. Rotational twin planes are present in this sample, much like the previous ones grown with the $\{1\,1\,1\}_B$ stabilisation method. The InAs QW is shown in Figure 4.24(A) and is the largest of the three, followed by the $In_{0.75}Ga_{0.35}As_{0.60}P_{0.40}$ well shown in Figure 4.24(B). The shortest material layer is the $In_{0.55}Ga_{0.45}As_{0.50}P_{0.50}$ well in Figure 4.24(C) which is only 4 atomic bilayers thick. The thinness of this layer is at the limit of what can be grown with classical MOCVD, as thinner layers begin to fall under the umbrella of atomic layer deposition (ALD) methods. Nevertheless, the creation of such a thin material layer with this definition demonstrates the strength of the deposition recipe used to achieve this result, despite the composition issues that were just discussed.

Growth rates Growth rates were calculated for the first and last three arsenide quantum wells end for the first and seventh InP barriers. The InP growth rate for the first barrier was $(23.8 \pm 0.3)\,\mathrm{nm\,min^{-1}}$ and $(24.0 \pm 0.4)\,\mathrm{nm\,min^{-1}}$ for the seventh barrier. These growth rates are in line with those seen in previous samples, as are those for the first and last quantum wells of $In_{0.75}Ga_{0.35}As_{0.60}P_{0.40}$, at $(39 \pm 3)\,\mathrm{nm\,min^{-1}}$ and $(44 \pm 2)\,\mathrm{nm\,min^{-1}}$.

The growth rates for the other two materials can be analysed by taking into account the V / III ratios. The growth rates of InAs wells have the largest increase of all material layers, going from $(26.4 \pm 0.2)\,\mathrm{nm\,min^{-1}}$ to $(34 \pm 1)\,\mathrm{nm\,min^{-1}}$. This growth rate is higher than that of InP, as expected by the lower V / III ratio. On the other hand, the growth rate of the $In_{0.55}Ga_{0.45}As_{0.50}P_{0.50}$ is the lowest of the four, at $(11.6 \pm 0.9)\,\mathrm{nm\,min^{-1}}$ for the first well and



(A) ε_{xx} around QW1. (B) ε_{xx} around QW2. (C) ε_{xx} around QW3.

Figure 4.25: GPA analysis from BF-STEM images of the first three quantum wells of the nanowire pictured in Figure 4.22. (A) shows the first InAs quantum well, (B) shows the first $In_{0.75}Ga_{0.35}As_{0.60}P_{0.40}$ quantum well, and (C) shows the first $In_{0.55}Ga_{0.45}As_{0.50}P_{0.50}$ quantum well. The GPA calculations were kindly carried out by Marilyne Sousa.

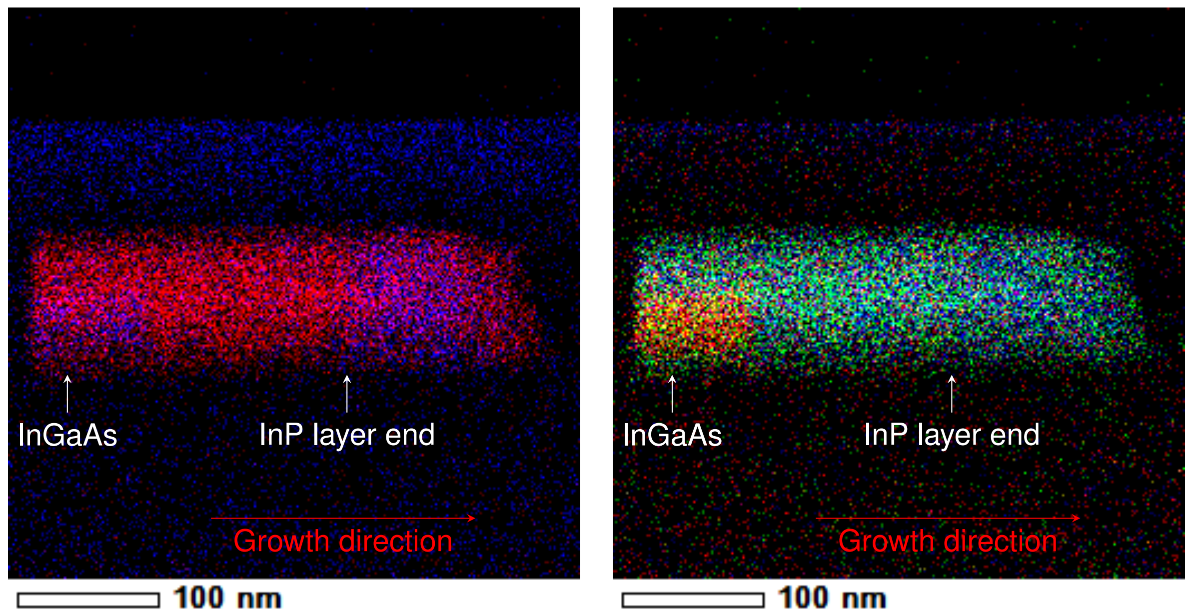
$(12.5 \pm 0.5)\,\mathrm{nm\,min^{-1}}$ for the last. This is despite the V / III ratio of 34.4 being much closer to that used in the second well.

Strain analysis Figure 4.25 shows part of the result of a geometric phase analysis (GPA) analysis of the images in Figure 4.24. In particular, all three images depict the intensity of the ε_{xx} component of the strain tensor, where "x" is the direction parallel to the bottom margin of each image, therefore coinciding with the $\langle 1\,1\,1 \rangle$ vector in the crystalline lattice. Figures 4.25(B) and 4.25(C) only show background noise, as is expected given the closeness of the quantum well's composition to the lattice match. Figure 4.25(A), on the other hand, shows a small difference in lattice constant corresponding to the pure InAs layer. This variation is small, and close to the noise level, but can be qualitatively seen in the image.

4.5.2 Antimonides

Another precursor available in the MOCVD setup was trimethyl antimony (TMSb). III-antimonides were, therefore, good candidates to expand the elements incorporated in the nanowires grown in the $\{1\,1\,1\}$ facet stabilisation method. The growth recipe for this sample employed a 30 s-long InGaAs nucleation layer followed by a 450 s-long InP stabilisation layer. The quantum well deposition loop contained three gallium antimonide (GaSb) deposition steps of varying length, 5 s, 10 s and 30 s. This sequence of steps went from small to large, separated by 100 s-long barrier-InP deposition steps to avoid excessive build-up of antimony. A 20 s-long phosphorus hold step followed the InP layers but also the GaSb layers to avoid antimony accumulation. The V / III ratio loaded into the reactor for the GaSb later deposition steps was 1.09, chosen based on previous experiments conducted on the same deposition set-up to maximise growth yield [74].

However, as shown by the EDS maps in Figure 4.26, this approach was unsuccessful. The



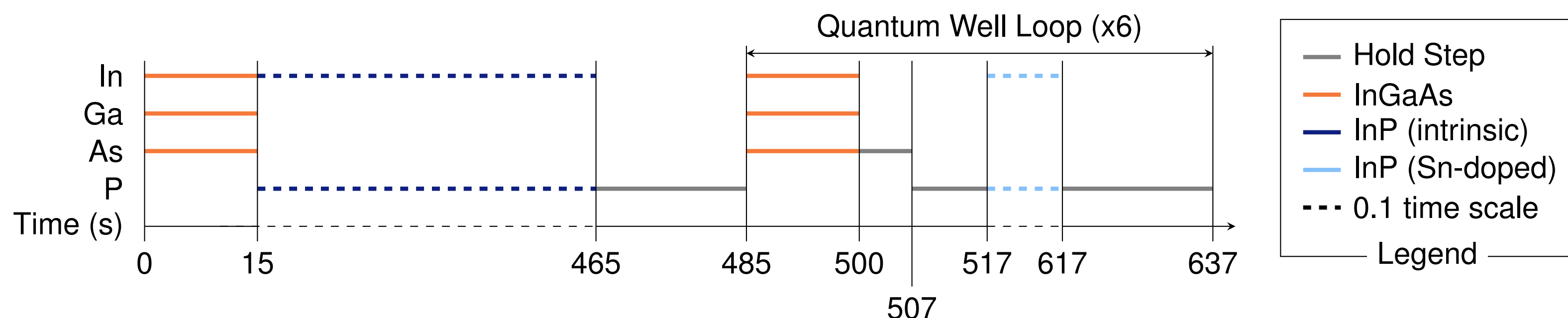
(A) III-element EDS map. Red In, blue Ga.

(B) V-element EDS map. Red As, green Sb, blue P/Pt.

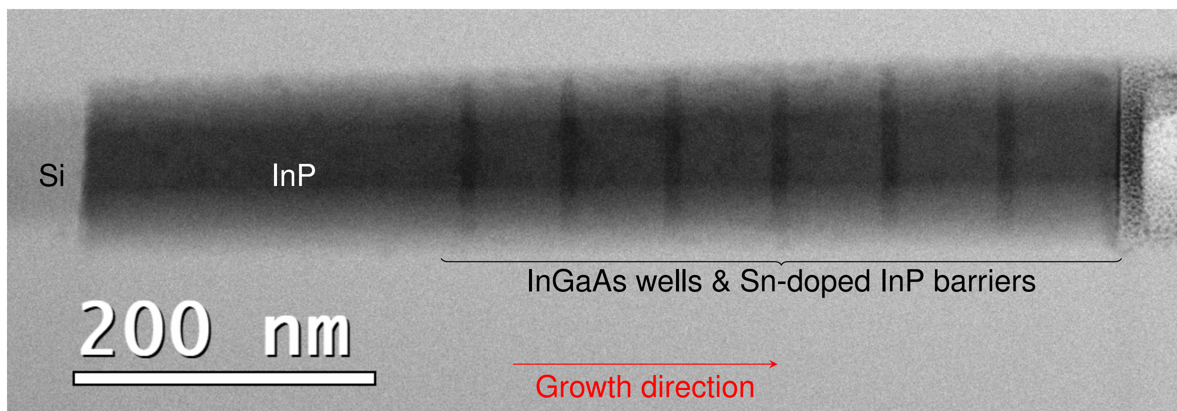
Figure 4.26: EDS overview maps of sample 8. The wires grew from left to right, as highlighted by the red arrow at the bottom of (A) and (B). (A) provides the most information on the structure of the wire. The InGaAs seed, revealed on the bottom left by the presence of Ga, has a low elongated profile, however the next InP layer, revealed by the In signal, completely fills the template showing indications of $\{111\}$ stabilisation. As Sb is introduced in the reactor, however, organised growth breaks down, and the wire ends with a random facet configuration. (B) highlights the InGaAs seed location, however, either due to the remains of an Sb droplet or closeness in EDS peak, the phosphide and antimonide layers are not distinguishable.

lamella used for the EDS analysis was cut from one of the most promising wires, which, while presenting an elongated InGaAs seed, saw the template being completely filled during the following InP deposition, as can be seen in Figure 4.26(A). However, introducing an antimonide layer caused extensive alloying, likely because of the formation of an antimony droplet, while also slowing the growth rate of the nanowire. The antimony signal in Figure 4.26(B) was calculated from the antimony L_α line that, at 3.604 keV is close in energy to the 3.286 keV indium K_α line. This is one of the possible explanations for the presence of antimony signal throughout the wire in the EDS map, the other being a contamination form during FIB lamella preparation from leftovers of the antimony droplet.

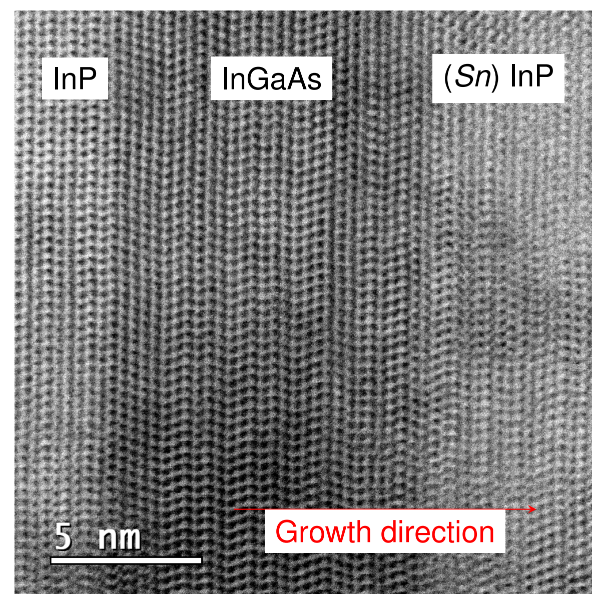
Due to project-related time constraints, further optimisation of the growth conditions for antimonide integration could not be performed.



(A) Precursor sequence for sample 9. Each line represents an active flow of the corresponding precursor into the reactor. The colour of the horizontal lines represents the target material. The dashed lines are time-compressed 10 times. The quantum well growth loop was executed six times.



(B) BF-STEM image of a lamella cut from a nanowire grown with recipe 9 with labelled material layers. The wire grew from the Si seed in the direction marked by the red arrow.



(C) BF-STEM of the first QW of the wire in (B).

Figure 4.27: MOCVD precursor sequence and STEM analysis of sample 9. (A) shows a schematic of the precursor sequence, with colour-coded recipe segments. (B) shows a BF-STEM overview image of a nanowire cut from sample 9. (C) shows a high resolution BF-STEM image of the first quantum well of the lamella in (B)

4.6 Doped semiconductors

The study of the effect of dopants on the $\{1\,1\,1\}$ growth regime is an important aspect to consider when bridging the gap between pure growth studies and device integration. Although an active component can incorporate quantum wells or not, the reliable stabilisation of a single-faceted growth front also helps with contacting devices with a plain intrinsic region. However, as the last sentence suggests, active photonic devices are usually doped, often in a p - i - n configuration. The impact on the growth mechanism of introducing dopants in the lattice and the reaction atmosphere, although in low quantities compared to the precursors of the main species, should, therefore, be studied.

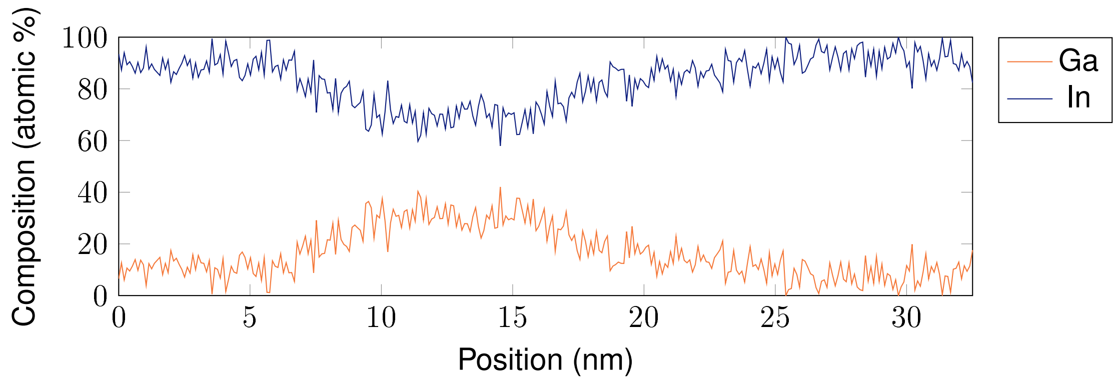
Tin is a n dopant [157] that has previously been used in the InP layer of successful TASE-grown devices [60]. Its metal-organic precursor, tetraethyl tin (TESn), was available in the MOCVD system, and therefore a growth run was carried out. The deposition recipe is shown in Figure 4.27(A), and features a standard step sequence, consisting of a 15 s long step for the InGaAs nucleation layer, followed by a 450 s-long i InP stabilisation layer. The following superlattice deposition loop contained a 15 s-long InGaAs well deposition step followed by the 7 s TBAs / 10 s TBP hold step. The barrier n-InP deposition step was 100 s in duration and was followed by a 20 s TBP hold step.

Figure 4.27(B) shows the BF-STEM image of a 30° FIB cross-section of a nanowire grown with the recipe shown in Figure 4.27(A). The silicon seed is on the left of the image, and the III-V material is at its centre enclosed by the top SiO_2 template and the bottom buried oxide layer. Its surface appears to be formed by a $\{1\,1\,1\}$ facet at the top and another, likely high-indexed, facet at the bottom. Despite this defect, initial nucleation was successful and the n-InP stabilisation layer formed a single $\{1\,1\,1\}$ growth front, reflected in its evolution by the shape of the InGaAs quantum wells.

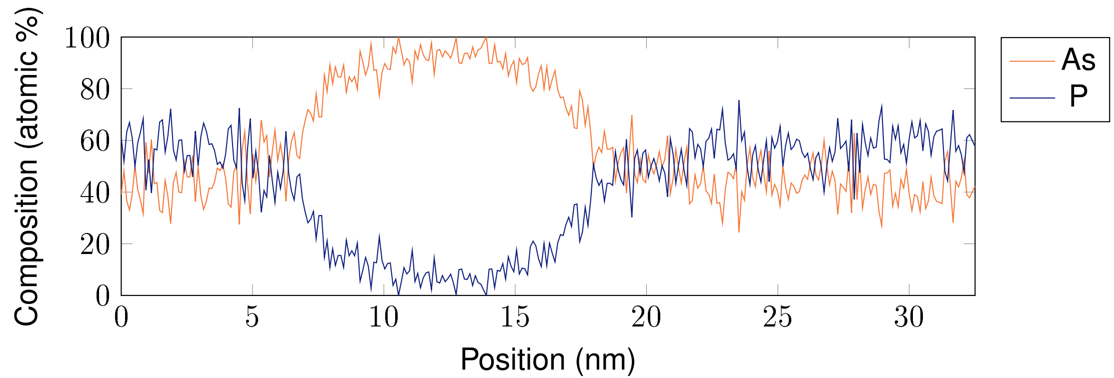
Figure 4.27(C) shows a high-resolution BF-STEM image of the first quantum well. The image does not show any particular difference from those seen for previous samples. Rotational twin planes are present throughout the whole sample, including the 10 nm-thick quantum wells.

EDS analysis The TESn / (TESn + TMIn) ratio loaded in the reactor was 0.037, way too low to be reflected in EDS spectra. Regardless, the composition graphs of Figure 4.28 raise another point of interest. Figure 4.28 shows the composition of the III-V nanowire as a function of the position struck by the electron beam of the STEM as it moved across the quantum well shown in Figure 4.27(C), from left to right. The noise level of the spectra is around 15 %.

The III group element composition graph of Figure 4.28(A) reveals a $In_{0.75}Ga_{0.35}As$ composition for the quantum well. However, the V group element composition graph in Figure 4.28(B) shows very high alloying for the barrier layers, which have a real composition of $InP_{0.6}As_{0.4}$. The file containing the growth recipe was double-checked to ensure that the TBAs flow was cut off during InP deposition, and it was found that the recipe was programmed



(A) EDS linescan: III atomic percentage vs position.



(B) EDS linescan: V atomic percentage vs position.

Figure 4.28: EDS linescan compositional data (in atomic percentage) for the (A) III group elements and (B) V group elements across the first quantum well of sample 9 (shown in Figure 4.27(C)).

correctly. This left a mystery as to the origin of the high arsenic concentration found in this and other EDS spectra of this sample. The likely explanation is an equipment malfunction.

However, this finding does show that it is not only a pure phosphide layer that can stabilise a single $\{1\,1\,1\}$ growth front within a TASE template, but also phosphide arsenides. This result shows that tin has no negative effect on growth with a single-facet growth front, making it a good dopant for device applications.

4.7 Discussion and future developments

This chapter explored a variety of MOCVD-grown TASE structures with various layer thicknesses and semiconductor materials. The $\{1\,1\,1\}$ single growth front stabilisation growth regimen was confirmed to be an attractive methodology for controlling defects and material composition. Initially limited to a high V-III ratio InP, it was shown that a high V-III ratio InAsP can also provide the same $\{1\,1\,1\}$ stabilisation effect.

This growth methodology was easy to apply to the new substrate, the growth rates on the

$\langle 1\,1\,0 \rangle$ substrate differed from those recorded for the $\{0\,0\,1\}$ SOI wafer but remained comparable. Small fluctuations in growth rate were observed from one sample to the other but remained within the same value ranges within both InP and InGaAs.

The most significant impact on growth rates was observed in samples grown in a competitive environment. The presence of many parasitic crystals deeply affected the growth of TASE nanowires and the growth regimen within the template. The effective V / III ratio alteration in this environment was enough to cause the wire to lose its single-faceted growth front. This effect should be considered when attempting dense integration of TASE structure, especially if they differ in shape and size.

As expected, the photoluminescence analysis of the InGaAs QWs showed dependence on their size and composition. Importantly, it was shown that the signal originating from $\{1\,1\,1\}$ single-facet heterointerface quantum wells was sharper than that of a sample with a large multi-faceted InGaAs nucleation layer.

Another important achievement shown in this chapter was the growth of a single crystal from multiple nucleation points, resulting in a crystalline quality comparable to that of single-nucleation nanowires. This was shown to be a reproducible process in Figure 4.13. This result was made possible by the highly controlled growth regimen created during the high V-III ratio deposition of InP, resulting in a layer-by-layer growth of $\{1\,1\,1\}$ atomic planes. Further yield calculations for this multi-seed single structure and a study of their performance as a function of size are interesting research avenues.

This layer-by-layer growth was again observed in 4 atomic layers thin InGaAs growth. This experiment pushed growth to the limits of what MOCVD deposition can achieve and close to the territory of ALD, revealing the merit of the growth front stabilisation method and its limitations. The heterointerfaces were shown to be finite and function as transition areas between two III-V materials, and to have a width greater than 2 nm. The strain analysis of a lattice-mismatched InAs in a InP matrix showed a low change in the lattice constant, indicative of local strain being present in the InAs layer. Further optimisation of the growth recipe for the deposition of GaAs and GaSb in thin layers will complement these findings and expand the knowledge base past the lattice-matched InP-InGaAs case.

The presence of tin precursor in doping concentrations in the reactor did not affect the stabilisation of the $\{1\,1\,1\}$ facet. Therefore, this element is an ideal candidate for further electrical analysis concerning the *n*-doping of structures grown with the growth stabilisation method. Further investigation to find a *p*-dopant that also does not interfere with the facet-stabilising effect would complete the doping toolset for p - i - n structures.

Although quantitative data on the reliability of this deposition methodology was presented, a quantitative study exploring the yield of the growth stabilisation method is a strong next step in demonstrating its value.

Chapter 5

Growth yield analysis

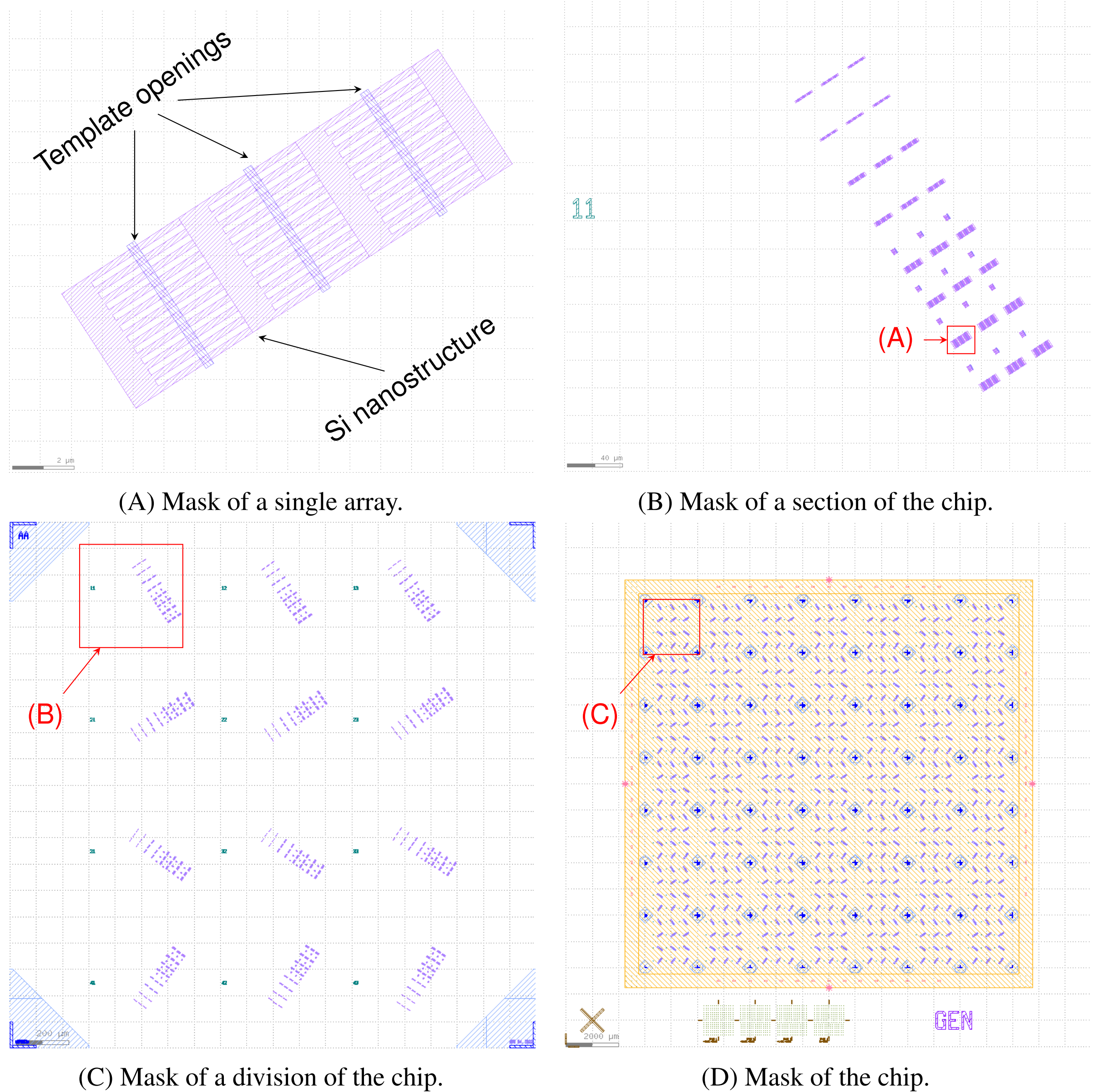
Chapters 3 and 4 showed how the $\{1\,1\,1\}$ facet stabilisation method affects the internal composition and morphology of nanowires grown with the template assisted selective epitaxy (TASE) process. These results, obtained on $(0\,0\,1)$ and $(1\,1\,0)$ silicon on insulator (SOI) wafers with different device layer thicknesses, showed reliable growth rates and structural results. However, a quantitative analysis of this growth method's yield is needed to understand its success rate better.

This chapter presents the research my co-authors and I carried out and published in [2, 3]. The structure and appearance of the surface of samples 6 and 7 is described. The assumption of correlation between the internal structure seen with scanning transmission electron microscopy (STEM) and the top-down low-resolution data collected with scanning electron microscopy (SEM) is explained. A statistical analysis that compares the wires between defect-free and defective and evaluates the impact of parasitic crystal growth is presented, involving 15 840 wires equally divided between the two above-mentioned samples.

The second half of the chapter focuses on using the dataset containing 240 SEM images as input data for the supervised training of a machine learning algorithm for automatically classifying wires. Using digital image processing, a strategy is presented to isolate each single wire from the 240 arrays. The ability to create single-wire images enables the use of a lightweight image classifier. Finally, the performance of the splitting algorithm and the resulting classifier are examined, together with some improvements to the former.

5.1 Sample characteristics

The yield analysis will focus on samples 6 and 7, grown on $(1\,1\,0)$ SOI wafers, which were introduced in Sections 4.4 and 4.5.1, respectively. In particular, the yield calculations will involve single nucleation nanowires grown in arrays like those shown in Figure 4.2(B). These structures supported 66 nucleation sites each and were grown with 4 template widths: 70 nm, 140 nm,



(A) Mask of a single array.

(B) Mask of a section of the chip.

(C) Mask of a division of the chip.

(D) Mask of the chip.

Figure 5.1: Mask used for the EBL and optical lithography exposition of $(1\,1\,0)$ substrates. Different colours denote different mask layers. The in-plane $\langle 1\,1\,0 \rangle$ direction runs parallel to the bottom margin of the images. (A) shows a single array of the kind illustrated in Figure 4.2(B). (B) shows a section of the chip, marked by the number 11, containing 24 arrays, 6 for each template width (70 nm, 140 nm, 210 nm, and 280 nm). 12 merge structures are also visible. (C) shows a division of the chip, containing 12 sections. (D) shows the full mask of the chip, containing 49 divisions. The sample area measuring 1.5 cm × 1.5 cm is highlighted in yellow.

210 nm, and 280 nm.

5.1.1 Lithography masks

Figure 5.1 shows the digital mask that was used during the TASE process in the electron beam lithography (EBL) definition of markers, micro-structures, and template openings and to fabricate the optical lithography mask used to create the marker protections, as explained in Section 2.4. Figure 5.1(A) shows how a single 66-nanowire array looks like in the EBL mask. This single array is placed in a section, shown in Figure 5.1(B), of the chip, together with 23 others, totalling 6 array per nanowire size per section. Sections are further grouped in divisions, one of which, marked AA, is shown in Figure 5.1(C). Each division contains a total of 12 sections. Each of the sections is orientated so that the nanowires in each array and merge structure are closely aligned with one of the in-plane $\langle 1\,1\,1 \rangle$ directions, or 20° misaligned from them. This results in a series of fishbone patterns across the mask used to pattern the entire chip, shown in Figure 5.1(D). The 1.5 cm × 1.5 cm sample area of each chip, highlighted in yellow, contains 49 divisions, resulting in a total of 1 254 528 nanowire single nucleation sites (therefore, without taking into account the merge structures).

Each section is identified by a number, in the case of the one in Figure 5.1(B) it is 11, and two letters that, in turn, identify the division of the mask in which it is found. Therefore, the naming convention defines, in order, the row and the column of the division within the chip, starting at the top left of Figure 5.1(D), and the row and column of the section within the division, starting at the top left of each division. In this example, AA11 is the top-leftmost section in the entire chip.

A STEM analysis of every nanowire is impossible due to the damage caused by focused ion beam (FIB) lamella preparation to the area immediately surrounding each cut-out. Still, even if a single cut per array was performed, a total of 19 008 lamellae would have to be manufactured and analysed per sample. This task is too time-consuming and resource-intensive to be viable. Therefore, a different approach must be found to tackle the problem of yield calculation.

5.1.2 Internal morphology and reproducibility in TASE nanowires

Stabilisation of a single $\{1\,1\,1\}$ facet for the internal superlattice heterointerfaces of the nanowires was observed in all phosphide-arsenide samples since it was first achieved in sample 3 (Section 3.4). Eliminating the ambiguity of facet selection due to the substrate $(1\,1\,0)$ discussed in Section 4.2 limits the outcome of the tetramethylammonium hydroxide (TMAH) etching to a single facet seed, a condition which is achieved reliably since sample 4. Similarly, from sample 4 onwards, the seed facet and the end facet of the wires have been parallel or showed a misalignment of 3° in sample 6 (Section 4.4). Finally, with the minimisation of indium-gallium arsenide (InGaAs) nucleation layer thickness introduced in sample 5 (Section 4.3) all important material

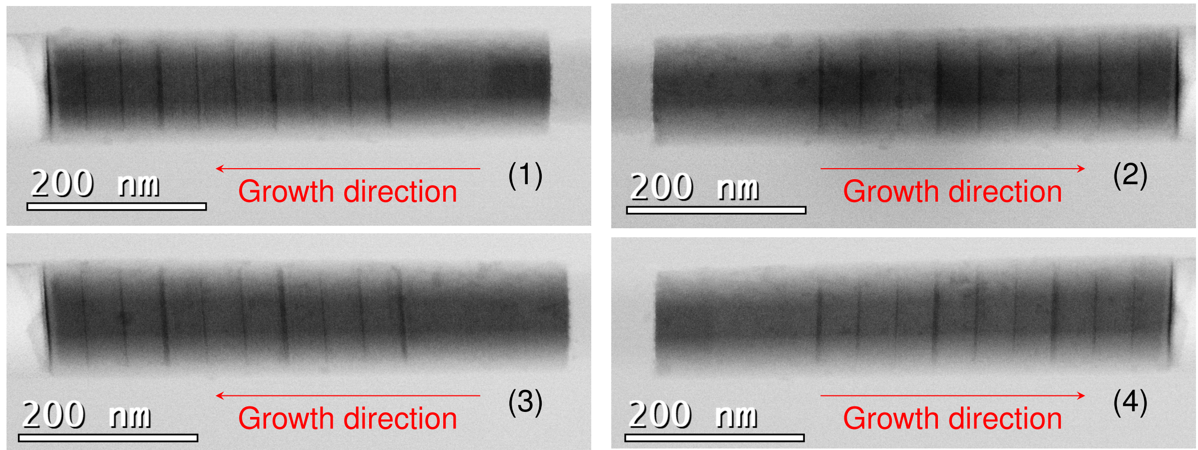


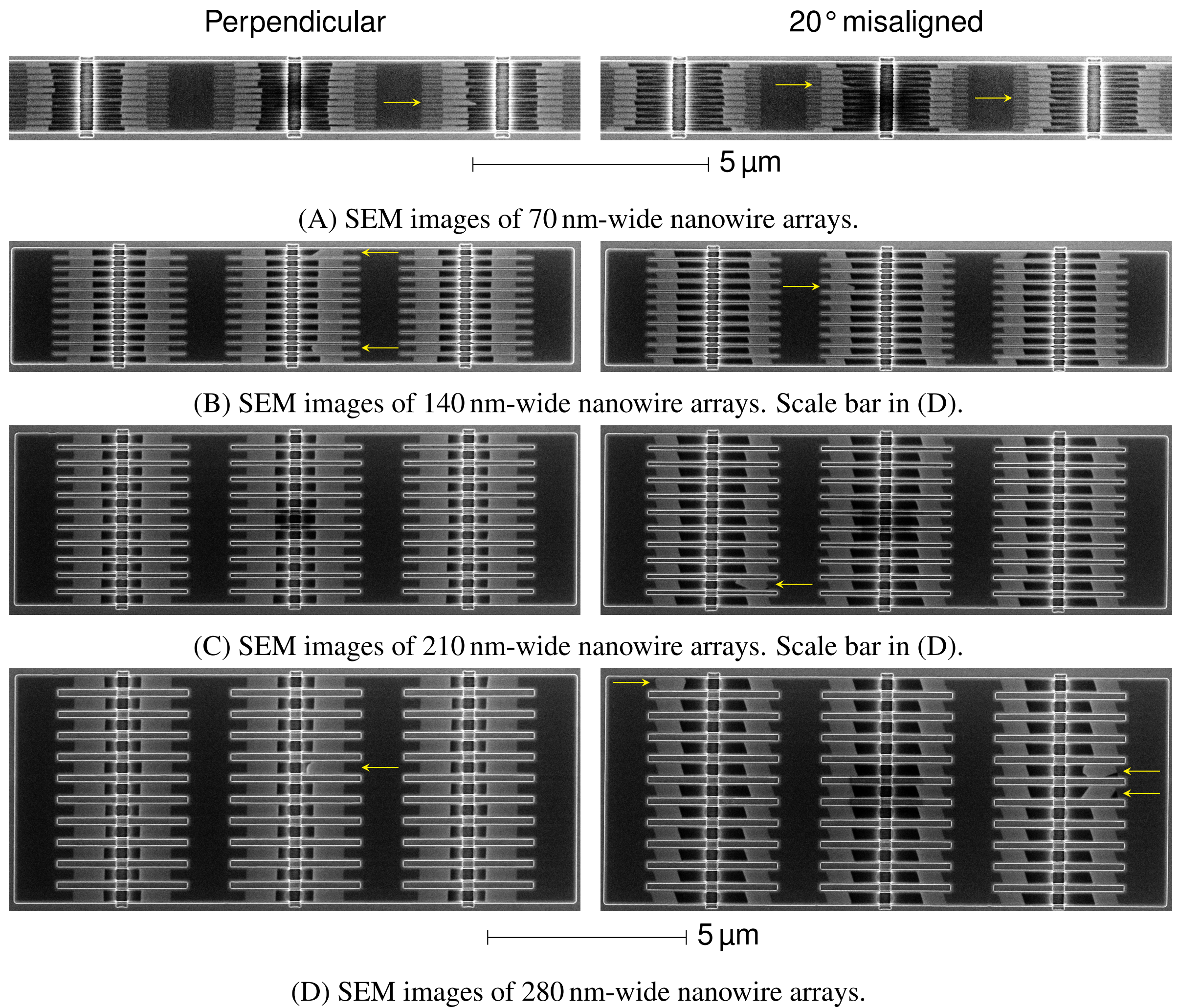
Figure 5.2: Four BF-STEM images of different nanowires from the lamella cut for sample 7. They all share similar growth rates and internal structures.

layers are heterointerfaced with a single $\{1\,1\,1\}$ facet.

Figure 5.2 shows four BF-STEM overview images of the same number of nanowires from the lamella cut from sample 7. These images confirm the observations made in the previous paragraph regarding the relation between silicon (Si) / III-V semiconductor interface and the nanowire end-facet shapes mirrored in all important interior phosphide-arsenide heterointerfaces. An approximation can therefore be made by inferring that if the silicon seed consists of a single $\{1\,1\,1\}$ facet, the III-V material fully covers it, and the end-wire surface is a single $\{1\,1\,1\}$ facet parallel to the silicon seed the internal morphology also developed as-desired, with $\{1\,1\,1\}$ single-facet heterointerfaces. Therefore, these metrics can be used to define a defect-free wire.

These specifications do not require a full STEM analysis. Instead, a SEM survey of the arrays in the sample is sufficient to assess the growth yield. One such survey, resulting in an open access dataset [13], was carried out on samples 6 and 7. Figure 5.3 shows eight images of the arrays of sample 6 taken from this dataset. A first distinction can be made by "Perpendicular" wires, so-called because the heterointerfaces in defect-free nanowires are perpendicular to all four template walls, and 20° misaligned wires, which owe their name to the tilt of the template channels from the $\langle 1\,1\,1 \rangle$ direction.

The dataset was collected manually using the SEM beam of the dual-beam SEM - FIB tool. Due to project time constraints, sampling became necessary to gather a full suite of images representative of the 19 008 arrays. Five sections were selected in each chip, mostly at random. However, for sample 7, a perpendicular and a 20° misaligned section in the AA division were selected to ensure a representation of the border divisions of the chip. Another difference between the two samples is that while for sample 6 sections were randomly drafted and changed for each of the five positions, for sample 7 two division was randomly selected, within which two more sections were imaged. The fifth and final perpendicular section was once again randomly chosen. These sections are reported in Table 5.1. Three parallel and two 20° misaligned sections were imaged for both samples.



(A) SEM images of 70 nm-wide nanowire arrays.

(B) SEM images of 140 nm-wide nanowire arrays. Scale bar in (D).

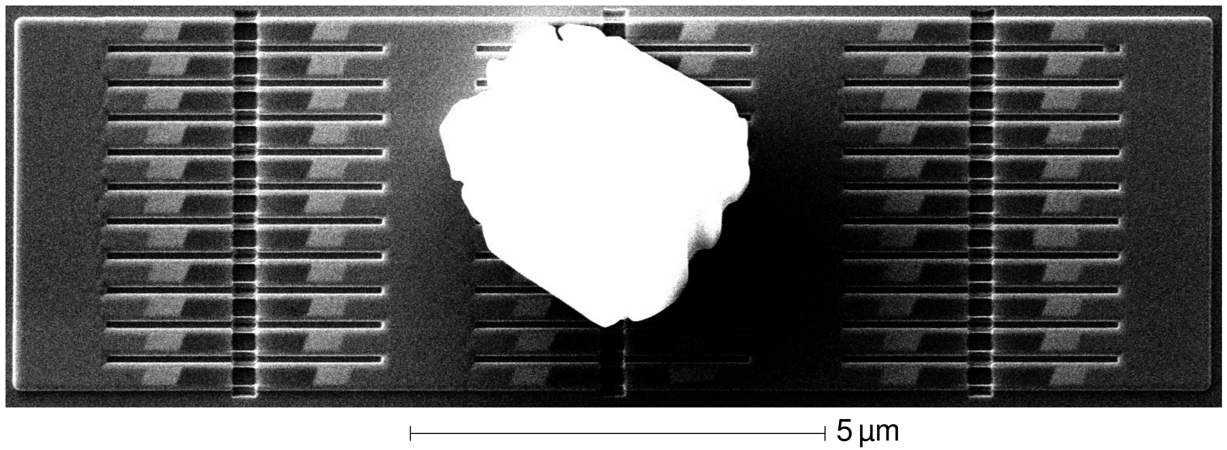
(C) SEM images of 210 nm-wide nanowire arrays. Scale bar in (D).

(D) SEM images of 280 nm-wide nanowire arrays.

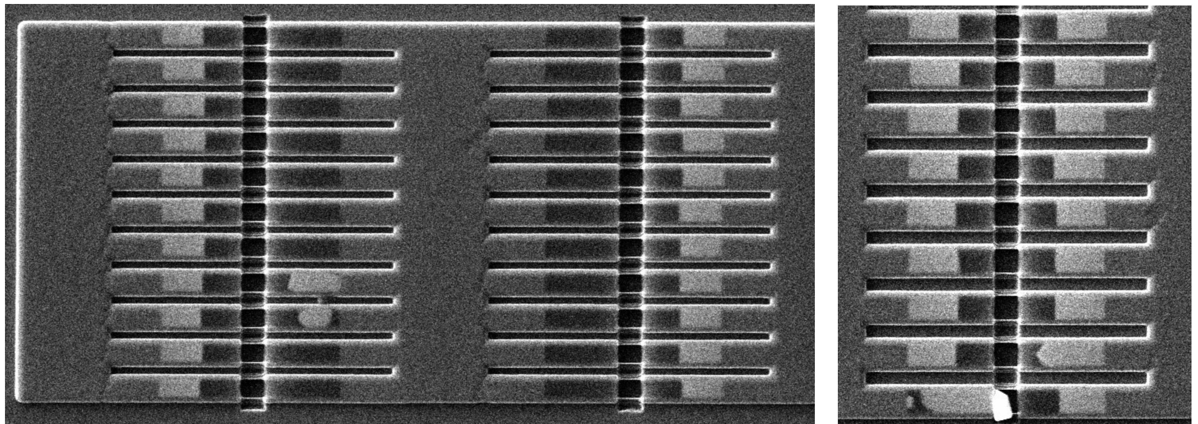
Figure 5.3: SEM top-view images of III-V nanowire arrays with defective wires marked by yellow arrows. (A), (B), (C), and (D) show both perpendicular and 20° misalligned arrays with template widths of 70 nm, 140 nm, 210 nm, and 280 nm, respectively. This Figure was adapted from the work of Brugnolotto *et al.* [2] under the terms of the CC BY 4.0 licence [130].

Table 5.1: Randomly selected sections for the array dataset.

	Sections				
Sample 6	BB13	CD22	DE42	FB13	GG31
Sample 7	AA32	AA41	DE11	DE22	FC11



(A) Parasitic growth covering some growth sites in sample 7.



(B) Un-nucleated sites in sample 7.

(C) Template nucleation.

Figure 5.4: Arrays from sample 7 presenting different types of defects. The scale bar for all three images is in (A). (A) shows a parasitic crystal hiding numerous nucleation sites from view. (B) shows several nucleation sites where nucleation has not occurred. Two sites also contain defective wires. (C) shows a template with nucleation on the Si seed, resulting in a small III-V particle, while the larger wire nucleated on the SiO_2 wall and grew out of the template. This Figure was adapted from the work of Brugnolotto *et al.* [2] under the terms of the CC BY 4.0 licence [130].

This means that 240 arrays containing 15 840 nucleation sites were imaged. This number represents 0.63 % of the wires in the two chips. As such, it can be helpful to provide a first estimate of the yield, and constitutes a dataset from which automated yield calculation methods can be built on.

5.1.3 SEM-observable defects in TASE nanowires

Defective wires were marked with yellow arrows in the nanowire arrays of Figure 5.3. All these defective wires can be detected by looking at the wire-end interface. None of the wires mirroring the defective wires are defective. Each defective wire is isolated, having no immediate defective neighbour, except for two. Some of the defective wires also have partially covered seeds, as is

most evident in the two neighbouring 280 nm 20° misaligned array. However, unideal nucleation is not the only reason for defective growth, as seen in the 140 nm and 280 nm perpendicular wires, which fully cover the silicon seed.

The length of the nanowires does not change significantly with the change in width of the TASE templates, as can be seen by comparing the lengths of the nanowires in Figure 5.3(A) with those of the nanowires in Figure 5.3(B), 5.3(C), and 5.3(D), once the slight magnification used for presentation purposes in Figure 5.3(A) is taken into account. Therefore, compared to their neighbours, abnormally long or short III-V material segments in some nucleation sites can indicate undesired defects in the wire's internal structure.

Loss of growth selectivity can negatively affect the yield of defect-free nanowires. In Figure 5.4(A), the large parasitic crystal in the centre of the image hides many nucleation sites from view. Parasitic crystals often grow in places where impurities or geometric features on the surface of the chip provide unwanted nucleation sites. The lack of nucleation at several growth sites shown in Figure 5.4(B) can be considered another "defect" because it does not produce a nanowire where one is expected. Lack of nucleation occurs when a SiO_2 layer covers the silicon seed and, therefore, is caused by hydrofluoric acid (HF) not entirely stripping this passivating layer or being unable to reach it due, for example, to the presence of a bubble on the chip surface during the pre-growth HF dip. In Figure 5.4(B), this defect occurs in nucleation sites that share their template opening with defect-free nanowires, making the bubble hypothesis less likely. Figure 5.4(C) shows a growth site where nucleation co-occurred on both the silicon seed surface and the SiO_2 inner template wall. The crystal nucleated on the silicon surface was quickly cut off from the precursor supply when the other crystal grew to fill the width of the template. The defective crystal then grew faster than the other crystals around it due to its starting point being closer to the template opening and the random crystalline orientation resulting from the nucleation on the template wall. Had the undesired nucleation occurred closer to the opening of the template, it could have resulted in a parasitic growth similar to that in Figure 5.4(A).

5.2 Yield study

The 240 array images discussed in the previous sections were manually examined. The resulting count revealed that 14 660 wires out of 15 840 nucleation sites grew defect-free, therefore satisfying all the criteria explained so far. This results in a total yield of 92.55 % [2]. The yield can be broken down between sample 6 and 7: for sample 6, 91.59 % of the wires, or 7254 out of 7920, grew without visible defects, and therefore assumed to be defect-free, a figure that grows to 93.51 %, or 7406 out of 7920 for sample 7. Despite InP-lattice-matched arsenide layers being the only type of heterolayer in sample 6 and mismatched indium arsenide (InAs) layers being present in sample 7, the total yield is very similar for both samples, showing that lattice mismatch had no impact on this metric.

Table 5.2: Overview of the distribution of defect types for samples 6 and 7 [2].

	Defect categories and occurrence						
	Wrong Facet	Hidden by Parasitic	Oxide Nucleated	Seed Exposed	Long	Short	Ungrown
Sample 6	164	230	2	0	5	204	61
% of category	*44.6 %*	*47.2 %*	*11.8 %*	*0 %*	*62.5 %*	*98.8 %*	*75.3 %*
Sample 7	204	257	15	8	3	7	20
% of category	*55.4 %*	*52.8 %*	*88.2 %*	*100 %*	*37.5 %*	*1.2 %*	*24.7 %*
Total	**368**	**487**	**17**	**8**	**8**	**211**	**81**

Table 5.3: Overview of the distribution of defect types between perpendicular and 20° misaligned sites [2].

	Defect categories and occurrence						
	Wrong Facet	Hidden by Parasitic	Oxide Nucleated	Seed Exposed	Long	Short	Ungrown
Perpendicular	208	315	7	4	5	5	20
% of category	*56.5 %*	*64.7 %*	*41.2 %*	*50 %*	*62.5 %*	*2.4 %*	*24.7 %*
20° misaligned	160	172	10	4	3	206	61
% of category	*43.5 %*	*35.3 %*	*58.8 %*	*50 %*	*37.5 %*	*97.6 %*	*75.3 %*
Total	**368**	**487**	**17**	**8**	**8**	**211**	**81**

The 1180 defective wires are broken down between the two samples and by defect category in Table 5.2. The seven defect classes are: "wrong facet", which comprises the wires where the end interface is not parallel to the $\{1\,1\,1\}$ seed interface, "hidden by parasitic", counting the nucleation sites that are covered by a parasitic crystal and therefore not visible, "oxide nucleated", which counts the wires that nucleated on the template oxide, "seed exposed" wires have the correct end surface but did not fully cover the seed surface, "long" and "short" wires are only defective in terms of length when compared to those around them, and "ungrown" wires, or lack of wires, counts the nucleation sites that did not experience growth.

The three most numerous categories for the total number of defects are "hidden by parasitic", "wrong facet", and "short", with totals of 487, 368, and 211, respectively. The other categories are one order of magnitude lower. The category "hidden by parasitic" is different from the others in the sense that a single defect hides multiple wires, close to 15, or 14.87 on average, from view, as shown in Figure 5.4(A). As such, the status of the hidden wires is unknown. If these hidden nucleation sites are ignored for yield calculation, the total number of surveyed sites falls to 15 379, while the number of defect-free wires remains unchanged. Under this approximation, the total yield rises by 2.77 % to 95.32 %.

Data on defective wires can also be divided between perpendicular and 20° misaligned growth sites, as shown in Table 5.3. The total number of perpendicular growth sites surveyed is 9504 (60 % of the total): higher than the number of 20° misaligned sites, which is 6336 (40 % of the total). This is caused by three out of five sections containing perpendicular growth sites for

Table 5.4: Overview of the distribution of defect types between perpendicular and 20° misaligned sites in sample 6 [2].

	Defect categories and occurrence						
	Wrong Facet	Hidden by Parasitic	Oxide Nucleated	Seed Exposed	Long	Short	Ungrown
Perpendicular	81	170	1	0	4	0	0
% of category	*49.8 %*	*79.9 %*	*50 %*	-	*80 %*	*0 %*	*0 %*
20° misaligned	83	51	1	0	1	204	61
% of category	*50.6 %*	*22.1 %*	*50 %*	-	*20 %*	*100 %*	*100 %*
Sample total	**164**	**230**	**2**	**0**	**5**	**204**	**61**

both samples. As a result, the total number of defects in the perpendicular sections is expected to be higher if the same possibility of defective wire presence is expected. However, suppose the presence of a tilted seed surface is expected to be a disadvantage for the growth of defect-free wires. In that case, this should be reflected in an equal or higher number of defective wires for the misaligned sites.

A first count of the total number of defective wires points to this conclusion, with 564 (47.8 % of the total) defective wires for the perpendicular growth sites and 616 (52.2 % of the total) for the 20° misaligned sections. However, when breaking down the defects into each category, it becomes apparent that a third of all defects in the 20° misaligned growth sites are in the short category, which is two orders of magnitude larger compared to the perpendicular growth sites. This was caused by the nucleation sites of section GG31 in sample 6 presenting numerous nucleation and growth issues, reflected in the higher number of short and ungrown wires. This could be ascribed to the different orientations of the silicon seed but could just as easily be due to the surface characteristics of the seed, such as residual oxide cover, or to the flow of the precursor over the sample, independent of geometry.

Four of the other five categories closely follow the expected defect ratios between the two types of nucleation sites, which comprise the other two categories with more than 100 defective wires. The presence of parasitic crystals is purely stochastic, and given that they can vary in size, the 64.7 % / 35.3 % split in this category is expected. However, the split in the "wrong facet" category is the most indicative of the actual difference in the performance of the facet stabilisation method, as it concentrates on analysing the relationship between the shapes of the seed and end-wire interface. This 56.5 % / 43.5 % split denotes a slight prevalence of defective wires for the 20° misaligned sites, but remains close to the 60 / 40 split of the sample sizes.

5.2.1 Growth yields of wires containing lattice-matched heterolayers

Table 5.4 shows a breakdown of the defective wires surveyed on sample 6 between perpendicular and 20° misaligned growth sites and defect category. Sample 6 contained wires with twelve lattice-matched InGaAs quantum wells. As discussed in the previous section, the total growth

Table 5.5: Overview of the distribution of defect types between perpendicular and 20° misaligned sites in sample 7 [2].

	Defect categories and occurrence						
	Wrong Facet	Hidden by Parasitic	Oxide Nucleated	Seed Exposed	Long	Short	Ungrown
Perpendicular	127	145	6	4	1	5	20
% of category	*62.3 %*	*56.4 %*	*40 %*	*50 %*	*33.3 %*	*71.4 %*	*100 %*
20° misaligned	77	112	9	4	2	2	0
% of category	*37.7 %*	*43.6 %*	*60 %*	*50 %*	*66.7 %*	*28.6 %*	*0 %*
Sample total	**204**	**257**	**15**	**8**	**3**	**7**	**20**

yield for this sample is 91.59 %. The singular growth yields for the perpendicular and misaligned sites in this sample are 94.84 % and 86.71 %, respectively. This 8.13 % difference is driven mainly by section GG31, which is responsible for all of the "short" and "ungrown" wires in this sample.

Aside from the contribution coming from section GG31, this sample mainly presented "wrong facet" and "hidden by parasitic" defective wires. The latter category shows a very high imbalance compared to the expected 60 / 40 distribution given by the random nature of parasitic nucleation. A significant contribution to this figure comes from section BB13, where 96 templates were covered by parasitic growth: this is 19.7 %, or close to a fifth, of the total number of templates covered by parasitic growth in a single sector, which itself represents a tenth of the data. On the other hand, the likelihood that a wire develops defects is much more closely matched between the two types of nucleation sites while being slightly higher for the 20° misaligned sample.

5.2.2 Growth yields of wires with lattice-mismatched heterolayers

The statistics that highlight the distribution of each category of defects between seed types in sample 7 are shown in Table 5.5. Sample 7 contains strained arsenide layers in the form of InAs quantum wells in an InP matrix as well as some close to lattice-matched InGaAs layers. The total growth yield for this sample was 93.51 %, higher than for the previous sample, which only contained unstrained interfaces. This is mainly due to the presence of many nucleation issues in section GG31 of sample 6. Thus, the main factors affecting the growth yield are more related to surface treatment issues than to the actual growth recipe loaded in the reactor. The growth yield for the perpendicular and 20° misaligned are very close at 93.73 % and 93.75 %, respectively.

For this sample, the categories "wrong facet" and "hidden by parasitic" exceed 200 wires each, in total, closely following the 60 / 40 distribution given by a stochastic process. The most unbalanced category consists of the 20 ungrown wires for the perpendicular growth sites. These all originate from a single array in section AA41, and are shown in Figure 5.4(B). Therefore, the analysis of this sample also confirms that, aside from some discrepancies closely related to

surface treatment issues, the growth yield follows the expected 60 / 40 distribution.

In conclusion, the presence of strained arsenide heterolayers does not significantly impact the total growth yield, generating a difference of only around 1.92 % in its favour. However, looking at the metric that is more closely related to the growth dynamic, wires growing with the wrong end facet, a stronger impact can be seen. Table 5.2 shows a 10.8 % difference in this metric, ammounting to a total of 40 defective nanowires. This could mean that, when nucleation issues are resolved, the presence of strain in the nanowire can affect the overall growth yield.

5.3 Image processing for yield calculation

After the manual analysis carried out on the 15 840 wires shown in the 240 SEM images dataset [13], it became clear that carrying out such a task manually for each sample would consist in a lot of tedious and time-consuming work. To retain the ability to calculate the yield information on TASE nanowires, the dataset could be processed to become the input data for a machine learning algorithm to automatically classify each wire between "defective" and "non defective".

The code for the digital image processing was written by me, but I would like to acknowledge the important contribution from Preslav Aleksandrov who first proposed the wire splitting approach with the use of parsing kernels illustrated in the next pages. The code described in this section is available in an open-source repository [14]. The approach selected for this automation was to train a simple classifier with supervised training on images of a single wire extracted from the images of the 240 array. Given the choice of supervised training, manual labelling of 15 840 wires across 240 images had to be carried out. Then, the 240 images had to be digitally split into single wires, half of which were mirrored to maintain the same seed-wire-empty template left to right sequence in each resulting image.

5.3.1 Image preprocessing

The open-source software and Python [158] library `labelme` [159] was used to generate the labelling data for each array image. A reduced subset of label classes was employed compared to the manual analysis in the previous section. They distinguished between parallel and tilted wires, which describe the orientations of the templates in which the wires grew and corresponded to the "Perpendicular" and "20° misaligned" categories of the previous section. These two types of wires were further subdivided into two classes by adding "defect" or "perfect". A fifth class was created to represent parasitic crystals because they are a very different kind of defect and should, therefore, be easily identified by any classifier.

These five classes, plus a sixth generated according to the outcome of the digital wire-splitting algorithm, are used to label the data that form the input for the supervised classifier. Examples of what each wire image looks like are provided in Figure 5.5 complete with their

Table 5.6: Class encodings for the training of the classifier [3].

Class	Parasitic	Wire Parallel Defect	Wire Parallel Perfect	Wire Tilted Defect	Wire Tilted Perfect	Null
Encoding	0	1	2	3	4	5

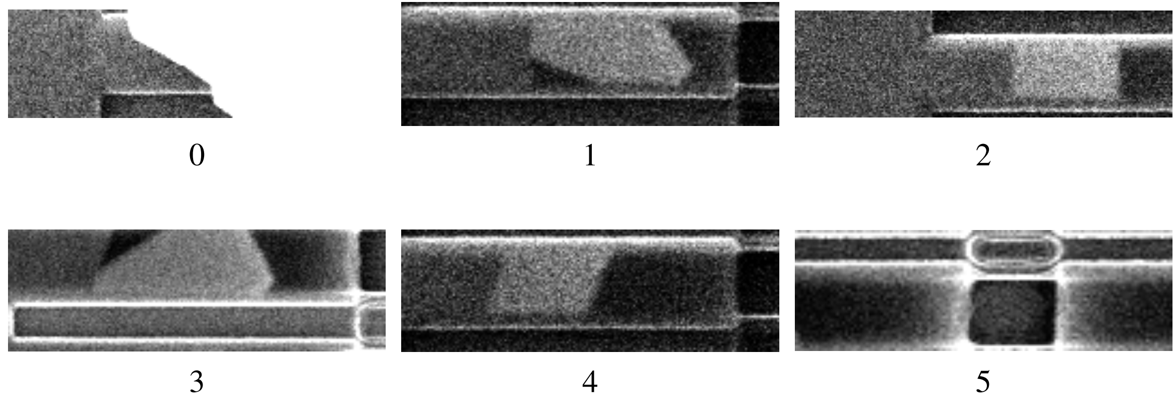


Figure 5.5: Examples of each class of wire [3]. The numbers below each image are the respective encodings, which can be interpreted from Table 5.6.

encodings, which are summarised in Table 5.6. At the end of the labelling process, each `.tiff` raw image will have a `.json` file containing the labels for the wires (and eventual parasitic crystals) it contains. These labels are stored as coordinate pairs describing the position of the vertices of the polygon drawn when labelling the object in the image, with a coordinate system based on the pixel coordinates in the image itself. These groups of coordinate pairs are associated with the manually assigned label describing the object. This `.json` file also contains a binary representation of the image that can be viewed with the `labelme` library.

Digital image splitting algorithm

The main challenge facing the creation of the input data set is to produce images of isolated nanowires from an image such as that in Figure 5.6. This particular image was captured with low contrast; other images, such as those seen in Figure 5.5 were captured under different acquisition settings. The variety of acquisition conditions makes it challenging to define hardcoded intensity levels to, for example, detect whether or not a wire is there and what shape it has.

However, a constant for all images is the magnification and orientation, plus or minus 1° or 2°, of the nanowire arrays. Another constant is the information panel at the bottom of the image. While useful for human interpretation of the image, this part of the image is not necessary for a machine. Given its regular nature, it can be easily removed from all images by cutting a constant number of pixel rows. The geometry of the nanowire array remains constant as well, varying only in vertical size, with minor fluctuations in position inside the image.

Figure 5.6 shows the concept for the initial cutting steps. The first cut, highlighted in orange, using hard-coded coordinates, excludes the information panel at the bottom of the image and the

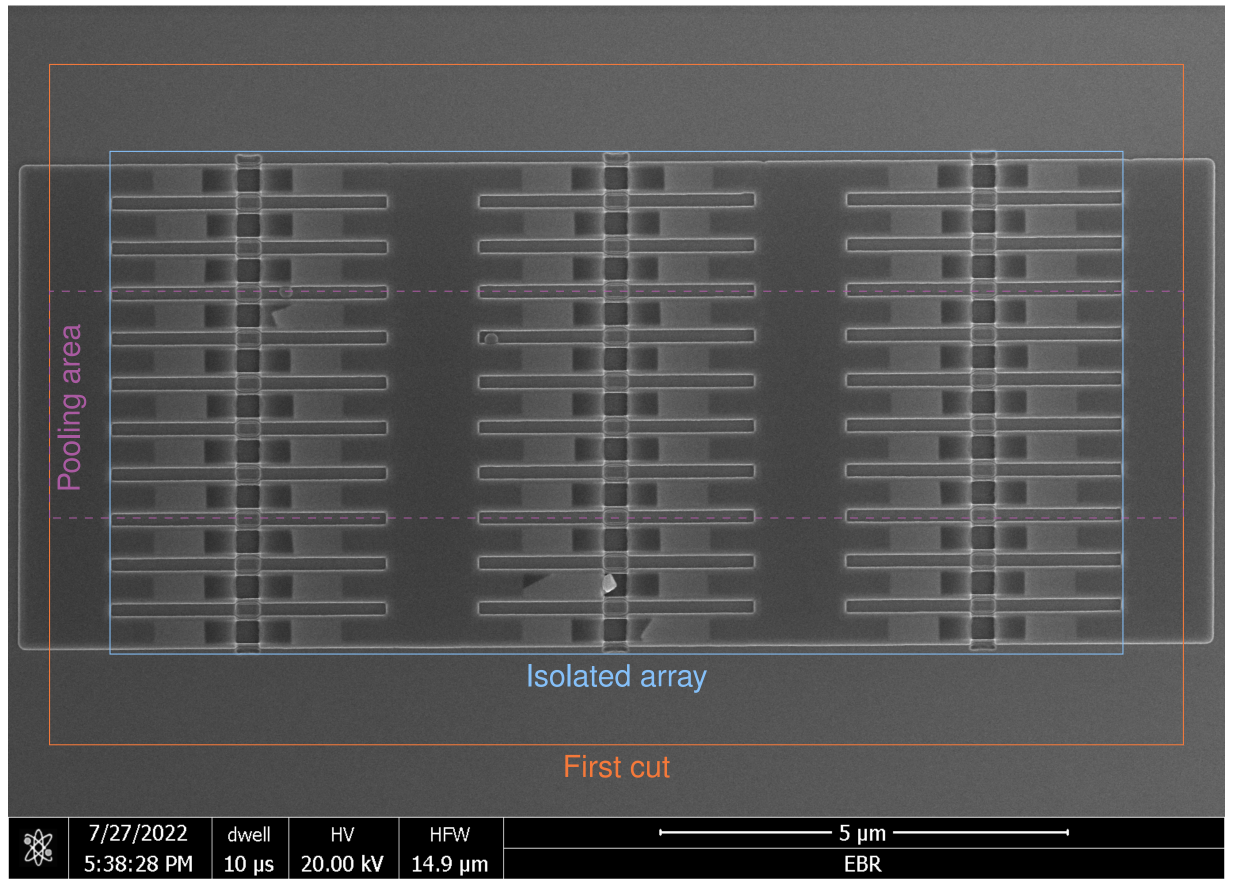


Figure 5.6: A raw SEM image of a nanowire array. This is an example of the starting state of the images in the unprocessed dataset, in particular, this image has low contrast. The cutting process is also shown with rectangles of different colours.

Figure 5.7: Simplified example illustrating the operation of the `max_pool` and `min_pool` kernels. This Figure was reprinted from the work of Brugnolotto *et al.* [3] under the terms of the CC BY 4.0 licence [130].

nanowire array's left and right side walls. The coordinates of the next cut are computed on the basis of the relative intensities within a specific pooling area, represented by dashed purple lines. After four such operations, one per each side of the nanowire array, only the image data within the blue rectangle remain, and the nanowire array is therefore isolated.

Keeping track of the coordinates of the vertices of each cut is essential to correlate the label data in the `.json` file to the data in the image itself. The splitting algorithm uses the binary representation of the raw image contained in the `.json` label file to create a `numpy` [160, 161] array populated by `uint8` values. Each value gives the intensity of a pixel as an 8-bit unlabelled integer, which varies from 0 to 255. Therefore, the resulting `numpy` array is the mathematical description of a black-and-white image. The data for all images are stored in its `numpy` array form in a variable inside a Python `class`, also containing its file name, label (once assigned) and coordinates relative to the raw image. These coordinates are kept updated throughout the image pre-processing steps.

The first hardcoded cut is performed by eliminating the first 100 and the last 200 `numpy` array rows and the first and last 50 `numpy` array columns. This operation eliminates the information panel at the bottom of the image and the bright lateral edges of the nanowire array, a step necessary to determine the exact cutting points. Figure 5.8 shows how the precise image-cutting concept illustrated in Figure 5.6 is implemented. First, a copy of the image is made, and its top and bottom thirds are cut to isolate the pooling area and exclude the two remaining edges of the nanowire array. A denoising algorithm from the `opencv` library [162, 163] was employed to eliminate pixels that, due to noise, might be too dark or too bright and, therefore, impact the detection of the correct edges with the pooling method.

The pooling method is based on two kernels parsing the `numpy` array and overwriting its values to highlight vertical edges. These kernels are called `min_pool` and `max_pool`. Aside from selecting either a minimum or maximum value, the implementation of the two kernels is identical. For brevity, the `max_pool` method will be discussed. Intensity values within a box 5 pixels tall and 2 pixels wide are considered, and the maximum value is selected. Afterwards, the box is moved by one pixel to the right, and the procedure is repeated. Therefore, there is a 1 pixel of horizontal overlap so that if none of the 5 new pixels has a higher value than the ones in the previous box, the last high value is carried over. This box is horizontally moved starting at the top left of the image and, once the end of the rows is reached, is moved back to the beginning of the row and moved down by 5 pixels. As a result, there is no vertical carryover of values. A simplified example of the operation of these two kernels, with differently sized boxes, is shown in Figure 5.7.

The resulting `numpy` arrays are visualised in Figure 5.8. Initially, the `max_pool` and `min_pool` operations were meant to identify the beginning and the end of the III-V segment. This is accomplished very well by the `min_pool` operation. Thick dark lines can be seen in the `min_pool` output starting at the position corresponding to the end of the leftmost III-V

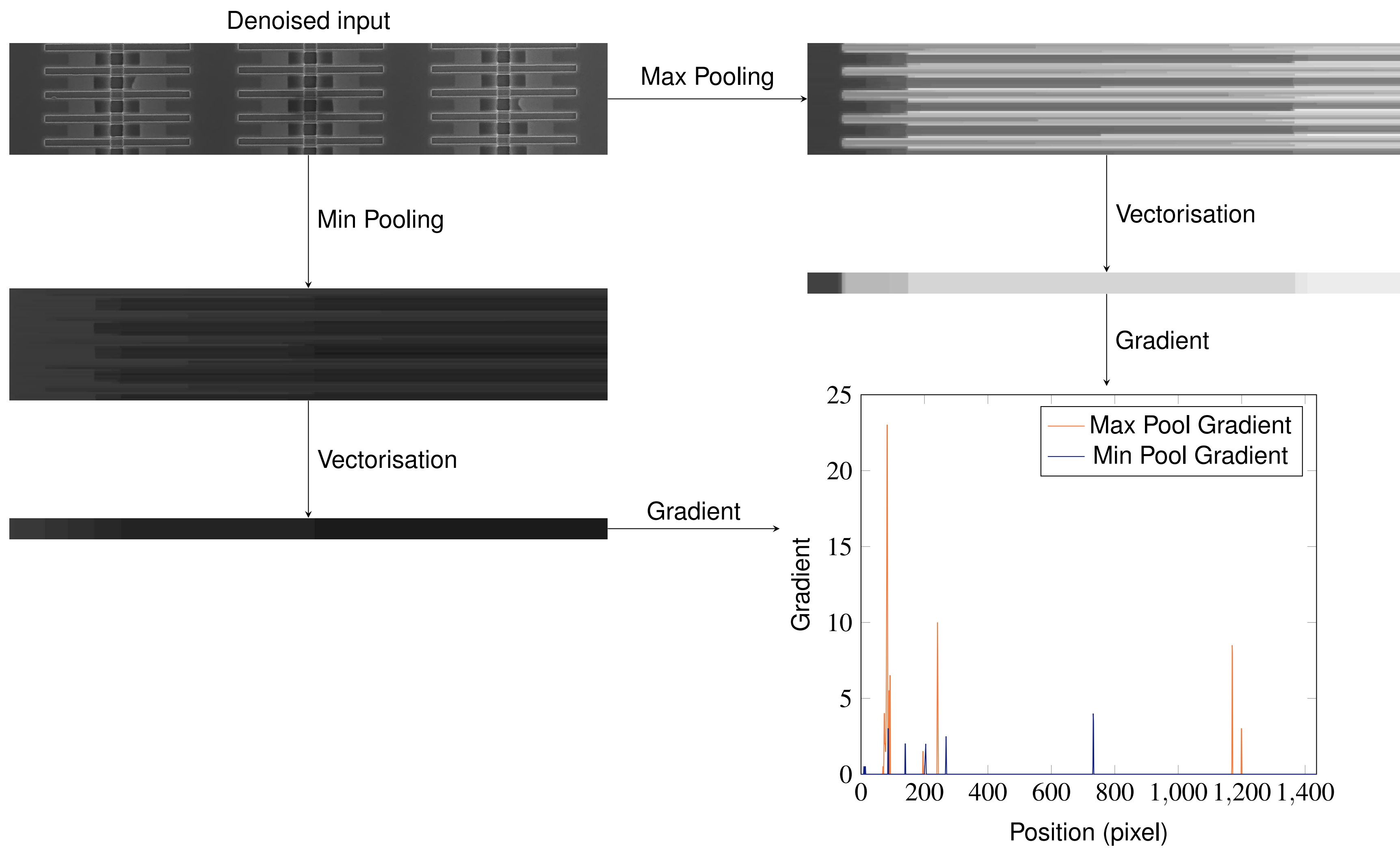
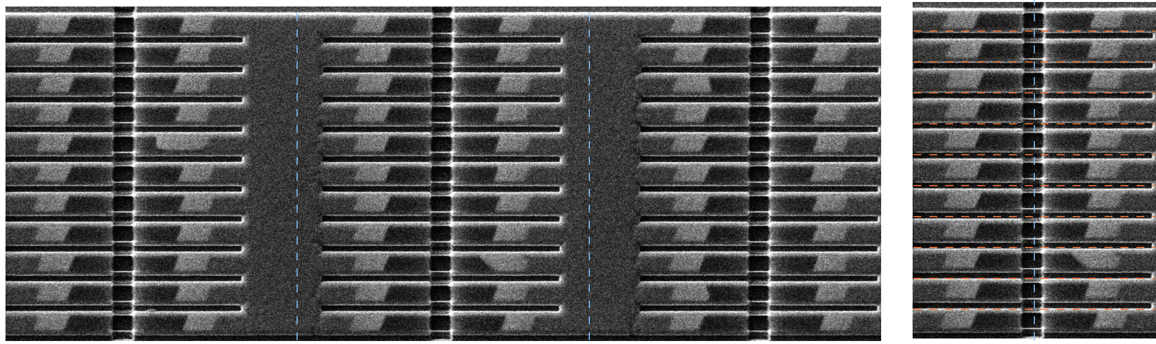


Figure 5.8: Max and min-pooling operations with vectorisation and gradient calculation for cut-point identification.



(A) Isolated nanowire array and division in columns. (B) Final cuts

Figure 5.9: Final cuts for the isolation of single wires. (A) shows an image of a nanowire array as it appears after a successful cut with the method shown in Figure 5.8. The light blue dashed lines show the division in three equally sized parts picturing the three columns. (B) shows a column after it has been reduced to the 22 wires, a light blue vertical line shows how the image is divided in two equally sized parts, while the 10 equally-spaced orange horizontal lines show the final subdivision into single wires.

segments in the denoised input. Unfortunately, the result of the `max_pool` is dominated by the internal template sidewalls of the nanowire array.

This difference in outcome is the reason why the idea of isolating only the area of the image corresponding to the III-V nanowires was abandoned and, instead, the goal shifted to isolating the portion of seed, nanowire and empty templates together, as was shown in Figure 5.5.

To determine the cut-point the `numpy` arrays resulting from the pooling operations were vectorised, as in, reduced to one-dimensional `numpy` arrays, by taking the maximum value, for the `max_pool` output, or the minimum value, for the `max_pool` output, of each column. The gradient of both vectors was then calculated using the `gradient` method of the `numpy` library, which returned the ratio of the variation in intensity to the variation in the position in the vector. The results of this operation for the image used as an example in this section are also shown in Figure 5.8.

During the development of the splitting algorithm, it was found that due to the shading in the SEM image both vectors had their largest gradients in the area corresponding to the introduction of the side walls of the comb tooth template. Furthermore, for the initial, smaller dataset used in the early trials, it was also found that taking the largest gradient further down the vector resulted in a tighter cut. Unfortunately, as seen in the plot in Figure 5.8 this had to be changed in the code revisions carried out after the initial classifier training to include a handful of images for which the maximum gradient was much further after the desired cut point. In the first iterations of the splitting algorithm this would result in the image being excluded from the input dataset.

The procedure used to isolate this cut point is repeated after rotating the `numpy` array to calculate the cut points for all four sides of the nanowire array. The final result of these cutting operations is shown in Figure 5.9(A). The nanowire array is perfectly centred in this image, and the columns containing the nanowires can be split easily by dividing the image into three equally

Table 5.7: Percentages of each class in the input dataset after preprocessing with the original splitting algorithm.

Class	Parasitic	Wire Parallel Defect	Wire Parallel Perfect	Wire Tilted Defect	Wire Tilted Perfect	Null
Percentage	1.8 %	1.2 %	25.8 %	1.2 %	18 %	11.2 %

sized parts, as shown by the light blue dashed lines, resulting in three nanowire column images.

The remaining silicon anchor areas in the nanowire array column images can be trimmed out with the same algorithm used to isolate the array (Figure 5.8), resulting in an image like that of Figure 5.9(B), showing the central column of the nanowire array in Figure 5.9(A) after refinement. By splitting this image in half vertically along the middle and then dividing the two halves horizontally in 11 equally-sized parts the single wires are isolated.

Label assignment

After completion of image splitting, each image must be assigned a label for supervised classifier training to take place. The coordinates of the position of the vertices delimitating each resulting image within the parent raw image were recorded throughout all transformation. They can be compared with the coordinates of the label saved in the `.json` file created by `labelme` during labelling.

To determine which label to assign to each refined image, the label list for the parent image is loaded and the coordinates of each point defining a label are checked to verify if they fall in the area corresponding to the refined image. When a label does it is added to a list. Ideally, the length of the list after all labels are processed should be 1, only containing the label corresponding to the wire type (parallel or tilted) and growth result (perfect or defect). However, the splitting algorithm does not always create the expected result, often due to the cut points being incorrect. This, plus some images containing two labels either due to nucleation on the internal template walls or parasitic III-V crystals growing on top of the nanowire array (as seen in Figure 5.4) means that some images will have either 0 or more than 1.

Images with 0 labels are removed from the input dataset and are not considered. Images with more than one label that do not contain a defective or parasitic label are assigned to the `Null` class. Conversely, if there is a defective or parasitic label, it is assigned to the image. Table 5.7 shows the breakdown of the composition of the dataset resulting from the splitting algorithm in its first iteration. The percentages add up to 59.2 % as the remaining 40.2 % of images was incorrectly cut by the algorithm resulting in no matches with existing labels.

Aside from the flaws of the splitting algorithm, another issue is that the dataset is heavily unbalanced. The perfect wires dominate in quantity, having more than 10 times the number of defective wires. 25.8 % of the wires are parallel perfect, and 18 % are tilted perfect, reflecting very well the 60 % / 40 % split of the raw dataset between parallel and tilted arrays. Parallel and

tilted defective wires make up an equal percentage (1.2 %) of the splitting algorithm's output. 1.8 % of the output consists of images of parasitic crystals, and, finally, 11.2 % was assigned as `Null` class.

5.3.2 Training

A compact model consisting of two convolutional layers, followed by three linear layers and based on the `pytorch` [164, 165] framework was chosen. First, a block of two convolutional layers (`torch.nn.Conv2d`) received the input image, which was normalised to a standard size. The first convolutional layer applies 6 filters to the starting image with a 5 x 5 kernel size. The second convolutional layer applies 16 filters of the same size. Each convolutional layer is followed by a ReLu activation function (`torch.nn.ReLu`) and a max pool operation (`torch.nn.MaxPool2d`) with a 2 x 2 kernel size. Second, the output of the convolutional layers is then flattened to a one-dimensional vector using `torch.nn.Flatten`. Thirdly, the vector goes through three linear layers (`torch.nn.Linear`), each separated by the application of a ReLu activation function to their output. The final layer outputs a vector with a length of 6 [14]. Each value in this vector represents the probability of the input image to belong to the corresponding class, as estimated by the classifier. The class with the highest probability then becomes the predicted class.

This simple model architecture showed good performance when classifying commonly used datasets, such as CIFAR-10 [166]. The input dataset as resulting from the splitting algorithm and label assignment was divided into a training set, comprising 70 % of the data, and a validation set containing the remaining 30 %. The sets were filled with random images, respecting the original composition of the dataset.

The three metrics of loss, F_1 score, and confusion matrix were used to evaluate the classifier's performance [167]. The F_1 score is a metric which rates the performance of a predictive operation. It consists in the harmonic mean of recall (R) and precision (P).

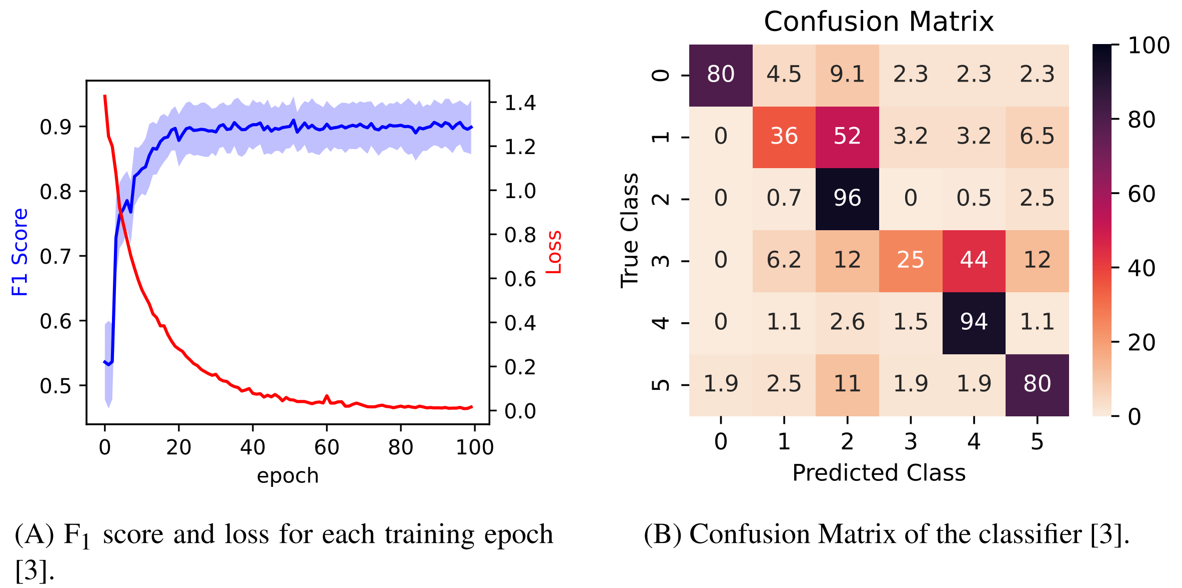
$$F_1 = \frac{2}{R^{-1} + P^{-1}} \tag{5.1}$$

Recall and precision are defined as the ratio of true positives (tp) to the sum of true positives and false negatives (fn) and the sum of true positives and false positives (fp), respectively.

$$R = \frac{tp}{tp + fn} \qquad \text{and} \qquad P = \frac{tp}{tp + fp} \tag{5.2}$$

This is valid for a two-class problem, but adjustments can be made to calculate these metrics for a multi-class situation. Macro averages of each class' precision and recall were employed. This method calculates precision and recall class-wise and then uses them to produce a single value metric by arithmetic mean.

The confusion matrix is a useful tool to visualise the performace of the classifier. It shows



(A) F_1 score and loss for each training epoch [3].

(B) Confusion Matrix of the classifier [3].

Figure 5.10: Training metrics for the classifier [3]. (A) shows the evolution of the F_1 score and the loss during training. (B) shows the confusion matrix of the trained classifier calculated on the test fraction. This Figure was adapted from the work of Brugnolotto *et al.* [3] under the terms of the CC BY 4.0 licence [130].

the number of items that were assigned to a predicted class divided according to their real class. An example of a confusion matrix, which was normalised on the population of each true class, is shown in Figure 5.10(B). Because of how the normalisation was carried out, the diagonal elements (top left to bottom right) represent the recall as a percentage. The higher the recall for each class, the better the classifier is at assigning the correct class to an item.

The cross-entropy loss function (`torch.nn.CrossEntropyLoss`), integrated with stochastic gradient descent (`torch.optim.SGD`), guided the learning process. Cross-entropy loss compares two distributions and returns a lower value the more similar the two distributions are. In this case, the two distributions are the label distributions of the training data as predicted by the classifier and the real distribution of labels in the training set. Stochastic gradient descent reduces computational load by only calculating the gradient using a single, randomly-selected, data point rather than considering the entire data set. This is particularly useful when dealing with large and complex data sets.

The classifier was trained until loss saturation was achieved, a process that lasted 100 epochs. The red curve in Figure 5.10(A) shows the saturation process, with loss, shown on the y-axis on the right side, reaching 0 at the end of the 100 training epochs. The blue line in Figure 5.10(A) shows the evolution of the F_1 score during training, with the shaded area around it representing the 97 % confidence interval on this metric. This F_1 score was calculated for each mini-batch of 20 images in the test set, and the arithmetic means of the so-obtained F_1 scores and relative error were calculated. The best classifier achieved an F_1 score of 0.91 ± 0.04 (97 % confidence interval). However, this metric alone is insufficient to properly assess the classifier's performance

Table 5.8: Percentages of each class in the input dataset after preprocessing with the revised splitting algorithm.

		Wire Parallel		Wire Tilted		
Class	Parasitic	Defect	Perfect	Defect	Perfect	Null
Percentage	2.6 %	1.5 %	35.9 %	1.2 %	24.4 %	0 %

given the very high imbalance in the dataset.

The confusion matrix in Figure 5.10(B) provides a much clearer assessment of the class-specific performance of the classifier, each value is given as a percentage. The classifier works very well at classifying images containing parasitic crystals, perfect parallel and tilted wires, and `Null` images. These four classes have recalls of 80 % or higher, with wire perfect classes showing a recall of 96 % and 94 % for parallel and tilted wires, respectively. However, the defective classes have very low recalls, with perfect parallel wires correctly identified only 36 % of the time and their tilted counterparts only 25 % of the time. When the off-diagonal components of the confusion matrix are examined, it is easily seen that defective wires are more often than not incorrectly classified as perfect. This is likely due to the disproportionate prevalence of perfect wires, but also to the relatively minor visible alteration of some of the defective wires compared to their perfect counterparts.

Collecting more images of defective wires is therefore a necessary step to create a more balanced input set and improve the recall of defective classes. It is worth noting that, despite the splitting algorithm's mixed success in properly processing half of the raw dataset, the classifier still managed to assign four out of six classes with very high accuracy.

5.3.3 Improvements to the digital image splitting algorithm

Changes were made to make the `Null` class unnecessary by allowing the algorithm to discriminate between multiple labels on the same image. This was done by computing the area of the intersections of each label polygon with the images using the `shapely` [168] library. The label with the highest intersection area is then assigned to the image.

Another change concerned the cut-point determination in the algorithm shown in Figure 5.8. The algorithm was changed to only process each image with the `max_pool` kernel and calculate the associated vectors and gradient. This solved the issue of the wrong point being chosen due to the influence of the `min_pool` kernel discussed in previous sections.

The results of these two modifications are shown in Table 5.8. Only 34.4 % of the raw dataset is marked for deletion in this version of the splitting algorithm. It is worth noting, however, that the classes that benefit the most from these modifications are the wire perfects. Indeed, while the wire parallel defect class gained 0.3 % more share of the raw dataset, the wire parallel perfect class gained 10.1 %. Similarly, the share of wire tilted defect class stays unchanged, while the wire tilted perfect increases by 6.4 %. These new results, coupled with the high recall for the

`Null` class, point to the original splitting algorithm being already sufficiently apt for the task of creating a dataset to train a classifier.

5.4 Discussion and future directions

This chapter explored the yield statistics for the $\{1\,1\,1\}$ growth front stabilisation method introduced and developed in Chapters 3 and 4. The survey carried out on 15 840 nucleation sites across 240 nanowire arrays found a global yield of 92.55 % [2]. It also highlighted the three most common defects, which were wires that grew with the wrong facet, totalling 368 wires or 31.19 % of defective sites, short wires, 211 or 17.88 % of defective sites, and the highest defect category: growth sites hidden by parasitic crystals with 487 sites or 41.27 % of defective sites. The number of wires hidden by parasitic crystals is so high that if they were excluded from the yield calculation, the total yield would grow by 2.77 % to 95.32 %.

Nucleation-related issues represented two-thirds (796 or 67.46 %) of the recorded defects, mostly due to surface treatment-related issues, such as loss of selectivity and seed surface conditions. This points to the strength of the facet stabilisation method as a reliable and controlled approach to the growth of monolithically integrated III-V crystals on chip-sized surfaces, supplementing observations on a more local level regarding the merging of multiple crystals in a single structure shown in Section 4.3.1.

The survey of the two samples that resulted in the statistical data on growth yield also produced a labelled dataset containing 240 SEM images [13], publicly available for use under the CC BY 4.0 licence [130]. In this chapter, the dataset was used to train a classifier that could distinguish between the two orientations of the nanowire arrays. The classifier achieved good performance in discriminating "perfect" wires between tilted and parallel but struggled with the identification of defective wires. This can be attributed to the high imbalance in the dataset, which can be resolved by collecting more images of defective wires of both kinds to supplement the currently available data. Further improvements can also be made to the wire-splitting algorithm, where a different approach might yield a more reliable solution to the determination of the cut points.

Chapter 6

Conclusions

The work presented in this thesis focused on the identification of the conditions under which the metal-organic chemical vapor deposition (MOCVD) of III-V semiconductors in template assisted selective epitaxy (TASE) templates results in a growth front consisting of a single $\{1\,1\,1\}_B$ facet, the integration of thin heterostructures capable of quantum confinement in a TASE nanowire, the properties of the nanowires grown with this method, and its yield. The study initially only focussed on the lattice matched $In_{0.55}Ga_{0.45}As$ and InP semiconductors.

The process began by analysing a single heterostructure consisting of two material segments, which showed the difference in growth front morphology between indium-gallium arsenide (InGaAs) grown with a low V / III ratio and indium phosphide (InP) grown with a high V / III ratio. As seen in Figure 3.5(A), the low V / III InGaAs layer grew with the arrowhead growth front, well known in literature [50], consisting of two $\{1\,1\,0\}$ faces on the upper half of the wire and a $\{1\,1\,1\}$ facet at the bottom. Conversely, in the high V / III ratio InP segment the growth rate was increased along the $\{1\,1\,0\}$ directions, resulting in the annihilation of the two top $\{1\,1\,0\}$ facets to the benefit of the bottom $\{1\,1\,1\}$ facet. Therefore, it became clear that a high V / III ratio InP growth regimen achieves the goal of stabilising the single-facet growth front.

However, when quick switching between precursors was attempted to create a thin heterostructure, the resulting nanowire, seen in Figure 3.8, showed a high composition intermixing of elements of the III group in the heterointerfaces coupled with the integration delay between elements of the III and V group. This caused the III and V concentration gradients to be misaligned. However, the V group element energy dispersive X-Ray spectroscopy (EDS) map also showed potential for well-defined quantum confinement structures.

Some recipe adjustments were made to build on the stabilisation of the $\{1\,1\,1\}$ facet shown to occur in InP growth with high V / III ratios, solve III - V integration delay, and improve III group element definition at the heterointerface. The introduction of hold steps in the recipe was shown to achieve all of these objectives in Figure 3.11. Later experiments showed that increasing the length of the InP stabilisation segment and reducing the deposition time of the InGaAs nucleation layer reduced variability in the stabilisation results. This created a platform allowing

for consistent III group element integration across the entire growth front and for constant growth rates, simplifying layer thickness control in quantum confinement structures.

Which of the two available $\{1\,1\,1\}$ facets would stabilise as a growth front in the $(0\,0\,1)$ silicon on insulator (SOI) wafer remained, however, a stochastic problem. A switch to a $(1\,1\,0)$ SOI wafer was made to allow for a consistent selection of best aligned $\{1\,1\,1\}$ in-plane facet. For comparison, the device layer silicon of the $(0\,0\,1)$ wafer was 220 nm thick, while the new $(1\,1\,0)$ wafer had a device layer thickness of 70 nm. As the device layer's thickness determines the nanostructures' height, the new nanowires' growth rates changed slightly compared to those of the nanowires grown on the $\{0\,0\,1\}$ substrate but remained comparable.

Growth in a competitive environment was studied on an area of the chip with diffused parasitic nucleation. Here, the nanowires competed with each other, but also with crystals unconstricted by the TASE template. The presence of these crystals, which acted as larger and larger capture centres for precursors as their surface area grew, changed the effective V / III ratio inside the TASE template. As a result, the growth rates of each consecutive material layer started to diminish despite the growth front progressing towards the template opening - a situation which was accompanied by a growth rate increase in previous nanowires. Finally, even the stabilising effect given by the high injected V / III ratio broke down and a multi-faceted growth front was re-established. This effect should be accounted for in the growth of dense sets of TASE structures with different shapes.

The $\{1\,1\,1\}_B$ stabilisation method proved to be an exciting avenue to grow defect-free single crystals from simultaneous nucleation on multiple seeds, as shown in Figure 4.13. The defect-free merging of the three seed crystals was achieved thanks to the layer-by-layer growth on $\{1\,1\,1\}$ atomic planes enabled by the highly controlled growth regimen established during the deposition of InP with a high V / III ratio.

The deposition of InGaAs layers with a thickness of four atomic bi-layers was an achievement at the very limit of what can be accomplished with metal-organic chemical vapor deposition (MOCVD), highlighting both the merits and limitations of the recipe developed in this thesis. It also showed how any heterointerface achievable with this method is finite with a width larger than 2 nm. The quantum well consisting of lattice-mismatched indium arsenide (InAs) between two InP segments was analysed with geometric phase analysis (GPA). This thin layer showed a very small change in lattice constant, synonymous with local strain.

A survey was carried out across two of the samples to establish yield statistics for TASE on $(1\,1\,0)$ SOI using the single-facet $\{1\,1\,1\}$ growth front method. 240 nanowire arrays were imaged, resulting in a dataset of 15 840 nucleation sites. Yield calculations showed how 14 660 wires grew with the intended end facet, indicative of an early stabilisation of the $\{1\,1\,1\}$ facet as the growth front, and resulting in a total yield of 92.55 %. The three most common reasons for defective wires were:

1. nucleation sites hidden by parasitic crystals: 487 sites, 41.27 % of defective and 3.07 %

of total sites;

2. nucleation sites ending with the wrong facet configuration: 368 sites, 31.19 % of defective and 2.32 % of total sites;

3. significantly shot wires: 211 sites, 17.88 % of defective and 1.33 % of total sites.

Together, nucleation-related issues represented 67.47 % of the recorded defects, cementing the facet stabilisation method as a reliable approach to the growth of III-V semiconductor on silicon, since further optimisation of pre-MOCVD surface treatments would eliminate these defects.

The data set used in this yield study is publicly available [13] under the terms of the CC BY 4.0 licence [130]. In it, each wire and parasitic crystal has been given one of five labels: "Parasitic", "Wire_Straigh_Perfect", "Wire_Straigh_Defect", "Wire_Tilted_Perfect", and "Wire_Tilted_Defect". In this thesis, the images that make up the data set were first split down to individual wires using an automated splitting algorithm [14] and then used in a simple classifier. Training metrics (see the confusion matrix in Figure 5.10(B)) showed a marked classification ability for parasitic crystals and perfect wires, whether straight or tilted. However, due to data set imbalance, the model's ability to classify defective wires was not very high.

6.1 Future directions

In some areas, the addition of more data can complement the research presented in this thesis. Statistical data on the growth yield of multi-seed structures, recipe optimisation for the deposition of gallium arsenide (GaAs) and gallium antimonide (GaSb) layer, and investigation of the effect of *p* dopants on growth would enrich this work. Further development on the wire splitting algorithm presented in Chapter 5 and perhaps a different approach could also improve its performance.

Studies on the controlled merging of crystals grown with the method presented in this thesis could explore the effect of larger platelet areas and seed spacing on the final defect concentrations. Constructing an appropriately sized cell for in-situ transmission electron microscopy (TEM) analysis could empower this approach by allowing real-time imaging of the growth dynamics occurring at the merging stage of the three crystals.

Politypism caused by the high density of a single type of defect, the rotational twin plane (RTP), remained an issue in all samples and is a by-product of the $\{1\,1\,1\}$ stabilisation method. Two research avenues can be explored to reduce the amount of RTPs in TASE nanowires or eliminate them. The first is to carefully adapt the growth recipe by tuning the V / III ratios and growth temperatures depending on the growth stage, as seen in both selective area growth (SAG) [76] and vapour-liquid-solid (VLS) epitaxy [118]. In-situ TEM could also be instrumental in shedding light on the dynamic of twin-plane formation in enclosed templates. The

second avenue would be to apply the template design used by Goswami et al. in [53] on the $(1\,1\,0)$ SOI and focus on stabilising a single $\{1\,1\,0\}$ facet as the growth front.

Another avenue of research could explore the effect of the morphology of the silicon seed on the morphology of the growth front. A method for selecting a specific $\{1\,1\,1\}$ facet between the two available during growth along a $\langle 1\,1\,0\rangle$ direction on a $(0\,0\,1)$ SOI could see better growth reproducibility on this commonly used substrate. Furthermore, the use of a different etchant to create a $\{1\,1\,0\}$ seed facet coupled with growth conditions enhancing the growth in $\{1\,1\,1\}$ directions could also achieve a single-facet heterointerface in TASE nanowire growth, and a yield study for comparison with the $\{1\,1\,1\}$ stabilisation method used in this work would enrich the knowledge on the subject.

Further research on the stability of the single-facet growth front in TASE templates could shed light on any potential mechanisms with which a return to a multi-faceted growth front could occur, such as critical layer thicknesses of lattice-mismatched semiconductors.

Another important avenue of characterisation which was not explored in the present work is the analysis of the electrical and electro-optical properties of the nanowires containing quantum wells fabricated with the facet stabilisation method. For example, their introduction in the i region of a p - i - n photodetector is expected to lead to reduced dark currents [59], and measurements to confirm these findings would be a natural next step in the integration of this growth regimen in the fabrication of TASE-based PICs.

Appendix A

Fabrication and characterization tools

The Binning and Rohrer Nanoscience Center (BRNC) is a facility at IBM Research Europe – Zurich, in Rueschlikon, Zurich, Switzerland. It consists of a cleanroom and Noise-free lab. All the experimental work on the growth and characterisation of nanostructures presented in this work took place at IBM Research Europe - Zurich, most of it within the BRNC itself.

A.1 Cleanroom tools

The BRNC cleanroom is a 950 m^2 area with different rooms ranging in cleanroom classification from 100 (ISO 5) to 10'000 (ISO 7). Most of the chemicals and tools used during the template assisted selective epitaxy (TASE) process and sample preparation are within these rooms.

The following tools, located in the BRNC cleanroom, were used:

- wet benches, as fume hoods are impractical in a cleanroom: while in fume hoods, the vapours and gasses are aspirated upwards, on the wet benches they are evacuated through the work surface, thanks to holes in it and an applied negative pressure gradient under it. These workstations have smaller tools, such as spin coaters for resist application, hot plates, and ultrasound baths. Solution-based etching can also be carried out on wet benches safely with different dangerous chemicals such as strong acids and bases and toxic reagents,

- plasma-enhanced chemical vapour deposition (PECVD) tool: Oxford Plasma Pro 100 for silicon oxide deposition,

- atomic layer deposition (ALD) tool: Oxford FlexAL,

- reactive ion etching (RIE) tool: Oxford Plasma Pro NPG 80, which employs a chemically active plasma to etch oxides or metal,
- inductively-coupled plasma (ICP) etching tool: Oxford Plasmalab System 100. This tool employs a chemically active inductively coupled plasma to achieve extremely anisotropic etching of silicon,
- mask aligner: Seuss Mask Aligner MA6 to execute photolithography steps with pre-written metal masks,
- rapid thermal annealer Annealsys AS-one 150 for high-temperature annealing treatments of deposited material layers,
- dual beam focused ion beam (FIB) tool: FEI Helios NanoLab 450S, for SEM imaging; and lamella cutting, manipulation, and thinning,
- plasma cleaner PVA TePla Plasma Asher for the removal of resist traces and surface preparation,
- reflectometer: Nanospec II 150-VIS to measure the thickness of deposited material layers,
- multiple optical microscopes to monitor the fabrication process,
- Raman spectroscope: ND-MDT NTEGRA Spectra.

A.2 Noise-free labs tools

The BRNC Noise-free labs consist of $176\,\mathrm{m}^2$ of noise-shielded laboratory area. The shielding limits vibration noise to $300\,\mathrm{nm\,s}^{-1}$ at 1 Hz, and to $10\,\mathrm{nm\,s}^{-1}$ at frequencies higher than 100 Hz; temperature fluctuations to 0.01 °C; humidity variations to 2 %; acoustic noise level to 21 dBc; and electromagnetic noise to 0.3 nT AC, and to 15 nT DC [169]. These technical specifications are instrumental in successfully recording atomic-resolution scanning transmission electron microscopy (STEM) images, making the laboratory rooms a tool in their own right.

Two of the tools in the Noise-free labs were used in this work, relating to the STEM measurements I carried out. The first is the plasma cleaner Fischione Model 1020 for the final oxygen-argon plasma cleaning (effective in removing hydrocarbon contamination) of the lamella before insertion in the STEM.

The scanning transmission electron microscope JEOL ARM200F is the second tool. This microscope is equipped with a cold field emission gun placed in a 200 kV extraction and acceleration potential drop (emitting with an energy width of less than 0.3 eV), hexapole optics, bright field (BF), annular dark field (ADF), and high angle annular dark field (HAADF) detectors. Two spectroscopic techniques are also available on this microscope in the form of energy

dispersive X-Ray spectroscopy (EDS) and electron energy loss spectroscopy (EELS). The EDS tool JED-2300T was used to characterise the samples. This tool is equipped with a 100 mm^2 detector surface that allows for very fast EDS mapping. The detector is equipped with an ultra-thin window, which provides excellent performance for analysing light elements. Resolution for the Mn Kα line is less than 138 eV. 1 sr collection solid angle. This tool can also be operated as a transmission electron microscope (TEM).

A.3 Other tools

Outside both the cleanroom and Noise-free lab, the following tools were instrumental in achieving the experimental results:

- scanning electron microscope (SEM): Hitachi SU8000 type II to monitor the fabrication process,
- a VeecoP125 metal-organic chemical vapor deposition (MOCVD) setup in which the III-V nanowires were grown. The vertical reactor contains a showerhead, which introduces precursors in the chamber. The rotating susceptor can accommodate three 2-inch wafers, or smaller pieces, such as the 2 cm $\times$ 2 cm dices used in this work, utilising carriers [1].

The precursors used in MOCVD are:

- trimethyl indium (TMIn),
- trimethyl gallium (TMGa),
- *tert*-butyl arsine (TBAs),
- *tert*-butyl phosphine (TBP),
- trimethyl antimony (TMSb),
- tetraethyl tin (TESn) (as a dopant)

The Gatan Microscopy Suite (GMS) software was used to record and later analyse the microscopy images and EDS data. L-Edit and KLayout were used to design and visualise the electron beam lithography (EBL) and optical lithography masks in GDSII format.

Tools that I did not operate personally but were used in the fabrication or characterisation of my samples were:

- sputter tool: Von Ardenne CS 320S to deposit the tungsten that makes up the electron beam lithography markers,

- electron beam lithography tool Vistec EBPG 5200+ for exposure of electron-sensitive resists,
- laser writer: Heidelberg DWL 2000 for the creation of optical lithography masks (glass substrate, metallic layer mask),
- dicer tool: ADT ProVectus LA 7100 for dicing large wafers into smaller dices,
- a “home-built” photoluminescence spectroscope for photoluminescence characterisation.

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