Fabrication and Characterization of $MoTe_2$ Field Effect Transistor

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Abstract

For nearly half a century, the scaling of silicon (Si) CMOS field-effect transistors (FETs) has driven advancements in microelectronics, as predicted by Moore's Law. However, as device dimensions reach nanometre scales, the physical limitations of traditional materials have become evident. Two-dimensional (2D) materials, such as transition metal dichalcogenides (TMDCs), present a promising alternative for next-generation devices due to their unique properties, including flexibility and high carrier mobility. These materials are particularly well-suited for 'More than Moore' devices, which aim to enhance CMOS technology by introducing additional functionalities.

This dissertation investigates the fabrication and characterisation of MoTe2-based FETs. First, a novel chemical vapour deposition (CVD) method for the selective growth of 2H- and 1T-$MoTe_2$ using $FeTe_2$ and Mo (or MoO_3) precursors is presented. Second, a back-gate $MoTe_2$ FET fabrication process is developed, integrating CVD with photolithography, which offers a scalable alternative to exfoliation techniques. The fabrication process utilises a double-layer photolithography method, employing an auxiliary water-soluble resist (SPR92) to protect $MoTe_2$ from damage.

Finally, the electrical performance of the $MoTe_2$ FETs is evaluated, comparing Pd/Au and Ti/Au contact metals. Pd/Au contacts exhibit lower contact resistance (~0.79 MΩ·μm) and form ohmic contacts, while Ti/Au shows higher resistance (~2.06 MΩ·μm) due to a larger Schottky barrier. Both devices demonstrate p-type operation with a mobility of ~2.5 $cm^2/V \cdot s$, though Pd/Au contacts deliver superior performance, including a higher Ion/off ratio (10^4), lower sub-threshold swing (1V/dec), and a threshold voltage of -45 V. These findings suggest that further optimisation of contact metals could improve the performance of p-type $MoTe_2$ FETs for future applications.

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Thesis Contributions:

Some of the work undertaken in this thesis was performed in collaboration with others. The details of collaboration are listed below.

• TEM images and EDX spectra of 2H- and 1T-$MoTe_2$ were obtained by Dr. Donald A. MacLaren at the University of Glasgow.

Author’s declaration：

I declare that, except where explicit reference is made to the contribution of others, that this dissertation is the result of my own work and has not been submitted for any other degree at the University of Glasgow or any other institution.

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Conferences:

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Contents

1.0 Introduction

Metal-oxide-semiconductor field-effect transistors (MOSFETs) have long been the foundational building blocks of semiconductor chips. The increasing demand for computational power within a fixed chip size has driven the continuous scaling down of MOSFET dimensions[1]. n 1965, Gordon Moore proposed the now-famous Moore's Law, predicting that the density of transistors on a chip would double approximately every two years[2]. For over half a century, this prediction has proven remarkably accurate, driving advancements in electronic devices such as computers and smartphones. Achieving Moore's Law necessitates the ongoing reduction in the size of individual transistors, enabling a greater number of transistors to be accommodated on the same silicon wafer, thus increasing the computational power of the chip[3]. However, Moore's Law not only forecasts an increase in transistor density but also implies a reduction in the cost of individual transistors and improvements in their performance[4]. One method to achieve these goals is to enhance the processing speed of chips while simultaneously reducing their energy consumption. Today, over 2.5 trillion MOSFETs can be placed on a single silicon wafer. Despite the semiconductor industry's adherence to Moore's Law, which predicts transistor density doubling every two years, significant challenges have arisen since the invention of the first transistor in 1947[5].

Semiconductor process scaling has progressed through various phases, with corresponding iterations in transistor configurations. Beginning with the era of "happy scaling", it has evolved into architecture-driven scaling, characterised by strained silicon and high-k metal gates, followed by post-Moore scaling technologies such as FinFETs[6] The current generation includes gate-all-around FETs (GAAFETs) and

multi-bridge channel FETs (MBCFETs).[7] However, challenges related to cost, performance, and area efficiency have emerged, affecting at least one of these metrics, as illustrated in Figure 1.1.

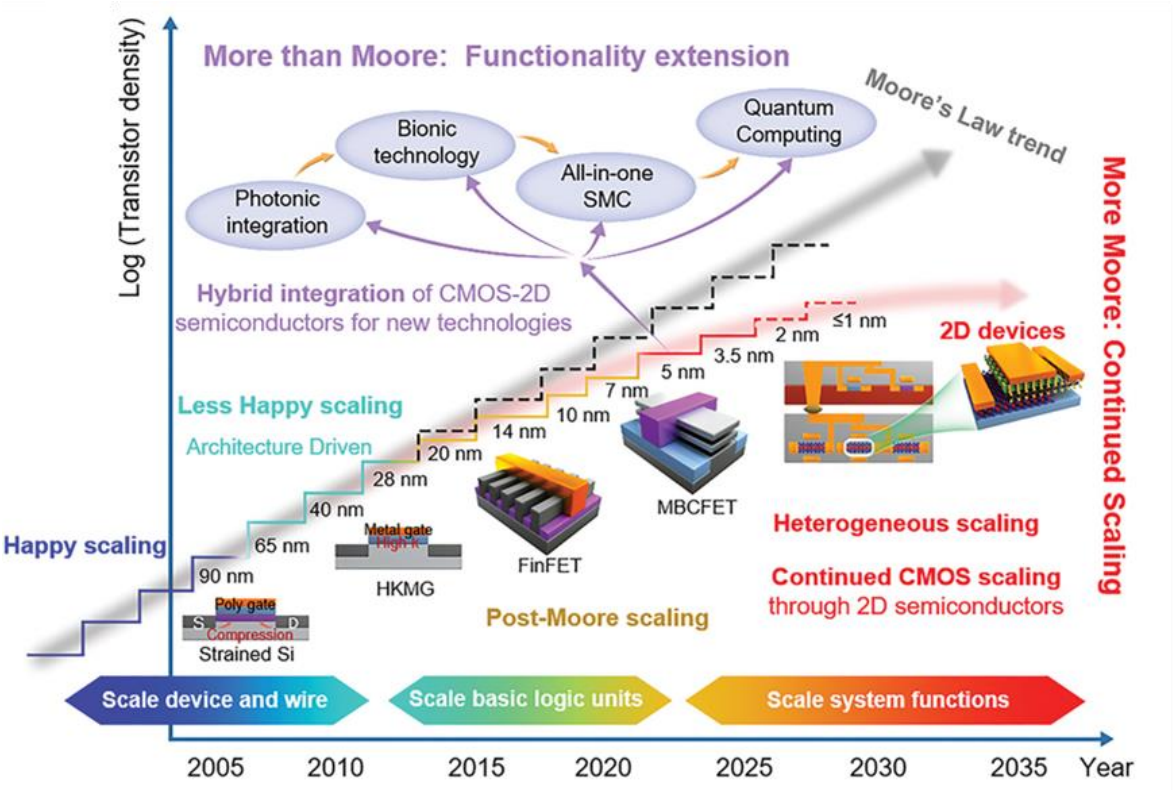


Figure 1.1 Silicon IC nodes evolve, facing challenges at sub-5 nm scales. Introducing 2D materials along "More Moore" and "More than Moore" paths enables continued CMOS scaling and hybrid integration for functional scaling in new technologies[8].

Moore's Law has encountered sustainability challenges as chip sizes shrink to sub-10 nm levels, largely due to the physical limitations of bulk materials[9]. Further scaling exacerbates these issues, particularly as gate dielectric thicknesses must be reduced to maintain device performance[1]. The manufacturing of silicon FETs faces inherent process and technical hurdles, contributing to a slowdown in miniaturisation[10]. As transistor dimensions shrink, the short-channel effect intensifies, leading to reduced threshold voltages, carrier velocity saturation, degradation of sub-threshold

characteristics, and inefficient channel cutoff by the gate[11]. These factors significantly increase leakage currents and energy dissipation in silicon transistors. Additionally, power and efficiency bottlenecks persist in silicon integrated circuits (ICs), which have yet to approach the Landauer switching limit. The inherent thickness of bulk silicon also poses challenges in connecting the source and drain to the channel surface and matching doping levels between the bottom and top channel surfaces[12]. Consequently, current transistor architectures limit design to a single top gate, severely restricting the area efficiency of silicon transistors[2].

The final channel thickness of FETs could be reduced to below 1 nm[13]. However, achieving this is extremely challenging for any three-dimensional (3D) semiconductor crystal due to increased charge carrier scattering at the interface between the channel and gate dielectric material, which induces a significant decrease in mobility[13]. Researchers are exploring materials such as carbon nanotubes[14,15] and III-V semiconductors[16] to address short-channel effects (e.g., reduced control over the channel and increased leakage current) in next-generation electronics. While ultra-thin body (UTB) semiconductors[17] made of 3D materials show promise, their rough surfaces lead to carrier scattering[18,19] which degrades performance and necessitates further research to improve electrostatic properties[20].

Two-dimensional (2D) semiconductors have emerged as promising candidates to circumvent the short-channel effect challenges associated with Si MOSFETs[21], thanks to their unique atomically layered structure and typically dangling-bond-free surfaces. The past decade has seen considerable progress in scaling down the size of 2D transistors through various approaches, with physical gate lengths shrinking

from the micrometre scale to sub-nanometre levels, all while demonstrating impressive performance—highlighting their potential as a replacement for Si MOSFETs[22].

Since the introduction of graphene in 2004, a variety of one-dimensional and two-dimensional materials have been extensively studied, consistently attracting attention from researchers across multiple fields. Many of these materials offer superior properties, such as high conductivity, high mobility, sensitivity to external stimuli, a high surface-to-volume ratio, and ease of thinning down to atomic-scale thickness[23]. The discovery of graphene generated significant interest due to its high carrier mobility, flexibility, and mechanical strength. However, despite these appealing properties, graphene cannot be used in field-effect transistors because it lacks a sizeable native band gap[24]. Artificially generating a band gap in graphene can limit its mobility, increase operational complexity, and reduce device performance[25]. Other 2D or van der Waals materials, such as transition metal dichalcogenides (TMDCs), have the general formula MX_2, where M represents a transition metal from groups VI-VII (e.g., Mo, W, Nb, Re) and X is a chalcogen (e.g., S, Se, Te) [26]. The typical structure of MX_2 is shown in Figure 1.2.

A layer of M atoms is sandwiched between two layers of X atoms, forming a single layer. In TMDCs, an indirect-to-direct band gap crossover occurs when reducing the material from bulk to monolayer. The band gap in TMDCs ranges from 1 eV to 2 eV[27]. These materials exhibit high mobility, with up to 8,550 $cm^2 V^{-1} s^{-1}$ for p-type and 16,000 $cm^2 V^{-1} s^{-1}$ for n-type materials, respectively[28]. FET devices made from TMDCs have demonstrated promising performance, such as a low sub-threshold swing of 60 mV/decade and an ION/OFF ratio of 10^8 [29]. Due to its considerable band gap of approximately 1 eV and high mobility, theoretically around 8,500 $cm^2 V^{-1} s^{-1}$ [30],

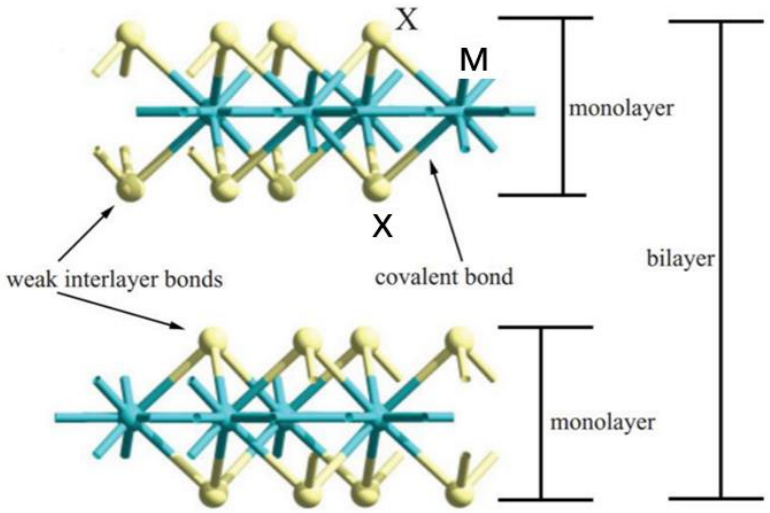


Figure 1.2 The MX_2 crystal structure description for TMDC materials the atomic structure of layered transition metal dichalcogenides of MX_2 type (TM, transition metal; X, chalcogenide). Different sheets of MX_2 are composed of three atomic layers X–M–X, where M and X are covalently bonded, and sheets are held together by weak interlayer bonds,

atomically thin layers of $MoTe_2$ have emerged as strong contenders against traditional semiconductors, especially graphene, in applications including low-power FETs, memory and optoelectronic devices, chemical sensors, and flexible, transparent electronics [30]. $MoTe_2$, a type of TMDC, also shows promise in mitigating short-channel effects[31]. These unique properties drive interest in ultrathin TMDCs as non-zero bandgap semiconductors and metals[32]. When reduced to a monolayer, semiconductor TMDCs shift from an indirect to a direct band gap, enhancing gate electrostatic properties and significantly reducing leakage current[33]. $MoTe_2$'s band gap, which is close to that of silicon, makes it highly relevant for semiconductor applications in electronics[34], The design of digital FET devices should prioritise atomic-scale thin films, preferably monolayers, for optimal performance. Developing

atomically thin, large-area, high-quality $MoTe_2$ films is essential for their potential adoption in mass production[35].

Consequently, my doctoral research aimed to optimise a chemical vapour deposition (CVD) process for producing high-quality $MoTe_2$ films and to develop $MoTe_2$ FETs directly from the CVD-produced films using photolithography. This research involved investigating the physical characteristics of 2H- and 1T-$MoTe_2$ films through Scanning Electron Microscopy (SEM), Raman spectroscopy, and Atomic Force Microscopy (AFM). Additionally, the study explored the performance of back-gated $MoTe_2$-FETs, with a particular focus on Fermi-level pinning (FLP) suppression and bipolar FET behaviour. A p-type dominant $MoTe_2$-FET was achieved by employing a high-work function metal as an ohmic contact electrode. The following chapters detail the findings of this research:

Chapter 2: This chapter provides background information on $MoTe_2$, including its structure, synthesis methods, and characterisation techniques. It begins by discussing the fundamental elements and properties of TMDCs, then elucidates the crystal structures and properties of 2H- and 1T-$MoTe_2$. Various synthesis and fabrication methods for $MoTe_2$ and FETs are also outlined.

Chapter 3: This chapter introduces the instruments and principles employed throughout the research. It covers the physical characterisation techniques used for $MoTe_2$ films and FET devices, including SEM, AFM, Energy Dispersive X-ray Spectroscopy (EDX), and Raman spectroscopy. Methods for measuring the electrical properties of $MoTe_2$ and FET characteristics are then described.

Chapter 4: This chapter presents and discusses the novel CVD synthesis processes developed for $MoTe_2$ in this work. It details improvements achieved in CVD synthesis for both 2H- and 1T-$MoTe_2$ systems, along with characterisation data obtained from Raman spectroscopy, SEM, and AFM analyses. The film transfer method and investigations into the electrical properties of $MoTe_2$ are also discussed.

Chapter 5: This chapter describes the steps involved in fabricating $MoTe_2$ FETs using traditional photolithography techniques, along with the optimised processes developed in this study. It provides detailed steps for $MoTe_2$-FET production using a double-layer photolithography process and outlines the characterisation of each step. A summary of the overall process and optimised device preparation sequence is also provided.

Chapter 6: This chapter analyses the electrical performance of $MoTe_2$ FETs, evaluating the effects of the investigated parameters on device performance. The results regarding contact resistance and their comparative analysis are discussed in detail.

Chapter 7: This final chapter summarises the key achievements of the doctoral research on $MoTe_2$-FET devices and offers suggestions for future work. It highlights the development of novel CVD synthesis processes, improvements in CVD synthesis for 2H-$MoTe_2$ systems, and the fabrication of $MoTe_2$ FETs using traditional photolithography techniques, as well as the analysis of their electrical performance. Recommendations for future research include further optimisation of device fabrication processes, exploration of alternative synthesis methods, investigation of novel device architectures, and deeper analysis of device performance under varying conditions. These suggestions aim to advance the understanding and application of $MoTe_2$-FET devices in future nanoelectronics research.

Reference:

1. Das, S., Sebastian, A., Pop, E., McClellan, C. J., Franklin, A. D., Grasser, T., Knobloch, T., Illarionov, Y., Penumatcha, A. V., Appenzeller, J., Chen, Z., Zhu, W., Asselberghs, I., Li, L.-J., Avci, U. E., Bhat, N., Anthopoulos, T. D., & Singh, R. (2021). Transistors based on two-dimensional materials for future integrated circuits. *Nature Electronics*, *4*(11), Article 11. https://doi.org/10.1038/s41928-021-00670-1

2. Connected society. (2018). *Nature Electronics*, *1*(1), Article 1. https://doi.org/10.1038/s41928-017-0020-x

3. Iqbal, M. W., Firdous, F., Manzoor, M., Ateeq, H., Azam, S., Aftab, S., Kamran, M. A., Rehman, A. ul, & Majid, A. (2020). Study of electrical attributes of molybdenum ditelluride (MoTe2) FET using experimental and theoretical evidences. *Microelectronic Engineering*, *230*, 111365. https://doi.org/10.1016/j.mee.2020.111365

4. *Promises and prospects of two-dimensional transistors | Nature*. (n.d.). Retrieved 1 May 2024, from https://www.nature.com/articles/s41586-021-03339-z

5. Schaller, R. R. (1997). Moore's law: Past, present and future. *IEEE Spectrum*, *34*(6), 52–59. https://doi.org/10.1109/6.591665

6. Hisamoto, D., Lee, W.-C., Kedzierski, J., Takeuchi, H., Asano, K., Kuo, C., Anderson, E., King, T.-J., Bokor, J., & Hu, C. (2000). FinFET-a self-aligned double-gate MOSFET scalable to 20 nm. *IEEE Transactions on Electron Devices*, *47*(12), 2320–2325. https://doi.org/10.1109/16.887014

7. Loubet, N., Hook, T., Montanini, P., Yeung, C.-W., Kanakasabapathy, S., Guillom, M., Yamashita, T., Zhang, J., Miao, X., Wang, J., Young, A., Chao, R., Kang, M., Liu, Z., Fan, S., Hamieh, B., Sieg, S., Mignot, Y., Xu, W., … Khare, M. (2017). Stacked nanosheet gate-all-around transistor to enable scaling beyond FinFET. *2017 Symposium on VLSI Technology*, T230–T231. https://doi.org/10.23919/VLSIT.2017.7998183

8. Wang, S., Liu, X., & Zhou, P. (2022). The Road for 2D Semiconductors in the Silicon Age. *Advanced Materials*, *34*(48), 2106886. https://doi.org/10.1002/adma.202106886

9. Chhowalla, M., Jena, D., & Zhang, H. (2016). Two-dimensional semiconductors for transistors. *Nature Reviews Materials*, *1*(11), 1–15. https://doi.org/10.1038/natrevmats.2016.52

10. Liu, Y., Duan, X., Huang, Y., & Duan, X. (2018). Two-dimensional transistors beyond graphene and TMDCs. *Chemical Society Reviews*, *47*(16), 6388–6409. https://doi.org/10.1039/C8CS00318A

11. Ferain, I., Colinge, C. A., & Colinge, J.-P. (2011). Multigate transistors as the future of classical metal-oxide-semiconductor field-effect transistors. *Nature*, *479*(7373), 310–316. https://doi.org/10.1038/nature10676

12. *International Roadmap for Devices and Systems lithography roadmap*. (n.d.). Retrieved 1 May 2024, from https://www.spiedigitallibrary.org/journals/journal-of-micro-nanopatterning-materials-and-metrology/volume-20/issue-4/044601/International-Roadmap-for-Devices-and-Systems-lithography-roadmap/10.1117/1.JMM.20.4.044601.full

13. Tang, L., & Zou, J. (2023). p-Type Two-Dimensional Semiconductors: From Materials Preparation to Electronic Applications. *Nano-Micro Letters*, *15*(1), 230. https://doi.org/10.1007/s40820-023-01211-5

14. Jurczak, M., Collaert, N., Veloso, A., Hoffmann, T., & Biesemans, S. (2009). Review of FINFET technology. *2009 IEEE International SOI Conference*, 1–4. https://doi.org/10.1109/SOI.2009.5318794

15. Yu, B., Chang, L., Ahmed, S., Wang, H., Bell, S., Yang, C.-Y., Tabery, C., Ho, C., Xiang, Q., King, T.-J., Bokor, J., Hu, C., Lin, M.-R., & Kyser, D. (2002). FinFET scaling to 10 nm gate length. *Digest. International Electron Devices Meeting,* 251–254. https://doi.org/10.1109/IEDM.2002.1175825

16. Stobbe, S., Lindelof, P. E., & Nygård, J. (2006). Integration of carbon nanotubes with semiconductor technology: Fabrication of hybrid devices by III–V molecular beam epitaxy. *Semiconductor Science and Technology*, *21*(11), S10–S16. https://doi.org/10.1088/0268-1242/21/11/S02

17. Ridaoui, M., Pastorek, M., Fadjie, A. B. D., Wichmann, N., Jaouad, A., Maher, H., & Bollaert, S. (2016). Ultra-thin body InAs-MOSFETs with elevated source/drain contacts. *2016 Compound Semiconductor Week (CSW) [Includes 28th International Conference on Indium Phosphide & Related Materials (IPRM) & 43rd International Symposium on Compound Semiconductors (ISCS)*, 1–2. https://doi.org/10.1109/ICIPRM.2016.7528832

18. Vashishtha, V., & Clark, L. T. (2021). Comparing bulk-Si FinFET and gate-all-around FETs for the 5 nm technology node. *Microelectronics Journal*, *107*, 104942. https://doi.org/10.1016/j.mejo.2020.104942

19. Schmidt, D., Cepler, A., Durfee, C., Pancharatnam, S., Frougier, J., Breton, M., Greene, A., Klare, M., Koret, R., & Turovets, I. (2022). Development of SiGe Indentation Process Control for Gate-All-Around FET Technology Enablement. *IEEE Transactions on Semiconductor Manufacturing*, *35*(3), 412–417. https://doi.org/10.1109/TSM.2022.3168585

20. Vaqueiro, P., & Powell, A. V. (2010). Recent developments in nanostructured materials for high-performance thermoelectrics. *Journal of Materials Chemistry*, *20*(43), 9577–9584. https://doi.org/10.1039/C0JM01193B

21. Lin, Z., Wang, C., & Chai, Y. (2020). Emerging Group-VI Elemental 2D Materials: Preparations, Properties, and Device Applications. *Small*, *16*(41), 2003319. https://doi.org/10.1002/smll.202003319

22. Liu, Y., Weiss, N. O., Duan, X., Cheng, H.-C., Huang, Y., & Duan, X. (2016). Van der Waals heterostructures and devices. *Nature Reviews Materials*, *1*(9), 1–17. https://doi.org/10.1038/natrevmats.2016.42

23. Gupta, A., Sakthivel, T., & Seal, S. (2015). Recent development in 2D materials beyond graphene. *Progress in Materials Science*, *73*, 44–126. https://doi.org/10.1016/j.pmatsci.2015.02.002

24. Canadell, E., LeBeuze, A., El Khalifa, M. A., Chevrel, R., & Whangbo, M. H. (1989). Origin of metal clustering in transition-metal chalcogenide layers MX2 (M = Nb, Ta, Mo, Re; X = S, Se). *Journal of the American Chemical Society*, *111*(11), 3778–3782. https://doi.org/10.1021/ja00193a002

25. Rao, C. N. R., Sood, A. K., Subrahmanyam, K. S., & Govindaraj, A. (2009). Graphene: The New Two-Dimensional Nanomaterial. *Angewandte Chemie International Edition*, *48*(42), 7752–7777. https://doi.org/10.1002/anie.200901678

26. Furchi, M. M., Polyushkin, D. K., Pospischil, A., & Mueller, T. (2014). Mechanisms of Photoconductivity in Atomically Thin MoS2. *Nano Letters*, *14*(11), 6165–6170. https://doi.org/10.1021/nl502339q

27. Jariwala, D., Sangwan, V. K., Lauhon, L. J., Marks, T. J., & Hersam, M. C. (2014). Emerging Device Applications for Semiconducting Two-Dimensional Transition Metal Dichalcogenides. *ACS Nano*, *8*(2), 1102–1120. https://doi.org/10.1021/nn500064s

28. Iqbal, M. W., Iqbal, M. Z., Khan, M. F., Shehzad, M. A., Seo, Y., Park, J. H., Hwang, C., & Eom, J. (2015). High-mobility and air-stable single-layer WS2 field-effect transistors sandwiched between chemical vapor deposition-grown hexagonal BN films. *Scientific Reports*, *5*. Scopus. https://doi.org/10.1038/srep10699

29. *Spin and pseudospins in layered transition metal dichalcogenides | Nature Physics*. (n.d.). Retrieved 1 May 2024, from https://www.nature.com/articles/nphys2942

30. Castro Neto, A. H. (2001). Charge Density Wave, Superconductivity, and Anomalous Metallic Behavior in 2D Transition Metal Dichalcogenides. *Physical Review Letters*, *86*(19), 4382–4385. https://doi.org/10.1103/PhysRevLett.86.4382

31. Kanungo, S., Ahmad, G., Sahatiya, P., Mukhopadhyay, A., & Chattopadhyay, S. (2022). 2D materials-based nanoscale tunneling field effect transistors: Current developments and future prospects. *Npj 2D Materials and Applications*, *6*(1), Article 1. https://doi.org/10.1038/s41699-022-00352-2

32. Ahmed, S. (2019). *Transition metal dichalcogenides (TMDCs) based diluted magnetic semiconductors (DMS)* [Thesis, UNSW Sydney]. https://doi.org/10.26190/unsworks/21364

33. Gao, F., Yang, H., & Hu, P. (2018). Interfacial Engineering for Fabricating High-Performance Field-Effect Transistors Based on 2D Materials. *Small Methods*, *2*(6), 1700384. https://doi.org/10.1002/smtd.201700384

34. Lezama, I. G., Ubaldini, A., Longobardi, M., Giannini, E., Renner, C., Kuzmenko, A. B., & Morpurgo, A. F. (2014). Surface transport and band gap structure of exfoliated 2H-MoTe2 crystals. *2D Materials*, *1*(2), 021002. https://doi.org/10.1088/2053-1583/1/2/021002

35. Fraser, J. P. (2021). *The chemical vapour deposition of MoTe2 thin films and their applications* [PhD, University of Glasgow]. https://doi.org/10.5525/gla.thesis.82642

2.0 Background and Literature Review

Two-dimensional (2D) materials are characterised by their atomically layered structures, with van der Waals (vdW) bonds and weak covalent or ionic bonds between the layers. Among 2D materials, graphene stands out as a notable example, significantly stimulating interest in the application of 2D materials[1]. One of the distinguishing qualities of graphene is its exceptionally high electron mobility of up to 200,000 $cm^2 V^{-1} s^{-1}$[2], which sets it apart from traditional bulk semiconductor materials. However, its zero band gap limits its application in semiconductor technologies [3,4]. The rapid development of graphene and ultra-thin material manufacturing technologies has driven the exploration of additional 2D materials. The large family of Transition Metal Dichalcogenides (TMDCs) encompasses a variety of material properties, including metals, semiconductors, and insulators. Unlike graphene, TMDCs possess key properties, such as a low dielectric constant [1] These characteristics make TMDC materials highly attractive for the development of advanced, high-performance field-effect transistors (FETs) [5].

2.1 Transition Metal Dichalcogenides (TMDCs)

TMDCs, a versatile class of 2D materials, have garnered significant attention due to their unique structures and diverse properties, ranging from insulating to metallic behaviour. Unlike graphene, which lacks a band gap, TMDCs possess a direct band gap within the near-infrared and visible spectrum, making them ideal candidates for semiconductor applications. The most common TMDC structure is the MX_2-type semiconductor, where M represents a transition metal (such as molybdenum or tungsten) and X is a chalcogen atom (such as sulphur, selenium, or tellurium) [6].

Particularly significant are Group 6 TMDCs, such as MoS_2, $MoSe_2$, and $MoTe_2$, which are thermodynamically stable semiconductors with thickness-dependent band gaps. These materials transition from indirect band gaps in multilayer forms to direct band gaps in monolayers, a tuneable band structure that is critical for applications in electronics and optoelectronics[7]. Moreover, the crystal structure of TMDCs plays a vital role in determining their dielectric properties, which significantly affect their performance in electronic devices, such as FETs, by influencing factors like polarizability and dielectric anisotropy[8].

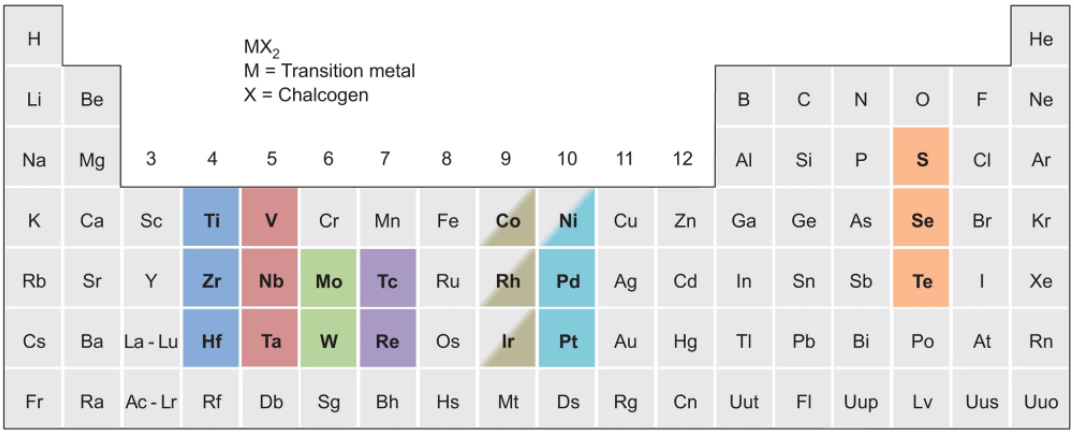


Figure 2.1 The periodic table highlights the transition metal atoms and chalcogens that predominantly form layered structures[7].

The carrier mobility of TMDCs is a critical parameter that determines the efficiency with which charge carriers (electrons and holes) move through the material in response to an electric field, directly influencing the speed and performance of electronic devices. While the carrier mobility of TMDCs is generally lower than that of graphene, it remains adequate for various applications, including low-power electronics and optoelectronics, with typical values ranging from 1 to 100 $cm^2/V{\cdot}s$ in materials like MoS_2. Carrier mobility in TMDCs can be further enhanced through techniques such as dielectric engineering, substrate optimisation (e.g., using

hexagonal boron nitride), and strain engineering. The dielectric properties of TMDCs are also vital in improving mobility by reducing impurity scattering and enhancing electrostatic control over the channel in FETs, leading to improved device performance. Additionally, phase transitions in materials such as $MoTe_2$, specifically the transformation from the semiconducting 2H phase to the metallic 1T phase, offer further tunability of their dielectric response, broadening their application potential in areas ranging from low-power electronics to photodetectors.

The crystal structure of a semiconductor significantly influences its dielectric properties, which in turn affect its overall performance in electronic and optoelectronic devices. The arrangement of atoms and the nature of chemical bonding—whether ionic, covalent, or van der Waals—determines how the material interacts with external electric fields, influencing its polarizability and dielectric anisotropy[9]. Stronger chemical bonds often result in a higher dielectric constant, enhancing the material's ability to store and manipulate electric charge[10,11]. Furthermore, crystal symmetry plays a crucial role in dielectric behaviour, with lower symmetry frequently leading to anisotropic dielectric properties[12]. In the case of TMDCs like $MoTe_2$, dielectric properties are layer-dependent, meaning the dielectric constant varies with the number of atomic layers, providing a tunable platform for FETs and optoelectronic devices[13]. This tunability is further amplified by phase transitions, such as the shift from the 2H to 1T phase in $MoTe_2$, which drastically alters the dielectric response and expands the range of applications.

Defects and the dimensionality of TMDC materials also influence their dielectric screening capabilities, essential for minimising impurity scattering and enhancing carrier mobility. This is particularly important in FETs, where high carrier mobility is

critical for optimal device performance[7]. A higher dielectric constant (ϵ_r) improves electrostatic control over the channel, leading to improve on/off current ratios, lower threshold voltages (V_{Th}), and more efficient low-power switching. In optoelectronics, a higher dielectric constant reduces exciton binding energy, facilitating electron-hole pair separation and increasing the efficiency of devices like solar cells and photodetectors[8,14].

Thus, the dielectric properties of TMDCs like $MoTe_2$ are of paramount importance in the development of next-generation semiconductors, offering a balance of high carrier mobility, effective dielectric screening, and layer-dependent tunability[15]. These features position TMDCs as promising candidates for advancing research in low-power electronics and high-efficiency optoelectronic devices, addressing key limitations of traditional semiconductor materials[12]. The combination of tuneable electronic properties, high on/off current ratios, and potentially enhanced carrier mobility makes TMDCs suitable for a wide range of semiconductor applications. Furthermore, their mechanical flexibility and robust dielectric screening make them ideal materials for flexible electronics and advanced optoelectronics. With their strong light-matter interaction, TMDCs also hold significant promise in optoelectronic applications such as photodetectors, solar cells, and LEDs. As research continues to improve the performance of TMDCs, these materials are poised to play a pivotal role in the future of low-power, high-efficiency electronic and optoelectronic devices.

2.2 Molybdenum Ditelluride ($MoTe_2$)

$MoTe_2$, a type of TMDC, possesses several intriguing and valuable properties. Unlike graphene, $MoTe_2$ exhibits both metallic characteristics and a non-zero band gap, enabling the formation of a band gap without altering the material or device design[16].

As its thickness is reduced to a monolayer, the indirect band gap transitions to a direct one [17]. This shift imparts $MoTe_2$ with distinctive optical and electrical properties, positioning it as a promising candidate for the development of high-performance optoelectronic devices[18].

$MoTe_2$ was chosen as the semiconductor material for this research due to its exceptional dielectric and electronic properties, which make it particularly well-suited for advanced FETs and optoelectronic devices. The dielectric constant of $MoTe_2$ plays a pivotal role in its operation within FETs, directly influencing the gate capacitancee $C_{ox} = \frac{\epsilon_r \epsilon_0}{t_{ox}}$. A higher ϵ_r allows for improved electrostatic control over the channel, enhancing the on/off current ratio and reducing the threshold voltage (VTh), both of which are critical for efficient switching. This facilitates better modulation of carriers within the channel, contributing to the development of high-performance, low-power electronics. Additionally, the dielectric constant affects the exciton binding energy in optoelectronic applications, where the binding energy is inversely proportional to the square of the dielectric constant $E_b \propto \frac{1}{\epsilon_r^2}$. A higher dielectric constant reduces the exciton binding energy, facilitating easier separation of electron-hole pairs and improving the efficiency of devices such as photodetectors and solar cells

Furthermore, the mobility of $MoTe_2$ is a crucial factor underpinning its utility in FET applications. According to the mobility equation $\mu = \frac{q\tau}{m^*}$, $MoTe_2$ demonstrates high carrier mobility due to its low effective mass (m^*). allowing for rapid charge transport, which is essential for high-speed transistor operations. The crystalline structure and high dielectric constant of $MoTe_2$ also help minimise phonon and impurity scattering, increasing the mean free time (τ) between scattering events and further boosting

mobility. These attributes translate directly into enhanced FET performance, with higher on-state currents, lower power consumption, and faster switching speeds. Such characteristics make $MoTe_2$ an appealing material for next-generation low-power, high-frequency electronic applications, justifying its selection for this research on optimising device performance.

The dielectric properties of $MoTe_2$, particularly in its 2H phase, are of great importance for its use in electronic and optoelectronic devices, given its notable anisotropy. It exhibits a high in-plane dielectric constant (15–20) and a lower out-of-plane constant (5–7), making it highly suitable for FET applications. The high dielectric constant enhances gate control, improving charge modulation and boosting FET performance. Additionally, it provides effective electric field screening, reducing exciton binding energy, which is advantageous for optoelectronic applications such as photodetectors. $MoTe_2$'s dielectric properties also affect its phase transitions between the semiconducting 2H and metallic 1T phases, crucial for phase-change memory devices. Its low dielectric loss further strengthens its suitability for low-power electronics, positioning $MoTe_2$ as a highly promising material for next-generation devices.

2.2.1 Structure and Properties of 2H-$MoTe_2$

2H-$MoTe_2$ is a semiconducting material with an indirect band gap of approximately 0.9 eV, which increases to around 1.10 eV in its monolayer form, making it comparable to silicon (Si). However, unlike Si, 2H-$MoTe_2$ undergoes a transition to a direct band gap when reduced to a monolayer, due to its distinctive crystal structure[9,19]. This hexagonal structure comprises closely packed molybdenum (Mo) atoms sandwiched between two layers of tellurium (Te) atoms, with weak van der Waals forces holding

the Te-Mo-Te layers together in a hexagonal pattern along the c-axis. Each Mo atom is coordinated with six Te atoms in a triangular prismatic arrangement (Figure 2.2)[20].

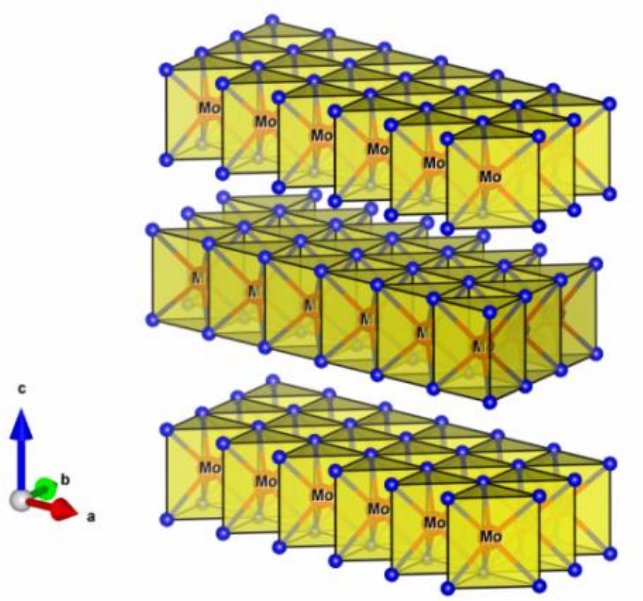


Figure 2.2 Crystal structure of 2H-$MoTe_2$ showing the unit cell and highlighting the Te termination planes of each Te-Mo-Te layer. Orange spheres represent Mo atoms, while Te atoms are represented by blue spheres[20].

The polymorph's designation in Ramsdell notation as '2H' stems from its hexagonal structure ('H') and the two van der Waals layers in its unit cell[21,22]. Crystallographic data for 2H-$MoTe_2$ is summarized in Table 2.1[23].

Table 2.1 Summary of the crystallographic data of 2H-$MoTe_2$ as determined by Puotinen and Newnham[23]

Crystal System	**Hexagonal**
Space Group	$P6_3/mmc$
Lattice Parameters	a = 3.519 Å, c = 13.964 Å α=β= 90°, γ= 120°
Z	2

In bulk, it possesses an indirect band gap (~0.9 eV), with a valence band maximum at the K point and a conduction band minimum along the Γ-K symmetry line (Figure 2.3A) [24]. As the number of layers decreases, the band gap widens, reaching ~1.10 eV for a monolayer.

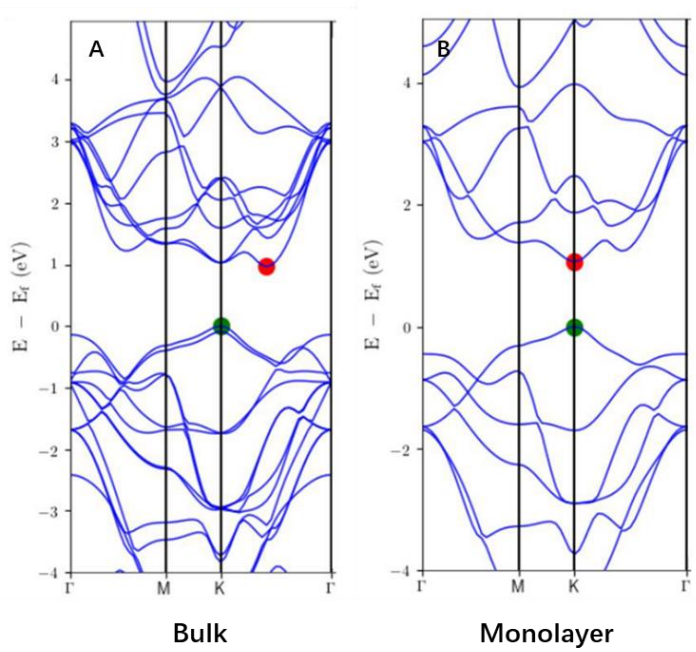


Figure 2.3 Band structure of bulk 2H-$MoTe_2$ (A) and monolayer 2H-$MoTe_2$ (B)[24]

The isolated monolayer of 2H-$MoTe_2$ exhibits a direct band gap, with both the valence band maximum and conduction band minimum located at the K point (Figure 2.3B) [24]. This transition from an indirect to a direct band gap as the material is thinned makes 2H-$MoTe_2$ highly attractive for optoelectronic applications[9,19]. The direct band gap of monolayer 2H-$MoTe_2$ (~1.1 eV) allows for more efficient photon emission and absorption, as both electrons and holes possess the same crystal momentum, enabling direct optical transitions. In contrast, indirect band gap materials, such as crystalline silicon, require electrons to pass through an intermediate state, transferring momentum to the crystal lattice before photon emission can occur[24]. The layer-

dependent nature of the band gap in 2H-$MoTe_2$ is particularly appealing for electronic and optoelectronic applications, including photodetectors, as demonstrated by several studies utilising few-layer 2H-$MoTe_2$ for device fabrication[25–27].

2.2.2 Structure and Properties of 1T-$MoTe_2$

Mo atoms in 1T-$MoTe_2$ are strongly bonded to two Te atom layers, separated by van der Waals forces, forming the monoclinic 1T phase. In this phase, Mo atoms exhibit twisted octahedral coordination with six Te atoms (Figure 2.3)[20], in contrast to the trigonal prismatic coordination seen in 2H-$MoTe_2$.

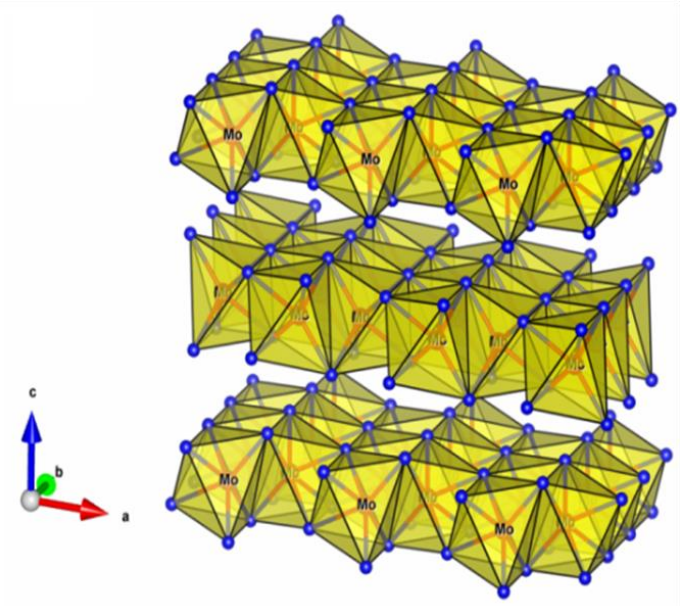


Figure 2.3 Crystal structure of 1T-$MoTe_2$ showing the unit cell and highlighting the Te termination planes of each Te-Mo-Te layer[20].

This results in buckling of the Te sheets as the Mo atoms are displaced from the centre of each {$MoTe_6$} octahedron[28]. Due to this altered crystal symmetry, 1T-$MoTe_2$ exhibits vastly different electronic properties from the semiconducting 2H phase, including metallic conductivity and unique phenomena such as topological superconductivity

and high magnetoresistance[20]. The 1T-$MoTe_2$ polymorph is designated using Ramsdell notation, with 'T' indicating the distorted octahedral structure, and '1' referring to the single full van der Waals layer in the unit cell[29–32]. Crystallographic data for 1T-$MoTe_2$ is summarized in Table 2.2[33].

Table 2.2 Summary of the crystallographic data of 1T-$MoTe_2$ as determined by Brown[33]

Crystal System	Monoclinic
Space Group	$P2_1/m$
Lattice Parameters	a = 6.330 Å, b = 3.469 Å
	c = 13.860 Å, β = 93°
Z	4

As a Weyl semimetal in bulk form, 1T-$MoTe_2$ also shows potential for energy storage and conversion applications[34–36], such as replacing platinum in dye-sensitized solar cells and serving as an electrocatalyst for hydrogen production from water[29–32]. Its metallic conductivity further broadens its scope in energy applications, distinguishing it from the semiconducting nature of 2H-$MoTe_2$[34–36].

2.3 Synthesis and Fabrication Methods for $MoTe_2$ and $MoTe_2$ FETs

Synthesis of controllable materials is the first prerequisite to achieving the requirements of many potential high-performance devices. Therefore, two main methods for preparing 2D semiconductors are considered: “top-down” and “bottom-up”[37].

2.3.1. Top-down Method: Mechanical Exfoliation

In top-down approaches, 2D semiconductors are derived from their bulk counterparts by exfoliating van der Waals (vdW) layers through methods such as mechanical exfoliation, liquid-phase exfoliation, or electrochemical exfoliation[37]. These processes isolate single-layer or few-layer flakes from bulk $MoTe_2$ crystals[38]. The top-down method has become a standard technique for synthesising 2D semiconductors and fabricating 2D field-effect transistors (2D-FETs), with $MoTe_2$ being a natural candidate for this approach. Mechanical exfoliation, in particular, is widely utilised due to the weak vdW interactions between the layers of such materials, allowing the extraction of thin 2D sheets from bulk crystals[39]. Given its simplicity and its historical significance—having been employed by Geim and Novoselov in their pioneering exfoliation of graphene[40] mechanical exfoliation is the focus of this chapter. The micromechanical exfoliation technique, famously involving the use of Scotch tape, opened new avenues for the study of 2D materials (Figure 2.4)[39,40].

In this method, adhesive tape is used to peel off layers from a bulk TMDC material. When the tape is pressed onto the bulk crystal and subsequently peeled away, thin sheets adhere to the tape as its adhesive force overcomes the vdW interactions between layers. These exfoliated sheets can then be transferred onto an insulating substrate, typically SiO_2/Si, where they are identified by optical contrast. Any tape residue left behind can be removed using solvents such as isopropyl alcohol (IPA)[41].

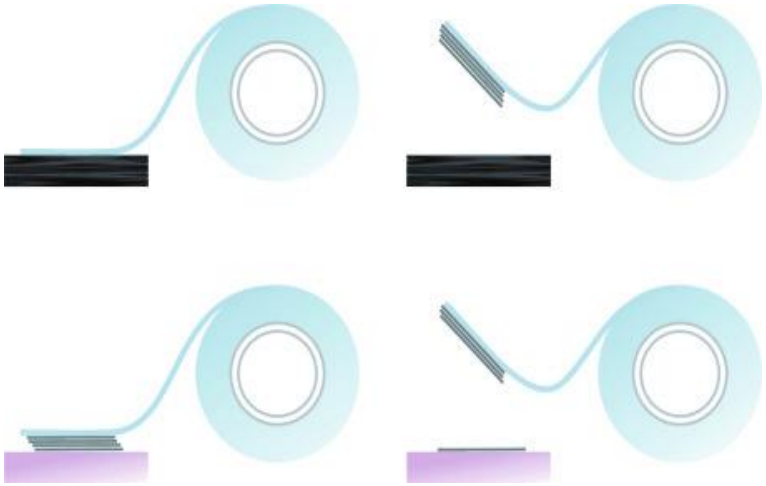


Figure 2.4 The mechanical exfoliation technique ("Scotch tape" method) for producing 2D material. Top: Adhesive tape cleaves the top few layers of graphite from a bulk crystal of the material. Bottom left: The tape with graphitic flakes is then pressed against the substrate of choice. Bottom right: Some flakes stay on the substrate[40].

Figure 2.5 illustrates an example of a $MoTe_2$-FET fabricated using mechanical exfoliation and photolithography[42]. The process can be described as using photolithography to pattern the contact metal, followed by transferring the exfoliated film onto the metal. Despite its advantages, this method has notable limitations, particularly for large-scale, high-throughput production, as the size and shape of the exfoliated flakes are challenging to control [9,43]. Additionally, the quality of crystal edges and regions may be compromised during the exfoliation process, which can negatively impact overall device performance.

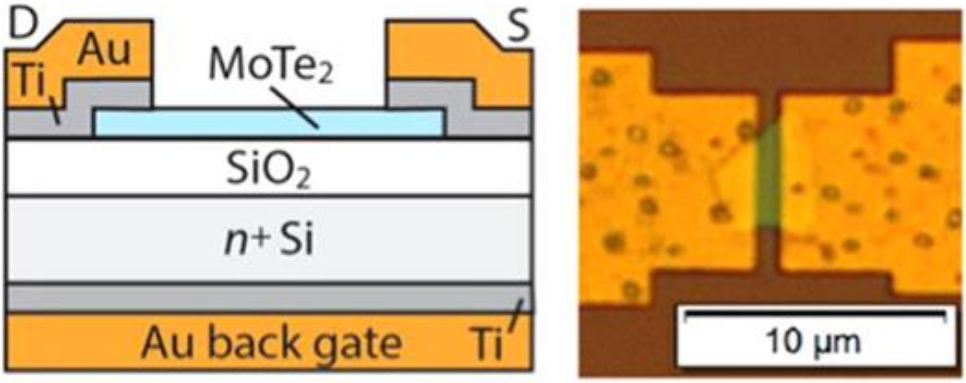


Figure 2.5 Schematic cross-section of a $MoTe_2$ FET and an optical top-view micrograph of the source-drain contacts where the $MoTe_2$ channel flake is visible[42].

2.3.2. Bottom-up Method: Chemical Vapour Deposition (CVD)

The bottom-up method is another widely used approach for preparing 2D semiconductors, offering significant potential for synthesising large-area 2D materials with electronic-grade quality at a reasonable cost. Among these, chemical vapour deposition (CVD) is regarded as the most promising low-cost, high-yield technique, with strong industrial compatibility for the large-scale growth of high-quality TMDCs[44]. Importantly, the morphology, phase, domain size, number of layers, and defect levels of CVD-grown TMDCs can be effectively controlled by adjusting various growth parameters, including temperature, carrier gas flow rate, pressure, growth time, substrate type, and precursor ratios [45–52].

For $MoTe_2$ thin films, the most commonly used synthesis method involves hot-wall CVD at atmospheric pressure, utilising various precursors. Atmospheric pressure CVD is favoured for its simplicity, typically involving a quartz tube capable of withstanding high temperatures and rapid heating/cooling cycles. Essential components of a CVD system include a tube furnace, reaction chamber, flow-controlled carrier gas, connected substrate, and appropriate precursors (Figure 2.6)[53].

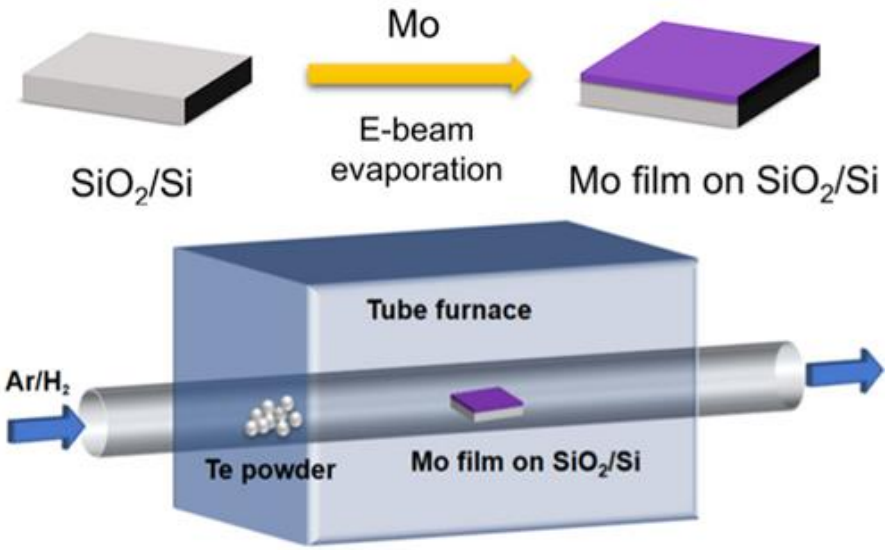


Figure 2.6 Schematic illustration of the synthesis process[53]

In this technique, $MoTe_2$ is synthesised from two material precursors under high temperature and gas flow. One of the key advantages of CVD is its ability to fabricate large-scale films, with the mass and thickness of the precursor layer correlating directly with the final $MoTe_2$ film. The primary limitations in scalability are the size of the substrate and the reaction chamber [38]. This method has been applied in this work and is discussed in detail in Chapter 4, where $MoTe_2$ is synthesised using CVD with $FeTe_2$ as a precursor.

However, a challenge in using the bottom-up approach to fabricate TMDC-based FETs is achieving a clean interface between the gate dielectric and the channel, as this contact area is susceptible to adsorbates and impurities (including solvent and polymer residues) during the fabrication process [54]. Additionally, it is important to note that current methods for batch device fabrication still rely on material transfer processes, which are not ideal for achieving the precise thickness and shape control required for specific device applications.

2.4 $MoTe_2$ Field Effect Transistor (FET)

Since the first demonstration of MoS_2 FET devices, extensive efforts have been made to further explore the material properties and device applications of TMDC semiconductors[55,56]. TMDC-based FETs utilise a thin layer of TMDC material, ranging from a monolayer to several nanometres, to form the conducting channel. Similar to conventional FETs, an electric field modulates the conduction within the channel. In TMDC-based FETs, the electric field polarises the gate dielectric, affecting the channel's conductivity for one carrier type or another. These devices show significant promise for the fabrication of transistor networks with dimensions below 10 nm, offering potential for flexible electronics applications.

$MoTe_2$, in particular, has garnered substantial interest due to its ambipolar transport behaviour and thickness-dependent tuneable band gap[29,57,58]. As the channel thickness increases, $MoTe_2$ FETs exhibit p-type, ambipolar, or n-type characteristics[59]. Theoretically, the maximum carrier mobility in $MoTe_2$ is predicted to be much higher than current experimental values, with reported mobilities of 8,550 $cm^2V^{-1}s^{-1}$ and 16,000 $cm^2V^{-1}s^{-1}$ for p-type and n-type materials, respectively[60]. However, discrepancies between theoretical and experimental results may be attributed to substrate interface effects, surface adsorbates, and material defects[61]. Early studies of $MoTe_2$ FETs on SiO_2/Si substrates reported lower mobilities, in the range of 1 to 20 $cm^2V^{-1}s^{-1}$ [62].

Despite significant advancements, the fabrication of high-performance FETs based on 2D materials continues to face challenges, such as high contact resistance, low Ion/off ratios, poor air stability, and notable hysteresis. However, the absence of dangling bonds and the atomically clean surfaces of TMDCs make them highly suitable for

electrostatic gating and 2D semiconductor channels, with the potential to replace silicon technology. Achieving low contact resistance is critical for maximising the "on" current, enhancing optical response[63,64], and enabling high-frequency operation[63,65].

2.4.1 Field Effect Transistor operation

A field-effect transistor (FET) is a device that controls the current flow through a semiconductor material using an electric field. In an FET, the gate terminal modulates the current between the source and drain by generating an electric field within the semiconductor when a voltage is applied to the gate. Various types of FETs exist, including junction field-effect transistors (JFETs), metal-oxide-semiconductor field-effect transistors (MOSFETs), and metal-semiconductor field-effect transistors (MESFETs). In this work, we focus on a detailed review of MOSFETs.

A MOSFET has three primary terminals: source (S), gate (G), and drain (D). Based on the type of charge carriers that conduct the current, MOSFETs are classified as either n-channel (NMOS) or p-channel (PMOS). Additionally, MOSFETs can operate in either enhancement mode or depletion mode, depending on whether a conducting channel is present or absent when no voltage is applied to the gate terminal.

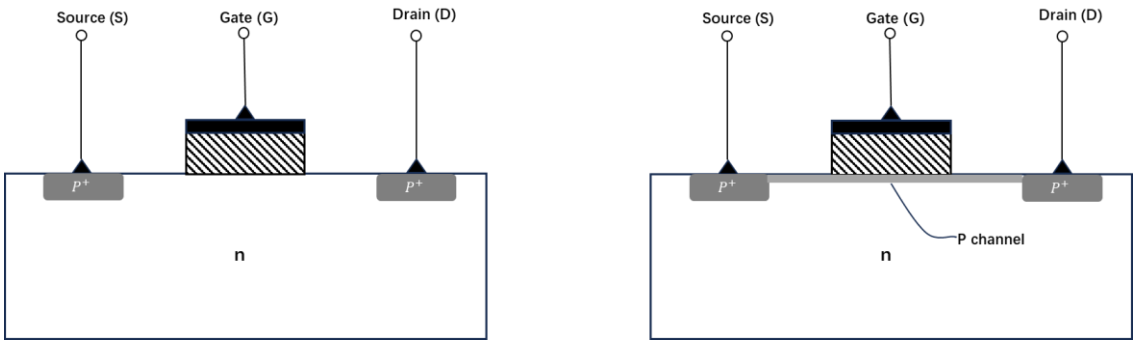


Figure 2.7 p-channel MOSFET cross section. Enhancement mode(left) and depletion mode (right)

In an enhancement-mode PMOS (PMOS-enhancement), there is no conducting channel between the two p-doped regions under zero gate bias, meaning the device

is in the "off" state. When a negative gate voltage (V_G) is applied, it repels electrons in the p-type substrate. Once the applied voltage reaches a certain threshold (V_{Th}), an inversion layer of holes forms beneath the gate, allowing current to flow between the source and drain, thus turning the device "on." This inversion layer acts as a channel for charge carriers to migrate between the source and drain terminals.

Conversely, in a depletion-mode PMOS (PMOS-depletion), a channel exists between the source and drain even when no voltage is applied to the gate. A positive gate bias is required to repel holes from the channel and "turn off" the device. When the device is in the "on" state ($V_G < V_{Th}$), applying a bias between the drain and source terminals drives the migration of carriers through the channel. As the drain bias increases, FETs operate in two distinct regions. Initially, with a small bias between the source and drain (V_{DS}), the device operates in the linear or ohmic region, where the channel behaves like a resistor, and the drain current (I_D) increases linearly with the applied drain voltage.

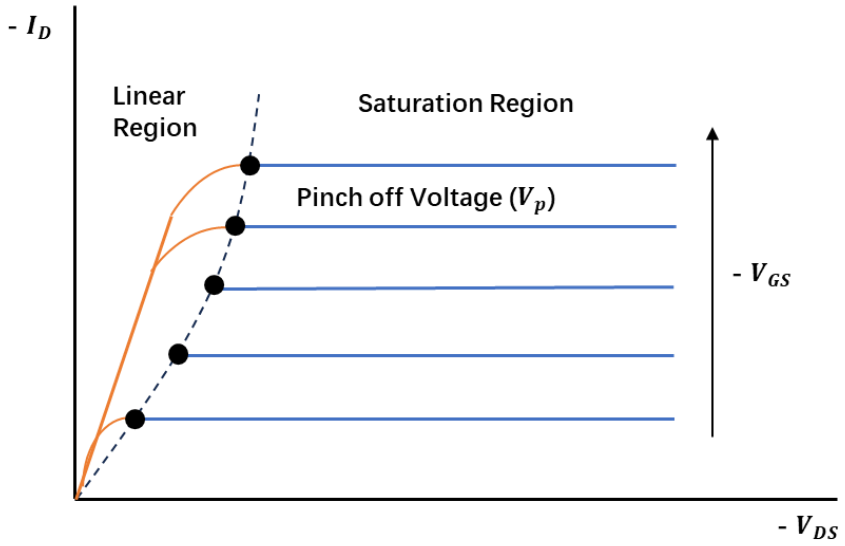


Figure 2.8 p-channel MOSFET I_{DS}-V_{DS} curve

Equation 2.1 expresses the current in the linear region, and W and L are the width and length of the gate terminal, respectively. C_{ox} is the capacitor between the gate metal and semiconductor, and μp is the mobility of holes in the semiconductor.

$$I_D = \frac{W\mu_p C_{ox}}{2L}\left[2(V_{SG} + V_{th})V_{SD} - V_{SD}^2\right] \qquad equation\ (2.1)$$

With drain bias increasing at some point, the bias reaches saturation voltage (V_{sat}), where the thickness of inversion layer near drain terminal reduces to zero that is called pinch-off point.

$$V_{SD(sat)} = V_{SG} + V_{Th} \qquad equation\ (2.2)$$

Beyond this point, the voltage keeps constant with drain bias increasing. That means the number of carriers transported from the source is constant, and the current no longer changes with the drain voltage. This region is the saturation region.

$$I_{D(sat)} = \frac{W\mu_p C_{ox}}{2L}\left(V_{SG} + V_{Th}^2\right) \qquad equation\ (2.3)$$

Figure 2.8 shows the I_D and V_D curve under the ideal situation. The slope on the graph indicates the on-resistance (R_{on}) of the FET device. This resistance comprises a series of resistance that includes the contact resistance ($R_{contact}$), channel resistance ($R_{channel}$) and under gate resistance ($R_{undergate}$).

$$R_{\mathbf{on}} = 2R_{contact} + 2R_a + R_{\mathbf{undergate}} \qquad equaiton\ (2.4)$$

The on/off switching mechanism in conventional integrated circuit FETs is governed by the modulation of the Schottky barrier height through gate biasing. Figures 2.9 illustrate the two most common gate configurations in FETs. In an n-type semiconductor, applying a positive gate bias lowers the conduction and valence bands relative to the Fermi level, aligning the Fermi level with the conduction band. This reduces the width of the Schottky barrier and facilitates electron tunnelling, thereby enabling conduction. Conversely, applying a negative gate bias raises the conduction and valence bands relative to the Fermi level, increasing the Schottky barrier width, which inhibits tunnelling and suppresses conduction.

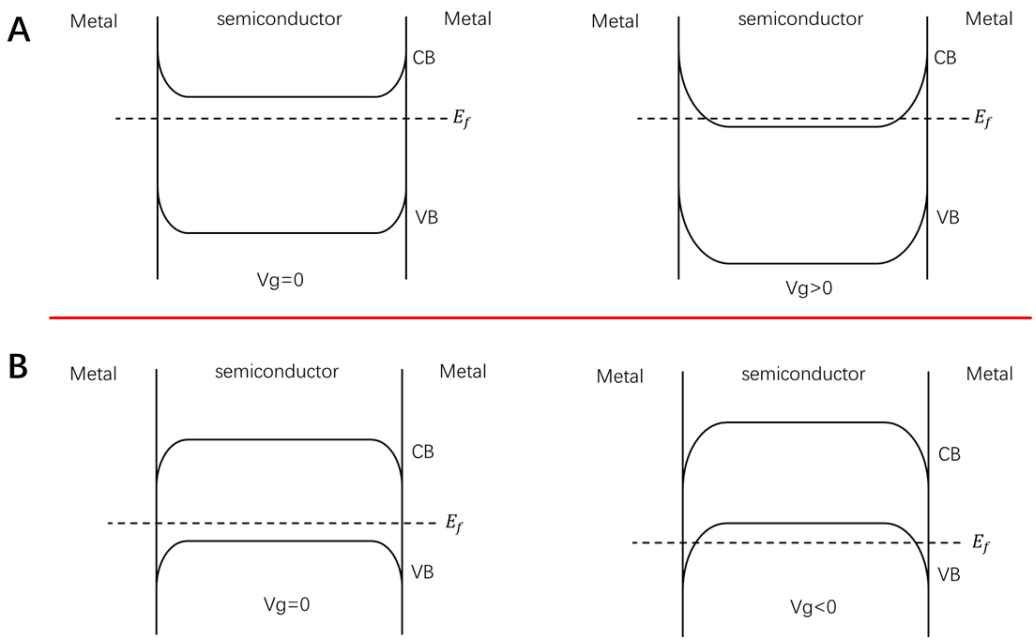


Figure 2.9 (A) A schematic of band bending in a p-type field effect transistor semiconductor with no applied gate voltage and a negative applied gate voltage. (B) A schematic of band bending in an n-type field effect transistor semiconductor with no applied gate voltage and a positive applied gate voltage.

For a p-type semiconductor, the opposite behaviour occurs: a negative gate bias induces conduction, while a positive gate bias inhibits it. At extreme biases, the transistor either reaches its maximum saturation current (the "ON" state) or the current is blocked due to a widened Schottky barrier (the "OFF" state). The ability to modulate the gate bias to toggle between these states is what makes FETs indispensable in electronic switching applications.

2.5 Short Channel Effect (SCEs)

The aggressive downscaling of devices has introduced new challenges, collectively referred to as short-channel effects (SCE), which become significant as the distance between the source and drain regions decreases. In conventional MOSFET architectures, the source and drain junctions create depletion regions that effectively reduce the channel length. This reduction, combined with electric fields penetrating

the channel, weakens the gate's control, as the channel potential is influenced not only by the gate voltage but also by the voltages applied to the source and drain terminals[66]. Figure 2.10 visually depicts this effect, showing how the depletion region at the drain junction expands with increasing drain voltage.

To mitigate SCE, extensive research is being undertaken to identify alternative materials that could replace silicon in future technologies. Among the most promising candidates are III-V semiconductors, germanium, and 2D materials, with the latter gaining significant attention in recent years. The following sections will explore the general properties, potential applications, and primary limitations of these materials.

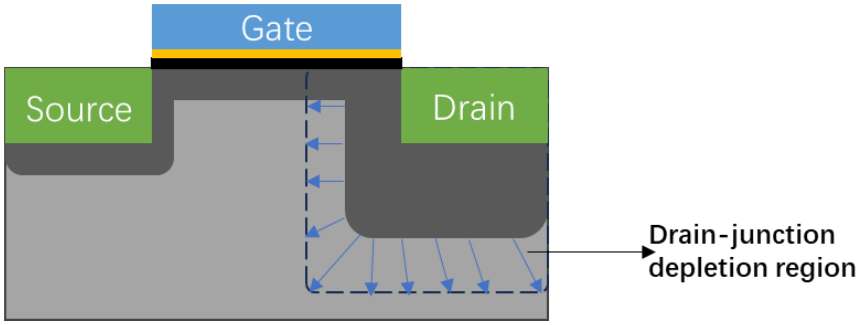


Figure 2.10 example of drain-junction depletion region, responsible for short-channel effect[66]

Another critical issue in modern semiconductor technology is power consumption. Figure 2.11 illustrates the two primary components of power consumption in MOSFET technology as a function of gate length: active power density and subthreshold power density. Active power is primarily determined by the device's operating frequency, while subthreshold power is influenced by leakage currents in the off-state. The former is closely tied to the device's operational speed, with higher frequencies resulting in increased active power consumption.:

$$P_{Act} = CV_{DD}^2 f \qquad equation\ (2.5)$$

where P_{Act} is the active power consumption, C is the load capacitance, V_{DD} is the supply voltage and f is the operation frequency. The latter, subthreshold power consumption, depends on the OFF current, I_{OFF}:

$$\boldsymbol{P_{\text{Sub}} = V_{DD} I_{OFF}} \qquad \boldsymbol{equation\ (2.6)}$$

Although active power consumption can be reduced by scaling down V_{DD}, this approach adversely affects I_{ON}, thereby compromising device performance. This is why, beyond the 100 nm technology node, improvements in device performance no longer relied solely on dimensional scaling,[67]

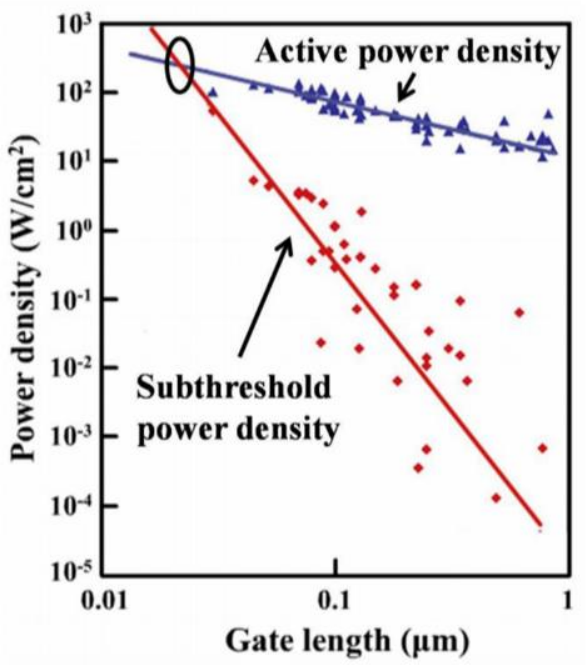


Figure 2.11 Active and subthreshold power densities for Si MOSFETs with respect of gate length. The cross-over point at 20-nm gate length indicates where subthreshold power density surpasses active power density[71].

Instead, enhancements in drive current were achieved through techniques such as increasing carrier mobility via uniaxial strain,[68] incorporating high-k oxides[69], and

introducing novel architectures[70]. As shown in Figure 2.11, for gate lengths below 20 nm, subthreshold power density surpasses active power density[71]. This highlights the need for materials or architectures that can achieve lower I_{OFF} to optimize power consumption in advanced semiconductor technologies.

2.6 Tunnel Field Effect Transistor (TFET)

Transition metal dichalcogenides (TMDCs) have demonstrated significant potential for high-performance electronic devices. Due to their unique properties and two-dimensional nature, TMDCs are especially promising for Tunnel Field-Effect Transistor (TFET) applications. Unlike conventional MOSFETs, TFETs can achieve a subthreshold swing below the theoretical limit of 60 mV/decade, which is critical for developing low-power devices such as portable electronics and sensors[72].

The operational principles of these two architectures differ substantially. As schematically shown in Figure 2.12[72], an n-type MOSFET switches on when the applied gate voltage sufficiently lowers the energy barrier between the source and drain, enabling electron transport through the conduction band of the semiconductor. In contrast, in an n-channel TFET, carriers originate from the valence band in the source. The gate voltage lowers the conduction band in the channel until it overlaps with the valence band in the source, allowing carrier tunnelling.

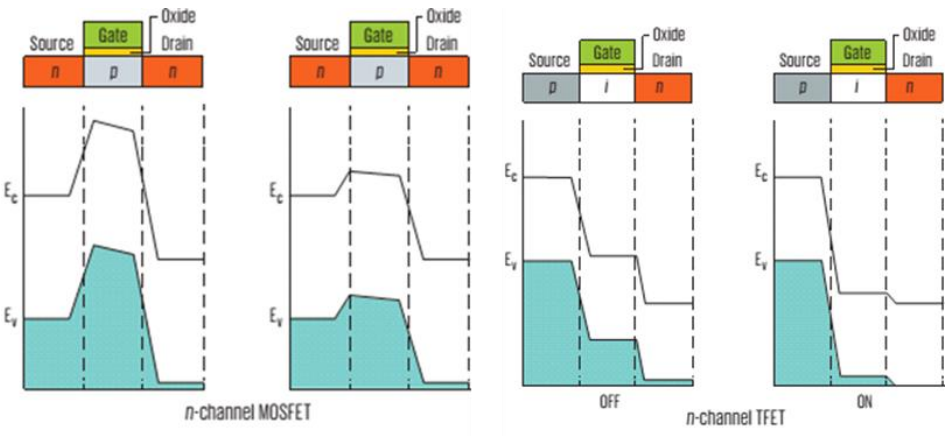


Figure 2.12 Comparison of band diagrams of (a) a n-channel MOSFETs and (b) a n-channel TFET during off and on operation, showing the main difference between their working principle. The terms EC and EV refer to the minimum energy of the conduction band and maximum energy of the valence band, respectively[72].

The differences in bandgap and electron affinity between various TMDCs can be leveraged to achieve optimal alignment of the conduction and valence bands in the source and drain regions, which can be composed of two distinct materials[72,73]. Since both materials are layered, the interface is theoretically free from defect states or dangling bonds, which would otherwise introduce inelastic trap-assisted tunnelling in the OFF-state and degrade device performance[74–76]. In this context, Li et al.[77] conducted theoretical simulations to explore the band alignment in vertically stacked WSe_2 and $SnSe_2$ structures. They reported a subthreshold swing of approximately 14 mV/dec for both p- and n-type TFETs at a V_{DS} of 0.4V, demonstrating superior energy efficiency compared to other architectures. Similarly, Sarkar et al.[78] fabricated a comparable architecture using p-type Germanium and bilayer MoS_2. Although the desired I_{ON} performance was not achieved, a steep subthreshold slope of ~31.1 mV/dec was observed over nearly four orders of magnitude[78].

Although promising, the study and experimental exploration of TFETs based on 2D semiconductors are still in their early stages. To compare the characteristics of 2D materials with other semiconductors, MOSFET architectures can be used as a benchmark, as they have been extensively utilized to analyse and study the properties of these materials. MOSFETs based on TMDCs can be considered analogous to fully depleted SOI due to their intrinsically thin nature, making the study and optimization of this architecture highly relevant.

To better understand their behaviour in relation to short-channel effects (SCE), various properties must be considered. The minimization of SCE can be quantified by considering the natural length (λ), which represents the extent of the electric field lines from the source and drain regions within the channel. For a single-gate MOSFETs, as evaluated by Yan et al.[79], the natural length is expressed as:

$$\boldsymbol{\lambda = \sqrt{\frac{\varepsilon_{Ch}}{\varepsilon_{ox}} t_{Ch} t_{ox}}} \qquad \boldsymbol{equation\ (2.7)}$$

Where $\boldsymbol{\varepsilon_{Ch}}$ is the electrical permittivity of the channel material, $\boldsymbol{\varepsilon_{ox}}$ is the electrical permittivity of the oxide, $\boldsymbol{t_{Ch}}$ is the channel thickness and tox is the oxide thickness. In general, good subthreshold behaviour is achieved when the natural length is 5 to 10 times smaller than the effective channel length[79]. As channel lengths are scaled down to comply with Moore's law, the natural length must also decrease to ensure robust device performance. Although Equation 2.7 was derived for fully depleted SOI and may not be strictly applicable to 2D materials[5], thinner channels tend to be more effective in mitigating short-channel effects (SCE), a trend observed across all semiconductor devices[80].

However, the electrical properties of 3D semiconductors degrade significantly when scaled down to 5–10 nm. To illustrate the impact of material properties at reduced thicknesses, one can initially consider semiconductor carrier mobility. The relatively high mobility of transition metal dichalcogenides (TMDCs) can be attributed to their low effective mass. Figure 2.13 compares the effective masses of various materials, illustrating the inverse relationship between effective mass and carrier mobility. For aggressively scaled devices (sub-5 nm), the reduced distance between the source and drain regions increases the likelihood of quantum mechanical source-drain tunnelling, which degrades the subthreshold swing, increases I_{OFF} and indirectly reduces I_{ON} as gate work functions are adjusted to match specific I_{OFF} values.

Interestingly, materials with lower mobility but higher effective mass could become more suitable for future devices[81–83]. Notably, 2D semiconductors generally exhibit higher effective masses (as seen in Figure 2.13), making them more resistant to SCE. Moreover, both mobility and effective mass can be optimized through strain engineering[84,85], offering another approach to tune the electronic properties of 2D semiconductors.

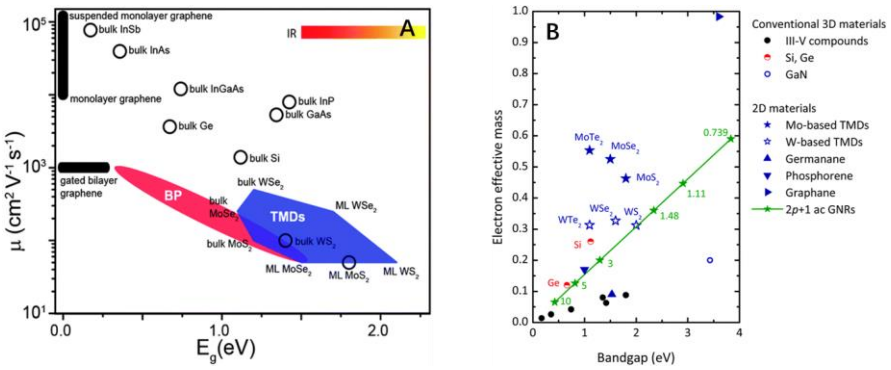


Figure 2.13 (A) Plot of mobilities versus band gap for TMDs, Si, Ge and III-V. The colour scale represents the energy range of visible and infrared light with respect to the band gap energy[80]*. (B) Electron effective mass versus bandgap*[5]*.*

In addition, following Equation 2.7, the natural length λ is also directly proportional to the dielectric constant of the semiconductor, $\boldsymbol{\varepsilon_{Ch}}$. he dielectric constant of TMDCs (~3–6) is generally lower than that of traditional semiconductors like silicon (Si, ~12), germanium (Ge, ~16), or III-V materials (~9–16). Therefore, for the same oxide or channel thickness, the immunity to short-channel effects (SCE) in TMDC-based devices is higher, offering a significant advantage in downscaled architectures. This reduced dielectric constant leads to shorter natural lengths, improving gate control and overall device performance as channels are scaled down.

An additional advantage that applies to both MOSFETs and Tunnel Field-Effect Transistors (TFETs) is the material interface. As introduced in earlier sections, the absence of dangling bonds in TMDCs enhances performance in TFETs by reducing trap-assisted tunnelling. Furthermore, for both MOSFET and TFET architectures, a high-quality semiconductor-oxide interface is critical. In TMDCs, the theoretically perfect interface between the oxide layer and the 2D semiconductor results in a low density of interface traps, which improves subthreshold swing, mobility, and overall device reliability. This perfect interface leads to lower leakage currents and higher device stability over time.

$MoTe_2$, in particular, shows promise for integration into heterojunction TFETs, where different materials are combined to optimize tunnelling efficiency. The defect-free heterostructures that can be formed with $MoTe_2$ further enhance device performance, making it a strong candidate for TFET-based low-power electronics. These factors emphasize the importance of understanding TFETs when researching $MoTe_2$ for semiconductor applications, as combining these technologies could result in significant advancements in energy-efficient electronics.

Table 2.3 Summary of $MoTe_2$ FET fabrication and electrical properties

Substrate	Film Thickness	Type	Mobility	On/Off Ratio	Fab method	Contact metal	Reference
300nm SiO2/Si	2.1nm	p	543.9 cm2/Vs	10^2	CVD+ doping	Te nanoweir	[7]
90nm SiO2/Si	6nm			4.89x10^4	Transfer+Doping	10nm/90nm Ni/Au	[10]
SiO2/Si	5L	ambipolar	25-36	10^4-10^5	Doping	25nm/15nm Ag/Au	[14]
300nm SiO2/Si	5nm	p		101.4	UV+O3+transfer	5nmAg/50nmAu	[22]
300nm SiO2/Si	17nm		8	6x10^3	Transfer+ doping	5nmCr/100nmAu	[23]
300nm SiO2/Si	2.4nm	p	5-50	10^5-10^6		5/50 Ti/Au	[28]
300nm SiO2/Si	28nm	ambipolar	58.9		hBN+UV+transfer	Cr/Au	[42]
300nm SiO2/Si	27.3nm	ambipolar	48	10^7	HfO2+Al2O3+transfer	2nmCr/10nmAu	[32]
30nmSiO2/Si	7-14L	n	129-137	10^6-10^7	80K+AlOx escaple+transfer	Ag	[35]
300nm SiO2/Si	8.4nm	n	8.8	5x10^4	transfer	10Ti/50Au	[45]
300nm SiO2/Si	6.52nm		102.43	10^6	DUV+O2 Doping+ transfer	3nmCr/30nmAu	[53]
300nm SiO2/Si	5.5nm	ambipolar	12		Transfer+doping	10nmPd/50nmAu	[60]
300nm SiO2/Si	5.5nm	ambipolar	154		in suit potassium+transfer	Pd/Au	[55]
300nm SiO2/Si	5-7nm	p	26		chemical doping+transfer	10nmTi/60nmPd	[67]
300nm SiO2/Si	few	p	0.12	6.66x10^2	Transfer+doping	Ni	[74]
300nm SiO2/Si	4L	ambipolar		10^7	hBN encapsulated+laser induced+transfer	1T-MoTe2	[77]
300nm SiO2/Si	8.5nm		15		Transfer+doping	1T-MoTe2	[80]
300nm SiO2/Si	5nm		23		Transfer+doping	1T-MoTe2	[81]

The mobility and carrier type of $MoTe_2$ are strongly influenced by several factors, including contact metal, film thickness, fabrication methods, and doping techniques:

1. Contact Metal: The choice of contact metal plays a significant role in determining the carrier type. High work function metals such as palladium (Pd) and platinum (Pt) tend to favour p-type conduction by facilitating hole injection into the $MoTe_2$ channel. Conversely, low work function metals like titanium (Ti)

and aluminium (Al) promote n-type behaviour, enhancing electron injection. The metal-semiconductor interface significantly affects charge carrier injection efficiency, influencing device performance.

2. Film Thickness: The thickness of $MoTe_2$ has a pronounced impact on its electrical properties. Monolayer $MoTe_2$ typically exhibits higher mobility and ambipolar behaviour, where both electrons and holes can act as charge carriers depending on the applied gate voltage. In contrast, multilayer $MoTe_2$ usually shows p-type conduction with lower mobility. This reduction in mobility in thicker layers is due to increased scattering from interlayer interactions and defects, which impede carrier transport.
3. Fabrication Methods: The quality of $MoTe_2$ films is greatly influenced by the fabrication technique used. Mechanical exfoliation and molecular beam epitaxy (MBE) generally yield higher-quality films with fewer defects, resulting in improved mobility. These methods preserve the crystalline structure better, minimizing grain boundaries and other imperfections. On the other hand, chemical vapor deposition (CVD), while scalable, often introduces grain boundaries and defects, which can degrade mobility due to scattering at the grain boundaries.
4. Doping Techniques: Doping is a critical tool for controlling the carrier type in $MoTe_2$. Electron donors such as alkali metals can introduce n-type behavior by donating electrons to the material, while hole donors (e.g., certain p-type dopants) enhance p-type conduction by creating holes. However, excessive doping can introduce scattering centers, which degrade mobility by increasing carrier scattering and impeding efficient charge transport.

These factors make it essential to optimize the combination of contact metals, thickness, fabrication methods, and doping strategies to achieve the desired electrical performance in $MoTe_2$-based devices. Balancing these parameters is crucial for developing high-performance field-effect transistors (FETs) and other electronic applications using $MoTe_2$.

2.7 Contact Engineering in 2D Semiconductor

One of the most critical factors determining the electronic behaviour of a FET is the interface where the semiconductor meets the metal contact[63,86–88]. This interface plays a pivotal role in influencing whether the device exhibits ohmic or Schottky contact behaviour during conduction. When a semiconductor and a metal come into contact, the Fermi level of the semiconductor is compelled to align with that of the metal. This alignment causes the semiconductor's conduction and valence bands to bend, resulting in the formation of either a depletion region with a Schottky barrier, an accumulation region leading to ohmic contacts, or a flat band condition where neither type of barrier is present. A notable interface phenomenon is Fermi level pinning (FLP), which often prevents the interface from adhering to the ideal Schottky-Mott rule, a behaviour frequently observed in 2D devices [89]. As a member of the TMDC family, $MoTe_2$ is also subject to these challenges.

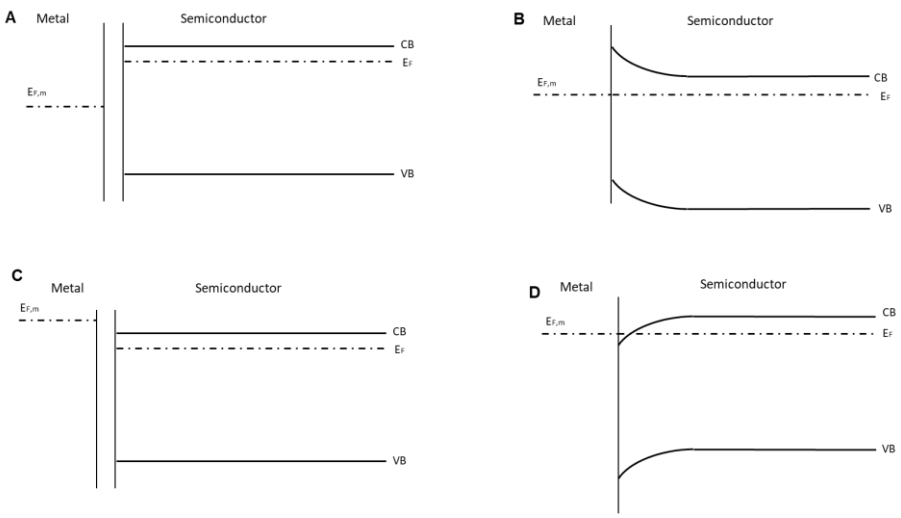


Figure 2.14 A schematic illustration of two types of contact formed by an n-doped semiconductor with a metal. (A) Before contact with a higher work function metal; (B) after contact forming a Schottky contact with the metal; (C) before contact with a lower work function metal; (D) after contact forming an Ohmic contact.

In particular, when an n-type semiconductor is paired with a high work function metal (Figure 2.14 B), or a p-type semiconductor is paired with a low work function metal (Figure 2.15 B), a depletion region forms, where the concentration of charge carriers is reduced, and an energy barrier to conduction develops across the interface. This behaviour arises due to the alignment of the semiconductor's Fermi level with the metal's work function, which causes bending of the semiconductor's conduction and valence bands, resulting in the creation of a depletion region with a corresponding energy barrier.

Conversely, when an n-type semiconductor is paired with a low work function metal (as depicted in Figure 2.14 D), or a p-type semiconductor is combined with a high work function metal (as shown in Figure 2.15 D), a region is formed where charge carriers can accumulate. This occurs only when the Fermi level is sufficiently unpinned. In this configuration, an ohmic contact is established, as charge carriers encounter no barrier

across the interface. Consequently, the resistance to charge carriers is lowered, leading to ohmic behaviour.

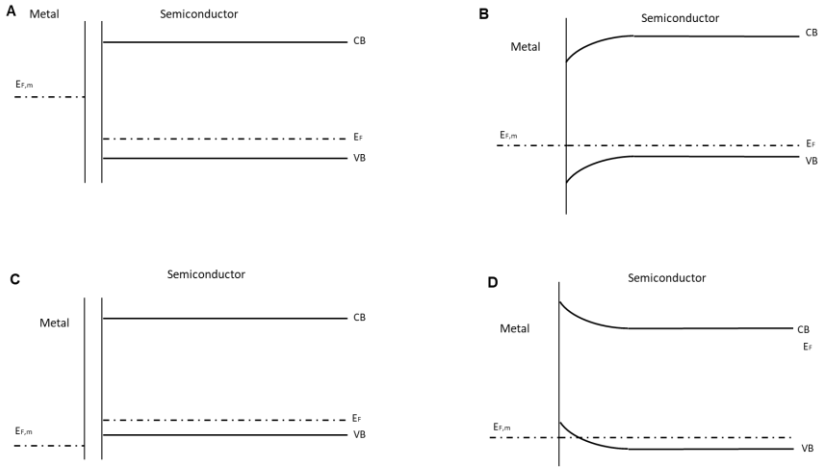


Figure 2.15 A schematic illustration of two types of contact formed by an p-doped. semiconductor with a metal. (A) Before contact with a lower work function metal; (B) after contact forming a Schottky contact with the metal; (C) before contact with a higher work function metal; (D) after contact forming an Ohmic contact.

Compared to silicon, 2D materials possess atomically flat surfaces with extremely low densities of dangling bonds or charge traps, making them highly promising for establishing ohmic contacts with metals. However, conventional doping techniques, widely used in silicon devices, are often ineffective when applied to 2D materials due to their atomically thin nature. Techniques such as heavy doping, ion implantation, or chemical doping with aggressive reactants can severely damage the crystal lattice or introduce significant defects, ultimately degrading the material's properties and performance. As a result, alternative doping approaches are required to preserve the structural integrity and electrical characteristics of 2D materials without compromising their effectiveness[91,92].

Achieving low contact resistance is essential for scaled semiconductor devices, particularly for 2D semiconductors, where minimising this resistance is critical for optimal device performance[63]. The challenge of reducing contact resistance has been extensively studied from material, electrical, and theoretical perspectives. Despite these efforts, there is still no universally reliable process for achieving ohmic contacts with TMDCs, and in many instances, the contact is characterised by high Schottky barriers. Notably, these results span both low and high work-function metals, though no clear trend emerges regarding the influence of varying the metal contact.

To explain the behaviour of 2D-metal contacts, Figures 2.14 and 2.15 show the band diagram of a metal-semiconductor interface before contact. Here, ϕ_M and ϕ_S represent the work functions of the metal and semiconductor, respectively, while qχq\chiqχ denotes the semiconductor's electron affinity. When the metal and semiconductor come into contact, electron migration from the semiconductor to the metal creates a depletion region at the interface, forming a potential barrier[90]. At the semiconductor-metal interface, the potential barrier is determined by the difference between the work functions of the metal and the semiconductor:

$$\boldsymbol{qV_i = q\phi_M - q\phi_S} \qquad \boldsymbol{equation\ (2.8)}$$

On the metal side, the built-in potential barrier formed is known as Schottky barrier height (SBH) and it is given by:

$$\boldsymbol{q\phi_B = q\phi_M - q\chi} \qquad \boldsymbol{equation\ (2.9)}$$

This barrier leads to rectifying behaviour, where current predominantly flows in one direction. When a positive voltage bias is applied to the metal, the potential barrier is

reduced for electrons in the semiconductor, increasing the electron current flow from the semiconductor to the metal. Conversely, when a negative voltage bias is applied, the barrier is raised, reducing the current flow. Importantly, the Schottky barrier height (SBH) remains unchanged in both cases, resulting in a rectifying, non-linear I-V characteristic. A similar mechanism applies to p-type semiconductors, where holes serve as the majority carriers[93].

A further challenge arises from FLP at the metal contact. Das et al.[86] demonstrated that the Schottky barriers between metals and MoS_2 deviate from expectations based on the energy difference between the metal's work function and the semiconductor's Fermi level. Their findings revealed that even metals expected to form p-type contacts exhibited electron injection behaviour consistent with n-type contacts. This pinning effect makes the SBH largely independent of the metal's work function, instead depending on the Schottky pinning factor SSS, as expressed by:

$$q\phi_B = S(q\phi_M - q\phi_{CNL}) + (q\phi_{CNL} - q\chi) \qquad equation(2.10)$$

Where ϕ_{CNL} is the charge neutrality level with respect of the vacuum level and

S is equal to:

$$S = {d\phi_B}/{d\phi_M} \qquad equation\ (2.11)$$

In an unpinned interface, S=1S = 1S=1, meaning the Schottky barrier height (SBH) strictly follows the metal's work function. However, as SSS approaches 0, the interface becomes pinned, rendering the SBH nearly independent of the metal. Contact resistance remains a significant bottleneck in implementing $MoTe_2$ and other TMDCs

in modern technologies. Although several strategies exist for reducing contact resistance and mitigating Fermi level pinning (FLP)—such as interface engineering, doping, annealing, and process optimisation—there remains notable variability in experimental results. Furthermore, any proposed technique must be compatible with standard semiconductor processing and ensure proper device behaviour with minimal short-channel effects (SCE).

Given the nanoscale dimensions and unique properties of 2D materials, establishing a fundamental understanding of 2D/metal contacts is imperative for optimising device performance. In general, 2D materials exhibit two main types of contact geometries: top contact and edge contact. In top contact, metal is deposited directly onto the surface of the 2D material, facilitating easier contact formation between the metal and the semiconductor. By contrast, edge contact involves contacting the 2D material along its edges, resulting in a more limited contact area, which poses challenges in achieving efficient charge injection.

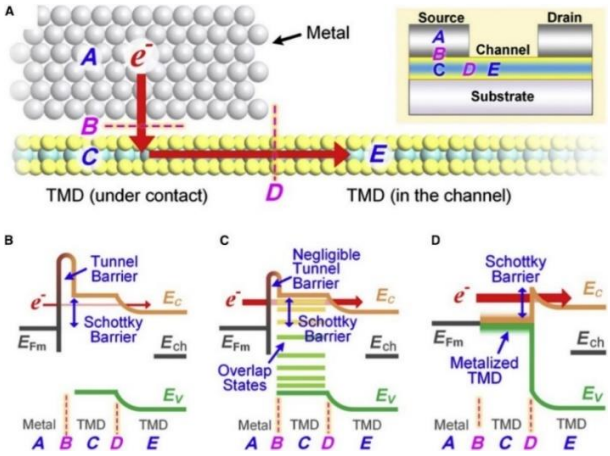


Figure 2.16 (A) Cross-sectional view of current flows through TMDC/metal materials contact. (B) Band diagrams for weak adhesion induced a tunnel barrier (C) Band diagrams for partial orbitals overlap with induced interfacial states inside the TMDC (D) Band diagrams for strong hybridisation with induced metallisation of TMDC[94,95].

Top contact is the more widely adopted method for fabricating 2D FET devices, as it provides greater control and reliability in establishing a robust interface between the metal and the 2D material[63]. In this work, $MoTe_2$ FETs are fabricated using top contact geometry, making it essential to focus on the electronic properties of metals and 2D materials with such contacts.

Zheng et al. (2021demonstrated energy level alignments (ELA) at the interfaces of different TMDC/metal contacts, offering valuable insights into the contact behaviour at these interfaces[95]. The current flows in the direction indicated by the red arrow in their study, with TMDC/metal contacts divided into three categories based on the strength of the interfacial interactions (Figure 2.16 B, C, D). When the interface adhesion between the TMDC and metal is very weak, a van der Waals (vdW) gap forms between the materials, introducing an additional tunnel barrier (Figure 2.16 B). This barrier, along with the Schottky barrier height, limits the efficiency of carrier injection[94].

In cases where metals exhibit strong interaction with the TMDC interface, the tunnel barrier becomes negligible, but metal or surface defects can induce overlapping states (Figure 2.16 C), leading to Fermi level pinning (FLP) at a specific energy level within the TMDC's bandgap[95,96]. This type of contact is prevalent in most 2D devices. In situations where the metal strongly hybridises with the TMDC, metallisation of the TMDC can occur, causing the bandgap to disappear. In such cases, the contact is dominated by an interface within the TMDC itself (Figure 2.16 D), which is thinner and smoother compared to previous configurations. Under these conditions, ohmic contact can be more easily achieved due to the strong hybridisation.

2.8 Reference:

1. Huang, X., Yin, Z., Wu, S., Qi, X., He, Q., Zhang, Q., Yan, Q., Boey, F., & Zhang, H. (2011). Graphene-Based Materials: Synthesis, Characterization, Properties, and Applications. *Small*, *7*(14), 1876–1902. https://doi.org/10.1002/smll.201002009

2. Bolotin, K. I., Sikes, K. J., Jiang, Z., Klima, M., Fudenberg, G., Hone, J., Kim, P., & Stormer, H. L. (2008). Ultrahigh electron mobility in suspended graphene. *Solid State Communications*, *146*(9), 351–355. https://doi.org/10.1016/j.ssc.2008.02.024

3. Ni, Z. H., Yu, T., Lu, Y. H., Wang, Y. Y., Feng, Y. P., & Shen, Z. X. (2008). Uniaxial Strain on Graphene: Raman Spectroscopy Study and Band-Gap Opening. *ACS Nano*, *2*(11), 2301–2305. https://doi.org/10.1021/nn800459e

4. Han, M. Y., Özyilmaz, B., Zhang, Y., & Kim, P. (2007). Energy Band-Gap Engineering of Graphene Nanoribbons. *Physical Review Letters*, *98*(20), 206805. https://doi.org/10.1103/PhysRevLett.98.206805

5. Schwierz, F., Pezoldt, J., & Granzner, R. (2015). Two-dimensional materials and their prospects in transistor electronics. *Nanoscale*, *7*(18), 8261–8283. https://doi.org/10.1039/C5NR01052G

6. Yang, E., Ji, H., & Jung, Y. (2015). Two-Dimensional Transition Metal Dichalcogenide Monolayers as Promising Sodium Ion Battery Anodes. *The Journal of Physical Chemistry C*, *119*(47), 26374–26380. https://doi.org/10.1021/acs.jpcc.5b09935

7. Chhowalla, M., Shin, H. S., Eda, G., Li, L.-J., Loh, K. P., & Zhang, H. (2013). The chemistry of two-dimensional layered transition metal dichalcogenide nanosheets. *Nature Chemistry*, *5*(4), 263–275. https://doi.org/10.1038/nchem.1589

8. Mann, J., Ma, Q., Odenthal, P. M., Isarraraz, M., Le, D., Preciado, E., Barroso, D., Yamaguchi, K., von Son Palacio, G., Nguyen, A., Tran, T., Wurch, M., Nguyen, A., Klee, V., Bobek, S., Sun, D., Heinz, Tony. F., Rahman, T. S., Kawakami, R., & Bartels, L. (2014). 2-Dimensional Transition Metal Dichalcogenides with Tunable Direct Band Gaps: MoS2(1–x)Se2x Monolayers. *Advanced Materials*, *26*(9), 1399–1404. https://doi.org/10.1002/adma.201304389

9. Keum, D. H., Cho, S., Kim, J. H., Choe, D.-H., Sung, H.-J., Kan, M., Kang, H., Hwang, J.-Y., Kim, S. W., Yang, H., Chang, K. J., & Lee, Y. H. (2015). Bandgap opening in few-layered monoclinic MoTe2. *Nature Physics*, *11*(6), Article 6. https://doi.org/10.1038/nphys3314

10. *Tunable Dielectric Properties of Transition Metal Dichalcogenides*. (n.d.). https://doi.org/10.1021/nn201698t

11. Coleman, J. N., Lotya, M., O'Neill, A., Bergin, S. D., King, P. J., Khan, U., Young, K., Gaucher, A., De, S., Smith, R. J., Shvets, I. V., Arora, S. K., Stanton, G., Kim, H.-Y., Lee, K., Kim, G. T., Duesberg, G. S., Hallam, T., Boland, J. J., … Nicolosi, V. (2011).

Two-Dimensional Nanosheets Produced by Liquid Exfoliation of Layered Materials. *Science*. https://doi.org/10.1126/science.1194975

12. Sun, J., Hannon, J. B., Tromp, R. M., Johari, P., Bol, A. A., Shenoy, V. B., & Pohl, K. (2010, November 9). *Spatially-Resolved Structure and Electronic Properties of Graphene on Polycrystalline Ni* (world) [Research-article]. ACS Publications; American Chemical Society. https://doi.org/10.1021/nn102167f

13. Ji, H., Joo, M.-K., Yun, Y., Park, J.-H., Lee, G., Moon, B. H., Yi, H., Suh, D., & Lim, S. C. (2016, July 15). *Suppression of Interfacial Current Fluctuation in MoTe2 Transistors with Different Dielectrics* (world) [Research-article]. ACS Publications; American Chemical Society. https://doi.org/10.1021/acsami.6b02085

14. Radisavljevic, B., Radenovic, A., Brivio, J., Giacometti, V., & Kis, A. (2011). Single-layer MoS2 transistors. *Nature Nanotechnology*, *6*(3), Article 3. https://doi.org/10.1038/nnano.2010.279

15. Iqbal, M. W., Firdous, F., Manzoor, M., Ateeq, H., Azam, S., Aftab, S., Kamran, M. A., Rehman, A. ul, & Majid, A. (2020). Study of electrical attributes of molybdenum ditelluride (MoTe2) FET using experimental and theoretical evidences. *Microelectronic Engineering*, *230*, 111365. https://doi.org/10.1016/j.mee.2020.111365

16. Cho, B., Yoon, J., Lim, S. K., Kim, A. R., Kim, D.-H., Park, S.-G., Kwon, J.-D., Lee, Y.-J., Lee, K.-H., Lee, B. H., Ko, H. C., & Hahm, M. G. (2015). Chemical Sensing of 2D Graphene/MoS2 Heterostructure device. *ACS Applied Materials & Interfaces*, *7*(30), 16775–16780. https://doi.org/10.1021/acsami.5b04541

17. Splendiani, A., Sun, L., Zhang, Y., Li, T., Kim, J., Chim, C.-Y., Galli, G., & Wang, F. (2010). Emerging Photoluminescence in Monolayer MoS2. *Nano Letters*, *10*(4), 1271–1275. https://doi.org/10.1021/nl903868w

18. Mouri, S., Miyauchi, Y., & Matsuda, K. (2013). Tunable Photoluminescence of Monolayer MoS2 via Chemical Doping. *Nano Letters*, *13*(12), 5944–5948. https://doi.org/10.1021/nl403036h

19. Lezama, I. G., Ubaldini, A., Longobardi, M., Giannini, E., Renner, C., Kuzmenko, A. B., & Morpurgo, A. F. (2014). Surface transport and band gap structure of exfoliated 2H-MoTe2 crystals. *2D Materials*, *1*(2), 021002. https://doi.org/10.1088/2053-1583/1/2/021002

20. Fraser, J. P., Masaityte, L., Zhang, J., Laing, S., Moreno-López, J. C., McKenzie, A. F., McGlynn, J. C., Panchal, V., Graham, D., Kazakova, O., Pichler, T., MacLaren, D. A., Moran, D. A. J., & Ganin, A. Y. (2020). Selective phase growth and precise-layer control in MoTe2. *Communications Materials*, *1*(1), Article 1. https://doi.org/10.1038/s43246-020-00048-4

21. Trigunayat, G. C., & Verma, A. R. (1976). Polytypism and Stacking Faults in Crystals with Layer Structure. In F. Lévy (Ed.), *Crystallography and Crystal Chemistry of Materials with Layered Structures* (pp. 269–340). Springer Netherlands. https://doi.org/10.1007/978-94-010-1433-5_6

22. Liu, X.-C., Zhao, S., Sun, X., Deng, L., Zou, X., Hu, Y., Wang, Y.-X., Chu, C.-W., Li, J., Wu, J., Ke, F.-S., & Ajayan, P. M. (2020). Spontaneous self-intercalation of copper atoms into transition metal dichalcogenides. *Science Advances*, *6*(7), eaay4092. https://doi.org/10.1126/sciadv.aay4092

23. *The crystal structure of MoTe2*. (n.d.). https://doi.org/10.1107/S0365110X61002084

24. Jain, A., Ong, S. P., Hautier, G., Chen, W., Richards, W. D., Dacek, S., Cholia, S., Gunter, D., Skinner, D., Ceder, G., & Persson, K. A. (2013). Commentary: The Materials Project: A materials genome approach to accelerating materials innovation. *APL Materials*, *1*(1), 011002. https://doi.org/10.1063/1.4812323

25. Octon, T. J., Nagareddy, V. K., Russo, S., Craciun, M. F., & Wright, C. D. (2016). Fast High-Responsivity Few-Layer $MoTe_2$ Photodetectors. *Advanced Optical Materials*, *4*(11), 1750–1754. https://doi.org/10.1002/adom.201600290

26. Pezeshki, A., Shokouh, S. H. H., Nazari, T., Oh, K., & Im, S. (2016). Electric and Photovoltaic Behavior of a Few-Layer α-$MoTe_2$/MoS_2 Dichalcogenide Heterojunction. *Advanced Materials*, *28*(16), 3216–3222. https://doi.org/10.1002/adma.201504090

27. Kuiri, M., Chakraborty, B., Paul, A., Das, S., Sood, A. K., & Das, A. (2016). Enhancing photoresponsivity using MoTe2-graphene vertical heterostructures. *Applied Physics Letters*, *108*(6), 063506. https://doi.org/10.1063/1.4941996

28. Vellinga, M. B., de Jonge, R., & Haas, C. (1970). Semiconductor to metal transition in MoTe2. *Journal of Solid State Chemistry*, *2*(2), 299–302. https://doi.org/10.1016/0022-4596(70)90085-X

29. Qi, Y., Naumov, P. G., Ali, M. N., Rajamathi, C. R., Schnelle, W., Barkalov, O., Hanfland, M., Wu, S.-C., Shekhar, C., Sun, Y., Süß, V., Schmidt, M., Schwarz, U., Pippel, E., Werner, P., Hillebrand, R., Förster, T., Kampert, E., Parkin, S., … Medvedev, S. A. (2016). Superconductivity in Weyl semimetal candidate MoTe2. *Nature Communications*, *7*(1), Article 1. https://doi.org/10.1038/ncomms11038

30. Yan, B., & Felser, C. (2017). Topological Materials: Weyl Semimetals. *Annual Review of Condensed Matter Physics*, *8*(1), 337–354. https://doi.org/10.1146/annurev-conmatphys-031016-025458

31. Jiang, J., Liu, Z. K., Sun, Y., Yang, H. F., Rajamathi, C. R., Qi, Y. P., Yang, L. X., Chen, C., Peng, H., Hwang, C.-C., Sun, S. Z., Mo, S.-K., Vobornik, I., Fujii, J., Parkin, S. S. P., Felser, C., Yan, B. H., & Chen, Y. L. (2017). Signature of type-II Weyl semimetal phase in MoTe2. *Nature Communications*, *8*(1), Article 1. https://doi.org/10.1038/ncomms13973

32. Yuan, S., Luo, X., Chan, H. L., Xiao, C., Dai, Y., Xie, M., & Hao, J. (2019). Room-temperature ferroelectricity in MoTe2 down to the atomic monolayer limit. *Nature Communications*, *10*(1), Article 1. https://doi.org/10.1038/s41467-019-09669-x

33. Brown, B. E. (n.d.). *The crystal structures of WTe2 and high-temperature MoTe2*. https://doi.org/10.1107/S0365110X66000513

34. Hussain, S., Patil, S. A., Vikraman, D., Mengal, N., Liu, H., Song, W., An, K.-S., Jeong, S. H., Kim, H.-S., & Jung, J. (2018). Large area growth of MoTe2 films as high performance counter electrodes for dye-sensitized solar cells. *Scientific Reports*, *8*(1), Article 1. https://doi.org/10.1038/s41598-017-18067-6

35. McGlynn, J. C., Cascallana-Matías, I., Fraser, J. P., Roger, I., McAllister, J., Miras, H. N., Symes, M. D., & Ganin, A. Y. (2018). Molybdenum Ditelluride Rendered into an Efficient and Stable Electrocatalyst for the Hydrogen Evolution Reaction by Polymorphic Control. *Energy Technology*, *6*(2), 345–350. https://doi.org/10.1002/ente.201700489

36. McGlynn, J. C., Dankwort, T., Kienle, L., Bandeira, N. A. G., Fraser, J. P., Gibson, E. K., Cascallana-Matías, I., Kamarás, K., Symes, M. D., Miras, H. N., & Ganin, A. Y. (2019). The rapid electrochemical activation of MoTe2 for the hydrogen evolution reaction. *Nature Communications*, *10*(1), Article 1. https://doi.org/10.1038/s41467-019-12831-0

37. Tang, L., & Zou, J. (2023). p-Type Two-Dimensional Semiconductors: From Materials Preparation to Electronic Applications. *Nano-Micro Letters*, *15*(1), 230. https://doi.org/10.1007/s40820-023-01211-5

38. Samadi, M., Sarikhani, N., Zirak, M., Zhang, H., Zhang, H.-L., & Moshfegh, A. Z. (2018). Group 6 transition metal dichalcogenide nanomaterials: Synthesis, applications and future perspectives. *Nanoscale Horizons*, *3*(2), 90–204. https://doi.org/10.1039/C7NH00137A

39. Novoselov, K. S., Geim, A. K., Morozov, S. V., Jiang, D., Zhang, Y., Dubonos, S. V., Grigorieva, I. V., & Firsov, A. A. (2004). Electric Field Effect in Atomically Thin Carbon Films. *Science*, *306*(5696), 666–669. https://doi.org/10.1126/science.1102896

40. Novoselov, K. S. (2011). Graphene: Materials in the Flatland (Nobel Lecture). *Angewandte Chemie International Edition*, *50*(31), 6986–7002. https://doi.org/10.1002/anie.201101502

41. Yamamoto, M., Wang, S. T., Ni, M., Lin, Y.-F., Li, S.-L., Aikawa, S., Jian, W.-B., Ueno, K., Wakabayashi, K., & Tsukagoshi, K. (2014). Strong Enhancement of Raman Scattering from a Bulk-Inactive Vibrational Mode in Few-Layer MoTe2. *ACS Nano*, *8*(4), 3895–3903. https://doi.org/10.1021/nn5007607

42. Fathipour, S., Ma, N., Hwang, W. S., Protasenko, V., Vishwanath, S., Xing, H. G., Xu, H., Jena, D., Appenzeller, J., & Seabaugh, A. (2014). Exfoliated multilayer MoTe2 field-effect transistors. *Applied Physics Letters*, *105*(19), 192101. https://doi.org/10.1063/1.4901527

43. Seok, J., Lee, J.-H., Cho, S., Ji, B., Kim, H. W., Kwon, M., Kim, D., Kim, Y.-M., Oh, S. H., Kim, S. W., Lee, Y. H., Son, Y.-W., & Yang, H. (2017). Active hydrogen evolution

through lattice distortion in metallic MoTe2. *2D Materials*, *4*(2), 025061. https://doi.org/10.1088/2053-1583/aa659d

44. Wang, J., Xu, X., Cheng, T., Gu, L., Qiao, R., Liang, Z., Ding, D., Hong, H., Zheng, P., Zhang, Z., Zhang, Z., Zhang, S., Cui, G., Chang, C., Huang, C., Qi, J., Liang, J., Liu, C., Zuo, Y., … Liu, K. (2022). Dual-coupling-guided epitaxial growth of wafer-scale single-crystal WS2 monolayer on vicinal a-plane sapphire. *Nature Nanotechnology*, *17*(1), Article 1. https://doi.org/10.1038/s41565-021-01004-0

45. Xu, X., Zhang, Z., Qiu, L., Zhuang, J., Zhang, L., Wang, H., Liao, C., Song, H., Qiao, R., Gao, P., Hu, Z., Liao, L., Liao, Z., Yu, D., Wang, E., Ding, F., Peng, H., & Liu, K. (2016). Ultrafast growth of single-crystal graphene assisted by a continuous oxygen supply. *Nature Nanotechnology*, *11*(11), Article 11. https://doi.org/10.1038/nnano.2016.132

46. Liu, C., Xu, X., Qiu, L., Wu, M., Qiao, R., Wang, L., Wang, J., Niu, J., Liang, J., Zhou, X., Zhang, Z., Peng, M., Gao, P., Wang, W., Bai, X., Ma, D., Jiang, Y., Wu, X., Yu, D., … Liu, K. (2019). Kinetic modulation of graphene growth by fluorine through spatially confined decomposition of metal fluorides. *Nature Chemistry*, *11*(8), Article 8. https://doi.org/10.1038/s41557-019-0290-1

47. Kim, H.-U., Kanade, V., Kim, M., Kim, K. S., An, B.-S., Seok, H., Yoo, H., Chaney, L. E., Kim, S.-I., Yang, C.-W., Yeom, G. Y., Whang, D., Lee, J.-H., & Kim, T. (2020). Wafer-Scale and Low-Temperature Growth of 1T-WS2 Film for Efficient and Stable Hydrogen Evolution Reaction. *Small*, *16*(6), 1905000. https://doi.org/10.1002/smll.201905000

48. Lin, Y.-C., Yeh, C.-H., Lin, H.-C., Siao, M.-D., Liu, Z., Nakajima, H., Okazaki, T., Chou, M.-Y., Suenaga, K., & Chiu, P.-W. (2018). Stable 1T Tungsten Disulfide Monolayer and Its Junctions: Growth and Atomic Structures. *ACS Nano*, *12*(12), 12080–12088. https://doi.org/10.1021/acsnano.8b04979

49. Umrao, S., Jeon, J., Jeon, S. M., Choi, Y. J., & Lee, S. (2017). A homogeneous atomic layer MoS2(1−x)Se2x alloy prepared by low-pressure chemical vapor deposition, and its properties. *Nanoscale*, *9*(2), 594–603. https://doi.org/10.1039/C6NR07240B

50. Yoo, Y., Degregorio, Z. P., & Johns, J. E. (2015). Seed Crystal Homogeneity Controls Lateral and Vertical Heteroepitaxy of Monolayer MoS2 and WS2. *Journal of the American Chemical Society*, *137*(45), 14281–14287. https://doi.org/10.1021/jacs.5b06643

51. Gao, Y., Hong, Y.-L., Yin, L.-C., Wu, Z., Yang, Z., Chen, M.-L., Liu, Z., Ma, T., Sun, D.-M., Ni, Z., Ma, X.-L., Cheng, H.-M., & Ren, W. (2017). Ultrafast Growth of High-Quality Monolayer WSe2 on Au. *Advanced Materials*, *29*(29), 1700990. https://doi.org/10.1002/adma.201700990

52. Chen, J., Zhao, X., Grinblat, G., Chen, Z., Tan, S. J. R., Fu, W., Ding, Z., Abdelwahab, I., Li, Y., Geng, D., Liu, Y., Leng, K., Liu, B., Liu, W., Tang, W., Maier, S. A., Pennycook, S. J., & Loh, K. P. (2018). Homoepitaxial Growth of Large-Scale Highly

Organized Transition Metal Dichalcogenide Patterns. *Advanced Materials*, *30*(4), 1704674. https://doi.org/10.1002/adma.201704674

53. Zhang, X., Jin, Z., Wang, L., Hachtel, J. A., Villarreal, E., Wang, Z., Ha, T., Nakanishi, Y., Tiwary, C. S., Lai, J., Dong, L., Yang, J., Vajtai, R., Ringe, E., Idrobo, J. C., Yakobson, B. I., Lou, J., Gambin, V., Koltun, R., & Ajayan, P. M. (2019). Low Contact Barrier in 2H/1T′ MoTe2 In-Plane Heterostructure Synthesized by Chemical Vapor Deposition. *ACS Applied Materials & Interfaces*, *11*(13), 12777–12785. https://doi.org/10.1021/acsami.9b00306

54. Ji, H., Joo, M.-K., Yi, H., Choi, H., Gul, H. Z., Ghimire, M. K., & Lim, S. C. (2017). Tunable Mobility in Double-Gated MoTe2 Field-Effect Transistor: Effect of Coulomb Screening and Trap Sites. *ACS Applied Materials & Interfaces*, *9*(34), 29185–29192. https://doi.org/10.1021/acsami.7b05865

55. Yang, Y., Zhu, X., Zhang, K., Zhu, H., Chen, L., & Sun, Q. (2021). Observation of different transport behaviors in a two-dimensional MoTe2 field-effect transistor with engineered gate stack. *Microelectronic Engineering*, *237*, 111497. https://doi.org/10.1016/j.mee.2020.111497

56. Liu, W., Kang, J., Sarkar, D., Khatami, Y., Jena, D., & Banerjee, K. (2013). Role of Metal Contacts in Designing High-Performance Monolayer n-Type WSe2 Field Effect Transistors. *Nano Letters*, *13*(5), 1983–1990. https://doi.org/10.1021/nl304777e

57. Ruppert, C., Aslan, B., & Heinz, T. F. (2014). Optical Properties and Band Gap of Single- and Few-Layer MoTe2 Crystals. *Nano Letters*, *14*(11), 6231–6236. https://doi.org/10.1021/nl502557g

58. Pradhan, N. R., Rhodes, D., Feng, S., Xin, Y., Memaran, S., Moon, B.-H., Terrones, H., Terrones, M., & Balicas, L. (2014, June 4). *Field-Effect Transistors Based on Few-Layered α-MoTe2* (world) [Research-article]. ACS Publications; American Chemical Society. https://doi.org/10.1021/nn501013c

59. Rani, A., DiCamillo, K., Khan, M. A. H., Paranjape, M., & Zaghloul, M. E. (2019). Tuning the Polarity of MoTe2 FETs by Varying the Channel Thickness for Gas-Sensing Applications. *Sensors*, *19*(11), Article 11. https://doi.org/10.3390/s19112551

60. Iqbal, M. W., Iqbal, M. Z., Khan, M. F., Shehzad, M. A., Seo, Y., Park, J. H., Hwang, C., & Eom, J. (2015). High-mobility and air-stable single-layer WS2 field-effect transistors sandwiched between chemical vapor deposition-grown hexagonal BN films. *Scientific Reports*, *5*. Scopus. https://doi.org/10.1038/srep10699

61. Duong, N. T., Park, C., Nguyen, D. H., Nguyen, P. H., Tran, T. U., Park, D. Y., Lee, J., Nguyen, D. A., Oh, J. H., Yu, Y. S., & Jeong, M. S. (2021). Gate-controlled MoTe2 homojunction for sub-thermionic subthreshold swing tunnel field-effect transistor. *Nano Today*, *40*, 101263. https://doi.org/10.1016/j.nantod.2021.101263

62. Ji, H., Lee, G., Joo, M.-K., Yun, Y., Yi, H., Park, J.-H., Suh, D., & Lim, S. C. (2017). Thickness-dependent carrier mobility of ambipolar MoTe2: Interplay between interface

trap and Coulomb scattering. *Applied Physics Letters*, *110*(18), 183501. https://doi.org/10.1063/1.4982680

63. Allain, A., Kang, J., Banerjee, K., & Kis, A. (2015). Electrical contacts to two-dimensional semiconductors. *Nature Materials*, *14*(12), Article 12. https://doi.org/10.1038/nmat4452

64. Lopez-Sanchez, O., Lembke, D., Kayci, M., Radenovic, A., & Kis, A. (2013). Ultrasensitive photodetectors based on monolayer MoS2. *Nature Nanotechnology*, *8*(7), Article 7. https://doi.org/10.1038/nnano.2013.100

65. Krasnozhon, D., Lembke, D., Nyffeler, C., Leblebici, Y., & Kis, A. (2014). MoS2 Transistors Operating at Gigahertz Frequencies. *Nano Letters*, *14*(10), 5905–5911. https://doi.org/10.1021/nl5028638

66. Ferain, I., Colinge, C. A., & Colinge, J.-P. (2011). Multigate transistors as the future of classical metal–oxide–semiconductor field-effect transistors. *Nature*, *479*(7373), Article 7373. https://doi.org/10.1038/nature10676

67. Moore, G. E. (2003). No exponential is forever: But 'Forever' can be delayed! [semiconductor industry]. *2003 IEEE International Solid-State Circuits Conference, 2003. Digest of Technical Papers. ISSCC.*, 20–23 vol.1. https://doi.org/10.1109/ISSCC.2003.1234194

68. Thompson, S., Anand, N., Armstrong, M., Auth, C., Arcot, B., Alavi, M., Bai, P., Bielefeld, J., Bigwood, R., Brandenburg, J., Buehler, M., Cea, S., Chikarmane, V., Choi, C., Frankovic, R., Ghani, T., Glass, G., Han, W., Hoffmann, T., … Bohr, M. (2002). A 90 nm logic technology featuring 50 nm strained silicon channel transistors, 7 layers of Cu interconnects, low k ILD, and 1 /spl mu/m/sup 2/ SRAM cell. *Digest. International Electron Devices Meeting,* 61–64. https://doi.org/10.1109/IEDM.2002.1175779

69. Mistry, K., Chau, R., Choi, C.-H., Ding, G., Fischer, K., Ghani, T., Grover, R., Han, W., Hanken, D., Hattendorf, M., He, J., Allen, C., Hicks, J., Huessner, R., Ingerly, D., Jain, P., James, R., Jong, L., Joshi, S., … Cappellani, A. (2007). A 45nm Logic Technology with High-k+Metal Gate Transistors, Strained Silicon, 9 Cu Interconnect Layers, 193nm Dry Patterning, and 100% Pb-free Packaging. *2007 IEEE International Electron Devices Meeting*, 247–250. https://doi.org/10.1109/IEDM.2007.4418914

70. Auth, C., Allen, C., Blattner, A., Bergstrom, D., Brazier, M., Bost, M., Buehler, M., Chikarmane, V., Ghani, T., Glassman, T., Grover, R., Han, W., Hanken, D., Hattendorf, M., Hentges, P., Heussner, R., Hicks, J., Ingerly, D., Jain, P., … Mistry, K. (2012). A 22nm high performance and low-power CMOS technology featuring fully-depleted tri-gate transistors, self-aligned contacts and high density MIM capacitors. *2012 Symposium on VLSI Technology (VLSIT)*, 131–132. https://doi.org/10.1109/VLSIT.2012.6242496

71. Nowak, E. J. (2002). Maintaining the benefits of CMOS scaling when scaling bogs down. *IBM Journal of Research and Development*, *46*(2.3), 169–180. IBM Journal of Research and Development. https://doi.org/10.1147/rd.462.0169

72. Jena, D. (2013). Tunneling Transistors Based on Graphene and 2-D Crystals. *Proceedings of the IEEE*, *101*(7), 1585–1602. https://doi.org/10.1109/JPROC.2013.2253435

73. Li, M. (Oscar), Esseni, D., Snider, G., Jena, D., & Grace Xing, H. (2014). Single particle transport in two-dimensional heterojunction interlayer tunneling field effect transistor. *Journal of Applied Physics*, *115*(7), 074508. https://doi.org/10.1063/1.4866076

74. Esseni, D., & Pala, M. G. (2013). Interface Traps in InAs Nanowire Tunnel FETs and MOSFETs—Part II: Comparative Analysis and Trap-Induced Variability. *IEEE Transactions on Electron Devices*, *60*(9), 2802–2807. IEEE Transactions on Electron Devices. https://doi.org/10.1109/TED.2013.2274197

75. *Operation and Design of van der Waals Tunnel Transistors: A 3-D Quantum Transport Study | IEEE Journals & Magazine | IEEE Xplore*. (n.d.). Retrieved 13 September 2024, from https://ieeexplore.ieee.org/document/7571124

76. Pala, M. G., & Esseni, D. (2013). Interface Traps in InAs Nanowire Tunnel-FETs and MOSFETs—Part I: Model Description and Single Trap Analysis in Tunnel-FETs. *IEEE Transactions on Electron Devices*, *60*(9), 2795–2801. IEEE Transactions on Electron Devices. https://doi.org/10.1109/TED.2013.2274196

77. Li, M. O., Esseni, D., Nahas, J. J., Jena, D., & Xing, H. G. (2015). Two-Dimensional Heterojunction Interlayer Tunneling Field Effect Transistors (Thin-TFETs). *IEEE Journal of the Electron Devices Society*, *3*(3), 200–207. IEEE Journal of the Electron Devices Society. https://doi.org/10.1109/JEDS.2015.2390643

78. Sarkar, D., Xie, X., Liu, W., Cao, W., Kang, J., Gong, Y., Kraemer, S., Ajayan, P. M., & Banerjee, K. (2015). A subthermionic tunnel field-effect transistor with an atomically thin channel. *Nature*, *526*(7571), Article 7571. https://doi.org/10.1038/nature15387

79. Yan, R.-H., Ourmazd, A., & Lee, K. F. (1992). Scaling the Si MOSFET: From bulk to SOI to bulk. *IEEE Transactions on Electron Devices*, *39*(7), 1704–1710. IEEE Transactions on Electron Devices. https://doi.org/10.1109/16.141237

80. Schmidt, H., Giustiniano, F., & Eda, G. (2015). Electronic transport properties of transition metal dichalcogenide field-effect devices: Surface and interface effects. *Chemical Society Reviews*, *44*(21), 7715–7736. https://doi.org/10.1039/C5CS00275C

81. Sylvia, S. S., Park, H.-H., Khayer, M. A., Alam, K., Klimeck, G., & Lake, R. K. (2012). Material Selection for Minimizing Direct Tunneling in Nanowire Transistors. *IEEE Transactions on Electron Devices*, *59*(8), 2064–2069. IEEE Transactions on Electron Devices. https://doi.org/10.1109/TED.2012.2200688

82. Luisier, M., Lundstrom, M., Antoniadis, D. A., & Bokor, J. (2011). Ultimate device scaling: Intrinsic performance comparisons of carbon-based, InGaAs, and Si field-effect transistors for 5 nm gate length. *2011 International Electron Devices Meeting*, 11.2.1-11.2.4. https://doi.org/10.1109/IEDM.2011.6131531

83. Li, X., Mullen, J. T., Jin, Z., Borysenko, K. M., Buongiorno Nardelli, M., & Kim, K. W. (2013). Intrinsic electrical transport properties of monolayer silicene and MoS 2 from first principles. *Physical Review B*, *87*(11), 115418. https://doi.org/10.1103/PhysRevB.87.115418

84. Castellanos-Gomez, A., Roldán, R., Cappelluti, E., Buscema, M., Guinea, F., van der Zant, H. S. J., & Steele, G. A. (2013). Local Strain Engineering in Atomically Thin MoS2. *Nano Letters*, *13*(11), 5361–5366. https://doi.org/10.1021/nl402875m

85. Lu, N., Guo, H., Li, L., Dai, J., Wang, L., Mei, W.-N., Wu, X., & Zeng, X. C. (2014). MoS2/MX2 heterobilayers: Bandgap engineering via tensile strain or external electrical field. *Nanoscale*, *6*(5), 2879–2886. https://doi.org/10.1039/C3NR06072A

86. Das, S., Chen, H.-Y., Penumatcha, A. V., & Appenzeller, J. (2013). High Performance Multilayer MoS2 Transistors with Scandium Contacts. *Nano Letters*, *13*(1), 100–105. https://doi.org/10.1021/nl303583v

87. Liu, H., Neal, A. T., & Ye, P. D. (2012). Channel Length Scaling of MoS2 MOSFETs. *ACS Nano*, *6*(10), 8563–8569. https://doi.org/10.1021/nn303513c

88. Liu, H., Si, M., Najmaei, S., Neal, A. T., Du, Y., Ajayan, P. M., Lou, J., & Ye, P. D. (2013). Statistical Study of Deep Submicron Dual-Gated Field-Effect Transistors on Monolayer Chemical Vapor Deposition Molybdenum Disulfide Films. *Nano Letters*, *13*(6), 2640–2646. https://doi.org/10.1021/nl400778q

89. Liu, Y., Guo, J., Zhu, E., Liao, L., Lee, S.-J., Ding, M., Shakir, I., Gambin, V., Huang, Y., & Duan, X. (2018). Approaching the Schottky–Mott limit in van der Waals metal–semiconductor junctions. *Nature*, *557*(7707), Article 7707. https://doi.org/10.1038/s41586-018-0129-8

90. Tung, R. T. (董梓則). (2014). The physics and chemistry of the Schottky barrier height. *Applied Physics Reviews*, *1*(1), 011304. https://doi.org/10.1063/1.4858400

91. Zheng, X., Calò, A., Albisetti, E., Liu, X., Alharbi, A. S. M., Arefe, G., Liu, X., Spieser, M., Yoo, W. J., Taniguchi, T., Watanabe, K., Aruta, C., Ciarrocchi, A., Kis, A., Lee, B. S., Lipson, M., Hone, J., Shahrjerdi, D., & Riedo, E. (2019). Patterning metal contacts on monolayer MoS2 with vanishing Schottky barriers using thermal nanolithography. *Nature Electronics*, *2*(1), Article 1. https://doi.org/10.1038/s41928-018-0191-0

92. Jang, J., Kim, Y., Chee, S.-S., Kim, H., Whang, D., Kim, G.-H., & Yun, S. J. (2020). Clean Interface Contact Using a ZnO Interlayer for Low-Contact-Resistance MoS2 Transistors. *ACS Applied Materials & Interfaces*, *12*(4), 5031–5039. https://doi.org/10.1021/acsami.9b18591

93. *The PN Junction Diode by Neudeck, Gerold W.: Good (1983) 1st. | Better World Books*. (n.d.). Retrieved 13 September 2024, from https://www.abebooks.com/first-edition/PN-Junction-Diode-Neudeck-Gerold-W/31458663355/bd

94. Kang, J., Liu, W., Sarkar, D., Jena, D., & Banerjee, K. (2014). Computational Study of Metal Contacts to Monolayer Transition-Metal Dichalcogenide Semiconductors. *Physical Review X*, *4*(3), 031005. https://doi.org/10.1103/PhysRevX.4.031005

95. Zheng, Y., Gao, J., Han, C., & Chen, W. (2021). Ohmic Contact Engineering for Two-Dimensional Materials. *Cell Reports Physical Science*, *2*(1), 100298. https://doi.org/10.1016/j.xcrp.2020.100298

96. Batra, I. P., Tekman, E., & Ciraci, S. (1991). Theory of Schottky barrier and metallization. *Progress in Surface Science*, *36*(4), 289–361. https://doi.org/10.1016/0079-6816(91)90014-U

3.0 Physical and Electrical Characterizations of $MoTe_2$ films and $MoTe_2$-FETs

It is crucial to thoroughly characterise both the surface and electrical properties of $MoTe_2$ following its synthesis and during the fabrication of FETs. This chapter outlines the equipment and methods used to analyse $MoTe_2$ films, as well as the processes employed to assess the performance of $MoTe_2$-based FETs. The primary focus includes techniques such as Scanning Electron Microscopy (SEM), Energy Dispersive X-ray Spectroscopy (EDX), Atomic Force Microscopy (AFM), and Raman spectroscopy to evaluate the crystalline structure and surface roughness of the $MoTe_2$ films. Additionally, the Van der Pauw (VDP) and Transfer Length Method (TLM) techniques are described for characterising the film's electrical properties. Finally, the methods for measuring output and transfer characteristics to demonstrate the electrical performance of $MoTe_2$ FETs are introduced.

3.1 Physical Characterization

3.1.1 Optical Microscopy

An optical microscope uses lenses to magnify images, making them easier for the human eye to observe. It is a highly convenient characterisation tool, commonly employed to inspect the general smoothness of the film surface and the shape of thin films after synthesis. Additionally, it is useful for examining surface details of FET devices with features larger than 1 μm.

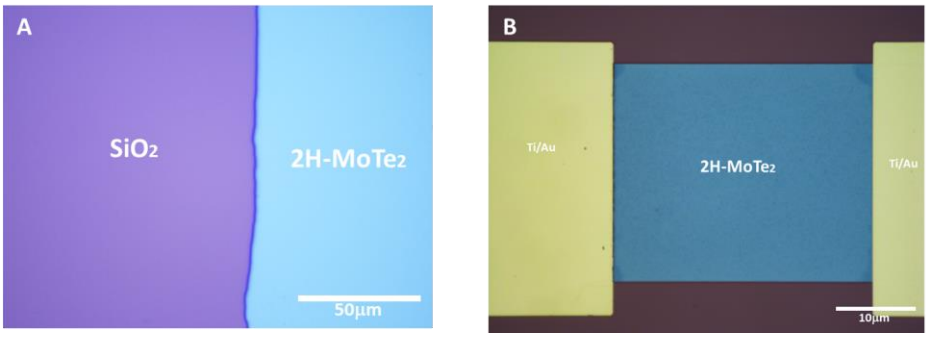


Figure 3.1 example of (A) Optical microscope image of a $MoTe_2$ film showing the bare SiO_2 substrate (purple part) and (B) 2H-$MoTe_2$ FET fabricated on SiO_2/p++Si substrate.

Figure 3.1 presents an example of the characterisation of a $MoTe_2$ film and a $MoTe_2$ FET structure using optical microscopy. However, the resolution of optical microscopy is limited by the system's diffraction limit. Therefore, if features smaller than the micron scale need to be analysed, alternative techniques must be employed.

3.1.2 Scanning Electron Microscopy (SEM) coupled with Energy-Dispersive X-ray Spectroscopy (EDX)

Scanning Electron Microscopy (SEM) operates by bombarding a sample surface with a focused electron beam. The resulting detection signals provide detailed information about the sample's topography and surface morphology. As accelerated electrons interact with the sample surface, they dissipate energy through various signals, such as secondary and backscattered electrons, which are used to form SEM images. With an excellent spatial resolution of approximately 1 nm, SEM is a powerful tool for characterising 2D nanoscale structures.

However, it is important to note that the electron beam can potentially damage 2D films. High-energy electron interactions with materials can displace atoms, create defects, and induce structural changes. For 2D materials like TMDCs, this can lead to

defects, disorder, or even alterations in their electronic or mechanical properties. Despite these risks, SEM remains an indispensable tool for investigating 2D materials. To minimise damage, it is recommended to operate SEM in low-energy mode when characterising these materials in subsequent work.

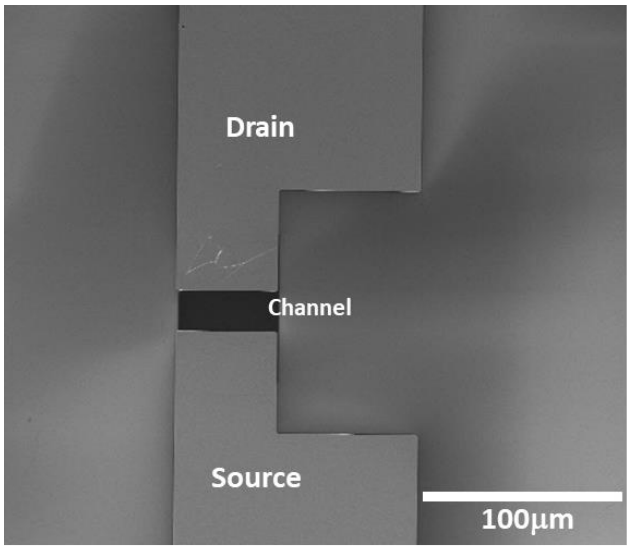


Figure 3.2 Top-down SEM image of the $MoTe_2$ FET

The size of the electron beam spot is determined by the wavelength of the electrons generated by the electron beam source. Figure 3.2 presents a structural image of an exfoliated $MoTe_2$ FET analysed using SEM.

Energy-Dispersive X-ray Spectroscopy (EDX) is another valuable technique for determining local elemental composition and stoichiometry. When exposed to an electron beam, the sample emits X-rays with characteristic energies specific to the elements present. EDX utilises this data to identify the elemental composition of the sample. However, EDX has certain limitations, including the inability to accurately quantify the material's mass[1].

3.1.3 Atomic Force Microscopy (AFM)

For 2D materials, surface roughness and thickness are critical parameters that significantly influence FET performance. Characterising these geometric and surface properties with molecular-level resolution is essential for optimising device performance[2]. In this context, Atomic Force Microscopy (AFM) has emerged as a powerful tool for investigating surface roughness and thickness in 2D-FET research [3]. AFM's versatility allows it to operate under various environmental conditions, such as liquids and gases, making high-resolution surface observations and force measurements relatively straightforward[4].

AFM utilises a physical probe to scan the surface of 2D materials, generating a 3D profile that reveals the film's surface topology, roughness, and thickness. The key components of an AFM system include a probe, laser, photodetector, piezoelectric scanner, and controller. Figure 3.3 illustrates the configuration of an AFM system, and all measurements in this project are conducted at room temperature under ambient air conditions.

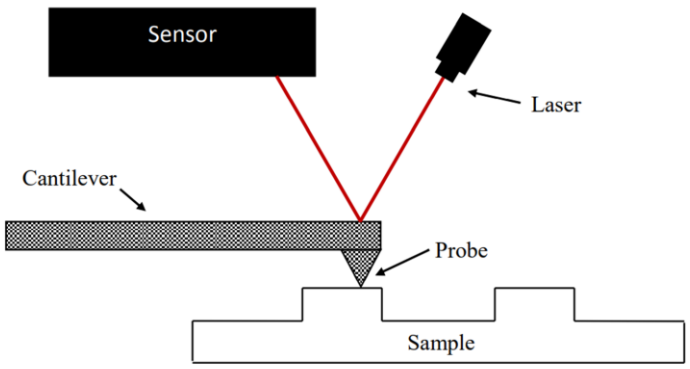


Figure 3.3 Illustration of an AFM setup[5].

The probe consists of a sharp tip, typically with a radius between 2 and 20 nm, attached to the end of a micromachined cantilever, often made from Si or Si_3N_4[2]. A laser beam is reflected from the back of the cantilever, and its position is detected by a four-segment photodiode. The vertical deflection and lateral deformation of the cantilever are measured based on the position of the incident beam on the detector. The probe scans across the sample surface by modulating the piezoelectric scanner in response to applied voltages.

AFM height imaging is used not only to observe flat surface morphology but also to evaluate the size and shape of deposited materials on flat surfaces. Surface roughness is a crucial quantitative parameter derived from height images, and two common metrics are used to assess roughness:

- Average roughness (Ra)**:** This is the arithmetic mean of the height values (Z) within the sampling length. Since Ra averages over the entire sampling length, it is less affected by infrequent surface features such as dirt or scratches. However, Ra does not provide information about surface shape, meaning that very different profiles can yield similar Ra values.
- Root mean square roughness (Rq)**:** This is the square root of the mean of the squares of the Z values over a given sampling length. Unlike Ra, Rq places greater emphasis on larger height deviations, making it more representative of surfaces with less frequent but prominent features. While Rq can be skewed by anomalies like dirt, it is better suited for surfaces with structures such as pillars.

In this study, a Bruker Dimension Icon AFM was used in ScanAsyst mode to measure the surface roughness of CVD-grown $MoTe_2$ films. Figure 3.4 provides an example of the AFM measurement of the $MoTe_2$ surface roughness.

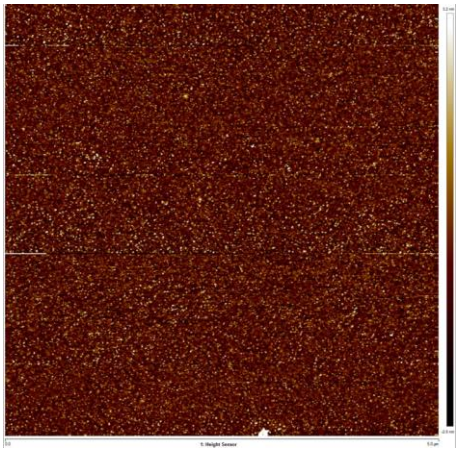


Figure 3.4 An AFM image of the $MoTe_2$ film

The thickness of the $MoTe_2$ film was measured over a 5 μm² area on the bare SiO_2/Si substrate. To accurately measure the film thickness, a method was employed (as shown in Figure 3.5) to create a step between the $MoTe_2$ film and the SiO_2/Si substrate.

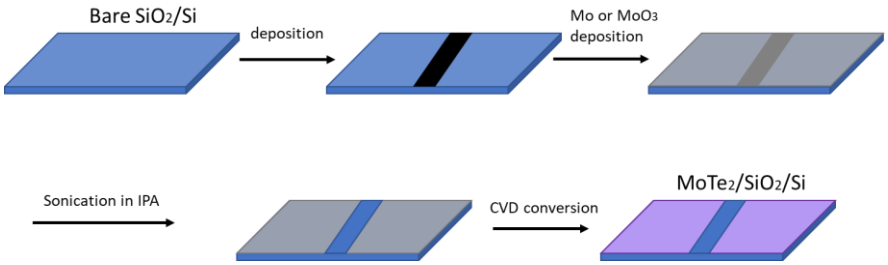


Figure 3.5 Method used to create a step between $MoTe_2$ film and SiO_2/Si substrate for AFM thickness measurements.

This step enabled the precise determination of the film's thickness. After preparing the substrate, it was transferred to a CVD reactor for the $MoTe_2$ conversion reaction, which is detailed in the following chapter. The reaction resulted in the formation of a $MoTe_2$ film with a strip of bare SiO_2/Si, facilitating AFM measurements to determine the film thickness. Figure 3.6 provides an example of using AFM to measure the thickness of the $MoTe_2$ film.

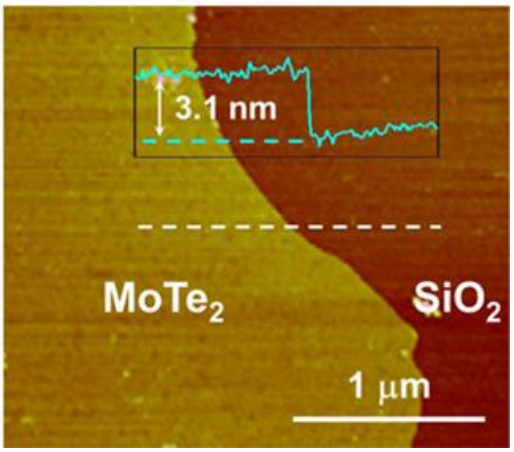


Figure 3.6 AFM image of the CVD-grown $MoTe_2$, the height profile (inset) indicates that the film has a thickness of 3.1 nm[6]

3.1.4 Raman Spectroscopy

Raman scattering is a fundamental spectroscopic technique widely used to investigate molecular vibrations[7]. This method is valuable for identifying substances based on their unique spectral peaks, which provide insights into their chemical structure. Raman spectroscopy primarily involves various interactions between light and matter. In this technique, a monochromatic light source illuminates a sample, and the scattered photons are analysed. When a molecule is exposed to monochromatic light, two types of scattering occur: elastic and inelastic scattering.

In elastic scattering, also known as Rayleigh scattering, the frequency, wavelength, and energy of the photons remain unchanged. In contrast, inelastic scattering, which forms the basis of Raman spectroscopy, involves a shift in photon frequency due to the excitation or relaxation of molecular vibrations. In this process, photons either lose energy (Stokes scattering) or gain energy (anti-Stokes scattering)[8]. As a result, three types of scattering phenomena can be observed: Rayleigh, Stokes, and anti-Stokes scattering[9].

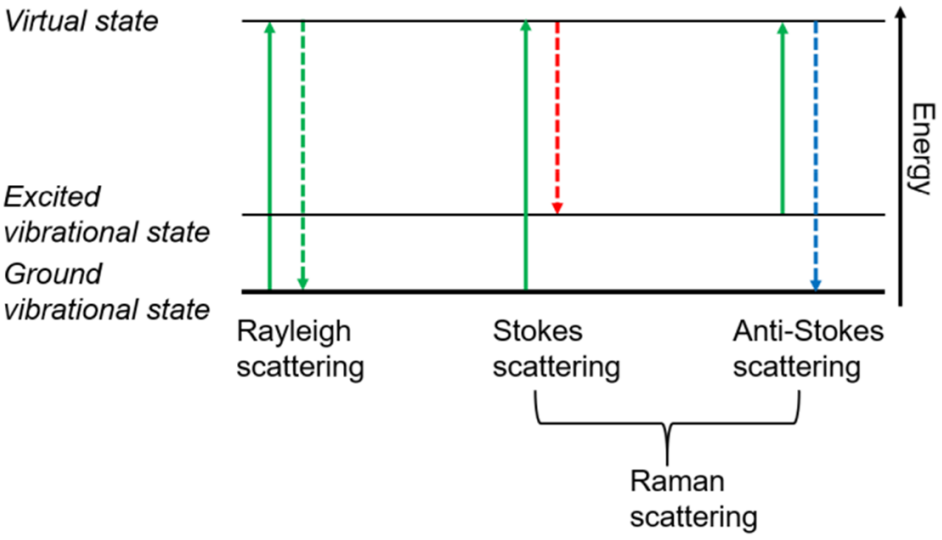


Figure 3.7 Diagram depicting Rayleigh, Stokes, and anti-Stokes scattering processes[10].

Figure 3.7 illustrates the mechanism of Raman scattering. The first is Rayleigh scattering[11]. where incident light interacts with a molecule without any net energy exchange, resulting in scattered light with the same frequency as the incident light. The second type is Stokes Raman scattering [7], where the scattered light has a lower frequency due to energy transfer from the photon to the molecule. Lastly, if the photon gains vibrational energy from the molecule, the scattered light will have a higher frequency than the incident light, a process known as anti-Stokes Raman scattering [12].

Raman spectroscopy has been widely used for the structural characterization and property studies of $MoTe_2$[14,15]. Figure 3.8 presents the Raman spectra for both the 2H and 1T phases of $MoTe_2$. The Raman spectra of the fabricated $MoTe_2$ films were acquired using a Horiba JY HR800 spectrometer, with a 532 nm laser excitation (10 mW laser intensity) and a 600 g/mm grating. For typical measurements, ten spectral acquisitions were performed using a 50× objective, with an accumulation time of 10 seconds per spectrum[12].

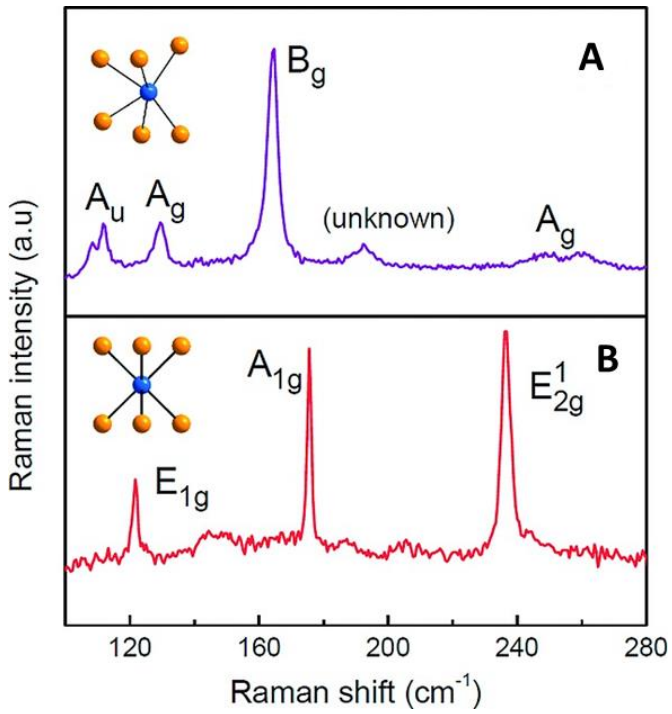


Figure 3.8 Raman spectra of (A) 1T-$MoTe_2$ and (B) 2H-$MoTe_2$ recorded at room temperature using Ar-laser (514.4 nm) excitation[13].

3.1.5 Powder X-Ray Diffraction and Rietveld Refinement (XRD)

X-ray Diffraction (XRD) is a highly versatile technique that provides both chemical and phase information for materials analysis. While XRD traditionally requires crystalline samples, it can also be used to assess the crystallinity of polymers. Although it is commonly employed for bulk sample analysis, advancements in optical systems have made it feasible to analyse thin films, even those less than 10 nm thick [16]. XRD works by exploiting the interference of X-rays scattered by atoms in a material. When X-rays encounter a periodic atomic structure, they are elastically scattered, and diffraction occurs because the atomic spacing is on the same order of magnitude as the wavelength of the X-rays (~100 pm). This scattering can be visualized as the reflection

of X-rays from two parallel atomic planes separated by a distance, *d*. Constructive interference between these waves occurs when the Bragg equation is satisfied.:

$$2d\,sin\theta = n\lambda \qquad equation\ (3.1)$$

where *n* is an integer, *λ* is the X-ray wavelength, *d* is the interplanar spacing, and *θ* is the diffraction angle. When X-rays interact with the ordered atomic arrangement of a crystalline material, they produce a diffraction pattern with reflections at specific angles *θ*, corresponding to different atomic planes (*d*) within the material. Figure 3.9 illustrates the constructive interference described by Bragg's law.

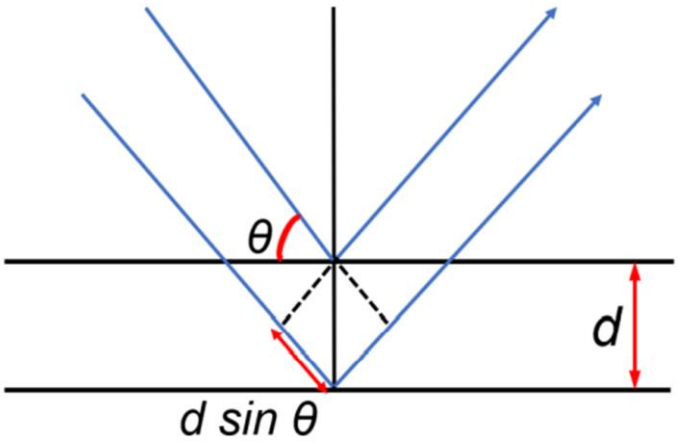


Figure 3.9 Bragg's law, constructive interference between X-rays will occur when the additional path length 2d sin θ equals an integral multiple of the wavelength λ[18].

A PANalytical X'Pert Pro diffractometer, equipped with a Cu Kα radiation source (λ = 1.54178 Å), was utilised in Bragg-Brentano geometry to perform powder X-ray diffraction (PXRD). The resulting diffraction patterns reveal the types and positions of atoms in the material, as X-rays scatter in proportion to the number of electrons in each atom[19]. The angles and intensities of the diffraction peaks provide essential

structural information. This technique was employed to confirm the structure of the $FeTe_2$ powder compounds.

3.2 Electrical Characterisation Method

Various electrical characterisation techniques were employed to evaluate the performance of the $MoTe_2$ films and the fabricated FET devices prepared in this study. These techniques are divided into two categories. The first focuses on material characterisation, which can be assessed using transmission line measurements (TLM) and van der Pauw (VDP) measurements.

3.2.1 Van Der Pauw (VDP) Measurement

The van der Pauw (VDP) measurement technique is a practical and widely used method for evaluating key properties of semiconductor materials, such as carrier concentration, sheet resistance, and carrier mobility. It utilises the Hall effect to characterise the electrical properties of materials, regardless of their geometry, provided the sample has a flat surface and is sufficiently thin compared to its width, essentially forming a two-dimensional (2D) structure.

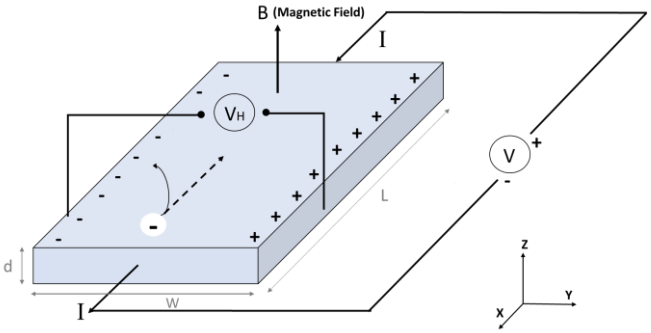


Figure 3.10 Diagram of the Hall Effect with geometry for semiconductors exhibiting electron and hole carriers.

Figure 3.10 illustrates the Hall effect and its corresponding geometry for measuring semiconductor properties. When current flows through a material, an external magnetic field (Bz) causes charge carriers to deviate from their straight path, resulting in charge accumulation along the edges of the material. Eventually, sufficient charge accumulates to counterbalance the Lorentz force, allowing the current to resume a straight trajectory. The potential difference generated between the two sides of the material due to this charge accumulation is referred to as the Hall voltage (V_{Hall})

Figure 3.11 Image of the nanometric HL5500PC hall measurement system

In this work, the Hall effect is utilised for VDP measurements using the "Nano 550 Hall Kit," a 4-probe Hall measurement system, as illustrated in Figure 3.11. The primary purpose of the VDP technique in this project is to evaluate the film after CVD synthesis, ensuring the successful conversion of Mo to $MoTe_2$. However, it is important to note that these measurements are conducted at room temperature under ambient air conditions. Therefore, the results are used for inspection purposes only, rather than for detailed analysis.

3.2.2 Transmission Line Measurement (TLM) and Contact Resistance

Contact resistance ($R_{contact}$) between 2D semiconductors and 3D metal electrodes is a critical factor in the fabrication of 2D FET devices. The interface between 2D semiconductors and metals often suffers from tunnelling barriers, defect-induced interface states, and orbital overlap, all of which can significantly increase $R_{contact}$ at the interface[20]. Accurately characterizing metal contact performance is therefore of paramount importance. Several techniques for measuring $R_{contact}$ have been developed and explored [21–25]. with the TLM being one of the most widely used and comprehensive techniques for extracting $R_{contact}$ values [26]. This section focuses on the application of the TLM method to determine $R_{contact}$ in 2D-FET devices. The advantages and limitations of this approach are discussed, along with critical factors to consider when applying it to 2D materials. TLM is particularly advantageous for extracting both the sheet resistance R_{sheet} of the material and the $R_{contact}$ between the semiconductor and metal electrodes.

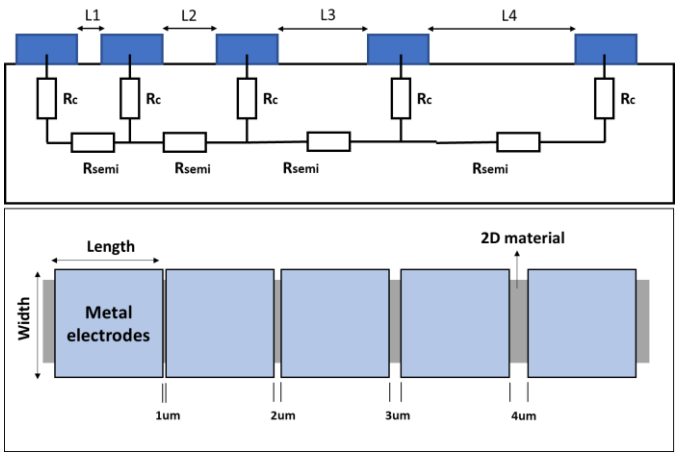


Figure 3.13 TLM structure modelled as a resistor networking, showing increasing gaps between metal and the top view of TLM configuration showing different channel lengths.

In the transmission line method (TLM), multiple contact pads are fabricated in a geometry where the channel length, or the spacing between the contacts, varies (denoted L_1, L_2, etc.), while the contact dimensions remain constant. Figure 3.13 illustrates the typical TLM geometry. A potential difference is applied between two ohmic contacts, and the resulting current is measured to calculate the resistance using Ohm's law. The total resistance between adjacent contacts is then plotted as a function of the distance between the contacts. If the contact resistance remains constant and the sheet resistance (R_{sheet}) of the material is uniform, the plot will exhibit a linear relationship.

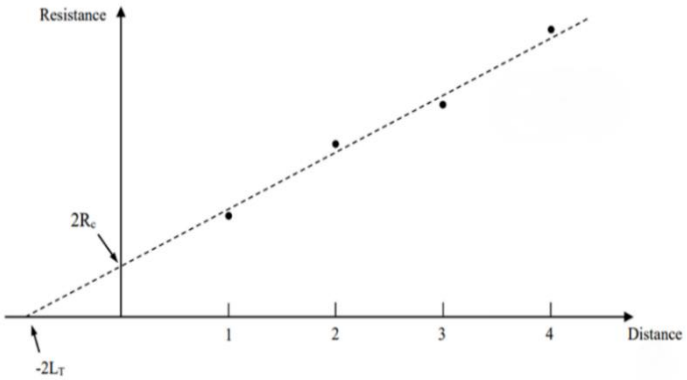


Figure 3.14 A linear fit of the plot of R_{total} versus channel length giving rise to $R_{contact}$, R_{sheet} and L_T

The total resistance (R_{total}) between two contacts is a function of the metal electrode length and can be described as:

$$\boldsymbol{R_{total} = 2R_{contact} + R_{semi}} \qquad \boldsymbol{equation\ (3.2)}$$

Where R_{total} is the contact resistance at the interface, and R_{semi} is the resistance of the semiconductor channel between the contacts. Given that $R_{contact} \gg R_{metal}$ (where R_{metal} represents the negligible resistance of the metal electrodes due to their high

conductivity), the contribution of R_{metal} is typically disregarded, simplifying the expression for R_{total} as:

$$\boldsymbol{R_{\text{total}} = 2R_{\text{contact}} + R_{\text{sheet}} \frac{L}{W}} \qquad \boldsymbol{equation\ (3.3)}$$

Where R_{sheet} is the sheet resistance of the semiconductor, L is the length between the contacts, and WWW is the width of the semiconductor channel.

The intercept of the linear fit at zero distance provides 2 $R_{contact}$ while the slope of the line gives R_{sheet}, the sheet resistance of the material, according to the equation:

$$\boldsymbol{R_{sheet} = \text{ Slope x } W} \qquad \boldsymbol{equation\ (3.4)}$$

TLM is widely adopted for determining $R_{contact}$ and R_{sheet} in 2D-FETs due to its straightforward fabrication and analysis process. This technique provides valuable insights into the contact and material resistances, which are essential for optimizing the performance of 2D semiconductor devices.

3.3 Summary

This chapter outlines the characterisation and measurement procedures employed for MoTe2 films synthesized via CVD. The methods used to analyse the surface morphology and structural properties of $MoTe_2$ include optical microscopy, SEM, AFM, Raman spectroscopy, and XRD. Additionally, electrical characterisation techniques, such as TLM and VDP measurements, are employed to evaluate the electrical quality and performance of the fabricated 2D films.

3.4 Reference:

1. Goldstein, J. I., Newbury, D. E., Michael, J. R., Ritchie, N. W. M., Scott, J. H. J., & Joy, D. C. (2018). *Scanning Electron Microscopy and X-Ray Microanalysis*. Springer. https://doi.org/10.1007/978-1-4939-6676-9

2. Ishida, N. (2024). Chapter 4—Atomic force microscopy. In A. Otsuki, S. Jose, M. Mohan, & S. Thomas (Eds.), *Non-Destructive Material Characterization Methods* (pp. 89–125). Elsevier. https://doi.org/10.1016/B978-0-323-91150-4.00011-2

3. Binnig, G., Quate, C. F., & Gerber, Ch. (1986). Atomic Force Microscope. *Physical Review Letters*, *56*(9), 930–933. https://doi.org/10.1103/PhysRevLett.56.930

4. Chen, X., Li, B., Liao, Z., Li, J., Li, X., Yin, J., & Guo, W. (2022). Principles and Applications of Liquid-Environment Atomic Force Microscopy. *Advanced Materials Interfaces*, *9*(35), 2201864. https://doi.org/10.1002/admi.202201864

5. Crawford, K. G. (2017). *Surface transfer doping of diamond using transition metal oxides* [PhD, University of Glasgow]. https://eleanor.lib.gla.ac.uk/record=b3289324

6. Zhou, L., Xu, K., Zubair, A., Liao, A. D., Fang, W., Ouyang, F., Lee, Y.-H., Ueno, K., Saito, R., Palacios, T., Kong, J., & Dresselhaus, M. S. (2015). Large-Area Synthesis of High-Quality Uniform Few-Layer MoTe2. *Journal of the American Chemical Society*, *137*(37), 11892–11895. https://doi.org/10.1021/jacs.5b07452

7. Das, R. S., & Agrawal, Y. K. (2011). Raman spectroscopy: Recent advancements, techniques and applications. *Vibrational Spectroscopy*, *57*(2), 163–176. https://doi.org/10.1016/j.vibspec.2011.08.003

8. Bertrand, M. J. (1998). Handbook of Instrumental Techniques for Analytical Chemistry Edited by Frank A. Settle. Prentice Hall: Upper Saddle River. 1997. xxi + 995 pp. ISBN 0-13-177338-0. *Journal of the American Chemical Society*, *120*(26), 6633–6633. https://doi.org/10.1021/ja975671k

9. Willard, H. H., Merritt, J., Dean, J. A., & Settle, J. (1988). *Instrumental methods of analysis, 7th edition*. https://www.osti.gov/biblio/5209599

10. *Modern Raman Spectroscopy* (1st ed.). (2019). John Wiley & Sons, Ltd. https://doi.org/10.1002/9781119440598

11. Raman Spectroscopy in Daily Lab-life. (2013). In *Practical Raman Spectroscopy – An Introduction* (pp. 101–148). John Wiley & Sons, Ltd. https://doi.org/10.1002/9781119961284.ch5

12. Fleischmann, M., Hendra, P. J., & McQuillan, A. J. (1974). Raman spectra of pyridine adsorbed at a silver electrode. *Chemical Physics Letters*, *26*(2), 163–166. https://doi.org/10.1016/0009-2614(74)85388-1

13. Jana, M. K., Singh, A., Sampath, A., Rao, C. N. R., & Waghmare, U. V. (2016). Structure and Electron-Transport Properties of Anion-Deficient MoTe2: A Combined Experimental and Theoretical Study. *Zeitschrift Für Anorganische Und Allgemeine Chemie*, *642*(23), 1386–1396. https://doi.org/10.1002/zaac.201600314

14. Abstreiter, G. (1991). Micro-Raman spectroscopy for characterization of semiconductor devices. *Applied Surface Science*, *50*(1), 73–78. https://doi.org/10.1016/0169-4332(91)90141-6

15. Gouadec, G., & Colomban, P. (2007). Raman Spectroscopy of nanomaterials: How spectra relate to disorder, particle size and mechanical properties. *Progress in Crystal Growth and Characterization of Materials*, *53*(1), 1–56. https://doi.org/10.1016/j.pcrysgrow.2007.01.001

16. Nasrazadani, S., & Hassani, S. (2016). Chapter 2—Modern analytical techniques in failure analysis of aerospace, chemical, and oil and gas industries. In A. S. H. Makhlouf & M. Aliofkhazraei (Eds.), *Handbook of Materials Failure Analysis with Case Studies from the Oil and Gas Industry* (pp. 39–54). Butterworth-Heinemann. https://doi.org/10.1016/B978-0-08-100117-2.00010-8

17. Whittig, L. D., & Allardice, W. R. (1986). X-Ray Diffraction Techniques. In *Methods of Soil Analysis* (pp. 331–362). John Wiley & Sons, Ltd. https://doi.org/10.2136/sssabookser5.1.2ed.c12

18. Pecharsky, V. K., & Zavalij, P. Y. (Eds.). (2009). Fundamentals of Crystalline State and Crystal Lattice. In *Fundamentals of Powder Diffraction and Structural Characterization of Materials* (pp. 1–15). Springer US. https://doi.org/10.1007/978-0-387-09579-0_1

19. Mathew, S., Abraham, A. R., Chintalapati, S., Sarkar, S., Joseph, B., & Venkatesan, T. (2020). Temperature Dependent Structural Evolution of WSe2: A Synchrotron X-ray Diffraction Study. *Condensed Matter*, *5*(4), Article 4. https://doi.org/10.3390/condmat5040076

20. Choi, M. S., Qu, D., Lee, D., Liu, X., Watanabe, K., Taniguchi, T., & Yoo, W. J. (2014). Lateral MoS2 p–n Junction Formed by Chemical Doping for Use in High-Performance Optoelectronics. *ACS Nano*, *8*(9), 9332–9340. https://doi.org/10.1021/nn503284n

21. Xu, Y., Gwoziecki, R., Chartier, I., Coppard, R., Balestra, F., & Ghibaudo, G. (2010). Modified transmission-line method for contact resistance extraction in organic field-effect transistors. *Applied Physics Letters*, *97*(6), 063302. https://doi.org/10.1063/1.3479476

22. Berger, H. H. (1972). Models for contacts to planar devices. *Solid-State Electronics*, *15*(2), 145–158. https://doi.org/10.1016/0038-1101(72)90048-2

23. Chern, J. G. J., & Oldham, W. G. (1984). Determining specific contact resistivity from contact end resistance measurements. *IEEE Electron Device Letters*, *5*(5), 178–180. https://doi.org/10.1109/EDL.1984.25875

24. Mohney, S. E., Wang, Y., Cabassi, M. A., Lew, K. K., Dey, S., Redwing, J. M., & Mayer, T. S. (2005). Measuring the specific contact resistance of contacts to semiconductor nanowires. *Solid-State Electronics*, *49*(2), 227–232. https://doi.org/10.1016/j.sse.2004.08.006

25. Kamimura, K., Okada, S., Nakao, M., Onuma, Y., & Yamashita, S. (2002). Characterization of contact resistance of low-value resistor by transmission line model (TLM) method. *Electronics and Communications in Japan (Part II: Electronics)*, *85*(3), 16–22. https://doi.org/10.1002/ecjb.1095

26. Mitta, S. B., Choi, M. S., Nipane, A., Ali, F., Kim, C., Teherani, J. T., Hone, J., & Yoo, W. J. (2020). Electrical characterization of 2D materials-based field-effect transistors. *2D Materials*, *8*(1), 012002. https://doi.org/10.1088/2053-1583/abc187

4.0 $MoTe_2$ Synthesis, Characterization and Application

A critical step towards the practical application of $MoTe_2$, as outlined in the introductory chapter, is the fabrication of high-quality, large-area, atomically thin $MoTe_2$ films. Initial studies on $MoTe_2$ primarily relied on top-down exfoliation methods to obtain material flakes. While exfoliation produces high-quality flakes, these are typically small, irregularly shaped, and randomly distributed on the substrate, which limits scalability for industrial applications[1–4]. Consequently, alternative methods for the synthesis of $MoTe_2$ must be explored if it is to be integrated into future technologies.

Recent studies have shown that using 2H-$MoTe_2$ as an interface material with metallic 1T-$MoTe_2$ is more effective for creating ohmic contacts than traditional metals. However, current experimental findings suggest that synthesising pure phases of both 1T- and 2H-$MoTe_2$ simultaneously on the same substrate under chemical vapour deposition (CVD) conditions remains challenging. A review of previous experiments indicates that additional modifications, such as patterning or electrostatic doping of the synthesised materials, may be required to achieve this.

From a manufacturing perspective, CVD-based synthesis methods in an industrial setting present significant challenges, particularly due to the multiple processing steps involved and the high costs associated with efficient precursor materials. Therefore, developing a reliable method for growing thin films of both $MoTe_2$ polymorphs simultaneously on a single substrate remains a key focus, especially when exploring cost-effective precursor alternatives.

The primary objective of this chapter is to explore a novel CVD process for the preparation of pure-phase $MoTe_2$ and to identify a viable alternative to traditional tellurium (Te) precursors. Atomic force microscopy (AFM), X-ray diffraction (XRD), and Raman spectroscopy were employed to characterise the phase structure and assess the quality of the 1T- and 2H-$MoTe_2$ films synthesised using this new CVD approach. Additionally, if experimental conditions permit, the feasibility of simultaneously depositing 1T- and 2H-$MoTe_2$ films on the same substrate under unified conversion conditions will also be investigated.

4.1 Background of CVD Synthesis $MoTe_2$

Optimising the CVD process and systematically analysing the variables affecting the system can lead to a more efficient and cost-effective synthesis compared to the methods described in Chapter 2. Unlike other molybdenum-based transition metal dichalcogenides (TMDCs), such as MoS_2 and $MoSe_2$, $MoTe_2$ typically does not adopt a hexagonal structure unless grown via CVD[5–7]. The two polymorphs of $MoTe_2$, 1T and 2H, are in direct competition during deposition at typical CVD temperatures (~650 °C) due to the small energy difference between the two phases (~0.36 eV per formula unit), as illustrated in Figure 4.1. This small energy gap makes the 2H phase thermodynamically more stable than the 1T phase, enabling relatively easy phase transitions with minimal energy input. This phase flexibility holds significant potential for future applications of $MoTe_2$[8].

The polymorphism of $MoTe_2$ presents both a challenge and an exciting opportunity. Specifically, the ability to manipulate CVD parameters to control phase purity opens up possibilities for producing phase-pure thin films of either 1T- or 2H-$MoTe_2$.

Optimising these parameters can enhance the technological potential of $MoTe_2$ for various applications.

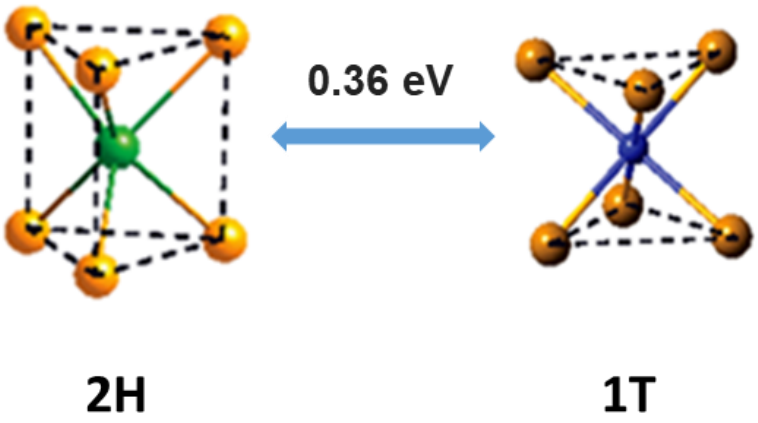


Figure 4.1 depiction of the energy difference between the $MoTe_2$ polymorphs per formula which under the room temperature and the air atmosphere[8]

Initial investigations into $MoTe_2$ were based on flakes produced through top-down exfoliation. However, varying CVD parameters can produce pure-phase films of either 1T- or 2H-$MoTe_2$. Tellurium (Te) has been widely used as the primary raw material for CVD reactions in numerous past experimental studies.

To develop more robust and cost-effective synthesis methods, multiple experiments are required to evaluate the impact of various factors, such as synthesis environment, temperature, gases, and precursors, on the final product. As summarised in Table 4.1, different molybdenum sources (e.g., Mo films or MoO_3 films) can produce both 1T- and 2H-$MoTe_2$ with distinct structural properties when using Te as the chalcogen precursor. The data indicate that MoO_3 tends to preferentially form the 2H-$MoTe_2$ phase, whereas Mo favours the formation of the 1T-$MoTe_2$ phase. These findings

demonstrate that the choice of precursor plays a critical role in determining the crystal structure of the synthesised $MoTe_2$.

Table 4.1 Conditions used for the CVD of 2H-$MoTe_2$ and 1T-$MoTe_2$ on SiO_2/Si substrate reported in literature: broken down into controllable variables.

$MoTe_2$ crystalline structure	Mo Source	Te Source (g)	Substrate Temperature (℃)	Source Temperature (℃)	Time (min)	Heating Cooling Rate ℃/ min	Gas, flow rate (sccm)	Ref.
2H	Mo film (1-3 nm)	Te (0.8)	635	635	60	40.67/ open furnace after growth period	H2/Ar 5/5	[4]
	Mo fim (3nm)	Te	700		120	50/ natural cooling to 500 ℃	H2/Ar 7.5/42.5	[5]
	MoO_2 film (30 nm)	Te	700	600	60	17.5/-	H2/Ar	[12]
	Mo film (50 nm)	Te(2)	650	650	180	30/5	H2/Ar 100/500	[16]
	MoO_3 film	Te(0.1)	650	650	30	natural cooling to. 500 ℃	H2/Ar 4/3	[17]
1T	Mo film (1-3 nm)	Te (0.8)	635	535	60	40.6/ open furnace after growth period	H2/Ar 5/5	[4]
	Mo fim (3nm)	Te	800	-	120	50/ natural cooling to 500 ℃	H2/Ar 7.5/42.5	[5]
	MoO_2 film (30 nm)	Te	800	600	60	20/-	H2/Ar	[12]
	Mo film (50 nm)	Te(2)	650	650	20	30/5	H2/Ar 100/500	[16]
	MoO_3 film	Te(0.1)	650	650	30	-/open furnace after growth period	H2/Ar 4/3	[17]

For tellurium (Te) sources, key factors such as vapor temperature and pressure must be carefully controlled. The deposition of $MoTe_2$ is highly sensitive to both the substrate temperature and the temperature of the Te vapor source. Specifically, the deposition rate of 2H-$MoTe_2$ increases significantly with higher tellurium vapor temperatures and pressures. In contrast, lowering the Te source temperature and vapor pressure favours the formation of the 1T-$MoTe_2$ phase. As indicated in Table 4.1, 1T-$MoTe_2$ is more likely to form at higher substrate temperatures, while 2H-$MoTe_2$ remains more stable at lower substrate temperatures. This behaviour is attributed to differences in Te vacancy concentrations at varying substrate temperatures[11].

4.2 Experimental Method

4.2.1 Substrate Structure and Cleaning

The primary substrate used in this work is SiO_2/Si (12 mm²), a widely utilised platform for studying 2D materials. Optical microscopy allows for rapid, non-destructive determination of the thickness of 2D materials through the optical contrast provided by the SiO_2 layer[9,10]. Additionally, this substrate remains stable in various chemical environments at elevated temperatures ranging from 600 to 1000 °C, making it suitable for high-temperature processes. Its frequent use in the semiconductor industry and compatibility with advanced manufacturing technologies facilitate the future integration of $MoTe_2$.

The substrates used in this study were sourced from Inseto. Prior to processing, the substrates were thoroughly cleaned using an ultrasonic bath in acetone for 10 minutes, followed by cleaning with isopropyl alcohol (IPA). The substrates were then dried under a stream of nitrogen (N_2), and their cleanliness was verified through optical microscopy inspection.

4.2.2 Mo and MoO_3 Deposition

Various techniques such as thermal evaporation, electron beam evaporation, atomic layer deposition, and sputter deposition can be employed to deposit precursor films, allowing precise control over the resultant 2D film thickness. These methods offer the advantages of ease of operation and the ability to fabricate large-area films with controllable shape and geometry. In this study, a Plassys MEB550s electron-beam evaporator was used to deposit high-purity molybdenum (99.95%) films onto SiO_2/Si substrates via electron beam physical vapor deposition (EBPVD). The electron beam

gun operated with an emission current of 220 mA, achieving a deposition rate of 0.07 nm/s under a vacuum of 1×10^{-6} mbar.

Conversely, MoO_3 films were deposited by thermal evaporation using 99.99% Pi-Kem MoO_3 in a Plassys MEB400 system under a vacuum of 2×10^{-6} mbar. A quartz crystal microbalance was utilised in both deposition systems to ensure precise control over the Mo and MoO_3 film thickness, with an accuracy of 99%[11].

4.2.3 Synthesis and Characterization of $FeTe_2$ Precursor

A pestle and mortar were used to mix tellurium (Te, Alfa Aesar, 99.999%) and iron (Fe, Alfa Aesar, 99+%) powders in stoichiometric proportions. The resulting powder mixture was placed in a silica boat and transferred to the hot zone of a Renton tube furnace. The furnace temperature was ramped from room temperature to 500 °C at a rate of 10 °C/min, held at this temperature for 14 hours, and then cooled back to room temperature at the same rate. Figure 4.2 shows the chemical vapour deposition (CVD) system used for synthesising $FeTe_2$. During the reaction, a gas mixture of 5% H_2/Ar was continuously pumped through the furnace at a flow rate of 300 sccm.

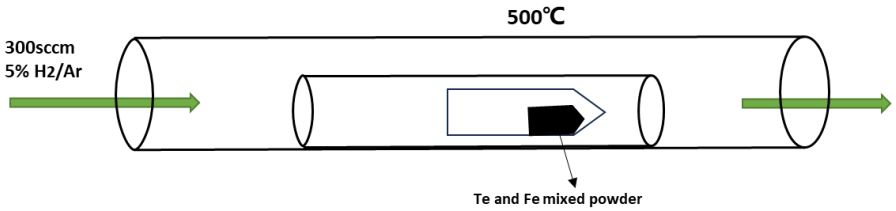


Figure 4.2 Schematic of the flow CVD reactor for synthesis of the $FeTe_2$

In this work, $FeTe_2$ is primarily utilized as a precursor for the synthesis of $MoTe_2$ thin films, offering an advantage over pure Te by fully utilizing the Te content and allowing for recyclability. The use of metallic Te powder as a Te source is well-documented, with

literature indicating that over 100mg of Te is typically required for $MoTe_2$ thin film synthesis, which is considered excessive[12–14].

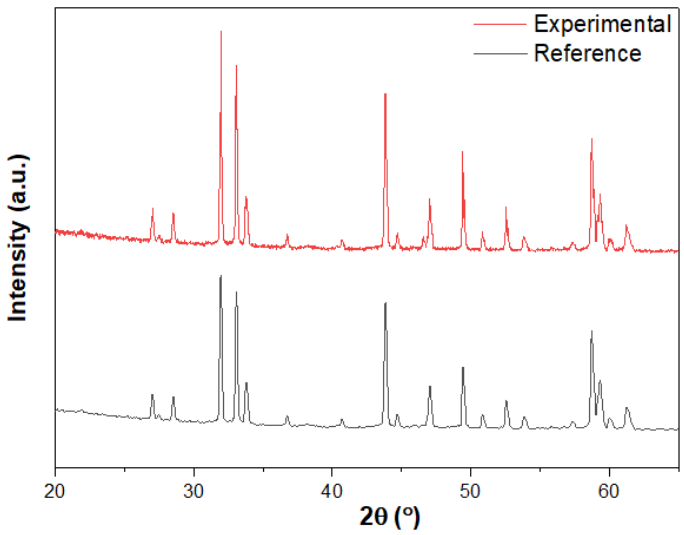


Figure 4.3 XRD patterns of synthesised $FeTe_2$ *and referenced data comparison*[15].

Figure 4.3 compares the powder X-ray diffraction (PXRD) pattern of the synthesized $FeTe_2$ with reference data, demonstrating the successful synthesis of phase-pure $FeTe_2$. Given that tellurium (Te) is the primary chalcogen in the synthesis, maintaining a continuous and stable supply of Te throughout the deposition process is critical. Additionally, thermogravimetric analysis (TGA) of the synthesized $FeTe_2$ indicates that it decomposes at approximately 600 °C. As shown in Figure 4.3, the PXRD patterns of the synthesized $FeTe_2$ closely match those of the simulated $FeTe_2$, with most peaks aligning precisely, thus confirming the phase purity of the product used in the CVD process.

4.3 CVD system for synthesising $MoTe_2$

4.3.1 Flow CVD setup and synthesis process

A CVD setup with an open-flow system is depicted in Figure 4.4. Approximately 300 mg of Te or $FeTe_2$ powder was placed into a 14.5 cm quartz tube (12 mm inner diameter, 15 mm outer diameter), positioned 5 cm upstream of the SiO_2/Si substrate, which had either Mo or MoO_3 deposited on it for conversion to $MoTe_2$. The quartz tube was then inserted into a 50.5 cm quartz working tube (inner diameter: 22 mm, outer diameter: 25 mm) to ensure that the substrate was positioned in the hot zone of the Lenton tube furnace.

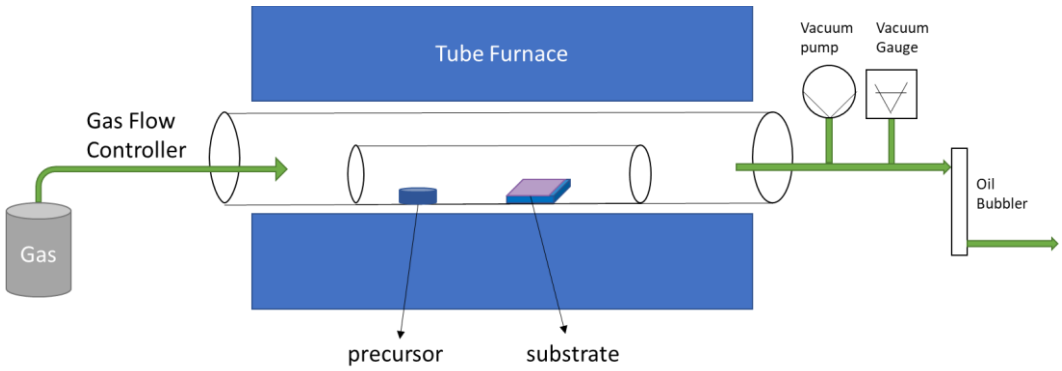


Figure 4.4 Schematic of the flow CVD reactor

As described, the CVD system consists of a quartz tube connected to a vacuum pump and instrumentation for process control. The vacuum pump evacuates the reactor to create an oxygen-free environment, while a vacuum gauge monitors the pressure to ensure effective evacuation. Pure argon (Ar) and a 5% hydrogen/argon (H_2/Ar) gas mixture are introduced into the reaction chamber via a three-way valve. The CVD process follows these steps:

1. The system pressure is reduced to 1 × 10^{-2} mbar, and 5% H_2/Ar gas is introduced. This step is repeated three times to ensure minimal oxygen contamination in the reactor.
2. The tube furnace is then heated to the desired temperature at a rate of 5°C per minute, while the carrier gas flow is maintained at 300 sccm.
3. The furnace is held at the target temperature for 4 hours, after which it is cooled to room temperature at the same rate of 5°C per minute.

The primary objective of the experiments in this chapter is to identify suitable substitutes for elemental Te and to optimize the conditions for synthesizing pure phases of 1T- and 2H-$MoTe_2$. By employing this CVD system, experimental conditions for the synthesis of these pure phases were established. Key parameters such as residence time, precursor type, and precursor temperature were varied to assess their influence on $MoTe_2$ synthesis, with both Te and $FeTe_2$ used as experimental precursors.

After conducting comparative tests and characterizations, $FeTe_2$ was determined to be an effective substitute for Te as a precursor. In prior studies, Mo and MoO_3 films were pre-deposited on substrates and subsequently tellurized into $MoTe_2$ using elemental Te. However, the low evaporation temperature of Te, combined with extended synthesis times, led to rapid Te depletion, resulting in $MoTe_2$ evaporation and poor-quality films.

In contrast, using $FeTe_2$ as a precursor offered improved control over the residence time, significantly impacting the crystal morphology of the resulting $MoTe_2$ film. The final phase of the $MoTe_2$ film was determined by the Mo precursor, enabling the production of pure-phase 2H- and 1T-$MoTe_2$ films. $FeTe_2$ pellets are easy to handle,

requiring approximately 300 mg for synthesis. A 300 nm SiO_2/Si substrate was used for the deposition of the precursor film, with $MoTe_2$ growth confirmed by observing the contrast change in the substrate's colour.

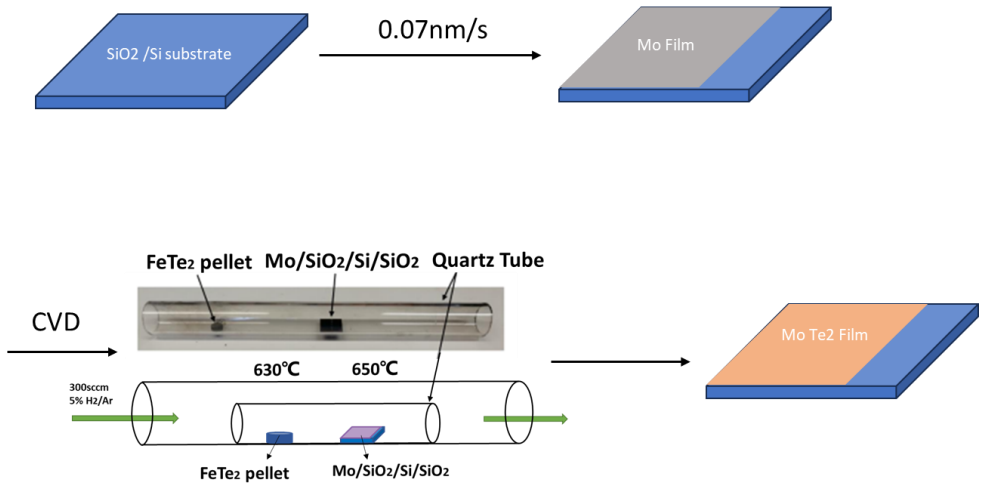


Figure 4.5 Film transformation in each step and the temperature change in the furnace for the $MoTe_2$ *CVD process*

When the tube is inserted into the working zone of the Lenton tube furnace, the substrate is positioned centrally within the heating zone. After placing the various precursor films inside the reactor, $FeTe_2$ particles were positioned 5 cm upstream in the reaction tube. To minimize oxygen contamination, the system was evacuated three times to a pressure of 2×10^{-2} mbar before initiating the CVD process. Figure 4.5 illustrates the molybdenum deposition process via CVD and the corresponding temperature profile of the furnace. The substrate was held at a dwell temperature of 650°C, while the $FeTe_2$ pellet was maintained at 630°C for 4 hours. Slow heating and cooling rates of 5°C/min were used, with a 5% H_2/Ar gas mixture bubbled through at a flow rate of 300 sccm. The same procedure was followed to convert the MoO_3 deposit into 1T-$MoTe_2$.

X-ray diffraction (XRD) was employed to evaluate the crystallinity of the synthesized $MoTe_2$. The peak positions in the XRD pattern provide insights into the crystal structure and lattice parameters of the material. The intensity of the peaks is influenced by the atomic arrangement, crystal orientation, and overall crystallinity of the sample. Two prominent peaks corresponding to the (002) and (004) planes, which are perpendicular to the c-axis of the hexagonal lattice, are characteristic of $MoTe_2$ in XRD analysis.

In this experiment, the reaction temperature was identified as a critical factor influencing the synthesis process. Previous studies have indicated that common temperatures for $MoTe_2$ synthesis range from 600°C to 700°C, with typical settings at 600°C, 650°C, and 700°C. Figure 4.6 presents the XRD results of the synthesized product, which were used to determine the optimal temperature and evaluate the quality of the material produced.

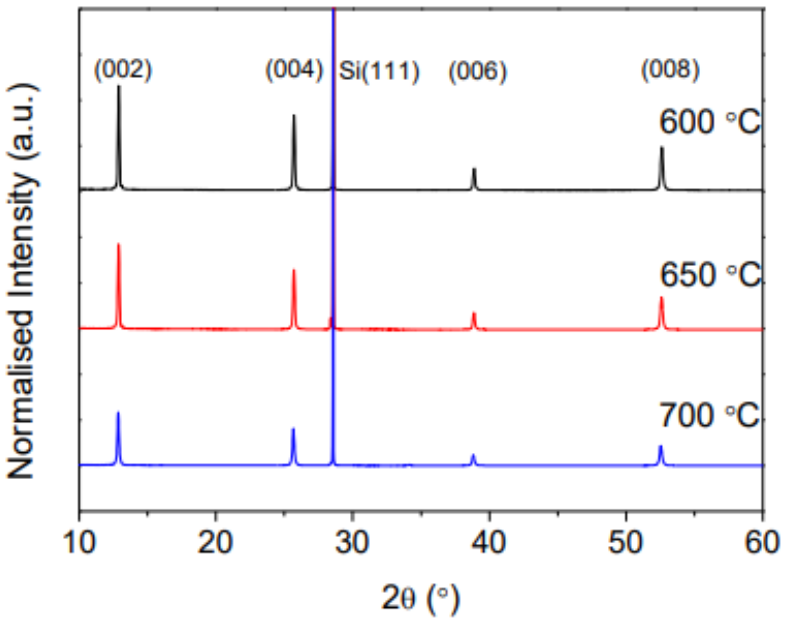


Figure 4.6 XRD of 5nm $MoTe_2$ films synthesised with Mo via reactions at 600, 650 and 700 ˚C.

The XRD pattern shown in Figure 4.6 reveals sharp characteristic peaks, indicating that the synthesized $MoTe_2$ thin film is crystalline. The observed peaks correspond to the (001) family, specifically the (002) and (004) planes, further confirming the crystallinity of the film. However, XRD alone is insufficient to distinguish between the 2H and 1T phases of $MoTe_2$, as it cannot fully resolve the material's crystalline structure. Therefore, additional characterization techniques are required to determine the specific phase. To address this, the samples were subjected to Raman spectroscopy, with the results presented in Figure 4.7.

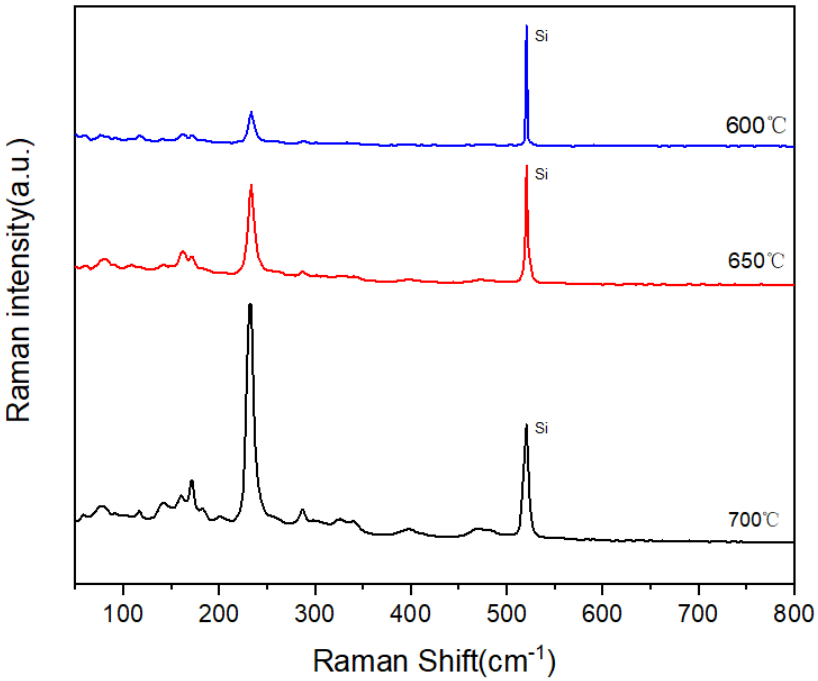


Figure 4.7 Raman spectra of $MoTe_2$ films synthesised via reactions at 600, 650 and 700˚C.

The Raman spectra (Figure 4.7) clearly demonstrate that the 2H phase of $MoTe_2$ forms at all three tested temperatures, with characteristic peaks observed at 118, 170, and 233 cm^{-1}. Notably, the intensity of these peaks increases with rising reaction

temperature, suggesting that 700°C is the optimal temperature for synthesizing 2H-$MoTe_2$ films. However, after conducting multiple tests, it was noted that films produced at 700°C exhibited a lack of uniformity. Consequently, 650°C was selected as the preferred temperature for synthesizing uniform, high-quality thin films.

4.3.2 Optimized CVD Process and Characterization

The vacuum step in the CVD system is implemented to minimise the presence of atmospheric gases, particularly oxygen, within the reaction chamber, ensuring that the process occurs in a controlled, oxygen-free environment. To evaluate whether this vacuum step could be bypassed, a series of experiments were conducted to determine if the CVD process could proceed effectively under an optimised gas environment without prior evacuation. Te and $FeTe_2$ were used as reference and control materials, respectively, to compare the outcomes.

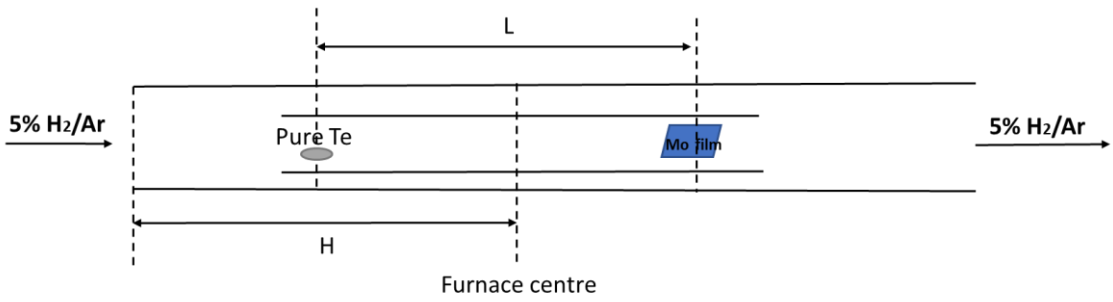


Figure 4.8 Diagram and schematic illustrating the flow CVD reactor setup for Mo films reacted with Te at 650 °C.

Initial experiments were conducted under conditions identical to those of the $FeTe_2$ reaction system, with a dwell time of 4 hours. Through these tests, the optimal evaporation temperature for Te was determined, and modifications were made to the spatial arrangement of the sample within the furnace. The CVD conditions were

maintained by adjusting the position of the Te particles, with a gas flow rate of 300 sccm, as illustrated in Figure 4.8. Subsequent experiments were performed under varying conditions, and the samples were analysed using Raman spectroscopy. Key parameters, such as gas flow rate and the distance between the precursor and the substrate, were systematically varied.

In this section, $FeTe_2$ precursors were employed in a conventional flow CVD system to synthesise pure-phase 1T-$MoTe_2$ and 2H-$MoTe_2$. The phase of $MoTe_2$ produced was dictated by the type of Mo precursor: MoO_3 facilitated the formation of 1T-$MoTe_2$, while elemental Mo resulted in 2H-$MoTe_2$. Insufficient vacuuming during the CVD process can lead to oxygen infiltration, causing unwanted mixed-phase products and oxide formation. To mitigate this issue, the experimental procedure was modified by increasing the gas flow rate and extending the duration of gas circulation prior to heating to establish an oxygen-free environment without relying on a vacuum pump. The test gas was circulated for up to 10 minutes to ensure thorough purging of the reaction chamber.

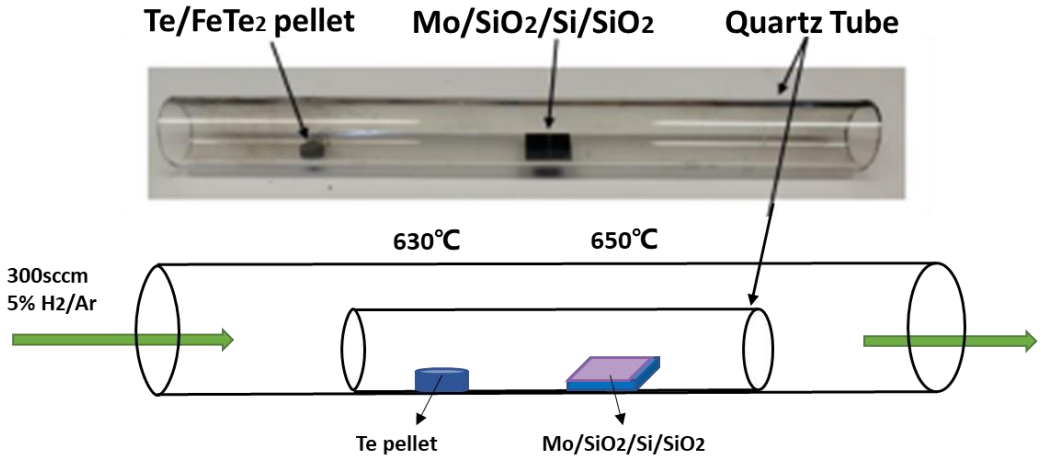


Figure 4.9 The furnace diagram of the CVD reaction

To assess the effectiveness of the modified setup, comparative experiments were conducted using both Te and $FeTe_2$ as precursors. The positioning of the precursor and substrate within the furnace is illustrated in Figure 4.9, while the schematic of the enhanced experimental setup is presented in Figure 4.10. Given the adjustments made to the gas flow parameters, these comparative experiments focused on key variables, including precursor type, reaction time, and gas flow rate.

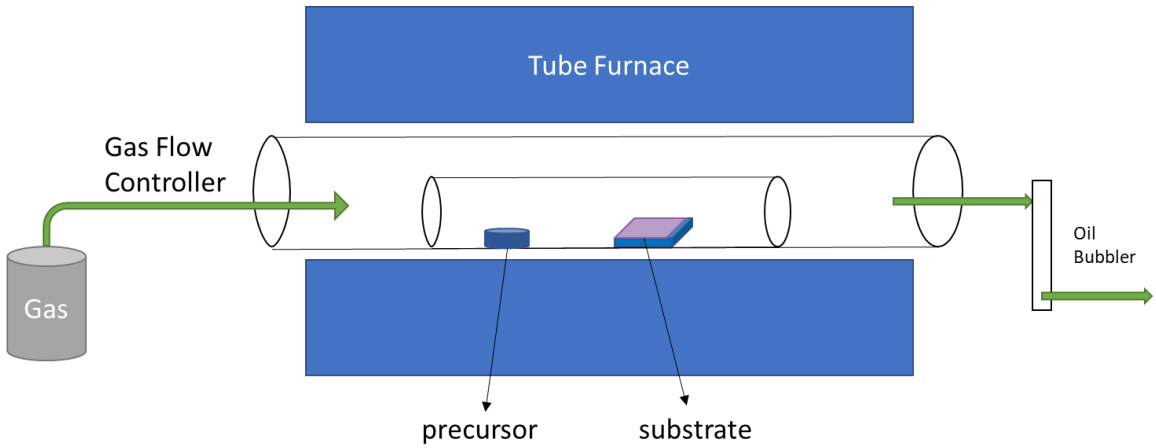


Figure 4.10 Optimized CVD system with removing vacuum pump equipment.

To avoid the formation of intermediate phases during the conversion of MoO_3 to 1T-$MoTe_2$, direct synthesis of 2H-$MoTe_2$ from elemental Mo was employed. Therefore, Mo was selected as the precursor in this experiment.

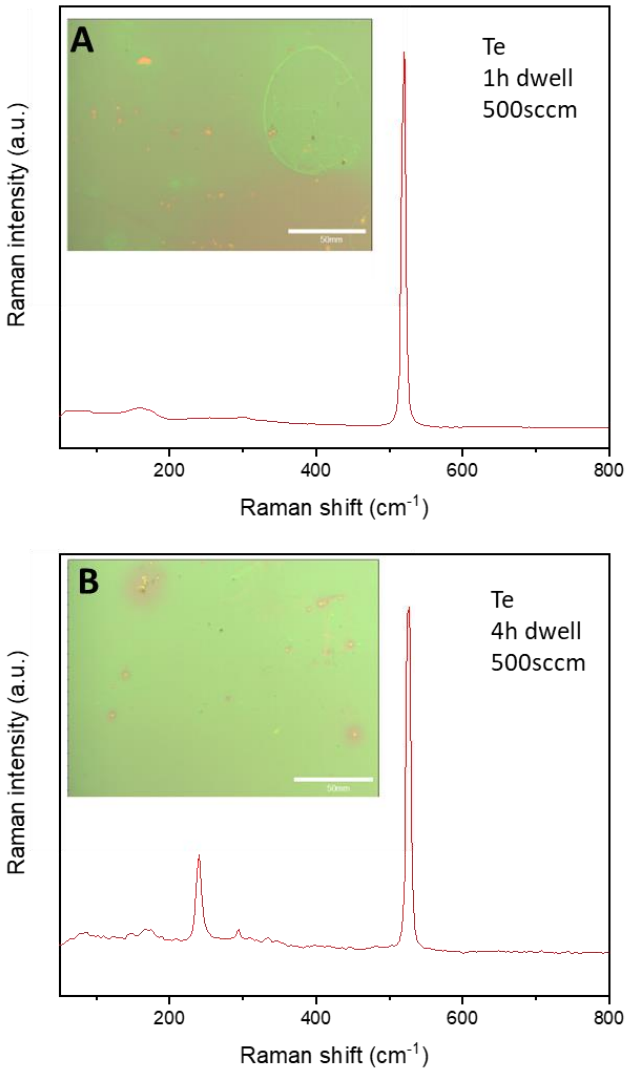


Figure 4.11 Raman result and optical microscope image about $MoTe_2$ *film convert with Te on (A) 1h Dwell reaction time and (B) 4h Dwell reaction time.*

Due to the low evaporation temperature of Te, a significant amount of pure Te was required for the experiments. Approximately 300 mg of Te, the same amount used in the $FeTe_2$ experiments, was utilized. Following the removal of the vacuum step, the gas flow rate was increased to 500 sccm, up from the previous rate of 300 sccm. The products obtained from various reaction times and gas flow rates were analyzed, with the Raman spectroscopy results for 5 nm $MoTe_2$ presented in Figure 4.11. The 4-hour

reaction time was found to be optimal for producing high-quality, continuous $MoTe_2$ films, as confirmed through multiple optical microscopy comparisons.

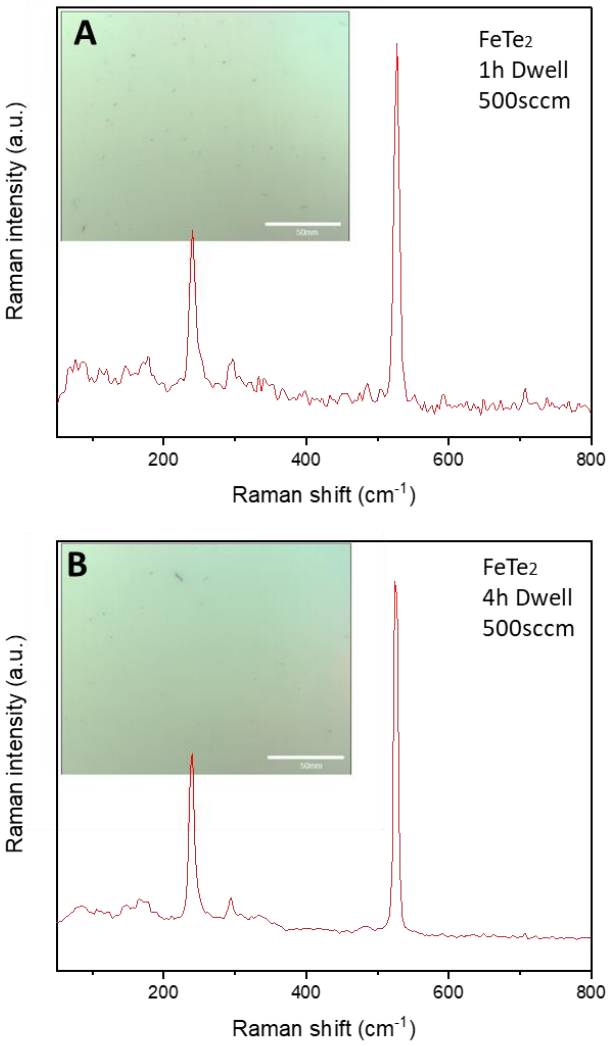


Figure 4.12 Raman result and optical microscope about $MoTe_2$ *film convert with* $FeTe_2$ *on (A) 1h Dwell reaction time and (B) 4h Dwell reaction time.*

After establishing the baseline system parameters, additional experiments were conducted to evaluate the effects of reduced gas flow rates and varying precursor quantities. The results, illustrated in Figure 4.12, reveal the absence of any discernible characteristic peaks associated with $MoTe_2$ in the Raman spectra. Instead, the spectra

predominantly display peaks corresponding to the underlying Si substrate, indicating either incomplete film formation or insufficient $MoTe_2$ deposition under these modified conditions.

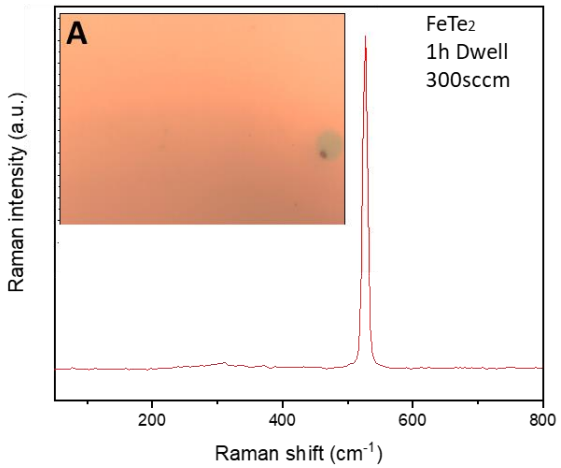


Figure 4.13 Raman spectroscopy and optical microscope image on the film converted with $FeTe_2$ with a 1h Dwell reaction.

Optical microscopy images of the samples further corroborate this finding, showing that only a small portion of the Mo thin film remains on the substrate. This observation suggests that the formation of $MoTe_2$ was hindered due to inadequate gas flow during the CVD process, possibly compounded by the presence of residual air. The introduction of air likely contributed to the evaporation or degradation of the film in the high-temperature environment. These findings underscore the critical need to optimize the CVD system by increasing the reaction gas flow rate, which would facilitate the rapid and efficient deposition of the desired $MoTe_2$ film while minimizing evaporation and oxidation.

4.3.3 CVD Reaction Process Principle

To investigate the formation of intermediate products in a chemical reaction, utilizing powder as a precursor can extend the reaction time, enabling the observation of such intermediates. In this study, solid powders of Mo and MoO_3 were employed to explore the reasons behind the distinct crystal structures yielded by different precursors. Approximately 5 mg of Mo and MoO_3 were deposited on the same substrate under identical CVD conditions. Raman spectroscopy was utilized to monitor the progression of the reaction.

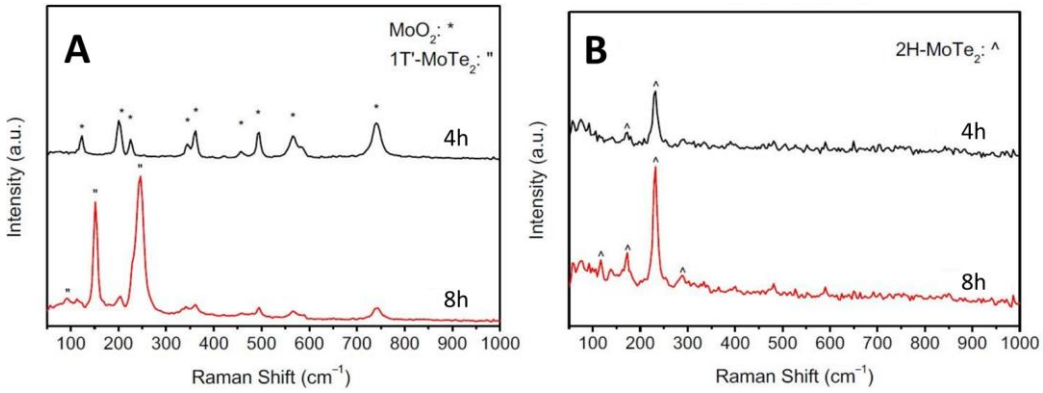


Figure 4.14 Raman spectrum on the (A) 1T-$MoTe_2$ and (B) 2H-$MoTe_2$ synthesis with long reaction time length.

$FeTe_2$ was found to provide a stable and sufficient Te vapor supply for extended CVD processes due to its higher decomposition temperature, making it preferable over elemental Te. Previous studies indicate that, under CVD conditions, 1T-$MoTe_2$ is initially formed and subsequently converted into 2H-$MoTe_2$ with prolonged reaction times. This phase transformation highlights the phase-selective nature of the CVD system.

The Raman spectroscopy results revealed that the low vapor pressure of Te in the system leads to the conversion of MoO_3 to MoO_2 and subsequently to 1T-$MoTe_2$. Conversely, when using Mo as the precursor and ensuring adequate Te vapor pressure, the film can directly transform into 2H-$MoTe_2$ without passing through intermediate oxides. If this hypothesis holds, the optimal vapor pressure of pure Te should theoretically align with the outcomes achieved using $FeTe_2$.

A comprehensive cross-sectional analysis confirmed the successful preparation of uniform, high-crystallinity 2H- and 1T-$MoTe_2$ films at 650°C. These films were further validated through Raman spectroscopy, AFM, SEM, and other characterization methods. The next step involves exploring potential applications for the $MoTe_2$ films synthesized via the CVD method.

4.4 Characterization of 2H-$MoTe_2$

After establishing the experimental parameters for the successful synthesis of 2H-$MoTe_2$, various characterization techniques were employed to evaluate the properties of the prepared films. These techniques included Raman spectroscopy, scanning electron microscopy (SEM), and atomic force microscopy (AFM).

AFM proved particularly useful for measuring the thickness of the 2H-$MoTe_2$ films, enabling precise analysis of films with varying thicknesses to assess their uniformity and surface morphology. Each characterization method played a critical role in evaluating the crystallinity, surface topography, and thickness of the films, providing a comprehensive understanding of the material's structural and physical properties.

4.4.1 SEM and EDX

The $MoTe_2$ film prepared using a 3 nm Mo precursor is depicted in Figure 4.15. The interface between the film and the substrate was analyzed using energy-dispersive X-ray spectroscopy (EDX) and scanning electron microscopy (SEM). The results confirm the distribution of two primary elements, molybdenum (Mo) and tellurium (Te), throughout the film. Additionally, elements inherent to both the substrate and the film were detected. This analysis provides strong evidence for the successful synthesis of $MoTe_2$ via the chemical vapor deposition (CVD) process.

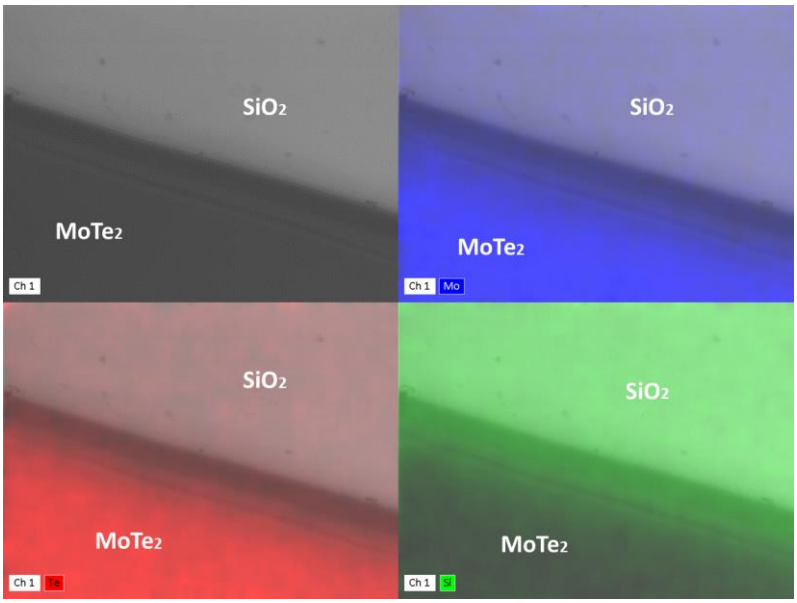


Figure 4.15 The EDX mapping results in $MoTe_2$ converted from 3nm Mo film.

The observed gradual color variation across the film can be attributed to differences in thickness at the interface between the film and the substrate. This non-uniform deposition likely leads to regions with varying thicknesses, resulting in the color changes observed. Such variations are consistent with the non-flat morphology of the deposited film, as indicated by the interface analysis.

4.4.2 Raman Spectrum

As mentioned in Section 4.1, Raman spectroscopy plays a vital role in confirming the successful synthesis of $MoTe_2$ thin films and distinguishing between their various crystal forms. The Raman spectra of the 2H-$MoTe_2$ films produced via the CVD process, illustrated in Figure 4.16, prominently display characteristic peaks corresponding to the 2H phase. Specifically, the peak modes E_1g, A_1g, and E_2g^2 are observed at 119 cm^{-1}, 171 cm^{-1}, and 234 cm^{-1}, respectively. These results confirm the presence of the 2H-$MoTe_2$ phase, aligning with the reference data presented in Chapter 3.

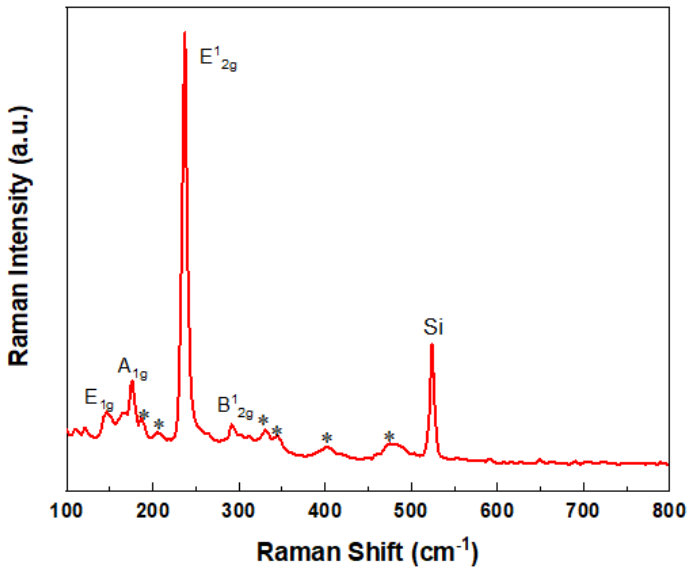


Figure 4.16 532 nm Raman spectrum of a 2H-$MoTe_2$ *film on a* SiO_2*/Si substrate. Modes associated with* $MoTe_2$ *are highlighted.*

Additionally, the absence of the monolayer's phonon-active out-of-plane mode at 289 cm^{-1} suggests that the sample comprises a few layers rather than a single monolayer. The presence of weak secondary peaks at 138 cm^{-1}, 185 cm^{-1}, 200 cm^{-1}, 326 cm^{-1},

342 cm^{-1}, 400 cm^{-1}, and 470 cm^{-1} further corroborates the successful formation of pure-phase 2H-$MoTe_2$. These second-order resonance peaks confirm the phase purity and crystallinity of the $MoTe_2$ films synthesized using the modified open-flow CVD system[16–19].

4.4.3 AFM for Film Surface Roughness

AFM provides detailed insights into the surface features and roughness of thin films, including feature height and surface roughness metrics[20]. Figure 4.18 presents the 2D topography of a sample where 1 nm of Mo was deposited onto a SiO_2/Si substrate and subsequently converted to 2H-$MoTe_2$. The R_q was measured for each sample, confirming the uniformity of the film surface.

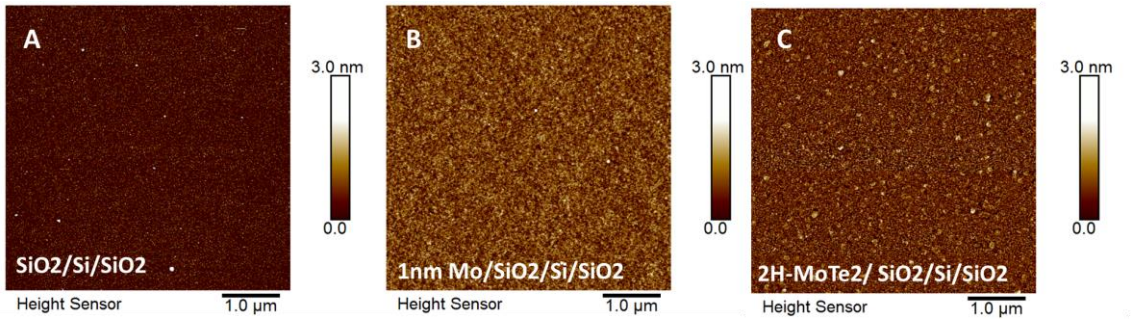


Figure 4.17 AFM 2D roughness profiles of 5 µm × 5 µm area of the surfaces of (A) SiO_2/Si pristine substrate (B) 1 nm Mo/ SiO_2/Si and (C) $MoTe_2$ SiO_2/Si.

The root mean square roughness (Rq) of the 2H-$MoTe_2$ films synthesized from the Mo precursor was measured at 0.65 nm and 0.6 nm, as summarized in Table 4.3. These values are notably higher than the 0.45 nm Rq observed for the cleaned substrates. The similarity in surface roughness between the 1 nm Mo films and the 2H-$MoTe_2$ films suggests that the transformation from Mo to $MoTe_2$ during the experiment preserves the original surface morphology. This finding is consistent with recent literature,

indicating that the CVD synthesis of 2H-$MoTe_2$ films maintains comparable surface roughness to the original Mo films[21]. Additionally, it is noted that a low gas flow rate can contribute to film cracking by increasing the thermal coefficient mismatch between the substrate and the film, which adversely affects the film's uniformity and integrity.

4.4.4 AFM for Thickness of 2H-$MoTe_2$

As mentioned in the literature review, 2H-$MoTe_2$ undergoes a critical transition from an indirect to a direct bandgap when reducing the material from bulk to monolayer form. This highlights the importance of accurately characterizing the thickness of the $MoTe_2$ film. Figure 4.18 illustrates the 2D topography of the film-substrate interface, along with the height distribution profile. The thickness of the 2H-$MoTe_2$ layer was determined by initially depositing Mo films of varying thicknesses, followed by optimizing the CVD parameters to grow $MoTe_2$ films of different thicknesses. The films shown in Figure 4.18 were synthesized by converting 4-7 nm thick Mo films using the CVD method. The precise interface between the $MoTe_2$ layer and the substrate was defined through the marker pen method, as discussed in Chapter 3.

The observed increase in surface roughness of polycrystalline $MoTe_2$ films, measured via AFM, correlates directly with the increasing film thickness. This phenomenon can be attributed to several interconnected factors. Primarily, the growth of grain size with increasing thickness plays a significant role. In thinner films, smaller grain sizes result in a relatively smooth surface, leading to lower roughness values. As the film thickness increases, the grains grow larger and begin to coalesce, resulting in more pronounced grain boundaries and surface irregularities. Additionally, the relaxation of grain boundaries in thicker films can lead to edge effects, where the boundaries form ridges or steps, further contributing to increased surface roughness. The more significant

variation in grain boundary heights in thicker films accentuates this roughness, creating a more irregular surface.

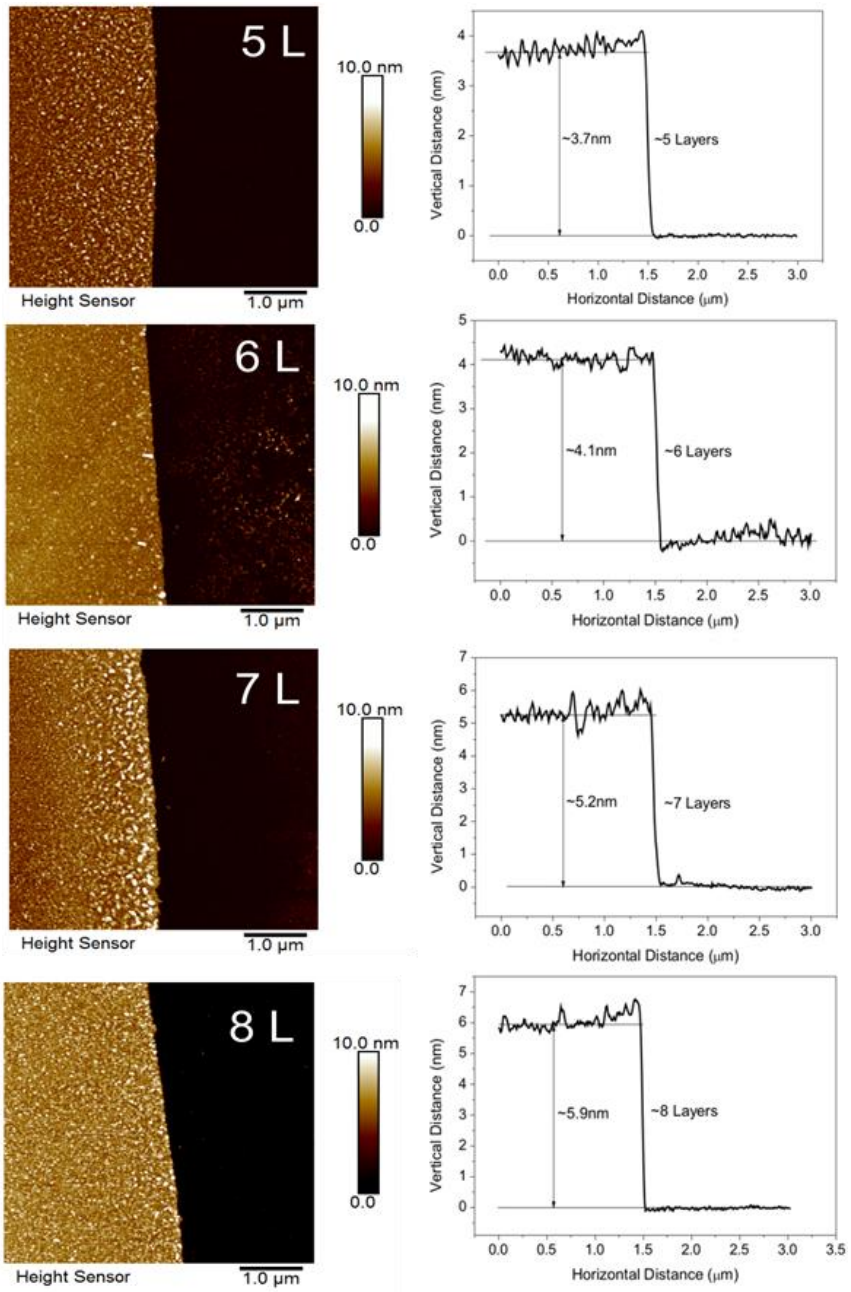


Figure 4.18 2D topographic and height profiles of the interface between 2H-$MoTe_2$ *films thickness ranging from 5-8 layers and substrates.*

Moreover, AFM roughness measurements of $MoTe_2$ films show increased uncertainty for thicker films, as indicated by larger error bars. This likely stems from the greater

surface inhomogeneity, driven by the growth of larger grains and more pronounced boundary features. These variations introduce increased variability in localized measurements by the AFM tip. In contrast, thinner films, which have more uniform surfaces and smaller grains, exhibit more consistent roughness values, reflected in smaller uncertainties. The combined effects of grain growth, edge phenomena, and measurement uncertainty provide a comprehensive explanation for the roughness evolution in $MoTe_2$ films as their thickness increases.

Table 4.3 The roughness summary of different layers of $MoTe_2$

Layer of $MoTe_2$	Roughness (nm)
8	2.86
7	2.15
6	1.75
5	1.28

Table 4.3 presents the surface roughness measurements for $MoTe_2$ films with thicknesses ranging from 5 to 8 layers, clearly demonstrating that surface roughness increases with film thickness. This trend reveals important insights into the structural evolution of $MoTe_2$ films synthesized via the CVD method. The increased roughness with thicker films likely indicates a transition to a more polycrystalline structure. This can be attributed to the formation of grain boundaries as the film thickens. As the $MoTe_2$ film grows, multiple crystal grains with varying orientations develop, and the number of grain boundaries increases. These boundaries contribute to the growing complexity of the $MoTe_2$ film, resulting in thicker films exhibiting more heterogeneous surface morphologies. The increased structural disorder associated with the formation

of grain boundaries explains the observed trend of increasing roughness in thicker $MoTe_2$ films.

The trend in surface roughness provides compelling evidence supporting the polycrystalline structure of the $MoTe_2$ films. Although Raman spectroscopy has limitations in differentiating between atomic arrangements or specific crystal structures, further investigations were carried out in collaboration with the School of Physics to strengthen these findings. Transmission Electron Microscopy (TEM) analysis, as detailed in the appendix, conclusively confirmed the polycrystalline nature of the synthesized $MoTe_2$ films.

The combination of surface roughness measurements and TEM analysis offers robust support for the conclusion that the $MoTe_2$ films produced through the modified CVD process exhibit a polycrystalline structure. This evidence aligns with the observed increase in surface roughness with film thickness, which is associated with the growth of grain boundaries and the development of a more complex, disordered structure as the films become thicker. The collaboration between AFM, Raman spectroscopy, and TEM analysis establishes a thorough understanding of the film's structural characteristics, confirming the polycrystalline nature of the $MoTe_2$ films.

4.5 Characterization of 1T-$MoTe_2$

In the previous experiments, intriguing results were observed regarding the phase composition of $MoTe_2$ films, as demonstrated in Figure 4.19. The Raman spectra revealed that the CVD $MoTe_2$ films consist of a mixture of 2H and 1T phases. The figure illustrates different regions labeled as 2H and 1T, indicating the presence of both phases within the synthesized films.

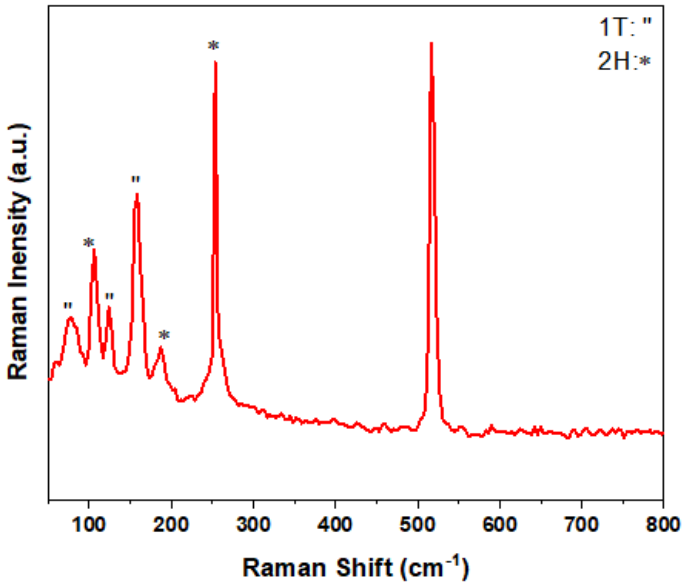


*Figure 4.19 Raman spectrum of film with partially oxidised Mo film. Peaks associated with 2H- $MoTe_2$ are marked with *, peaks associated with 1T- $MoTe_2$ are marked with ".*

The mixed-phase $MoTe_2$ observed in this study was produced from a partially oxidized Mo film (1 nm), with Raman spectroscopy revealing key insights into its composition. As shown in Figure 4.19, the peaks at 234 cm^{-1} and 289 cm^{-1} correspond to the 2H-$MoTe_2$ phase, while characteristic peaks for the 1T-$MoTe_2$ phase are evident in the bulk metal spectrum. The distances between these peaks (78, 110, and 161 cm^{-1}) deviate from expected values based on literature, indicating a complex phase behaviour.

The distinct phases of $MoTe_2$ are significantly influenced by the precursor materials utilized in the synthesis. Generally, Mo is known to favor the formation of the 2H phase, whereas MoO_3 tends to produce the 1T phase. The presence of mixed-phase $MoTe_2$ in this instance may stem from oxidation occurring during the CVD process or from

insufficient inert gas conditions. For example, if some of the Mo films partially oxidized to MoO_x during synthesis, this could lead to the formation of mixed phases.

Moreover, extended exposure of the $Mo/SiO_2/Si$ thin film samples to ambient laboratory air prior to or during the synthesis could further exacerbate the oxidation process. Such exposure would increase the likelihood of forming a mixed-phase material due to the partial conversion of Mo to its oxidized state, which can subsequently affect the final crystallization of $MoTe_2$. This finding highlights the importance of maintaining controlled synthesis conditions and minimizing exposure to air to achieve the desired phase purity in $MoTe_2$ films.

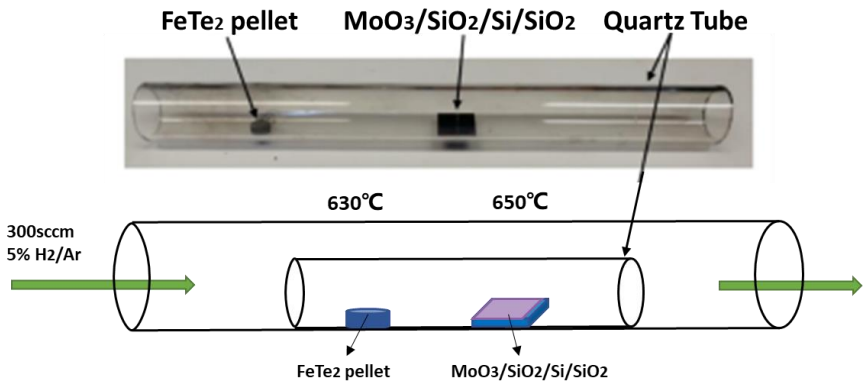


Figure 4.20 Photograph and schematic showing the same closed CVD reactor used for the deposition of 2H-$MoTe_2$, MoO_3 replaces the previously used Mo.

To mitigate the issues related to oxidation and phase mixing, the experimental setup was revised by using $MoO_3/SiO_2/Si$ films as the precursor instead of $Mo/SiO_2/Si$. This modification was aimed at achieving a clearer distinction between the 1T and 2H phases of $MoTe_2$, as well as reducing the unintended oxidation that contributed to mixed-phase formation.

Figure 4.20 presents the results obtained using MoO_3 as the precursor under the modified CVD process. The goal of these experiments was to establish more consistent phase formation and improve the overall quality of the $MoTe_2$ films by leveraging the distinct properties of MoO_3. Unlike Mo, which typically forms the 2H phase, MoO_3 is known to favor the formation of the 1T phase. This change was expected to reduce the oxidation effects observed in previous experiments, as the higher oxidation state of MoO_3 would be less susceptible to further oxidation during the CVD process.

The results indicate a more controlled synthesis, with clearer separation between the 1T and 2H phases. Raman spectroscopy confirmed this improvement, showing more defined characteristic peaks corresponding to the targeted phases of $MoTe_2$. Additionally, the shift in precursor choice helped mitigate the presence of undesirable mixed-phase products, as the oxidation processes were more controlled, leading to films with higher phase purity and better crystallinity.

This revision in precursor choice proved effective in addressing the oxidation challenges and enhancing the consistency and quality of the $MoTe_2$ films produced. The use of MoO_3 thus emerged as a more suitable approach for achieving precise phase control in $MoTe_2$ synthesis via CVD.

4.5.1 EDX and SEM

The Raman spectroscopy data indicates that the Ag mode peak at 161 cm^{-1} exhibits uniform intensity across the entire 1T-$MoTe_2$ film, confirming a consistent phase distribution throughout. This uniform intensity not only highlights the homogeneity of

the film's composition but also indicates successful control over the CVD growth process, resulting in a high-quality, well-formed 1T-$MoTe_2$ layer.

Supporting this analysis, Figure 4.21 presents SEM and EDX data from the film-substrate interface, reinforcing the observations made from the Raman spectroscopy. The EDX elemental distribution map demonstrates that both molybdenum (Mo) and tellurium (Te) are evenly distributed throughout the film. This even distribution is visually represented by the uniform colouring in the EDX maps, indicating that the film's composition does not vary significantly across its surface.

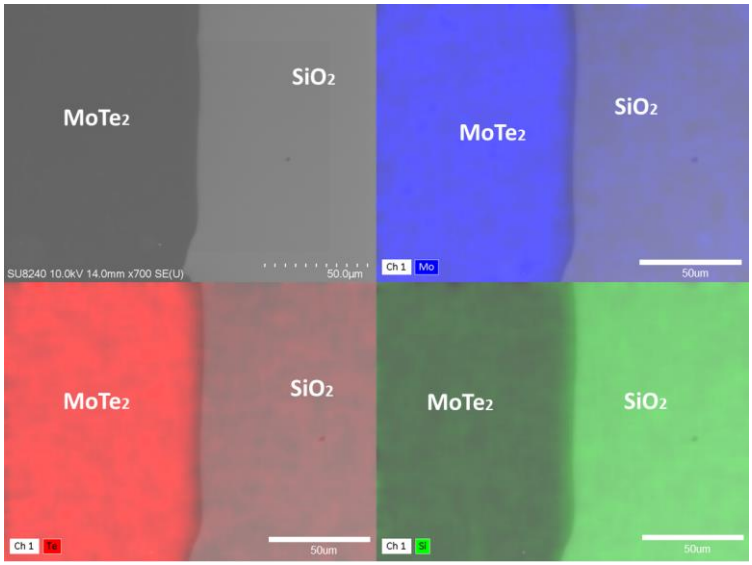


Figure 4.21 EDX mapping image of 1T- $MoTe_2$ including Mo, Te, and Si.

Additionally, the consistent termination of Mo and Te at the edge of the film signifies a well-defined interface between the 1T-$MoTe_2$ layer and the SiO_2/Si substrate. The presence of silicon (Si) is also observed throughout both the film and substrate, as expected, since Si serves as the foundational material for the $MoTe_2$ growth. This uniform distribution of elements, coupled with the consistency revealed by the Raman spectroscopy, suggests a robust synthesis method, enabling the production of high-

quality 1T-$MoTe_2$ films with uniform properties—essential for potential applications in electronics and optoelectronics.

In conclusion, the complementary data from Raman spectroscopy, SEM, and EDX analyses provide a comprehensive assessment of the film's quality, showing that the modified synthesis approach

While EDX provides valuable information on elemental distribution, it does not supply details regarding the crystalline structure of the film. To accurately characterise the phases of $MoTe_2$, including the 2H and 1T forms, additional methods are required. Techniques such as X-ray diffraction (XRD) or selected-area electron diffraction (SAED) in transmission electron microscopy (TEM) can be employed to differentiate between these phases based on their distinct crystallographic signatures.

4.5.2 Raman Spectrum

The Raman spectroscopy data depicted in Figure 4.22 confirms the successful growth of the metallic 1T-$MoTe_2$ phase from $MoO_3/SiO_2/Si$ substrates. The Raman peaks between 50 and 400 cm^{-1} display distinct characteristic modes associated with the 1T-$MoTe_2$ phase. Specifically, the Ag modes observed at 80, 108, 125, 161, 251, and 265 cm^{-1}, along with the Bg mode at 186 cm^{-1}, serve as clear indicators of the 1T structure. These peaks are distinguishable from those of the 2H phase, further confirming the presence of the metallic phase. Additionally, the absence of peaks at 225 cm^{-1} and 740 cm^{-1}, which are associated with MoO_3 and MoO_2, indicates the complete conversion of the MoO_3 precursor into 1T-$MoTe_2$. This further validates the efficacy of the CVD process in transforming MoO_3 into the desired 1T-$MoTe_2$ phase without residual oxides[16,17].

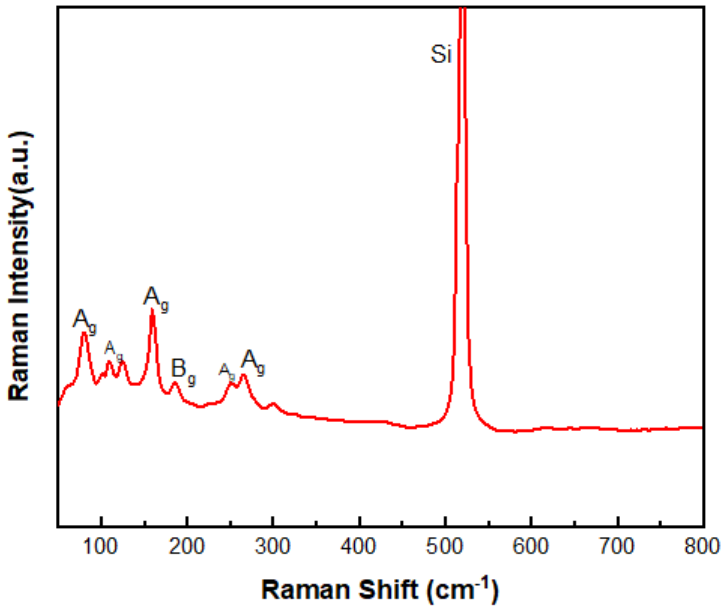


Figure 4.22 532 nm Raman spectrum of a 1T- $MoTe_2$ film on the substrate.

Raman spectra collected from random points across the sample exhibited consistent peak positions and intensities, demonstrating the uniformity and quality of the 1T-$MoTe_2$ film produced via the CVD process. This uniformity highlights the reliability of MoO_3 as a precursor for growing high-quality, homogeneous 1T-$MoTe_2$ films, which is crucial for practical applications where phase purity and uniformity are essential.

4.5.3 Surface Roughness

AFM measurements on the 3 nm MoO_3 precursor film and the resultant 1T-$MoTe_2$ film underscore the importance of surface quality in the CVD process. The surface roughness values indicate that the roughness of the original MoO_3 precursor film was Rq = 0.480 nm, while the converted 1T-$MoTe_2$ film exhibited a slightly increased roughness of Rq = 0.512 nm. This minor increase in roughness suggests that the uniformity and smoothness of the $MoTe_2$ film are directly influenced by the quality of

the precursor film and the precision of the deposition technique. Variations in roughness imply minor surface alterations during the CVD process.

This observation aligns with prior studies, which demonstrate that precursor quality and deposition control significantly affect the growth of thin films and their final structural integrity. Controlling the thickness of CVD-produced films is critical, particularly considering the drastic changes in the band structure of $MoTe_2$ phases as thickness decreases.

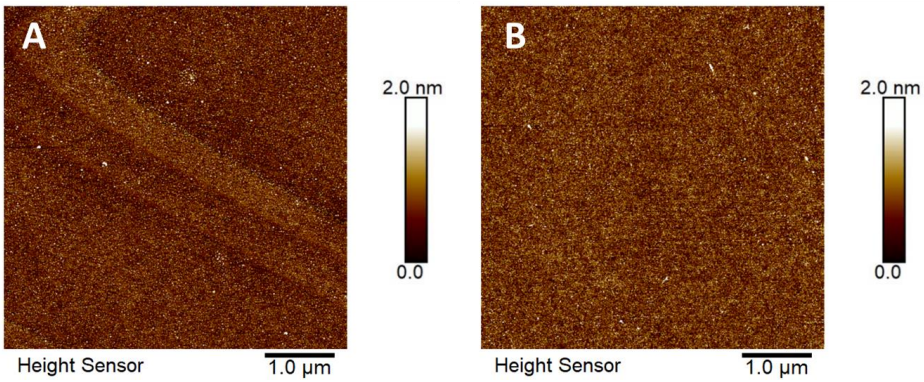


Figure 4.23 2D topographic profiles of 5µm × 5µm area of the surfaces of (A) MoO_3/ SiO_2/Si and (B) 1T- $MoTe_2$ / SiO_2/Si.

For example, thin films (less than 10 nm) of the 1T phase exhibit superior performance compared to thicker films (over 10 nm), akin to the 2H phase, which shows a transition in bandgap behaviour as it approaches monolayer thickness. Therefore, ensuring precise control over the thickness and surface roughness of $MoTe_2$ films is essential for achieving optimal electronic and structural properties[12,13,22].

AFM serves as a valuable tool in this context, providing insights into film uniformity and roughness, which are crucial indicators of film quality, performance potential, and the effectiveness of the CVD process in producing high-quality 1T-$MoTe_2$ thin films.

These factors directly influence the electronic and catalytic properties of $MoTe_2$, particularly in applications requiring uniform, thin-layered films.

4.5.4 Thickness evaluation

To control the thickness of the 1T-$MoTe_2$ film, the thickness of the MoO_3 precursor layer was systematically varied. This approach allowed for precise tuning of the film thickness, as confirmed by the marker-pen method, which created a distinct step between the 1T-$MoTe_2$ film and the substrate for accurate thickness measurements. The corresponding AFM 2D images and height profiles in Figure 4.24 clearly illustrate this interface, providing detailed insights into the thickness variations. The results from the AFM analysis indicate a direct relationship between the thickness of the MoO_3 precursor layer and the final thickness of the 1T-$MoTe_2$ film. Specifically, as the precursor layer was made thicker, the resulting $MoTe_2$ film thickness increased proportionally, confirming effective control over film thickness by adjusting the precursor layer.

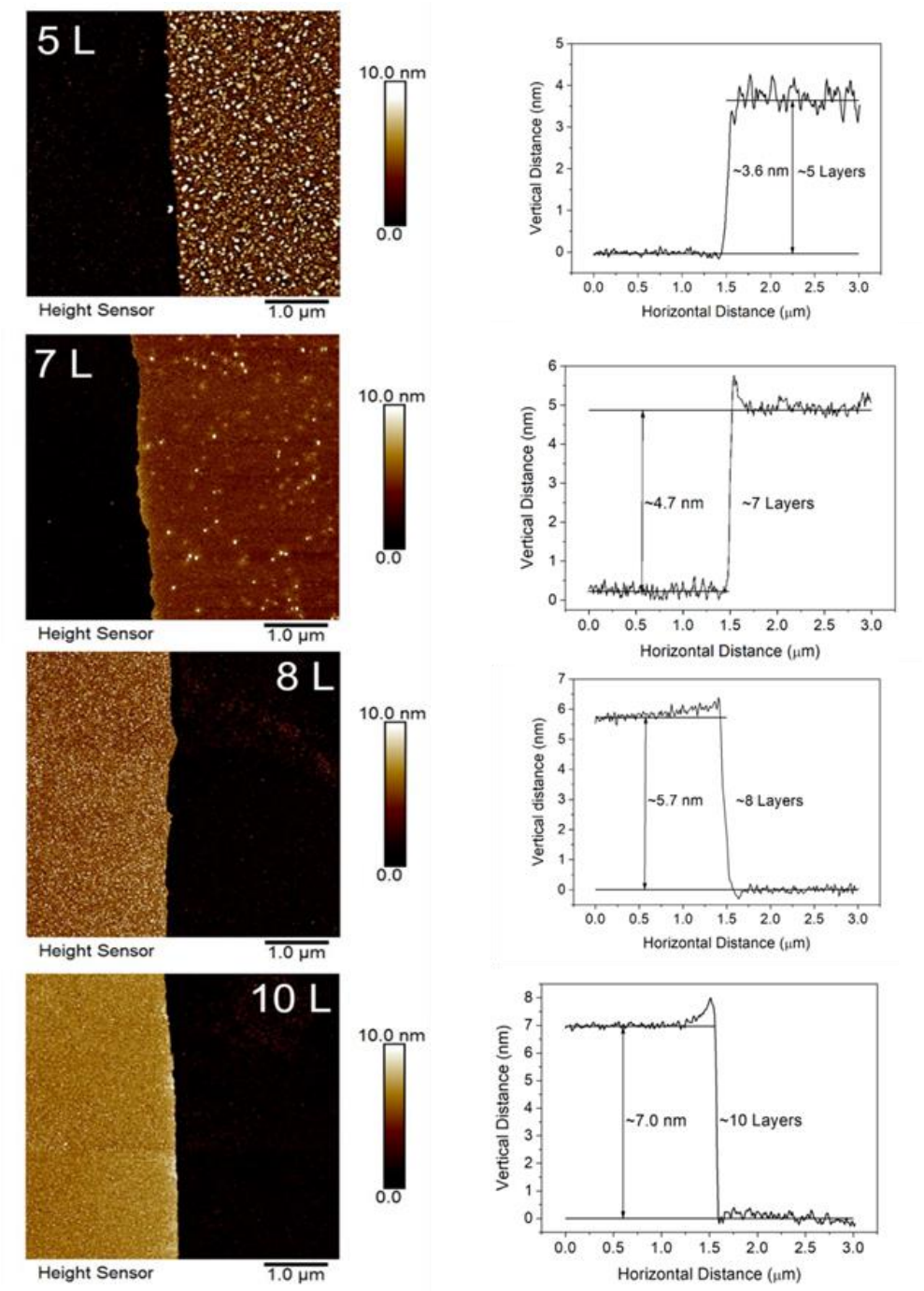


Figure 4.24 2D topographic and height profiles of the interface between few-layered 1T- $MoTe_2$ films with 5,7,8,10 layers.

However, a noticeable increase in roughness at the interface between the substrate and the 1T-$MoTe_2$ film was observed, likely due to oxidation effects. This may have occurred because the synthesis was not conducted in a cleanroom environment,

exposing the process to air and introducing oxygen, which altered the film's properties and stability. This highlights the critical importance of carrying out the deposition in a controlled, inert atmosphere to prevent unintended oxidation, which can compromise the quality and structural integrity of $MoTe_2$ thin films. These findings underscore the necessity of stringent environmental controls during the CVD process to ensure uniformity and prevent defects. Proper control of precursor thickness and synthesis conditions is essential for producing high-quality 1T-$MoTe_2$ films.

The higher surface roughness observed in polycrystalline 1T-$MoTe_2$ films compared to 2H-$MoTe_2$ films grown via CVD can be attributed to inherent differences in their crystal structures, phase stability, and growth mechanisms, particularly as film thickness increases. The 1T-$MoTe_2$ phase, with its distorted octahedral structure, is metastable and prone to instability. This instability results in less uniform growth, contributing to increased surface roughness. In contrast, the 2H-$MoTe_2$ phase, characterised by a stable trigonal prismatic structure, exhibits more uniform growth, leading to a smoother surface.

As the film thickness increases, the instability of the 1T phase becomes more pronounced, resulting in greater roughness due to stress-induced phase transitions and the generation of defects. Conversely, the thermodynamically stable 2H phase maintains a smoother surface even at greater thicknesses. The polycrystalline nature of 1T-$MoTe_2$ films also plays a key role in their increased roughness. In the 1T phase, small grains with random orientations coalesce unevenly, forming grain boundaries and surface defects that contribute to roughness. Although these grains grow as the film thickens, their coalescence remains uneven, further increasing surface roughness.

In contrast, the 2H phase grows in larger, more uniform grains with fewer grain boundaries, resulting in smoother films.

Additionally, surface energy and deposition kinetics influence these outcomes. The metastable 1T phase has a higher surface energy, making smooth, layer-by-layer growth less favourable and leading to rougher surfaces. In contrast, the 2H phase, with lower surface energy and more stable atomic configurations, promotes smoother film formation. As the thickness of the 1T-$MoTe_2$ film increases, internal stresses lead to more defects and larger, unevenly coalescing grains, further contributing to roughness. In the 2H phase, however, the film grows with fewer defects and maintains a smoother surface, even as thickness increases.

Therefore, the higher surface roughness of polycrystalline 1T-$MoTe_2$ films results from their metastability, grain structure, and phase instability, which become more pronounced with increasing thickness. In contrast, the thermodynamically stable 2H-$MoTe_2$ phase produces smoother films with better grain alignment and fewer defects. Despite being synthesised under identical CVD conditions, the fundamental differences between these two phases lead to distinct surface roughness characteristics.

4.6 Comparison of simultaneously deposited 1T- and 2H-$MoTe_2$

The experimental design and implementation of the CVD system demonstrated the ability to simultaneously produce 2H- and 1T-$MoTe_2$ films by varying the precursor films. In this experiment, 3 nm Mo and 3 nm MoO_3 were deposited on the same substrate, with a clean portion of the substrate masked for comparison. The combined

substrate was then placed into the CVD growth system previously utilised, and the growth process was conducted under the same experimental parameters.

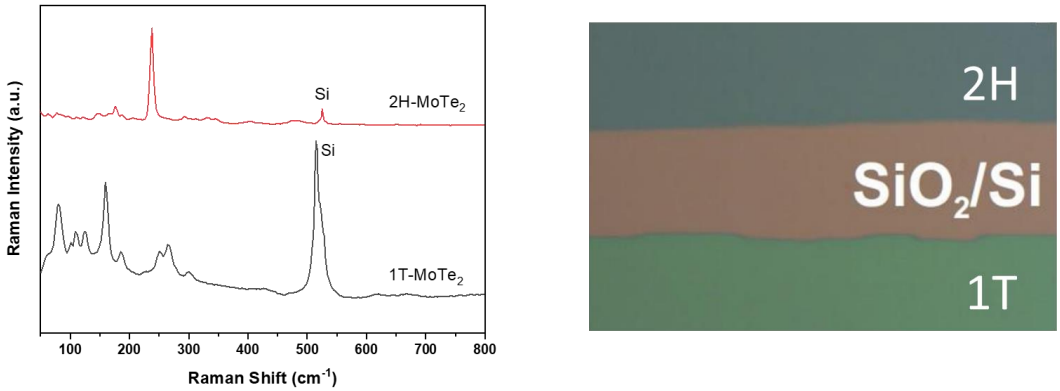


Figure 4.25 Raman spectra from 1T- and 2H- $MoTe_2$ grown simultaneously on the substrate and an optical image of the two $MoTe_2$ phases.

Afterwards, Raman spectroscopy was employed to characterise the resulting samples. The experimental results revealed that 2H-$MoTe_2$ and 1T-$MoTe_2$ thin films, with distinct crystalline forms, were successfully grown on different sections of the same substrate. The Mo precursor led to the formation of 2H-$MoTe_2$, while the MoO_3 precursor resulted in 1T-$MoTe_2$, confirming that both crystal phases could be produced simultaneously in a single-step reaction without the need for post-growth modifications. This breakthrough in the synthesis process holds significant potential for expanding the applications of $MoTe_2$, as it allows for direct control of crystal phases during film growth. The ability to grow both 1T and 2H phases of $MoTe_2$ on the same substrate opens new avenues for optoelectronics, sensors, transistors, and energy storage devices.

Additionally, this method provides a pathway for the future design and preparation of multi-phase electronic applications, allowing for more integrated and versatile device

architectures. The findings from this research showcase a flexible and scalable approach to producing phase-specific $MoTe_2$ films, thereby advancing the material's usability in next-generation technologies.

4.7 Application

As discussed in Chapter 2, the literature review reveals a substantial body of research focused on the application of $MoTe_2$. Analysis of the data indicates that most applications involve the use of exfoliated $MoTe_2$ thin films, which are either obtained through CVD or procured in bulk form. Different applications impose specific requirements on the $MoTe_2$ films, including variations in substrate, carrier, and thickness. However, the current methodologies for growing $MoTe_2$ present challenges when integrated into large-scale preparation and production processes.

4.7.1 Exfoliation Film Flexibility

The task involves conducting a transfer test on a pre-prepared $MoTe_2$ film to assess and demonstrate its flexible transfer capabilities. The objective is to validate the smooth and adaptive transfer ability of the CVD film for various applications, ensuring that the film remains functional and flexible throughout the transfer process. This evaluation aims to provide insights into the film’s performance and transfer characteristics.

Initially, we employed a widely used and straightforward method from the literature, which involves adhering the film to substrates using Scotch tape, transferring the film to those substrates, and then removing the tape with acetone to obtain the transferred film. However, this method proved ineffective for CVD-grown thin films. Experimental results indicated that the Scotch tape was unable to transfer the film from the substrate

due to the bonding interactions between the Mo and SiO_2 layers, which extend beyond the van der Waals forces typically addressed by this method.

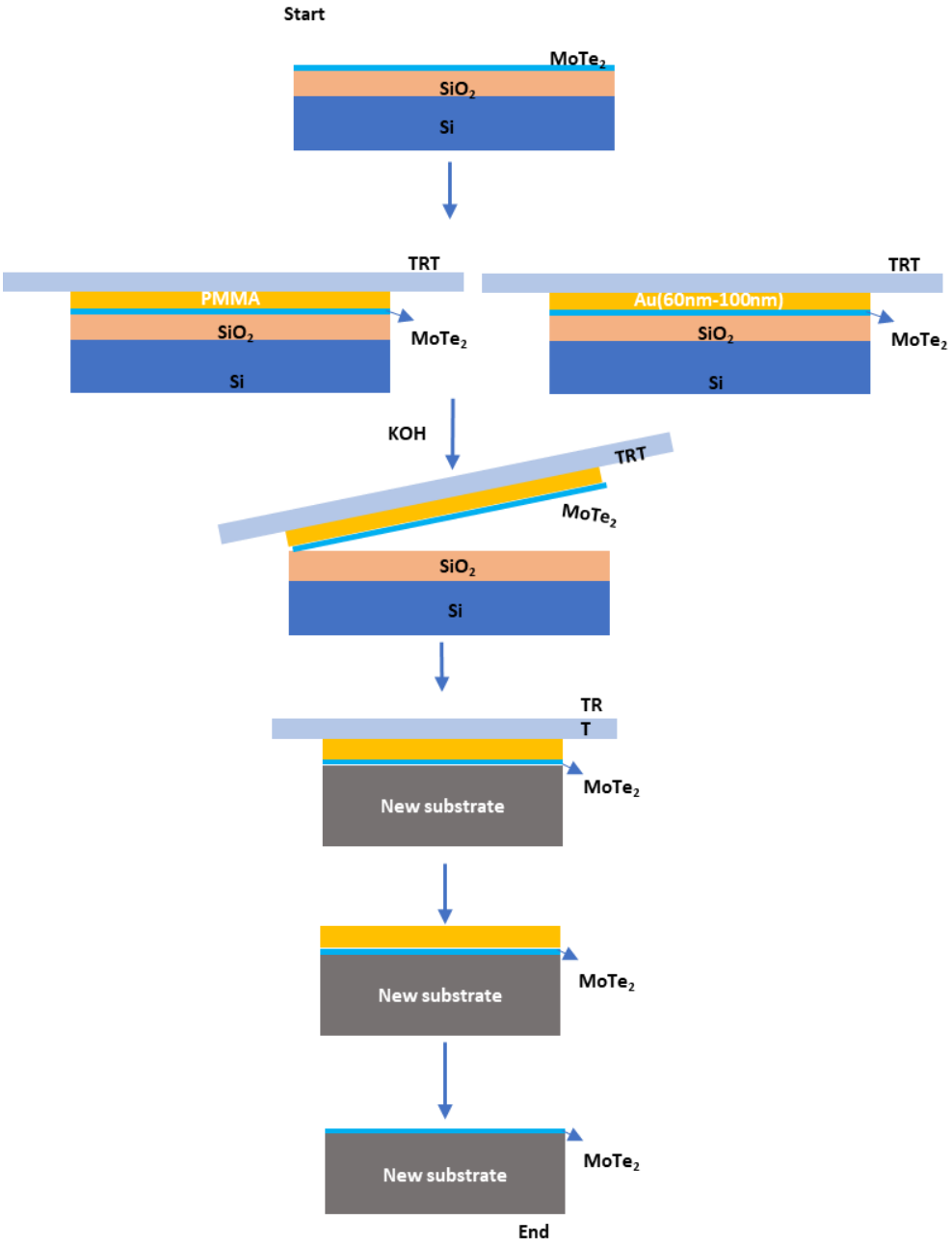


Figure 4.26 The diagram of the CVD film transfer processes with Au and PMMA as assistance layers.

Consequently, alternative transfer techniques were explored. The literature suggests using an auxiliary layer of gold (Au) and thermal release tape (TRT) for the transfer process. This method involves applying the Au layer, transferring the film, and then

removing the metal layer via wet etching to obtain the transferred film. Given the limitations encountered in the laboratory and insights from the literature review, photoresist was chosen as the auxiliary layer to minimise residues from the wet etching process. To separate the film from the substrate, a 20% KOH solution was used as the exfoliation agent, as sulfuric acid failed to detach the film effectively. After transferring the film and TRT to a new substrate, heating at 90 °C for 30 seconds allows the tape to change from clear to white, facilitating its removal from the auxiliary layer. Finally, acetone and wet etching are employed to remove the PMMA and the Au layer, yielding the transferred $MoTe_2$ films. The film transfer procedure is illustrated in Figure 4.26. The process involves the following steps:

1. Spin 1.26 μm of polymethylmethacrylate (PMMA) or Au onto the $MoTe_2$ film.
2. Obtain PMMA/$MoTe_2$ or Au/$MoTe_2$.
3. Adhere the correctly sized TRT to the PMMA or Au surface.
4. Press the assembly against a flat plate to transfer the film, ensuring uniform force across the sample and substrate.
5. Remove the PMMA with the lift-off solution or remove the Au with wet etching.
6. Check the film condition after transferring to the new substrate.

The $MoTe_2$ films with the Au auxiliary layer were subsequently characterised using optical microscopy, Raman spectroscopy, and scanning electron microscopy, as shown in Figure 4.27.

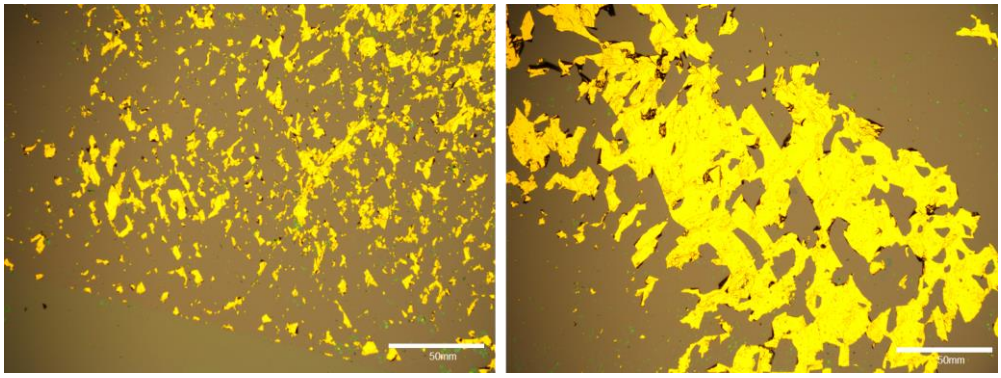


Figure 4.27 The optical microscope results using Au as an assist layer transfer $MoTe_2$ *film.*

Following the wet etching process with gold (Au), it became apparent from the results that the sample could not maintain its original shape. The films were observed to separate, fracture, and adhere to the Au layer, indicating that thin CVD-grown films are not well-suited for transfer using Au as an auxiliary layer.

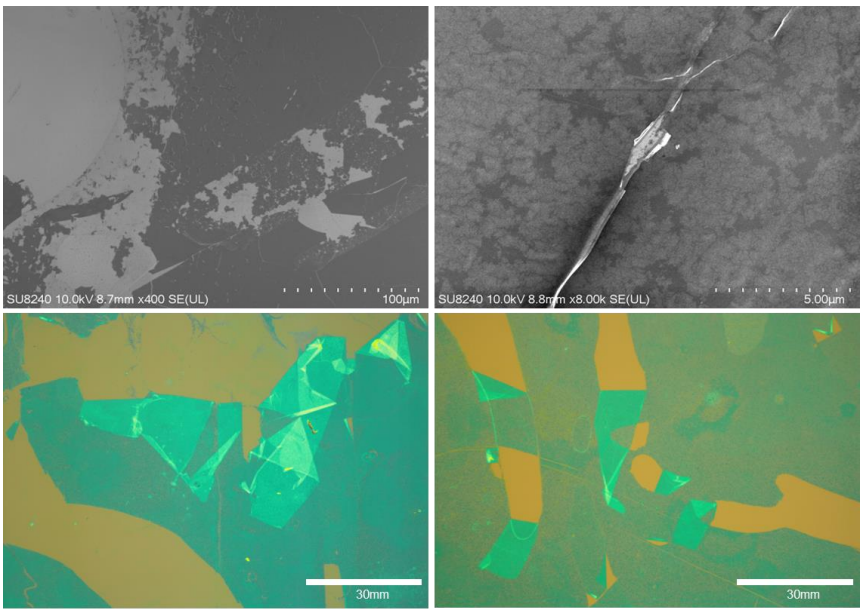


Figure 4.28 The optical microscope and SEM result about using the PMMA as an assisting layer transfer the $MoTe_2$ *film.*

The comparative results with PMMA as the auxiliary layer are shown in Figure 4.28. In this case, the film was successfully transferred to a new substrate, demonstrating

superior performance with PMMA. The successful transfer was confirmed; however, the transferred film exhibited slight chipping and curling. Optical microscopy results revealed the presence of small particles and uneven film thickness. To verify that $MoTe_2$ retains its original properties after transfer, Raman spectroscopy was performed. The Raman spectra, illustrated in Figure 4.29, indicate no significant difference between the $MoTe_2$ film before and after transfer, confirming that the film's morphology and crystal structure remain intact.

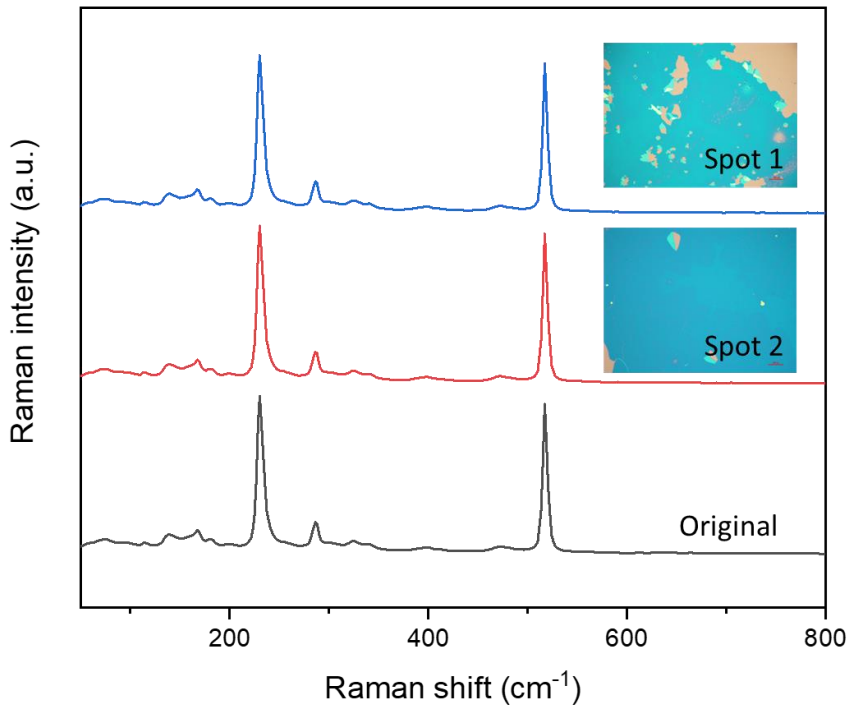


Figure 4.29 Raman spectroscopy on transferred film with PMMA as assist layer compared with original layers.

Despite these successful results, the film experienced fracturing and curling due to its thinness and the varying force applied during the transfer process. Nevertheless, these findings demonstrate that CVD-produced $MoTe_2$ films can be effectively transferred to other substrates, thereby facilitating potential future applications.

4.8 Chapter Summary

In conclusion, a novel CVD method has been developed for the phase-selective deposition of 2H- and 1T-$MoTe_2$ thin films using an innovative $FeTe_2$ precursor. Phase selectivity is achieved through the choice of molybdenum precursor, wherein Mo transforms into 2H-$MoTe_2$ and MoO_3 transforms into 1T-$MoTe_2$. This technique enables the simultaneous deposition of both phases on the same substrate within a single CVD process, offering spatial control over the distribution of the phases and allowing for precise regulation of the number of layers, thereby tuning the properties of the $MoTe_2$ films.

The $MoTe_2$ films were extensively characterised using Raman spectroscopy, AFM, and XRD to ensure their quality and consistency. Additionally, AFM provided rapid and accurate measurements of the film thickness. The successful transfer of $MoTe_2$ films from the substrate demonstrates the potential of this new CVD method to expand the range of applications for $MoTe_2$ in various technological fields.

4.9 Reference:

1. Cho, S., Kim, S., Kim, J. H., Zhao, J., Seok, J., Keum, D. H., Baik, J., Choe, D.-H., Chang, K. J., Suenaga, K., Kim, S. W., Lee, Y. H., & Yang, H. (2015). Phase patterning for ohmic homojunction contact in MoTe2. *Science*, *349*(6248), 625–628. https://doi.org/10.1126/science.aab3175

2. Ma, R., Zhang, H., Yoo, Y., Degregorio, Z. P., Jin, L., Golani, P., Ghasemi Azadani, J., Low, T., Johns, J. E., Bendersky, L. A., Davydov, A. V., & Koester, S. J. (2019). MoTe2 Lateral Homojunction Field-Effect Transistors Fabricated using Flux-Controlled Phase Engineering. *ACS Nano*, *13*(7), 8035–8046. https://doi.org/10.1021/acsnano.9b02785

3. Zhu, X., Li, A., Wu, D., Zhu, P., Xiang, H., Liu, S., Sun, J., Ouyang, F., Zhou, Y., & Xiong, X. (2019). Tunable large-area phase reversion in chemical vapor deposited few-layer MoTe2 films. *Journal of Materials Chemistry C*, *7*(34), 10598–10604. https://doi.org/10.1039/C9TC03216A

4. Zhang, X., Jin, Z., Wang, L., Hachtel, J. A., Villarreal, E., Wang, Z., Ha, T., Nakanishi, Y., Tiwary, C. S., Lai, J., Dong, L., Yang, J., Vajtai, R., Ringe, E., Idrobo, J. C., Yakobson, B. I., Lou, J., Gambin, V., Koltun, R., & Ajayan, P. M. (2019). Low Contact Barrier in 2H/1T′ MoTe2 In-Plane Heterostructure Synthesized by Chemical Vapor Deposition. *ACS Applied Materials & Interfaces*, *11*(13), 12777–12785. https://doi.org/10.1021/acsami.9b00306

5. Manzeli, S., Ovchinnikov, D., Pasquier, D., Yazyev, O. V., & Kis, A. (2017). 2D transition metal dichalcogenides. *Nature Reviews Materials*, *2*(8), 17033. https://doi.org/10.1038/natrevmats.2017.33

6. Zhou, J., Lin, J., Huang, X., Zhou, Y., Chen, Y., Xia, J., Wang, H., Xie, Y., Yu, H., Lei, J., Wu, D., Liu, F., Fu, Q., Zeng, Q., Hsu, C.-H., Yang, C., Lu, L., Yu, T., Shen, Z., … Liu, Z. (2018). A library of atomically thin metal chalcogenides. *Nature*, *556*(7701), Article 7701. https://doi.org/10.1038/s41586-018-0008-3

7. Zhang, Y., Yao, Y., Sendeku, M. G., Yin, L., Zhan, X., Wang, F., Wang, Z., & He, J. (2019). Recent Progress in CVD Growth of 2D Transition Metal Dichalcogenides and Related Heterostructures. *Advanced Materials*, *31*(41), 1901694. https://doi.org/10.1002/adma.201901694

8. Kolobov, A. V., Fons, P., & Tominaga, J. (2016). Electronic excitation-induced semiconductor-to-metal transition in monolayer MoTe2. *Physical Review B*, *94*(9), 094114. https://doi.org/10.1103/PhysRevB.94.094114

9. Huang, J.-K., Pu, J., Hsu, C.-L., Chiu, M.-H., Juang, Z.-Y., Chang, Y.-H., Chang, W.-H., Iwasa, Y., Takenobu, T., & Li, L.-J. (2014). Large-area synthesis of highly crystalline WSe(2) monolayers and device applications. *ACS Nano*, *8*(1), 923–930. https://doi.org/10.1021/nn405719x

10. Ni, Z. H., Wang, H. M., Kasim, J., Fan, H. M., Yu, T., Wu, Y. H., Feng, Y. P., & Shen, Z. X. (2007). Graphene Thickness Determination Using Reflection and Contrast Spectroscopy. *Nano Letters*, *7*(9), 2758–2763. https://doi.org/10.1021/nl071254m

11. Wajid, A. (1997). On the accuracy of the quartz-crystal microbalance (QCM) in thin-film depositions. *Sensors and Actuators A: Physical*, *63*(1), 41–46. https://doi.org/10.1016/S0924-4247(97)80427-X

12. Tao, L., Chen, K., Chen, Z., Cong, C., Qiu, C., Chen, J., Wang, X., Chen, H., Yu, T., Xie, W., Deng, S., & Xu, J.-B. (2018). 1T′ Transition Metal Telluride Atomic Layers for Plasmon-Free SERS at Femtomolar Levels. *Journal of the American Chemical Society*, *140*(28), 8696–8704. https://doi.org/10.1021/jacs.8b02972

13. Song, X., Wang, Y., Zhao, F., Li, Q., Ta, H. Q., Rümmeli, M. H., Tully, C. G., Li, Z., Yin, W.-J., Yang, L., Lee, K.-B., Yang, J., Bozkurt, I., Liu, S., Zhang, W., & Chhowalla, M. (2019). Plasmon-Free Surface-Enhanced Raman Spectroscopy Using Metallic 2D Materials. *ACS Nano*, *13*(7), 8312–8319. https://doi.org/10.1021/acsnano.9b03761

14. Naylor, C. H., Parkin, W. M., Ping, J., Gao, Z., Zhou, Y. R., Kim, Y., Streller, F., Carpick, R. W., Rappe, A. M., Drndić, M., Kikkawa, J. M., & Johnson, A. T. C. (2016).

Monolayer Single-Crystal 1T′-MoTe2 Grown by Chemical Vapor Deposition Exhibits Weak Antilocalization Effect. *Nano Letters*, *16*(7), 4297–4304. https://doi.org/10.1021/acs.nanolett.6b01342

15. Fraser, J. P., Masaityte, L., Zhang, J., Laing, S., Moreno-López, J. C., McKenzie, A. F., McGlynn, J. C., Panchal, V., Graham, D., Kazakova, O., Pichler, T., MacLaren, D. A., Moran, D. A. J., & Ganin, A. Y. (2020). Selective phase growth and precise-layer control in MoTe2. *Communications Materials*, *1*(1), Article 1. https://doi.org/10.1038/s43246-020-00048-4

16. Wang, T., Li, J., & Zhao, G. (2014). Synthesis of MoS2 and MoO3 hierarchical nanostructures using a single-source molecular precursor. *Powder Technology*, *253*, 347–351. https://doi.org/10.1016/j.powtec.2013.12.005

17. Jin, Y., & Shen, P. K. (2015). Nanoflower-like metallic conductive MoO2 as a high-performance non-precious metal electrocatalyst for the hydrogen evolution reaction. *Journal of Materials Chemistry A*, *3*(40), 20080–20085. https://doi.org/10.1039/C5TA06018D

18. Guo, H., Yang, T., Yamamoto, M., Zhou, L., Ishikawa, R., Ueno, K., Tsukagoshi, K., Zhang, Z., Dresselhaus, M. S., & Saito, R. (2015). Double resonance Raman modes in monolayer and few-layer ${\mathrm{MoTe}}_{2}$. *Physical Review B*, *91*(20), 205415. https://doi.org/10.1103/PhysRevB.91.205415

19. Yamamoto, M., Wang, S. T., Ni, M., Lin, Y.-F., Li, S.-L., Aikawa, S., Jian, W.-B., Ueno, K., Wakabayashi, K., & Tsukagoshi, K. (2014). Strong Enhancement of Raman Scattering from a Bulk-Inactive Vibrational Mode in Few-Layer MoTe2. *ACS Nano*, *8*(4), 3895–3903. https://doi.org/10.1021/nn5007607

20. Eaton, P., & West, P. (2010). *Atomic Force Microscopy*. Oxford University Press. https://doi.org/10.1093/acprof:oso/9780199570454.001.0001

21. Zhou, L., Xu, K., Zubair, A., Zhang, X., Ouyang, F., Palacios, T., Dresselhaus, M. S., Li, Y., & Kong, J. (2017). Role of Molecular Sieves in the CVD Synthesis of Large-Area 2D MoTe2. *Advanced Functional Materials*, *27*(3), 1603491. https://doi.org/10.1002/adfm.201603491

22. Lv, Q., Wu, X., Tan, J., Liu, B., Gan, L., Li, J., Huang, Z.-H., Kang, F., & Lv, R. (2021). Ultrasensitive molecular sensing of few-layer niobium diselenide. *Journal of Materials Chemistry A*, *9*(5), 2725–2733. https://doi.org/10.1039/D0TA09520F

5.0 $MoTe_2$ FET Fabrication Method and Process Flow

As electronic devices scale down to nanometre dimensions, increasingly complex fabrication methods are required, particularly for challenging materials like two-dimensional (2D) structures consisting of only one or a few monolayers. Due to the delicate nature of thin-film structures, fabricating electrical devices using 2H-$MoTe_2$ presents significant challenges. The primary objective of this research is to integrate the thin-film CVD synthesis techniques, as outlined in previous chapters, with traditional photolithography methods, which predominantly follow a bottom-up fabrication approach. This integration aims to produce a series of FET devices with varying film thicknesses, lateral dimensions, and spatial configurations. Compared to top-down approaches, such as flake exfoliation, this strategy offers greater flexibility and adaptability. Furthermore, the direct growth of $MoTe_2$ layers on specific substrates is better suited for mass production than exfoliation-based techniques.

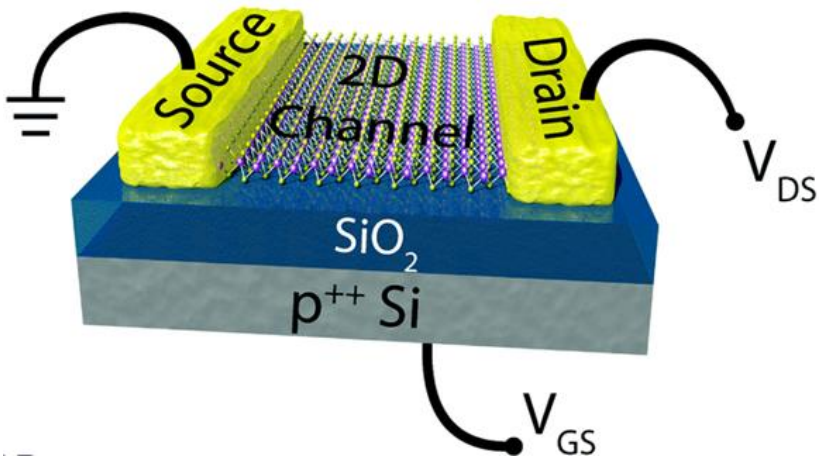


Figure 5.1 Schematic diagram of a typical backgated multilayer 2D device with Ti/Au[1].

Figure 5.1[1] shows a schematic of a typical back-gated $MoTe_2$ FETs, which includes Ti/Au source and drain contacts, SiO_2 as the gate dielectric, and a highly doped Si substrate serving as the back gate. A back-gated FET comprises a metal gate on the

substrate's underside, a 2D semiconductor channel between the source and drain, and an insulating gate oxide that separates the channel from the gate. The source-drain voltage (V_{ds}) controls the current through the semiconductor channel (drain current, I_{ds}), while the gate voltage (V_{gs}) modulates this current by altering the channel's conductivity[2].

This chapter details the fabrication process developed for 2H-$MoTe_2$ FETs, focusing on thin-film preparation and subsequent structural evaluation. Test structures, such as transfer length method (TLM) and FET devices, were fabricated using these techniques. A crucial aspect of this work is the preservation of the $MoTe_2$ thin film during conventional semiconductor processing to ensure optimal device performance. Specifically, the lithography recipe was updated and refined to protect the $MoTe_2$ film and maintain FET functionality throughout fabrication.

The primary lithography techniques used in semiconductor fabrication include photolithography, electron beam lithography (EBL), and nanoimprint lithography (NIL)[3]. In this work, photolithography was exclusively used. Photolithography involves using ultraviolet (UV) light to project a geometric pattern from a photomask onto a photosensitive polymer, or "photoresist"[3]. One of photolithography's key advantages is its exceptional reproducibility, due to the streamlined procedure that follows mask production, which includes photoresist spinning, UV exposure, and development[4]. However, a limitation of this method is the reduced design flexibility once the mask is fabricated.

5.1 Photolithography and Process

Photolithography is the most widely used technique in modern semiconductor manufacturing for patterning microscale features. In this process, a mask is placed over the photoresist to expose it to a predefined pattern, enabling the transfer of the pattern onto the photoresist-coated surface. In contact lithography, the mask directly interfaces with the photoresist during exposure.

The photomask used in this study comprises two layers, each corresponding to different features: one layer for the $MoTe_2$ and another for the contact metal. This straightforward double-layer mask design prioritises the preservation of the thin film's integrity while minimising potential damage. Detailed procedures for these steps will be elaborated upon in the following sections.

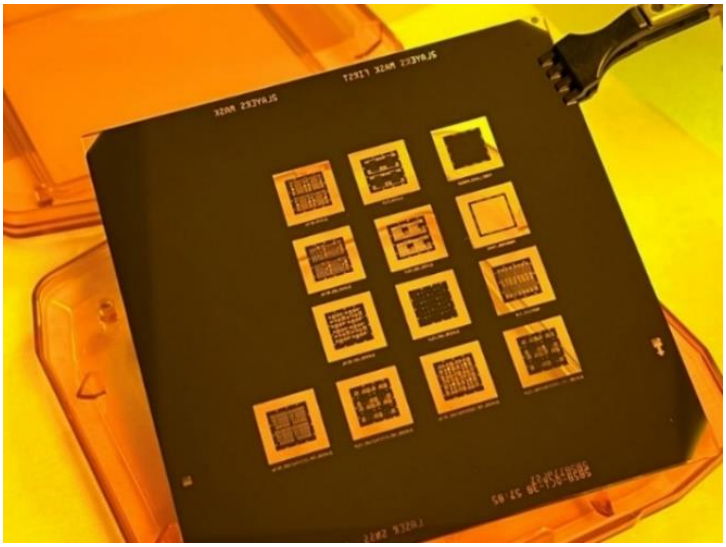


Figure 5.2 Photograph of photolithography mask used for the fabrication of $MoTe_2$ FETs as fabricated by the external company.

For this experiment, heavily p-doped silicon was employed as the global back gate. Figure 5.2 presents a photograph of the photomask designed for the back-gated

$MoTe_2$ FET. After exposure, the sample was developed in a solution to remove the exposed regions of the photoresist, resulting in the desired pattern being imprinted on the surface, as illustrated in Figure 5.3. Due to the large number of micrometre-sized features in the FET, only optical lithography was utilised for fabrication.

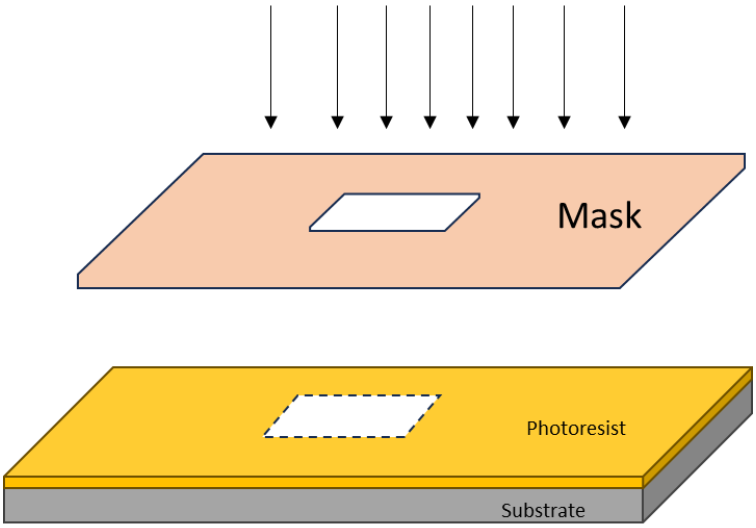


Figure 5.3 Illustration of photolithography, selectively exposing a photoresist-coated sample to light through a patterned mask[5].

The key advantages of photolithography include its compatibility with modern manufacturing processes and its efficiency in rapidly producing devices. Furthermore, photolithography is essential for industrial-scale mass production, rendering it suitable for experiments that require thin-film materials to be produced in large quantities. In this study, photolithography was employed to develop and validate the experimental plan. The process involved several steps, including the application of different photoresist layers, development, O_2 plasma "de-scumming" to clean the substrate, and the lift-off procedure.

5.2 $MoTe_2$ FET Fabrication Process Flow

To address the sensitivity of $MoTe_2$ thin films during field-effect transistor (FET) fabrication, it is essential to develop and optimise new methods that can replace mechanical exfoliation. The combination of photolithography with advanced chemical vapour deposition (CVD) techniques to create a systematic fabrication process is an area of significant research interest. However, minimising the negative impact of the fabrication process on the thin film is critical. In this study, a back-gated $MoTe_2$ FET structure was employed. As outlined in Table 5.1, the fabrication process consists of four primary stages: precursor Mo patterning via CVD, synthesis and characterisation of 2H-$MoTe_2$, definition of metal contacts, and construction of the back-gate electrode.

Table 5.1 Summary of the main step for fabricating $MoTe_2$ FET

Step	Description
1	Patterned Mo deposited and lifted off
2	Patterned Mo film converted to $MoTe_2$
3	Ohmic contact patterned and deposited
4	Back gate formed

This chapter focuses on optimising the manufacturing process for back-gated $MoTe_2$ FETs using the previously described photolithography techniques. The $MoTe_2$ films produced in this study are illustrated in Figure 5.4. Patterned growth of $MoTe_2$ was achieved by defining the Mo precursor film through photolithography, while the CVD

conversion of Mo to $MoTe_2$, as detailed in Chapter 4, allowed for control over the number of $MoTe_2$ layers by adjusting the thickness of the Mo precursor.

The SiO_2/Si substrates, which are 500 μm thick and measure 12 × 12 mm², were sourced from Inseto and prepared by sonicating in acetone and isopropyl alcohol (IPA) for 10 minutes each, followed by nitrogen drying. Contact metal patterns were defined using physical vapour deposition (PVD) in conjunction with photolithography. Special attention was given to the effects of direct contact metal deposition on the $MoTe_2$ film and the structural changes that occurred when preparing the back-gate electrode. To maintain the uniformity of the deposited film, it is crucial to ensure that the exposed surface is free of impurities, such as resist residue, prior to material deposition.

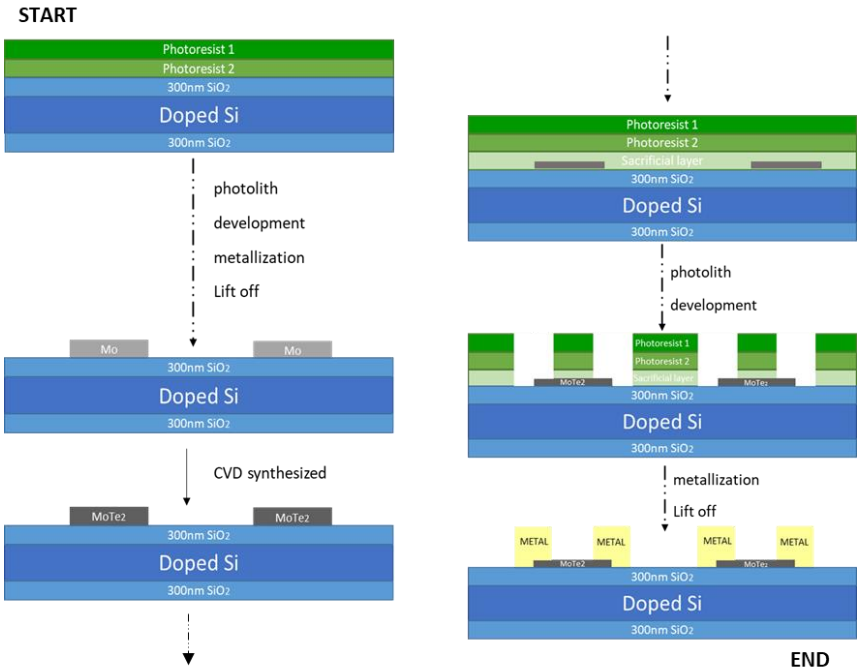


Figure 5.4 The top structure about film and metal contact definition fabrication process combined with $MoTe_2$ CVD and photolithography technology.

5.3 1st layer Feature Defined: $MoTe_2$ Feature

As previously mentioned, the $MoTe_2$ FET device designed in this work primarily employs a double-layer mask to pattern both 2H-$MoTe_2$ and the contact metal. Therefore, it is essential to examine the photolithographic patterning steps for these two layers separately.

The first step involves defining the 2H-$MoTe_2$ pattern on the substrate, with the primary challenge being the precise patterning of the Mo precursor. A double-layer photoresist is exposed and developed to create the desired structure on the substrate. Subsequently, a 5 nm Mo film is deposited into the pattern using a Plassys MEB400 electron beam evaporation system. Following the lift-off process, the patterned Mo film remains on the substrate. The process flow for the first layer is illustrated in Figure 5.5.

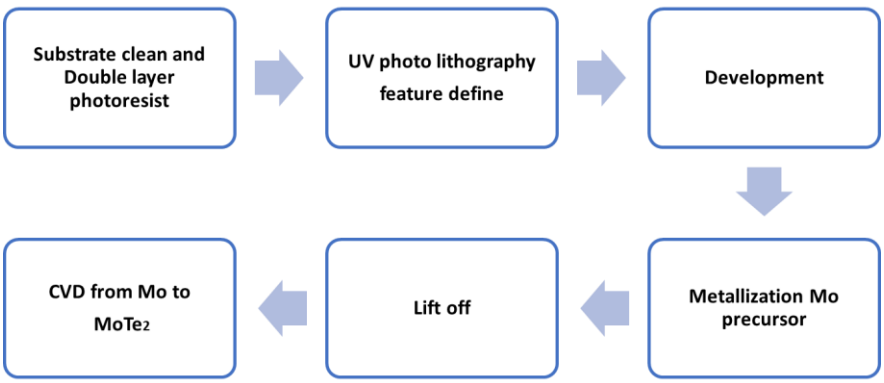


Figure 5.5 Process flow for $MoTe_2$ with controlled feature

As previously noted, residual photoresist can adversely affect the uniformity and surface roughness of the deposited material. Once the Mo is patterned, it is transferred to the CVD system for conversion into 2H-$MoTe_2$. The following sections will provide

a detailed discussion of the research, characterization, and specific steps involved in the preparation of 2H-$MoTe_2$.

5.3.1 Markers

Alignment is crucial for performing multi-layer lithography. In this process, photolithography is used to achieve patterning on the substrate through metallization and a double-layer photoresist. During the photolithography step, the marker metal must undergo the CVD process at 650°C[6]. Most metals tend to deform or melt at such high temperatures, making them unsuitable as reliable markers.

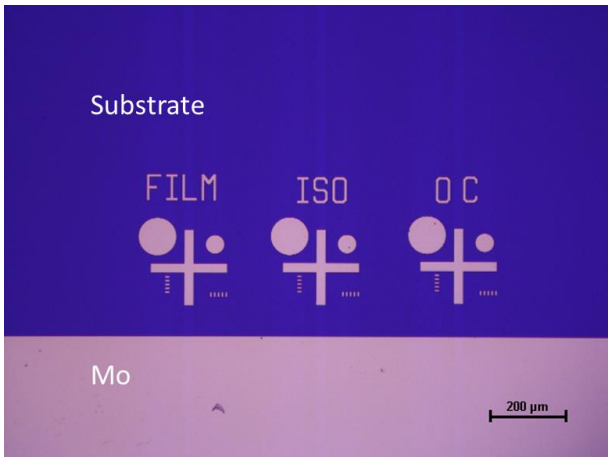


Figure 5.6 Photolithography markers with Mo deposition

Additionally, to prevent contamination of the CVD reaction with other metals that could affect the synthesis, 30 nm Mo was selected as the marker material, minimizing the risk of impurity generation. Figure 5.6 presents an optical microscope image of the Mo marker, illustrating its role in avoiding contamination and ensuring material purity throughout the process. The films produced via CVD exhibit high reflectivity, which is advantageous for observation and characterization.

5.3.2 Selective development Solution and Ash recipe

The first step in defining the Mo pattern involves spin-coating a double photoresist layer. LOR3A and S1805 photoresists were applied to the substrate through spin-coating, followed by a baking process to remove excess solvent. The pattern was subsequently defined using the MA6 mask aligner and developed.

The surface roughness of $MoTe_2$ significantly impacts the performance of electronic devices, and the roughness of the Mo films directly influences the quality of the resulting $MoTe_2$ film. Additionally, the roughness of the original substrate in the developed areas plays a crucial role in determining the final surface characteristics of the film. Therefore, ensuring a smooth, residue-free substrate after development is essential for achieving accurate film definition.

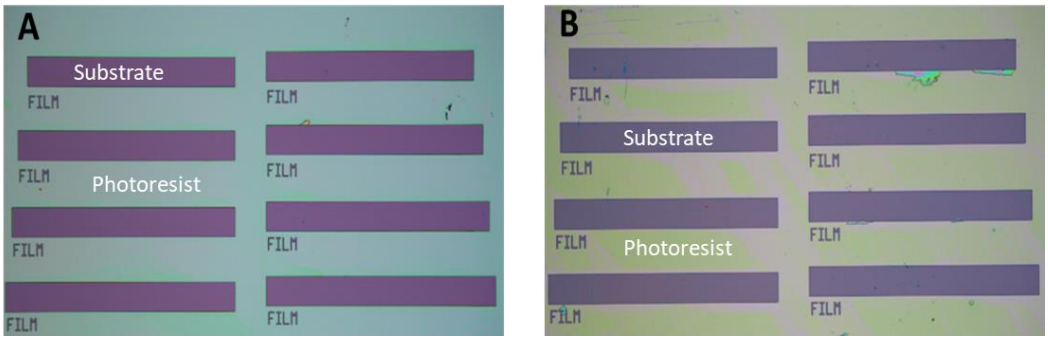


Figure 5.7 The optical microscope image for the defined Mo feature with (A) CD-26 and (B) MF-139 development result

To optimize the photolithography process, the effects of different developing solutions on the deposited films were studied and compared, with the results presented in Figure 5.7. Samples developed with CD-26 exhibited a cleaner substrate surface with minimal residue, while those developed with MF-139 retained more photoresist residue. Consequently, CD-26 was selected as the primary developer for this study. Figure 5.8

illustrates a comparative optical microscope image of the sample before and after the ashing process. The ashing effectively removed residual photoresist from the SiO_2 substrate using oxygen plasma at 100 W for 1 minute.

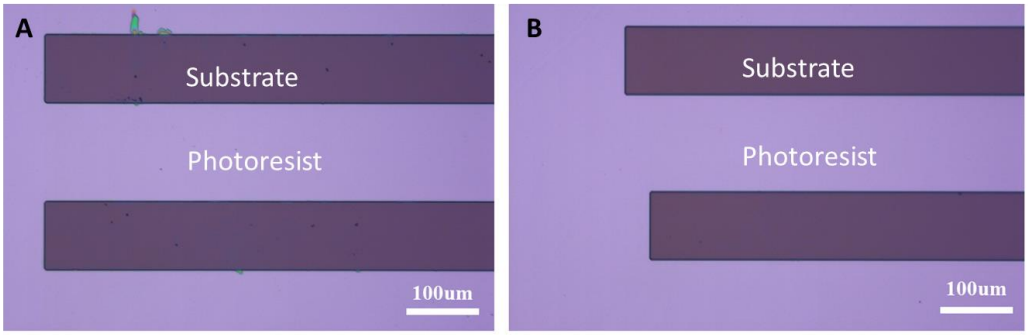


Figure 5.8 The developed sample using an oxygen ash before (left) and after (right)

5.3.3 Lift-off solution selective

As outlined in previous studies, after achieving a clean and smooth developed substrate, the next step is the metal deposition of Mo films followed by lift-off to prepare patterned Mo films for conversion to 2H-$MoTe_2$ via CVD. During the lift-off process, the resist and the deposited Mo films are immersed in a solution. It is essential to minimize Mo oxidation, as it can negatively affect the conversion process to 2H-$MoTe_2$.

The lift-off process involves submerging the sample in a solution, with dissolution accelerated in a 50°C water bath. To evaluate the impact of different solutions on the oxidation of Mo films, two lift-off solutions, 1165 and SVC-14, were compared. Two samples, each deposited with 5 nm Mo films, underwent lift-off in these solutions.

Atomic force microscopy (AFM) and scanning electron microscopy (SEM) were utilized to evaluate the patterned Mo films, with the results shown in Figures 5.9 and 5.10. The roughness measurements for Mo in Figure 5.9 were as follows: (A) Rq = 0.65 nm and

(B) Rq = 0.96 nm, indicating a slight increase in roughness with the SVC-14 solution. However, SEM images revealed no significant visible differences between the two samples.

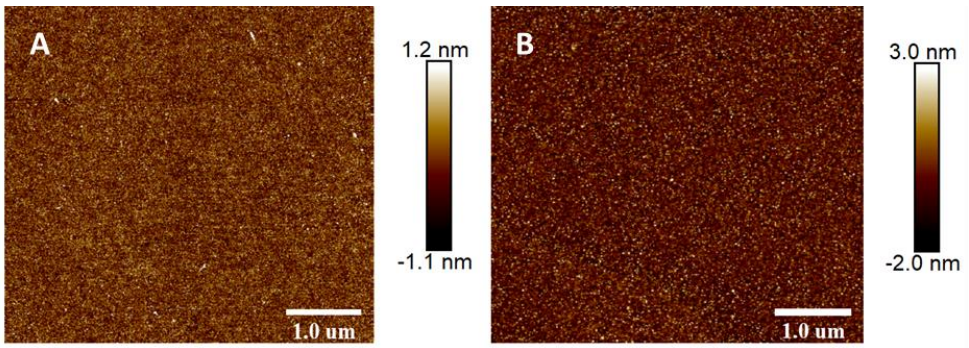


Figure 5.9 The AFM characteristic on the defined Mo film with (A) 1165 and (B) SVC-14 lift off solution.

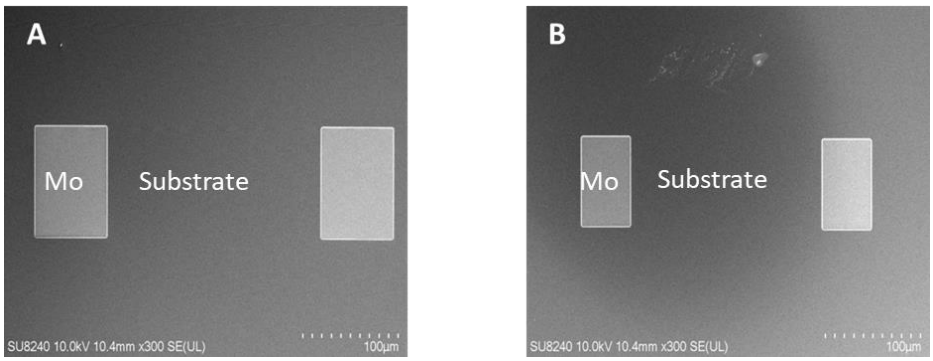


Figure 5.10 The SEM characteristic on the Mo film feature with (A) 1165 and (B) SVC-14 lift off solution.

Since AFM and SEM cannot directly determine the oxidation state of molybdenum (Mo) films, both samples were synthesized into $MoTe_2$, and their crystal structures were analyzed using Raman spectroscopy[8]. presents a comparison of the Raman spectra for both samples. The red spectrum, corresponding to the sample processed with the SVC-14 lift-off solution, exhibits peaks at 80, 108, 125, 161, 251, and 265 cm^{-1}. These peaks are consistent with the 1T-$MoTe_2$ phase, indicating the presence of Mo oxides

that caused the conversion to 1T-$MoTe_2$ rather than the desired 2H phase. Furthermore, a peak at 171 cm^{-1}, characteristic of the 2H-$MoTe_2$ phase, was also observed, suggesting a mixture of phases. This result implies that oxidation occurred during the lift-off process, leading to partial conversion of the Mo film to 1T-$MoTe_2$[8]. In contrast, the blue spectrum, corresponding to the sample processed with the 1165 lift-off solution, displays peaks at 171, 234, and 289 cm^{-1}, which are characteristic of the pure 2H-$MoTe_2$ phase. This indicates that the 1165 solution effectively prevented Mo oxidation, preserving the desired 2H-$MoTe_2$ structure without significant contamination by the 1T phase. These results demonstrate the importance of selecting an appropriate lift-off solution to control the phase purity of $MoTe_2$ during fabrication

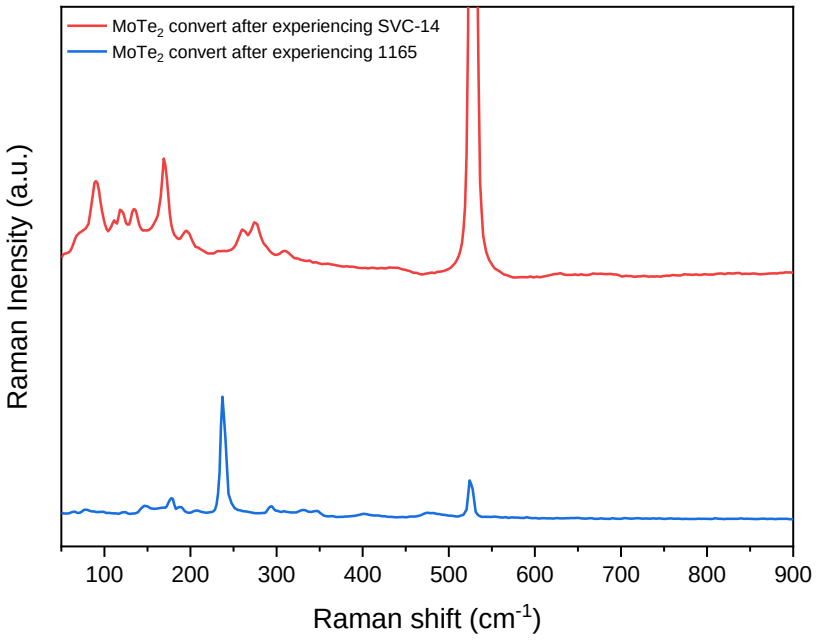


Figure 5.11 The Raman characterisation result for Mo film converted to $MoTe_2$ after experiencing the 1165 and svc-14 lift-off solution.

Therefore, based on the analysis of the chemical vapour deposition (CVD) synthesis method, this sample contains certain molybdenum oxides. This indicates that during

the lift-off process, the molybdenum is sufficiently oxidised to result in the formation of the 1T phase, while the pure 2H phase is not obtained. In contrast, the blue Raman results for the 1165 solution reveal characteristic peaks at 171, 234, and 289 cm^{-1}, corresponding to the 2H-$MoTe_2$ phase. This indicates that the molybdenum film lifted off and developed using the 1165 solution can successfully produce the 2H phase.

Consequently, the 1165 lift-off solution is deemed suitable for preparing $MoTe_2$ field-effect transistors (FETs) based on this comparative analysis. To further confirm that the $MoTe_2$ obtained through the 1165 lift-off solution is suitable for FET fabrication, the roughness and surface morphology of both Mo and $MoTe_2$ films were characterised using atomic force microscopy (AFM), with the results presented in Figures 5.12..

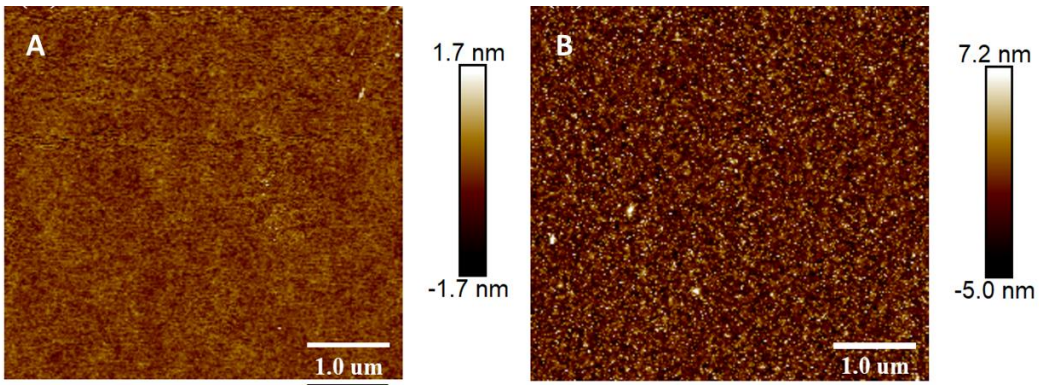


Figure 5.12 The AFM result on the defined (A) Mo and (B) $MoTe_2$ with 1165 lift-off solution.

To further validate the suitability of $MoTe_2$ produced using the 1165 solution for field-effect transistor (FET) fabrication, the roughness and surface morphology of both Mo and $MoTe_2$ films were analysed using atomic force microscopy (AFM), as illustrated in Figure 5.12. The surface roughness increased from 0.652 nm (Mo) to 1.285 nm ($MoTe_2$) after the chemical vapour deposition (CVD) conversion. Scanning electron microscopy (SEM) results further confirmed that the $MoTe_2$ film was continuous, supporting its potential for device fabrication, as displayed in Figure 5.13.

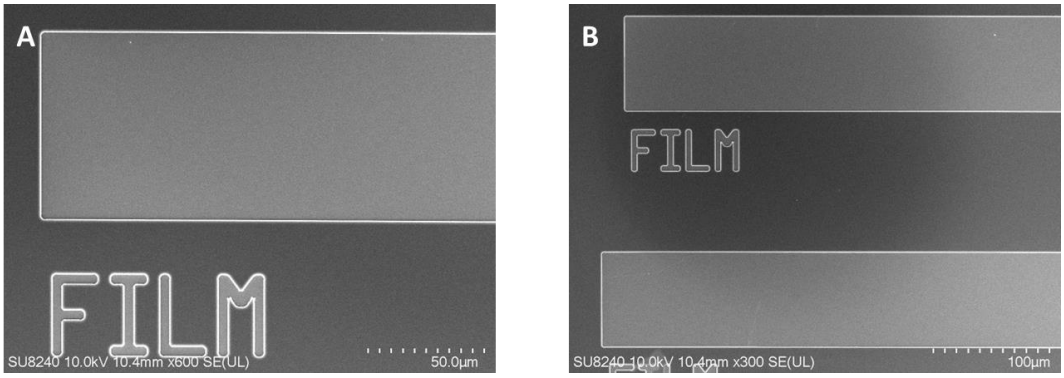


Figure 5.13 The SEM result on the defined (A) Mo and (B) $MoTe_2$ with 1165 lift-off solution.

5.4 2nd layer Feature Define: Ohmic Contact Metal

The process for patterning the contact metal structures follows the same fundamental steps as those used to define the molybdenum (Mo) precursor thin film. Figure 5.14 illustrates the photolithographic process employed to prepare the ohmic metal contacts. A double-layer photoresist is applied to define the metal pattern, which is then developed on the $MoTe_2$ surface. Following development, metal deposition and lift-off are performed to achieve the desired patterned metal contacts.

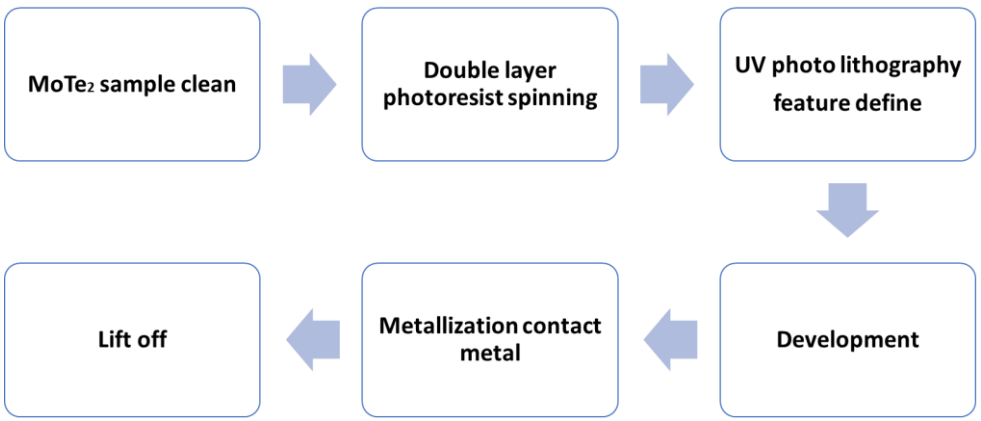


Figure 5.14 Process flow for contact metal definition

The primary distinction between the photolithography processes for the molybdenum (Mo) precursor and the contact metal layers is that the latter requires an additional photolithography step on the pre-deposited $MoTe_2$ layer. This step is critical, as it ensures that the $MoTe_2$ remains undamaged during the fabrication of the second-layer structure, particularly during the definition of the metal contacts.

5.4.1 Characterization of Patterned Contact Metal with 1st Layer Recipe

The structure depicted in Figure 5.15 was fabricated following the process outlined in the same figure, combined with the first photolithography recipe, to define the contact metal pattern on the $MoTe_2$ layer.

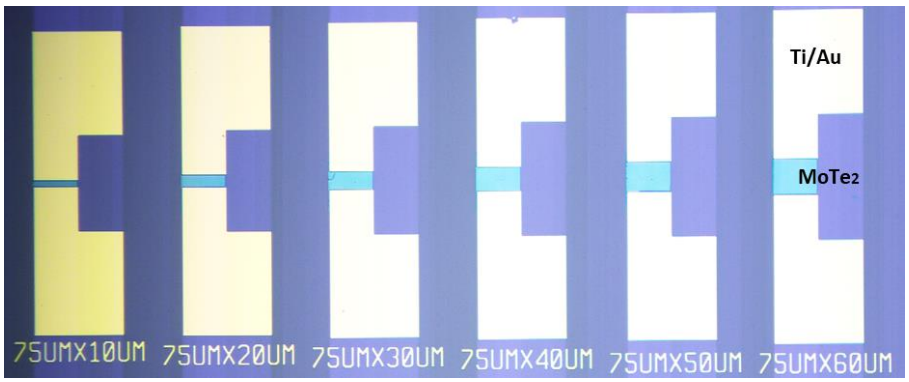


Figure 5.15 The image of contact metal patterned on $MoTe_2$ with 1st layer photolithography recipe.

A two-probe current-voltage (I-V) measurement was conducted to evaluate the current flow between the $MoTe_2$ film and the contact metal (20 nm Ti/80 nm Au). The results indicated that no measurable current above the system's noise floor could be detected through the film. Following thorough testing and examination, it was determined that a gap existed between the edge of the ohmic contact metal and the $MoTe_2$ film. Figure 5.16 provides detailed measurements obtained using various techniques, including (A)

optical microscopy, (B) scanning electron microscopy (SEM), (C) atomic force microscopy (AFM), and (D) optical profilometry.

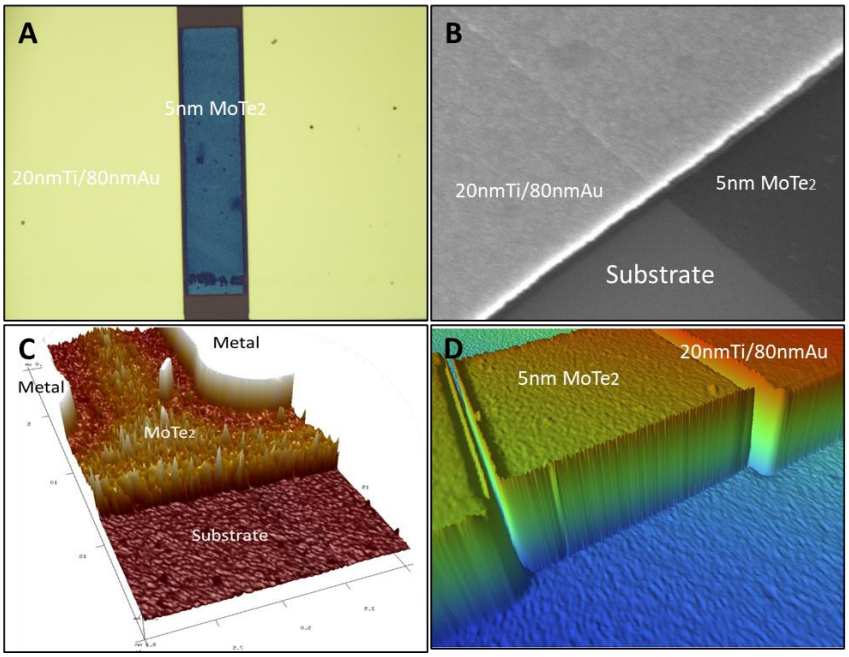


Figure 5.16 The characterisation of contact metal patterned on $MoTe_2$ occurred gap problem with (A) Optical Microscope, (B) SEM, (C) AFM, and (D) Optical Profiler

This gap likely resulted from the $MoTe_2$ film fracturing during the preparation of the second-layer structure, which prevented direct contact with the metal. The causes of this fracture are discussed in the subsequent section. Addressing these issues necessitated improving and optimising the photolithography recipe to better accommodate the definition of metal contacts, ensuring the successful fabrication of field-effect transistor (FET) devices. Furthermore, the atomic force microscopy (AFM) results shown in Figure 5.16 revealed a significant increase in surface roughness compared to the data presented earlier. Thus, maintaining the uniformity and continuity of the $MoTe_2$ film remains a critical concern that warrants further attention.

5.4.2 Inspection of impact of development process on $MoTe_2$ films

As previously discussed, photoresist residue may have contributed to the increased surface roughness of $MoTe_2$ films, particularly since the oxygen ash cleaning procedure following development was intentionally omitted to prevent potential damage to the $MoTe_2$ film. Another possible explanation for the gap observed between the ohmic metal and the $MoTe_2$, as shown in Figure 5.16, is the potential etching of $MoTe_2$ by the developer solution. To investigate this, a comparative study was conducted on the choice of developer and development time. The results are presented in Figure 5.17, with panels (A) and (B) showing the results from using CD-26, while panel (C) illustrates the outcome of using MF-139.

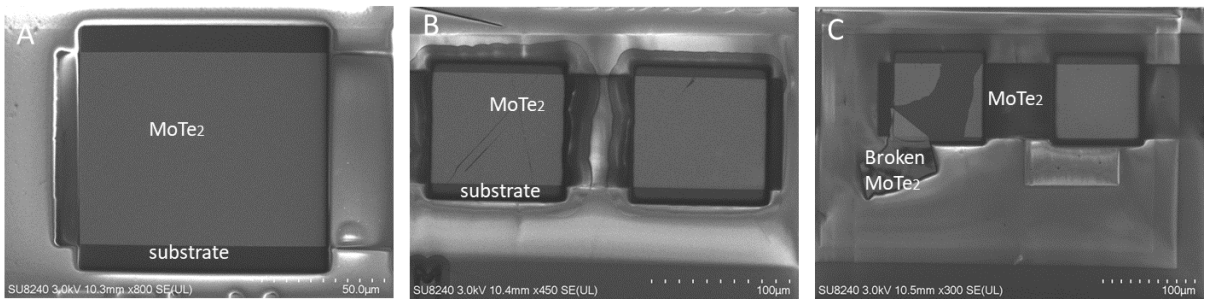


Figure 5.17 SEM results for FET fabrication using various developer recipes.

The comparison between CD-26 and MF-139 revealed significant differences in performance. CD-26 proved more effective, leaving less photoresist residue than MF-139. Additionally, optimising the development time was found to be critical; a 1-minute development period produced a cleaner and more uniform film surface compared to the longer 1 minute 20 seconds duration. Scanning electron microscopy (SEM) analysis further supported these findings, revealing minor cracks in samples developed with CD-26 for 1 minute 20 seconds. Therefore, a 1-minute development time using CD-26 in the second-layer lithography process for defining metal contacts

is recommended as the optimal approach to achieve high-quality patterned metal contact structures.

5.4.3 Optimized 2nd Photolithography Recipe for Metal Contact Definition

Further inspection and analysis revealed that development and lift-off are critical steps for achieving direct contact with $MoTe_2$. To address issues related to film etching or fracturing, which led to separation from the ohmic metal, a control experiment was designed. In this experiment, samples underwent photoresist spin coating, followed by development using CD-26 and lift-off with 1165. Notably, metal deposition was omitted at this stage to facilitate the observation of changes in the $MoTe_2$ film. This approach allowed for the simultaneous observation of regions covered and developed by the photoresist, enabling a comparative analysis. The results of this comparative experiment are presented in Figure 5.18.

Figure 5.18 $MoTe_2$ film after development using CD26 and lift-off without metallisation.

Under an optical microscope, distinct colour differences were observed between the photoresist-covered and developed areas on the same $MoTe_2$ film. The developed regions appeared darker and rougher, with pronounced dividing lines compared to the undeveloped areas.

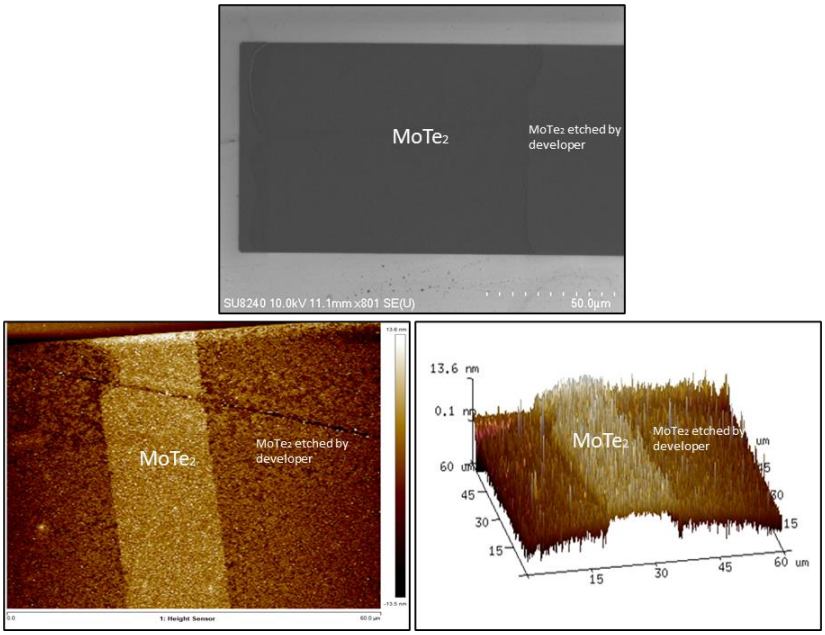


Figure 5.19 illustrates SEM and AFM measurements for the interface between the etched and unetched $MoTe_2$ film.

Further examination using AFM and SEM, as shown in Figure 5.19, provided additional insights. The SEM images and AFM 3D measurements indicated that the developed areas of the $MoTe_2$ film were etched. This suggests that the developer interacted with the $MoTe_2$ film during the development process, causing an etching reaction. The AFM results reveal that the surface roughness of the developed region (Rq = 1.2 nm) is significantly higher than that of the undeveloped region (Rq = 0.85 nm). This difference suggests that when metal is deposited onto $MoTe_2$ immediately after development, the increased roughness of the damaged area will likely result in film breakage, which could disrupt the current flow through the device. These findings emphasise the critical role of the developer in achieving optimal ohmic contact with $MoTe_2$.

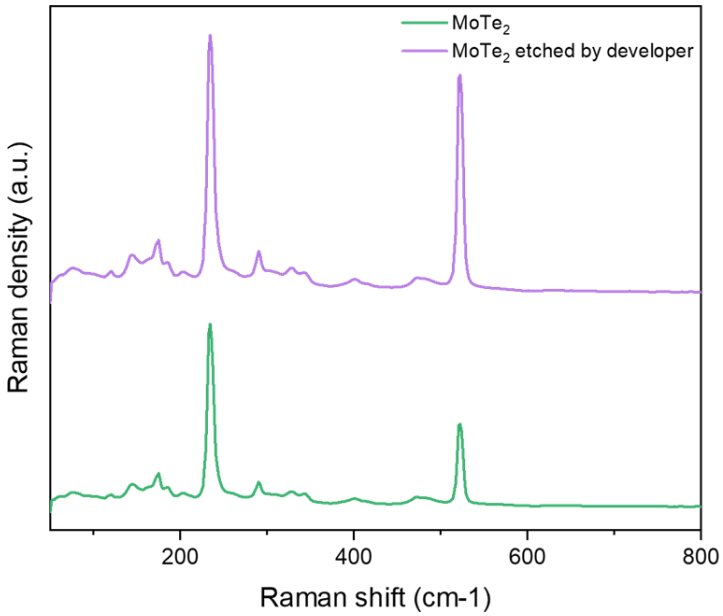


Figure 5.20 The Raman characteristic for the $MoTe_2$ film etched by the developer and covered with resist.

Moreover, the results indicate that the lift-off process used to remove the photoresist does not adversely affect the integrity of the $MoTe_2$, providing a promising method for preserving its structure during subsequent fabrication steps. To assess whether the developer-induced damage impacted the film's properties, Raman spectroscopy was conducted on both the damaged and undamaged regions, with the results displayed in Figure 5.20. The Raman spectra demonstrate that, despite the physical etching caused by the developer, the crystalline structure of the $MoTe_2$ remains intact in both regions, as evidenced by the retention of the 2H phase. These results suggest that while the developer etches the $MoTe_2$ film, it does not alter its crystalline structure.

Consequently, the photolithography process for defining metal contacts on the second-layer structure must be revised to prevent damage to the $MoTe_2$ film. This revision involves selecting a more suitable developer that minimises etching and physical

damage. Figure 5.21 presents test results obtained from using various developers, highlighting that $MoTe_2$, particularly when prepared via chemical vapour deposition (CVD), exhibits sensitivity to alkaline developers.

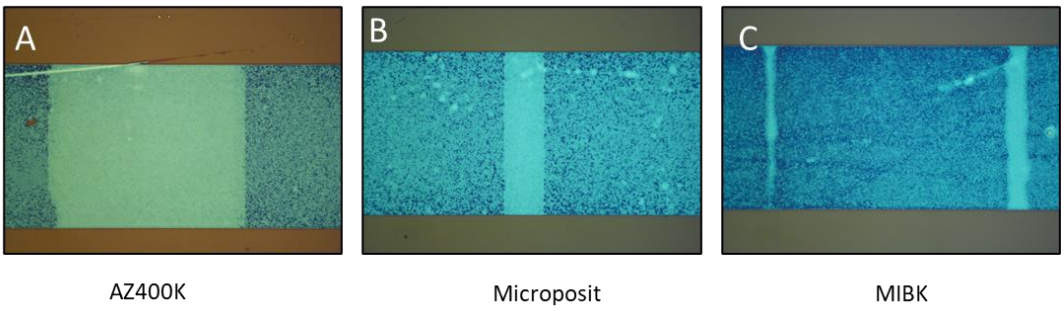


Figure 5.21 illustrates the impact of (A) AZ400K, (B) Microposit and (C) MIBK developers on the CVD $MoTe_2$ film.

This finding also provides insight into the granular and cracked appearance of films transferred using potassium hydroxide (KOH), as observed in Chapter 4. Given this sensitivity, optimising developer choice alone is insufficient to fully mitigate film damage. To prevent direct contact between the $MoTe_2$ and the developer, an effective solution is to introduce an assist layer of SPR.92 resist. SPR.92 is a water-soluble photoresist that serves as a protective barrier, preventing direct developer-induced etching of the $MoTe_2$ while also facilitating pattern transfer for metal contacts. This method offers a robust approach to preserving the integrity of the $MoTe_2$ during the metal deposition process. The use of SPR.92 successfully enables the transfer of the designed pattern onto the $MoTe_2$ surface without causing any etching or damage to the material. By introducing this assist layer, the contact metal structure can be accurately formed on the $MoTe_2$, maintaining its integrity. The device structure fabricated using this optimised process is shown in Figure 5.22.

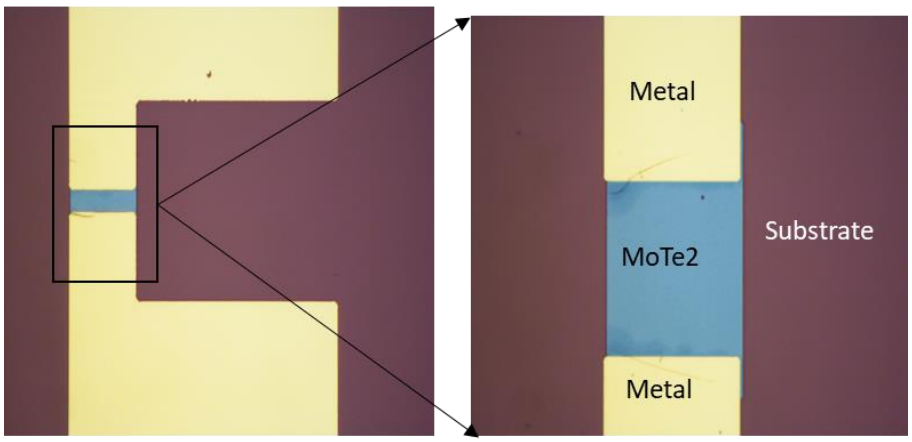
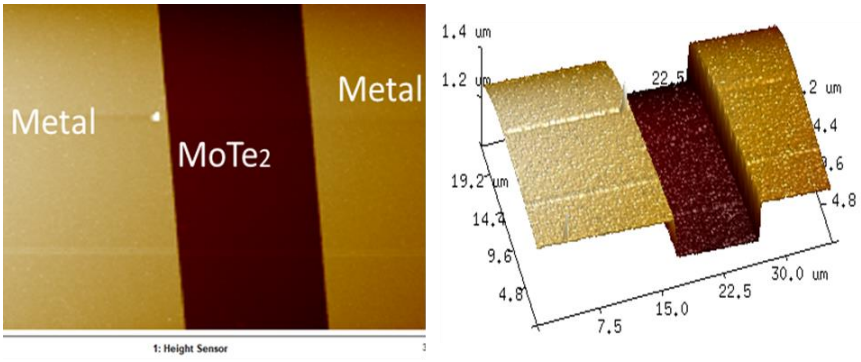


Figure 5.22 The optical microscope image of the FET structure following an optimised fabrication process using SPR.92 resist.

Figure 5.23 presents the atomic force microscopy (AFM) measurement results of samples fabricated using the optimised resist and development process. The data indicate that the film's roughness remains within acceptable limits, confirming the effectiveness of the refined fabrication method in accurately defining the contact metal pattern. As expected, there is a slight increase in roughness with the added thickness of the $MoTe_2$ layers, with the 8-layer $MoTe_2$ film exhibiting a roughness of approximately 2 nm. Following the photolithography process, the roughness of the $MoTe_2$ film, measured at 1.53 nm, remains well within the acceptable range defined by the new chemical vapour deposition (CVD) system.



Surface	Rq (nm)
2H-$MoTe_2$	1.53
Metal	2.48

Figure 5.23 AFM result for the interface between $MoTe_2$ and contact metal.

With the $MoTe_2$ and contact metal structure in place, the next phase of device processing focused on preparing the upper structure of the field-effect transistor (FET) prior to incorporating the back gate. Figure 5.24 shows a scanning electron microscopy (SEM) image of the fabricated devices and test structures. The image clearly demonstrates the smoothness and uniformity of both the $MoTe_2$ film and the metal contacts, with no observable gaps between the ohmic metal and the $MoTe_2$ thin film, representing an improvement over previous failed device.

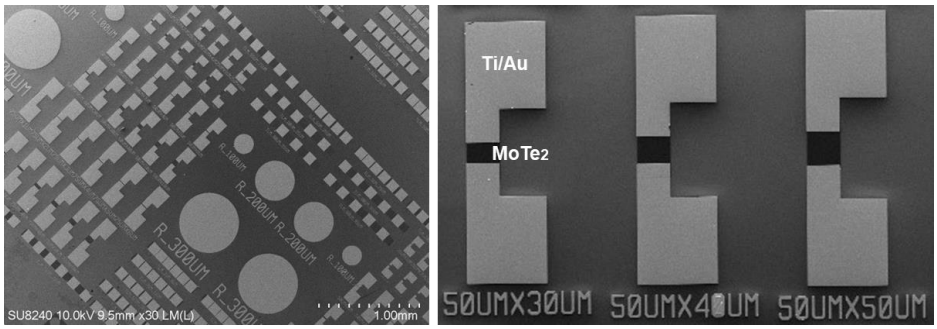


Figure 5.24 Top structure of SEM after 2nd layer metal feature definition recipe optimised.

In the modified process, SPR.92 resist was first spin-coated onto a clean, well-defined $MoTe_2$ film, followed by the application of double photoresist layers. This was succeeded by a series of photolithography steps, including exposure, development, metallisation, and lift-off, culminating in the construction of the second-layer metal structure. At this stage, the upper structure of the field-effect transistor (FET) has been completed, with the final task being the development of the back gate electrode.

5.5 Backgate Preparation

The field-effect transistors (FETs) employ a back-gate configuration to minimise the impact of the photolithography process on the upper structure while enabling gating and charge accumulation beneath the ohmic contacts. The substrate used was highly p-doped silicon, double-polished, with a 100 nm thick SiO_2 layer on both the top and bottom surfaces. To establish a uniform contact surface and ensure that the heavily doped silicon functions as the back gate electrode, the 100 nm SiO_2 layer on the backside of the substrate needed to be removed. Two primary techniques for SiO_2 removal are wet etching and dry etching.

5.5.1 Dry Etch and Wet Etch SiO_2

The initial investigation evaluated the effectiveness of the dry etching process using CH_3/Ar gas to remove SiO_2 from the backside of the silicon wafer. With an etch rate of 34 nm/min, the etching process was set to run for 9 minutes. Post-etching, the surface roughness of the samples was measured to be in the range of 3–5 nm. However, both the surface roughness and the SiO_2 removal were insufficient to meet the fabrication requirements. Consequently, the potential of wet etching as an alternative method for SiO_2 removal was investigated. Wet etching utilised a 1:10 HF

$_2$O solution for SiO_2 dissolution.

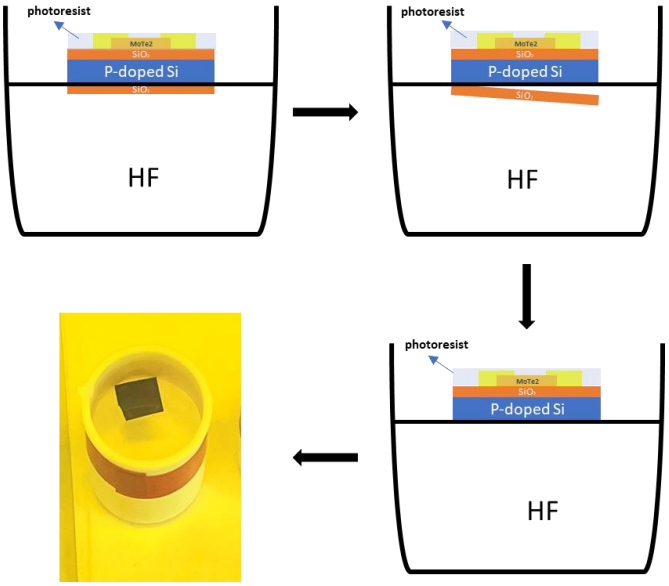


Figure 5.25 Diagram of HF solution remover backside SiO_2

It is important to note that the 100 nm top SiO_2 layer is essential as a gate dielectric between the silicon wafer and the $MoTe_2$ film on the wafer surface. One drawback of wet etching is its anisotropic nature, which limits control over the etching direction. Immersing the entire sample in hydrofluoric acid (HF) is not feasible since the upper 3D structure (SiO_2, ohmic contacts, and $MoTe_2$ film) must be protected. To address this, a photoresist layer was applied to safeguard the upper structure. The flotation and surface tension of the solution ensured that only the backside of the substrate made contact with the HF solution. Figure 5.25 illustrates the experimental setup for removing SiO_2 from the substrate's backside using the HF solution. In this process, a 1:10 HF:O $_2$ solution dissolves SiO_2 at a rate of 50 nm/min, allowing for the complete removal of the 100 nm SiO_2 layer in approximately 4 minutes.

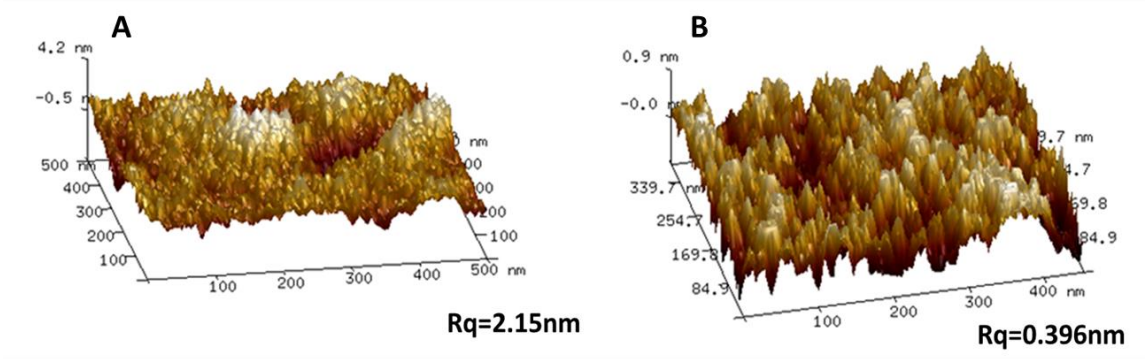


Figure 5.26 AFM for the back side of substrate after (A) Dry etch and (B) wet etching.

The effectiveness of the two methods was further assessed by comparing the surface roughness of the substrate's backside after dry and wet etching. As shown in the AFM scans in Figure 5.26, wet etching resulted in a significantly smoother surface, making it a more suitable option for preparing the back gate electrode.

5.5.2 Back-gate Contract Preparation

After the removal of SiO_2, a contact metal was uniformly deposited across the entire backside of the substrate. Since the device employs a global back gate electrode, no further patterning or photolithography is required. Direct metallisation, consisting of a 20 nm Ti/80 nm Au layer, was applied, followed by the use of silver conductive adhesive (Ag DAG) to bond the metallised surface to a copper substrate, creating a stable platform for probe testing. Ag DAG, a silver pastes commonly used in electronic applications, provides strong adhesion between the sample surface and the copper foil. Figure 5.27 illustrates the complete setup of the device.

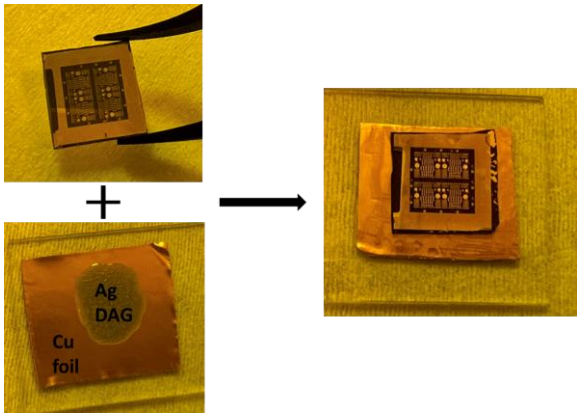


Figure 5.27 The diagram of $MoTe_2$ FET back contact with Cu foil via Ag DAG

5.6 Back gate 2H-$MoTe_2$ FET Fabrication Process Flow Optimises

Sections 5.3, 5.4, and 5.5 describe the three primary stages of the FET fabrication process: the definition and production of the $MoTe_2$ film, the definition of the ohmic contact metal, and the formation of the back gate. The sequence of these fabrication steps was carefully planned, considering the potential impact of the Mo-to-$MoTe_2$ CVD process and the thermal processing involved in both the top ohmic contacts and the backside gate contact.

A strategy was developed to optimise the preparation of the back gate contact. This included covering the back gate with a protective layer of photoresist, as well as applying photoresist and metallisation during the preparation of the upper structure. Initially, the back gate was formed before the CVD process, with the aim of assessing whether the temperature used during CVD could also serve to anneal the back contact metal, allowing it to alloy with the silicon substrate during the $MoTe_2$ film definition stage. However, testing revealed that the 20 nm Ti/80 nm Au back gate metallisation could not withstand the CVD process temperature of 650°C, as shown in Figure 5.28.

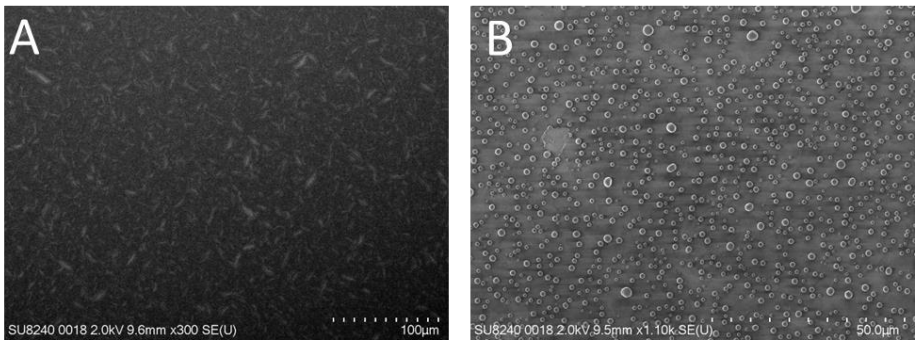


Figure 5.28 SEM image for the Ti/Au back gate metal after experiencing the CVD process.

As a result, an alternative approach was considered, in which the back gate was formed and annealed after the surface ohmic contacts were established. The optimized and detailed fabrication steps for this improved process are illustrated in Figure 5.29.

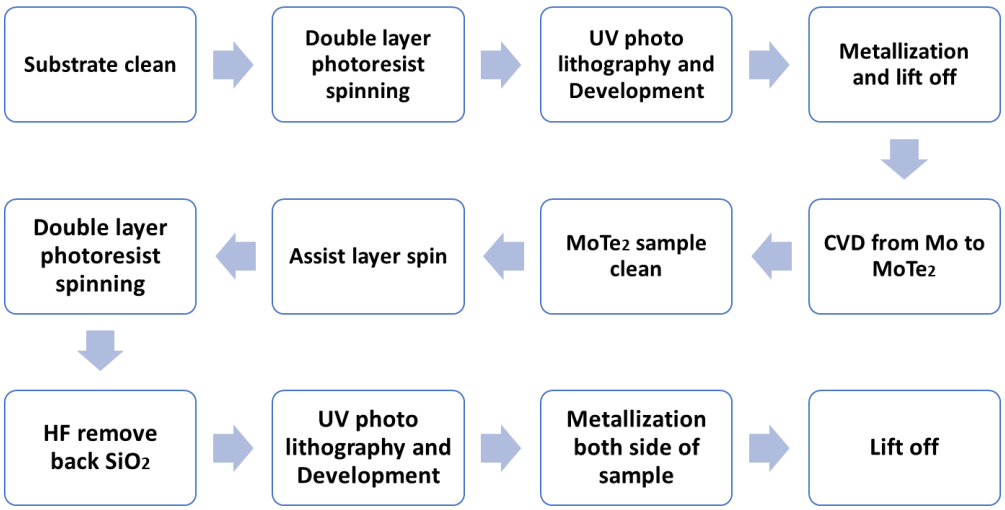


Figure 5.29 Optimized back gate $MoTe_2$ FET down to up fabrication process

5.7 Summary

This chapter focuses on the fabrication of FETs by integrating conventional photolithography technology with the novel CVD method for $MoTe_2$ introduced in Chapter 4. Through the optimisation of the photolithography process, a bottom-up $MoTe_2$ FET fabrication method has been developed by combining these two techniques. Key elements of this approach include controlling film characteristics, the CVD synthesis of $MoTe_2$, defining contact metals, and constructing the back gate electrode.

The core of the process lies in the integration of multiple transistor production techniques, such as surface treatment, physical vapour deposition (PVD), photolithography (including photoresist coating, spinning, exposure, and development), and both wet and dry etching. Throughout the fabrication process, several analytical techniques, including SEM, AFM, optical microscopy, and Raman spectroscopy, were employed to monitor the film and device conditions.

This chapter provides a concise overview of the methodologies and processes for integrating two-dimensional materials with photolithography. It outlines photolithography preparation recipes specifically designed for thin-film FETs and discusses strategies for their optimisation. This approach offers significant potential for advancing controllable fabrication procedures for various CVD-produced two-dimensional material FETs in the future.

5.8 Reference:

1. Kim, D. M., Kim, S., & Kim, T. (2021). Accurate Analysis of Schottky Barrier Height in Au/2H–MoTe2 Atomically Thin Film Contact. *Electronic Materials Letters*, *17*(4), 307–314. https://doi.org/10.1007/s13391-021-00284-x

2. Mitta, S. B., Choi, M. S., Nipane, A., Ali, F., Kim, C., Teherani, J. T., Hone, J., & Yoo, W. J. (2020). Electrical characterization of 2D materials-based field-effect transistors. *2D Materials*, *8*(1), 012002. https://doi.org/10.1088/2053-1583/abc187

3. Larson, J. M., & Snyder, J. P. (2006). Overview and status of metal S/D Schottky-barrier MOSFET technology. *IEEE Transactions on Electron Devices*, *53*(5), 1048–1058. https://doi.org/10.1109/TED.2006.871842

4. Buitrago, E., Fernández-Bolaños, M., & Ionescu, A. M. (2012). Vertically stacked Si nanostructures for biosensing applications. *Microelectronic Engineering*, *97*, 345–348. https://doi.org/10.1016/j.mee.2012.03.017

5. Berkowski, K. L., Plunkett, K. N., Yu, Q., & Moore, J. S. (2005). Introduction to Photolithography: Preparation of Microscale Polymer Silhouettes. *Journal of Chemical Education*, *82*(9), 1365. https://doi.org/10.1021/ed082p1365

6. Fraser, J. P., Masaityte, L., Zhang, J., Laing, S., Moreno-López, J. C., McKenzie, A. F., McGlynn, J. C., Panchal, V., Graham, D., Kazakova, O., Pichler, T., MacLaren, D. A., Moran, D. A. J., & Ganin, A. Y. (2020). Selective phase growth and precise-layer control in MoTe2. *Communications Materials*, *1*(1), Article 1. https://doi.org/10.1038/s43246-020-00048-4

7. Gao, F., Yang, H., & Hu, P. (2018). Interfacial Engineering for Fabricating High-Performance Field-Effect Transistors Based on 2D Materials. *Small Methods*, *2*(6), 1700384. https://doi.org/10.1002/smtd.201700384

8. Zhang, K., Bao, C., Gu, Q., Ren, X., Zhang, H., Deng, K., Wu, Y., Li, Y., Feng, J., & Zhou, S. (2016). Raman signatures of inversion symmetry breaking and structural phase transition in type-II Weyl semimetal MoTe2. *Nature Communications*, *7*(1), Article 1. https://doi.org/10.1038/ncomms13552

6.0 Contact Metal Study of MoTe2 Field Effect Transistor

It is important to acknowledge the inherent sensitivity of 2D materials to environmental factors[1], which can significantly impact device reliability and performance. Contaminants such as organic residues from the fabrication process and chemi-sorbates from the ambient environment[2], as well as exposure to atmospheric oxygen and moisture[3], can degrade the material's electronic properties over time. These factors contribute to increased contact resistance at the metal-semiconductor interface, reduced carrier mobility due to scattering mechanisms[4], and threshold voltage shifts that affect the transistor's switching characteristics[5]. Additionally, issues in metal contact deposition, such as poor adhesion or non-uniform coverage, further exacerbate contact resistance and hinder current injection from the metal into the semiconductor[3].

The high surface-area-to-volume ratio of 2D materials amplifies these issues, making the devices highly susceptible to surface contamination and degradation, which can introduce variability and reliability concerns. This presents significant challenges for process integration, particularly when attempting to scale beyond laboratory settings. Exfoliated materials are especially vulnerable to environmental degradation, as the absence of encapsulation leaves the surface exposed to air, resulting in oxidation and other degradation mechanisms. These challenges make it difficult to fabricate back-gated, top-contact FET structures with consistent performance under ambient conditions[6].

Therefore, stable encapsulation and packaging technologies, such as the use of passivation layers or protective coatings, are crucial to mitigate these degradation

pathways and ensure reliable, long-term device operation. In this study, we focus on FETs fabricated using CVD of $MoTe_2$, a TMDC with a tunable bandgap, which holds promise for large-scale integration. Specifically, we examine the effects of various contact metals, such as gold, titanium, and palladium, on the metal-semiconductor interface, as well as the influence of different substrate dielectric environments, including SiO_2 and high-k dielectrics, on device performance metrics like mobility, SS, and contact resistance.

`6.1 Introduction

The fabrication and characterisation of back-gated $MoTe_2$ FETs with controlled $MoTe_2$ layers represent a significant advancement in two-dimensional (2D) semiconductor technology. These devices are highly sensitive to various factors, including substrate effects, Schottky barrier heights, and dielectric environmental conditions, all of which can impact device performance. To address these challenges, innovative chemical vapour deposition (CVD) techniques for synthesising $MoTe_2$, combined with optimised fabrication processes, have been introduced, as detailed in Chapters 4 and 5.

Understanding the structure and electrical properties of $MoTe_2$ FETs is essential for validating the use of CVD-grown $MoTe_2$ in electronic applications, particularly in terms of device polarity and mobility. The polarity and mobility of each device are assessed by analysing their output and transfer characteristics. Devices that exhibit an increase in current under negative reverse bias are classified as p-doped, signifying hole conduction, while those demonstrating increased current under positive reverse bias are categorised as n-doped, indicative of electron conduction. Some devices display bipolar behaviour, with both electrons and holes contributing to conduction under different bias conditions. This classification provides insight into the doping

characteristics of the $MoTe_2$ films, and the nature of the contacts formed between the metal and the 2D material.

The structure of the back-gated $MoTe_2$ FET is illustrated in Figure 6.1(A). The CVD-grown $MoTe_2$ is deposited onto a SiO_2/Si substrate, with precise positioning of the $MoTe_2$ film. Two different ohmic contact metal strategies, Ti (20 nm)/Au (80 nm) and Pd (20 nm)/Au (80 nm), are applied directly onto the structured $MoTe_2$ film to explore their effects on device performance. Electrical measurements, conducted at room temperature, were performed using a Summit 12k automatic probe station in direct current (DC) mode. These measurements, illustrated in Figure 6.1(B), provide critical data on the electrical performance of the devices, including output and transfer characteristics. The study focuses on the impact of the different contact metals on the device's overall performance, with particular emphasis on the Schottky barrier formed between the contact metals and $MoTe_2$.

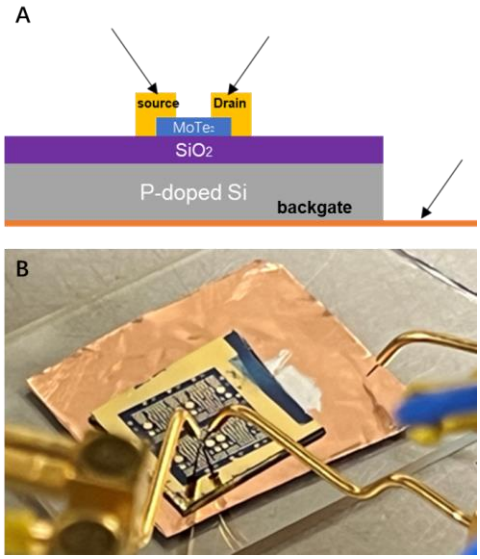


Figure 6.1 (A) Schematic diagram of back-gated $MoTe_2$ FET cross section and (B) The picture of the FET measurement with probes.

The choice of contact metal is a key parameter in optimising the performance of $MoTe_2$ FETs. The use of titanium (Ti) and palladium (Pd), with their differing work functions, allows for an investigation into how metal-$MoTe_2$ interfaces impact the formation of ohmic versus Schottky contacts. This distinction significantly influences the contact resistance, which is a crucial factor in determining the overall efficiency of the 2D FETs. By comparing the two contact metal strategies, the study aims to optimise the metal-$MoTe_2$ interface, reduce contact resistance, and improve device performance. The findings presented in this chapter provide valuable insights into the electrical behaviour, polarity, and contact engineering necessary for advancing the practical application of $MoTe_2$ FETs in 2D nanoelectronics.

This chapter examines the influence of various contact metals and dielectric environments on the output and transfer characteristics of back-gated $MoTe_2$ FETs. To quantify the contact resistance between the ohmic metal and $MoTe_2$, the transfer length method (TLM) is utilised. The electrical performance of the FETs is compared under two distinct ohmic contact metal configurations. Each FET in this study is fabricated with a channel width of 50 μm. The $MoTe_2$ layer is synthesised from a 5 nm Mo film, yielding approximately eight layers of $MoTe_2$ via CVD. The source-to-drain contact distance ranges from 1 μm to 6 μm, with 1 μm increments.

6.2 TLM Measurement and Contact Resistance ($R_{contact}$) of $MoTe_2$ FET

TMDCs semiconductors have emerged as promising candidates for post-silicon nanoelectronics, primarily due to their atomic-scale thickness and intrinsic non-zero band gaps. In 2D short-channel electronic devices, contact resistance becomes a critical limiting factor in scaling down integrated circuits. Planar metal contacts on vdW semiconductors often suffer from unpredictably high contact resistances between the

metal and the TMDC, hindering device performance. Among TMDC materials, 2H-$MoTe_2$ is notable for its band gap in the range of 1–2 eV, which is comparable to that of silicon[7]. However, its application in 2D electronic devices is challenged by environmental instability and high contact resistance. Additionally, intrinsic $MoTe_2$ transistors exhibit ambipolar transfer characteristics, suggesting that the FLP effect at the metal-$MoTe_2$ interface is relatively weak compared to sulphur-terminated TMDCs like MoS_2[8].

This section investigates contact resistance in $MoTe_2$ FET devices by evaluating two different metal contact configurations: Ti/Au and Pd/Au. Titanium (Ti), with a work function of 4.3 eV, is lower than that of $MoTe_2$ (4.6 eV, as referenced in[7]), resulting in higher Schottky barrier heights and p-type behaviour in the resulting contacts. The primary objective of this work is to optimise the metal-$MoTe_2$ interface to minimise contact resistance and thereby enhance device performance.

Contact resistance is extracted using transfer length method (TLM) plots, and the performance of FETs with different contact metals is compared. All devices are fabricated on 100 nm SiO_2/p-doped (<0.005 Ω·cm) silicon substrates to enable consistent performance evaluation. CVD-grown $MoTe_2$, approximately eight layers thick, is transferred onto the substrates using photolithography, followed by the deposition of the metal contacts—either Ti (20 nm)/Au (80 nm) or Pd (20 nm)/Au (80 nm)—which are also defined through photolithography. Figure 6.2(A) presents a cross-sectional schematic of two typical devices: Type I, featuring Ti/Au contacts on 2H-$MoTe_2$, and Type II, featuring Pd/Au contacts. The electrical performance of both device types is compared in Figure 6.2(B).

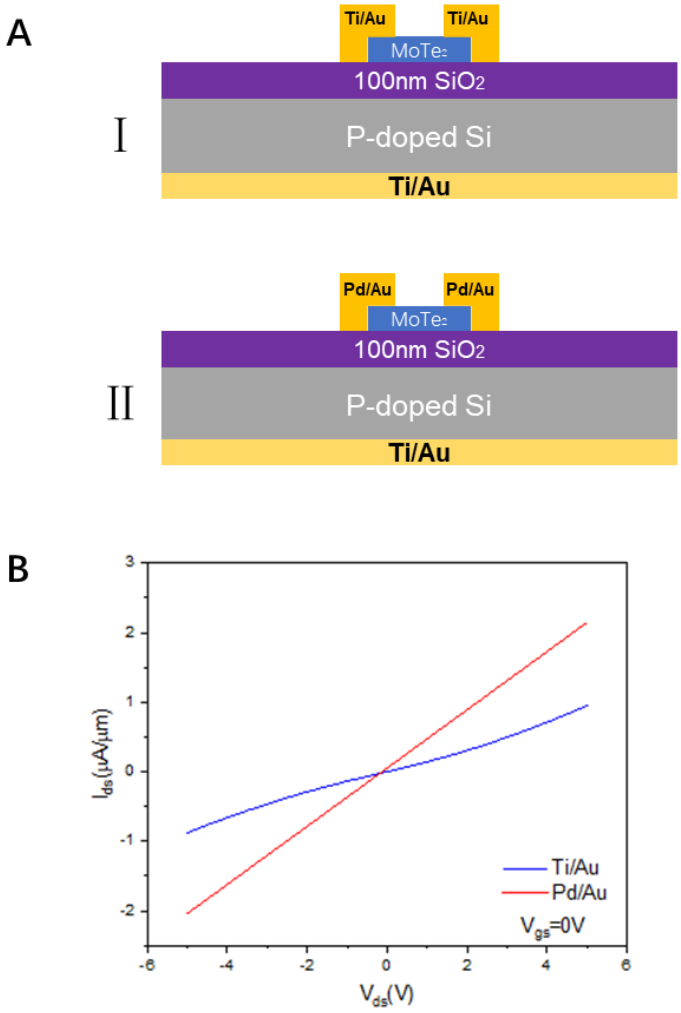


Figure 6.2 (A) schematic of back-gate $MoTe_2$ FET with different contact metal and (B) I-V curves measured from TLM with 2μm gap between source/drain of two type devices under 0 backgate bias.

The graph in Figure 6.2(B) clearly illustrates that the only variable differing between Type I and Type II devices is the contact metal. Both curves represent FET structures with a channel width of 50 µm and a channel length of 2 µm between the source and drain. The I-V curve for Type I (blue line) demonstrates a pronounced nonlinear relationship between I_{DS} and V_{DS} . In contrast, the I-V curve for Type II (red line) exhibits a linear relationship.

Notably, the Type II device achieves a significantly higher ON current, approximately double that of Type I under the same V_{DS}. The maximum currents measured are 2.2 μA/μm for Type II and 0.9 μA/μm for Type I, both at zero applied gate bias. This discrepancy suggests that Type I devices experience higher contact resistance ($R_{contact}$) which impedes efficient charge carrier transport. To quantify $R_{contact}$, TLM structures were fabricated on back-gated $MoTe_2$ FETs[8].

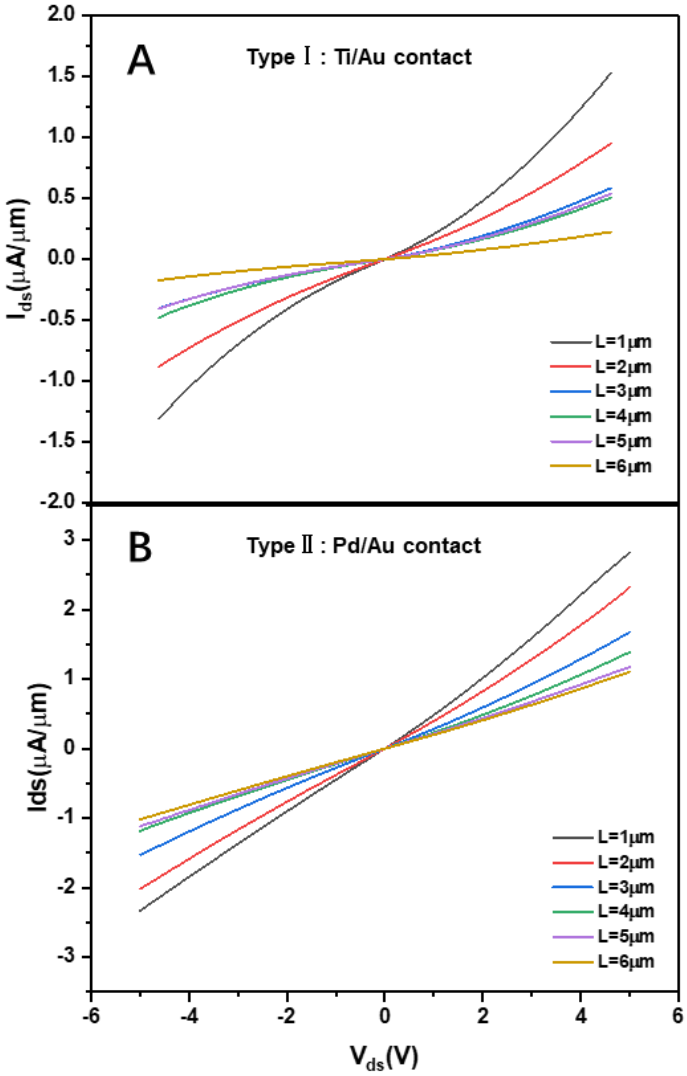


Figure 6.3 The I-V curve of $MoTe_2$ devices with different channel widths with (A) Ti/Au contact and (B) Pd/Au contact under zero backgate bias.

Figure 6.3 displays representative I-V measurements for both Type I (Ti/Au) and Type II (Pd/Au) devices, with channel lengths varying from 1 μm to 6 μm and a fixed channel width of 50 μm. In Figure 6.3(A), Ti/Au contact devices exhibit a nonlinear increase in output current as a function of the applied source-drain voltage. In contrast, Figure 6.3(B) shows a linear increase in output current for Pd/Au contact devices under the same conditions. These findings align with the trends observed in Figure 6.2 and support the hypothesis that Pd/Au forms superior ohmic contacts with $MoTe_2$, while Ti/Au contacts behave more like nonlinear Schottky contacts, characterized by higher contact resistance.

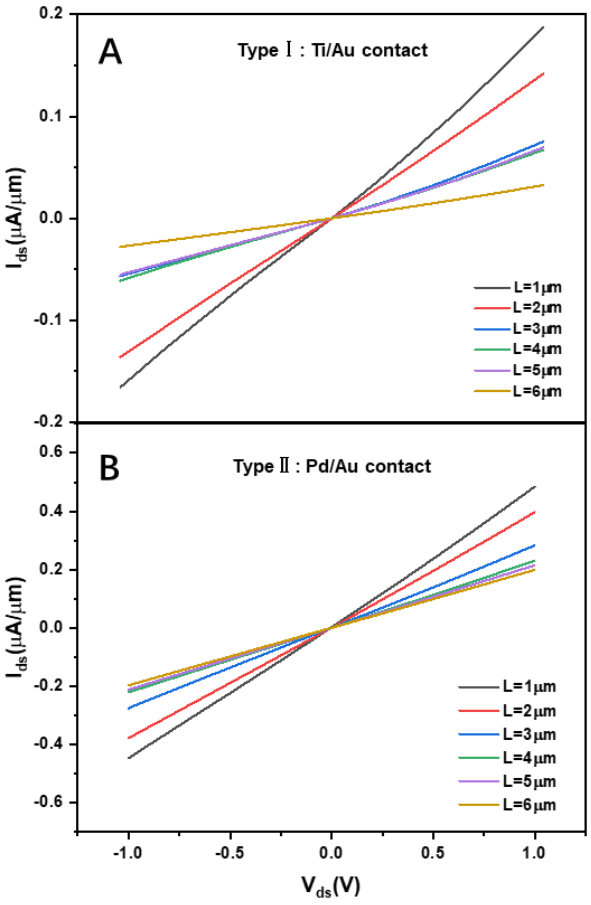


Figure 6.4 The I-V curve from -1V to 1V of $MoTe_2$ devices with different channel widths with (A) Ti/Au contact and (B) Pd/Au contact.

Furthermore, Ti/Au contact devices with channel lengths of 3 μm, 4 μm, and 5 μm exhibit remarkably similar behaviour. This uniformity may be attributed to the polycrystalline nature of the $MoTe_2$ material or fabrication-related factors, such as Ti evaporation, which could introduce surface roughness or other defects in the metal layer, leading to increased contact resistance.

To minimize errors in the TLM plot and calculations, it is essential to focus on the linear region of the I-V curve. Therefore, total resistance (R_{total}) was extracted from the VDS range of -1 V to 1 V, where the data exhibits more linear behaviour, as shown in Figure 6.4. Within this range, both Ti/Au and Pd/Au devices show a nearly linear relationship between I_{DS} and V_{DS}, with differences in current attributed to the varying contact resistance at the two metal interfaces.

According to TLM and Ohm's law, the total resistance (R_{total}) is derived from the slope of the I-V curve. However, the nonlinear behaviour observed over the broader bias range of -5 V to 5 V complicates the generation of an accurate TLM plot. This deviation from linearity indicates difficulties in precisely extracting contact resistance, as the expected linear relationship between current and voltage necessary for straightforward TLM analysis is not maintained. Figure 6.5 presents the total resistance (R_{total}) values extracted from the I-V characteristics of Ti/Au and Pd/Au devices within the -1 V to 1 V range, as shown in Figures 6.4(A) and 6.4(B).

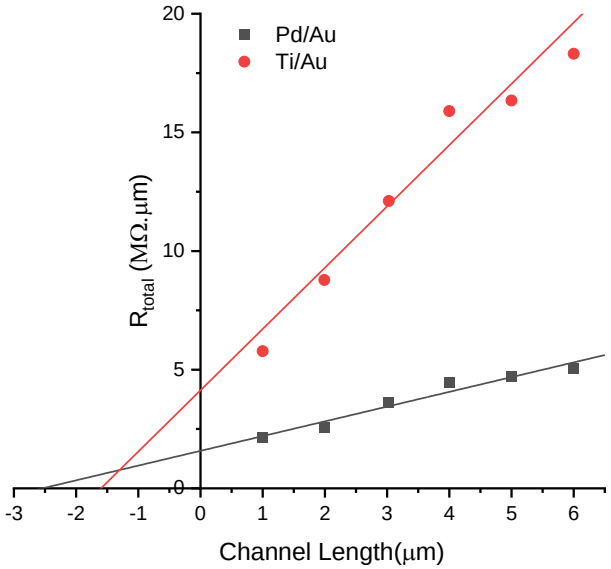


Figure 6.5 The TLM Plotted the R_{total} versus channel length(L) for $MoTe_2$ FET with Pd/Au and Ti/Au contact.

As expected, R_{total} increases with channel length for both device types, confirming the expected scaling behavior of resistance with channel length. The difference in resistance between the Ti/Au and Pd/Au contacts further emphasizes the higher contact resistance associated with Ti/Au interfaces compared to Pd/Au. By combining the TLM equation (Equation 6.1) with the extracted resistance values, the contact resistance for both device types were determined:

$$\boldsymbol{R_{total} = 2R_{contact} + R_{sheet}\frac{L}{W}} \qquad \boldsymbol{equation\ (6.1)}$$

According to the TLM equation, the y-axis intercept ($2R_{contact}$) represents the contact resistance, while the x-axis intercept corresponds to $2L_T$, the transfer length. The fitting lines for Pd/Au (black) and Ti/Au (red) in Figure 6.6 demonstrates distinct differences. The Pd/Au device exhibits a lower y-axis intercept, indicating significantly lower

contact resistance compared to the Ti/Au device. This observation suggests a higher Schottky barrier at the Ti/Au-$MoTe_2$ interface, which contributes to the increased contact resistance observed for the Ti/Au configuration.

These results align with the principles of contact engineering discussed in Chapter 2, where it was established that contact resistance ($R_{contact}$) decreases as the work function of the contact metal increases. $MoTe_2$ typically forms p-type FETs, and since Ti has a lower work function (4.3 eV) compared to Pd (5.6 eV), the contact resistance for Ti/Au is expected to be higher. The extracted parameters shown in Figure 6.6 confirm this trend. The Pd/Au device exhibits a contact resistance of 0.79 MΩ·μm, representing a three-fold reduction compared to the contact resistance of the Ti/Au device, which is 2.06 MΩ·μm. This significant improvement underscores the critical role of selecting appropriate contact metals to optimize the performance of $MoTe_2$-based FETs.

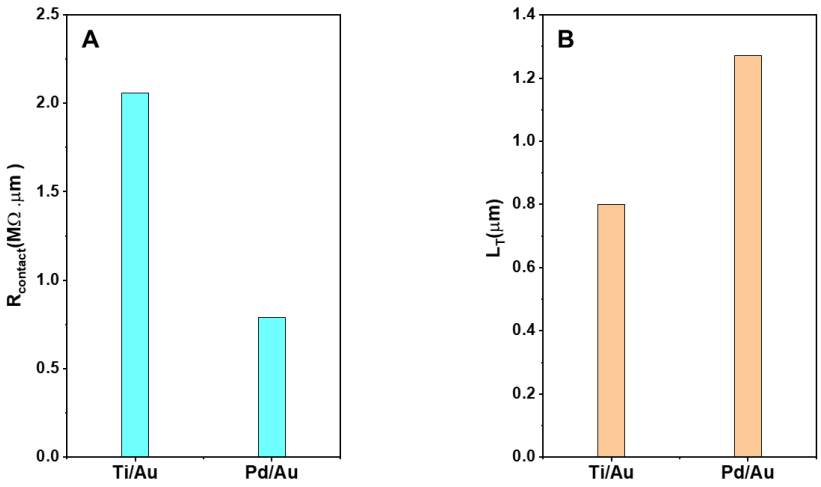


Figure 6.6 The (A) contact resistance ($R_{contact}$), and (B) Transfer Length (L_T) of type Ⅰ and Ⅱ devices extracts from the TLM plot and equation 6.1.

In summary, the Type I device with Ti/Au contacts exhibited significantly higher contact resistance compared to the Type II device with Pd/Au contacts, which successfully formed ohmic contacts with $MoTe_2$. While the experiments clearly demonstrated differences in contact resistance between these two metal interfaces, further studies, particularly involving temperature-dependent measurements, are necessary to accurately determine the Schottky barrier height. This information could provide deeper insights into contact behavior and pave the way for improved device design and performance.

As anticipated, the width-normalized contact resistance for Pd/Au remained consistently lower than that of Ti/Au, reinforcing its effectiveness in reducing contact resistance. However, variations in the extracted transfer length are likely attributed to the polycrystalline nature of the CVD-grown $MoTe_2$, which introduces structural inconsistencies across different regions of the material. This suggests that further investigations into material uniformity could provide valuable insights for enhancing device reproducibility.

Interestingly, despite the variations in sheet resistance observed in the TLM plot, it is well established that sheet resistance should not directly influence contact resistance. This discrepancy indicates the need for further exploration of material-specific properties or potential fabrication inconsistencies that may contribute to the observed differences in sheet resistance between the samples.

Ultimately, the system developed for fabricating $MoTe_2$ FETs with different contact metals has demonstrated significant potential for reducing contact resistance, thereby improving device performance. The versatility of this approach extends beyond $MoTe_2$

to other two-dimensional materials with varying band structures, broadening its potential applications in the development of next-generation nanoelectronics.

6.3 $MoTe_2$ FET Electrical Result with Pd/Au and Ti/Au Contact

The transfer and output characteristics of a field-effect transistor (FET) are critical for evaluating its performance, providing essential insights into parameters such as carrier mobility, threshold voltage, and the on/off current ratio. In the case of two-dimensional materials like $MoTe_2$, high contact resistance between the metal contacts and the semiconductor can significantly impair the overall functionality of the FET. Therefore, understanding the transfer characteristics is essential for assessing and enhancing device performance.

Figure 6.7 presents the transfer characteristics of $MoTe_2$ FETs with Ti/Au and Pd/Au contacts, measured at room temperature (RT) with a channel length of 2 μm. The graph illustrates the variation in drain-source current (I_{DS}) as a function of gate-source voltage (V_{GS}) over a range from -60 V to 60 V, with the drain-source voltage (V_{DS}) varying from 0.1 V to 0.9 V in 0.1 V increments. To ensure that the devices remain in the linear operating region and avoid nonlinear behaviour or high-field effects, a narrow V_{DS} range was selected for the transfer characteristic measurements. This approach simplifies data interpretation and provides a clearer understanding of the device's intrinsic properties, including mobility, threshold voltage, and the dominant type of conduction (p-type or n-type behaviour).

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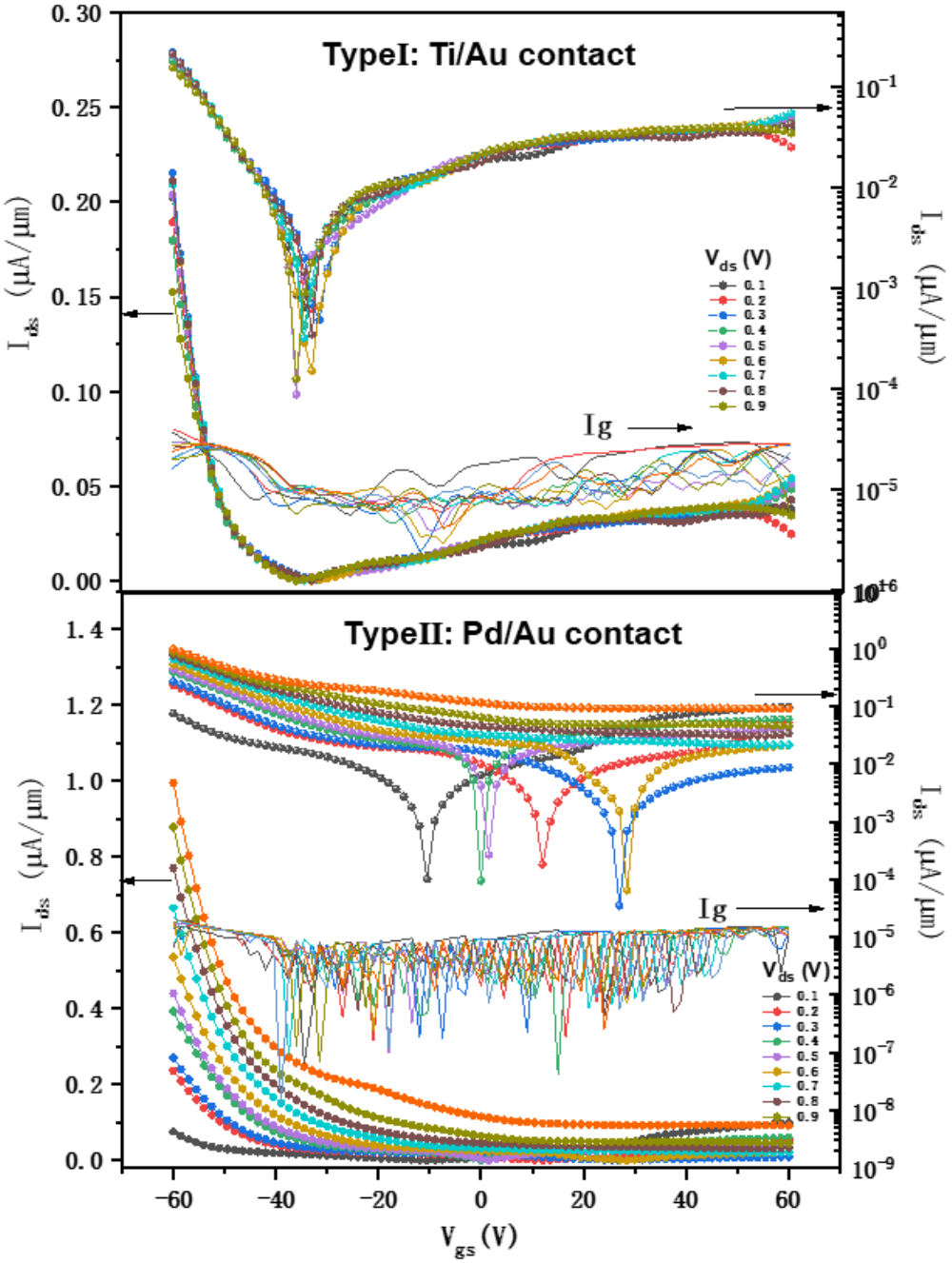

Figure 6.7 Transfer characteristic with Drain-to-Source excitation voltage V_{ds} of 0.1 to 0.9V in linear and logarithmic scale (A) Ti/Au-and (B) Pd/Au-contact $MoTe_2$ FETs with L=2μm.

In the analysis of the p-type $MoTe_2$ FET, the transfer characteristics exhibit a significant increase in drain-source current (I_{DS}) once the gate-source voltage (V_{GS}) surpasses

the threshold voltage (V_{Th}). Prior to reaching V_{Th}, IDS remains minimal as the channel is not fully formed, and the gate current (I_G) is negligible due to the insulating behaviour of the gate dielectric. After V_{Th}, the channel begins to form, facilitating a rapid rise in IDS as more holes are injected into the conductive channel. Concurrently, a noticeable increase in I_G is observed, attributed to the stronger electric field across the gate dielectric. This increase in gate leakage current may be caused by mechanisms such as Fowler-Nordheim tunnelling or trap-assisted tunnelling, particularly in regions where the dielectric may have imperfections. However, I_G remains much smaller than I_{DS}, indicating that while there is some leakage, the gate dielectric still provides effective insulation. The dominant I_{DS}, which is orders of magnitude higher than I_G, confirms that the primary current flow through the source-drain channel is functioning as expected. Although the increasing gate leakage current does not significantly impair device performance at this stage, monitoring I_G is crucial, as a more pronounced increase could indicate potential degradation of the gate dielectric over time, adversely affecting long-term device stability and performance.

The comparison of transfer characteristics between Ti/Au and Pd/Au contacts highlights the significant impact of contact metal choice on FET performance. Devices with Pd/Au contacts, which form superior ohmic interfaces with $MoTe_2$, demonstrate higher I_{DS} across the V_{GS} range compared to those with Ti/Au contacts, which suffer from higher contact resistance, leading to reduced drain currents. This comparison underscores the critical role of contact engineering in optimizing the performance of FETs based on 2D materials like $MoTe_2$.

In $MoTe_2$-based FETs, the switching mechanism is governed by the modulation of channel conductivity through V_{GS}. In these p-type devices, applying a negative V_{GS}

induces the accumulation of holes (positive charge carriers) in the channel, forming a conductive pathway between the source and drain. This gate-induced control of carrier concentration transitions the device from the "off" state, where the channel is depleted of carriers, to the "on" state, where the channel is sufficiently populated with holes to support significant I_{DS}. The transfer characteristics (Figure 6.7) reveal a proportional increase in I_{DS} with more negative V_{GS}, indicating efficient switching. This clear modulation of channel conductivity with respect to V_{GS} reinforces the gate's crucial role in controlling the device's operational state.

A key parameter in evaluating these devices is the behaviour of the gate leakage current (I_{GS}), which remains negligibly small, in the picoampere (pA) range, as the device transitions from the off-state to the on-state. Before reaching VTh, the leakage current is minimal, effectively excluding it as a limiting factor in off-state performance. After exceeding V_{Th}, while the device enters the on-state with a marked increase in IDS, the associated rise in leakage current remains modest and within acceptable operational parameters. This increase is primarily due to the enhanced gate-induced conduction in the channel, rather than parasitic effects or material defects. The low leakage current ensures that off-state leakage does not degrade the on-off current ratio, nor does it contribute to excessive power dissipation, confirming that the device maintains high switching efficiency.

The type of metal contacts used significantly influences device performance, particularly the on current (I_{ON}). Pd/Au contacts, which form ohmic interfaces with $MoTe_2$, facilitate efficient hole injection due to the favourable alignment of the metal work function with $MoTe_2$'s valence band maximum. This alignment leads to a lower Schottky barrier height, reduced contact resistance, and consequently, higher I_{ON},

enhancing the efficiency of the switching process. In contrast, devices with Ti/Au contacts, which exhibit Schottky-like behaviour, experience higher contact resistance and reduced I_{ON}, although they still maintain low leakage current. The consistently low leakage observed with both contact types further supports the conclusion that the performance of these devices is not compromised by leakage mechanisms.

Despite the slight increase in leakage current after the device transitions into the on-state, this behaviour is typical of FETs and does not significantly impair performance. In $MoTe_2$-based FETs, I_{GS} remains in the picoampere range, much lower than IDS during operation, allowing the device to maintain a high on-off current ratio. This ensures efficient switching with minimal power losses attributable to leakage. Excessive off-state leakage could degrade device performance and increase power consumption, but the low observed leakage confirms that gate modulation of the channel is not hindered by parasitic leakage. The switching mechanism is primarily driven by the gate's ability to control carrier concentration in the channel.

For p-type operation, a negative V_{GS} induces hole accumulation at the $MoTe_2$ surface, enhancing channel conductivity. Devices with Pd/Au contacts benefit from reduced contact resistance, owing to the formation of ohmic contacts, ensuring minimal contact-related limitations during switching. The lack of current saturation observed in the transfer curves suggests that short-channel effects (SCEs), such as drain-induced barrier lowering (DIBL), rather than leakage currents, are more likely to influence device performance. These effects, along with threshold voltage roll-off, reduce gate control at higher V_{DS}, leading to premature current rise, but are unrelated to leakage.

Defects introduced during fabrication, such as those from photolithography and metal deposition, could create trap states in the $MoTe_2$ channel, which might potentially

increase leakage by capturing and releasing charge carriers. However, the consistently low leakage current, even in the presence of such defects, indicates that device performance is not significantly compromised by these traps. Moreover, while defects at the metal-semiconductor interface could potentially induce electron injection, the observed leakage remains too small to affect device operation, further confirming that leakage does not dominate the switching behaviour.

Thus, the performance of $MoTe_2$-based FETs is not impaired by leakage currents. Leakage remains minimal across the operating voltage range, ensuring high on-off current ratios and efficient switching. The slight increase in leakage after V_{Th} is part of the normal FET switching process and is not attributable to parasitic effects or defects. Instead, the switching performance is primarily dictated by gate modulation of the channel, with the choice of metal contacts (Pd/Au or Ti/Au) playing a critical role in determining contact resistance and I_{ON}. The low leakage current supports the conclusion that these devices exhibit robust performance, with leakage currents too small to interfere with switching efficiency or overall device operation. Consequently, the $MoTe_2$ FETs demonstrate reliable and efficient operation, unaffected by performance degradation due to leakage currents.

The results presented in Section 6.2 focus on contact resistance measurements using the TLM structure for different contact metals. Figures 6.8 (A) and (B) illustrate the output characteristics, normalized by channel width, for $MoTe_2$ FETs with a 2 μm source-drain gap at various gate biases for devices with Ti/Au and Pd/Au contacts, respectively.

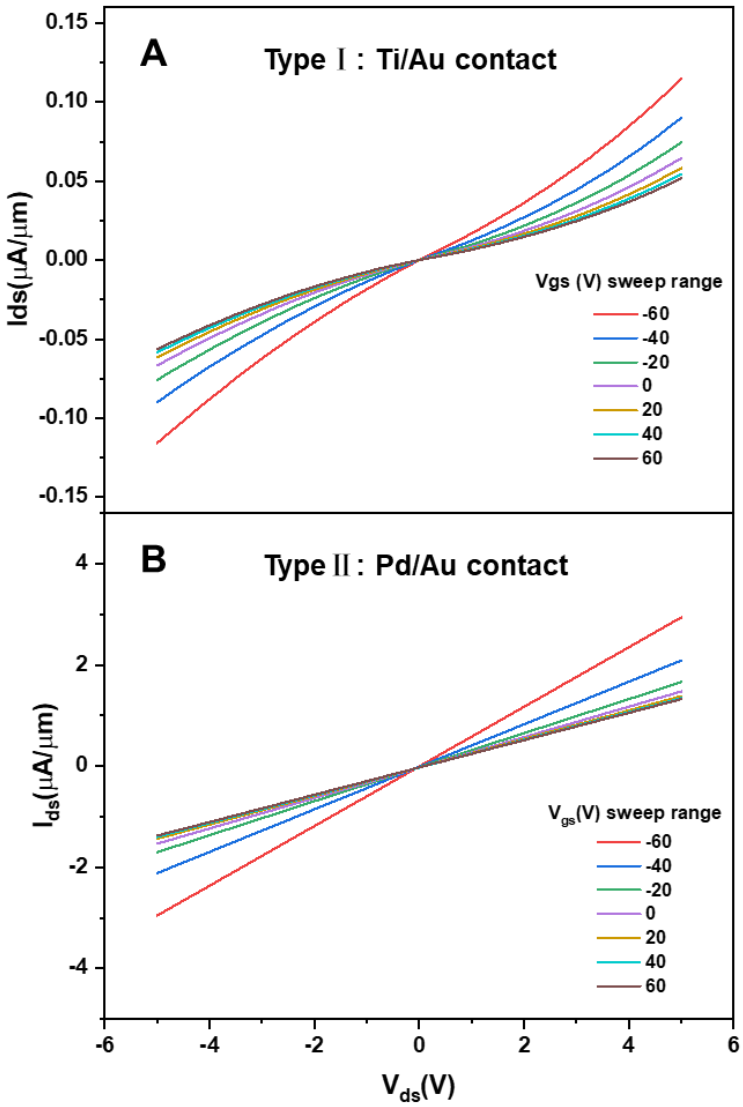

Figure 6.8 The output characteristic of 2μm $MoTe_2$ FET with (A) Ti/Au-contact and (B) Pd/Au-contact with different V_{gs} range from -60V to 60V with step 20V.

For Type I devices featuring Ti/Au contacts, the output curves exhibit non-linear behaviour, indicating that the Ti/Au-$MoTe_2$ interface forms a higher Schottky barrier for electron injection. At a back gate voltage (V_{BG}) of -60 V, the on-current (I_{ON}) is approximately 0.13 μA/μm, which is significantly lower than the 3 μA/μm observed for devices with Pd/Au contacts. This difference is primarily attributed to the variations in Schottky barrier heights between the two contact metals, with Pd/Au providing a more

favourable alignment for hole injection, resulting in lower contact resistance. Additionally, the room-temperature I_{DS} versus V_{DS} characteristics for Pd/Au contact devices demonstrate linear behaviour across various gate voltages. This linearity confirms the formation of ohmic contacts between Pd/Au and 2H-$MoTe_2$. In contrast, the non-linear characteristics observed in the Ti/Au devices emphasize the substantial differences in contact behaviour between the two metal types.

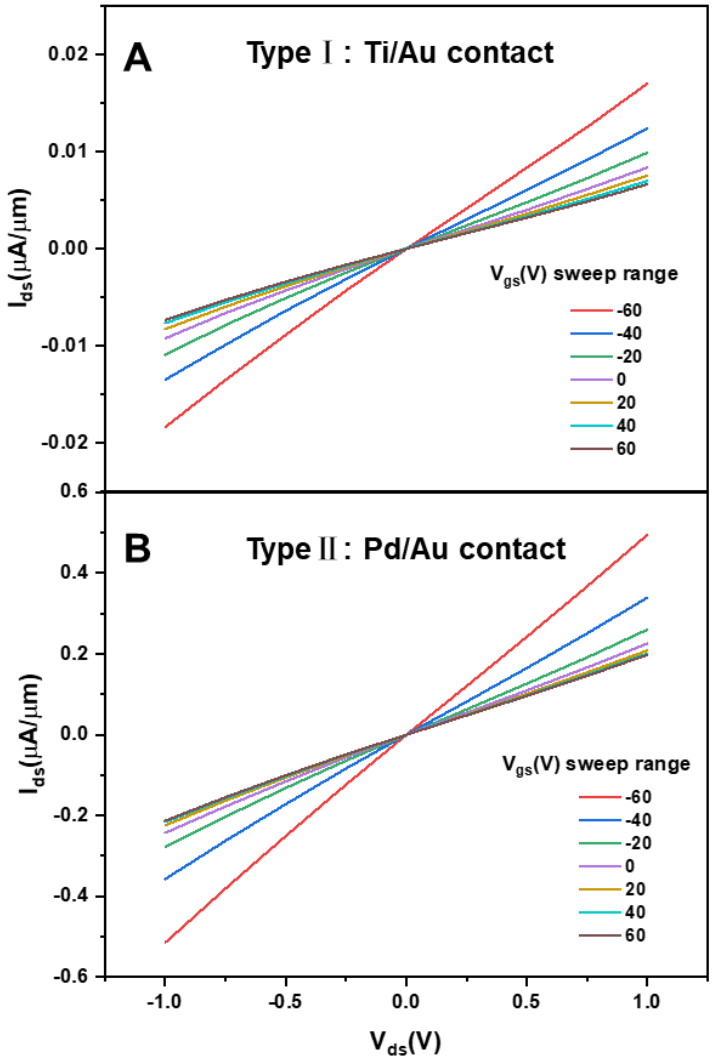

Figure 6.9 The output characteristic (from -1V to 1V) of 2μm $MoTe_2$ FET with (A) Ti/Au-contact and (B) Pd/Au-contact with different V_{gs} range from -60V to 60V with step 20V.

Both Type I (Ti/Au) and Type II (Pd/Au) devices exhibit a clear increase in on-current (I_{ON}) with more negative back-gate voltage (V_{BG}) sweeps, reinforcing their predominantly p-type behaviour. This trend is consistent with the transfer characteristics, where negative gate voltages enhance hole conduction, supporting the p-type operation of $MoTe_2$-based FETs. As VBG becomes more negative, the accumulation of holes at the $MoTe_2$ channel increases, resulting in improved channel conductivity and higher I_{ON}. The output characteristics measured with the source-drain voltage (V_{DS}) swept from -1 V to 1 V show a more linear relationship between I_{DS} and V_{DS} for the Pd/Au contact devices, as illustrated in Figure 6.9. This improved linearity strongly indicates that Pd/Au forms superior ohmic contacts with $MoTe_2$, especially in the p-type regime, where efficient hole injection is essential for optimal device performance. In contrast, the non-linear behaviour observed in the I_{DS} versus V_{DS} output characteristics of Ti/Au devices, as shown in Figure 6.8(A), is indicative of a Schottky barrier at the metal-semiconductor (M-S) junction. This barrier arises due to the mismatch between the work function of Ti (4.33 eV) and $MoTe_2$.

It is important to note that the $MoTe_2$ bandgap data referenced in this analysis comes from previous studies, which serve as a guide to interpreting the observed device behaviour. However, a more precise determination of the actual $MoTe_2$ bandgap through experimental validation would enhance the accuracy of the conclusions regarding contact behaviour[9]. Figure 6.10 provides a schematic of the p-$MoTe_2$ contact band diagrams for different contact metals, illustrating how the alignment of the metal's work function with the $MoTe_2$ valence band impacts the formation of Schottky or ohmic contacts.

A critical factor influencing the M-S junction behaviour is the phenomenon of Fermi level pinning (FLP). FLP occurs when the Fermi level of the semiconductor becomes "pinned" near the charge neutrality level (CNL) due to surface states at the M-S interface. These surface states trap charges, making the effective Schottky barrier height less sensitive to variations in the metal's work function. As depicted qualitatively in Figure 6.11(A), in an undoped semiconductor with surface states, the Fermi level tends to align near the charge neutrality point, affecting the overall contact resistance and current flow. This FLP effect could be particularly relevant for explaining the higher contact resistance observed in Ti/Au devices, as the surface states may hinder ideal carrier injection across the M-S interface.

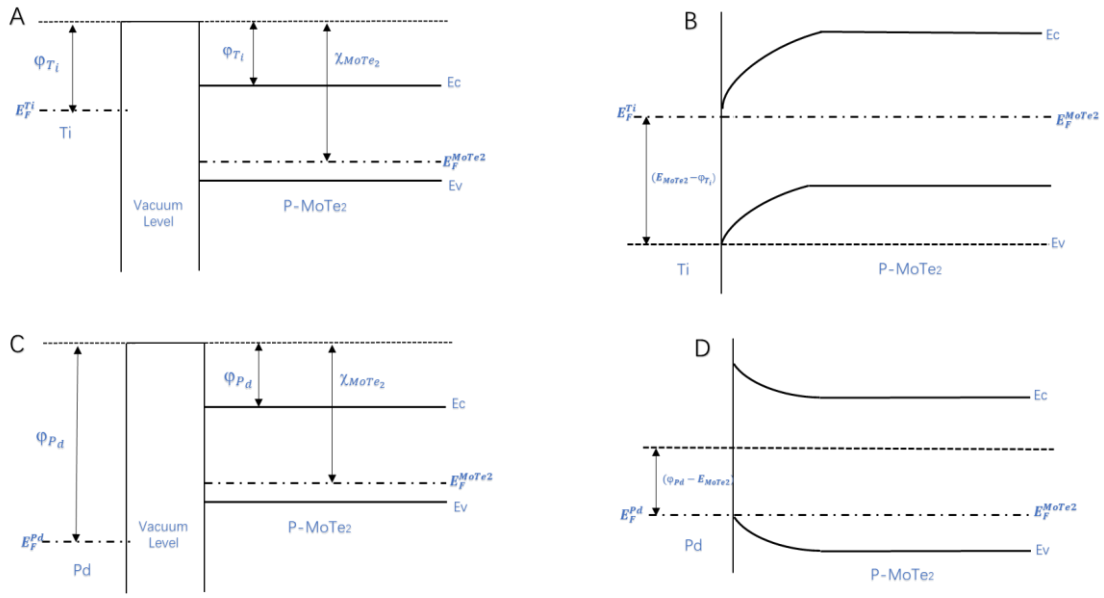

Figure 6.10 Band profile of Pd/$MoTe_2$/Ti [9]

In p-doped materials, the positioning of the Fermi level relative to the charge neutrality level (CNL) is crucial for understanding the charge dynamics at the metal-semiconductor (M-S) interface. When the Fermi level shifts below the CNL, there is a predominance of filled surface states compared to unfilled ones, resulting in a net

positive charge at the surface. This situation can lead to an effective electric field that influences carrier transport across the M-S junction, potentially increasing contact resistance. Conversely, in n-doped materials, when the Fermi level moves above the CNL, more surface states remain unfilled, creating a net negative charge that can facilitate electron injection into the semiconductor.

This charge imbalance at the surface plays a significant role in affecting the M-S interface properties and can diminish the sensitivity of the contact characteristics to the metal's work function. Ideally, in the absence of strong Fermi level pinning, a higher work function metal like palladium (Pd, 5.6 eV) would be expected to enhance the performance of contacts in p-type semiconductors by lowering the Schottky barrier height and improving carrier injection. On the other hand, titanium (Ti), with a lower work function of 4.3 eV, would typically be less effective in this role, leading to higher contact resistance and reduced current flow.

However, the scenario changes when strong Fermi level pinning occurs. In such cases, the behaviour of the M-S contact becomes less reliant on the work function of the metal due to the limited range of the Fermi level, which is predominantly governed by surface states. This restriction results in a situation where, despite the theoretical advantages of using a high work function metal, the actual performance gains may be minimal if the surface states cause strong pinning. In cases of particularly robust pinning, a higher work function metal like Pd could provide significant performance improvements by effectively lowering the Schottky barrier height, allowing for better carrier injection compared to lower work function metals like Ti.

This highlights the complex interplay between doping levels, work function, and surface states in determining the performance of contacts in p-type materials.

Understanding this interplay is essential for optimizing contact designs in 2D materials such as $MoTe_2$, as it impacts overall device efficiency and performance.

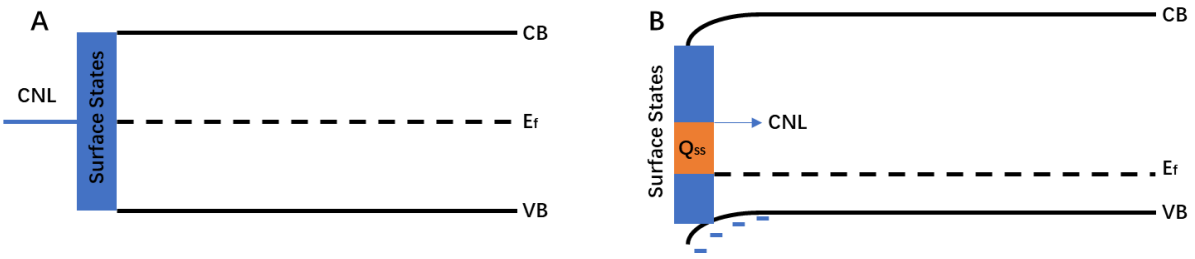

Figure 6.11 A qualitative schematic of a semiconductor with surface states that pin the Fermi Level in the case of (A) no doping and (B) P-type doping.

In this study, the results indicate that while Pd/Au contacts outperform Ti/Au contacts, the overall performance difference between the two device types is not particularly pronounced. This observation may suggest that Fermi level pinning at the $MoTe_2$ interface is not especially strong, allowing for moderate sensitivity to the work function of the contact metal without producing dramatic shifts in performance.

Mobility of $MoTe_2$ FET devices

The carrier mobility (μ_{FE}) of $MoTe_2$ FETs with different metal contacts was investigated using the transfer characteristics (V_{BG}-I_{DS}) shown in Figure 6.9. The field-effect intrinsic mobility (μ_{FE}^*) of the $MoTe_2$ FET is defined by Equation 6.2:

$$\mu_{FE}* = \frac{L}{WC_{ox}V_{ds}} g_m * \qquad equation\ (6.2)$$

where C_{ox} represents the oxide capacitance per unit area for a 100 nm thick SiO_2/Si substrate, and L and W denote the length and width of the $MoTe_2$ channel, respectively. This equation provides an estimate of the intrinsic mobility. However, it is important to

note that the calculated mobility is influenced by external factors such as the device environment (e.g., air vs. vacuum), temperature, and contact resistance. Therefore, this mobility serves as a comparative measure of the performance of different metal contacts rather than representing the pure intrinsic mobility of the material.

A critical parameter in Equation 6.2 is the intrinsic transconductance (g_m^*). Transconductance measures the rate of change of drain current with respect to gate voltage at a constant drain voltage, providing insight into the gate's effectiveness in modulating the drain current. While extrinsic transconductance accounts for parasitic effects such as contact resistance, intrinsic transconductance isolates the gate's direct influence on current modulation. The extrinsic transconductance (g_m) is given by:

$$g_{\mathrm{m}} = \frac{\mathrm{d}I_{ds}}{\partial V_{\mathrm{b}g}} \qquad \textbf{equation (6.3)}$$

For intrinsic transconductance (g_m^*), this calculation excludes the voltage drop across the source resistance (R_{source}), which includes both the sheet resistance of the $MoTe_2$ channel and the contact resistance ($R_{contact}$). Therefore, the intrinsic transconductance equation is modified as:

$$g_m^* = \frac{dI_{ds}}{dV_{bg}^*} \qquad \textbf{euqation (6.4)}$$

Here, V_{bg}^* represents the intrinsic back-gate voltage, accounting for the voltage drops at the source and gate contacts. The source resistance (R_{source}), illustrated in Figure 6.12, is a combination of the contact resistance and the channel's sheet resistance. This adjustment is essential for accurately capturing intrinsic device performance, as it eliminates the influence of parasitic resistances, enabling a more accurate

comparison of behaviour between different metal contact devices. The measured values for extrinsic transconductance, channel resistance, and contact resistance are used to calculate the intrinsic transconductance of the $MoTe_2$ FETs using the following equation.

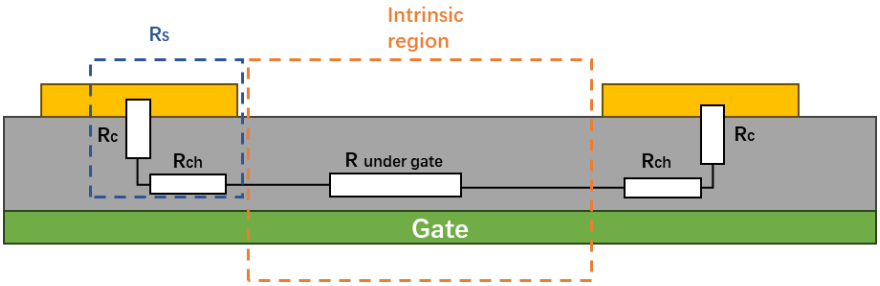

Figure 6.12 Simplified FET model showing "intrinsic" region in red, and access resistance R_s in purple.

The intrinsic transconductance values for the $MoTe_2$ FETs are presented in Figure 6.13. The results demonstrate that transconductance increases with more negative back-gate voltage, indicating stronger gate modulation. Devices with Pd/Au contacts exhibited a higher g_m^*, reaching 0.065 μS/μm, compared to Ti/Au contact devices, which showed an intrinsic transconductance of 0.0275 μS/μm at an applied V_{ds}=0.9V:

$$g_m^* = \frac{dI_{ds}}{d(V_{gs} - I_{ds}R_s)} \qquad \textbf{euqation (6.4)}$$

The intrinsic transconductance values for the $MoTe_2$ FETs are shown in Figure 6.13. The results indicate that transconductance increases with more negative back-gate voltage, demonstrating stronger gate modulation. Devices with Pd/Au contacts exhibited higher g_m^* at 0.065 μS/μm compared to the Ti/Au-contact devices, which displayed an intrinsic transconductance of 0.0275 μS/μm at an applied V_{DS}=0.9 V.

Using Equations 6.2 and 6.5, along with the data from Figure 6.13, the maximum mobility for Ti/Au contact devices was calculated to be 3.45 $cm^2/V \cdot s$, whereas Pd/Au contact devices exhibited slightly lower mobility at 2.85 $cm^2/V \cdot s$ at Vds=0.1V. This finding suggests that the mobility of the $MoTe_2$ FETs is relatively independent of contact resistance. Despite the higher transconductance of the Pd/Au devices, the mobility values for both Ti/Au and Pd/Au contact devices are comparable, indicating that mobility is more strongly influenced by the intrinsic properties of the $MoTe_2$ channel than by the specific metal-semiconductor interface.

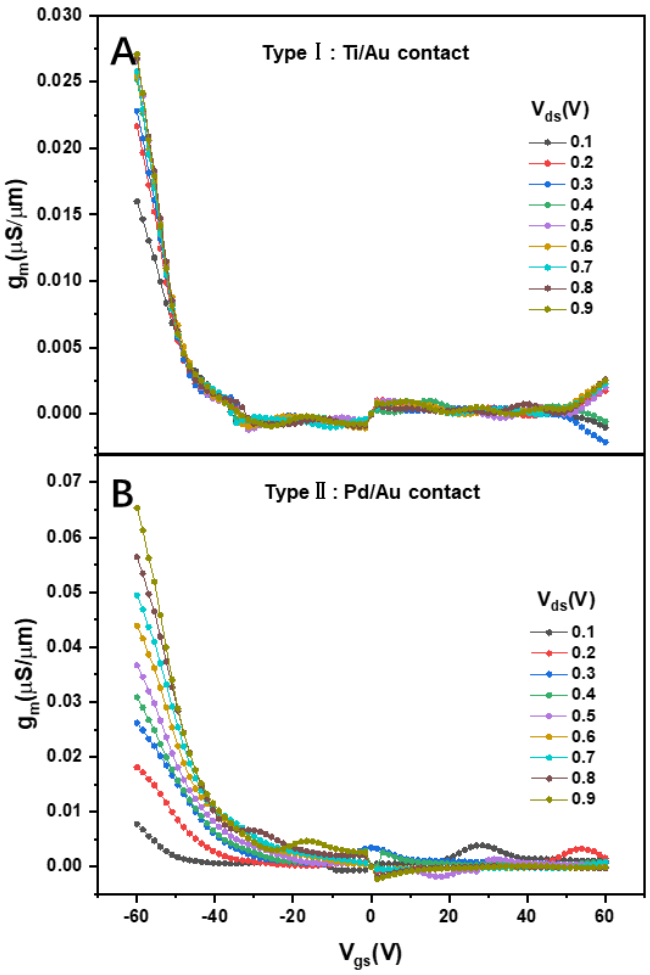

Figure 6.13 The intrinsic transconductance for (A) Ti/Au contact and (B) Pd/Au contact $MoTe_2$ FET devices

$I_{on/off}$ of $MoTe_2$ FET

The switching ratios of the two $MoTe_2$ FET devices are summarised in Figure 6.14. The histogram indicates that channel length is not the dominant factor influencing the switching ratio, as the bar heights do not correlate with changes in channel length. However, it is evident that FETs with Pd/Au contacts generally exhibit higher switching ratios compared to those with Ti/Au contacts. At V_{DS}=0.4V, the on/off current ratios for the p-type FETs are approximately 10^4 for Pd/Au contacts and 10^3 for Ti/Au contacts. These results are consistent with the literature, which reports switching ratios around 10^4 for similar devices.

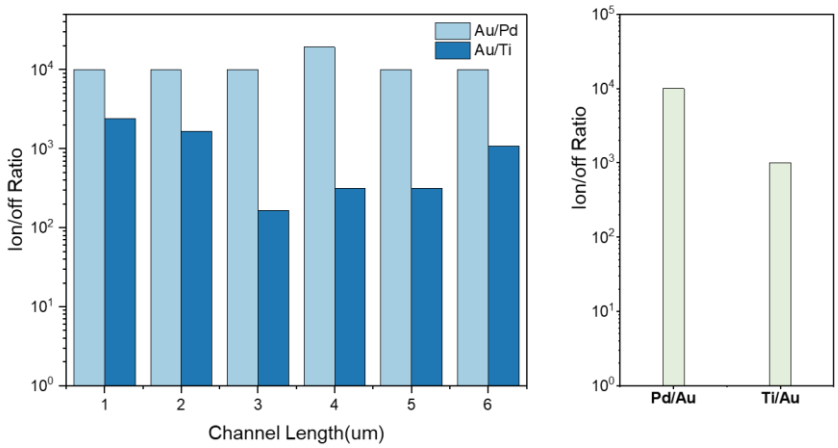

Figure 6.14 $I_{on/off}$ ratio vs different channels from 1μm to 6μm with step 1μm and maximum $I_{on/off}$ ratio for Pd/Au and Ti/Au -contact $MoTe_2$ FETs.

On the right side of Figure 6.14, a comparison of the average switching ratios between the two types of devices is presented. Notably, the Pd/Au-contact FET achieves an on/off current ratio of 10^4, indicating its potential suitability for switching applications. Although an on/off ratio below 10^4 does not represent the highest performance

achievable in other studies, it remains sufficient for certain applications requiring efficient switching.

The performance of the $MoTe_2$ FETs, which are predominantly p-type, exhibits some n-channel behaviour before fully establishing strong p-channel turn-on and turn-off characteristics. This behaviour is likely linked to an increase in off-state current, which is positively correlated with higher V_{DS}. The rise in off-state current at elevated drain voltages can contribute to a reduced overall switching ratio, particularly at higher V_{DS}. Thus, while Pd/Au-contact FETs demonstrate better switching performance than Ti/Au-contact devices, improvements in minimising off-state current could further enhance their switching ratios.

V_{Th} of $MoTe_2$ FET devices

The V_{Th} represents the gate-source voltage at which a FET begins to conduct, marking its "switch-on" point. For significant conduction, the gate-source voltage must exceed V_{Th}. Therefore, a higher V_{Th} requires a larger gate-source voltage to activate the device. Several methods have been used to extract V_{Th} in $MoTe_2$ FETs, including the linear extrapolation (LE) method, the Y-method, and the constant-current method. In this study, the LE method was employed, where V_{Th} is determined by linearly extrapolating the I_{DS}−V_{GS} curve in the linear regime[14]. The intercept of the extrapolated curve on the V_{GS} axis corresponds to the threshold voltage. This method typically uses the tangent to the I_{DS}−V_{GS} curve at the point of peak transconductance (g_m).

Figure 6.15 shows the extraction of V_{Th} for two representative FETs using the LE method, revealing no clear relationship between V_{Th} and V_{DS}. The average V_{Th} for Ti/Au-contact devices is approximately 50V, significantly higher than the average value

of -45V for Pd/Au-contact devices. This indicates that Pd/Au devices require a lower gate voltage to turn on, resulting in more efficient performance. The lower V_{Th} in Pd/Au FETs is attributed to the specific properties of the contact metal and its interaction with the $MoTe_2$ channel.

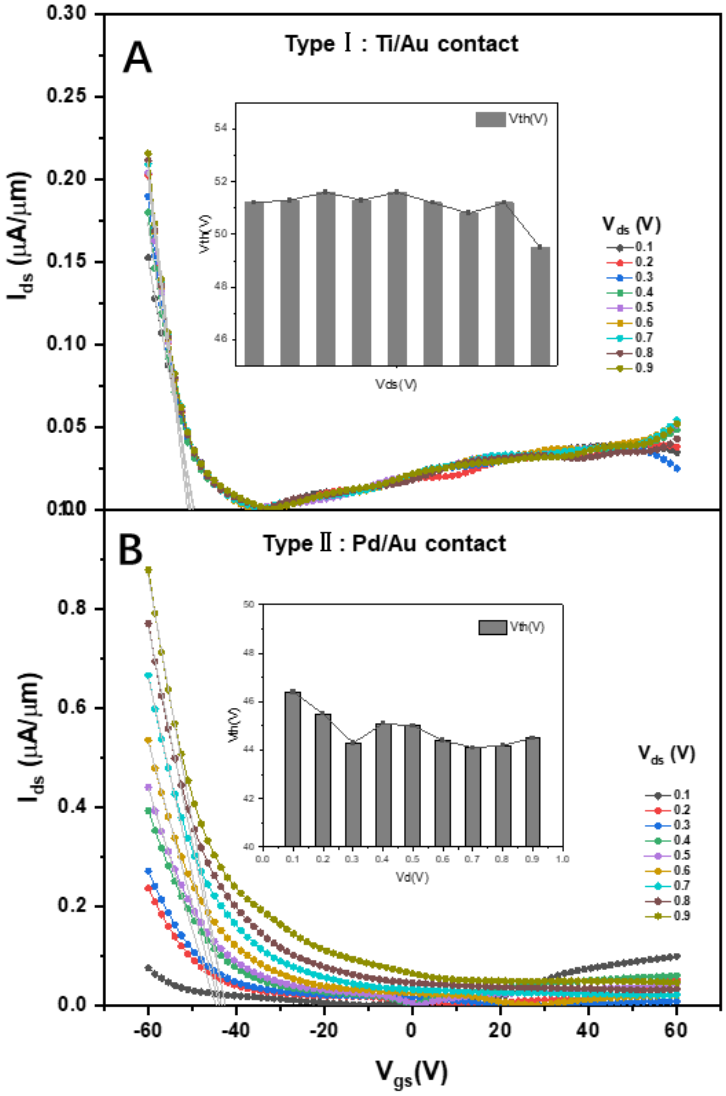

Figure 6.15 V_{Th} extracted for Pd/Au and Ti/Au -contact $MoTe_2$ FETs with LE-Method.

One primary factor influencing V_{Th} is carrier density modulation under varying bias conditions. As the gate-source voltage increases, the carrier density in the channel

rises, causing the FET to transition from the off-state to the on-state. The magnitude of this change is governed by both the intrinsic properties of $MoTe_2$ and the characteristics of the metal-semiconductor interface. For example, the higher Schottky barrier at the Ti/Au interface creates a larger depletion region, necessitating a higher V_{GS} to induce sufficient charge carriers for conduction, which explains the higher V_{Th} in Ti/Au devices. Conversely, the lower Schottky barrier at the Pd/Au interface facilitates more efficient carrier injection, thereby reducing the threshold voltage.

Bias conditions also significantly impact V_{Th} by affecting trap states and surface charge distributions at the metal-semiconductor interface. Under higher V_{DS} , the electric field across the $MoTe_2$ channel increases, potentially altering carrier distribution and affecting V_{Th}. For instance, higher V_{DS} can lead to enhanced carrier depletion or accumulation, depending on the contact metal, potentially shifting the threshold voltage. However, in this study, no significant correlation between V_{Th} and V_{DS} was observed, suggesting that variations in V_{Th} are primarily influenced by the properties of the metal-semiconductor interface rather than external bias conditions[9].

An analysis of the transfer line measurement (TLM) results suggests that the higher contact resistance in Ti/Au devices is due to the larger Schottky barrier height at the metal-semiconductor interface. This higher barrier requires a greater gate voltage to achieve the same level of carrier injection as in Pd/Au devices, thereby raising the threshold voltage. Several factors contribute to the difference in V_{Th} between Ti/Au and Pd/Au contacts in p-type $MoTe_2$ FETs, including differences in metal work function, Schottky barrier height, contact resistance, chemical interactions, and surface states. These factors collectively influence the turn-on characteristics and overall device performance[14].

Variations in carrier density modulation under different gate biases also play a critical role in determining device behaviour. A higher carrier density, induced by a more negative gate voltage in p-type devices, results in a more conductive channel, thereby lowering the effective threshold voltage[9]. However, the presence of traps or defects, particularly near interfaces with higher Schottky barriers (such as Ti/Au), can capture free carriers and increase the effective V_{Th}. Therefore, understanding trap states and interface properties is essential for optimising device performance.

A comparison of the transfer characteristics between devices with Ti/Au and Pd/Au contacts reveals a significant shift in V_{Th} , emphasising the impact of the metallisation process and surface cleanliness during fabrication. The polycrystalline nature of $MoTe_2$ and potential impurities at the metal-$MoTe_2$ interface introduce variability in V_{Th}, particularly when many devices are fabricated on the same substrate. Consequently, the quality of the $MoTe_2$ material, the deposited metal, and the metal-semiconductor interface are critical factors affecting device performance. Further experimental and theoretical studies are needed to fully understand and optimise these metal-semiconductor interfaces, making this a crucial area for future research.

Subthreshold Swing (SS) of $MoTe_2$ FET

The subthreshold swing (SS) is a critical parameter for evaluating the switching efficiency of a FET, particularly as device scaling continues in semiconductor technology. It quantifies the sharpness of the transistor's switching behaviour and measures how efficiently a device transitions between the off-state and the on-state. Specifically, the SS defines how much gate voltage (V_{GS}) is required to change the I_{DS} by one order of magnitude (a factor of 10). The ideal SS value is 60 mV/decade at room temperature; however, achieving this is challenging due to intrinsic material

limitations and device structures[14]. SS can be calculated using Equation 6.4, as follows:

$$SS = \frac{dV_{gs}}{d(\log I_{ds})} \qquad equation\ (6.4)$$

Lower subthreshold swing (SS) values correspond to sharper switching, which minimises power consumption and improves the overall performance of the FET. In this study, the transfer curves of $MoTe_2$ FETs with Pd/Au and Ti/Au contacts were analysed. The lowest SS for the Pd/Au-contact FET was 800 mV/dec, while the Ti/Au-contact FET exhibited a higher SS of 1100 mV/dec. These results highlight that Pd/Au contacts offer superior switching performance due to the lower SS. This improvement can be attributed to the more efficient metal-semiconductor interface provided by the Pd/Au contacts, which reduces contact resistance and enhances the switching behaviour.

Additionally, FETs with varying channel lengths were tested. Although no direct relationship between channel length and SS was observed, the general trend showed that Pd/Au-contact devices consistently demonstrated lower SS values compared to their Ti/Au counterparts. This consistent reduction in SS for Pd/Au-contact devices makes them more suitable for high-performance applications, however, even the best-performing $MoTe_2$ FETs in this study are still far from the ideal SS of 60 mV/dec.

The role of contact resistance is crucial in determining the SS of $MoTe_2$ FETs. Contact resistance adds an extra component in series with the transistor channel, which hampers the switching speed by slowing down the charging and discharging processes during transitions. This increased resistance requires a larger gate voltage to effectively control the flow of current, leading to higher SS values[10,15–18].

In the case of $MoTe_2$ FETs with Ti/Au contacts, the higher contact resistance directly contributes to their poorer switching performance, as indicated by the larger SS. The higher Schottky barrier and less efficient carrier injection at the Ti/Au-$MoTe_2$ interface cause the device to respond more slowly, degrading overall switching performance. On the other hand, Pd/Au contacts form a more favourable metal-semiconductor interface, leading to lower contact resistance. This enables faster and more efficient switching, resulting in lower SS values. Consequently, reducing contact resistance is essential for achieving better switching performance and minimising power dissipation in $MoTe_2$ FETs.

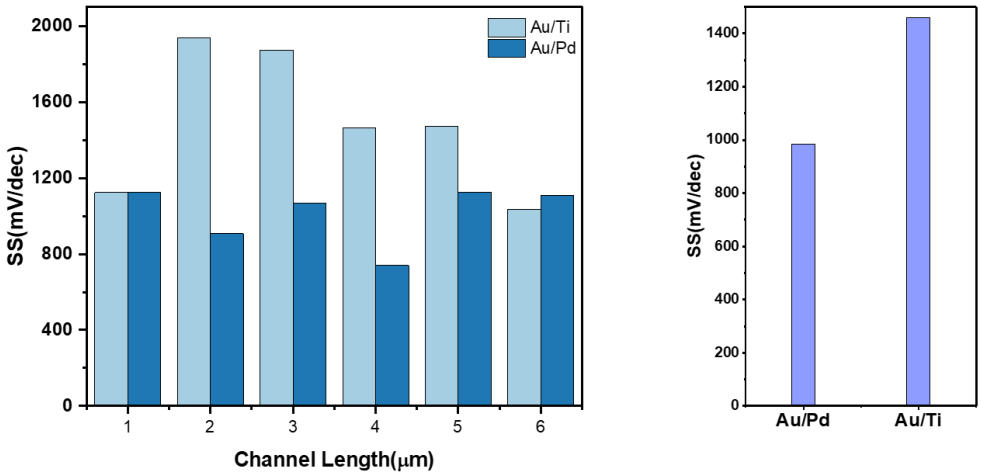

Figure 6.16 Summary SS vs different channel lengths from 1μm to 6μm with step 1μm and maximum SS ratio for Pd/Au and Ti/Au -contact $MoTe_2$ FETs.

Figure 6.16 illustrates the SS values as a function of different channel lengths (ranging from 1 μm to 6 μm in 1 μm increments) for $MoTe_2$ FETs with Pd/Au and Ti/Au contacts. The Pd/Au-contact devices consistently exhibit lower SS values across various channel lengths, confirming their superior performance in terms of switching efficiency. However, despite this improvement, both types of FETs remain far from the theoretical

limit of 60 mV/dec, indicating that further optimisation of the metal-semiconductor interface and contact resistance is necessary to approach the ideal SS values. In summary, contact resistance plays a crucial role in determining the subthreshold swing in $MoTe_2$ FETs. By optimising the metal contacts, particularly through the use of Pd/Au, the contact resistance can be reduced, thereby enhancing the switching performance of the device. However, further research is required to push the SS values closer to the ideal 60 mV/dec for practical applications.

6.4 Comparison with previous works on $MoTe_2$ FETs

In summary, the performance indicators of Pd/Au and Ti/Au contact devices demonstrate that the choice of contact metal significantly affects key parameters such as the $I_{on/off}$ ratio, SS, and V_{Th}, but has a minimal impact on device mobility. These differences in performance are likely attributable to contact resistance and the weak FLP effect associated with variations in Schottky barrier height at the metal-semiconductor interface. However, further detailed investigations are required to better understand these mechanisms.

Table 6.1 summarises the numerical values of the main parameters of both devices.

Parameter	Pd/Au Contact	Ti/Au Contact
Mobility ($cm^2V^{-1}s^{-1}$)	2.5	2.6
$I_{on/off}$ Ratio	10^4	10^3
SS(mV/dec)	1000	1400
V_{Th}(V)	45	50

Table 6.1 summarizes the numerical values of the main parameters for the two devices. When comparing the performance indicators, Pd/Au contact $MoTe_2$ FETs exhibit superior performance compared to Ti/Au contact devices. Specifically, Pd/Au FETs

show a higher $I_{on/off}$ ratio, lower SS, and lower V_{Th}, suggesting more efficient switching behavior and lower power consumption. As expected, the different contact metals do not appear to have a significant effect on channel mobility between the two device types. To further contextualize these findings, I reviewed and collected comparative data from other studies on $MoTe_2$ FET performance

Table 6.2 Comparison of $MoTe_2$ FET performance between this work and literature work[10,15–18]

	Contact Metal	$MoTe_2$ Thickness	Fabrication Method	Ion/off Ratio	Mobility ($cm^2V^{-1}s^{-1}$)	On Current	SS (mV/dec)	Reference
Type I (this work)	Ti/Au	8nm	In-suit photolith	10^3	2.6	0.26μA/μm	1400	This work
Type II (this work)	Pd/Au	8nm	In-suit photolith	10^4	2.6	1μA/μm	1000	This work
Example 1	Ti/Au	few	Transfer	10^3	0.35	95nA	-	[10]
Example 2	Pd/Au	4.2nm	Transfer	10^6	11	3.3μA	-	[10]
Example 3	Ti	3-6L	Transfer	10^2	8	10μA/μm	-	[15]
Example 4	Ti/Au	5.6	Transfer	10^4	~0.5	0.5μA		[16]
Example 5	Pd	Few	Transfer	10^4	0.29	5nA		[17]
Example 6	Pd	4nm	Transfer +laser induce	10^5	13.6	~6.25μA	96	[18]

Table 6.2 presents a comparison between the fabricated devices in this study and six examples from the literature, providing a broader perspective on $MoTe_2$ FET performance across different research efforts. Unfortunately, due to the variability in film flexibility and fabrication methods among studies, it is challenging to find devices fabricated under identical parameters to those used in this work. Devices reported in the literature often employ top-down transfer techniques, which significantly impact material properties and enhance overall device performance. In contrast, the bottom-up growth method used in this study, such as CVD, can introduce material defects and

grain boundaries, potentially degrading electrical properties. While this method is advantageous for large-scale production, it is known to affect factors such as carrier mobility and subthreshold swing (SS), leading to lower performance when compared to devices fabricated using more controlled top-down approaches.

One key factor contributing to the lower mobility observed in this study, compared to literature values, is the impact of material defects and grain boundaries. The CVD growth process, while suitable for producing large-area films, inherently results in polycrystalline material with grain boundaries that act as scattering centres for charge carriers. These boundaries impede carrier transport, reducing the field-effect mobility (μ) in the devices. In contrast, many literature studies utilise top-down exfoliation or other transfer methods that preserve the pristine quality of the $MoTe_2$ flakes, leading to much higher carrier mobility. Additionally, material defects such as vacancies or dislocations introduced during CVD growth can create localized trap states within the semiconductor. These trap states further reduce mobility by capturing charge carriers and preventing them from contributing to current flow, thereby lowering the overall device performance.

Another factor contributing to the lower mobility in this project is related to the fabrication techniques used, particularly photolithography. The photolithography processes can introduce additional non-uniformities and defects at the metal-semiconductor interface, which increase contact resistance. Higher contact resistance impedes the efficient injection of carriers from the metal contacts into the $MoTe_2$ channel, thereby reducing the overall carrier mobility in the FETs. This contact resistance, coupled with potential interface issues, limits performance compared to

optimised devices in the literature that often utilise more sophisticated fabrication techniques with precise control over the contact interfaces.

Moreover, the absence of doping in the devices studied here likely contributes to the relatively lower mobility values. In many high-mobility $MoTe_2$ FETs reported in the literature, doping techniques are employed to modulate carrier concentration and reduce contact resistance, enhancing carrier transport through the channel. The lack of doping in the devices fabricated for this project leads to a natural limitation in mobility, as the carriers in the channel are not efficiently injected and transported. This is evident in the comparison of devices in Table 6.2, where doped devices show not only higher mobility but also significantly lower SS values, further indicating the influence of doping on overall device performance.

External factors, such as channel length and the choice of contact metals, also play a significant role in determining mobility. Shorter channel lengths, as used in some literature examples, can result in higher mobility due to reduced scattering and resistance along the channel. Additionally, the choice of Pd/Au or Ti/Au contact metals in this study, while effective, may not offer the same level of carrier injection efficiency as contact materials used in other studies, further contributing to the lower mobility observed.

Given these constraints, it is not surprising that the FETs produced in this work, though within an acceptable performance range, exhibit lower mobility and higher SS compared to devices in the literature. Overall, these discrepancies can be attributed to differences in fabrication methodologies, material quality, and the absence of doping, which collectively hinder the optimisation of electrical properties in the FETs presented in this study.

6.5 Summary

This chapter primarily summarises the characteristics of $MoTe_2$-based FET devices fabricated using a combination of novel CVD technology and traditional photolithography. TLM measurements and analyses of the transfer and output characteristics of $MoTe_2$ FETs are presented, focusing on the influence of metal contacts on device performance.

The study first investigates the effects of different contact metals by analysing the contact resistance, output, and transfer characteristics of $MoTe_2$ FET devices. Key device parameters were extracted and evaluated. It was found that Pd/Au contacts form ohmic interfaces with $MoTe_2$ more readily than Ti/Au, leading to lower contact resistance and improved device performance. In contrast, the higher potential barrier of Ti/Au increases the likelihood of forming a Schottky contact, which reduces carrier injection and decreases the carrier concentration within the device.

Additionally, our results indicated that while the choice of contact metal does not significantly affect the mobility of $MoTe_2$ FETs, it does have a notable impact on the $I_{on/off}$ ratio, SS, and V_{Th}. Devices with Pd/Au contacts, which possess a higher work function and lower contact resistance, demonstrated superior overall performance, confirming predominantly p-type operation.

Through a comprehensive analysis of the different devices, it was demonstrated that synthesising $MoTe_2$ films using $FeTe_2$ as a precursor in CVD, combined with traditional photolithography, effectively produces $MoTe_2$ FETs with performance comparable to those reported in the literature, which are typically fabricated using exfoliation and top-

down methods. This work highlights the potential of this fabrication approach for scalable, high-performance $MoTe_2$ devices**.**

6.6 Reference:

1. Pradhan, N. R., Rhodes, D., Feng, S., Xin, Y., Memaran, S., Moon, B.-H., Terrones, H., Terrones, M., & Balicas, L. (2014, June 4). *Field-Effect Transistors Based on Few-Layered α-MoTe2* (world) [Research-article]. ACS Publications; American Chemical Society. https://doi.org/10.1021/nn501013c

2. Kim, S., Konar, A., Hwang, W.-S., Lee, J. H., Lee, J., Yang, J., Jung, C., Kim, H., Yoo, J.-B., Choi, J.-Y., Jin, Y. W., Lee, S. Y., Jena, D., Choi, W., & Kim, K. (2012). High-mobility and low-power thin-film transistors based on multilayer MoS2 crystals. *Nature Communications*, *3*(1), Article 1. https://doi.org/10.1038/ncomms2018

3. Larentis, S., Fallahazad, B., Movva, H. C. P., Kim, K., Rai, A., Taniguchi, T., Watanabe, K., Banerjee, S. K., & Tutuc, E. (2017). Reconfigurable Complementary Monolayer MoTe2 Field-Effect Transistors for Integrated Circuits. *ACS Nano*, *11*(5), 4832–4839. https://doi.org/10.1021/acsnano.7b01306

4. Qiu, H, Pan, L, Yao, Z, Li, J, Shi, Y, & Wang, X. (2012). Electrical characterisation of back-gated bi-layer MoS2 field-effect transistors and the effect of ambient on their performances. *Applied Physics Letters*, *100*(12), 123104. https://doi.org/10.1063/1.3696045

5. Gao, J., Li, B., Tan, J., Chow, P., Lu, T.-M., & Koratkar, N. (2016). Ageing of Transition Metal Dichalcogenide Monolayers. *ACS Nano*, *10*(2), 2628–2635. https://doi.org/10.1021/acsnano.5b07677

6. Kim, K., Larentis, S., Fallahazad, B., Lee, K., Xue, J., Dillen, D. C., Corbet, C. M., & Tutuc, E. (2015). Band Alignment in WSe2–Graphene Heterostructures. *ACS Nano*, *9*(4), 4527–4532. https://doi.org/10.1021/acsnano.5b01114

7. Yang, S., Xu, X., Xu, W., Han, B., Ding, Z., Gu, P., Gao, P., & Ye, Y. (2020). Large-Scale Vertical 1T′/2H MoTe2 Nanosheet-Based Heterostructures for Low Contact Resistance Transistors. *ACS Applied Nano Materials*, *3*(10), 10411–10417. https://doi.org/10.1021/acsanm.0c02302

8. Liu, Y., Guo, J., Zhu, E., Liao, L., Lee, S.-J., Ding, M., Shakir, I., Gambin, V., Huang, Y., & Duan, X. (2018). Approaching the Schottky–Mott limit in van der Waals metal–semiconductor junctions. *Nature*, *557*(7707), Article 7707. https://doi.org/10.1038/s41586-018-0129-8

9. Parilla, P. A., Dillon, A. C., Parkinson, B. A., Jones, K. M., Alleman, J., Riker, G., Ginley, D. S., & Heben, M. J. (2004). Formation of Nanooctahedra in Molybdenum Disulfide and Molybdenum Diselenide Using Pulsed Laser Vaporization. *The Journal of Physical Chemistry B*, *108*(20), 6197–6207. https://doi.org/10.1021/jp036202+

10. Iqbal, M. W., Firdous, F., Manzoor, M., Ateeq, H., Azam, S., Aftab, S., Kamran, M. A., Rehman, A. ul, & Majid, A. (2020). Study of electrical attributes of molybdenum ditelluride (MoTe2) FET using experimental and theoretical evidences. *Microelectronic Engineering*, *230*, 111365. https://doi.org/10.1016/j.mee.2020.111365

11. Jing, X., Illarionov, Y., Yalon, E., Zhou, P., Grasser, T., Shi, Y., & Lanza, M. (2020). Engineering Field Effect Transistors with 2D Semiconducting Channels: Status and Prospects. *Advanced Functional Materials*, *30*(18), 1901971. https://doi.org/10.1002/adfm.201901971

12. Rani, A., DiCamillo, K., Khan, M. A. H., Paranjape, M., & Zaghloul, M. E. (2019). Tuning the Polarity of MoTe2 FETs by Varying the Channel Thickness for Gas-Sensing Applications. *Sensors*, *19*(11), Article 11. https://doi.org/10.3390/s19112551

13. Choi, K., Lee, Y. T., Kim, J. S., Min, S.-W., Cho, Y., Pezeshki, A., Hwang, D. K., & Im, S. (2016). Non-Lithographic Fabrication of All-2D α-MoTe2 Dual Gate Transistors. *Advanced Functional Materials*, *26*(18), 3146–3153. https://doi.org/10.1002/adfm.201505346

14. Yang, Y., Zhu, X., Zhang, K., Zhu, H., Chen, L., & Sun, Q. (2021). Observation of different transport behaviours in a two-dimensional MoTe2 field-effect transistor with engineered gate stack. *Microelectronic Engineering*, *237*, 111497. https://doi.org/10.1016/j.mee.2020.111497

15. Conan, A., Bonnet, A., Zoaeter, M., & Ramoul, D. (1984). Dependence of the Total Mobility in a One-Band Model Applicationto n-Type MoTe2. *Physica Status Solidi (b)*, *124*(1), 403–410. https://doi.org/10.1002/pssb.2221240144

16. Sarkar, D., Xie, X., Liu, W., Cao, W., Kang, J., Gong, Y., Kraemer, S., Ajayan, P. M., & Banerjee, K. (2015). A subthermionic tunnel field-effect transistor with an atomically thin channel. *Nature*, *526*(7571), Article 7571. https://doi.org/10.1038/nature15387

17. Smithe, K. K. H., Suryavanshi, S. V., Muñoz Rojo, M., Tedjarati, A. D., & Pop, E. (2017). Low Variability in Synthetic Monolayer MoS2 Devices. *ACS Nano*, *11*(8), 8456–8463. https://doi.org/10.1021/acsnano.7b04100

18. Nasr, J. R., Schulman, D. S., Sebastian, A., Horn, M. W., & Das, S. (2019). Mobility Deception in Nanoscale Transistors: An Untold Contact Story. *Advanced Materials*, *31*(2), 1806020. https://doi.org/10.1002/adma.201806020

19. Das, S., Sebastian, A., Pop, E., McClellan, C. J., Franklin, A. D., Grasser, T., Knobloch, T., Illarionov, Y., Penumatcha, A. V., Appenzeller, J., Chen, Z., Zhu, W., Asselberghs, I., Li, L.-J., Avci, U. E., Bhat, N., Anthopoulos, T. D., & Singh, R. (2021). Transistors based on two-dimensional materials for future integrated circuits. *Nature Electronics*, *4*(11), Article 11. https://doi.org/10.1038/s41928-021-00670-1

20. Aftab, S., Iqbal, M. W., Afzal, A. M., Khan, M. F., Hussain, G., Waheed, H. S., & Kamran, M. A. (2019). Formation of an MoTe2 based Schottky junction employing

ultra-low and high resistive metal contacts. *RSC Advances*, *9*(18), 10017–10023. https://doi.org/10.1039/C8RA09656B

21. Huang, J.-H., Deng, K.-Y., Liu, P.-S., Wu, C.-T., Chang, W.-H., Lee, Y.-J., & Hou, T.-H. (n.d.). *Large-Area Two-Dimensional Layered MoTe2 by Physical Vapor Deposition and Solid-Phase Crystallization in a Tellurium-Free Atmosphere*.

22. Long, G., Maryenko, D., Shen, J., Xu, S., Hou, J., Wu, Z., Wong, W. K., Han, T., Lin, J., Cai, Y., Lortz, R., & Wang, N. (2016). Achieving Ultrahigh Carrier Mobility in Two-Dimensional Hole Gas of Black Phosphorus. *Nano Letters*, *16*(12), 7768–7773. https://doi.org/10.1021/acs.nanolett.6b03951

23. Liu, D., Chen, X., Yan, Y., Zhang, Z., Jin, Z., Yi, K., Zhang, C., Zheng, Y., Wang, Y., Yang, J., Xu, X., Chen, J., Lu, Y., Wei, D., Wee, A. T. S., & Wei, D. (2019). Conformal hexagonal-boron nitride dielectric interface for tungsten diselenide devices with improved mobility and thermal dissipation. *Nature Communications*, *10*(1), Article 1. https://doi.org/10.1038/s41467-019-09016-0

24. Luo, P., Zhuge, F., Wang, F., Lian, L., Liu, K., Zhang, J., & Zhai, T. (2019). PbSe Quantum Dots Sensitized High-Mobility Bi2O2Se Nanosheets for High-Performance and Broadband Photodetection Beyond 2 μm. *ACS Nano*, *13*(8), 9028–9037. https://doi.org/10.1021/acsnano.9b03124

25. Qin, J.-K., Liao, P.-Y., Si, M., Gao, S., Qiu, G., Jian, J., Wang, Q., Zhang, S.-Q., Huang, S., Charnas, A., Wang, Y., Kim, M. J., Wu, W., Xu, X., Wang, H.-Y., Yang, L., Khin Yap, Y., & Ye, P. D. (2020). Raman response and transport properties of tellurium atomic chains encapsulated in nanotubes. *Nature Electronics*, *3*(3), Article 3. https://doi.org/10.1038/s41928-020-0365-4

26. Wang, C.-Y., Liang, S.-J., Wang, S., Wang, P., Li, Z., Wang, Z., Gao, A., Pan, C., Liu, C., Liu, J., Yang, H., Liu, X., Song, W., Wang, C., Cheng, B., Wang, X., Chen, K., Wang, Z., Watanabe, K., … Miao, F. (2020). Gate-tunable van der Waals heterostructure for reconfigurable neural network vision sensor. *Science Advances*, *6*(26), eaba6173. https://doi.org/10.1126/sciadv.aba6173

27. Dean, C. R., Young, A. F., Meric, I., Lee, C., Wang, L., Sorgenfrei, S., Watanabe, K., Taniguchi, T., Kim, P., Shepard, K. L., & Hone, J. (2010). Boron nitride substrates for high-quality graphene electronics. *Nature Nanotechnology*, *5*(10), Article 10. https://doi.org/10.1038/nnano.2010.172

28. Liu, E., Fu, Y., Wang, Y., Feng, Y., Liu, H., Wan, X., Zhou, W., Wang, B., Shao, L., Ho, C.-H., Huang, Y.-S., Cao, Z., Wang, L., Li, A., Zeng, J., Song, F., Wang, X., Shi, Y., Yuan, H., … Xing, D. (2015). Integrated digital inverters based on two-dimensional anisotropic ReS2 field-effect transistors. *Nature Communications*, *6*(1), Article 1. https://doi.org/10.1038/ncomms7991

29. Liang, S.-J., Cheng, B., Cui, X., & Miao, F. (2020). Van der Waals Heterostructures for High-Performance Device Applications: Challenges and Opportunities. *Advanced Materials*, *32*(27), 1903800. https://doi.org/10.1002/adma.201903800

30. Pi, L., Wang, P., Liang, S.-J., Luo, P., Wang, H., Li, D., Li, Z., Chen, P., Zhou, X., Miao, F., & Zhai, T. (2022). Broadband convolutional processing using band-alignment-tunable heterostructures. *Nature Electronics*, *5*(4), Article 4. https://doi.org/10.1038/s41928-022-00747-5

31. Yang, S., Liu, K., Xu, Y., Liu, L., Li, H., & Zhai, T. (2023). Gate Dielectrics Integration for 2D Electronics: Challenges, Advances, and Outlook. *Advanced Materials*, *35*(18), 2207901. https://doi.org/10.1002/adma.202207901

32. Valletta, A., Gaucci, P., Mariucci, L., Pecora, A., Cuscunà, M., Maiolo, L., Fortunato, G., & Brotherton, S. D. (2009). Role of gate oxide thickness in controlling short channel effects in polycrystalline silicon thin film transistors. *Applied Physics Letters*, *95*(3), 033507. https://doi.org/10.1063/1.3177196

33. Liu, A., Zhu, H., Sun, H., Xu, Y., & Noh, Y.-Y. (2018). Solution Processed Metal Oxide High-κ Dielectrics for Emerging Transistors and Circuits. *Advanced Materials*, *30*(33), 1706364. https://doi.org/10.1002/adma.201706364

34. Tian, J., Wang, Q., Huang, X., Tang, J., Chu, Y., Wang, S., Shen, C., Zhao, Y., Li, N., Liu, J., Ji, Y., Huang, B., Peng, Y., Yang, R., Yang, W., Watanabe, K., Taniguchi, T., Bai, X., Shi, D., … Zhang, G. (2023). Scaling of MoS2 Transistors and Inverters to Sub-10 nm Channel Length with High Performance. *Nano Letters*, *23*(7), 2764–2770. https://doi.org/10.1021/acs.nanolett.3c00031

35. Yin, L., Wang, Z., Wang, F., Xu, K., Cheng, R., Wen, Y., Li, J., & He, J. (2017). Ferroelectric-induced carrier modulation for ambipolar transition metal dichalcogenide transistors. *Applied Physics Letters*, *110*(12), 123106. https://doi.org/10.1063/1.4979088

36. Pereira, L., Barquinha, P., Fortunato, E., & Martins, R. (2005). Influence of the oxygen/argon ratio on the properties of sputtered hafnium oxide. *Materials Science and Engineering: B*, *118*(1–3), 210–213. Scopus. https://doi.org/10.1016/j.mseb.2004.12.030

37. Mleczko, M. J., Yu, A. C., Smyth, C. M., Chen, V., Shin, Y. C., Chatterjee, S., Tsai, Y.-C., Nishi, Y., Wallace, R. M., & Pop, E. (2019). Contact Engineering High-Performance n-Type MoTe2 Transistors. *Nano Letters*, *19*(9), 6352–6362. https://doi.org/10.1021/acs.nanolett.9b02497

38. Empante, T. A., Zhou, Y., Klee, V., Nguyen, A. E., Lu, I.-H., Valentin, M. D., Naghibi Alvillar, S. A., Preciado, E., Berges, A. J., Merida, C. S., Gomez, M., Bobek, S., Isarraraz, M., Reed, E. J., & Bartels, L. (2017). Chemical Vapor Deposition Growth of Few-Layer MoTe2 in the 2H, 1T′, and 1T Phases: Tunable Properties of MoTe2 Films. *ACS Nano*, *11*(1), 900–905. https://doi.org/10.1021/acsnano.6b07499

7.0 Conclusion and Future Work

7.1 Conclusion

This study provides a comprehensive overview of the complete process for fabricating CVD $MoTe_2$-based FETs, encompassing film preparation, device fabrication, and performance verification.

First, a novel chemical vapour deposition (CVD) system was successfully developed to deposit both 2H- and 1T-phase $MoTe_2$ thin films by directly tellurising a Mo-based precursor layer using a $FeTe_2$ precursor, rather than elemental tellurium. The phase selectivity was found to depend on the choice of the Mo precursor; specifically, Mo was preferentially converted into 2H-$MoTe_2$, while MoO_3 yielded 1T-$MoTe_2$. The resulting films were thoroughly characterised using Raman spectroscopy, atomic force microscopy (AFM), and scanning electron microscopy (SEM). The characterisation results confirmed that the films were phase-pure and uniform across the substrate. Furthermore, it was observed that the morphology of the precursor film directly influenced the morphology of the resulting $MoTe_2$ film. By adjusting the thickness of the precursor layer, the number of $MoTe_2$ layers could be effectively controlled, with AFM employed to measure the resulting film thickness. The successful transfer of CVD-grown $MoTe_2$ using different auxiliary transfer layers demonstrated the material's versatility for a wide range of applications.

Next, the study discusses the optimisation of the fabrication process for back-gated $MoTe_2$ FETs, combining CVD growth with traditional photolithography techniques. This work demonstrates both the feasibility of using CVD-grown 2H-$MoTe_2$ in semiconductor applications and the potential for large-scale production of 2D-FETs.

During device fabrication, it was found that the developer and lift-off solutions influenced the etching and crystallinity of the $MoTe_2$ film. Consequently, an optimised photolithography process was established, using 1165 as the lift-off solution and introducing an auxiliary SPR.92 layer to protect the $MoTe_2$ during metal patterning. This process sequence was further refined through comparative experiments, ultimately leading to the successful fabrication of $MoTe_2$ FETs.

Finally, the electrical performance of the fabricated 2H-$MoTe_2$ FETs was evaluated, with a focus on output and transfer characteristics. Through performance analysis and critical parameter extraction, the factors influencing device behaviour were identified. Initially, the effect of contact metal was studied, revealing that devices with thin-film Au/Pd contacts exhibited significantly lower contact resistance (0.79 MΩ·μm) and formed ohmic contacts, in contrast to Au/Ti contacts. The transfer characteristics of the $MoTe_2$ devices displayed predominantly p-type ambipolar behaviour. Notably, the Au/Pd-contacted devices demonstrated superior electrical performance, with a SS of 1 V/dec, a mobility of 2.5 $cm^2/V{\cdot}s$, and an on/off current ratio of 10^4. Furthermore, the study also investigated the influence of the gate dielectric on the performance of the $MoTe_2$ FETs.

7.2 Future work

The exploration of 2D semiconductor materials, such as transition metal dichalcogenides (TMDCs) like $MoTe_2$, presents significant opportunities for advancing future electronic applications due to their unique properties. However, realising the full potential of these materials requires overcoming critical challenges, particularly in contact engineering and novel stacking methods. Addressing these challenges is essential for enhancing device performance, scalability, and cost-effectiveness.

A primary focus in the development of 2D materials lies in reducing contact resistance, as this can significantly improve charge injection and overall field-effect transistor (FET) functionality. Traditional doping methods are often less effective for 2D semiconductors, and edge contact approaches face limitations in scalability. Specialized metals, such as Pd/Au, have shown promise in reducing contact resistance in $MoTe_2$-based devices, but further exploration of higher work function metals and 2D contact materials could yield even greater improvements. Additionally, innovative fabrication methods are necessary to achieve consistent, low-resistance ohmic contacts, which are crucial for pushing the performance boundaries of FET devices.

Alongside contact engineering, the optimisation of gate dielectrics, such as the use of Al_2O_3, could enhance device performance by reducing leakage currents and improving mobility. Concurrently, refining stacking and fabrication techniques offers further potential for advancing 2D devices. Current methods, such as electron-beam lithography and photolithography, have proven successful in producing $MoTe_2$ FETs; however, enhancements in transfer processes and the refinement of CVD to produce high-quality, single-crystal films could further improve performance.

The simultaneous growth of both 1T- and 2H-phase $MoTe_2$ on the same substrate, utilising 1T-$MoTe_2$ as a contact material, presents an innovative approach to improving device functionality. Furthermore, adjusting the thickness of $MoTe_2$ films and exploring various gate dielectric materials could optimise key device parameters such as the on/off ratio, subthreshold swing (SS), and mobility. Techniques like dual gating and the creation of heterostructures with other 2D materials may further enhance the versatility

of $MoTe_2$-based FETs, opening avenues for advanced applications in nanoelectronics and flexible devices.

While the challenges are formidable, the potential of 2D materials like $MoTe_2$ to revolutionise the semiconductor industry and challenge the limits of Moore's Law remains compelling. Through sustained research into contact engineering, stacking methods, and material properties, 2D semiconductors hold the promise of driving the next wave of technological advancements in the field of electronics.

Appendix

A1 Transmission Electron Microscopy (TEM) characteristic on 2H-and 1T- MoTe2

High-resolution transmission electron microscopy (HRTEM) was used to evaluate the crystallinity of 2H-$MoTe_2$ films transferred onto TEM grids.

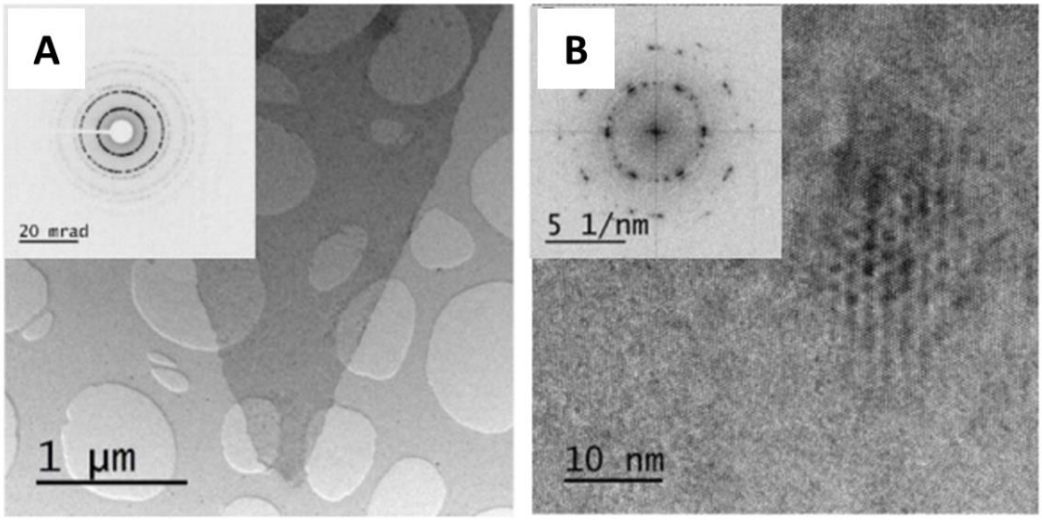

Figure A1.1 2H-$MoTe_2$ *film supported by porous carbon on a TEM grid, the pore network is visible as a support, (A) the darker area in the centre of the image represents the* $MoTe_2$ *film (B) Diffraction from a selected area is shown as a series of diffraction rings rather than spots.*

To determine whether iron contamination in the $MoTe_2$ samples originated from $FeTe_2$ precursors, energy analytical dispersive XPS was performed on the samples under a transmission electron microscope. Diffraction of selected areas confirmed the polycrystalline nature of the film as revealed by area-specific electron diffraction, as the test results appeared as diffraction rings as opposed to spots (Figure A1.1 A). Examine the sample at a higher magnification to accurately represent the crystal structure and orientation (Figure A1.2 B). In addition, ripples exist between the crystal layers in the image's centre. However, it is impossible to determine whether the CVD-

produced films are polycrystalline or whether they are destroyed during transfer to the TEM grid and therefore appear polycrystalline. The crystallinity of CVD-prepared 1T-$MoTe_2$ TEM result displayed in A1.2

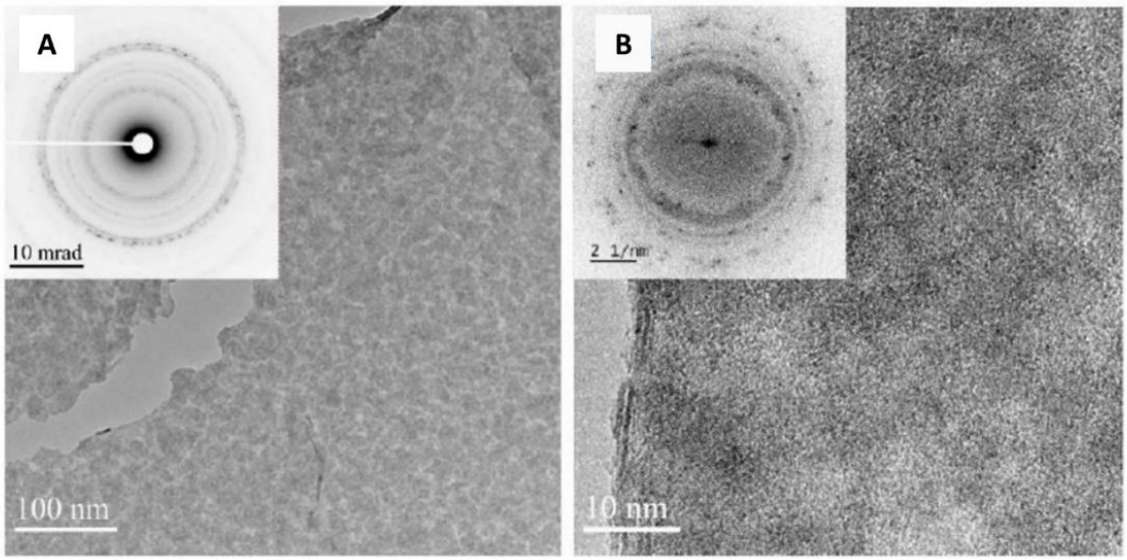

Figure A1.2 TEM images of 1T- $MoTe_2$ inset with selected area electron diffraction (A) collected with a nominal 40 cm cameral length and (B) Fourier transform.

Figure A1.2 displays test results indicating that the as-prepared 1T-$MoTe_2$ films are polycrystalline with a domain size of approximately 10 nm. This was confirmed by electron diffraction patterns of selected regions, which displayed a series of diffraction rings instead of spots.

A2 Fabrication Process Lists

1. Clean SiO_2/Si substrate by ultrasonication in acetone for 10mins, followed by isopropanol for 10 mins. Dry clean with N_2 gun for following fabrication.
2. O_2 plasma clean with 100mW for 3min to remove remaining surface moisture.

3. Prebake substrate with hot plate at 180 degrees for 5min to remove other contamination.
4. Spin coat LOR3A onto substrate at 6000rmp for 30s.
5. Hard bake substrate with LOR 3A at 180 degrees for 5min
6. Allow substrate to cool for 30s.
7. Spin coat Shipley 1815 onto substrate with 4000rmp for 60s.
8. Hard bake the substrate at 115 degrees for 3min.
9. Allow substrate to cool for 30s.
10. Expose substrate using mask aligner 6 for 3s.
11. Develop using CD-26 photoresist develop for 1min 15s.
12. Rinse substrate in RO water.
13. Dry clean substrate with N_2 gun.

A3 Back-gate of $MoTe_2$ FET fabrication process

1. Spin LOR3A onto substrate.
2. Float the substrate on to the HF solution for removing the backside SiO_2.
3. Rinse substrate in RO water.
4. Dry clean with N_2 gun
5. Metallization the gate metal
6. Drop Ag DAG onto the Cu foil.