Simulation, fabrication and characterisation of III-V photodetectors

Cristina Martínez Oliver

Submitted in fulfilment of the requirements for the

Degree of Doctor of Philosophy

School of Engineering

College of Science and Engineering

University of Glasgow

October 2024

Abstract

Photonic Integrated Circuits (PICs) are set to revolutionise optical communication and sensing technologies by enabling the integration of optical interconnects directly into electronic chips, which can significantly reduce the power required to transmit data. Currently, electrical interconnects suffer losses ranging from 50% to 80% due to thermal dissipation, which can be mitigated with existing Mach-Zehnder optical modulators that are already on the market. These modulators are millimetre-scale devices, consuming energy in the picojoule per bit range. However, by leveraging devices in the micrometre to nanometre scale, power consumption can potentially be reduced by a factor of 1,000, achieving levels in the attojoule per bit range [1]. A key challenge in the development of PICs is the integration of efficient and high-performance devices such as photodetectors, particularly those based on III-V semiconductors for near-infrared (NIR) applications, onto silicon platforms.

This thesis explores the integration of III-V nanowire photodetectors on silicon substrates using Template-Assisted Selective Epitaxy (TASE), a technique that offers precise control over nanowire placement and geometry, making it highly suitable for PIC applications. The research presented herein covers the entire spectrum of work from simulation to fabrication, followed by a detailed electrical and optical characterisation to evaluate device performance.

This project began with device simulations using the Sentaurus TCAD software, with which a comprehensive study of III-V materials was conducted. The heterostructure (n-InP/i-InGaAs/p-InP) emerged as the most suitable material combination for photodetectors' optical performance optimisation, outperforming simpler heterostructures such as pure InP and InGaAs. A secondary study examined the effects of mid-bandgap traps within the devices, and showed how the variability in current-voltage (I-V) curves is highly dependent on the position and concentration of these defects, highlighting their significant impact on device characteristics. The simulations were then used to analyse the electrical behaviour of the fabricated devices and address the observed variability in their I-V characteristics.

Following the simulation phase, photodetectors were fabricated with a focus on optimising critical steps such as material growth and doping techniques. The electrical characterisation of these devices revealed substantial variability in I-V characteristics across different devices, a consequence largely attributed to the crystallographic orientation of the silicon substrate used in their fabrication. This variability presents significant challenges for achieving reliable comparisons between devices, highlighting the need for meticulous control over fabrication steps and the importance of selecting the appropriate substrate to achieve consistent and reliable device performance.

The following optical characterisation aimed to study the influence of design variations on device responsivity after light-coupling through a waveguide, marking a step toward their integration into a full optical link. However, the high variability found in the electrical characterisation led to a shift in focus for this work. The subsequent optical study, where the devices were optically characterised at low temperatures for potential use in quantum technologies, a thermal anomaly was observed in which measurements on a 300 nm wide device, down to 5 K, showed an unexpected increase in dark current below 200 K. This was explained through the presence of defects in the devices. An optical anomaly was also observed, requiring further research and explanation which is outside the scope of this thesis.

The findings of this work provide important insights into the challenges and potential solutions for integrating III-V photodetectors into silicon-based PICs, contributing to the advancement of optical communication.

Acknowledgements

This Thesis is part of the “Defect Simulation and Material Growth of III-V Nanostructures - European Industrial Doctorate” (DESIGN-EID) program that has received funding from the European Union’s Horizon 2020 research and innovation programme under the Marie Skłodowska-Curie grant agreement No 860095.

I would like to express my sincere gratitude to my two supervisors, Professor Vihar Georgiev and Professor Kirsten Moselund, for their guidance and support throughout this project. It has been a great privilege to work with such outstanding scientists over the past years, and I could not have done it without them.

I would also thank the rest of the DESIGN consortium, including supervisors Heinz Schmid, Marilyne Sousa and Soren Smidstrup, and students Enrico Brugnolotto and Christian Dam Vedel. It was a pleasure collaborating with and learning from all of you.

Special thanks go to Professor Young and Doctor Millar, who served as examiners during my viva, for reviewing my thesis and providing invaluable feedback.

The opportunity to work and live in two different countries enriched this PhD experience, making it more diverse and rewarding. Along the way, I met many wonderful people and was fortunate to form lasting friendships with many of them

I extend my gratitude to the Device Modelling group, now called Deep Nano, at the University of Glasgow. Finally sharing an office space after having only seen each other remotely during COVID made the writing of this thesis much more bearable.

My deepest thanks go to the IBM Research lab in Zurich, specially the QTP and PSI groups. The conversations and shared breaks made this PhD journey truly memorable. I would like to particularly acknowledge Markus Scherrer, Simone Iadanza, Myriam Rihani, Isabel Bollier, Jakub Dranczewski and Anna Fisher for the productive discussions and their willingness to lend a hand whenever needed.

Special mention to Doctor Heike Riel, team leader and manager of the whole Science of Quantum and Information Technology department at IBM, for her interest and support in my research.

Also thank the Cleanroom Operations Team of the Binning and Rohrer Nanoscience Centre for their help and support during the fabrication performed at IBM.

To my international friends from the Master's programme, thank you for our yearly reunions across Europe. Learning about your research and industrial careers has been a great inspiration for my own journey.

I would also like to mention my lifelong friends back home, for always encouraging me and motivating me to finish so that I can return. Although we see each other less often now, whenever we reunite, it feels as though no time has passed.

Lastly, my heartfelt thanks go to my family—my parents and brothers—for their constant support from afar. Your efforts to understand my research, little by little each time, have been one of the many ways you've shown your love and support throughout this long journey I embarked on.

Ian, thank you for always pushing me to be the best version of myself, for offering advice, and for thinking ahead on everything important to succeed in this PhD journey. You've kept me going through the toughest moments, and I will be forever grateful.

Table of Contents

Abstract ... **ii**

Acknowledgements ... **iv**

List of publications ... **viii**

List of Tables ... **x**

List of Figures ... **xi**

Declaration ... **xxi**

Abbreviations ... **xxii**

1. Introduction ... **1**

1.1. Project description ... 1

1.2. Literature review ... 2

1.3. Semiconductors ... 8

1.4. Photodetectors ... 11

1.4.1. III-V photodetectors ... 17

2. TCAD simulations ... **19**

2.1. Overview of Sentaurus Tools ... 21

2.2. Materials study ... 27

2.3. Study on traps ... 32

3. Fabrication of III-V photodetectors ... **39**

3.1. III-V on Si integration techniques ... 40

3.1.1. Heterogeneous integration ... 42

3.1.2. Monolithic integration ... 43

3.2. Monolithic integration of InP/InGaAs photodetectors by TASE ... 46

3.2.1. Materials growth ... 59

3.2.2. Zinc diffusion optimisation ... 62

4. Photodetectors' characterisation ... **70**

4.1. Electrical measurements ... 70

4.1.1. Matching simulations ... 73

4.2. Optical characterisation 82
4.2.1. Free-space illumination 86
4.2.2. Waveguide coupled 87
4.2.3. Low temperature measurements 93

5. Summary and Outlook 102

5.1. Future directions 109

6. Bibliography 111

List of publications

- **Journal articles**

C. Martinez-Oliver, M. Scherrer, S. Iadanza, H. Schmid, K. Moselund and V. Georgiev, “Simulation and Fabrication of Monolithic III-V Photodetectors on Si: the Role of Growth Facets and Localization of Heterojunctions,” IEEE Transactions on Electron Devices, vol. 71, no. 10, pp. 6124-6130, 2024. DOI: 10.1109/TED.2024.3437333

- **Conference proceedings**

C. Martinez-Oliver, K. E. Moselund and V. P. Georgiev, “Evaluation of material profiles for III-V nanowire photodetectors,” in 2021 International Conference on Numerical Simulation of Optoelectronic Devices (NUSOD), Turin, Italy, 2021. DOI: 10.1109/NUSOD52207.2021.9541533

- **Attended conferences**

  - Presentation

2021 International Conference on Numerical Simulation of Optoelectronic Devices (NUSOD), online

2023 Fall Meeting of the European Materials Research Society (E-MRS) in the University of Technology in Warsaw (Poland), “Monolithic integration of waveguide-coupled III-V photodetectors on silicon”

  - Poster

2022 NanoPhoton conference on fundamentals and applications of semiconductor nanocavities, in Copenhagen (Denmark)

- **Summer schools**

  - Presentation

  2022 SiNANO Modelling and Simulation Summer School in the University of Glasgow (Scotland, UK)

  - Poster

  2023 Nanophotonics and its Applications for Society Summer School in École Polytechnique Fédérale de Lausanne (EPFL), Switzerland

- **Under preparation**

  2024 Annual IEEE International Electron Devices Meeting (IEDM) in San Francisco, California, “Ultra-Low Temperature Characterization of Fully-Integrated III-V Photodetectors for Quantum Networks”

List of Tables

Table 1-1. List of semiconductor materials typically used in optoelectronic applications with their band gap type and energy in μm at room temperature. 8

List of Figures

Fig 1-1. Band gap (eV) of III-V materials with their lattice constant. The lines joining the binary compounds represent the respective ternary and quaternary compounds, which can have direct (solid line) or indirect (dashed line) band gaps. Figure modified (coloured and $In_{0.53}Ga_{0.47}As$ added) from [44], reproduced with permission from Springer Nature.....10

Fig 1-2. Absorption coefficients versus wavelength for some semiconductor materials. Figure modified (coloured) from [45], reproduced with permission from Springer Nature. 10

Fig 1-3. Schematic of the behaviour inside a p-n diode as photons are absorbed, generating electron-hole pairs in the different regions. 12

Fig 1-4. Typical current-voltage (I-V) curve for a diode. The black curves correspond to the characteristics of a device without light, while the coloured curves correspond to the characteristics when light is applied, increasing its intensity. On the left the curves have been plotted in linear scale, while on the right the modulus of the current has been plotted in logarithmic scale for a better visualisation of the current values at reverse bias. 14

Fig 1-5. Responsivity of some photodetectors compared with an ideal quantum efficiency one (η=100%). Figure from [45], reproduced with permission from Springer Nature.....16

Fig 2-1. Diagram of the Synopsys Sentaurus TCAD tools organised based on their specific functions. 20

Fig 2-2. Screenshot of Sentaurus Workbench displaying the toolbar buttons, the organisation of projects, and an open project with various tools and parameters arranged in a family-tree view. 21

Fig 2-3. Results of SNMESH simulations of a Delaunay mesh, composed of tetrahedra (left) and of a tensor-product mesh, composed of cuboid elements (right). 23

Fig 2-4. Screenshot of Sentaurus Visual user interface with various 3D, 2D and 1D plots of a p-i-n III-V device.....26

Fig 2-5. Top: sketch of the simulation domain showing the p-i-n diode geometry with dimensions x = 220 nm, y = 1000 nm and z = 200 nm, the metal contacts, transparent to the light, the SiO_2 BOX and the Si substrate. The source of light has been added to the top to visualise the simulation setup. Bottom: optical generation-coloured plots for the fully InP device, the fully InGaAs device and the InP/InGaAs/InP heterostructure, for wavelengths of 800 nm, 1100 nm and 1300 nm [59] reproduced with permission © 2021 IEEE.....28

Fig 2-6. Current in linear (top) and logarithmic (bottom) scale as a function of the wavelength for the fully InP device, the fully InGaAs device and the InP/InGaAs/InP heterostructure [59] reproduced with permission © 2021 IEEE.....29

Fig 2-7. Current response in a) linear and b) logarithmic scale as a function of the laser power for the fully InP device, the fully InGaAs device and the InP/InGaAs/InP heterostructure, for wavelengths of 800 nm and 1300 nm. 30

Fig 2-8. Simulated I-V curves at four different laser powers and two different wavelengths a) for the three studied structures (InGaAs and InP homojunctions and InP/InGaAs/InP heterostructure) and b) comparing them with silicon instead of InP.....31

Fig 2-9. Top row: the band diagrams for the three nanowires along the length of the devices. Middle row is their electron density. Bottom row is the hole densities. All simulations are presented at -2 V of applied bias [59] reproduced with permission © 2021 IEEE.....32

Fig 2-10. I-V characteristics of a fabricated photodiode (solid lines) in the dark (brown) and with different laser powers applied. Simulated I-V characteristics of an ideal photodiode (dotted lines) in the dark (brown) and with different laser powers applied. 33

Fig 2-11. a) Image of a section of the simulated NW where the surrounding oxide is in transparent blue and the mesh can be seen on the NW regions (blue for p-InP, yellow for i-InGaAs and red for n-InP) and on the metal contacts. b), c) and d) Comparison of the experimental I-V curve without applied light (black) and the I-V curves for the simulated devices with different concentrations of b) bulk traps, c) interface traps and d) surface traps. 34

Fig 2-12. I-V curves from experimental (black) and simulated devices with no traps (yellow), and different locations of traps: a) the top surface of the device on the interface with the oxide around it (orange), the bottom surface of the device on the interface with the oxide around it (pink), both top and bottom surfaces (red), b) in the bulk of the device (blue), on the interfaces between the InP and the InGaAs (green), both on the bulk and the interfaces (cyan), c) both bulk and surfaces with a concentration of 1e13 cm^{-3} and 1e13 cm^{-2} respectively (light purple) and with a concentration of 1e14 cm^{-3} and 1e14 cm^{-2} respectively (dark purple), and d) with bulk, interface and surfaces traps altogether, with concentrations of 1e13 cm^{-3} and 1e13 cm^{-2} respectively (light brown) and with concentrations of 1e14 cm^{-3} and 1e14 cm^{-2} respectively (dark brown), as specified in the legends. 35

Fig 2-13. I-V curves with increasing laser power from a) experimental and b) - d) simulated devices with different location of traps: b) bulk (1e13 cm^{-3}), c) interface (1e13 cm^{-2}) and d) surface (1e10 cm^{-2}).....37

Fig 2-14. Comparison of the experimental I-V curve without applied light (black) and the I-V curves for the simulated devices with different concentrations of bulk and surface traps. 37

Fig 3-1. Schematic of antiphase boundaries defects at atomic steps of the Si substrate. Figure modified (cropped) from [69] under the terms of the CC BY 4.0 license [70].....41

Fig 3-2. Schematic of some integration techniques of III-V on Si. The heterogeneous integration techniques include wafer bonding, die bonding and transfer printing. The monolithic integration techniques include buffered layer, selective area growth (SAG), and aspect ratio trapping (ART).....42

Fig 3-3. a) Demonstration of TASE's capabilities shown through Scanning Electron Microscopy (SEM) images. Figure modified (cropped) from [50], with permission from the Copyright Clearance Centre. b) False-coloured SEM of the top view of a p-i-n nanostructure, with the colours on the device referring to the different doped regions, and a bright field Scanning Transmission Electron Microscopy (STEM) image of a cross section of the nanostructure below. Figure modified (cropped) from [48], under the terms of the CC BY 4.0 license [70]. 45

Fig 3-4. Schematic of the steps for the fabrication of photonic devices using TASE. The different steps include (1) silicon patterning of the top layer of an SOI wafer, (2) silicon oxide deposition, (3) window opening on one end of the silicon shape, (4) etch of the silicon leaving a seed, (5) growth of the III-V materials, and (6) deposition of the metal contacts after a second window opening on the other end of the device. 47

Fig 3-5. Images from L-edit software of the design of the devices. a) Straight and funnel devices with the lowest (20 nm) and highest (600 nm) values of width. b) Three joined funnel devices and five joined straight devices. c) Design of the contacts with 2 and 3 pads and a contacted NW. d) Design of the waveguide coupled devices with tapered and non-tapered waveguides and different mirror designs (a low-contrast Bragg grating, a high-contrast Bragg grating, and a demi Zone-Plate). 49

Fig 3-6. SEM images of a) a straight and b) a funnel NWs and c) the test structures after the Si patterning step.....51

Fig 3-7. Schematic of the resulting SiO_2 layers deposited by ALD (left), PECVD with silane (SiH4) precursor (centre) and PECVD with tetraethoxysilane (TEOS) precursor (right). ..51

Fig 3-8. SEM images of the WG coupled Si structures with a layer of ALD SiO_2 around. 52

Fig 3-9. SEM images of two buried Si structures with the template opening hole. 53

Fig 3-10. SEM images of the empty templates (dark) after the Si etch back. The lighter area corresponds to the remaining Si used for the nucleation of the III-V materials. 54

Fig 3-11. SEM (a-f) and EDX (g-h) images of p-InGaAs/p-InP/i-InGaAs/n-InP/InGaAs-seed NWs of different lengths and widths. Phosphorus is indicated in green, representing the InP regions, arsenic in red, and gallium in blue, with the red and blue areas collectively representing InGaAs. 56

Fig 3-12. SEM (a-c) and EDX (d) images of the final steps of the two-step growth method to fabricate funnel-shaped devices, with the arrows indicating the growth directions. a) Corresponds to the covering of the first template opening hole by ALD, b) shows the second template opening and etching of the remaining Si, c) is after the second growth process, and d) shows the different materials on a fully grown device, with phosphorus indicated in green, representing the InP regions, arsenic in red, and gallium in blue, with the red and blue areas collectively representing InGaAs. 57

Fig 3-13. SEM (a-c) and optical microscopy (d) images of the steps to contact the fabricated devices. a) Corresponds to the EBL step to define the contacting holes after thinning the whole sample down, b) is after the RIE step to expose the III-V materials, c) and d) show an SEM and an optical microscopy image after the metal contacts have been deposited. 59

Fig 3-14. SEM images of III-V nanowires, a) with Sn doped InP, b) with i-InGaAs, c) with Zn doped InP and d) with Zn doped InGaAs. 60

Fig 3-15. Linear scale I-V characteristics of selected p-InGaAs nanowires with different widths, b) being a zoomed in version of a). 61

Fig 3-16. Schematic of the fabrication process for the Zn-diffusion sample. 62

Fig 3-17. Images from L-edit software; a) and b) from the holes and c) and d) from the TLM bars. The pink areas correspond to the patterning of the SiO_2 (i.e. the areas with exposed InGaAs). The golden rectangles correspond to the metal contacts' layer. 63

Fig 3-18. SEM images of a) - d) the patterned holes with different sizes and separations and e) a TLM bar. 63

Fig 3-19. SEM images of a) a pair of holes and b) a TLM bar, after Zn diffusion in As atmosphere at 510 ºC after annealing at 650 ºC. 64

Fig 3-20. SEM image and EDX analysis for As, In and Zn for the first Zn diffused sample. 65

Fig 3-21. SEM images of the holes on the sample annealed at a) - b) 650 °C, and c) - d) 600 °C under an As atmosphere and no Zn diffusion. 65

Fig 3-22. a) and b) SEM images of the holes' surfaces after the Zn diffusion at 510 ºC with an optimised annealing temperature of 600 ºC. c) and d) I-V curves of two pairs of contacted holes with their respective SEM images. 66

Fig 3-23. a) Current at 2 V versus the holes' separation, and b) the results of the TLM measurements on the bars with different widths (W) to obtain the contact resistance of the doped InGaAs. 67

Fig 3-24. EDX of the sequence growth for three nanowires with three different widths: a) 500 nm, b) 400 nm, and c) 200 nm. Phosphorus is indicated in green, representing the InP regions, arsenic in red, and gallium in blue, with the red and blue areas collectively representing InGaAs. 68

Fig 4-1. a) Experimental I-V curves from the measured NW devices in dark current [125] reproduced with permission © 2024 IEEE. A cut-off in current density is set to 105 A/cm^2 during measurement to avoid damaging the small devices. b) Current density values extracted from (a) at a voltage value of -1 V, plotted against the device width for better visualisation. 71

Fig 4-2. a) Expected growth fronts of III-V materials on a (001) SOI wafer [125] reproduced with permission © 2024 IEEE. b) Coloured top-view SEM images of fabricated devices with different widths (100 to 600 nm) with the metal contacts (Ni/Au) incorporated.....72

Fig 4-3. a) Simulated I-V curves for devices with different widths (100 to 600 nm) and different growth facets. b) Current density values of the devices for the expected growth fronts, shown in its legend, extracted from (a) at a voltage value of -2 V, with respect to the width for better visualisation, [125] reproduced with permission © 2024 IEEE.....74

Fig 4-4. Simulated I-V curves for devices with the InGaAs shifted from the n-contact to the p-contact, as illustrated on the 3D plots next to the main graph. An inset of the experimental curves is provided for comparison. Colour 2D plots (right) show the hole current density at -2 V when the InGaAs is on the n-side, and the electron current density at -2 V across the entire range of InGaAs positioning [125] reproduced with permission © 2024 IEEE. 75

Fig 4-5. On the left are the coloured top-view SEM images. The colours indicate the position of the junction at the top of the device, which may be tilted towards the substrate and thus not be visible in a top-view EDX. On the right are the highlighted respective I-V curves of the devices shown in the SEM images on the left [125] reproduced with permission © 2024 IEEE. 77

Fig 4-6. a) Experimental I-V curves coloured with respect to the length of the measured devices [125] reproduced with permission © 2024 IEEE. b) Current density values extracted from (a) at a voltage value of -1 V, plotted against the device length for better visualisation. 78

Fig 4-7. TEM images of the cross section of the n-InP/i-InGaAs/p-InP/p-InGaAs fabricated devices a) on a (001) SOI platform showing different crystals and changes of orientation within the device and b) on a (110) SOI platform showing straight facets all along the device. 79

Fig 4-8. I-V characteristics of 100 devices grown a) on a (001) SOI wafer and b) on a (110) SOI wafer. The colours correspond to the width of the devices. 80

Fig 4-9. SEM images of the test structures from a grown sample in a) a (001) SOI wafer and b) a (110) SOI wafer. 80

Fig 4-10. Simplified schematic of the optical setup used for the electro-optical measurements. The orange light path corresponds to the imaging of the sample under white light illumination while the red path corresponds to measurement of the photoluminescence (PL) signal. The excitation lasers are coupled into the setup through fibres. Inside the cryostat, an objective focuses light onto the sample. 83

Fig 4-11. Photoinduced I-V characteristics for free-space illuminated devices at room temperature for increasing laser powers shown by the multicoloured arrow at a) $\lambda = 1100$ nm (up to ~60.8 μW) and b) $\lambda = 1500$ nm (up to ~2.22 μW) for a 600 nm wide device, and c) $\lambda = 1350$ nm (up to ~1.97 μW) and d) $\lambda = 1550$ nm (up to ~1.76 μW) for a 400 nm wide device. 86

Fig 4-12. Simulated wavelength response of the grating coupler design in transmission (blue) and reflection (red). Note the different ranges on the two y-axis. 88

Fig 4-13. SEM images of the waveguide coupled devices: a) and b) without a back-reflecting mirror, a) a 300 nm wide NW with a straight WG and b) a 100 nm wide NW with a tapered WG. c) Show 300 nm wide devices with a low-contrast Bragg grating, d) with a high-contrast Bragg grating, and e) - f) with a demi Zone-Plate with different magnification values. 88

Fig 4-14. a) Wavelength response plot of a waveguide coupled device. The polarisation of the fiber has been aligned to get a maximum light response of the device at 1300 nm (blue) and at 1550 nm (purple). On the right, infrared camera images of the devices response to coupled light with b) a 1550 nm and c) a 1300 nm wavelength. 89

Fig 4-15. Photoinduced I-V characteristics at room temperature for a straight waveguide coupled 100 nm wide device without back-reflection for increasing laser powers shown by the multicoloured arrow at a) λ = 1200 nm, b) λ = 1300 nm, c) λ = 1450 nm, d) λ = 1550 nm. 90

Fig 4-16. I-V curves at room temperature for straight waveguide coupled 100 nm wide devices for increased laser power at 1310 nm (left column) and 1550 nm (right column) for straight waveguide coupled devices with a) and b) no back-reflecting mirror, c) and d) a low contrast Bragg grating, e) and f) a high-contrast Bragg-grating, and g) and h) a demi Zone-Plate. The 100% power out of the fiber at 1310 nm is 119 μW and at 1550 nm is 106 μW. 92

Fig 4-17. Dark current I-V characteristics for a 100 nm wide device at temperatures that go from 300 K to 80 K. 94

Fig 4-18. Arrhenius plot for the 100 nm wide devices. The different curves correspond to the current values extracted at different reverse voltages. The temperatures range from 80 K to 300 K. The inset displays the activation energy versus the voltage, extracted from the slope of fitting the data. 95

Fig 4-19. I-V curves for increased laser power at 80K for a straight waveguide coupled 100 nm device with no back-reflecting mirror at a) 1300 nm and b) 1550 nm. 96

Fig 4-20. I-V characteristics at temperatures ranging 5 K to 300K for a 300 nm wide device a) in dark current and b) in photocurrent illuminating it from the top with light with a 1550 nm wavelength and 100% of laser power. 97

Fig 4-21. Dark-current density (blue) and photocurrent density (red) at -1 V of applied voltage with respect to the temperature, from the data in Fig 4-20. The vertical lines group the measurements performed on different days. Note the different ranges on the two y-axis. 97

Fig 4-22. Dark resistivity of InGaAs with temperature. The y axis shows the ratio between the resistivity at a temperature T and the resistivity at 300 K [135], reproduced with permission from Springer Nature. 99

Fig 4-23. Normalised current values over the dark current for a power sweep (0% - 20%) at a 1550 nm wavelength for temperatures ranging from 5 K to 300 K, specified in the legend. 100

Fig 4-24. Normalised current values over the dark current for a power sweep (0% - 20%) at 30 K for wavelengths ranging from 1250 nm to 1700 nm, specified in the legend. 100

Fig 5-1. a) Simulated I-V curves at four different laser powers and two different wavelengths for the three studied structures (InGaAs and InP homojunctions and InP/InGaAs/InP heterostructure). b) I-V curves from experimental (black) and simulated devices with many different locations of traps, specified in the legend. 103

Fig 5-2. a) and b) I-V curves of two pairs of contacted holes with their respective SEM images for the study of Zn doping diffusion. c) – e) EDX of the sequence growth for c) – d) two straight nanowires with different widths and e) a funnel-shaped device. Phosphorus is indicated in green, representing the InP regions, arsenic in red, and gallium in blue, with the red and blue areas collectively representing InGaAs 104

Fig 5-3. On the left are the coloured top-view SEM images. The colours indicate the position of the junction at the top of the device, which may be tilted towards the substrate and thus not be visible in a top-view EDX. On the right are the highlighted respective I-V curves of the devices shown in the SEM images on the left [125] reproduced with permission © 2024 IEEE. 105

Fig 5-4. a) - b) TEM images of the cross section of fabricated devices and c) - d) I-V characteristics of 100 devices, grown a) and c) on a (001) SOI platform, and b) and d) on a (110) SOI platform. The colours of the I-V curves correspond to the width of the devices. 106

Fig 5-5. a) – b) Photoinduced I-V characteristics at room temperature for free-space illuminated 400 nm wide device for increasing laser powers at a) λ = 1350 nm (up to ~1.97 µW) and b) λ = 1550 nm (up to ~1.76 µW). c) – d) Photoinduced I-V characteristics at room temperature for a straight waveguide coupled 100 nm wide device without back-reflection for increasing laser powers at c) λ = 1300 nm and d) λ = 1550 nm.....107

Fig 5-6. a) Arrhenius plot for the 100 nm wide devices. The different curves correspond to the current values extracted at different reverse voltages. The temperatures range from 80 K to 300 K. The inset displays the activation energy versus the voltage, extracted from the slope of fitting the data. b) Dark-current density at -1 V of applied voltage with respect to the temperature for a 300 nm wide device. The vertical lines group the measurements performed on different days. c) - d) Normalised current values over the dark current for a power sweep (0% - 20%) c) at a 1550 nm wavelength for temperatures ranging from 5 K to 300 K, and d) at 30 K for wavelengths ranging from 1250 nm to 1700 nm, specified in the legend. 108

Declaration

I declare that, except where explicit reference is made to the contribution of others, this dissertation is the result of my own work and has not been submitted for any other degree at the University of Glasgow or any other institution.

Printed name: Cristina Martínez Oliver

Abbreviations

η Quantum efficiency

λ Wavelength

ρ Responsivity

BOX Buried Oxide

CMOS Complementary Metal Oxide Semiconductor

E_g0 Band gap energy at 0K

e^--h^+ Electron-hole pair

EMW Electromagnetic Wave Solver

ESR Early-Stage Researcher

FDTD Finite-Difference Time-Domain

GU University of Glasgow

IBM International Business Machines Corporation

IR Infrared

I-V Current-voltage

NIR Near-infrared

NW Nanowire

PD Photodetector

PIC Photonics Integrated Circuit

PL Photoluminescence

RC Resistance - Capacitance, circuit's time constant

SDE Structure Device Editor

SDEVICE Sentaurus Device

SRH Shockley-Read-Hall

SNMESH Sentaurus Mesh generator

SNR Signal-to-Noise Ratio

SOI Silicon on Insulator

SVISUAL Sentaurus Visual

SWB Sentaurus Workbench

TCAD Technology Computer-Aided Design

TLM Transfer Length Method

WG Waveguide

Elements, Chemicals, and Materials

AlAs Aluminium arsenide

AlGaAs Aluminium Gallium Arsenide

As Arsenic

Au Gold

BHF Buffered Hydrofluoric acid

CSAR Chemical Semi-Amplified Resist

DEZn Diethyl zinc

DHF Diluted Hydrofluoric Acid

GaAs Gallium Arsenide

GaN Gallium Nitride

Ge Germanium

H_2O_2 Oxide Peroxide

H_2SO_4 Sulfuric acid

HBr Hydrobromic Acid

Hex-SiGe Hexagonal Silicon Germanium

HSQ Hydrogen Silsesquioxane

InAs Indium Arsenide

InP Indium Phosphide

InSb Indium Antimonide

InGaAs Indium Gallium Arsenide

Ni Nickel

O_2 Oxygen

PMMA Polymethyl methacrylate

Si Silicon

SiH_4 Silane

SiO_2 Silicon oxide

Sn Tin

TBAs Tert-butyl arsine

TBP Tert-butyl phosphine,

TEOS Tetraethoxysilane

TESn Tetraethyl tin

TMAH Tetramethylammonium hydroxide

TMGa Trimethyl gallium

TMIn Trimethyl indium

Zn Zinc

W Tungsten

Characterisation and Fabrication Techniques

ALD Atomic Layered Deposition

ART Aspect Ratio Trapping

EBL Electron Beam Lithography

EDX Energy Dispersive X-ray Spectrometer

FIB Focused Ion Beam

ICP Inductively-Coupled Plasma

MOCVD Metal-Organic Chemical Vapour Deposition

PECVD Plasma-Enhanced Chemical Vapor Deposition

RIE Reactive Ion Etching

RTA Rapid Thermal Annealing

SAG Selective Area Growth

SEM Scanning Electron Microscopy

STEM Scanning Transmission Electron Microscopy

TASE Template-Assisted Selective Epitaxy

TEM Transmission Electron Microscopy

1. Introduction

1.1. Project description

This PhD is part of a Marie-Curie project that includes three Early-Stage Researchers (ESRs) and three institutions; University of Glasgow (GU), IBM Research Zurich and Synopsys. All the ESRs spent approximately a third of the time in GU and the remainder in one of the other institutions. I carried out my research in GU for the first 14 months, and in IBM for the following 26 months (22 months + 4 months of extension).

The whole project is titled "Defect Simulations and Material Growth of III-V Nanostructures" and is a European Industrial Doctorate. Its main objective was to study the defects in III-V semiconductors and try to exploit them in the development of novel devices or, at least, to mitigate their deteriorating impact on electro-optic device performance. Each ESR had their own PhD project with a defined role to achieve this overall objective. ESR1, Enrico Brugnolotto, focussed on the growth of III-V materials in confined templates and did the experimental analysis of crystalline defects, strain, and composition intermixing occurring during growth at heterointerfaces in quantum confinement structures. I am ESR2 and my role has been to optimise the detector's structure, such as the specific materials used via TCAD simulations and analysis in the University of Glasgow, and to fabricate and characterise the devices electrically and optically at IBM. My personal goal has been to obtain statistical data about the devices' behaviour and use the initial simulations to study the effect of the different parameters involved on their final characteristics. ESR3, Christian Dam Vedel, was responsible for simulating III-V defects using first-principle methods, bridging the gap between Technology Computer-Aided Design (TCAD) simulations and first-principles in the context of these defects.

1.2. Literature review

The amount of information being transmitted around the world has increased the quantity and density of electronics required, which has resulted in an energy problem due to the thermal losses in electrical interconnects ranging from 50% to 80% of their energy consumption. Due to the emergence of cloud services, big data and e-commerce, data centres have become some of the biggest users of electricity [2]. The relatively poor performance of metal interconnects is limiting energy efficiency, as parasitic capacitances and energy dissipation dominate electronics' efficacy [3]. As electrical lines are scaled down, their performance degrades due to increased complexity, making it challenging for them to match the scaling of individual electrical devices like transistors, which continue to follow Moore's law [4]. Therefore, the performance of electrical chips is restricted by this so-called electrical interconnect bottleneck.

The high bandwidth potential of optical interconnects has already been exploited in large area networks. For several decades, optical fibres have been replacing copper lines in long distance telecommunications allowing for multiple signals to be sent through a single fibre network by wavelength transmission multiplexing.

However, electrical interconnects still dominate on-chip wiring. The advantages of integrated optics at this level can overcome the interconnect bottleneck problem, enabling low power data transmission. For this reason, the research on complementary metal oxide semiconductor (CMOS) compatible nanoscale photonic devices to achieve chip level optical interconnect has great importance. In addition to increasing bandwidth and reducing power consumption, the high-speed data transmission capabilities of optics would significantly benefit the efficiency of electronic computation.

Achieving effective optical interconnects requires several key components. Optical modulators have already demonstrated energy efficiency, but implementing optical memory poses challenges due to the nature of light. Nonetheless, some advancements have been made using phase-change materials. Another essential component is the optical link itself.

A photonic integrated circuit (PIC) relies on an optical link, which consists of three main components; an electrical-to-optical converter (i.e. a light source, emitter or laser), a waveguide (WG) to transmit the optical signal through the chip, and an optical-to-electrical converter (i.e. a photodetector). The first and last components are critical limiting factors in achieving energy-efficient computation through optoelectronics, as they tend to lose the most energy and must be scaled down to minimise energy consumption.

The performance of an optical link depends on several critical factors. First, it must offer a high bandwidth to support high data transfer rates in communication systems, and a low power consumption for on-chip and chip-to-chip communications, where heat dissipation is a challenge. Latency is another important aspect; an optical link must have low latency to ensure minimal delay in data transmission for real-time application. To ensure a clean signal transmission with minimal interference, which is vital for reducing errors and preserving data integrity, an optical link must also have a high signal-to-noise ratio whilst maintaining a high sensitivity to detect weak optical signals with minimal loss. As the demand for data transmission grows, the optical link must also be scalable. This scalability is enabled through techniques like wavelength-division multiplexing, which allows multiple data streams to be sent simultaneously at different wavelengths, increasing the capacity of the system.

In terms of materials, those used for optical links must be compatible with CMOS processes for widespread implementation, as it allows for integration into standard manufacturing lines. Both photodetectors and lasers require an active material for efficient absorption and emission of light, while the waveguide material needs to be transparent to the working wavelength.

Extensive research into silicon (Si) and its optical properties has established it as the preferred material for passive optical components. Silicon has been widely used in electronics and is cheap and abundant, making it the perfect candidate for such applications. Given silicon's optical properties and low-loss characteristics, it emerged as the preferred material for developing devices including lasers [5], modulators [6], and photodetectors in the visible region [7]. For near-infrared (NIR) applications above 1100 nm wavelength, Si becomes transparent, making it an ideal material for waveguides and enabling significant advancements in scaling optical links [8].

The Silicon on Insulator (SOI) platform for electronics further supports its use in waveguides, as it can strongly confine light when insulated by silicon oxide (SiO_2). While Si optics offer many advantages, including a bandwidth increase, high-speed data transmission for datacom and telecom bands, and the ability to use complementary metal oxide semiconductor (CMOS) process-compatible fabrication technologies, this transparency also makes it unsuitable as an active material in photodetectors within PICs. This limitation provided researchers motive to further investigate other materials [9].

The ultimate limit of the energy a photodetector needs for operating is limited by its capacitance, except in the quantum regime, where the limit is set by shot noise. The reduced size of on-chip devices would allow for low capacitances, i.e., low power communication. Additionally, a reduced capacitance means a lower RC (resistance - capacitance) time and an increase in the RC limited frequency response. The challenge to reach this goal lies in the need for a material with a high absorption coefficient to achieve high optical absorption despite the reduced dimensions of the photodetector. Similarly, light sources' energy consumption scales with the device size but need the energy density of the electromagnetic field, which provides the energy for the light emission, to be highly overlapped with the gain material, which will amplify the light. This sets the requirement for high optical gain and confinement.

PICs' components need to be scalable to connect many devices while keeping a low power consumption and providing high bandwidth. Furthermore, they need to be integrated onto CMOS chips which contain mainly Si components, as long electrical connections increase the overall energy budget of the interconnect due to line charge-up. For it to be better than an electrical interconnect, the energy requirement has been identified to be 10fJ/bit [1, 10].

The need to co-integrate different materials to fulfil the different functions of WG (transparency) and detection (absorption), while also being compatible with CMOS, presents a significant challenge. Each individual component requires specific optimisations to achieve high-speed and low-power on-chip optical links.

Existing approaches for integrated detectors for optical communication systems leverage a variety of materials and architectures, from germanium and III-V semiconductors to 2D materials, quantum dots, and plasmonic structures.

State-of-the art high speed photodetectors have predominantly relied on germanium (Ge) or silicon-germanium (SiGe) compounds, largely due to Ge's compatibility with CMOS processes. Scaled Ge photodetectors (PDs) have demonstrated high bandwidth and notable responsivity, enabling baud rates up to 100 GBd [11, 12]. However, the expansion of photonic applications beyond data communication into areas like sensing [13], displays [14], and high-performance computing [15] showed how Ge PDs struggle to meet several of the requirements for these applications.

Ge photodetectors' main limitation is their dark current, which ranges from 10 nA to several microamperes, caused by crystalline defects formed during heteroepitaxy [16]. This high dark current leads to a low signal-to-dark current ratio, often needing amplifying circuits, such as transimpedance amplifiers, to boost the signal. Furthermore, while Ge has a cut-off wavelength of 1800 nm, its absorption coefficient decreases significantly beyond 1550 nm due to its indirect bandgap, making it unsuitable for longer wavelength applications. While efforts have been made to improve Ge-based photodetectors through GeSn alloys [17] and the introduction of strain via SiGe layers [18], challenges related to high dark current and longer wavelength detection persist.

2D materials emerged as promising candidates for optoelectronic device fabrication [19]. Graphene, a 2D material with semi-metallic characteristics and a zero bandgap, attracted considerable attention in photodetection due to its ability to interact with light across a wide range of wavelengths, from terahertz to ultraviolet. However, because graphene is atomically thin, it has a low absorption coefficient, only absorbing about 2.3% of incident light.

Meanwhile, transition metal dichalcogenides (TMDCs) such as MoS_2, WS_2, $MoSe_2$, and WTe_2 offer semiconducting properties and varied bandgaps, making them suitable for optoelectronic applications [20]. For NIR detection, $PtSe_2$ is particularly promising due to its relatively small bandgap [21]. Despite their potential, 2D material-based photodetectors often suffer from performance issues, such as degradation in ambient conditions and slow response times caused by charge trapping, which results in persistent photocurrent after the light source is turned off.

Various III-V van-der-Waals multilayer-structure materials are also being investigated as potential layered photodetector materials, expanding the scope beyond traditional 2D materials. When III-V semiconductors are reduced to two dimensions, they exhibit unique electronic, optical, and structural properties that can enhance their performance in optoelectronic applications [22]. However, these materials are still in their early stages of development, and further research is required to better understand their properties, optimise synthesis methods, and explore their full range of applications.

Quantum dot (QD) photodetectors represent another emerging solution [23]. QDs are promising photoactive materials for infrared photodetectors due to their flexibility, ease of processing, and high absorption coefficients. Traditionally, QDs are composed of heavy metals such as lead (Pb), cadmium (Cd), and mercury (Hg), with common QDs including PbS, PbSe [24, 25], HgS, and HgTe [26, 27]. However, these materials pose toxicity concerns. As a result, researchers are exploring less toxic alternatives, such as I-VI compounds (Ag_2S, Ag_2Se, Ag_2Te) [28, 29], III-V compounds (InP, InAs, InSb) [30], and even graphene quantum dots [31]. Despite their potential, further study is needed to refine their synthesis, characterisation, and performance.

The performance of photodetectors can be significantly enhanced through the use of complex layered structures or advanced designs such as plasmonic nanostructures [32]. Plasmonic PDs, in particular, are engineered to improve light absorption by the mediation of surface plasmon polaritons (SPPs). These are hybrid particles formed by coherent oscillations of free electrons at metal-dielectric interfaces or boundaries, coupled with electromagnetic waves. SPPs enhance the photodetector's response to light typically by exciting resonant modes. These detectors primarily use noble metals, which support strong plasmon resonant modes, facilitating detection through mechanisms like internal photoemission or electron-hole generation.

III–V materials, whether in bulk form, 2D layers, or quantum dots, are highly promising for optoelectronic devices. These materials offer high absorption coefficients and a tunable direct bandgap, thanks to their binary, ternary, and quaternary compositions. This flexibility enables the development of high-performance photodetectors for applications ranging from near-infrared to mid-infrared wavelengths [33, 34]. Moreover, III-V materials are well-suited for use as active optical emitters such as lasers [35, 36] and LEDs [37, 38]. Since III-V compounds are already used as on-chip lasers in silicon photonics, their integration as photodetectors on silicon photonics platforms is a natural progression [39, 40].

This project emerged from the desire to scale and integrate optical devices on silicon CMOS chips to obtain high speed and low power data transmission, for potential future optical on-chip communication. When it comes to the demand for PDs for the near-infrared (NIR) range, the applications are vast, spanning from high-speed data transmission in fiber-optic telecommunications to advanced imaging and sensing technologies. As already mentioned, as electronic circuits reach their physical limits in terms of speed and power consumption, optical interconnects become essential for enabling faster on-chip and chip-to-chip communication. III-V materials, known for their high efficiency in light detection and low noise, make these photodetectors well-suited for applications requiring high sensitivity and precision, including quantum technology and cryptography, which are emerging areas benefiting from their unique properties.

This thesis specifically focusses on the simulation, fabrication and optimisation of III-V photodetectors integrated on Si by using a Technology Computer-Aided Design (TCAD) software called Sentaurus by Synopsys and a fabrication technique called Template-Assisted Selective Epitaxy (TASE).

1.3. Semiconductors

In most semiconductors used for absorption, the dominant absorption mechanism is intrinsic band-to-band absorption. This type of absorption happens when the photon energy is greater than the material band gap. Incident photons with a wavelength shorter than the upper cut-off wavelength of the material become absorbed as they travel in the semiconductor and generate an electron-hole (e^--h^+) pair. The photon intensity decreases exponentially with the depth of the semiconductor following the Beer–Lambert law, and the majority of the photon absorption occurs within an area defined as the penetration depth (when optical intensity is reduced to 1/e of its initial value). Some typical semiconductors used in CMOS and optical technologies for different applications are shown in Table 1-1 with their type of band gap and the value of band gap energy (E_g) in the form of cut-off wavelength in μm at 300K.

Table 1-1. List of semiconductor materials typically used in optoelectronic applications with their band gap type and energy in μm at room temperature.

Material	Band gap type	Band gap energy (μm)
Si	Indirect	1.1 [a]
Ge	Indirect	1.88 [a]
GaAs	Direct	0.87 [b]
InSb	Direct	7.1 [b]
AlAs	Indirect	0.57 [b]
InAs	Direct	3.5 [b]
InP	Direct	0.91 [b]
GaN (bulk)	Direct	0.36 [b]
$Al_xGa_{1-x}As$	Direct below x=0.39	0.77(x=0.39) to 0.87 (x=0) [b]
$In_{0.53}Ga_{0.47}As$	Direct	1.68 [b]
Hex-$Si_{1-x}Ge_x$	Direct for 0.65<x<1	1.85 (x=0.65) to 3.54 (x=1) [c]

[a] Reference [41]

[b] Reference [42]

[c] Reference [43]

The values for the band gap energies for III-V semiconductors shown in Table 1-1 are extracted from reference [42]. In this work, the band gap energy at 0 K (E_g0) is given together with two adjustable parameters (α and β). By using the empirical Varshini form (also given in [42]), the E_g at any desired temperature can be obtained using equation 1.1.

$$E_g(T) = E_g(T = 0) - \frac{\alpha \cdot T^2}{T + \beta} \tag{1.1}$$

Once calculated for binary compounds, the E_g of ternary alloys can be derived through equation 1.2.

$$E_g(A_{1-x}B_x) = (1 - x) \cdot E_g(A) + x \cdot E_g(B) - x \cdot (1 - x) \cdot C \tag{1.2}$$

where A and B are the binary compounds forming the alloy, x is the molar fraction, and C is the so-called bowing parameter, which takes into account the deviation from a linear interpolation between A and B. This deviation can be seen in the lines joining the binary compounds in Fig 1-1.

All these parameters and formulas are provided in [42], and give values in eV, which are then converted into μm to visualise the maximum value of wavelength of light these materials will absorb (cut-off wavelength).

In indirect bandgap semiconductors such as Si, the absorption process near the band edge requires both the absorption of a photon and a phonon (lattice vibration). This additional requirement leads to a lower absorption coefficient compared to direct bandgap materials, as the probability of indirect transitions is lower. Some indirect bandgap semiconductors, such as Ge, have direct transitions at shorter wavelengths, although this limits the operational wavelengths. In contrast, direct bandgap materials like many III-V semiconductors and their alloys have straightforward photon absorption process all the way to their band edge. The absorption coefficient for different semiconductor materials is plotted against incident wavelengths in Fig 1-2.

This is not as important for photodetectors as it is for lasers, as at typical operating temperatures there are generally sufficient phonons available to facilitate the transition. The widespread use of CMOS image sensors demonstrates that even an indirect bandgap material can work very well as a PD.

However, as the future aimed application for the fabricated photodetectors is for them to be integrated in a full optical link where both emitters and detectors will be jointly fabricated, the use and integration of a direct band-gap material is justified, as it can fulfil both functions. For this reason, there are two main requirements for a material to be used in the final photodetectors; to have a cut-off wavelength larger than the targeted wavelength (1300 - 1550 nm) and to have a direct band gap for better efficiency.

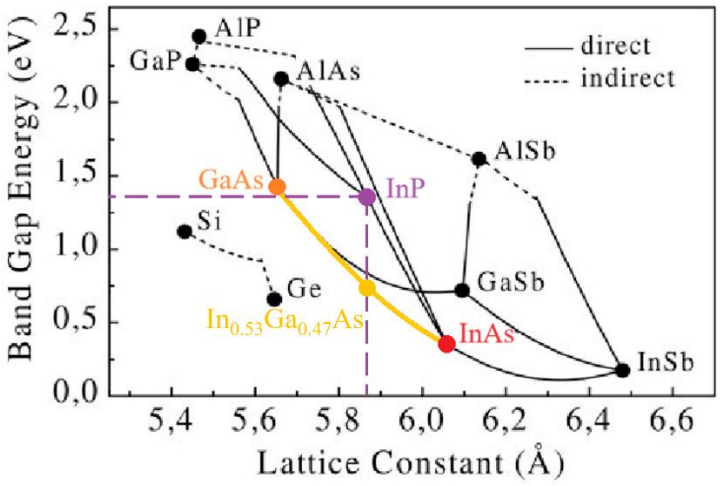


Fig 1-1. Band gap (eV) of III-V materials with their lattice constant. The lines joining the binary compounds represent the respective ternary and quaternary compounds, which can have direct (solid line) or indirect (dashed line) band gaps. Figure modified (coloured and $In_{0.53}Ga_{0.47}As$ added) from [44], reproduced with permission from Springer Nature.

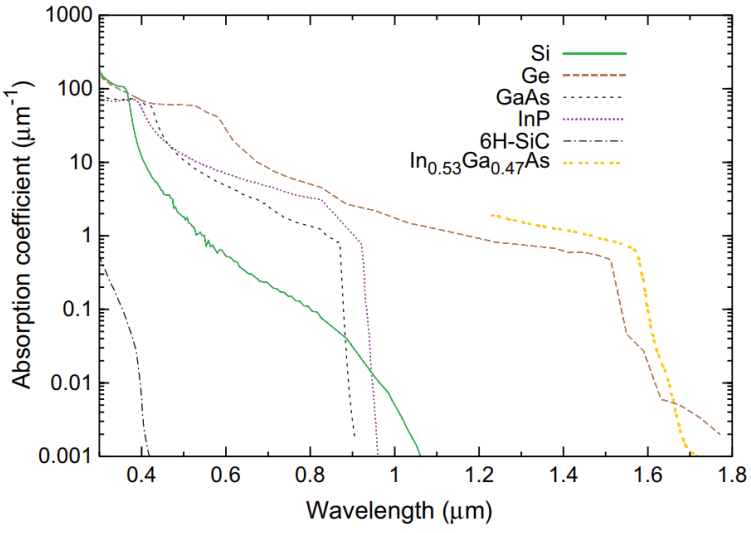


Fig 1-2. Absorption coefficients versus wavelength for some semiconductor materials. Figure modified (coloured) from [45], reproduced with permission from Springer Nature.

Another advantage of III-V semiconductors is their versatility in element combinations, with the majority being direct band gap materials. The range of wavelengths that III-V materials encompass goes from approximately 360 nm to 7100 nm. Ternary and quaternary III-V compounds, which are made from three or four elements with different element percentages, fill up the wavelength gaps between the binary compounds. This is illustrated in Fig 1-1, where the dots, representing the binary compounds, are joined using dashed lines for indirect band gap materials or solid lines for direct band gap materials, which represent the ternary and quaternary compounds.

An example illustrating the ternary compound used in this work is the (yellow) line that joins GaAs (orange dot) with InAs (red dot), which represents the ternary compound $In_{1-x}Ga_xAs$, from x=1 (GaAs) to x=0 (InAs). Band gap energies in eV of various III-V semiconductors are plotted against their lattice constant in the graph in Fig 1-1. This highlights an important feature and the main issue to solve when integrating different III-V materials together in a heterostructure and onto Si, as a variety of defects arise when growing epitaxially if the lattice constants are too different (high lattice mismatch) [46].

InP and $In_{0.53}Ga_{0.47}As$ are the materials used in this work. The specific concentration of 53% of Indium in InGaAs has been chosen to match with the lattice constant of InP and facilitate the integration of both materials in a heterostructure. Its band gap allows for detection up to 1680 nm, which includes the desired telecom and datacom bands, used in optical fibre communication.

1.4. Photodetectors

Some of the material characteristics to take into account when building a photodetector are the absorption coefficient (α) and the doping. The absorption coefficient provides information about the decay of the optical intensity within the material, which is also wavelength dependant. At around 1600 nm, while some materials such as Ge have a penetration depth of ~100μm, for InGaAs this thickness is reduced to ~1μm. This is because indirect band gap materials' absorption coefficient tends to decay more gradually with wavelength, while direct band gap materials have a sharp decaying α, as shown in Fig 1-2. This will impact the size of the fabricated photodetector since any material beyond the decay length from the illuminated surface will absorb nominal light and thus contribute minimally to its performance.

Doping allows semiconductors' electrical conductivity to be modified by a change in carrier concentration, which shifts its effective Fermi level. The photodetectors built in this project consist of p-i-n diodes, which include a p-doped material, an intrinsic material (undoped or lightly doped) and an n-doped material.

The dopants on p-doped materials are made of elements that have a low number of valence electrons, so that extra holes are incorporated. For n-doped materials, the dopants have a high number of valence electrons, so that these can be donated to the original material. Examples of p-type dopants and n-type dopants (and the ones used within this project) are zinc (Zn) and tin (Sn) respectively.

The simplest form of a diode is a p-n junction. When p-doped and n-doped materials come into contact, a depletion zone is formed. Due to the extra holes and electrons in each region, an electric field develops in the centre, pointing towards the p-side of the junction. When photons are absorbed, e^--h^+ pairs are generated. If this occurs within the depletion zone, the electric field separates these pairs, which will move in opposite directions due to the inbuilt electric field, generating a photocurrent. However, if photons are absorbed far from the centre, the generated e^--h^+ pairs will likely recombine due to the absence of an electric field. This process is illustrated in Fig 1-3.

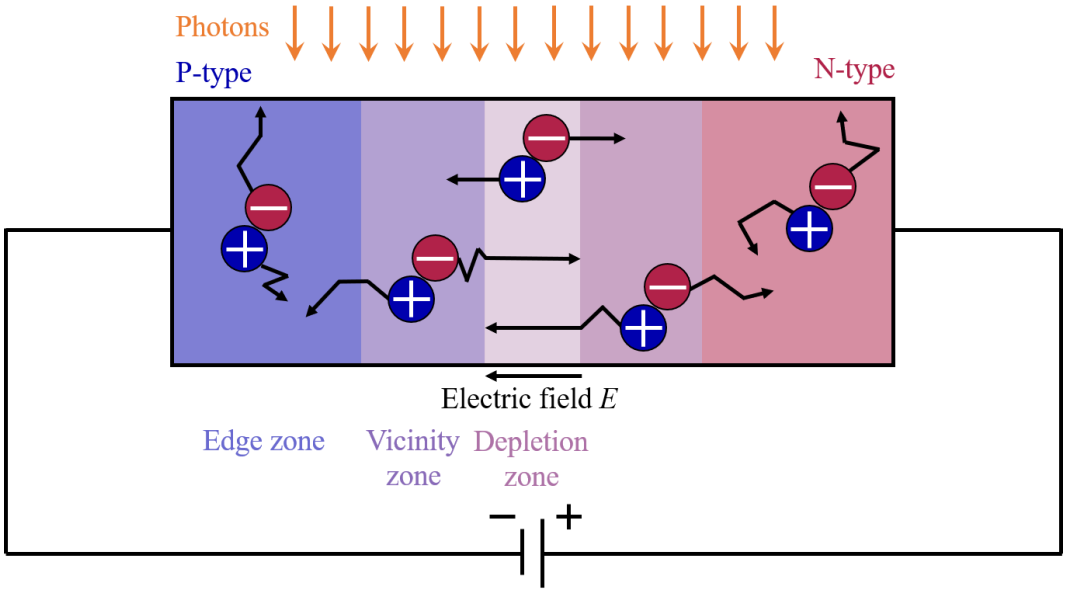


Fig 1-3. Schematic of the behaviour inside a p-n diode as photons are absorbed, generating electron-hole pairs in the different regions.

The use of p-i-n photodiodes allows for the collection of more photogenerated carriers. Adding an intrinsic material between the n- and p-doped materials increases the size of the depletion zone. When light is absorbed in the i-region, e^--h^+ pairs are generated and move in opposite directions due to the inbuilt electric field, producing a photocurrent. Another advantage of the intrinsic region is the reduction of the junction capacitance, which, as previously mentioned, is a limiting factor for a photodetector. As a minor disadvantage, since it is usually not the primary constraint, it increases the transit time of the photodetectors.

The e^--h^+ pairs generated when a photon with a larger energy than the band gap of the material is absorbed can be detected by applying a negative voltage into a semiconductor. When applying a positive voltage, the electrons on the n-side will be attracted to the positive side of the circuit, and any photogenerated electrons will add to that already large current value. When reversing the voltage polarity (reverse bias), the n-region electrons will not be attracted to the now negative pole. Nevertheless, a small leakage current, on the order of nanoamperes, will be detected due to thermal effects and defect states. This is called dark current. In reverse bias, any electron-hole pairs generated by the absorption of a photon will have a significant impact on the current passing through the device. This photocurrent is the means a photodetector detects light: by transforming an optical signal into an electrical signal.

A typical current-voltage (I-V) curve for a diode, shown in Fig 1-4, follows the expression in equation 1.3,

$$i = i_s \cdot \left[\exp\left(\frac{eV}{kT}\right) - 1\right] - i_p \tag{1.3}$$

where k is Boltzmann's constant (k = 1.380649 × 10^{-23} J/K), T is the temperature, e is the elementary charge (e = 1.602176634×10^{-19} C), V is the voltage, i_s is the saturation current in reverse bias (dark current) and i_p is the photocurrent.

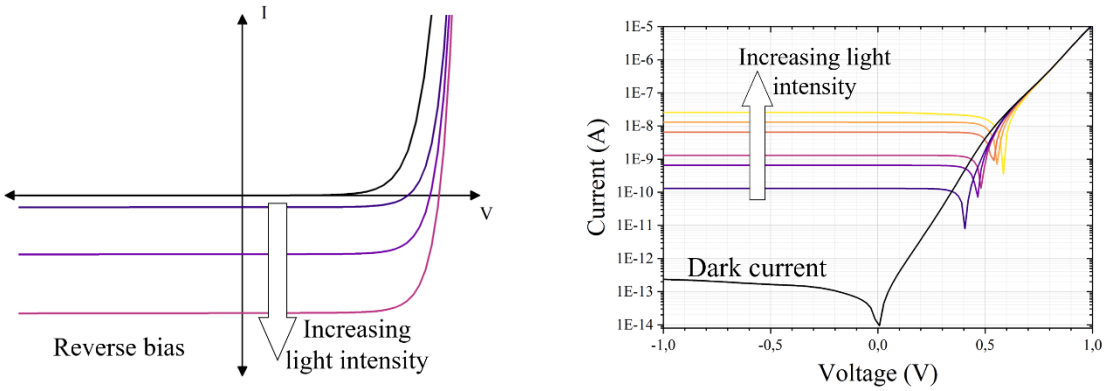


Fig 1-4. Typical current-voltage (I-V) curve for a diode. The black curves correspond to the characteristics of a device without light, while the coloured curves correspond to the characteristics when light is applied, increasing its intensity. On the left the curves have been plotted in linear scale, while on the right the modulus of the current has been plotted in logarithmic scale for a better visualisation of the current values at reverse bias.

As seen in Fig 1-4, the I-V curves from photodetectors are easier to visualise on a logarithmic scale (right). However, it is important to note that negative values appear as positive on this scale. Negative current values simply indicate direction; the magnitude is what is significant, not the sign. The logarithmic scale highlights how the black curve (dark current) crosses the zero current line at zero voltage, by the position of its peak. When light is applied, the curve shifts downward on the linear scale, causing the zero current peak to move to a positive voltage value.

Photodetectors made for optical interconnects need specific characteristics to have a good device performance. Some of the figures of merit that characterise it are the following [47]:

- Signal-to-noise ratio (SNR). It is defined as the ratio of the power of a signal to the power of its noise, and it is an important figure of merit for a detection system. Its expression can be found in equation 1.4,

$$SNR = \frac{\overline{s^2}}{\overline{s_n^2}} = \frac{\overline{s^2}}{\sigma_s^2} \tag{1.4}$$

  where $\bar{s}$ is the mean value of the noise in a signal and σ_s^2 is the mean square deviation of that signal. In a photodetector, the signal s can represent the number of photons, the photon flux, the photocurrent, or the photovoltage [47].

A higher SNR indicates more signal than noise, and it is crucial to have high photocurrent values compared to the dark current. The dark current value depends on the noise in the photodetector or in the circuit, which can be of quantum or thermal origin.

The input signal power that yields a SNR of one in a 1 Hz output bandwidth is known as the Noise Equivalent Power (NEP). The inverse of the NEP is defined as the detectivity of a photodetector. A higher detectivity indicates that the photodetector is better suited for detecting weak signals, as it implies greater sensitivity and lower noise interference.

- Quantum efficiency (η). The quantum efficiency is defined as the ratio between the generated e^--h^+ pairs contributing to current and the number of incident photons. This is wavelength dependant as only incident photons with an energy higher than the band gap of the material will be absorbed, so it is determined by the absorbing material as shown in Fig 1-2. η depends on the internal quantum efficiency (probability of photogenerating e^--h^+ pairs), the optical transmission efficiency and the carrier collection efficiency. The expression for the quantum efficiency follows equation 1.5,

$$\eta = (1 - \mathcal{R}) \cdot \varsigma \cdot [1 - \exp(-\alpha d)] \tag{1.5}$$

which contains the power transmittance ($T = 1 - \mathcal{R}$) at the surface of the device, the collection efficiency of the photogenerated carriers (ς), and the fraction of photons absorbed in the material ($1 - \exp(-\alpha d)$).

- Responsivity (ρ). The responsivity is the ratio between the output current signal and the power of the input optical signal. Due to some recombination of generated e^--h^+ pairs along the semiconductor or reflections of the light on its surface, the responsivity is reduced and the quantum efficiency, even at the peak of the semiconductors' spectral response, does not reach ideality (100%). This can be seen in Fig 1-5. The expression for the responsivity is shown in equation 1.6,

$$\rho = \frac{i_p}{P} = \frac{e}{hv}\eta = \frac{\lambda_0}{1.24}\eta \tag{1.6}$$

which relates the electric current (i_p) flowing in the device to the incident optical power (P). It is linearly proportional to the wavelength (λ) and to the quantum efficiency (η).

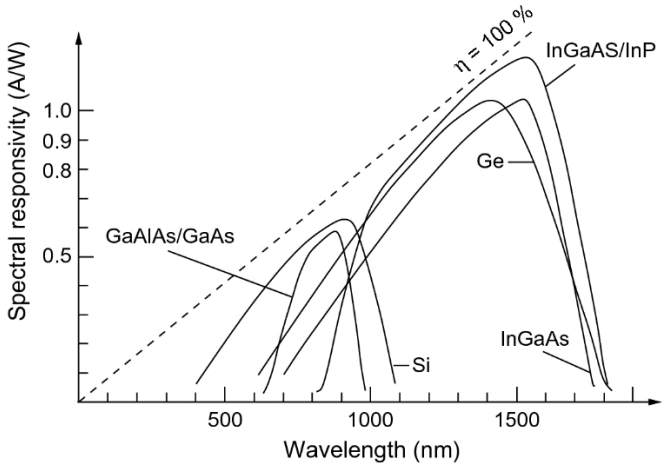


Fig 1-5. Responsivity of some photodetectors compared with an ideal quantum efficiency one (η=100%). Figure from [45], reproduced with permission from Springer Nature.

- Bandwidth. The last characteristic is device bandwidth, as it is one of the reasons to transition from electronics to optically transmitted signals. It is related to its frequency response and it should be higher than the temporal variations in the applied signal [47, 48]. The 3dB frequency seen in equation 1.7 defines the photodetector bandwidth, which corresponds to the frequency at which the radio frequency response of the detector has dropped to half its original value.

$$f_{3dB,RC} = \frac{1}{2\pi RC} = \frac{1}{2\pi(C_J + C_P)(R_S + R_L)} \tag{1.7}$$

  The 3dB frequency is inversely proportional to the RC time constant of the photodetector, determined by its capacitance.

Detailed theoretical descriptions with important formulas for these and other parameters are extensively explained in [47].

1.4.1. III-V photodetectors

Due to the direct and tunable bandgap of III-V semiconductor materials, there is a great interest in integrating them either monolithically or heterogeneously on silicon to exploit their complementary properties and, in particular, the direct bandgap of III-Vs for opto-electronic devices, including emitters such as LEDs and lasers, densely integrated with CMOS [1, 37].

The combination of the advantages from the advanced state of silicon technology with the potential of the direct and tunable bandgap of III-V materials could result in complex photonic structures for high-speed data communications [49, 50].

As mentioned before, the III-V materials chosen for this project are indium phosphide (InP) and indium gallium arsenide (InGaAs). InP has been used for photonic devices extensively, as it provides a high-sensitivity and fast response photodetector with a very low dark current when working with short wavelengths (below its band edge of around 900 nm) [51, 52]. InGaAs is a versatile material because it is a ternary compound and its band-gap can be tuned from the near-infrared to the mid-infrared regions by adjusting the ratio between indium and gallium. It is also known for having a small leakage current and high electron mobility [53]. The specific ratio targeted, as already mentioned, is approximately $In_{0.53}Ga_{0.47}As$ to lattice-match with InP and reduce the density of defects at their interface [54, 55, 56].

In this work, a heterojunction is used so that the material in the p- and n-regions (InP, with a cut-off wavelength of 900 nm) does not absorb light within the targeted wavelength range (1300 – 1550 nm), ensuring all absorption occurs in the i-region (InGaAs, with a cut-off wavelength of 1680 nm). Proper integration of these two materials with each other and onto Silicon is crucial for good photodetector performance, highlighting the importance of lattice-matching between the III-V materials and the research on various fabrication techniques involving CMOS technologies.

The following chapters are organised as follows:

- **Chapter 2** explains the use and functions of the simulation software employed to simulate the III-V photodetectors. It then presents the initial results, which include a materials study and a study on traps.

- **Chapter 3** introduces the integration techniques of III-V onto silicon, with a focus on the TASE method used to fabricate the photodetectors in this project. Afterwards, it presents the different fabricated devices, the challenges encountered, and the solutions implemented to achieve III-V p-i-n photodetectors.

- **Chapter 4** presents the different characterisation results of the fabricated devices, both electrical and optical. It also includes the simulation work done to match the electrical characterisation, providing a better understanding of the results. Finally, it includes the optical characterisation of some devices at low temperatures.

2. TCAD simulations

This chapter explains the functions of the simulation software used to model the III-V photodetectors. The objective was to become familiar with simulating III-V photodetectors through a materials study, alongside a preliminary investigation on how to potentially match the simulations with experimental results by incorporating traps into the simulations.

At the time of this study, IBM had published work on 60 nm thick InGaAs p-i-n detectors and was transitioning towards a 220 nm thick p-InP/i-InGaAs/n-InP photodetector, which was only published in 2022. The materials study presented here served to confirm the superior performance of heterostructure devices compared to homostructure ones.

The traps study was conducted after IBM provided preliminary data on the 220 nm devices. Since the experimental data lacked detailed information about the devices, the primary focus was not on precise matching but rather on understanding the impact of trap location within similar types of devices.

As technologies become more complex in terms of fabrication techniques and material combinations, the semiconductor industry increasingly relies on Technology Computer-Aided Design (TCAD) to investigate advanced device performance while minimising costs. TCAD serves as a strategy to test different geometries, materials, doping levels, and device dimensions before committing time and resources in the lab. It is the fastest and most cost-effective way to evaluate the key parameters of the desired device.

In this project, the state-of-the-art TCAD simulation software Sentaurus™ [57] is used to study III-V photodetectors. Design variations and numerical simulations are performed to validate the materials used and to understand which parameters affect the performance of the fabricated devices. Sentaurus incorporates tools for process simulation, device creation, device simulation, and interconnect modelling and extraction, all within an interactive simulation environment featuring a dynamic graphical user interface (GUI) for managing simulation tasks and analysing the results. The package tools available on the platform are shown in Fig 2-1.

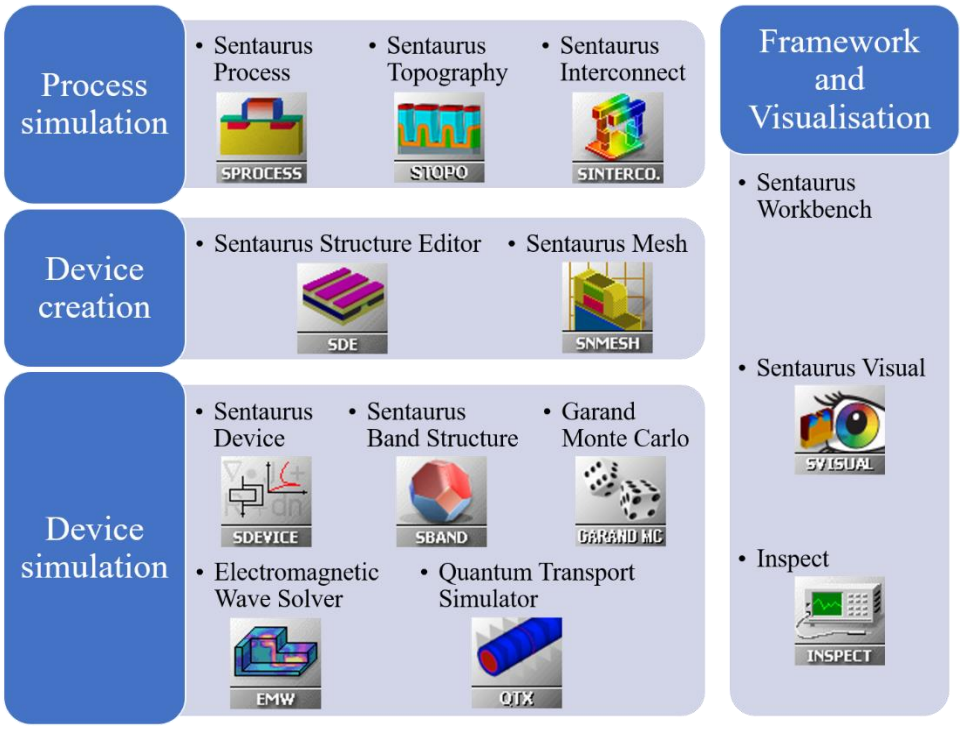


Fig 2-1. Diagram of the Synopsys Sentaurus TCAD tools organised based on their specific functions.

The process of simulating the devices for this project begins with generating the structure using the Structure Device Editor (SDE). SDE includes definition of the geometry, materials, doping profiles, contact regions, and an initial mesh. The mesh is then refined using the Sentaurus Mesh generator (SNMESH), which creates the discretised mesh files needed for other tools, such as the Delaunay mesh for electrical calculations and the tensor mesh for electromagnetic simulations. The Electromagnetic Wave Solver (EMW), which uses the Finite-Difference Time-Domain (FDTD) method to solve Maxwell's equations, is employed to find the optical mode distribution in the materials. These results are then input into Sentaurus Device (SDEVICE) to numerically solve carrier transport equations and obtain current-voltage (I-V) curves and other characteristics of the devices. Sentaurus Visual (SVISUAL) is then used to visualise the structure from SDE, the optical mode distribution from EMW, and the electrical characteristics from SDEVICE, including band-gap, I-V curves, and electron or hole carrier densities distribution, among others.

2.1. Overview of Sentaurus Tools

- **Sentaurus Workbench (SWB):** Serving as the framework for Sentaurus TCAD software, SWB provides an environment for creating, editing, and organising the flow of simulations. It facilitates the setup of the desired tools, the addition of parameters for design-of-experiment splits, and the visualisation of execution and results. Each tool has its own input file for separate coding. Simulations are displayed as a family tree and can be organised into projects and folders for easy access and a clear overview. An example of how SWB looks like in a simulation project is shown in Fig 2-2.

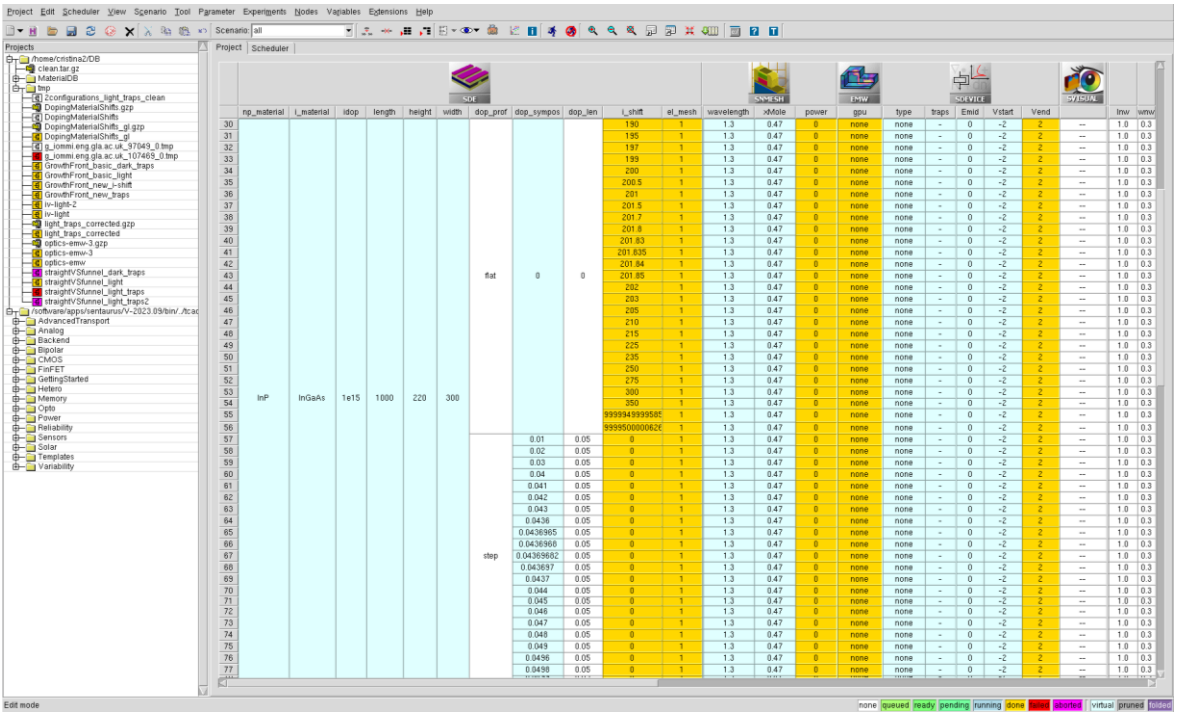


Fig 2-2. Screenshot of Sentaurus Workbench displaying the toolbar buttons, the organisation of projects, and an open project with various tools and parameters arranged in a family-tree view.

- **Sentaurus Structure Editor (SDE):** Device generation through SDE can be done either interactively or using scripts. Geometrical elements such as lines, 2D shapes (rectangles and circles) and 3D bodies (cuboids, spheres and cylinders) are defined by their spatial coordinates and materials. For example, defining a cuboid requires specifying the coordinates of the opposite corners. For complex shapes, all vertices can be defined, joined into faces, and then stitched into a final body. Boolean operations, like merge (AB), new replaces old (ABA), old replaces new (BAB), new overlaps old (ABiA), and old overlaps new (ABiB), can superpose shapes and delete existing regions.

Defined shapes are named as regions to allow the addition of parameters such as doping or mesh onto them. SDE also supports if/else statements and varying parameters in SWB for more device variability.

After geometrically defining the device, a constant or profile-defined doping can be added by specifying the species, concentration, and if using an analytical function like Gaussian or decaying, their specific parameters. The next step is to define the contacts, which can be done by setting them on already existing bodies or finding an existing face or line on a region and setting them there. Finally, the mesh is added by defining refinement windows, functions, and sizes, and placing them on specific regions, materials, or interfaces.

The advantage of using SDE instead of a process simulator is a reduced simulation cost and the ability to test more device concepts. However, this comes at the expense of accuracy in capturing certain characteristics. Since the fabrication process for this project is already known and the structures are feasible, there was no need to simulate it.

- **Sentaurus Mesh (SNMESH):** This tool produces finite-element meshes for other TCAD tools. It can create a 3D mesh composed of tetrahedra for electrical simulations, known as a Delaunay mesh. Since SDE includes built-in capabilities for creating this type of mesh, SNMESH is generally not necessary for pure electrical simulations. However, for optical simulations with EMW, a tensor-product mesh consisting of cuboid elements is required, which cannot be defined using SDE's built-in capabilities. The two types of mesh can be seen in Fig 2-3.

  To build the tensor mesh required for EMW, the boundary file in TDR format from SDE, containing the structure, doping, and refinement information, is imported. A tensor mesh is then created in the different regions, materials, and/or directions. The tensor mesh is built based on the wavelength to be used in the simulations, with refinement specified in nodes-per-wavelength values.

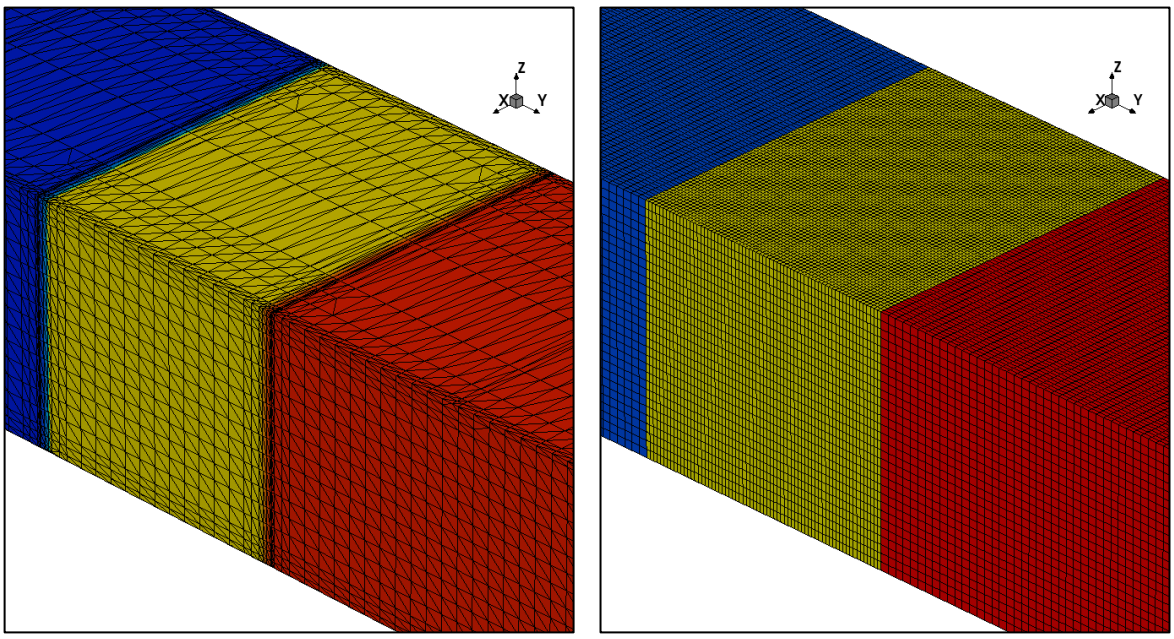


Fig 2-3. Results of SNMESH simulations of a Delaunay mesh, composed of tetrahedra (left) and of a tensor-product mesh, composed of cuboid elements (right).

- **Electromagnetic Wave Solver (EMW):** EMW is a solver based on the FDTD method that numerically solves the temporal evolution of electromagnetic waves in a device structure defined on a tensor grid. The primary result used in subsequent electrical simulations is the absorbed photon density distribution. Detailed information on the FDTD method can be found in the Sentaurus Device Electromagnetic Wave Solver user guide and in [58].

  The EMW command file, which contains the coding for this tool, consists of different sections describing specific aspects of the simulation. The important sections used for this project are:

  - Complex Refractive Index (CRI): Defines the refractive index and extinction coefficient dependencies (mole fraction, wavelength, temperature, carrier density, or material gain). For this project, the dependency has been defined based on wavelength.

  - Dispersive Media: Accounts for the dispersive behaviour of frequency-dependent materials in FDTD. Different models are available for various types of dispersive materials. For this project, the SingleDipoleDrude model was used to create a dispersive medium for each Complex Refractive Index (CRI) value whose imaginary part is larger than its real part. This is usually used for devices with inhomogeneous CRI profiles.

- Boundary: Sets the type and placement of the boundary conditions. Available types of boundary conditions include perfect electric conductor (*PEC*), perfect magnetic conductor (*PMC*), periodic boundary conditions for normal (*periodic*) and oblique (*periodicoblique*) incidence, and absorbing boundary conditions. For this project, the boundary conditions for X and Y were set to PeriodicOblique and for Z to Convolutional perfectly matched layer (CPML). This is the typical simulation setup for CMOS image sensor and solar-cell applications. Periodic-oblique applies to plane wave excitations with both normal and oblique incidence, and CPML is an absorbing boundary condition.

- **Sentaurus Device (SDEVICE):** This tool includes advanced physical models for electrothermal, mixed-mode device, and circuit simulations for 1D, 2D and 3D semiconductor devices. It numerically simulates their electrical behaviour through physical device equations describing carrier distribution and conduction mechanisms. Due to the meshing of the devices, the properties are only defined at certain points in space, with the rest obtained by interpolation.

  The first part of the code in SDEVICE is the device definition. It includes the sections of *File*, *Electrode*, *Thermode* and *Physics*. Various physical models are used for the simulation of the III-V photodetectors, including:

  - Heterointerfaces: For abrupt heterojunctions, this model treats discontinuous datasets by introducing double points at the interfaces. One of the points holds the information for one side of the interface, and the other holds the information for the opposite side.

  - Shockley-Read-Hall (SRH) recombination: Recombination through deep defect levels in the band gap. The SRH lifetimes can depend on doping, temperature, and electric field, and can include trap-assisted tunnelling through different models.

    This type of recombination is the most relevant in the studied devices. It takes place through the capture of one carrier at a time, either an electron or a hole, by a trap or defect with its energy somewhere in the band gap. The defects can go through the processes of electron and hole capture, and electron and hole emission. A defect can only capture one electron at a time, and only a hole if there is already an electron trapped.

The process of trapping an electron can result in the annihilation of an electron-hole pair if a hole gets subsequently captured, or in the reemission of the trapped charge. An electron captured can be thermally reemitted back to the conduction band. For this reason, the mid-bandgap traps are the ones with a bigger impact on the devices' performance, as it takes the same thermal energy to capture and reemit charges.

- Mole fraction: The mole fraction (x) of ternary and quaternary alloys can only be defined through SDEVICE. If not specified, x = 0.5 is assumed.

- Traps: Traps are important in device physics as they provide doping, enhance recombination, and increase leakage in insulators. SDEVICE allows for different types of traps with different energy distributions in bulk and interface regions and provides multiple models for capture and emission rates. The energy distribution can be defined through a single energy level, or with uniform, exponential or Gaussian distributions, or through a user-defined table distribution. During the traps study on this project, traps were introduced in different areas of the device, with their energy level consistently set at mid-bandgap to maximise their influence on device performance, as outlined above.

After defining the physical models, the solve methods are defined by the *Math* and *Solve* sections, which specify simulation parameters rather than device-specific settings. The *Math* section defines parameters such as the number of threads used, the number of iterations, and other numerical settings. The *Solve* section consists of a series of commands to be performed in order. These commands operate at different levels, where lower-level commands serve as parameters for higher-level ones.

Finally, the *Plot* section specifies which device characteristics to save at the end or during the simulation to the plot file. It can include spatial-dependent datasets such as doping profiles, space charge distribution, electron and hole mobilities, or Shockley-Read-Hall recombination rates, providing insights into the device's internal behaviour. Additionally, a *CurrentPlot* section can be defined to add specific scalar data over specific domains (materials, regions, or interfaces), such as the absorbed photon density or the band gap, to the plot file.

- **Sentaurus Visual (SVISUAL):** This plotting software within SWB is used to visualise data from simulations and experiments. SVISUAL allows interactive work with data through both a user interface and a scripting language, enabling the visualisation of physical simulation results in 1D, 2D, and 3D. Users can modify plots to gain new perspectives and create visualisations displaying fields, geometries, and regions, as well as view I-V curves, doping profiles, and band gap plots. The tool provides features such as zoom, pan, rotate, and measure/probe tools for detailed data extraction

  There are two ways of using SVISUAL: integrating the tool into the simulation flow or accessing it separately. The latter is done by selecting a simulation node (yellow cells in Fig 2-2) and clicking on the Visualise button in the top toolbar (eye symbol). This displays the Sentaurus Visual option, which opens and displays the files that contain graphical data from the selected node. The SVISUAL interface can be seen in Fig 2-4.

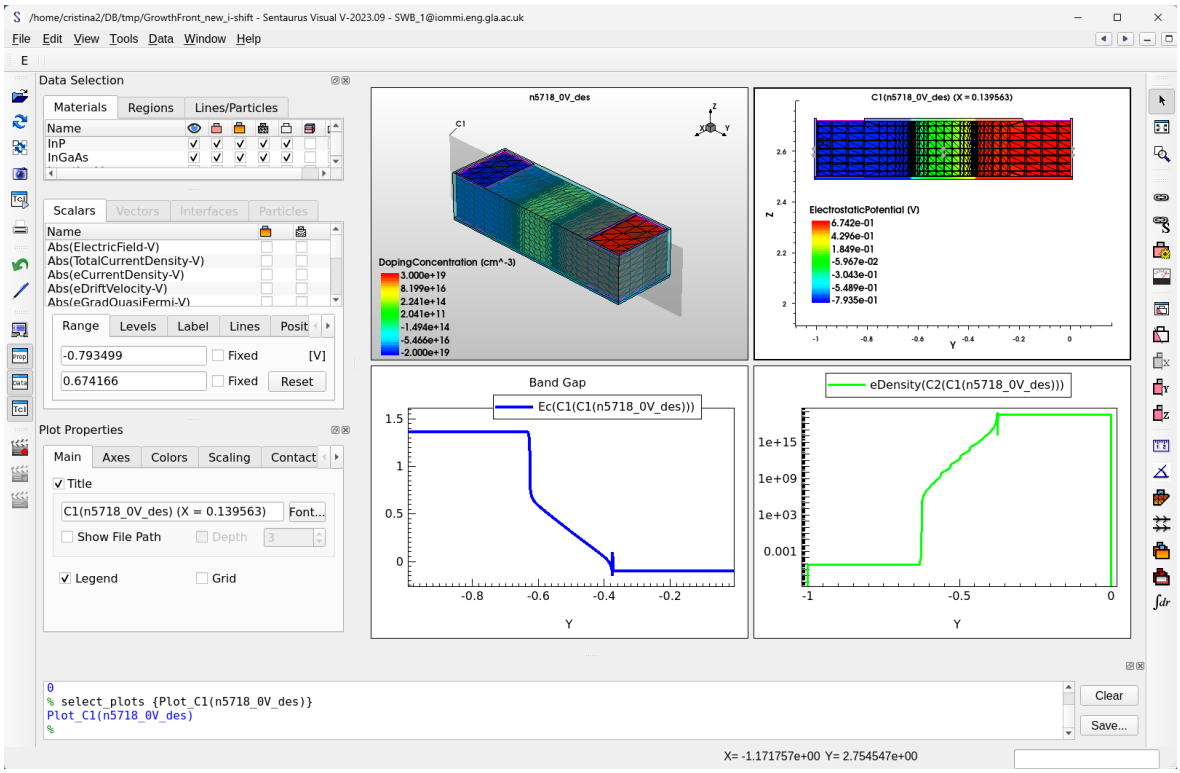


Fig 2-4. Screenshot of Sentaurus Visual user interface with various 3D, 2D and 1D plots of a p-i-n III-V device.

2.2. Materials study

The project started by performing simulations and thus studying the parameters that play an important role in the final device operation. These parameters include the materials used, the species and amount of doping on each region, and the dimensions of the photodetector. These variables affect the signal-to-noise ratio, the responsivity, and the speed of the photodetector. This phase of the project involved learning how to use Sentaurus TCAD tools.

The materials study was conducted by simulating a p-i-n nanowire (NW) photodetector made of different combinations of InP and $In_{0.55}Ga_{0.45}As$ materials: two homostructures of InP and InGaAs NWs, and a heterostructure composed of p-InP/i-InGaAs/n-InP. The findings of the study resulted in the submission and publication of a conference paper at the 21st International Conference on Numerical Simulation of Optoelectronic Devices (NUSOD2021) (see [59]).

Although the perfect lattice match between InP and $In_{1-x}Ga_xAs$ occurs when the molar fraction of the latter is x=0.47, $In_{0.55}Ga_{0.45}As$ was chosen for this study. Given the uncertainty surrounding the exact molar fraction of the devices based on experimental data obtained from IBM, where the devices were later fabricated, a slightly different molar fraction was proposed for simulations. This choice does not significantly alter the device setup and is a standard practice in both academia and industry.

For the materials study, devices with the same architecture and dimensions (comparable to those previously experimentally demonstrated by IBM [60]) were evaluated. Since the aim was to assess the impact of the material composition rather than optimise the device architecture or coupling schemes, which might be highly wavelength dependent, the simulations were performed using free-space detection [59]. The top part of Fig 2-5 shows the simulation domain, including the device geometry from SDE and the source of light. The bottom part of Fig 2-5 presents the optical generation-coloured plots for each device at different wavelengths obtained from EMW.

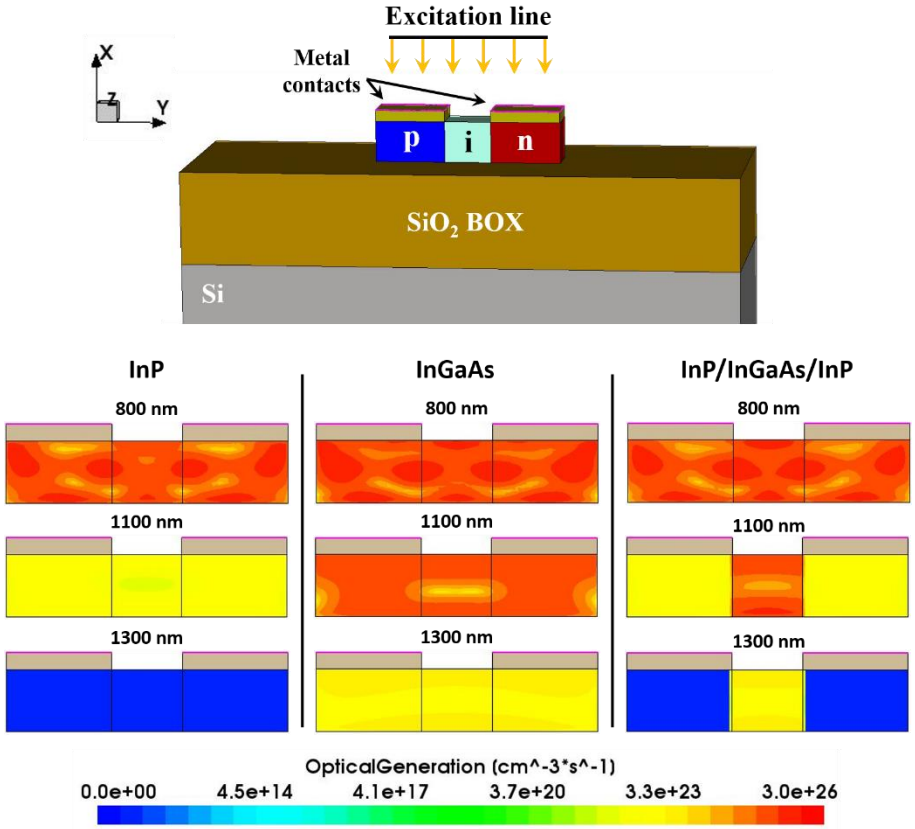


Fig 2-5. Top: sketch of the simulation domain showing the p-i-n diode geometry with dimensions x = 220 nm, y = 1000 nm and z = 200 nm, the metal contacts, transparent to the light, the SiO_2 BOX and the Si substrate. The source of light has been added to the top to visualise the simulation setup. Bottom: optical generation-coloured plots for the fully InP device, the fully InGaAs device and the InP/InGaAs/InP heterostructure, for wavelengths of 800 nm, 1100 nm and 1300 nm [59] reproduced with permission © 2021 IEEE.

To closely resemble the future fabricated devices, the nanowires' height was set at 220 nm, matching the thickness of the top silicon layer of the used SOI. Their width was chosen to be 200 nm, with the p- and n-regions each being 375 nm long, and the i-region measuring 250 nm in length. The underlying oxide has a thickness of 500 nm to ensure optical isolation in a fully integrated scheme. The excitation line is placed 500 nm above the nanowire, illuminating the full structure to resemble reality in the experimental setup. The metal contacts are considered transparent to avoid the impact of metal absorption and reflection when evaluating wavelength dependence.

The optical generation plots shown in the bottom of Fig 2-5, reveal that optical generation in the InP regions decreases more rapidly compared to the InGaAs region as the excitation laser wavelength increases from 800 nm to 1300 nm. This is expected since InP has a higher band-gap (1,27 eV) compared to InGaAs (0,73 eV), and therefore has a cut-off wavelength of 977 nm [59].

The next step involved obtaining the absorption response of the current for the three structures as a function of wavelength. This was achieved by inserting the optically simulated results from EMW into SDEVICE and obtaining the current at -0,5 V of applied voltage at different wavelengths. The results are shown in Fig 2-6.

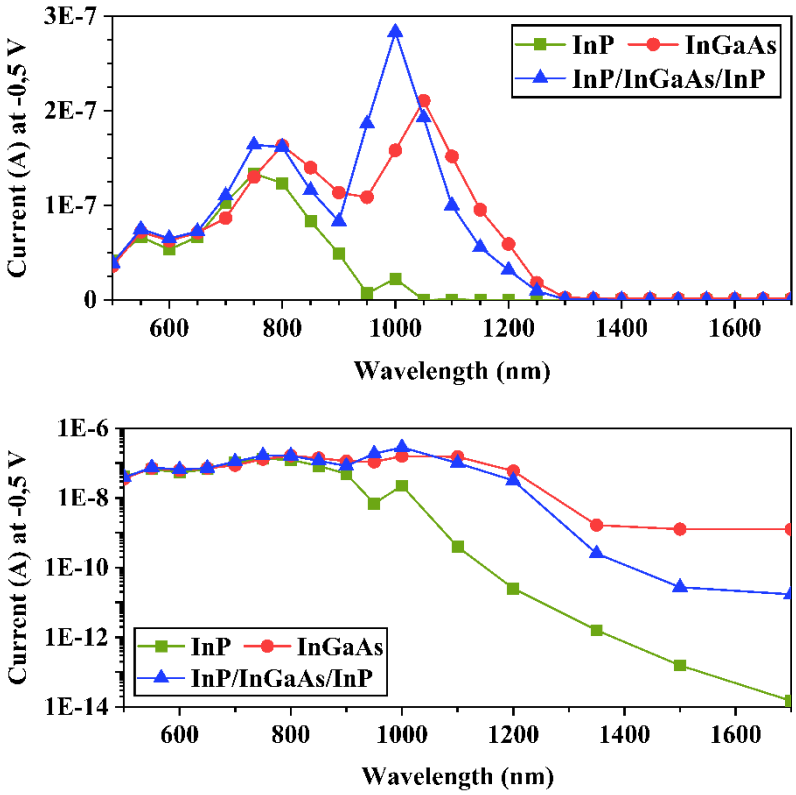


Fig 2-6. Current in linear (top) and logarithmic (bottom) scale as a function of the wavelength for the fully InP device, the fully InGaAs device and the InP/InGaAs/InP heterostructure [59] reproduced with permission © 2021 IEEE.

As expected, all the curves show a gradual decline with increasing wavelength. The peaks observed around 1000 nm may be attributed to reflections within the simulations and do not accurately represent real-world conditions. InP provides efficient detection at shorter wavelengths but drops off rapidly near its band-edge at 900 - 1000 nm. In both the homojunction and heterojunction structures, InGaAs serves as the active absorption material, extending the absorption edge further into the NIR. The heterostructure nanowire reaches its peak current at around 1000 nm. The pure InGaAs device achieves its highest photocurrent at slightly longer wavelengths, most likely as a result of the larger volume of InGaAs in the nanowire [59].

Fig 2-7 shows the power sweep of signal power for two different wavelengths at a reverse bias of -0,5 V, in linear and logarithmic scale. A linear increase in current with respect to laser power can be observed in all cases for 800 nm in Fig 2-7a. However, as seen in Fig 2-7b, efficiency is markedly lower at 1300 nm, with the pure InP device exhibiting the lowest efficiency. This correlates with the lower optical generation observed in Fig 2-5 [59].

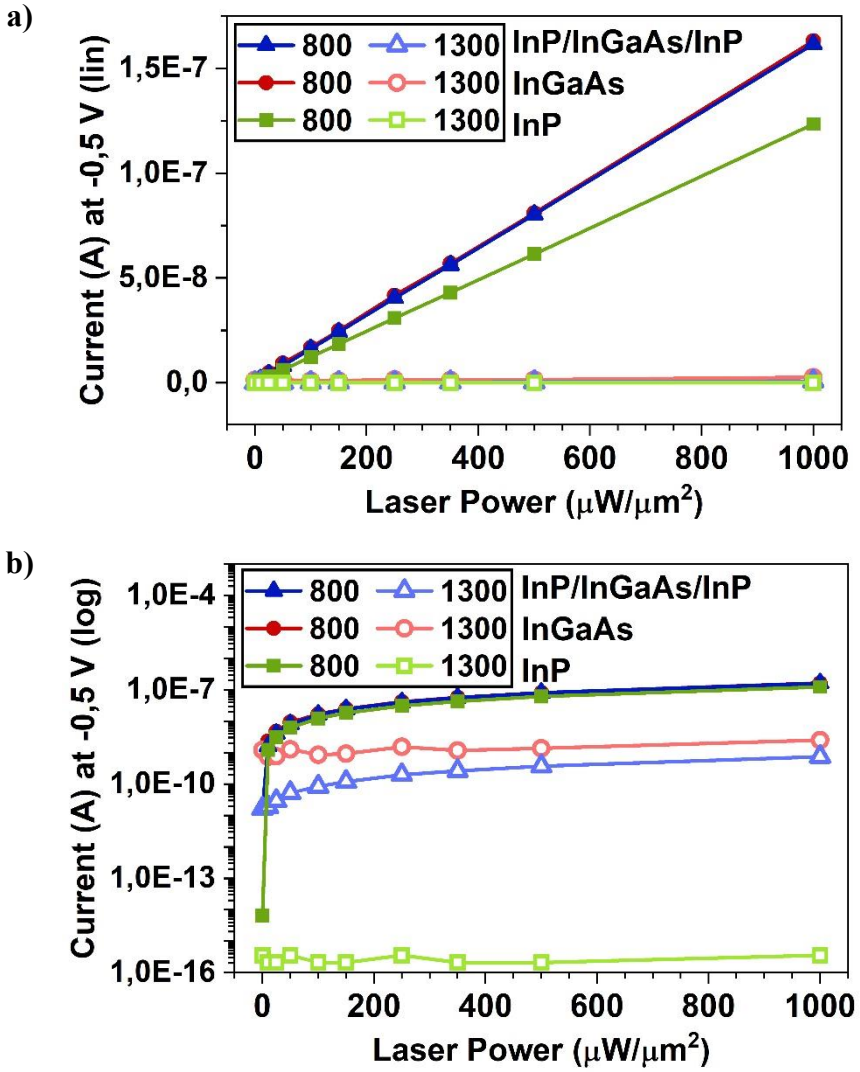


Fig 2-7. Current response in a) linear and b) logarithmic scale as a function of the laser power for the fully InP device, the fully InGaAs device and the InP/InGaAs/InP heterostructure, for wavelengths of 800 nm and 1300 nm.

To better illustrate the trend observed in Fig 2-7, the I-V curves were plotted at four different laser powers and two different wavelengths for the three studied structures (Fig 2-8a) [59]. As an additional study, a fully silicon nanowire was simulated to compare III-V and type IV semiconductors. The I-V curves for Si are shown in the bottom graph of Fig 2-8b.

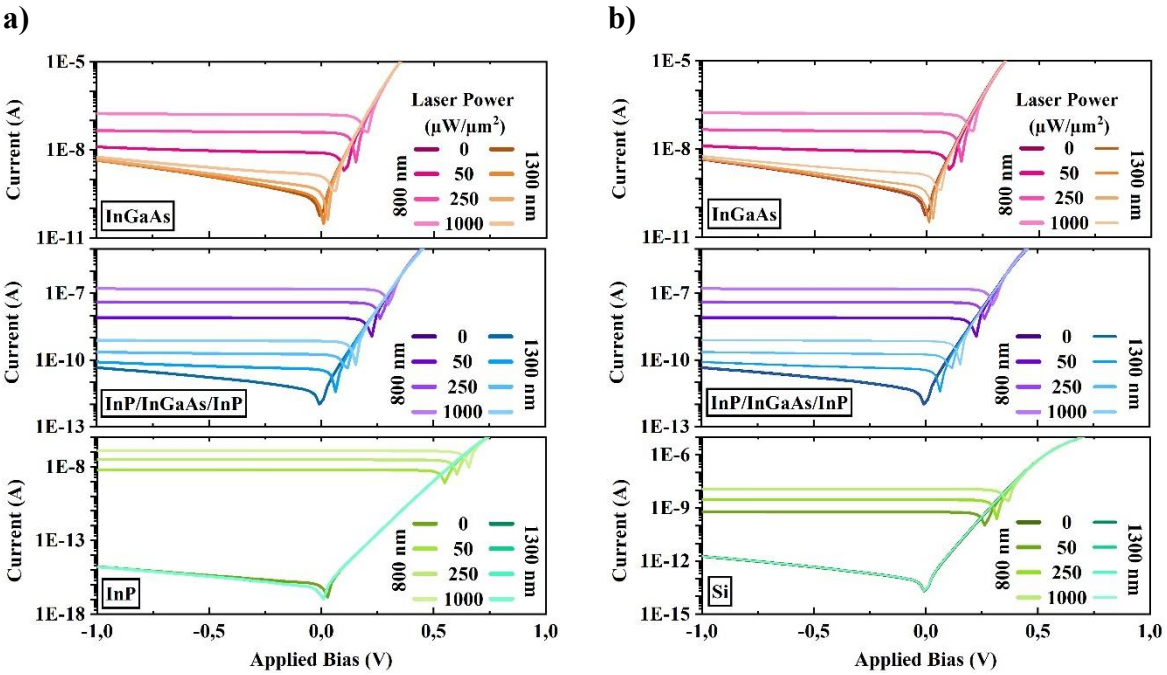


Fig 2-8. Simulated I-V curves at four different laser powers and two different wavelengths a) for the three studied structures (InGaAs and InP homojunctions and InP/InGaAs/InP heterostructure) and b) comparing them with silicon instead of InP.

The benefit of the larger bandgap of InP and Si is evident in the graphs of Fig 2-8, as they show a much lower dark current compared to their photocurrent. In general, the InGaAs NW shows higher values of current, which has the advantage of being in a measurable range when it comes to normal noise levels in probe stations. However, there is not a big change in current at higher wavelengths, so incident photons are not well detected. For the heterostructure, the InP barriers result in a reduced dark-current compared to the fully InGaAs device, with a value in between the two homostructures, while still reaching roughly the same photocurrent values as the pure InGaAs device [59]. This provides enough dark/photocurrent difference to be used as a photodetector, and in a measurable range of currents.

The band diagrams for the three nanowire structures together with their electron and hole densities at -2 V of applied bias are shown on Fig 2-9. As the heterostructure nanowire is made from two different materials, the band structure shows a step-like profile at the interface between the materials. This step explains the behaviour of the electrons and holes in the two plots below. The InP nanowire has its lowest density of electrons on the p side and of holes on the n side. However, even though the p and n regions of the heterostructure are also made of InP, the number of electrons and holes remaining in those areas is higher. This is due to the energy barriers that both electrons and holes cannot surpass easily [59].

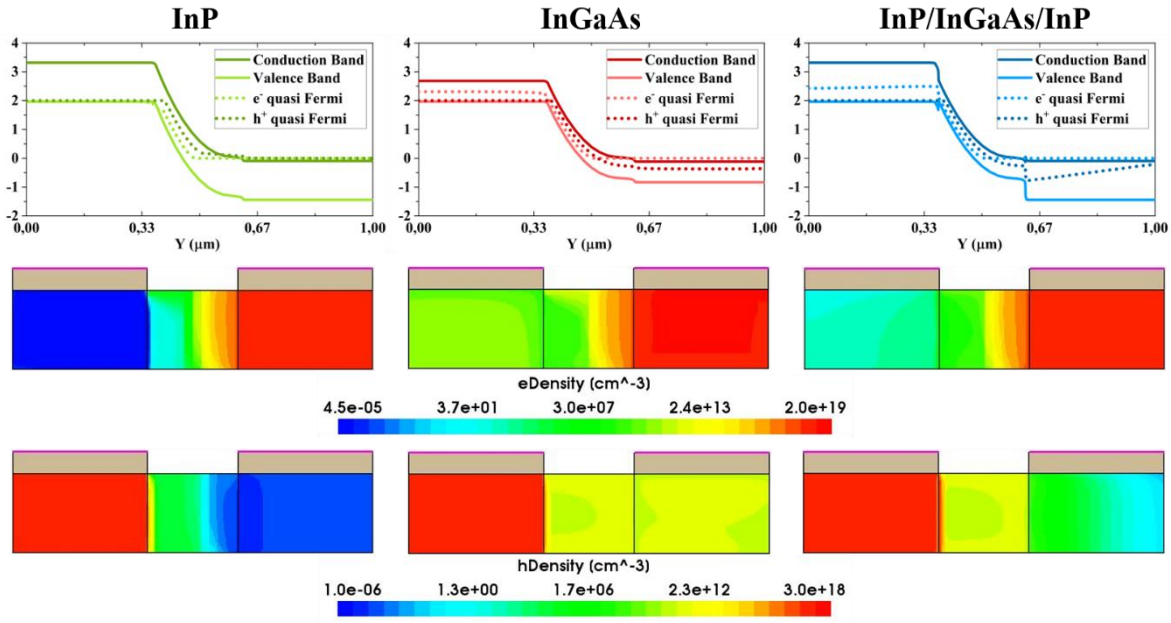


Fig 2-9. Top row: the band diagrams for the three nanowires along the length of the devices. Middle row is their electron density. Bottom row is the hole densities. All simulations are presented at -2 V of applied bias [59] reproduced with permission © 2021 IEEE.

2.3. Study on traps

The following study focused on incorporating traps into the device simulations. The objective was to match simulations with experimental data provided by IBM, which involved p-InP/i-InGaAs/n-InP devices. Fig 2-10 shows a comparison between the I-V curves of the experimental devices and the simulated devices without traps. When aligning experimental data with simulations, it is essential to focus on the shape of the curves rather than their absolute values, as certain parameters from the experimental devices are not fully captured in the simulation model.

The vertical position of the curves can be influenced by factors such as random dopants incorporated from the experimental setup during growth, device interface roughness, and properties resulting from material intermixing during the growth process. Additionally, key parameters affecting the I-V curves include series resistance and the capacitance of the photodiode. These comprise the diode's intrinsic resistance and capacitance, as well as the contact resistance and parasitic capacitance. The latter, which depend on the metal contacts, are not accounted for in the model and can affect both the vertical position and shape of the I-V curves, i.e. the linearity in the diode’s response

In an ideal diode, the I-V characteristics follow the equation presented in section 1.4 (equation 1.3), with the ideality factor (n) being equal to 1. Deviations from this ideality result in lower values of n. Trap levels in the device are another factor that can influence the ideality factor and, subsequently, the shape of the I-V curves. This study focuses on how these traps impact the shape of the curves and how their inclusion in the simulated diodes can explain the observed deviations.

Consequently, to account for the inability of the model to capture some of these properties, the simulated curves were vertically adjusted to be on top of the experimental ones and facilitate the comparison of their shapes. In the case of the simulated curves from Fig 2-10, they correspond to the I-V characteristics of an ideal diode.

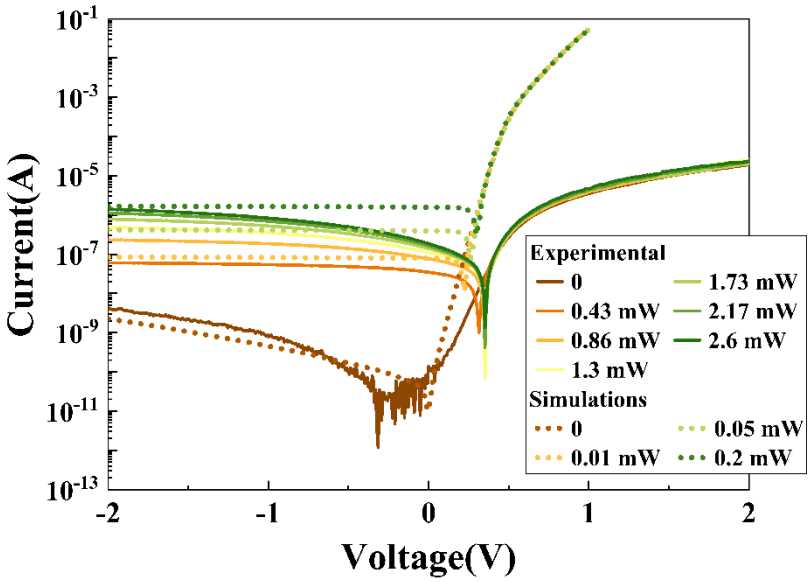


Fig 2-10. I-V characteristics of a fabricated photodiode (solid lines) in the dark (brown) and with different laser powers applied. Simulated I-V characteristics of an ideal photodiode (dotted lines) in the dark (brown) and with different laser powers applied.

To be able to obtain results with higher convergency values, the mesh in the NW and at the interfaces was refined and a layer of 5 nm SiO_2 was added around the NW (Fig 2-11a). The areas where the traps were introduced are in the bulk of the NW (InP and InGaAs regions), at the interface between the different regions (p/i and i/n interfaces), and at the surface of the NW (between the NW and the oxide around it). This was done in dark current for different concentrations of traps, trying only to match the experimental I-V curve without applied light. The results can be seen in Fig 2-11 where Fig 2-11b shows results for bulk traps, Fig 2-11c for interface traps and Fig 2-11d for surface traps.

As seen in the graphs, all the types of traps tend to increase the dark current values and decrease the forward bias ones, which are deviations from the ideality of the diode's response. This is because traps tend to induce e^--h^+ recombinations as they create extra energy levels in the middle of the gap. For the reverse current, as electrons and holes try to tunnel through the band gap, extra energy levels help to promote this process. This behaviour can also be observed experimentally in [61], where the authors measure the I-V curves for fresh and aged samples.

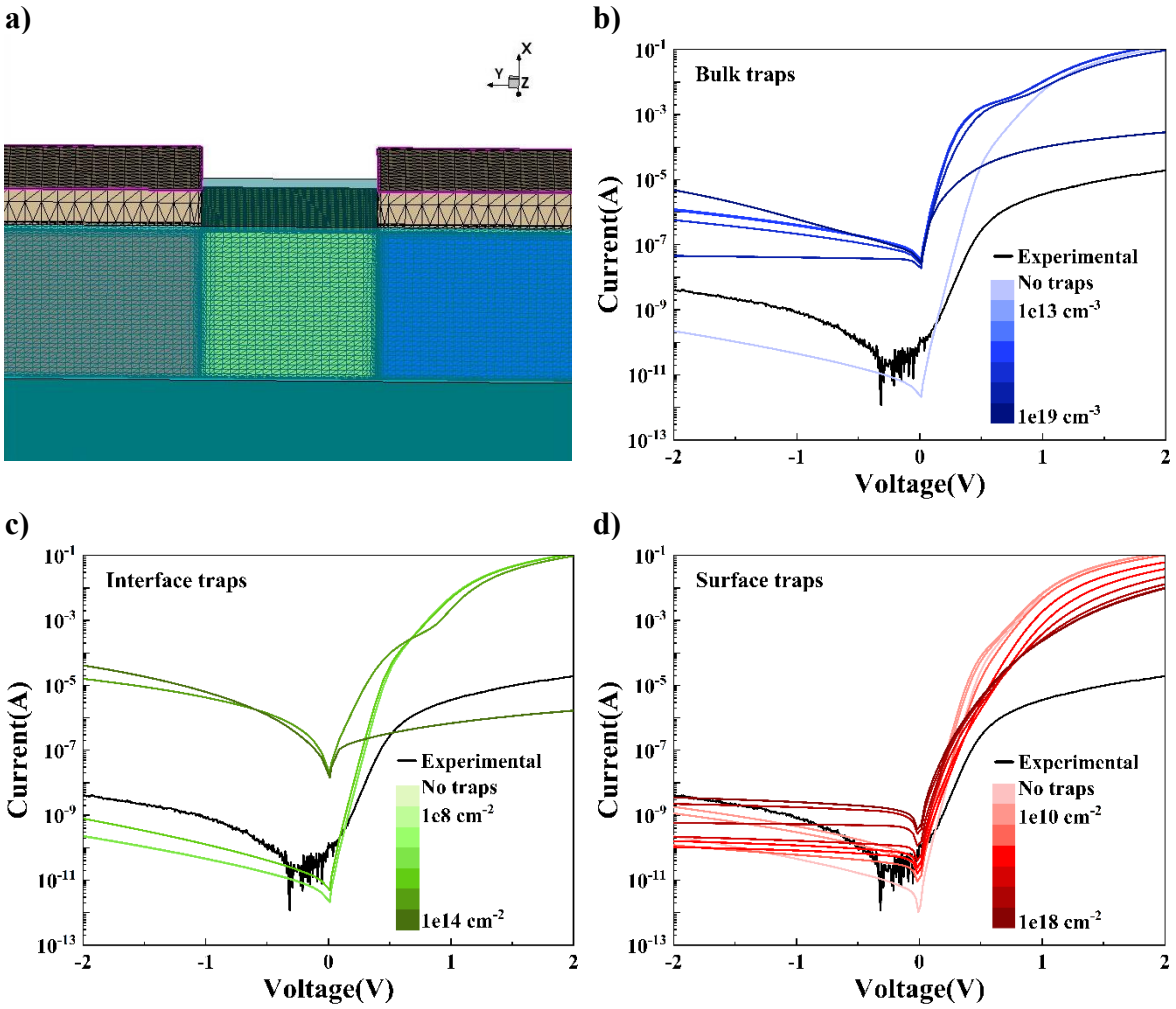


Fig 2-11. a) Image of a section of the simulated NW where the surrounding oxide is in transparent blue and the mesh can be seen on the NW regions (blue for p-InP, yellow for i-InGaAs and red for n-InP) and on the metal contacts. b), c) and d) Comparison of the experimental I-V curve without applied light (black) and the I-V curves for the simulated devices with different concentrations of b) bulk traps, c) interface traps and d) surface traps.

After these results and observing the variability in these three locations of traps, a study was undertaken to assess the I-V curves when different combinations of trap locations are considered. This can be seen in Fig 2-12, where the variability increases even further when taking into account the different surfaces independently and combining them with bulk and interface traps.

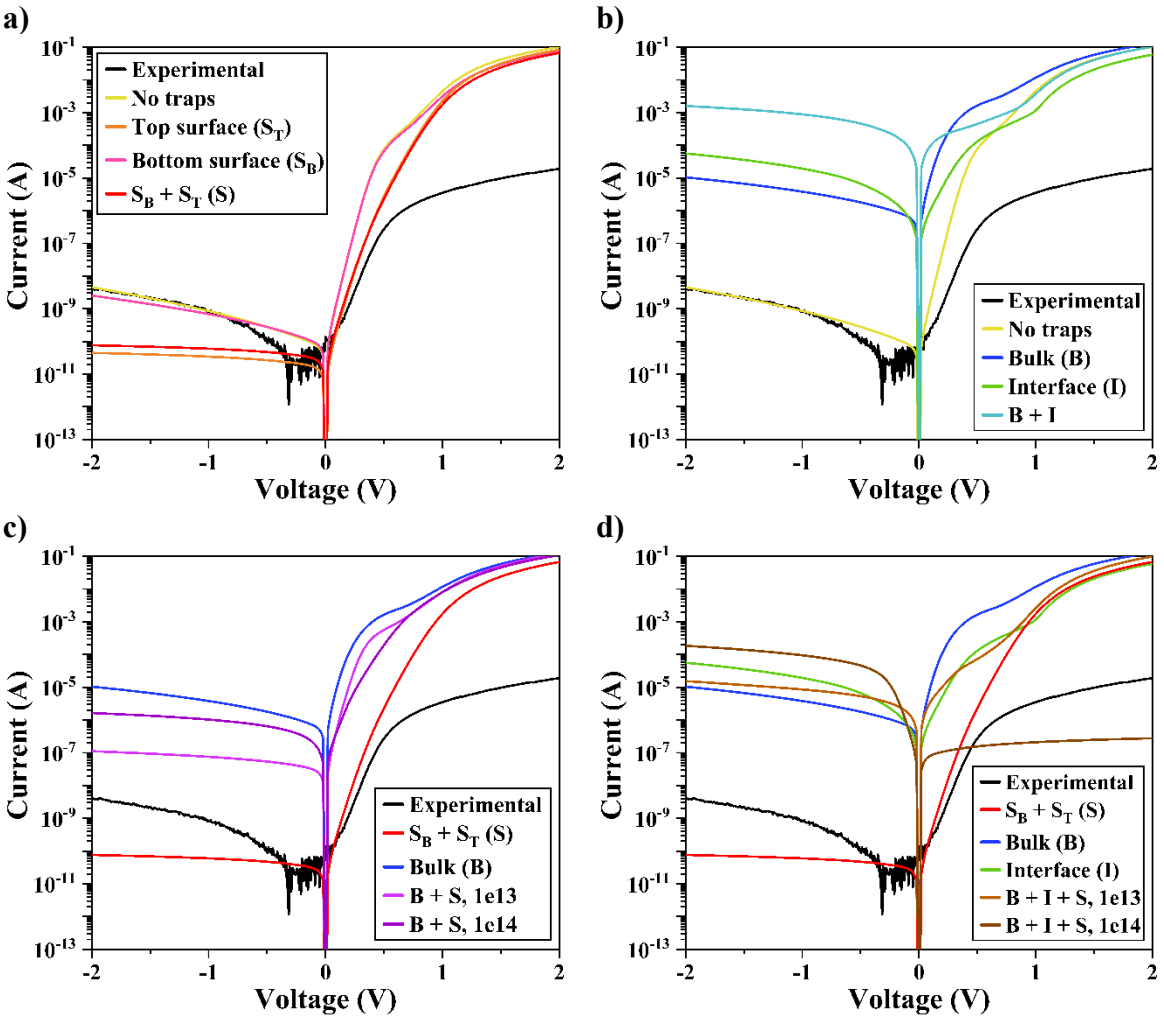


Fig 2-12. I-V curves from experimental (black) and simulated devices with no traps (yellow), and different locations of traps: a) the top surface of the device on the interface with the oxide around it (orange), the bottom surface of the device on the interface with the oxide around it (pink), both top and bottom surfaces (red), b) in the bulk of the device (blue), on the interfaces between the InP and the InGaAs (green), both on the bulk and the interfaces (cyan), c) both bulk and surfaces with a concentration of 1e13 cm^{-3} and 1e13 cm^{-2} respectively (light purple) and with a concentration of 1e14 cm^{-3} and 1e14 cm^{-2} respectively (dark purple), and d) with bulk, interface and surfaces traps altogether, with concentrations of 1e13 cm^{-3} and 1e13 cm^{-2} respectively (light brown) and with concentrations of 1e14 cm^{-3} and 1e14 cm^{-2} respectively (dark brown), as specified in the legends.

From Fig 2-10 it was already evident that the curve without traps (in yellow in Fig 2-12a and b) aligned well with the experimental dark current, but the on-current followed ideality. Fig 2-12a shows that traps on the bottom surface of the device have minimal impact on current since they are far from the conducting path. In contrast, traps on the top surface significantly affect the device's characteristics by reducing dark current. This reduction is likely due to the capture of charge carriers that would otherwise contribute to the dark current.

From Fig 2-12b it can be observed that interface traps have a slightly greater effect on both the on and off currents than bulk traps. When both types of traps are present, the device exhibits a more resistive response. Fig 2-10c and d show that when surface traps are combined with interface and bulk traps, the latter exert a stronger influence, as the I-V characteristics of these combinations resemble those of interface and bulk traps. Additionally, it is evident that the higher the concentration of traps, the more pronounced their effects on the device's performance.

A light source was also applied to the simulations for the three trap locations studied previously. The results can be seen in Fig 2-13, where the black-grey lines are the experimental results for different laser powers, the blue lines are for bulk traps simulations, the green lines for interface traps, and the red lines are for surface traps simulations, all of them performed at different laser powers.

The increased dark current previously observed in Fig 2-12 for devices with bulk and interface traps suggests that the dark current-photocurrent ratio will decrease when these types of traps are present. This is particularly evident for bulk traps, as shown in Fig 2-13. The device with surface traps shows the highest photoresponse. However, it should be noted that the concentration of surface traps in these simulations is relatively low. As previously demonstrated in Fig 2-11d, increasing the concentration of surface traps results in the device exhibiting more resistive behaviour, which could diminish its overall performance.

A closer look on the I-V curves in Fig 2-12 revealed that the best match with the experimental curve, in terms of their shape, are those incorporating both bulk and surface traps, represented in light and dark purple. Different concentrations of this combination of trap locations were simulated to try to refine the fit, as shown in Fig 2-14. However, given the number of variables involved, it is not possible to uniquely match the experimental data in a way that provides a reliable description of the trap distribution. As such, even achieving a perfect fit with the experimental data does not fully explain the device's electrical behaviour.

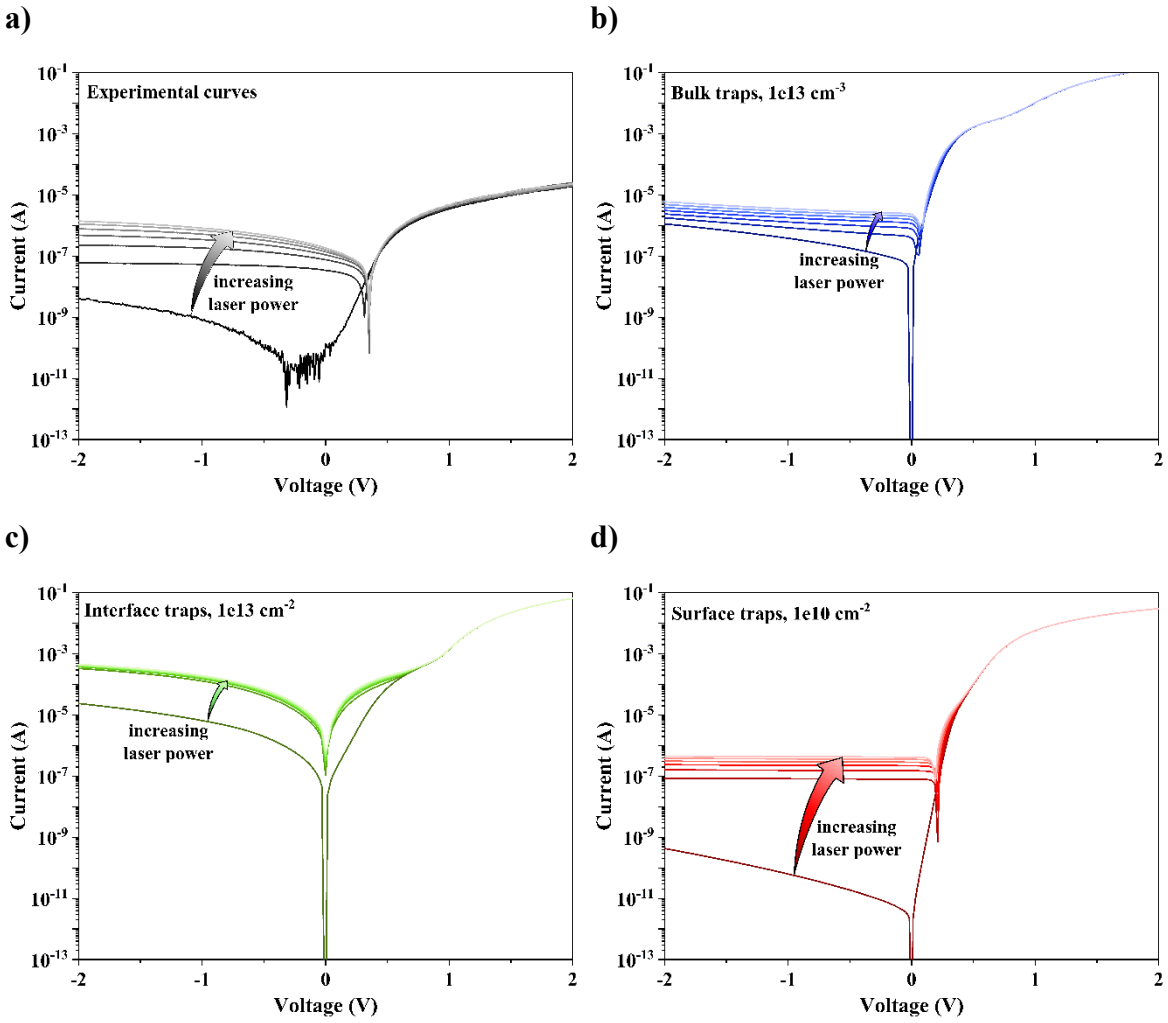


Fig 2-13. I-V curves with increasing laser power from a) experimental and b) - d) simulated devices with different location of traps: b) bulk (1e13 cm^{-3}), c) interface (1e13 cm^{-2}) and d) surface (1e10 cm^{-2})

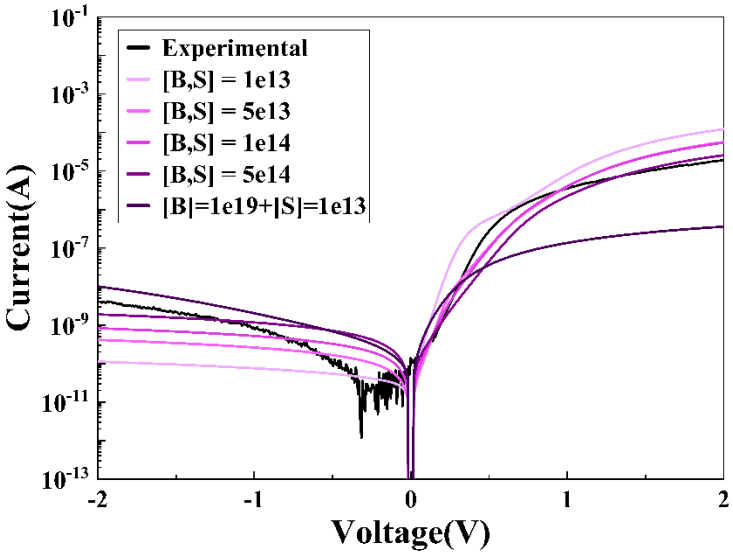


Fig 2-14. Comparison of the experimental I-V curve without applied light (black) and the I-V curves for the simulated devices with different concentrations of bulk and surface traps.

It is evident from the data provided that traps play a significant role in these scaled devices. However, due to the limited availability of experimental devices and the significant variation in I-V curves among those provided during the simulation phase of this project, the decision was made to fabricate additional devices with a wide range of dimensions. This approach aimed to establish a statistical foundation for a more detailed and accurate calibration of the simulations.

The research on this thesis started with the results presented in this chapter, where III-V photodetectors were simulated using Sentaurus TCAD. The first study performed on the III-V materials of interest in this study identified the heterostructure (n-InP/i-InGaAs/p-InP) as the most effective for optimising optical performance compared to simpler heterostructures like pure InP or InGaAs.

A subsequent study was performed on the role of mid-bandgap traps in different areas of the device. Their impact on the ideality of the device can be observed on the I-V characteristics presented, where both the on and off currents deviate from the linearity of the diode's response. This study emphasised the impact of mid-bandgap traps on device performance due to generation-recombination effects.

3. Fabrication of III-V photodetectors

This chapter introduces the integration techniques of III-V materials onto silicon, with a particular emphasis on Template-Assisted Selective Epitaxy (TASE), the method used to fabricate the photodetectors in this project. A step-by-step explanation is provided on achieving fully functional devices. The initial TASE devices primarily consisted of vertical nanowires covered and refilled with III-V materials [62]. TASE has since been applied in various fields, including tunnel field-effect transistors (TFETs) [63], solar cells [64], lasers [65] and photodetectors [48, 60].

The first horizontal photodetectors fabricated using TASE focused on low-capacitance, high-speed performance, consisting of 60 nm thick InGaAs p-i-n detectors. These became the first demonstration of high-speed data reception using ultra-scaled III-V photodetector [48]. However, despite being directly coupled to a silicon nanowire, these devices were too thin to support a propagating mode, and the metal contacts on top would have induced absorption losses.

A second demonstration of TASE's potential for photodetectors was presented in 2022, involving devices like those in this work: 220 nm thick p-InP/i-InGaAs/n-InP waveguide coupled photodetectors, which were thermally and optically characterised [60]. Different waveguide coupling schemes were explored, with T-shape coupling identified as the optimal configuration. However, due to a lack of reproducibility across devices, a full comparison was not possible.

The work presented in this thesis builds on this previous research by providing statistical data for TASE-fabricated photodetectors to better understand the various parameters influencing their performance. This chapter presents the different fabricated devices (straight, funnel, and waveguide-coupled designs), while addressing challenges such as optimising p-doping and the solutions implemented to achieve III-V p-i-n photodetectors. The large number of fabricated devices provides the statistical data necessary to analyse their electrical and optical characteristics.

3.1. III-V on Si integration techniques

There is great interest in the integration of high quality III-V compound semiconductors either monolithically or heterogeneously on silicon to exploit their complementary properties and, in particular, the direct bandgap of III-Vs for opto-electronic devices densely integrated with CMOS [1, 37]. However, lattice, thermal and polarity mismatch between the materials makes epitaxial growth of III-V compounds on silicon challenging [46, 66, 67].

As mentioned in section 1.3, the lattice match between InP and InGaAs depends on the In to Ga ratio in the latter, which has been chosen to avoid any mismatch. However, both III-V materials have a mismatch of around 8% with Si (see Fig 1-1). This mismatch will cause strain at the interface, promoting the formation of defects that could alter the optical properties of the III-V layers and be prejudicial to the performance of the devices.

Another important consideration when integrating materials is the thermal expansion coefficient. Growth techniques typically involve high temperatures, and, during cooling, thermal stress can be induced in the interfaces if the coefficients do not match. Since the thermal expansion coefficient of Si ($2.59 \cdot 10^{-6}$ °C^{-1}) is closer to that of InP ($4.75 \cdot 10^{-6}$ °C^{-1}) than of $In_{0.53}Ga_{0.47}As$ ($5.66 \cdot 10^{-6}$ °C^{-1}), less thermal stress would be induced when growing InP on Si [68]. In this project, however, a higher selectivity of InGaAs on Si was observed, requiring the addition of an InGaAs seed layer in the fabrication process to reduce the InP parasitic growth on the SiO_2 surface of the sample. One way to minimise the thermal stress is by optimising the growth temperature.

The polarity mismatch occurs because III-V materials contain two or more atomic species and crystallise mainly in a cubic lattice. Due to the crystallographic structure of Si and the fact that surfaces are not atomically flat, the nucleation and growth of III-V materials will result in the formation of III-III and V-V bonds if mono-atomic layer steps are present. These types of defects, known as antiphase boundaries, can carry a high charge and negatively impact device performance. An overview of these defects is shown in Fig 3-1.

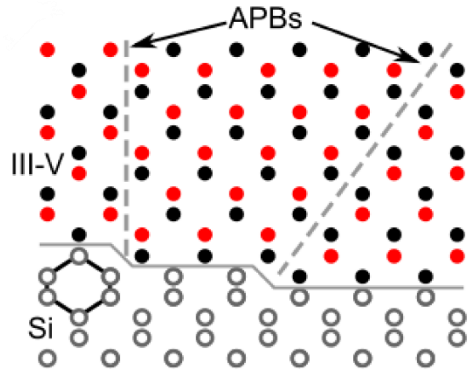


Fig 3-1. Schematic of antiphase boundaries defects at atomic steps of the Si substrate. Figure modified (cropped) from [69] under the terms of the CC BY 4.0 license [70].

An approach to reduce the impact of the mismatch issues is growing the devices with the shape of a nanowire (NW). The interface between this nanostructure and silicon is small enough to accommodate a local expansion or shrinking of the lattice spacing without generating defects, thereby producing high quality crystalline materials despite the lattice mismatch. [48]. The ability to integrate non-lattice matched material combinations in the NW geometry also makes them interesting as building blocks for any type of opto-electronic devices such as solar cells, lasers, field-effect transistors and, of course, photodetectors [71, 72, 73, 74].

The majority of existing techniques for growing NWs produce them vertically orientated, which requires having to transfer them individually to arrange them horizontally [74, 75] or having vertical devices [37, 76, 77]. Different ways to approach the fabrication of NW photodetectors include: growing III-V semiconductors on top of another lattice-matched III-V material substrate [74, 76], using catalytic Au particles [75], or a III-V selective area [37, 77] on top of a Si substrate.

These NW techniques are sufficient for laboratory-sized device fabrication, but they are not ideal for large-scale production. This section provides an overview of various integration techniques for III-V semiconductors onto Si, categorised into two broad groups; heterogeneous and monolithic integration techniques. A schematic of some of these techniques is shown in Fig 3-2. A detailed explanation of the technique used in this project is provided in section 3.2.

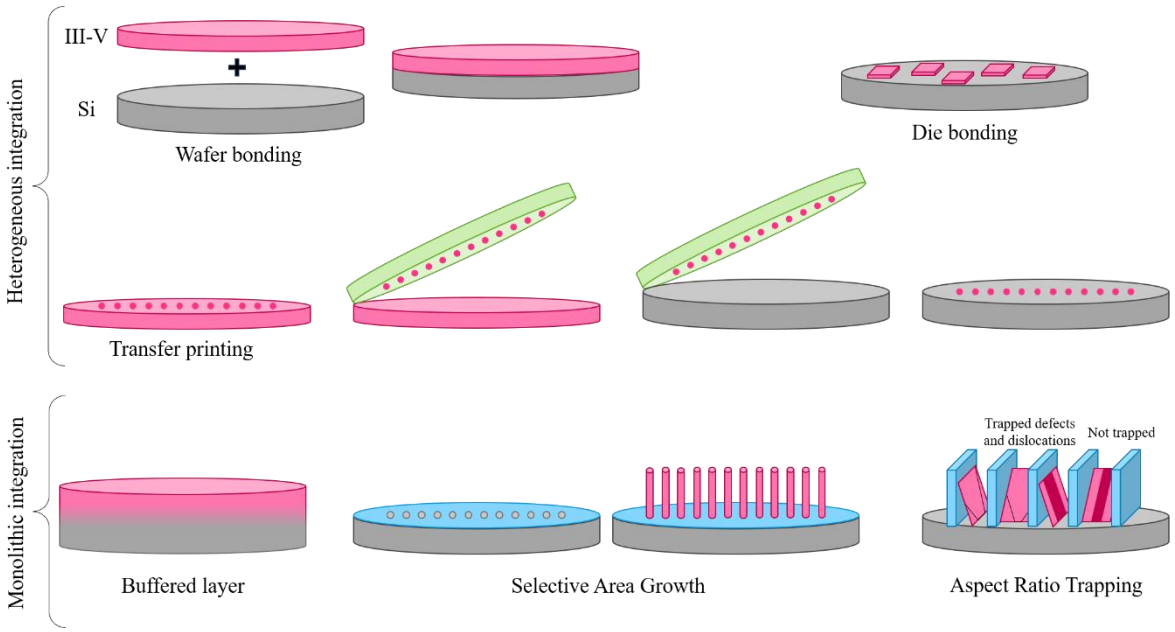


Fig 3-2. Schematic of some integration techniques of III-V on Si. The heterogeneous integration techniques include wafer bonding, die bonding and transfer printing. The monolithic integration techniques include buffered layer, selective area growth (SAG), and aspect ratio trapping (ART)

3.1.1. Heterogeneous integration

Heterogeneous integration methods involve growing III-V materials on a different substrate, typically one that is perfectly lattice-matched, and then transferring them onto the desired silicon wafer [78]. The lattice-matched substrates enable perfect epitaxial growth and reduce defects in the final structures, with the best-performing structures selected for transfer. These techniques have demonstrated excellent results for PD performance [79, 80]. They are well-established in industry because they can be optimised separately without needing to disrupt or adapt current CMOS lines, only adding an extra bonding step at the end [40, 81]. However, transfer methods lack nanometre-scale precision [81] and may result in transfer-related defects [82] or irregular geometries due to the required bonding temperature. Additionally, maintaining CMOS standards can make these new techniques more expensive. For full optical links, the final structures being on a different layer than the silicon requires the light to be coupled into the top layer, reducing the efficiency of light transmission.

- Wafer and die bonding. These methods consist of joining the desired wafer or several die onto a Si wafer. The joined platforms may already have structures on them or could be completely flat, requiring patterning after they form a unified structure. There are several techniques for wafer and die bonding depending on the type of bond used, sometimes incorporating an additional adhesion layer [83, 84]. Post processing steps are usually required, such as annealing to strengthen the bonds between the wafers or etching to remove the bottom layer of a sacrificial wafer [85].

- Transfer printing. In this method, the grown structures are removed from the original substrate using techniques such as peeling or chemical etching onto a typically flexible material. This material is then used as a stamp to align and transfer the structures onto the target substrate [86, 87].

3.1.2. Monolithic integration

Monolithic integration techniques consist of epitaxially growing the III-V materials directly onto the silicon substrate. They address the drawbacks of heterogeneous integration by offering high precision, shorter fabrication times, and lower costs. However, they lack the benefits of lattice-matched substrates and the ability to select only the best devices.

The lattice mismatch between III-V materials and silicon presents a significant challenge in these fabrication methods, as defect formation negatively impacts the performance of electronic and photonic devices. Moreover, growth parameters such as temperature may need to be adjusted to align with existing CMOS processes, which might compromise the final product. However, integrating the III-V fabrication process into CMOS lines could reduce the cost of final devices by eliminating the need for specialised facilities.

- Buffered layer growth. A uniform layer of the crystalline III-V material is deposited over the entire Si wafer, resulting in a uniform layer that can later be etched to obtain the desired structures. This technique aims to grow a sufficiently thick layer to trap defects at the bottom and create a top layer with a very low defect density, enabling the fabrication of high-quality optical devices [88, 89, 90, 91]. Annealing the epitaxial layer helps reduce the number of defects caused by the mismatch with the underlying wafer.

However, depending on the mismatch between the III-V material and Si, a second buffer layer might be needed to reduce defects, potentially resulting in buffer layers that are too thick for close integration with the Si electronics below [92, 93]. Additionally, annealing can cause wafer bending (bow) due to the thermal expansion coefficient mismatch [94].

- Selective Area Growth (SAG). This technique consists of growing the III-V materials in a designated area. By masking the Si wafer and patterning the mask, small nucleation openings are exposed to promote the growth of III-V materials in precise positions. The final structures typically take the form of nanowires, which can be comprised of a single material or exhibit different doping profiles and heterostructures, either radially or vertically [95, 96, 97]. Due to the small interface with the Si seed, the defects are locally contained and do not spread further [89]. However, this technique often results in vertically oriented NWs, potentially requiring a pick-and-place technique for their transfer.

- Aspect Ratio Trapping (ART) techniques. This epitaxial approach confines defects close to the seed by using high aspect ratio oxide trenches. During growth, defects along specific crystallographic planes terminate at the oxide sidewalls, allowing dislocation-free material to grow out of the cavities [98]. Unfortunately, the geometry of the grown structures is limited, and large templates are required. Additionally, since multiple nucleation points are used, the merging of these areas can result in the formation of grain boundaries, which can negatively impact the performance of electrical and optical devices [99, 100].

- Template Assisted Selective Epitaxy (TASE) is explained in detail in section 3.2. Evolving from SAG and NW growth, TASE uses a precisely defined small nucleation point and an oxide template to guide the growth. Its advantage lies in the precise definition of structures in position and shape on the Si layer, which are then covered by oxide to create templates. These templates are accessed through a small opening, where the Si is etched, leaving only a small seed to nucleate and grow the III-V materials from [101, 102].

TASE allows for growth in any direction and focuses on planar growth, meaning the III-V devices end up in the same layer as the Si electronics. This alignment allows for more efficient integration of the optoelectronics platform [49, 50, 48]. However, being an advanced integration technique involves several complex steps. Multiple fabrication tools and procedures need to be followed, before the growth of the III-V materials, to build and prepare the templates, and after to access the devices for contacting. This can increase the probability of procedural mistake. The growth process can result in parasitic crystal formation on the mask, requiring additional cleaning steps to remove them from the surface of the final chip [103].

Microscopy images exemplifying the capabilities of this technique are shown in Fig 3-3a. IBM has demonstrated the monolithic integration of scaled InGaAs photodetectors on Silicon [50] and is moving towards heterostructure devices. An SEM image of an InGaAs p-i-n nanostructure device fabricated using TASE can be seen in Fig 3-3b.

a) **b)**

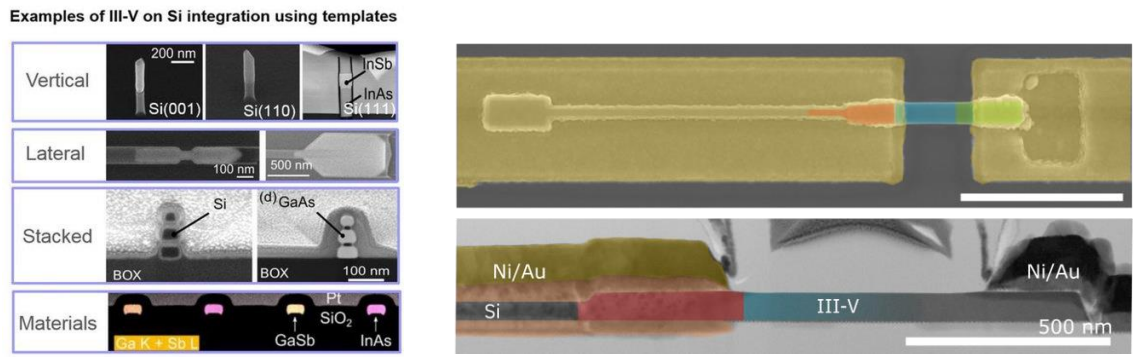


Fig 3-3. a) Demonstration of TASE's capabilities shown through Scanning Electron Microscopy (SEM) images. Figure modified (cropped) from [50], with permission from the Copyright Clearance Centre. b) False-coloured SEM of the top view of a p-i-n nanostructure, with the colours on the device referring to the different doped regions, and a bright field Scanning Transmission Electron Microscopy (STEM) image of a cross section of the nanostructure below. Figure modified (cropped) from [48], under the terms of the CC BY 4.0 license [70].

As mentioned in section 1.2, TASE is the technique used in this project to fabricate the III-V photodetectors integrated on a Si wafer. A more detailed explanation of the steps and tools needed to achieve a final device using TASE is presented in the following sections.

3.2. Monolithic integration of InP/InGaAs photodetectors by TASE

To overcome the integration and growth challenges of III-V materials on Si platforms for optoelectronic devices, IBM developed in 2005 the Template-Assisted Selective Epitaxy (TASE) technology. TASE is a monolithic integration technique that allows the fabrication of nanostructures with varied shapes including nanowires, cross-bars, hexagonal microdisks, platelets, or larger sheets [50, 101, 104, 105]. Different integration schemes are possible, such as lateral and vertical growth directions or even stacked configurations [105, 106, 101], enabling in-situ doping and sharp heterojunctions.

Initially created to overcome integration challenges arising from lattice and thermal mismatches between silicon and III-V materials, TASE was originally intended for electronic applications such as vertical and lateral TFETs, among others [107, 63, 104, 108]. However, its focus has since shifted towards photonics applications, including lasers (microdisks, photonic crystal cavities, topological lattices), LEDs, photodetectors [109, 65, 110, 60], and even quantum computing applications [102].

The epitaxial growth in TASE begins from a single nucleation point on a Si seed and extends into a pre-defined SiO_2 template. These templates provide both direction and shape for the growth, and passivation of the III-V materials by preventing contact with air. As a result, the process means to produce single-crystalline, dislocation-free devices with minimal surface states and defects concentrated at the interface with the seed, contributing to low optical losses in photonic applications.

TASE allows the definition of all silicon features, including electronics, photonic devices, and Si passives, in a single lithographic step, facilitating self-alignment and dense integration of electronics and photonics [111, 112]. The III-V materials ultimately replace the previously defined silicon features, creating a full optical link between electronics and the active and passive components of a photonic integrated circuit (emitter, waveguide and photodetector) [113].

The fabrication steps needed to achieve a fully integrated photonic device on a Si wafer by using TASE are shown in Fig 3-4 and explained below. This process has been previously established; however, the specifics regarding wafer characteristics, design, and growth parameters have been adapted and are specific to this work.

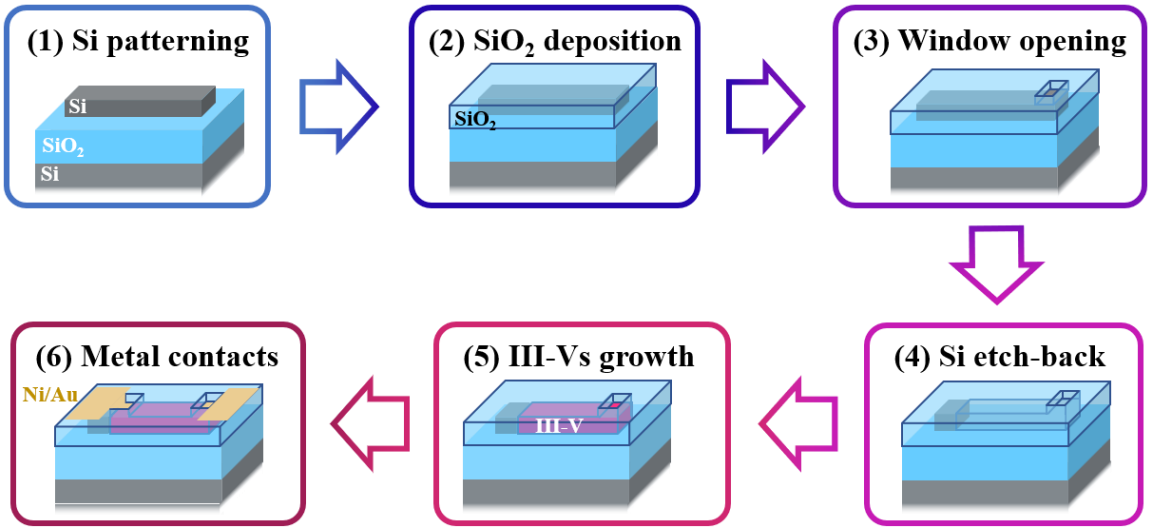


Fig 3-4. Schematic of the steps for the fabrication of photonic devices using TASE. The different steps include (1) silicon patterning of the top layer of an SOI wafer, (2) silicon oxide deposition, (3) window opening on one end of the silicon shape, (4) etch of the silicon leaving a seed, (5) growth of the III-V materials, and (6) deposition of the metal contacts after a second window opening on the other end of the device.

0. **Wafer and design preparation.** The substrate consists of an 8-inch Silicon on Insulator (SOI) wafer comprising a 220 nm Si layer on top of a 2 µm thick Buried Oxide (BOX) layer of SiO_2, sitting on a bulk Si backplate. The top Si layer has a certain crystallographic orientation; in this thesis, (001) and (110) wafers were investigated. These orientations influence the growth of the III-V materials, and the thickness of the top Si layer determines the height of the final devices.

   As the alignment between lithographic steps is crucial, Electron Beam Lithography (EBL) markers need to be added onto the SOI wafer as a pre-processing step. These markers need to be placed on the same layer as the top Si to allow for planarisation of the sample and need to be encapsulated in SiO_2 to protect them from etching agents.

By using optical lithography, trenches are defined and further etched using a Reactive Ion Etching (RIE) technique. A thin layer of SiO_2 is then deposited by Plasma-Enhanced Chemical Vapor Deposition (PECVD) to protect the Si layer before depositing a tungsten (W) layer through sputtering. The tungsten EBL markers provide the high contrast in the SEM imaging needed for alignment during the lithography steps. The final step is the encapsulation of the markers in SiO_2 by PECVD and the dicing of the wafer onto 6 x 6 cm^2 samples, which contain nine identical 2 x 2 cm^2 chips. For the samples prepared during this work, the tungsten markers were added by PhD students Enrico Brugnolotto and Markus Scherrer.

Before starting the process, the design of the chips is made using a software called L-Edit. It is a hierarchical physical layout editor that allows for both coding and drawing the lithography masks. Each 2 x 2 cm^2 chip is arranged in a 7 x 7 grid of cells to focus on different device geometries and designs and increase the variability and statistical data obtained. Some of these designs are shown in Fig 3-5.

Device width is the simplest parameter to vary across the chip surface. Growth rate increases logarithmically with the template width. Narrower NWs take longer to grow because tighter templates and smaller openings make it more challenging for the precursors to enter and reach the reaction surface. Conversely, wider structures require a higher amount of precursors to fill the template channel. For very narrow devices ($\lessapprox$ 50 nm) there is a strong width dependence, whereas for wider devices ($\gtrapprox$ 100 nm) there is no significant dependence of the growth on the device width. Therefore, the studied template widths range from 20 nm to 600 nm.

The funnel devices are incorporated into the design to study the effect of making the intrinsic region smaller while keeping p and n regions large enough to have a good contact. These devices are grown in two different steps to ensure a good quality of the crystal. The joined NWs would allow to investigate how the current scales with 3 and 5 nanowires in parallel. However, only measurements on single NWs were performed during the work of this thesis.

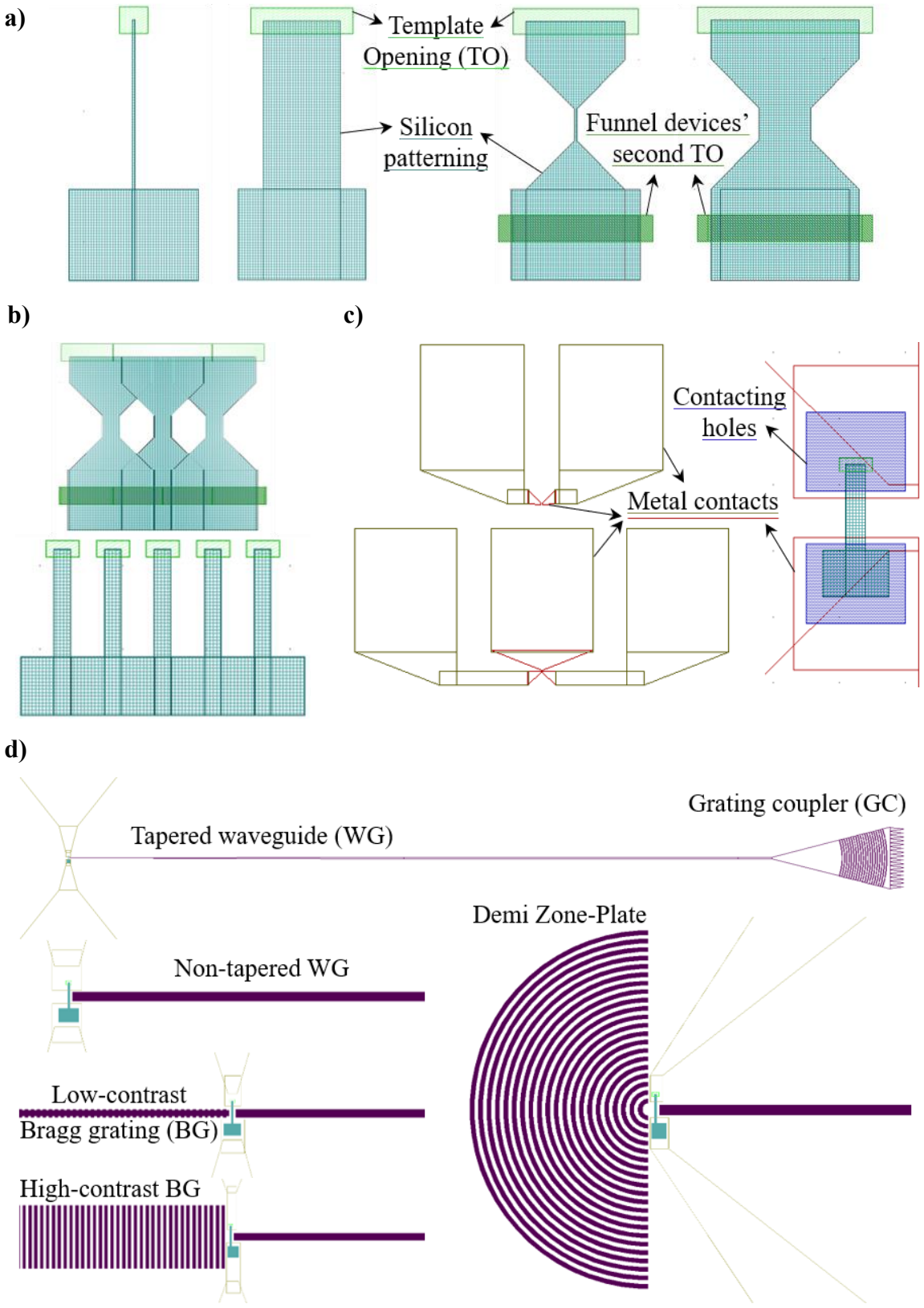


Fig 3-5. Images from L-edit software of the design of the devices. a) Straight and funnel devices with the lowest (20 nm) and highest (600 nm) values of width. b) Three joined funnel devices and five joined straight devices. c) Design of the contacts with 2 and 3 pads and a contacted NW. d) Design of the waveguide coupled devices with tapered and non-tapered waveguides and different mirror designs (a low-contrast Bragg grating, a high-contrast Bragg grating, and a demi Zone-Plate).

The NW designs shown in Fig 3-5 (turquoise) are longer than the final devices as they also include a silicon seed at the bottom and an area at the top to prevent the III-V materials from coming out of the template opening (light green). The funnel devices have a second template opening at the bottom (dark green) to enable the growth of the NW from both ends. The contacts include two differently coloured regions to allow for the definition of different resolutions during the e-beam exposure; a coarser region (golden) and a finer area (red) where the contacts meet the devices. For the desired contacted NWs, an extra area is defined (blue) to etch down the SiO_2 template and reach the devices.

1. **Si patterning.** Once the pattern has been designed, the first EBL step begins, enabling very high resolution and alignment of the structures. The wafer is cleaned in a Piranha solution (H_2SO_4 2:1 H_2O_2) to remove any surface residues. A 100 nm thick layer of Hydrogen Silsesquioxane (HSQ) resist is applied onto the sample via spin-coating, and the final resist thickness depends on variables such as spin-coating time and speed. Pre- and post-bake steps are needed to improve resist adhesion.

   After the exposure of the first layer (turquoise in Fig 3-5), the resist has to be developed. HSQ is a negative resist, meaning the exposed areas harden and become insoluble to the developer. The exposure dose and development time are crucial criteria to ensure the correct geometry and dimensions of the final structures are transferred onto the sample. An EBL technician is in charge of exposing the samples, taking into account resist type and spin-coating parameters.

   By using inductively-coupled plasma RIE (ICP - RIE), the unprotected part of the top Si layer is etched in a hydrobromic acid (HBr) and oxygen (O_2) atmosphere, so that only the patterned structures remain intact. This etching mixture guarantees that the remaining Si structures have straight sidewalls. The sample is then inspected using Scanning Electron Microscopy (SEM), and the resist is removed with Buffered Hydrofluoric acid (BHF) followed by a surface cleaning in a Piranha solution. The resulting structures are shown in Fig 3-6a and b. The test structures added to the design to examine the growth characteristics are shown at the bottom, in Fig 3-6c.

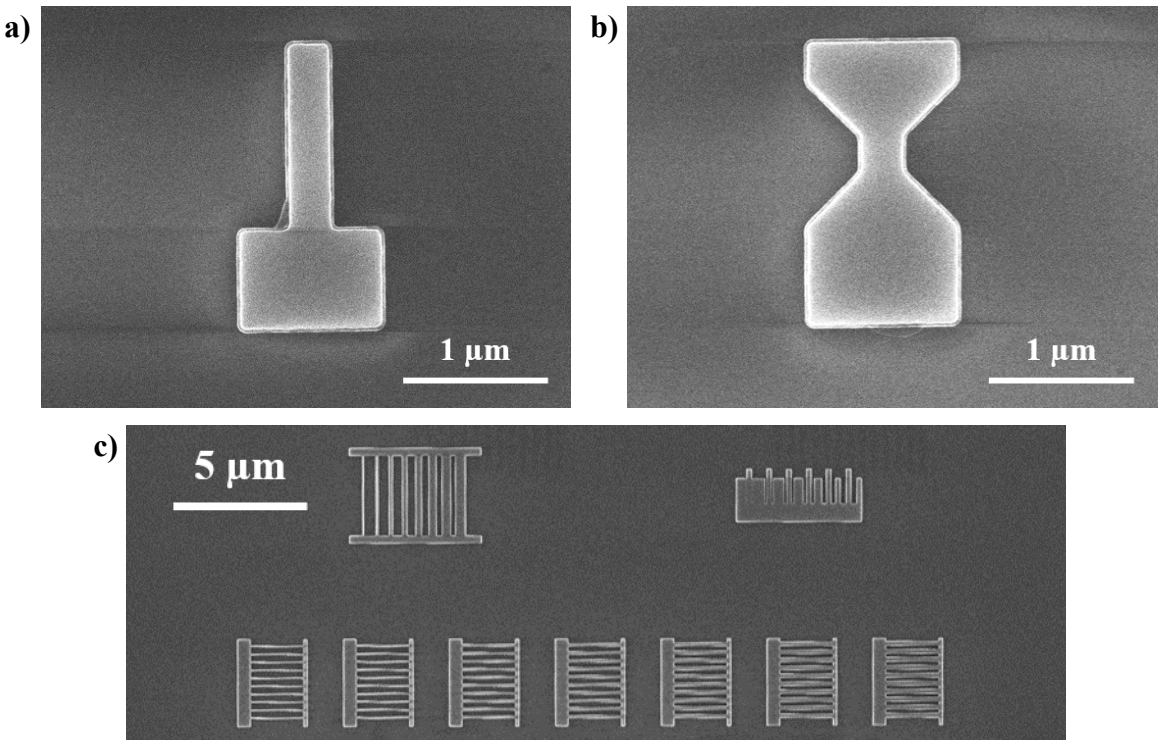


Fig 3-6. SEM images of a) a straight and b) a funnel NWs and c) the test structures after the Si patterning step.

2. **Template deposition.** The next step is to encapsulate the Si structures by depositing SiO_2 in order to create the template inside which the growth occurs. The method resulting in the highest quality SiO_2 is Atomic Layered Deposition (ALD), but this method is also the most time consuming. An alternative method is to use PECVD, and, depending on the precursor used, the resulting layer will have a different morphology. A schematic of the oxide layer morphologies obtained using the three different methods is shown in Fig 3-7.

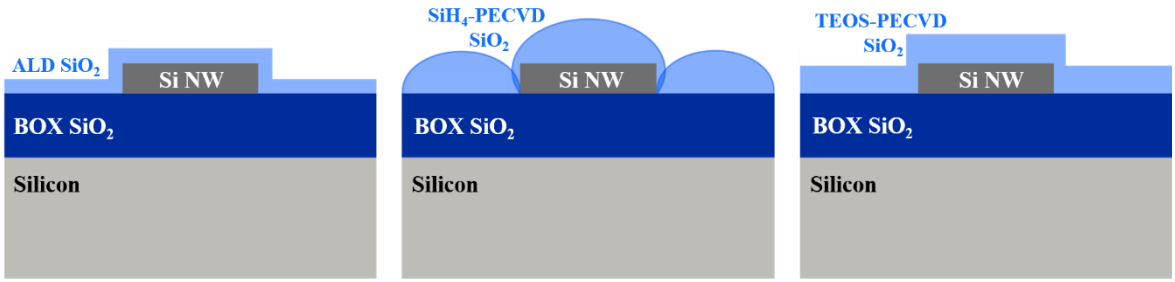


Fig 3-7. Schematic of the resulting SiO_2 layers deposited by ALD (left), PECVD with silane (SiH4) precursor (centre) and PECVD with tetraethoxysilane (TEOS) precursor (right).

As illustrated, using silane as precursor in PECVD for non-planar samples creates a non-uniform layer that will cause a higher etching rate on the edges. Using tetraethoxysilane (TEOS) instead, improves the conformality of the final layer, with a higher thickness on the horizontal surfaces compared with the vertical ones [114].

Considering all the factors discussed previously, it was determined that a first layer of 50 - 100 nm of ALD oxide would be deposited, followed by 300 - 250 nm of TEOS - PECVD. In Fig 3-8 some of the Si structures with the waveguide and mirrors can be seen after the ALD SiO_2 layer has been deposited. An additional top oxide layer, required to create a planar SiO_2 surface, is deposited by spin-coating the sample with HSQ (chemical structure of the polymer $[HSiO_{3/2}]_n$), which decomposes into a SiO_2-like structure via a combination of pyrolysis and oxidation when annealed above 800 °C [115, 116]. Previous investigations conducted by IBM found that a temperature up to 1000 °C was necessary to make the resulting oxide resistant to Diluted Hydrofluoric Acid (DHF), which is required in a following step. A Rapid Thermal Annealing (RTA) tool is used to expose the chip to this temperature. After this step, the oxide layer is thinned down with RIE, and the wafer is diced into nine identical 2 x 2 cm^2 chips.

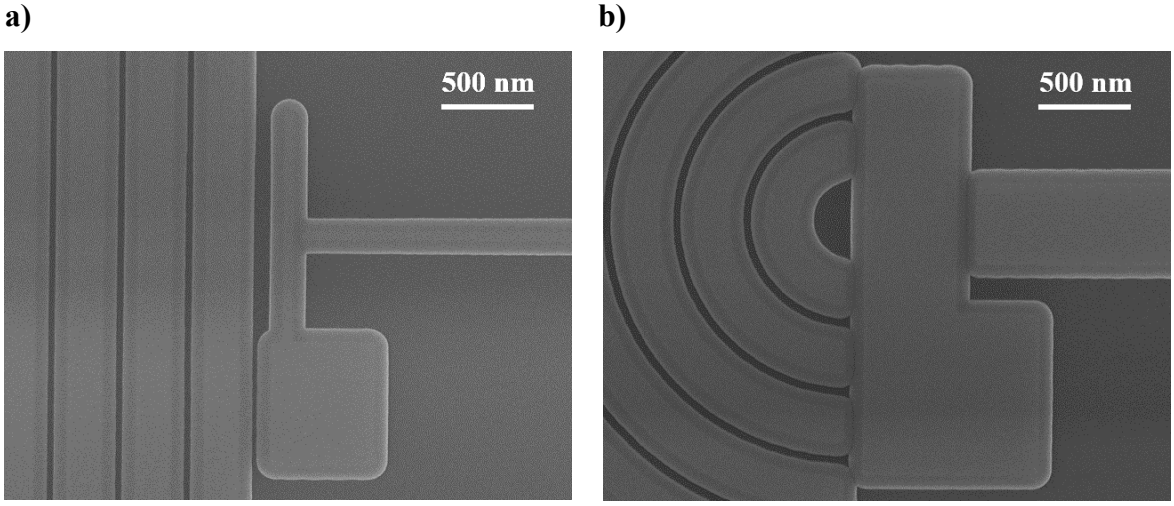


Fig 3-8. SEM images of the WG coupled Si structures with a layer of ALD SiO_2 around.

3. **Template opening.** To proceed with the growth, a hole has to be created to access the Si structures beneath the oxide templates. This is done through a second EBL step, where the template opening holes (light green in Fig 3-5) are patterned. For this step, a Chemical Semi-Amplified Resist (CSAR) is used, which is a positive resist. The exposed area becomes soluble to the developer and is subsequently washed away. The SiO_2 holes are etched through RIE, and the remaining CSAR is removed using a combination of O_2 plasma, Anisole solvent at 80 °C, and hot Piranha solution. The structures after this fabrication step can be seen in Fig 3-9.

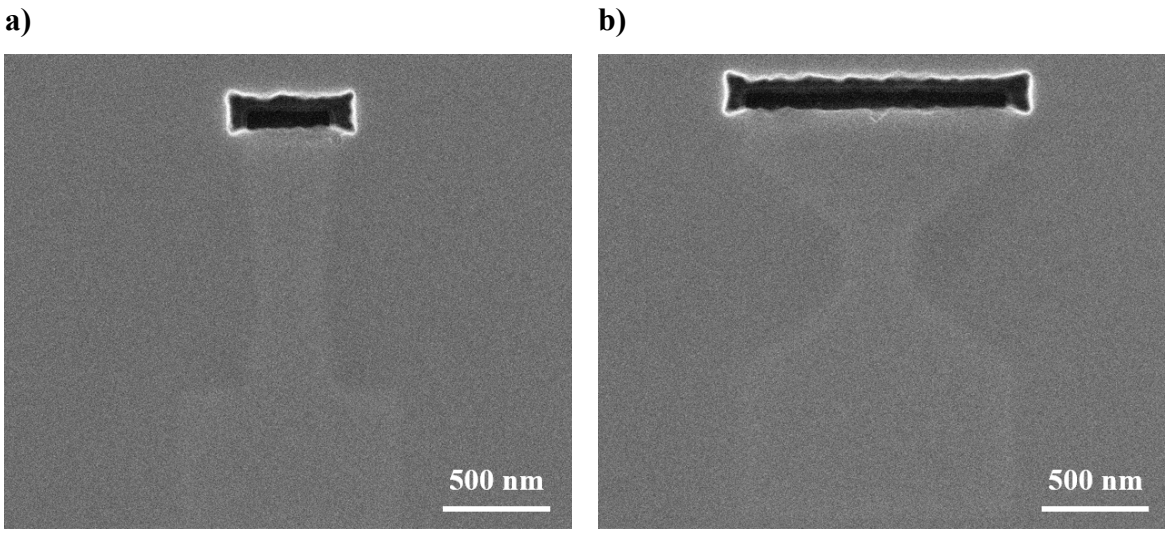


Fig 3-9. SEM images of two buried Si structures with the template opening hole.

4. **Silicon back-etch.** Access to the inner Si structures allows the creation of the hollow SiO_2 templates. As the end of the NWs are exposed, a few nanometres of native oxide form by exposure to air. The first step involves etching away this oxide layer by immersing the sample in DHF for ten seconds. Immediately after, the sample is introduced in a heated solution of tetramethylammonium hydroxide (TMAH), which etches back the Si selectively. The temperature and concentration of the TMAH solution are critical parameters that determine the etch rate of silicon and must be carefully controlled. A 2% TMAH solution is placed in a temperature-controlled water bath at 80 °C, resulting in an etch rate of 60 nm/min for Si. The sample is submerged in the solution and the back etching process is precisely timed to reach the silicon seed, to approximately 18 minutes, leaving a Si{111} facet, which is tilted relative to the (001) wafer surface. Two SEM images of the structures after this step are shown in Fig 3-10. As can be seen, the funnel structure on the right is only etched half way, as the growth for those devices is done in two steps.

5. **III-Vs growth.** At this point in the process, the sample contains the hollow SiO_2 templates that will accommodate the III-V materials forming the photonic devices, with a Si seed to nucleate and start the growth from. To ensure that native oxide does not form on the Si seed, which would prevent the nucleation of the III-V materials, a rapid transfer of the sample from the TMAH solution to the Metal-Organic Chemical Vapour Deposition (MOCVD) chamber is required.

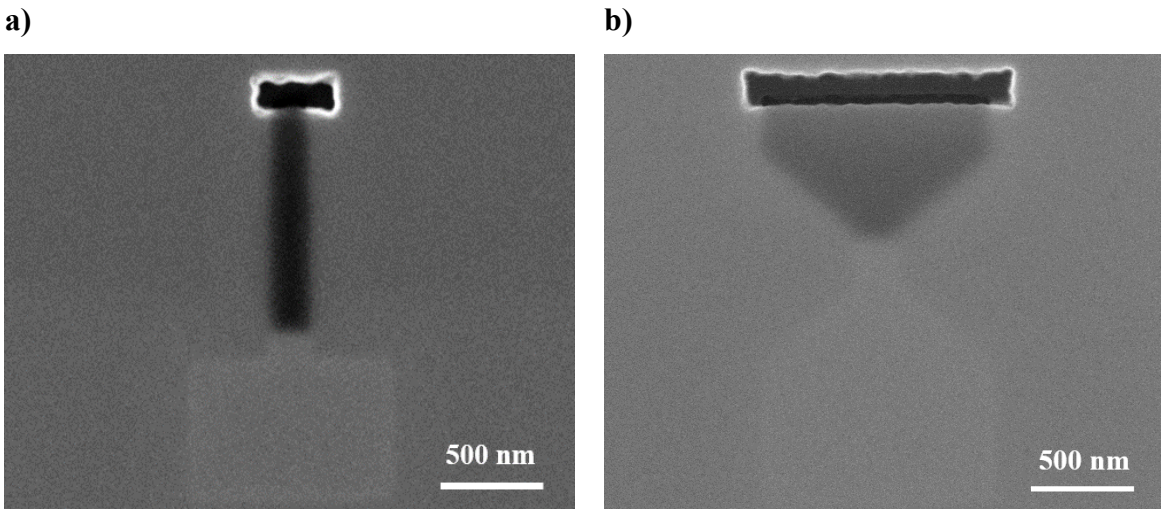


Fig 3-10. SEM images of the empty templates (dark) after the Si etch back. The lighter area corresponds to the remaining Si used for the nucleation of the III-V materials.

The growth of the III-V materials is achieved through MOCVD, a technique where precursor gases for each element of the targeted material are injected into a heated chamber under vacuum. These precursors diffuse through the vapour and along the surfaces until they reach the growth substrate, initiating nucleation and epitaxial growth of the III-V materials in the desired area.

Examples of the precursor gases used in this project for the growth of InP and InGaAs and their n-type (Sn) and p-type (Zn) doping species include: trimethyl indium (TMIn), tert-butyl phosphine (TBP), trimethyl gallium (TMGa), tert-butyl arsine (TBAs), tetraethyl tin (TESn) and diethyl zinc (DEZn). These precursors have been extensively studied for years to ensure they pyrolyse at growth temperatures without decomposing at room temperature, have moderately high vapour pressure, do not participate in parasitic reactions with other precursors, and provide with high-quality materials with negligible carbon contamination [117, 118].

The final growth sequence of the photodetectors in this project consists of i-InGaAs / n-InP (Sn doped) / i-InGaAs / p-InP (Zn doped) / p-InGaAs (Zn doped). The initial InGaAs region was added as a nucleation seed, as InP's selectivity to Si over SiO_2 is not as high. The p-InGaAs region at the end was included in the sequence because p-InP has poor contact resistance with metal contacts.

To achieve ohmic contacts between p-InGaAs and the metal, the hole concentration levels must be over 5e19 cm^{-3} [119]. As demonstrated in the following section (3.2.1), this high concentration could not be achieved by adding the Zn precursor during the growth process, and the III-V materials had to be p-doped by Zn diffusion on a separate MOCVD run.

After the growth process, the samples are inspected using SEM and Energy Dispersive X-ray Spectrometer (EDX), which allows the concentration mapping of the different atomic species, ensuring that each section has the intended length. On the top three SEM images in Fig 3-11 (a, b and c), the difference between InGaAs (lighter) and InP (darker) can be seen, revealing the different growth fronts that can occur when growing III-Vs on a (001) SOI wafer. This contrast arises from the interaction of electrons with the sample, as SEM imaging is influenced by factors such as material composition. In this case, InGaAs appears brighter due to Z-contrast, which results from the atomic mass difference between InGaAs and InP. However, this contrast is not consistently visible across all SEM images of the grown devices, as the SiO_2 layer on top has varying thicknesses depending on the sample and the fabrication step when the image was taken.

The bottom two images in Fig 3-11 (g and h) correspond to an EDX analysis of two different NWs. In these images, phosphorus is indicated in green, representing the InP regions, arsenic in red, and gallium in blue, with the red and blue areas collectively representing InGaAs. Some noise can be observed outside the NW areas, likely caused by EDX background noise and peaks from the SiO_2 substrate that overlap with the elements of interest.

Although the growth of the III-V materials occurs at 580 °C, the sample is first heated to 750 °C to desorb any remaining impurities from the growth surface. This cannot be done before the Zn diffusion run, as the III-V materials would melt and combine, so a maximum of 610 °C is reached before diffusing the Zn at 510 °C. The Zn diffusion process is highly sensitive to time, temperature, and precursor concentration. Higher temperatures reduce doping levels in the material, and prolonged exposure at lower precursor concentrations would cause the Zn to diffuse too far into the NW, resulting in extensive p-doping [120]. The optimal diffusion time determined in this project to exactly reach the p-InP region and achieve ohmic contacts on the p-InGaAs is two minutes.

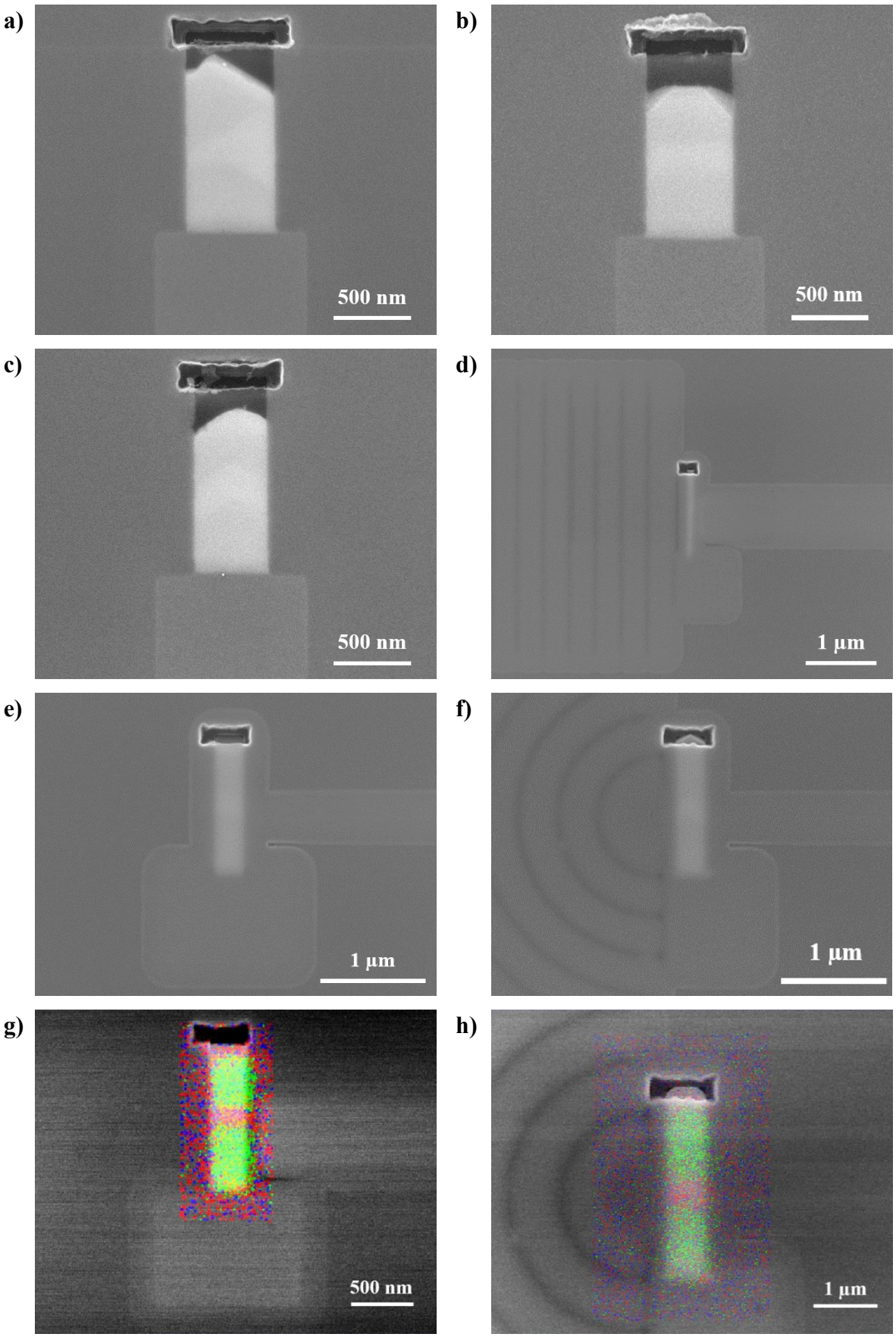


Fig 3-11. SEM (a-f) and EDX (g-h) images of p-InGaAs/p-InP/i-InGaAs/n-InP/InGaAs-seed NWs of different lengths and widths. Phosphorus is indicated in green, representing the InP regions, arsenic in red, and gallium in blue, with the red and blue areas collectively representing InGaAs.

During this project, the process to fabricate funnel-shaped devices was optimised through a two-step growth method. In this approach, steps 3 to 5 (Template opening, Silicon back-etch and III-Vs growth) are repeated after conformally covering the first template opening holes (light green in Fig 3-5) with SiO_2 via ALD and defining the second holes (dark green in Fig 3-5) through EBL. Those extra steps are illustrated in the SEM and EDX images from Fig 3-12.

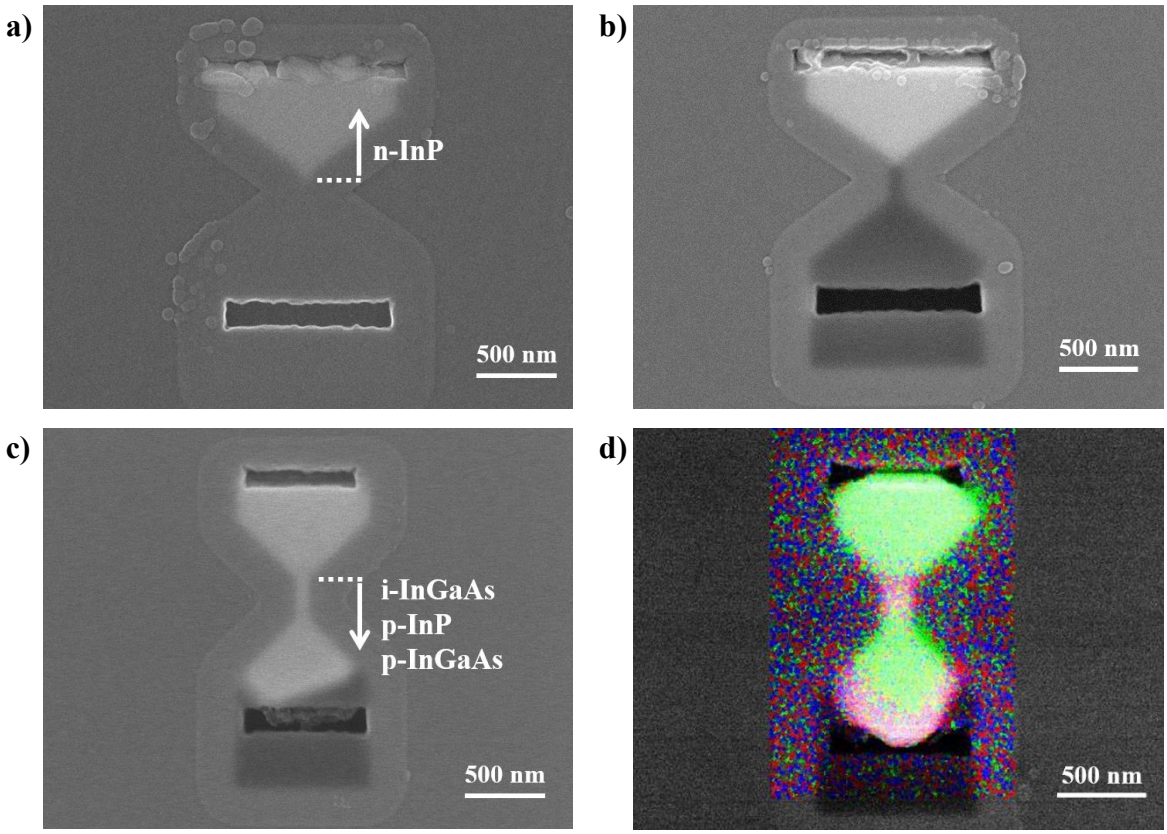


Fig 3-12. SEM (a-c) and EDX (d) images of the final steps of the two-step growth method to fabricate funnel-shaped devices, with the arrows indicating the growth directions. a) Corresponds to the covering of the first template opening hole by ALD, b) shows the second template opening and etching of the remaining Si, c) is after the second growth process, and d) shows the different materials on a fully grown device, with phosphorus indicated in green, representing the InP regions, arsenic in red, and gallium in blue, with the red and blue areas collectively representing InGaAs.

6. **Metal contacts.** The contacts' fabrication process starts by thinning down the oxide template to approximately 50 nm above the NWs to ensure the physical step created by the oxide when the contacting holes are created is not too high for metal deposition. This is performed in multiple steps of RIE, with frequent monitoring of oxide thickness using a reflectometer to ensure the devices remain protected.

Next, the contacting holes (blue squares in Fig 3-5c) are defined with EBL using a polymethyl methacrylate (PMMA) resist. RIE is then used again to remove the oxide from the holes, making sure that the III-V materials are not fully exposed, as the RIE process etches them more rapidly than SiO_2. Leaving a small amount of oxide during this step also helps shield the devices from the resist during the final EBL step.

Finally, the contact area is defined using two layers of different PMMA resists to ensure proper lift-off of the metal without damaging the contacts. The combination of two resists, each with a different development speed, induces an under-cut effect, as the bottom resist creates larger holes than the top one. This leaves an area free of metal that allows the solvent to reach the resist during the lift-off process. The sample is then submerged in BHF to remove the last nanometres of oxide on top of the devices, before adding the metals using an evaporator. A base layer of 100 nm of nickel (Ni) is deposited, followed by a top layer of 10 nm of gold (Au) to achieve ohmic contacts with the III-V materials [121, 122]. Lastly, the excess metal is carefully lifted off by submerging the sample in acetone. These last steps are illustrated in Fig 3-13.

The characterisation of the fabricated devices is performed both electrically and optically. Electrical characterisation is conducted using a probe station to obtain I-V curves and measure the dark current. Optical characterisation is carried out using an optical setup with a tunable-wavelength supercontinuum laser (640 nm – 2000 nm), which shines light through a lens or an optical fibre to obtain the photocurrent I-V curves. Although the optical setup also allows for dark current measurements (with the light off), the measurement of low current values is limited by parasitic noise in the system due to the electrical connections.

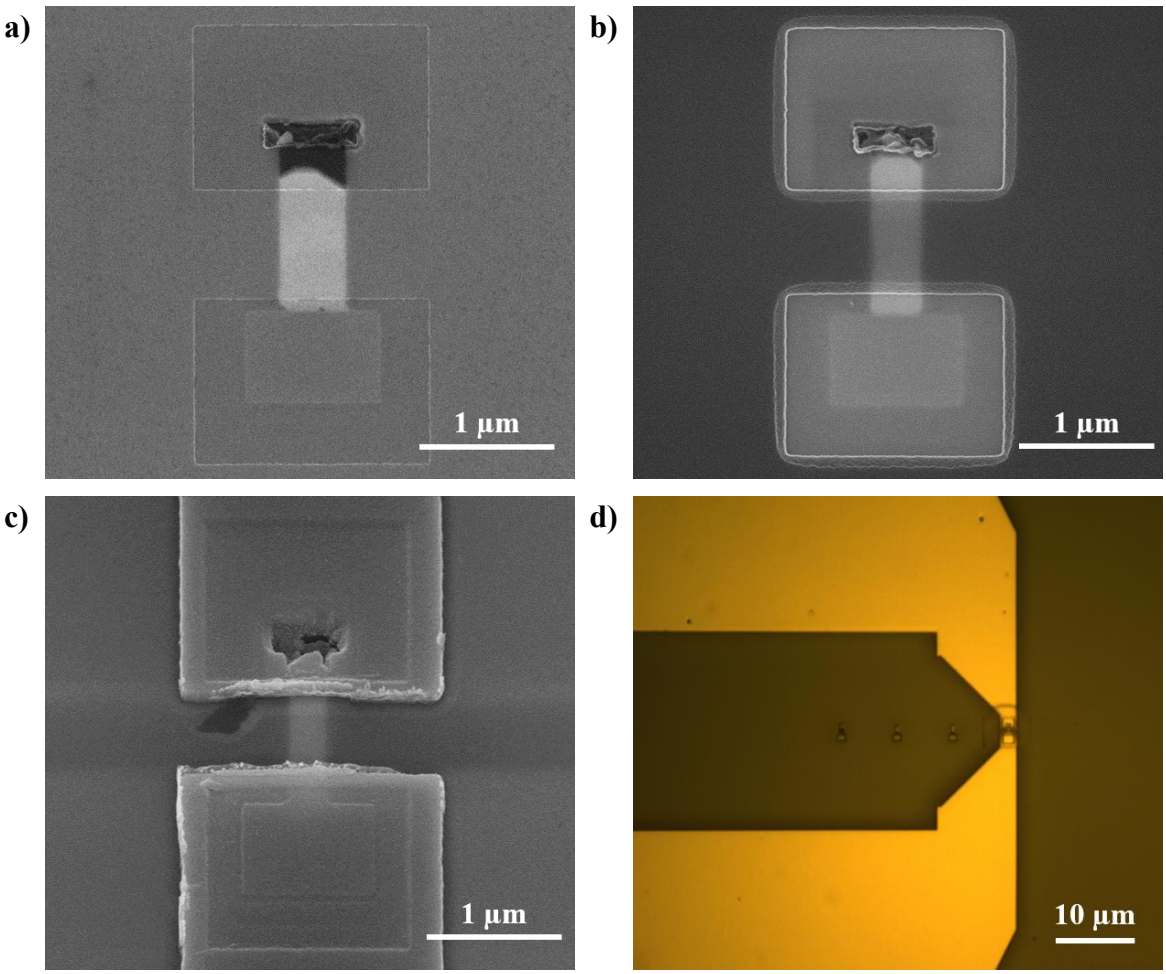


Fig 3-13. SEM (a-c) and optical microscopy (d) images of the steps to contact the fabricated devices. a) Corresponds to the EBL step to define the contacting holes after thinning the whole sample down, b) is after the RIE step to expose the III-V materials, c) and d) show an SEM and an optical microscopy image after the metal contacts have been deposited.

3.2.1. Materials growth

The first optimisation step for the fabrication of the photodetectors involved determining the growth rates of the individual materials for the final sequence. Although this sequence (n-InP (Sn doped) / i-InGaAs / p-InP (Zn doped) / p-InGaAs (Zn doped)) has previously been used for photodetectors, the earlier devices were fabricated to be 60 nm thick [48], while the 220 nm thick devices used in this project required updated growth parameters.

SEM images of four different samples are shown in Fig 3-14, where each NW contains a different III-V material. The wire from the first sample, shown in Fig 3-14a, indicates that it was back-etched too long a time, leaving a hole at the bottom of the wire due to the directed growth. The sample from Fig 3-14b contains both i-InP and i-InGaAs, deposited in two separate growth runs.

As a first test, the samples shown in Fig 3-14c and Fig 3-14d incorporated Zn precursor in doping concentration during the growth process and not by diffusion. This study revealed that the growth rate is not constant along the nanowires. Growth is faster near the template opening, as the precursors do not need to travel far into the template. For this reason, the growth rate for the materials closer to the template opening in the final devices, p-InP and p-InGaAs, required further adjustment. Additionally, the already mentioned dependence of the growth rate on the width was observed. Narrower nanowires take longer to grow due to the smaller openings, which hinder the precursors from reaching the seed. The growth rate increases logarithmically with respect to template width, as wider templates require a greater amount of precursors to achieve full growth, but also allow for a higher precursor flux to reach the growing crystal, thereby accelerating the growth process.

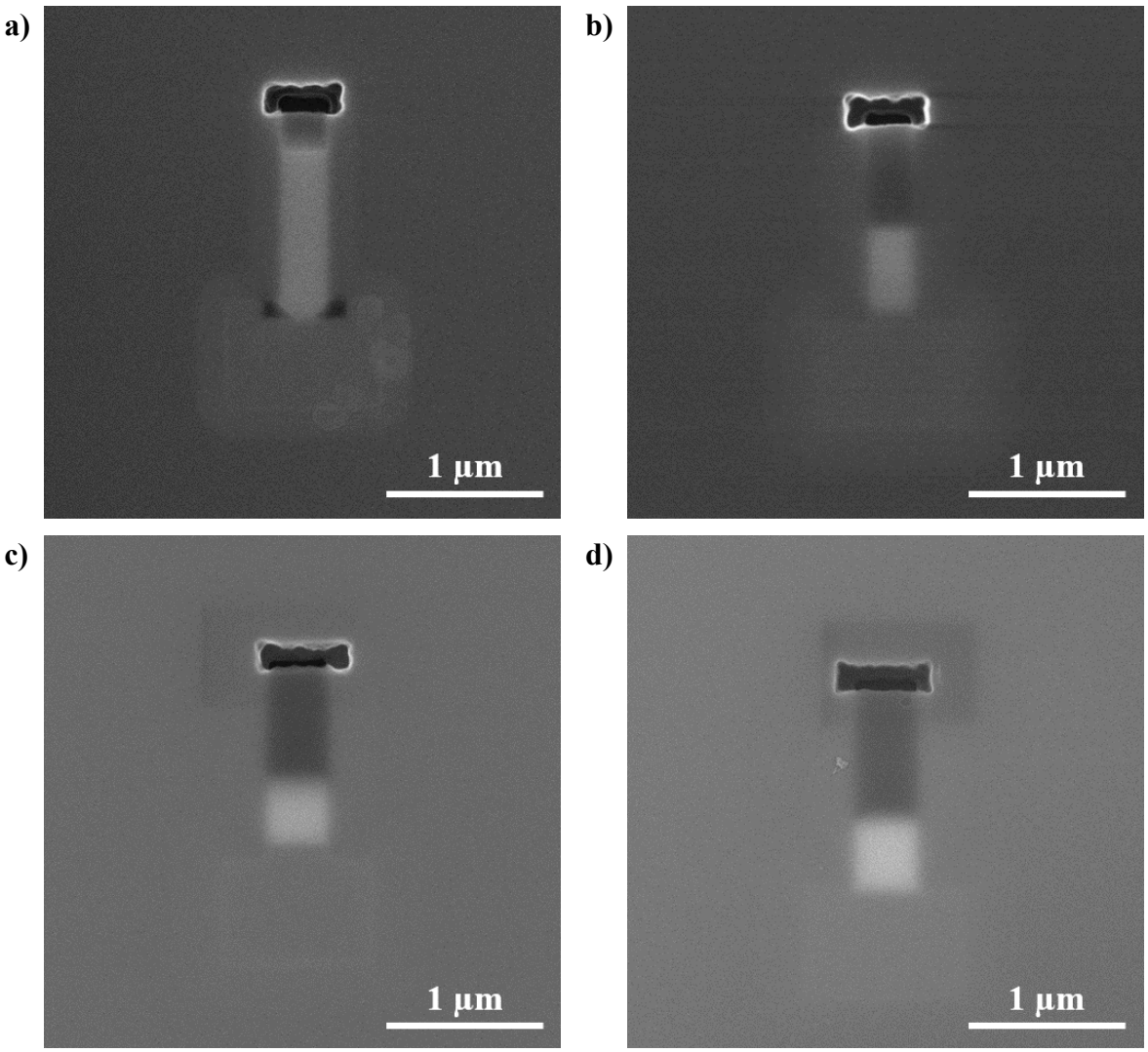


Fig 3-14. SEM images of III-V nanowires, a) with Sn doped InP, b) with i-InGaAs, c) with Zn doped InP and d) with Zn doped InGaAs.

The next step in the materials growth consisted in ensuring that the p-doped materials have enough doping levels to prevent the formation of a Schottky barrier with the metal contact. To achieve this, fully p-InGaAs grown NWs were selected and contacted. The process of NW selection involves choosing from 12 different NWs within reach of each contact, as the space occupied by the contacts is large enough to accommodate several NWs. Given that the growth process is not uniform in wafers with this crystal orientation, this allows for the selection of the best-grown wires for contacting.

The contacted wires are in the width range of 300 – 600 nm due to the difference in length with the narrower ones. The current-voltage (I-V) curves obtained through a two-point measurement from the electrical contacts of the devices can be seen in Fig 3-15.

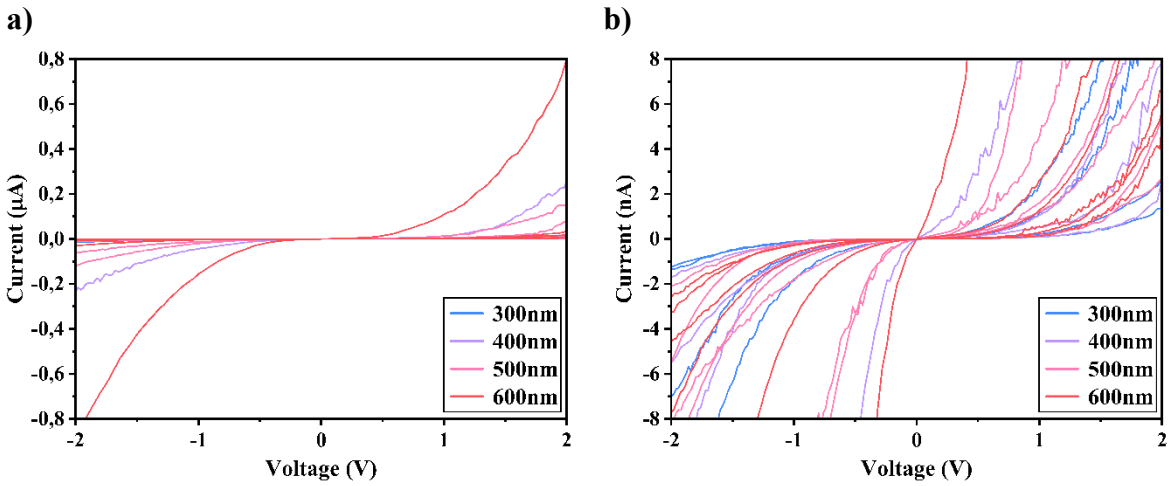


Fig 3-15. Linear scale I-V characteristics of selected p-InGaAs nanowires with different widths, b) being a zoomed in version of a).

If the Zn concentration was high enough to achieve an Ohmic contact between the p-InGaAs and the metal, the I-V curves would appear as straight lines. However, as shown in Fig 3-15, this is not the case, and the contacted NWs form a Schottky barrier. After researching the literature, it was decided to perform the Zn doping by diffusion. The temperature, Zn flow rate and time of diffusion are crucial parameters for achieving ohmic contacts [120]. Therefore, the next step was to optimise the p-doping of InGaAs on InP.

3.2.2. Zinc diffusion optimisation

To perform the Zn diffusion optimisation, a different type of sample was fabricated. These consisted of a diced InP wafer on top of which 100 nm of InGaAs and 50 nm of SiO_2 were deposited. The oxide layer acts as a mask and was patterned by laser writing and etched by RIE and BHF to obtain holes of different sizes separated by different distances to enable the determination of the Zn diffusion depth. A schematic of the sample is shown in Fig 3-16.

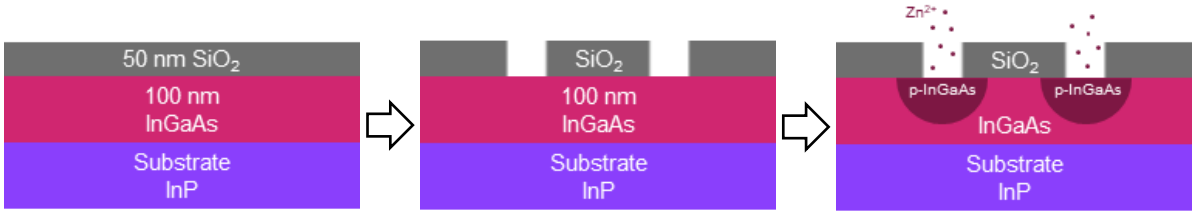


Fig 3-16. Schematic of the fabrication process for the Zn-diffusion sample.

Another pattern transferred onto the oxide was different size bars to perform Transfer Length Method (TLM) measurements. This method allows the resistance of the p-doped InGaAs to be calculated. The bars measure from 20 to 80 µm in length with widths ranging from 2 to 8 µm proportionally. Images of all the designs as they appear in the L-Edit software can be seen in Fig 3-17, where the pink areas correspond to the patterning areas on the SiO_2 mask, which end up with the InGaAs layer exposed, and the golden rectangles to the metal contacts' layer.

The hole sizes obtained with this design range from 600 to 1600 nm and their separation distances range between 300 to 2100 nm. Some SEM images of the obtained holes and a TLM bar after patterning the oxide can be seen in Fig 3-18. Due to the resolution of the available resists in combination with the laser writer used to expose the samples, the final shape of the holes becomes increasingly rounded as their size decreases.

As illustrated in the schematic from Fig 3-16, when the Zn diffusion is performed, an area of InGaAs (and InP if the doping length is large enough) gets doped. As already mentioned, some of the factors that affect the doping profile are the diffusion time, the temperature, and the precursor's flow rate [120]. The electrical response obtained from contacting the holes will depend on the doping level achieved during diffusion and on the diffusion length.

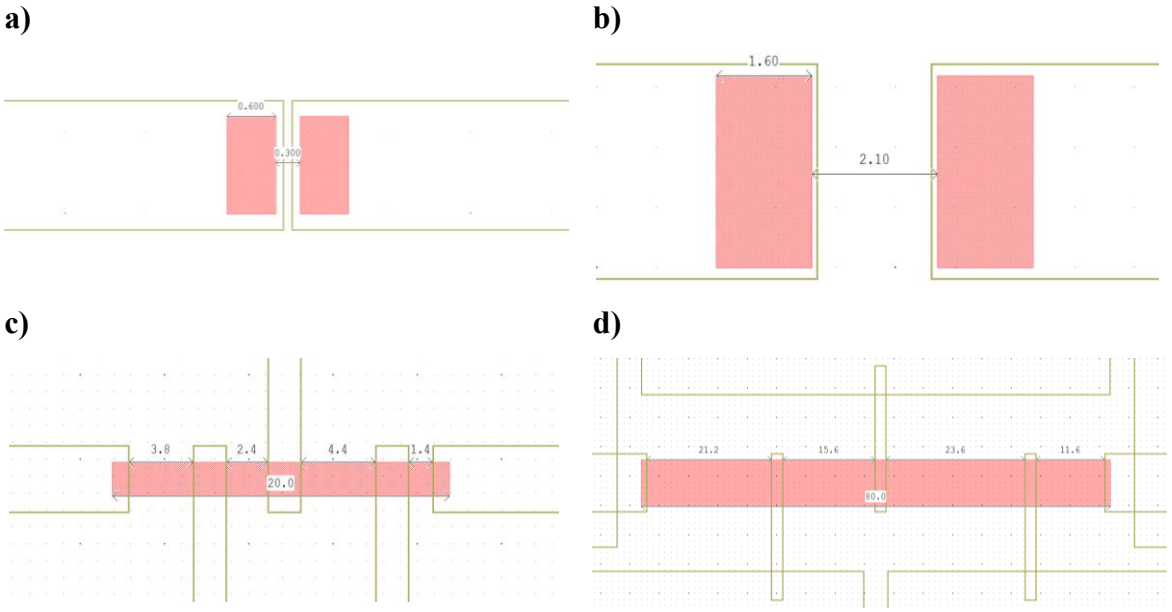


Fig 3-17. Images from L-edit software; a) and b) from the holes and c) and d) from the TLM bars. The pink areas correspond to the patterning of the SiO_2 (i.e. the areas with exposed InGaAs). The golden rectangles correspond to the metal contacts' layer.

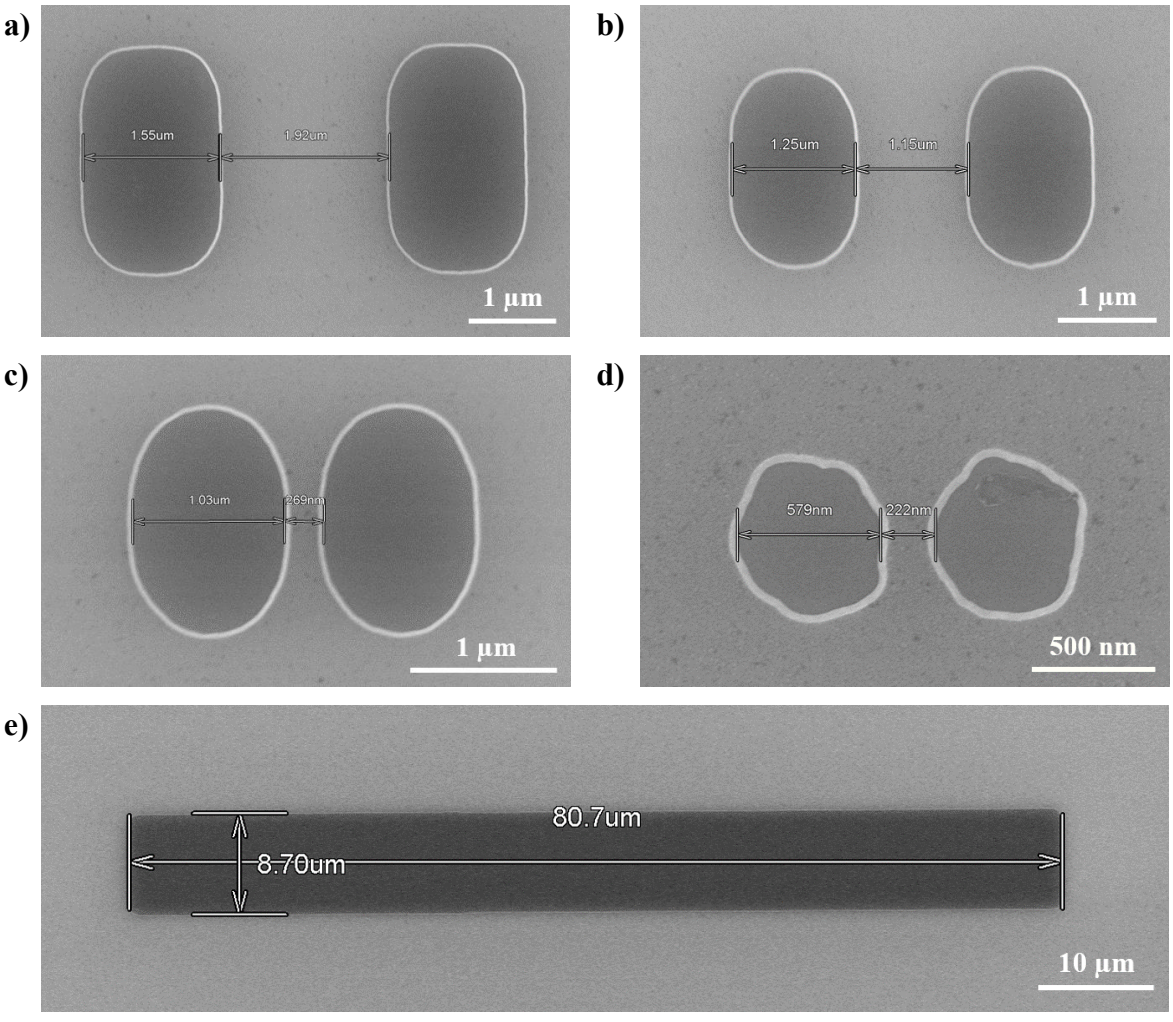


Fig 3-18. SEM images of a) - d) the patterned holes with different sizes and separations and e) a TLM bar.

The first diffusion conditions were chosen following the results in [120], where the sample was first annealed to 650 °C and then the Zn diffusion was performed at 510 °C for five minutes. The Zn flow rate employed by the authors was higher than the one allowed by the setup used in this work, so it was set to the maximum available instead. To avoid arsenic (As) desorption, the doping process was performed in an As atmosphere. Some SEM images of the first sample after the diffusion process are shown in Fig 3-19.

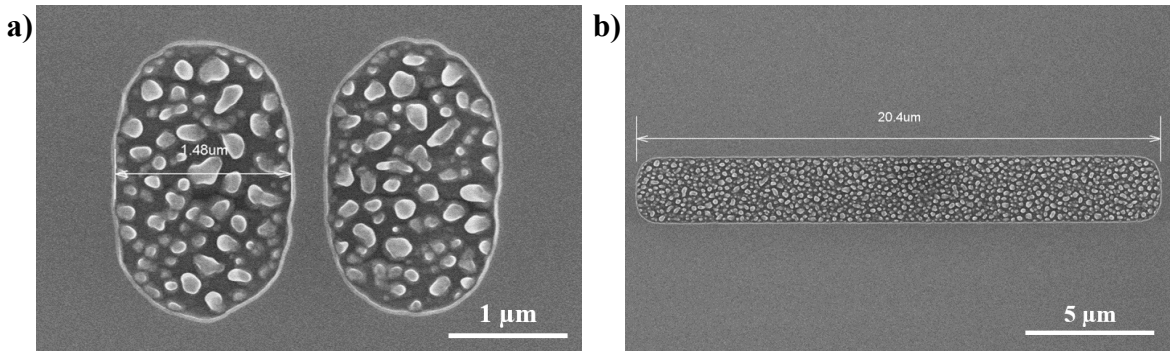


Fig 3-19. SEM images of a) a pair of holes and b) a TLM bar, after Zn diffusion in As atmosphere at 510 ºC after annealing at 650 ºC.

As seen in Fig 3-19, the InGaAs surface after diffusion became rough, exhibiting droplet-like features. Several hypotheses were considered at this point. Initially, it was thought that the ratio between As and Zn during the diffusion was wrong, potentially enabling the nucleation of Zn nanoparticles. To investigate this hypothesis, an EDX analysis was performed on the sample, as shown in Fig 3-20.

The EDX analysis revealed that the droplets on the sample were not Zn but As. From these results, two further hypotheses emerged: the Zn could be displacing the As, causing it to nucleate on the surface and form As droplets [123], or the annealing at 650 °C might be melting the InGaAs, resulting in a rough surface. To test the first hypothesis, a second sample was annealed at 650 °C and then brought down to 510 °C (the diffusion temperature) without introducing any Zn into the chamber. SEM images of the results from this anneal test are shown in Fig 3-21a and Fig 3-21b. To test the second hypothesis, additional samples were annealed at several lower temperatures before being brought to the diffusion temperature, also without adding Zn precursors. SEM images of a sample annealed at 600 °C is presented in Fig 3-21c and Fig 3-21d.

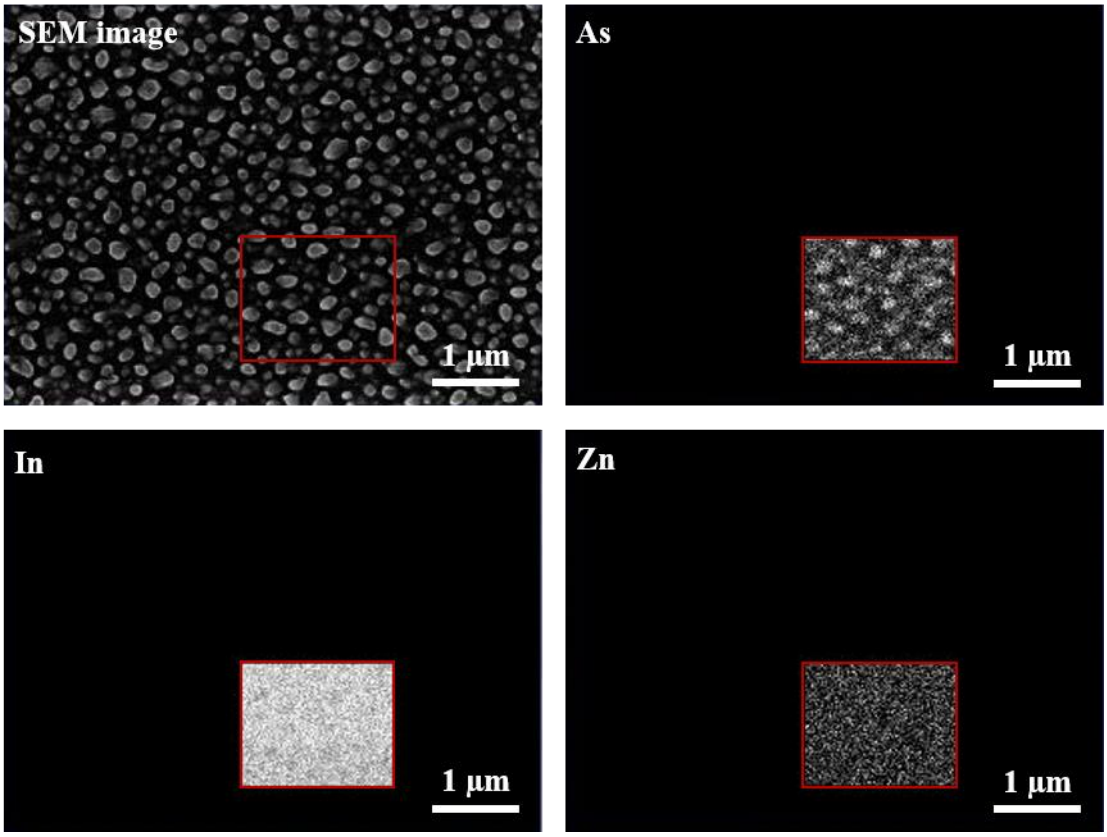


Fig 3-20. SEM image and EDX analysis for As, In and Zn for the first Zn diffused sample.

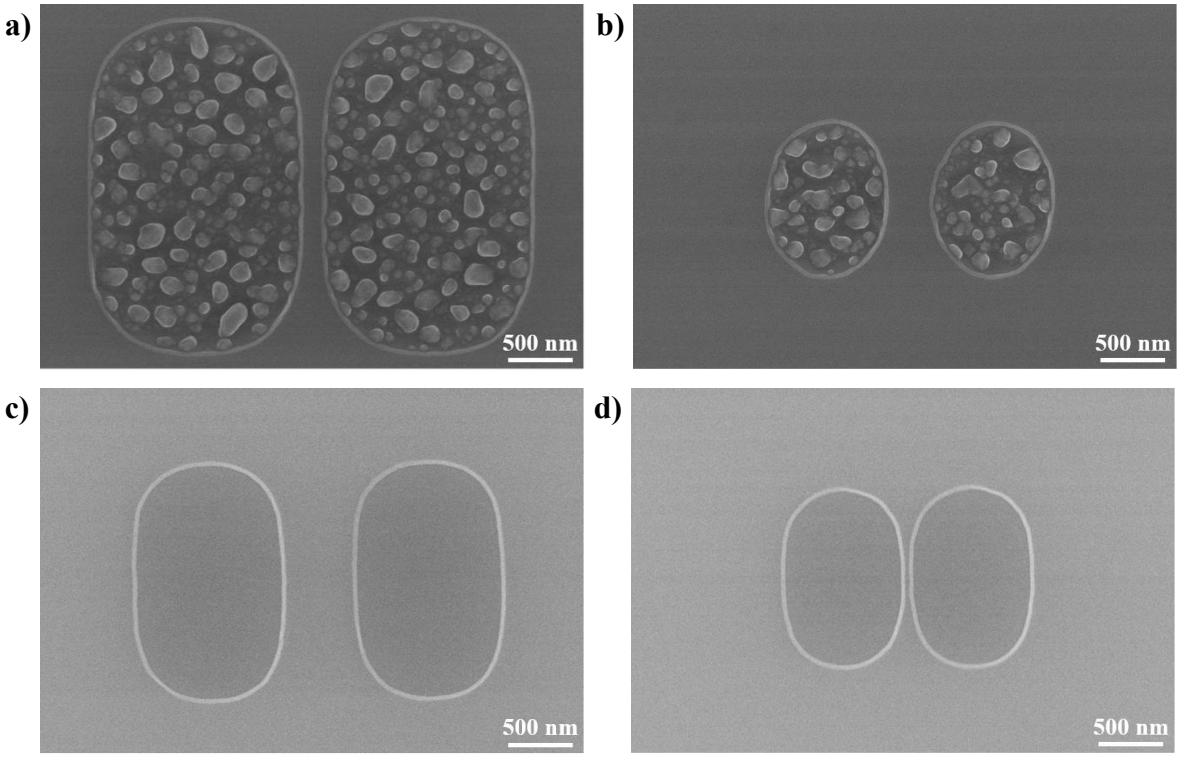


Fig 3-21. SEM images of the holes on the sample annealed at a) - b) 650 °C, and c) - d) 600 °C under an As atmosphere and no Zn diffusion.

In Fig 3-21, the roughness of the sample can be seen to remain high when it is annealed at 650 °C, even without any Zn added into the chamber. However, surface roughness is absent when annealing at 600 °C (or lower). This confirmed the hypothesis of the high temperature being the responsible of the rough surface and not the Zn incorporation. Therefore, a third sample was annealed at 600 °C and Zn was diffused at 510 °C for five minutes. SEM images of the resulting holes' surfaces are shown in Fig 3-22a and Fig 3-22b, presenting smooth InGaAs surfaces.

The doping length was determined from I-V curves once the holes were contacted. A lithography step using a laser writer was performed to define the positions of the contacts. Alignment with a laser writer is not as precise as with the e-beam, but it avoids the additional steps required to create e-beam markers. Slight misalignment is acceptable in this case, as the metal only needs to make contact with the surface of the holes, without needing to completely cover them. The resulting I-V curves for two pairs of contacted holes, along with their respective SEM images, are shown in Fig 3-22c and Fig 3-22d.

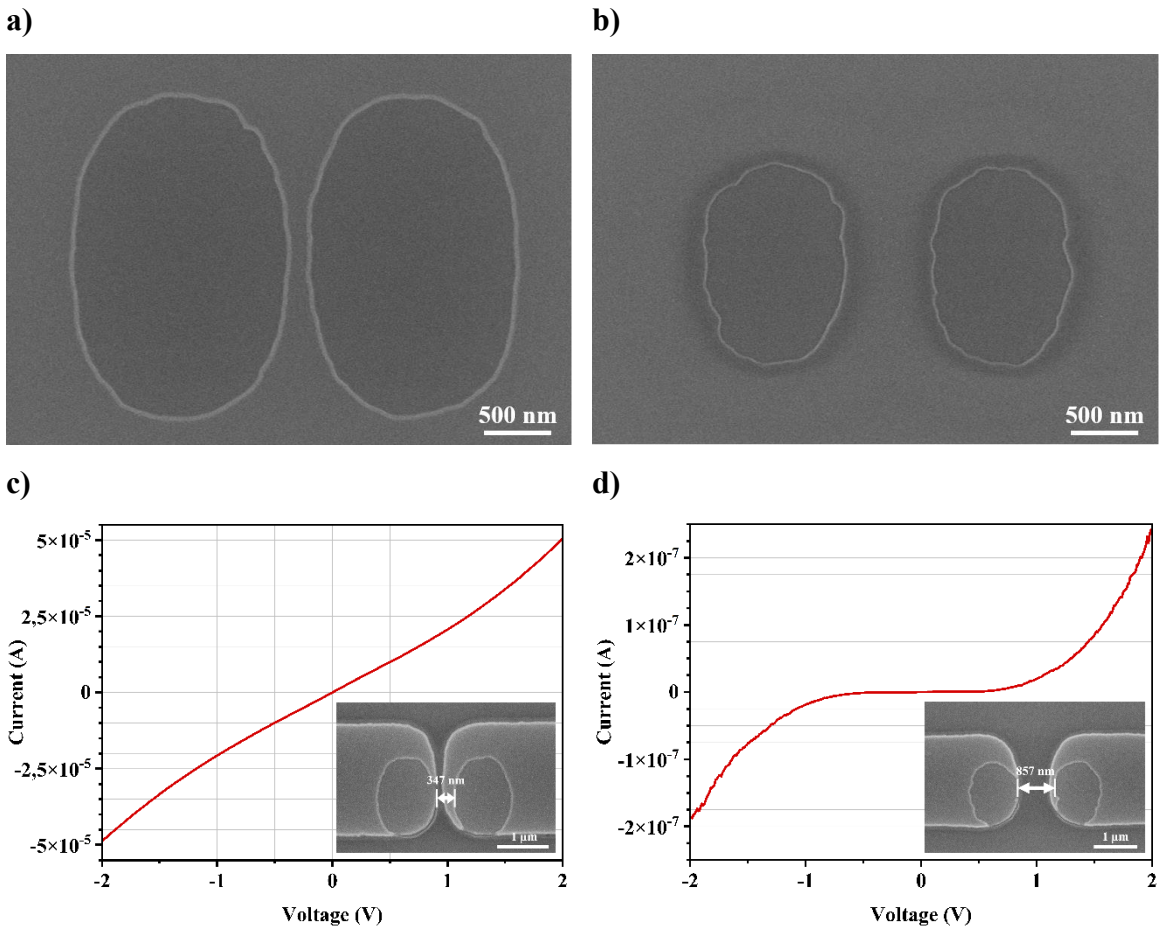
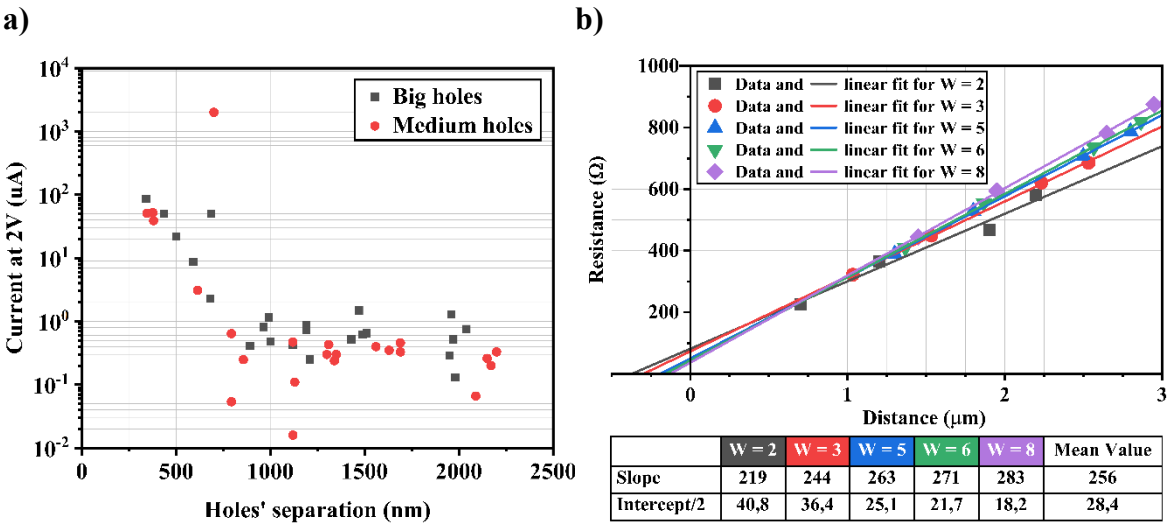


Fig 3-22. a) and b) SEM images of the holes' surfaces after the Zn diffusion at 510 ºC with an optimised annealing temperature of 600 ºC. c) and d) I-V curves of two pairs of contacted holes with their respective SEM images.

The diffusion length can be extracted from the correlation between the holes' separation and their I-V curves. As seen in Fig 3-22c, when the holes are closer, the resulting I-V curve is almost a straight line, indicating a fully diffused channel between the holes. As the distance increases, shown in Fig 3-22d, the curve becomes more diode-like, implying that the InGaAs is not fully p-type between the holes. The current at 2 V also decreases for the diode-like curves and can be plotted against the hole separation to better visualise this trend, as shown in Fig 3-23a.

Another important parameter is the contact resistance, which can be extracted from the TLM measurements. The total measured resistance is the sum of the resistance from both metal contacts ($2R_C$) and the resistance of the semiconductor, which can be expressed as the sheet resistance multiplied by the ratio of the length to the width ($R_{sheet} \cdot \frac{L}{W}$). This implies that the total resistance is linearly dependent on the contact separation length.

The configuration of the contacts on the bars, shown in Fig 3-17c and Fig 3-17d, allows for measurements along various distances. The resistance values versus the distance between the contacts are then plotted, as shown in Fig 3-23b, showing a clear linear dependence. By extrapolating the graph to L=0, i.e. where the lines intersect the Y-axis, the residual resistance is obtained, which corresponds to twice the contact resistance [124]. Since different sizes of bars were fabricated on the sample, they have been plotted separately depending on their width (W).



	W = 2	W = 3	W = 5	W = 6	W = 8	Mean Value
Slope	219	244	263	271	283	256
Intercept/2	40,8	36,4	25,1	21,7	18,2	28,4

Fig 3-23. a) Current at 2 V versus the holes' separation, and b) the results of the TLM measurements on the bars with different widths (W) to obtain the contact resistance of the doped InGaAs.

By harnessing the results of this study on Zn diffusion and the previous growth rate study presented in section 3.2.1, the p-i-n devices were able to be fully fabricated. The diffusion parameters used for p-doping achieved sufficient doping levels to ensure good contact resistance between the p-InGaAs layer and the Ni/Au contacts. While additional optimisation to assess the InP p-doping levels was possible, the decision was made to proceed with full device fabrication due to time constraints. The first sequence growth for these final devices after the optimisation of all the growth steps (length of the segments and Zn diffusion) was performed, obtaining the NWs shown in the EDX images in Fig 3-24. As previously mentioned, in these images, phosphorus is indicated in green, representing the InP regions, arsenic in red, and gallium in blue, with the red and blue areas collectively representing InGaAs.

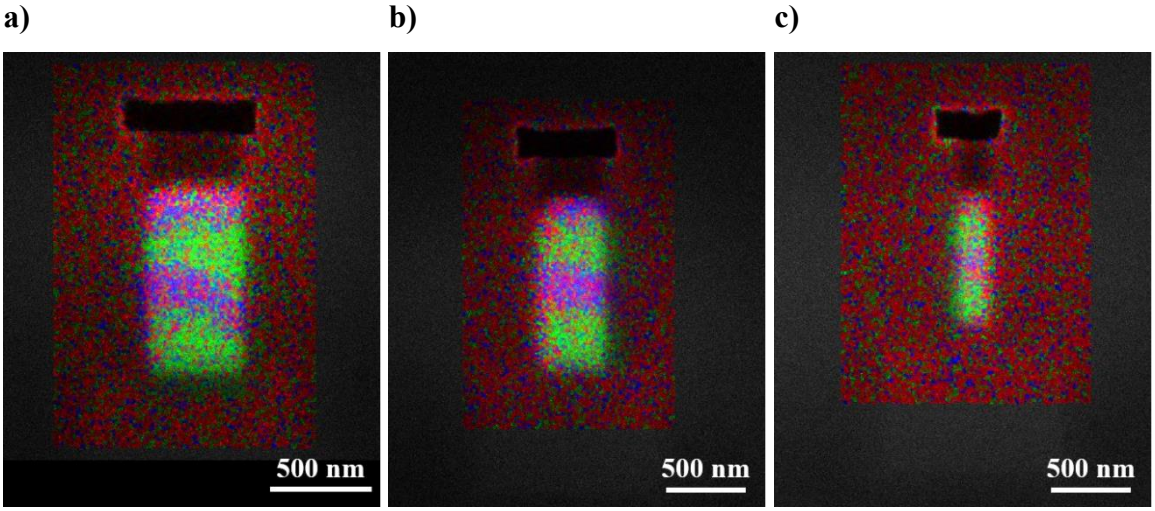


Fig 3-24. EDX of the sequence growth for three nanowires with three different widths: a) 500 nm, b) 400 nm, and c) 200 nm. Phosphorus is indicated in green, representing the InP regions, arsenic in red, and gallium in blue, with the red and blue areas collectively representing InGaAs.

This chapter presented a detailed, step-by-step explanation on how to achieve fully functional III-V photodetectors using TASE. While TASE had previously been used to fabricate both 60 nm and 220 nm thick photodetectors, the latter showed a significant lack of reproducibility across devices. This inconsistency prompted the work presented in this thesis, which aims to provide statistical data from a large number of fabricated devices in order to better understand the various factors influencing their electrical and optical performance.

The fabrication process presented focused on refining material growth and doping techniques, with particular attention to Zn diffusion for the p-doping of the photodetectors. Additionally, the fabrication of the first funnel-shaped devices was optimised by introducing a two-step growth process. This marks the first demonstration of a double-growth technique in TASE structures, with the aim of enhancing device performance.

4. Photodetectors' characterisation

This chapter presents the electrical and optical characterisation of the TASE-fabricated photodetector devices. As previously mentioned, the 60 nm thick InGaAs p-i-n photodetectors from earlier work [48] demonstrated low-capacitance and high-speed performance but were unsuitable for waveguide light coupling. The more recent 220 nm thick waveguide coupled heterostructure devices [60] were characterised thermally and optically, focusing on different light coupling schemes from the waveguide to the device.

This chapter provides the first comprehensive analysis of the electrical characterisation of in-plane 220 nm thick heterostructure photodetectors, addressing the reproducibility challenges that previously made device comparisons difficult. The statistical data obtained from the large number of fabricated devices, combined with TCAD simulations, aim to explain the variability observed across devices.

Optical characterisation of the fabricated devices was also performed, although meaningful comparisons between devices were limited by the significant variability in their electrical characteristics. Individual devices were measured at low temperatures to explore their behaviour and potential applications in quantum technologies.

4.1. Electrical measurements

To evaluate the process variability of the TASE method, statistical data from various photodetectors was compiled. Electrical measurements were carried out on the first fabricated sample's devices, and a selection of I-V curves from the straight NWs is shown in Fig 4-1. The current density is plotted instead of the current to account for the different conducting areas of the devices. The curves are colour-coded based on their respective device width, with corresponding SEM images of some contacted devices.

Ideally, one would expect the current density plot to be the same for all devices. However, as seen in Fig 4-1, there is no clear correlation between the current density value and the width of the devices. In earlier work on the much more scaled devices with a height of only 60 nm [48], dark currents densities were found to be increased for the smallest geometries, attributed to the influence of surface states. In the present study with much larger devices, such correlation is not observed.

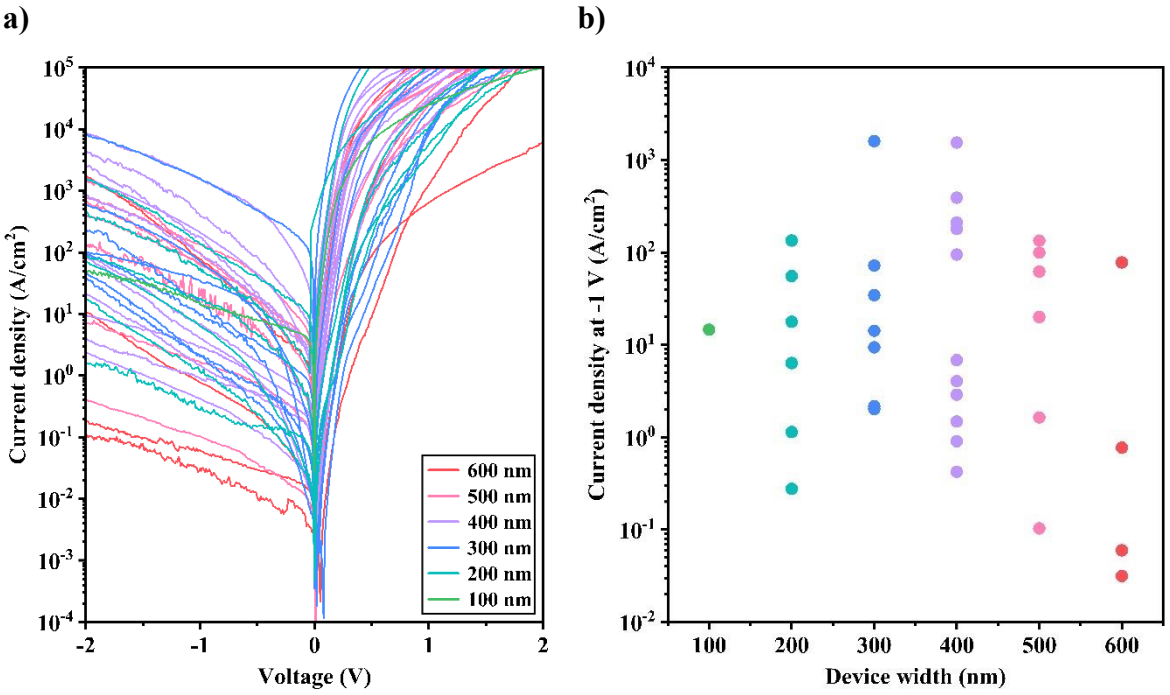


Fig 4-1. a) Experimental I-V curves from the measured NW devices in dark current [125] reproduced with permission © 2024 IEEE. A cut-off in current density is set to 105 A/cm² during measurement to avoid damaging the small devices. b) Current density values extracted from (a) at a voltage value of -1 V, plotted against the device width for better visualisation.

In Fig 4-1a, a selection of the most diode-like I-V curves has been plotted, illustrating the significant variability between devices without any evident trend related to width. This can be more easily observed in Fig 4-1b, where the current density value at -1 V of applied voltage has been plotted with device length. This selection represents 35% of the total contacted devices. There are two primary reasons for this percentage not being higher. Firstly, during the process of making the openings for the contacts, the sample was over-etched, leading to deep trenches around some NWs, which prevented the metal from having a conductive path to the devices.

Secondly, the SOI wafer used for building these devices presented challenges. Generally, III-V growth is most favourable along a <111> direction or a <011> direction, usually resulting in single {111} facet growth fronts. However, on a conventional (001) SOI substrate, several of these planes are exposed. Adding to the complexity, in order to start with a smooth Si surface for nucleation, the silicon back etch is performed using the highly anisotropic etchant TMAH to start out on a Si{111} facet, which is tilted relative to the wafer surface. This leads to non-uniform growth along the NWs, with growth fronts that are not orthogonal to the wafer surface but tilted.

The growth fronts shown in Fig 4-2a result from the competition between the <111> and <110> directions [126]. While using a (110) SOI substrate could theoretically solve this issue, such substrates are not commercially available in photonic grade, i.e. with sufficient thickness for optical waveguiding [127, 102]. Furthermore, seed nucleation can occur in different locations on the crystallographic surface, potentially leading a single nanowire to develop two crystals with different growth fronts due to competing growth fronts. A combination of stochastic processes, crystallographic plane orientation, and seed nucleation location results in the high variety of growth profiles observed in the fabricated nanowires.

The coloured SEM images in Fig 4-2b illustrate the top view of various fabricated devices, where the different materials can be seen. They highlight the diversity in facets and the length difference between widths, where can be seen that as the devices get thinner, they also get shorter. That illustrates again the dependence of the growth rate on the width that was mentioned in section 3.2.1.

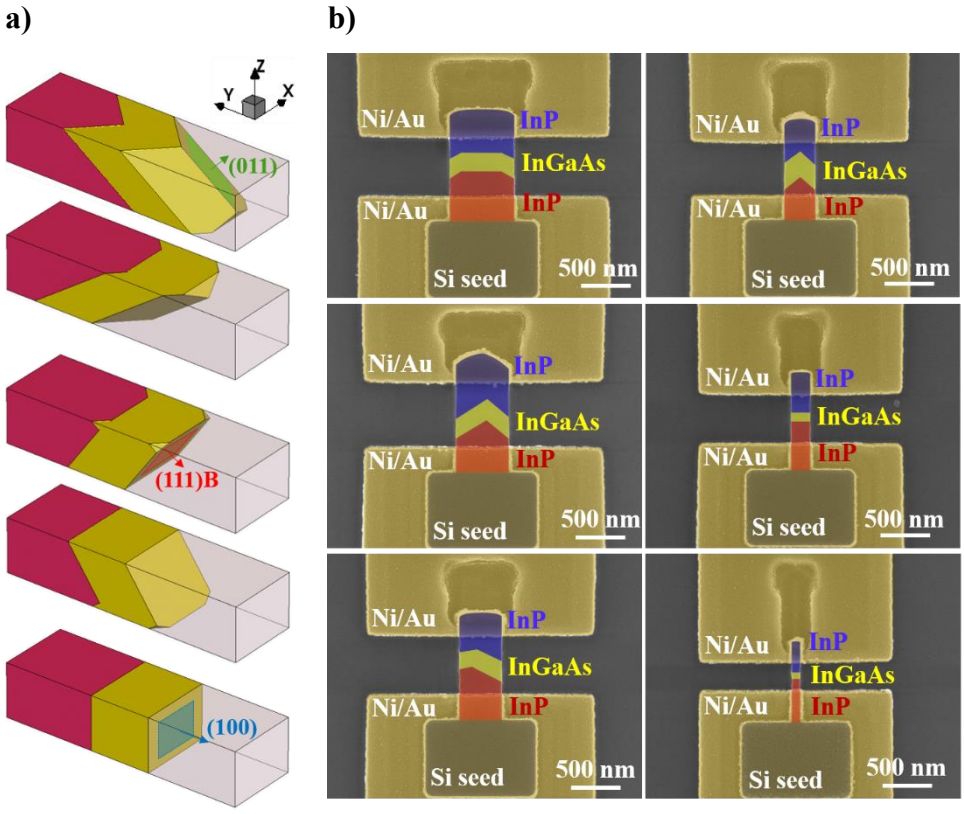


Fig 4-2. a) Expected growth fronts of III-V materials on a (001) SOI wafer [125] reproduced with permission © 2024 IEEE. b) Coloured top-view SEM images of fabricated devices with different widths (100 to 600 nm) with the metal contacts (Ni/Au) incorporated.

For all these reasons, the i-InGaAs region may sometimes end up contacted, resulting in an I-V curve that appears resistive (symmetrical). This variation in growth profile can be responsible for the significant variability in I-V curves, which is discussed in the following section.

4.1.1. Matching simulations

By using TCAD simulations and considering the different growth fronts that the III-Vs can produce when grown on a (001) SOI wafer, this section provides insights into the performance and explains the variability of the device characteristics among the fabricated photodetectors shown in Fig 4-1. These results have been published in IEEE Transactions on Electron Devices (TED) journal [125].

The initial hypothesis for the observed variability was that it was due to the influence of the differently tilted facets, as these could deform the electric field and impact the response of the current along the devices. The following I-V curves in Fig 4-3a were obtained after simulating the facets shown in Fig 4-2a. The current density values at -2 V of applied voltage are shown in Fig 4-2b, with the different facets shown again as a legend.

In these simulations, the devices were modelled as ideal photodiodes, without including the effects of traps, and with the contacts assumed to be Ohmic, i.e. with no contact resistance or parasitic capacitance. This approach isolates the effect of the facets themselves, allowing for a clearer analysis of how the facet orientation alone influences the electrical behaviour of the devices.

The I-V curves presented in Fig 4-3a exhibit a spread of an order of magnitude, primarily due to the varying widths simulated. The plot in Fig 4-3b represents the current density values at -2 V of applied voltage, plotted for the different widths and growth facets. This plot shows that devices exposing complementary facets (represented by different shades of green and different shades of red) have consistent current density values across all device widths. Additionally, although the difference in current density for the various facets is not substantial, it increases with the width of the devices.

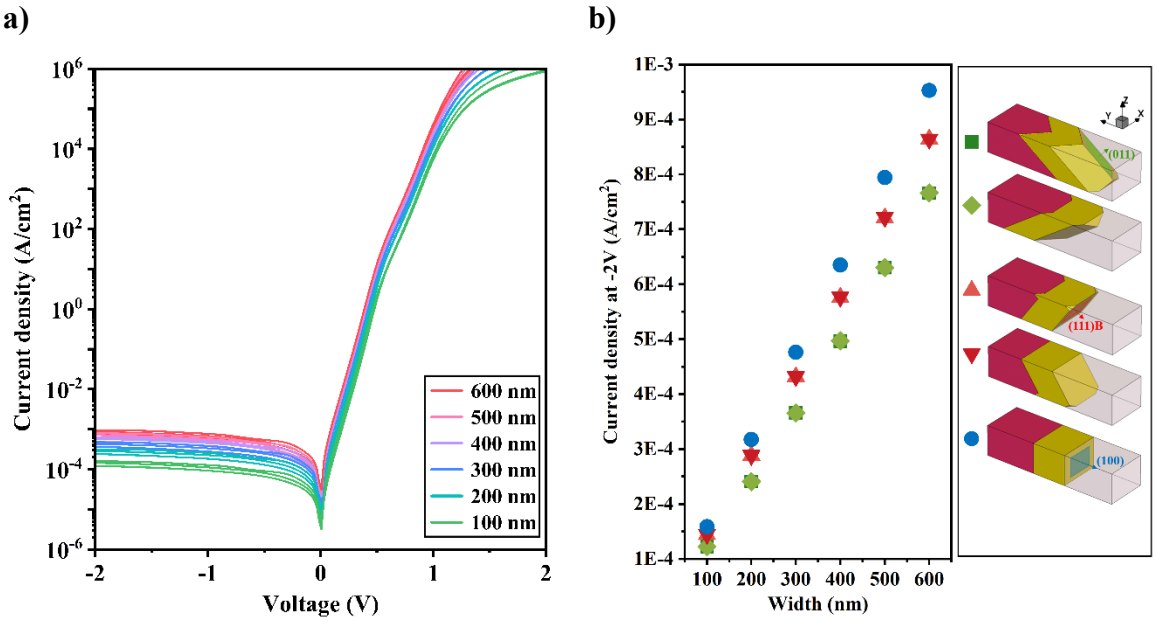


Fig 4-3. a) Simulated I-V curves for devices with different widths (100 to 600 nm) and different growth facets. b) Current density values of the devices for the expected growth fronts, shown in its legend, extracted from (a) at a voltage value of -2 V, with respect to the width for better visualisation, [125] reproduced with permission © 2024 IEEE.

Due to the limited variability in these simulated I-V curves, an alternative approach was considered. As observed in the SEM images in Fig 4-2b, the difference in growth front within the devices leads to non-uniform growth speeds and situates the InGaAs region differently in relation to the contacts. As previously mentioned, this can result in the InGaAs being contacted, either by the p-contact, the n-contact, or both.

Furthermore, as presented in section 3.2.2, the p-doping is introduced into the devices by diffusion after the growth, which could cause the InGaAs region to be p-doped if it is too close to the growth opening. This could result in a gradient of p-type dopants and possible variations in the location of the p-i junction.

Given that the geometry of the facets had only a minor impact on device characteristics (Fig 4-3), the simulations were simplified by using a straight junction geometry, i.e. a growth front in the <100> direction, while the InGaAs region is shifted from the p-contact to the n-contact.

The issue of doping being introduced into the InGaAs region was addressed by incorporating a slight doping gradient, with p-doping penetrating slightly into the InGaAs region. While this adjustment does not fully capture the behaviour of the majority of the devices, the focus of these simulations is primarily on the positioning of materials rather than the precise doping profile.

The I-V curves resulting from these simulations are shown in Fig 4-4, with an inset for comparison to the experimental I-V curves shown in Fig 4-1. The simulated curves are colour-coded as indicated in the 3D plots adjacent to the main plot. Here, the position of the contacts is fixed, and only the location of the InGaAs with respect to the contacts is gradually varied, emulating the position variation resulting from different growth rates. The InGaAs region is shifted from under the cathode (red curves) to under the anode (purple curves).

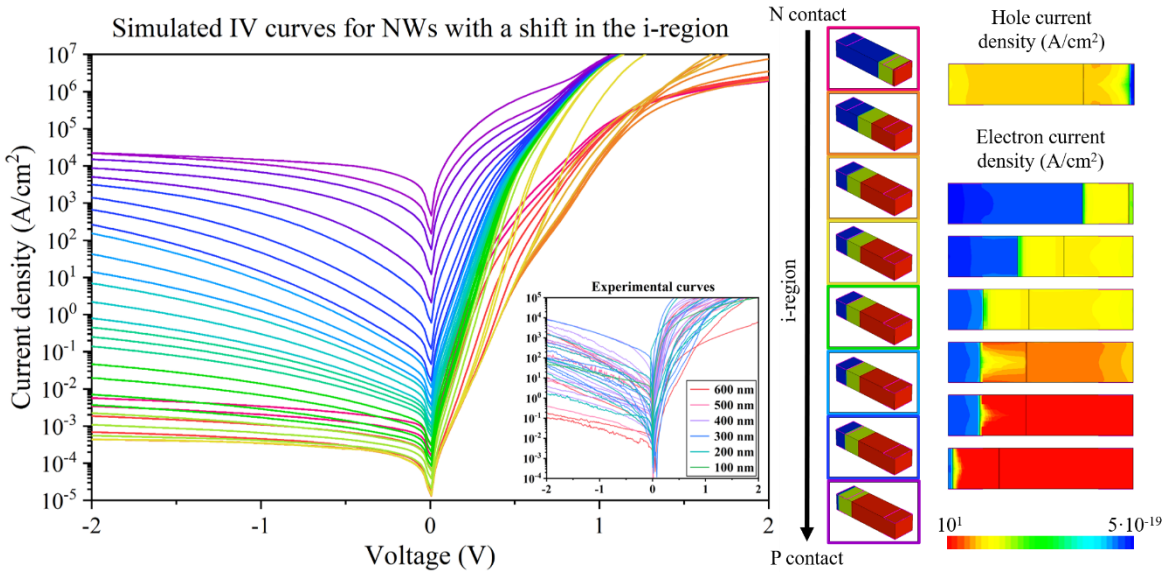


Fig 4-4. Simulated I-V curves for devices with the InGaAs shifted from the n-contact to the p-contact, as illustrated on the 3D plots next to the main graph. An inset of the experimental curves is provided for comparison. Colour 2D plots (right) show the hole current density at -2 V when the InGaAs is on the n-side, and the electron current density at -2 V across the entire range of InGaAs positioning [125] reproduced with permission © 2024 IEEE.

In the simulated curves in Fig 4-4, it can be observed that the change in the ON-current (positive values of applied voltage) occurs when the InGaAs material is contacted by the p-contact (yellow curves). The jump in the OFF-current (negative values of applied voltage) from 10^{-3} A/cm^2 to 10^{3} A/cm^2 occurs slightly later in the InGaAs region shifting (green-blue curves). As mentioned earlier, a gradient of p-doping is added into the InGaAs region to emulate the fabrication process, and this change in dark current occurs as the p-contact reaches the i-doping in the InGaAs region of the NW.

Since the InGaAs from the i-region is slightly n-doped (10^{16} cm^{-3}), the more significant change occurs when this gets closer to the p-side. Contacting the InGaAs material by the n-contact (cathode) only causes an OFF-current jump of one order of magnitude (red curves), contrasting with the seven orders of magnitude jump when contacted by the p-contact (anode). For this reason, during the simulation, smaller steps in InGaAs region shifting were modelled as this one approaches the p-contact, to achieve a uniform range of curves in the current density. This is illustrated in the 3D plots acting as a legend on the side of the I-V curves.

After examining the simulated curves, as shown in Fig 4-4, it becomes clear that the large impact on the dark current due to a shift in the heterojunction position is of a similar range in terms of current density as that observed in the experimental curves in Fig 4-1. Hence, the shift in the heterojunction position might partly explain the large variability in I-V characteristics.

On the right side in Fig 4-4, the coloured plots of the electron and hole current densities at -2 V are shown. The slight increase in (dark) current density when the InGaAs is under the n-contact (red curves) can be attributed to the elevated hole current density. The evolution of the electron current density explains the increase in total current density as the InGaAs region approaches the p-side. The electron current density remains constant until the InGaAs reaches the anode, at which point it increases rapidly, causing a significant increase in the total dark current density.

To further corroborate the simulation results, the InGaAs region of different NWs with the same width but different lengths were investigated. In Fig 4-5, the coloured top-view SEM images of a selection of three nanowires are shown with their corresponding experimental I-V curves highlighted on the graph on the right.

As can be observed, the first device (1), which has the highest dark OFF-current density, has the InGaAs region contacted by both the n- and p- contacts. The second device (2), although having the same length as the previous one, remains uncontacted due to a different growth front in the InGaAs, resulting in a lower dark OFF-current density value. The third NW (3) has the InGaAs region furthest from the contacts, implying the lowest dark OFF-current density of the three. These results align with the simulations presented in Fig 4-4 and highlight the importance of a controlled growth front when fabricating the devices [125].

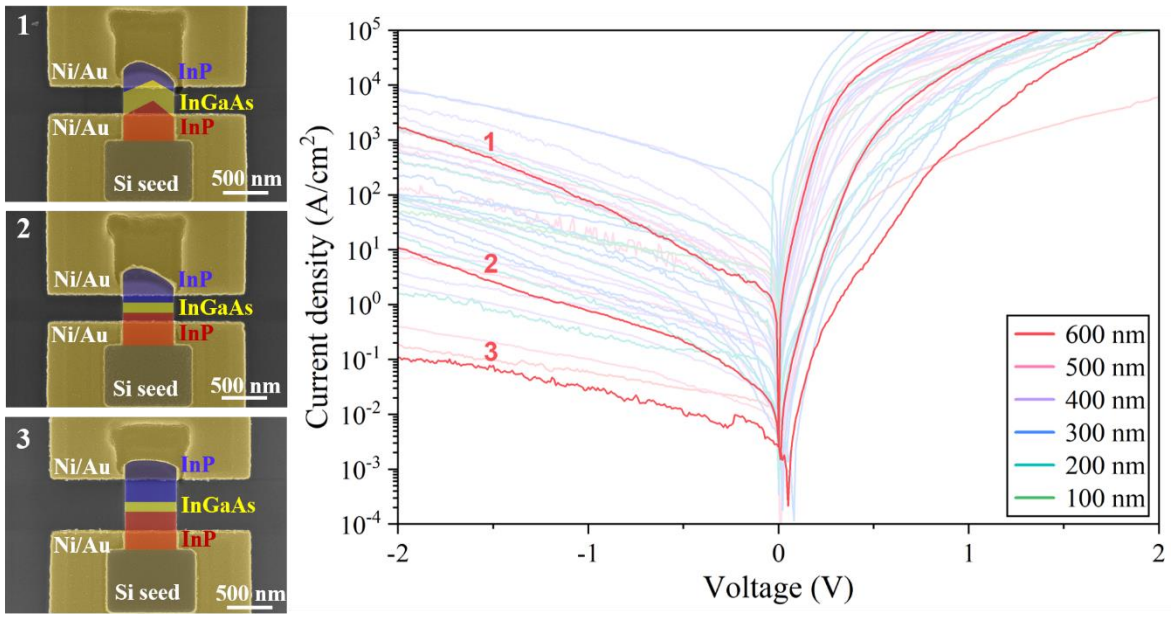


Fig 4-5. On the left are the coloured top-view SEM images. The colours indicate the position of the junction at the top of the device, which may be tilted towards the substrate and thus not be visible in a top-view EDX. On the right are the highlighted respective I-V curves of the devices shown in the SEM images on the left [125] reproduced with permission © 2024 IEEE.

The three devices presented in Fig 4-5 highlight the limitations of the simulations regarding the impact of Zn diffusion on the devices. In the first device, where the InGaAs region is positioned very close to the growth opening, Zn diffusion would likely result in significant p-doping of the InGaAs region. In contrast, the third device, with a longer p-InP region, might experience incomplete p-doping in the p-InP region. These variations are not accounted for in the simulations, as they focus on the position of the materials without fully considering the impact of doping profiles with regard to how Zn diffusion affects each individual device differently.

The experimental data presented in Fig 4-1 showed no clear trend in current density relative to device width. Moreover, Fig 4-5 demonstrates that the dark OFF-current density of a device is significantly influenced by its length. Therefore, to identify a trend, the experimental data was re-coloured based on the length of the NWs, measured from the bottom of the n-region (in red in the SEM images from Fig 4-5) to the top of the p-region (in blue in the SEM images from Fig 4-5). This re-coloured data is displayed in Fig 4-6.

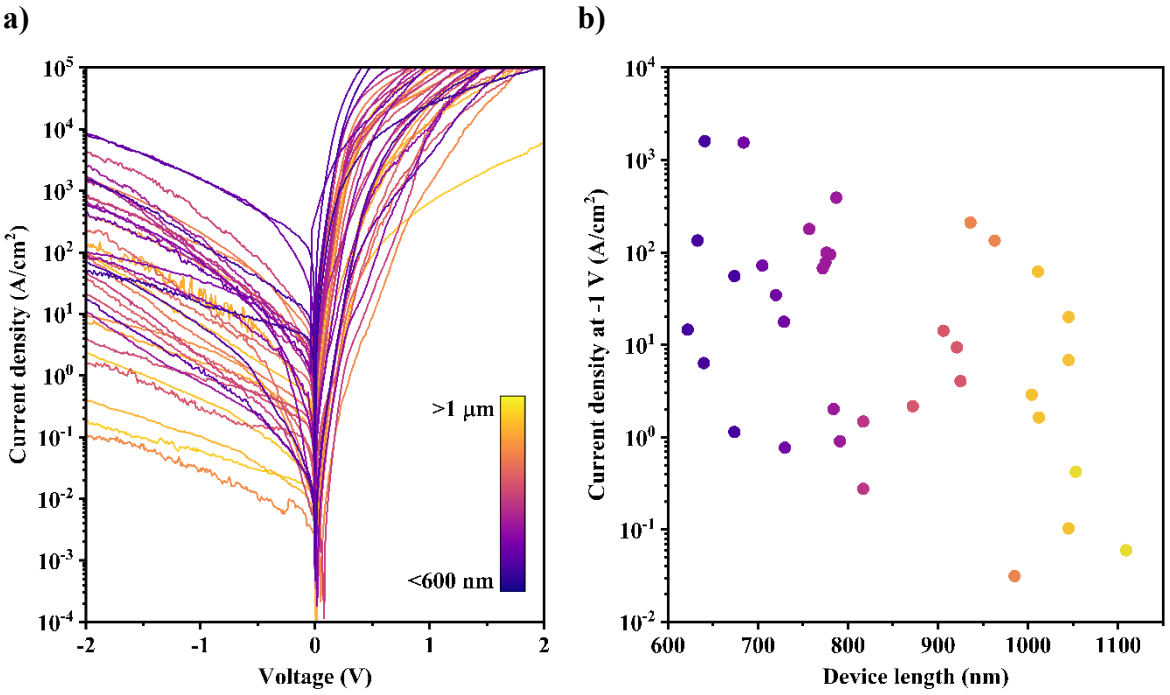


Fig 4-6. a) Experimental I-V curves coloured with respect to the length of the measured devices [125] reproduced with permission © 2024 IEEE. b) Current density values extracted from (a) at a voltage value of -1 V, plotted against the device length for better visualisation.

As a general trend, it can be observed that longer devices tend to have lower dark current densities due to the higher likelihood of the InGaAs region being further from the contacts. However, this trend is not always consistent, as the growth front can cause the InGaAs to be positioned under one or both contacts, as shown in Fig 4-5 with devices 1 and 2. Additionally, potential defects in the NWs may further impact the consistency of this trend.

It can thus be concluded that the variations in growth fronts, as shown in Fig 4-2, are the primary cause of the significant variability observed in the fabricated devices [125]. These variations influence the shape and length of the different regions within the devices. As mentioned before, the different crystallographic directions have distinct growth rates, which not only result in devices with varying lengths but also produce different facets on the grown nanowires.

Additionally, although the impact of these variations on the incorporation of Indium and the composition of the InGaAs is not expected to play a significant role, it is not entirely dismissed [111]. These variations in length also lead to different doping profiles, which could be an area of future research.

The most effective way to improve control during the growth of the III-V materials would be to use a (110) SOI substrate. This substrate aligns with the optimal growth direction of InP, thereby ensuring the stabilisation of a flat growth front [127]. Fig 4-7 presents Transmission Electron Microscopy (TEM) images of the cross-sections of devices fabricated on both (001) SOI and (110) SOI substrates, obtained through a Focused Ion Beam (FIB) cut.

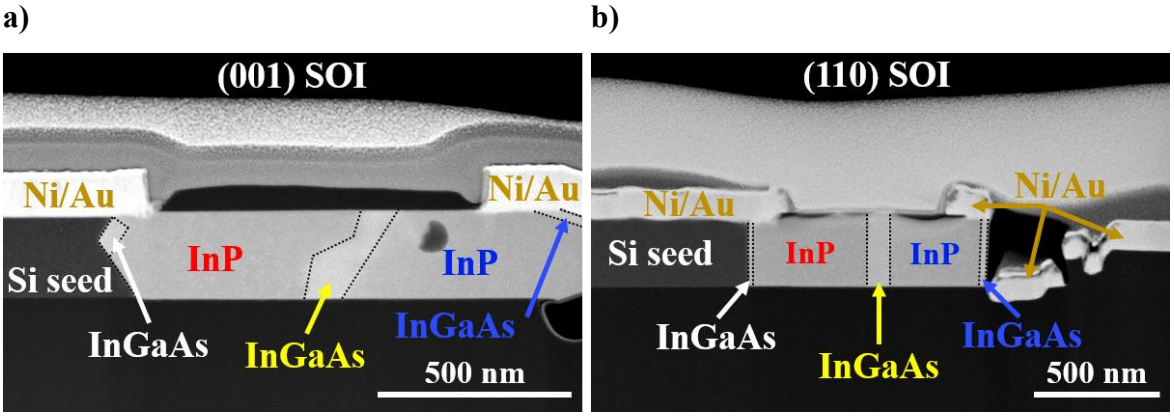


Fig 4-7. TEM images of the cross section of the n-InP/i-InGaAs/p-InP/p-InGaAs fabricated devices a) on a (001) SOI platform showing different crystals and changes of orientation within the device and b) on a (110) SOI platform showing straight facets all along the device.

The images in Fig 4-7 clearly illustrate the contrast between the two types of SOI wafers and their significant impact on the growth of III-V materials. The device grown on a (110) SOI (Fig 4-7b) exhibits perfectly straight interfaces, while the device grown on a (001) SOI (Fig 4-7a) presents different growth fronts and potentially different crystal structures within the device. The effect of these differences on the electrical performance of the devices is presented in the graphs in Fig 4-8, which plot a selection of 100 devices from each wafer type.

By analysing 100 devices of each wafer type, rather than only the highest-performing ones, the full range of electrical performance variability becomes apparent. Although the (110) SOI wafer used had to be thinned down to obtain the desired thickness of the devices, resulting in a lower quality of the Si layer, the I-V characteristics obtained from these devices outmatch the ones from the (001) SOI platform. Using an optimal wafer, such as a (110) SOI, substantially reduces the performance variability of the devices by three orders of magnitude. This marks the first demonstration of III-V photodetectors integrated by TASE on a (110) SOI platform, resulting in atomically smooth interfaces and straight growth fronts.

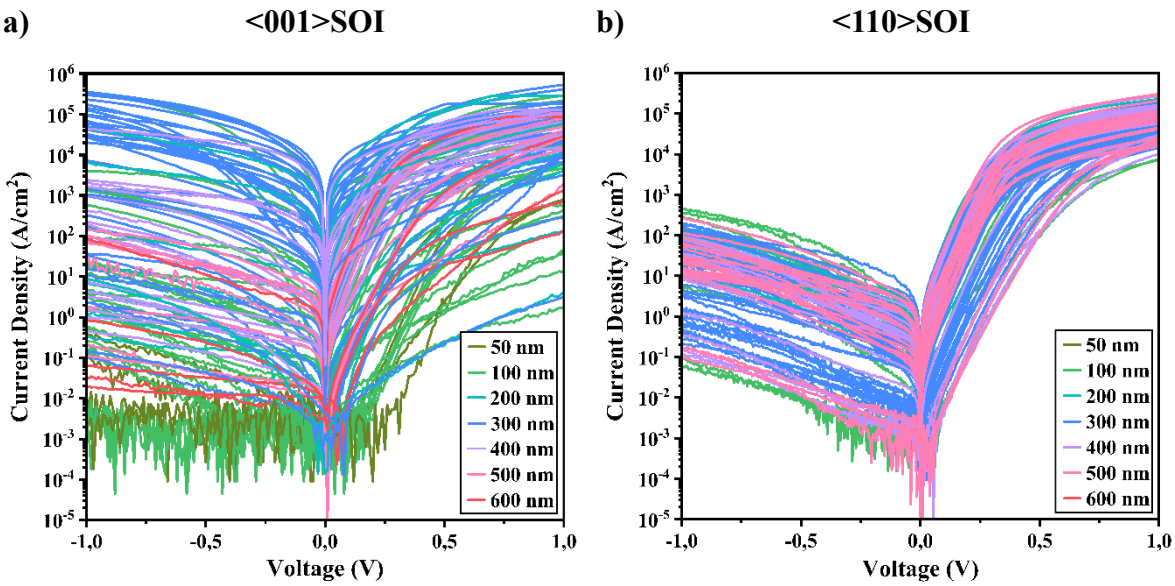


Fig 4-8. I-V characteristics of 100 devices grown a) on a (001) SOI wafer and b) on a (110) SOI wafer. The colours correspond to the width of the devices.

While the variation in device length on the (110) SOI platform is not as pronounced as it is on the (001) SOI, a slight variation persists, likely coming from the width differences and the position in the sample. It has been observed that different regions within the 2x2 cm^2 chip tend to exhibit varying final device lengths, possibly due to the positioning of the sample holder in the MOCVD chamber.

The variability in growth rates for devices grown in each platform can be clearly seen in the test structures included in the different samples. SEM images of these test structures, for a (001) SOI and a (110) SOI are shown in Fig 4-9a and Fig 4-9b, respectively. This enhancement in device reliability advances the integration of these devices into a full optical link, promoting more efficient integration of the optoelectronics platform.

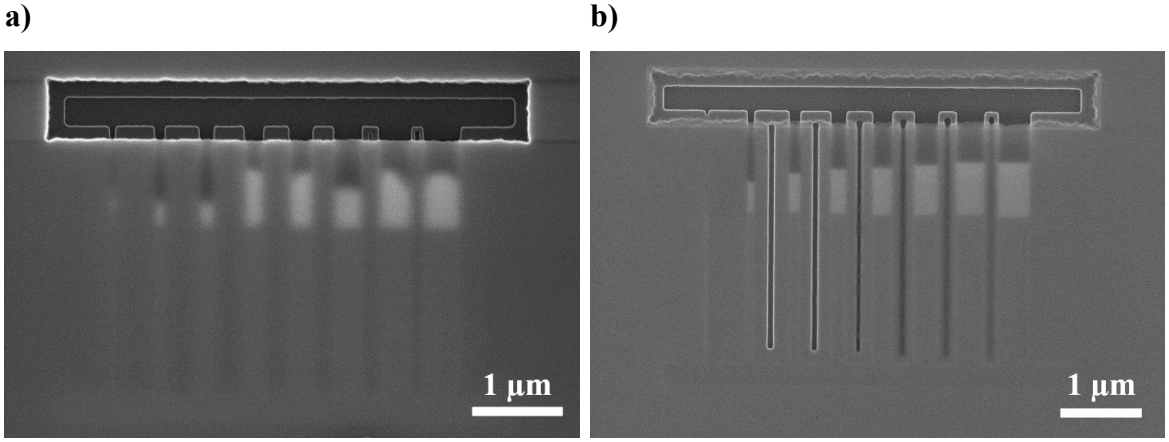


Fig 4-9. SEM images of the test structures from a grown sample in a) a (001) SOI wafer and b) a (110) SOI wafer.

Improvement is necessary to further reduce the variability in the electrical performance of the photodetectors. One approach, which began being explored during this thesis, is the fabrication of funnel-shaped devices. These devices, as previously demonstrated, are grown using a two-step growth process from both ends of the device. This method could help maintain the InGaAs region more centred within the device and farther from the contacts, which may reduce variability in electrical performance. However, the drawback of this approach is that it introduces additional complexity to an already intricate fabrication process.

A second approach could involve increasing the overall length of the device, particularly the InP regions. This would ensure that the InGaAs region in the centre does not overlap with the contacts, thus improving performance by minimising unwanted interactions with the electrical contacts. However, the disadvantage of this method is that it may lead to larger device footprints, which could increase the overall size and cost of the photodetectors, as well as complicate their integration into compact photonic circuits. Additionally, larger devices could suffer from increased capacitance, which may affect their high-speed performance.

The electrical characterisation of the large number of fabricated devices provided the statistical data needed to analyse and understand the source of the variability between them. The primary factor contributing to this variability was identified as the positioning of the InGaAs region relative to the contacts. This discovery points to a key area for improvement in future research, focusing on optimising and enhancing the reliability of the devices.

4.2. Optical characterisation

In this section, free-space illumination was first conducted on the devices without waveguide coupling, allowing for the optical characterisation of the fabricated photodetectors and confirmation of their functionality. Different illumination powers and wavelengths were used in this study to assess the devices' response under different conditions.

Subsequently, a second study was carried out on waveguide-coupled devices, as a step toward integrating the photodetectors into a complete optical link. Despite the inclusion of mirrors designed for back-reflection in the device designs, no definitive conclusions were reached due to the significant variability in electrical performance across individual devices.

The waveguide-coupled devices were also used to explore the performance of the photodetectors at cryogenic temperatures. This study was conducted in collaboration with a master's student, who continued the measurements after my departure from IBM. All results from this study have been included in this thesis to ensure a comprehensive conclusion. It is clearly indicated in the results section where the measurements were performed by someone else, beginning from Fig 4-20 onward.

To optically characterise the devices, a home-built optical setup is used, as shown in Fig 4-10. This setup was built by previous PhD students in the group at IBM. The setup features two light paths: one for the excitation source (red) and the other for imaging (orange), which are combined using a removable pellicle beamsplitter.

A tuneable-wavelength supercontinuum laser (NKT Photonics SuperK Extreme) spanning 640 nm to 2000 nm serves as the excitation source, emitting picosecond pulses at a 78 MHz repetition rate. A short pass filter at 1160 nm wavelength is added to block higher harmonics from the pump laser. A dichroic beamsplitter separates the excitation and detection paths. The detection path includes a long pass filter at 1160 nm to block unwanted reflections before reaching the spectrometer (Princeton Instruments Acton SpectraPro SP-2500).

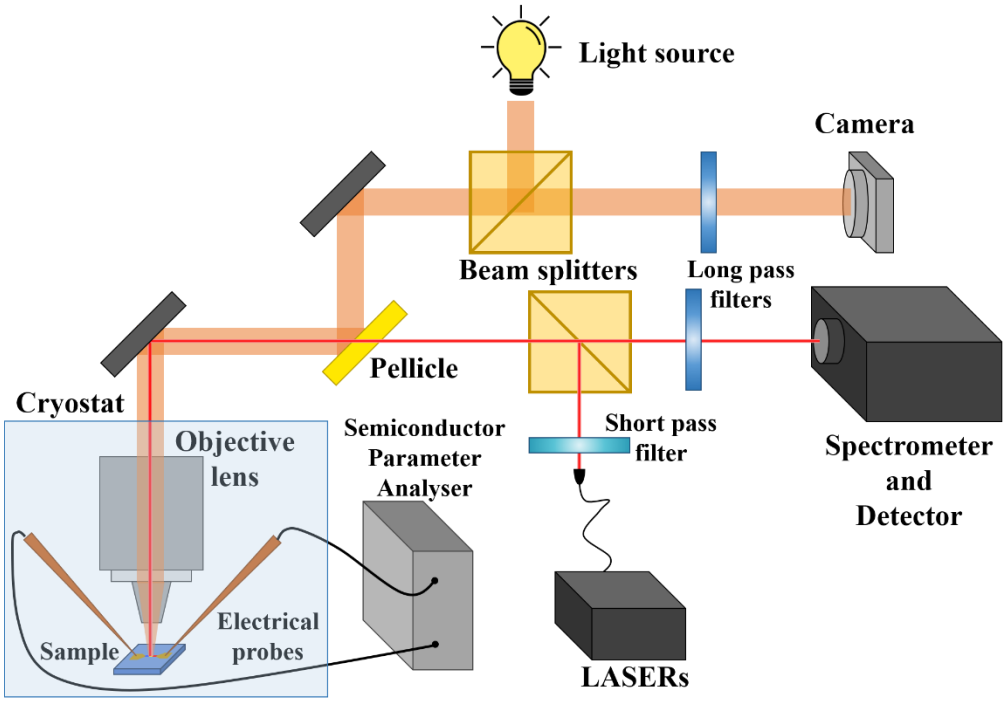


Fig 4-10. Simplified schematic of the optical setup used for the electro-optical measurements. The orange light path corresponds to the imaging of the sample under white light illumination while the red path corresponds to measurement of the photoluminescence (PL) signal. The excitation lasers are coupled into the setup through fibres. Inside the cryostat, an objective focuses light onto the sample.

In the (red) light path shown in the schematic of Fig 4-10, the sample is illuminated through a 10x magnification objective lens, which focuses the laser onto the sample. Higher magnification objective lenses are larger and cannot fit with the hight of the electrical probes. Alternatively, devices can be excited by directly positioning an optical fiber above the sample, though this setup prevents the use of an objective lens in the cryostat for imaging. The holders used for the fibers align them with the sample at a 10° angle to its surface.

For the imaging path, a white light source illuminates the sample, which is then captured by a camera. Another long pass filter is added to remove the pump laser. The imaging optical path is used to carefully position the desired device under the excitation light path and align the electrical probes with its metal contacts.

The sample is placed on a sample holder stage equipped with x-y-z-piezo actuators for precise positioning. The electrical contact probes also have x-y-z-piezo actuators to control their movements accurately for electrical characterisation of the devices.

Temperature measurements were later performed with this setup using a vacuum chamber. The chamber size prevents the use of the objective lens, requiring the use of the direct fibre excitation. The stage can be cooled down to 80 K using liquid Nitrogen or to 5 K with liquid Helium. Temperature is controlled using a proportional-integral-derivative (PID) controller with several temperature sensor inputs and heating outputs.

The responsivity of the nanowires varies depending on whether they are illuminated from above in free space through a lens or using a fiber and through a waveguide from the side. Responsivity (ρ), previously explained in section 1.4 (equation 1.6) and defined as the ratio of generated photocurrent to the power reaching the sample, can be estimated for both scenarios.

Given that dark current measurements are often noisy, the responsivity is typically calculated as the difference in photocurrent at 100% and 10% laser powers, divided by the corresponding difference in power levels. This approach reduces the impact of noise and provides a more accurate representation of the device's response to incident light.

For free-space illumination, the spot size of the laser on the sample must be multiplied by the top absorbing area of the nanowire, primarily the InGaAs region, which depends on the device width. Additionally, as both cases account for different dimensions on the wire, the thickness of the wire will serve as the absorption length comparison, incorporated through the Beer-Lambert law.

For the waveguide-coupled case, the responsivity calculation involves multiplying the laser power by the grating coupling efficiency and the ratio of the waveguide's cross-sectional area to the side-absorbing InGaAs region of the nanowire, which remains constant across all wires. However, unlike free-space illumination, the absorption length varies with the width of the device and is incorporated into the Beer-Lambert law.

In both cases, the responsivity will be calculated at a wavelength of 1550 nm, as the absorption coefficient and laser power vary with different wavelengths. Additionally, for the waveguide-coupled scenario, the grating coupling efficiency is not constant across wavelengths, which further impacts the calculation of responsivity. Taking into account the optical setup, the responsivity in both free-space and waveguide coupling configurations can be expressed as follows:

$$\rho_{free\ space} = \frac{i_p}{P} = \frac{i_{100\%} - i_{10\%}}{(P_{100\%} - P_{10\%}) \cdot \frac{w \cdot l_{InGaAs}}{A_{spot\ size}} \cdot (1 - e^{-\alpha \cdot t})} \quad (4.1)$$

$$\rho_{waveguide\ coupled} = \frac{i_p}{P} = \frac{i_{100\%} - i_{10\%}}{(P_{100\%} - P_{10\%}) \cdot \eta_{GC} \cdot \frac{t \cdot l_{InGaAs}}{A_{waveguide}} \cdot (1 - e^{-\alpha \cdot w})} \quad (4.2)$$

where $i_{100\%}$ and $i_{10\%}$ are the photocurrent values at -0.5 V at 100% and 10% laser power respectively, $P_{100\%}$ and $P_{10\%}$ are the corresponding laser powers which reach the sample plane in the case of the free space illumination and out of the fiber in case of the waveguide coupled one, η_{GC} is the simulated grating coupler's efficiency, w is the width of the device, l_{InGaAs} is the length of the InGaAs region, t is the thickness of the device, $A_{spotsixze}$ is the laser's spot size area, $A_{waveguide}$ is the lateral area of the waveguide, and α is the absorption coefficient, which at 1550 nm for InGaAs is 0.6 μm^{-1}.

For the free-space illumination case, the wire with a 400 nm width, as shown in the photoinduced I-V characteristics in Fig 4-11d, is used to calculate the responsivity, which gives a value of $\rho_{free\ space}$ = 0.048 A/W. For waveguide-coupled illumination, the 100 nm wide wire shown in Fig 4-15d is used, giving a value of $\rho_{waveguide\ coupled}$ = 0.018 A/W. Although the difference in wire widths makes a direct comparison difficult, there is no available data for the same wire width under both free-space and waveguide-coupled illumination methods.

To estimate the responsivity of the fabricated devices, several assumptions were made. In case of the 400 nm wide device, the length of the InGaAs region has been measured to approximately 220 nm, while for the 100 nm wide device is approximately 130 nm. For the waveguide-coupled case, the grating coupling efficiency is assumed to be 39%, based on simulations, though the actual value is likely lower due to fabrication imperfections. Factors such as defects in the nanowires and deviations from ideal conditions are not considered in this estimation. Similarly, Fresnel losses at the air/material interface are also neglected. All these factors would likely reduce the final responsivity values.

4.2.1. Free-space illumination

The first step of optical characterisation involved free-space illumination of the devices through the optical lens in a reflection mode setup. To confirm that the fabricated devices function as photodetectors, their current response was measured as a function of different illumination powers at different wavelengths.

The I-V curves for 600 nm and 400 nm wide devices are shown in Fig 4-11, where a power sweep (with different power scales) was performed for wavelengths (λ) of 1100 nm and 1500 nm for the 600 nm device, and 1350 nm and 1550 nm for the 400 nm device. These wavelengths were selected to avoid absorption from InP, which has a cut-off at λ ≈ 1000 nm.

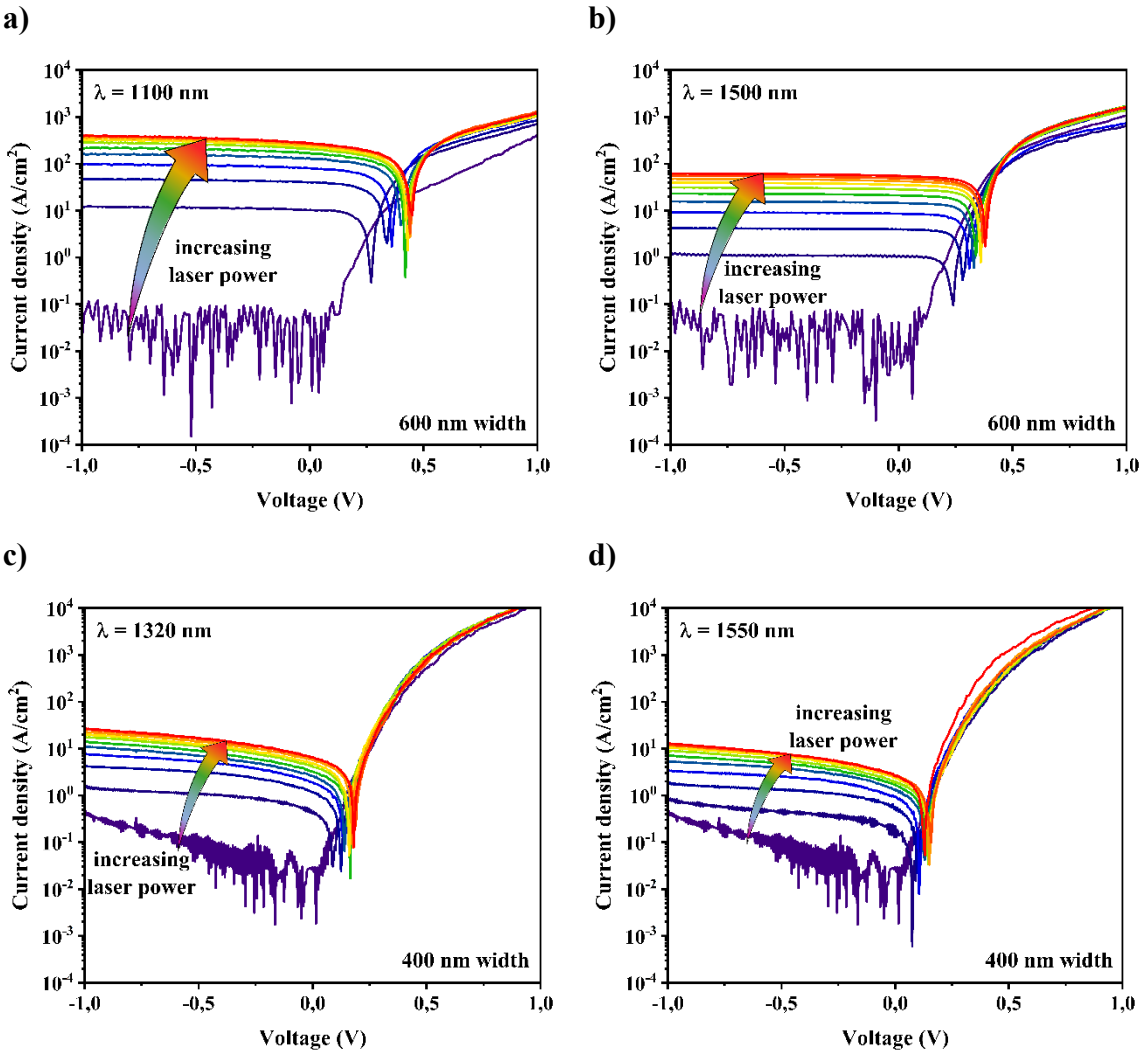


Fig 4-11. Photoinduced I-V characteristics for free-space illuminated devices at room temperature for increasing laser powers shown by the multicoloured arrow at a) λ = 1100 nm (up to ~60.8 μW) and b) λ = 1500 nm (up to ~2.22 μW) for a 600 nm wide device, and c) λ = 1350 nm (up to ~1.97 μW) and d) λ = 1550 nm (up to ~1.76 μW) for a 400 nm wide device.

The I-V characteristics exhibit the expected behaviour for the fabricated devices. The difference between the dark current and the photocurrent spans several orders of magnitude, indicating good responsivity values for photodetection.

As expected, the lowest wavelength measured (λ = 1100 nm) shows the highest responsivity due to InGaAs having a higher absorption coefficient at shorter wavelengths, as shown in Fig 1-2. However, the wavelengths of interest for photonic integrated circuits (PICs) are those beyond the Si absorption edge (λ = 1300 nm), which still demonstrate a significant difference between dark and photocurrent, spanning several orders of magnitude. The highest wavelength measured (λ = 1550 nm) shows the lowest difference between dark current and photocurrent, as it is near the absorption edge of InGaAs, which reaches a null absorption around 1700-1800 nm [128].

As illustrated in Fig 4-1, the devices show significant variability in their I-V curves, affecting both dark and photocurrent values. This variability prevents direct comparison between different devices, so the wavelength comparisons can only be made within the same device.

4.2.2. Waveguide coupled

The next optical characterisation step involved measuring the current response of waveguide (WG) coupled devices, advancing towards achieving a full optical link. The waveguide coupler design was performed by post-doc researcher Simone Iadanza, including an appropriate grating coupler design necessary for routing the laser between optical fibers and the photonic integrated circuit, targeting a wavelength of 1550 nm with a coupling efficiency of 39%. The simulated response of the grating coupler, including the wavelength dependency of the transmission and reflection, is shown in Fig 4-12.

The simplest design added onto the fabricated samples consists of a grating coupler connected to a straight WG that reaches the devices. The WG has the same thickness as the wires (220 nm) and a width of 450 nm. Additional designs, intended to improve the signal reaching the devices, include tapered WGs to expand the mode and reduce reflection from its flat surface, as well as various mirrors (low-contrast Bragg grating, high-contrast Bragg grating, demi Zone-Plate) to reflect back scattered light. These designs are illustrated in Fig 3-5d, and SEM images of fabricated devices with different configurations are shown in Fig 4-13.

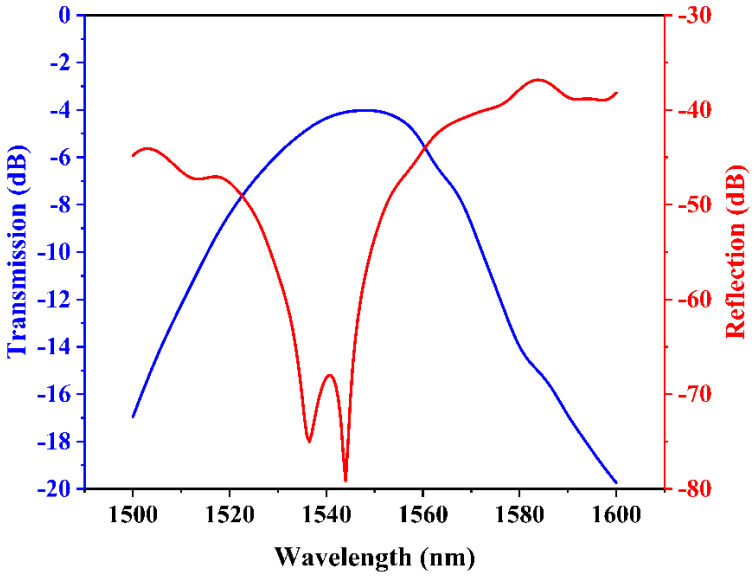


Fig 4-12. Simulated wavelength response of the grating coupler design in transmission (blue) and reflection (red). Note the different ranges on the two y-axis.

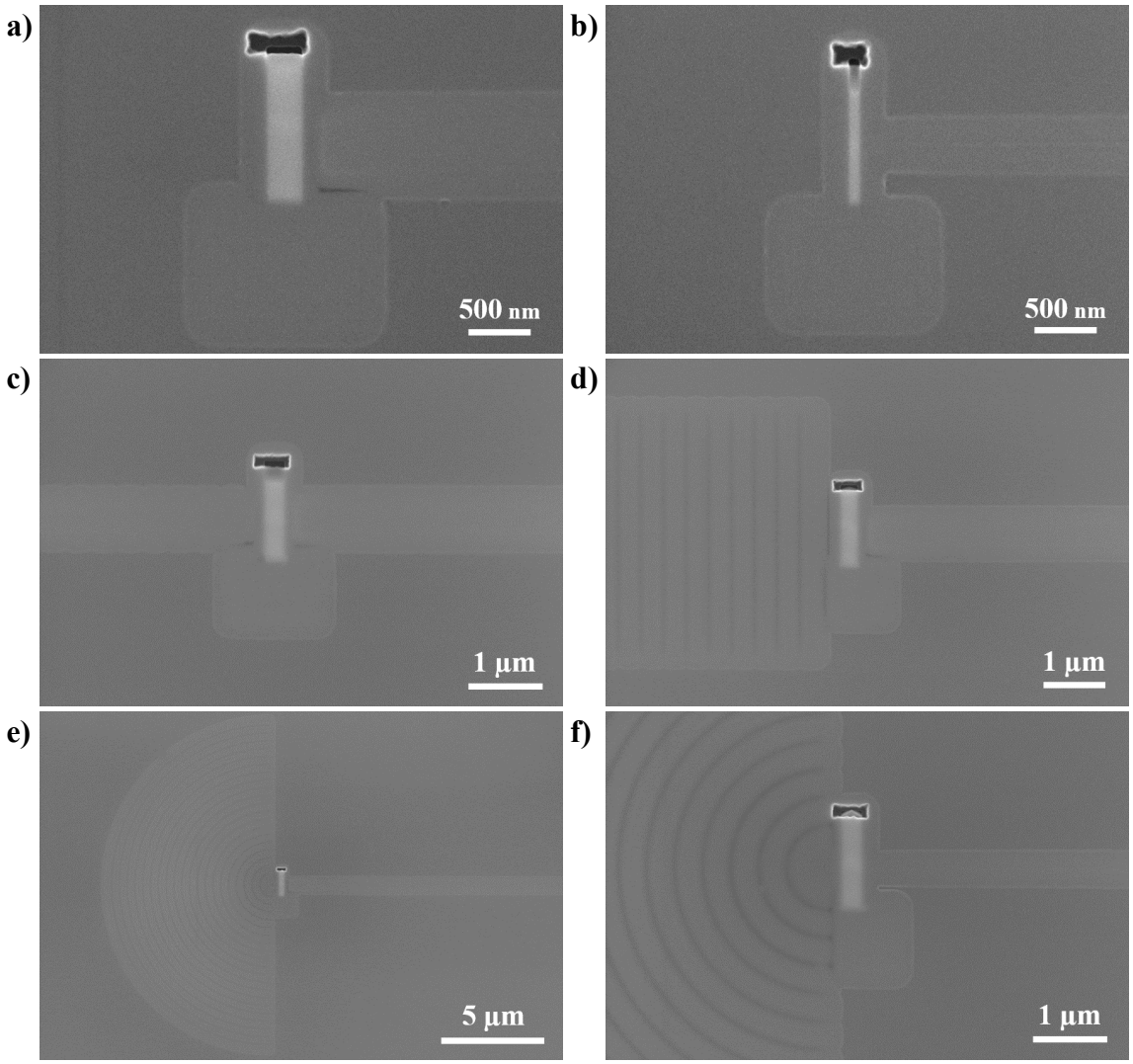


Fig 4-13. SEM images of the waveguide coupled devices: a) and b) without a back-reflecting mirror, a) a 300 nm wide NW with a straight WG and b) a 100 nm wide NW with a tapered WG. c) Show 300 nm wide devices with a low-contrast Bragg grating, d) with a high-contrast Bragg grating, and e) - f) with a demi Zone-Plate with different magnification values.

The initial test on these samples was a wavelength sweep to confirm the grating coupler response. The first sweep, ranging from 1200 nm to 1600 nm in steps of 50 nm and from 1500 nm to 1600 nm in steps of 10 nm, is shown with purple lines in Fig 4-14a. The light purple line indicates two peaks: the expected one at 1550 nm and another around 1300 nm.

For each device and wavelength measured, the fiber needed to be aligned with the grating coupler, in the x-y-z position and in polarisation. A realignment of the fiber for a 1300 nm wavelength was necessary before performing a second wavelength sweep, shown with blue lines in Fig 4-14a.

Images from the infrared (IR) camera of a device response while coupling light through the grating coupler for the two wavelengths, 1550 nm and 1300 nm, are shown in Fig 4-14b and Fig 4-14c, respectively. On the top of the images there is the fiber in dark, with light escaping from the fiber due to the loses of the grating coupler, which has an efficiency of less than 39%. On the bottom of the images, the electrical probes can be seen in black coming out of the sides and on the metal contacts, in light grey. In the centre between the contacts is where the wire is, and some light can be seen reaching it from the end of the waveguide.

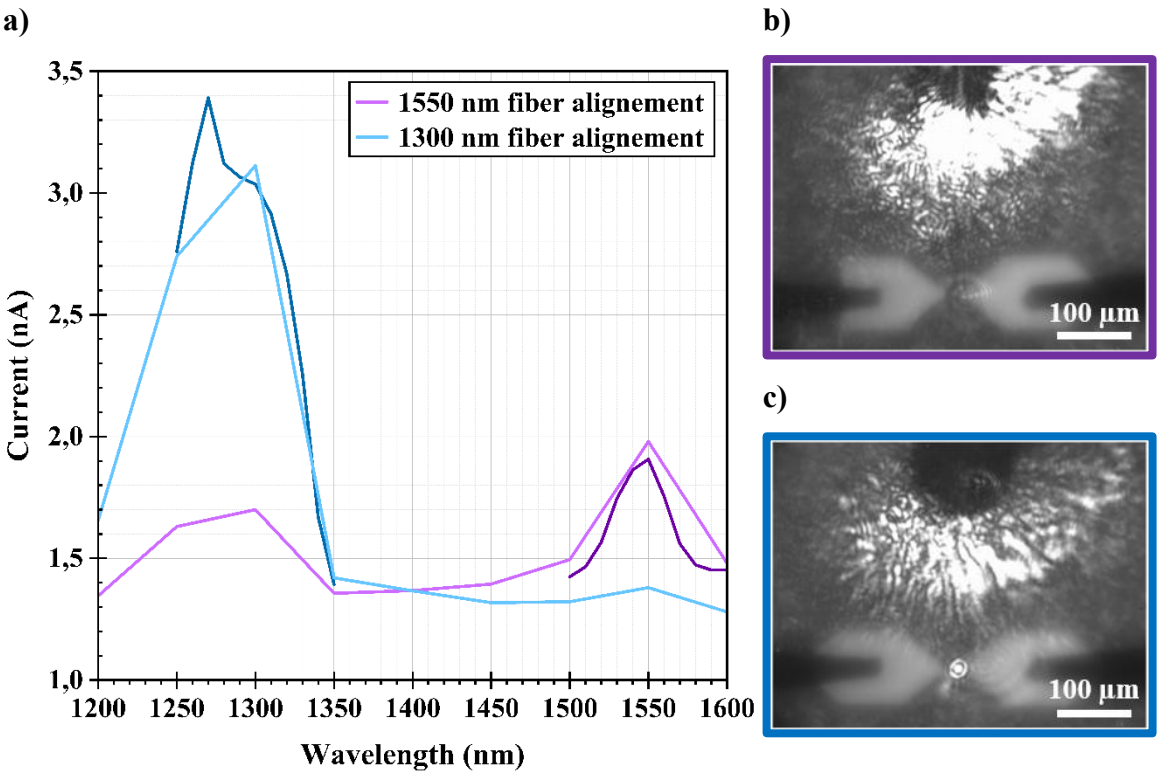


Fig 4-14. a) Wavelength response plot of a waveguide coupled device. The polarisation of the fiber has been aligned to get a maximum light response of the device at 1300 nm (blue) and at 1550 nm (purple). On the right, infrared camera images of the devices response to coupled light with b) a 1550 nm and c) a 1300 nm wavelength.

The fabricated devices with waveguide coupling have widths of 50 nm, 100 nm, 300 nm, and 500 nm. As they were fabricated on a (001) SOI, their I-V characteristics exhibit a wide spread similar to those shown in the previous subsection (Fig 4-8a). This variability complicates the comparison between devices with different designs (tapered/straight waveguides and different mirrors for back-reflection). These designs were also fabricated on a (110) SOI wafer, but due to time constraints, no optical characterisation was performed on them. This is already a topic of research that has continued after the work in this thesis.

The wavelength response observed in Fig 4-14 is shown as I-V plots for increasing laser powers at different wavelengths. These plots can be seen in Fig 4-15, where a mere 100 nm difference in wavelength, from both previously observed peaks, results in a half-order magnitude difference in the photocurrent obtained on a 100 nm wide device. This device is coupled with a straight WG and does not have any mirror for back-reflection.

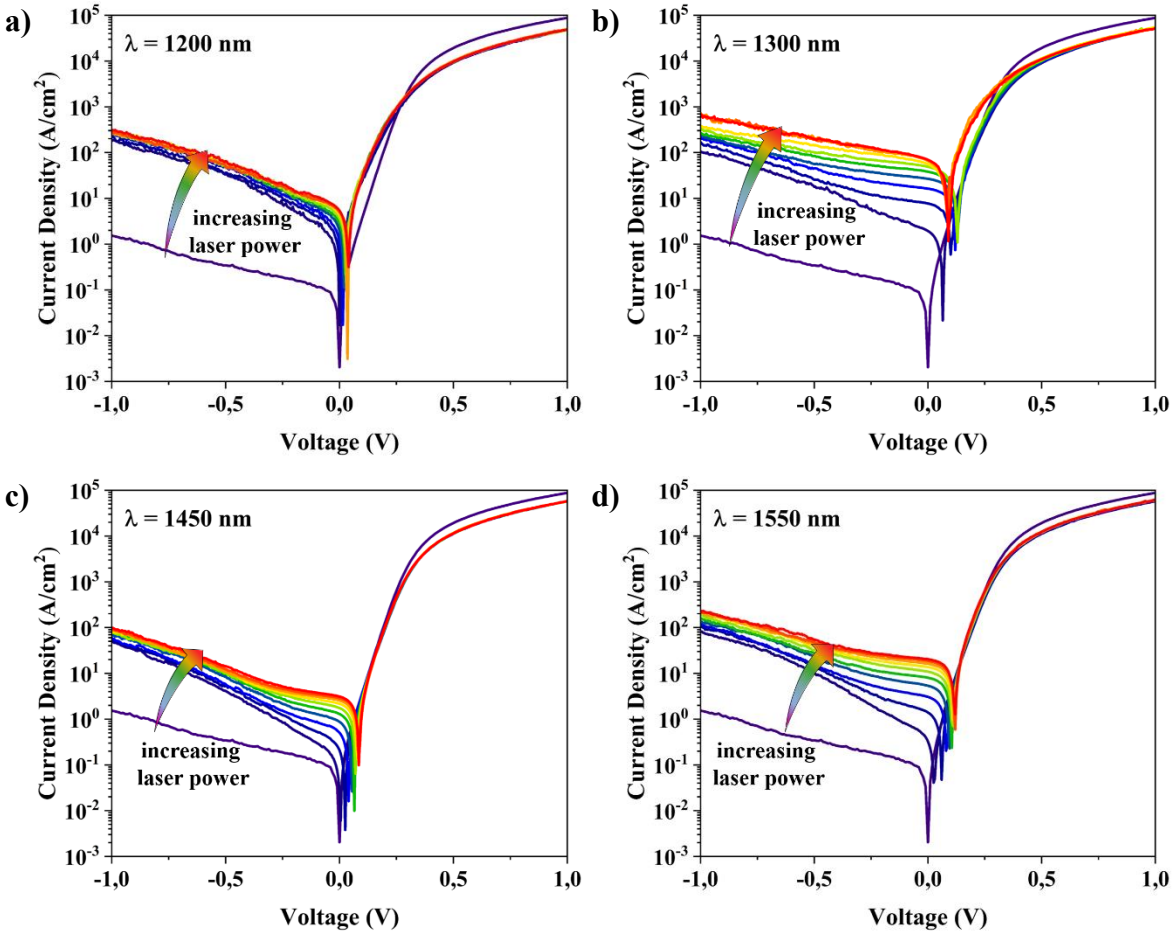


Fig 4-15. Photoinduced I-V characteristics at room temperature for a straight waveguide coupled 100 nm wide device without back-reflection for increasing laser powers shown by the multicoloured arrow at a) λ = 1200 nm, b) λ = 1300 nm, c) λ = 1450 nm, d) λ = 1550 nm.

Another reproducibility issue comes from the optical setup used. Due to the various capabilities of the setup and the high demand from researchers for different experiments, results may vary from day to day even when using the same settings. Consequently, only measurements performed on the same day are plotted together and used for comparison. The electrical connections of the setup have shown parasitic values that interfere with the low current values obtained from the I-V characteristics of the fabricated devices. This electrical leakage noise is due to nonstable and weak shielded wires connecting the electrical probes to the Agilent. For this reason, the dark current I-V curves plotted are usually the ones obtained in the clean-room, as the setup's parasitic current values are lower there.

Despite the lack of reproducibility, plots for the different device designs on a (001) SOI are shown in Fig 4-16, for 100 nm wide devices. These include straight WG coupled devices with different mirrors (and no mirror) for increasing laser power at both 1310 nm and 1550 nm wavelengths.

As previously mentioned, differences in optical performance between design variations are not apparent due to the variability in the electrical performance of the devices. The dark-current I-V curves vary in both shape and current density values, and the high parasitic current values of the optical setup hinder the responsivity of some devices. Nevertheless, all the devices exhibit an increase in current density at negative voltage values for both plotted wavelengths, with slightly higher photocurrent values at 1310 nm than at 1550 nm, as would be expected.

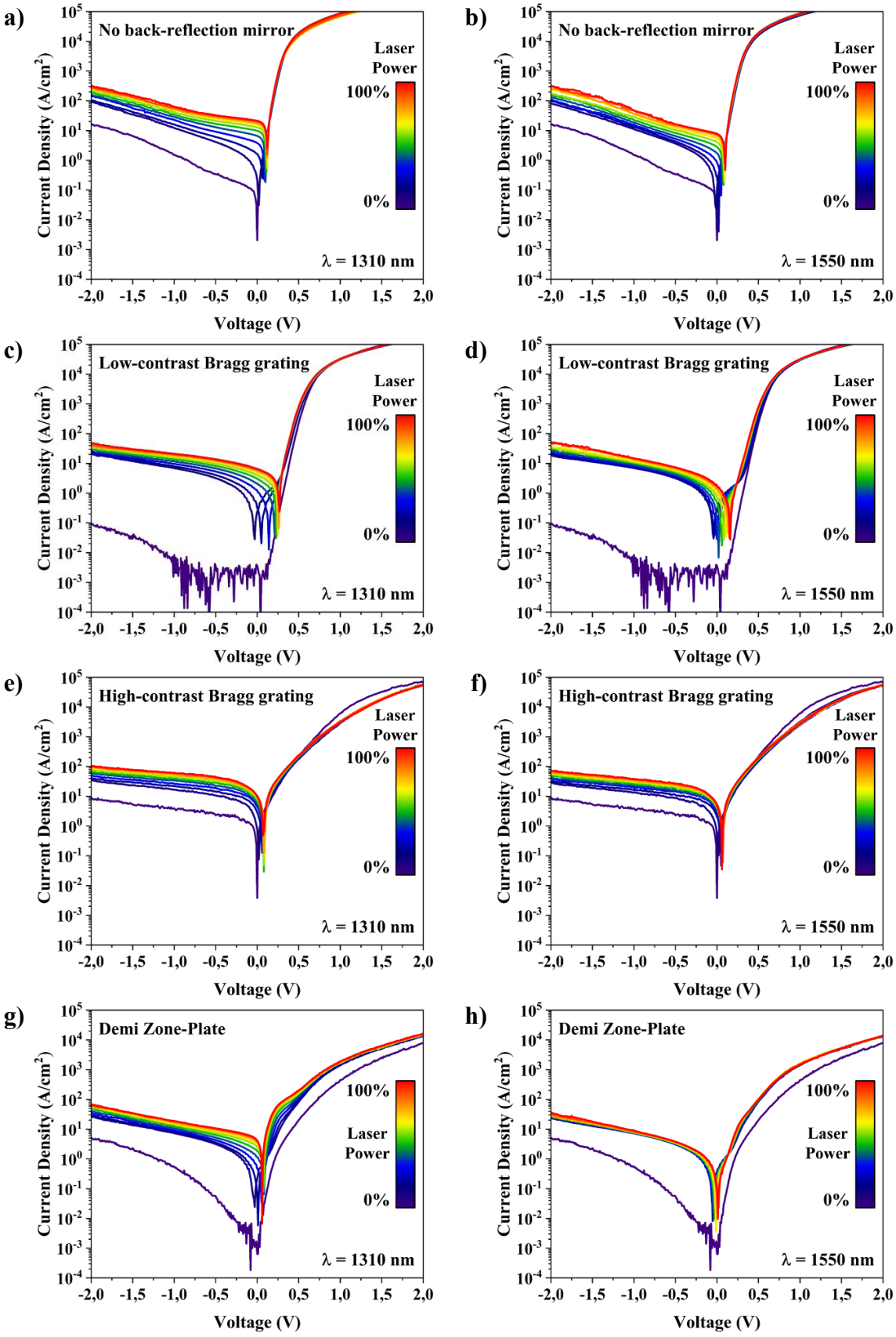


Fig 4-16. I-V curves at room temperature for straight waveguide coupled 100 nm wide devices for increased laser power at 1310 nm (left column) and 1550 nm (right column) for straight waveguide coupled devices with a) and b) no back-reflecting mirror, c) and d) a low contrast Bragg grating, e) and f) a high-contrast Bragg-grating, and g) and h) a demi Zone-Plate. The 100% power out of the fiber at 1310 nm is 119 μW and at 1550 nm is 106 μW.

4.2.3. Low temperature measurements

This section includes the work undertaken in collaboration with Myriam Rihani as part of her Master's Thesis titled "Cryogenic Characterisation and System Modelling of Photonic Devices for Quantum Technologies" at EPFL. It explores the performance of the III-V NW devices at cryogenic temperatures as electro-optic converters for quantum computing technologies.

Optical interconnects present several advantages over electronic ones in quantum technologies. Unlike electrical connections, optical interconnects can handle much higher data rates, with current technologies enabling transmission speeds of up to several terabits per second (Tbps) over a single optical fiber [129, 130]. This is orders of magnitude greater than what conventional electrical interconnects can achieve, typically capped at a few gigabits per second (Gbps) per channel [131]. The higher bandwidth [132] and low crosstalk characteristics [133] are critical for maintaining the fidelity of quantum information. Additionally, quantum applications such as quantum error correction, where real time decoding is crucial, could benefit from the lower latency of optical interconnects.

These factors make optical interconnects ideal for complex tasks like signal multiplexing, where maintaining signal integrity and reducing inter-channel interference are of the highest importance. Integrating electro-optic converters on a silicon chip at cryogenic temperatures is a crucial step towards realising large-scale quantum systems.

Following the earlier optical characterisation of waveguide-coupled devices at room temperature, measurements were taken at different temperatures, ranging from 300 K to 80 K using liquid Nitrogen, and from 300 K to 5 K using liquid Helium.

The selected devices measured demonstrated high on/off contrast between reverse and forward bias in their dark behaviour. Given that dark current changes with temperature, all the I-V curves plotted in this subsection were obtained in the cryostat. The dark-current I-V curves at different temperatures for the same device that was optically characterised at room temperature (as shown in Fig 4-16a and b) are presented in Fig 4-17.

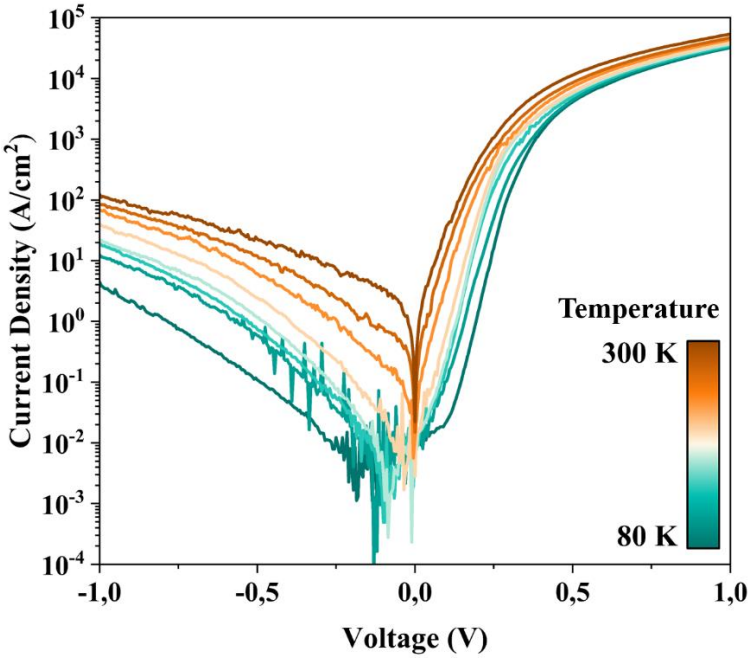


Fig 4-17. Dark current I-V characteristics for a 100 nm wide device at temperatures that go from 300 K to 80 K.

Although the dark-current measurements should show a dip in the I-V curves at 0 V, the lower temperature ones exhibit a shift of the dip to the left. This is due to these curves reaching the electrical leakage noise levels of the system, preventing them from reaching the real current values at those voltages. Despite this, the dark current decreases with temperature as expected, and the forward bias slope becomes steeper. This behaviour is attributed to several factors, including the reduction in thermally generated electron-hole pairs, the decreasing impact of traps, and the intrinsic carrier concentration decreasing with temperature, alongside bandgap narrowing.

The dark current values in reverse bias from Fig 4-17 allow the extraction of the activation energy using the Richardson-Dushman model. This model assumes that carriers acquire sufficient thermal energy to overcome the potential barrier, making it typically valid under lower electric fields and higher temperatures. The temperature dependence of dark current is described by the equation:

$$I_{dark} = A \cdot T^{3/2} \cdot \exp\left(-E_a/k_B T\right) \tag{4.3}$$

where E_a is the activation energy, A is the Richardson constant, k_B is the Boltzmann constant and T is the temperature. According to this equation, plotting ln $(I/T^{3/2})$ versus $1/k_B T$ at different voltages should yield straight lines. The slope of these lines provides the activation energy, E_a, as derived from experimental I-V Arrhenius plots shown in Fig 4-18.

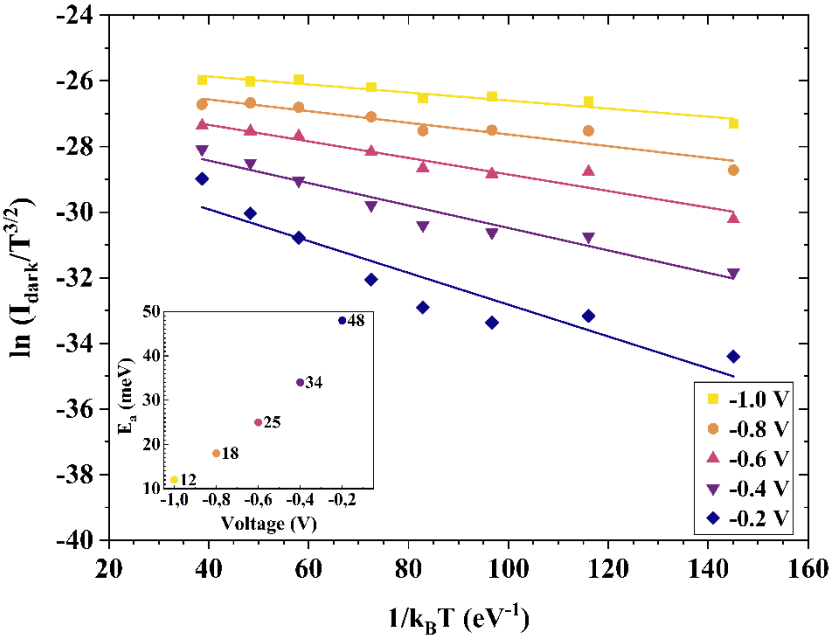


Fig 4-18. Arrhenius plot for the 100 nm wide devices. The different curves correspond to the current values extracted at different reverse voltages. The temperatures range from 80 K to 300 K. The inset displays the activation energy versus the voltage, extracted from the slope of fitting the data.

The low activation energy values obtained from the Arrhenius plot in Fig 4-18 suggest that the dark current might originate from trap-assisted tunnelling current. This is consistent with other studies on p-InP/i-InGaAs/n-InP photodiodes, where similar low activation energies (of the same order of magnitude) have been reported [134].

Due to the large amount of optical data collected at each temperature, the laser sweep depicted in Fig 4-19 is shown only at 80 K for 1300 nm and 1550 nm wavelengths. The behaviour is similar to that observed at room temperature, with 1300 nm producing a higher response than 1550 nm. Compared to the curves in Fig 4-16a and Fig 4-16b, both dark current and photocurrent values are lower at 80 K than at 300 K. However, the difference between 0% and 100% of power is greater at 80 K, indicating higher responsivity.

The use of the cryostat introduced a new challenge in comparing optical measurements at different temperatures. Temperature changes in the setup caused movement of internal elements, such as the fiber and electrical probes. Stabilising the temperature in the cryostat before starting measurements is crucial to prevent misalignment of the fiber, which can significantly affect the amount of light coupled into the devices. Unfortunately, this step was not always executed with precision, leading to some photocurrent measurements that may not be fully reliable regarding the amount of light reaching the device.

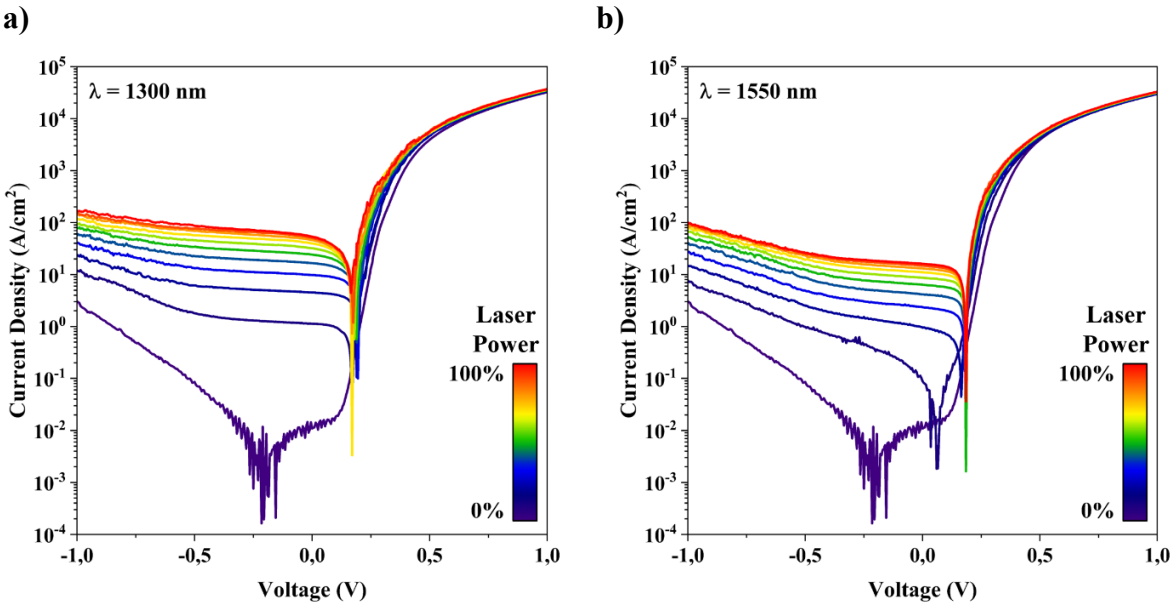


Fig 4-19. I-V curves for increased laser power at 80K for a straight waveguide coupled 100 nm device with no back-reflecting mirror at a) 1300 nm and b) 1550 nm.

The measurements shown below were performed by Myriam Rihani and Simone Iadanza on the devices fabricated during this work, following the low-temperature optical characterisation, in the weeks after departing IBM.

The optical evolution of a device over a broader temperature range, from 5 K to 300 K, is shown in Fig 4-20. This figure illustrates the current density value at -1 V for both dark current and at 100% laser power, at a wavelength of 1550 nm. This device, which is 300 nm wide and has a low-contrast Bragg grating, is illuminated from the top with the fiber rather than through its waveguide.

The I-V curves in Fig 4-20 show unexpected behaviour regarding the off-current values. The on-current behaviour of the curves, both in dark current and photocurrent (since light does not significantly affect forward bias), matches expectations as the temperature decreases, leading to a steeper slope.

However, in reverse bias, photocurrent values were expected to increase with temperature. The observed behaviour could be due to fiber misalignment during temperature changes in the cryostat, as mentioned earlier. In Fig 4-21, where photocurrent values at -1 V with respect to temperature are plotted in red, and the vertical dashed lines group the measurements by the day they were performed, it can be seen that the general trend by day is a reduction in the photocurrent with decreasing temperature, and the jump may be due to the previously mentioned setup issues.

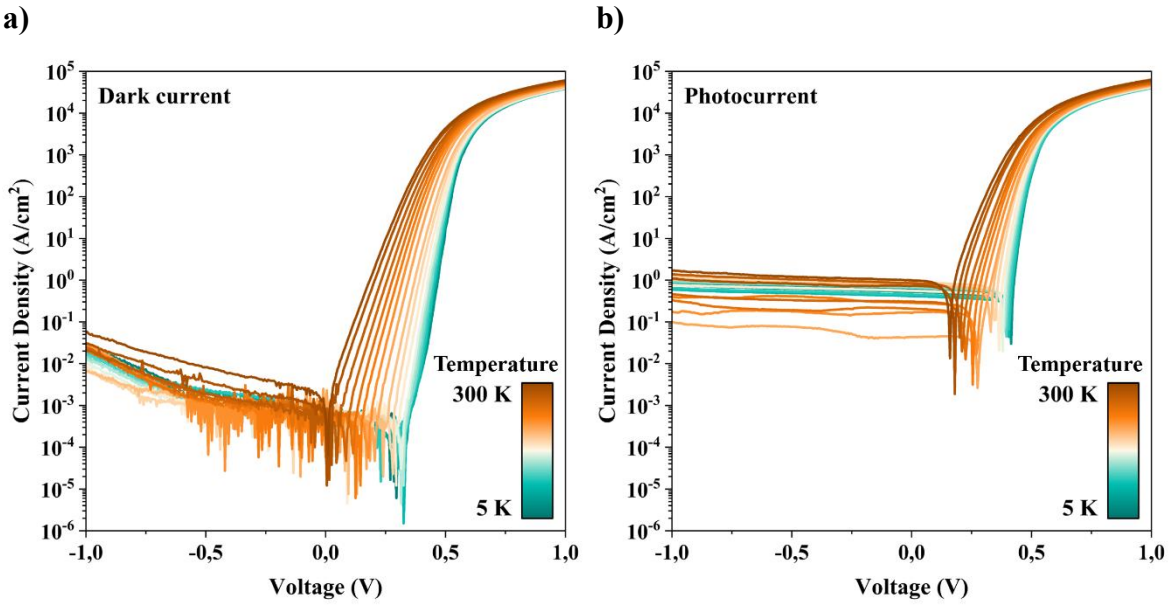


Fig 4-20. I-V characteristics at temperatures ranging 5 K to 300K for a 300 nm wide device a) in dark current and b) in photocurrent illuminating it from the top with light with a 1550 nm wavelength and 100% of laser power.

In regards to the dark-reverse current, the observed behaviour does not match theoretical predictions of a decrease in current with temperature due to diminished thermal excitation of charge carrier, as previously seen in Fig 4-17 for a different device. This new behaviour can be better observed in Fig 4-21, where the dark current density values at -1 V with respect to temperature are plotted in blue.

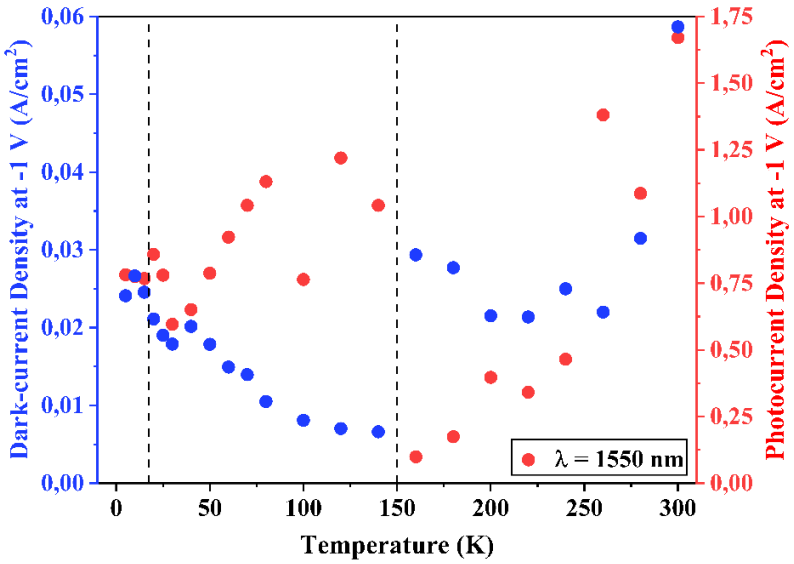


Fig 4-21. Dark-current density (blue) and photocurrent density (red) at -1 V of applied voltage with respect to the temperature, from the data in Fig 4-20. The vertical lines group the measurements performed on different days. Note the different ranges on the two y-axis.

As already mentioned, the dashed lines in Fig 4-21 correspond to different measurement days. Furthermore, the measurements performed at temperatures between 160 K and 300 K were done by using liquid Nitrogen, while those below 140 K were performed with liquid Helium. This could affect the baseline current levels of the measurements.

Despite the jump in current, two trends can be observed in the dark current. From 300 K to 200 K, the general trend is a decrease in dark current with temperature, as expected. For temperatures lower than 200 K, the current density values increase as the temperature decreases.

This behaviour has been observed previously in the work of Liqiang Tian et al. [135], where the resistivity of undoped $In_{0.53}Ga_{0.47}As$ was measured over a 5 K to 300 K temperature range. When comparing trends, the resistivity from their work can be considered as the inverse of the current from this project's experimental data.

The data presented in Tian's paper, shown in Fig 4-22, presents two main trends in resistivity with temperature: an increase in resistivity as the temperature decreases between 300 K and 130 K (regimes V and IV) and between 28 K and 5 K (regime I), and a decrease in resistivity with temperature between 130 K and 40 K (regimes III and II). These regimes, similarly observed in this thesis' data in Fig 4-21 but for different temperature ranges, have been modelled in Tian's work to be related to shallow donor impurity levels and deep defect levels [135].

The theoretical study presented in Tian's article [135] aligns well with their experimental data and can be explained by the competition between mobility carrier scattering and the ionisation process. Increasing the temperature reduces carrier mobility due to scattering processes, which increases resistivity. On the other hand, this same temperature increase leads to the ionisation of different impurity or defect energy levels, which induces a decrease in resistivity due to the presence of more carriers.

The two regions where a decrease in resistivity with an increase in temperature is observed result from the ionisation of defects with different energy levels in the band gap of InGaAs, which have different activation energies leading to two separate ionisation processes at two different temperature ranges [135]. Due to the difference in materials and doping between Tian's work and the work presented in this thesis, these activation energies might differ, which would explain the regions not matching exactly in terms of temperature values.

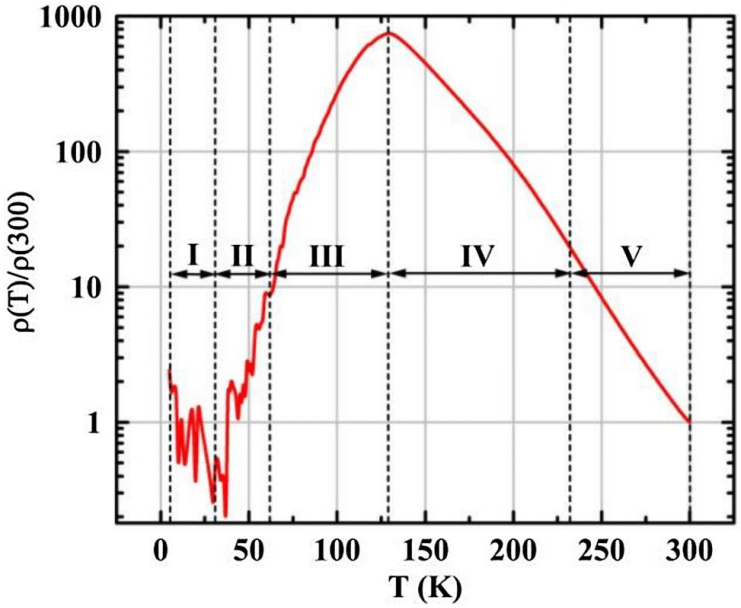


Fig 4-22. Dark resistivity of InGaAs with temperature. The y axis shows the ratio between the resistivity at a temperature T and the resistivity at 300 K [135], reproduced with permission from Springer Nature.

According to Tian, resistivity behaviour is determined by which mechanism dominates between scattering and ionisation. The change in resistivity at low temperature (range I) is determined by the ionisation of shallow donor impurity levels and the scattering of ionised impurities. For the second trend (regions II and III), the change in resistivity is affected by polar optical phonon scattering. In the last regions (IV and V), resistivity changes due to the ionisation of the deep defect levels and polar optical phonon scattering [135].

In this thesis, the trap-dependent effect observed with increasing temperature was also observed optically at low temperatures, where increasing laser power led to a reduction in photocurrent. In Fig 4-23, the detector's photocurrent, normalised over the dark current for better data visualisation, is plotted at a wavelength of 1550 nm as the laser power increases from 0% to 20%. This is done for different temperatures, specified in the legend.

This observed effect is wavelength dependant, as a higher wavelength is associated with a lower photon energy and a lower absorption in InGaAs. In Fig 4-24, the temperature has been fixed at 30 K and the normalised photocurrent has been plotted over the laser power, which has been varied from 0% to 20%. Since illumination was applied from the top, the wavelength response from the grating coupler can be disregarded. This allows for a focused study of wavelengths ranging from 1250 nm to 1700 nm, with the specific wavelength values detailed in the plot legend.

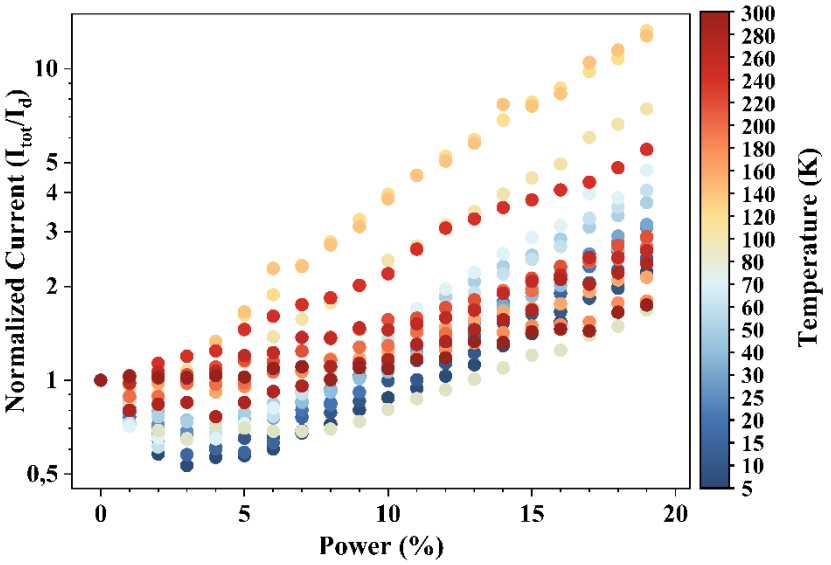


Fig 4-23. Normalised current values over the dark current for a power sweep (0% - 20%) at a 1550 nm wavelength for temperatures ranging from 5 K to 300 K, specified in the legend.

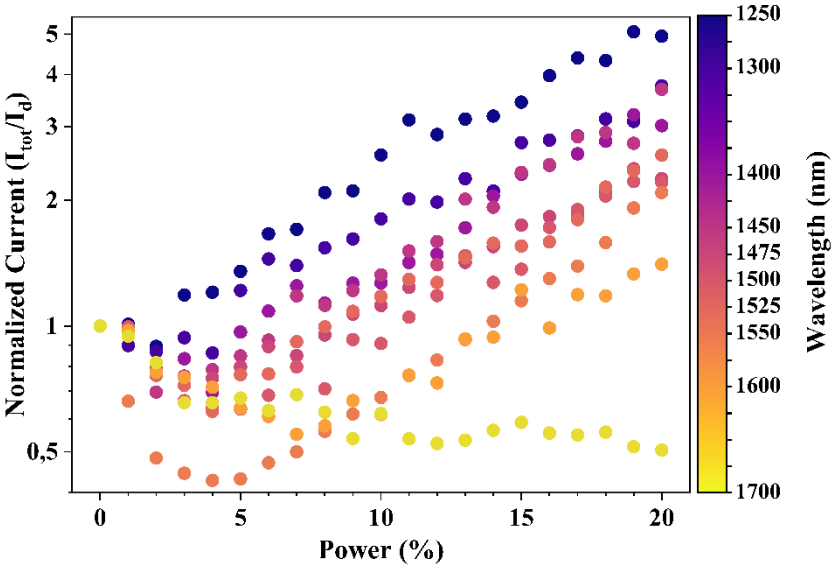


Fig 4-24. Normalised current values over the dark current for a power sweep (0% - 20%) at 30 K for wavelengths ranging from 1250 nm to 1700 nm, specified in the legend.

The observed optical behaviour in Fig 4-23 and Fig 4-24 has been accepted onto the 70th Annual IEEE International Electron Devices Meeting (IEDM2024). A more detailed theoretical study of this phenomenon is required for a thorough explanation of the observed behaviour, which falls beyond the scope of this thesis. This topic will be the focus of a future publication.

In this section, individual devices were optically characterised. First, free-space illumination was used to confirm their functionality. As a step towards integrating the photodetectors into an optical link, new devices were tested with light coupled through a waveguide. Despite the inclusion of various mirrors for back reflection in the designs, the variability in electrical performance between devices made it difficult to compare their impact. Responsivity values were calculated for both types of illumination, resulting in $\rho_{\text{free space}} = 0.048$ A/W and $\rho_{\text{waveguide coupled}} = 0.018$ A/W.

Additionally, waveguide-coupled devices were studied at low temperatures. Initial results from a 100 nm wide device confirmed the expected behaviour of reduced dark current at lower temperatures, enabling the calculation of activation energy across different reverse bias values, with results ranging from 12 meV to 48 meV. However, subsequent measurements on a 300 nm wide device, down to 5 K, showed an unexpected increase in dark current below 200 K. This anomalous behaviour is likely attributable to defects within the device, which will require further investigation to fully understand their origin.

5. Summary and Outlook

This thesis investigated the integration of III-V nanowire photodetectors onto silicon substrates for Photonic Integrated Circuits (PICs) using Template-Assisted Selective Epitaxy (TASE). By combining the benefits of III-V semiconductor materials with silicon photonic platforms, this research aims to advance optical communication and sensing technologies, particularly by reducing power consumption through efficient optical interconnects.

Earlier studies demonstrated TASE-fabricated photodetectors, but challenges such as the thinness of 60 nm devices, which were unsuitable for supporting propagating modes, and the lack of reproducibility in 220 nm thick waveguide-coupled devices highlighted the need for further investigation. This thesis provided a statistical analysis of these 220 nm p-InP/i-InGaAs/n-InP photodetectors and their electrical performance, supported by TCAD simulations to explain device variability. The optical characterisation confirmed the functionality of the devices through both free-space illumination and waveguide coupling, moving closer to their integration into a complete optical link. Low-temperature measurements of individual devices were performed to explore their potential for applications in quantum technologies.

The research began with the simulation of III-V photodetectors using Sentaurus TCAD. The first study performed on the III-V materials of interest in this study identified the heterostructure (n-InP/i-InGaAs/p-InP) as the most effective for optimising optical performance compared to simpler heterostructures like pure InP or InGaAs, as shown in Fig 5-1a.

A subsequent study was performed on the role of mid-bandap traps, which emphasised their impact on device ideality. As demonstrated in Fig 5-1b, the presence of these traps caused deviations in both the on and off currents, disrupting the linearity of the diode's response. This deviation was attributed to generation-recombination effects, which degrade device performance.

Furthermore, the simulations provided crucial insights into the electrical behaviour of the fabricated devices, which exhibited considerable variability in current-voltage (I-V) characteristics.

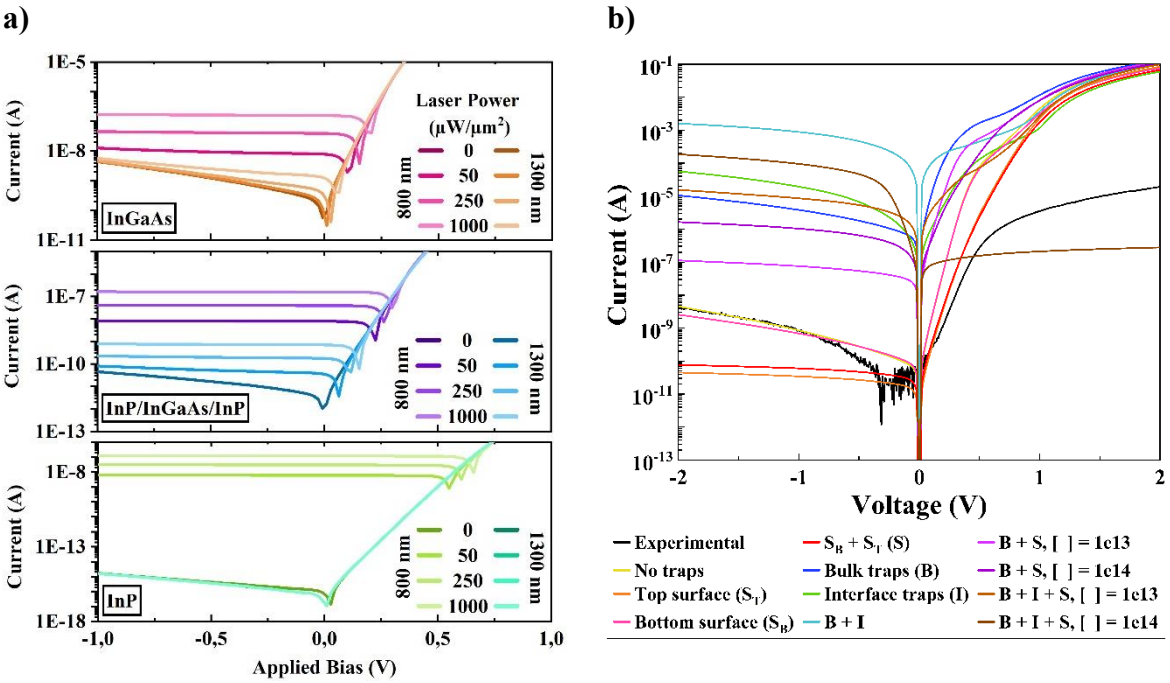


Fig 5-1. a) Simulated I-V curves at four different laser powers and two different wavelengths for the three studied structures (InGaAs and InP homojunctions and InP/InGaAs/InP heterostructure). b) I-V curves from experimental (black) and simulated devices with many different locations of traps, specified in the legend.

Following the simulation phase, a detailed step-by-step explanation was provided on how to achieve fully functional III-V photodetectors using TASE. The fabrication of photodetectors focused on refining material growth and doping techniques. An additional study was conducted on doping diffusion, optimising the Zn p-doping in the final devices. The results of optimisation and the EDX images of fully grown NWs with different widths can be seen in Fig 5-2 a) – b) and c) – d), respectively.

Moreover, the fabrication of funnel-shaped devices was optimised through a two-step growth method, marking the first demonstration of a double growth technique on TASE structures. This approach aims to enhance overall device performance, though further studies are necessary to fully characterise and optimise these devices. The EDX image of a fully grown funnel-shape structure can be seen in Fig 5-2e.

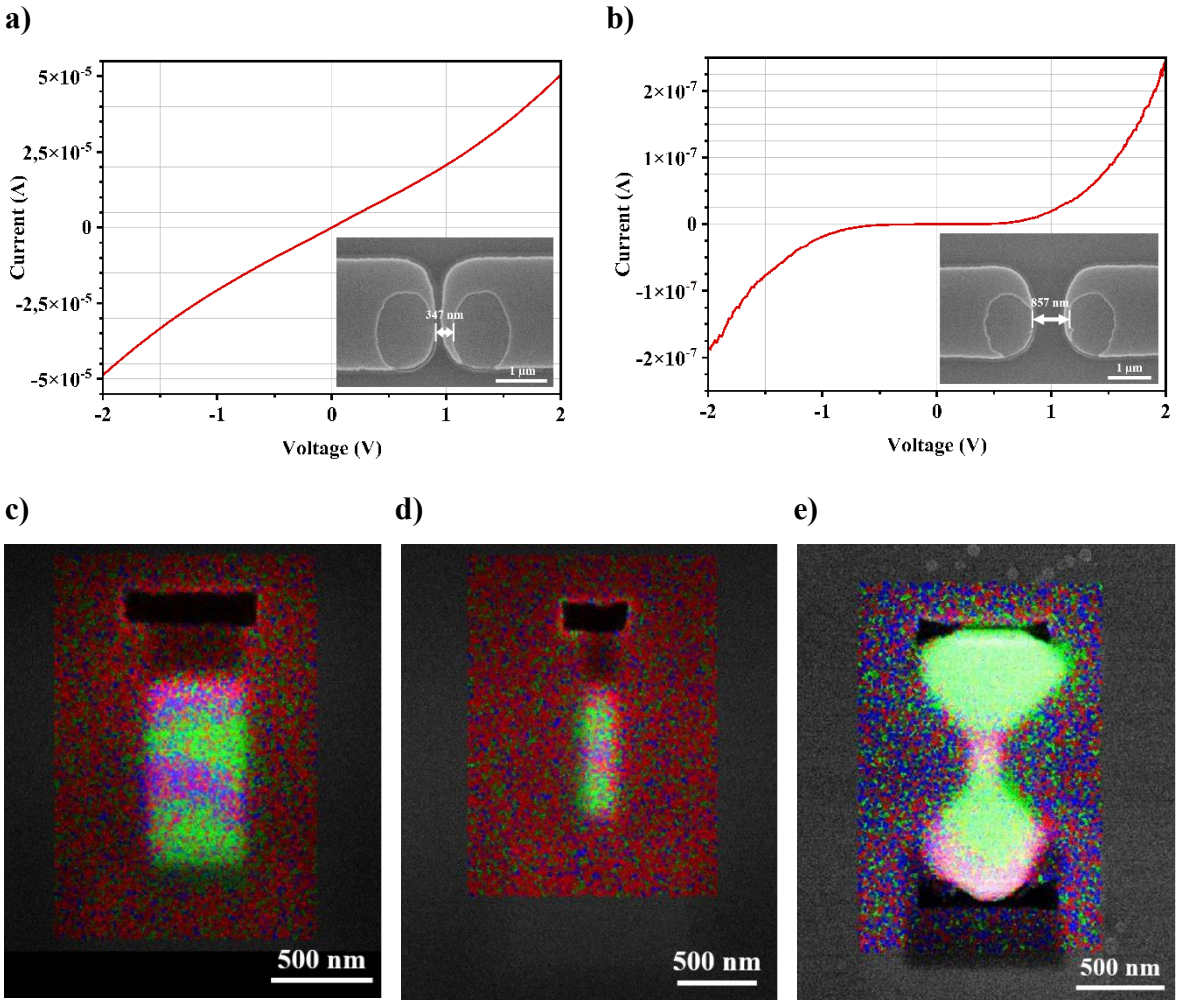


Fig 5-2. a) and b) I-V curves of two pairs of contacted holes with their respective SEM images for the study of Zn doping diffusion. c) – e) EDX of the sequence growth for c) – d) two straight nanowires with different widths and e) a funnel-shaped device. Phosphorus is indicated in green, representing the InP regions, arsenic in red, and gallium in blue, with the red and blue areas collectively representing InGaAs

Electrical characterisation of the fabricated devices revealed significant variability in their I-V curves, which simulations attributed to the positioning of the InGaAs region inside the nanowire relative to the metal contacts, which is a consequence of the crystallographic orientation of the silicon substrate.

The findings highlighted the importance of meticulous control over fabrication processes and careful substrate selection to achieve consistent and reliable device performance. Some coloured SEM images of fabricated devices with the same width but different length and growth fronts, and their I-V characteristics highlighted in the plot with the dark current of some selected fabricated devices are shown in Fig 5-3.

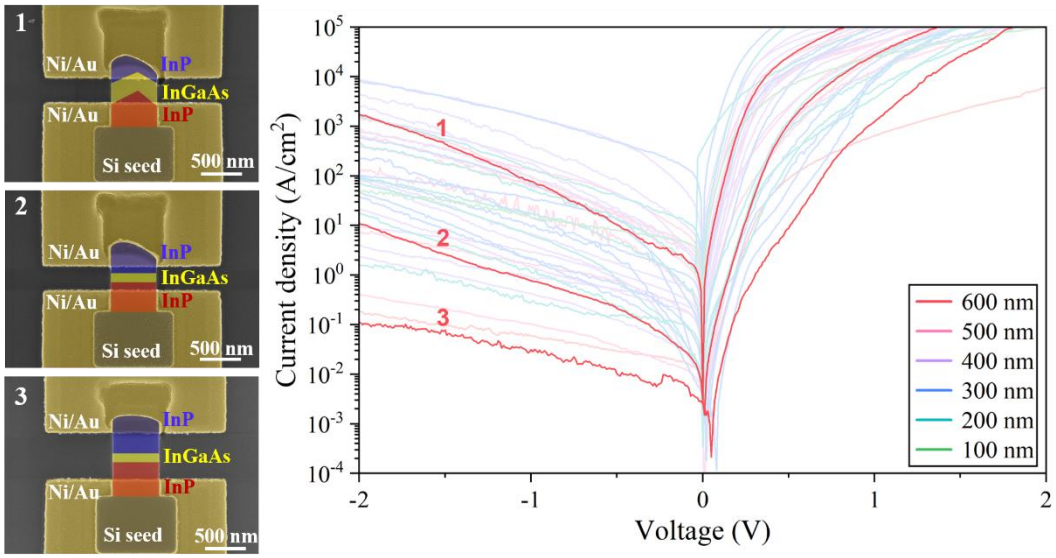


Fig 5-3. On the left are the coloured top-view SEM images. The colours indicate the position of the junction at the top of the device, which may be tilted towards the substrate and thus not be visible in a top-view EDX. On the right are the highlighted respective I-V curves of the devices shown in the SEM images on the left [125] reproduced with permission © 2024 IEEE.

The high variability in the I-V characteristics of the devices fabricated on a (001) SOI substrate led to the fabrication of devices on a (110) SOI substrate, despite its lower quality. The results, as shown in Fig 5-4a, revealed that the I-V characteristics of the devices grown on the (110) substrate outperformed those grown on the (001) substrate. The successful fabrication of these devices, which exhibited atomically smooth interfaces and straight growth fronts as shown in Fig 5-4b, represents the first demonstration of III-V photodetectors integrated by TASE on a (110) SOI platform.

The study concluded that further improvements are required to reduce the variability in the electrical performance of the devices. Although using (110) SOI substrates for CMOS Si devices is feasible, as there is no significant difference in electronics compared to (001) SOI, the shift would only be convincing if a fully functional, high-performance optical link is demonstrated.

Two potential approaches were proposed to improve the performance of devices grown on (110) SOI. The first involves using funnel-shaped devices, which could help keep the InGaAs region more centred within the devices and farther from the contacts, thus reducing performance variability. However, this approach adds complexity to the fabrication process. The second approach involves increasing the length of the InP regions to ensure the InGaAs region remains distant from the contacts. This, however, introduces the risk of increased device capacitance, which may negatively impact high-speed performance.

Further research is required to balance performance improvements, variability reduction, and maintaining high-speed functionality in order to achieve fully operational optical links for on-chip communication.

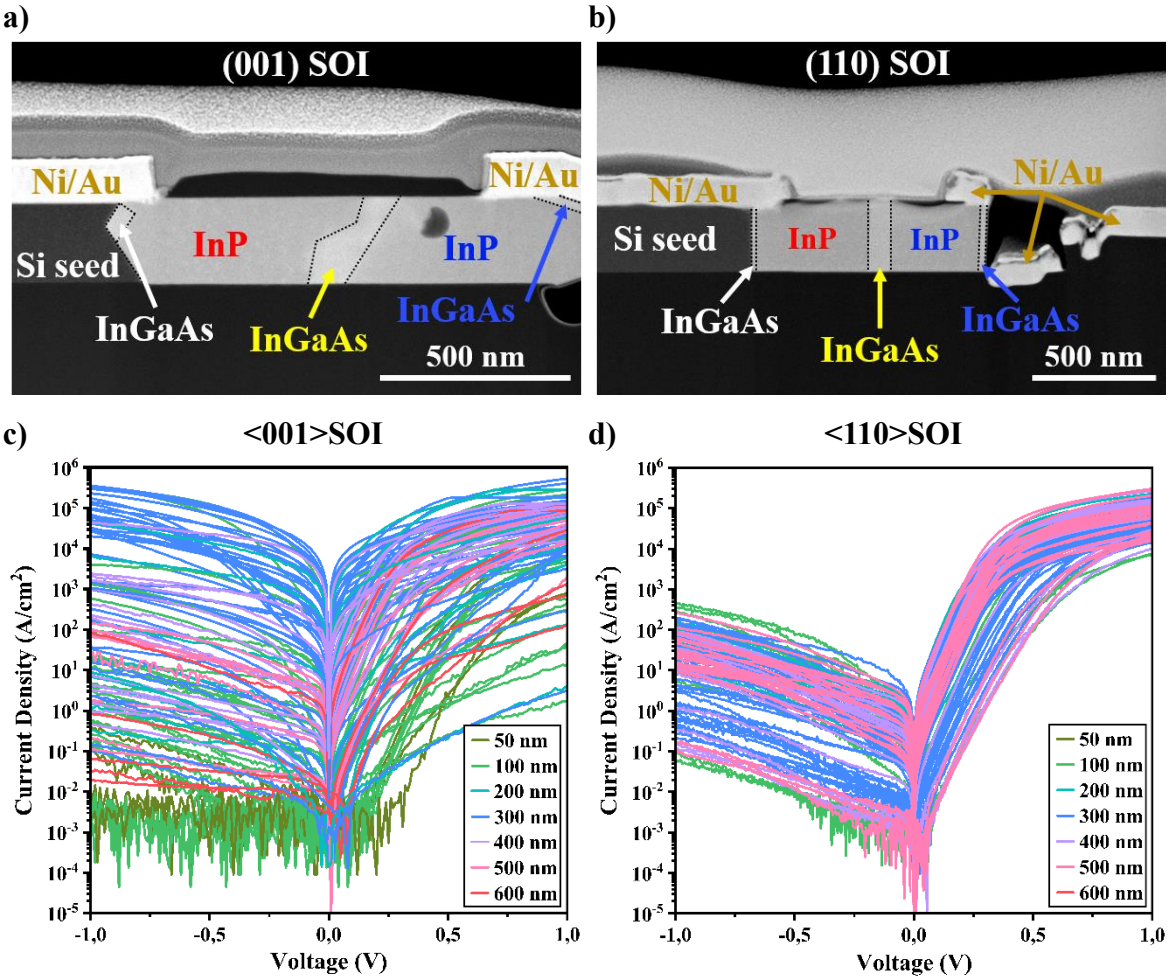


Fig 5-4. a) - b) TEM images of the cross section of fabricated devices and c) - d) I-V characteristics of 100 devices, grown a) and c) on a (001) SOI platform, and b) and d) on a (110) SOI platform. The colours of the I-V curves correspond to the width of the devices.

The optical characterisation initially confirmed the functionality of the fabricated photodetectors through free-space illumination. Subsequent efforts aimed at integrating these devices into full optical links by testing new devices via waveguide coupling. However, due to the high electrical variability, the study did not reach definitive conclusions regarding the impact of tapered waveguides and mirrors for back-reflection.

Responsivity values were calculated for both the free-space and waveguide coupling mechanisms based on the photoinduced characteristics shown in Fig 5-5 b and d respectively. The obtained values are $\rho_{\text{free space}} = 0.048$ A/W and $\rho_{\text{waveguide coupled}} = 0.018$ A/W. A selection of the I-V curves of devices illuminated from the top and through a waveguide can be seen in Fig 5-5 a) – b) and c) – d), respectively.

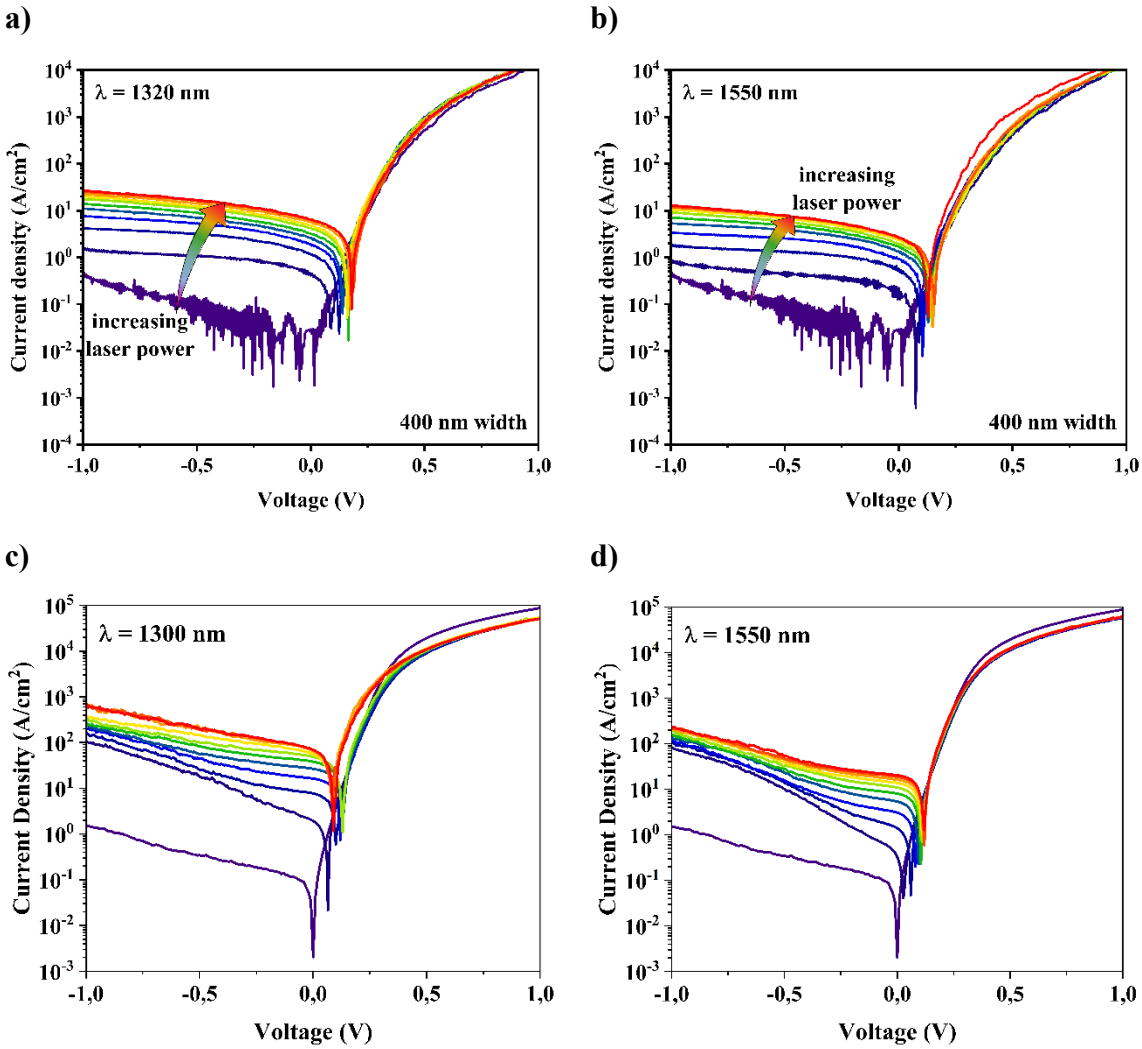


Fig 5-5. a) – b) Photoinduced I-V characteristics at room temperature for free-space illuminated 400 nm wide device for increasing laser powers at a) λ = 1350 nm (up to ~1.97 μW) and b) λ = 1550 nm (up to ~1.76 μW). c) – d) Photoinduced I-V characteristics at room temperature for a straight waveguide coupled 100 nm wide device without back-reflection for increasing laser powers at c) λ = 1300 nm and d) λ = 1550 nm.

The focus shifted to exploring device performance at low temperatures. Initial findings from a 100 nm wide device demonstrated a reduction in dark current as temperatures were decreased, as would be expected. These results allowed for the calculation of activation energy at various reverse bias values, represented in the Arrhenius plot shown in Fig 5-6a, with results between 12 meV and 48 meV.

In contrast, subsequent measurements on a 300 nm wide device, performed down to 5 K, exhibited an unexpected increase in dark current as the temperature dropped below 200 K, as shown in Fig 5-6 b. This optical anomaly was further investigated, leading to the results presented in Fig 5-6 c) – d). It was found that the current reduction in response to increased optical power was both temperature and wavelength dependent. This phenomenon is likely attributed to defects within the device and requires further investigation to understand their origin, which will be the subject of future works.

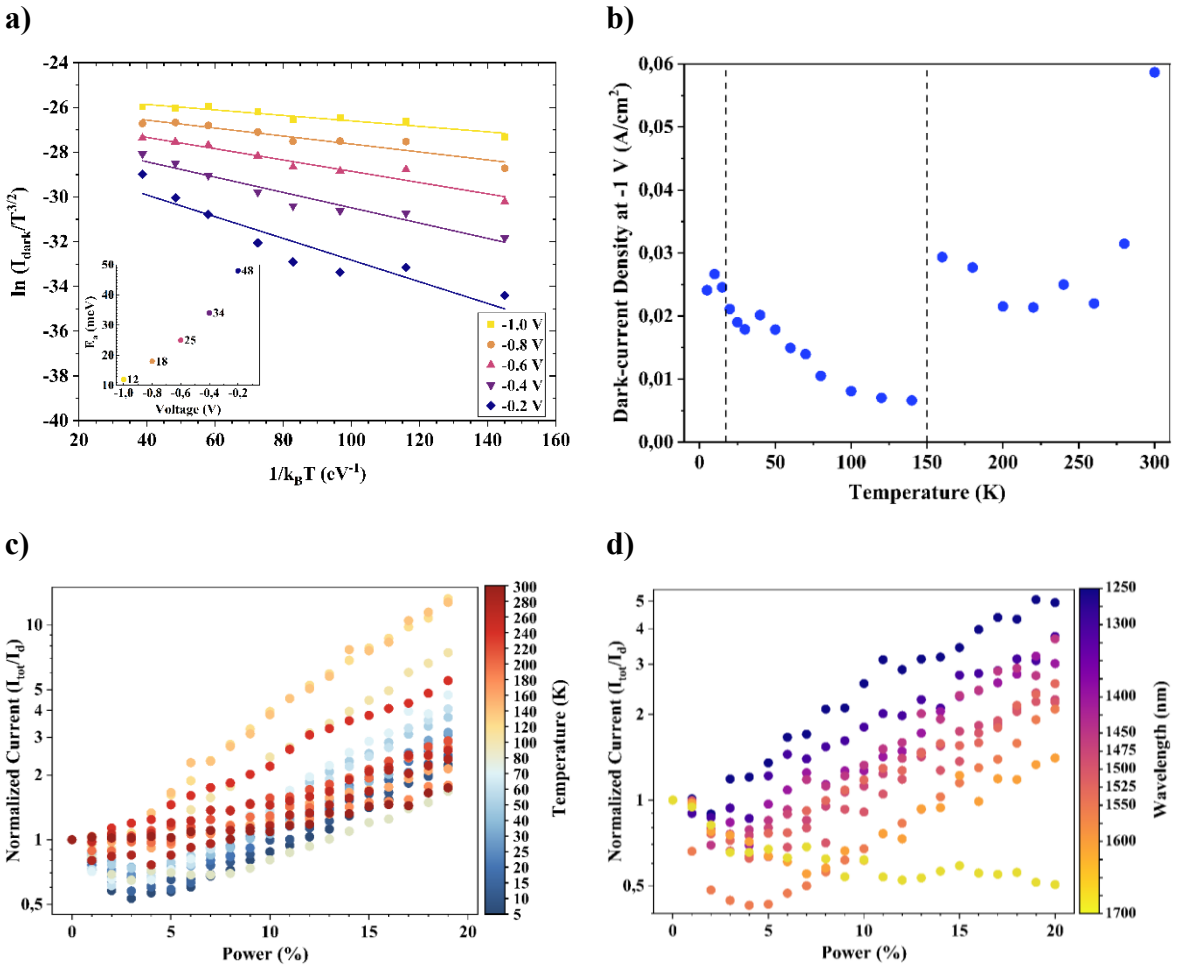


Fig 5-6. a) Arrhenius plot for the 100 nm wide devices. The different curves correspond to the current values extracted at different reverse voltages. The temperatures range from 80 K to 300 K. The inset displays the activation energy versus the voltage, extracted from the slope of fitting the data. b) Dark-current density at -1 V of applied voltage with respect to the temperature for a 300 nm wide device. The vertical lines group the measurements performed on different days. c) - d) Normalised current values over the dark current for a power sweep (0% - 20%) c) at a 1550 nm wavelength for temperatures ranging from 5 K to 300 K, and d) at 30 K for wavelengths ranging from 1250 nm to 1700 nm, specified in the legend.

5.1. Future directions

During this thesis several sample types were fabricated: single straight NWs on a (001) SOI, waveguide coupled straight devices on both (001) SOI and (110) SOI, and funnel-shaped devices on a (001) SOI. The complex fabrication process for funnel-shaped devices, requiring a double growth technique, highlighted the need for further optimisation. Enhancing these devices and performing their optical and electrical characterisation would enrich this work and provide deeper insights into the potential of TASE and III-V photodetectors for on-chip communications, which could be the topic of future research.

Although some devices were fabricated onto a (110) SOI wafer, these devices faced challenges due to inferior material quality from a thicker top silicon layer, which needed etched down resulting in further damage to the wafer's surface. Future work should focus on using high-quality (110) SOI wafers with the desired silicon thickness to eliminate this step and enhance the reproducibility and reliability of the photodetectors.

A second area of potential research could be focused in optimising the performance of the photodetectors, after this thesis provide with insights into the source of the variability between devices. This could encompass both the funnel-shape devices and the longer straight devices, trying to keep the InGaAs region centred and far from the contacts.

With improved device reproducibility, a renewed focus on optical characterisation is essential as a future research topic. This includes comparing straight and tapered waveguides and evaluating different back-scattering mirrors to determine the most effective designs for optical integration.

Additionally, further investigation into the observed phenomena of the optical power at cryogenic temperatures could provide valuable insights into the defects of the devices. This is already a topic of research that has continued after the work in this thesis.

Finally, integrating these devices into full optical link would be essential steps toward advancing their practical applications in optical communications and sensing technologies. This includes the fabrication of a III-V-based laser for the opposite end of the waveguide and conducting comprehensive system-level testing to assess the performance and practical feasibility of the optical link.

By addressing these future research directions, significant advancements can be made in integrating III-V photodetectors into silicon-based PICs, contributing to the enhancement of optical communication and sensing technologies and supporting the development of quantum technologies.

6. Bibliography

[1] D. A. B. Miller, “Attojoule Optoelectronics for Low-Energy Information Processing and Communications,” *Journal of Lightwave Technology,* vol. 35, no. 3, pp. 346-396, 2017. DOI: 10.1109/JLT.2017.2647779.

[2] P. Delforge and J. Whitney, “Data Center Efficiency Assessment - Scaling Up Energy Efficiency Across the Data Center Industry: Evaluating Key Drivers and Barriers.,” *Natural Resources Defense Council (NRDC) and Anthesis,* no. Issue Paper #IP:14-08-A., August 2014.

[3] J. D. Meindl, “Beyond Moore's Law: the interconnect era,” *Computing in Science & Engineering,* vol. 5, no. 1, pp. 20-24, 2003. DOI: 10.1109/MCISE.2003.1166548.

[4] M. M. Waldrop, “The chips are down for Moore's law,” *Nature,* vol. 530, no. 7589, pp. 144-147, 2016. DOI: 10.1038/530144a.

[5] Y. Han, H. Park, J. Bowers and K. Lau, “Recent advances in light sources on silicon,” *Advances in Optics and Photonics,* vol. 14, p. 404–454, 2022, DOI: 10.1364/AOP.455976.

[6] J. Mulcahy, F. H. Peters and X. Dai, “Modulators in Silicon Photonics—Heterogenous Integration & and Beyond,” *Photonics,* vol. 9, no. 1, p. 40, 2022, DOI: 10.3390/photonics9010040.

[7] G. Chen, Y. Yu, Y. Shi, N. Li, W. Luo, L. Cao, A. J. Danner, A. Q. Liu and X. Zhang, “High-Speed Photodetectors on Silicon Photonics Platform for Optical Interconnect,” *Laser & Photonics Reviews,* vol. 16, no. 12, 2022, DOI: 10.1002/lpor.202200117.

[8] P. D. Dobbelaere, S. Abdalla, S. Gloeckner, M. Mack, G. Masini, A. Mekis, T. Pinguet, S. Sahni, D. Guckenberger, M. Harrison and A. Narasimha, “Si Photonics Based High-Speed Optical Transceivers,” in *European Conference and Exhibition on Optical Communication*, 2012. DOI: 10.1364/ECEOC.2012.We.1.E.5.

[9] K. Asakawa, Y. Sugimoto and S. Nakamura, “Silicon photonics for telecom and data-com applications,” *Opto-Electronic Advances,* vol. 3, no. 10, p. 200011 , 2020. DOI: 10.29026/oea.2020.200011.

[10] C.-Z. Ning, “Semiconductor nanolasers and the size-energy-efficiency challenge: a review,” *Advanced Photonics,* vol. 1, no. 1, 2019. DOI: 10.1117/1.ap.1.1.014002.

[11] S. Lischke, A. Peczek, J. S. Morgan, K. Sun, D. Steckler, Y. Yamamoto, F. Korndörfer, C. Mai, S. Marschmeyer, M. Fraschke, A. Krüger, A. Beling and L. Zimmermann, “Ultra-fast germanium photodiode with 3-dB bandwidth of 265 GHz,” *Nature Photonics,* vol. 15, p. 925–931, 2021, DOI: 10.1038/s41566-021-00893-w .

[12] X. Hu, D. Wu, D. Chen, L. Wang, X. Xiao and S. Yu, “180 Gbit/s Si3N4 -waveguide coupled germanium photodetector with improved quantum efficiency,” *Optics Letters,* vol. 46, no. 24, pp. 6019-6022, 2021, DOI: 10.1364/OL.438962.

[13] T. Hu, B. Dong, X. Luo, T.-Y. Liow, J. Song, C. Lee and G.-Q. Lo, “Silicon photonic platforms for mid-infrared applications,” *Photonics Research,* vol. 5, no. 5, pp. 417-430, 2017, DOI: 10.1364/PRJ.5.000417.

[14] K. Kim and Y. Park, “Future photonics convergence on Si,” in *The 9th International Conference on Group IV Photonics (GFP)*, San Diego, CA, USA, 2012, DOI: 10.1109/GROUP4.2012.6324066.

[15] D. Liang, A. Roshan-Zamir, Y.-H. Fan, C. Zhang, B. Wang, A. Descos, W. Shen, K. Yu, C. Li, G. Fan, G. Kurczveil, Y. Hu, Z. Huang, M. Fiorentino, S. Kumar, S. M. Palermo and R. G. Beausoleil, “Fully-Integrated Heterogeneous DML Transmitters for High-Performance Computing,” *Journal of Lightwave Technology,* vol. 38, p. 3322–3337, 2022, DOI:10.1109/JLT.2019.2959048.

[16] J. Michel, J. Liu and L. Kimerling, “High-performance Ge-on-Si photodetectors,” *Nature Photonics,* vol. 4, no. 8, p. 527–534, 2010. DOI: 10.1038/nphoton.2010.157.

[17] H. Tran, T. Pham, J. Margetis, Y. Zhou, W. Dou, P. C. Grant, J. M. Grant, S. Al-Kabi, G. Sun, R. A. Soref, J. Tolle, Y.-H. Zhang, W. Du, B. Li, M. Mortazavi and S.-Q. Yu, “Si-Based GeSn Photodetectors toward Mid-Infrared Imaging Applications,” *ACS Photonics ,* vol. 6, no. 11, pp. 2807-2815, 2019. DOI: 10.1021/acsphotonics.9b00845.

[18] A. K. Sood, J. W. Zeller, R. A. Richwine, Y. R. Puri, H. Efstathiadis, P. Haldar, N. K. Dhar and D. L. Polla, “SiGe Based Visible-NIR Photodetector Technology for Optoelectronic Applications,” in *Advances in Optical Fiber Technology: Fundamental Optical Phenomena and Applications*, InTech, 2015. DOI: 10.5772/59065.

[19] M. Malik, M. A. Iqbal, J. R. Choi and P. V. Pham, “2D Materials for Efficient Photodetection: Overview, Mechanisms, Performance and UV-IR Range Applications,” *Frontiers in Chemistry,* vol. 10, p. 905404, 2022. DOI: 10.3389/fchem.2022.905404.

[20] A. Rani, A. Verma and B. C. Yadav, “Advancements in transition metal dichalcogenides (TMDCs) for self-powered photodetectors: challenges, properties, and functionalization strategies,” *Materials Advances,* vol. 5, no. 9, pp. 3535-3562, 2024. DOI: 10.1039/d3ma01152f.

[21] L.-H. Zeng, S.-H. Lin, Z.-J. Li, Z.-X. Zhang, T.-F. Zhang, C. Xie, C.-H. Mak, Y. Chai, S. P. Lau, L.-B. Luo and Y. H. Tsang, “Fast, Self-Driven, Air-Stable, and Broadband Photodetector Based on Vertically Aligned PtSe2/GaAs Heterojunction,” *Advanced Functional Materials,* vol. 28, no. 16, p. 1705970, 2018. DOI: 10.1002/adfm.201705970.

[22] S. Mirzakuchaki and A. Nazary, “Chapter Four - 2D III-V semiconductors,” in *Semiconductors and Semimetals*, vol. 113, I. H. Abidi, Ed., Elsevier, 2023, pp. 101-144. DOI: 10.1016/bs.semsem.2023.10.004.

[23] Z. Wang, Y. Gu, X. Li, Y. Liu, F. Liu and W. Wu, “Recent Progress of Quantum Dot Infrared Photodetectors,” *Advanced Optical Materials,* vol. 11, no. 19, p. 2300970, 2023. DOI: 10.1002/adom.202300970.

[24] H. Wu and Z. Ning, “Tutorial: Lead sulfide colloidal quantum dot infrared photodetector,” *Journal of Applied Physics,* vol. 133, no. 4, p. 041101, 2023. DOI: 10.1063/5.0133809.

[25] W. K. Bae, J. Joo, L. A. Padilha, J. Won, D. C. Lee, Q. Lin, W.-k. Koh, H. Luo, V. I. Klimov and J. M. Pietryga, "Highly Effective Surface Passivation of PbSe Quantum Dots through Reaction with Molecular Chlorine," *Journal of the American Chemical Society,* vol. 134, no. 49, pp. 20160-20168, 2012. DOI: 10.1021/ja309783v.

[26] K. Chang and W.-K. Lou, "Helical Quantum States in HgTe Quantum Dots with Inverted Band Structures," *Physical Review Letters,* vol. 106, no. 20, p. 206802, 2011. DOI: 10.1103/PhysRevLett.106.206802.

[27] M. K. Jana, P. Chithaiah, B. Murali, S. B. Krupanidhi, K. Biswasa and C. N. R. Rao, "Near infrared detectors based on HgSe and HgCdSe quantum dots generated at the liquid–liquid interface," *Journal of Materials Chemistry C,* vol. 1, no. 39, pp. 6184-6187, 2013. DOI: 10.1039/C3TC31344A.

[28] C. Zhao, C. Chen, R. Wei, Y. Zou, W. Kong, T. Huang, Z. Yu, J. Yang, F. Li, Y. Han, C. Guo and W. Yu, "Laser-Assisted Synthesis of Ag2S-Quantum-Dot-in-Perovskite Matrix and Its Application in Broadband Photodetectors," *Advanced Optical Materials,* vol. 10, no. 1, p. 2101535, 2022. DOI: 10.1002/adom.202101535.

[29] S. B. Hafiz, M. R. Scimeca, P. Zhao, I. J. Paredes, A. Sahu and D.-K. Ko, "Silver Selenide Colloidal Quantum Dots for Mid-Wavelength Infrared Photodetection," *ACS Applied Nano Materials ,* vol. 2, no. 3, pp. 1631-1636, 2019. DOI: 10.1021/acsanm.9b00069.

[30] T. Kim, D. Shin, M. Kim, H. Kim, E. Cho, M. Choi, J. Kim, E. Jang and S. Jeong, "Development of Group III–V Colloidal Quantum Dots for Optoelectronic Applications," *ACS Energy Letters,* vol. 8, no. 1, pp. 447-456, 2023. DOI: 10.1021/acsenergylett.2c02489.

[31] Y. Dong, C. Chen, X. Zheng, L. Gao, Z. Cui, H. Yang, C. Guo, Y. Chi and C. M. Li, "One-step and high yield simultaneous preparation of single- and multi-layer graphene quantum dots from CX-72 carbon black," *Journal of Materials Chemistry,* vol. 22, no. 18, pp. 8764-8766, 2012. DOI: 10.1039/C2JM30658A.

[32] A. Ahmadivand, M. Karabiyik and N. Pala, "6 - Plasmonic photodetectors," in *Photodetectors. Materials, Devices and Application*, B. Nabet, Ed., Woodhead Publishing, 2016 , pp. 157-193. DOI: 10.1016/B978-1-78242-445-1.00006-3.

[33] A. Ren, L. Yuan, H. Xu, J. Wu and Z. Wang, “Recent progress of III–V quantum dot infrared photodetectors on silicon,” *Journal of Materials Chemistry C,* vol. 7, pp. 14441-14453, 2019, DOI: 10.1039/C9TC05738B.

[34] K. Sun and A. Beling, “High-Speed Photodetectors for Microwave Photonics,” *Applied Sciences,* vol. 9, no. 4, p. 623, 2019, DOI: 10.3390/app9040623.

[35] S. Chen, W. Li, J. Wu, Q. Jiang, M. Tang, S. Shutts, S. N. Elliott, A. Sobiesierski, A. J. Seeds, I. Ross, P. M. Smowton and H. Liu, “Electrically pumped continuous-wave III-V quantum dot lasers on silicon,” *Nature Photonics,* vol. 10, p. 307–311, 2016, DOI: 10.1038/nphoton.2016.21 .

[36] S. Mauthe, N. V. Triviño, Y. Baumgartner, M. Sousa, D. Caimi, T. Stöferle, H. Schmid and K. E. Moselund, “InP-on-Si optically pumped microdisk lasers via monolithic growth and wafer bonding,” *IEEE Journal of Selected Topics in Quantum Electronics,* vol. 25, no. 6, pp. 1-7, 2019, DOI: 10.1109/JSTQE.2019.2915924.

[37] R. Chen, K. W. Ng, W. S. Ko, D. Parekh, F. Lu, T.-T. D. Tran, K. Li and C. Chang-Hasnain, “Nanophotonic integrated circuits from nanoresonators grown on silicon,” *Nature Communications,* vol. 5, no. 4325, 2014. DOI: 10.1038/ncomms5325.

[38] N. Li, K. Han, W. Spratt, S. Bedell, J. Ott, M. Hopstaken, F. Libsch, Q. Li and D. Sadana, “Ultra-low-power sub-photon-voltage high-efficiency light-emitting diodes,” *Nature Photonics,* vol. 13, p. 588–592, 2019, DOI: 10.1038/s41566-019-0463-x.

[39] G. Roelkens, L. Liu, D. Liang, R. Jones, A. Fang, B. Koch and J. Bowers, “III-V/silicon photonics for on-chip and intra-chip optical interconnects,” *Laser and Photonics Reviews,* vol. 4, no. 6, p. 751–779, 2010, DOI: 10.1002/lpor.200900033.

[40] J. M. Ramirez, H. Elfaiki, T. Verolet, C. Besancon, A. Gallet, D. Néel, K. Hassan, S. Olivier, C. Jany, S. Malhouitre, K. Gradkowski, P. E. Morrissey, P. O'Brien, C. Caillaud, N. Vaissière, J. Decobert, S. Lei, R. Enright, A. Shen and M. Achouche, “III-V-on-Silicon Integration: From Hybrid Devices to Heterogeneous Photonic Integrated Circuits,” *IEEE Journal of Selected Topics in Quantum Electronics,* vol. 26, no. 2, p. 1–13, 2020, DOI: 10.1109/JSTQE.2019.2939503.

[41] M. E. Levinshtein, S. L. Rumyantsev and M. S. Shur, Properties of advanced semiconductor materials: GaN, AlN, InN, BN, SiC, SiGe, John Wiley & Sons, 2001.

[42] I. Vurgaftman, J. R. Meyer and L. R. Ram-Mohan, "Band parameters for III–V compound semiconductors and their alloys," *Journal of Applied Physics,* vol. 89, pp. 5815-5875, 2001. DOI: 10.1063/1.1368156.

[43] E. Fadaly, A. Dijkstra, J. Suckert, D. Ziss, M. v. Tilburg, C. Mao, Y. Ren, V. v. Lange, K. Korzun, S. Kölling, M. Verheijen, D. Busse, C. Rödl, J. Furthmüller, F. Bechstedt, J. Stangl, J. Finley, S. Botti, J. Haverkort and E. Bakkers, "Direct-bandgap emission from hexagonal Ge and SiGe alloys," *Nature,* vol. 580, pp. 205-209, 2020. DOI: 10.1038/s41586-020-2150-y.

[44] A. Bett, F. Dimroth, G. Stollwerck and O. Sulima, "III-V compounds for solar cell applications," *Applied Physics A,* vol. 69, pp. 119-129, 1999. DOI: 10.1007/s003399900062.

[45] H. Zimmermann, Silicon Optoelectronic Integrated Circuits, vol. 3, Berlin, Heidelberg: Springer Berlin Heidelberg, 2000.

[46] B. Kunert, Y. Mols, M. Baryshniskova, N. Waldron, A. Schulze and R. Langer, "How to control defect formation in monolithic III/V hetero-epitaxy on (100) Si? A critical review on current approaches," *Semiconductor Science and Technology,* vol. 33, no. 9, 2018. DOI: 10.1088/1361-6641/aad655.

[47] J. Liu, "Photodetectors," in *Photonic Devices*, Cambridge, Cambridge Univeristy Press, 2005, pp. 926-1017. DOI: 10.1017/CBO9780511614255.015.

[48] S. Mauthe, Y. Baumgartner, M. Sousa, Q. Ding, M. D. Rossell, A. Schenk, L. Czornomaz and K. E. Moselund, "High-speed III-V nanowire photodetector monolithically integrated on Si," *Nature Communications,* vol. 11, no. 4565, 2020. DOI: 10.1038/s41467-020-18374-z.

[49] P. Tiwari, S. Mauthe, N. V. Trivino, P. Staudinger, M. Scherrer, P. Wen, D. Caimi, M. Sousa, H. Schmid, K. E. Moselund, Q. Ding and A. Schenk, "Scaled III-V optoelectronic devices on silicon," in *2020 International Conference on Numerical Simulation of Optoelectronic Devices (NUSOD)*, 2020. DOI: 10.1109/NUSOD49422.2020.9217747.

[50] P. Tiwari, S. Mauthe, N. V. Triviño, P. Staudinger, M. Sousa, Y. Baumgartner, M. Scherrer, H. Schmid and K. E. Moselund, “Monolithic III-V microdisk lasers on silicon by template-assisted selective epitaxy,” in *Proc. SPIE 11356, Semiconductor Lasers and Laser Dynamics IX, 113560B*, 2020. DOI: 10.1117/12.2561058.

[51] J. Wang, M. S. Gudiksen, X. Duan, Y. Cui and C. M. Lieber, “Highly Polarized Photoluminescence and Photodetection from Single Indium Phosphide Nanowires,” *Science,* vol. 293, no. 5534, pp. 1455-1457, 2001. DOI: 10.1126/science.1062340.

[52] X. Yan, B. Li, Y. Wu, X. Zhang and X. Ren, “A single crystalline InP nanowire photodetector,” *Applied Physics Letters,* vol. 109, no. 5, p. 053109, 2016. DOI: 10.1063/1.4960713.

[53] H. Tan, C. Fan, L. Ma, X. Zhang, P. Fan, Y. Yang, W. Hu, H. Zhou, X. Zhuang, X. Zhu and A. Pan, “Single-Crystalline InGaAs Nanowires for Room-Temperature High-Performance Near-Infrared Photodetectors,” *Nano-Micro Letters,* vol. 8, p. 29–35, 2016. DOI: 10.1007/s40820-015-0058-0.

[54] T. Pearsall, “Ga0.47In0.53As: A ternary semiconductor for photodetector applications,” *IEEE Journal of Quantum Electronics,* vol. 16, no. 7, pp. 709-720, 1980. DOI: 10.1109/JQE.1980.1070557.

[55] K. Sugii, H. Koizumi and E. Kubota, “Precision lattice parameter measurements on doped indium phosphide single crystals,” *Journal of Electronic Materials,* vol. 12, pp. 701-712, 1983. DOI: 10.1007/BF02676797.

[56] J. W. Wagner, “Preparation and Properties of Bulk In1 − x Gax As Alloys,” *Journal of The Electrochemical Society,* vol. 117, no. 9, 1970. DOI: 10.1149/1.2407767.

[57] Synopsys, Inc., Mountain View, CA, US, “Sentaurus Device User Guide,” Version U-2022.12, 2022.

[58] A. Taflove, S. C. Hagness and M. Piket-May, “9 - Computational Electromagnetics: The Finite-Difference Time-Domain Method,” in *The Electrical Engineering Handbook*, W. CHEN, Ed., Academic Press, 2005, pp. 629-670. DOI: 10.1016/B978-012170960-0/50046-3.

[59] C. Martinez-Oliver, K. E. Moselund and V. P. Georgiev, “Evaluation of material profiles for III-V nanowire photodetectors,” in *2021 International Conference on Numerical Simulation of Optoelectronic Devices (NUSOD)*, Turin, Italy, 2021. DOI: 10.1109/NUSOD52207.2021.9541533.

[60] P. Wen, P. Tiwari, S. Mauthe, H. Schmid, M. Sousa, M. Scherrer, M. Baumann, B. I. Bitachon, J. Leuthold, B. Gotsmann and K. E. Moselund, “Waveguide coupled III-V photodiodes monolithically integrated on Si,” *Nature Communications,* vol. 13, no. 909, 2022. DOI: 10.1038/s41467-022-28502-6.

[61] M. Kielar, M. Daanoune, O. François-Martin, B. Flament, O. Dhez, A. Pandey, S. Chambon, R. Clerc and L. Hirsch, “Insights into the Failure Mechanisms of Organic Photodetectors,” *Advanced Electronic Materials,* vol. 4, no. 1700526, 2018. DOI: 10.1002/aelm.201700526.

[62] M. Borg, H. Schmid, K. E. Moselund, D. Cutaia y H. Riel, «Mechanisms of template-assisted selective epitaxy of InAs nanowires on Si,» *Journal of Applied Physics,* vol. 117, nº 14, p. 144303, 2015. DOI: 10.1063/1.4916984.

[63] K. E. Moselund, D. Cutaia, H. Schmid, M. Borg, S. Sant, A. Schenk and H. Riel, “Lateral InAs/Si p-Type Tunnel FETs Integrated on Si—Part 1: Experimental Devices,” *IEEE Transactions on Electron Devices,* vol. 63, no. 11, pp. 4233-4239, 2016. DOI: 10.1109/TED.2016.2606762.

[64] N. V. Triviño, P. Staudinger, N. Bologna, H. Riel, K. Moselund and H. Schmid, “Template-assisted selective epitaxy for III-V vertical nanowires on Si tandem solar cells,” in *2019 Compound Semiconductor Week (CSW)*, Nara, Japan, 2019. DOI: 10.1109/ICIPRM.2019.8819066.

[65] S. Mauthe, P. Tiwari, M. Scherrer, D. Caimi, M. Sousa, H. Schmid, K. E. Moselund and N. Vico Triviño, “Hybrid III–V Silicon Photonic Crystal Cavity Emitting at Telecom Wavelengths,” *Nano Letters,* vol. 20, no. 12, pp. 8768-8772, 2020. DOI: 10.1021/acs.nanolett.0c03634.

[66] T. Nishinaga, Handbook of Crystal Growth, 2nd ed., vol. 3, Elsevier, 2015.

[67] Q. Li and K. M. Lau, “Epitaxial growth of highly mismatched III-V materials on (001) silicon for electronics and optoelectronics,” *Progress in Crystal Growth and Characterization of Materials,* vol. 63, no. 4, pp. 105-120, 2017, DOI: 10.1016/j.pcrysgrow.2017.10.001.

[68] P. Y. Yu and M. Cardona, Fundamentals of Semiconductors, Berlin, Heidelberg: Springer Berlin Heidelberg, 2010.

[69] Y. Du, B. Xu, G. Wang, Y. Miao, B. Li, Z. Kong, Y. Dong, W. Wang and H. Radamson, “Review of Highly Mismatched III-V Heteroepitaxy Growth on (001) Silicon,” *Nanomaterials,* vol. 12, no. 741, 2022. DOI: 10.3390/nano12050741.

[70] Creative Commons Attribution 4.0 International license, [En línea]. Available: https://creativecommons.org/licenses/by/4.0/. [Último acceso: July 2024].

[71] A. Pan, W. Zhou, E. Leong, R. Li, A. Chin and B. Zou, “Continuous alloy-composition spatial grading and superbroad wavelength-tunable nanowire lasers on a single chip,” *Nano Letters,* vol. 9, no. 2, p. 784–788, 2009. DOI: 10.1021/nl803456k.

[72] T. Katsuhiro, Y. Masatoshi and F. Takashi, “A III-V nanowire channel on silicon for high-performance vertical transistors,” *Nature,* vol. 488, no. 7410, p. 189–192, 2012. DOI: 10.1038/nature11293.

[73] M. Wang, G. Yue, Y. Lin, X. Wen, D. Peng and Z. Geng, “Synthesis, optical properties and photovoltaic application of the SnS quasi-one-dimensional nanostructures,” *Nano-Micro Letters,* vol. 5, no. 1, pp. 1-6, 2013. DOI: 10.3786/nml.v5i1.p1-6.

[74] J. Miao, W. Hu, N. Guo, Z. Lu, X. Zou, L. Liao, S. Shi, P. Chen, Z. Fan, J. C. Ho, T.-X. Li, X. S. Chen and W. Lu, “Single InAs Nanowire Room-Temperature Near-Infrared Photodetectors,” *ACS Nano,* vol. 8, no. 4, p. 3628–3635, 2014. DOI: 10.1021/nn500201g.

[75] X. Dai, S. Zhang, Z. Wang, G. Adamo, H. Liu, Y. Huang, C. Couteau and a. C. Soci, “GaAs/AlGaAs Nanowire Photodetector,” *Nano Letters,* vol. 14, no. 5, p. 2688–2693, 2014. DOI: 10.1021/nl5006004.

[76] A. C. Farrell, P. Senanayake, X. Meng, N. Y. Hsieh and D. L. Huffaker, “Diode Characteristics Approaching Bulk Limits in GaAs Nanowire Array Photodetectors,” *Nano Letters,* vol. 17, no. 4, p. 2420–2425, 2017. DOI: 10.1021/acs.nanolett.7b00024.

[77] A. Brenneis, J. Overbeck, J. Treu, S. Hertenberger, S. Morkötter, M. Döblinger, J. J. Finley, G. Abstreiter, G. Koblmüller and A. W. Holleitner, “Photocurrents in a Single InAs Nanowire/Silicon Heterojunction,” *ACS Nano,* vol. 9, no. 10, p. 9849–9858, 2015. DOI: 10.1021/acsnano.5b03017.

[78] I. E. Zadeh, A. W. Elshaari, K. D. Jöns, A. Fognini, D. Dalacu, P. J. Poole, M. E. Reimer and V. Zwiller, “Deterministic Integration of Single Photon Sources in Silicon Based Photonic Circuits,” *Nano Letters,* vol. 16, no. 4, pp. 2289-2294, 2016. DOI: 10.1021/acs.nanolett.5b04709.

[79] S. Kanazawa, T. Fujisawa, K. Takahata, T. Ito, Y. Ueda, W. Kobayashi, H. Ishii and H. Sanjoh, “Flip-Chip Interconnection Lumped-Electrode EADFB Laser for 100-Gb/s/λ Transmitter,” *IEEE Photonics Technology Letters,* vol. 27, p. 1699–1701, 2015, DOI: 10.1109/LPT.2015.2438076.

[80] G. Chen, J. Goyvaerts, S. Kumari, J. V. Kerrebrouck, M. Muneeb, S. Uvin, Y. Yu and G. Roelkens, “Integration of high-speed GaAs metal-semiconductor-metal photodetectors by means of transfer printing for 850 nm wavelength photonic interposers,” *Optics Express,* vol. 26, no. 5, pp. 6351-6359, 2018, DOI: 10.1364/OE.26.006351.

[81] Z. Wang, A. Abbasi, U. Dave, A. Groote, S. Kumari, B. Kunert, C. Merckling, M. Pantouvaki, Y. Shi, B. Tian, K. V. Gasse, J. Verbist, R. Wang, W. Xie, J. Zhang, Y. Zhu, J. Bauwelinck, X. Yin, Z. Hens, J. V. Campenhout, B. Kuyken, R. Baets, G. Morthier, D. V.Thourhout and G. Roelkens, “Novel Light Source Integration Approaches for Silicon Photonics,” *Laser & Photonics Reviews,* vol. 11, no. 4, 2017. DOI: 10.1002/lpor.201700063.

[82] D. Jevtics, B. Guilhabert, A. Hurtado, M. Dawson and M. Strain, “Deterministic integration of single nanowire devices with on-chip photonics and electronics,” *Progress in Quantum Electronics,* vol. 85, no. 100394, 2022. DOI: 10.1016/j.pquantelec.2022.100394.

[83] S. Bao, Y. Wang, K. Lina, L. Zhang, B. Wang, W. A. Sasangka, K. E. K. Lee, S. J. Chua, J. Michel, E. Fitzgerald, C. S. Tan and K. H. Lee, "A review of silicon-based wafer bonding processes, an approach to realize the monolithic integration of Si-CMOS and III–V-on-Si wafers," *Journal of Semiconductors,* vol. 42, no. 2, 2021. DOI: 10.1088/1674-4926/42/2/023106.

[84] G. Roelkens, J. V. Campenhout, J. Brouckaert, D. V. Thourhout, R. Baets, P. R. Romeo, P. Regreny, A. Kazmierczak, C. Seassal, X. Letartre, G. Hollinger, J. Fedeli, L. D. Cioccio and C. Lagahe-Blanchard, "III-V/Si photonics by die-to-wafer bonding," *Materials Today,* vol. 10, no. 7-8, pp. 36-43, 2007. DOI: 10.1016/S1369-7021(07)70178-5.

[85] M. Yokoyama, R. Iida, Y. Ikku, S. Kim, H. Takagi, T. Yasuda, H. Yamada, O. Ichikawa, N. Fukuhara, M. Hata, M. Takenaka and S. Takagi, "Formation of III–V-on-insulator structures on Si by direct wafer bonding," *Semiconductor Science and Technology,* vol. 28, no. 9, 2013. DOI: 10.1088/0268-1242/28/9/094009.

[86] J. Zhang, G. Muliuk, J. Juvert, S. Kumari, J. Goyvaerts, B. Haq, C. O. d. Beeck, B. Kuyken, G. Morthier, D. V. Thourhout, R. Baets, G. Lepage, P. Verheyen, J. V. Campenhout, A. Gocalinska, J. O'Callaghan, E. Pelucchi, K. Thomas, B. Corbett, A. J. Trindade and G. Roelkens, "III-V-on-Si photonic integrated circuits realized using micro-transfer-printing," *APL photonics,* vol. 4, no. 11, 2019. DOI: 10.1063/1.5120004.

[87] R. Kou, T. Hiratani, H. Yagi, H. Kuwatsuka, T.-H. Yen, M. Okano, M. Ohno, H. Kawashima, K. Suzuki, N. Fujiwara, H. Shoji and K. Yamada, "Inter-layer light transition in hybrid III-V/Si waveguides integrated by μ-transfer printing," *Optics Express,* vol. 28, no. 13, pp. 19772-19782, 2020. DOI: 10.1364/OE.394492.

[88] K. Bhatnagar, J. Rojas-Ramirez, R. Contreras-Guerrero, M. Caro and R. Droopad, "Heterointegration of III–V on silicon using a crystalline oxide buffer layer," *Journal of Crystal Growth,* vol. 425, pp. 262-267, 2015. DOI: 10.1016/j.jcrysgro.2015.02.022.

[89] M. Cantoro, C. Merckling, S. Jiang, W. Guo, N. Waldron, H. Bender, A. Moussa, B. Douhard, W. Vandervorst, M. M. Heyns, J. Dekoster, R. Loo and M. Caymaxa, "Towards the Monolithic Integration of III-V Compound Semiconductors on Si: Selective Area Growth in High Aspect Ratio Structures vs. Strain Relaxed Buffer-mediated Epitaxy," in *2012 IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS)*, La Jolla, CA, 2012. DOI: 10.1109/CSICS.2012.6340064.

[90] Y. Wan, Q. Li, A. Y. Liu, A. C. Gossard, J. E. Bowers, E. L. Hu and K. M. Lau, "Temperature characteristics of epitaxially grown InAs quantum dot micro-disk lasers on silicon for on-chip light sources," *Applied Physics Letters,* vol. 109, no. 1, 2016. DOI: 10.1063/1.4955456.

[91] M. Tang, S. Chen, J. Wu, Q. Jiang, K. Kennedy, P. Jurczak, M. Liao, R. Beanland, A. Seeds and H. Liu, "Optimizations of Defect Filter Layers for 1.3-μm InAs/GaAs Quantum-Dot Lasers Monolithically Grown on Si Substrates," *IEEE Journal of Selected Topics in Quantum Electronics,* vol. 22, no. 6, pp. 50-56, 2016. DOI: 10.1109/JSTQE.2016.2551941.

[92] A. Ghosh, M. Clavel and M. Hudait, "Impact of buffer architecture on the performance of heterogeneously integrated III-V-on-Si solar cells," in *2016 IEEE 43rd Photovoltaic Specialists Conference (PVSC)*, Portland, OR, USA, 2016. DOI: 10.1109/PVSC.2016.7750066.

[93] Y. N. Buzynin, M. N. Drozdov, A. N. Buzynin, V. V. Osiko, B. N. Zvonkov, Y. N. Drozdov, A. E. Parafin, A. V. Murel, O. I. Khrykin, A. E. Luk'yanov, F. A. Luk'yanov and R. A. Sennov, "Heteroepitaxial III–V films on fianite substrates and buffer layers," *Bulletin of the Russian Academy of Sciences: Physics,* vol. 73, pp. 485-490, 2009. DOI: 10.3103/S106287380904011X.

[94] M. Miyoshi, A. Watanabe and T. Egawa, "Modeling of the wafer bow in GaN-on-Si epiwafers employing GaN/AlN multilayer buffer structures," *Semiconductor Science and Technology,* vol. 31, no. 105016, 2016. DOI: 10.1088/0268-1242/31/10/105016.

[95] K. Tomioka, T. Tanaka, S. Hara, K. Hiruma and T. Fukui, "III–V Nanowires on Si Substrate: Selective-Area Growth and Device Applications," *IEEE Journal of Selected Topics in Quantum Electronics,* vol. 17, no. 4, pp. 1112-1129, 2011. DOI: 10.1109/JSTQE.2010.2068280.

[96] B. Mayer, L. Janker, B. Loitsch, J. Treu, T. Kostenbader, S. Lichtmannecker, T. Reichert, S. Morkötter, M. Kaniber, G. Abstreiter, C. Gies, G. Koblmüller and J. J. Finley, "Monolithically Integrated High-β Nanowire Lasers on Silicon," *Nano Letters,* vol. 16, no. 1, pp. 152-156, 2016. DOI: 10.1021/acs.nanolett.5b03404.

[97] E. Memisevic, J. Svensson, M. Hellenbrand, E. Lind and L.-E. Wernersson, "ertical InAs/GaAsSb/GaSb tunneling field-effect transistor on Si with S = 48 mV/decade and Ion = 10 μA/μm for Ioff = 1 nA/μm at Vds = 0.3 V," in *2016 IEEE International Electron Devices Meeting (IEDM)*, San Francisco, CA, USA, 2016. DOI: 10.1109/IEDM.2016.7838450.

[98] T. A. Langdo, C. W. Leitz, M. T. Currie, E. A. Fitzgerald, A. Lochtefeld and D. A. Antoniadis, "High quality Ge on Si by epitaxial necking," *Applied Physics Letters,* vol. 76, pp. 3700-3702, 2000. DOI: 10.1063/1.126754.

[99] J. Z. Li, J. Bai, C. Major, M. Carroll, A. Lochtefeld and Z. Shellenbarger, "Defect reduction of GaAs/Si epitaxy by aspect ratio trapping," *Journal of Applied Physics,* vol. 103, no. 10, 2008. DOI: 10.1063/1.2924410.

[100] J. Li, J. Hydrick, J. Park, J. Li, J. Bai, Z. Cheng, M. Carroll, J. Fiorenza, A. Lochtefeld, W. Chan and Z. Shellenbarger, "Monolithic Integration of GaAs/InGaAs Lasers on Virtual Ge Substrates via Aspect-Ratio Trapping," *Journal of The Electrochemical Society,* vol. 156, no. 7, 2009. DOI: 10.1149/1.3129463.

[101] H. Schmid, M. Borg, K. Moselund, L. Gignac, C. M. Breslin, J. Bruley, D. Cutaia and H. Riel, "Template-assisted selective epitaxy of III–V nanoscale devices for co-planar heterogeneous integration with Si," *Applied Physics Letters,* vol. 106, p. 233101, 2015. DOI: 10.1063/1.4921962.

[102] M. F. Ritter, H. Schmid, M. Sousa, P. Staudinger, D. Z. Haxell, M. A. Mueed, B. Madon, A. Pushp, H. Riel and F. Nichele, "Semiconductor Epitaxy in Superconducting Templates," *Nano Letters,* vol. 21, no. 23, pp. 9922-9929, 2021. DOI: 10.1021/acs.nanolett.1c03133.

[103] A. Goswami, B. Markman, S. T. Š. Brunelli, S. Chatterjee, J. Klamkin, M. Rodwell and C. J. Palmstrøm, "Confined lateral epitaxial overgrowth of InGaAs: Mechanisms and electronic properties," *Journal of Applied Physics,* vol. 130, no. 8, 2021. DOI: 10.1063/5.0050802.

[104] H. Schmid, D. Cutaia, J. Gooth, S. Wirths, N. Bologna, K. E. Moselund and H. Riel, "Monolithic integration of multiple III-V semiconductors on Si for MOSFETs and TFETs," in *2016 IEEE International Electron Devices Meeting (IEDM)*, San Francisco, CA, USA, 2016. DOI: 10.1109/IEDM.2016.7838340.

[105] Z. Yan, Y. Han, L. Lin, Y. Xue, C. Ma, W. K. Ng, K. S. Wong and K. M. Lau, "A monolithic InP/SOI platform for integrated photonics," *Light: Science & Applications,* vol. 10, no. 200, 2021. DOI: 10.1038/s41377-021-00636-0.

[106] N. Bologna, S. Wirths, L. Francaviglia, M. Campanini, H. Schmid, V. Theofylaktopoulos, K. E. Moselund, A. F. i. Morral, R. Erni, H. Riel and M. D. Rossell, "Dopant-Induced Modifications of GaxIn(1–x)P Nanowire-Based p–n Junctions Monolithically Integrated on Si(111)," *Applied Materials and Interfaces,* vol. 10, no. 38, pp. 32588-32596, 2018. DOI: 10.1021/acsami.8b10770.

[107] D. Cutaia, K. E. Moselund, M. Borg, H. Schmid, L. Gignac, C. M. Breslin, S. Karg, E. Uccelli and H. Riel, "Vertical InAs-Si Gate-All-Around Tunnel FETs Integrated on Si Using Selective Epitaxy in Nanotube Templates," *IEEE Journal of the Electron Devices Society,* vol. 3, no. 3, pp. 176-183, 2015. DOI: 10.1109/JEDS.2015.2388793.

[108] C. Convertino, C. Zota, H. Schmid, D. Caimi, M. Sousa, K. Moselund and L. Czornomaz, "InGaAs FinFETs Directly Integrated on Silicon by Selective Growth in Oxide Cavities," *Materials,* vol. 12, no. 1, p. 87, 2019. DOI: 10.3390/ma12010087.

[109] S. Wirths, B. F. Mayer, H. Schmid, M. Sousa, J. Gooth, H. Riel and K. E. Moselund, "Room-Temperature Lasing from Monolithically Integrated GaAs Microdisks on Silicon," *ACS Nano,* vol. 12, no. 3, pp. 2169-2175, 2018. DOI: 10.1021/acsnano.7b07911.

[110] M. Scherrer, S. Kim, H. Choi, C.-W. Lee and K. E. Moselund, “Topological lasing from embedded III-V 1D photonic crystal lattices in the telecom O-band,” in *SPIE Nanoscience + Engineering*, San Diego, California, USA, 2021. DOI: 10.1117/12.2594421.

[111] M. Borg, L. Gignac, J. Bruley, A. Malmgren, S. Sant, C. Convertino, M. D. Rossell, M. Sousa, C. Breslin, H. Riel, K. E. Moselund and H. Schmid, “Facet-selective group-III incorporation in InGaAs template assisted selective epitaxy,” *Nanotechnology,* vol. 30, no. 084004, 2019, DOI: 10.1088/1361-6528/aaf547.

[112] M. Borg, H. Schmid, J. Gooth, M. D. Rossell, D. Cutaia, M. Knoedler, N. Bologna, S. Wirths, K. E. Moselund and H. Riel, “High-mobility GaSb nanostructures cointegrated with InAs on Si,” *ACS Nano,* vol. 11, no. 3, p. 2554–2560, 2017, DOI: 10.1021/acsnano.6b04541.

[113] P. Tiwari, P. Wen, S. Mauthe, M. Baumann, B. I. Bitachon, H. Schmid, J. Leuthold and K. E. Moselund, “Butt-Coupled III-V Photodetector Monolithically Integrated on SOI with data reception at 50 Gbps OOK,” in *2021 Optical Fiber Communications Conference and Exhibition, OFC 2021 – Proceedings*, 2021, DOI: 10.1364/OFC.2021.F2C.2.

[114] R. Wieland, “SiO2,” in *Handbook of 3D Integration*, P. Garrou, C. Bower and P. Ramm, Eds., Wiley-VCH, 2008, pp. 107-120. DOI: 10.1002/9783527623051.ch6.

[115] J. Chen, «The comparative study of thermal stability among silicon dioxide, fluorinated silicate glass, hydrogen silsesquioxane, and organosilicate glass dielectrics on silicon,» *Thin Solid Films,* vol. 516, nº 18, pp. 6013-6019, 2008. DOI: 10.1016/j.tsf.2007.10.109.

[116] C. W. Holzwarth, T. Barwicz and H. I. Smith, “Optimization of hydrogen silsesquioxane for photonic applications,” *Journal of Vacuum Science & Technology B,* vol. 25, no. 6, p. 2658–2661, 2007. DOI: 10.1116/1.2787832.

[117] G. B. Stringfellow , “Non-hydride group V sources for OMVPE,” *Journal of Electronic Materials,* vol. 17, pp. 327-335, 1988. DOI: 10.1007/BF02652114.

[118] F. Maury, “Organometallic molecular precursors for low-temperature MOCVD of III–V semiconductors,” *Advanced Materials,* vol. 3, no. 11, pp. 542-548, 1991. DOI: 10.1002/adma.19910031104.

[119] K. Vanhollebeke, M. d'Hondt, I. Moerman, P. v. Daele and P. Demeester, “Zn doping of InP, InAsP/InP, and InAsP/InGaAs heterostructures through metalorganic vapor phase diffusion (MOVPD),” *Journal of Electronic Materials,* vol. 30, no. 8, pp. 951-959, 2001. DOI: 10.1007/BF02657716.

[120] A. Marchevsky, J. Mørk and K. Yvind, “Doping technologies for InP membranes on silicon for nanolasers,” in *Proc. SPIE 10939, Novel In-Plane Semiconductor Lasers XVIII*, San Francisco, California, US, 2019. DOI: 10.1117/12.2509487.

[121] S. Mehari, A. Gavrilov, S. Cohen, P. Shekhter, M. Eizenberg and D. Ritter, “Measurement of the Schottky barrier height between Ni-InGaAs alloy and In0.53Ga0.47As,” *Applied Physics Letters,* vol. 101, no. 7, 2012. DOI: 10.1063/1.4746254.

[122] E. Ghegin, P. Rodriguez, M. Pasquali, I. Sagnes, J. L. Lábár, V. Delaye, T. Card, J. D. Fonseca, C. Jany and F. Nemouchi, “CMOS-Compatible Contacts to n-InP,” *IEEE Transactions on Electron Devices,* vol. 64, no. 11, pp. 4408-4414, 2017. DOI: 10.1109/TED.2017.2747619.

[123] J. Decobert and G. Patriarche, “Transmission electron microscopy study of the InP/InGaAs and InGaAs/InP heterointerfaces grown by metalorganic vapor-phase epitaxy,” *Journal of Applied Physics,* vol. 92, no. 10, p. 5749–5755, 2002. DOI: 10.1063/1.1513891.

[124] G. K. Reeves and H. B. Harrison, “Obtaining the specific contact resistance from transmission line model measurements,” *IEEE Electron Device Letters,* vol. 3, no. 5, pp. 111-113, 1982. DOI: 10.1109/EDL.1982.25502.

[125] C. Martinez-Oliver, M. Scherrer, S. Iadanza, H. Schmid, K. Moselund and V. Georgiev, “Simulation and Fabrication of Monolithic III-V Photodetectors on Si: the Role of Growth Facets and Localization of Heterojunctions,” *IEEE Transactions on Electron Devices,* vol. 71, no. 10, pp. 6124-6130, 2024. DOI: 10.1109/TED.2024.3437333.

[126] M. Knoedler, N. Bologna, H. Schmid, M. Borg, K. E. Moselund, S. Wirths, M. D. Rossell and H. Riel, “Observation of Twin-free GaAs Nanowire Growth Using Template-Assisted Selective Epitaxy,” *Crystal Growth and Design,* vol. 17, no. 12, pp. 6297-6302, 2017, DOI: 10.1021/acs.cgd.7b00983.

[127] E. Brugnolotto, H. Schmid, V. Georgiev and M. Sousa, “In-Plane III–V Nanowires on Si(110) with Quantum Wells by Selective Epitaxy in Templates,” *Crystal Growth & Design,* vol. 23, no. 11, pp. 8034-8042 , 2023, DOI: 10.1021/acs.cgd.3c00806.

[128] G. Barbarino, R. d. Asmundis, G. D. Rosa, C. M. Mollo, S. Russo and D. Vivolo, “Silicon Photo Multipliers Detectors Operating in Geiger Regime: an Unlimited Device for Future Applications,” in *Photodiodes - World Activities in 2011*, InTech, 2011, DOI: 10.5772/21521.

[129] C. Sun, M. Wade, Y. Lee, J. Orcutt, L. Alloatti, M. Georgas, A. Waterman, J. Shainline, R. Avizienis, S. Lin, B. Moss, R. Kumar, F. Pavanello, A. Atabaki, H. Cook, A. Ou, J. Leu, Y.-H. Chen, K. Asanović, R. Ram, M. Popović and V. Stojanović, “Single-chip microprocessor that communicates directly using light,” *Nature,* vol. 528, no. 7583, pp. 534-538, 2015. DOI: 10.1038/nature16454.

[130] P. J. Winzer, D. T. Neilson and A. R. Chraplyvy, “Fiber-optic transmission and networking: the previous 20 and the next 20 years,” *Optics express,* vol. 26, no. 18, pp. 24190-24239, 2018. DOI: 10.1364/OE.26.024190.

[131] D. A. B. Miller, “Rationale and challenges for optical interconnects to electronic chips,” *Proceedings of the IEEE,* vol. 88, no. 6, pp. 728-749, 2000. DOI: 10.1109/5.867687.

[132] G. Keiser, “Optical Fiber Communications,” in *Wiley Encyclopedia of Telecommunications*, J.G. Proakis, 2003. DOI: 10.1002/0471219282.eot158.

[133] I. T. Monroy and E. Tangdiongga, Crosstalk in WDM Communication Networks, NY: Springer New York, 2002. DOI: 10.1007/978-1-4757-3594-9.

[134] T. K. O. Vu, M. T. Tran, N. X. Tu, N. T. T. Bao and E. K. Kim, “Electronic transport mechanism and defect states for p-InP/i-InGaAs/n-InP photodiodes,” *Journal of Materials Research and Technology,* vol. 19, pp. 2742-2749, 2022. DOI: 10.1016/j.jmrt.2022.06.028.

[135] L. Tian, L. Zhang, E. Li, W. Ji, J. Horvat, J. C. Cao, W. Shi and C. Zhang, “Thermal characteristic of dark resistivity of InGaAs photoconductive semiconductor switches,” *Journal of Materials Science: Materials in Electronics,* vol. 30, p. 15339–15344, 2019. DOI: 10.1007/s10854-019-01907-8.