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Advanced Hydrogen-Terminated Diamond Field Effect Transistor Technology

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Submitted in fulfilment of the requirements for the
Degree of Doctor of Philosophy

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Abstract

Diamond demonstrates excellent properties for use in high-power and high-frequency electronic devices due to its wide band gap, high carrier mobility, and thermal conductivity. Traditional doping methods prove difficult in diamond due to its strong carbon to carbon bonds and the deep energy levels of most dopants. To overcome these difficulties, transfer doping has emerged as a viable alternative, particularly for hydrogen terminated p-type doped diamond. Hydrogen-terminated diamond is widely used for MOSFET fabrication because of its low thermal activation energy.

Given the sensitive nature of hydrogen termination of diamond, this work explores multiple alternative fabrication methods to replace the conventional gold sacrificial layer and protect the hydrogen termination from damage caused by plasma or air exposure during the fabrication process. H-diamond MESFETs with and without ALD Al_2O_3 encapsulation were fabricated and measured. Device properties such as drain current and gate leakage current were observed to improve after Al_2O_3 deposition. After the encapsulation, the drain current improved from 16.3 mA/mm to 37.5 mA/mm, while the gate leakage current dropped from 2.49 mA/mm to 0.05 mA/mm. However, high-temperature measurements revealed device degradation at elevated temperatures up to 450K, with the drain current decreasing from 39.6 mA/mm at room temperature to 10 mA/mm at 450K.

Accumulation channel MOSFETs on H-diamond were fabricated using high-temperature annealing and both PVD and ALD Al_2O_3. With this method, MOSFETs on H-diamond do not rely on transfer doping formed by air adsorbates and hydrogen termination. However, hydrogen termination is still required under the gate to form an accumulation channel. These devices exhibited normally-off properties ($I_{on}/I_{off} = 10^9$) and achieved a maximum drain current of 110 mA/mm. The threshold voltage ($V_{th} < -5\ V$) represents the lowest state-of-the-art value for hydrogen-terminated diamond MOSFETs. The carrier concentration and mobility extracted by the CV analysis is $2 \times 10^{12}\ cm^{-2}$ and 110 $cm^2/V \cdot s$, respectively.

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Associated Publications

Journal Entries

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Chunlin Qu, Isha Maini, Jingyi Zhang, Alexey Ganin, David A. J. Moran, (2024) *Catalytic-enhanced thermal hydrogen-temination of diamond for electronic applications*. (Under Review)

Conferences

Chunlin Qu, Isha Maini, Kevin G. Crawford and David A.J. Moran, (2022) *Lift-off Resist as a Protective Layer for Hydrogen-terminated Diamond MOSFET Fabrication*, Surface and Bulk Defects in Diamond (SBDD) workshop 2022, Hasselt, Belgium 9 - 11 March. (Poster)

Chunlin Qu, Isha Maini, Kevin G. Crawford and David A.J. Moran, (2022) *Aluminium as a Protective Layer for Hydrogen-Terminated Diamond MOSFET Fabrication*, UK Semiconductors 2022, Sheffield, UK 6 - 8 July. (Oral)

Declaration

With the exception of chapters 1, 2 and 3, which contain introductory material, all work in this thesis was carried out by the author unless otherwise explicitly stated.

Chapter 1

Introduction

Diamond possesses several remarkable properties that make it highly desirable for various applications, including electronic devices.

Firstly, its wide band gap of 5.47 eV enables diamond-based electronic devices, such as MOSFETs, to potentially operate at high temperatures without excess excitation of electrons or holes, ensuring stable performance even in extreme conditions. Additionally, this wide band gap contributes to its exceptionally high breakdown field of 10 MV/cm, surpassing that of other materials like 4H-SiC and GaN [1], [2]. This high breakdown field allows diamond to withstand high voltages without experiencing impact ionization or avalanche breakdown.

Moreover, diamond exhibits extraordinary thermal conductivity, four times higher than 4H-SiC and twenty times higher than GaN [3], [4]. This outstanding thermal conductivity, stemming from its efficient phonon transport facilitated by strong chemical bonding and light atomic mass, enables efficient thermal conduction, minimizing thermal losses in high-power diamond-based devices.

Another advantageous property of diamond is its high carrier mobility. In intrinsic single-crystal CVD diamond, the reported achieved highest mobility of electrons and holes in diamond is 1945 $cm^2/V \cdot s$ and 2285 $cm^2/V \cdot s$, respectively [5]. In comparison, widely used high-temperature electronic materials like SiC have significantly lower carrier mobility for electrons (950 $cm^2/V \cdot s$) and holes (260 $cm^2/V \cdot s$) [6], [7]. This high carrier mobility in diamond allows carriers to reach saturation velocity faster, enhancing the overall performance and speed of electronic devices.

Overall, the combination of these outstanding properties makes diamond an attractive material for various electronic applications, offering potential high-temperature operation, high break-

down voltage, efficient thermal management, and superior carrier mobility.

Boron and phosphorus were well explored as dopants in diamond to prepare p-type and n-type diamond [8], [9]. However, the high thermal activation energy of Boron-doped diamond (0.37 eV) and Phosphorus (0.6 eV) limited its application. Hydrogen-terminated diamond has been extensively studied in the last decades as a substitution for p-type diamond. The lowest sheet resistance, 719 $\Omega/\square$, of hydrogen-terminated diamond was reported by Sato et al. [10]. And the hole mobility of the hydrogen-terminated diamond has been reported between 3 $cm^2/V \cdot s$ to 300 $cm^2/V \cdot s$ [11], [12].

In this work, the fabrication of Field Effect Transistors with hydrogen-terminated diamond is explored. This thesis starts with the background and literature review of hydrogen-terminated diamond and related theoretical introduction.

In Chapter 4, the fabrication process is discussed in detail. Each fabrication step used in this work is discussed thoroughly. The last two sections of this chapter give the fabrication flows of hydrogen-terminated diamond MESFETs and MOSFETs in detail. Chapter 5 gives a brief introduction to the equipment (SEM, AFM, and Surface Profiler) used for surface profiling and methods used for electrical measurement.

Chapter 6 explores a new method, "Spillover", to hydrogen-terminate the diamond surface rather than using hydrogen plasma. Low-concentration hydrogen (5%), high temperature (900°C), and catalyst metals (Pd and Pt) were used in this work to complete the termination process.

Chapter 7 concludes alternative fabrication methods explored to protect the hydrogen termination on the diamond surface during the fabrication process or form a better ohmic contact. Lift-off resist (LOR) was explored to be used as a Au sacrificial layer substitution and Pd was explored to be used to form an ohmic contact on hydrogen-terminated diamond.

Chapter 8 discusses the electrical characteristics of hydrogen-terminated MESFETs. The device properties were measured during air exposure and at elevated temperatures. TLM and VDP structures were fabricated on the same sample and measured to help understand the ohmic contact behaviour against air exposure duration and elevated temperature.

Chapter 9 reports on accumulation-mode hydrogen-terminated diamond MOSFETs fabricated with physical vapor deposition (PVD) Al_2O_3. Devices' transfer and output characteristics are discussed to understand the devices' behaviour. The Split C-V method is used to extract the carrier mobility and concentration. Record low threshold voltage (<-5 V) combined with high drain current (110 mA/mm) were achieved with these devices.

Chapter 2

Background: Diamond as a Semiconductor

Diamond possesses many properties, such as wide band gap, robustness and chemical inertness, making it an attractive material for many areas, including electrical applications. This chapter will discuss diamonds as a promising material for semiconductor electronic device applications.

The chapter commences by examining the diamond crystal structure and delves into the advantages that diamond derives from its stringent arranged crystal lattice. Following this is a brief introduction to the diamond's growth methods. Then impurities doping and surface transfer doping of diamond are discussed and compared in detail, which leads to the reason that later choice is employed in this research. Succeeding this is an introduction of metal-semiconductor (MESFET) and metal-oxide-semiconductor (MOSFET) theories to explain the operation of hydrogen-terminated diamond FETs.

2.1 Diamond Structure

Carbon, a fundamental element in the periodic table, serves as the cornerstone of life on our planet. The atomic structure of carbon is shown in Figure 2.1. There are 2 electrons on 1s orbital and two on 2s orbital while the remaining two electrons are on p orbitals. Figure 2.1 shows the electronic configuration of ground-state carbon. Two electrons on 2s orbitals can migrate to the p orbital in the excited state and hybridise with other electrons from different atoms to form various materials.

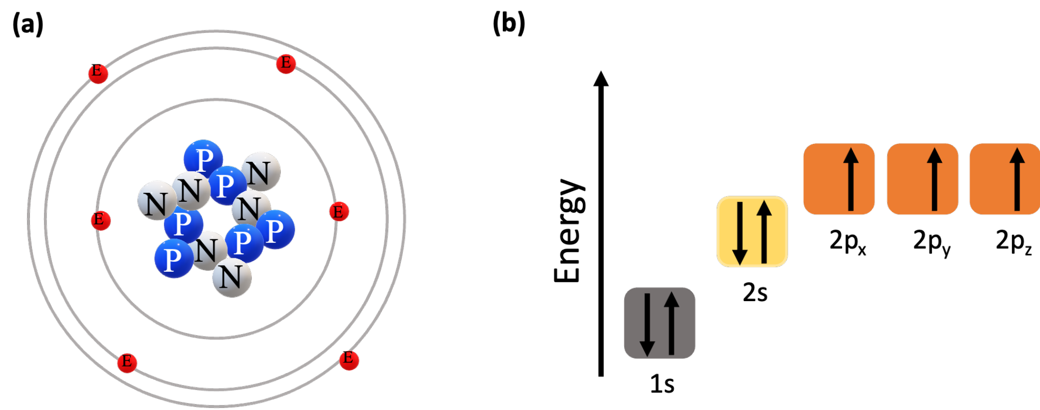


Figure 2.1: Carbon atomic structure and ground state electronic configuration [13].

In nature, elemental carbon has two allotropes: graphite with sp2-hybridisation and diamond with sp3-hybridisation [14]. In sp2-hybridisation, one 2s orbital and two p orbitals hybridise into three orbitals with an angle of 120° between each orbital. This hybridisation is also called trigonal hybridisation. In the case of graphite, one carbon atom is connected to 3 adjacent carbon atoms with covalent bonding on a layer plane. The overlap of sp2-hybridisation orbitals forms three σ-bonding, the most robust covalent bonding, and leaves a loose π-electron that plays a vital role in graphite electronic properties [15]. On the opposite of solid bonding between each carbon atom on the same plane layer, each plane layer is bonded to others with weak Van der Walls force that makes graphite shows different properties in the vertical direction. The presence of Van der Walls force in the vertical direction makes it possible to extract a solitary layer of graphite out of the bulk graphite. And this single layer of graphite is known as graphene.

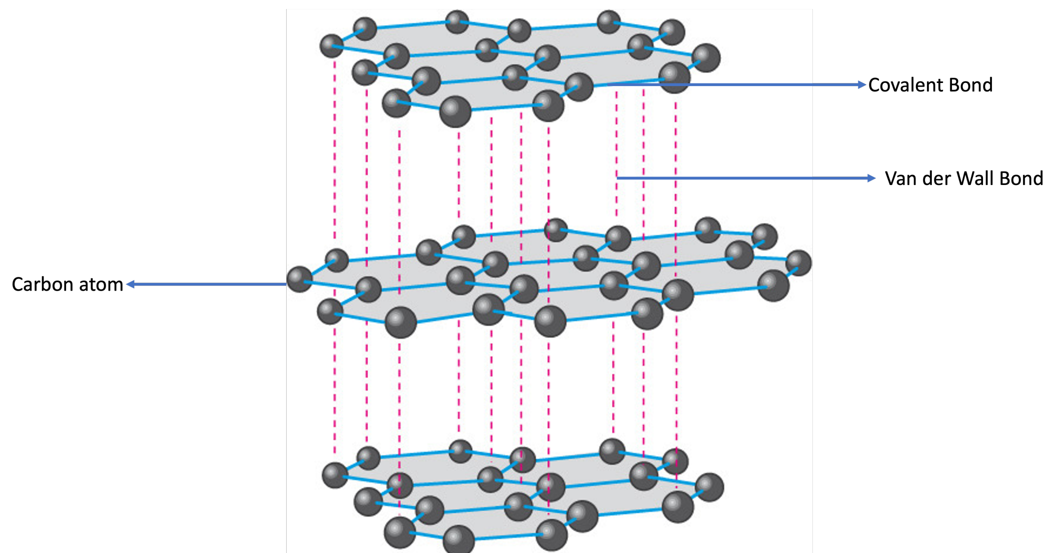


Figure 2.2: Graphite atomic Structure.

In sp3-hybridisation, one 2s orbital and three p orbitals hybridise into four orbitals with an angle of 109.5° between two adjacent orbitals [16]. This hybridisation is also named tetrahedral hybridisation and is applied in the diamond structure. When assembling many carbon atoms with sp3-hybridisation, each carbon atom can connect to 4 other carbon atoms, and the overlapped orbitals form 4 σ-bonding in a three-dimensional space. This structure contributes to many of diamond's properties. First, those strong carbon-carbon covalent bonds make diamond one of the hardest and chemically inert materials. In the excited state, all four electrons are occupied with forming the bonds in the diamond, and no extra electron can be excited to the conduction band with visible wavelength. Therefore pure diamond shows a transparent appearance [16].

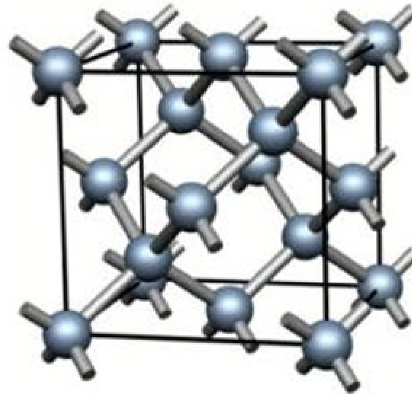


Figure 2.3: Diamond lattice structure [17].

Because carbon atoms are small in size, they can approach each other relatively closely before experiencing a repulsive force, which is a characteristic that contributes to the formation of short carbon bonds [18]. This short bond and the overlap of orbitals give rise to a significant energy separation between antibonding orbital and bonding orbitals. That means a big forbidden band sits between the conduction and valence bands. In diamond, the forbidden band gap has an energy of 5.47 eV at room temperature (300 K) [19]. Therefore, an intrinsic diamond is usually considered an insulator or ultra wide-band gap semiconductor. That makes diamond potentially suitable for high-temperature electronic applications because the wide band gap can stop excess excitation of electrons from the top of the valence band to the bottom of the conduction band [20].

As a wide-bandgap material, diamond lacks enough carriers to travel through the material and carry thermal energy for heat dissipation. However, the rigid carbon structure and covalent bonds help diamonds to transport phonon effectively, which gives diamonds the highest thermal conductivity (24 $Wcm^{-1}K^{-1}$) among known wide band gap semiconductors [19]. The high thermal conductivity makes diamonds a promising candidate for high-power devices.

$$V_s = \sqrt{\frac{8E_{opt}}{3\pi m^*} tanh(E_{opt}/2kT)} \quad (2.1)$$

Applied high electric fields increase carriers' drift velocity in semiconductors. Nevertheless, the interaction between carriers and crystal lattice makes carriers lose their energy rapidly by optical phonon emission. Together with other scattering mechanisms, semiconductor carriers always reach a velocity that can not be exceeded; that is known as the saturation velocity (V_s) as shown in Equation 2.1. Saturation velocity benefits from high optical energy (E_{opt}) and low effective mass (m^*), and diamond has the highest optical phonon energy that gives rise to a very high saturation velocity, 1.2×10^7 $cm\ s^{-1}$ and 2.7×10^7 $cm\ s^{-1}$ for holes and electrons, respectively [19]. A high saturation velocity makes diamonds a potential material for the high-frequency application.

Intrinsic Materials Properties				
	CVD Diamond	Si	GaN	4H-SiC
Bandgap(eV)	5.47	1.1	3.44	3.2
Holes Saturation velocity($\times 10^{-7} cm\ s^{-1}$)	1.2	0.72	0.63	1
Electron Saturation velocity($\times 10^{-7} cm\ s^{-1}$)	2.7	0.86	2.5	3
Breakdown field($MV cm^{-1}$)	10	0.3	5	3
Hole mobility($cm^2 V^{-1} s^{-1}$)	3800	480	200	120
Electron mobility($cm^2 V^{-1} s^{-1}$)	4500	1450	440	900
Thermal conductivity($W cm^(-1) k^(-1)$)	24	1.5	1.3	5

Table 2.1: Semiconductor properties comparison between CVD Diamond, Si, GaN and 4H-SiC [19], [21]–[23].

Except for those properties mentioned above, the carrier mobility in ultra-pure and single crystal diamond has been measured at 2285 cm^2/V for electrons and 1945 cm^2/V for holes, which is also the highest recorded values among wide-bandgap materials [5]. That means carriers moving through a diamond can reach the saturation velocity at lower electric field. Table 2.1 shows the comparison of diamond and other semiconductor materials.

2.2 Synthetic Diamond Production

In nature, carbon-containing materials, such as organic matter, experience extreme pressure and heat near the earth's mantle area, forming natural diamonds. However, the high cost and uncontrollable impurities of natural diamonds mean that they are not suitable for electronic device fabrication. Compared to natural diamonds, synthetic diamonds exhibit higher purity, lower cost, better consistency and customizable size and shapes [24]. Those advantages make synthetic diamonds a better choice for device fabrication.

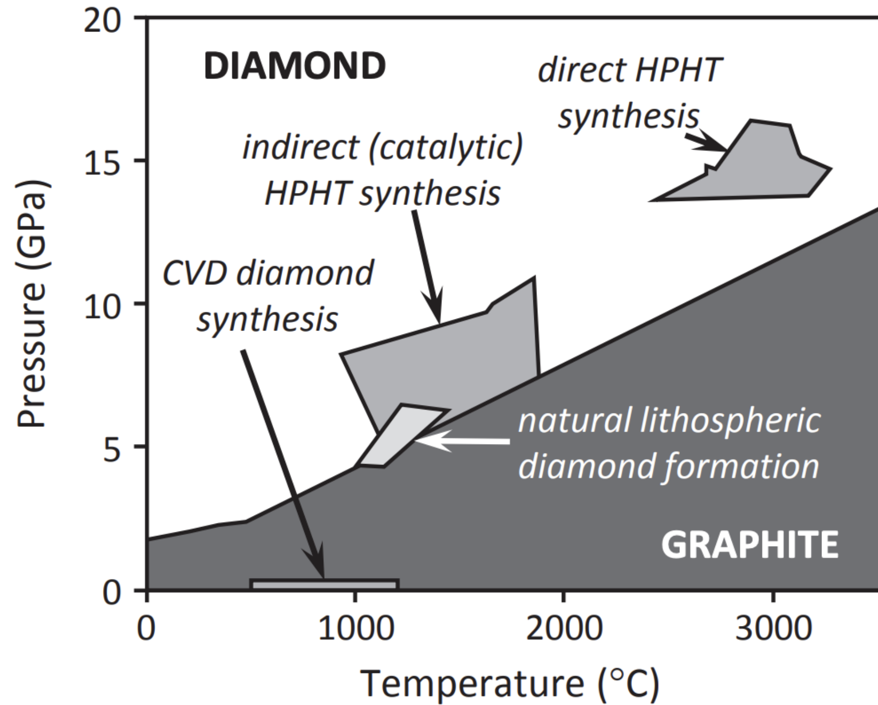


Figure 2.4: Carbon phase under different conditions and the conditions for HPHT diamonds and CVD diamonds. Direct HPHT and indirect synthesis refer to the process without or with diamond seeds [25].

From a thermodynamic perspective, diamond is unstable compared to graphite, meaning that if a suitably high pressure and high temperature are applied, graphite can be transformed into diamond [26]. In the 1950s, General Electric Company announced the first high-pressure and high-temperature (HPHT) diamond [27]. Diamond seeds were placed in a chamber with a pressure of 5-6 Gpa and temperature of 1300 °C to 1600 °C. The carbon source, usually graphite and catalyst, would be sent into the growth chamber to stimulate diamond synthesis [25].

HPHT method synthesises diamonds by applying temperature and pressure at the region where the diamond is at its stable regime. Diamonds can also be formed at their meta-stable regime, which leads to chemical vapour deposition (CVD). Hydrogen and hydrocarbons, such as C_2H_2 or CH_4, the mixture is introduced in the reaction chamber where different techniques like plasma, hot surface and combustion flames are used to activate reactants to create radicals, molecular, and ionic species [28]. This process happens at a pressure of 2 to 50 Kpa, much lower than that of HPHT methods. Meanwhile, a lower temperature, compared to the HPHT method, on the substrate surface is kept at 600 °C to 1200 °C[25]. Cleaned substrates with or without diamond seeds are used to prepare single-crystal or polycrystalline diamonds. Because of the use of hydrogen, CVD synthetic diamond shows a hydrogen-terminated surface. Figure 2.5 illustrates the plasma assisted CVD diamond growth chamber and the growth process.

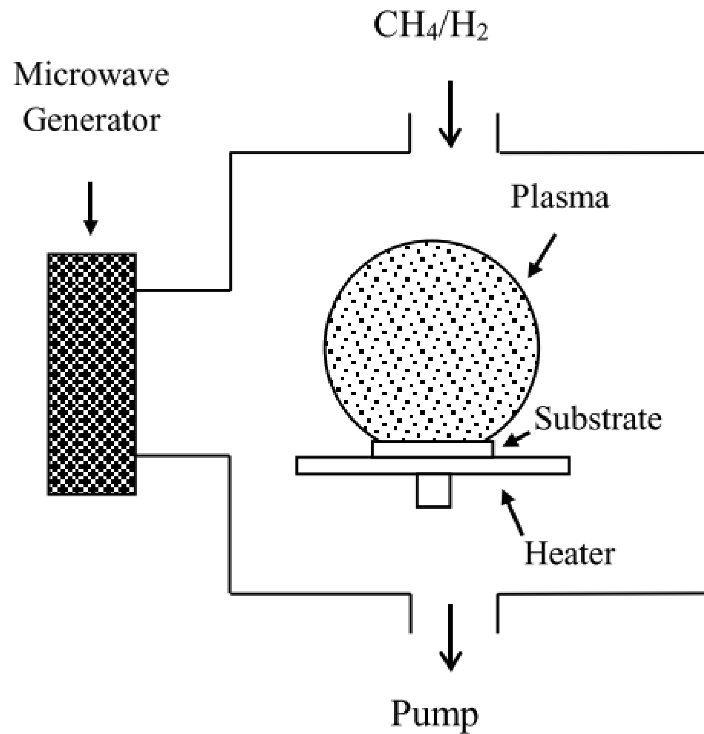


Figure 2.5: Diagram of CVD growth chamber [29].

Compared to the HPHT method, the CVD method is more widely used because of the lower cost benefits from lower pressure, higher purity, easier doping, and higher scalability. In this work, all of diamonds used for devices fabrication are CVD-grown diamonds.

2.3 Doping of Diamond

Impurity doping intentionally adds small amounts of foreign atoms (impurities) to semiconductor materials to modify its electrical properties. The impurities are usually from a different element group of elements than the semiconductor and act as either donor or acceptor, creating excess electrons (n-type doping) or holes (p-type doping).

Ion implantation and diffusion are two critical methods for impurity doping [30]. In the diffusion doping process, semiconductor materials are placed under a high-temperature environment with a gas containing the desired dopant flow through the surface. The chamber pressure influences the doping depth and concentration. Since the impurities need to travel through the semiconductors, this method may lead to a deviated uniformity in the vertical direction. In addition, diamonds' tight and stringent lattice structure makes diffusion difficult [31].

Compared to diffusion doping, ion implantation has better uniformity. In the ion implantation process, energetic ions beam with energy between 300 eV and 5 MeV are introduced into the

semiconductor. The ion beam can travel up to 10 μm under the substrate's surface, so ion implantation has better uniformity than diffusion [30]. However, the energetic ion beams are always accompanied by lattice damage. In diamond, the metastable sp3 configuration can be converted to graphite with stable sp2 configuration in the following annealing process that is aimed to remove the lattice damages caused by the ion beams [32].

Thus, during-growth-doping is more commonly used for diamonds. As previously mentioned, chemical vapour deposition (CVD) and high-pressure high-temperature (HPHT) are used for diamond synthetic production. The substance that contains desired dopants can be introduced into the growth chamber to acquire doped diamonds [33]. Though the arrangement of the atoms in the diamond structure limits the choice of available impurities. Boron, phosphorus and nitrogen are widely used in doping diamonds.

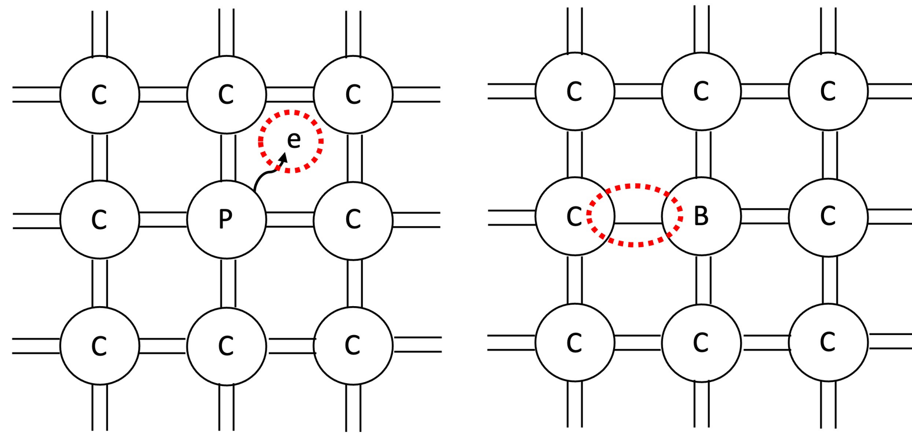


Figure 2.6: N-type and P-type doped diamond lattice with Phosphorus and Boron as example.

As mentioned above, carbon has four electrons in the valence shell. An n-type doped diamond requires an element, such as nitrogen, phosphorus or sulfur, with more than four electrons in the valence shell [34]. When the desired dopant substitutes one carbon atom's position, the valence shell's additional electron is introduced into the diamond lattice. The most common impurity in diamond is nitrogen [35]. Diamond can be classified into two types, Type I and Type II , in terms of the existence of nitrogen. While in natural diamonds, nitrogen tends to be aggregated (Type Ia), in synthetic diamonds, it is typically present as single substitution atoms (Type Ib). Nitrogen acts as a donor in diamond lattice, but the ionisation energy level (1.7 eV) is far too deep to be used as a useful donor at room temperature [36]. At room temperature, sulfur-doped diamond has been observed to exhibit mobility between $250-600$ $cm^2V^{-1}s^{-1}$, along with a thermal activation energy of 0.38 eV [37]. Nevertheless, later research shows that unintentionally induced boron impurities could cause it. Currently, the only unambiguous n-type dopant for diamond is phosphorus which has an activation energy level of 0.6 eV at room temperature [8].

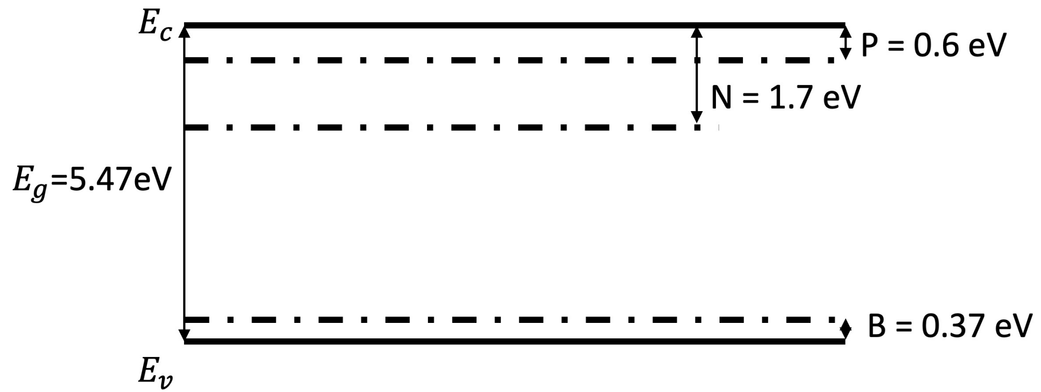


Figure 2.7: The energy levels of different dopants in diamond.

For a p-type doped diamond, an element with fewer electrons on valence orbit is required to create a vacancy at the donor's level. Boron-doped p-type diamonds are found in nature and developed in synthetic diamonds [35]. The addition of boron-containing gas, such as diborane, into the mixture gas of hydrogen, carbon contains gas during the CVD growth process achieves boron-doped p-type diamonds [38]. Though the boron-doped diamonds are well developed, compared to the activation energy level of typical boron-doped silicon (0.045 eV), the boron-doped diamond still shows a relatively high activation energy of 0.37 eV.

Because of the high activation energy level of both p-type doped diamond and n-type doped diamond, at room temperature, the concentration of carriers in doping diamond is deficient. Higher dopant concentration contributes to a better carrier concentration. However, the carriers' mobility reduces significantly due to the additional impurity scattering in the diamond lattice. A potential strategy to alleviate this issue in bulk materials is delta doping. Delta doping is a method where a thin layer of boron atoms is introduced into the diamond lattice, forming a two-dimensional layer of dopants at a thickness of a few atomic layers. The confinement of carriers in a thin layer causes them to move away from the regions with ionised impurities, called delocalisation. It has been proposed that this delocalisation can reduce the impurity scattering in the highly doped diamond, thus exhibiting both high concentration and high mobility at room temperature [39]. The high precision requirement of the boron-doped monolayer in synthetic diamonds thus far has limited the development of this method. with little improvement in p-type diamond observed experimentally thus far using these delta doping techniques.

2.4 Surface transfer doping of diamond

The free dangling bond of carbon on the diamond surface can be terminated by various elements such as oxygen and hydrogen, which dramatically changes the surface electronic properties and allows for an alternative doping process known as "surface transfer doping" .

Electron affinity (χ) is referred to as the energy required to excite electrons from the bottom of the conduction (E_{CBM}) band to the vacuum level (E_{vac}). Moreover, ionisation potential (I) can be calculated by the addition of band gap (E_g) and electron affinity because it is defined as the energy required to excite electrons from the top of the valence (E_{VBM}) band to the vacuum level. As an intrinsic diamond with no surface termination, the electron affinity and ionisation potential are 0.4 eV and 5.87 eV, respectively.

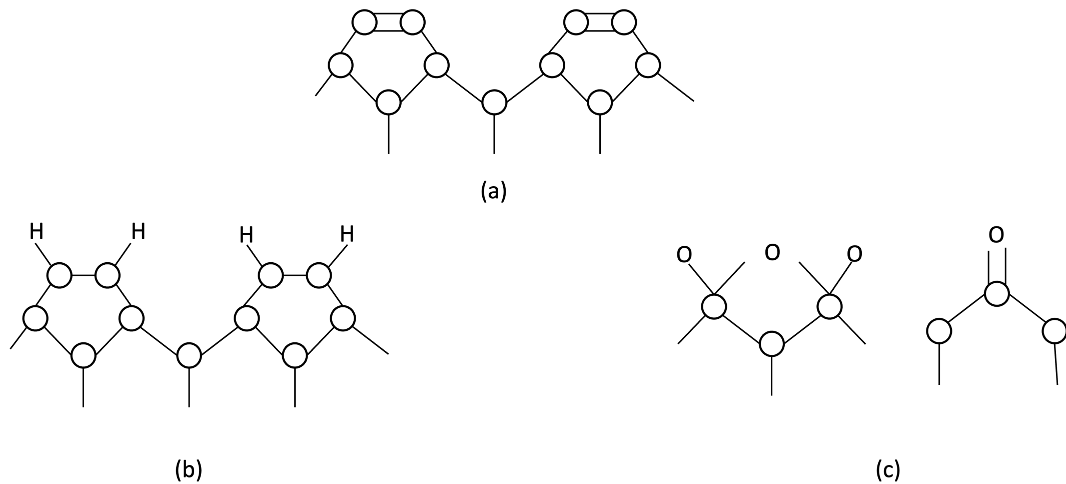
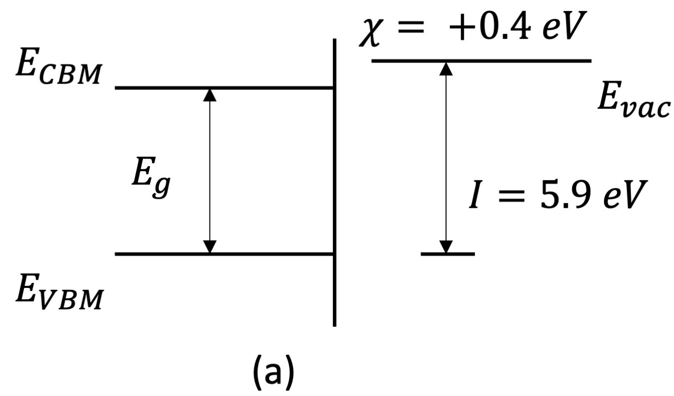
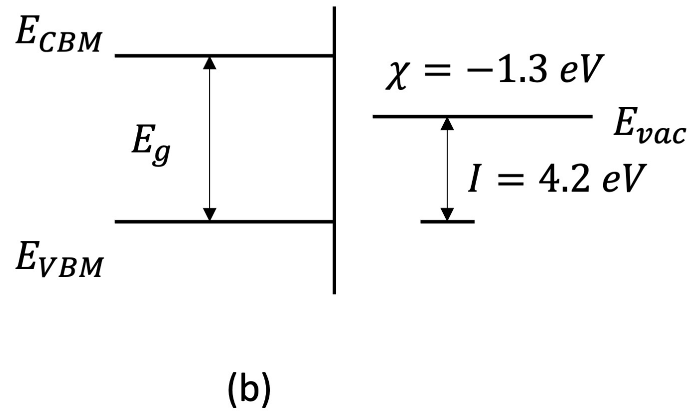


Figure 2.8: The atomic structure of diamond surface with different terminations. (a) Diamond surface without termination, carbon atoms form double-bonded dimers. (b) Hydrogen terminated diamond surface forms $(2 \times 1) : H$ reconstruction. (c) Oxygen terminated diamond surface form $(1 \times 1) : O$ reconstruction in the form of "ether" or "ketone".

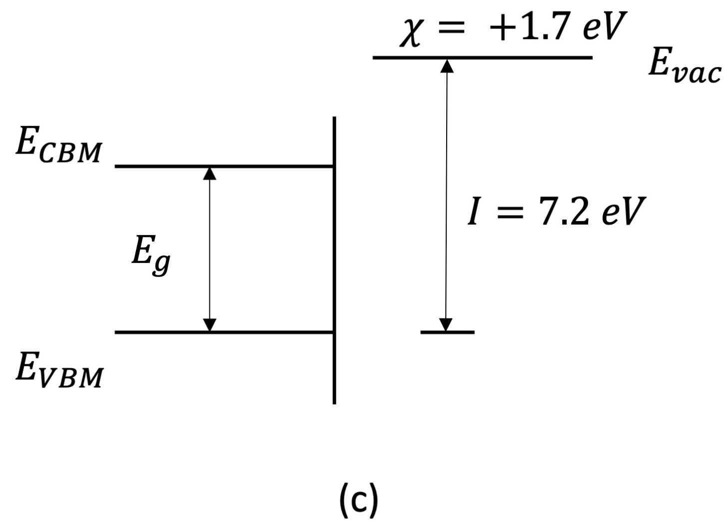
When the surface of the diamond is terminated with oxygen, the surface carbon atoms reconstruct with oxygen atoms to $(1 \times 1) : O$ structure where the oxygen either double bonded with one carbon atom to form "ketone" or single bond to form ether structure [40]. Due to the higher electronegativity of oxygen than that of carbon atoms, the electron affinity of the diamond surface increases to 1.7 eV, which also brings the ionisation potential of the diamond to 7.2 eV.



(a)



(b)



(c)

Figure 2.9: Energy band diagram of diamond with different surface terminations. (a) Clean surface (b) Hydrogen termination (c) Oxygen termination. Due to the electronegativity between the carbon atoms and hydrogen/oxygen atoms, the electron affinity of diamond surface with different termination decreased (with hydrogen) or increased (with oxygen).

However, with hydrogen as the surface termination, the surface reconstructs to (2×1) : H structure [41]. Hydrogen atoms form a single bond with carbon atoms. The electronegativity difference between carbon and hydrogen atoms creates a dipole on the diamond surface. Usually, a semiconductor's vacuum level situates above the conduction band minimum to stop low-energy electrons from escaping to the vacuum. But the dipole on the hydrogen-terminated diamond surface drags the vacuum level below the conduction band minimum by 1.3 eV and brings ionisation potential to 4.2 eV [42]. This property is called negative electron affinity (NEA).

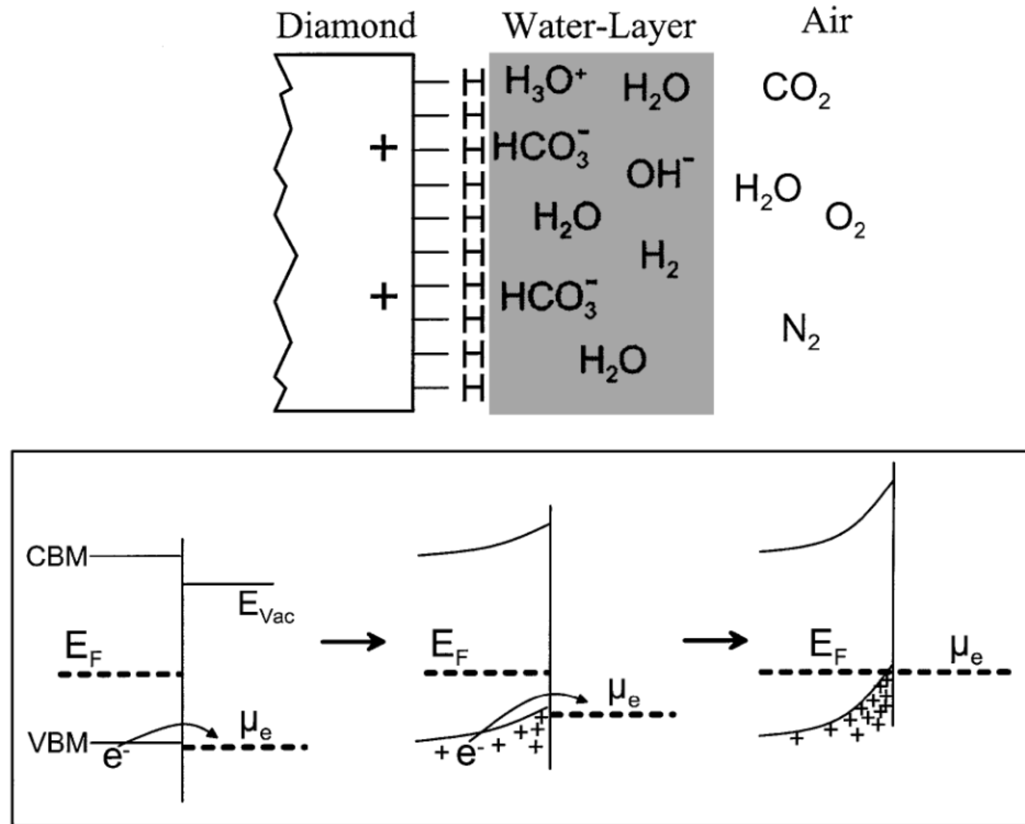


Figure 2.10: Using air adsorbates as an example, energy band diagram for surface transfer doping on a hydrogen-terminated diamond [43].

The relatively small ionisation potential induced by NEA provides a small barrier for the diamond to transfer electrons from the valence band to an energetically favourable electron acceptor on the diamond surface. Such a material should have the lowest unoccupied molecular orbital (LUMO) or single occupied molecular orbital (SOMO) close to or below the valence band maximum of the diamond [44]. In other words, materials with electron affinity greater than hydrogen-terminated diamond ionisation potential (4.2 eV) are generally required. It is reported that air-exposed hydrogen-terminated diamond surface creates a series of chemical groups, such as H_3O^+ and HCO_3^-, to behave as an electron acceptor on the diamond surface [43]. When those air adsorbates come into contact with the hydrogen-terminated diamond surface, excess electrons in the diamond valence band transfer to the lowest unoccupied molecular orbital in

those chemical groups and pull up and bend the energy band to create a holes accumulation layer near the surface. Except for the air adsorbates, other materials like MoO_3, V_2O_5, ReO_3, and WO_3 also act as surface acceptors to transfer excess electrons on the diamond surface [45]–[50].

2.5 Metal semiconductor interfaces

Due to the work function difference, when metal and semiconductor materials are brought together, electrons transport contributes to fermi level form new thermal equilibrium and different types of contact [30]. This section introduces the two most common metal-semiconductor contact: ohmic contact and Schottky contact. In addition, metal oxide semiconductor (MOS) contact will be introduced to understand field effect transistors operation.

2.5.1 Schottky Contact

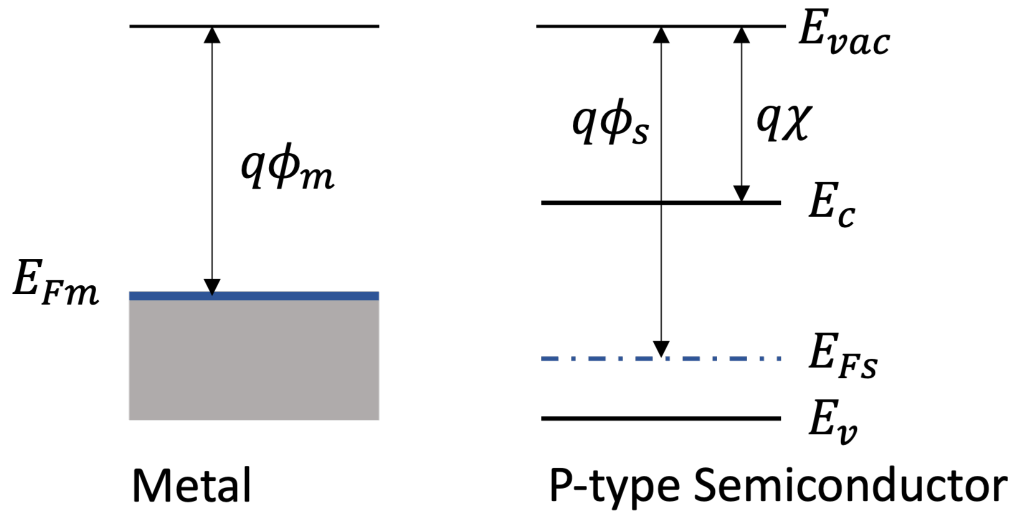
Work function (ϕ) is the energy difference between the Fermi level within a material and the external vacuum level. If a metal with a work function (ϕ_m) is smaller than the work function of a p-type semiconductor (ϕ_s), when they are in contact, electrons in the metal flow to the semiconductor where the Fermi level is lower than that of metal, which also neutralises the majority carriers, holes, in the semiconductor and creates a depletion layer near the metal-semiconductor interface. The depletion layer has a barrier that stops electrons from flowing from metals to semiconductors.

Figure 2.11 shows the band diagram of Schottky contact made with a p-type semiconductor before and after equilibrium. ϕ_{Bp} is defined as the ideal barrier height from the metal side. Equation 2.2 given the expression of this barrier height, where E_g is the bandgap energy.

$$q\phi_{Bp} = E_g - (q\phi_m - q\chi) \tag{2.2}$$

From the side of the semiconductor, the height of the built in barrier can be expressed as equation 2.3.

$$V_b = \phi_s - \phi_m \tag{2.3}$$



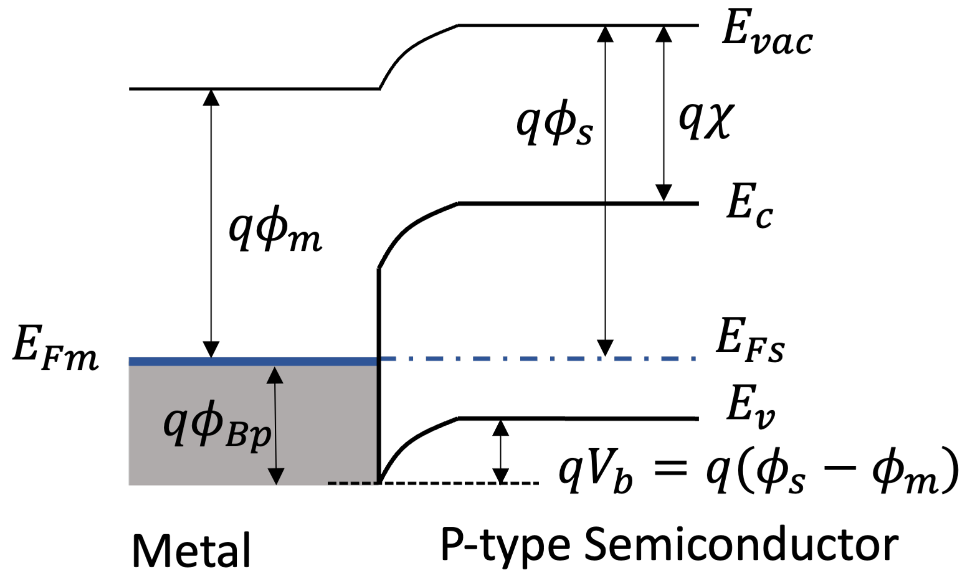


Figure 2.11: Energy band diagram of P-type Schottky contact.
(a) The diagram before contact. (b) Metal and semiconductor making contact and achieving new thermal equilibrium.

Due to the barrier in the metal and semiconductor interface, Schottky contact has rectifying properties. That means that when there is a forward bias applied to the contact, current can flow through more effortlessly than a reverse bias. In the case of metal and p-type semiconductors, the forward bias is when a negative bias is applied to the metal. Figure 2.12 shows the band diagram of p-type Schottky contact with forward bias. The forward bias (negative) attracts the majority carriers (holes) in the semiconductor close to the interface and pulls down the barrier, which makes it easier for electrons to travel from the metal to the semiconductor.

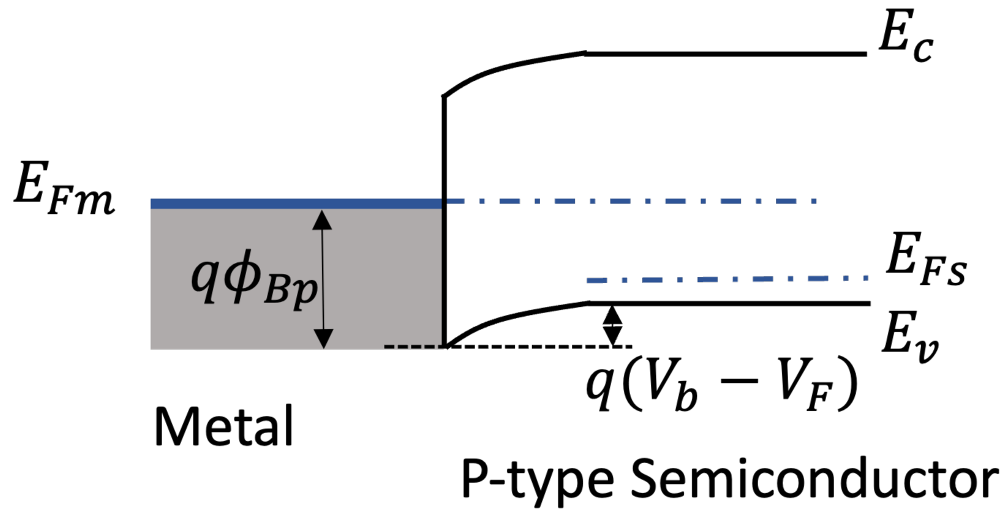


Figure 2.12: P-type Schottky contact with forward bias.

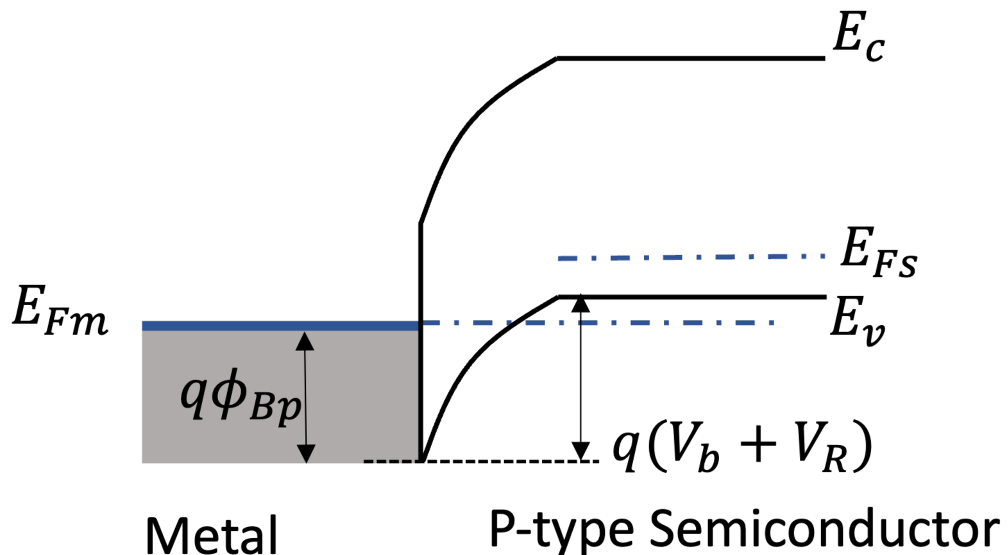


Figure 2.13: P-type Schottky contact with reverse bias.

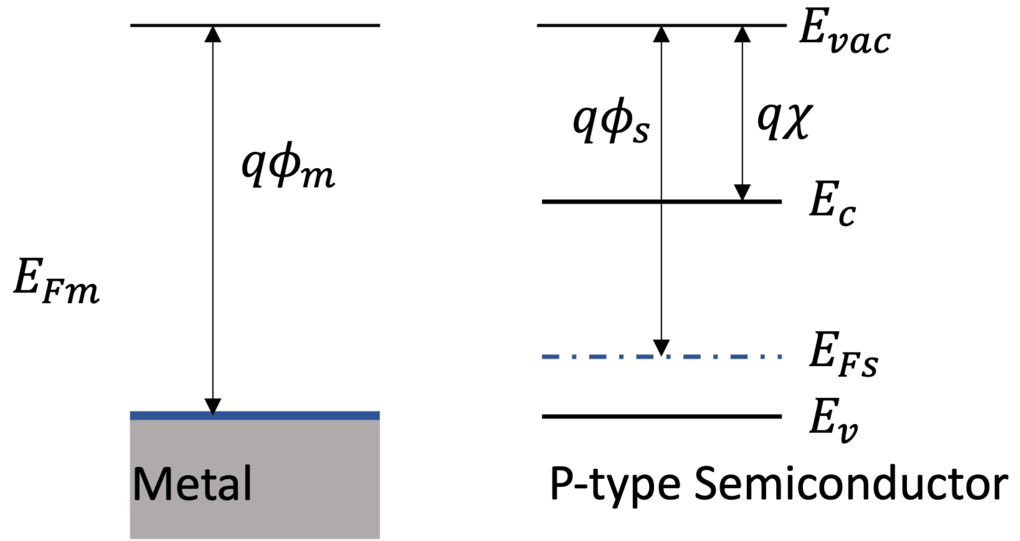
If the bias on metal changes to positive, the contact works in the reverse mode. The positive bias repels holes in semiconductor away and widens the depletion region. The increased barrier makes it more difficult for electrons travel from the metal to the semiconductor.

This rectifying behaviour of Schottky contact can be used as a gate terminal for a MESFET. At forward bias, devices are turned on and off at reverse bias. Though the reverse bias can turn off the contact, there is still some current flow through the interface. There are three ways electrons can overcome the barrier, field emission, thermionic emission and thermionic field emission [30]. Field emission happens when the depletion layer is too thin, and quantum mechanical tunnelling may occur. Field emission depends on the carrier concentration and width of the depletion layer. Thermionic emission usually happens when the electrons acquires enough thermal energy, increasing exponentially as the temperature increases. The last one, thermionic field emission, occurs when electrons obtain enough thermal energy to tunnel the barrier above the Fermi level.

2.5.2 Ohmic Contact

Different from the Schottky contact, Ohmic contact is a non-rectifying contact. That means when metal and semiconductors make a contact, there is a negligible barrier in the interface, which allows current to pass through the interface with a small voltage drop compared to the drop across the whole device.[30] For a p-type semiconductor, ohmic contact happens when ϕ_m is greater than ϕ_s.

Figure 2.14 shows the band diagram of a p-type semiconductor before and after forming an ohmic contact. Because the work function of the metal is greater than that of the semiconductor, electrons in the semiconductor flow into the metal where there is a lower energy band, which leaves holes in the semiconductor and forms a holes accumulation layer in the interface, which makes it easier to transport electrons from the metal to the semiconductor. That is how ohmic contact forms on a p-type semiconductor, creating very small barrier for current travel.



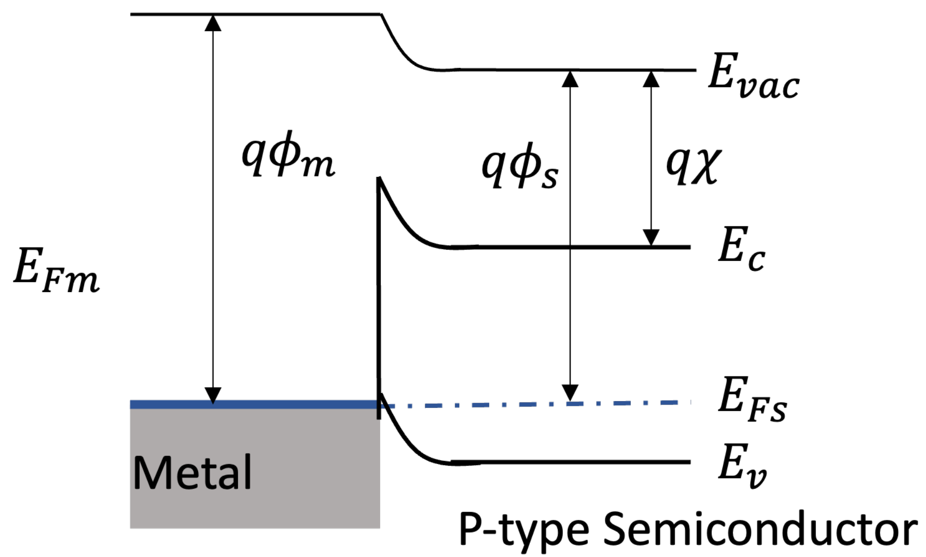


Figure 2.14: Band diagram of p-type semiconductor ohmic contact.
(a) before contact (b) after contact.

2.5.3 MOS Contact

Metal-Oxide-Semiconductor contacts plays a crucial role in MOSFET operation, which will be talked about in the next section. Figure 2.15 shows an ideal MOS structure. t_{OX} indicates the thickness of the oxide layer, and ε_{OX} is the dielectric constant of the oxide.

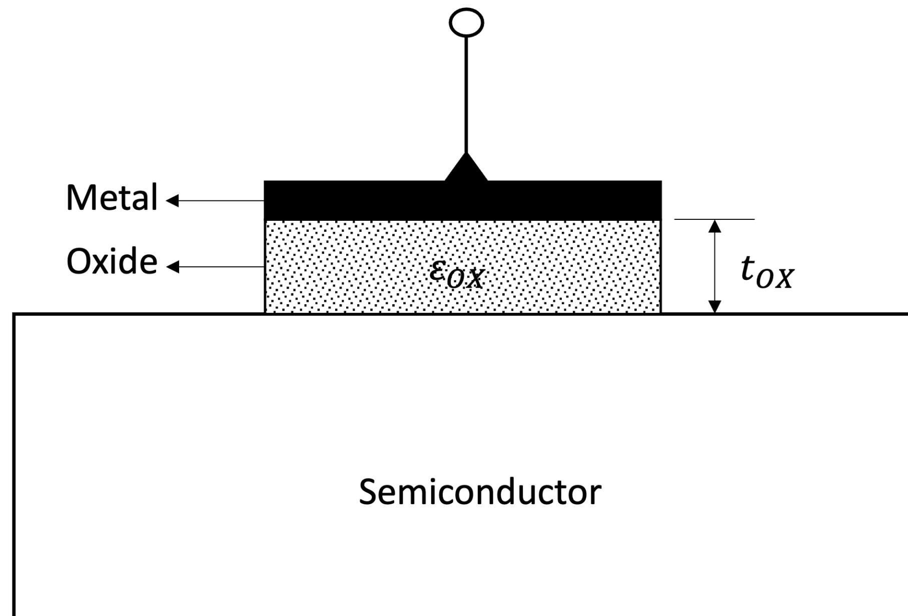


Figure 2.15: Ideal MOS Structure.

An ideal MOS contact can be treated as a parallel capacitor with the metal and semiconductor as upper and lower plates. If a p-type semiconductor is used, when a negative bias is applied on the metal side, an electric field point to the metal plate is created. When the electric field crosses through the semiconductor, the majority carriers (holes) in the semiconductor are pulled to the oxide-semiconductor interface. In the band diagram, a hole's accumulation layer is created near the oxide-semiconductor interface.

However, suppose a positive bias is applied to the metal gate. In that case, it will produce an electric field in the opposite direction to the electric field generated when a negative bias voltage is applied to the gate. That electric field repels holes away from the oxide-semiconductor interface and leaves ionised charges to form space charge region. When the applied bias increases, more negative charges are left near the oxide-semiconductor interface. The Fermi level is closer to the conduction band than valence, which means the semiconductor near the oxide-semiconductor region has been turned into n-type semiconductor.

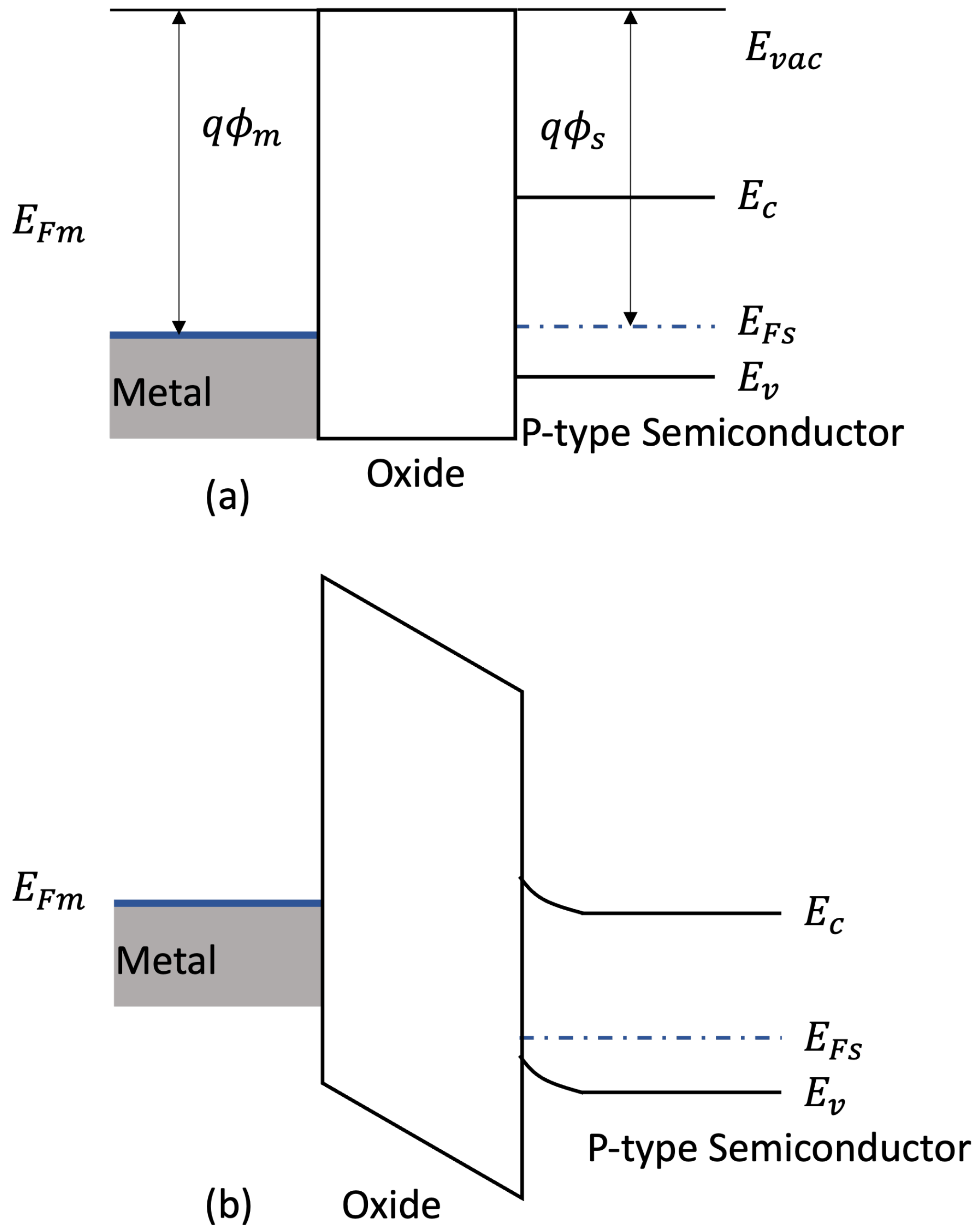


Figure 2.16: Energy band diagram of MOS contact.
(a) Ideal MOS energy band diagram when the semiconductor and metal work function is the same. (b) When a negative bias is applied to the metal gate.

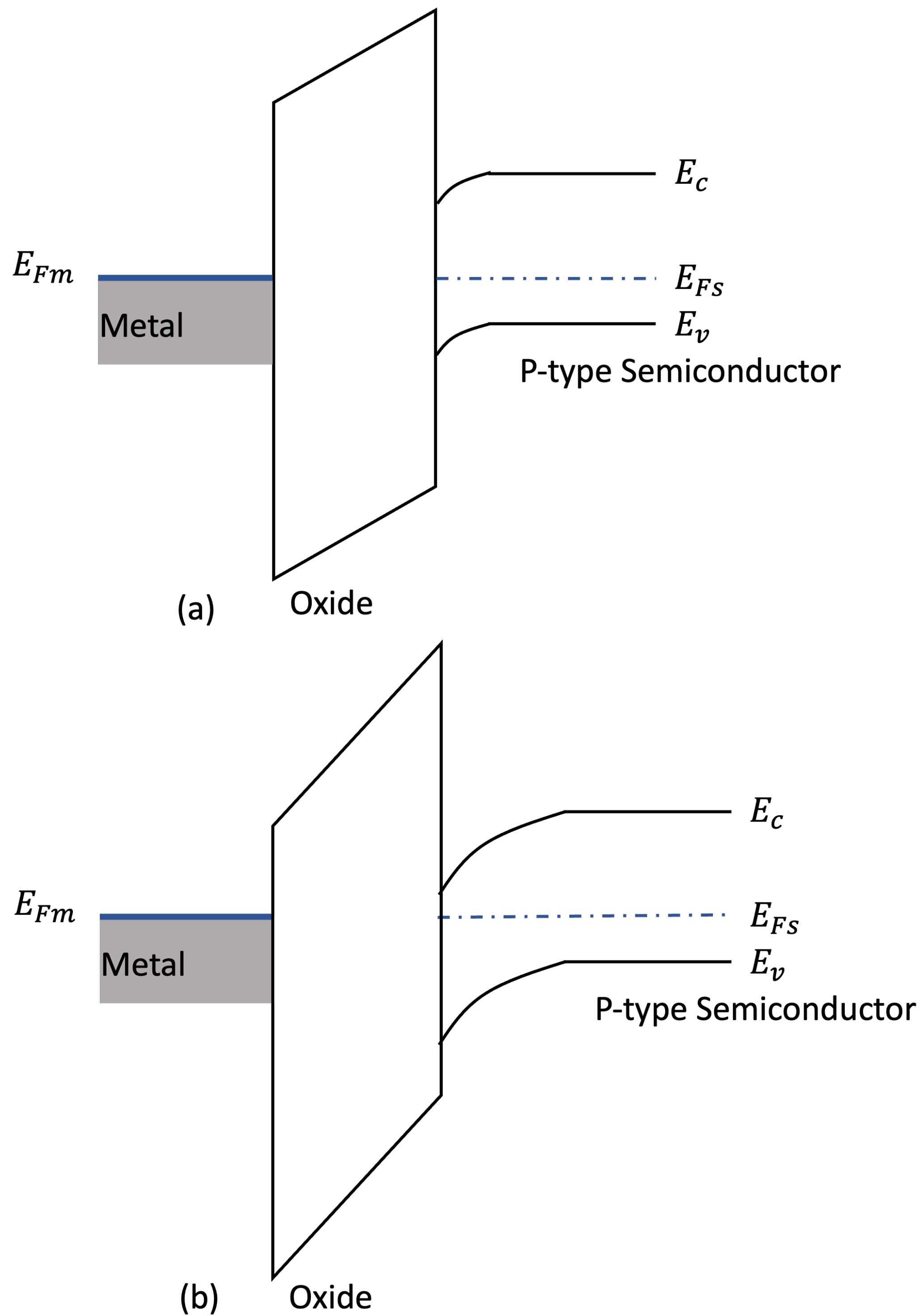


Figure 2.17: Energy band diagram of MOS contact.
(a) When there is a positive bias applied to the metal gate, space charge region formed (b) Keep increasing positive bias, a inversion layer forms near the oxide-semiconductor interface.

A MOS contact is used in FET devices to adjust the channel depth by changing the bias applied on the metal gate terminal to turn on and off the device.

2.6 Field Effect Transistor operation

A field effect transistor (FET) is a device that uses an electric field to control the current flow through a semiconductor material. In an FET, a voltage applied to the gate creates an electric field in the semiconductor, which controls the current flow between the source and drain terminals. There are several types of FETs, including junction field transistors (JEFTs), metal-oxide-semiconductor transistors (MOSFETs), and metal-semiconductor transistors (MESFETs). In this work, MOSFETs and MESFETs will be reviewed in detail.

2.6.1 MOSFET

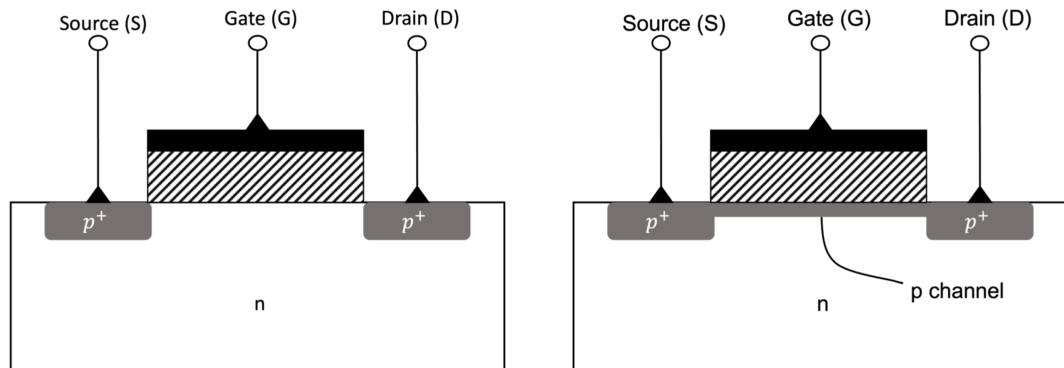


Figure 2.18: p-channel MOSFET cross section. Enhancement mode (left) and depletion mode (right).

A MOSFET contains three terminals source (S), gate (G), and drain (D). Depending on the channel types, MOSFETs are divided into n-channel (NMOS) and p-channel (PMOS). MOSFET is divided into enhancement mode and depletion mode depending on whether there is a channel under the gate terminal when no voltage is applied. For enhancement mode p-channel MOSFET (PMOS-enhancement), there is no channel between two highly doped p regions, which means the device is off when there is no voltage applied to gate terminal. A negative voltage applied to the gate (V_G) repels electrons doped in the substrate. When the bias is high enough, threshold voltage (V_{th}), an inversion layer of charge, a layer where the original minimum carries turns to the majority, forms under the gate terminal and performs as a channel to allow carriers to travel through the source and drain. However, in a depletion mode p-channel MOSFET (PMOS-depletion), a channel exists between the source and drain without bias on the gate terminal-a positive bias is required on the gate to repel holes in the channel and turn off the device.

When the MOSFET is in the on-state ($V_G > V_{th}$), a bias applied on the drain terminal can push the carriers to migrate between source and drain. Traditionally, the majority carriers are expected to travel from source to drain. With increasing the bias applied on the drain, FETs work under two regions. The first region is when a small bias is applied between the source and drain (V_{GS}). This

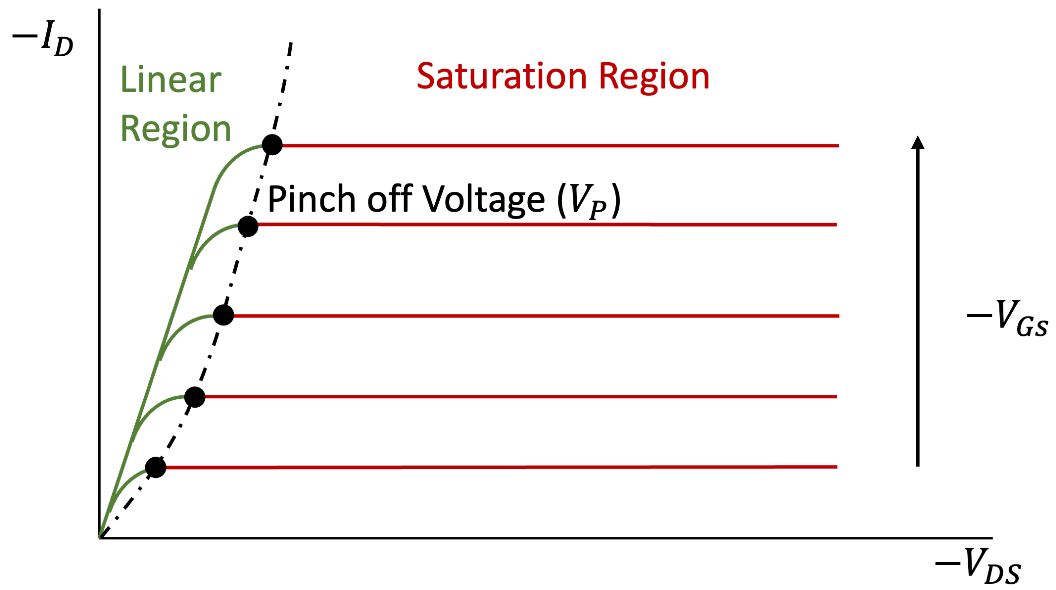


Figure 2.19: p-channel MOSFET I_{DS} - V_{DS} curve.

region is linear or ohmic region where drain current (I_D) increases proportionally to the increase of drain voltage because the channel behaves as a resistor. Equation 2.4 expresses the current in the linear region, and W and L are the width and length of the gate terminal, respectively. C_{ox} is the capacitor between the gate metal and semiconductor, and μ_p is the mobility of holes in the semiconductor.

$$I_D = \frac{W\mu_p C_{ox}}{2L}[2(V_{SG}+V_{th})V_{SD}-V_{SD}^2] \tag{2.4}$$

With drain bias increasing, at some point, the bias reaches saturation voltage (V_{sat}), where the thickness of inversion layer near drain terminal reduces to zero; that is called pinch-off point.

$$V_{SD(sat)} = V_{SG}+V_{th} \tag{2.5}$$

Beyond this point, the voltage keeps constant with drain bias increasing. That means the amount of carriers transported from the source is constant, and the current no longer changes with the drain voltage. This region is the saturation region.

$$I_{D(sat)} = \frac{W\mu_p C_{ox}}{2L}(V_{SG}+V_{th}^2) \tag{2.6}$$

Figure 2.19 shows the I_D and V_D curve under the ideal situation. The slope on the graph indicates the on-resistance (R_{on}) of the FET device. This resistance comprises a series of resistance that includes the contact resistance (R_c), channel resistance (R_a) and under gate resistance ($R_{undergate}$).

$$R_{on} = 2R_c + 2R_a + R_{undergate} \tag{2.7}$$

2.6.2 MESFET

Instead of using oxide to create a capacitor as the gate terminal, MESFET is a device fabricated with Schottky contact as the gate terminal. As mentioned in the previous section, due to the work function difference, the metal-semiconductor contact creates a depletion layer when the electrons in the metal diffuse into the semiconductor. Depends on if the depletion area can totally break the channel, MESFET can be divided into depletion mode, which is normally on at zero bias and enhancement mode, which is normally off at zero bias. The barrier thickness in the interface changes with the applied bias on the metal terminal. For a p-channel MESFET, a positive bias increases the barrier and allows less current to get through. For a depletion mode MESFET, the device can be turned off if the bias is big enough.

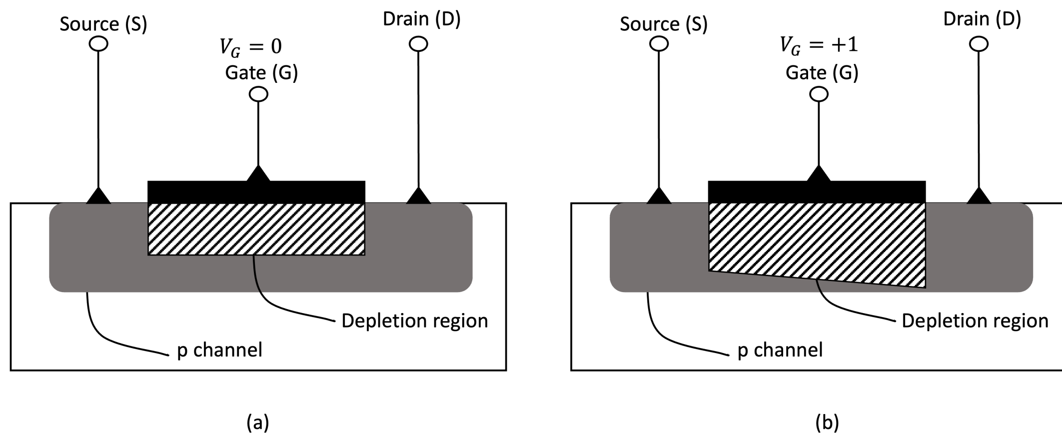


Figure 2.20: p-channel depletion mode MESFET with no bias and positive bias.

For a p-channel depletion mode MESFET, the working mode is similar to p-type MOSFET. When the bias applied on drain terminal is small, the device works on linear region. However, with the bias applied on the drain increase, the Schottky barrier on the drain side is more reversed-biased. When the bias is high enough, the depletion region on the drain side reaches the insulating substrate, and that is called pinch-off. Beyond this point, the current reaches the saturation current $I_{D(sat)}$ and no longer changes.

$$I_{D(sat)} = \frac{\mu_n \varepsilon_s W}{2L}(V_{GS} - V_T)^2 \tag{2.8}$$

2.7 Chapter Summary

This chapter briefly describes synthetic diamond and the advantages of using diamond as electronic device material over other wide band gap materials. Challenges of doping diamond have been introduced, and an institutional way, surface transfer doping, of applying diamond as an electronic devices is reviewed. In addition, fundamental theories of FET devices are discussed.

Chapter 3

Literature Review

Continuing from the previous chapter, this section delves deeper into surface transfer doping of diamond, providing in-depth insights and highlighting recent advancements in this field. Subsequently, it explores methods for hydrogen termination of diamond surfaces, introducing an alternative technique known as Spillover, which was employed in this study to hydrogenate the diamond surface. Following this, there is a review of contact metals on hydrogen-terminated diamond surfaces, aiming to elucidate the formation of ohmic contacts on diamond. Lastly, the chapter concludes with an exploration of the cutting-edge technology in the realm of diamond surface transfer doping Field-Effect Transistors (FETs).

3.1 Surface transfer doping

In the previous chapter, the challenges associated with utilizing boron or phosphorus doped diamond at room temperature was discussed, as well as alternative strategies like delta doping and surface transfer doping. However, due to the stringent precision demands of boron delta doping and the limited enhancements observed in p-type delta doping diamond, the practical applicability of this method is constrained. On the other hand, surface transfer doping shows greater promise for the fabrication of high performance diamond-based devices.

10The first experimentally observed surface transfer doping was reported in 1989 when Landstrss et al. measured a fairly low resistivity of $10^6\ \Omega \cdot cm$ on type IIa single crystal diamond without any impurity doping [51]. This value is much lower than that of diamond without hydrogen termination ($10^{16}\ \Omega \cdot cm$) [29]. This phenomenon was initially explained by the diffusion of hydrogen into the diamond to contribute as an acceptor state [52]. However, in 1990, Grot et al.[53] proposed that the hydrogen induced surface conductivity can be removed by chemical cleaning process which can only remove non-carbon contamination on the diamond surface.

This discovery contradicts the previously mentioned theory about the surface conductivity of hydrogen terminated diamond. Soon after this discovery, Junji et al.[54] reported that the Kelvin Probe measurement and X-Ray Photoelectron Spectroscopy shows evidence that electrons on hydrogen terminated diamond surface transferred into unknown acceptor states on the surface. It provided a strong evidence for a hole accumulation layer sitting below the hydrogen terminated diamond surface.

As discussed in the previous chapter that hydrogen terminated diamond surface exhibits negative electron affinity (NEA), and this property can be used to verify if the surface termination on diamond has been changed. Negative electron affinity on hydrogen terminated diamond was first observed by Himpsel et al.[55] in 1979 with observation of excited electrons when the photons energy is lower than that of theoretical prediction.

In 2000, with the help of NEA, Maier et al.[43] proposed a series of experiments verifying a few crucial facts about the surface conductivity of hydrogen terminated diamond. In their experiment, a hydrogen terminated diamond is kept in an ultra-high vacuum (UHV) system and experienced high temperature annealing. With in-situ measurement, the surface conductivity is observed to drop after annealing, while the measured negative electron affinity (NEA) confirms the existence of hydrogen termination on the diamond surface. Following the experiment, half of the sample surface is protected, with the other half exposed to electron beams aiming at removing hydrogen termination. The measurement of electron affinity confirms that the protected surface remains the termination; however, the half exposed to electron beams loses the termination. After exposing the sample to air for three days, the protected half regains the surface conductivity, while the part exposed to electron beams remains highly resistive. They indicate that the surface conductivity of hydrogen terminated diamond not only comes from the hydrogen termination, but also caused by the air adsorbates acting as acceptor. Because the lowest unoccupied molecular orbitals of the air adsorbates are below the valence band top of the hydrogen terminated diamond, electrons transfer from the diamond to the surface and show surface conductivity, and this process is governed by the following redox reaction,

$$2H_3O^+ + 2e^- \rightleftharpoons H_2 + 2H_2O \quad (3.1)$$

Later experiment carried by other groups proposed that oxygen-ion are responsible for the surface conductivity of hydrogen terminated diamond [56]–[58]. Back to 1999, Gi et al.[59] reported that the surface resistivity of hydrogen terminated diamond decreases when the sample is exposed to NO_2 flow. Following this report, many groups proposed NO_2 induced surface conductivity on the hydrogen terminated diamond surface. Until 2013, the lowest NO_2 induced sheet resistance of hydrogen terminated diamond, 719 $\Omega/\Box$, was reported by Sato et al.[10].

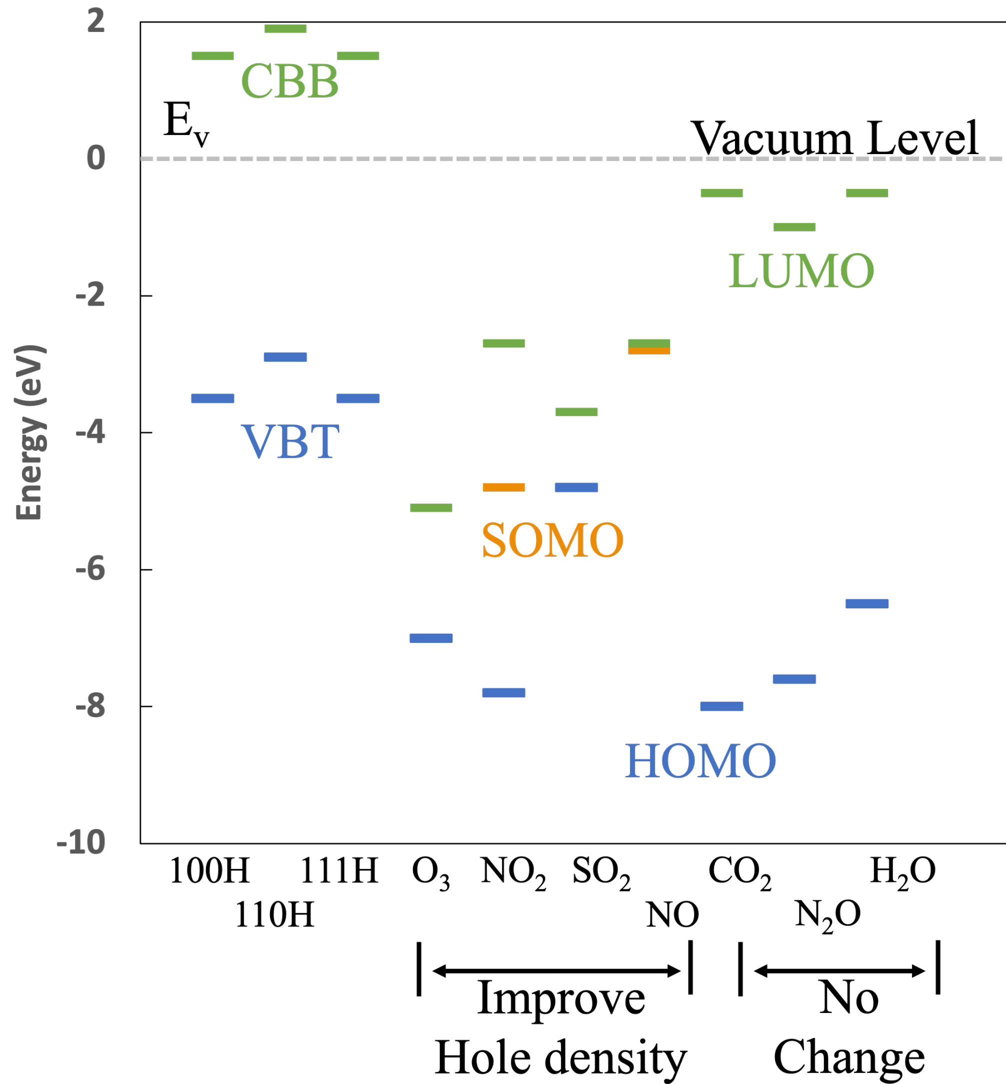


Figure 3.1: Energy levels of various molecular orbitals and H-diamond with different surface orientation [44].

In 2013, Takagi et al.[60] conducted a detailed investigation on the transfer capability of various of airbone species on H-diamond based on experimental results and first-principles calculations. Their report indicates that the airbone species such as NO_2, SO_2, NO and O_3, with lowest unoccupied molecular orbitals (LUMO) below or near the valence band top (VBT) contributes to the surface conductivity. However, airbone species such as CO_2, N_2O and H_2O, with LUMO higher than the VBT of diamond has little or no effect on surface conductivity. This was later verified by Kubovic et al.[56], who reported that samples exposed to O_3 lead to the largest increase of carrier concentration and exhibited good stability.

With these early experiments, the mechanism of high surface conductivity on H-diamond becomes clearer. Airborne adsorbates play crucial roles in this process, and molecules with LUMO near the VBT of H-diamond act as electron acceptors that can improve surface conductivity.

Additionally, metal oxides are explored to improve both the stability and conductivity of H-diamond. In 2013, Russell et al.[61] reported a boost in surface carrier concentration with MoO_3 deposition on H-diamond. In 2014, Tordjman et al. [49] reported the same MoO_3-induced effect on H-diamond, with carrier densities up to $1 \times 10^{14}\ cm^{-2}$. Both experiments indicate that MoO_3 acts as an electron acceptor, with the conductance band minimum situated below the valence band maximum of H-diamond. The migration of electrons from H-diamond to MoO_3 drives the energy band of H-diamond upward, forming a hole accumulation layer near the surface of H-diamond.

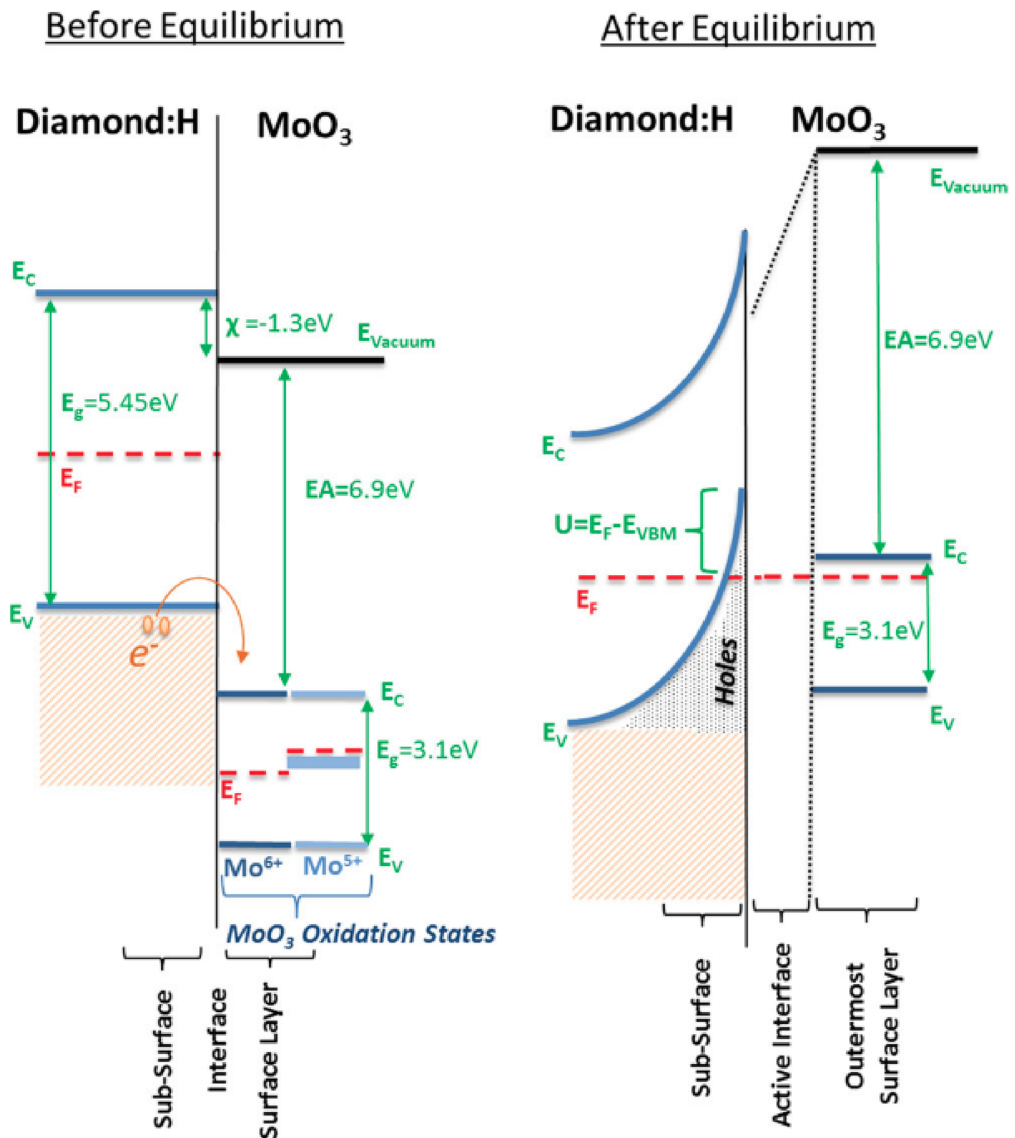


Figure 3.2: Band diagram of MoO_3/H-diamond before and after thermal equilibrium [49].

This work demonstrates the potential of applying metal oxides with high electron affinity (EA) to act as acceptors and improve the surface conductivity of H-diamond. Transition metal oxides such as ReO_3, WO_3, V_2O_5, Nb_2O_5, and CrO_3 have been reported following the success of MoO_3 [45], [46], [48], [50]. In Verona et al.'s report, the sheet resistance of samples covered with transition metal oxide is only around one-tenth of that of samples exposed to air. Additionally, the carrier concentration of samples covered with transition metal oxide is ten times that of air-exposed samples. High-temperature stability is also reported up to 300 °C with V_2O_5 and MoO_3 coverage [45], and up to 400 °C for ReO_3 covered samples [48].

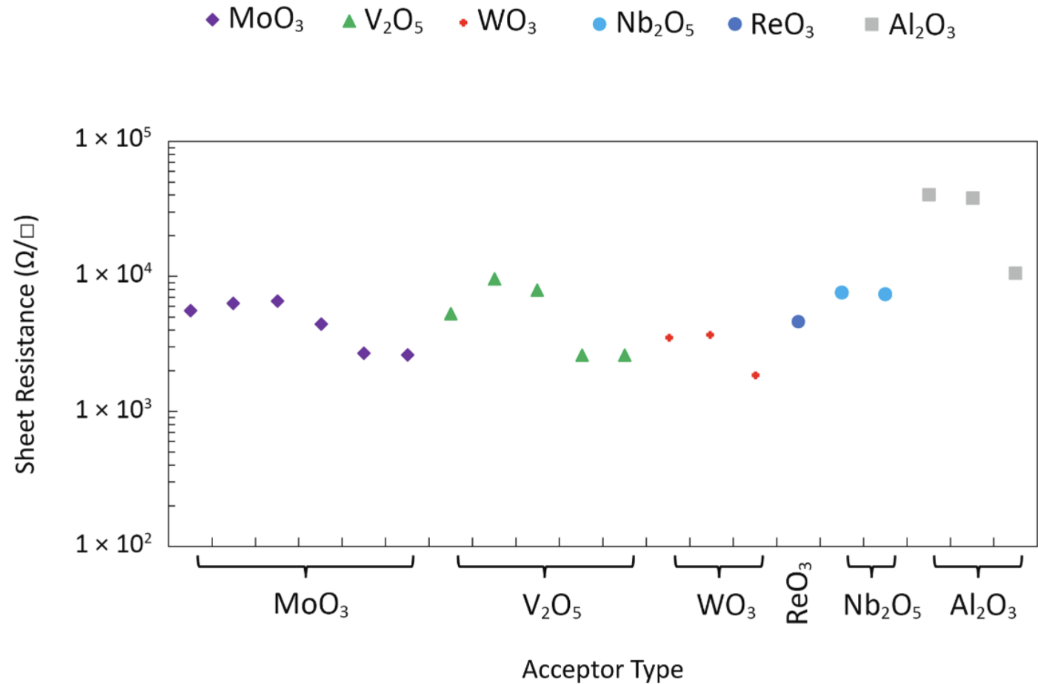


Figure 3.3: Sheet Resistance of H-diamond with and without transition metal as surface acceptor[62].

Transition metal oxides have been reported to improve the surface conductivity and thermal stability, making them ideal materials for encapsulating H-diamond devices. However, another group of materials, high dielectric constant materials, has drawn attention from researchers. Hiraiwa et al. [63] reported that the use of Al_2O_3 can encapsulate and stabilize the surface conductivity of H-diamond surfaces. In 2016, Verona et al. [50] compared the thermal stability of H-diamond with or without oxide protection. Their results show that the surface conductivity of air-exposed H-diamond drops drastically between 25 °C and 300 °C, whereas the surface conductivity of H-diamond with high work function oxide protection or Al_2O_3 protection can remain stable up to 250 °C and 400 °C, respectively. Kawarada et al. [64] also reported that the surface stability of H-diamond depends on the deposition temperature of Al_2O_3, and they reported a device that remains stable up to 400 °C with Al_2O_3 deposited under 450 °C.

Figure 3.4 illustrates the electron affinities of various materials compared to the band diagram of diamond with different terminations. As previously discussed, the conduction band minimum (CBM) of all transition metal oxides is situated below the valence band maximum (VBM) of hydrogen-terminated diamond, allowing them to act as electron acceptors. However, high dielectric materials, such as Al_2O_3, have their CBM situated above the VBM of H-diamond, indicating that Al_2O_3 should theoretically be unable to contribute to the surface conductivity of H-diamond. Nonetheless, Al_2O_3 has been found to improve the surface conductivity of H-diamond, but only when deposited by Atomic Layer Deposition (ALD).

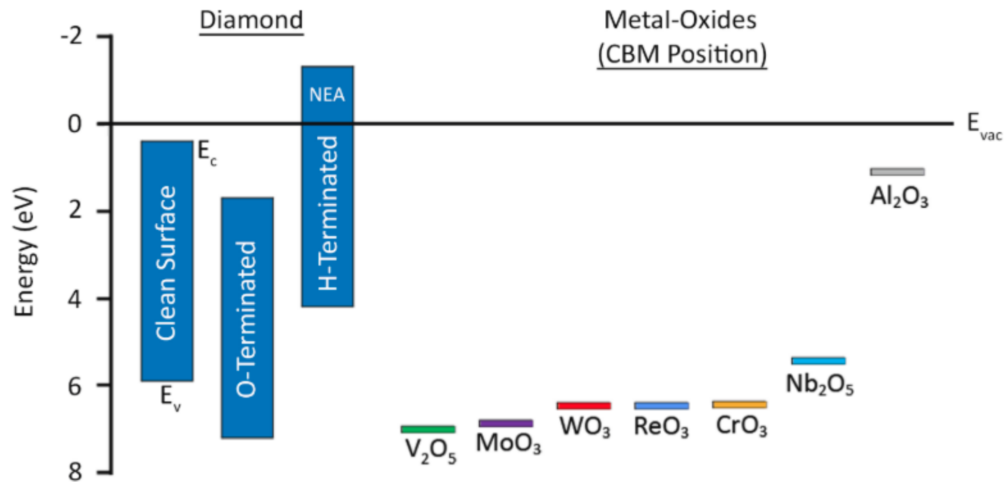


Figure 3.4: Electron affinities of different metal oxides compared to the bandgap of diamond with no termination, oxygen termination and hydrogen termination[62].

In 2012, Kawarada et al. [65] demonstrated that H-diamond with Al_2O_3 deposited by ALD on the surface does not require air exposure to achieve surface conductivity. Soon after, they proposed that unoccupied energy levels may exist in Al_2O_3, situated below the VBM of H-diamond [66]. Later, using XPS, Ren et al. [67] observed a large band offset of 3.3 eV between the H-diamond and Al_2O_3 interface. They also suggested the presence of interstitial aluminium and oxygen vacancy defects, which act as electron acceptors. Currently, all reports of Al_2O_3-improved conductivity on H-diamond surfaces have been accomplished by atomic layer deposition (ALD) technique. In contrast, Verona et al. [50] utilized electron beam deposition of Al_2O_3, however, the sheet resistance of H-diamond increased to 38.6 $k\Omega/\square$, which is more than two times the sheet resistance before deposition.

In conclusion, the mechanism behind the conductivity of H-diamond has been investigated over the past several years. The most convincing explanation is that air adsorbates on the surface act as electron acceptors and create a hole accumulation layer on the diamond surface. Subsequent studies have also explored other materials, such as high electron affinity materials and high dielectric constant materials, to substitute air adsorbates in order to improve conductivity as well as stability.

3.2 Diamond surface hydrogen termination

Diamond surfaces can be hydrogen-terminated using various methods. As discussed in the previous chapter, diamond can be grown using the chemical vapor deposition (CVD) method, where hydrogen and hydrocarbons serve as precursors and act as the source of hydrogen termination. Nowadays, the most popular and optimized method for diamond growth and in-situ hydrogen termination is microwave plasma-enhanced chemical vapor deposition (PCVD) [68].

Ex-situ plasma-assisted hydrogen termination methods are widely used in research areas. In this method, oxygen-terminated diamond is exposed to hydrogen plasma in a vacuum chamber with temperatures ranging between 500 °C and 800 °C [69], [70]. Although this method can complete hydrogen termination in a few minutes, the roughness of the diamond surfaces varies depending on factors such as the power of the plasma, chamber temperature, time, and other parameters. In Crawford's work [71], atomic force microscopy (AFM) measurements showed that the surface roughness of diamond samples increased after the hydrogen termination process, with roughness worsening at higher plasma powers. In 2011, Philip et al. [70] observed that longer durations of hydrogen plasma smoothed the diamond surface. They did not observe hydrogen plasma etching pits reported in Crawford et al.'s work with this prolonged plasma treatment. However, this effect was only observed after 2 hours of treatment. With properly set parameters, one can modify the diamond surface to achieve a smooth hydrogen-terminated surface using ex-situ plasma-assisted methods [72].

Thermal hydrogenation is another method for hydrogenating diamond surfaces. In 1993, Ando et al. [73] achieved hydrogenation on oxygen-terminated diamond surfaces. The experiment was conducted under atmospheric pressure and high temperatures (below 900 °C), with pure hydrogen flowing through the chamber for several hours. A similar experiment was carried out in 2013 by Seshan et al. [74], where hydrogen-terminated diamond was obtained with pure hydrogen flow at 800 °C. These experiments reveal the possibility of thermally hydrogenating diamond. Earlier than these two reports, Pate et al. hydrogenated diamond surfaces with hydrogen atoms rather than molecular atoms [75]. In their experiment, a heated tungsten filament (1800 °C) was used to generate atomic hydrogen and terminate the diamond surface. High-resolution electron energy loss spectroscopy (HREELS) and photo-stimulated ion desorption (PSID) results revealed a diamond surface with hydrogen termination after exposure to atomic hydrogen under ultra-high vacuum.

Diamond surface hydrogenation has been well studied in the past several years. Ex-situ plasma-assisted hydrogenation methods contribute to achieving a good hydrogen-terminated diamond surface. In addition, thermal hydrogenation with molecular or atomic hydrogen also shows good potential for terminating diamond surfaces with hydrogen.

3.3 Spillover mechanics

Spillover refers to a process where H_2 molecules are dissociated by a metal catalyst, such as Pt and Pd, into H atoms, and these H atoms migrate on the contact support materials [76]. The essence of this process lies in the interaction between active hydrogen atoms and the support materials, wherein hydrogen migrates from the hydrogen-rich phase to a hydrogen-poor phase.

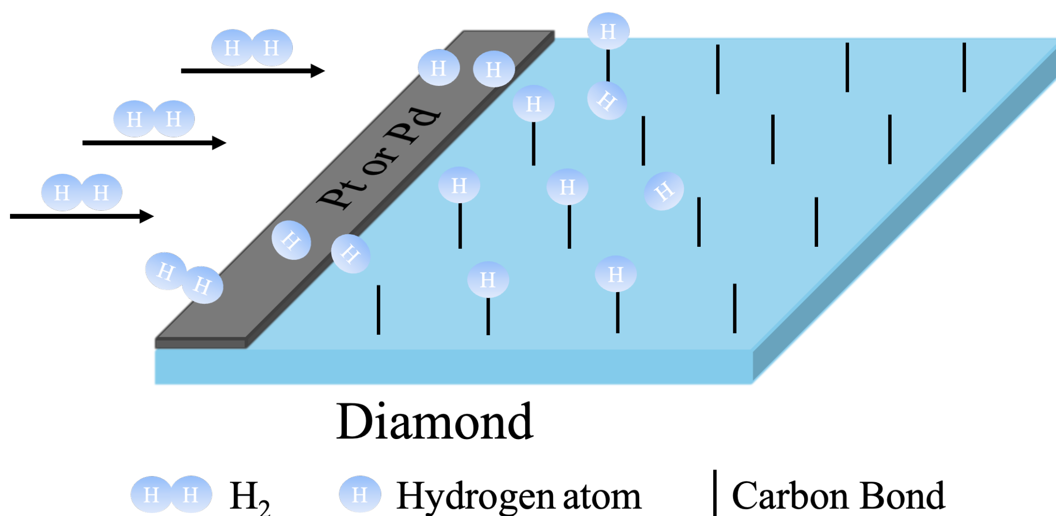


Figure 3.5: Hydrogen spillover process.
Catalytic metal (Pd or Pt) dissociation of the hydrogen molecule into atoms those migrate to the non-metallic support surface (diamond). [77].

In 1964, Khoobiar reported that yellow WO_3 is reduced by H_2 to blue WO_{3-x} when Pt is used as a catalyst [78]. This phenomenon was explained as the dissociative chemisorption of H_2 molecules on the Pt surface, followed by migration of the resulting H atoms to the yellow WO_3 particles, leading to their reduction to blue WO_{3-x}. Soon after, Boudart et al. coined the term "spillover" to describe this process, wherein dissociated H atoms diffuse from the metal catalyst to support materials such as carbon-based materials and TiO_2 [79]. Recent research on spillover has shown that the proton-electron pairs formed by H atoms can migrate onto support materials such as MoO_3 [80], [81].

In 2010, Triwahyono et al. conducted a study on the kinetics of hydrogen adsorption over Pt/MoO_3. Their results showed that H atoms are formed when H_2 passes through the catalyst metal, such as Pt, rather than on the surface of the support material (MoO_3). Subsequently, the electrons reduce the reducible cations of MoO_3, while the protons bind to the surface oxygen anions [82].

Hydrogen spillover onto reducible materials such as TiO_2, WO_3, and CeO_2 has been well studied and confirmed [83]–[85]. In 2017, Karim et al. conducted a series of experiments and verified that spillover occurs on reducible support materials such as TiO_2 irrespective of the distance.

However, on non-reducible materials such as Al_2O_3, this effect is barely detectable when the distance between the catalyst metal and the oxide is increased [86].

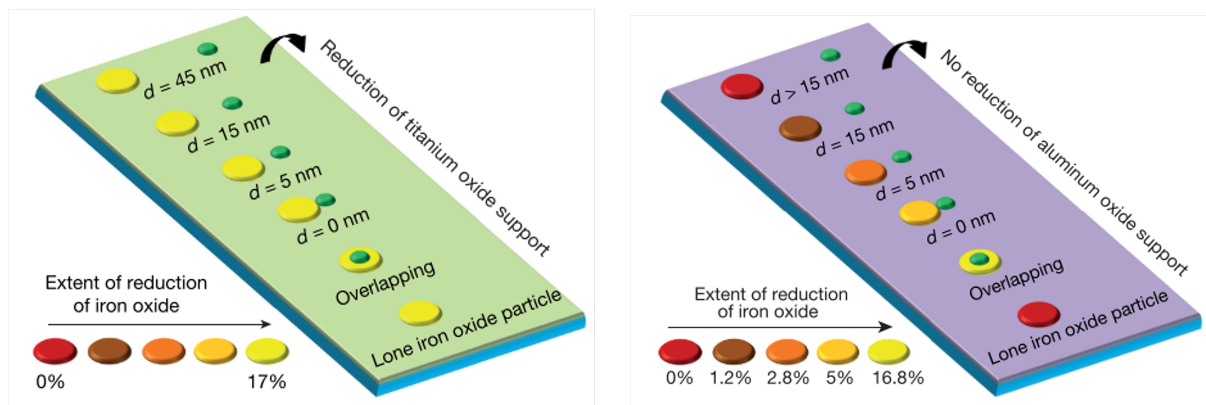


Figure 3.6: Hydrogen spillover on different support material.
Left, diagram of reduction grade on reduction support material TiO_2. Right, diagram of reduction grade on non-reduction support materials Al_2O_3. The green dots is the catalyst metal Pt in both images [86].

The spillover phenomenon on non-reducible support materials remains controversial. Despite reports in recent years about hydrogen spillover on non-reducible support materials such as Al_2O_3 and SiO_2, the process is energetically unfavorable [87], [88]. In order for hydrogen spillover to occur onto the support material, a new bond between hydrogen atoms and support materials with energy similar to that of the metal-hydrogen bond is required. However, non-reducible materials cannot form this bond with hydrogen atoms [76]. The observed hydrogen spillover on non-reducible materials has also been explained as being due to defects on the material surface contributing to the breakdown of the metal-hydrogen bond [89].

Spillover on carbon-based materials is also energetically unfavorable. The calculated $C-H$ binding energy is approximately 0.8 eV, which is smaller than that required to break the metal-hydrogen binding, such as the 3.8 eV bond energy in the case of $Pt-H$ binding [90]. This means that hydrogen atoms on the metal surface cannot migrate to the surface of carbon-based materials. However, this only applies to carbon-based surfaces without defects. If defects exist on the material surface, one can expect hydrogen atoms to migrate from the metal surface to unsaturated carbon-based materials to form $C-H$ bonds. In 2003, Mitchell et al. reported that $C-H$ bonds form on carbon edge sides where free dangling bonds are observed before the spillover process [91]. This supports the theory that spillover can occur on carbon-based surfaces with free dangling bonds.

When it comes to the hydrogenation of diamond surfaces, the surface can first be oxidized with an acid cleaning process, which will be discussed in the next chapter. Then, defects, or free dangling carbon bonds, can be created by heating the oxygen-terminated diamond under vac-

uum. The temperature required to desorb the oxygen on the (100) diamond surface is reported to be 600 °C [92]. With free dangling carbon bonds exposed, hydrogen atoms dissociated by transition metals such as Pd and Pt are able to migrate to the diamond surface and form $C-H$ bonds, thus hydrogenating the diamond surface.

Hydrogen spillover has been detected on both reducible materials and non-reducible materials with defects on the surface. To make the process energetically possible for carbon-based materials, free dangling carbon bonds are required for the migration of hydrogen atoms dissociated by catalyst metals. These findings provide theoretical support for hydrogen-terminated diamond surfaces via thermal spillover processes.

3.4 Contact metal on hydrogen terminated diamonds

In the previous chapter, we introduced the metal-semiconductor interface. In this section, we will delve into the metal-hydrogen-terminated diamond contact to review the metal contacts used in device fabrication.

As discussed previously, to form an ohmic contact on a p-type semiconductor, a metal with a work function (ϕ_m) greater than that of the semiconductor (ϕ_s) is desirable. This allows electrons from the semiconductor to flow into the metal, bending the semiconductor's band and forming an accumulation area at the interface to facilitate easy current flow. Au has been the most commonly used ohmic metal for hydrogen-terminated diamond due to its high work function. Reported lowest contact resistance formed by Au on H-diamond is 0.9 $\Omega \cdot mm$ [93]. Contact resistance reported by other groups varies from 3 $\Omega \cdot mm$ to 5 $\Omega \cdot mm$ [94]–[96]. Additionally, metals with high work functions like Pd have also been explored for use as ohmic contact metals, with reported contact resistance as low as 0.42 $\Omega \cdot mm$ [97].

To form Schottky contacts on hydrogen-terminated diamond, a metal with a lower work function is used. This allows electrons in the metal to migrate into the hydrogen-terminated diamond, forming a depletion area and creating an energy barrier to hinder electron transfer when the junction is reverse biased. Metals like Al, Pb, Zn, and Ti have been reported to form large Schottky barriers on hydrogen-terminated diamond surfaces [98]. The extrapolated Schottky barrier heights vary from 0.58 eV to 0.39 eV.

3.5 Field Effect transistors

As discussed in the previous chapter, hydrogen-terminated diamond (H-diamond) exhibits great potential for applications such as high-power, high-frequency, and high-temperature metal-oxide-semiconductor field-effect transistors (MOSFETs). Despite its limitations in thermal sta-

bility, appropriate passive layers and surface carrier acceptors can significantly improve both the thermal stability and conductivity.

The first hydrogen-terminated diamond FETs were demonstrated by Kawarada et al. in 1994 [99]. In their experiment, a chemical vapor deposition (CVD) grown hydrogen-terminated (100) diamond was used as the substrate. Low work function Al and high work function Au were utilized to form Schottky and ohmic contacts, respectively. With a gate length of 10 μm, this device achieved a highest drain current of 1.6 mA/mm and a highest transconductance of 200 $\mu S/mm$. To fully turn off the device, the gate length was increased to 40 μm. However, this resulted in a drop in drain current to 0.14 mA/mm and transconductance to 20 $\mu S/mm$. Following this pioneering device, subsequent devices with adapted geometry and improved surface conditions were fabricated.

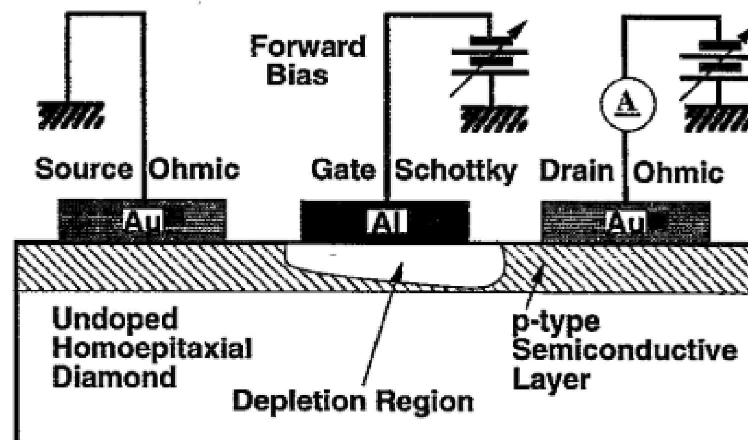


Figure 3.7: Structures of first H-diamond MESFETs[99].

Russell et al. demonstrated a metal-semiconductor field-effect transistor (MESFET) with Al as the Schottky contact in 2012 [96], with the gate length reduced to 50 nm. They achieved a maximum drain current exceeding 295 mA/mm with a transconductance of 78 mS/mm. However, the measured leakage current reached up to 0.02 mA/mm.

In contrast to using metals with low work function for Schottky gate contacts, devices with gate dielectric layers insulators were fabricated to create a metal-insulator-H-diamond interface, aiming to improve breakdown voltage potential, reduce leakage current, and enhance surface termination stability. Transition metal oxides have been utilized to improve the surface conductivity of hydrogen-terminated diamond by acting as electron acceptors. In 2016, Verona et al. reported metal-insulator-semiconductor field-effect transistors (MISFETs) on hydrogen-terminated diamond with V_2O_5 as the gate dielectric [100]. They observed stable surface conductivity of hydrogen-terminated diamond up to 200 °C, and at room temperature, the surface conductivity remained stable after 30 days of air exposure. Additionally, the maximum drain

current extracted from MISFETs with a gate length of 2 μm was 280 mA/mm, which was 80 mA/mm higher than the MESFETs with the same gate length. However, the gate leakage current of 40 μA was even higher than that of the previously discussed MESFETs [96].

In 2017, Ren et al. demonstrated the first hydrogen-terminated MOSFETs with MoO_3 as the insulator layer [101]. The maximum drain current for a gate length of 4 μm was 33 mA/mm. However, the breakdown voltage (roughly 2 V) was relatively low and might restrict the maximum current. Moreover, the leakage current of the device with 10 nm of MoO_3 was similar to that of the same devices with 3 nm of Al_2O_3, indicating that a higher thickness of transition metal oxide is required to restrict the drain leakage.

Crawford et al. reported the highest drain current of 700 mA/mm for FETs with a 50 nm gate fabricated on hydrogen-terminated diamond [93]. Instead of using V_2O_5 as the insulator layer under the gate, the oxide was used to encapsulate the entire device. However, the device suffered from drain-induced barrier lowering and thus poor off-state performance.

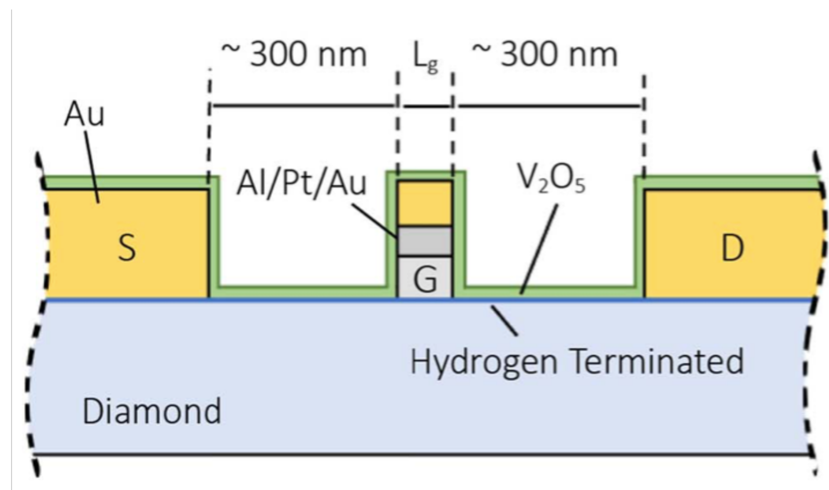


Figure 3.8: Structures of Crawford demonstrated FETs[93].

In summary, the utilization of transition metal oxides as dielectric materials to enhance the surface conductivity of hydrogen-terminated diamond and improve device properties requires further investigation. Reported metal-insulator-semiconductor field-effect transistors (MISFETs) with transition metal oxides as the insulator layer exhibit limited improvement and suffer from similar leakage issues as metal-semiconductor field-effect transistors (MESFETs) devices.

Another group of oxides with high dielectric constants, such as Al_2O_3, SiO_2, TiO_2, and HfO_2, have been explored as gate dielectric materials. Hydrogen-terminated diamond metal-oxide-semiconductor field-effect transistors (MOSFETs) with SiO_2 as the dielectric material were first demonstrated in 1999 [102]. However, the maximum drain current achieved with this device was only 18 mA/mm, significantly lower than that reported for hydrogen-terminated MESFETs

and MISFETs with transition metal oxides as the dielectric.

In 2013, Liu et al. demonstrated normally-off diamond MOSFETs with HfO_2 as the gate dielectric, showcasing low leakage drain current, indicating the potential of using high dielectric materials to mitigate drain leakage issues. The maximum drain current of 37.6 mA/mm also represented an improvement compared to the first MOSFETs built with SiO_2.

Among the mentioned materials, Al_2O_3 is the most popular and widely used one as both a dielectric layer and channel passivation layer. Hirama et al. illustrated a MOSFET with alumina gate insulator in 2007 [103]. Their device featured a 3 nm layer of aluminum deposited on the gate position, followed by self-oxidation of this metal layer to form Al_2O_3. Subsequently, aluminum was deposited on the oxide to form the gate stack. The measured maximum drain current of 790 mA/mm and an I_{on}/I_{off} ratio of 10^9 demonstrated a drastic improvement compared with MESFETs.

In 2019, Yu et al. demonstrated a T-shaped gate with atomic layer deposition (ALD) Al_2O_3 as the dielectric layer [104]. In this device, thermal-assisted ALD was utilized to grow Al_2O_3 as the dielectric layer under a 90 °C to reduce the leakage current. The final DC measurements of the device showed a maximum drain current of 703 mA/mm and a gate leakage current as low as 0.6 nA/mm.

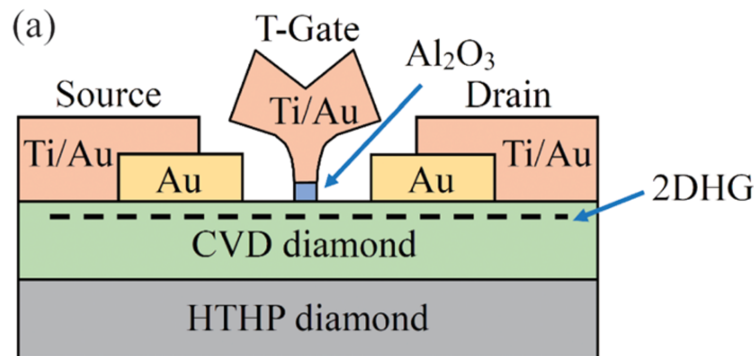


Figure 3.9: Cross section of T-shaped gate MOSFETs[104].

To mitigate off-state leakage current and enhance the breakdown voltage, various high-dielectric materials have been tested on hydrogen-terminated diamond, including multi-layer dielectric structures such as $HfSiO_4/Al_2O_3$, ZrO_2/Al_2O_3, $LaAlO_3/Al_2O_3$, and YSZ/Al_2O_3 [105]–[108]. However, a common issue among all these reported devices is the low drain current ($\leq$ 20 mA/mm). The highest drain current achieved with passivation was reported in 2012 [109]. By exposing hydrogen-terminated diamond to NO_2, Hirama et al. demonstrated a MISFETs using Al_2O_3 as passivation with a maximum drain current of 1.35 A/mm, which remains the highest recorded drain current thus far.

Due to the intrinsic properties of air-exposed hydrogen-terminated diamond, most of the demonstrated devices discussed above are "normally-on" devices. However, for applications requiring minimized off-state leakage current and improved device properties under high-power usage, "normally-off" hydrogen-terminated diamond devices are more desirable. High-dielectric materials are effectively used to create a larger energy barrier to reduce gate leakage and achieve "normally-off" FETs on hydrogen-terminated diamond. Nevertheless, the low drain current limits the applications of these devices. Other strategies, such as partially oxidizing the hydrogen-terminated surface, have been reported to fabricate "normally-off" devices, but the maximum drain current achieved was only recorded as 21 mA/mm [110]. To achieve higher drain current and "normally-off" devices on hydrogen-terminated diamond, further exploration of additional methods is necessary.

3.6 Chapter Summary

The chapter provides a comprehensive literature review covering several key aspects related to diamond surface transfer doping, hydrogen termination methods, spillover mechanisms, contact metals, and the development of diamond surface transfer doping field-effect transistors (FETs).

Surface transfer doping emerges as a promising approach to enhance diamond surface conductivity by introducing hydrogen and other acceptor materials. Various methods, including ex-situ plasma-assisted hydrogenation and thermal hydrogenation, are explored for hydrogen termination of diamond surfaces, aiming to improve their electrical properties.

Spillover mechanisms, extensively studied, elucidate the migration of hydrogen atoms from metal catalysts to support materials, including diamond surfaces. This understanding is crucial for optimizing spillover processes and enhancing surface conductivity.

In terms of contact metals, investigations focus on forming ohmic contacts using metals like Au and Pd, as well as forming Schottky contacts using metals such as Al, Pb, Zn, and Ti. Understanding the properties of these contacts is essential for device fabrication and performance optimization.

The development of diamond surface transfer doping FETs represents significant progress in utilizing diamond for electronic applications. Various device configurations and dielectric materials are explored to improve device performance and stability. However, challenges persist in achieving low gate leakage current and high maximum drain current for practical applications.

Overall, the literature review provides valuable insights into the current state and future directions of research in this field, highlighting both advancements and remaining challenges.

Chapter 4

Fabrication

The scaling of electronic devices to nanometre dimensions necessitates advanced fabrication techniques, which become increasingly challenging when working on a diamond substrate with processing-sensitive hydrogen termination on the surface. This chapter introduces the fabrication processes and techniques established in this work.

The chapter commences with the preparation of diamond samples, encompassing the cleaning and surface hydrogenation. Subsequently, it introduces and compares in detail two of the most important lithography techniques: photolithography and e-beam lithography. Metal contacts on the sample surface are formed through physical vapour deposition and wet etching, both of which will be reviewed in this chapter. Additionally, two techniques, atomic layer deposition (ALD) and e-beam evaporation, employed to deposit the oxide layers, will be introduced in detail. To protect the surface, various alternative fabrication processes are explored, with the results of those alternative fabrication processes discussed. Finally, the chapter concludes with the discussion of a customised fabrication process for diamond FET devices.

4.1 Sample Preparation

A clean and uncontaminated material surface is essential for nanofabrication, particularly for fabrication on hydrogen-terminated diamond surfaces, as the device performance strongly depends on the surface quality and cleanliness. A rough surface with defects increases the trapped charge and scattering mechanics, thereby decreasing the carrier mobility[111], [112]. The initial step in creating a device on a diamond surface involves smoothing the surface and reducing surface defects.

4.5 $mm \times 4.5\ mm$ CVD grown (100) single crystal diamond samples were purchased from Element Six with surface roughness between 2 nm to 7 nm. To smooth the surface down to the

sub-nanometer scale, samples were sent to Technical Diamond Polishing for scaif polish. AFM is used to measure the surface roughness before and after polishing. Table 4.1 represents the AFM measurement results of 5 samples before and after polishing.

Surface Roughness	Sample 1	Sample 2	Sample 3	Sample 4	Sample 5
R_q Before Polish(nm)	1.32	3.72	2.4	1.98	3.05
R_q After Polish(nm)	0.71	0.86	0.44	0.65	0.31

Table 4.1: Samples surface roughness R_q before and after scaife polish. Data measured with AFM in 5μm scanning size.

Figure 4.1 shows the AFM results of the sample surface before scaife polishing. As these samples are recycled from previous experiments, the surface is in poor condition, with etch pits and scratches clearly visible.

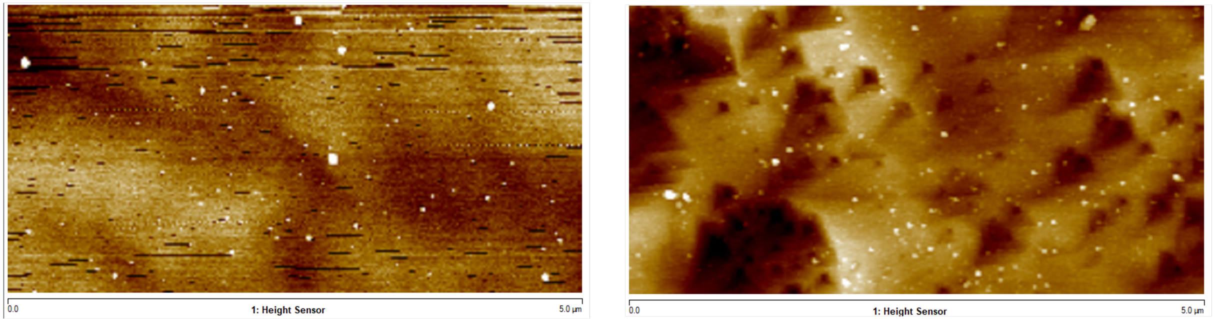


Figure 4.1: AFM scan results of sample surface before polish.

Figure 4.2 depicts the AFM results of the sample surface after scaife polishing, revealing a reduction in surface roughness R_q from a few nanometers to sub-nanometer level. Additionally, the polish grains are observable post-polishing. It is noteworthy that a few white dots persist on the sample surface after scaife polishing. These white dots, observed with AFM, are presumed to be contamination remnants from the polishing process. Subsequently, acid cleaning and solvent cleaning are employed to terminate the surface with oxygen and eliminate the contamination.

To eliminate metal trace contaminants and accumulated hydrocarbon and oxygenated compounds from the sample surface, a two step acid cleaning process was carried out after the polish. The initial step involves immersing the diamond samples in boiled Aqua Regia (a $1:1$ mixture of HNO_3 and HCl) for 15 minutes. Subsequently, the samples were rinsed in RO water three times to remove any residual acid remaining on the surface. The second acid cleaning steps entails rinsing the samples in a boiled acid mixture of concentrated ($\geq 95\%$) H_2SO_4 and

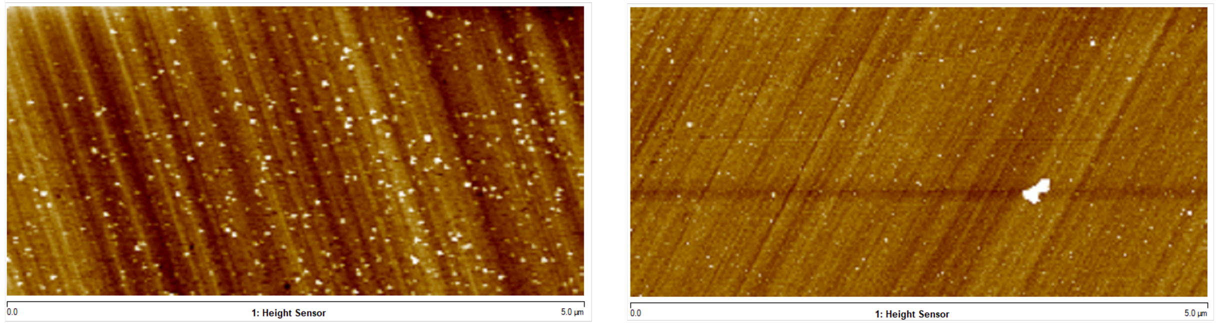


Figure 4.2: AFM scan results of sample surface After polish.

concentrated (65%) HNO_3 in a $3:1$ ratio. After 20 minutes in the boiled acid, the samples were rinsed in RO water three times. The second step is primarily serves for surface oxidation, which is crucial for the subsequent surface hydrogenation process.

After the acid clean, samples may still retain some acid residue on the surface. To rectify this, samples underwent a solvent clean process. A 5-minute rinse in acetone with ultrasonic water bath facilitates the removal of any grease and unwanted particles on the sample surface. Subsequently, a 5-minute rinse in IPA with ultrasonic water bath aims to eliminate any residual acetone. It is imperative to transfer the sample into IPA promptly to prevent acetone from drying on the sample surface, as this can be difficult to remove and may impact subsequent fabrication processes. Figure 4.3 displays the AFM scan results of samples after the acid clean and solvent clean process. In comparison to the scan results before cleaning, the presence of white dots on the sample surface is significantly reduced.

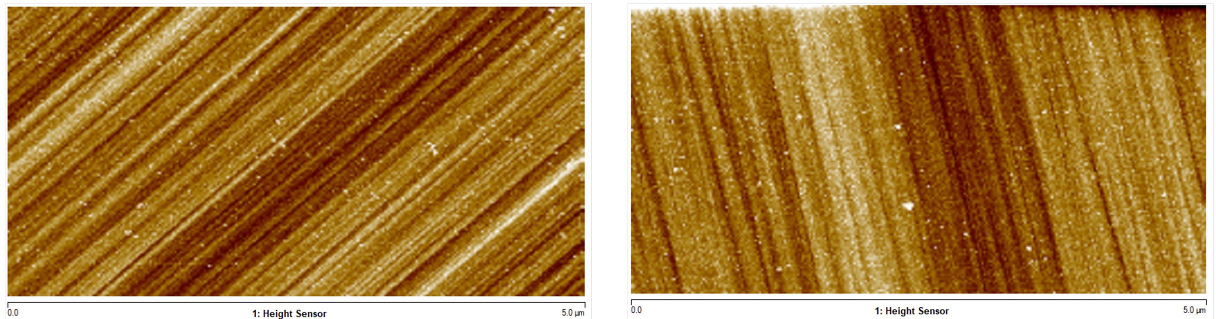


Figure 4.3: AFM scan results of sample surface after the cleaning process.

The samples were then packed in membrane box to prevent samples flips during the transit. They were subsequently dispatched to RMIT University in Australia for plasma hydrogen termination. In this process, oxygen-terminated diamond samples were placed in a vacuum chamber with the sample holder heated up to 800 °C. This temperature was maintained to prevent the etching of the diamond surface, which can dramatically roughen the surface and prevent the thermal desorption of hydrogen termination[92], [113]. Subsequently, hydrogen plasma with a power of 1000 W was directed onto the sample surface. After termination was complete, but before

the plasma were turned off, the holder temperature is reduced to 700 °C. Finally, the chamber temperature is gradually decreased back to the room temperature.

The sample surface may undergo modification by the hydrogen plasma, where both treatment duration and substrate temperature can influence the surface roughness[71], [114], [115]. AFM is utilised post-termination to ensure the surface remains sufficiently smooth enough for subsequent fabrication steps. Additionally, Hall measurements are conducted to confirm surface conductivity over time, ensuring hydrogen termination has been achieved. Figure 4.4 illustrates the surface roughness of diamond sample before and after hydrogen plasma treatment. On average, the surface roughness of more than half of samples increased by 0.3 *nm*, while a small proportion decreased by 0.1 *nm*. Overall, the surface remains in good condition to progression to the next step.

Subsequent to the roughness measurement, Hall kit measurements were conducted to assess surface conductivity. Four probes placed on four corners of the sample and made contact with the sample directly. The conductivity is measured six times over a span of ten days. This aims to characterise any changes in the conductivity over time and determine the duration required for conductivity stabilisation. Figure 4.4 illustrates a significant drop in conductivity across all samples within 2 to 3 days, followed by stabilisation or a slight increase in conductivity after day 9.

After all those aforementioned preparation, a solvent clean, as mentioned above, is conducted to remove any potential contamination induced during transit and plasma treatment. At this stage, the samples are ready to proceed to the subsequent stages.

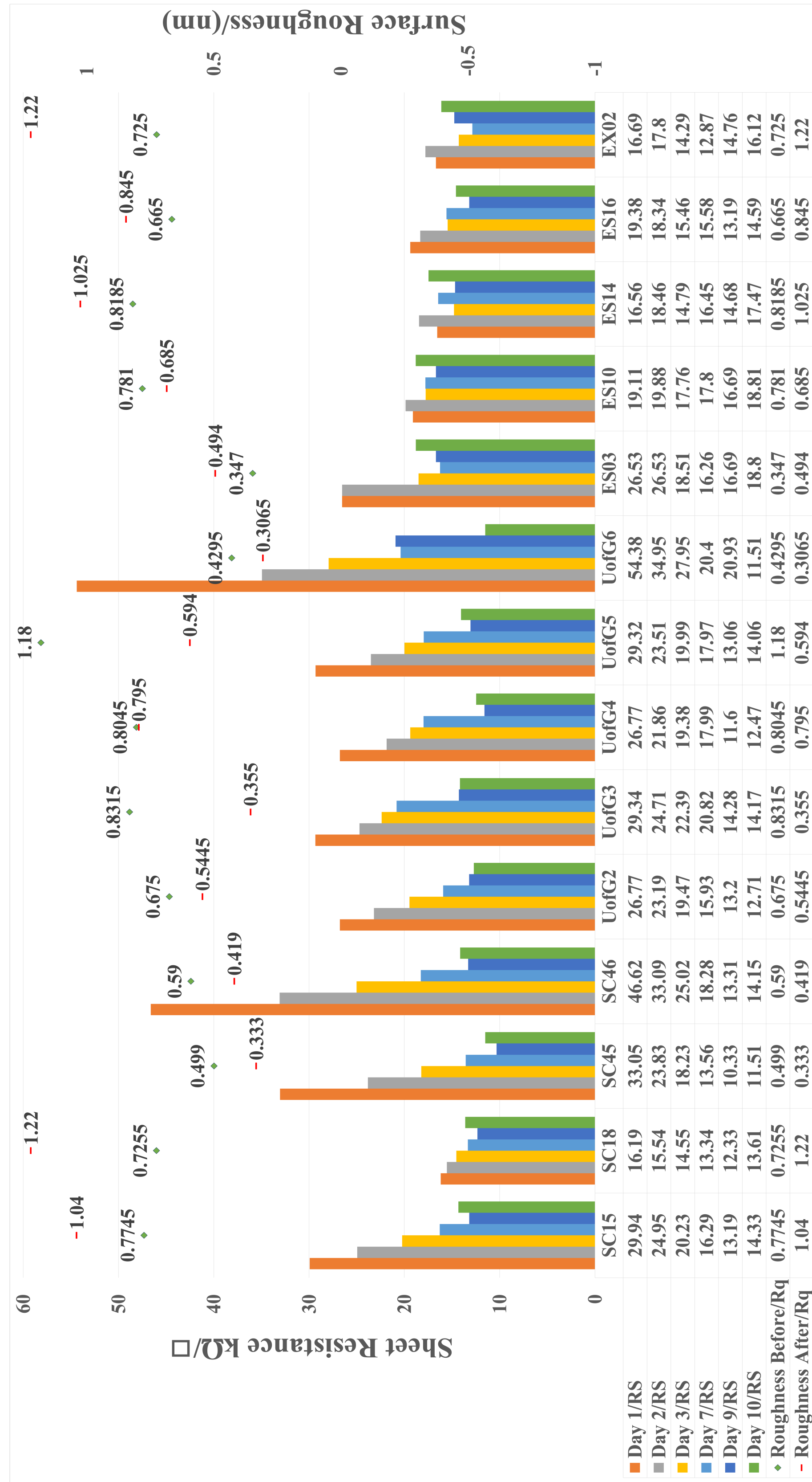


Figure 4.4: AFM scan results and Hall kit measurement of sample surface before and after hydrogen plasma treatment.

4.2 Resist spinning

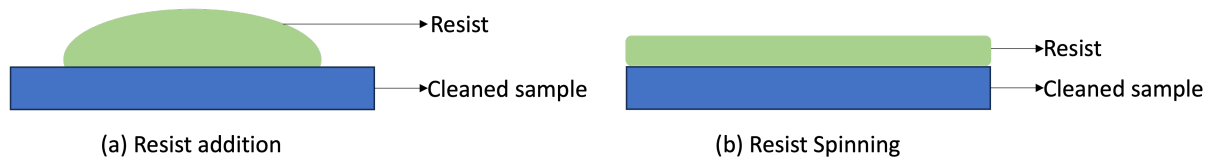


Figure 4.5: Resist before and after spinning.

Resist spinning is a process used to spread photoresist or e-beam resist into a uniform layer on the sample surface for subsequent exposure and development steps. Cleaned samples are mounted in the middle of a chuck, which is held by a vacuum system underneath. A specific amount of resist, typically enough liquid to cover 70% of the sample surface, is dispensed onto the sample surface using a pipette. Following the addition of the resist, the sample is spun at a high speed (thousands of revolutions per second), whereby centrifugal force spreads the resist into an uniform layer. The final thickness of the resist is highly dependent on the spinning speed; higher speed generally result in a thinner resist layers, although the thickness gradually stabilises when the spinning speed reaches a certain level[116]. Samples with a uniform resist layer are then transferred to hotplate or oven to bake the resist, evaporating the solvent from the resist. Different baking duration and temperature are applied to different resist to achieve optimal profiles after development.

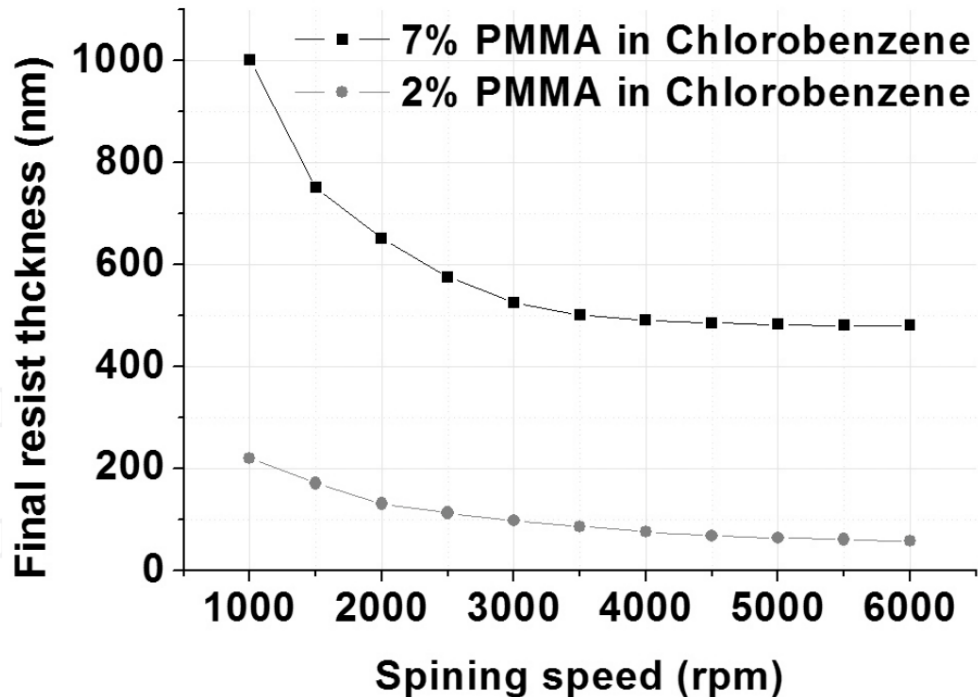


Figure 4.6: Resist thickness versus spinning speed with ebeam resist as example[116].

The resist used in this thesis include Lift Off Resist (LOR), 50 K 12% and 200 K 4% e-beam resist and photoresist S1805. With customised spinning speed and baking durations, they yield resist thickness of 300 nm, 310 nm, 150 nm and 500 nm respectively.

4.3 Photo-lithography exposure

Photo-lithography is a process where photo-resist is employed to transfer desired patterns from a photomask to the sample surface. Photoresist typically consists of long chain polymer whose structure can be altered by UV light with specific wavelengths. In positive photoresist, exposure to UV light breaks the polymer chains into shorter ones, enabling selective removal of the exposed area by specific solvents such as TMAH and diluted Microposit. In contrast, in negative photoresist, the polymer is hardened by UV light. The machine utilised in this thesis is SUSS MicroTec Mask Aligner 6 (MA6).

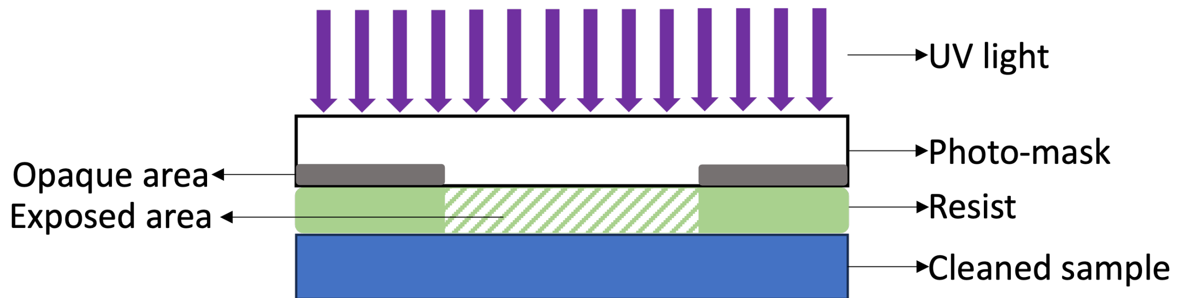


Figure 4.7: Photolithography with photo-mask contact with the sample surface. The opaque area made of chrome blocked the UV light from exposing the resist.

A photomask is a partially opaque and partially transparent mask made of chrome and quartz. Desired patterns are written onto the mask, where the chrome blocks the UV light while the quartz areas allow the UV light to travel through and expose the photoresist.

After resist spinning, samples are loaded on the Mask Aligner 6 (MA6) holder and held steady by a vacuum system under the holder. The photomask is secured by vacuum between the sample and the UV light source. A customised exposure duration and contact mode is set up in the system, after which UV light is directed to expose the sample surface through the photomask.

When a design necessitates multiple times of exposure to form the final patterns, a manual alignment process is required. Markers, typically cross patterns, are employed for alignment purposes, placed at the four edges of the sample during the initial exposure. The sample holder in MA6 is adjustable in the X and Y directions and can be rotated in the θ direction. For all subsequent exposures following the initial one, samples are adjusted in three directions to align the markers fabricated in the first exposure with those on the photomask. This step ensures that each exposure is aligned with the previous one.

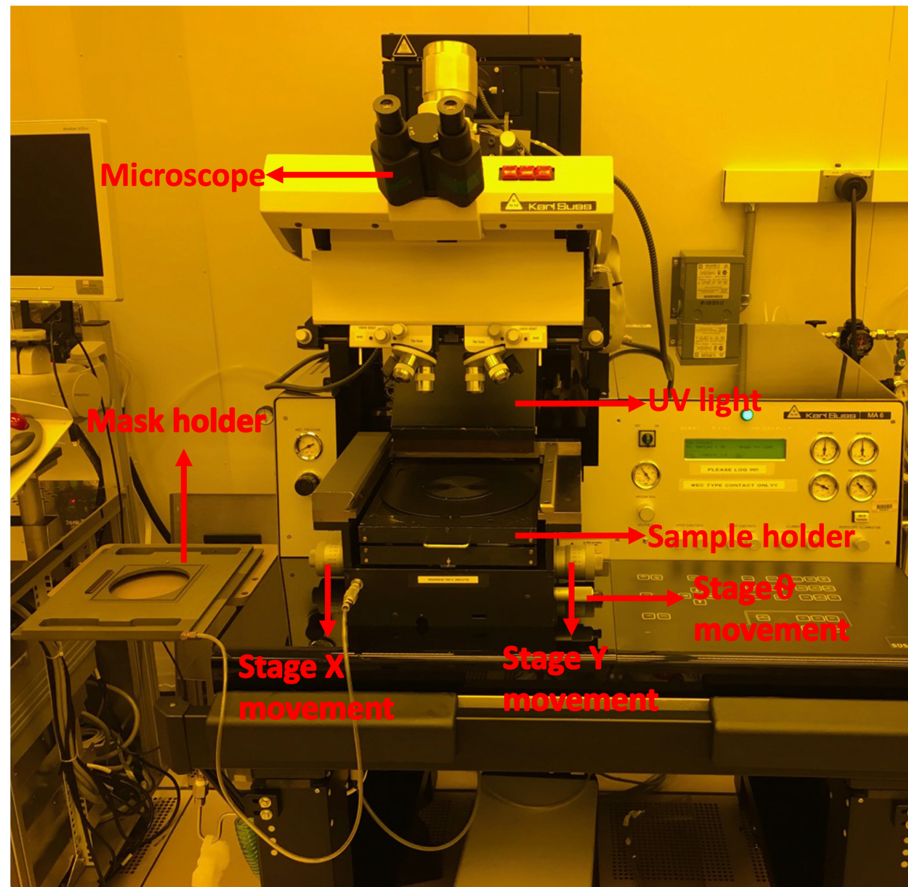


Figure 4.8: Photolithography Mask Aligner 6 (MA6)

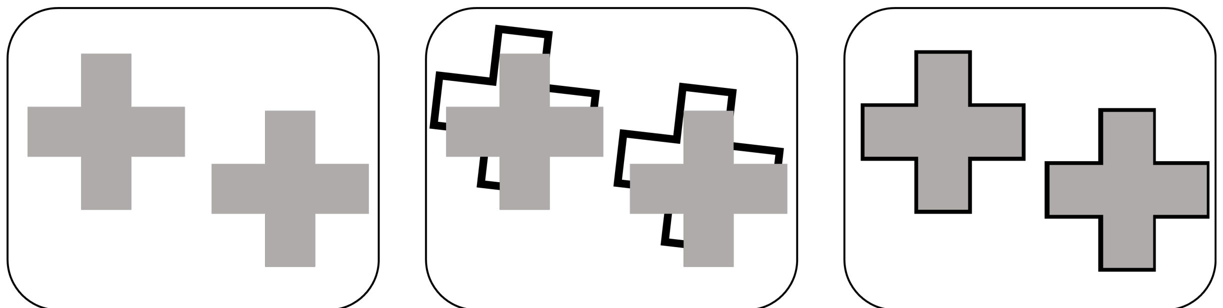


Figure 4.9: Marker used in photo-lithography.
The left is the marker made on the sample surface. The middle is the process of adjusting the marker on the sample according to the marker on the mask. The right one is after alignment, the cross on the mask overlaps with the marker on the sample surface.

The smallest feature size achievable via photolithography is highly determined by the wavelength of the light source. To enhance the resolution of photolithography, a light source with a shorter wavelength is required. Currently, Deep UV light, Extreme UV (EUV) light and X-ray are widely employed to improve the resolution. ASML company has achieved resolution of 5 nm and 3 nm with EUV photo-lithography. The mask aligner used in this thesis provides a minimum resolution of around 2 μm.

4.4 Electron beam lithography

Electron beam lithography (EBL) is a technique used to expose electron beam sensitive resist on the sample surface to transfer desired patterns. EBL utilises an electron beam instead of UV light.

One advantage of using EBL over photolithography is that the patterns are designed using CAD software, and the files are exported as GDS file. These GDS files are then fractured using another software, Beamer, and expored as GPF files. Cjob is used to read GPF files and setup the exposure. The final step involves submitting the job on James Watt Nanofabrication Centre (JWNC) website. Subsequently, the machine can read the design files and use them directly to move the electron beams on the sample surface and expose the designed area, providing more flexibility to EBL compared to photo-lithography.

As the exposure is carried out by electron beams, in the case of insulated samples such as diamond, electrons may accumulate on the sample surface. When a sufficient amount accumulates, the electrons can deflect incident electron beams, leading to distortion of patterns and affecting accuracy. To mitigate this issue, a charge dissipation layer (CDL), typically a thin layer of metal, is added on the ebeam resist. This CDL channels all electrons to the ground. In this thesis, Au, Al and sputtered Au and Pd mix are utilised as CDL in different stages.

The second advantage of using EBL over photo-lithography is that EBL provides higher resolution. As discussed in the previous part that we can only achieve a resolution of 2 μm with MA6. To achieve finer feature, EBL is necessary. The smallest feature size is determined by the minimum spot size the electron can produce, which is in turn determined by the wavelength of electron emitted. It is also determined by the amount of electron backscatter, which is dependent on the accelerating voltage and material being written.

The equipment utilised in this thesis is the EBPG5200, with Figure 4.10 depicting the simplified structure of the e-beam system. Electron beams, generated by thermally assisted field emission sources, are accelerated by the anode. The accelerated electron beams pass through a set of magnetic deflection coils, which tilt and shift the incident alignment onto the substrate. A series of apertures are employed in the system to converge and exclude scattered electrons, thereby controlling spot size and current density. The final patterns are defined by the main and subfield deflection coils. Analogue driven signals, generated by the patterns generator, deflect the electron beam to produce patterns designed by the user. The beam blanker in the column is utilised to turn the electron beams on and off.

Most of jobs completed in this work requireed multiple steps, necessitating alignment to ensure that each step overlays with the previous exposure. In electron beam lithography, a different

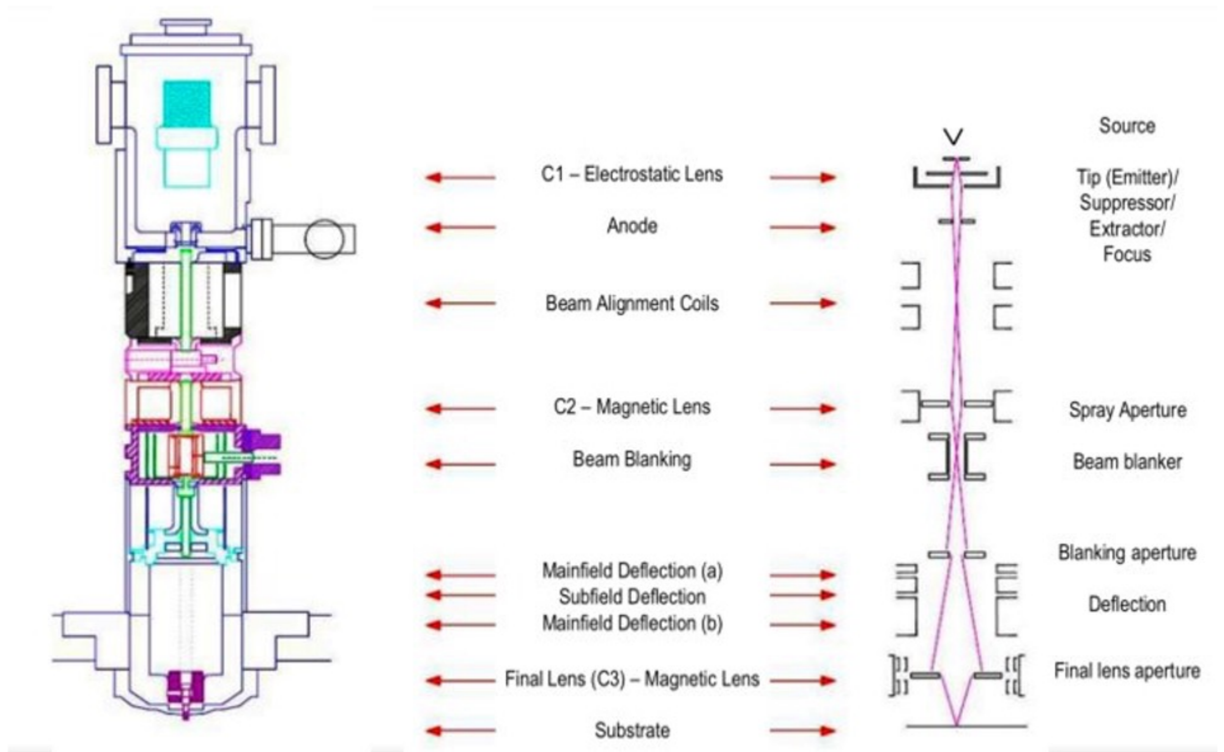


Figure 4.10: Simplified representation of EBPG. Information from [117]

markers set are employed compared to photolithography. Instead of manual alignment, the EBPG can automatically search for registered marker positions. A set of markers, consisting of individual squares sized at 20 μm, are fabricated on the four corners of the sample. By uploading the markers coordinates, the machine can search for the correct position and form electron beam images at each position. These images then are analyses by algorithms, enabling the machine to adjust the position and offset of the sample to complete the alignment process. To ensure clear electron beam images, metals with higher atomic numbers are recommended, as they have more back-scattered electrons to form a clear image. Au and Pd are used in this work.

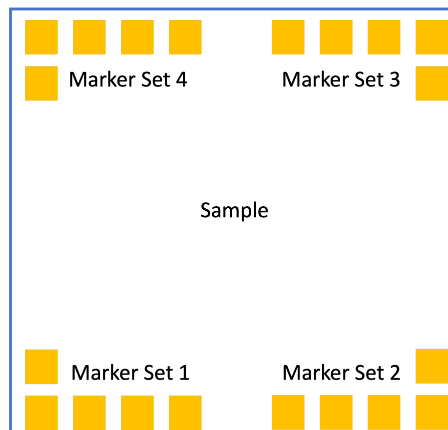


Figure 4.11: Typical marker sets used in Ebeam lithography.

4.5 Resist Development

After exposure, resist should be developed in a specific solvent. In the case of using positive resist, which is compatible with both e-beam and photolithography, the exposed area is supposed to be removed while the unexposed area remains on the surface. Ideally, there should be no resist left on the area where resist exposed to the UV light or the electron beams. However, in many cases, the unexposed area usually is affected lightly, and the exposed area may retain a small amount of resist on the sample surface, which is known as resist residue.

Resist residue can cause a series of issues for the next fabrication steps. The residue affects the adhesion between the metal and substrate. For metal-substrate contact, the residue also builds up a capacitor which influences the properties of the devices. To remove the resist residue, a low-power oxygen plasma is typically used to clean the surface[118]. This process, known as ashing or descumming, involves oxygen plasma under vacuum chamber interacting with the resist, oxidising it into gaseous species such as carbon dioxide (CO_2) or carbon monoxide (CO)[119]. The plasma power and duration can be adjusted to adapt to the different types of resist applied on the surface. Extra care required in this step, as hydrogen termination can be easily damaged by oxygen plasma. Some alternative methods have been explored to avoid the damage to hydrogen termination, which will be talked about later.

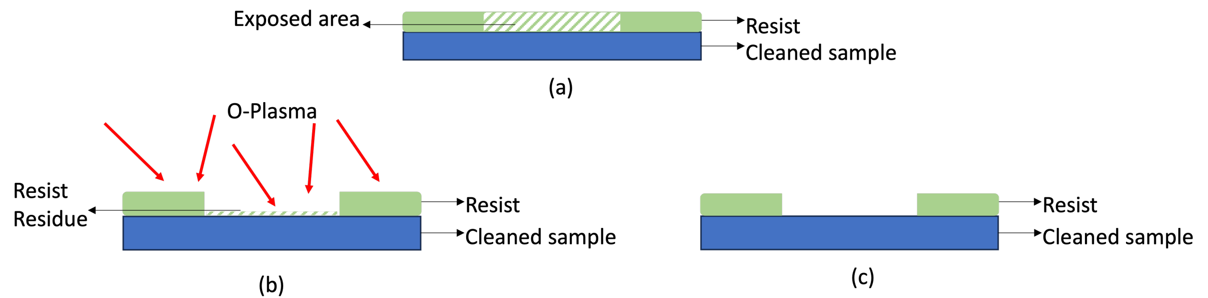


Figure 4.12: Resist development and ashing.
(a) Sample with positive resist after exposure. (b) Sample with positive resist after development with resist residue left on the exposed area. (c) After ashing, the resist residue is removed.

For both photo and e-beam resist, development is affected by temperature, development duration, solvent concentration, and resist thickness. Additionally, the exposure duration used in photolithography and dose applied in e-beam lithography influences the development as well. The parameter for the resist used in this work are listed in the table below.

4.6 Metallisation & lift-off

Metalisation is a crucial step for pattern transfer and metal-semiconductor contact formation. Various techniques, such as physical vapor deposition (PVD), chemical vapor deposition (CVD)

and electroplating, are employed for metal deposition. In this work, PVD is used for this purpose.

PVD is a process whereby solid-state target metals are transformed into the vapor phase, and vaporised metal is then condensed onto the sample surface. To vaporise the target metal, either thermal evaporation or electron beam evaporation can be used. Electron beam evaporation is utilised in this work for metal deposition. It is imperative that the deposition chamber maintains high vacuum conditions; otherwise, gaseous molecules and other particles may disrupt the film uniformity and introduce contamination. In addition, the high vacuum chamber prevents oxidisation of the metal.

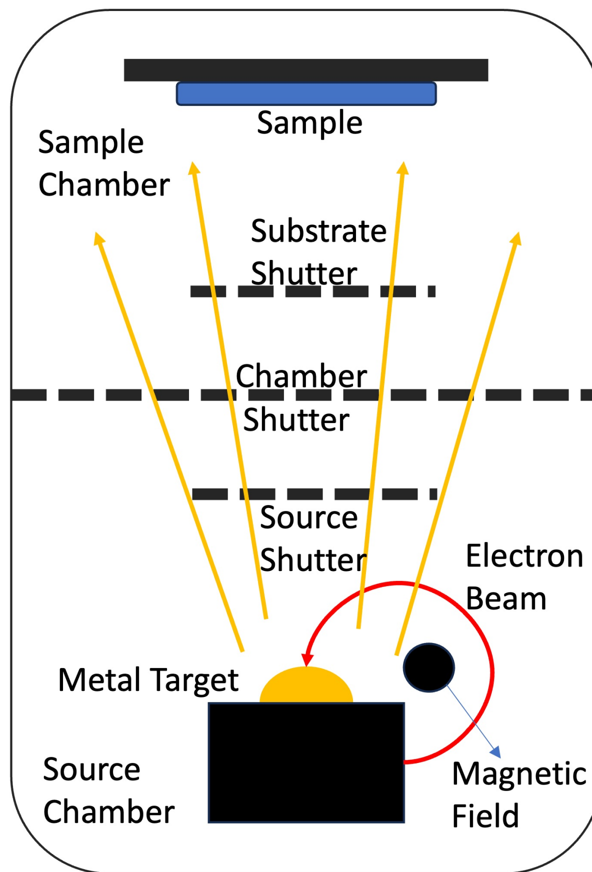


Figure 4.13: Simplified electron beam evaporation chamber.

Figure 4.13 illustrates the simplified inner structure of an electron beam evaporation machine. The chamber is separated into two main chambers: the source chamber and the sample load chamber. The chamber containing the metal target is maintained under high vacuum to prevent contamination and oxidation of the metals. After loading the sample onto the sample holder, the loading chamber is evacuated using a rough pump and cryo pump to reduce the pressure inside the chamber. When the pressure in the loading chamber approaches that of the source chamber, the shutter between the two chambers is opened. Electron beams are then used to heat up the

metal target to its melting point. Once the evaporation rate stabilises at the desired rate, the substrate and source shutter are opened to allow the metal deposit onto the sample surface.

The entire process is completed under high vacuum conditions, and the deposition rate and thickness are monitored by a gold-plated Quartz Crystal Microbalance (QCM). The QCM is positioned near the sample location. As material is deposited on the crystal, its resonance frequency changes. This change is correlated with the mass change, providing valuable information about the deposition rate and thickness.

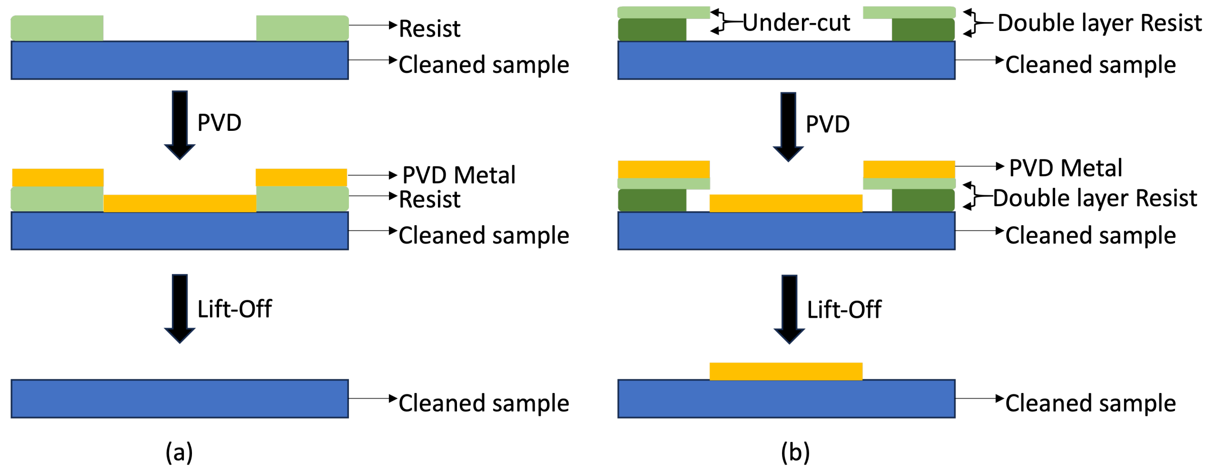


Figure 4.14: Lift-off process for sample with single layer of resist (a) and sample with double layers of resist (b).

Lift-off is a process whereby the unexposed resist is removed by specific solvent, leaving the metal deposited only on the developed area of the surface. This process completes the pattern transfer. Electron beam evaporation is a non-conformal process which means that the deposition is unable to cover the edge wall of the sample unless the sample is tilted to a specific angle. However, with a single layer of resist, the metal might still adhere to the resist edge wall, potentially causing the metal on the developed area to be partially or totally stripped off during the lift-off process. To address this issue, a double layer resist is applied to create a structure known as an under-cut, which assists the lift off process.

Figure 4.14 illustrates the differences between single layer resist lift-off and double layer lift-off techniques. With a single layer of resist, the metal edges adhere to the resist edges, which can cause the lift-off process to fail. However, using two layers of resist with different sensitivities to the UV light or electron beams creates a structure called an "under-cut". This structure serves two purposes: firstly, it isolates the metal from the resist, and secondly, it provides spaces between the resist and the metal, which helps the lift-off solvent dissolve the resist from the inside.

In this work, LOR is utilised as the bottom layer for photo-lithography. Since LOR is not sensitive to UV light, the development of the top layer S1805 does not affect it. However, LOR can be etched by Tetramethylammonium Hydroxid (TMAH). As TMAH etches LOR faster than S1805, with proper controll of duration, LOR can create an under-cut. For e-beam lithography, resist with different molecular weight and concentrations are chosen to establish the under-cut. Molecular weight is linked to resist sensitivity, and concentration is associated with resist thickness. A lower molecular weight implies higher sensitivity, while a higher concentration results in a thicker resist after baking. Therefore, 50 K 12% PMMA is employed as the bottom layer, while 200 K 4% PMMA serves as the top layer.

The lift-off is usually conducted in a 50 °C water bath, with the sample immersed in a specific solvent for few hours or overnight. The solvent used for LOR lift-off is SVC-14, while the solvent used for PMMA lift-off is acetone.

4.7 Selective Etching of metals

Selective etching of metals is crucial for subtractive pattern transfer. Dry etching and wet etching are commonly employed techniques to remove unwanted materials from the sample surface.

Dry etching is a process that utilises plasma to etch away unwanted materials. The process involves chemical reactions between the ions and materials, and physical bombardment. In the vacuum chamber, all by-products are pumped out of the system. Dry etching is an anisotropic process, meaning that it produces a controlled and directional etch profile. For example, ashing, a mild dry etch process using oxygen plasma, is commonly employed to remove the resist residue. However, the ions and radicals generated during the dry etching can potentially damage the hydrogen termination.

To protect the diamond surface termination, wet etching is necessary. Wet etching is a purely chemical process involves soaking samples in specific chemicals to remove unwanted materials. This process is isotropic, meaning it etches uniformly in all directions. Wet etch offers advantages such as simple equipment requirements, high throughput and high selectivity compared to dry etching. In this study, wet etching is employed to remove unwanted gold from the diamond surface. The solvent used for wet etching is a mixture of KI/I_2. The etching rate can be regulated by diluting the solvent with RO water and adjusting the reaction temperature, thus enabling a more controlled etch profile.

$$2Au + I_2 \rightleftharpoons 2AuI \tag{4.1}$$

In this work, a gold 'sacrificial' layer is employed to protect the hydrogen-terminated diamond surface from contamination by resist residue or damage from plasma. Following photo or e-

beam lithography, the sample is developed and then subjected to ashing in oxygen plasma. The gold layer acts as a barrier, protecting the termination from the plasma. The subsequent step involves wet etching of the gold to transfer the pattern to the sample surface or open the windows in the Au layer.

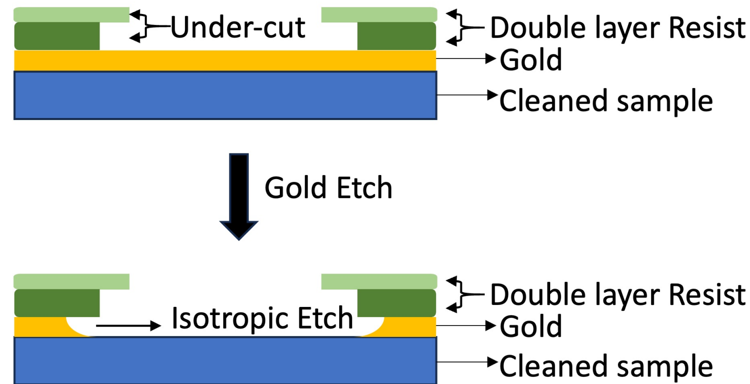


Figure 4.15: Gold wet etch with isotropic etching profiles.

4.8 Oxide deposition

Deposition of the oxide layer is a crucial aspect of the fabrication process. It can serve as a gate oxide to create a capacitor. As discussed in the previous chapter, the oxide with a LUMO near the hydrogen-terminated diamond valence band maximum acts as an electron acceptor and improves surface conductivity. It is essential to choose the appropriate method for oxide deposition for the intended purpose.

There are many different methods to put oxide on the sample surface, such as chemical vapour deposition (CVD), physical vapour deposition (PVD), atomic layer deposition (ALD). In this work, ebeam PVD, thermal PVD and ALD are applied to deposit oxide for different purpose.

As we talked in the previous part, PVD is commonly employed for metal deposition. It may also be used for oxide deposition. The fundamentals principles of PVD metal and PVD oxide deposition are similar. In the case of MoO_3 and V_2O_5 deposition, the process is carried out using thermal PVD deposition within Plassys 5 system. The main distinction between thermal PVD and e-beam PVD lies in the method of vaporization. In thermal PVD, the oxide is vaporized by heating the holder to the material's melting point, after which the evaporated material condenses onto the sample surface to form a thin film. A gold-plated quartz crystal microbalance is employed to monitor the deposition rate and thickness.

In contrast, the deposition of Al_2O_3 differs slightly from other oxide due to its higher melting point, which is approximately a few thousand degrees Celsius. In this case, electron beams are

utilized to heat up and evaporate the target from a solid state to a vapor state.

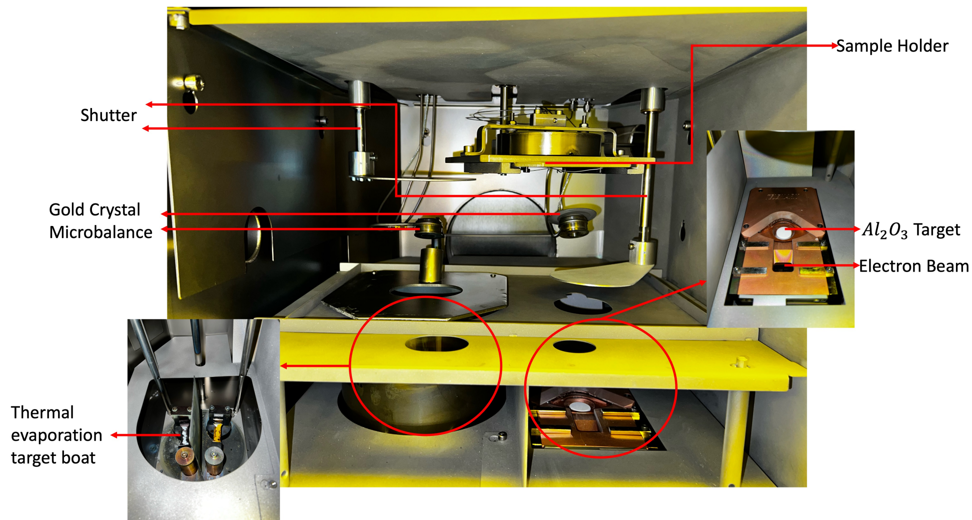


Figure 4.16: The inner structure of Plassys 5 (used for PVD of oxide materials).
The left part of the chamber is designated for thermal deposition, where materials such as Mo_2O_3 and V_2O_5 are used. Conversely, the right part of the chamber is designated for electron beam evaporation, which is suitable for materials with high melting point, such as Al_2O_3. A shutter between the target and the sample holder prevents materials from condensing on the sample surface until the deposition process stabilises. Additionally, a Gold Crystal Microbalance (GCM) situated between the sample holder and target material is utilised to monitor the deposition rate and thickness.

ALD is also employed in this work for the deposition of Al_2O_3. ALD is a thin film deposition technique that enables precise control over film thickness at the atomic level. It operates through a sequential, self-limiting surface reaction based on the temporal separation of two or more reactants. This approach allows for the deposition of conformal and uniform thin films on substrates with complex geometries [120].

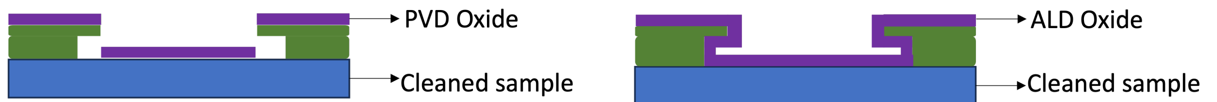


Figure 4.17: PVD and ALD oxide deposition profile.
ALD deposition provides a better thickness control, uniformity, conformal profile and complex geometries.

Precursors are chemicals that contain the elements necessary for the target material deposition in ALD. Typically, two or more precursors are used for the deposition of a single material. The precursor is introduced into the vacuum chamber, where it reacts with the substrate surface to form a single layer of chemical groups containing one of the element required in the final material. Before the next precursor reacts with the previous products, the chamber is purged to remove all remaining precursor and potential by-products.

Using Al_2O_3 deposition as an example, precursor 1, contains Al, reacts with the substrate, followed by a chamber purge to clean the chamber. Subsequently, precursor 2, containing O, is introduced into the chamber to form Al_2O_3 with the previous Al. The chamber is purged again to remove all by-products. This constitutes a complete deposition cycle for ALD, where each cycle only grows one single atomic layer of Al_2O_3 due to the self-limiting nature of this process. This cycle is repeated to achieve the desired thickness of materials.

To activate the substrate surface and facilitate reaction with the precursors, thermal or plasma energy is applied during the reaction step. Plasma-enhanced ALD offers several advantages, including a wider choice of materials, increased growth rate, improved material properties and reduced substrate temperatures [120]. However, for sensitive samples like hydrogen-terminated diamond, exposure to plasma during this process can potentially damage the surface. Therefore, caution must be exercised when employing plasma-enhanced ALD on such substrates.

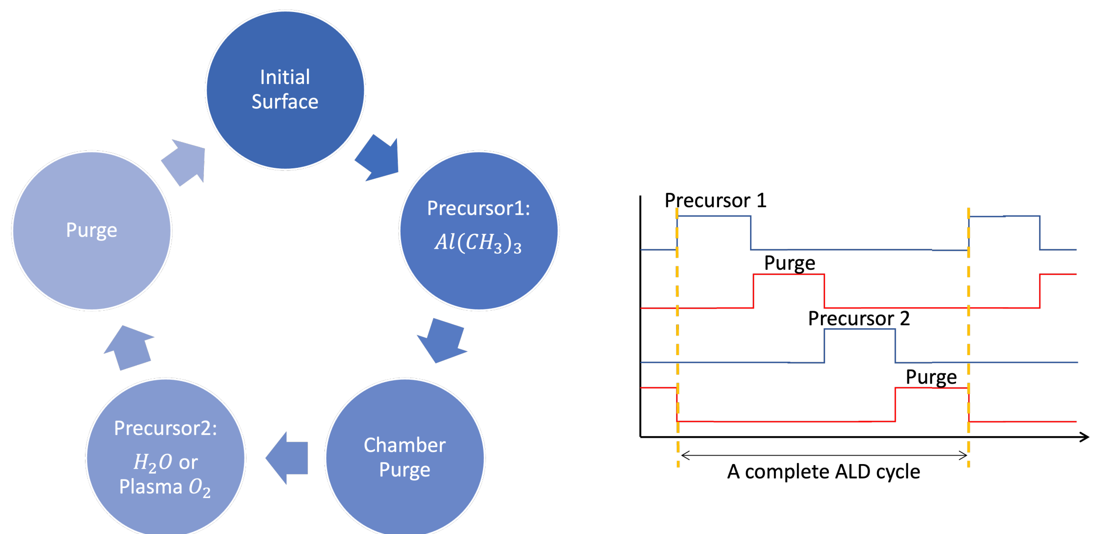


Figure 4.18: A complete ALD cycle with ALD Al_2O_3 as an example.
If the process is a thermal process, H_2O is used as the second precursor to provide oxygen. If the process is plasma enhanced, O_2 plasma is used as the source of oxygen.

In the case of Al_2O_3 deposition, H_2O serves as the source of oxygen in thermal deposition, while O_2 plasma is utilised in the plasma-enhanced deposition. In this work, to preserve the integrity of the hydrogen-terminated diamond surface, all Al_2O_3 deposition is conducted using thermal ALD.

An experimental investigation was designed to explore the effects of thermal ALD and plasma-enhanced ALD on the surface conductivity of hydrogen-terminated diamond. Three 3 mm single polished diamond samples (A,B and C) underwent an acid cleaning process and hydrogen termination with partners in Australia. Prior to proceeding to the next step, all three samples underwent solvent cleaning to remove potential contamination on the diamond surface post-hydrogen

termination.

Following the cleaning process, four-probe VDP measurement were conducted. Silver dag was applied to the four corners of the samples to ensure good contact between the probes and sample surface, particularly after the oxide deposition. The sheet resistance of these three samples in air was measured as 9 $k\Omega/\square$, 11 $k\Omega/\square$ and 9 $k\Omega/\square$ separately.

Subsequently, the three samples underwent Al_2O_3 ALD under different parameters to investigate the influence of different ALD processes on the hydrogen termination. Sample A was subjected to a standard thermal ALD Al_2O_3 deposition recipe, with a reaction activation temperature of 200 °C. Sample B underwent the same recipe as sample A, but with an additional in-situ anneal at 400 °C for one hour anneal before the deposition, aimed at removing any potential air adsorbates on the hydrogen-terminated diamond surface. Sample C underwent O_2 plasma-enhanced Al_2O_3 deposition without annealing. All three samples received a 10 nm thickness of Al_2O_3 on the surface.

Following the deposition, VDP measurements were conducted again to assess surface conductivity. The addition of silver dag before deposition facilitates easy probing through the silver stack to make contact with the diamond surface. Post-deposition, the sheet resistance of sample A dropped from 9$k\Omega/\square$ to 6$k\Omega/\square$, Sample B sheet resistance increased to 20$k\Omega/\square$ from 11$k\Omega/\square$ and Sample C sheet resistance is too high to be measured by the machine.

Sample	A	B	C
Process	Thermal ALD	Thermal ALD with 400°C annealing	Plasma ALD
R_s Before deposition	9 $k\Omega/\square$	11 $k\Omega/\square$	9 $k\Omega/\square$
R_s After deposition	6 $k\Omega/\square$	20 $k\Omega/\square$	$> 2\ M\Omega/\square$

Table 4.2: Sheet resistance change after ALD deposition under different growth conditions.

The decrease of the sheet resistance of sample A suggests that the thermal ALD process has enhanced the surface conductivity of the hydrogen-terminated diamond. Although the exact mechanism behind this improvement remains unclear (because the electron affinity of Al_2O_3 should not be high enough to act as an electron acceptor on H-diamond), it is hypothesized that specific defects exist in the oxide layer act as acceptor, thereby enhancing conductivity [121].

The sheet resistance of sample B increased by 9 $k\Omega/\square$ after the deposition. This may be contributed to two factors: Firstly, the annealing process removed air adsorbates, potentially depleting acceptors on the surface. Secondly, the high temperature annealing may have damaged

the hydrogen termination. To discern the cause of the increased sheet resistance, Sample B was treated with Buffered Oxide Etchants (BOE) to remove all the Al_2O_3, followed by VDP measurement. The sheet resistance remained the same after wet etching of the oxide as when measured with Al_2O_3 encapsulation and a few days exposure in air, indicating that the annealing process most likely desorbed part of hydrogen termination from the diamond surface. Given the vacuum level in the ALD chamber is between 200 mTorr and 80 mTorr, potentially partial oxygen termination in the chamber could have occurred during the annealing process for sample B.

Sample C subjected plasma-enhanced ALD, exhibited no measurable conductivity after Plasma ALD Al_2O_3 deposition. The oxygen plasma used in the second precursor can remove hydrogen and oxygen-terminates the diamond surface, rendering it non-conductive. After BOE removal of the Plasma ALD Al_2O_3 and exposure to air, the VDP measurement indicated no measurable surface conductivity, confirming that the hydrogen termination has most likely been removed/damaged by the ALD plasma.

Overall, to preserve the hydrogen termination on the diamond surface and maximise conductivity, the optimal approach for ALD Al_2O_3 deposition in this study is thermal ALD without the annealing process. Plasma-enhanced deposition can damage the hydrogen termination. Further experiments are warranted to elucidate the effects of annealing on the sample , as hydrogen termination should not be removed by a one-hour 400 °C annealing [122], [123].

4.9 Diamond MESFETs Fabrication Flow

In a typical hydrogen-terminated diamond MESFETs fabrication process, several key steps are involved, including marker placement, isolation, bondpad, active region etching, gate formation and oxide deposition. The smallest feature size of the diamond MESFET in this study is 2 μm. Thus photo lithography is used for the fabrication. Figure 4.19 illustrates the fabrication for the hydrogen-terminated diamond MESFETs, wherein ALD Al_2O_3 serves as the encapsulating oxide.

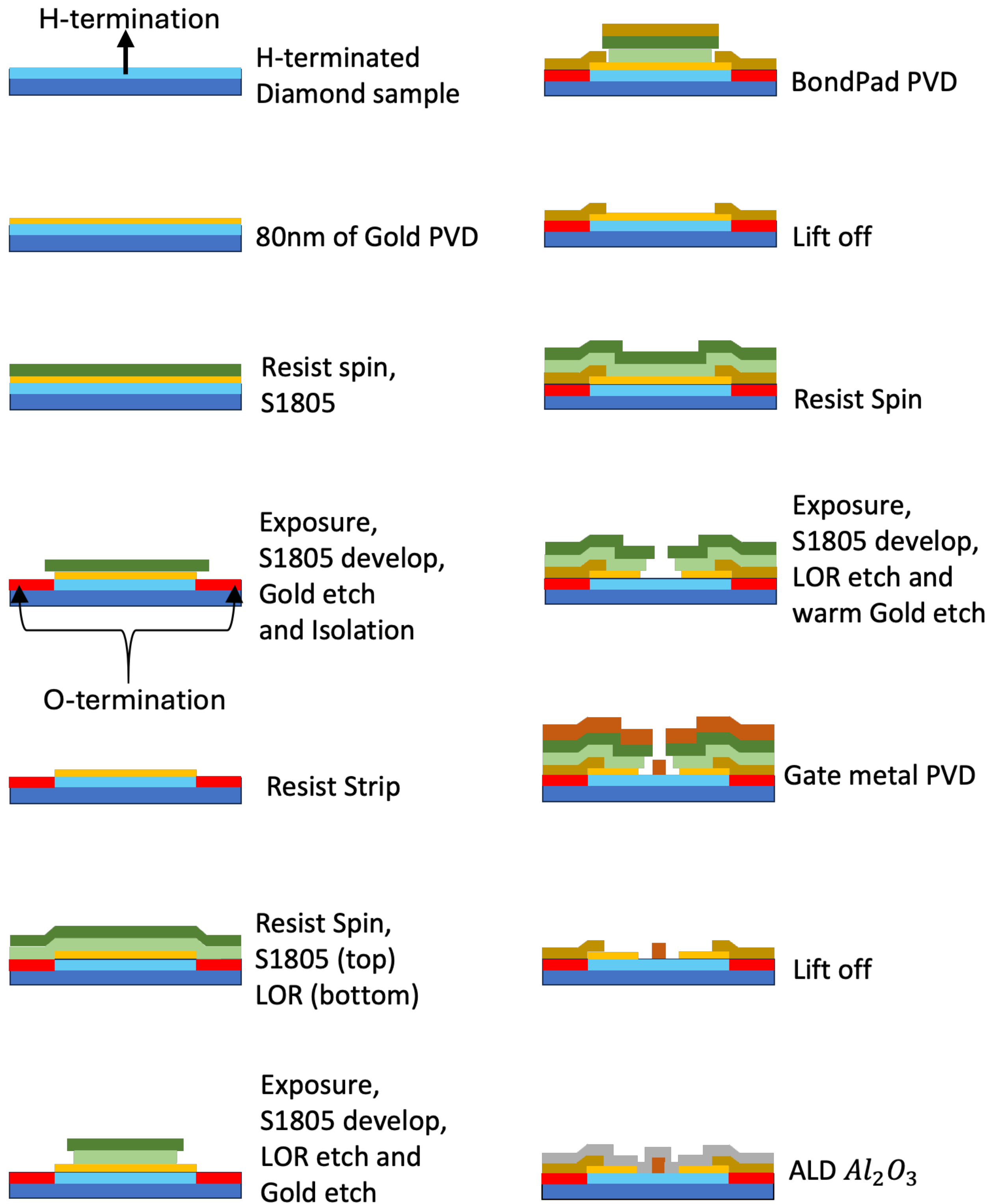


Figure 4.19: Fabrication of hydrogen terminated diamond MESFETs with gold sacrificial layer to protect the surface conductivity and ALD Al_2O_3 as encapsulating layer.

Sample clean

A 4.5 *mm* $\times$ 4.5 *mm* double-polished (100) single crystal diamond sample was purchased from Element six. A hot acid clean was employed to eliminate the potential metal contamination and oxidize the diamond surface. Subsequently, the samples underwent solvent cleaning procedures before being sent to Australia for hydrogen termination using hydrogen plasma. Following the hydrogen termination, a solvent clean consists of 5 minutes in acetone followed by 5 minutes IPA with ultrasonic was conducted to remove any residue contamination.

Gold sacrificial layer deposition

The initial stage involved depositing a layer of gold onto the diamond surface to shield the surface termination from potential damage during subsequent ashing processes. Additionally, this thin layer serves as the ohmic contact pad in the subsequent steps. Samples were secured onto the holder, and an 80 *nm* layer of gold was evaporated onto the diamond surface using an electron beam.

Markers

The fabrication involves multiple layers of lithography to be completed. To align each layer with the previous one, makers are fabricated on the sample surface during first exposure. Double layers of resists are employed for the convenience of lift-off process. LOR and S1805 are used as the bottom and top layer, respectively. After the development of S1805, oxygen plasma asher is utilized to remove the resist residue. Subsequently, CD-26 (2.5% TMAH) was applied to remove the LOR underneath the developed top layer of resist, with over-etching applied to create an undercut. Another round of ashing is conducted to eliminate LOR residue. Following this, a gold wet etch is employed to remove the gold underneath. The metallization for markers used in this work consists of 20 *nm* of Titanium and 80 *nm* of Gold. Titanium aids in ensuring gold adherence to the diamond surface. Subsequently, the sample is immersed in SVC-14 for an overnight water bath at 50 °C. Upon retrieval from the water bath, a pipette is used to fully remove the resist, followed by cleaning the sample surface with IPA.

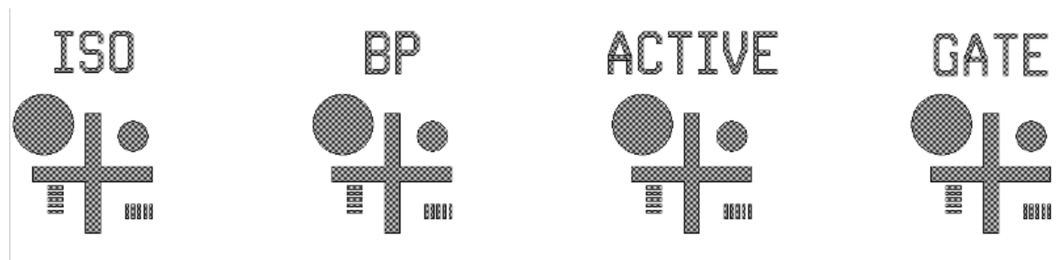


Figure 4.20: Marker used in photo-lithography

Isolation

Isolation is a crucial step aimed at electrically isolating devices on the substrate from each other, ensuring that the current is confined to a single device. To achieve this, the hydrogen termination over the surface, where insulation is required, must be removed. The sample with marker on is spun with a single layer of resist. An undercut is not necessary in this step since it is defined by subtract process(wet etch) instead of addition process (lift-off). The MA6 is utilized to align the pattern with the previous marker exposure. Subsequently, the sample is developed and ashed to remove the unwanted resist. Following this, gold etching is applied to remove the gold where the photo-resist has been developed. The final step involves oxygen plasma ashing to replace all the hydrogen termination with oxygen, resulting in the formation of the isolation area. An overnight acetone with water bath is utilized to strip off the resist. The remaining gold on the surface serves as both a protection layer for the hydrogen termination and an ohmic contact metal.

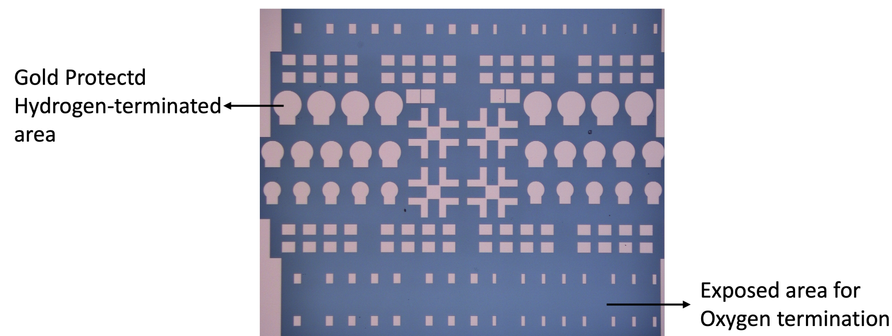


Figure 4.21: Sample with gold after isolation step.

Bond pads

The ohmic pad is formed from 80 *nm* of gold that is too thin and fragile for the measurement by physical probing directly without causing damage to the contacts. Therefore a more robust and thicker bond pad layer is fabricated over the ohmic pad. Similar to the fabrication of marker level, a double layer of resist is spun onto the surface. After the development and etching of the two layers of resist, gold is wet etched to open the window for the bond pad. Ebeam PVD is used to deposit 10 *nm* of Ti and 180 *nm* of Au as the bond pad metal stack. Titanium here performs as an adhesion layer, increasing the robustness of the top gold layer. The sample is then rinsed in SVC-14 for lift off.

Active device region

Test structures like TLM and VDP require partial removal of gold to expose the hydrogen termination surface for measurement. Similar to the isolation step, wet etching is used to transfer

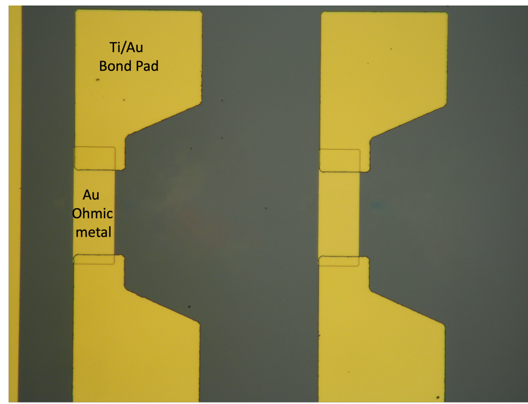


Figure 4.22: MESFETs after Bond Pad lift off.

the pattern, a single layer of photo-resist is sufficient for the process. S1805 is spun and baked onto the sample surface. The MA6 aligns the active area with the exist patterns. A 1:4 ratio of Microposit to RO water is used to develop the exposed resist. Since the smallest feature in this step is 2 μm, a hot gold etch is employed to control the etch rate and achieve a better etch profile. One portion of the Au etch is diluted with ten portions of RO water. Then, the solvent is heated to 60 °C on a hotplate. The sample is then immersed in the solvent for 10 seconds to remove the unwanted gold. An overnight water bath in SVC-14 is required after the gold etch to strip off the resist.

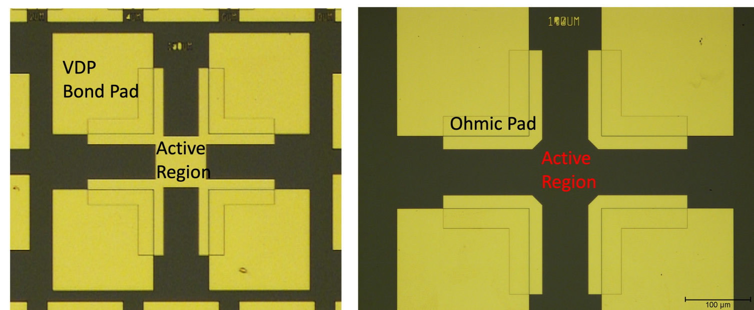


Figure 4.23: Active region fabrication before and after gold etch.

Gate

The next step for a diamond MESFET is the gate level. A lift-off process is required for this additional step. LOR and S1805 are used as the bottom layer and top layer, respectively. After exposure and development, ashing is employed to remove all the resist residue. Then, a warm gold etch is used to achieve smooth edges. This gold etch not just open the window for gate metal deposition but also separate the remaining gold into two ohmic metals. Then ebeam PVD is used to deposit 20 nm of Aluminium, 20 nm of platinum and 80 nm of gold on the sample surface as gate metal stack. Lift off is performed after the deposition, and a pipette is used to remove the resist and metal carefully.

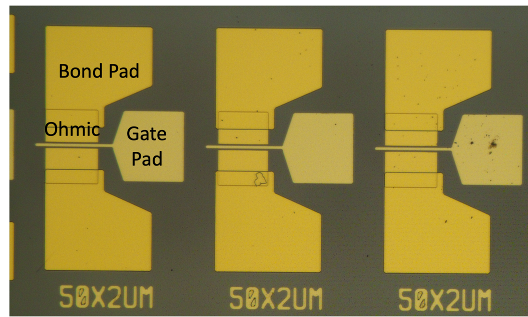


Figure 4.24: MESFETs after gate lift off.

Oxide deposition

To improve the thermal stability and surface conductivity, following the gate step, 10 *nm* of thermal ALD Al_2O_3 is deposited on the sample surface to encapsulate the device. To ensure proper contact between the measurement probes and the bond pad metal, an additional step is carried out to open a window over the bond pad and gate pad. Subsequently, the sample is immersed in 2% of buffered oxide enchants (BOE) for 100 seconds to remove the unwanted Al_2O_3.

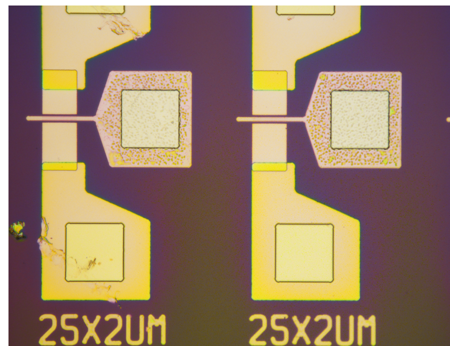


Figure 4.25: Resist over bond pad and gate pad is exposed and developed. Thermal ALD Al_2O_3 is wet etched by BOE to provide access to bondpads for probing.

4.10 Accumulation Channel diamond MOSFETs Fabrication Flow

Normally-off, "Accumulation Channel" diamond MOSFETs in this work are fabricated with electron beam lithography, which shares similarities with the photo lithography process used for MESFETs. This subsection will primarily focus on providing additional details regarding the different fabrication steps while simplifying those that are similar. The key steps include markers, isolation, ohmic pad, bond pad, oxide deposition and gate.

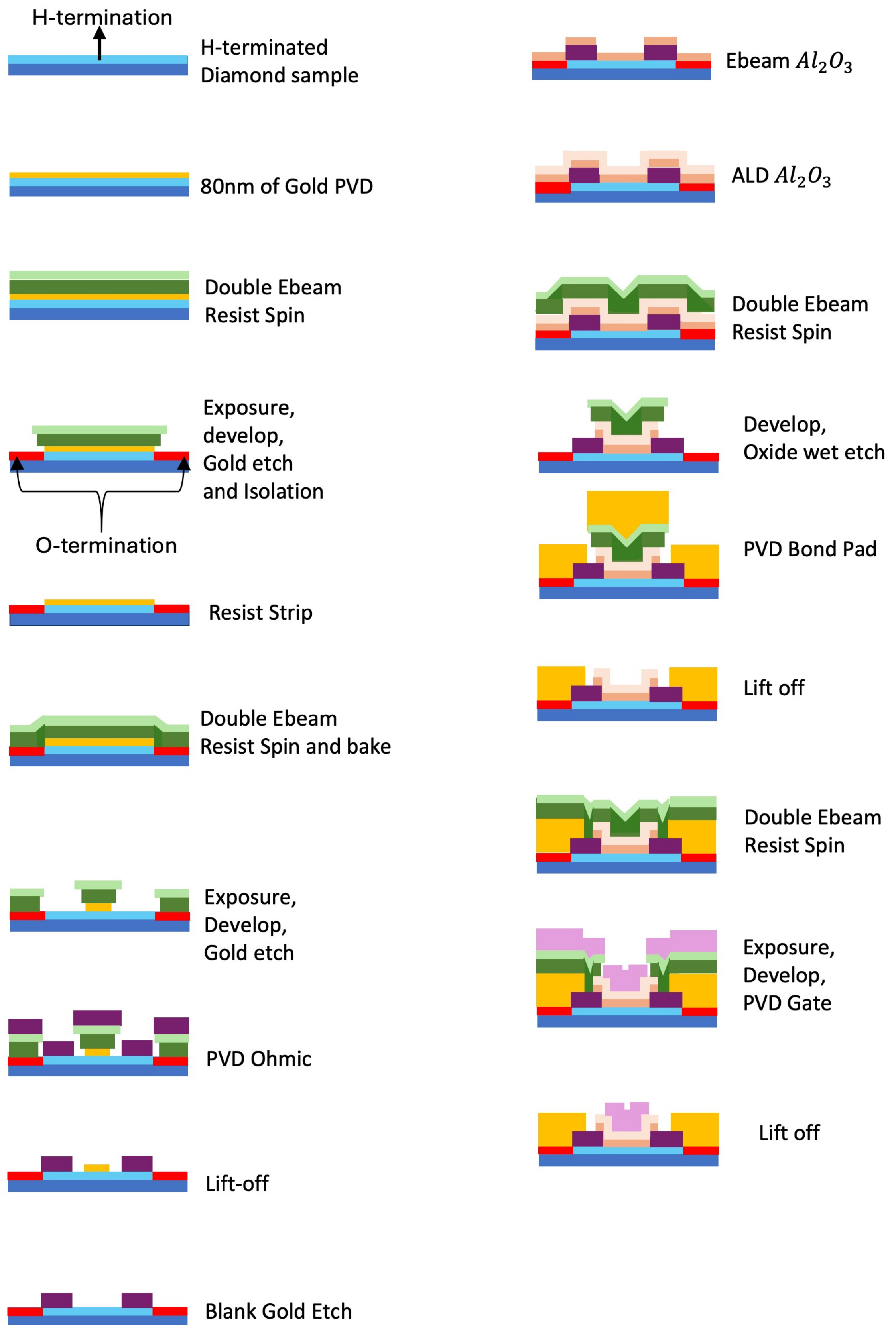


Figure 4.26: Normally-off "Accumulation Channel" hydrogen terminated diamond MOSFETs fabrication flow.

Sample Preparation

A single crystal (100) single-polished diamond sample is purchased from element six. Thorough cleaning, including acid cleaning and solvent cleaning, is conducted to oxidize the surface and remove potential contamination. Subsequently, the sample is sent to our collaborator in Australia for hydrogen termination. After the termination process, the sample is cleaned with acetone and IPA. Following the termination process, the sample is exposed in air for a few days, and Hall kit is used to monitor the surface conductivity. Once the surface conductivity reaches the optimal value and becomes stable, a sacrificial layer of 80 nm of gold is deposited on the diamond surface.

Markers and Isolation

The makers used for Ebeam lithography are different from those used in photolithography. Ebeam lithography markers consist of several 20 μm squares. A double layer of PMMA is used for the lift-off marker fabrication. After spining and baking, a thin layer of metal (a mix of Au and Pd) is sputtered onto the sample surface as a charge dissipation layer (CDL) to channel all electrons to the ground and prevent pattern distortion. The marker layers in the design file are uploaded to EBPG5200.

The first step after exposure is to rinse the sample in pure gold wet etch for 30 seconds to remove the CDL. Subsequently, the sample is developed in MIBK:IPA 1:1 developer for 30 seconds, followed by a 30 seconds rinse in IPA. Due to the sensitivity of the developer to temperature, a water bath is used to warm up the solvent to 23 °C before development. As the bottom layer of PMMA is more sensitive to the electron beams, an undercut is formed after the development.

Prior to the wet etch of the gold layer, an 80W 2-minute oxygen plasma ashing is employed to remove the resist residue. Then,a 40-second room temperature gold etch with a 1:4 gold etch to RO water ratio is used to remove the unwanted gold. Following this, 20 nm of Titanium and 100nm of Palladium are deposited using the PVD method. Since there is a gold blanket etch later, Palladium is used as marker instead of gold to avoid damaging of the markers. The lift off involves soaking in acetone with a 50 °C of water bath for 4 hours.

Isolation is processed in a similar manner to marker fabrication. To ensure alignment with the previous step, coordinates of four markers on each corners of the sample are submitted to EBPG. The machine can then locate the marker position by detecting the backscattered electrons from the metal marker and the substrate diamond. After the development and gold etch, the isolated area is exposed to air. Subsequently, an 80 W 3-minute of oxygen plasma is employed to replace the exposed hydrogen-terminated with oxygen, resulting in an insulating surface. Two isolation test structures can be found in figure4.27, with three yellow pads in a row both at the top and

bottom of the design, facilitating testing for isolation completeness.

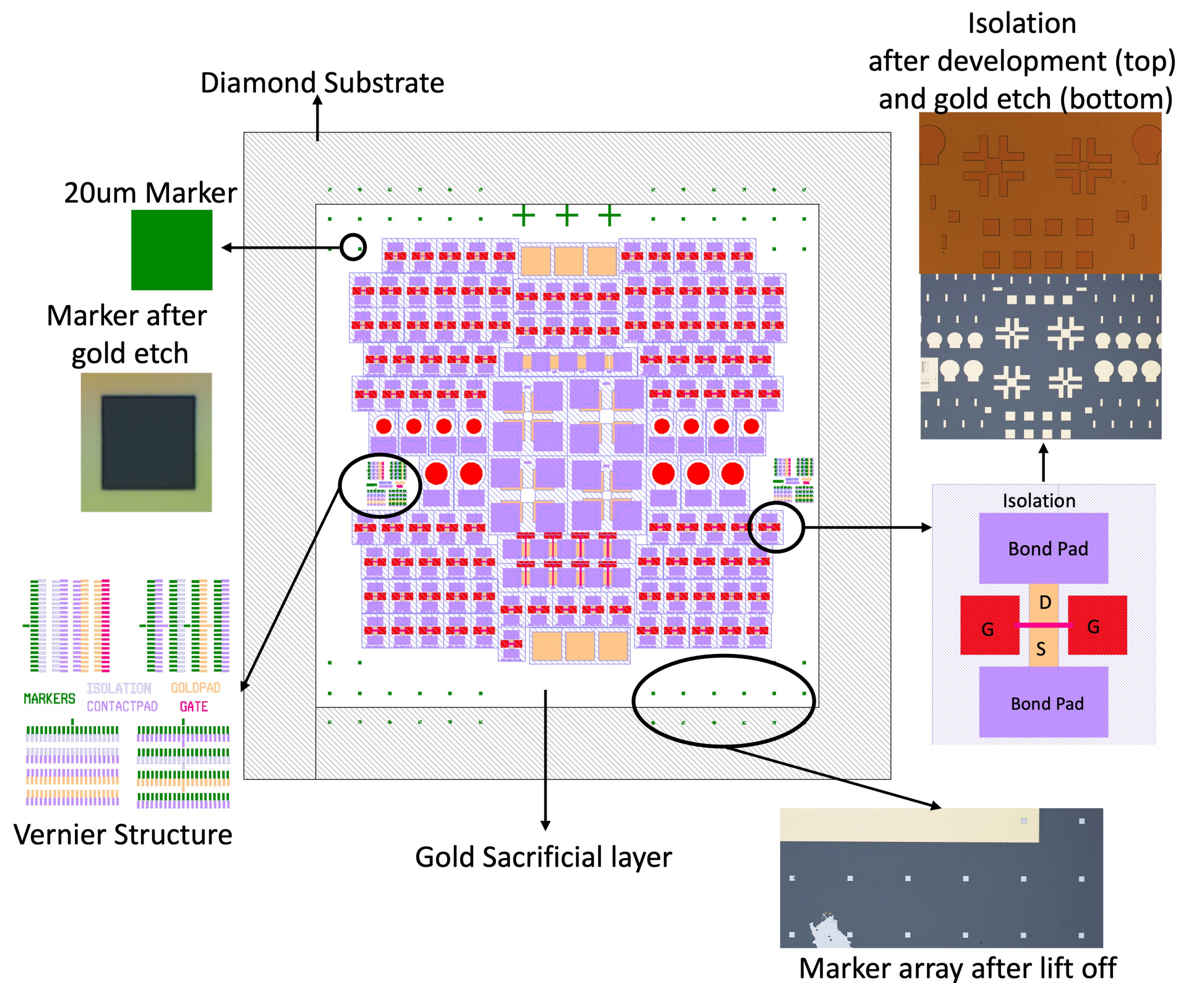


Figure 4.27: The L-edit design of MOSFETs and images of isolation and marker structure.

Ohmic Contact

In contrast to photolithography, where the ohmic contact is formed from the gold sacrificial layer, ebeam lithography employs an addition method to apply ohmic contact to the sample, offering more choices for the ohmic metal. Therefore, a double layer of PMMA is used in this step to create an undercut for the lift-off process. A CDL is sputtered on the double layer of PMMA and later removed by gold wet etch. The PMMA is exposed, developed and ashed to remove all the resist from the area where the ohmic pad will be placed. Subsequently, room temperature gold wet etching is utilized to remove the gold and create an opening for ohmic pad deposition. The next step involves using ebeam PVD to evaporate 80nm of Palladium onto the sample surface, followed by a 4-hour acetone soak in 50 °C water bath to complete the lift off process.

The choice of different ohmic metals in ebeam lithography is motivated by the observation that the ohmic contact between hydrogen-terminated diamond and Pd exhibits lower contact resistance and better adhesion compared to that of Au. Fabrication and measurements are carried out to verify this assertion, and the experimental results will be discussed in greater detail in the subsequent chapter.

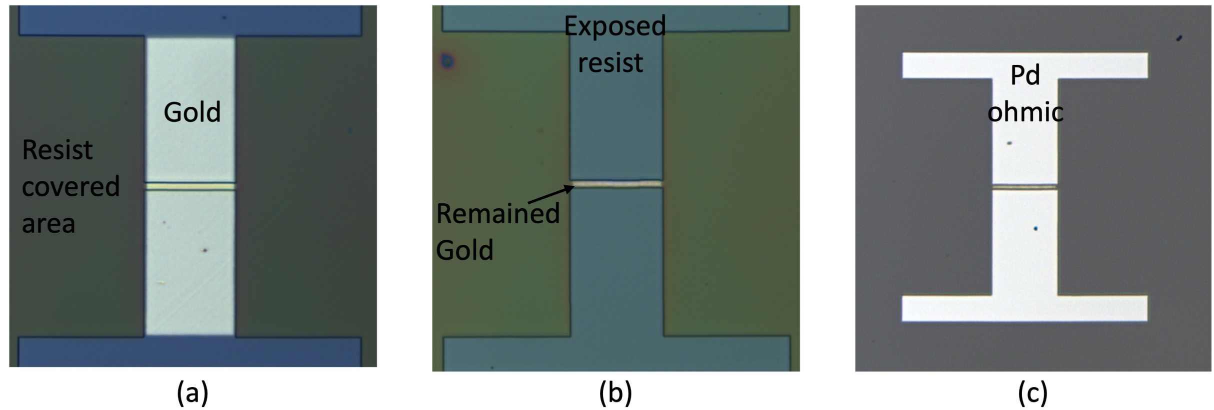


Figure 4.28: Ohmic level optical image.
(a) ohmic pad develop (b) ohmic pad gold etch (c) Pd ohmic lift off.

Oxide deposition

After the fabrication of the ohmic pad on the diamond surface, a blank gold etch is performed to remove all the remaining gold used to protect the hydrogen termination. Then sample is mounted into PLASSYS 5 for ebeam Al_2O_3 deposition. Before the start of the deposition, a one-hour anneal at 350 °C is conducted to desorb the air adsorbates between the source and drain. Subsequently, 35 nm of ebeam Al_2O_3 was deposited on the diamond surface at a rate of 0.02 nm/s.

As discussed earlier, ebeam deposition is non-conformal, meaning that the edge wall can not be uniformly covered with deposition materials. Therefore, to address this issue, 15 nm of thermal ALD Al_2O_3 is deposited on the diamond surface after the ebeam deposition. This 15 nm of ALD Al_2O_3 prevents the gate metal and ohmic pad shorted. The deposition of oxide layer serves as both devices gate dielectric and protection layer over the surface hydrogen termination.

Bond Pad

Bond Pads are placed on the ohmic contact to establish a robust contact for the later measurement. A double layer of ebeam lithography resist is applied by spinning and baking it onto the sample surface. After development and ashing, the area designated for the bond pad is cleaned up. To establish direct contact between the ohmic contact and the bond pad, the oxide on the

bond pad position needs to be removed. To prevent potential damage to the hydrogen termination, wet etching is preferred over dry etching. The sample was immersed in 5% buffered oxide etchant for 45 seconds to eliminate the unwanted oxide on the ohmic contact. Over etching of the oxide layer is necessary to ensure proper contact formation between the bond pad metal and the ohmic contact.

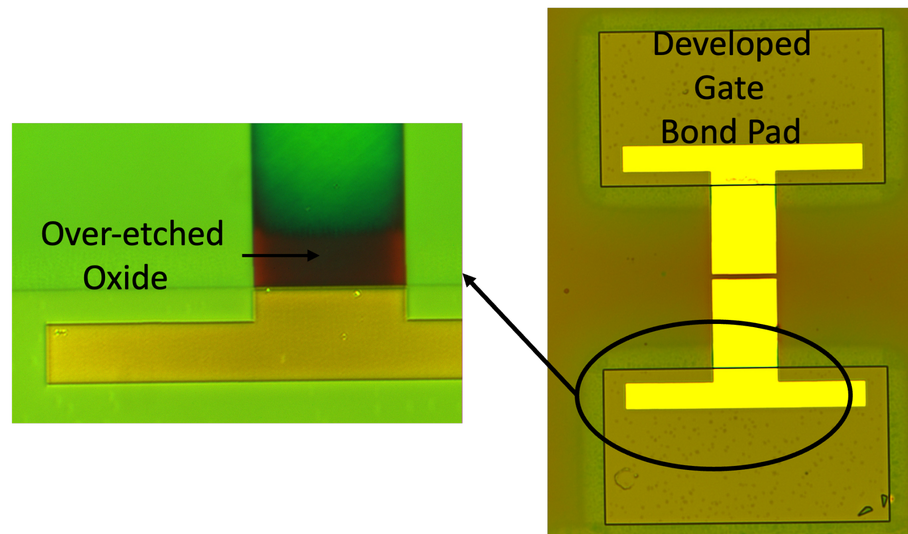


Figure 4.29: Optical microscope image of bond pad oxide etching. The colour contrast shows the evidence of oxide layer over etch.

After wet etching the oxide layer, PVD is employed to deposit a metal stack consisting of 20 *nm* of titanium and 160 *nm* of gold for the bond pad metal stack. Titanium functions as the adhesion layer and enhances the durability of the gold layer. Subsequently, the sample is immersed in acetone with 50 °C water bath for overnight to remove unwanted metal and resist. Figure 4.30 displays the microscope image of the MOSFETs after bond pad lift-off process.

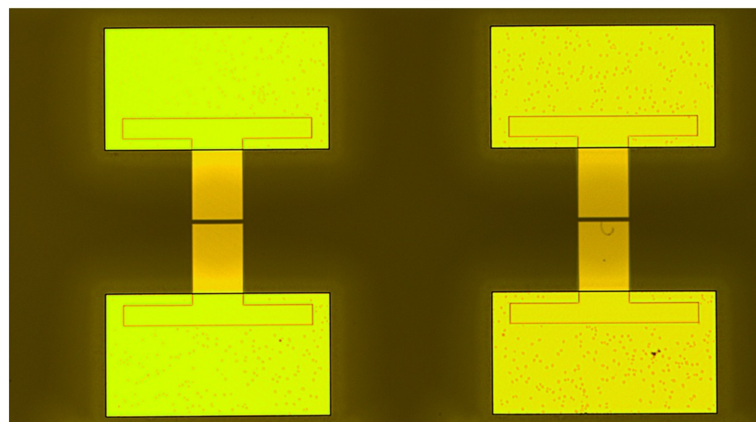


Figure 4.30: Optical microscope image of bond pad after lift off.

Gate

The final structure in this fabrication process is the gate. A double layer of e-beam resist is spun and baked onto the sample surface. The EBPG is utillized to expose the gate area, followed by a 30-second development in a 23 °C 1:1 MIBK:IPA developer to remove the exposed e-beam resist. Then, an 80W oxygen plasma treatment is employed to eliminate the resist residue. The gate metal stack is deposited onto the sample surface using the PVD method. This stack consists of 20 *nm* of aluminium, 20 *nm* of platinum and 100 *nm* of gold, which are evaporated onto the sample surface. The sample is then submerged in acetone at 50 °C water bath overnight for lift-off process.

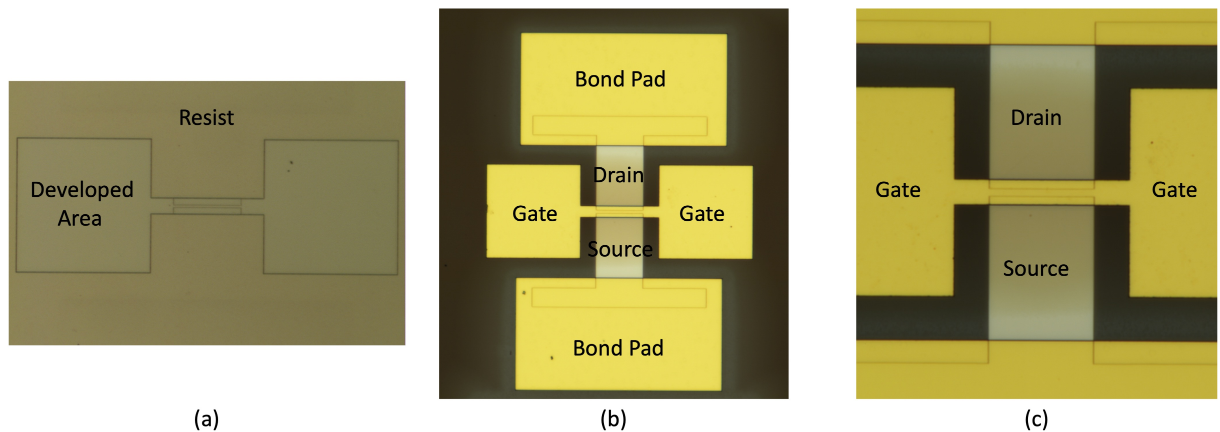


Figure 4.31: Optical microscope image of gate level fabrication.
(a) Developed Sample after metal deposition (b) Gate metal lift off (c) Enlarge part of the gate structure.

4.11 Chapter Summary

This chapter delves into the techniques and processes employed in the fabrication of diamond-based devices, focusing on photo lithography, e-beam lithography, and various physical vapor deposition (PVD) methods. It also discusses the selection and application of different types of resists for lithography, notably the use of double resist layers to create undercut structures.

The chapter provides a detailed exploration of each fabrication step, including sample cleaning, resist spinning, wet etching and lift-off processes, elucidating the significance of each stage in device manufacturing.

The final sections of the chapter offer comprehensive insights into the fabrication of hydrogen-terminated MESFETs and normally-off MOSFETs, highlighting the intricate procedures involved in their construction and emphasizing the importance of precise execution at each stage of the process.

Chapter 5

Characterisation and Measurement

This chapter includes a variety of techniques applied to characterise and quantify diamond samples and the devices fabricated on the diamond surface. It covers two central parts, which are surface profiling and electrical measurement. Scanning Electron Microscope (SEM), Atomic Force Microscope (AFM) and Contact Profiler Dektak XT are introduced in the part of surface profiling. In the electrical measurement part, Transmission Line Measurement (TLM), Van Der Pauw Measurement (VDP) and Field Effect Transistor (FET) are covered by the fundamental to application.

5.1 Surface Profiling

5.1.1 SEM

In Scanning Electron Microscopy (SEM), a focused electron beam is applied to the sample surface to produce topographical images. Electron beams interact with samples, generating various signal types, including Secondary Electrons (SE), Backscattered Electrons (BSE), Auger Electrons, and Characteristic X-rays [124]. Of these signals, Secondary Electrons and Backscattered Electrons provide the majority of topographic information.

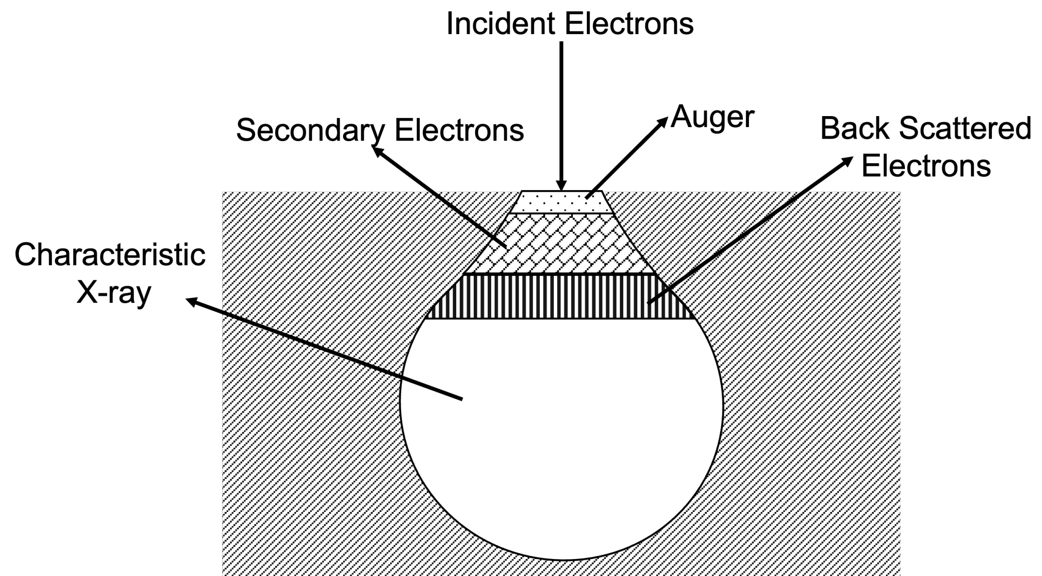


Figure 5.1: Illustration of signals generated by the interaction of incident electrons and the sample surface in Scanning Electron Microscopy.

There are two types of scattering that occur between incident electrons and specimen: elastic scattering and inelastic scattering. [125] Inelastic scattering occurs when incident electrons interact with the atoms and electrons on the sample's surface, resulting in a significant transfer of energy from the incident electrons to the target sample. This process excites loosely bound electrons, known as secondary electrons. Typically, secondary electrons have low energy and escape only a few nanometers from the sample surface before being detected. As a result, secondary electrons provide highly accurate topographic information with a resolution of approximately 10 nanometers[125].

Incident electrons deflect when interacting with the outer shell electrons or atomic nucleus of the sample, resulting in elastic scattering that generates backscattered electrons. Electrons undergoing elastic scattering can retain 60% to 80% of their initial energy. This means that electrons can travel a greater distance before being detected. thereby providing less precise topographic information with a resolution of approximately 1 μm[125].

However, it's important to note that backscattered electrons also contain valuable compositional information. Elements with higher atomic numbers possess more positive charges, leading to the generation of a greater number of backscattered electrons. As a result, the detector captures varying amounts of backscattered electrons from different elements, creating contrast in the final image.

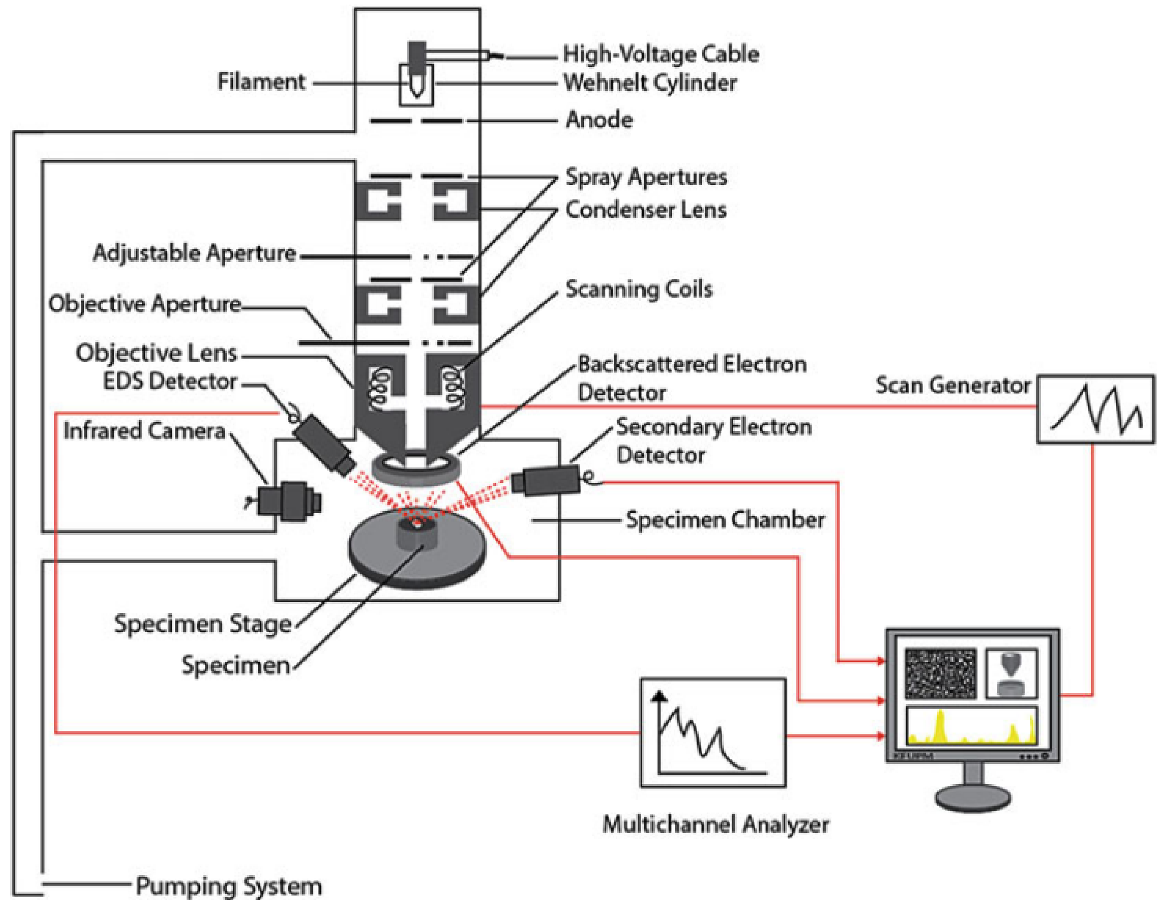


Figure 5.2: General SEM configuration. [126]

Figure 5.2 illustrates the configuration of a scanning electron microscope (SEM). The filament generates electron beams that initially have a width too broad for surface scanning. Consequently, SEM is equipped with a series of lenses to compress and focus this beam. The condenser lenses play a crucial role in converging and collimating the electron beams into a series of parallel streams. Within these condenser lenses, several types of apertures are applied to exclude scattered electrons, which contribute to the sharpness and shape of the electron beams.

Reducing the size of the aperture allows for an increased depth of field and a decrease in the final current, consequently enhancing the resolution of the final image. Before scanning the sample surface, the objective lens refocuses the electron beams to eliminate divergent electron beams. However, contamination on the aperture and defects in the lenses can cause beam profile distortion, leading to stretching of the final image in various directions. This optical defect is referred to as astigmatism. Therefore, stigmators located around the objective lens are employed to correct this beam shape distortion and ensure that the electron beams are focused into a circular pattern.

Focused electron beams are applied to the sample surface and scanned point by point, with control provided by the scanning coils around the objective lens. Electron detectors capture secondary electrons (SE) and backscattered electrons (BSE) by applying bias to the detector[124]. The resulting signals are then displayed on the view monitor.

The scanning electron microscope offers several advantages, including high resolution, high magnification, and the ability to provide both compositional and topographic information. Additionally, with the inclusion of an Energy-Dispersive X-ray Spectroscopy (EDS) detector, excited X-rays from the sample surface can be utilized for elemental analysis.

However, it's important to note that the fundamentals of using electron beams to form images limit the range of suitable samples. When analyzing insulating samples, two common issues that arise are surface charging and image drifting. Furthermore, the application of accelerated high-energy electron beams has the potential to alter or damage the sample surface.

5.1.2 AFM

The Atomic Force Microscope (AFM) is a type of microscope that utilizes the interaction forces between scanning tips and the atoms and molecules on a sample's surface to provide topographic information. This information includes surface roughness, imaging, and the manipulation of surface properties [127].

Figure 5.3 shows the configuration of Atomic Forces Microscope (AFM). Two main interaction forces come into play between the tips and the sample surface. When the tip is far from the surface, forces are negligible. As the tip approaches the sample surface, attractive forces, such as Van der Waals interactions, become dominant and can be sensed even when the tip and sample are separated by more than 10 nm. As the tips continue to move closer to the sample surface, repulsive forces, known as Coulombic interactions, take precedence in the interaction between the tips and the sample surface. The combination of these two types of forces forms the interaction curve between the sample surface and the tips[128].

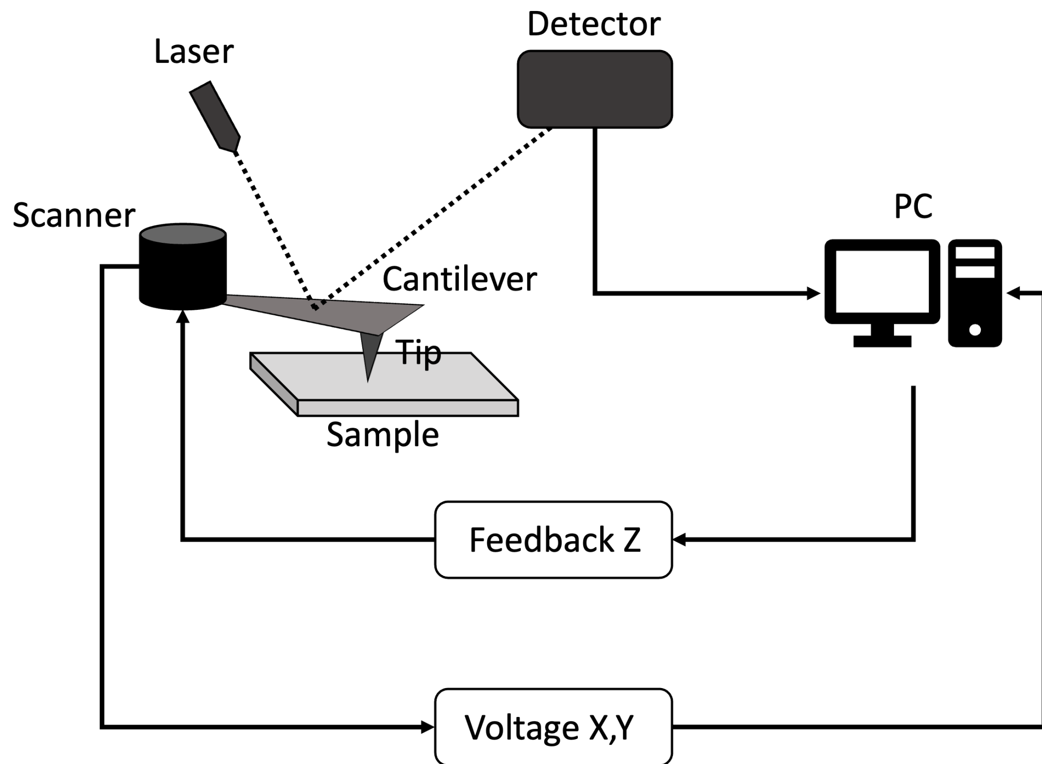


Figure 5.3: General configuration of Atomic Force Microscopy

These interaction forces cause slight movements in the connected cantilever, which are recorded by a focused laser beam. Consequently, the signal can be translated into a topographic image of the sample.

The cantilever is connected to a scanner constructed from piezoelectric material, which enables precise control of the tip's movement along the X, Y, and Z axes. By applying voltage to the scanner, it undergoes deformation, effectively maneuvering the tips across the sample surface[129].

When the tips make direct contact with the sample surface during the scanning process, they can easily become blunted or damaged. To prevent this, most AFMs employ a feedback circuit. This circuit maintains a constant distance between the tips and the sample surface by adjusting the tips' position up and down. This not only reduces damage to the AFM tips but also protects the delicate sample surface.

Several parameters are used to adjust the feedback system. The "setpoint" is the value for the amplitude or deflection that the feedback system aims to maintain. "Feedback gains" determine how quickly the system responds to the scanning signal. A slow scan rate and high feedback gains are typically chosen to achieve better scanning results. However, setting the feedback gains too high can lead to an unstable and oscillating system, causing high-frequency noise in

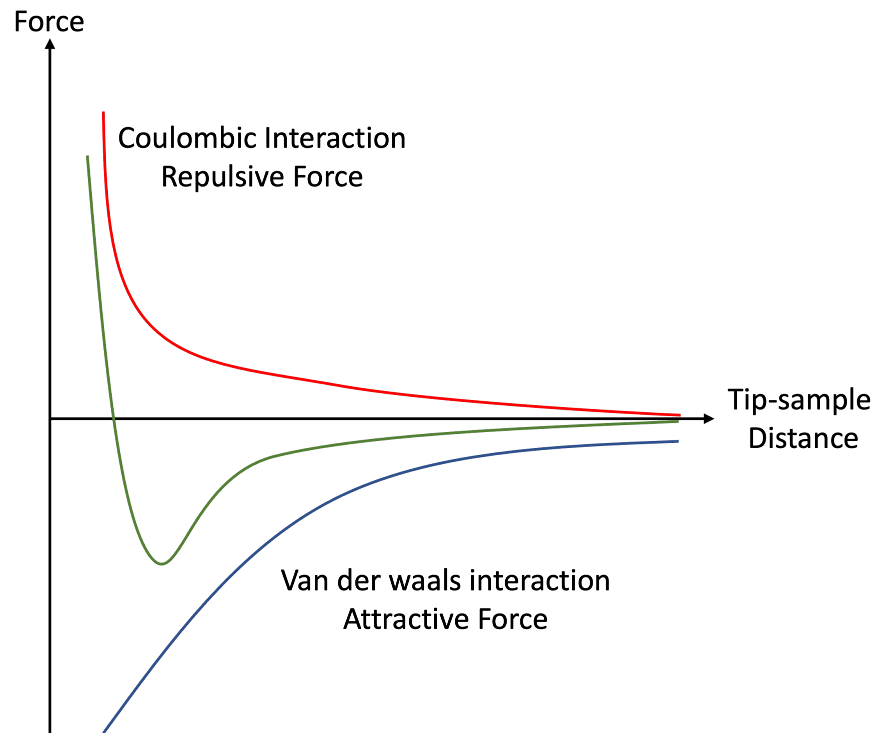


Figure 5.4: AFM tips and sample surface interaction curve.

the final image.

Tapping mode and contact mode are two fundamental operating modes in AFM[127]. In contact mode, the tips maintain continuous contact with the sample surface to collect topographic information. In contrast, tapping mode involves the vibration of the tips above the sample surface with intermittent contact. This approach prolongs the lifespan of the tips and reduces lateral forces. However, it's worth noting that the scanning speed in tapping mode is generally slower compared to contact mode.

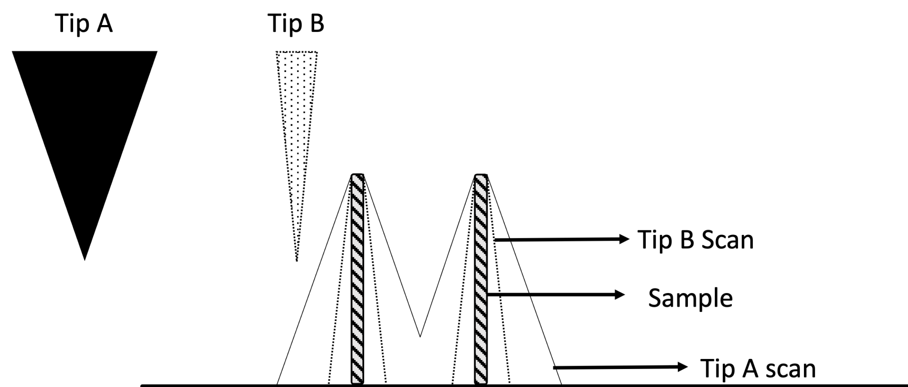


Figure 5.5: Image of different width of AFM tips scan a surface with high aspect ratio and density.

AFM data collection is susceptible to several common artifacts resulting from the tips, scanner, feedback, and ambient vibrations. The final AFM image is a convolution of the sample's topography and the tip's shape. Consequently, when the sample exhibits a larger aspect ratio than that of the tip, the scan results may be misrepresented. To obtain accurate results for samples with high aspect ratios, equally sharp tips are essential. This effect can lead to blind spots when scanning high-density features with wide tips. Figure 5.5 illustrates how tip thickness influences the final scan results. Additionally, there are other tip-related artifacts, such as multiple images caused by chipped tips, as shown in Figure 5.6.

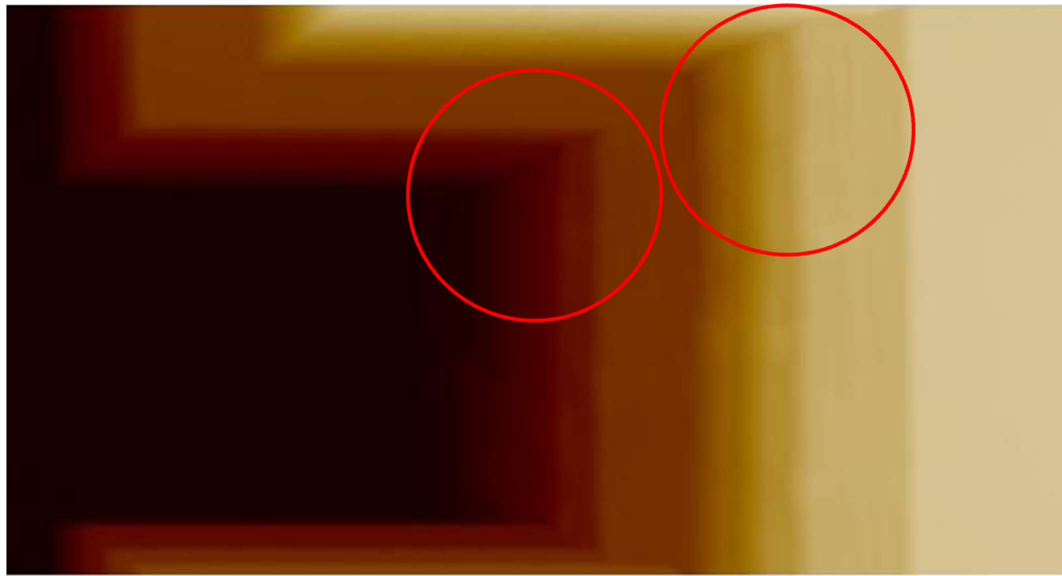


Figure 5.6: Double image caused by chipped AFM tip.

Scanner-related artifacts occur when the piezoelectric material exhibits non-ideal behavior, such as creep, non-linearity, and hysteresis[128]. These artifacts become noticeable when there are image distortions in the results.

Feedback-related artifacts emerge when there is a poor trace and retrace trajectory or when the gains are set too high. In the scanned image, these two feedback-related artifacts result in blurred images or high-frequency noise.

Lastly, ambient vibration-related artifacts typically manifest as horizontal bands in the image.

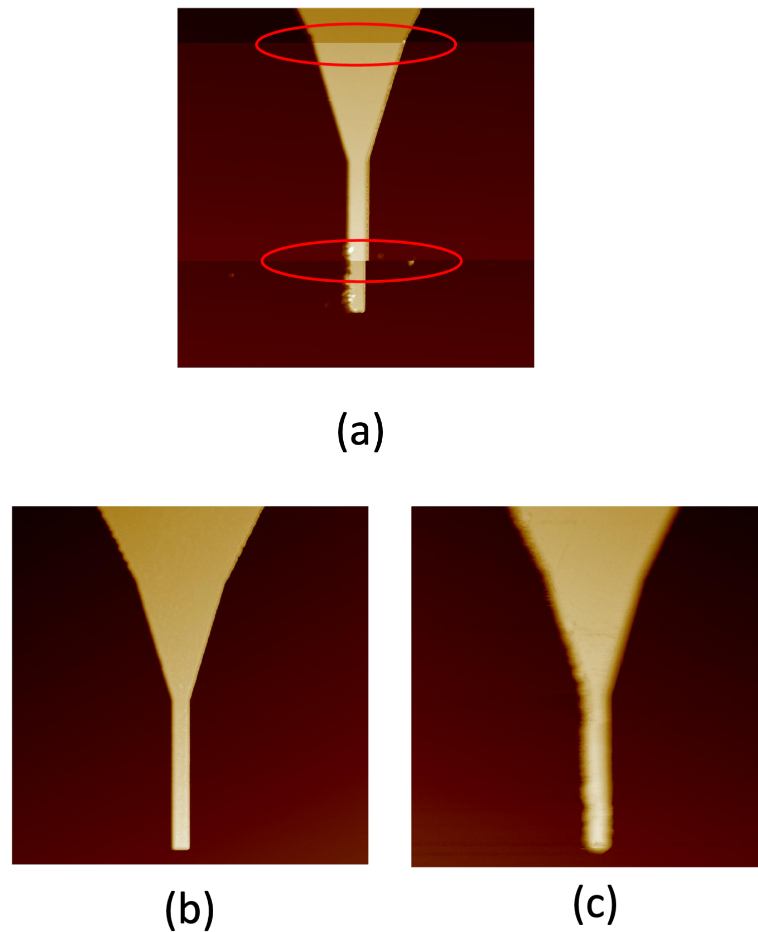


Figure 5.7: Scanner and Feedback-related artifacts of AFM
(a)Scanner creep related artefacts (b) Image with good trace and retrace tracking (c) Image with bad trace and retrace tracking causes feedback related artefacts.

5.1.3 Surface Profiler DektakXT

Surface Profiler Dektak XT is an equipment for step height measurement with a vertical resolution of 0.01 *nm* on 6500 *nm* range. Figure 5.8 shows the configuration of Surface Profiler.

Beneath the bridge structure, a sensor crafted from piezoelectric material and a stylus composed of diamond come together to create a measurement and feedback circuit, facilitating the collection of surface information. Initially, the measurement head descends to ensure that the stylus makes contact with the sample's surface. Subsequently, as the stylus traverses the surface, encountering raised or depressed features, it undergoes displacement either upward or downward. The sensor generates electrical signals that correspond to the stylus's displacement. Consequently, a computer processes these electrical signals, constructing a surface image of the measured area.

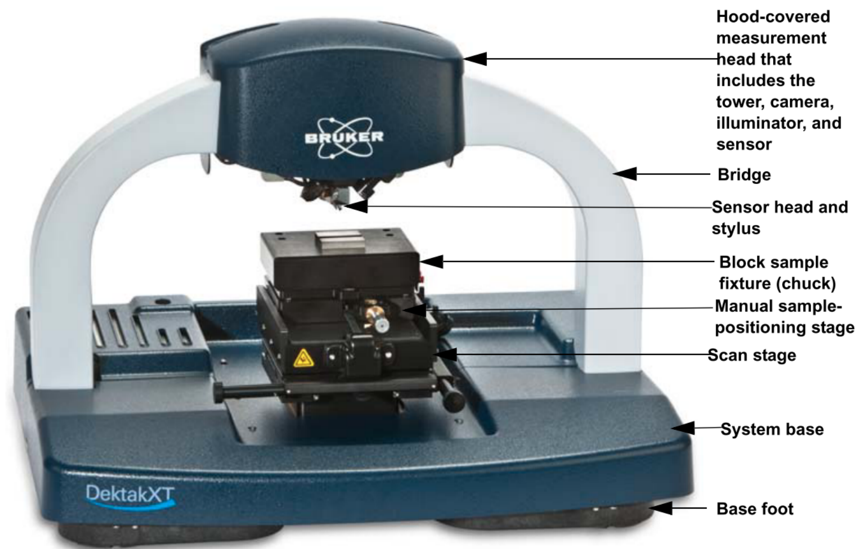


Figure 5.8: Configuration of Surface Profiler Dektak XT. [130]

The Surface Profiler DektakXT is widely employed for step height measurements. When compared to the Atomic Force Microscope (AFM), the Surface Profiler offers distinct advantages. It can scan larger areas at significantly higher rates, and its operation is generally more user-friendly than that of the AFM. However, the Surface Profiler has a noticeable drawback. Despite the ability to adjust the contact force, there is a risk of surface scratching by the stylus after measurements. Furthermore, the Surface Profiler is limited to scanning along a single axis, either the x-axis or y-axis, which means it cannot be used to characterize two-dimensional surface areas.

5.2 Electrical Measurement

5.2.1 Transmission Line Measurement (TLM)

Transmission Line Measurement (TLM) is used to measure contact resistance (R_C) between the ohmic metal and semiconductor as well the sheet resistance (R_S) of the semiconductor.

A series of same size ohmic contact metal are deposited on the semiconductor surface with vary distance (L_x) between each two adjacent pads. When a bias applied on two adjacent contact pads, current against voltage curve gives the resistance (R_T) between those two pads.

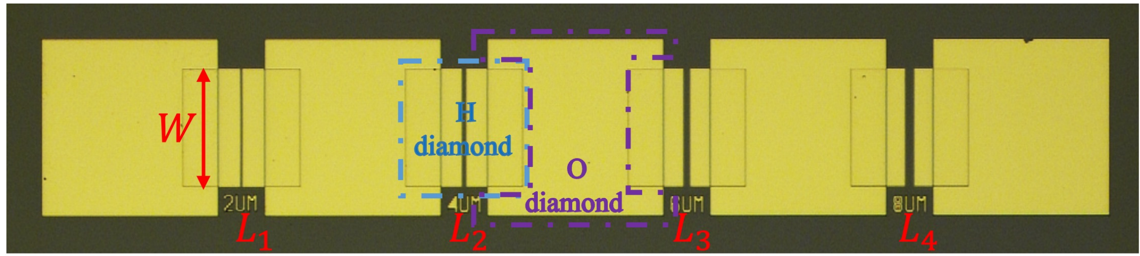


Figure 5.9: Optical Microscope Image of TLM structure on hydrogen terminated diamond surface.

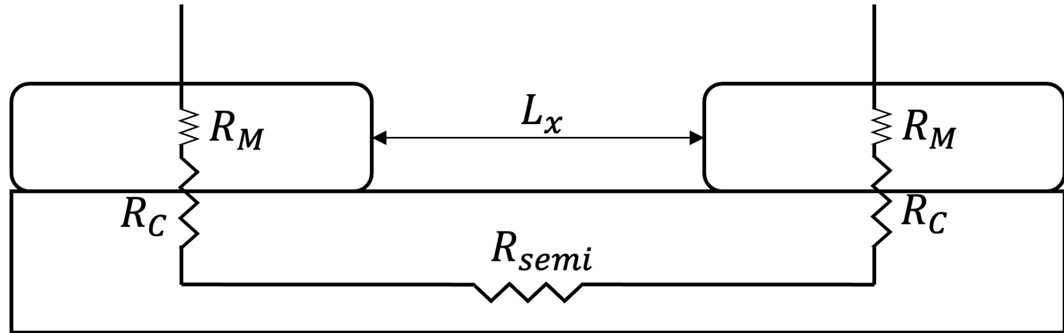


Figure 5.10: TLM gap graph.

The resistance measured above contains the resistance from three different parts those are the resistance between probes and ohmic metal R_M, contact resistance R_C and the semiconductor resistance R_{semi}.

$$R_T = 2R_M + 2R_C + R_{semi} \tag{5.1}$$

Since typically $R_M << R_C$, R_M is negligible, 5.1 can be simplified to,

$$R_T = 2R_C + R_{semi} \tag{5.2}$$

Because

$$R_{semi} = R_S \frac{L}{W} \tag{5.3}$$

where R_S is the sheet resistance, then we can get

$$R_T = 2R_C + \frac{R_S}{W} L \tag{5.4}$$

With applying bias on each two adjacent ohmic pads, R_T against L_x curve can be plotted as figure 5.11.

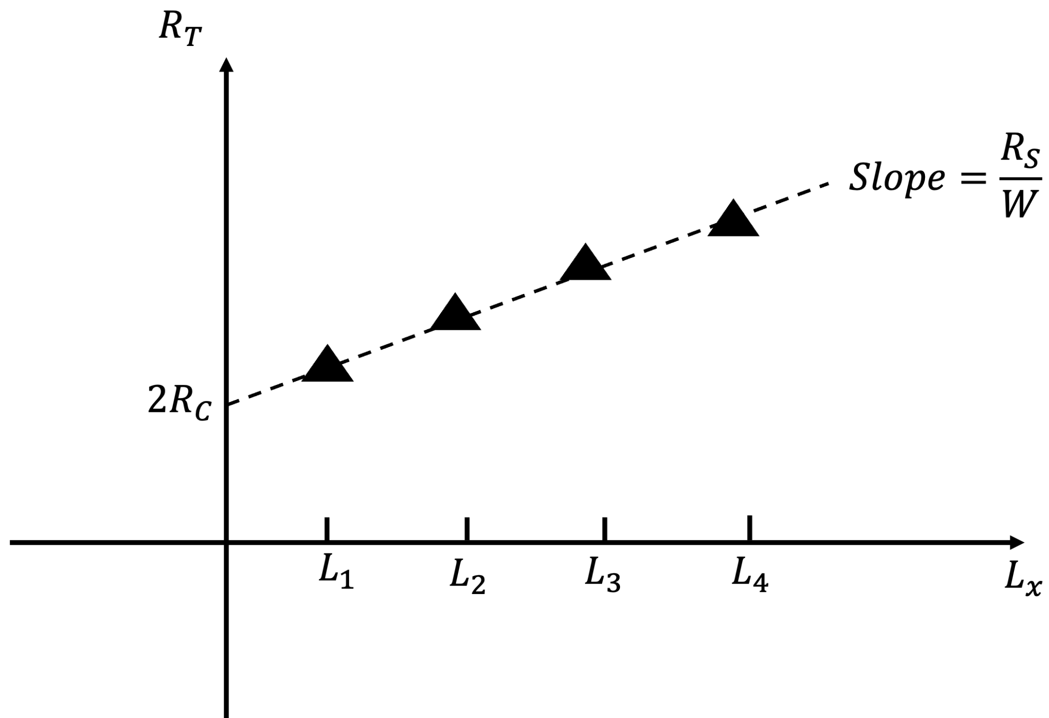


Figure 5.11: Ideal Plot of R_T against L_x.

5.2.2 Van Der Pauw Measurements (VDP)

Van der Pauw structure is an efficient way to characterise electrical properties, such as carrier mobility, carrier concentration, sheet resistance and carrier polarisation.

Figure 5.12 shows one of the basic principles (Hall effect) used for VDP structure to characterise the carriers properties. A magnetic field (B) applied perpendicularly to the surface of the substrate, in a direction perpendicular to the flow of electric current (I), propels electrons to move towards both sides of the substrate. The direction of electron movement is perpendicular to both the current and the magnetic fields. This behaviour leads to the accumulation of charges on both sides of the substrate, creating an internal electric field. As the number of charges increases, the newly generated internal electric field balances the force exerted on moving charges by the external magnetic field. Therefore, the moving charges can continue to move along the direction of the current. The potential associated with the electric field generated by the accumulated charges if known as the Hall voltage or V_h.

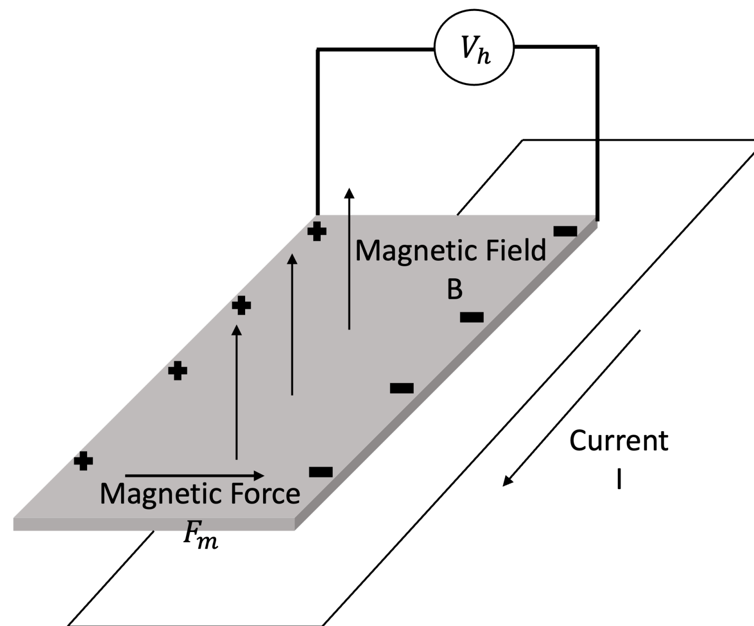


Figure 5.12: Hall effect

Nanometrics 550 Hall Kit 4 probes system is used for sheet resistance and hall coefficient measurement. Figure 5.13 shows the configuration of the equipment. Two of those probes push current through the sample surface and the other two measure the bias on the other two pads.

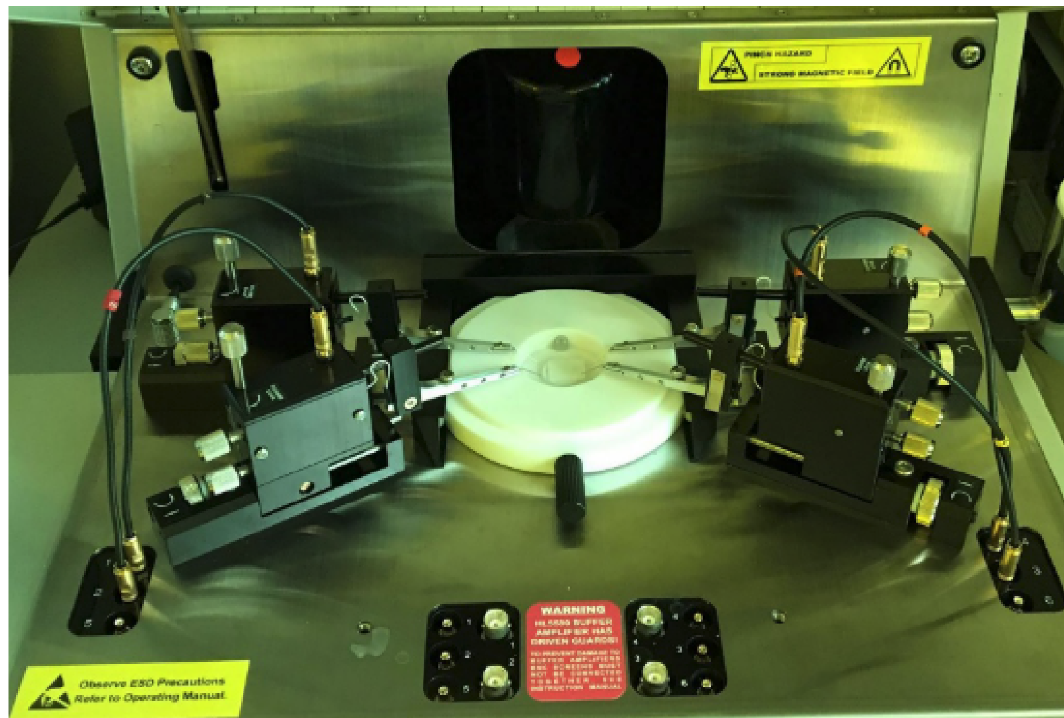


Figure 5.13: Nanometrics 550 Hall Kit 4 probes hall measurement system.

Figure 5.14 illustrates a microscope image of the VDP structure fabricated on a hydrogen terminated diamond surface. The middle hydrogen terminated area is designed to restrict the current

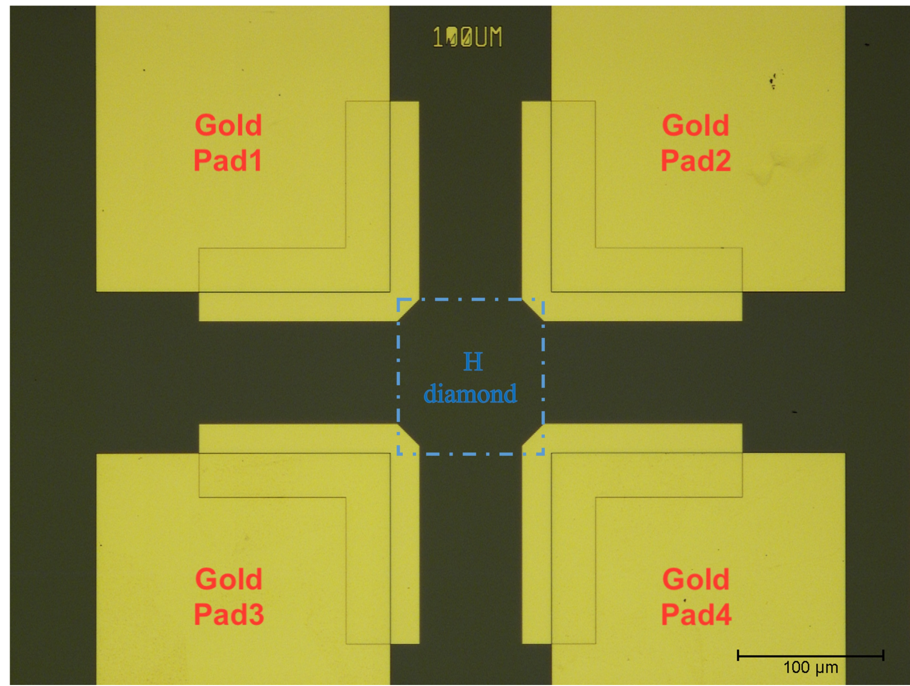


Figure 5.14: Microscope image of VDP structure for hall effect measurement.

flow and make sure a symmetric geology for the measurement which improve the carrier properties and sheet resistance measurement accuracy. The isolation is accomplished by oxygen plasma, and isolation structure was used to test the isolation. More details can be found in Chapter 4. When the probes get contact with pad 1 and pad 2, they inject current (I) into the structure, and the resulting voltage (V) can be measured by the other two probes over pad 3 and pad 4. These values of I and V are used to calculate the resistance (R_1). Subsequently, the probes apply current through pad 1 and pad 3 while measuring the voltage across pad 2 and pad 4 to obtain a second resistance (R_2). In the case of a uniform conducting sample surface, R_1 and R_2 should have the same value. Therefore, the sheet resistance can be calculated as follow,

$$R_S = \frac{\pi R}{ln2} \tag{5.5}$$

When the current flows through pad 1 and pad 4 with a positive magnetic field applied to the substrate, Hall voltage (V_h) can be measured across pad 2 and pad 3 using the other two probes. This process is then repeated by applying a negative magnetic field. The polarisation of the measured V_h indicates whether the majority carriers are holes (p-type) or electrons (n-type). Equation 5.6 demonstrates how to calculate hall coefficient using the measured V_h, applied current I and magnetic field B.

$$R_h = \frac{V_h}{IB} \tag{5.6}$$

With hall coefficient, the carrier concentration and mobility can be calculated as following equation, where n_s is the 2D carrier concentration, q is the unit charge, and μ is the carrier mobility.

$$n_s = \frac{1}{qR_h} \tag{5.7}$$

$$\mu = \frac{R_h}{R_S} \tag{5.8}$$

Hall measurement is crucial for characterizing the hydrogen terminated diamond surface. It is used to measure the surface conductivity degradation after completing the fabrication process. Additionally, mobility measurement contribute to the understanding of charge transport under low electric fields.

5.2.3 Field Effect Transistor (FET)

To understand the quality of transistor on hydrogen terminated diamond surface, it's necessary to carry out DC measurements on the devices. The measurement includes the output characteristics measurement, known as $I_d - V_d$ curve, and transfer characteristics measurement, known as $I_d - V_g$ curve.

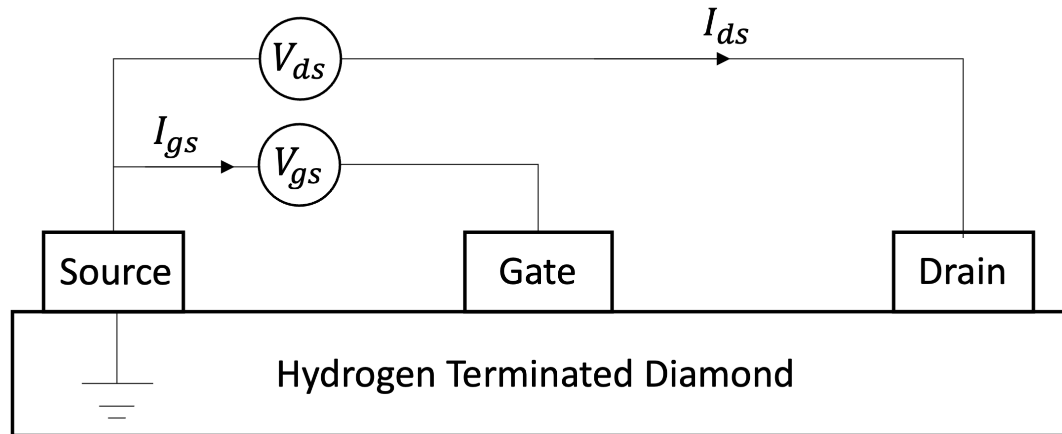


Figure 5.15: Simplified FET DC characteristics graph.

Output Characteristics

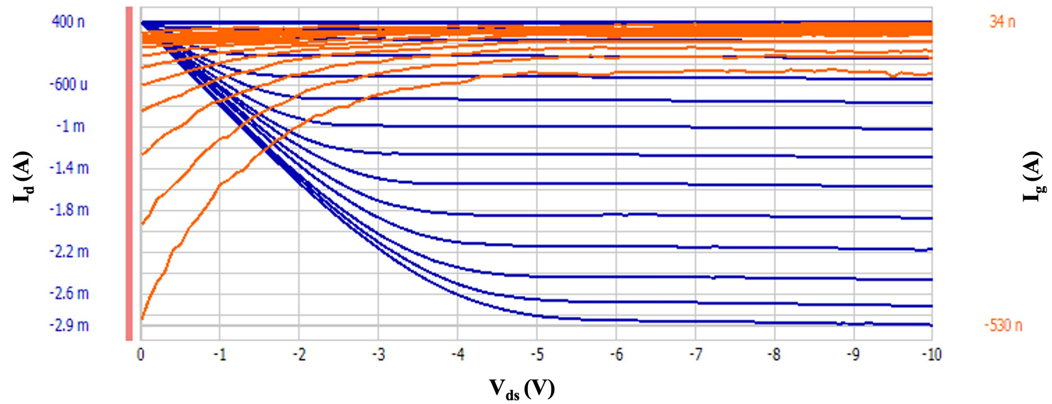


Figure 5.16: Example FET output characteristics.

Three probes are used to perform DC measurements with the source grounded. In the output characteristic, known as I_dV_d graph, voltage is applied and swept between the source and drain. The bias applied between the gate and source is stepped after each sweep between the source and drain. This measurement is used to obtain the maximum drain current I_{dmax}.

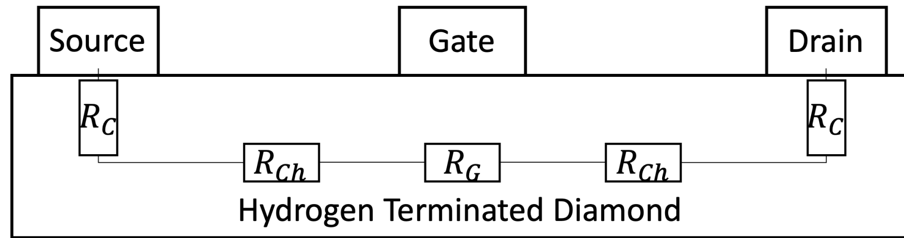


Figure 5.17: Simplified FET DC characteristics for R_{on}

In addition, DC measurement can provide the on-resistance R_{on}. Figure 5.17 demonstrates all the components of resistance included in the on-resistance. As previously discussed, TLM measurement provide information about the contact resistance R_C. According to the measurement result from VDP measurement, one can calculate the resistance between the source-gate channel and gate-drain channel, R_{ch}. When the device operates in the linear region, the on resistance can be calculated by Ohm's Law. With this information, the resistance under the gate, R_G, at a particular gate bias can be extracted.

$$R_{on} = 2R_C + 2R_{Ch} + R_G \tag{5.9}$$

One more important piece of information that can be extracted from output measurement is offstate breakdown voltage. To determine the breakdown voltage, the gate channel is held in the "off" state. In the case of hydrogen-terminated diamond devices, a positive bias is applied on the

gate. Then the voltage applied on the drain is swept from low to high until there is a significant increase in current, at which point the voltage is referred as the breakdown voltage.

Transfer Characteristics

Transfer characteristics ($I_d - V_g$) are obtained by sweeping voltage between the source and gate while incrementally adjusting the bias applied to the drain terminal. Transconductance g_m is an important parameter of a FET device, representing the change in drain current (I_{ds}) at a given drain voltage (V_{ds}) due to a change in gate voltage (V_{gs}). [30] It reflects the efficiency of changing drain current with respect to gate voltage under a given drain voltage.

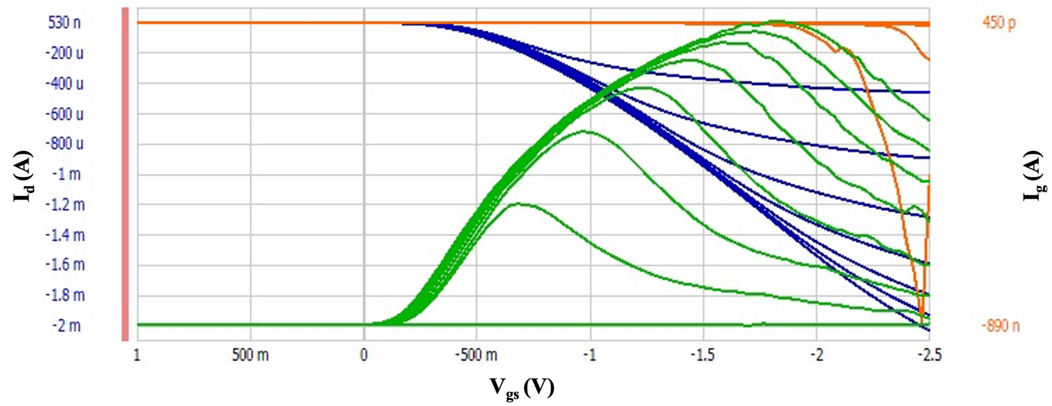


Figure 5.18: Example FET transfer characteristics.

Figure 5.18 shows the transfer characteristics, where the green plot represents the transconductance. In an ideal situation, where the parasitic resistances are neglected, intrinsic transconductance can be described as below,

$$g_m^* = (\frac{dI_{ds}}{dV_{gs}})_{V_{ds}} \tag{5.10}$$

However, if we take into account the voltage drop between the source and gate contacts, extrinsic transconductance can be defined as follows,

$$g_m = \frac{g_m^*}{1 + g_m^* R_s} \tag{5.11}$$

In equation 5.11, R_s represents the resistance between the source ohmic metal and channel region under the gate, and therefore comprises both the source ohmic contact resistance and any potential access resistance associated with the channel between the source and gate contacts, R_{Ch}. As discussed in Chapter Two and outlined in equation 2.4, we know that the drain current

$I_d s$ is a function of the channel's width-to-length ratio (W/L) and carrier's mobility (μ_p). Hence, high carrier mobility and width-to-length ratio contribute to a high transconductance.

Another important parameter extracted from the transfer characteristic is the threshold voltage (V_{th}), which is the minimum voltage required to maintain the conductive channel between the source and drain terminals. There are different methods to extract the threshold voltage. One method involves using peak transconductance to determine V_{th}. In this approach, a gate voltage is identified when the transconductance reaches its peak, and this voltage is then used to find the intersection point between the specific gate voltage and the $I_d - V_g$ curve. The tangent line at this point is used to determine the threshold voltage. The second method involves plotting the $I_d - V_g$ curve on a logarithmic scale. An off-state current is identified, which is then used to extract the threshold voltage. In this work, the second method was used to extract the threshold voltage as the first method can overestimated the value of the threshold voltage.

5.3 Chapter Summary

This chapter provides a detailed examination of the equipment used to characterize both topographic and electrical properties, including AFM, SEM, and Surface Profiler, which are employed to obtain surface images, surface roughness measurements, and step heights. Furthermore, we delve into electrical characterization methods such as TLM and VDP, which offer valuable insights into sheet resistance (R_S), contact resistance (R_C), carrier mobility (μ) and carrier concentration (n_p).

In the latter part of this chapter, we introduce FET device measurements. Output characteristics play a significant role in determining parameters such as maximum current, breakdown voltage, and on-resistance. Additionally, we extract the crucial parameter of transconductance (g_m) and threshold voltage (V_{th}) from transfer characteristics. All these methods collectively contribute to the fabrication of hydrogen-terminated diamond FET devices and enhance our understanding of their behavior.

Chapter 6

Surface Termination Results

As discussed in the previous chapter, plasma-assisted hydrogen termination is currently the most popular and well-developed method for terminating the diamond surface with hydrogen. However, it is noted that hydrogen plasma can roughen the diamond surface [71]. Additionally, the utilization of hydrogen plasma and a high vacuum chamber can result in escalated costs and restricted accessibility to the capability. High-temperature annealing of diamond in a hydrogen atmosphere has also been reported; however, the process typically requires pure hydrogen, a high vacuum environment, or diamond with large surface area such as diamond powder [73]–[75].

This chapter explores a new method, known as "Spillover", for terminating the diamond surface. The aim of this process is to utilise a lower-cost and more accessible method for terminating the surface of the diamond wafer with hydrogen, without the need of a high vacuum chamber or pure hydrogen.

6.1 Initialisation experiment

Single polished CVD diamond wafer provided by Element Six with a (100) surface orientation and dimensions of $4.7 \times 4.7\ mm$ were used. To remove any potential hydrocarbon and oxygenated compounds from the sample surface, the samples were immersed in freshly prepared aqua regia ($HNO_3 : HCl$ in a 1:1 ratio) and boiled on a hotplate for 10 minutes. Subsequently, a boiled solution consisting of a mixture of $H_2SO_4 : HNO_3$ in a 3:1 ratio was employed for oxidation to achieve a fully oxygen-terminated diamond surface and to remove any other metal contamination.

The sheet resistivity of samples was measured using a Nanometrics HL5500PC Hall Effect measurement system. Four probes made direct contact with the diamond surface. After the

acid cleaning step described above, the measurement four probes hall results indicated that all samples surface were insulating, suggesting that the samples are most likely oxygen terminated as the second oxidation step of the acid cleaning process mainly designed for surface oxygen termination.

Subsequently, PLASSYS II was employed for the deposition of platinum (Pt) onto the diamond samples, with a thickness of 100 nm and a deposition rate of 1 nm/s. To ensure that only one edge of the sample was covered with metal, a cleaned silicon shadow mask was utilized. Figure 6.1 illustrates the method used for mounting the samples on the holder.

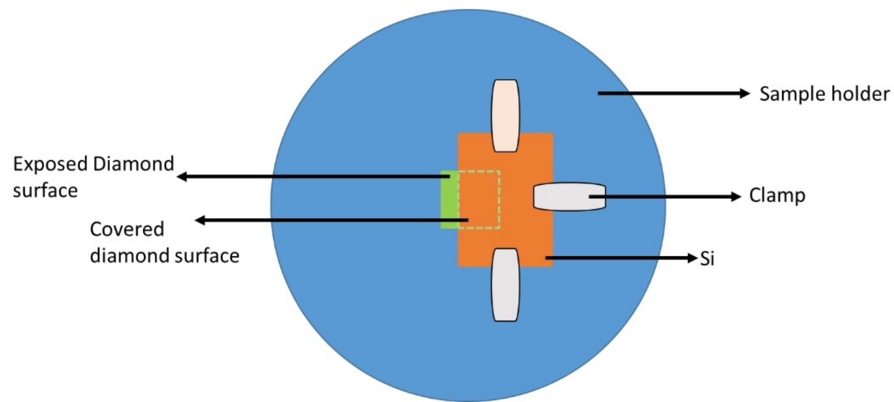


Figure 6.1: Image of masking the samples for metal deposition.

The spillover process was conducted in the School of Chemistry at the University of Glasgow. Prior to initiating the spillover experiment, the samples underwent degassing in a vacuum at 1×10^{-3} $mbar$.The temperature of the furnace was then gradually increased to either 800 °C or 900 °C at a rate of 5 °C/min and held at that temperature for 30 minutes. This degassing process was implemented to attempt to cleanse the diamond samples' surface and desorb all oxygen termination from the surface, leaving free dangling carbon bonds. It has been reported that the oxygen termination on diamond surface desorb at 600°C under vacuum (1×10^{-3} $mbar$) and 900°C for hydrogen termination [92].

Subsequently, the furnace temperature was then reduced to 500 °C at a rate of 5 °C/min. Once the temperature stabilized, a mixture consisting of 5% of H_2 and 95% of Ar was introduced into the furnace to terminate the diamond surface. The termination process varied in duration, followed by the cooling of the furnace to room temperature.

Results

The first experiment for sample one was conducted with the following parameters: 800 °C for 30 minutes for the degassing step, followed by 500 °C for 4 hours for the Spillover step. After the Spillover, the 4 probes hall measurement shows that only the area near the metal strip is

conducting. However the sheet resistance (3.6×10^5 $\Omega/\square$) was observed to be one order of magnitude higher than that typically reported for diamond hydrogen terminated by hydrogen plasma.

Sample	Degassing (°C)	Duration	Spillover (°C)	Duration	$R_s(\Omega/\square)$
Sample1	800	0.5	500	4	3.6×10^5
Sample1	800	2	500	4	4×10^4
Sample1	900	2	500	12	1.6×10^4
Sample2	800	0.5	500	4	$> 2 \times 10^6$
Sample2	900	2	500	12	1.5×10^4
Sample3	800	1	500	4	$> 2 \times 10^6$
Sample3	×	×	500	12	$> 2 \times 10^6$

Table 6.1: Experiment parameters of three different samples.

In the second experiment, the degassing duration was extended from 30 minutes to 2 hours, while all other parameters remained the same as the first experiment. The 4 probes hall kit measurement indicated that the sheet resistance (4×10^4 $\Omega/\square$) was one order of magnitude lower than in the first experiment.

For the last experiment, the degassing temperature was increased to 900 °C for 2 hours, and the termination step was prolonged to 12 hours. Consequently, the sheet resistance dropped to 1.6×10^4 $\Omega/\square$. However, it was noted that the conductivity on the surface was not continuous.

Two sets of experiments were conducted on sample two. 800 °C 30 minutes degassing and 500°C 4 hours Spillover was conducted in the first set of experiments. The 4 probes Hall measurement indicated that the surface remained insulating after the experiment.

For the second set of experiments, the degassing temperature and duration were increased from 800°C 30 minutes to 900°C 2 hours, and the Spillover duration was extended from 4 hours to 12 hours. The 4 probes hall kit measurement revealed that the surface became conducting after the spillover, with a sheet resistance of 1.5×10^4 $\Omega/\square$.

Two sets of experiments were designed for the third sample. In the first experiment, the degassing process involved heating to 800 °C for 1 hour to desorb the oxygen termination, followed by 500 °C for 4 hours for the hydrogen termination process. However, the Hall measurement showed that the surface remained insulating after the experiment.

In the second experiment for the third sample, the degassing process was omitted, and a 12-hour termination step at 500 °C was utilized to terminate the surface. Nevertheless, the surface remained insulating after the experiment.

The three sets of experiments conducted on sample one demonstrate that a degassing process

involving higher temperature (900 °C) and longer duration (2 hours) leads to an improvement in surface conductivity by one order of magnitude. Furthermore, prolonging the spillover duration also contributes to enhancing termination results.

The two sets of experiments carried out on sample two, repeating the first and the last sets of experiments conducted on sample one, confirm that a degassing temperature of 900 °C for 2 hours and a 12-hour spillover with hydrogen gas inlet are the optimal parameters for hydrogen-terminating the diamond surface. This observation is assumed to be attributed to the increased efficiency of oxygen desorption at 900 °C. However, more study in details need to be done to confirm the assumption.

In the first set of experiments on sample three, only the degassing duration was extended. The insulation of the diamond surface after the spillover indicates that the temperature used for degassing is more critical than the duration. Additionally, the last set of experiments conducted without a degassing process indicates the necessity of the degassing process for the subsequent termination process. It is assumed that this is because the degassing process desorbs the oxygen termination, exposing free dangling carbon bonds that can bond with hydrogen atoms during the spillover process.

Overall, these experiments confirm the necessity of the degassing process and explore the optimal parameters for both the degassing and spillover processes. Two additional sets of experiments were designed and completed to verify the efficacy of the spillover process.

6.2 Spillover with optimal parameters

As both Pt and Pd have been well studied as catalytic metals for the spillover process [131], [132], in this experiment, both metals were introduced as new variables to explore whether different catalytic metals affect the hydrogen termination of the diamond surface.

Three polished CVD diamond samples with surface roughness between 1nm to 2nm, designated as SC16, SC22 and SC10, were provided by Element Six, with a (100) surface orientation and dimensions of $4.7 \times 4.7\ mm$. The same acid and solvent cleaning process employed in the initialization experiment was carried out to clean and oxidize the diamond surface. Subsequently, 4 probes Hall kit measurements were conducted to confirm that all sample surfaces were insulating.

Next, the contact angle of the surface was measured using the KRUSS DSA30 Drop Shape Analyser to assess surface wettability. It has been reported that an oxygen-terminated diamond surface can transition from hydrophilicity to hydrophobicity with surface termination changing to hydrogen [133]. The water dose was optimized at $0.5\mu l$ to achieve the highest accuracy of the

measurement. Following this measurement, a methanol cleaning step was performed to remove any potential contamination residues.

PLASSYS II was utilized for the deposition of platinum (Pt) with a thickness of 100 nm on sample SC22, while PLASSYS IV was employed for the deposition of 100 nm of palladium (Pd) on sample SC16. The deposition rates for Pd and Pt were 0.3 nm and 1 nm per second, respectively. Pd and Pt act as catalyst to split hydrogen molecular into atoms which are expected to connect with the free dangling carbon bonds to hydrogen terminate the diamond surface [86], [134]. Sample SC10 was set as a blank control experiment where no metal was deposited on the sample surface. 5 minutes ultrasound alcohol (IPA) followed with a 5 minutes ultrasound acetone cleaning was conducted after the metal deposition to remove potential contamination induced by the holder and silicon shadow mask. Subsequently, the sample surface roughness was measured by atomic force microscopy (AFM).

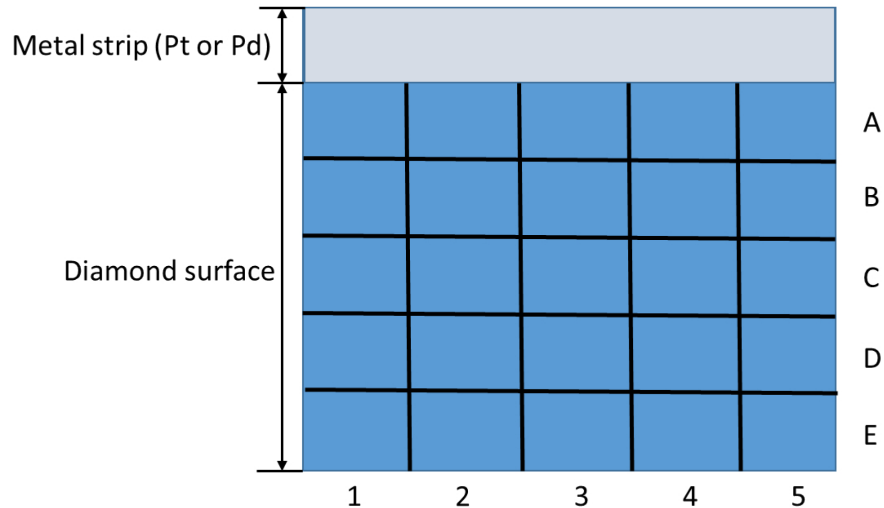


Figure 6.2: Diamond sample were split into 25 areas and 4 probes hall measurement is carried in each area following Spillover.

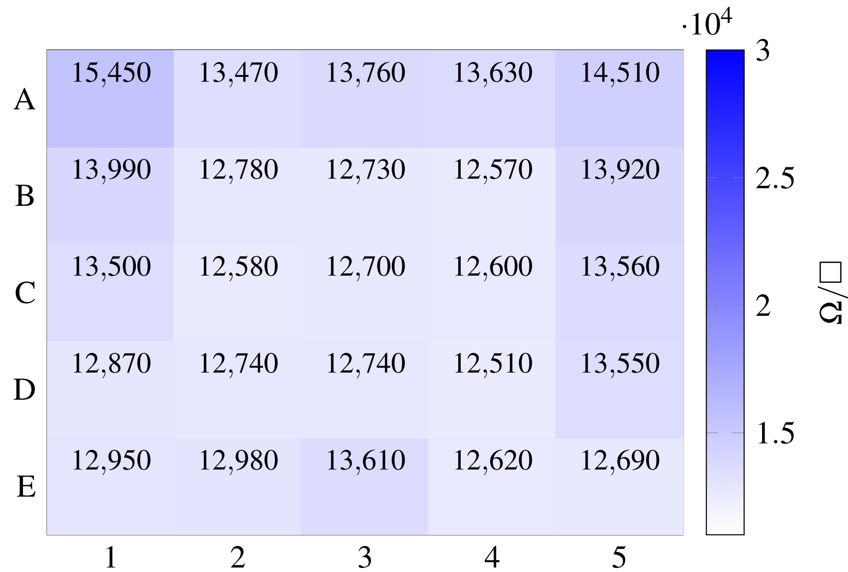
Simlilar to previous experiments, the spillover process was conducted in the School of Chemistry. Prior to the start of the spillover, both samples were degassed in a vacuum at 1×10^{-3} $mbar$. The temperature of the furnace was then raised to 900 °C at a rate of 5 °C per minute and held at 900 °C for 2 hours.

Subsequently, the furnace temperature was reduced to 500°C at a rate of 5°C per minute. Once the temperature stabilized, a mixture consisting of 5% H_2 and 95% Ar was introduced into the furnace to terminate the diamond surface. The termination process lasted for 12 hours, followed by the cooling of the furnace to room temperature.

A series of measurements were performed on the surface to characterize the samples. To investi-

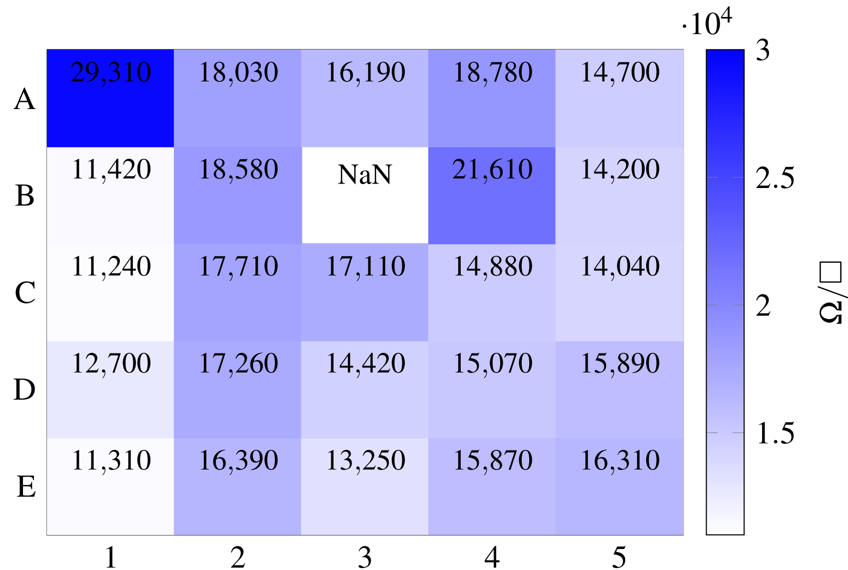
gate whether the surface conductivity changes with increasing distance between the sample and the metal strip, the samples were divided into 25 areas, and Hall measurements were conducted on each small area of the diamond surface. Additionally, atomic force microscopy (AFM) was utilized to characterize the surface roughness, and contact angle measurements were performed to confirm that the surface termination had been altered.

Four Probes Sheet Resistance Measurement



	1	2	3	4	5
A	15,450	13,470	13,760	13,630	14,510
B	13,990	12,780	12,730	12,570	13,920
C	13,500	12,580	12,700	12,600	13,560
D	12,870	12,740	12,740	12,510	13,550
E	12,950	12,980	13,610	12,620	12,690

Table 6.2: Sheet resistance of SC16 after spillover (100nm of Pd strip).



	1	2	3	4	5
A	29,310	18,030	16,190	18,780	14,700
B	11,420	18,580	NaN	21,610	14,200
C	11,240	17,710	17,110	14,880	14,040
D	12,700	17,260	14,420	15,070	15,890
E	11,310	16,390	13,250	15,870	16,310

Table 6.3: Sheet resistance of SC22 after spillover (100nm of Pt metal strip).

The initial results we are discussing pertain to the Hall measurements. Prior to the spillover process, the surfaces of both samples were found to be insulating. However, after the experi-

ment, both samples exhibited surface conductivity similar to that reported for sheet resistance of plasma hydrogen-terminated diamond i.e. $\approx 10\ K\Omega/\square$ [69], [135].

Sample SC16, with palladium (Pd) as the catalyst, demonstrated an average conductivity of $13.2\ k\Omega/\square$. Notably, this sheet resistance was slightly lower than that of sample SC22, which utilized platinum (Pt) as the catalyst metal, showing an average resistance of $16.9\ k\Omega/\square$.

As detailed in the experimental section, the surfaces of all three samples were partitioned into 25 smaller sections, and 4 probes Hall kit measurements were conducted on each individual segment. Table 6.2 and 6.3 present the sheet resistance of sample SC16 and SC22 following the spillover process. The colour shading of each small section represents the magnitude of the sheet resistance in that area, with darker colours indicating higher sheet resistance.

It is evident that, generally, the colour depth of SC16 is lighter than that of SC22, indicative of lower sheet resistance in SC16. Additionally, the more uniform colour shading on SC16 suggests that its sheet resistance distribution is more homogeneous, although SC22 exhibits a few sections with sheet resistance around $11\ k\Omega/\square$.

Furthermore, regarding the surface resistance of the two samples, we did not observe significant changes in sheet resistance gradients with increasing distance between the sampling sections and the metal catalyst. In the table, Row A is adjacent to the metal strip, while Row E represents the furthest section from the strip. To some extent, this suggests that the spillover occurring on the diamond surface is unaffected by the distance between the metal and the sampling point, at least for the sample dimensions inspected. Karim et al. reported that hydrogen spillover is influenced by the substrate material; if the surface is reducible, the spillover effects effectively reduce the oxide without being affected by the distance [86]. In the context of this study, we hypothesize that the 900 °C degassing process desorbs the oxygen termination on the diamond surface, leaving free dangling carbon bonds, thereby rendering the surface reducible. Consequently, the sheet resistance shows no significant relationship to the distance from the catalyst metal strip.

The blank control sample, SC10, without catalyst metal on the surface shows no measurable surface conductivity after the same Spillover process as the other samples with catalyst metal. It is assumed that the splitting of hydrogen molecular by catalyst metal, *Pt* and *Pd*, contributing to the hydrogen termination of the diamond surface. Which means, in this work, with low concentration of hydrogen gas as the hydrogen sources, catalyst metal plays crucial roles in terms of hydrogen termination.

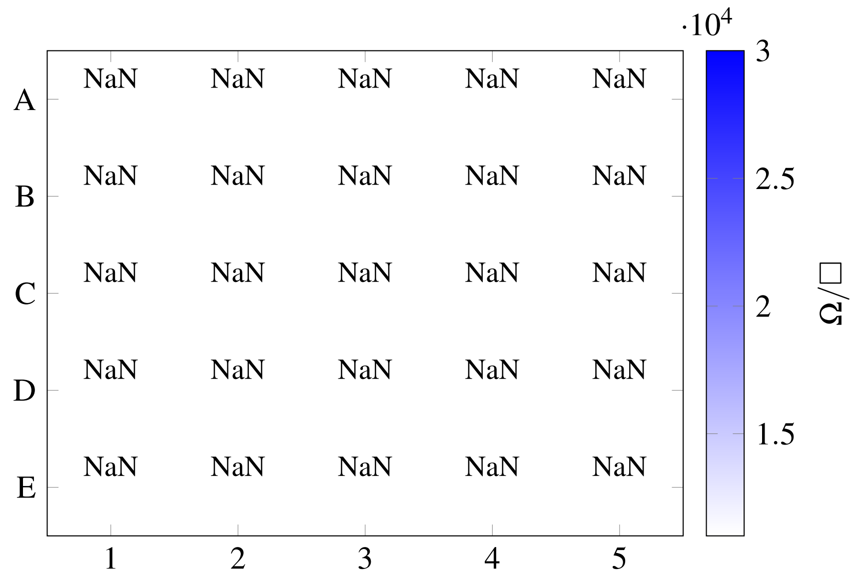


Table 6.4: Sheet resistance of SC10 after spillover (Blank control group).

AFM and Contact angle Measurement

Atomic force microscopy (AFM) was employed to characterize the surface roughness before and after the spillover process. The surface roughness of sample SC16 is slightly lower, and the roughness of sample SC22 slightly increased. Blank control sample SC10 shows a very consistent surface roughness before and after the hydrogen termination. Considering the reported surface roughness changes from 0.3nm to 1.6nm before and after the hydrogen termination with hydrogen plasma treatment[71] and potential measurement errors caused by different measurement spots on the sample surface, those roughness changes in this work is very low.

Measurement	Before (nm)	After (nm)
R1	1.98	1.51
R2	2.08	1.55
R3	1.55	1.39

Table 6.5: Surface roughness of SC16 (Pd) before and after spillover.

Measurement	Before (nm)	After (nm)
R1	1.69	1.61
R2	0.74	N/A
R3	1.17	1.47

Table 6.6: Surface roughness of SC22 (Pt) before and after spillover.

The surface contact angle of sample SC16 increased from 35.5° to 65°, while that of sample SC22 increased from 42.5° to 90° after the spillover process. This indicates that both samples

Measurement	Before (nm)	After (nm)
R1	1.08	1.01
R2	1.22	1.25
R3	1.14	0.9

Table 6.7: Surface roughness of SC10 (control) before and after spillover.

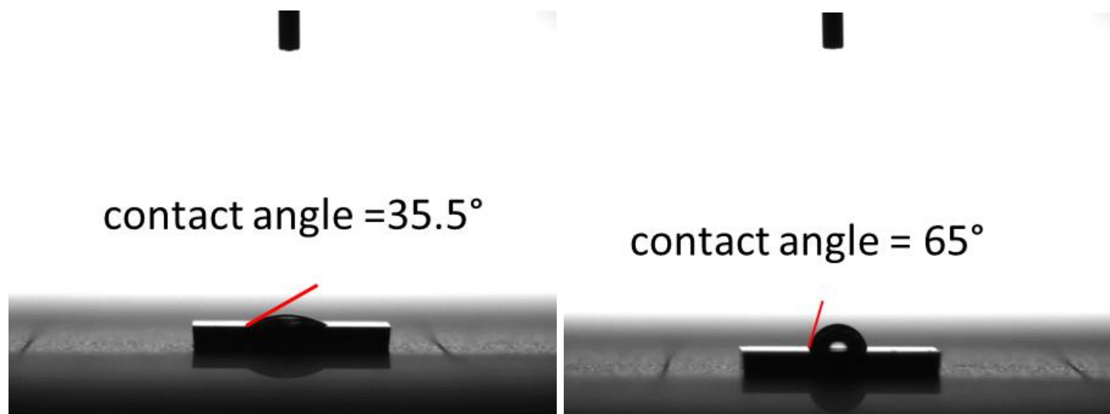


Figure 6.3: Contact angle measurement of SC16 before (left) and after (after) the spillover.

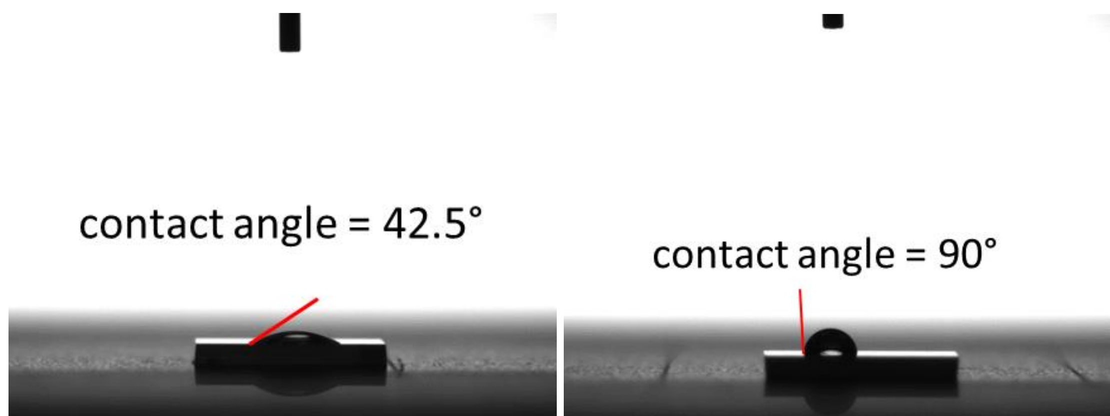


Figure 6.4: Contact angle measurement of SC22 before (left) and after (after) the spillover.

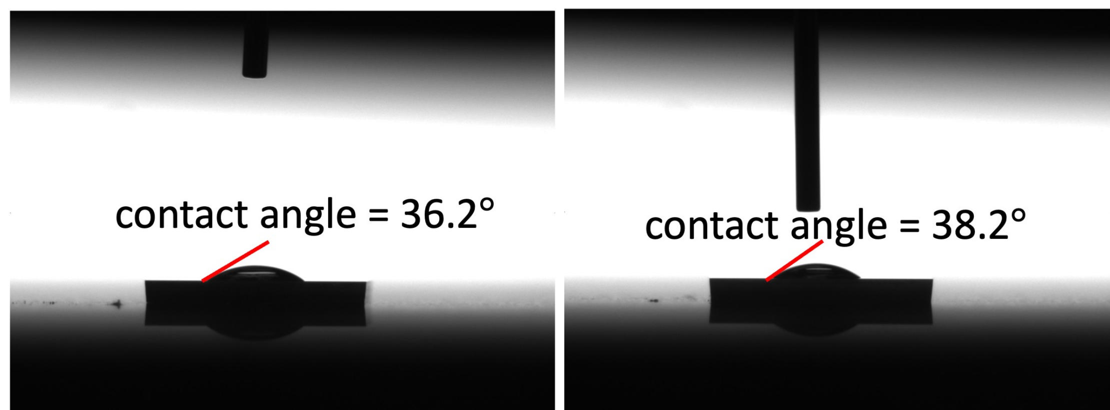


Figure 6.5: Contact angle measurement of SC10 before (left) and after (after) the spillover.

became more hydrophobic after the spillover. This observation aligns with literature findings suggesting that the wettability of an oxygen-terminated diamond surface is higher than that of a hydrogen-terminated diamond surface [136]. The contact angle measurement of blank control sample shows the contact angle keeps the same before(36.2°) and after(38.2°) the Spillover process.

Overall, these results indicate that SC16 and SC22 underwent hydrogen termination after the spillover process, although parameters may need further optimization to achieve a more uniform surface termination. Comparing with the results of the blank control sample S10 whose surface is insulating before and after the Spillover, the catalyst metal strip is playing crucial roles by splitting the hydrogen molecular into atoms in this work thus contribute to the Spillover.

6.3 Chapter Summary

This chapter presents the experiments conducted for surface hydrogen termination using the Spillover-based process. Seven sets of experiments were designed in the initialization phase to explore various parameters, including degassing temperature, duration, and spillover duration. The results highlight the necessity of a 900 °C two-hour degassing process to desorb oxygen termination on the diamond surface, thereby exposing free dangling carbon bonds. Subsequently, these bonds can connect with hydrogen atoms split by the catalyst metal, platinum or palladium, leading to hydrogen termination of the diamond surface.

The optimal parameters identified in the initialization phase were then applied to two samples, employing Pd and Pt as catalyst metals, respectively. Both samples exhibited surface conductivity after the spillover, with increased hydrophobicity indicating a change in surface termination. AFM results for sample SC16 and SC12 revealed minimal change in surface roughness post-termination. Blank control sample SC10 was carried out to verify the existence of the catalyst metal contribute to the surface termination by splitting the hydrogen into atoms.

In summary, a method for hydrogen termination of diamond surfaces using the thermal spillover process has been explored. The lowest achieved sheet resistance was 13.2 $k\Omega/\square$ with Pd as catalyst metal. These results are consistent with literature recorded values for plasma hydrogen terminated diamond. Additionally, the surface of SC16 exhibited minimal roughening after the spillover process, highlighting an advantage of using this method for diamond surface termination over plasma methods. This work appears to be the first study of the thermal hydrogen termination on diamond wafer with low concentration of hydrogen and temperature below 900 °C.

Chapter 7

Alternative Fabrication Results

In chapter 2, we established that the hydrogen-terminated diamond surface is highly susceptible to damage during fabrication and processing. Even low-power plasmas, such as oxygen ashing, can disrupt or replace this termination. This poses a significant challenge in the fabrication of devices on diamond surfaces, as oxygen plasma is commonly employed for the removal of resist residue post resist development. Furthermore, ambient environmental factors, including elevated temperatures, can variably desorb air adsorbates on the hydrogen-terminated diamond surface, which are required to instigate transfer doping in air-exposed H-diamond.

To safeguard the surface termination against damage during the fabrication process, gold is frequently utilised as a sacrificial layer. This chapter explores a few alternative fabrication methods to replace the gold sacrificial layer approach. Lift-off resist was investigated as protective layers in lieu of gold.

Another strategy to preserve the surface termination involves the avoidance of oxygen plasma usage. Consequently, hydrogen plasma is explored as an alternative method for resist residue removal.

Furthermore, the latter section of this chapter delves into the utilisation of Pd as a replacement for Au in contact metal applications to establish ohmic contact. As previously discussed, Pd has been documented to form ohmic contacts as Au. This segment of the experiment employs the Transmission Line Model (TLM) method to investigate the viability of substituting gold with palladium for the formation of ohmic contacts.

7.1 Lift-off Resist as protective layer

Gold serves as a sacrificial layer in the fabrication of devices on hydrogen-terminated diamond surfaces, playing three pivotal roles. Firstly, it shields the hydrogen termination throughout the fabrication procedure. Secondly, the sacrificial layer serves as an ohmic contact metal once the gate level is established. Following gate level development, gold undergoes over etching via wet etch to create the channel and expose the area for subsequent gate deposition. The last acts as a charge conduction layer if the process involves e-beam lithography. This method offers the advantage of safeguarding the surface from environmental damage. However, it presents drawbacks. Wet etching for gate window opening and ohmic contact formation result in a self-aligned gate level, positioning the gate centrally within the source-drain channel. Additionally, wet etching yields less controlled edge wall profiles for ohmic contact, potentially increasing contact area and reducing channel length accuracy.

Lift-off resist (LOR) is a UV and electron beam-insensitive resist type, susceptible to TMAH etching. Control over wet etch profile is achieved through spinning rate, baking time, and developer concentration adjustments [137]. LOR exhibits good adhesion to various materials and compatibility with both photo and e-beam resists, rendering it ideal for bi-layer lift-off processes. Controlled wet etch profiles enable undercutting in the range of 1 to 2 μm. Moreover, minimal residue post-wet etch may obviate the need for ashing or descum processes [138]. Thus, exposure of the hydrogen surface termination to oxygen plasma can be circumvented. Utilising LOR as a lift-off layer facilitates an additive process for ohmic metal, enabling the formation of ohmic contacts with precisely controlled sidewalls. Additionally, as discussed in the fabrication chapter, the gold sacrificial layer forms the final ohmic pad by wet etching in the middle of the gold before the deposition of gate metal, ensuring that the gate always sits in the middle of the source and drain. With the use of the LOR process, ohmic pads and gates are defined through two separate steps, enabling the adjustment of the gate position. This flexibility allows for precise control over the gate alignment relative to the source and drain, which is beneficial for optimizing device performance and characteristics.

TLM and VDP structure

Figure 7.1 depicts the simplified fabrication steps for TLM and VDP structures on hydrogen-terminated diamond utilising LOR and e-beam resist as a bi-layer lift-off method. Two single polished hydrogen terminated samples A and B with similar sheet resistance were used for the fabrication. Initial cleaning of hydrogen-terminated single polished diamond samples was conducted using acetone and IPA to eliminate any potential surface contamination. Subsequently, Hall Kit measurements were performed to assess sheet resistance.

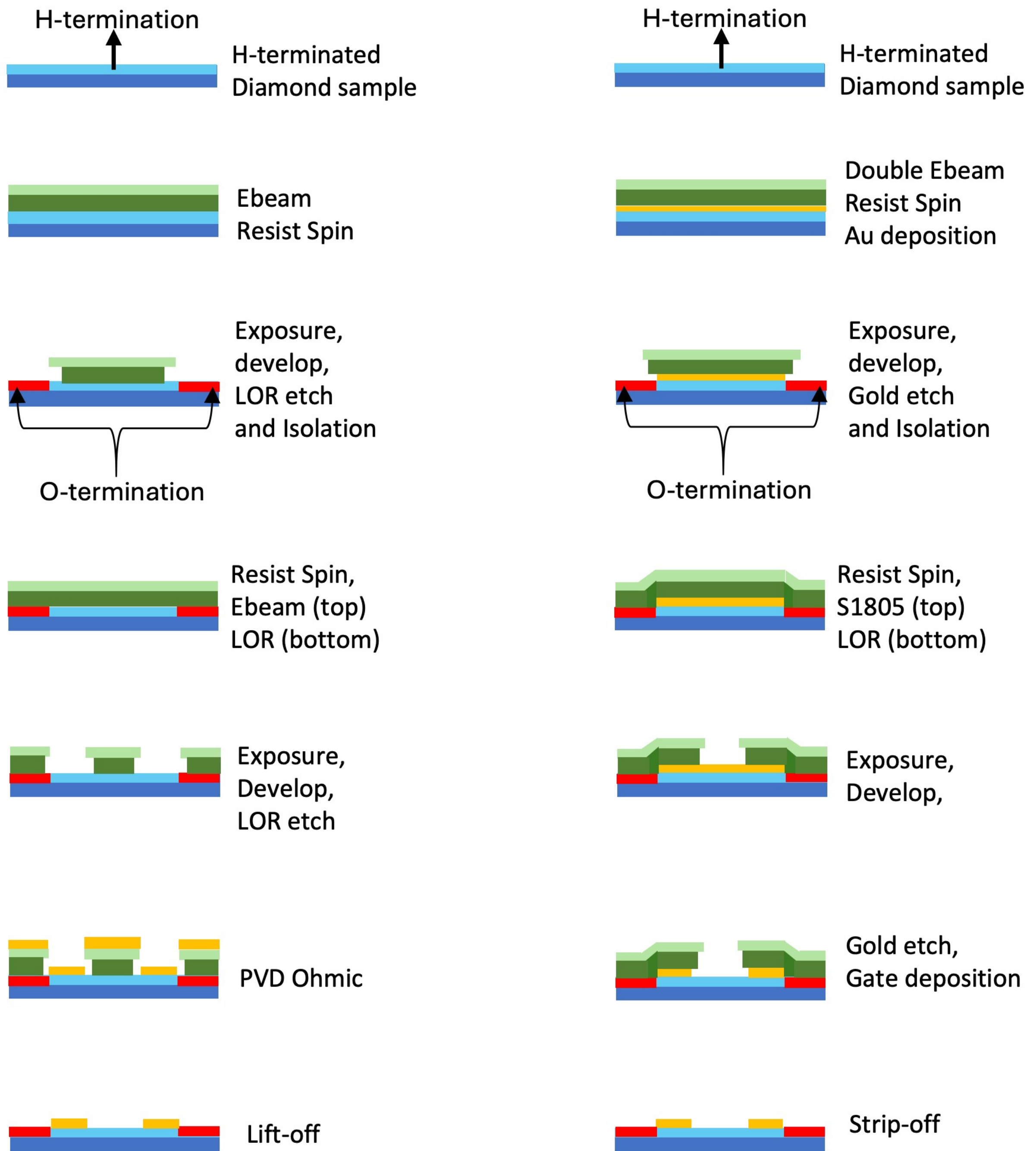


Figure 7.1: Fabrication steps of LOR method (Left) and gold sacrificial layer method(Right). The ohmic pad in LOR method is formed by lift-off method. The ohmic pad in gold sacrificial layer method is formed by the wet etch of the gold deposited in the first step. Former method results in a metal contacts with better profiles, and the later on gate fabrication is not limited to the ohmic metal steps. The gold sacrificial form the ohmic pad by over-etching the gold sacrificial layer which leads to a rough profile. In addition, the opened windows for wet etch is also used for gate deposition, which leads to a self-aligned gate level.

A layer of LOR 3A was spun (6000 rpm/s for 45 seconds) and baked (180 °C for 5 minutes) onto the surface as the first resist layer, followed by the spun (5000 rpm/s for 60 seconds) and bake (180 °C for 2 minutes) of e-beam resist atop the LOR. Following e-beam lithography, the e-beam resist undergoes development with 1:2 IPA:MIBK developer at 23 °C for 30 seconds. The sample was then subjected to oxygen plasma ashing for 1 minute at 80 W power to eliminate PMMA resist residue. A 40-second rinse in CD-26 (2.5% TMAH) was employed to etch (develop) the LOR resist beneath the developed e-beam resist. For isolation purposes, the sample was exposed to oxygen plasma once more to remove the exposed hydrogen termination.

For the ohmic metal and bond pad metal steps, Plassys 2 was utilised to deposit Au (ohmic metal 80nm) or Ti(10 nm)/Au(80 nm) (bond pad metal stack). Subsequently, an overnight rinse in SVC-14 in a 50 °C water bath was employed to strip off the resist and lift-off any unwanted metal.

The entire fabrication process encompasses the marker level, isolation, ohmic pad, and bond pad metal deposition stages. Following fabrication, the TLM VDP structure was measured using a probe station and Hall kit.

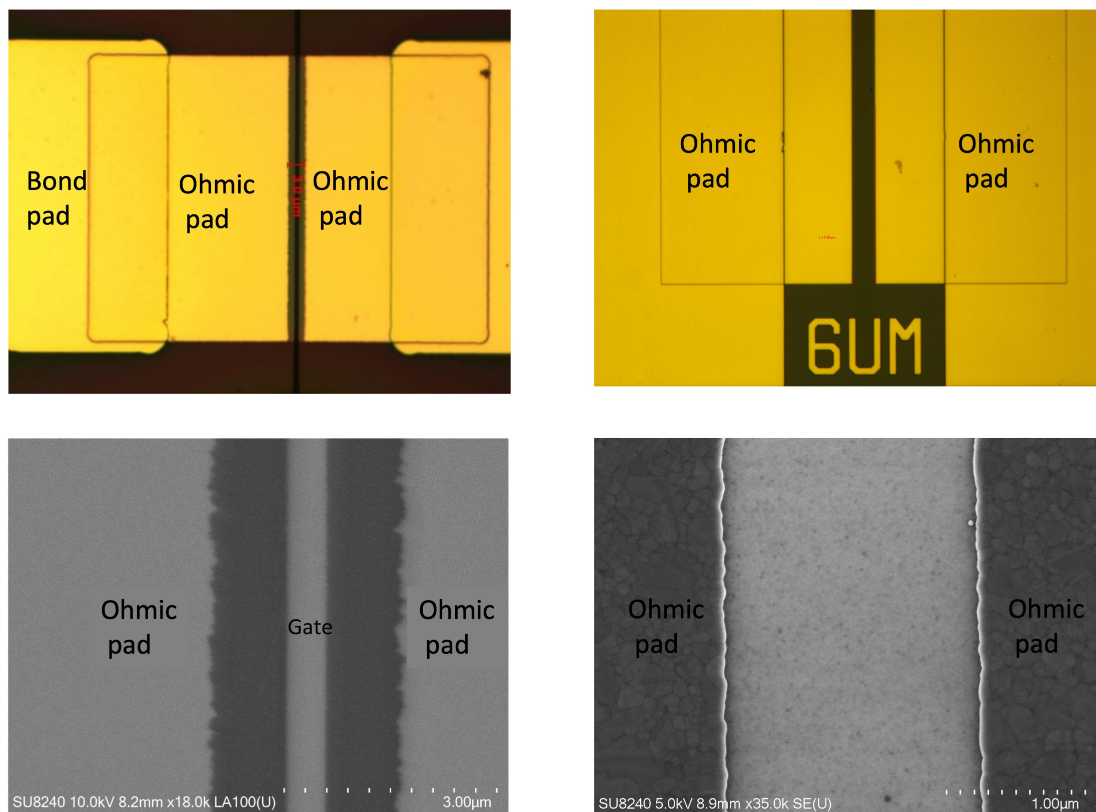


Figure 7.2: Structures of gold sacrificial layer methods (left)[20] and LOR lift off method (right). The optical images and SEM images are utilized to compare the difference in metal edge roughness between the gold sacrificial layer method and the LOR method. The metal formed by the LOR method exhibits smoother edges, even under higher magnification.

Figure 7.2 displays the optical and SEM images of ohmic pads formed using the gold wet etch and lift-off processes, respectively. It is evident that the edges of the lift-off ohmic pads are smoother than those of the gold wet-etched ones. This difference is particularly pronounced in the SEM image, where the magnification of the lift-off sample, at 35 k, is nearly double that of the wet-etched sample. Despite the higher magnification, the edge of the lift-off sample remains smoother. In terms of the roughness of the ohmic pad edge, the lift-off method evidently yields superior results.

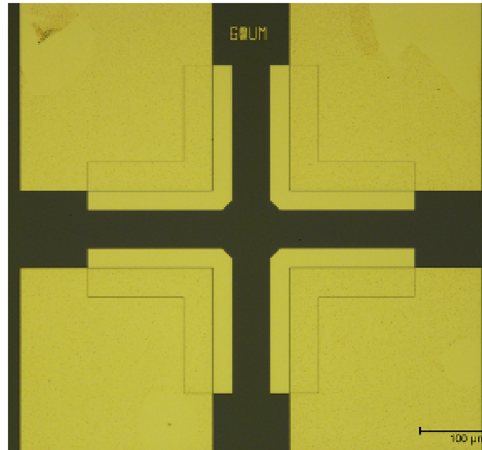


Figure 7.3: Optical image of VDP structure for Hall measuremnt.

Hall Kit measurements are conducted both before and after fabrication. Prior to device fabrication, four probes make direct contact with the sample surfaces. Sample A exhibits a sheet resistance of 1.8×10^4 $\Omega/\square$. Conversely, the sheet resistance of sample B measure is 1.7×10^4 $\Omega/\square$

Sample	**Status**	$R_s(\Omega/\square)$	**Status**	$R_s(\Omega/\square)$
Sample A	Before	1.8×10^4	After	2.4×10^4
Sample B	Before	1.7×10^4	After	6.8×10^4

Table 7.1: VDP measurement of Sample A and B before and after the fabrication.

Following fabrication, VDP structures were measured using the Hall Kit. The sheet resistance of samples A and B increases to 2.4×10^4 $\Omega/\square$ and 6.8×10^4 $\Omega/\square$, respectively. This increase in sheet resistance suggests damage to the hydrogen termination or the presence of resist residue. Particularly noteworthy is the nearly threefold increase in sheet resistance for sample B.

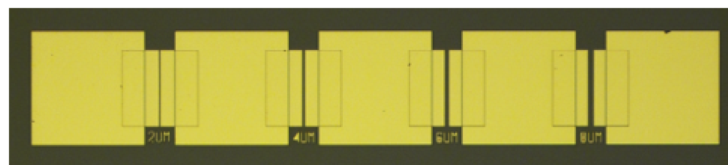


Figure 7.4: Optical image of TLM structure.

The TLM structure is assessed post-fabrication to derive the contact resistance and sheet resistance. Figure 7.5 presents a set of TLM structure measurement results. It is evident that the structure does not exhibit ohmic contact behaviour across the inspected voltage range, where the I-V curve should ideally be a straight line, with the slope of the plot reflecting the resistance of the contact.

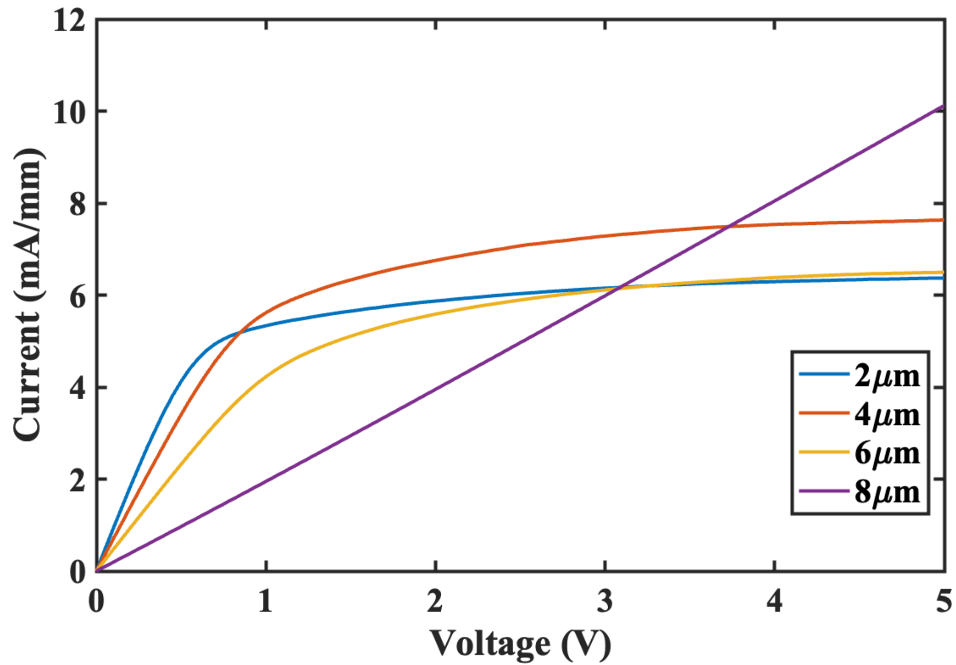


Figure 7.5: TLM result of sample A fabricated with LOR (Applied voltage 0 - 5 V).

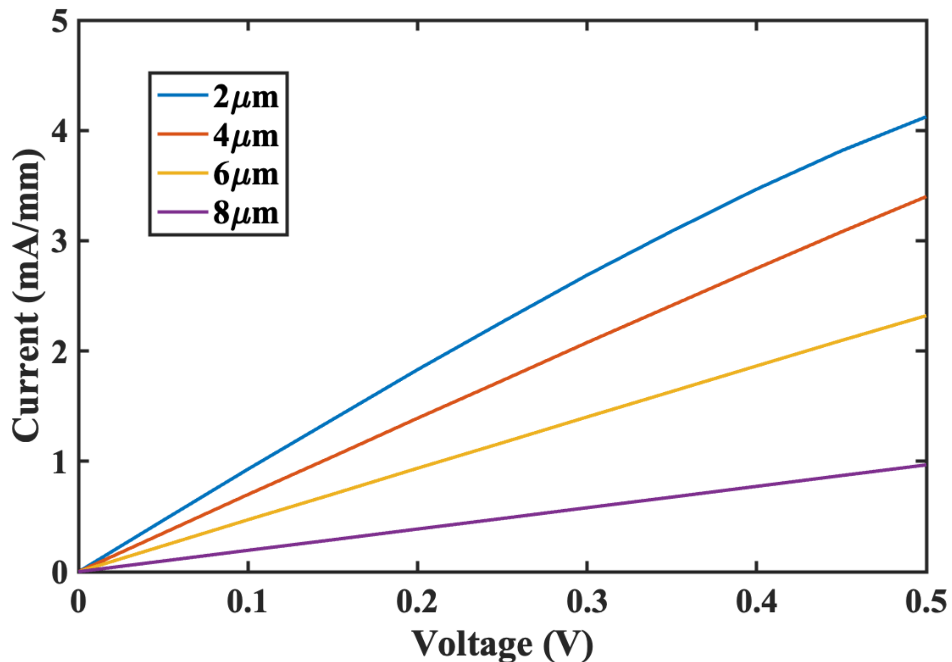


Figure 7.6: TLM result of sample A fabricated with LOR below 0.5V.

The observed non-linear behaviour in this sample suggests the potential presence of resist residue on the sample surface. Although the curve is not linear within the 0 to 5 volts range, a small linear region exists below 0.5 volts. To derive the contact resistance and sheet resistance from the TLM results, only data below 0.5 volts are utilised for the calculation. Figure 7.6 depicts the data plot below 0.5 volts.

The resistance between each gap is computed, and the value for each gap is utilised to plot a graph, with gap size as the x-axis and resistance as the y-axis. Equation 5.4 elucidates that the intercept represents two times the contact resistance, while the slope corresponds to the sheet resistance over the width of the contact pad. Figure 7.7 illustrates the final plot of TLM structure measurements. The sheet resistance measures $3.9396 \times 10^4\ \Omega/\square$, and after normalisation, the contact resistance is $17.1\ \Omega \cdot mm$. Notably, the contact resistance is larger than typically reported for Au on hydrogen terminated diamond which is $0.9 - 5\ \Omega \cdot mm$ [46], [93], [95]. The sheet resistance from the TLM is higher than that measured from the VDP structure. It is assumed that the influence of resist residue on the sheet resistance might vary across the sample surface.

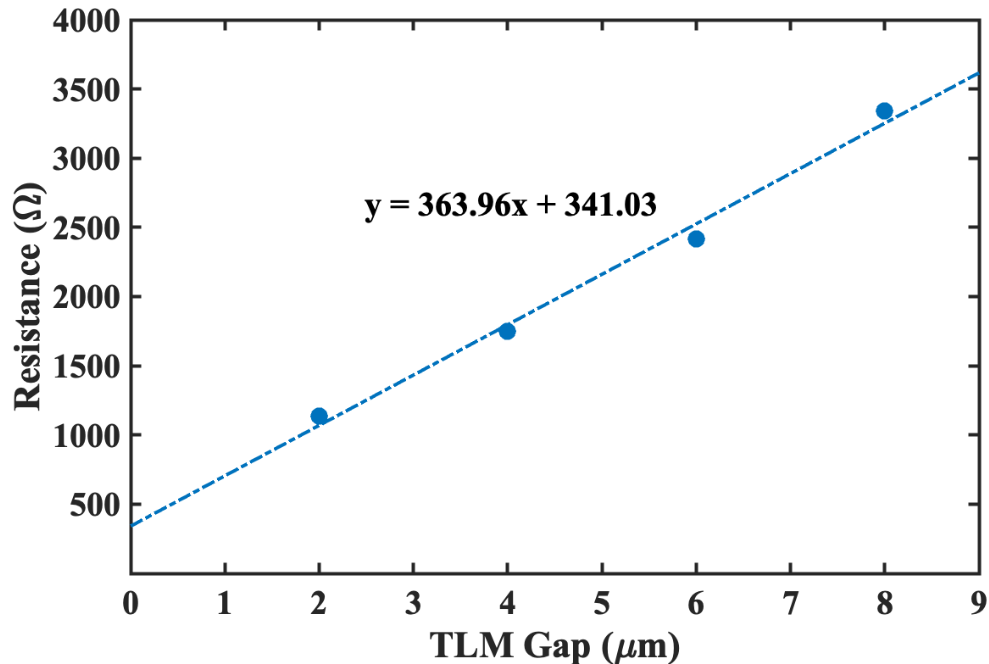


Figure 7.7: TLM results analyse of Sample A when data extracted below 0.5 V.

Figure 7.8 depicts the measurement of one set of TLM structures on sample B. The observed I-V curve exhibits non-linear behaviour in the measured range, and the current saturates between 1 to 2V, which is similar behaviour to sample A. It is assumed that the non-linear behaviour and saturation current in a designated ohmic contact are caused by the potential resist residue, which leads to poor metal-semiconductor contact between the ohmic pad and the H-diamond surface.The increased sheet resistance measured before and after fabrication with the Hall kit and the sheet resistance ($3.9396 \times 10^4\ \Omega/\square$) extracted from sample A contribute to the hypothesis

that the existence of the resist residue across the sample surface. The patchy resist residue under the Ohmic pad leads to poor Ohmic contact between the gold and the H-diamond surface. This is one of the reasons for the extremely high contact resistance extracted from the TLM measurement. The saturation of the current when the bias exceeds 1 V might be caused by the limited number of carriers or the low mobility of carriers in the TLM gap. This could result from the resist residue interfering with the H-diamond surface air adsorbates. Equation 7.1 demonstrate the current calculation with the carrier concentration,

$$I = q \cdot p \cdot \mu \cdot E \cdot A \tag{7.1}$$

where q is the elementary charge, p is the hole concentration, μ is the hole mobility, E is the electric filed and A is the cross sectional area.

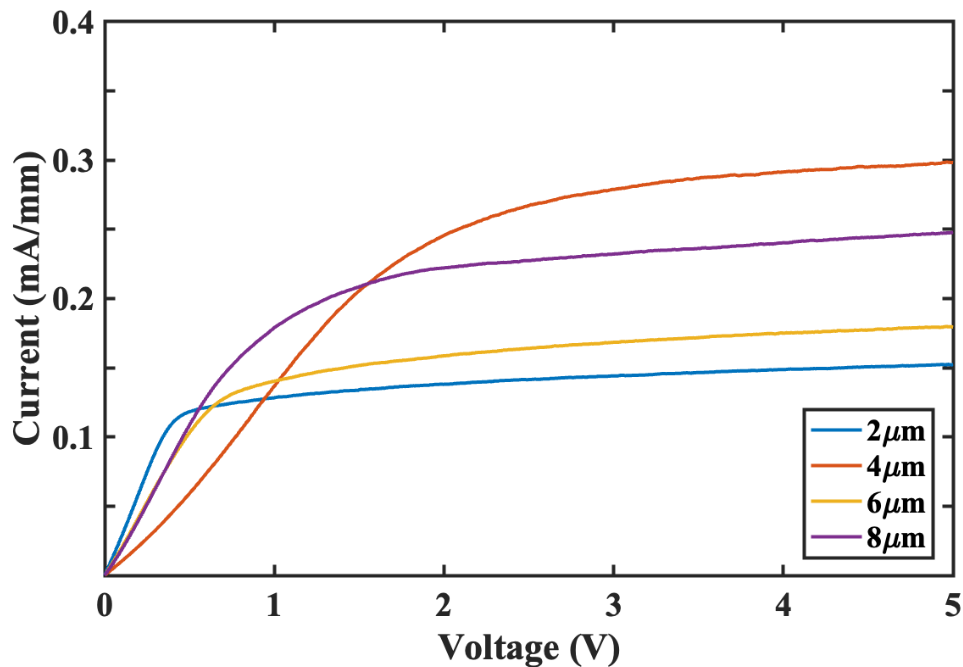


Figure 7.8: TLM result of sample B fabricated with LOR.

The electrical measurements, encompassing TLM and Hall measurements, reveal a notable increase in the sheet resistance of both samples following fabrication. The non-linear I-V curves in the measured range and saturation behaviours is assumed to be caused by the remained resist residue of LOR during the fabrication process. Extracting the contact resistance from sample A yields a value higher than the reported contact resistance between gold and hydrogen-terminated diamond. Taken together, these findings suggest that LOR remained residue on the sample surface, contributing to the observed deviations from expected electrical behaviour.

Resist residue Measurement

The electrical measurements have provided evidence suggesting the presence of resist residue beneath the ohmic contact. To validate this assertion, additional tests were conducted in this study. The initial test involved spinning LOR resist onto the sample surface and subsequently baking it. Following this, CD26 was employed to etch the resist for the same duration as used in the fabrication process. This procedure was repeated four times on the same sample, and after each iteration, the surface roughness was measured using AFM.

Figure 7.9 illustrates that after the initial spin and wet etch, the surface roughness increased by more than 0.5 nm for both samples. Subsequently, following the first spin, the roughness of both samples exhibited minimal change. This phenomenon may be attributed to the initial spin leaving a thin layer of resist on the surface, thereby resulting in the AFM scan measuring the roughness of the LOR resist rather than the sample surface itself. After this spin, the roughness stabilised at a certain level, as the potentially accumulated thin layer of LOR resist after each spin formed a surface similar to the initial layer of residue.

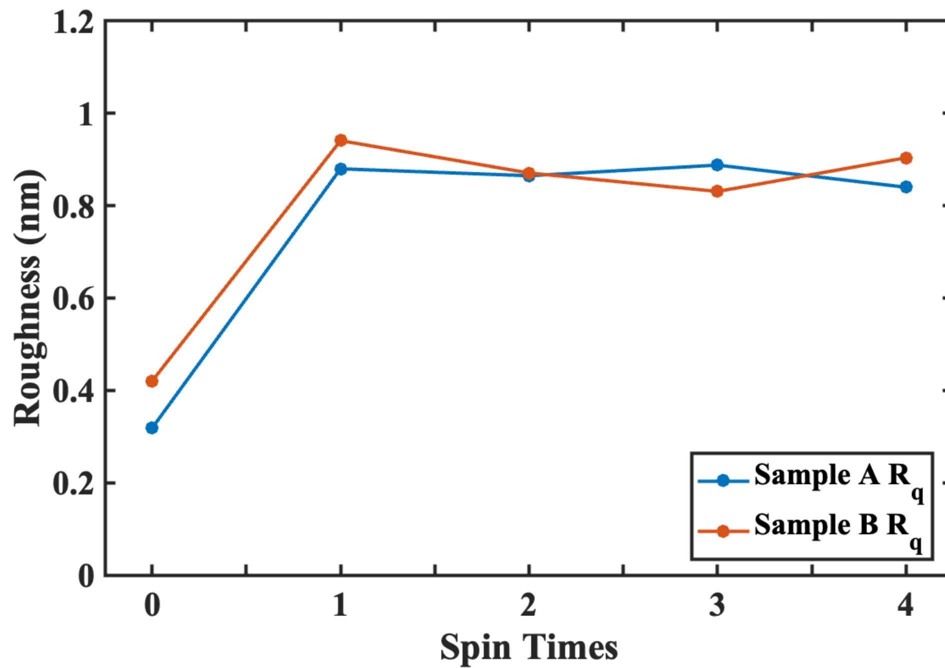


Figure 7.9: Sample surface roughness after four times of LOR spin and etch.

In accordance with the report by Macintyre et al. [118], another set of experiments was conducted in this study. This experiment involved spinning LOR 3A and PMMA resist onto the cleaned diamond surface, followed by a three-step fabrication process. Initially, a marker level was applied for subsequent alignment purposes. Subsequently, a 20 nm Ti layer and an 80 nm Au layer were deposited onto the sample surface. After lift-off of the marker metal, the sample was spun with the same resist stack. In this step, an array with horizontal lines was patterned

onto the resist. To create a surface devoid of resist residue, a 2-minute ashing process was performed after resist development. Instead of stripping off the resist, a second array of vertical lines was patterned onto the same resist stack in the third step. Ashing was omitted in this step to ensure that the resist residue remained on the surface. To mitigate errors caused by etching the diamond with oxygen plasma affecting the experimental results, a silicon wafer was utilized in this experiment.

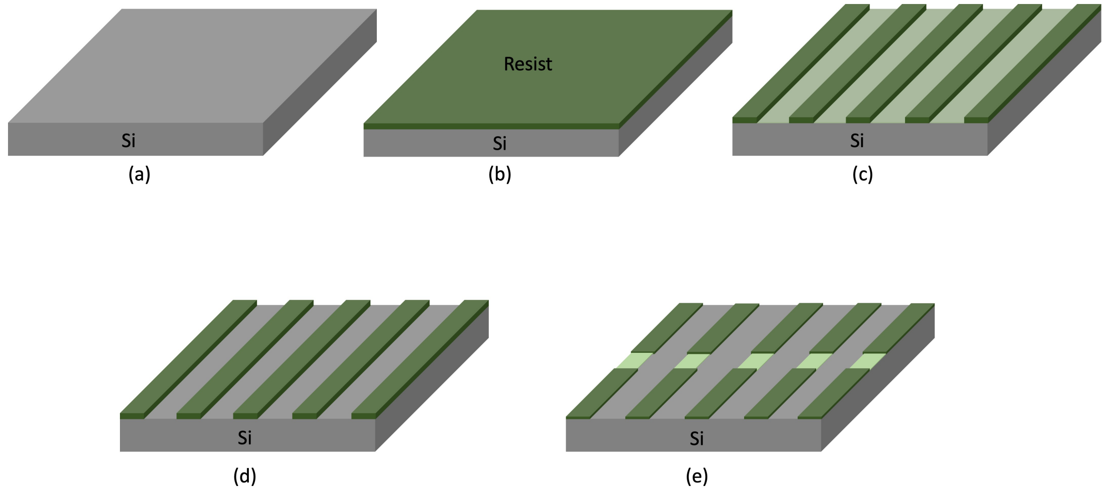


Figure 7.10: Simplified fabrication flow of resist residue test.
(a) Cleaned silicon sample. (b) LOR 3A and PMMA spin and baking. (c) First level of grate writing and develop, potential resist residue in light green. (d) Oxygen plasma engaged to remove the potential residue. (e) After oxygen plasma the second level of grate was completed on the rest of resist left on the sample surface and developed. "Step" between clean surface and resist residue created.

Figure 7.11 presents optical images depicting the sample surface after each step of the experiment. The initial image displays the sample surface subsequent to PMMA development and LOR wet etching, with a horizontal line array patterned onto the surface. The subsequent ashing step is aimed at removing the resist residue from the initially exposed area. The middle image illustrates the surface following the second exposure, with the PMMA on the top subsequently developed. The third image showcases the sample surface post-LOR wet etching by CD26. The

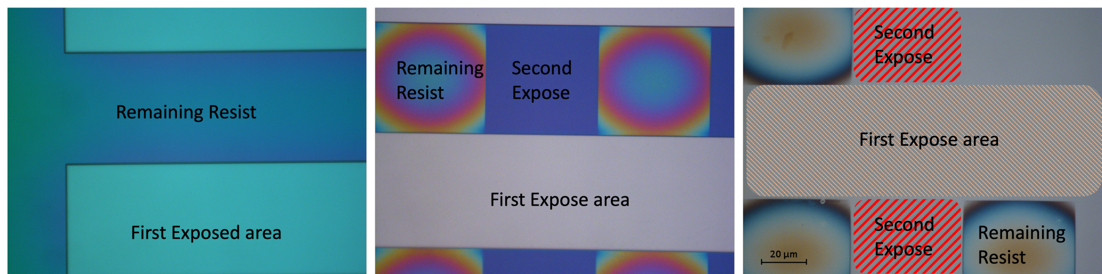


Figure 7.11: Optical image of LOR residue test structure fabrication. The first step of horizontal array written (left), exposure of vertical array (mid), vertical array LOR wet etch (right).

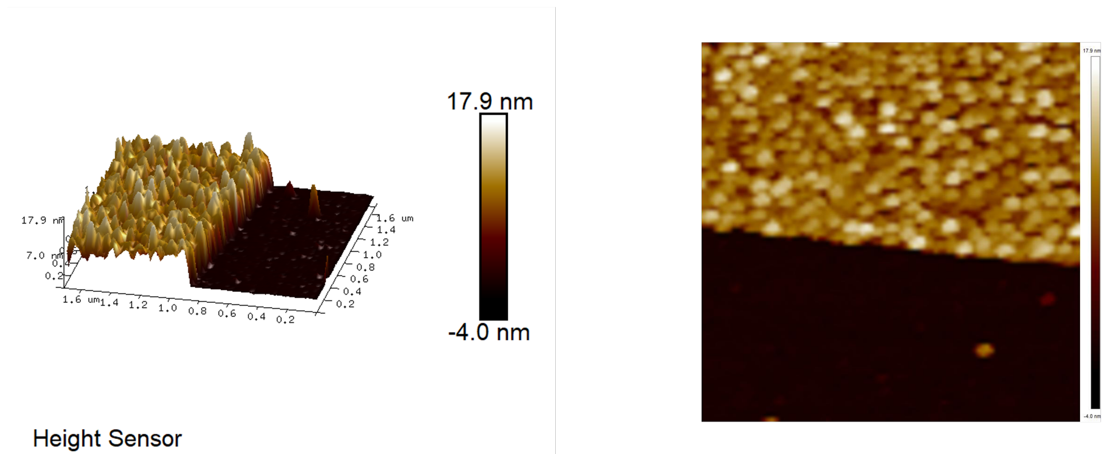


Figure 7.12: 2D and 3D rendering AFM image of area between the first expose and second expose.

red areas denote regions without oxygen ashing. Notably, a junction area is visible, where part of the surface is cleaned (ashed) while the other part retains the condition after LOR wet etching. Subsequently, AFM was employed to measure the junction area.

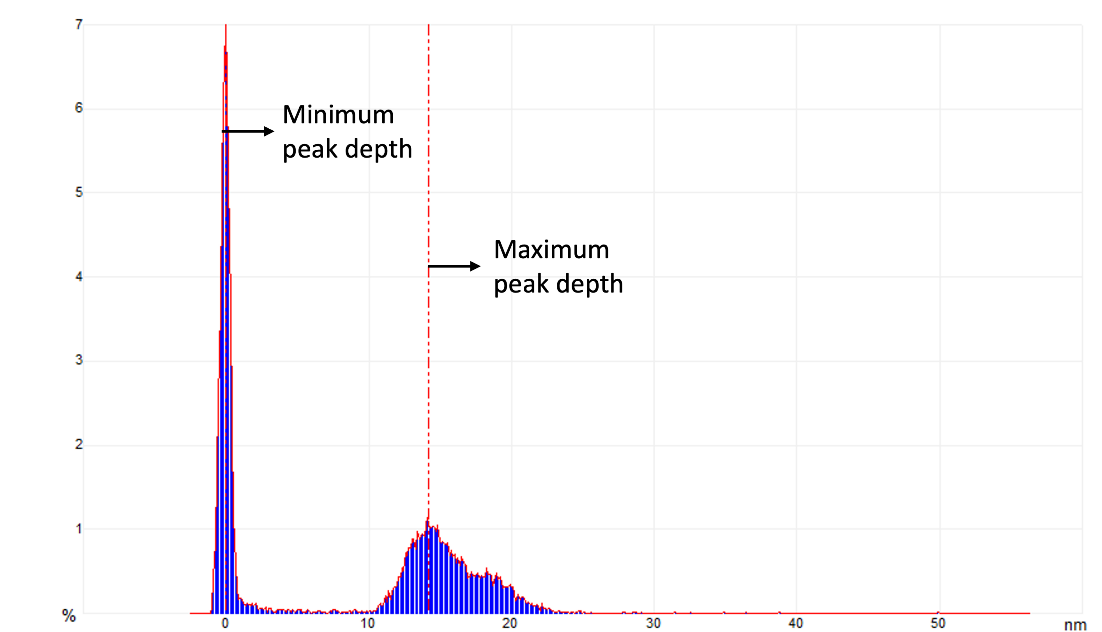


Figure 7.13: Histogram graph of AFM scan.
The left peak shows the minimum peak depth and the right peak shows the maximum peak depth. The distance between two peaks represents the depth of the measured step.

Figure 7.12 presents the AFM image depicting the scanning results over the junction area between the first exposed area and the second exposed area. The scanning results reveal a step between the two exposed areas. The smallest measured depth size in this study is 7 nm, while the largest step measures 14 nm. This observation is consistent with the hypothesis that wet-etched LOR leaves resist residue on the sample surface, and that this residue can be removed

by oxygen plasma ashing. Figure 7.13 displays the histogram graph of the depth measurements. The minimum peak depth is 0 nm, while the maximum peak depth is 14.2 nm.

All the results collectively indicate that LOR is not suitable as a protective layer for fabrication on hydrogen-terminated diamond due to the presence of resist residue. Removal of this residue necessitates the use of oxygen plasma, which in turn damages the surface termination.

7.2 Hydrogen Plasma resist residue removal

Instead of relying on a protective layer to preserve the surface hydrogen termination from damage caused by oxygen plasma, hydrogen plasma was investigated as an alternative for removing resist residue. Given that the hydrogen termination of diamond surfaces can be achieved through hydrogen plasma treatment, using hydrogen plasma to remove resist residue may prevent damage to the hydrogen surface termination. The initial phase involved establishing a hydrogen plasma etch recipe capable of removing resist while maintaining a well-controlled etching rate.

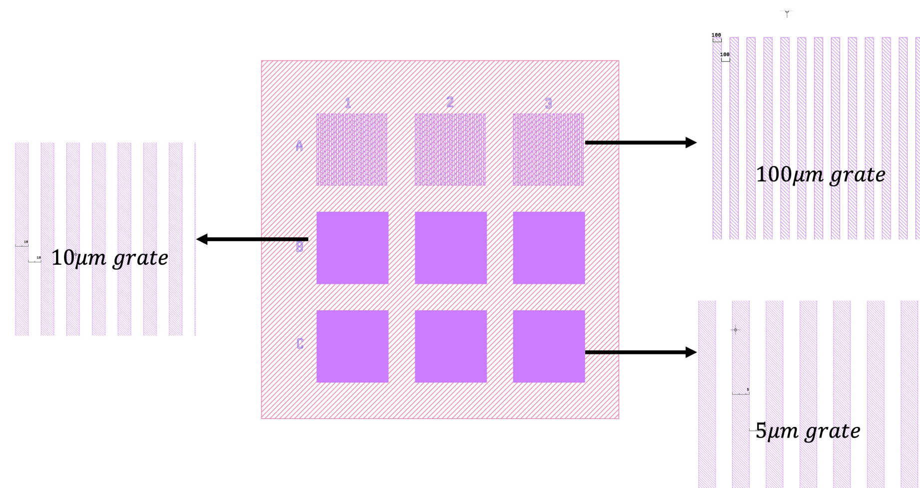


Figure 7.14: CAD image of e-beam lithography job design for hydrogen plasma etching test.

The experiment entails an e-beam lithography fabrication step to create a series of arrays with different line widths on a cleaned silicon substrate. The silicon sample is first cleaned and then coated with a bi-layer of PMMA resist to establish the same resist condition as that on the diamond sample. Subsequently, the sample was developed in 2:1 MIBK:IPA developer for 30 seconds at 23 °C to develop the exposed resist. Following development, oxygen ashing is conducted to remove any resist residue and ensure a clean profile for subsequent measurement steps.

Figure 7.14 illustrates the pattern for the e-beam lithography job. Three rows and three columns of arrays are written on the sample surface. The patterns in each row share the same architec-

ture, with the line widths of each row being 100 μm, 10 μm, and 5 μm from top to bottom, respectively.

To measure the etch rate of hydrogen plasma, a DEKTEK XT surface profiler is employed to scan across the surface before and after each dry etch step to compare the thickness difference. The ICP180 is utilised as the dry etch tool.

DEKTEK XT Measurement Results

To establish appropriate parameters for resist etching, an initial etching process was conducted with a coil power of 900 W and platen power of 8 W. The hydrogen flow, chamber pressure, and stage temperature were set at 50 sccm, 25 mTorr, and 20 °C, respectively. The duration of the dry etch was set to 2 minutes. Prior to the dry etch, the thickness of pattern A (with 100 μm array) was measured at 410 nm, while patterns B and C (with 10 μm and 5 μm arrays, respectively) measured at 350 nm. The difference in thickness between patterns of different sizes can be attributed to the proximity effect. Smaller features, having a higher density, can cause adjacent features to be overdosed with back-scattered electrons more than larger features, resulting in thinner resist after development.

Following the hydrogen dry etch, the thickness of pattern A decreased to 90 nm, yielding an etching rate of approximately 160 nm/min. Patterns B and C exhibited a thickness reduction to 40 nm, resulting in an etching rate of around 165 nm/min. While the etching rates for different patterns did not significantly differ, they were notably too fast for effective resist residue removal. Consequently, two additional sets of experiments were devised to decelerate the etching rate.

In the first modified parameter set, the coil power, which accelerates the ions in the coil, was adjusted. A series of dry etch tests were conducted with coil powers of 450 W, 300 W, 150 W, and 50 W. The thickness of the patterns was measured before and after the dry etch for each experiment. With a coil power of 450 W, the etching rates for patterns A, B, and C were approximately 99.6 nm/min, 99 nm/min, and 99.5 nm/min, respectively. Subsequently, as the coil power decreased to 300 W, the etching rates for all three patterns remained approximately the same at around 65 nm/min. Further reductions in coil power to 150 W and 50 W resulted in etching rates of 25 nm/min and 5.99 nm/min, respectively.

Figures 7.15, 7.16, and 7.17 illustrate the contact profiler measurement results of the grating structures before and after etching by hydrogen plasma. The coil power applied in this experiment was 50 W, with a duration of 10 minutes. The flow rate, platen power, chamber pressure, and stage temperature were set at 50 sccm, 8 W, 25 mTorr, and 20 °C, respectively. The height of the grating patterns for pattern A decreased from 405 nm to 344 nm, resulting in an etch rate

of 5.675 nm/min. For pattern B, the height decreased from 335.5 nm to 275 nm, giving an etch rate of 6.05 nm/min. Finally, the thickness of pattern C dropped from 330 nm to 267.3 nm, with an etch rate of 6.25 nm/min. The average etch rate with 50 W power was approximately 5.99 nm/min.

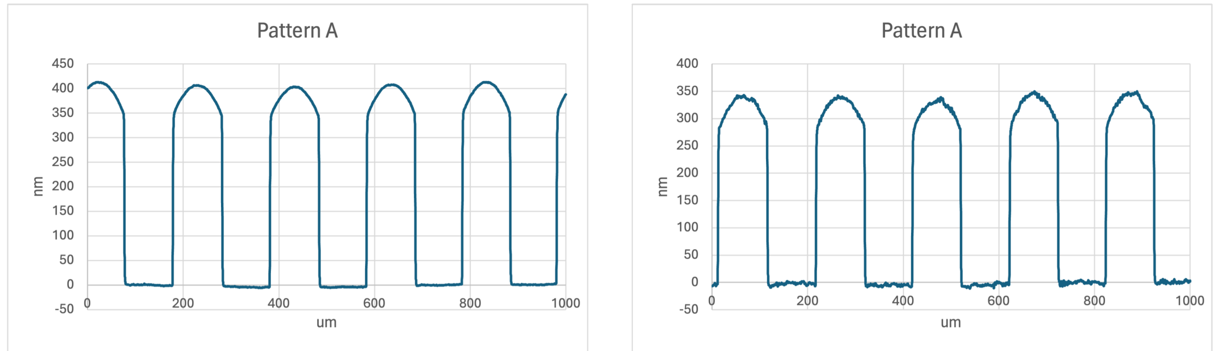


Figure 7.15: Resist thickness of pattern A before (left) and after (Right) dry etch with coil power of 50 W, hydrogen flow of 50 sccm and duration of 10 mins.

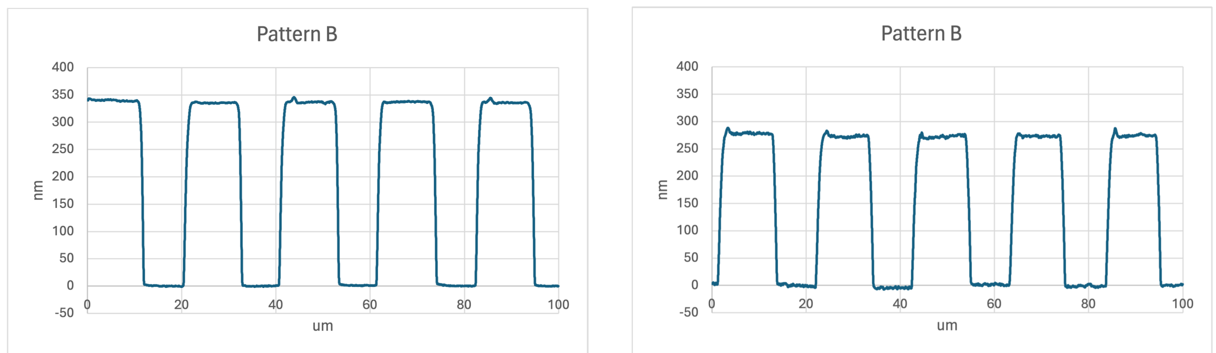


Figure 7.16: Resist thickness of pattern B before (left) and after (Right) dry etch with coil power of 50 W, hydrogen flow of 50 sccm and duration of 10 mins.

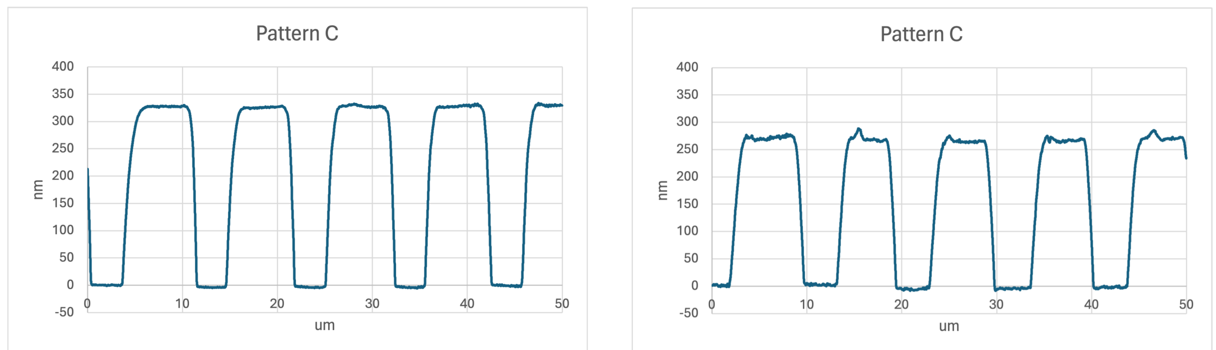


Figure 7.17: Resist thickness of pattern C before (left) and after (Right) dry etch with coil power of 50 W, hydrogen flow of 50 sccm and duration of 10 mins.

Figure 7.18 depicts the changes in etching rate with the decrease in coil power. As previous results shown, the reduction in power leads to a significant decrease in etching rate. Moreover, the etching rate for patterns with different feature sizes remains consistent. In order to further reduce the etching rate, two more sets of experiments were conducted with decreasing flow rates.

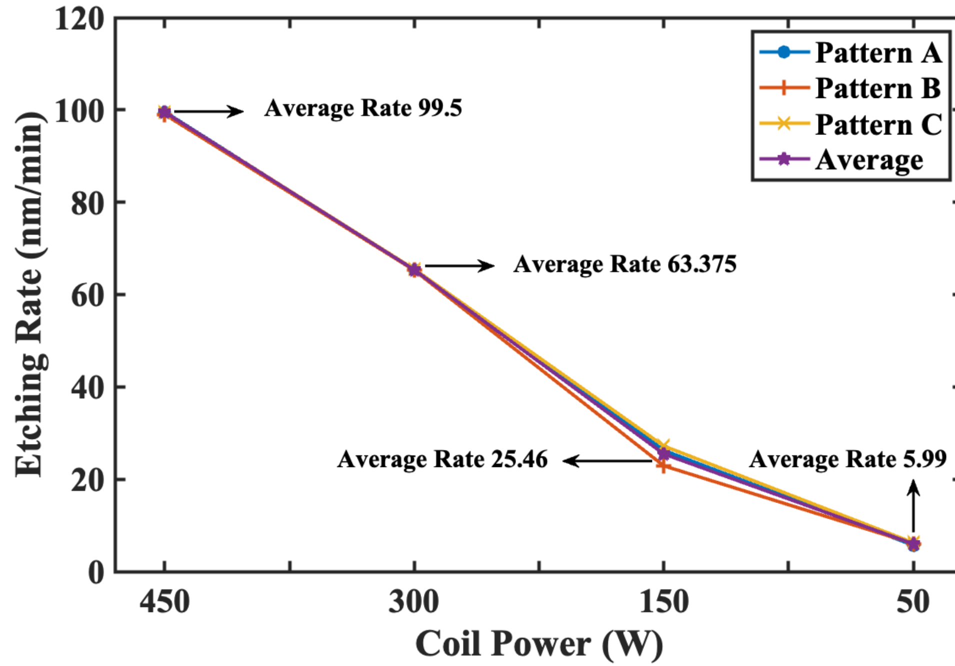


Figure 7.18: Hydrogen plasma etching rate of PMMA resist versus coil power change.

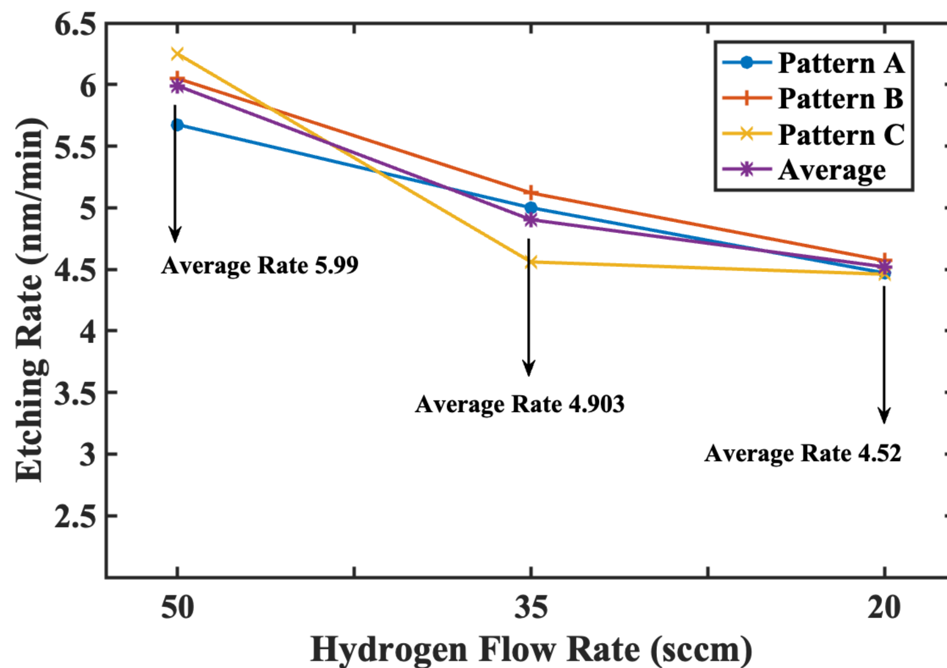


Figure 7.19: Hydrogen plasma etching rate of PMMA resist versus hydrogen flow rate change.

Based on the recipe with 50 W coil power, two more sets of experiemnt with decreasing flow rate were conducted. Figure 7.19 illustrates the changes in etching rate with varying hydrogen flow rates. Similar to the previous test, the etching rate remains consistent for different feature sizes. Furthermore, reductions in the flow rate led to decreases in the etching rate from 5.99 nm/min to 4.5 nm/min. For a standard oxygen plasma ashing process used in this work, ashing rate of PMMA resist is around 5 nm/min to 10 nm/min. Thus a hydrogen plasma etching rate of PMMA between 5.99 nm/min and 4.5 nm/min is ideal for the resist residue removal.

Two 3×3 mm hydrogen-terminated diamond samples were utilised to test the etching parameters and to verify whether this process preserves the hydrogen termination on the diamond surface. VDP measurements were used to assess the surface conductivity before and after the dry etch. Four probes made direct contact with the sample surface. The sheet resistance of both samples was on the order of 3×10^4 $\Omega/\square$. The oxygen plasma ashing process employed in this work aimed to remove resist residue with a thickness of around 10 nm. Thus a recipe with etching rate around 4.5 nm/mm was applied for the trial. The etching trial was conducted for one minute using a recipe with a coil power of 50 W, platen power of 8 W, flow rate of 20 sccm, pressure of 25 mTorr, and table temperature of 20°C. After hydrogen plasma etching, VDP measurements indicated that the sheet resistance of both samples was not measurable.

Despite achieving a well-controlled etching rate in the aforementioned experiments, when applied to hydrogen-terminated diamond samples, the Hall Kit measurements revealed that the diamond surface became not measurable after the dry etch process, contrary to hope of preserving the hydrogen termination on the diamond surface. One potential reason for the loss of surface conductivity may be attributed to the low stage temperature. It has been reported that the surface conductivity of hydrogen-terminated diamond decreases as the dry etch stage temperature decreases [139]. Another study suggests that hydrogen plasma etching conducted at room temperature tends to result in more surface defects and effectively etches off the diamond surface rather than preserving the termination [140]. Considering the findings from both reports, it is plausible that the plasma etching process employed in this study tended to etch off the surface, leading to the induction of an insulating diamond surface.

7.3 Pd as contact metal

This section presents the results of utilizing palladium (Pd) as an ohmic contact metal, aimed at investigating the difference between gold (Au) and palladium (Pd) ohmic contacts on hydrogen-terminated diamond. As discuses in the chapter 3, Au is suitable to form an ohmic contact on hydrogen terminated diamond due to its large work function (5.1-5.47 eV) that allows the conduction band sits near or below the valence band maximum of hydrogen terminated diamond which allows efficient charge transport between the Au and hydrogen terminated diamond. Pd

with a slightly higher work function (5.2-5.6 eV) than Au is energetically favourable to form ohmic contact with hydrogen terminate diamond as gold. A series of experiments were conducted for this purpose. Simple TLM structures were fabricated with either Au or Pd serving as the ohmic metal on two hydrogen-terminated diamond surfaces.

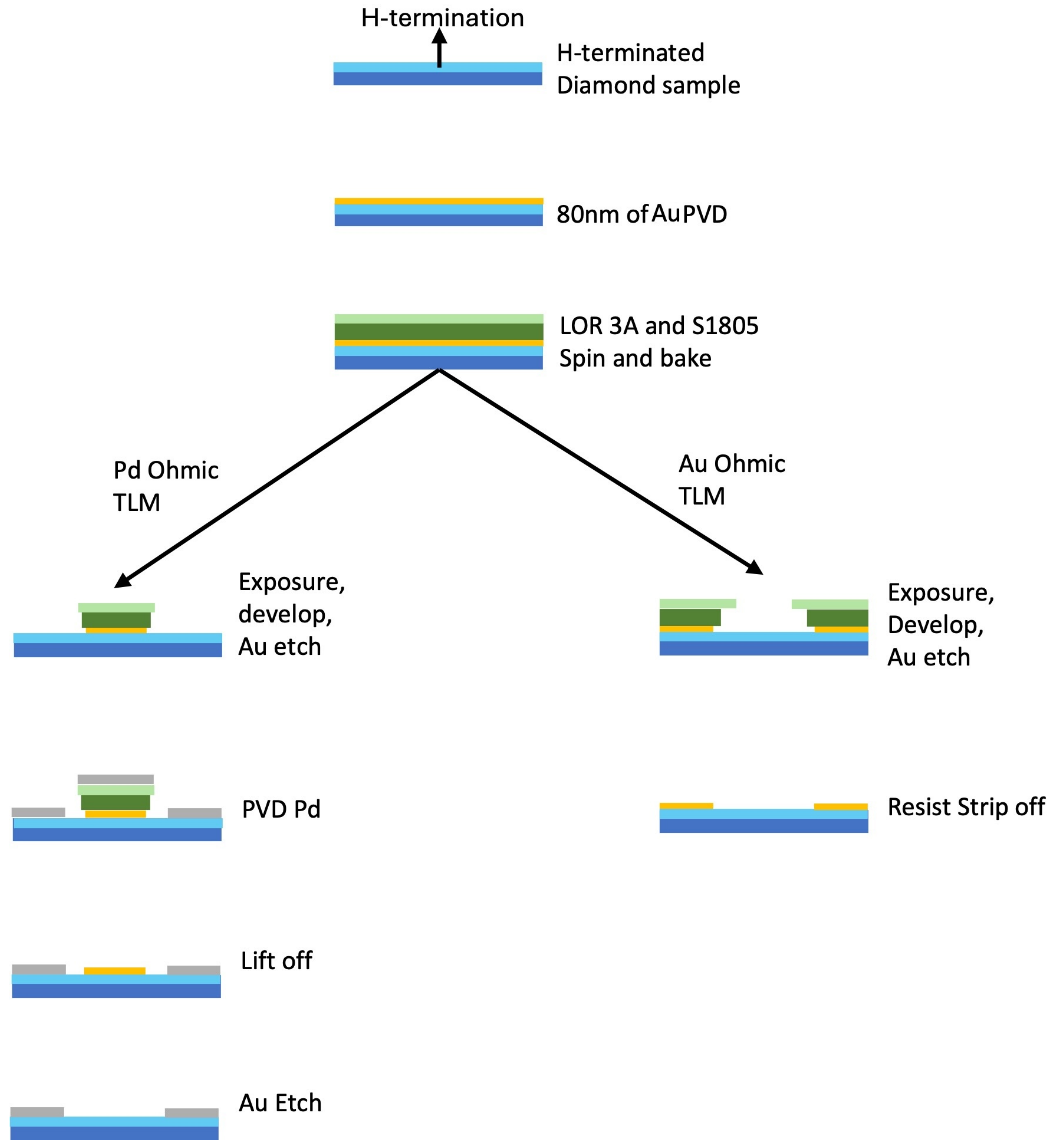


Figure 7.20: Fabrication flow of TLM with Pd or Au as ohmic contact metal.

Two single polished (100) diamond samples underwent cleaning and oxidation through an acid cleaning process as described previously. Subsequently, the samples were hydrogen-terminated using hydrogen plasma in Australia. Gold was then deposited on both samples to serve as a sacrificial layer. A bi-layer resist comprising LOR and S1805 was employed for photolithography. On sample A, 80 nm of Au was utilized as the TLM ohmic contact metal, while 80 nm if Pd was used for the ohmic contact metal on sample B. The TLM gap was set at 3 μm, 4 μm, 5 μm, 6 μm, and 7 μm. More details in terms of the resist process see Figure 7.20 and appendix A.1

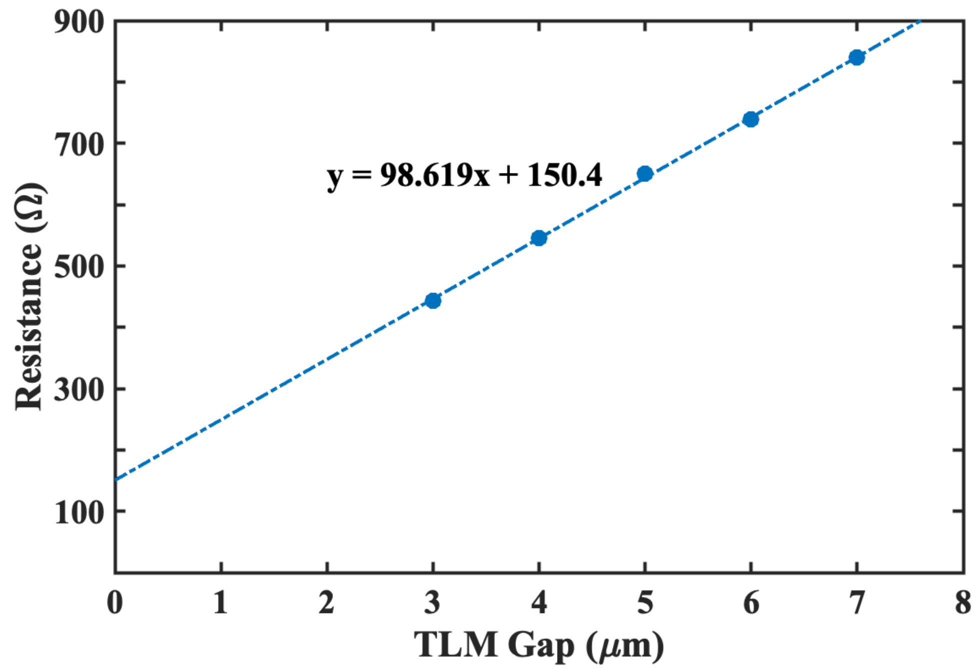


Figure 7.21: Au as ohmic metal TLM measurement results.

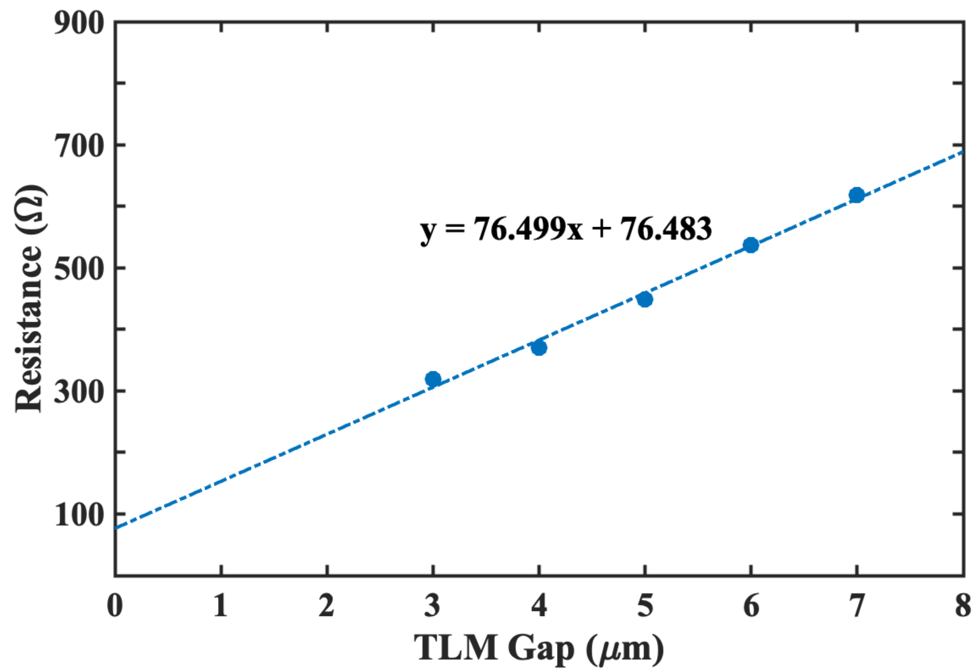


Figure 7.22: Pd as ohmic metal TLM measurement results.

Figure 7.21 and Figure 7.22 depict the TLM measurement results of the fabrication using Pd or Au as the ohmic metal. The sample employing Au as the ohmic metal exhibits a contact resistance of 7.52 $\Omega \cdot mm$ and a sheet resistance of 9.6 $k\Omega/\square$. The contact resistance of the TLM with Au as ohmic contact is within the range of literature reported ones, which is averagely around 5 $\Omega \cdot mm$ [46], [93], [95].

Conversely, the sample fabricated with Pd as the ohmic metal demonstrates a contact resistance of 3.82 $\Omega \cdot mm$, and a sheet resistance of 7.64 $k\Omega/\square$. This contact resistance is slightly higher than the literature recorded 0.4 $\Omega \cdot mm$ to 2.1 $\Omega \cdot mm$ [97], [141]of contact resistance formed between the Pd and hydrogen terminated diamond. However, this slight difference may be caused by the difference in the surface conditions, such as the sheet resistance. It has been observed that contact resistance between the hydrogen terminated diamond and Pd can be as high as 43 $\Omega \cdot mm$ when the sheet resistance of the hydrogen terminated diamond reaches 75 $k\Omega/\square$[142]. In conclusion, in this work, the contact resistance of Pd-formed ohmic contacts is lower compared to that of Au contacts when both diamond samples exhibits similar sheet resistance.

7.4 Chapter Summary

This chapter primarily discusses the results obtained from various non-traditional fabrication methods aimed at replacing the Au sacrificial layer commonly used in the fabrication of H-diamond FETs. LOR was investigated as an alternative to Au to protect the surface termination from damage caused by oxygen plasma and ambient environmental factors. However, the non-linear I-V characteristics observed in TLMs fabricated with LOR suggest the presence of resist residue. Subsequent AFM scans of the cross-grating structures on the diamond surface revealed that the resist residue could reach up to 14 nm.

The potential of using hydrogen plasma as a replacement for oxygen plasma to remove resist residue while preserving the surface termination was explored. Despite setting parameters that slowed the resist etching rate to 4.53 nm/min, surface conductivity measurements revealed that the surface had become insulating. The utilization of a low stage temperature in this process may have resulted in the hydrogen plasma etching off the diamond surface rather than just removind resist residue, thereby damaging the conductivity. Further optimisation of this process in future studies may yield better results however.

In the final part of the chapter, the ohmic contacts to H-daimond formed by Au and Pd were investigated and compared. The TLM results demonstrated that Pd forms an ohmic contact on the hydrogen-terminated diamond surface, with the contact resistance being lower than that of Au ohmic contact.

Chapter 8

Hydrogen terminated Diamond MESFETs

As discussed in the previous chapter, metals with low work function can be utilised on hydrogen-terminated diamond to form a Schottky contact. Aluminium (Al), lead (Pb), zinc (Zn), and titanium (Ti) have been reported to form Schottky contacts on hydrogen-terminated diamond[98]. Metals with high work function, such as gold (Au) and palladium (Pd), can be employed to form ohmic contacts on hydrogen-terminated diamond [97].

This chapter discusses the electrical measurement results of hydrogen-terminated diamond metal-semiconductor field-effect transistors (MESFETs) utilising an Al/Pt/Au metal stack for the gate and Au as the ohmic contact metal. Van der Pauw (VDP) and transmission line model (TLM) measurements yield results such as contact resistance (R_c), sheet resistance (R_s), carrier concentration (n_p), and carrier mobility (μ). MESFET measurements will illustrate device properties such as maximum drain current (I_{dmax}), transconductance (g), threshold voltage (V_{th}), and breakdown voltage.

The devices reported in this chapter were initially measured at room temperature. To assess the stability of the devices in ambient air, measurements were repeated after two weeks of exposure. Subsequently, atomic layer deposition (ALD) of Al_2O_3 was performed on the device surface to serve as encapsulation and electron acceptor. Further device measurements with Al_2O_3 were conducted at high temperature (400K) to explore thermal stability.

8.1 VDP and TLM structures with Au as contact metal

A 4.5×4.5 mm double-polished diamond sample was subjected to a two-step acid cleaning process, as detailed in the previous chapter(see appendix A.2), to remove potential contamination and residual fabrication structures. When the fabrication process commenced, the majority of samples were recycled, necessitating polishing to reduce surface roughness to below 1 nm.

Subsequently, the sample underwent hydrogen termination in Australia using hydrogen plasma. Upon its return, the sample was subjected to 2 to 3 days of exposure to ambient air to ensure stabilization of surface conductivity before fabrication commenced. The sample, sealed in a membrane sample box after the termination step, underwent an air exposure process, which facilitated the establishment of a layer of air adsorbates, thereby enhancing surface conductivity. Surface conductivity was monitored throughout this process using a VDP measurement process.

Following the stabilization of surface conductivity, a 50 nm gold sacrificial layer was deposited onto the surface by electron-ebeam evaporation to protect the hydrogen termination and function as the ohmic contact for devices. This step minimises the likelihood of exposure of the ohmic area and gate channel to ambient air and other steps, such as plasma ashing, which could potentially damage the surface termination. As the existed photo-lithography mask was designed to use gold sacrificial layer and ohmic metal, the device in this chapter used gold rather than palladium as ohmic contact. The fabrication process of the device has been elucidated in Chapter 4, with Figure 4.19 providing a detailed illustration of each step.

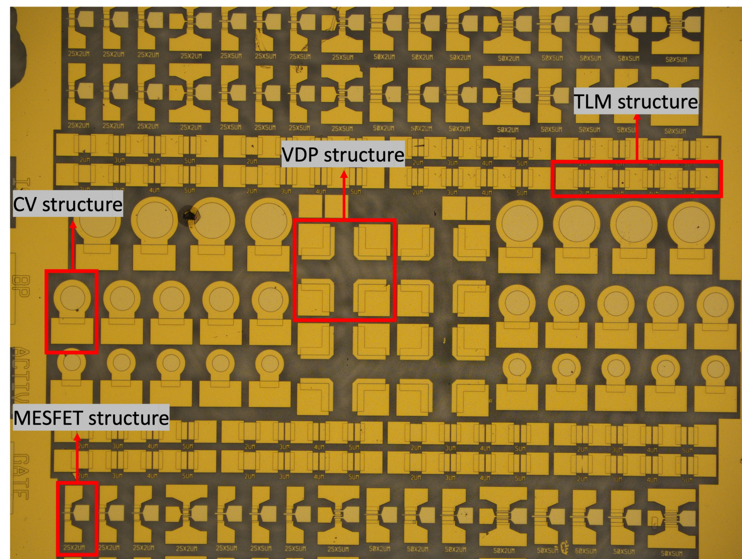


Figure 8.1: Optical image of sample with completed structures and devices fabricated with gold as sacrificial layer.

Following fabrication, a transmission line model (TLM) measurement was conducted, and Figure 8.2 presents the data extracted from this measurement. The width of the TLM structure is 75 μm, with a slope of 381.6 $\Omega/\mu m$. Calculating from this plot, the sheet resistance is determined to be 28.62 k$\Omega/\square$, consistent with the VDP-measured sheet resistance. Contact resistance can be derived from the intercept of this plot, yielding a value of 4.14 $\Omega \cdot mm$. This contact resistance value from the reported range for gold contacts on hydrogen-terminated diamond, typically falling between 4 to 5 $\Omega \cdot mm$ [95], [143].

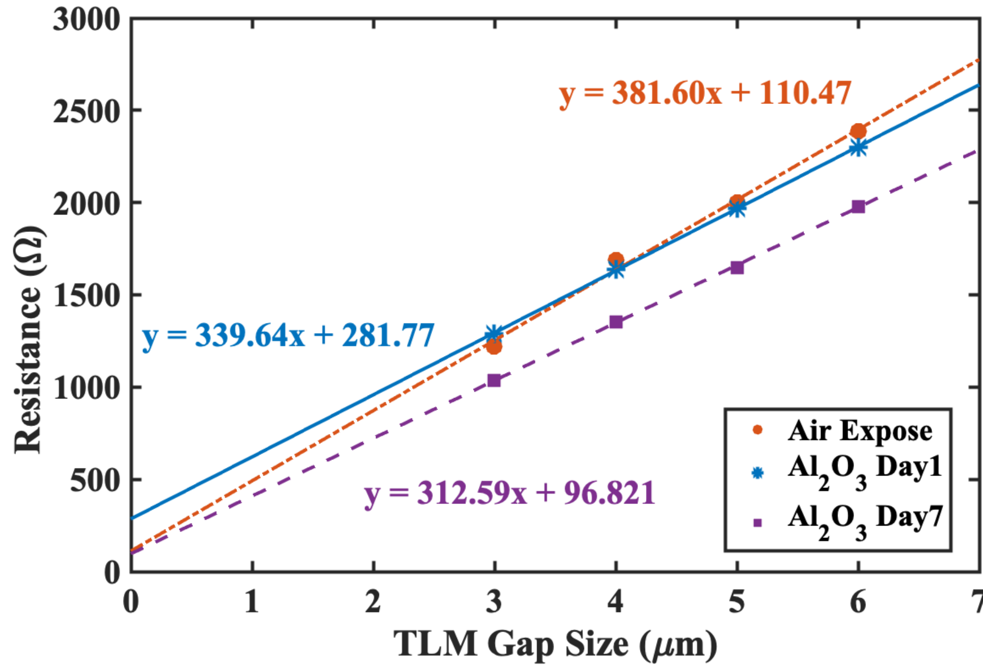


Figure 8.2: TLM results with sample exposed to air, day 1 and day 7 after ALD Al_2O_3 deposition.

In Chapter 4, experimental results of atomic layer deposition (ALD) of Al_2O_3 on hydrogen-terminated diamond were discussed (Table 4.2). VDP measurements revealed that thermal deposition of ALD Al_2O_3 improved surface conductivity from 9 kΩ/□ to 6 kΩ/□. This suggests that ALD Al_2O_3 enhances surface conductivity. Consequently, a 15 nm layer of ALD Al_2O_3 was deposited on the sample surface. Subsequent measurements were performed on both the TLM structure and the MESFETs, the latter to be discussed in the following section.

The blue line in Figure 8.2 represents the plot extracted from TLM measurement results. With a slope of 339.64 and an intercept of 281.77, the sheet resistance is calculated to be 25.425 kΩ/□ and the contact resistance to be 10.5375 $\Omega \cdot mm$. The sheet resistance decreased by more than 3 kΩ/□ after Al_2O_3 deposition, consistent with Chapter 4's findings. However, the doubled contact resistance post-deposition was unexpected, considering the protection of the contact area by the gold ohmic pad.

	Sheet Resistance (kΩ/□)	Contact Resistance ($\Omega \cdot mm$)
Air Adsorbates	28.620	4.14
Thermal ALD Al_2O_3	25.425	10.5375
7 days after Al_2O_3	23.4	3.63

Table 8.1: Sheet resistance and contact resistance after 30 days of air expose.

Subsequent to the sample that is covered with Al_2O_3 being exposed to ambient air for seven days, the TLM was remeasured. The purple dotted line in Figure 8.2 indicates that the sheet

resistance remained relatively stable. However, the contact resistance decreased from 10.537 $\Omega \cdot mm$ to 3.63 $\Omega \cdot mm$, returning to its value after initial device fabrication. Hypothetically, any airdsorbates between the H-diamond/gold interface was disturbed during the thermal ALD Al_2O_3 deposition. The reaction chamber temperature (200 °C) potentially can disturb the air adsorbates on the diamond surface. The underlying reasons for these changes in contact resistance will be explored further in subsequent measurements. However, this changes is temporary as the contact resistance measured with TLM back to normal seven days after the thermal oxide deposition.

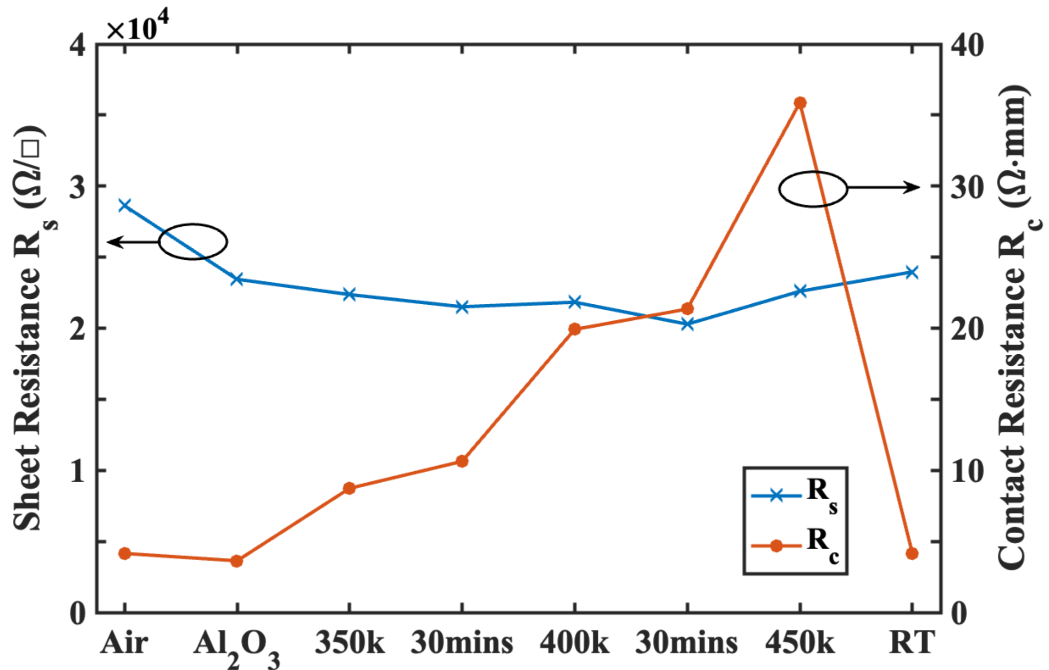


Figure 8.3: Sheet resistance and contact resistance before and after Al_2O_3 and under different temperature.

To assess the thermal stability of the sample following ALD Al_2O_3 coverage, high-temperature TLM measurements were conducted. The sample was placed on a heating stage and sealed under low vacuum conditions. The stage temperature was increased stepwise from room temperature (300 K) to 350 K, 400 K, and 450 K. At each temperature stage, TLM measurements were performed. Additionally, the stage temperature was maintained at each level for 30 minutes, with two measurements conducted at each stage, except for the highest temperature of 450 K, which was measured once for safety.

Figure 8.3 illustrates the sheet resistance and contact resistance of the TLM at various stages and temperatures. The sheet resistance of the sample surface exhibited slight fluctuations, ranging between 24 kΩ/□ and 21 kΩ/□ from room temperature to 450 K, returning to 22.5 kΩ/□ thereafter. This indicates that the surface conductivity of hydrogen-terminated diamond under ALD Al_2O_3 oxide remains relatively stable between room temperature and 450 K. In Crawford

et al report, the exposed to air hydrogen terminated diamond shows sheet resistance drop at around 345 K[144].

However, the contact resistance began to increase at 350 K. With continued temperature elevation, the contact resistance rose from 3.63 $\Omega \cdot mm$ at room temperature to 8.733 $\Omega \cdot mm$ at 350 K, with slight increments observed during each 30-minute temperature hold. The highest contact resistance measured was 35.87 $\Omega \cdot mm$ at 450 K.

A hypothesis posits that residual air adsorbates beneath the gold ohmic pad induce the temperature sensitivity of the hydrogen-terminated diamond. The gold forms an ohmic contact with the hydrogen-terminated diamond. However, the gold and H-diamond surface are just sticked together with weak Van der Wal forces. As the temperature rises, some air adsorbates are disrupted, which affects the contact between the gold and the hydrogen-terminated diamond. This hypothesis requires further investigation in future work. A potential experiment involves depositing gold on the hydrogen-terminated diamond after high-temperature (400 °C) annealing, which is used to remove the air adsorbates. The hypothesis can be confirmed if subsequent I-V testing of the sample at elevated temperatures shows constant contact resistance.

After the high-temperature measurements, the sample was stored at room temperature for 6 months. Subsequent TLM measurements showed that the sheet resistance remained consistent at 24 $k\Omega/\Box$, consistent with measurements before high-temperature testing and after oxide deposition. The contact resistance, which had increased to 35.87 $\Omega \cdot mm$ at 450 K, decreased to 4.1625 $\Omega \cdot mm$, matching the value measured after oxide deposition at room temperature. This decrease in contact resistance supports the hypothesis that the increase during high-temperature measurement resulted from residual air adsorbate disruption beneath the gold. Moreover, the temperature caused disruption is restored after the temperature drop back to the room temperature.

Similarly, this disrupt may occur on the hydrogen-terminated diamond surface between two TLM ohmic pads. However, it is assumed that defects potentially formed within the ALD Al_2O_3 layer may act as electron acceptors, enhancing surface conductivity. The ALD Al_2O_3 deposition process at 200°C can partially remove air adsorbates, allowing defect-mediated surface conductivity enhancement to dominate. This explains the stable sheet resistance despite the significant increase in contact resistance. Kevin et al. also observed enhanced thermal stability of surfaces covered with low work function material (V_2O_5) at temperatures up to 520 K [144].

Hall kit measurements were conducted before fabrication commenced. Four probes made direct contact with the sample's four corners, yielding a sheet resistance of 35.99 $k\Omega/\Box$. The higher sheet resistance of this sample, compared to reported values (2-20 $k\Omega/\Box$ [69], [145]), may be attributed to surface defects resulting from the sample recycling process. The higher sheet re-

sistance measured by VDP, compared to TLM-extracted values, may result from the inaccuracy of the VDP measurement. Since this measurement was not conducted with lithographically defined VDP structures on the sample surface, the sheet resistance results might vary from the real values and the values extracted from the TLM structures (28.62 $k\Omega/\square$).

Subsequently, VDP measurements were conducted again after ALD Al_2O_3 deposition with a VDP structures. The results showed a decrease in sheet resistance post-Al_2O_3 deposition ($24.17k\Omega/\square$), consistent with TLM measurements. As this VDP measurement were conducted on properly lithographically defined VDP structure, this result is relatively reliable. The post-high-temperature VDP measurements indicated the sheet resistance wasn't affected by the high temperature measurements. This results matches the finding concluded from the TLM measurements.

Table 8.2 presents the measurement results of the sample before and after oxide deposition.

	Sheet Resistance (k$\Omega/\square$)	Mobility ($cm^2/V \cdot s$)	Concentration (cm^2)
Air Adsorbates	35.99	NaN	NaN
ALD Al_2O_3	24.17	79.1	3.26×10^{12}
After High Temperature	25.7	79.1	3.07×10^{12}

Table 8.2: VDP measurement of the sample.

To conclude this section, both VDP and TLM structures were measured using a Hall Kit and probe station before and after ALD Al_2O_3 deposition. The thermal deposition of ALD Al_2O_3 on the sample surface resulted in improved surface conductivity, as evidenced by the drop in sheet resistance measured by both TLM and VDP structures. A increase of contact resistance after the ALD Al_2O_3 deposition was observed. However, seven days after the oxide deposition, TLM structures were remeasured, and the contact resistance returned to the level observed before the oxide deposition while the sheet resistance remained at a reduced amount.

Subsequently, the sample was subjected to elevated temperatures ranging from 350K to 450K. The sheet resistance remained relatively stable within this temperature range. The observed increase in contact resistance is assumed to be attributed to the potential disruption of air adsorbates under high temperatures, a phenomenon observed after both the thermal oxide deposition and during high-temperature measurements. Subsequent TLM and VDP measurements showed that the sheet resistance and contact resistance returned to its pre-high-temperature level.

This series of measurements confirms the efficacy of thermal ALD Al_2O_3 deposition in improving surface conductivity by 17% and highlights the impact of high temperatures on contact resistance, attributed to the air residue disruption.

This comprehensive analysis provides valuable insights into the thermal stability and surface properties of hydrogen-terminated diamond samples, essential for optimizing device performance and reliability in various applications.

8.2 MESFET measurement before and after air exposure

In the previous section, immediate measurements were conducted on the devices post-fabrication, followed by an additional measurement after covering the sample with 15 nm of ALD Al_2O_3. Both TLM and VDP results indicated an improvement in surface conductivity after Al_2O_3 deposition. This section will delve into the results of room temperature measurements of the air H-Diamond MESFETs.

The gate metal stack for the devices comprises 20 nm of aluminium (in contact with the H-diamond), 20 nm of platinum, and 80 nm of gold on the top.

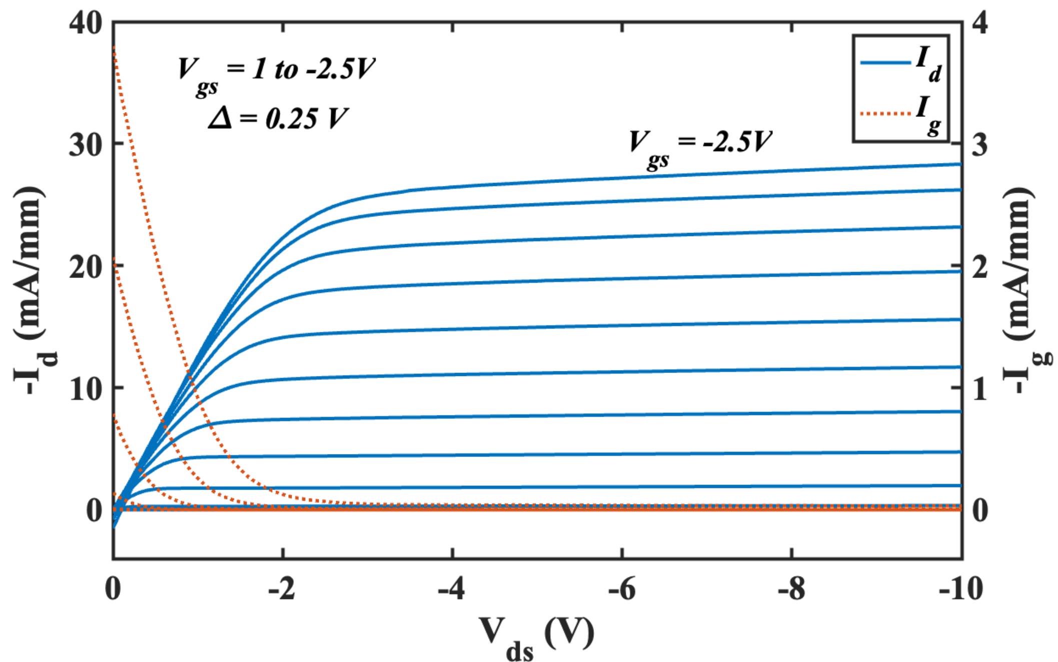


Figure 8.4: Output characteristics for $2\mu m$ MESFETs with H-diamond surface expose to air. Drain current is shown in blue solid line, and gate leakage current is shown in orange dot line.

In the acquired device I-V output characteristics depicted in Figure 8.4, it is evident that for a positive gate-source voltage, the device is turned off. As discussed in the previous chapter, the hydrogen-terminated diamond surface with air adsorbates forms a hole accumulation area, providing a channel for current flow. When a positive voltage is applied to the gate, holes near the surface are repelled, thus closing the channel when the voltage reaches threshold.

Conversely, when a negative voltage is applied to the gate, more holes are attracted to the sur-

face, increasing the charge density with the channel, allowing more current to flow through the channel. Increasing the negative voltage applied to the gate leads to higher drain current. When a fixed negative gate voltage is applied, increasing the drain voltage initially places the device in the linear region, where the on resistance can be extracted. As the drain-source voltage keep increasing, the drain current reaches saturation, representing the maximum drain current that can be extracted. In this device, a maximum drain current (I_{dmax}) of 28.3 mA/mm is observed at a gate voltage of -2.5V, with a gate length of 2 μm. The on resistance (R_{on}) is extracted as 90 $\Omega \cdot mm$. While this current is lower than the typically reported 100 mA/mm for air adsorbate devices [94], it remains comparable considering the much shorter gate length (250 nm) used in that report, and the much lower sheet resistance of the sample used in that work, which was around 7 k$\Omega/\square$.

The orange dot line in Figure 8.4 represents the gate leakage current. With a low drain-source voltage, the gate leakage current increases as the drain voltage decreases. When a high voltage is applied to the gate, more holes accumulate near the junction interface. If the drain-source voltage is not high enough, some carriers may tunnel through the Al-Diamond junction and flow through the gate, forming a gate leakage current. For instance, when the gate voltage is -2.5 V, gate leakage current is larger when the drain voltage is below -2.5 V, and increases exponentially when the drain voltage is below 1.5 V.

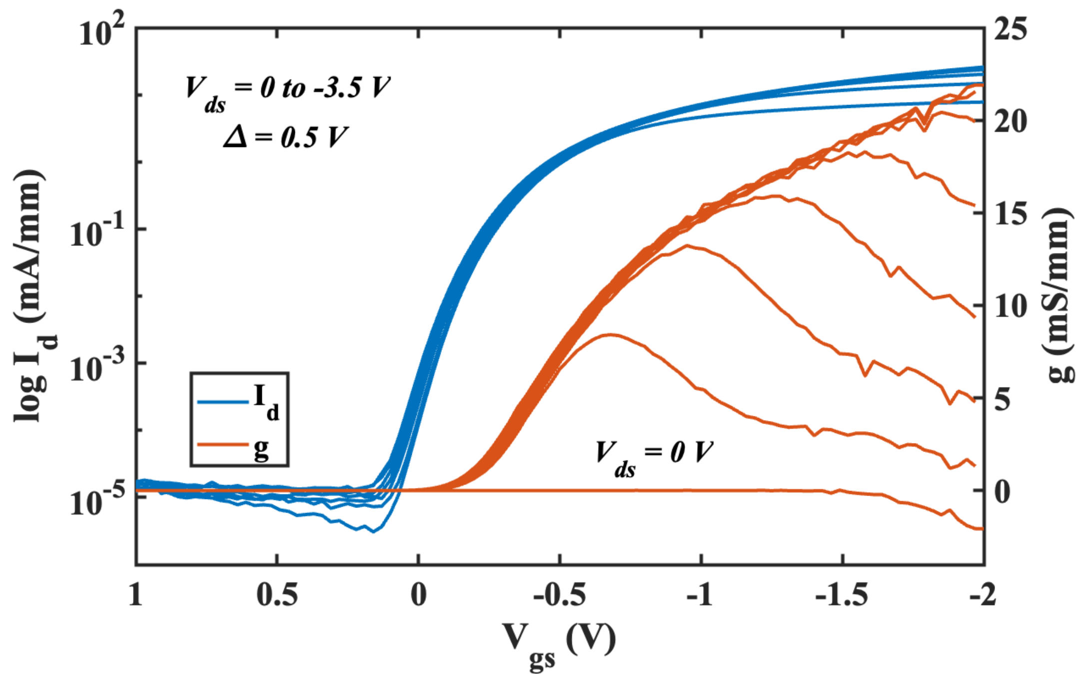


Figure 8.5: Transfer characteristic of 2μm MESFETs with H-diamond surface expose to air. Drain current is shown in blue solid line, and extrinsic transconductance is shown in orange line.

Figure 8.5 illustrates the transfer characteristic of the same 2 μm MESFETs device. The drain-

source voltage is swept from 0 to -3.5 V with a step of 0.5 V, and the drain current is plotted on a logarithmic scale. To extract threshold voltage, at the noise floor, when the drain current in the order of 1×10^{-5} mA/mm, the threshold voltage (V_{th}) occurs when the gate voltage is around 0.1 V; below this voltage, the device is fully on. For a set off-state current density of 1 $\mu A/mm$, $V_{th} < 0V$ is extracted across the inspected V_{ds} range of 1 V to -2 V. The I_{on}/I_{off} ratio from the graph is of the order of 10^6, which is two order of magnitude lower comparing to the reported 10^8 for hydrogen-terminated diamond MESFETs [146].

Transconductance reflects how efficiently a FET device can convert a change in gate voltage (V_{gs}) into a change in output current (I_{ds}). As depicted in Figure 8.5, the maximum extrinsic transconductance is approximately 22 mS/mm when the drain voltage is -3.5 V. This is not as high as reported values of 137 mS/mm and 150 mS/mm [96], [143]. However, this discrepancy may be due to the much higher sheet resistance (29 $k\Omega/\square$) of the sample in this work compared to the reported sheet resistance (11 $k\Omega/\square$) in the literature. In addition, the much shorter gate length (250 nm to 50 nm) in the literature compared with the gate length (2 μm) in this work also contributes to a higher transconductance.

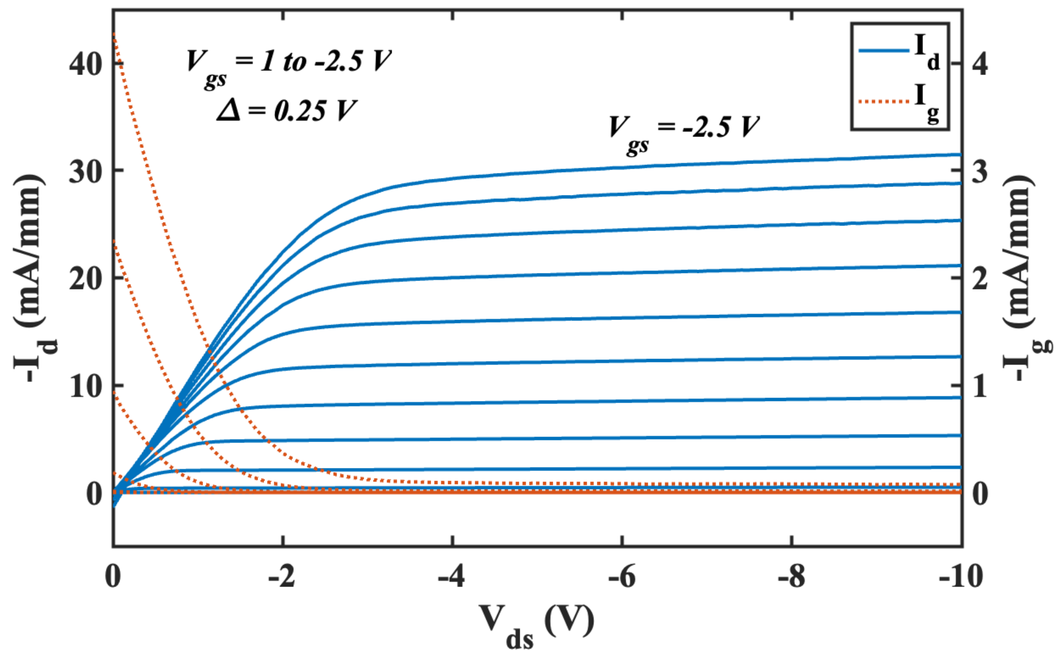


Figure 8.6: Output characteristics for $2\mu m$ MESFETs with atmospheric adsorbates after 14 days of air expose.

Figure 8.6 presents the output characteristics of the same MESFET devices after exposure to air for 14 days. The plot shows a slight increase in maximum drain current from 28.3 mA/mm to 31.5 mA/mm. The turn-on resistance after exposure is 88 $\Omega \cdot mm$, slightly lower than before the 14 days of air exposure. The highest gate leakage current is slightly shifted higher from 3.9 mA/mm to 4.3 mA/mm. This increase in maximum drain current and decrease in turn-

on resistance may be attributed to air exposure of the sample. During the fabrication process, although the surface was protected by the gold sacrificial layer, there is still a risk of disrupting the air adsorbates. However, this process is reversible; once the hydrogen-terminated surface is exposed to the air, air adsorbates can build up on the surface again, thereby improving surface conductivity, leading to an increase in drain current and a decrease in turn-on resistance.

Figure 8.7 illustrates the transfer characteristic of the same MESFET devices after 14 days of exposure to air. The threshold voltage at set off-state current 1 $\mu A/mm$, extrinsic transconductance, and I_{on}/I_{off} ratio after air exposure are 0 V, 22 mS/mm, and 10^7, respectively, which is consistent with the data extracted before the air exposure.

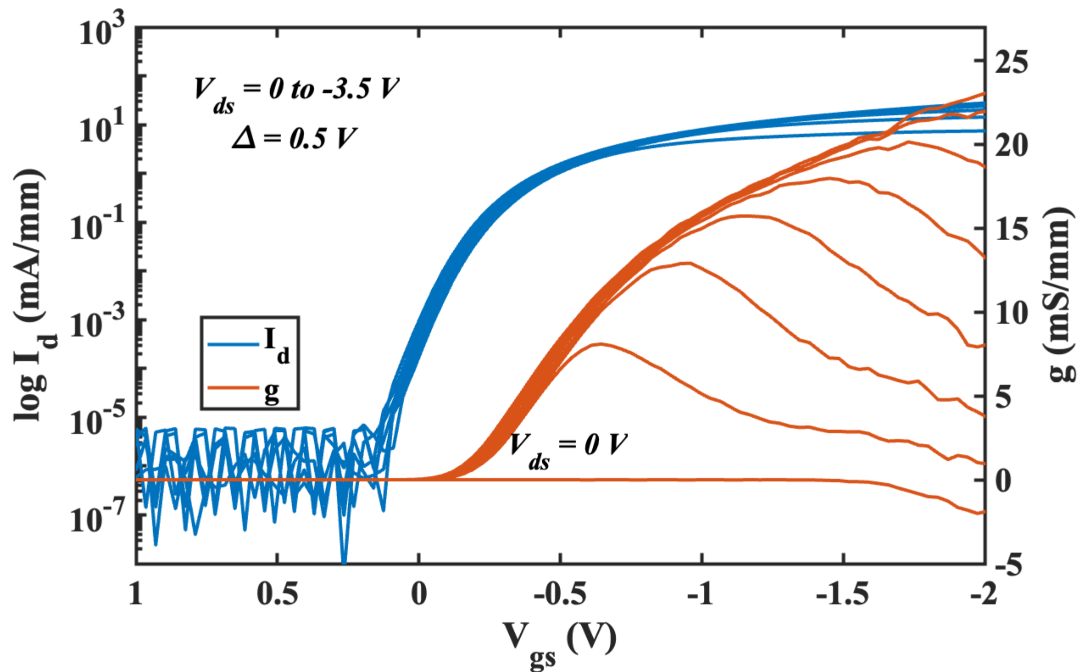


Figure 8.7: Transfer characteristic of $2\mu m$ MESFETs with atmospheric adsorbates after 14 days of air expose.

Multiple V_{ds} sweeps were conducted on one device with the same gate length and width. The actual sweep applied on this device is 20 times. However, all sweep results slightly fluctuated between the highest and lowest drain current; thus, only 5 sweeps, including the one with the highest drain current and the one with the lowest drain current, are plotted in this thesis. Figure 8.8 shows a very slight increase (4%) in maximum drain current after 3 sweeps, from 20.7 mA/mm to 21.6 mA/mm. Then the current started to drop back after the fourth sweep. The turn-on resistance changed slightly from 106 $\Omega \cdot mm$ to 103 $\Omega \cdot mm$. In this case, the device is considered working consistently after 20 repeated sweeps.

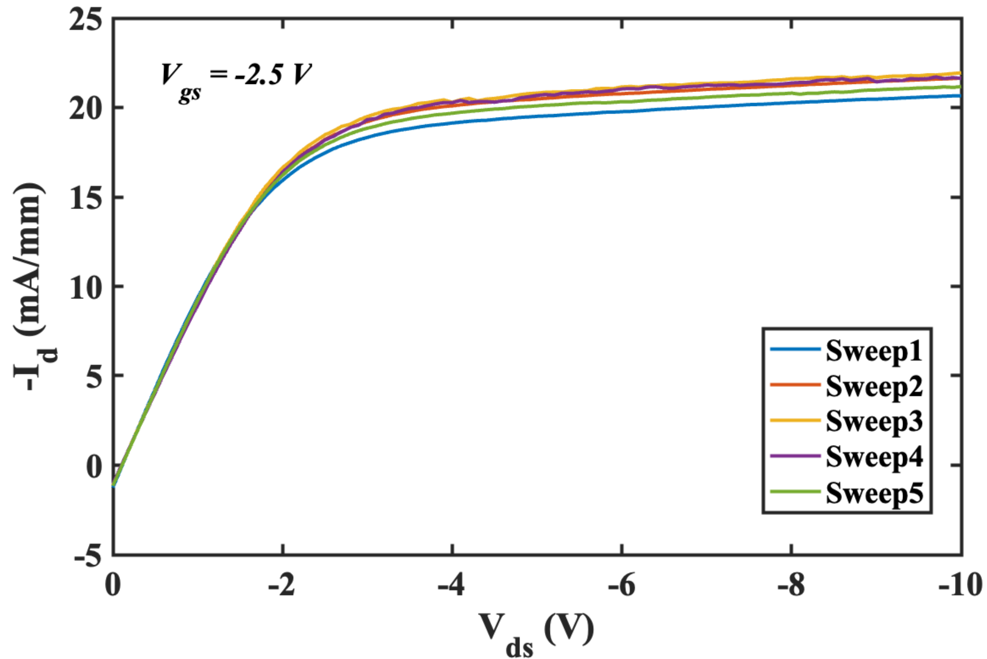


Figure 8.8: Output characteristics multiple sweep with gate bias $V_{gs} = -2.5V$.

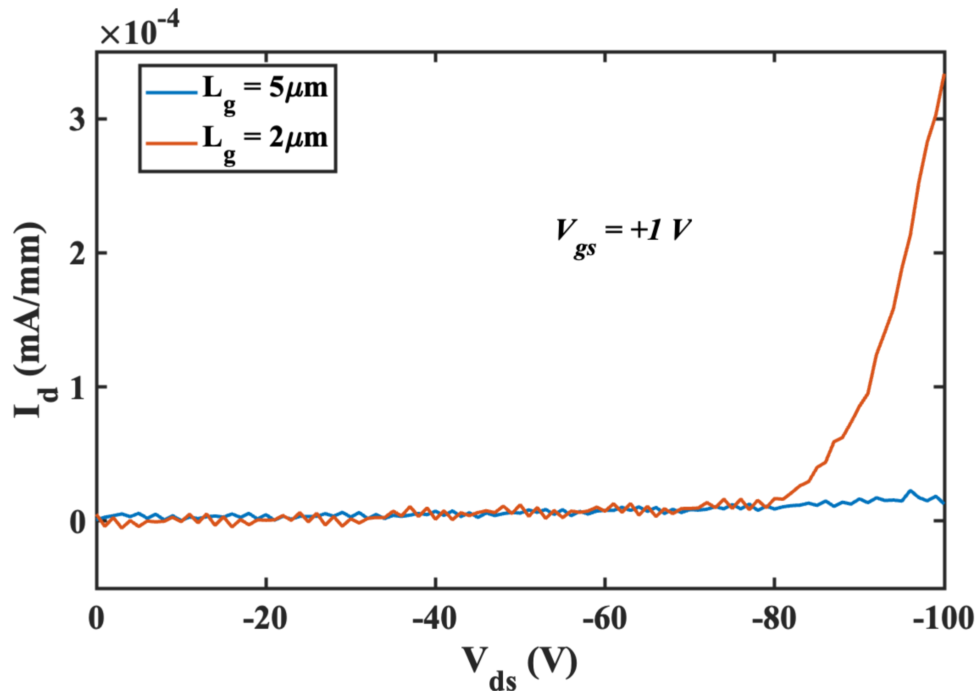


Figure 8.9: Off-state break test of devices with gate lengths of $2\mu m$ and $5\mu m$.

Figure 8.9 illustrates the off-state breakdown test of two devices with gate lengths of 2 μm and 5 μm, respectively, both with a gate width of 25 μm. To ensure the device is turned off, a +1V bias was applied to the gate. The measurement shows that the devices with gate length of 2 μm started to breakdown when the drain voltage is around 80V. For the device with a gate length of 5 μm, the breakdown voltage is higher than 100V, which is the limit of the measuremnt system

used.

In summary, longer air exposure may generally improve surface conductivity, leading to an increase in drain current and a slight decrease in turn-on resistance. However, other properties such as transconductance, I_{on}/I_{off} ratio, and turn-on resistance remain consistent before and after air exposure. Subsequent multiple sweeps on one device indicate that the device operates consistently after 20 sweeps. The off-state breakdown test demonstrates that a device with a gate width of 25 μm and length of 2 μm breaks down when the drain voltage reaches 80V.

	I_{dmax} (mA/mm)	$I_{gleakage}$ (mA/mm)	Peak g (mS/mm)	R_{on} ($\Omega \cdot mm$)	I_{on}/I_{off}	V_{th} (V)	Off-state Break-down (V)
Air Adsorbates	28.3	3.9	22	90	10^6	0	N/A
14 days expose	31.5	4.3	22	88	10^7	0	-80

Table 8.3: Comparison of device before and after 14 days of air expose.

8.3 MESFET with thermal ALD Al_2O_3

In the preceding section, the output and transfer characteristics of the MESFET after a 14-day period of air exposure were discussed, with a potential slight improvement in drain current and worse gate current leakage observed. This section will delve into the measurement results of the device after the deposition of 15 nm of thermal ALD Al_2O_3, providing a detailed comparison between the device before and after the Al_2O_3 deposition.

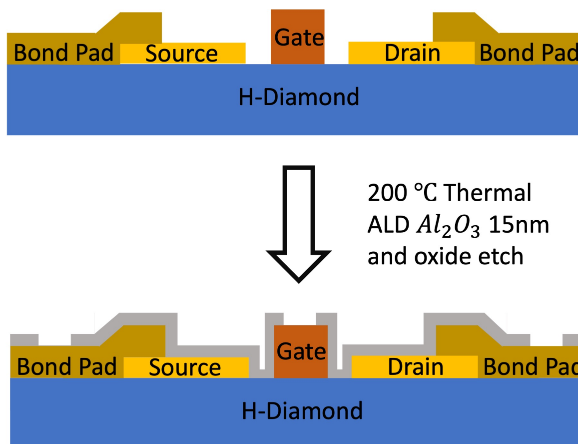


Figure 8.10: FET structure with atmospheric adsorbates (top) and 15nm of ALD Al_2O_3 (bottom). Ohmic contacts were 80nm Au and the gate contact was 20nm Al/20nm Pt/80nm Au.

Post-oxide deposition, an additional photolithography step was performed to open resist windows in the Al_2O_3 on the gate pad, source, and drain bond pads to allow for direct electrical

probing. Buffered oxide etch was then utilized to remove the Al_2O_3 over these contact regions. This step serves two purposes: firstly, it facilitates better contact, minimizing the need to probe through the Al_2O_3 and potentially damage the metal pad; secondly, it reduces the contact resistance between the pad and probe, thereby ensuring more accurate measurement results.

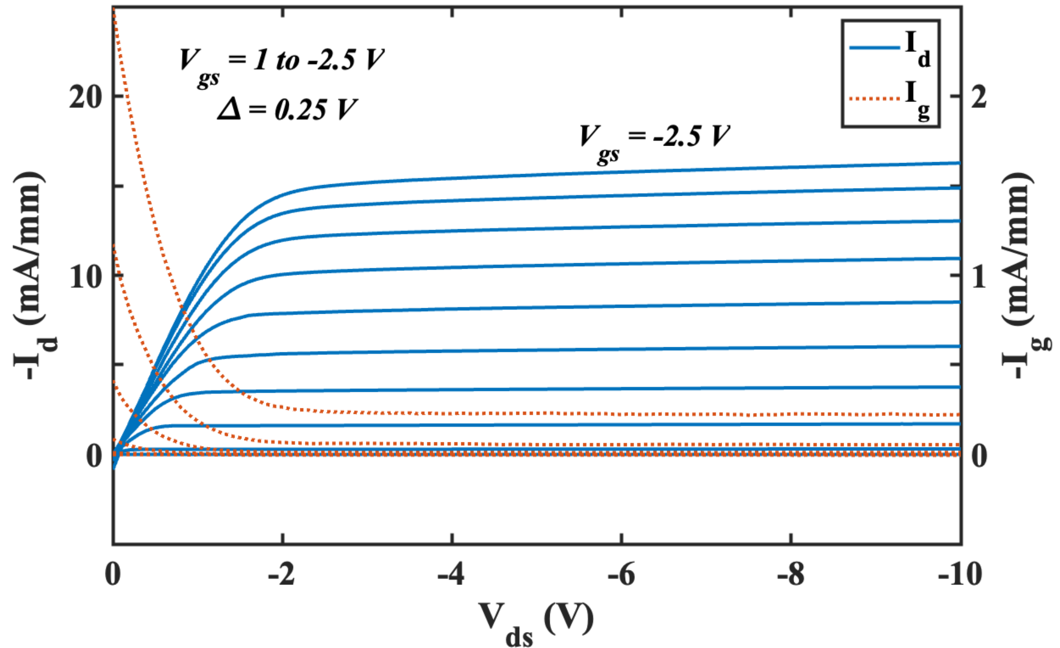


Figure 8.11: Output characteristics for 5 μm MESFETs with atmospheric adsorbates after 14 days of air expose.

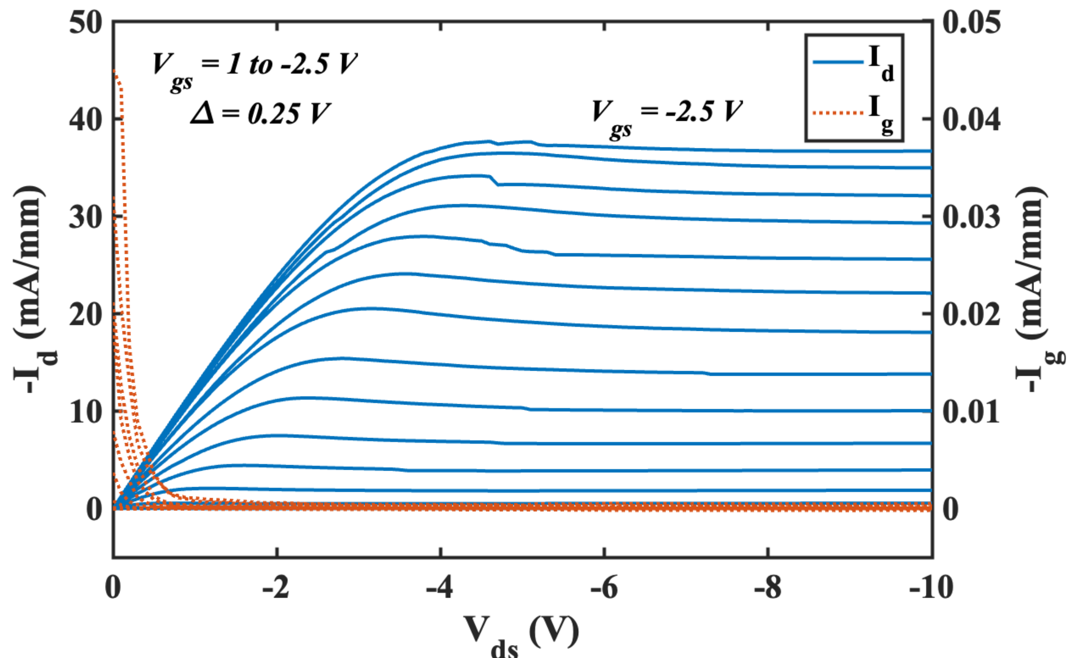


Figure 8.12: Output characteristics for 5 μm MESFETs with ALD Al_2O_3.

Figure 8.11 displays the output characteristics of a 5 μm long gate MESFET after 14 days of air exposure and before the deposition of ALD Al_2O_3. The maximum drain current is 16.3 mA/mm when the gate-source voltage is at -2.5 V. The drain current maximum is lower than that discussed above for the 2 μm gate device, which is most likely caused by a larger gate length. The gate leakage current increases with the decrease in drain-source voltage, with the maximum leakage gate current being 2.49 mA/mm. The linear working region is when the drain-source current is between 0 to -1.5 V when the gate voltage is at -2.5 V. The on resistance extracted from this linear region is 99 $\Omega \cdot mm$. The device operates in the saturation region when the drain voltage is lower than -1.5 V.

Figure 8.12 illustrates the output characteristics of the same device after the deposition of 15 nm ALD Al_2O_3. The maximum drain current is 37.5 mA/mm, which is twice the drain current before the oxide deposition. The device operates under the linear region when the drain-source voltage is between 0 and -4 V, a wider range than that of the air adsorbates devices. The on resistance is calculated as 90 $\Omega \cdot mm$. The on resistance includes the 2 times the ohmic contact resistance (R_c), channel resistance under the gate (R_{Gch}), and the source-to-gate and drain-to-gate channel resistance (R_{ch}). As discussed in the previous section, the deposition of ALD Al_2O_3 reduces the sheet resistance, which can reduce the channel resistance and subsequently the on resistance.

$$R_{on} = 2R_c + R_{ch} + R_{Gch} \tag{8.1}$$

The previous section discussed the TLM and VDP measurements before and after the ALD Al_2O_3 deposition. An improvement of the sheer resistance was observed from both measurements. This indicates the oxide might provide a higher concentration of carrier on the H-diamond surface, thus improve the maximum drain current of the MESFETs.

Apart from the improvement in maximum drain current and slightly reduced on resistance, the gate leakage current has improved dramatically. The maximum gate leakage current dropped from around 2.5 mA/mm to 0.05 mA/mm, which is a two-order-of-magnitude reduction in the gate leakage current. The decrease in the gate leakage further suggests that there is a larger barrier between the gate-diamond interface, which reduces the current flow through the gate.

Figure 8.13 and 8.14 illustrate the transfer characteristics for this device before and after the Al_2O_3 deposition. The threshold voltage shifted more depletion mode from -0.5 V to 0.6 V, further indicating that the Al_2O_3 provides higher carrier concentration, which takes a higher gate voltage to turn off the channel between the sourcce and drain contact. Another piece of evidence showing that carrier concentration change is the I_{on}/I_{off} ratio, which changed from 10^6 to 10^4. This change is caused by a higher off-state drain leakage current, which is increased due to the improvement of surface conductivity. Additionally, the transconductance after the oxide deposition (16 mS/mm) is slightly lower than that before the deposition, which is 18

mS/mm. As the extrinsic transconductance highly limited by total source access resistance, so it might be influenced gently by by sheet resistance, gate contact and ohmic contact.

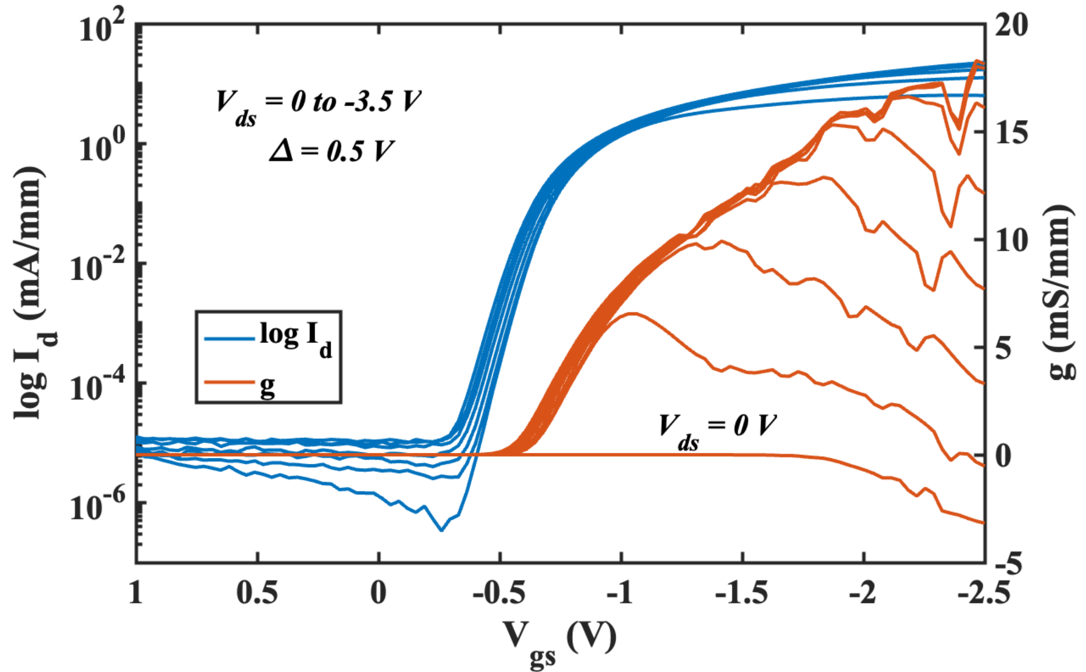


Figure 8.13: Transfer characteristics for 5 μm MESFETs with atmospheric adsorbates after 14 days of air expose.

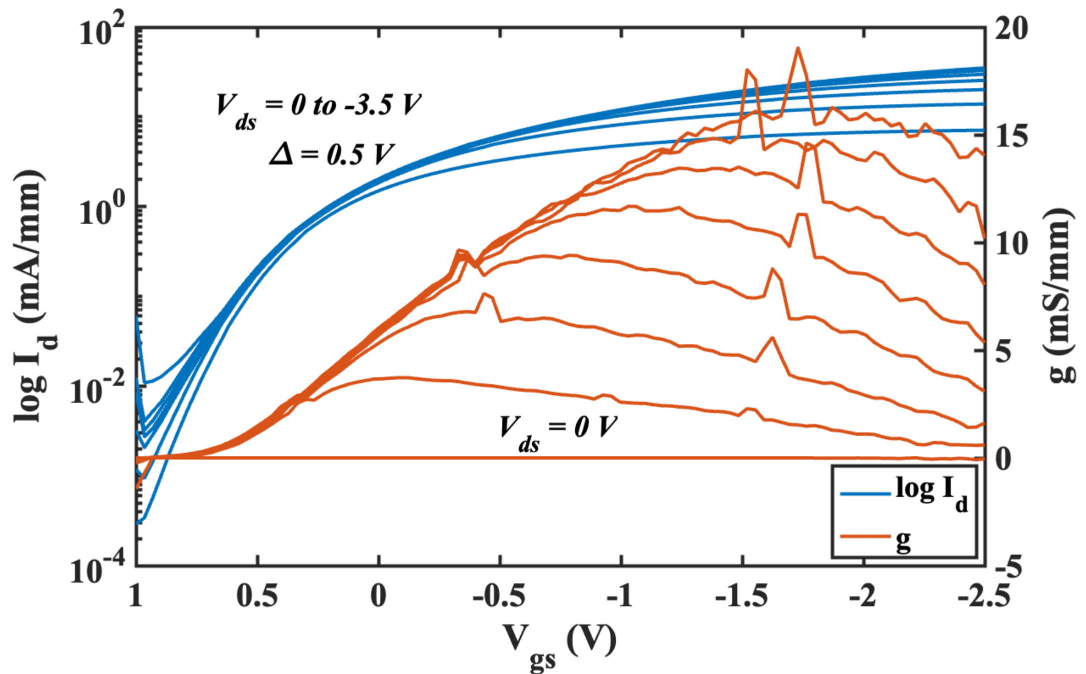


Figure 8.14: Transfer characteristics for 5 μm MESFETs with ALD Al_2O_3.

	I_{dmax} mA/mm	$I_{gleakage}$ mA/mm	Peak g mS/mm	I_{on} / I_{off}	V_{th} (V)	R_{on} $\Omega{\cdot}mm$	R_c $\Omega{\cdot}mm$	R_s k$\Omega/\square$	R_{ch} $\Omega{\cdot}mm$	R_{Gch} $\Omega{\cdot}mm$
Air	16.3	2.49	18	10^6	-0.5	99	4.15	28.6	28.6	33.5
ALD Al_2O_3	37.5	0.05	16	10^4	0.6	90	3.6	23.4	23.4	36

Table 8.4: Comparison of device before and after oxide deposition.

In summary, the maximum drain current of the devices improved from 16.3 mA/mm to 37.5 mA/mm after the deposition of ALD Al_2O_3. Due to the improvement in surface conductivity, the I_{on}/I_{off} ratio dropped because of the increase in off-state drain leakage current. The two-order-of-magnitude reduction in gate leakage current, lower transconductance indicate some chemical or physical modification to the gate contact occurred during the Al_2O_3 deposition process. Table 8.4 lists all the parameters extracted from the experimental results. The final calculation of the gate channel resistance after the oxide deposition slightly increased compared to that before the deposition. In conclusion, the ALD Al_2O_3 improves the surface conductivity, possibly explained by defects formed in the oxide growth process serving as acceptors. Further study required to explore the reduction of the gate leakage current.

8.4 MESFET high temperature measurement

In the final set of measurements conducted on this Al_2O_3 encapsulated sample, high-temperature measurements were performed. The sample was placed on a stage capable of heating up and sealed under a low to medium vacuum chamber. Measurements were taken at room temperature (300 K), 350 K, 400 K, and 450 K, respectively. To test the stability over the duration of heating, the stage was maintained at 300 K and 400 K for 30 minutes, and the sample was remeasured. In this section, the output and transfer characteristics of the same device with a gate width of 50 μm and a length of 5 μm at different temperatures will be discussed and compared.

Figure 8.15 and Figure 8.16 illustrate the output characteristics of one device at different temperatures. At room temperature, the maximum drain current is approximately 39.6 mA/mm when the gate-source voltage is -2.5 V and the drain-source voltage is -10 V. However, as the temperature increases, the maximum drain current starts to decrease. At 350 K, it drops to 27.4 mA/mm, and after 30 minutes at this temperature, it further decreases to 22.7 mA/mm. Subsequently, at 400 K, 400 K after 30 minutes, and 450 K, the maximum drain current is measured as 13.7 mA/mm, 11 mA/mm, and 10 mA/mm, respectively. This decrease in maximum drain current with elevated temperature may be caused by the disruption of air adsorbates under the gate, source, and drain contacts. As observed in the TLM measurements, the sheet resistance fluctuates slightly between 21 k$\Omega/\square$ and 24 k$\Omega/\square$ with elevated temperature, while the contact resistance increased from 3.8 $\Omega \cdot mm$ to 35.8 $\Omega \cdot mm$ with elevated temperature, thus providing

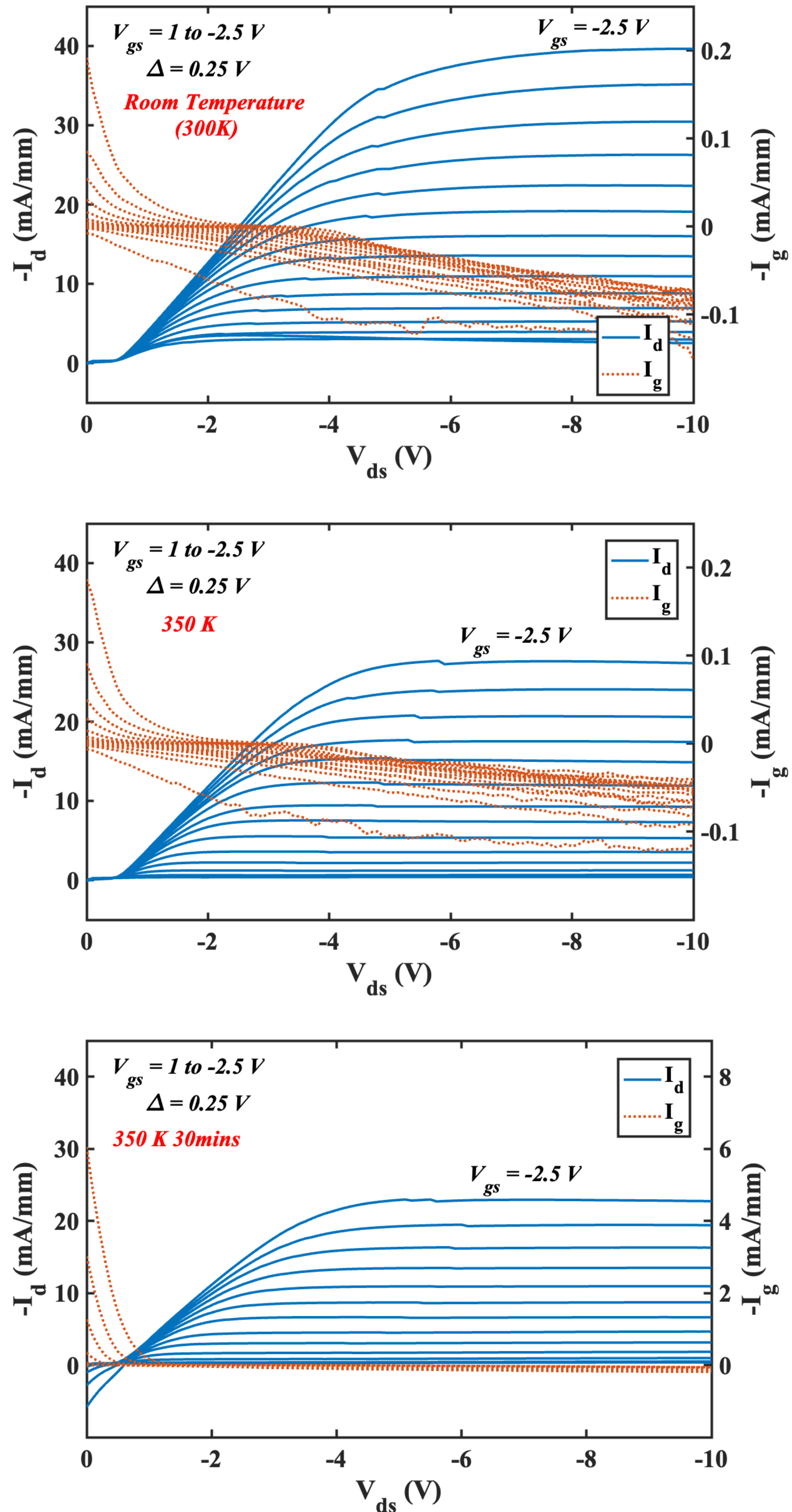


Figure 8.15: Output characteristics at 300 K, 350 K and 350 K for 30 mins.

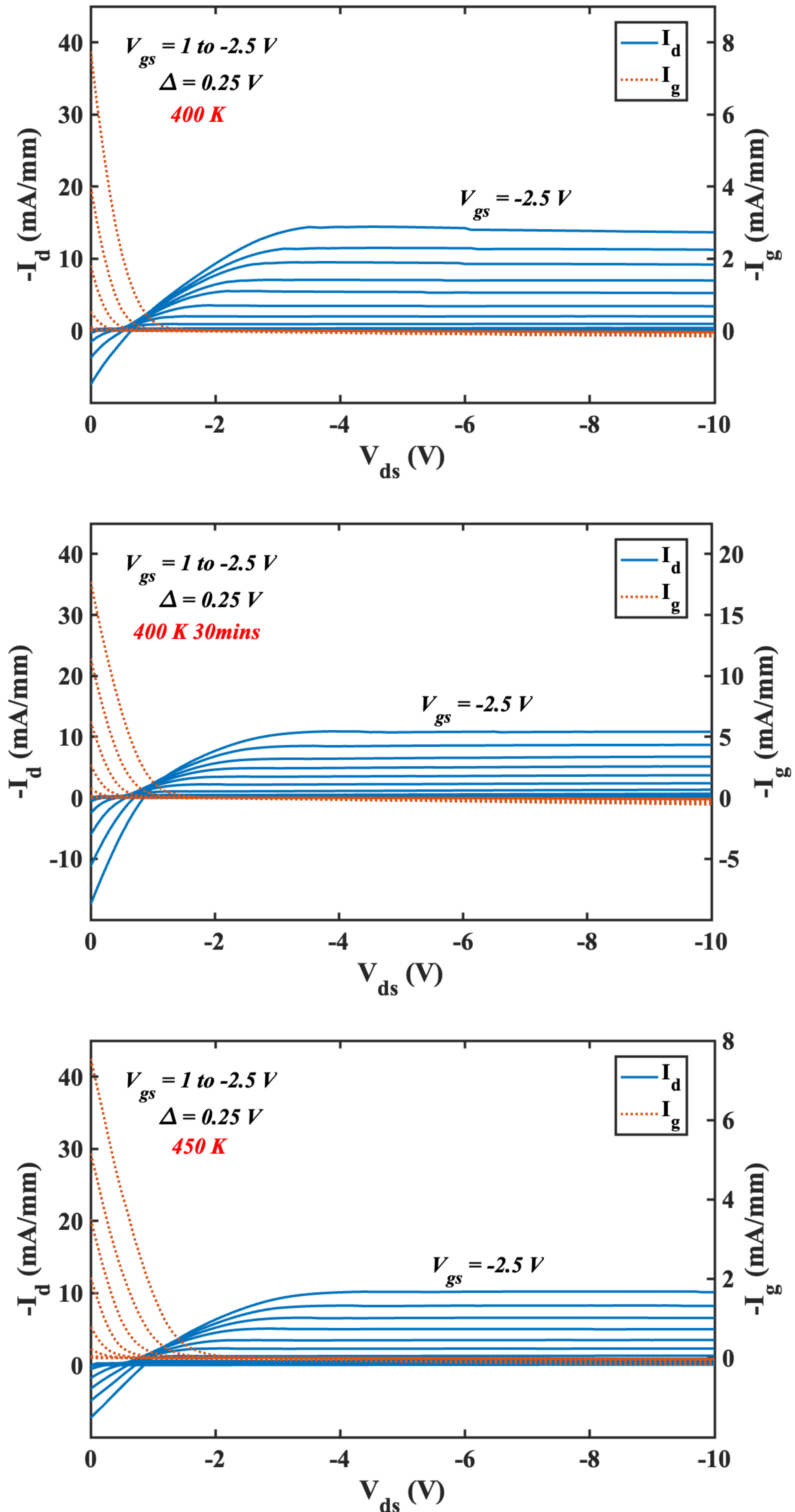


Figure 8.16: Output characteristics at 400 K, 400 K after 30 mins and 450 K.

further evidence that the temperature induced change in IV may predominantly be due to the alteration of the H-diamond/contact interfaces.

In the room temperature graph, the device cannot be turned off when the gate voltage is at 1 V. This could be attributed to the improved surface conductivity due to the oxide deposition. A similar phenomenon was observed in the previous section when comparing air adsorbates devices and devices after oxide deposition. A higher gate voltage was required to turn off the device after oxide deposition, as observed in the transfer characteristics comparison.

The gate leakage current remained at the same level, around 0.2 mA/mm, until 30 minutes after the temperature was elevated to 350 K. Subsequently, the leakage current increased to 6.05 mA/mm, which is one order of magnitude higher than the leakage before reaching this temperature. This increase occurred because the elevated measurement temperature provides carriers more energy to overcome the Schottky barrier between the Al and hydrogen-terminated diamond, allowing more current to flow through the gate.

Simultaneously, an opposite direction of current flow of 5.8 mA/mm was observed through the drain and source when the drain-source voltage was below -0.6 V, after the temperature was kept at 350 K for 30 minutes. This current increased with elevated temperature and peaked at -17.5 mA/mm after the temperature was kept at 400 K for 30 minutes, before decreasing to 7.33 mA/mm at 450 K. This current in the area where no bias was applied on the drain can be attributed to the gate leakage current. When a low bias is applied on the drain side and a comparatively high gate bias is applied, holes can be attracted to the gate and tunnel through the barrier to form a gate leakage current. As the temperature increases, carriers acquires more thermal energy, allowing more current to flow through the gate. When the leakage current reaches a certain level, 5.8 mA/mm in this study, a strong enough electric field is created on the source side. Consequently, the source is on a comparatively negative bias compared to the drain, where no or low bias is applied. As a result, holes start to flow from the drain to the source due to the bias difference, leading to the observation of opposite direction current in the output characteristics plot. This current decreases as the drain bias increases, thereby equalizing the bias difference between the drain and source.

	R_{on} ($\Omega\cdot mm$)	R_c ($\Omega\cdot mm$)	R_s ($\Omega/\square$)	R_{ch} ($\Omega\cdot mm$)	R_{Gch} ($\Omega\cdot mm$)
Room Temperature	114.5	3.63	23.44	23.44	60.36
350K	128	8.73	22.37	22.37	65.81
350K 30 minutes	133.97	10.63	21.51	21.51	69.70
400K	153.58	19.92	21.83	21.83	70.09
400K 30 minutes	166.14	21.35	21.29	21.29	80.86
450K	192.99	35.87	22.6	22.6	76.05

Table 8.5: Extracted resistance from the output characteristics plot at different temperature.

Using the sheet resistance, contact resistance extracted from the TLM measurement at different temperatures, and the on resistance from the output characteristics plot, the channel resistance and gate channel resistance can be calculated. Table 8.5 lists the calculated results of various resistances at different temperatures. The turn-on resistance increases with elevated temperature from 114.5 $\Omega \cdot mm$ to 192.99 $\Omega \cdot mm$ at 450 K, and the gate channel resistance also increases with temperature rise. This increase in gate channel resistance may be caused by the same mechanism that increases the contact resistance—the desorption of air adsorbates under the Al reducing the surface conductivity.

Figure 8.17 illustrates the transfer characteristics of the devices at different temperatures. The I_{on}/I_{off} ratio of this device at room temperature is only around 10^1. However, as discussed in the output characteristics plot, this device is not turned off when the gate voltage is 1 V. Therefore, the I_{off} value is not accurately represented in this plot. The transfer characteristics are measured when the gate voltage is between 1 V and -2.5 V. Thus, the I_{on}/I_{off} ratio is not accurately captured in this scenario. For the measurements of the device at other temperatures, as the temperature increases, both the on-drain-source current and the off-drain current decrease. Consequently, the I_{on}/I_{off} ratio remains in the order of 10^2.

The threshold voltage decreases with higher temperature. Which might caused by the thinner accumulation channel with the temperature increase. With decreased accumulation channel, the voltage required to turn off the device is lower.

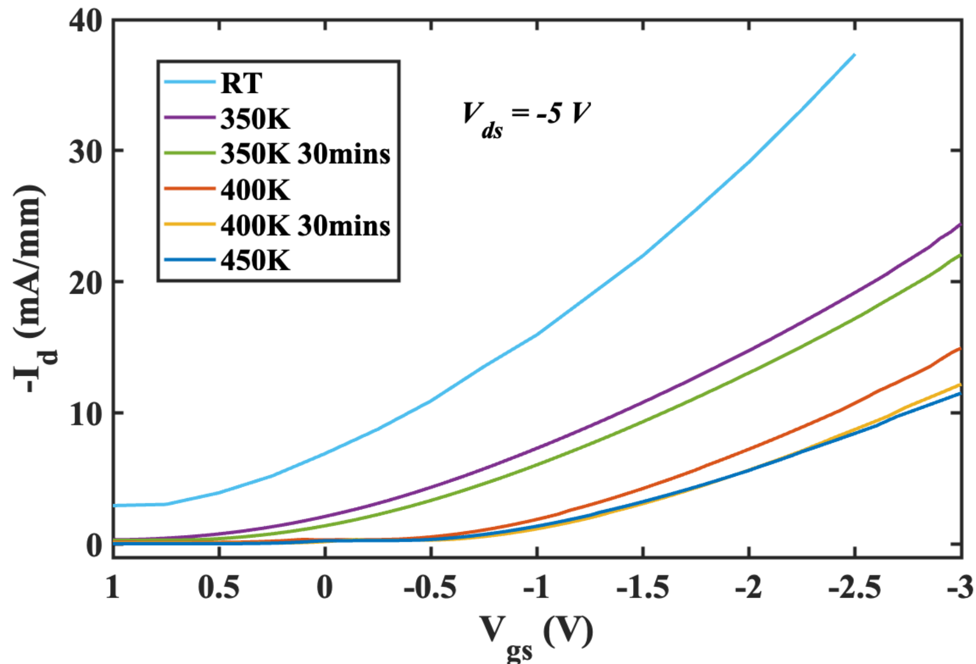


Figure 8.17: Transfer characteristics at different temperature.

Figure 8.18 plots the transconductance of the device at different temperatures. The transconduc-

tance decreases with elevating temperature from 17 mS/mm at room temperature to 6 mS/mm at 450 K. This reduction in transconductance indicates the performance degradation of the device, and the gate amplification ability is decreased. With temperature increase, carriers acquires more thermal energy to overcome the Schottky barrier between the Al and H-diamond interface, which affects the gate control over the device. Furthermore, the keep increasing contact resistance affect the transconductance too.

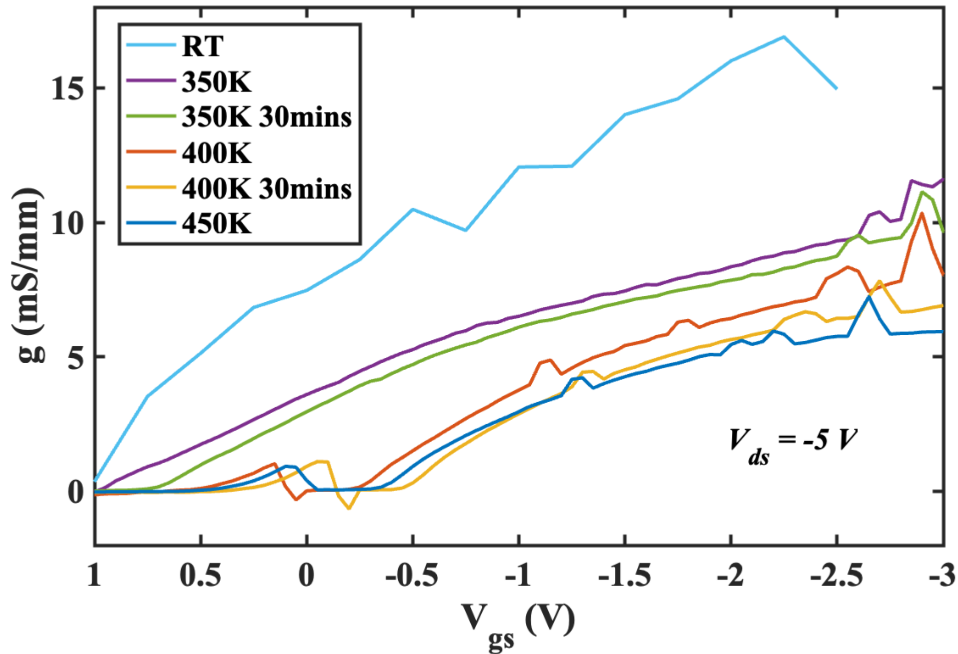


Figure 8.18: Transconductance at different temperature.

To summarise, the device's drain current decreased with elevated temperature. The increased gate channel resistance and ohmic contact resistance might be caused by the disruption of the air adsorbates under the gate and ohmic metal. The elevated temperature provides carriers more thermal energy to overcome the Schottky barrier between the Al and hydrogen-terminated diamond, thus increasing the gate leakage current. The drastically increased gate leakage current creates a comparatively negative field under the source end, which is responsible for the opposite flow direction of the drain-source current when the drain bias is low. The reduction in transconductance with elevated temperature confirms that the gate degrades under high temperatures.

8.5 Chapter Summary

This chapter examined devices fabricated with Au as a sacrificial layer to protect the surface termination. The devices were measured both with air adsorbates and following the deposition of 15 nm of thermal ALD Al_2O_3. Subsequently, high-temperature measurements were conducted between 300 K and 450 K.

To comprehend the device behaviour, TLM and VDP structures were fabricated on the same sample to extract parameters such as contact resistance, sheet resistance, carrier mobility, and carrier concentration. The VDP and TLM measurements indicated that the oxide deposition improved the surface conductivity of the hydrogen-terminated diamond. There were no significant changes observed in contact resistance before and after the oxide deposition. However, TLM measurements at different temperatures showed that the sheet resistance stabilized between 24 $k\Omega/\square$ and 21 $k\Omega/\square$. Nevertheless, the contact resistance increased drastically from 3.63 $\Omega \cdot mm$ to 35.87 $\Omega \cdot mm$ at 450 K. This increase in contact resistance might be caused by the modification of air adsorbates under the gold ohmic pad. Subsequent TLM structure measurements confirmed the drop in contact resistance to pre-high temperature measurement levels, providing further evidence for this hypothesis.

The MESFET with Al/Pt/Au as the gate metal stack was measured after fabrication and 14 days after exposure to air. A slight increase in the maximum drain current was observed, potentially due to the re-establishment of air adsorbates on the diamond surface. Then, a comparison of the device before and after the 15 nm Al_2O_3 deposition was conducted. The oxide deposition doubled the maximum drain current and reduced the gate leakage current by two orders of magnitude by providing more carriers. However, more study required to investigate the lower gate current leakage after the oxide deposition.

Subsequent high-temperature measurements illustrated that the device started to degrade once the temperature reached 350 K. The decrease in drain current, transconductance, gate channel resistance, and increase in gate leakage current imply that the gate loses its amplification ability with elevated temperature.

Chapter 9

Accumulation Channel H-Diamond MOSFETs

In the previous chapter, a H-diamond MESFETs was presented. The results demonstrated that ALD Al_2O_3 improved the surface conductivity of hydrogen-terminated diamond and enhanced thermal stability. Although the oxide effectively reduced the on-state gate leakage, the off-state source-drain current increased, thereby affecting the I_{on}/I_{off} ratio by two orders of magnitude. To mitigate the off-state source-drain current, an accumulation (enhancement) channel of MOSFET was fabricated and will be discussed in this chapter.

The currently reported normally-off hydrogen-terminated diamond MOSFETs exhibit some limitations in terms of the fabrication process or device properties. Devices employing gate oxides such as HfO_2 and Al_2O_3 as insulator layers typically show maximum drain currents below 40 mA/mm [147], [148]. Another strategy involves partially oxide-terminating the exposed diamond surface in the drain-source channel or doping the channel with nitrogen to induce impurities and create an energy barrier between the source and drain [110], [149]. However, the reported drain currents range between 5 to 20 mA/mm. Yu et al. [150] reported normally-off diamond devices with decent drain currents over 300 mA/mm and an I_{on}/I_{off} ratio over 10^7 by using Si-terminated drain-source gaps and boron-doped source and drain. By using h-BN as a dielectric material, Y. Sasama et al. [151] achieved normally-off hydrogen-terminated diamond devices with a maximum drain current around 200 mA/mm, high carrier mobility over 600 $cm^2V^{-1}s^{-1}$, and an I_{on}/I_{off} ratio of 10^8. Instead of using silicon termination or h-BN as dielectric materials, in this work, PVD Al_2O_3 was investigated and used as dielectric material on clean H-diamond surface to fabricate normally-off hydrogen-terminated diamond MOSFETs.

9.1 PVD Al_2O_3 deposition

As discussed previously, the conductivity of air-exposed H-diamond might be attributed to the presence of air adsorbates, which provide a hole accumulation layer near the diamond surface [43]. By removing the air adsorbates from the H-diamond, the surface conductivity also vanishes [43]. In this case, it is assumed that the hydrogen termination provides an unpinned Fermi level in the H-diamond. The Fermi pinning effect denotes the phenomenon wherein the Fermi level within a semiconductor material is fixed or "pinned" at a specific energy level near the interface between two materials. This can arise from defects or chemical bonding that trap charge carriers, thereby affecting altering the Fermi energy level near the interface [30], [152].

With the support of these theories, a normally-off device can be achieved by creating a hydrogen-terminated surface without any air adsorbates between the source and drain contacts. This cleaned surface (the surface without air adsorbates) creates an energy barrier between the source and drain contacts. However, since the hydrogen termination provides an unpinned Fermi level, once a gate bias is applied, the energy barrier between the source and drain will be decreased, thereby attracting carriers under the source and drain contacts to accumulate under the gate area and forming an accumulation channel to allow current flow between the drain and source. Thus, this normally-off device is also referred to as an accumulation channel H-diamond MOSFET. Figure 9.1 illustrates the energy band diagram.

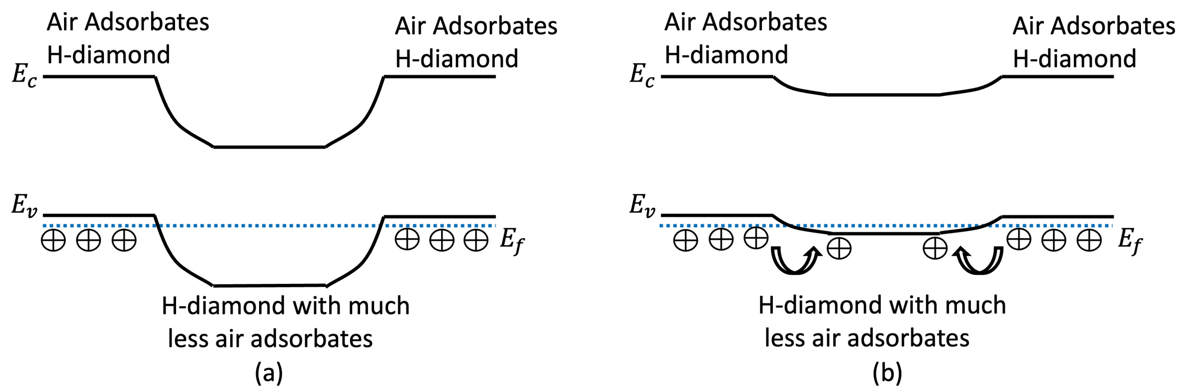


Figure 9.1: Energy diagram between the gate channel and source drain area.
(a) Band diagram without bias applied on the gate. (b) When a bias applied on the gate.

Oxides like V_2O_5 and Mo_2O_3 were explored in this group. Both oxides, with LUMO below the maximum valence band of H-diamond, were discovered to improve the surface conductivity by acting as an acceptors. ALD Al_2O_3 was discussed in the previous chapter, where an improvement of the surface conductivity was discovered. It is assumed that some defects in the ALD Al_2O_3 function as additional acceptors, thereby enhancing the surface conductivity of H-diamond. To achieve the normally-off device discussed above, an oxide that neither behaves as a surface acceptor nor damages the surface termination is required.

A 3 *mm* × 3 *mm* diamond sample was cleaned and hydrogen terminated in Australia. The sheet resistance was measured using a Hall Kit by contacting the surface with four probes until the sheet resistance stabilized. Then, silver dag was applied to the four corners of the sample to provide better contact during measurements. The measured sheet resistance after applying the silver dag was around 31.24 kΩ/□.

Subsequently, the sample was subjected to physical vapor deposition in PLASSYS 5, an one hour 300 °C annealing was performed when the vacuum level of the chamber reached to 1×10^{-7} mbar. This step is designed to remove most of the air adsorbates on the hydrogen terminated diamond surface[43]. Then 15 nm of Al_2O_3 was deposited on the sample surface after the chamber temperature back to room temperature. The sheet resistance was measured again using the Hall Kit, with four probes penetrating through the silver dag at the four corners of the sample. The measured sheet resistance increased to 867.6 kΩ/□ after the deposition.

To ensure that the oxide did not damage the hydrogen termination, the sample was rinsed in 10:1 buffered oxide etch (BOE) for 5 minutes. The hydrofluoric acid (HF) in the etch solution removed the oxide. A subsequent Hall Kit measurement conducted after oxide removal showed that the sheet resistance dropped back to 54.61 kΩ/□.

The experiments conducted here verified that E-beam vapor deposition of Al_2O_3 does not provide a lowest unoccupied molecular orbit to act as electron acceptors, thus improving the sheet resistance while suppressing the surface conductivity of hydrogen-terminated diamond. After removing the oxide, the recovery of the sheet resistance indicated that the increase in sheet resistance was not due to damaged hydrogen termination.

	Air Expose	Al_2O_3 deposition	After BOE etch
R_s ($k\Omega/\square$)	31.24	867.6	54.61

Table 9.1: Hall Kit sheet resistance measurement of the sample (1) in air (2) after 1 hour 300 °C annealing and 15 nm of Al_2O_3 deposition (3)Al_2O_3 removed by 5 minutes BOE wet etch.

The suppression of surface conductivity of hydrogen-terminated diamond after Al_2O_3 deposition can be explained as follows. Firstly, the Al_2O_3 may act as a passivation layer, preventing the hydrogen termination from contacting air and forming air adsorbates, thereby reducing the sheet resistance. During the annealing process, most of the air adsorbates could be removed theoretically. The oxide deposition could then isolate the surface from the air to form an adsorbates layer. After removing the oxide, air adsorbates re-established upon exposure to air. A more detailed study is needed to understand this phenomenon better. Gated VDP structures fabrication with different annealing temperature before the oxide deposition can be used to confirm the air-adsorbates removal. In addition, XPS can be used to detect the energy band bending and oxide quality.

9.2 MOSFETs measurement

The fabrication process of these MOSFETs has been detailed in Chapter 4, and the complete fabrication flow can be seen in Figure 4.26. A 4.5 mm×4.5 mm single polished diamond sample was hydrogen-terminated in Australia. The sheet resistance of the sample before fabrication was measured as 50 kΩ/□ which is higher than the desirable resistance ($\approx$ 10 $k\Omega/\square$) used for H-diamond device fabrication in most of those reported literature. Figure 9.2 illustrates the cross-section of the sample in the final steps. After depositing the ohmic pads and before the PVD Al_2O_3 deposition, a 350 °C in-situ annealing process was conducted to desorb air adsorbates from the diamond surface between the the source and drain contacts. It has been reported that air adsorbates on H-diamond can be fully removed at 400 °C[43], based on the experiment discussed in the previous section where a surface conductivity drop and recover on H-diamond was confirmed after 300 °C annealing, 350 °C was chosen as a safe temperature to remove air adsorbates on the H-diamond sample. Following deposition of 35 nm of PVD Al_2O_3 was conducted to serve as the dielectric material between the gate and the H-diamond. To prevent shorting between the gate and source-drain contacts, a 15 nm layer of ALD Al_2O_3 was deposited on top of the PVD oxide to cover all edge walls.

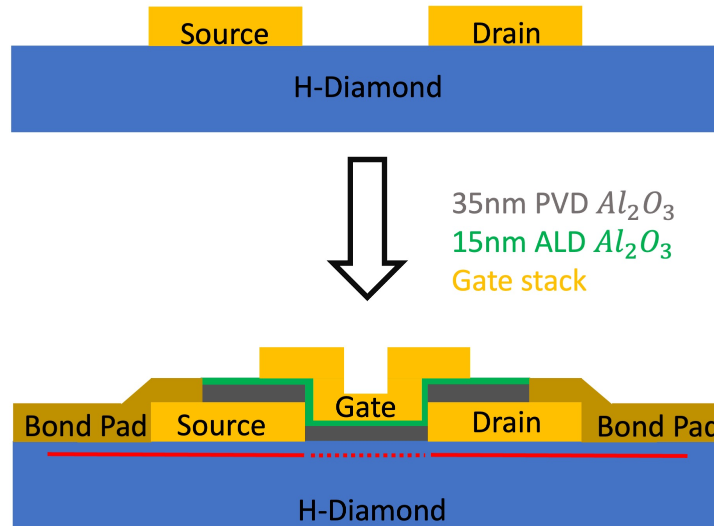


Figure 9.2: MOSFETs cross section structure.
The solid red line represents the 2DHG. The dotted red line represents the reduced carrier density 2DHG due to the 350 °C desorption process.

Figure 9.3 illustrates the output characteristics of MOSFETs with a gate/channel length of 1 μm and a width of 25 μm. The gate voltage ranges from 0 to -14 V, with a maximum drain current of 110 mA/mm recorded at -14 V gate voltage. Notably, (and despite the initial higher material R_{sh} values) this drain current surpasses that achieved by MESFETs which had a shorter gate length (2 μm) discussed in the preceding chapter. Previous studies report the highest drain current maximum, ranging between 110 mA/mm and 150 mA/mm, for MOSFETs employing oxide as

an insulator [153], [154]. Comparatively, the drain current attained in this study is within this range.

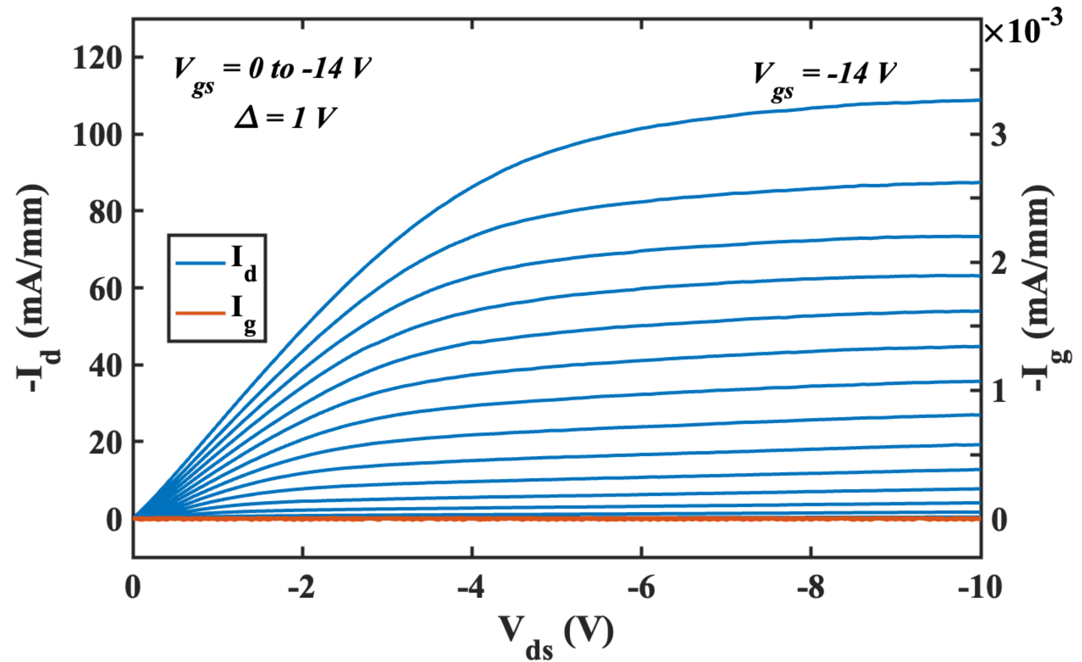


Figure 9.3: 25 μm wide, 3 μm gate length AC-MOSFETs output characteristics. V_{gs} sweep from 0 to -14 V with step of 1 V.

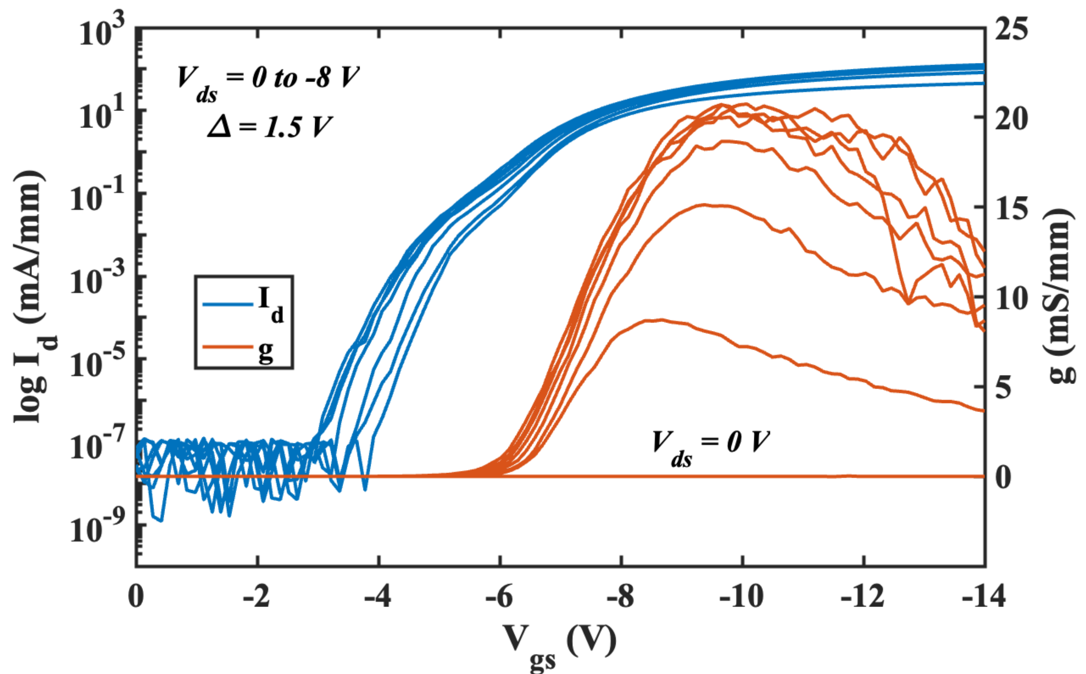


Figure 9.4: 25 μm wide, 3 μm gate length AC-MOSFETs transfer characteristics. V_{ds} sweep from 0 to -8 V with step of 1.5 V.

The on resistance, when the gate voltage is -14 V, is determined as 42 Ω·mm, marking a re-

duction of over fifty percent from the resistance observed in MESFET devices. Furthermore, examination of the output graph reveals negligible gate leakage current across the inspected range, estimated at approximately 10^{-7} mA/mm.

The transfer characteristics are depicted in Figure 9.4. The drain voltage was swept from 0 to -8 V, while the gate voltage stepped from 0 to -14 V in increments of 1.5 V. Notably, the I_{on}/I_{off} ratio exceeds 10^9, marking a three-order-of-magnitude enhancement compared to MESFET devices discussed in the preceding chapter, and surpassing by three orders of magnitude the reported MOSFETs with Al_2O_3 as the insulator, achieving a drain current of 135 mA/mm [154]. This notably higher ratio indicates superior switching behaviour, lower leakage current, and consequently, a better signal-to-noise ratio.

At the noise floor level, the threshold voltage is extracted as -4 V. At a set off-sate drain current 1 $\mu A/mm$ was extracted as -5 V, significantly surpasses the reported 1.8 V [154] around 7 V.

A depletion region calculation of the V_{th} is carried as follows, parameters used for the calculation are, metal work function φ_m = 4.33 eV, diamond surface work function φ_s = 1.45 eV, t_{ox} = 50 nm, dielectric constant κ_{ox} = 9, carriers concentration $N_a = 2 \times 10^{12}\ cm^{-2}$, intrinsic H-diamond carrier concentration $n_i = 10^{11}\ cm^{-2}$ [151], permittivity of free space $\varepsilon_0 = 8.85 \times 10^{-12}$ F/m. Here an ideal H-diamond surface without any adsorbates is assumed, with this ideal surface, Fermi level is assumed close to the middle of the band gap of the diamond. Considering the band gap of the diamond is 5.5 eV, the ideal Fermi level suppose to be 2.75 eV below the conduction band minimum. Due to the hydrogen termination induced negative electron affinity which is 1.3 eV below the conduction band minimum. Thus, a 1.45 eV of work function of H-diamond surface is used for the calculation.

In V_{fb} calculation, a perfect interface without trapped and fixed charges, where Q_f is assumed to be 0,

$$V_{fb} = \varphi_{ms} - \frac{Q_f}{C_{ox}} = \varphi_m - \varphi_{ms} = 2.88\ eV \tag{9.1}$$

In φ_f calculation room temperature 300 K is applied,

$$\varphi_f = \frac{kT}{q} ln(\frac{N_a}{n_i}) = 0.07\ eV \tag{9.2}$$

where K is Boltzmann constant 1.38×10^{-23} J/K, T is the absolute temperature and q is elementary charge 1.6×10^{-19} C, capacitance under the gate metal is calculated as below,

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} = \frac{\kappa_{ox}\varepsilon_0}{t_{ox}} = 1.59 \times 10^{-7}\ F/cm^2 \tag{9.3}$$

the depletion charge density is calculated as below,

$$Q_d = q \times N_a = 3.2 \times 10^{-7}\, C/cm^{-2} \tag{9.4}$$

Finally, the threshold voltage can be calculated as,

$$V_{th} = V_{fb} + 2\varphi_f + \frac{Q_d}{C_{ox}} = 2.88 + 0.14 + 2.01 = 5.03\, V \tag{9.5}$$

This calculated threshold voltage aligns well with the extracted threshold voltage (-5 V) with set-off current in the order of 10^{-3} mA/mm. And it explains the removal of the air-adsorbates on the H-diamond surface contributes to this large threshold voltage.

The transconductance extracted from this device measures approximately 22 mS/mm, a value within the range reported for hydrogen-terminated diamond devices designed for normally off operation. Notably, as this device represents the first iteration utilizing this fabrication method, numerous parameters remain open for optimization, potentially enhancing transconductance. For instance, adjusting the thickness of the oxide layer, as demonstrated in Liu et al.'s study [154], where a thinner oxide layer (100 nm) substantially increased transconductance (1410 mS/mm). Additionally, reducing the gate length could enhance gate control and subsequently improve transconductance. Furthermore, optimizing oxide deposition to mitigate interface traps and defects could enhance carrier mobility and consequently increase transconductance.

Ungated TLM structures were fabricated on the sample and measured using the probe station. The highest current recorded from the TLM structure was 1.6×10^{-3} mA/mm. This remarkably low current confirms the low surface conductivity post-PVD Al_2O_3 deposition, indicating a scarcity of carriers in the channel available for conduction when a bias is applied across the TLM ohmic pad. As per design this is most likely attributed to the desorption of air adsorbates during the 350 °C annealing process [43], coupled with the presence of the Al_2O_3 passivation layer that suppresses the 2DHG formation.

Conversely, in the present MOSFET devices, a hydrogen-terminated surface with minimal transfer doping is achieved between the source and drain channels. In the absence of gate bias, there is little active hole population in the channel and minimal carriers traverse between the source and drain, rendering the device normally off. Upon applying a negative gate bias, holes are drawn to the surface of the hydrogen-terminated diamond, forming a hole accumulation layer. This layer establishes a channel between the drain and source. Consequently, when a bias is applied to the drain terminal, current flows from drain to source, with the energy barrier between the hydrogen-terminated diamond and Al_2O_3 preventing carriers from flowing to the gate.

As discussed in at the start of this section, hydrogen termination provides unpinned Fermi level

on the diamond surface. In this investigation, the hydrogen termination on the diamond surface and the interface between the hydrogen termination and PVD Al_2O_3 both provide unpinned Fermi levels. The presence of these unpinned Fermi levels facilitates hole accumulation. The high drain current is indirect evidence of this theory. And more investigation such as XPS and KPFM which can measure the band bending on the interface and work function can be done to confirm.

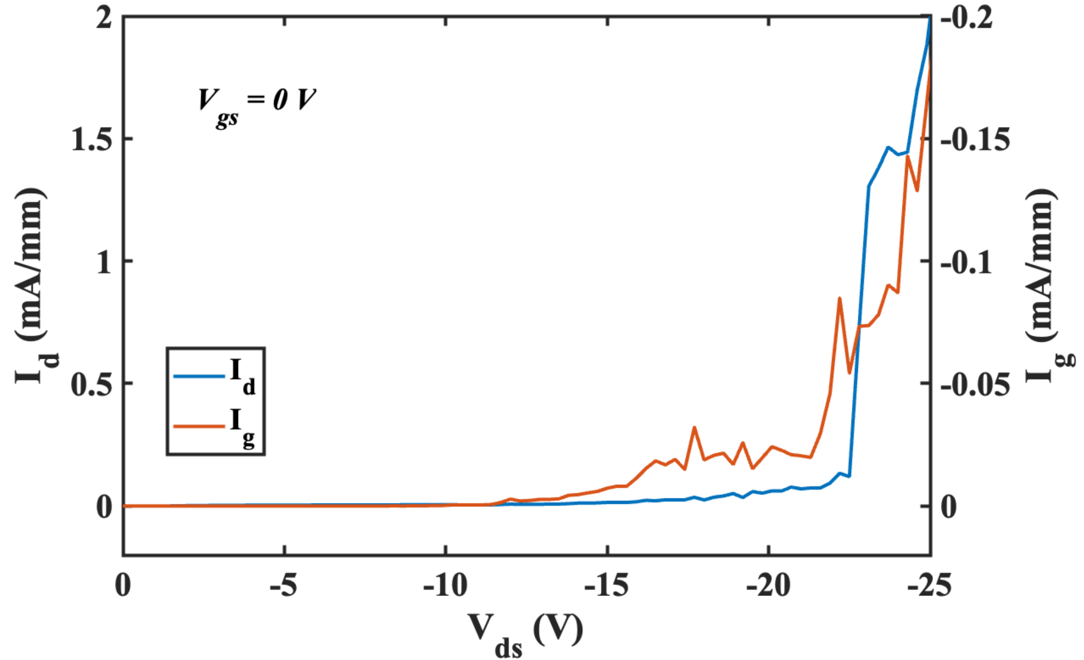


Figure 9.5: MOSFETs off-state breakdown measurement.

When the device is in the off state ($V_g = 0$ V), with more negative voltage applied to the drain terminal, carriers on the drain side accumulate enough energy to tunnel through the energy barrier between the gate channel and the source-drain side, potentially leading to off-state breakdown. Figure 9.5 illustrates the off-state breakdown measurement of this device, revealing that breakdown occurs at approximately 22.5 V drain-source voltage. Notably, this breakdown voltage is lower than the 80 V achieved in MESFET devices. This discrepancy is most certainly attributed to the architecture of these MOSFET devices, wherein the gate contact extends over the source and drain terminals as separated by only the ALD Al_2O_3 layer.

As discussed earlier in this section, the deposition of ALD Al_2O_3 aims to prevent gate shorting with the source and drain, with only around 15 nm of Al_2O_3 separating the edge wall of the source-drain contact and the gate. This thin oxide layer may prove insufficient, with the barrier potentially too thin to prevent high conduction when drain voltage reaches high levels. Consequently, optimizing the device architecture or increasing the thickness of the oxide layer may enhance the off-state breakdown voltage.

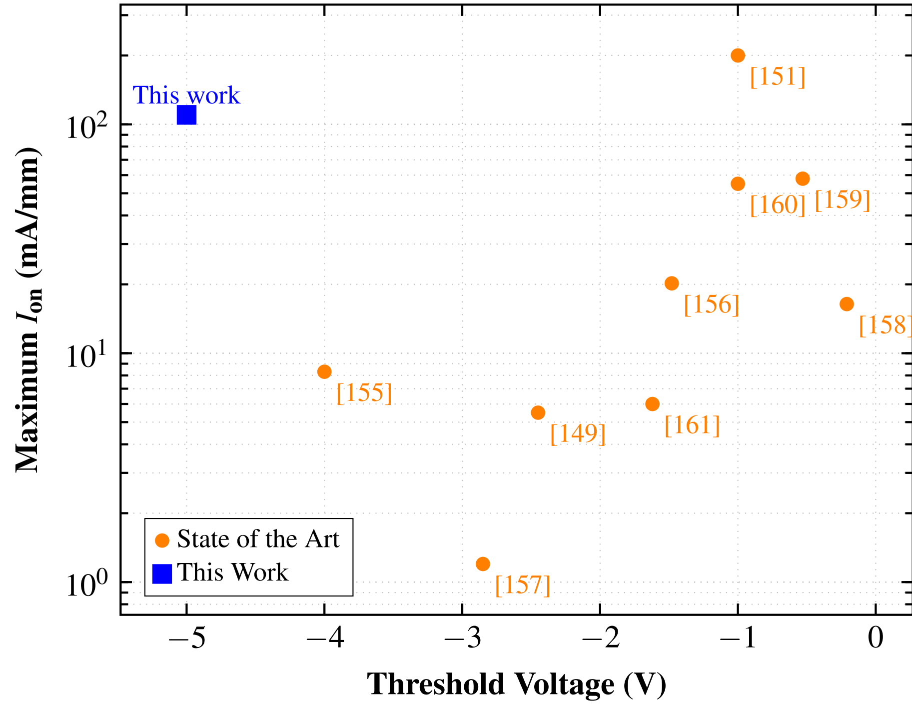


Figure 9.6: Benchmarks of threshold voltage and drain current maximum of the reported state-of-the-art normally-off hydrogen termination diamond MOSFETs.

9.3 Split CV measurement and mobility extraction

By measuring the capacitance between the gate and channel and integrating the CV curves, the carrier density can be extracted. With the calculated carrier density, the effective carrier mobility can be deduced using the following equation:

$$\mu_{eff} = \frac{1}{R_{sh} \cdot n \cdot q} \tag{9.6}$$

Here, R_{sh} represents the channel sheet resistance, n stands for the 2D carrier density, and q is the elementary charge constant [162], [163].

Split CV was conducted in this study to measure the gate-channel capacitance (C_{gc}). By grounding the drain and source terminals, a voltage range of -13 V to 1 V was applied to the gate terminal, while the capacitance was measured from the source terminal. Figure 9.7 illustrates the capacitance against voltage plot.

However, as depicted in the cross-section of the device in Figure 9.8, the overall capacitance under the gate terminal encompasses three components: the gate-to-source capacitor (C_{gs}), the gate-to-drain capacitor (C_{gd}), and the gate-to-channel capacitor (C_{gc}). C_{gs1} and C_{gd1} are the capacitors between the gate edges and the source and drain edges with 15 nm of ALD Al_2O_3 in the middle. It is necessary to deduct the parasitic capacitance between the gate and drain contacts,

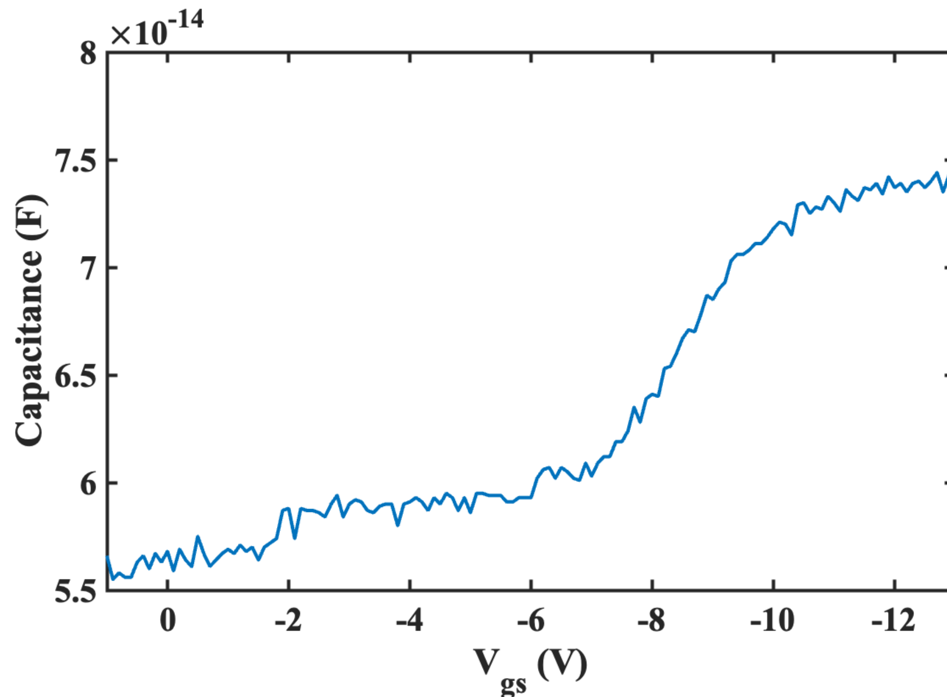


Figure 9.7: MOSFETs CV measurement at 1 MHz.

as well as between the gate and source contacts, from the overall capacitance to extract the effective device capacitance. In the off-state, the measured capacitance should be attributed to the total parasitic capacitance between the gate and the ohmic contacts, from figure 9.7 suggesting a range for the parasitic capacitance between 5.5×10^{-14} F and 5.9×10^{-14} F.

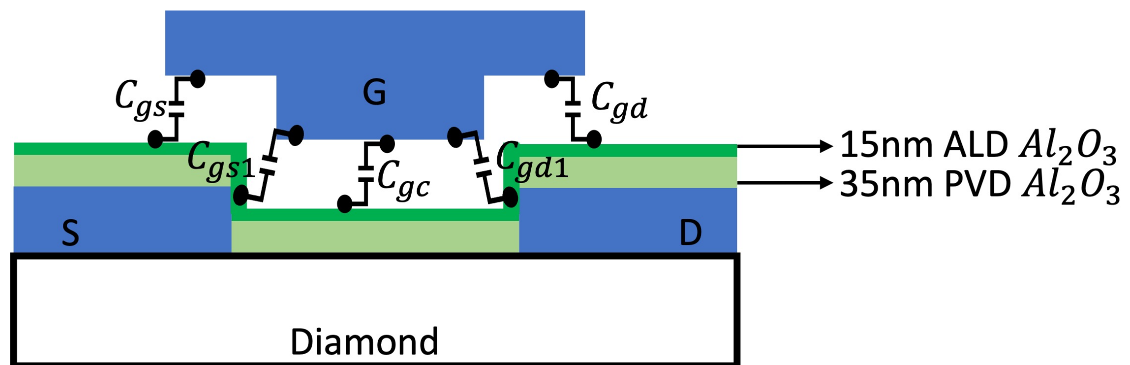


Figure 9.8: The capacitor distribution in the AC-MOSFETs.

To estimate the parasitic capacitance through calculation, several assumptions were made. First, neglecting the parasitic capacitances C_{gs1} and C_{gd1}. Compared to the 1 μm overlapping length between C_{gs} and C_{gd}, the overlapping length between the gate edge and the source (C_{gs1}) and drain (C_{gd1}) edges is only around 25 nm. This makes these two parasitic capacitors negligible. Assuming uniform oxide deposition, with a total thickness (d) of 50nm for two layers of Al_2O_3, and considering a gate extending 1μm over the source and drain sides, with a channel width

of 25μm, the total area (A) of the parasitic capacitor is 50 μm^2. A dielectric constant (κ) of 6.6 was utilized, selected based on the 15nm of low temperature plasma enhanced ALD Al_2O_3 and 35nm of PVD Al_2O_3. In addition, Figure 9.7 illustrates a parasitic capacitance at the level of 5.9×10^{-14} F before the V_{gs} reach the threshold voltage(-5 V).According to this parasitic capacitance extracted from the C-V measurement and the permittivity of free space ($\varepsilon_0 = 8.85 \times 10^{-12}$ F/m), a dielectric constant around 6.6 was calculated. A typical dielectric constant for Al_2O_3 is between 9 to 10. However the ALD grow Al_2O_3 dielectric has been measured as low as 7.1 when the growth temperature is around 100°C[164]. The low chamber temperature (100°C) and plasma-enhanced ALD process applied in this work could induce a low dielectric constant Al_2O_3 due to increased defects [165]. Moreover, the presence of pinholes and defects in the bottom layer of PVD Al_2O_3 might contribute to a lower dielectric constant. However, this aspect requires further investigation for verification.

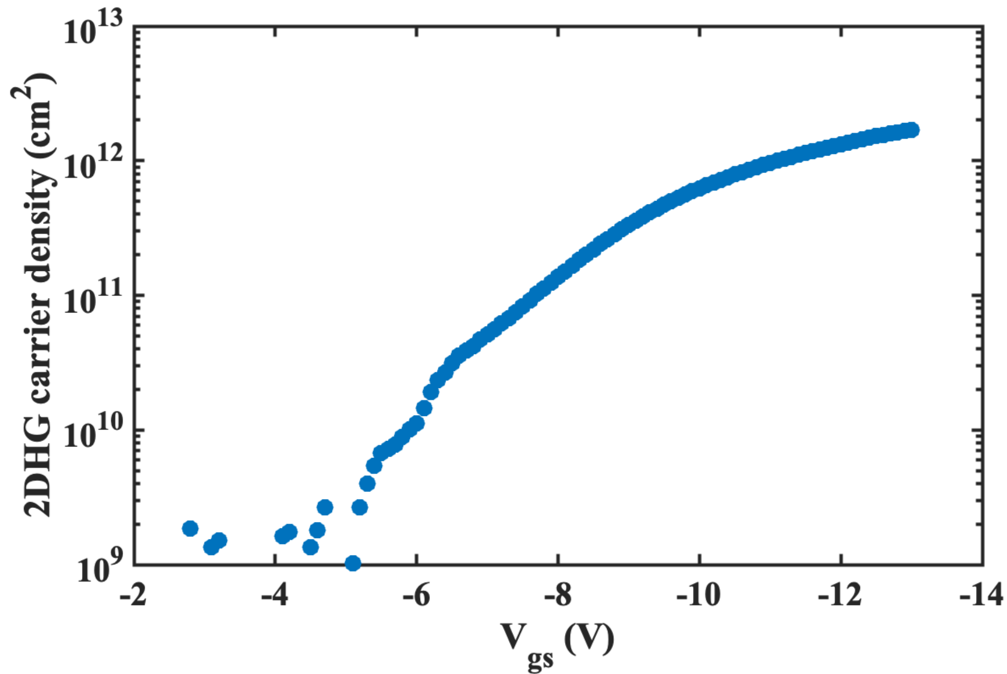


Figure 9.9: Carrier density versus gate voltage in logarithmic scale.

With the measured capacitance and estimated parasitic capacitance, the effective capacitance (C_{eff}) can be calculated. By integrating the area between the effective capacitance, the charge density (Q_i) can be determined:

$$Q_i = \int C_{eff} d(V_{gs}) \tag{9.7}$$

The charge density thus obtained can be translated into carrier density when divided by the elementary charge q. After normalization, the carrier density against gate voltage is plotted in Figure 9.9. Before the gate voltage reaches -5 V, a small number of carriers on the order of 2×10^9 cm^2 are observed, possibly originating from residual air adsorbates on the hydrogen-

terminated diamond surface or the noise floor of the measurement. As reported by Maier et al., complete desorption of air adsorbates on hydrogen-terminated diamond occurred at 400 °C under vacuum conditions [43]. Therefore, the 350 °C annealing temperature utilized in this study might have left some air adsorbate residue on the surface, contributing to the low carrier concentration below the threshold voltage. As the gate voltage increases, the carrier density reaches the accumulation area after -10 V, consistent with the CV measurement results.

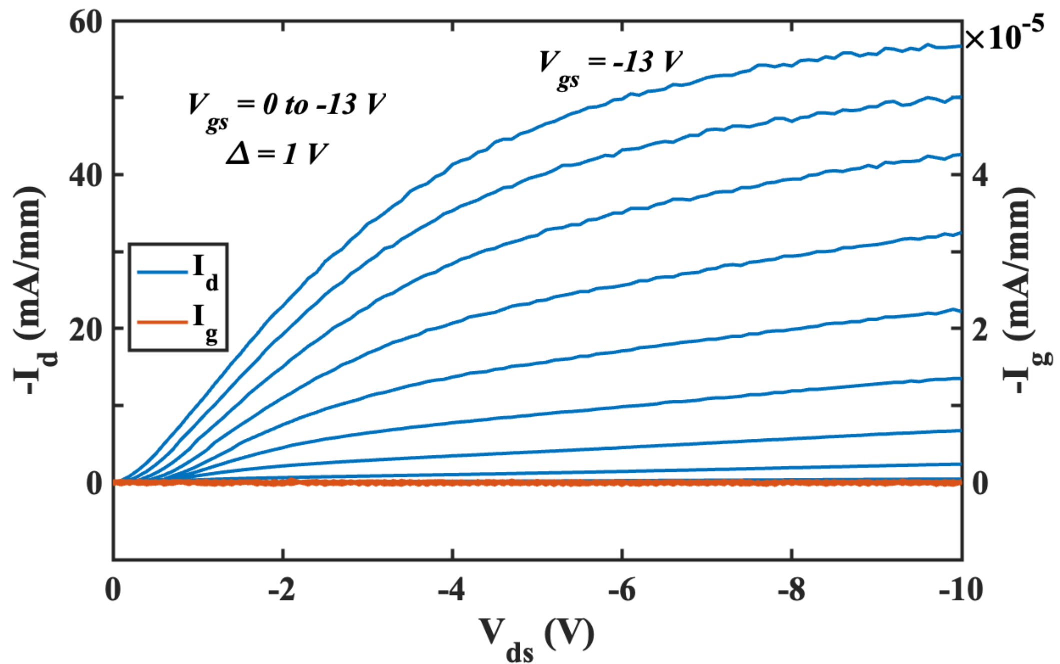


Figure 9.10: 25 μm wide, 1 μm gate length AC-MOSFET Output characteristics.

To extract the carrier mobility, the equation 9.6 mentioned at the beginning of this section should be employed. Output characteristics were conducted to derive the turn-on resistance (R_{on}). Figure 9.10 illustrates the output characteristics, with the maximum drain current recorded as 58 mA/mm, lower than the device discussed previously, possibly due to uneven termination and oxide deposition. The linear region is selected at V_{ds} equal to -2 V, and with increasing gate voltage, turn-on resistance is calculated using I_{ds} and V_{ds}.

Transfer characteristics are also depicted in Figure 9.11. The I_{on}/I_{off} ratio is on the order of 10^9, with maximum transconductance extracted as 17 mS/mm. The threshold voltage falls between -4 V and -5 V. All parameters from the transfer characteristics are consistent with the previously demonstrated device.

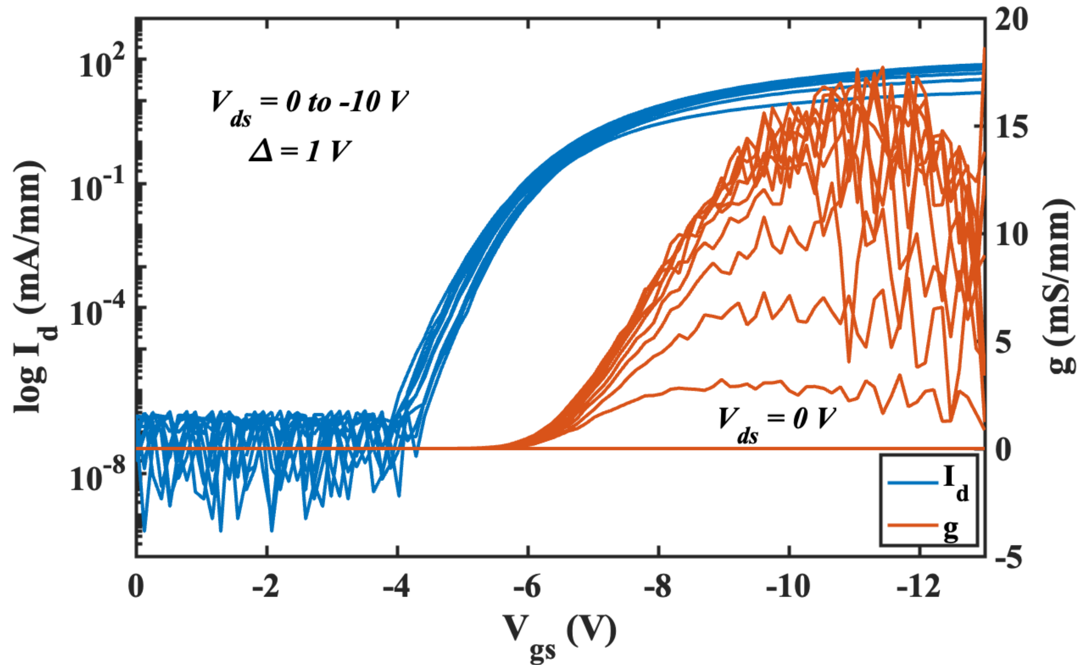


Figure 9.11: 25 μm wide, 1 μm gate length AC-MOSFET Transfer characteristics.

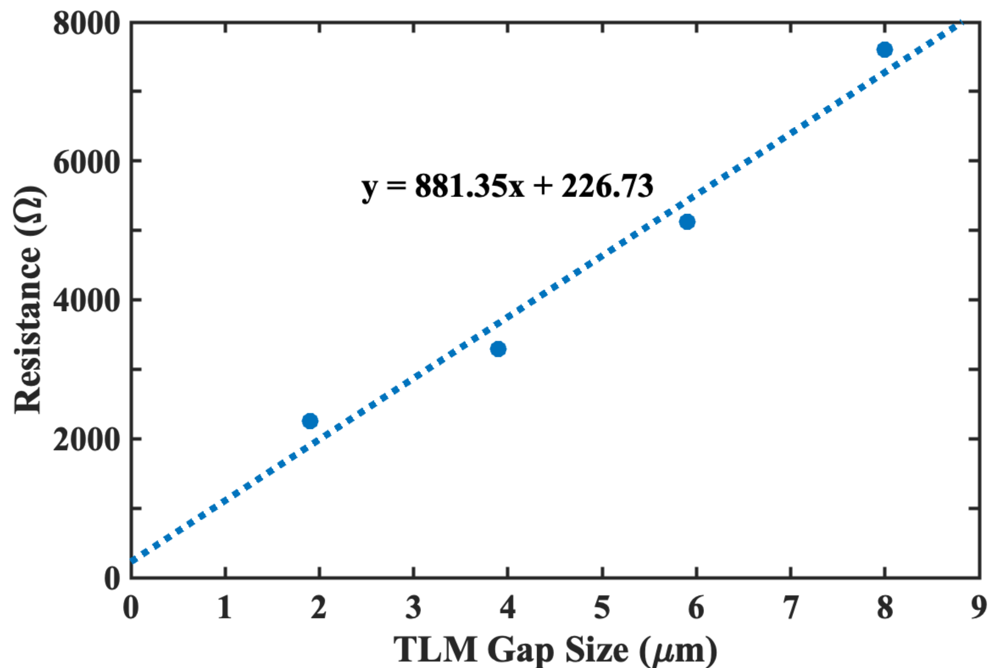


Figure 9.12: TLM measurement results after Al_2O_3 etched off.

In the final test for this device, TLM measurements were conducted to extract the contact resistance, following the calculation of turn-on resistance from the output characteristics. Due to the scarcity of holes in the channel area resulting from the annealing process, TLM measurements could only be performed after removing the oxide layer and allowing air adsorbates re-establish, forming a hole accumulation layer on the hydrogen-terminated diamond surface. A 10-minute

rinse in 1:10 buffered oxide etch was carried out to completely remove the oxide from the sample surface, ensuring no residual oxide remained. TLM measurements were then conducted post-etching. Figure 9.12 illustrates the TLM measurement results, with the intercept of the plot calculated as 226.73, resulting in a contact resistance of 11.3 $\Omega \cdot mm$.

Though this value exceeds the reported contact resistance formed between hydrogen-terminated diamond and Pd in Chapter 7, it's important to consider the difference in sheet resistance between this sample (50 k$\Omega/\square$) and the sample used in Chapter 7 (8.6 k$\Omega/\square$). The higher contact resistance may stem from this disparity in sheet resistance. Given that the FET source and gate contact width is 25 μm, the contact resistance can be converted to 453.46 Ω. It's assumed that the contact resistance measured here remains consistent when the surface is covered with Al_2O_3. Consequently, the total resistance between the two ohmic contact pads includes the resistance of the channel and two contact resistances resulting from the metal-substrate contact. As the area under the metal was protected throughout the measurement and fabrication process, a constant contact resistance with or without the oxide layer is assumed.

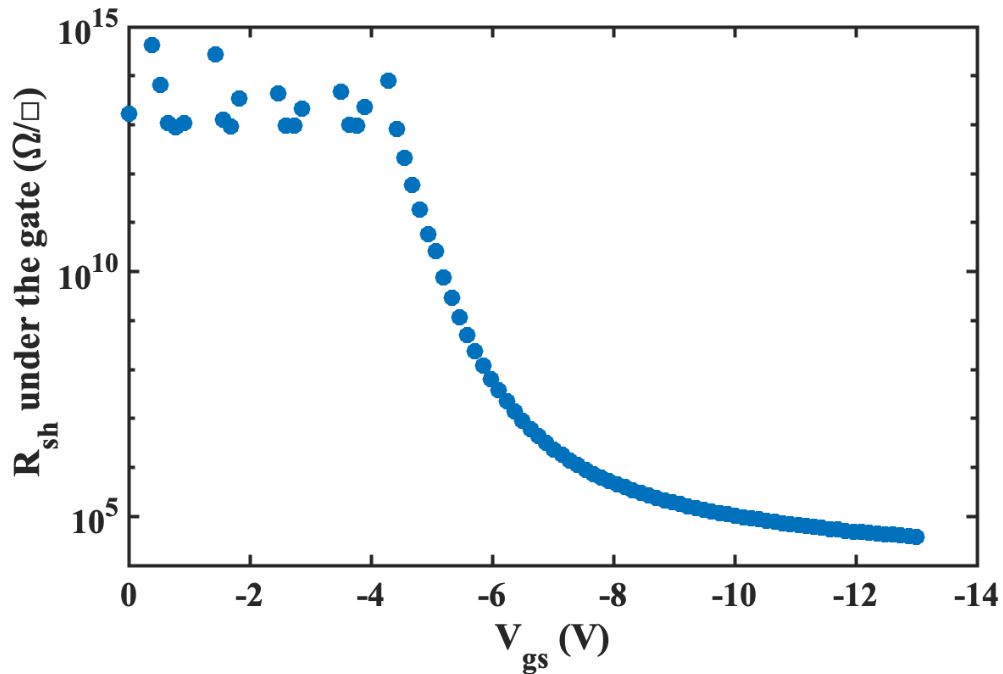


Figure 9.13: Sheet resistance versus gate source voltage.

With the turn-on resistance from the output characteristics and contact resistance from the TLM measurement, the resistance in the channel can be calculated using the following equation:

$$R_{channel} = R_{on} - 2R_c \tag{9.8}$$

Then, the sheet resistance can be determined using the equation:

$$R_s = \frac{R_{channel}}{W \times L} \tag{9.9}$$

where L and W represent the length and width of the gate channel, respectively. Figure 9.13 illustrates the extracted sheet resistance versus gate voltage. With the calculated R_s, carrier density n, and elementary constant q, the mobility can be computed using equation 9.6.

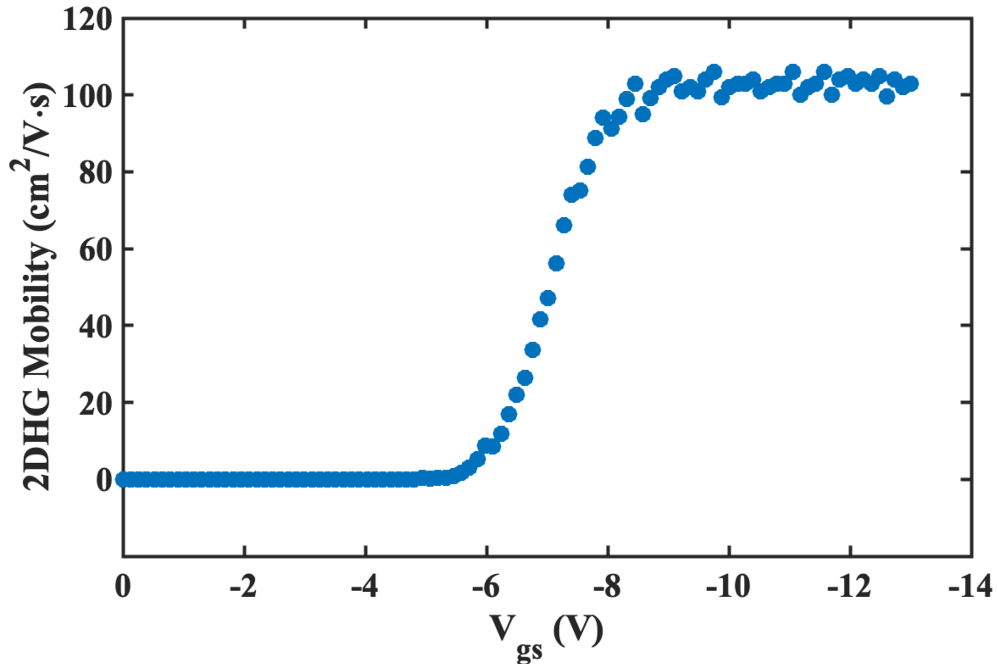


Figure 9.14: Mobility versus gate source voltage.

Figure 9.14 illustrates the calculated two-dimensional hole gas (2DHG) mobility under different gate biases. For lower gate bias ($\leq 6\,V$), the mobility is observed to be very close to 0, attributed to the very high R_{sh} in the channel when the device is in its off-state (Figure 9.11). As the gate voltage increases, holes from the adjacent source and drain 2DHG areas are attracted to the gate area, forming a hole accumulation region under the gate channel. At approximately -5V, which corresponds to the threshold voltage extracted from the transfer characteristics plot, the channel forms and expands with the increasing gate voltage. When the gate voltage exceeds -8 V, the mobility reaches saturation due to increased scattering. With a carrier concentration of around $2 \times 10^{12}\ cm^2$, the maximum mobility extracted from this device is approximately 105 $cm^2/V \cdot s$. This mobility is not as high as the values reported by Sasama et al. [151]. However, considering that the annealing temperature (350 °C) is not optimal for removing air-adsorbates, increasing the annealing temperature to 400 °C could result in a hydrogenated diamond surface with fewer surface defects. With a hydrogenated diamond surface exhibiting fewer surface defects, a higher mobility could, in theory, can be achieved.

In this section, the dielectric constant assumed for the calculation is 6.6. This choice is supported by the fact that "thin" ALD Al_2O_3 films (less than 35 nm) have been reported to exhibit a dielectric constant around 7. Additionally, the PVD oxide layer likely contains significant defects, which can further reduce the dielectric constant. The lowest parasitic capacitance observed, above 5.5×10^{-14} F as extracted from Figure 9.7, suggests a minimum dielectric constant of approximately 6.3. On the other hand, the maximum possible parasitic capacitance is below 6×10^{-14} F, implying a dielectric constant around 6.7.

If the dielectric constant were to vary within this range, from 6.3 to 6.7, the carrier mobility would consequently range from 75 $cm^2/V \cdot s$ to 140 $cm^2/V \cdot s$. This sensitivity underscores the importance of accurately determining the dielectric constant, as it significantly influences the calculated carrier mobility.

However the extracted mobility figures are well aligned with those reported previously for H-diamond which provides some confidence in the accuracy of the extraction process.

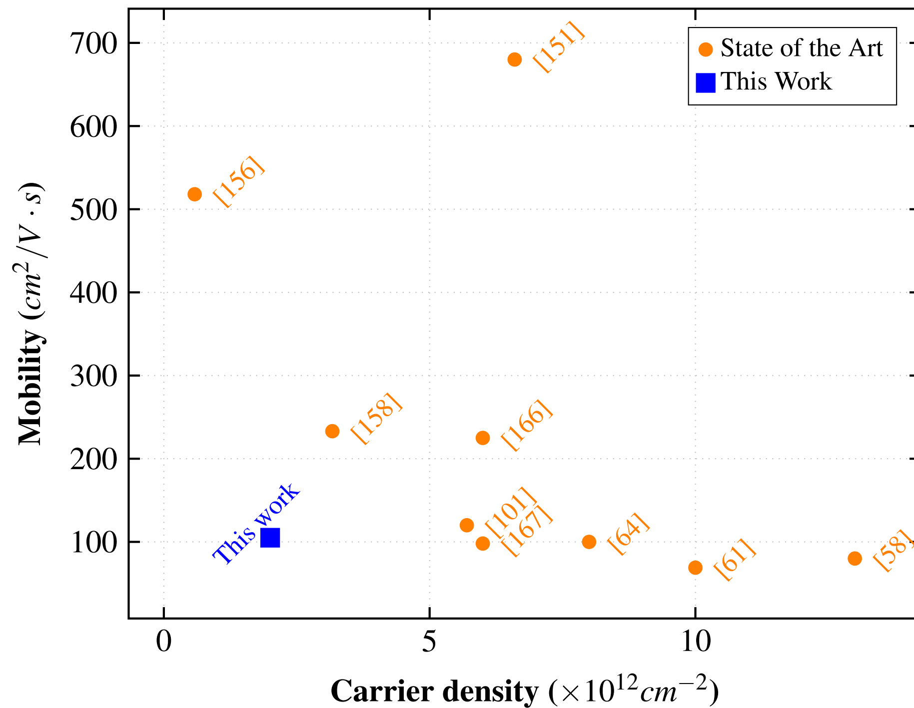


Figure 9.15: Benchmarks of carrier mobility versus the carrier density of the reported state-of-the-art hydrogen termination diamond.

9.4 Chapter Summary

In this chapter, an Accumulation Channel of hydrogen-terminated diamond MOSFETs has been demonstrated. Through a 350 °C anneal, the majority of air adsorbates were removed prior

to Al_2O_3 deposition. A 35 nm PVD Al_2O_3 layer was utilized as the insulator beneath the gate, while a 15 nm layer of low-temperature plasma-enhanced ALD Al_2O_3 was applied atop the PVD oxide to prevent gate short-circuiting with the source and drain ohmic pads.

The maximum drain current of 110 mA/mm was extracted with a channel length of 1 μm and width of 25 μm. The I_{on}/I_{off} ratio exceeding 10^9 was obtained from the transfer characteristics. The threshold voltage and transconductance were approximately -4 V and 22 mS/mm, respectively. The off-state breakdown voltage was measured at around -20 V.

By employing split CV measurement, the carrier concentration and mobility were extracted as 2×10^{12} cm^2 and 105 $cm^2/V \cdot s$, respectively. These calculations were based on the assumption of a dielectric constant of the oxide stacks being 6.6 and a parasitic capacitance of 5.84×10^{-14} F.

Overall, an Accumulation Channel device has been fabricated and measured. Numerous avenues for future work exist to enhance device properties. Improvements in the quality and adjustment of oxide thickness could enhance transconductance and off-state breakdown voltage. Gated Hall bar fabrication could offer a more accurate method for measuring mobility and concentration. Additionally, modifying the gate size may alter drain current and parasitic capacitance. These avenues present promising directions for optimizing device performance.

Chapter 10

Conclusions and Future Work

10.1 Conclusions

Diamond has been demonstrated as an highly promising material for high-power and high-frequency electronic devices due to its wide band gap, high thermal conductivity, and intrinsic mobility. In this work, the main purpose was to investigate the limitations of the existing fabrication methods of MOSFETs on H-diamond, thereby developing a novel method to improve the material and device properties, such as carrier mobility (μ), drain current (I_{ds}), I_{on}/I_{off} ratio, and threshold voltage (V_{th}).

In this work, Chapter 6 explored "Spillover" to hydrogen-terminate the diamond surface with catalyst metals (Pd and Pt) and hydrogen gas. With a designed 2-hour degassing process at 900°C followed by a 12-hour spillover process at 500°C, VDP measurements showed that the surface altered from insulator to conductor with sheet resistance around 13.2 $k\Omega/\square$, which is comparable to plasma-based hydrogen termination processes. The changes in surface hydrophilicity before and after the experiment also indicate the termination changes from oxygen to hydrogen. The absence of a requirement for a high vacuum system and no changes to the surface roughness are two advantages of this method over the traditional plasma-enhanced hydrogen termination process for diamond.

Chapter 7 explored alternative fabrication methods to replace the conventional gold sacrificial method in H-diamond FET fabrication. Lift-off resist was explored as an alternative protective layer; however, TLM measurements indicated the potential existence of resist residue. Further cross-fabrication verified around 14 nm of resist residue left on the surface. Subsequently, hydrogen plasma was investigated to remove the resist residue without damaging the surface termination. By altering the plasma power, stage temperature, and hydrogen flow rate, a slow etching recipe with an etching rate of 4.53 nm/s was established. Unfortunately, the H-diamond

surface turned into an insulator after the etching process. A potential explanation is that hydrogen plasma etches off diamond under low-temperature etching conditions. The final method explored in this chapter was Pd ohmic contact. TLM results illustrated that, on two H-diamond samples with similar sheet resistance, Pd contact showed lower contact resistance (3.82 $\Omega \cdot mm$) than that of gold contact (7.52 $\Omega \cdot mm$).

Chapter 8 reported H-diamond MESFETs fabricated using the conventional gold sacrificial layer method. The device was characterised after fabrication, after ALD Al_2O_3 deposition, and under high temperature. The measurements show that the ALD Al_2O_3 improved the drain current by a factor of two and reduced the gate leakage current by two orders of magnitude. However, the subsequent high-temperature tests showed that the devices degraded with elevated temperatures from 300K to 450K. The continually increasing contact resistance extracted from the TLM structure and decreasing transconductance measured from the MESFETs indicate there might be some disruption of air adsorbates under the gate contact and the ohmic contact.

The biggest achievement of this work is the Accumulation Channel MOSFETs reported in Chapter 9. By high-temperature (350 °C) annealing in a vacuum chamber and deposition of PVD Al_2O_3, a cleaned H-diamond area (an area without air adsorbates but with hydrogen termination) was created between the source and drain contacts, thus generating a normally-off device with an I_{on}/I_{off} ratio in the order of 10^9, a highest drain current of 110 mA/mm and threshold voltage $<$ -5 V with a gate width of 25 μm and length of 1 μm. The subsequent split CV measurement contributed to the calculation of carrier mobility and concentration, which are 105 $cm^2/V \cdot s$ and $2 \times 10^{12} cm^{-2}$, respectively. This device is the first demonstrated accumulation channel H-diamond MOSFET fabricated with PVD Al_2O_3.

10.2 Future work

Further work can be undertaken to optimise and verify many aspects of this research. For the spillover process, although a sheet resistance of 13.2 $k\Omega/\square$ has been achieved, several parameters, such as higher concentrations of hydrogen gas, faster flow rates, longer degassing durations, and extended spillover durations, can be explored to improve surface conductivity and uniformity. Furthermore, XPS can be a helpful tool to characterise the surface termination and provide solid evidence if the surface has been hydrogen terminated.

Regarding alternative fabrication methods, hydrogen plasma for resist residue removal still has potential to replace oxygen plasma by increasing the stage temperature. However, the compatibility of the resist used for fabrication with elevated temperatures needs to be considered to avoid damage and reduce the accuracy of the resist. Further experiments by fabricating TLM structures with Pd or Au on the same H-diamond sample can be conducted to enable stricter

comparisons. Additionally, more metals like Pb and Pt, with similar work functions to gold, could be explored to form better ohmic contacts.

Chapter 8's high-temperature measurements indicate a potential disruption of air adsorbates under the ohmic and gate contacts. Partially removing the air adsorbates with high-temperature annealing before the deposition of the contact metal could help determine if the increase in contact resistance and decrease in transconductance are caused by the disruption of air adsorbates. Fully removing the air adsorbates under the ohmic contact also helps explore the mechanism behind the ohmic contact between the H-diamond and high work function metals.

For the accumulation channel H-diamond device, Factors such as the thickness of the oxide and ohmic contact metal can be adjusted to achieve a more uniform capacitor between the gate and the substrate. The deposition of PVD Al_2O_3 can be optimised to achieve a more uniform oxide layer, improving the quality of the capacitor. Additionally, since there is a small overlapping area between the gate edges and the source and drain edges, which have only 15 nm of ALD Al_2O_3, the off-state breakdown in this work might also be improved by adjusting the thickness of the contact metal and the oxide to form a better contact. Furthermore, the annealing temperature can be increased to 400°C to fully remove the air adsorbates, potentially increasing carrier mobility by reducing scattering. Moreover, some device structures, such as the gate length, can be altered to achieve different device properties. To extract more accurate mobility data and contact resistance from this type of device, gated TLM and VDP structures can be fabricated on the H-diamond after the annealing process. Further measurements, such as high-temperature measurements, can also characterise the temperature stability of this device.

Appendix A

Appendix

	PMMA 50K 12%	PMMA 200k 4%	S1805	LOR 3A
Spinning	4500rpm 60secs	4500rpm 60secs	4500rpm 30secs	5000rpm 45secs
Baking	180°C 2mins	180°C 2mins	115°C 3mins	180°C 5mins
Development Solvent	1:1 MIBK:IPA	1:1 MIBK:IPA	1:1 Microposit: RO water	CD-26
Development	23°C 30secs	23°C 30secs	75secs	70secs
Ashing	80W 2mins	80W 2mins	100W 5mins	80W 5mins

Table A.1: Parameters for the resist used in this work. PMMA is e-beam resist, and S1805 is photo-resist. LOR stands for Lift-off resist which is not sensitive to either UV light nor e-beam, however it can be lift-off and etched by TMAH.

	Two stages Acid clean
Step 1	Mix 65%HNO_3 and 37%HCl in the ratio of 1:1
Step 2	Acid mixture heat up to 160°C to boil the mixture
Step 3	Sample rinsed in the boiled acid for 15 minutes
Step 4	Sample rinsed in RO water for 3 times to clean off the acid residue
Step 5	Mix 65%HNO_3 and 95%H_2SO_4 in the ratio of 1:3
Step 6	Acid mixture heat up to 240°C to boil the mixture
Step 7	Sample rinsed in the boiled acid for 15 minutes
Step 8	Sample rinsed in RO water for 3 times to clean off the acid residue

Table A.2: Parameters for the two stages acid cleaning process used in this work.

Step 1	Sample load and chamber vacuum down
Step 2	Stage heat up to 800°C
Step 3	Hydrogen plasma strike
Step 4	Stage cool down to 700°C
Step 5	Stop hydrogen plasma
Step 6	Chamber cool down to room temperature
Step 7	Chamber venting

Table A.3: Parameters for diamond hydrogen termination provided by Dr. Alastair Stacy from Australia.

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