Advancing Sensitivity and Performance of Capacitive Micromachined Ultrasound Transducers (CMUTs) for Medical Imaging

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Author's declaration

I hereby submit this thesis in fulfilment of the requirements for the degree of Master of Science in Mechanical Engineering (Research) at James Watt School of Engineering, University of Glasgow. This document is submitted solely for the purpose of this qualification.

I certify that this thesis is my original work, except where otherwise acknowledged or referenced. All information sources and literature used are properly referenced throughout the thesis.

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Date: 14.04.2025

Abstract

Ultrasound transducer technology has significantly contributed to advancements in medical imaging, continuously improving resolution, efficiency, and integration. Capacitive Micromachined Ultrasound Transducers (CMUTs) use electrostatic transduction to generate and detect sound waves, promise broader bandwidth, smaller size, and better integration with electronics than piezoelectric transducers, which improves Transduction efficiency and frequency response for next-generation imaging such as X-radiation (X-rays), Magnetic Resonance Imaging **(**MRIs), or standard photography.

This thesis focuses on improving CMUT sensitivity and performance for medical imaging through innovative design strategies, analytical modelling and optimized fabrication processes. The literature review covers ultrasound imaging principles, CMUT operation, and their use in diagnostics, therapy, biosensing, and airborne systems, while a comparison with PMUTs emphasizes CMUTs' improved electromechanical coupling and frequency response, supporting their role in advanced imaging. A fabrication process compatible with Complementary Metal Oxide Semiconductor (CMOS) is developed to support the integration of CMUTs with advanced electronic circuits, enabling the creation of compact and efficient imaging devices.

The research takes an experimental approach to improve a low-temperature sacrificial release method, enabling precise membrane formation with reduced stress. Various microfabrication techniques, including photolithography with photomask design using COMSOL, thin-film deposition, and etching, are refined to develop a scalable and reproducible fabrication process. To enhance CMUT sensitivity, the study uses analytical modelling with Hooke's Law and Euler-Bernoulli Beam Theory to analyse axial and bending stiffness in straight beams, then compares them to meander beams to assess their effect on CMUT sensitivity.

Experimental validation through capacitance-frequency (*C-F*) and capacitance-voltage (*C-V*) measurements confirms reliability, showing the Silicon Oxide (SiO_2) sacrificial layer remained stable without causing capacitance loss. Additionally, the measured permittivity of the sputtered SiO_2 closely aligns with values reported in previous studies, demonstrating consistency in material properties and fabrication precision.

In summary, this research has established a CMOS-compatible fabrication process and refines the dry etching release method to reduce stiction, laying the groundwork for advancing CMUT technology with improved reliability and adaptability for medical imaging. Future work aims to improve CMUT fabrication by adjusting material choices and enhancing the sacrificial release process.

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Table of Contents

List of Tables:

Table of Figures:

Table of Abbreviations

4TP	Four-terminal pair
2-D	Two-dimensional
3-D	Three-dimensional
AC	Alternating current
ALD	Atomic layer deposition
BHF	Buffered hydrofluoric acid
BOX	Buried oxide
BSA	Bovine serum albumin
C-F	Capacitance-frequency
C-V	Capacitance-voltage
CMOS	Complementary metal-oxide-semiconductor
CMUT	Capacitive Micro-machined Ultrasound Transducer
CMP	Chemical mechanical polishing
CVD	Chemical vapour deposition
DC	Direct current
DEAs	Dielectric elastomer actuators
DI	Deionized
DRIE	deep reactive ion etching
EBE	Electron Beam Evaporation
EBR	Edge Bead Removal
EMCC	Electromechanical Coupling Coefficient
EVAP	Electron-beam evaporation
FEM	Finite element method
H_C	High current
H_P	High potential
I-V	Current-voltage
IC	Integrated Circuit
ICP	Inductively Coupled Plasma
JWNC	James Watt Nano-Fabrication Centre
L_C	Low- current
L_P	Low-protentional
LOR	Lift-off resist
LPCVD	Low-pressure chemical vapour deposition
MA6	Mask aligner 6
MEMS	Micro-electromechanical systems
MRIs	Magnetic Resonance Imaging
MUTs	Micromachined Ultrasonic Transducers
NEMS	Nano-Electromechanical Systems
PECVD	Plasma - Enhanced Chemical Vapour Deposition
PMUT	Piezoelectric Micro-machined Ultrasonic Transducer
PW	Pulsed wave
PVD	Physical vapour deposition
QCM	Quartz crystal microbalance
RF	Radio frequency
RH	Relative humidity

RIE	Reactive ion etching
RX	Receiver mode
SAWs	Surface acoustic waves
SEM	Scanning Electron Microscopy
SNR	Signal-to-noise ratio
SOI	Silicon on insulator
SONAR	Sound Navigation and Ranging
TOBE	Top orthogonal to bottom electrode
TX	Transmitter mode
UV	Ultraviolet
VPE	Vapour-phase etching
X-Ray	X-radiation

List of Symbols

A	Amplitude
A_C	Cross-sectional area of the beam
A_e	Top electrode's area
A_{eff}	Effective area of the transducer membrane
Al	Aluminium
Al_2O_3	Aluminium oxide
Ar	Argon
Au	Gold
α	Beam angle measured from the horizontal axis
α_i	Incidence angle
b	Damping coefficient
BCB	Benzocyclo-butane
BCl_3	Boron trichloride
C_o	Transducer's static capacitance
CF_4	Carbon Tetrafluoride
CHF_3	Trifluoromethane
Cl_2	Chlorine
Cr	Chromium
D	Charge density vector
d	Diameter
d_1	Thickness of etched bottom layer
d_2	Thickness of etched higher layer
d_{31}	Sideways contraction and expansion
d_{33}	Movement perpendicular to the surface
dB	Decibel
δ_H	Deflection of horizontal segment of meander
δ_T	Deflection of the tilted segment of meander
δ_x	Axial displacement
δ_y	Vertical displacement
$[d]$	Piezoelectric coefficients
E_e	Electric field
E	Young's modulus
ε_o	Vacuum permittivity
ε_r	Relative permittivity
$[\varepsilon]$	Permittivity
F	Force
FBW	Fractional Bandwidth
F_e	Electrostatic forces
F_y	Force applied perpendicular to beam's length at the free end
g_o	Initial gap distance
g_{eff}	Effective gap height
H	Length of the horizontal segment of meander
H_2	Hydrogen
HF	Hydrofluoric acid
Hz	Hertz
I	Second moment of area
InP	Indium phosphide

IPA	Isopropyl alcohol
i_{th}	Number of vertical or tilted segment
KOH	Potassium hydroxide
k	Elastic coefficient
k_p	Spring constant
k_x	Axial stiffness
k_y	Bending stiffness
L	Length of beam
λ	Wavelength
M	External moment
m	Mass
MP 1165	Micro-posit Remover 1165
n	Number of periods
O_2	Oxygen
Mo	Molybdenum
N_2	Nitrogen
NH_3	Ammonia
N_2O	Nitrous oxide
PDMS	Polydimethylsiloxane
PMMA	Polymethyl methacrylate
Pt	Platinum
PZT	Lead Zirconate Titanate
R_0	Deposition rate at normal incidence
S	Strain
S_e	Selectivity
SF_6	Sulphur hexafluoride
Si	Silicon
SiC	Silicon Carbide
SiH_4	Silane
SiO_2	Silicon dioxide
Si_3N_4	Silicon Nitride
s	Distance between capacitance plate
$[s]$	Compliance constants
T_S	Stress
T	Length of the tilted segment of meander
Ti	Titanium
TMAH	Tetramethylammonium hydroxide
t	Beam's thickness
t_e	Etching duration
t_i	Insulator thickness
t_m	Membrane thickness
θ_H	Rotation angle of horizontal segment of meander
θ_T	Rotation angle of horizontal segment of meander
V	Voltage
v_{ac}	Alternating voltage
v_{DC}	Direct current voltage (bias voltage)
$V_{Collapse}$	Collapse voltage
w	Beam's width
η	Electro-mechanical coupling

Chapter 1: Introduction

1.1 Motivation

Capacitive Micromachined Ultrasound Transducers (CMUTs) have found uses in some aspects of medical ultrasound imaging by providing notable advantages over traditional piezoelectric transducers. This study offers an in-depth analysis of CMUTs, their role in medical imaging, and the impact of the sacrificial release method in improving their sensitivity and overall performance, aligning with the thesis motivation. The discussion is based on recent research, highlighting fabrication techniques, associated challenges, and potential future developments. CMUTs are microelectromechanical systems (MEMS) that produce and sense ultrasonic waves, offering excellent performance that makes them useful in medical imaging. They can function at high frequencies and offer a wide bandwidth, both essential for high-resolution imaging applications such as intravascular ultrasound (IVUS) [1]. These characteristics make them well-suited for capturing fine details in medical diagnostics, giving good image quality and diagnostic precision [2].

The silicon-based fabrication of CMUTs enables direct integration with electronics, resulting in compact and efficient transducer arrays. This integration is especially advantageous for advanced imaging techniques, where there is a growing need for enhanced sensitivity and performance [3]. Sensitivity, which refers to the ability to detect weak ultrasonic signals, enhances the signal-to-noise ratio (SNR), improving clarity and detail in medical images, and can be optimized by reducing CMUT cell radius to increase mass sensitivity to 0.46 Hz/ag and 0.44 Hz/ag [4], decreasing the electrostatic air gap, using embedding metallic layers to reduce gap height and boost sensitivity by 10% while increasing membrane thickness, Young's modulus, and DC bias voltage [5], [6], applying parametric amplification with ac pumping voltage to raise receiving sensitivity by at least 7 dB [7], and fine-tuning membrane material, radius, thickness, electrode size, and bias voltage to maximize SNR [8].

The progress in medical imaging technologies, fuelled by the need for higher resolution and superior image clarity, necessitates the development of transducers with improved performance. It has been highlighted that increasing CMUT sensitivity is vital for detecting weaker signals, which is necessary for applications such as 3D imaging. The transducer's ability to support diverse imaging modalities depends on its performance, particularly in terms of bandwidth and efficiency [9]. The challenge lies in achieving these improvements while

maintaining cost-effectiveness and reliability, which is where fabrication techniques like the sacrificial release method are relevant.

Research suggests that the method's precision in controlling structural parameters can significantly enhance CMUT performance. The sacrificial release method, a surface micromachining technique, is responsible for creating the vacuum gap beneath the transducer membrane. This process involves depositing a sacrificial layer onto the substrate, which is later removed using a selective etchant that does not affect the membrane layer [3]. This gap allows the membrane to move freely in response to ultrasonic waves, directly contributing to the transducer's sensitivity and overall performance. This method provides precise control over membrane deflection, which is important for optimizing electroacoustic performance [10]. Adjusting the gap height and membrane thickness helps decrease parasitic capacitance, which in turn enhances the transducer's receiving capability [11]. Furthermore, innovations such as through-wafer via interconnections improve electrical connectivity in 2D arrays, contributing to enhanced overall performance [1]. The sacrificial release method offers several advantages, including improved control over uniformity and mechanical properties, which are vital for achieving consistent device performance.

This thesis seeks to enhance the sensitivity and performance of CMUTs for medical imaging by optimizing the sacrificial release method and incorporating a meandering beam design. The study focuses on refining the process to improve membrane deflection, minimize parasitic capacitance, and increase overall efficiency. By addressing these factors, the research aims to contribute to the development of advanced CMUTs that align with the demanding standards of modern medical ultrasound systems. Integrating these advancements could broaden the use of ultrasound, improving accessibility and patient care.

1.2 Contributions to Knowledge

In CMUT fabrication, design and material selection are key factors influencing performance, durability, and ease of manufacturing. This study explores innovative approaches, including the adoption of a meandering membrane structure, replacing polyimide which was used previously as a sacrificial layer [12] with sputtered silicon dioxide (SiO_2), and utilizing Hydrofluoric acid (HF) vapour for sacrificial layer release. These advancements tackle persistent challenges while opening new opportunities in the field.

The meander design changes the way CMUT membranes manage mechanical stress and movement. Unlike a rigid, linear structure, this pattern enhances flexibility and distributes

stress more evenly, minimizing the risk of fractures and extending the membrane's lifespan [13]. This is not just about making the membrane last longer—this design also helps it move more smoothly and efficiently. That means better sensitivity and a wider bandwidth, which are essential for producing sharper images and more accurate sensing. Switching to sputtered SiO_2 as a sacrificial layer in CMUT fabrication is a major upgrade, especially for low-temperature processes used in above- Integrated Circuit (IC) integration. Traditionally, polyimide has been the preferred option because it is easy to apply and remove [14]. However, it has some major drawbacks. It easily absorbs moisture, its dielectric properties can be unpredictable, and it gradually breaks down over time, which can affect the long-term reliability of CMUTs [15]. Replacing polyimide [12] using sputtered SiO_2 overcomes these challenges by offering greater mechanical stability, more consistent electrical properties, and improved resistance to environmental conditions, making it a significantly more reliable option. [16]

Sputtered SiO_2 provides a fully inorganic, thermally stable, and low-defect alternative with excellent step coverage, uniformity, and strong adhesion to Al-metallized circuits, making it highly beneficial for advanced semiconductor technologies. In contrast, removing polyimide through oxygen (O_2) plasma ashing can introduce contamination and residual stress, compromising the accuracy of CMUT cavity formation [17] Meanwhile, sputtered SiO_2 deposition enables adjustable stress control and minimizes charge trapping, which is crucial for ensuring high performance and reliability.

A key benefit of sputtered SiO_2 is its excellent compatibility with Hydrofluoric acid (HF) vapour release. One of the biggest challenges with the conventional choice of wet etching, particularly when using polyimide, is stiction [18], where the CMUT membrane sticks and collapses due to surface tension as the liquid evaporates. This can result in defects, reduced fabrication yields, and inconsistent performance. HF vapour etching eliminates this issue by removing the sacrificial layer through a dry process, preserving membrane integrity and ensuring cleaner, more uniform cavity formation.

By combining sputtered SiO_2 with HF vapour etching, this work aims to create a CMOS-compatible fabrication process to make CMUTs more scalable and high-performing, for modern ultrasound applications. These improvements will optimise CMUTs for medical imaging, therapeutic ultrasound, industrial non-destructive testing, and emerging tech like wearable ultrasound devices. Additionally, this approach helps bridge the gap between MEMS and semiconductor manufacturing, making it easier to integrate CMUTs with advanced electronics for more compact and efficient ultrasound imaging systems.

In summary, this work brings together three improvements: a stress-optimized meander design, a stable sputtered SiO_2 sacrificial layer, and a carefully controlled HF vapour release process. By combining these elements, it aims to test and develop a more practical and scalable method for building more sensitive CMUTs. This approach moves beyond the limitations of traditional methods that rely on polyimide, making CMUT fabrication more efficient. With sputtered SiO_2 and HF vapour etching refining the sacrificial release process, this research opens the door for CMUTs to play a bigger role in medical imaging and other cutting-edge applications.

1.3 Thesis structure

This thesis is structured to provide a comprehensive exploration of CMUTs, covering their fundamental principles, fabrication processes, analytical modelling, performance evaluation, and future advancements. Each chapter builds upon the preceding one, offering a logical progression from theoretical background to practical implementation and optimization.

In Chapter 2, Literature Review, a comprehensive overview of ultrasound transducers is provided, focusing on micromachined ultrasound transducers (MUTs), their principles of operation, fabrication methods, and applications. The discussion begins with an introduction to ultrasound imaging, exploring its fundamental working principles and historical background. It then delves into MUTs, distinguishing between piezoelectric micromachined ultrasonic transducers (PMUTs) and CMUTs. A comparative analysis highlights their respective advantages and limitations, aiding in the selection of the most suitable transducer type for specific applications. The diverse applications of CMUTs are then examined, spanning medical imaging, therapeutic applications, chemical and biosensing, physical sensing, and airborne applications. Finally, the fabrication processes of CMUTs are explored, focusing on wafer bonding techniques, including direct, anodic, and polymer adhesive wafer bonding, as well as the sacrificial release method, providing insight into their role in achieving optimal device performance.

In Chapter 3, the analytical framework for understanding CMUT structures is discussed, beginning with an exploration of axial and bending stiffness. It utilises the fundamental concepts of stiffness in straight cantilever beams, employing Hooke's Law for axial stiffness and the Euler-Bernoulli Beam Theory for bending stiffness. The theory of meandering design is then introduced as a means of optimizing mechanical performance, followed by estimation of axial and bending stiffness. The chapter concludes with calculations that validate these

theoretical models, ensuring that the proposed design aligns with experimental and practical constraints.

In Chapter 4, the fabrication process is explored in detail, beginning with an overview of the cleanroom processes and tools for device manufacturing. Photolithography techniques, including photoresist spin coating, soft baking, alignment and exposure using an MA6 tool, and development processes, are thoroughly discussed, alongside the challenges associated with photolithography. The discussion then covers etching methods, lift-off techniques, and deposition methods such as physical vapour deposition (PVD) and chemical vapour deposition (CVD). Etching techniques, including wet and dry etching, and the HF vapour release tool are examined in depth, particularly focusing on their role in optimizing CMUT fabrication. Material selection criteria are outlined to ensure compatibility with the desired device performance. A step-by-step walkthrough of the CMUT fabrication process follows, detailing substrate cleaning, electrode deposition, sacrificial layer formation, membrane deposition, and final etching cycles required for device release. Emphasis is placed on the challenges and optimizations associated with the HF vapour etching process, aiming to enhance structural integrity and operational efficiency.

In Chapter 5, the measurement techniques used to evaluate the performance of capacitive part of CMUTs are presented. The setup for capacitance measurement is described in detail, including the analysis of capacitance-frequency (*C-F*) measurements from DC to 5 MHz and capacitance-voltage (*C-V*) measurements ranging from -2 V to 2 V. These measurements provide insights into the electrical behaviour and efficiency of the fabricated devices. Furthermore, the validation of the dielectric constant (ε_r) (for SiO_2 sacrificial layer) using *C-V* measurements is discussed, ensuring that the fabricated CMUTs meet the expected performance criteria.

Chapter 6 provides conclusions and outlines future work, which includes material optimization, sacrificial release refinement, numerical modelling, etching improvements, electrode adjustments, and passivation layer enhancement. These refinements aim to improve CMUT performance, reliability, and applicability in medical imaging and diagnostics.

Chapter 2: Literature Review

2.1 Background on ultrasound

After the sinking of the Titanic in 1912, Paul Langevin was commissioned to develop a device for discovering underwater items in the ocean. In 1915, motivated by the tragedy, he designed and constructed the first hydrophone, an invention that can claim to have been the first ultrasound transducer. It facilitated development of the first Sound Navigation and Ranging (SONAR) system, a technology that measures distance to an object through pulse-echo sending and returning sound [19].

The principles of pulse-echo technology, first developed for SONAR, became the basis for the medical application of ultrasound (frequency ≥ 20kHz) during and following World War II. In 1942, neurologist and physicist Karl Dussik first used ultrasound for diagnosing brain tumours at the University of Vienna. In 1948, its application in gallstone diagnostics was first reported by George Ludwig. Ultrasound scanners have increasingly been used in a range of medical specialties over the years, with widespread use in abdominal imaging, and echocardiography, for visualization of the heart. Another milestone in this evolution was the contribution of Ian Donald, whose invention of diagnostic ultrasound revolutionized obstetrics and gynaecology in the mid-20th century [20]. In the post-war period, ceramic resonators were designed with barium titanate to exploit its high permittivity and piezoelectric coefficients and, in the 1950s, lead zirconate titanate (PZT) ceramic replaced barium titanate for use in generating and receiving sound waves [21].

In solids, sound waves can travel in two ways: as longitudinal waves, where particles oscillate in the same plane as the wave, and as shear (or transverse) waves, where particles move perpendicular to the wave's path, as shown in Figure 2-1. For shear waves to exist, the material needs to be rigid enough for particles to "pull" on their neighbours. Fluids, like water or air, do not have this rigidity so they can support only longitudinal waves. Since the human body is mostly water, tissues are usually treated are usually treated as fluids in medical ultrasound and shear waves are often ignored. However, when designing ultrasound transducers, shear waves matter because the materials used in the transducer are solid and both types of waves can travel through them [19].

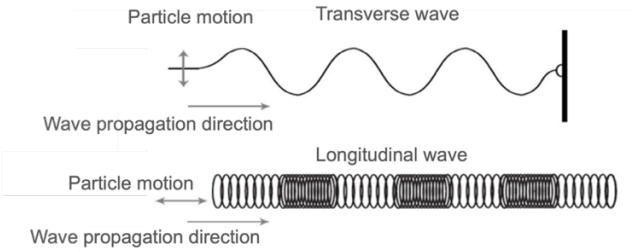


Figure 2-1: Illustration of Shear and Longitudinal Waves [19].

Human tissues like fat, muscle and blood each interact with sound waves in their own way which is the principle of ultrasound imaging. When an ultrasound machine sends a wave pulse into the body, part of the wave keeps traveling while the rest is reflected partially every time it is incident on a different layer of tissue. The transducer detects for these echoes and, by measuring when they return, the system calculates how deep each structure is. This process helps create the detailed images seen in an ultrasound scan [19].

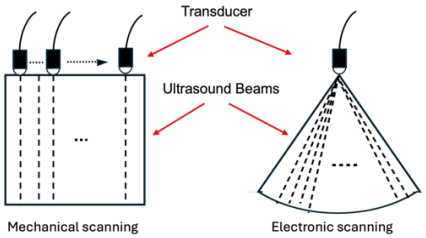


Figure 2-2: Steering the beam and creating an ultrasound image.

To create an ultrasound image, the transducer needs to send sound waves in different directions and capture the echoes that come back. This process, called beam steering, can be done in two ways: mechanically or electronically. As shown in Figure 2-2, mechanical beam steering moves the transducer using a motor to scan the area, but this method has drawbacks. In contrast, electronic beam scanning controls the timing of sound waves sent from different parts of the transducer, allowing for more precise imaging without needing moving parts. While this approach is more accurate, it also makes the device more complex [19].

2.2 Micromachined Ultrasound Transducers

A notable development in ultrasound imaging was seen in the adoption of MEMS technologies. These offer possibilities as a viable alternative to traditional bulk transducers, improving manufacturing processes and sometimes overall performance, paving the way for alternative ultrasound technology [22].

MEMS-based ultrasound transducers have the advantage that they use technology similar to complementary metal-oxide-semiconductors (CMOS). This means they can theoretically

be manufactured at a lower cost, with greater design flexibility. Because MEMS and CMOS can be integrated into the same package, unwanted electrical interference can sometimes be reduced while making the system smaller, lighter, and more energy-efficient [23].

Among the different types of MUTs, the two most common are CMUTs and PMUTs. These may helped overcome many of the limitations found in traditional bulk ultrasound transducers. In particular, they may offer better control over operating frequency [24] and provide a closer acoustic impedance match with biological tissues, which improves imaging performance [25]. However, MUTs are not used only for medical applications. They have been proposed for fluid sensing to measure viscosity, density, and flow rate [26], [27], [28], [29], as well as in humidity sensors [30], eye-tracking systems [31], and particle manipulation [32]. They may also have a role in chemical and gas detection [33], monitoring structural health in buildings and materials [34], [35] and in airborne technologies like gesture recognition and haptic feedback [36]. With their versatility and efficiency, MUTs maybe useful beyond just ultrasound imaging, making them potential technology for the future. This will be elaborated in detail in the following sections.

2.2.1 Principle of operation

Medical ultrasound involves the use of electro-acoustic signals, typically in the MHz range, for diagnostic purposes. To convert electrical signals into sound waves and vice versa, transducers act as both transmitters and receivers. In this regard, CMUTs and PMUTs function as actuators and sensors, utilizing a vibrating membrane in a flexural mode. To better understand how these devices operate in the mechanical domain, they can be modelled using a mass-spring-damper system, as shown in Fig. 2-3(a).

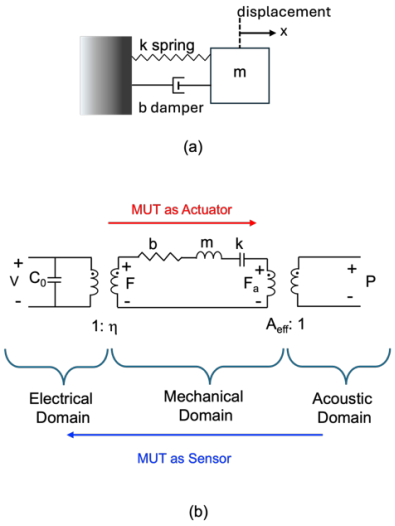


Figure 2-3: (a) Model of mass-spring and damper system (b) simplified Mason model.

Here, the membrane's flexion is approximated as the piston-like motion of a rigid plate with mass m. When an external force is applied, the membrane bends and generates an opposing force to restore equilibrium. This restoring effect can be represented by a spring with an elastic coefficient k. Additionally, energy losses, including acoustic and mechanical coupling losses, can be accounted for using a damper with a damping coefficient b. By applying Newton's second law, the flexural motion of the MUT membrane can be described through a second-order differential equation as below:

$$m\frac{d^2x}{d^2t} + b\frac{dx}{dt} + kx \quad = F \qquad \text{Eq. 2.1}$$

Here, x represents the flexural displacement of the MUT membrane, while F denotes the total force acting on it, which includes contributions from acoustic and electrostatic forces, as well as forces generated by the piezoelectric effect (if present) and ambient pressure. From Eq. 2.1, the MUT's resonant frequency can be determined. While the mass-spring-damper model effectively captures the membrane's flexural motion, it does not account for the transducer's electrical characteristics, which are essential for analysing and designing its front-end electronics. To address this, the equivalent circuit model, known as the Mason model Figure 2-3 (b) can be used. This provides a linearized representation of the electromechanical-acoustic behaviour of the transducer around a bias point, without considering nonlinear distortion effects [37], [38].

Despite its simplifications, the Mason model provides a framework for approximating MUT performance, allowing for the prediction of electrical and mechanical losses, as well as interactions between the transducer and the surrounding medium. In this model, the equivalent inductor, capacitor, and resistor correspond to the mass, spring, and damper of the mechanical system, respectively. The same Mason model applies whether the transducer operates as an actuator (transmitter, TX mode) or as a sensor (receiver, RX mode). In the electrical domain, a voltage (V) is either applied to or sensed by the MUT, depending on whether it functions as a transmitter or receiver. The transducer's static capacitance is represented by C_o. To bridge the electrical and mechanical domains, an ideal transformer with a ratio of 1:η is used, where η is the electromechanical coupling coefficient. Similarly, the mechanical domain is linked to the acoustic domain through another ideal transformer with a ratio of A_{eff}:1, where A_{eff} represents the effective area of the transducer membrane. This transformation process enables the conversion of voltage into force, which is then further translated into acoustic pressure [22].

The mass-spring-damper and Mason models effectively capture the fundamental working principles of MUTs; however, they involve significant simplifications and do not fully account for nonlinear behaviours and other non-idealities present in the device. To achieve more precise design and characterization of MUTs, the finite element method (FEM) - both static and dynamic - can be employed [26].

The next sections provide a more detailed explanation of the physics behind PMUTs and CMUTs, with a particular emphasis on their behaviour in biomedical applications.

2.2.2 Micro-machined ultrasound transducer

Ultrasonic signals are usually created using one of four main methods: the piezoelectric effect, magnetostriction, the photo-acoustic effect or electrostatics [39]. The most common of these is the piezoelectric effect, which is widely used in PMUTs and traditional bulk PZT transducers. Piezoelectricity occurs in certain materials, like piezoceramics and crystals, which change shape when an electric field is applied. At the same time, if these materials are physically can pressed or stretched, they generate an electrical charge [33]. This phenomenon can be explained using the fundamental equations of piezoelectricity:

$$S = [s^{E_e}][T_s] + [d^{T_s}]E_e \qquad \text{Eq. 2.2}$$

and

$$D = [d^{E_e}][T_s] + [\varepsilon^{T_s}]E_e \qquad \text{Eq. 2.3}$$

In this context, S and T_S represent strain and stress, while E_e stands for the electric field and D represents charge density. The behaviour of the material is determined by three key matrices: $[s]$, which defines compliance constants (measured in m²/N); $[\varepsilon]$, which describes permittivity (measured in F/m); and $[d]$, which contains the piezoelectric coefficients (measured in C/N). The way PMUTs work is based on flexural vibrations triggered by either d_{31} or d_{33} mode excitation. The d_{31} mode refers to sideways contraction and expansion, while the d_{33} mode involves movement perpendicular to the surface when voltage is applied. These vibrations are what generate ultrasonic waves when electricity is supplied and, in turn, create an electrical signal when exposed to an incoming ultrasound wave. To measure how effectively a device converts electrical energy into mechanical motion (and vice versa), the electromechanical coupling coefficient (EMCC) is used. This metric gives a good indication of the device's overall performance [40], [41].

Figure 2-4 shows a basic diagram of a PMUT transducer. It consists of a thin piezoelectric film, typically a few hundred nanometres to a micrometer thick, placed between two electrodes (top and bottom). Beneath this, there is a SiO_2 layer that helps support the piezoelectric film while it operates. This layer also plays an important role in converting sideways stress (from the d_{31} mode) into perpendicular displacement, allowing the membrane to vibrate in its flexural modes. Underneath these layers, there is a small cavity that is key to how the PMUT resonates. Its size is carefully designed to match the natural vibration frequency of the membrane. The exact resonant frequency of a PMUT depends on several factors, including its shape, size, boundary conditions, internal stress, and mechanical stiffness [42].

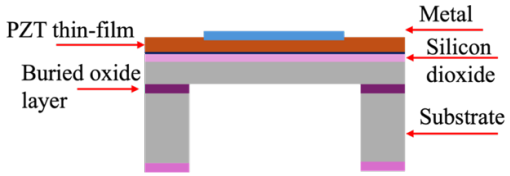


Figure 2-4: Schematic of a PMUT cross section.

Enhancing the frequency response of transducers to further shorten their impulse response can significantly improve image resolution and expand the operational range of a given device. Recent advancements in composite materials and single-crystal transducers have been centred around achieving this goal.

2.2.3 Capacitive micro-machined ultrasound transducer

Electrostatic transducers, such as CMUTs, initially were utilized in condenser microphones designed by Wente as early as 1917 [43]. Hunt later provided an in-depth analysis and design principles for electrostatic transducers, emphasizing their ability to achieve a flat and uniform frequency response [44]. In 1996, Ladabaum, Khuri-Yakub, and their team introduced a new way to make ultrasound transducers using surface micromachined technology. By using silicon nitride (Si_3N_4) membranes, they developed a more efficient method for creating transducers with a broad frequency response, making them suitable for immersion applications [45].

CMUTs operate based on electrostatic transduction, where a vibrating membrane plays a key role in generating and detecting sound waves. This membrane, which contains a conductive layer acting as the top electrode, moves in response to an applied voltage. The bottom electrode is typically part of the conductive substrate, and between them lies a cavity. When voltage is applied, an electric field forms within the cavity, allowing the device to convert electrical energy into mechanical vibrations and vice versa. [22] The membrane's shape—

which can be square, circular, or hexagonal—affects how it vibrates and how efficiently it transmits sound [46], [47], [48]. It is firmly attached at its edges, leaving the middle free to oscillate over the cavity. Depending on the design, the cavity can be vacuum-sealed or filled with air, with an electric field strength reaching several tens of volts per micron or even higher. This strong field contributes to efficient energy conversion [26]. To prevent short circuits, an insulating layer is added between the electrodes, ensuring the device operates safely and reliably. A schematic cross-section of a typical CMUT provides a view of this structure in Figure 2-5.

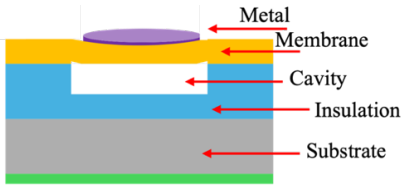


Figure 2-5: Schematic of a CMUT cross-section.

2.2.4 CMUT working principle

At a fundamental level, a CMUT functions similarly to a parallel-plate capacitor, where the top electrode is movable. To generate acoustic pressure waves, the diaphragm is actuated using electrostatic forces (F_e), causing it to vibrate in response to an applied voltage,

$$F_e = \frac{-A_e \varepsilon_0 \varepsilon_r V^2}{2(g_{eff}-x)^2} \qquad \text{Eq. 2.4}$$

In this setup, the top electrode's area is represented by A_e, while ε_o is the vacuum permittivity, and ε_r is the relative permittivity of the insulating and membrane materials, which are assumed to be the same. The applied voltage, V, controls the movement of the top electrode, with x representing its displacement. The effective gap height is calculated as:

$$g_{eff} = \frac{(t_i+t_m)}{\varepsilon_r} + g_0 \qquad \text{Eq. 2.5}$$

Where g_o is the initial gap distance when no voltage or external stress is applied, t_i is the insulator thickness, and t_m is the membrane thickness. By adjusting V, the electrostatic force changes dynamically, causing the diaphragm to vibrate and generate ultrasound waves [49]. When the CMUT operates as a sensor, external acoustic waves make the membrane oscillate, leading to capacitance variations. These variations are then converted into a changing voltage or current, allowing the device to detect sound waves [26].

Assuming the membrane moves by a displacement of x and the cavity is a vacuum, the CMUT can be modelled as an equivalent parallel-plate capacitor, with its capacitance determined by a standard equation [49].

$$C = \frac{A_e \varepsilon_0 \varepsilon_r}{g_{eff} - x} \quad \text{Eq. 2.6}$$

The operation of a CMUT, whether as an actuator or a sensor, follows the principles of Newton's second law and an electromechanical model, which results in a second-order differential equation describing its behaviour. This equation is non-linear in terms of the membrane's movement but, in most practical cases, the CMUT is operated with a large DC bias voltage (V_{DC}), which is then modulated by a small ac voltage (V_{ac}). This means the total applied voltage can be written as $V = V_{DC} + V_{ac}$ in actuation mode. This voltage combination causes the membrane to vibrate and generate ultrasound waves, while in sensing mode, incoming acoustic pressure causes the membrane to oscillate, leading to variations in capacitance. To simplify analysis, the electrostatic force acting on the membrane is often linearized as a function of the DC bias voltage to make calculations more manageable [49].

When a DC bias voltage is applied to the top electrode, it creates an electric field that pulls the membrane downward, allowing it to move in a spring-like motion. However, if this voltage becomes too high, the membrane's displacement increases to the point where the electrostatic force exceeds the physical stiffness of the membrane, causing it to collapse onto the bottom electrode. This is known as the pull-in phenomenon, a condition where the membrane can no longer return to its original position because the attraction between the electrodes is too strong [50]. The voltage at which this collapse happens is called the collapse voltage, marking the limit beyond which stable operation is no longer possible:

$$V_{collapse} = \sqrt{\frac{8K_p {g_{eff}}^3}{27\varepsilon_0 \varepsilon_R A}} \quad \text{Eq. 2.7}$$

In this case, K_p represents the spring constant in the mass-spring model, which helps describe how the membrane moves [49]. While collapse mode is usually avoided because of its non-linear behaviour, it has some advantages. When properly controlled, it can generate higher output pressure and improve electromechanical coupling, making it a useful alternative to conventional operation [50].

There are three main types of collapse mode, each working slightly differently: traditional collapse mode, collapse snap-back mode, and deep collapse mode [50]. In traditional collapse mode, the centre of the membrane touches the substrate, restricting its movement but still allowing controlled vibrations. Collapse snap-back mode starts by putting the CMUT into a collapsed state, but by carefully adjusting the voltage, the membrane is allowed to detach from the substrate, restoring some of its motion. Deep collapse mode happens when the applied ac voltage is higher than the collapse voltage, causing the membrane to push even further beyond its normal collapse point. The choice of which collapse mode to use depends on the specific application of the transducer. Since each mode affects things like sensitivity, efficiency, and operating range, selecting the right one helps ensure that the CMUT performs optimally for its intended application [22]. The equations for electrostatic force and capacitance assume ideal conditions such as perfectly parallel plates, vacuum-filled cavities, and uniform material properties. In practice, effects like dielectric charging, membrane curvature, and nonuniform electric fields can cause deviations, making advanced simulations and experimental validation necessary for accurate CMUT performance prediction.

2.3 Comparison between CMUT and PMUT

Compared to traditional piezoelectric transducers, CMUT arrays offer several advantages as well as certain challenges. A summary of these aspects is provided in Table 2-1.

Table 2-1: Comparison between CMUT and PMUT.

Feature	CMUT	PMUT
Impedance Matching	Highly efficient in both air and liquids, improving overall energy performance.	Less optimized, leading to lower energy efficiency.
Bandwidth	Wide bandwidth (over 100%), giving detailed and sharper images.	Moderate bandwidth (60-80%), slightly less detail.
Image Quality	Sharp images, good contrast, and an expanded field of view.	Acceptable images but missing CMUT's sharpness and contrast.
Manufacturing	Microfabrication allows for ultra-compact, high-frequency components.	Traditional fabrication, resulting in larger elements
Cost	Cost-effective when mass-produced	Can be more expensive due to fabrication complexity
Integration	Easily integrates with modern circuits and 3D stacking	Limited integration with modern electronic circuits
Sensitivity	Low sensitivity, limiting deep imaging performance	Higher sensitivity, better for detecting weaker signals
Penetration	Struggles to reach deep tissues effectively	More effective at penetrating deeper tissues
Reliability	Can suffer from charging issues over time	More stable and less affected by charging issues
Interference	Highly prone to cross-talk and acoustic wave interference	Less cross-talk and interference, providing clearer signals

One key benefit is their improved impedance matching in both air and fluid environments [51], [52], which allows for wider bandwidths. While piezoelectric transducers typically have a fractional bandwidth (*FBW*) of 60%-80%, CMUTs can easily exceed 100%, significantly enhancing signal transmission and reception. Bandwidth plays a crucial role in image resolution, as a wider bandwidth leads to higher resolution images. Studies comparing CMUT arrays with piezoelectric transducers in in-vitro imaging have shown that CMUTs can provide better radial resolution, a notable improvement in contrast, and a wider field of view [53], [54], [55]. A great advantage of CMUT operation is that by adjusting the DC bias voltage, you can selectively activate specific elements in the CMUT array. This makes it easy to switch between different sub-apertures while using the same set of TX/RX electronics, adding more flexibility to the system. On top of that, recent advancements have improved sensitivity [56] and significantly reduced second harmonic distortion [57].These advantages make CMUTs highly promising for ultrasound imaging applications, particularly in areas requiring high detail and accuracy.

One of the advantages of CMUTs over piezoelectric transducers is how they are manufactured. Thanks to photolithographic techniques, CMUTs can be made with extremely small features, both in terms of depth and lateral size. This supports tight packing of elements, which is essential for high-frequency ultrasound imaging, where precision and miniaturization matter [19]. Another major benefit is that CMUTs are built using micromachining, which allows multiple wafers to be processed in the same production run. When this process is optimized, it can significantly lower production costs per device for large numbers of devices compared to traditional manufacturing methods. Moreover, CMUTs can be directly integrated with their driving electronics using through-wafer vias and 3D stacking, meaning the transducers and multiple IC chips can be combined into a single, compact package. This level of integration can not only make devices more efficient, but also reduce size, improve performance, and simplify system design [58], [59].

One of the biggest challenges with CMUTs in medical imaging is their lower sensitivity, which limits how deeply sound waves can penetrate tissues [21], [53]. To improve this, researchers have experimented with different membrane shapes and sizes to make them more efficient at transmitting and receiving ultrasound waves. One promising approach is using a rectangular membrane design, which has shown better performance in certain applications [60]. Another way to boost sensitivity in RX mode is through a dual-electrode CMUT configuration, which helps pick up weaker signals more effectively [61], [62]. Another

issue that affects CMUTs and other MEMS devices is the charging effect [63], [64]. Because of the strong electric fields inside the transducer cavity or during fabrication, electrical charges can build up in unwanted areas. This can cause problems, especially when the CMUT operates in collapse mode, when the membrane is pulled down. If charge becomes over-accumulated, the membrane may get stuck and not return to its original position, leading to performance issues, reduced reliability, and a shorter lifespan for the device [65].

The other challenge that CMUTs might face, is acoustic cross-talk, which can interfere with how well the device operates and needs to be carefully controlled. This happens when acoustic waves unintentionally transfer between CMUT elements, either through the fluid-structure interface or the substrate that supports the device. As the CMUT membrane vibrates, it can send sound waves into neighbouring elements, causing interference and reducing overall performance. Two major contributors to this issue are surface acoustic waves (SAWs) that travel through the substrate and dispersive guided modes that form at the fluid-CMUT interface [66], [67]. Cross-talk also occurs when the membrane's vibrations create longitudinal waves that travel into the substrate. These waves can reflect from the bottom of the substrate and be picked up by the CMUT again, disrupting the intended signal pattern. To reduce this effect, one approach is adding a backing layer to the substrate, which helps absorb unwanted waves and prevent interference [67], [68]. Another method is thinning the substrate, which raises its resonance frequency above the CMUT's operating range. However, making the substrate too thin can create plate modes, like Lamb waves, which introduce more unwanted vibrations [69]. A more effective and advanced solution is using deep trench isolation, where physical barriers are placed between CMUT elements to block sound waves from spreading, significantly reducing cross-talk and improving performance [70]. To tackle these challenges, developers are continuing to work on refining CMUT parameters [22], while also making significant advancements in both structural design [71] and manufacturing techniques [72], [73].

2.4 Applications of CMUTs

CMUTs are utilized in a variety of fields, including medical imaging, chemical and biosensing, physical sensing, and other applications. As this work focuses on CMUTs for medical imaging, this particular application is discussed in detail in the following section.

2.4.1 Medical Imaging

CMUTs find uses in medical imaging, where both bandwidth and sensitivity play a role in image quality. Traditional piezoelectric thick-film transducers require front acoustic matching and backing layers to efficiently transmit ultrasound waves. Without the use of matching layers, they exhibit narrow bandwidth and high-Q behaviour, causing a ringing effect after excitation, which can reduce image clarity. To achieve high-resolution imaging, a narrow impulse response is necessary. High-bandwidth CMUTs provide this, leading to wider operational frequency range and improved image resolution [26]. When CMUTs operate near the pull-in voltage, their RX sensitivity increases significantly, enhancing the SNR [21], [74].

Caronti et al. demonstrated this by fabricating a 64-element 1D CMUT array with a centre frequency of 3.5 MHz and 130% fractional bandwidth when tested in immersion. These CMUTs, made using a sacrificial release process with SiNx as the membrane material, were successfully used to image a cyst phantom and a human carotid artery.[2] A study by Mills from General Electric Global Research compared the imaging performance of PZT arrays, surface-micromachined CMUTs, and bulk-micromachined CMUTs for scanning the human carotid artery and thyroid gland. The findings showed that CMUTs produced slightly better image quality than piezoelectric transducers in terms of resolution, but they were less effective for deeper tissue penetration [21].

Savoia et al. provided a detailed explanation of the system integration of an ultrasonographic system utilizing a 192-element CMUT array. The system incorporated a 12-MHz probe, which featured a surface-micromachined CMUT array with a Si_3N_4 plate. These CMUTs were fabricated using a reverse fabrication method, beginning with the deposition and patterning of the top electrode, followed by the deposition of the plate material. This approach allowed for the precise use of low-pressure chemical vapour deposition (LPCVD) Si_3N_4 as the CMUT plate. Additionally, the top-down fabrication method facilitated interconnects without requiring through-silicon vias. After wire bonding, a backing layer was introduced, and the base silicon beneath the Si_3N_4 plate layer was etched away. An acoustic lens was then integrated and the CMUT array was connected to the electronic circuitry to form the scanning probe. This probe was designed to be compatible with commercial ultrasound systems, enabling it to generate medical images [75]. Figure 2-6 presents the images obtained using the CMUT-based ultrasound probe and compares them with those captured by a piezoelectric thick-film-based ultrasound probe.

Zhao et al., in collaboration with Kolo Medical Inc., USA, developed and commercialized a 15-MHz, 256-element linear ultrasound array utilizing CMUT technology. This probe featured elements arranged with a pitch of 108 μm, an element elevation of 2.5 mm, and an element focus of 15 mm [76].

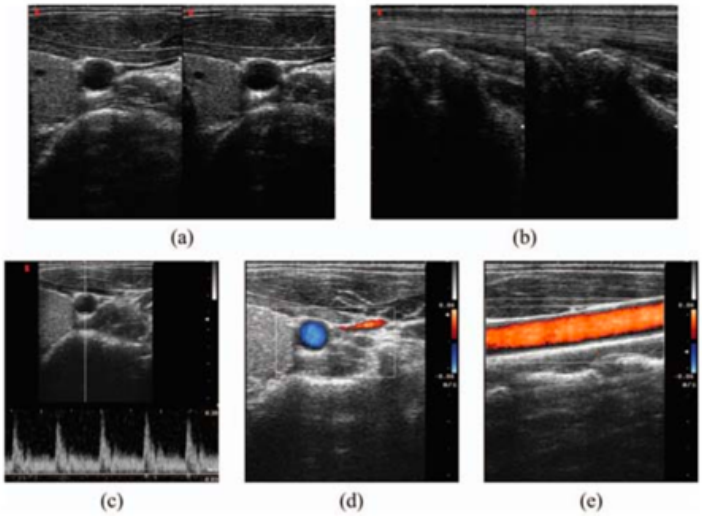


Figure 2-6: In vivo ultrasound images taken with an Esaote Technos imaging system set to a 13-MHz preset. (a) B-mode image of the carotid artery and (b) the forearm tendon, both shown with (left) a CMUT probe and (right) an Esaote LA435 piezoelectric thick-film transducer probe. (c) Pulsed wave (PW) Doppler and (d) and (e) color Doppler images of the same carotid artery. All images are displayed with a dynamic range of 55 dB. The imaging depth is 31 mm in (b) and 41 mm in (a), (c), (d), and (e) [26], [76] © 2021 IEEE. Used with permission.

To achieve better image resolution, high-frequency transducers are needed, especially for applications like intravascular imaging, ophthalmology, and dermatology, where clear and detailed imaging is crucial. Oralkan et al. developed CMUTs that operate at 30 and 45 MHz in immersion to enhance image quality [54]. This research expanded on their earlier work on high-frequency single-element transducers designed for lab-on-chip applications. The CMUT array was fabricated using a sacrificial micromachining process with Si_3N_4 plates. In their study, they also explored how the fill factor affects the frequency characteristics of CMUT elements. They found that when the fill factor was less than 25%, the fractional bandwidth dropped significantly, falling below 30%. These insights highlight the importance of optimizing design parameters for improved performance in high-resolution imaging [77].

Oralkan et al. also were the first to demonstrate volumetric imaging with CMUT technology. In this study, a 32 × 64 element CMUT array was flip-chip bonded to a glass fan-out chip, making it possible to wire-bond the electrical connections to a PCB. The individual cells were connected to the fan-out chip using through-silicon vias. For transmission, a fixed TX aperture was used without phasing, while dynamic beamforming was applied during reception. The transducer array was tested by imaging a parallel-plate phantom submerged in oil. The results

showed four distinct phantom interfaces, with dimensions that closely matched the actual physical measurements in both azimuth and elevation directions [78]. One of the biggest challenges in volumetric imaging with Two-dimensional (2-D) CMUT arrays is ensuring a reliable connection with the necessary electronics. Wygant et al. tackled this by using flip-chip bonding to integrate a 2-D CMUT array with a custom-designed. They used through-wafer vias to link the CMUT elements to bond pads at the base of the chip, allowing for efficient signal transmission. [58]

Miniaturization has been a major focus in developing CMUTs for catheter-based endoscopic imaging. In these cases, ring arrays are commonly used because they provide image quality similar to a fully populated 2-D array but with fewer transducer elements. The centre of the ring array can also be designed for multiple purposes, such as accommodating biopsy tools or optical fibres for photoacoustic imaging, making it a versatile option for medical applications [79]. The first prototype of a forward-viewing annular array for volumetric imaging was developed by Demirci et al. [80] and Oralkan et al. [81] This design featured a 64-element annular array with an inner diameter of 1.38 mm and an outer diameter of 2.56 mm. These devices were created using a surface micromachining technique and had a frequency range of 5–26 MHz, achieving 135% fractional bandwidth. However, one of the main challenges was the high parasitic capacitance caused by the bond pads, which could be reduced by incorporating through-wafer interconnects. Three-dimensional (3-D volumetric imaging using these annular arrays was later demonstrated by Yeh et al. [82]. The ring arrays were integrated with a custom-designed circuit, which helped minimize the impact of parasitic capacitance.

When synthetic phased array volumetric imaging was performed in an oil medium, the resulting 3-D images of metal structures were clear and well-defined. Building on this progress, the first fully integrated intravascular catheter using a CMUT ring array was later developed by Nikoozadeh et al. This 64-element CMUT ring array was connected to a custom-made IC using a flexible PCB. The IC was designed with built-in preamplifiers, protection circuitry, and a ±50 V bipolar pulse generator. The catheter was fully integrated with a real-time imaging platform, and its performance was tested by capturing images of metallic springs [83]. Figure 2-7 provides an image of the completed catheter.

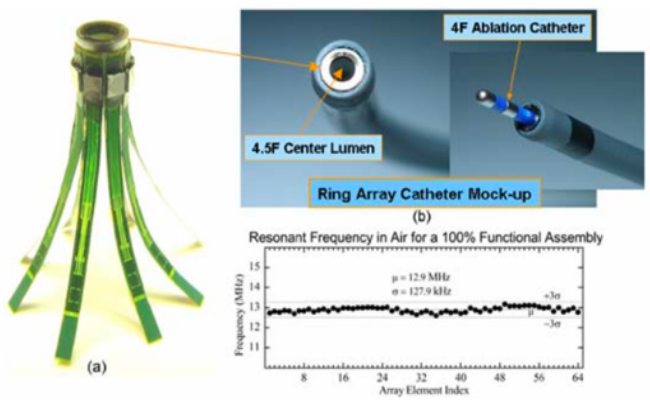


Figure 2-7:(a) A photo of a fully assembled ring, ready to be attached to a catheter. (b) An example of how the CMUT array is integrated with the catheter shaft. (c) Resonant frequencies of all 64 elements in the ring array when measured in air [84], © 2013 IEEE. Used with permission.

Building on this work, the same research team developed a more advanced quad-ring CMUT array with 512 elements for endoscopic and photoacoustic imaging applications [84]. The volumetric imaging capability of this ring array was demonstrated by successfully capturing images of nylon wire and metal ring phantoms. It also proved to be effective for photoacoustic imaging.

Zahorian et al. developed CMUT ring arrays on custom-designed CMOS circuitry, reducing parasitic capacitance by a factor of 200. This improvement led to a stronger SNR and better image quality. A 15-MHz CMUT ring array was fabricated on CMOS circuitry using a modified low-temperature surface micromachining process. The functionality of the CMUT-on-CMOS chip was successfully tested, and the SNR was reported to be sufficient to produce high-quality images [59].

Ultrasound transducers used in photoacoustic imaging need to have high sensitivity and wide bandwidth, and offer high axial and lateral resolution, while remaining unaffected by laser excitation. CMUTs can be designed to meet these requirements, making them compatible with photoacoustic imaging [85]. Vaithilingam et al. developed a 2-D CMUT array with integrated electronics specifically for three-dimensional photoacoustic imaging. This array, operating at 3.48 MHz with 16 × 16 elements, was created using the sacrificial release method and was flip-chip bonded onto a custom-made integrated circuit [69].

In a related development, Chen et al. designed an infrared-transparent CMUT array for photoacoustic imaging. The infrared transparency made it possible to integrate the infrared source directly beneath the array. This cascading approach enabled the development of a compact photoacoustic imaging head while ensuring more uniform illumination [86]. Chee et al. introduced a top orthogonal to bottom electrode (TOBE) architecture for a 2-D CMUT array

designed for volumetric photoacoustic imaging. The TOBE CMUTs were structured so that an entire column of data could be read simultaneously, requiring only N laser pulses and N receive channels for an N × N array. This design allows for high-resolution photoacoustic imaging while reducing hardware complexity [87]. Additionally, a multifrequency CMUT array was proposed for photoacoustic imaging. This design included interlaced low-frequency (1.74 MHz) and high-frequency (5.04 MHz) CMUTs, enabling wideband imaging. The square-shaped CMUTs were fabricated using surface micromachining, with Si_3N_4 as the plate material [88].

2.5 Fabrication process of CMUTs

Early capacitive ultrasonic transducers were made using traditional machining methods, where a rough metal surface served as the capacitor's back plate and a metallized mylar membrane acted as the top electrode [89]. As technology improved, micromachining techniques replaced conventional machining, allowing for the more precise formation of cavities on silicon substrates, leading to better performance and reliability [90], [91]. CMUTs are now mainly produced using two techniques, sacrificial release and wafer bonding, that offer different advantages in fabrication and performance [92] as will be explained in the following sections.

2.5.1 Wafer Bonding Method

The wafer-bonding method involves making the top and bottom parts separately, where the cavity and membrane are formed on different wafers before being bonded together, allowing for more flexibility in design [93]. In this process, the membrane wafer is attached to the cavity wafer, and the membrane is later separated from its original substrate [94], [95]. Wafer bonding techniques are typically grouped into direct bonding, anodic bonding, and polymer adhesive bonding. While each method has its own approach, they all ensure precise control over the cell's geometric dimensions [96]. Because the moving plate is made from single-crystal silicon, these cells have better mechanical properties than those using thin-film-deposited materials. They are thus less prone to internal defects and stress, which helps reduce mechanical loss [97].

Direct wafer bonding

In direct wafer bonding, the wafers are fused together through strong covalent bonds that develop at high temperatures [97]. An example of a direct wafer bonding process is illustrated in Figure 2-8.

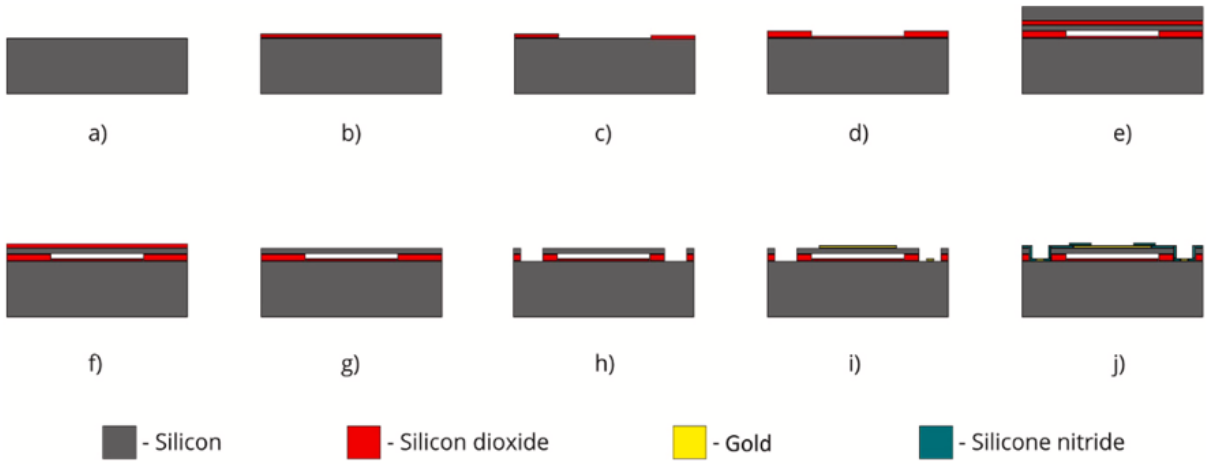


Figure 2-8: Steps of the direct wafer bonding: (a) preparing the prime wafer; (b) creating tiny support pillars through thermal oxidation; (c) etching to form a cavity; (d) adding an insulation layer using thermal oxidation; (e) bonding the wafers together; (f) handling wafer removal; (g) stripping away the oxide layer; (h) revealing the bottom wafer; (i) top electrode deposition; (j) applying a protective passivation layer [97], © 2024 Elsevier. Used with permission.

The wafer-bonding process starts with preparing a prime silicon wafer, ensuring it has the right doping levels for the desired resistance and minimizing depletion when bonding with a silicon-on-insulator (SOI) wafer [98], [99]. Thermal oxidation sets the cell height, followed by lithographic patterning and etching to create the gap. A second oxidation step adds an insulating layer to prevent electrode shorting, requiring high-quality oxidation to reduce the risk of charging and ion drift [98]. The bond between the prime and Silicon on insulator (SOI) wafer plays a crucial role in performance, relying on a smooth surface, which can be improved by using high-quality wafers or applying chemical mechanical polishing (CMP). In a vacuum environment, the wafers first adhere through weak Van der Waals forces before forming strong covalent bonds at high temperatures (800–1100°C) through thermal oxidation. Once the bonding is complete, the handling wafer and oxide layer are removed and wet etching with potassium hydroxide (KOH) or tetramethylammonium hydroxide (TMAH) is used to shape the silicon layer. The buried oxide (BOX) layer is removed using hydrofluoric acid (HF), and the final steps include etching vias, depositing electrodes, and optionally adding an insulating layer to prevent short circuits. A variation of this method, SiN-SiN bonding, creates an insulating membrane that helps reduce parasitic capacitance and allows for better optimization of electrode size, improving transduction efficiency [100]. Silicon membranes are still commonly used because SiN bonding requires a more complex CMP process [101].

Wafer bonding offers several benefits, such as greater flexibility in fill factor, uniform cavity formation, and precise gap height control, making it possible to achieve gaps smaller than 100 nm. Additionally, single-crystal membranes have well-defined properties, ensuring consistent

performance in centre frequency, bandwidth, and collapse voltage [102]. While this method has many advantages, it involves extensive wafer preparation, which can be expensive and may cause performance variations due to differences in wafer thickness. To address these challenges, several improvements have been made, including simplifying the fabrication process [22], reducing the number of masks required [103], preventing dielectric charging [104], managing temperature effects [105], [106], and incorporating transparent or flexible materials for enhanced functionality [85]. A common improvement is using SOI wafers with thick BOX layers, which help keep the electric field confined to the evacuated gap. This approach reduces ion drift and dielectric charging, which can lead to hysteresis and long-term voltage instability [72].

Anodic wafer bonding

Anodic wafer bonding works by applying a strong electrostatic field along with heat to bond alkali-containing glass to a silicon wafer. In this process, the silicon wafer acts as the anode, and the electrostatic field pulls it closer to the glass, gradually reducing the gap between them. When the silicon surface is pulled strongly enough toward the cation-depleted layer, it forms Si-O-Si bonds, creating a permanent bond. It is also possible to join two silicon wafers using a thin layer of glass, which needs to contain around 3% alkali metals like sodium or potassium to allow positive ion movement. Pyrex [107], [108] and Tempax glass [109] are commonly used for this type of anodic wafer bonding. Figure 2-9 provides an illustration of the process.

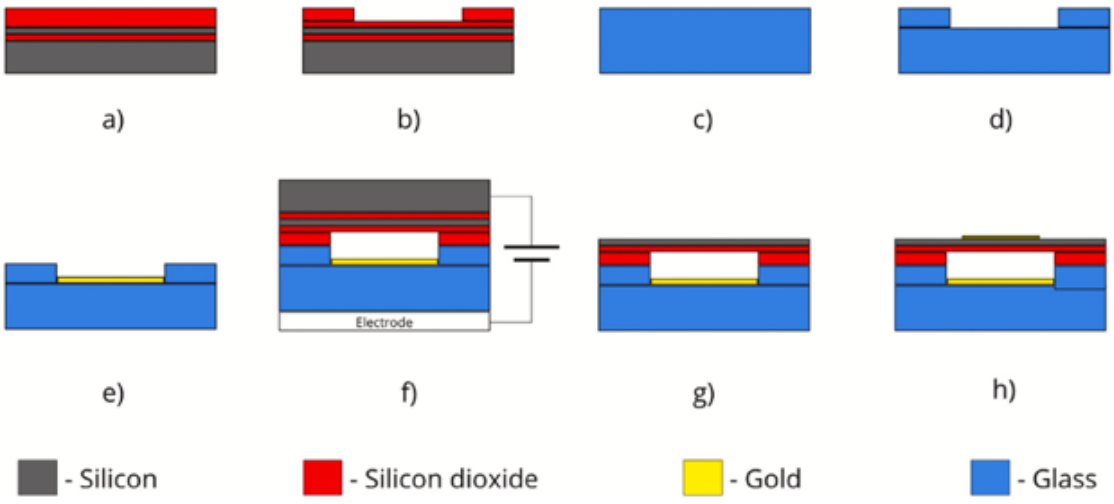


Figure 2-9: Steps of the anodic wafer bonding: (a) getting the prime wafer ready; (b) creating support pillars on the prime wafer using thermal oxidation; (c) preparing the glass wafer; (d) making pillars on the glass through thermal oxidation; (e) bottom electrode deposition; (f) bonding the wafers together using a high DC voltage; (g) handling layer removal; (h) top electrode deposition [97] , © 2024 Elsevier. Used with permission.

Anodic wafer bonding is beneficial because it requires less time to form a bond [108] and can create a strong connection without needing extremely high temperatures [107]. However, some studies suggest that the temperatures used in this process can be similar to those in direct wafer bonding [109]. This method makes bonding easier by reducing the need for a highly polished surface. However, it comes with challenges like higher costs, limited material options, and difficulties in ensuring strong insulation. Since glass is not conductive, an additional insulating layer is needed for the bottom electrode [110].

Polymer adhesive wafer bonding

Polymer-adhesive wafer bonding joins the top and bottom plates using polymer layers such as polymethyl methacrylate (PMMA), benzocyclo-butane (BCB), polydimethylsiloxane (PDMS), or polyimide for a reliable connection [97]. The process is illustrated in Figure 2-10:

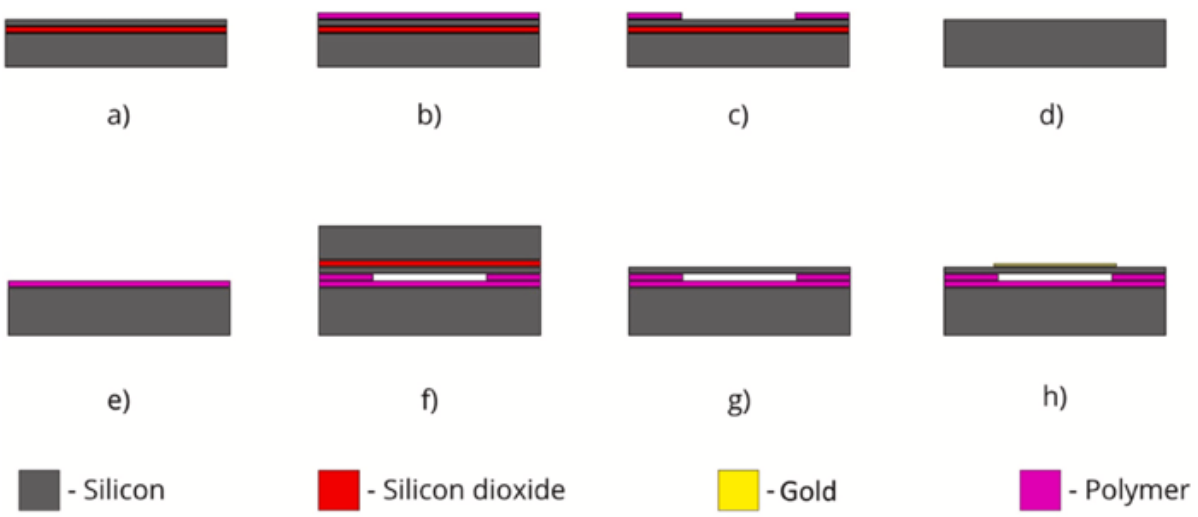


Figure 2-10: Steps of the polymer adhesive wafer bonding: (a) getting the top wafer ready; (b) applying a polymer layer on the top wafer and letting it solidify; (c) etching to create a cavity; (d) getting the prime wafer ready; (e) applying and solidifying a polymer layer on the prime wafer; (f) bonding the wafers together using polymer adhesive; (g) handling layer removal; (h) top electrode deposition [97], © 2024 Elsevier. Used with permission.

The wafers are first coated with a liquid polymer, which is then solidified. The polymer's properties depend on coating thickness and curing temperature. A strong bond forms when the wafers are pressed together with heat and pressure, ensuring full polymerization. Liquid-phase polymers improve bonding by maximizing bonding area, reducing stress, and resisting contamination. This method also works at lower temperatures, usually below 400°C, making it more efficient and reliable. However, polymer adhesives can weaken under high temperatures and certain chemicals, risking adhesion loss or deformation. Selecting the right polymer is essential to ensure stability during fabrication. Polymer layers are well-suited for

photoacoustic applications due to their transparency, which can reach 70% with minimal metallization impact [111].

2.5.2 Sacrificial Release Method

Since CMUTs were first developed in 1994, the sacrificial release method has been commonly used for their fabrication. Instead of directly forming a cavity, a temporary sacrificial layer is patterned and later removed after the top layers are added [97]. This approach makes it possible to create complex microstructures, including sensors [112], microfluidic devices [113], and flexible, stretchable electronics [114].

The process usually involves techniques like thin film deposition, photolithography, and thin film etching [115], [116]. The temperature used during fabrication is crucial, as it determines whether CMUTs can be integrated with electronics on the same wafer, categorizing them as either low- or high-temperature processes. When CMUTs are manufactured on the same silicon substrate as CMOS electronics, the process temperature must stay below 400°C giving a CMOS-compatible processes, while those that require higher temperatures are simply called high-temperature processes [92].

This method offers a faster release process than traditional wet etching [117] and can safely release delicate structures without manual intervention [118]. It has been successfully used with different materials, including metals [106], polymers [118], [119], and semiconductors such as germanium [120]. Recent advancements have made it even more effective, for example by embedding sacrificial layers to create thinner insulation and improve sensitivity [6], using ashing-assisted polysilicon release for better fabrication [121], and applying stress control techniques to enhance stability [122]. These approaches help tackle key challenges like ensuring membrane uniformity, minimizing stiction, and managing stress. They have also made it possible to create embossed CMUTs [123], 2D arrays on insulating substrates with through-wafer interconnects [115], and 3D imaging CMUT arrays with TOBE electrode configuration for improved performance [116]. While wafer bonding offers better control and higher yield during fabrication [92], the sacrificial release method remains a popular choice due to its compatibility with CMOS technology [124] and its ability to work with different substrates [115] making it suitable for a wide range of applications.

Different versions of the sacrificial release process have been developed, all based on the same core idea. A sacrificial layer is first added to the carrier substrate to create the cavity beneath the membrane. After the membrane is deposited, a specific etchant is used to remove the

sacrificial layer without affecting the membrane material. Various combinations of sacrificial layers, membranes, and substrates can be used to fabricate CMUTs. While the overall process stays the same, the choice of materials plays a key role in shaping the design, process control, and overall device performance [92]. A standard version of the sacrificial release process is shown in Figure 2-11.

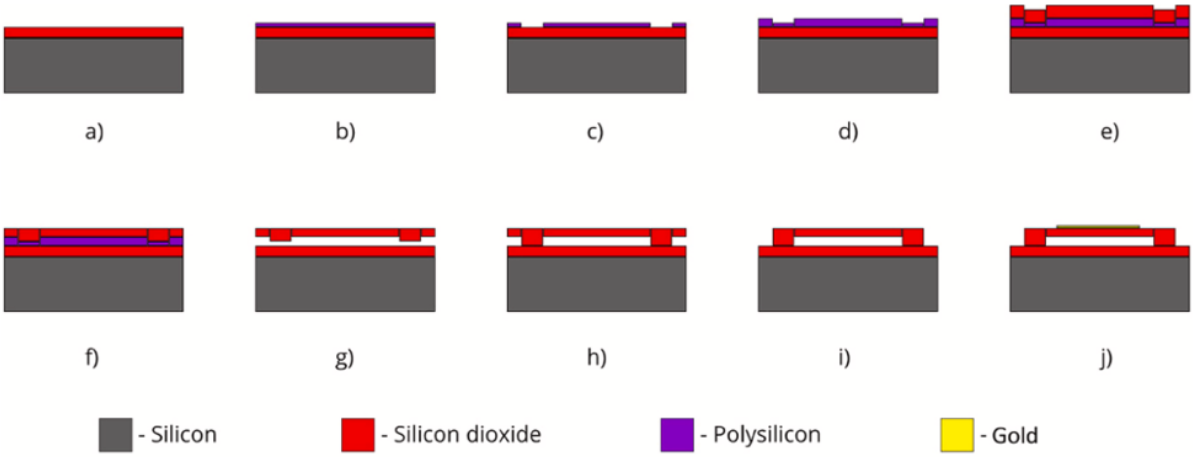


Figure 2-11: Sacrificial Release Process: (a) An insulator layer is deposited. (b) A polysilicon sacrificial layer is added. (c) Insulator pillars are formed. (d) A membrane layer is deposited. (e) The pillar is etched to create a channel to the sacrificial layer. f) The sacrificial layer is etched away. (g) The cavity is sealed by depositing an insulator using LPCVD. (h) A top electrode layer is deposited. (i) The bottom wafer is exposed. (j) The final top electrode layer is deposited [97], © 2024 Elsevier. Used with permission.

First, an insulating layer (SiO_2) is placed on the substrate, followed by a sacrificial polysilicon sacrificial layer which is patterned to define the post area between cells that helps shape the membrane [49]. To create an open cavity, small channels are etched either through the membrane or the supporting pillars. If the channels are made through the membrane, the cell remains unsealed. This unsealed design can be intentional, especially for Helmholtz structural CMUTs, which are designed to enhance the - 3 dB fractional bandwidth. Helmholtz structural CMUTs are a unique type designed to boost bandwidth and output pressure by combining squeeze film effects with Helmholtz resonance [125]. Unlike traditional CMUTs, they have open cavities with acoustic ports, making them especially effective for air-coupled applications where sound needs to travel efficiently through the air [126].

To seal the cell, a technique called LPCVD can be used [127]. By removing air from the cavity, the system's quality factor (Q) improves, though it also slightly reduces the cell's stiffness, leading to lower natural frequencies. Once the sacrificial layer is fully removed, the top electrode and its connections are added. One challenge with the sacrificial release process is that residual stress in the deposited layers can sometimes cause the membrane to crack when

released, potentially affecting the device's performance [92]. This issue can be prevented by using an insulating layer with low residual tensile stress less than 50 MPa.

One critical part of the sacrificial release process is to avoid stiction during the drying process after removing the sacrificial layer [124]. Stiction happens when tiny parts of a device stick together and, in CMUTs, this means the membrane attaching to the substrate electrode. The chances of this happening depend on factors like the size and thickness of the plate, the gap height, and the type of rinsing solution used. Choosing a liquid with low surface tension can help reduce adhesion and prevent stiction during the drying process after wet release [128].

Achieving a consistent gap during the sacrificial release process can be difficult. It mainly depends on the precision of deposition of the sacrificial layer (Fig. 2.11b) and how accurately the pillars are placed (Fig. 2.11c). Another important factor is the precision of etching of the sacrificial layer (Fig. 2.11f). Any inconsistencies in these steps can cause the final product to differ from its intended design. If the etching process is not done correctly, it can create extra stress in the moving plate, which can significantly affect how the transducer vibrates. Another challenge is that the release holes can only be a few microns in size, which limits the fill factor—the proportion of the CMUT area compared to the total aperture area. A smaller fill factor means lower output power, which reduces sensitivity and hence SNR.

A big advantage of the sacrificial release process is that it works at temperatures below 250°C, which helps reduce leftover stress after cooling. It is also a well-developed, simple, and reliable technique. However, finding the right balance between manufacturing efficiency, device performance, process control, and consistency is key. [97] Even though the sacrificial release process was the first commercially successful method, it still has not reached its full potential, especially compared to newer techniques. Recent research shows that using polymer-based CMUTs has made the process simpler and easier to control [73]. Polymers are also being explored as substrate materials for flexible devices because they offer excellent chemical resistance, thermal stability, mechanical flexibility, and biocompatibility [129], [130]. Another study [131] focused on developing fabrication guidelines for polymer-based CMUTs, using experimental results to help reduce the ongoing issue of high cross-talk between cells. The sacrificial release method can also be more difficult to achieve uniformity with compared to wafer bonding [49].

Despite its challenges, the sacrificial release process comes with several key benefits. It is a simple and reliable method that helps avoid the yield issues often seen with wafer bonding.

Moreover, it can be designed to work at processing temperatures around 250°C [132], making it an attractive option for post-processing integration with CMOS technology [59].

Vias and 2D Arrays

The sacrificial release process can be modified by adding extra steps to create electrical connections from the backside using through-wafer vias [58, p. 2], [133]. A device that follows this approach, based on the work of Moini et al. [134], is shown in Figure 2-12 (a).

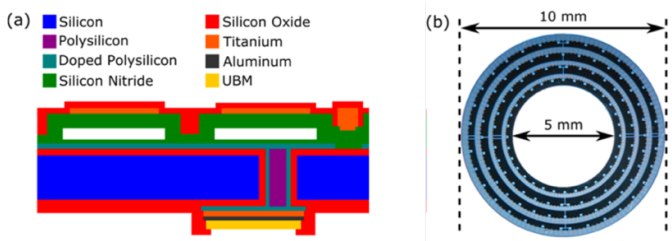


Figure 2-12: a) A sacrificial release CMUT design that includes vias for electrical connections on the backside. (b) A four-ring 2D CMUT array created using the sacrificial release process and through-wafer vias, as explained in [135], © 2016 IEEE. Used with permission.

To create vias, deep reactive ion etching (DRIE) is used to make holes through the wafer. These holes are then coated with conductive silicon and filled with undoped polysilicon. The bottom electrodes of the CMUTs are also made using conductive polysilicon. This approach makes it possible to build 2D arrays with electrical connections on the backside, like the ring array shown in Figure 2-12 (b) With backside electrical contacts, 2D arrays can be built with individually controllable elements. Some designs include rectangular 2D arrays for volumetric imaging [58] and ring arrays specifically made for forward-looking imaging at the tips of catheters [134].

2.6 Chapter summary

In summary, this chapter offers a comprehensive review of the core principles, advancements, and fabrication methods associated with CMUTs, focusing primarily on their application in medical imaging. It begins by introducing the fundamental concepts of ultrasound and provides an overview of the evolution of micromachined ultrasound devices, clearly distinguishing between PMUTs and CMUTs. The chapter details the electrostatic operating mechanism of CMUTs, emphasizing their advantages such as wide bandwidth, high-frequency performance, CMOS compatibility, and the potential for high-density array integration. These features make CMUTs highly suitable for advanced imaging techniques including IVUS and endoscopic ultrasound. A part of this chapter is dedicated to CMUT fabrication, with a strong focus on the

sacrificial release method. This technique allows for the formation of precise cavity structures and flexible membranes, which are critical for achieving high transduction sensitivity. Additionally, it supports low-temperature processing, essential for protecting CMOS circuitry, and enables batch fabrication and complex 2-D array designs. While there are challenges such as residual stress and membrane fragility, the overall benefits in design flexibility, fabrication control, and system-level integration position the sacrificial release process as a scalable solution for the development of CMUT-based imaging systems in healthcare applications.

Chapter 3: Modelling

3.1 Modelling framework

The meander-shaped design has consistently demonstrated its ability to improve sensor performance, particularly by enhancing sensitivity and ensuring a more linear output. In pressure sensing applications, meander-configured piezoresistors have shown superior responsiveness and accuracy compared to conventional designs [136]. In magnetic field sensors, the meander structure outperformed single-bar designs by offering enhanced soft magnetic characteristics and a higher magnetoimpedance ratio [137]. In CMUTs, carefully optimizing parameters such as membrane shape, venting strategies, and overall geometric design can lead to substantial improvements in bandwidth, sensitivity, and transduction efficiency [138]. This chapter presents the modelling and analysis of geometrically optimized CMUT configurations, with a particular focus on how the integration of meander-shaped designs enhances device sensitivity.

3.2 Analytical Modelling

Analytical modelling is a powerful tool for designing and optimizing compliant meandering structures, particularly in technologies like MEMS and CMUTs. One of its biggest advantages is the ability to quickly and accurately predict how these structures will behave mechanically, without the need for time-consuming simulations or expensive experimental tests [139]. This makes it especially useful in the early design phases, where designers need to experiment with different parameters and make quick adjustments to find the most efficient solutions. Researchers have repeatedly shown that it speeds up the design process while still delivering highly accurate performance prediction, which is why it has become such an essential tool for designing modern MEMS and CMUTs [140].

The design of compliant meanders is primarily influenced by several geometric factors such as amplitude (A), angle (α), length (L), and thickness (t), all of which play an important role in determining axial and bending stiffness. Balakrisnan et al., developed simple analytical equations to assess these effects, and their results were validated through numerical simulations and experimental tests [13]. This study demonstrates that changing the shape and size of meanders can effectively tune the mechanical properties of MEMS devices, allowing designers to find the right balance between flexibility and rigidity. This versatility is especially useful for

creating MEMS springs, flexible electronics, and dielectric elastomer actuators, where getting the perfect mix of stiffness and compliance is essential for both performance and durability.

To build effective datasets for analytical modelling, it is important to include a wide variety of geometric and material parameters to accurately predict how meandering structures will behave under different loads. This means considering not just the main design elements like amplitude and angle but also factors such as material directionality and nonlinear deformation. The analytical models presented in the Balakrisnan et al. study provide a robust framework for generating synthetic data, which can be effectively leveraged to train machine learning models for predicting intricate meander line designs. By comparing these predictions with simulations and real-world experiments, the models become even more accurate, ensuring they work reliably in practical applications [13].

In CMUTs, the electrodes are typically part of the membrane and substrate, and their design can influence the transducer's ability to vibrate effectively. By using compliant meanders, designers can create electrodes that are easier to stretch or compress (low axial stiffness) and can bend more readily in specific directions (adjustable bending stiffness), allowing for improved vibration. This is crucial for enhancing sensitivity, enabling the CMUT to detect weaker ultrasonic signals, which is vital for high-resolution medical imaging.

By combining analytical modelling with smart dataset design, designers can develop predictive algorithms for CMUT performance, helping them explore a wider range of design options more efficiently. In short, merging analytical methods with numerical testing can provide a powerful way to optimize meander shapes, leading to the development of MEMS with improved mechanical performance and functionality.

3.3 Axial Stiffness

Axial stiffness refers to a structure's ability to resist tensile or compressive stress along its length when subjected to a force. When it comes to meandered beams, this stiffness is affected by factors such as amplitude, horizontal length, and meander angle. A straight beam has the highest axial stiffness, meaning it offers the greatest resistance to deformation along its axis. However, introducing meandering significantly reduces axial stiffness, increasing flexibility [13]. This reduced stiffness enhances the responsiveness of CMUT electrodes to ultrasonic waves, improving their sensitivity. The mathematical model in the Balakrishnan et al. study accounts for geometric variations, illustrating how increased meandering decreases resistance to axial deformation.

3.4 Bending Stiffness

Bending stiffness refers to how much a structure resists bending when a force is applied perpendicular to its length. It is determined by the material's Young's modulus E and the beam's moment of inertia I. For CMUT electrodes, bending stiffness influences how the membrane moves in response to ultrasonic waves. Meandered designs lower bending stiffness by incorporating flexible sections, allowing for greater deflection while still preserving enough structural strength to prevent excessive deformation.

3.5 Axial and bending stiffness in straight Cantilever beam

For a cantilever beam, the stiffness coefficients k_x (axial stiffness) and k_y (bending stiffness) can be determined by applying Hooke's Law to axial deformation and utilizing Euler-Bernoulli Beam Theory to analyse bending deformation as shown in Figure 3-1.

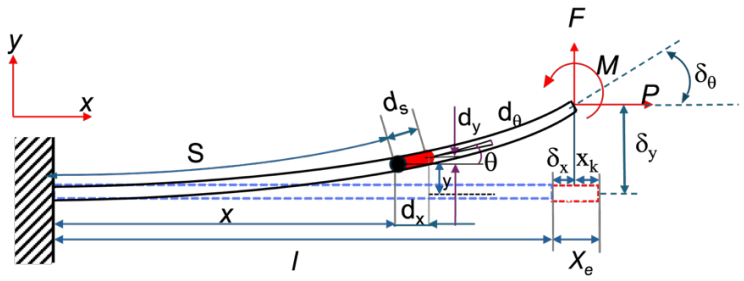


Figure 3-1: Deformation of a cantilever beam under the influence of both an applied end force (F) and an external moment (M).

3.5.1 Axial Stiffness – Hooke's Law

Axial stiffness quantifies the beam's resistance to stretch or compression along its longitudinal axis [13], [141]:

$$F_X = k_X \delta_x \qquad \text{Eq. 3.1}$$

Using Hooke's Law, the axial displacement caused by a force, F_x, acting along the beam's length can be expressed as:

$$\delta_x = \frac{F_x L}{E A_C} \qquad \text{Eq. 3.2}$$

Therefore, the axial stiffness can be defined as:

$$k_x = \frac{E A_C}{L} \qquad \text{Eq. 3.3}$$

where E is Young's modulus, A_C is cross-sectional area of the beam, L is length of beam and δ_x is axial displacement. For a rectangular cross section A_C is equal to:

$$A_C = wt \quad \text{Eq. 3.4}$$

where *w* represents the beam's width and t denotes its thickness. Thus, k_x can be expressed as:

$$k_x = \frac{Ewt}{L} \ (N/m) \quad \text{Eq. 3.5}$$

3.5.2 Bending Stiffness – Euler-Bernoulli Beam Theory

Bending stiffness refers to a cantilever beam's resistance to bending when a force, F_y, is applied perpendicular to its length at the free end. The resulting deflection at the tip can be determined using Eq. 2.6 [13], [141]:

$$\delta_y = \frac{F_y L^3}{3 E I} \quad \text{Eq. 3.6}$$

As a result, the bending stiffness can be defined as:

$$k_y = \frac{3EI}{L^3} \quad \text{Eq. 3.7}$$

Since $I = \frac{w \times t^3}{12}$ is the second moment of area for a rectangular beam (width = *w*, thickness = *t*)

$$k_y = \frac{3Ewt^3}{12L^3} = \frac{Ewt^3}{4\,L^3} \ (\text{N/m}) \quad \text{Eq. 3.8}$$

Validation of Analytical Modelling:

The analytical expressions for axial and bending stiffness have been verified through FEM simulations, as reported in the study by Balakrishnan et al [13]. As illustrated in Figures 3-2 (a) and 3-2 (b), the FEM and analytical results exhibit excellent agreement, validating the robustness of the implemented models.

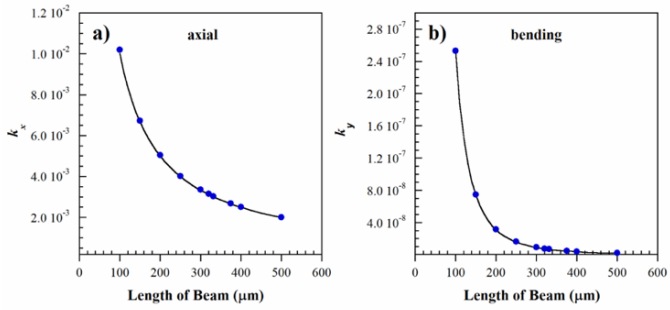


Figure 3-2: Evaluation of stiffness as a function of cantilever length, with black lines depicting analytical solutions and blue symbols representing FEM results obtained using Eq. 3.5 and 3.8 for (a) axial stiffness and (b) bending stiffness [13], reproduced with permission from © 2012 IOP Publishing Ltd.

This alignment underscores the reliability of the analytical approach, instilling confidence in its use for more complex geometries, such as meandered beam designs.

3.6 Theory of meander design

Meander paths, such as in-plane zigzags and serpentines or out-of-plane corrugations, are commonly used to reduce the stiffness of mechanical structures. This design approach preserves desired properties, like the high conductivity of metals or the strength of Si, without requiring a lower-modulus material that might compromise performance or fabrication compatibility. A practical example is the use of meandering polysilicon paths in micro-resonators, where they function as springs to tether proof masses [142]. Meandering paths and crenelations are frequently utilized to create stretchable metal film electrodes, essential for applications such as tenable capacitors [143], radio frequency (RF) switches [144], and stretchable electronics. These designs are particularly useful in flexible displays [145], stretchable circuits [146], flexible antennas [147] and dielectric elastomer actuators (DEAs) [148]. Patterned metals offer the advantage of being compatible with standard microfabrication processes, unlike certain other compliant electrodes. Metal films are typically deposited onto a compliant substrate, allowing for enhanced flexibility. While single-crystal gold (Au) films have a rupture strain of only 1–1.5% [149], patterning them in-plane enables them to withstand strains of up to 100% without rupturing while maintaining conductivity [150], [151]. This in-plane patterning is generally achieved using photolithography [152], whereas out-of-plane deformations are produced either by surface modelling [153] or by depositing metal onto a stretched substrate, which forms wrinkles upon relaxation[154]. Additionally, the stiffness of crenelated structures has been determined by summing the stiffness of individual segments in parallel or series using the cantilever stiffness equation [143], [155].

The traditional method of summing individual segment stiffness in parallel or series can lead to inaccuracies due to the neglect of segment interactions, potentially misestimating overall stiffness [144]. A closed-form analytical solution has been developed for a rectangular crenelated cantilever with guided-end boundary conditions [142]. Numerical simulations have been conducted for specific geometries, including rectangular, trapezoidal, and sinusoidal shapes, under different boundary conditions such as fixed-fixed and fixed-guided [142], [144], [156]. However, extending these findings to other geometries necessitates further simulations. While stiffness analyses of certain crenelated structures have been explored through analytical [142], numerically [156], [157] and experimental approaches, a comprehensive design guide that examines the influence of meander shape on stiffness is still lacking.

To assess the impact of design parameters, the Balakrisnan's study determines the axial and bending stiffness of meandering cantilevered structures based on their geometry Figure 3-3.

Stiffness, represented by the spring constant k, was calculated from the force required to produce a unit displacement, or vice versa. The fundamental unit of the beam structures, Figure 3-3 (b), consists of two sides of a trapezoid, as illustrated in Figure 3-3 (a). The primary variables examined include the tilt angle, α, measured from the horizontal, the amplitude, A, and the length of the horizontal segment, H. When $\alpha = 90^{o}$, the structure forms a square wave by repeating these units, while setting $H = 0$ results in a triangular wave pattern. Simplified analytical models based on classical beam theory provide accurate estimations of axial and bending stiffness, closely matching numerical simulations and experimental results. These models offer a reliable and efficient alternative to FEM for stiffness approximation across different geometries [13].

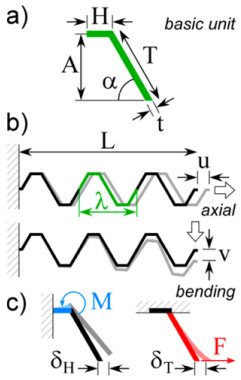


Figure 3-3: Parameters describing beam geometry. (b) A trapezoidal representation of the 3-period beams utilized in the Balakrisnan's study, showing the fixed-free boundary conditions along with the axial and bending displacements. (c) A schematic depiction of the main deformations occurring in the horizontal (blue) and inclined (red) segments of the basic unit during axial elongation [13], reproduced with permission from © 2012 IOP Publishing Ltd.

The first parameter which was modified was the tilt angle (α). The results indicate that as α increases, both axial and bending stiffness decrease. In fact, the axial stiffness, k_x, decreases by a factor of 4, and the bending stiffness k_y, decreases by a factor of 2 when α changes from 45° to 120°. Next, the amplitude, A, was varied for a rectangular crenelation while keeping α fixed at 90°. In this case, the axial stiffness decreases markedly with increasing crenelation height, following a $1/A^3$ trend, whereas k_y is less affected, decreasing roughly in proportion to $1/A$. Moreover, adding horizontal segments at the vertical centre does not change the axial stiffness; however, if these segments are placed away from the centre, k_x decreases. The bending stiffness is influenced by the overall length of the structure rather than the vertical positioning of additional horizontal segments. Additional numerical simulations were conducted to explore a more complex scenario involving a thin film placed on top of an out-of-plane corrugated elastomer with varying thickness [13].

These types of structures are commonly observed in compliant electrodes [153] and dielectric elastomer actuators [153], [158]. The results show that for this "filled" structure, when $2A = 0$, meaning there is no crenelation, its axial stiffness is approximately equal to that of the metal film. As the crenelation amplitude increases, the axial stiffness decreases dramatically by several orders of magnitude until it eventually reaches the stiffness of the elastomer. The bending stiffness of the filled structure when $2A = 0$ is already nearly equal to that of the elastomer alone. As the crenelation amplitude increases, the bending stiffness rises slightly at first, reaches a peak, and then gradually decreases until it stabilizes at the elastomer stiffness. This indicates that crenelation has only a small impact on bending stiffness. However, if crenelation is incorporated, it is important to carefully design its parameters to achieve the desired stiffness value [13].

3.6.1 Analytical Estimation of Axial Stiffness

To approximate the axial stiffness of the trapezoidal beams, the deflection of a single unit, as illustrated in Figure 3-4 (a), was determined using beam theory. The derivations were based on the following assumptions:

- The applied force is small and does not induce plastic deformation.
- The deflections remain small, allowing the use of the small-angle approximation, where $\sin\theta \approx \theta$. The maximum deflection observed in the beams was 10°, and even at 14°, the error from this approximation remains within 1%.
- The beam maintains a consistent thickness t, a uniform width w, and an isotropic, homogeneous modulus E.

The overall deflection was then calculated by multiplying the unit's deflection by the total number of units. In summary, the applied force, F, generates a moment $M = A \times F$ on the horizontal segment of the unit, denoted as H, where A represents the amplitude, or the vertical distance of segment, H, from the centre line, acting as the length of the moment arm. This moment induces bending in H, resulting in a rotation at the vertex connected to the tilted segment ,T, by an angle δ_H [141].

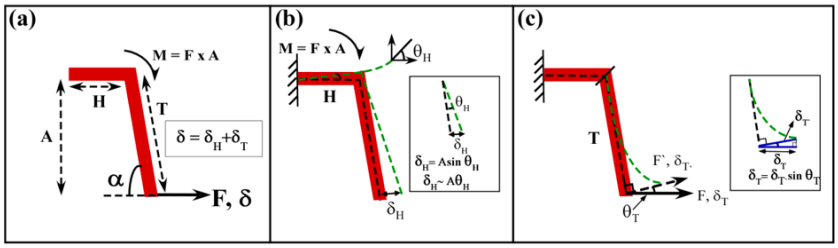


Figure 3-4: (a) The specific unit segment being analysed. (b) Rigid body rotation of the segment resulting from the deformation of segment H. The axial force generates a moment M on H, calculated as force multiplied by

offset, $M = F \times A$, leading to a rigid body rotation of T and causing a deflection, δ_H. (c) Segment T is modelled as a cantilever beam subjected to a point load at its tip, where the axial force induces a deflection δ_T. The overall deflection is determined by summing δ_H and δ_T [13], reproduced with permission from © 2012 IOP Publishing Ltd.

Here, θ_H is expressed in radians, H represents the length of the horizontal segment, E denotes the Young's modulus of the material, and I is the moment of inertia of the segment. The rotation, θ_H, is expressed as [141]:

$$sin\ (\theta_H) \approx \theta_H = \frac{MFH}{EI} = \frac{FAH}{EI} \quad \text{Eq. 3.9}$$

As a result, the tilted segment, T, undergoes rotation, causing the tip of T to deflect by δ_H, Figure 3-4 (c):

$$\delta_H = A\ sin\ (\theta_H) \approx A\theta_H = \frac{FA^2H}{EI} \quad \text{Eq. 3.10}$$

The tilted segment T is considered a cantilever beam with its top end fixed. When a force, F, is applied at the tip of the cantilever, it results in a deflection, δ_T, which is given by [141].

$$\delta_T = \frac{FT^3}{3EI} = sin\ \alpha\ \frac{Fcos\ (\theta_H + 90 - \alpha)\left(\frac{A}{sin\ \alpha}\right)^3}{3EI} \quad \text{Eq. 3.11}$$

Here, T represents the length of the segment T. By adding the two deflections:

$$\delta = \delta_H + \delta_T$$

$$\delta = \frac{FA^2\ H}{EI} + sin\ \alpha\ \frac{Fcos\ (\theta_H + 90 - \alpha)\left(\frac{A}{sin\ \alpha}\right)^3}{3EI} = \frac{FA^2\ H}{EI}\left(H + \frac{Acos\ (\theta_H + 90 - \alpha)}{3(sin\ \alpha)^2}\right) \quad \text{Eq. 3.12}$$

Defining the stiffness as $k_x = F/4n\delta$ where n represents the number of periods in the beam, the axial stiffness can be approximated. Additionally, for a rectangular cross-section, the moment of inertia is given by $I = \frac{wt^3}{12}$ leading to the following expression for the beam's axial stiffness.

$$k_x = \frac{Ewt^3}{48nA^2\left[H + \frac{Acos(\theta_H + 90 - \alpha)}{3(sin\ \alpha)^2}\right]} \quad \text{Eq. 3.13}$$

3.6.2 Analytical Estimation of Bending Stiffness

A more detailed analysis is necessary to obtain an accurate estimate of the bending stiffness, as it involves greater complexity compared to axial stiffness. This complexity arises because the moment arm varies along the length of the beam, depending on the segment's distance from the end, and because certain terms that were previously neglected have a more significant impact in this case. Both force-induced and moment-induced deflections and rotations must be

considered [13]. Figure 3-5 illustrates the different segments and dimensions within the meander.

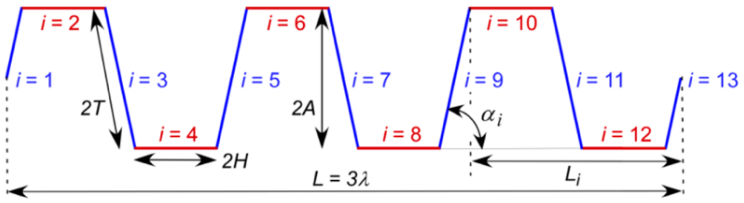


Figure 3-5: A schematic of a meander structure with $n = 3$ periods of length λ, illustrating the segment numbering along with the angle and *moment arm for segment* $i = 9$ [13], reproduced with permission from © 2012 IOP Publishing Ltd.

Prior to applying a force at the tip of the structure, the length of the moment arm for the i^{th} horizontal segment is given by:

$$L_i = L + \left[\frac{A}{tan\ \alpha_i} - \frac{i}{2}\frac{L}{2n}\right], i = \text{even (horizontal segments)} \qquad \text{Eq. 3.14}$$

Here, n represents the number of periods, and since $A = T\cos(\alpha_i - 90)$, the length of the first segment can be expressed as:

$$T\cos(\alpha_i) = A/tan(\alpha_i) \qquad \text{Eq. 3.15}$$

In the following analysis, it is assumed that L_i remains nearly unchanged during bending, which holds true for small deflections. The length of the moment arm for the i^{th} vertical or tilted segment is then given by:

$$L_i = L - \left[\frac{A}{tan\ \alpha_i} + \frac{(i-1)}{2}\frac{L}{2n}\right],\ i = \text{odd (vertical segments)} \qquad \text{Eq. 3.16}$$

except for $i = 13$, where it is zero since the moment at the beam's end is also zero.

The final bending stiffness formula, incorporating the contributions from all units, is derived as follows [13]:

$$\delta = \frac{FT}{EI}\left\{\left[\frac{T^2 cos^2\alpha_1}{3} + LTcos\alpha_1 + L^2\right] + 2\sum_{i=odd,i=3}^{4n-1}\left[\frac{(2T)^2 cos^2\alpha_i}{3} + 2L_i Tcos\alpha_i + {L_i}^2\right]\right\} + \frac{F(2H)}{EI}\sum_{i=even,i=2}^{4n}\left[\frac{(2H)^2}{3} + 2L_i + {L_i}^2\right] \qquad \text{Eq. 3.17}$$

The bending stiffness k_y is then given by:

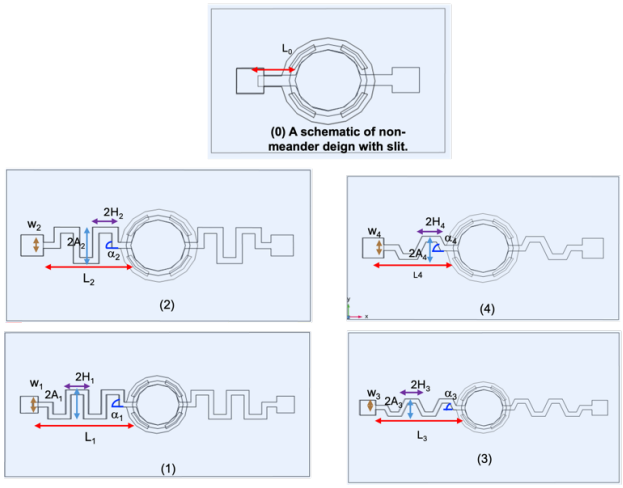
$$ky = \frac{F}{\delta} \qquad \text{Eq. 3.18}$$

The axial and bending stiffnesses of the mask design shown in Figure 3-6 were calculated using MATLAB, with the results presented below in Table 3-1 and Figure 3-7. For CMUT

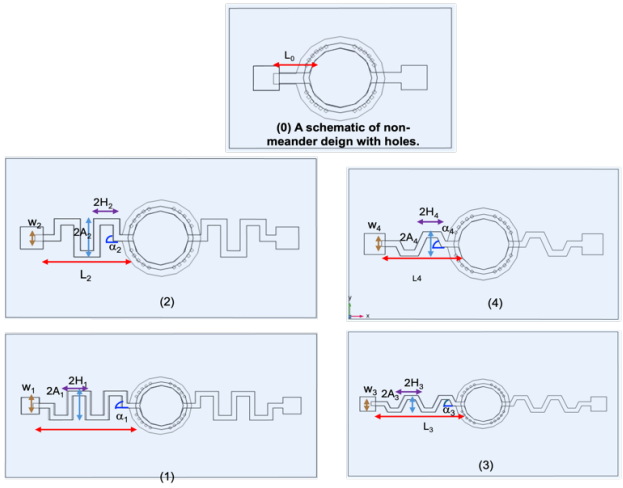
fabrication, Aluminium (Al) (70 nm) and silicon carbide (SiC, 1500 nm) were selected as the materials. Given the negligible thickness of Al compared to SiC, only SiC was considered in the calculations. Literature values for Young's modulus of SiC range from 100 to 400 GPa [159], and for greater structural stability [160], the higher value of $E = 400$ GPa was used, with a thickness of $t = 1500$ nm.

Table 3-1: Dimensions of straight beam (L_0) and meander beams ($L_0 - L_4$).

Dimension of the designs								Axial stiffness (N/m)	Bending Stiffness (N/m)
No.	L_i (m)	α_i (degree)	H_i (m)	A_i (m)	w_i (m)	T_i (m)	n	k_x (N/m)	k_y (N/m)
0	30.00E-05	0	-	-	2.00E-05	-	-	4.00E+04	2.50E-01
1	3.80E-05	90	4.50E-05	6.00E-05	2.00E-05	6.00E-05	2	1.20E+00	9.20E-02
2	2.75E-05	90	4.00E-05	6.00E-05	2.00E-05	6.00E-05	≈1	2.60E+00	2.33E-01
3	3.94E-05	65	3.00E-05	4.00E-05	2.00E-05	4.00E-05	2	3.93E+00	1.17E-01
4	2.44E-05	65	3.00E-05	4.00E-05	2.00E-05	4.00E-05	1	7.86E+00	3.87E-01



(a)



(b)

Figure 3-6: (a) Mask design with slit type release. (b) Mask design with release holes (All dimensions are specified in Table 3-1).

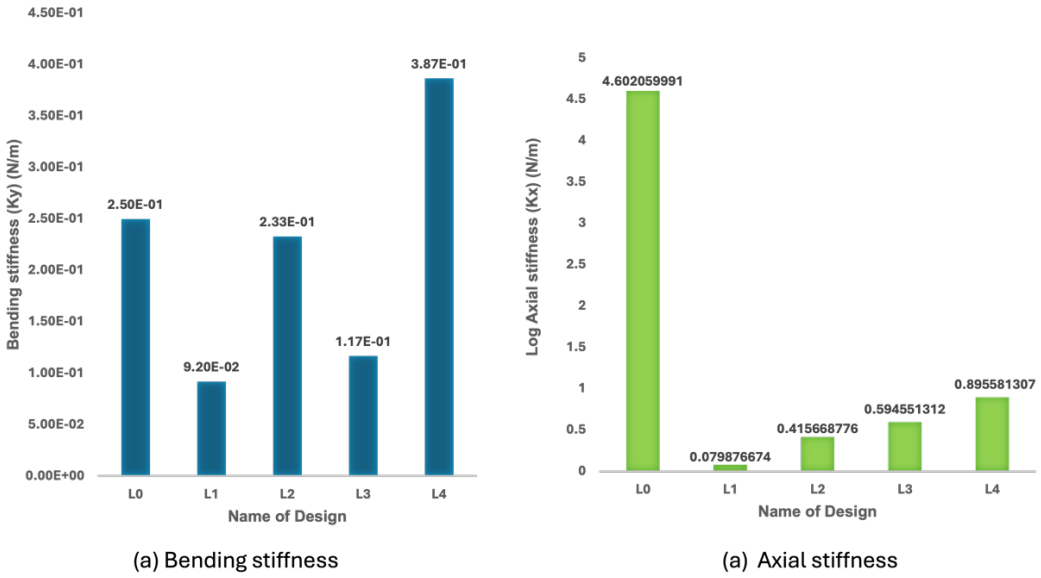


Figure 3-7: (a) Bending stiffness of the straight beam (L_0) and meander beams (L_1 - L_4), (b) Logarithm of Axial stiffness of the straight beam (L_0) and meander beams (L_1 - L_4).

The assessment of k_x and k_y based on the graphs in Figure 3-7 along with Table 3-1, highlights the influence of meander geometry on structural stiffness. The straight beam, L_0, has the highest axial stiffness due to the absence of meandering features, making it significantly more resistant to axial deformation. In contrast, the meander beams, L_1 to L_4, show a notable decrease in axial stiffness, with L_1 having the lowest value, followed by L_2, L_3, and L_4. This pattern indicates that the parameters defining the meander structure, including A, α, H, and L, play a significant role in determining stiffness properties. The meander beam L_1, having the highest amplitude, A_1 = 60 µm, and a tilt angle, α_1 = 90°, exhibits the lowest axial stiffness. This aligns with theoretical expectations, as a larger amplitude and steeper tilt angle lead to greater compliance, allowing more deformation under axial loading. L_2 retains the same amplitude as L_1 but features a reduced height, H_2 = 40 µm, and a shorter length, L_2 = 275 µm, resulting in slightly higher axial stiffness compared to L_1. L_3 and L_4 both have lower amplitudes, A_3 = 40 µm, A_4 = 40 µm, and smaller tilt angles α_3 = 65°, α_4 = 65°, which contribute to a gradual increase in axial stiffness. This confirms that decreasing amplitude and tilt angle enhances axial stiffness by reducing overall compliance.

According to previous research [13], axial stiffness in meander structures decreases as amplitude and tilt angle increase due to the added flexibility introduced by the meander design. The analytical and numerical models of Balakrisnan's study indicate that axial stiffness is inversely proportional to A and decreases as α increases, which aligns with the trends observed in the provided data. The gradual rise in stiffness from L_2 to L_4 follows theoretical expectations,

as reducing both amplitude and tilt angle restricts the deformation of the structure under axial loads. Therefore, this explanation is consistent with the fundamental behaviour of meander structures as described in this study. For k_y, the straight beam, L_0 has a moderate stiffness level, whereas L_1 exhibits the lowest bending stiffness. This reduction in k_y for L_1 is due to its large amplitude, which significantly increases its flexibility in bending. Although L_2 retains the same amplitude as L_1, its lower height and shorter overall length result in a higher bending stiffness, indicating a more rigid response. L_3 and L_4 further increase in bending stiffness, with L_4 reaching the highest value among the meander beams. Despite L_4 having a meandered shape, its shorter overall length plays a dominant role in increasing its bending stiffness. A shorter structure reduces the leverage effect of bending forces, making the beam more resistant to deformation. This trend follows theoretical expectations, where decreasing both the tilt angle and amplitude while maintaining a structured configuration enhances resistance to bending deformation. These findings suggest that k_x is primarily influenced by variations in A and α, whereas k_y depends more on L and H. Generally, straight beams, L_0, exhibit greater axial and bending stiffness than meander beams, $L_1 – L_4$, as their continuous and uninterrupted structure provides higher resistance to deformation. While meander designs with varying A, α, H, and L enhance flexibility and can be optimized to achieve an optimal balance between stiffness and compliance, straight beams remain the more rigid option overall.

The fabrication process which will be explained in the next chapter, begins with the design (1) in Figure 3-6 (a) (L_1 in Figures 3-7), chosen for its lower stiffness, which makes it more flexible and easier to handle during the initial stages of fabrication. Selecting this design helps mitigate the edge bead effect, a common issue in spin-coating processes where excess resist accumulates along the edges of the substrate due to surface tension and centrifugal forces [161]. This effect can lead to non-uniform coating thickness, impacting patterning accuracy and subsequent fabrication steps [162]. By starting with L_1, which has a more flexible structure, these fabrication challenges can be better managed.

Each design includes two structural variations for accessing the sacrificial layer: the slit-type release, Figure 3-6 (a), and the hole-release configurations, Figure 3-6 (b). The primary purpose of these release structures is to facilitate the removal of the sacrificial layer while ensuring the structural integrity of the final device. The slit-type release was selected as the preferred approach as it provides improved structural stability and mechanical robustness, leading to better device performance and reliability [12].

Chapter 4: CMOS-Compatible Fabrication of CMUT

Micro-fabrication processes, including CMUT fabrication, require carefully selected materials and specialized tools to ensure precision, efficiency, and compatibility at each stage. The sacrificial release process discussed in Section 2.5.2, was selected for fabrication due to its compatibility with the chosen material and available tools. This method operates at temperatures below 250°C, reducing residual stress after cooling, and is a well-established, simple, and reliable technique, making it a practical choice for this application. While newer techniques have emerged, it remains widely used due to its ease of implementation and effectiveness in achieving process control and consistency, particularly in polymer-based CMUT fabrication, where advancements have further simplified the process and improved controllability. Despite challenges in achieving uniformity compared to wafer bonding, the sacrificial release method mitigates yield issues commonly encountered in alternative approaches. Furthermore, its lower processing temperature makes it highly suitable for seamless post-processing integration with CMOS technology.

Figure 4-1 presents a comprehensive overview of the CMUT fabrication process, outlining the materials and tools used in this work. The following sections focus on the most frequently used processes—photolithography and lift-off—while a detailed description of all tools and equipment is provided in Appendix A.

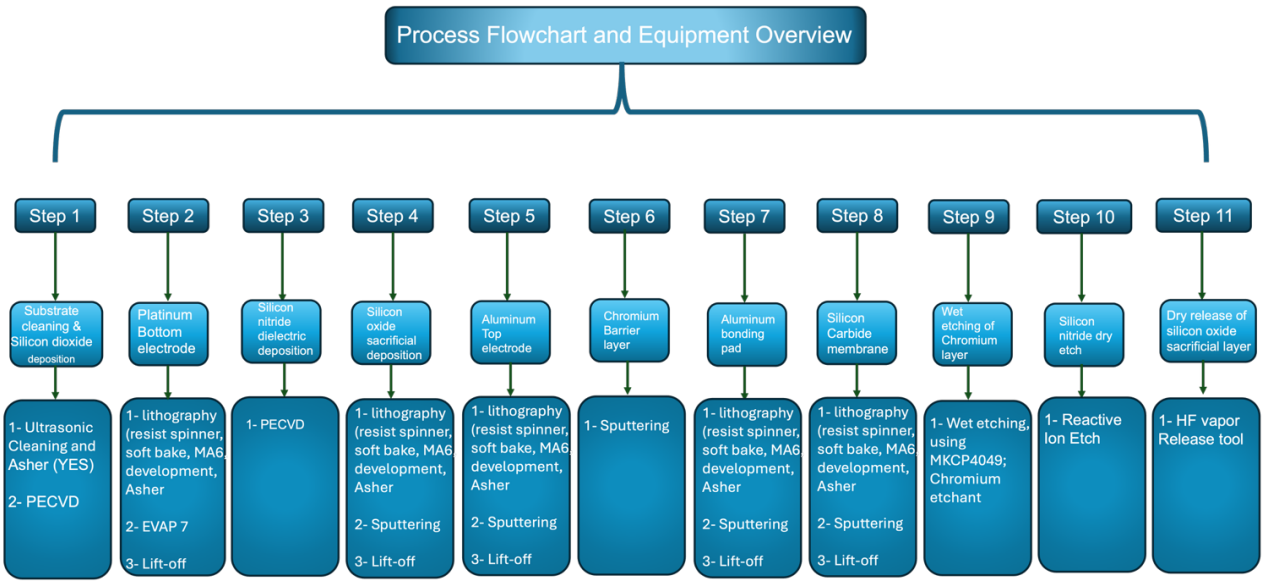


Figure 4-1 : Process flowchart and equipment overview of CMUT fabrication.

4.1 Methods

4.1.1 Photolithography

Photolithography is a fundamental process in microfabrication, allowing for the accurate imprinting of detailed patterns onto a wafer or substrate. Figure 4-2 illustrates this process, which involves a series steps, each contributing to the reliability of the final structures.

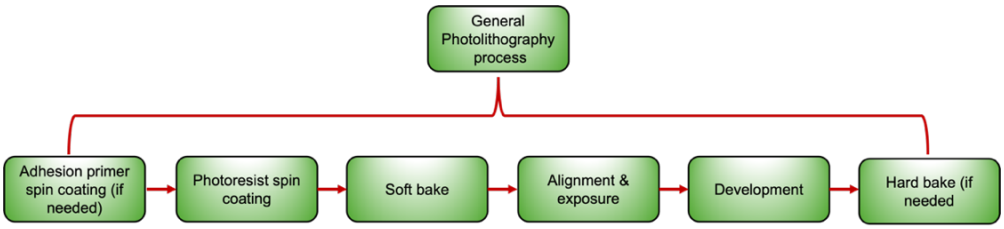


Figure 4-2: General photolithography process flowchart.

Each of these steps is explained in detail in Section A.2.

Role of photomasks in photolithography

In photolithography, a photomask plays a fundamental role in defining patterns on a substrate. It consists of a transparent glass or quartz base with opaque Cr patterns that selectively allow or block light during the exposure process. The interaction between the mask and the positive or negative photoresist, determines the final pattern transferred onto the wafer. Figure 4-3 illustrates the structural design of masks.

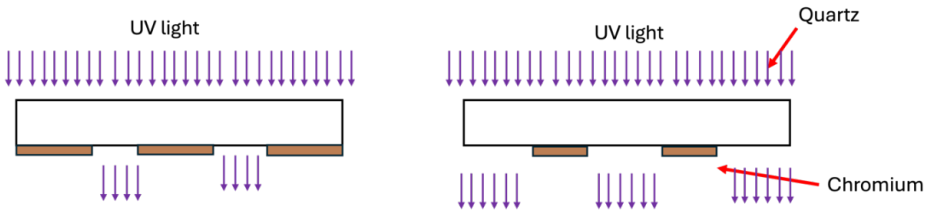


Figure 4-3:Schematic of a photomask structure used in photolithography.

Figure 4-4 presents the mask design for CMUT, developed using COMSOL (COMSOL, Inc, Germany) and L-EDIT (Siemens EDA, USA).

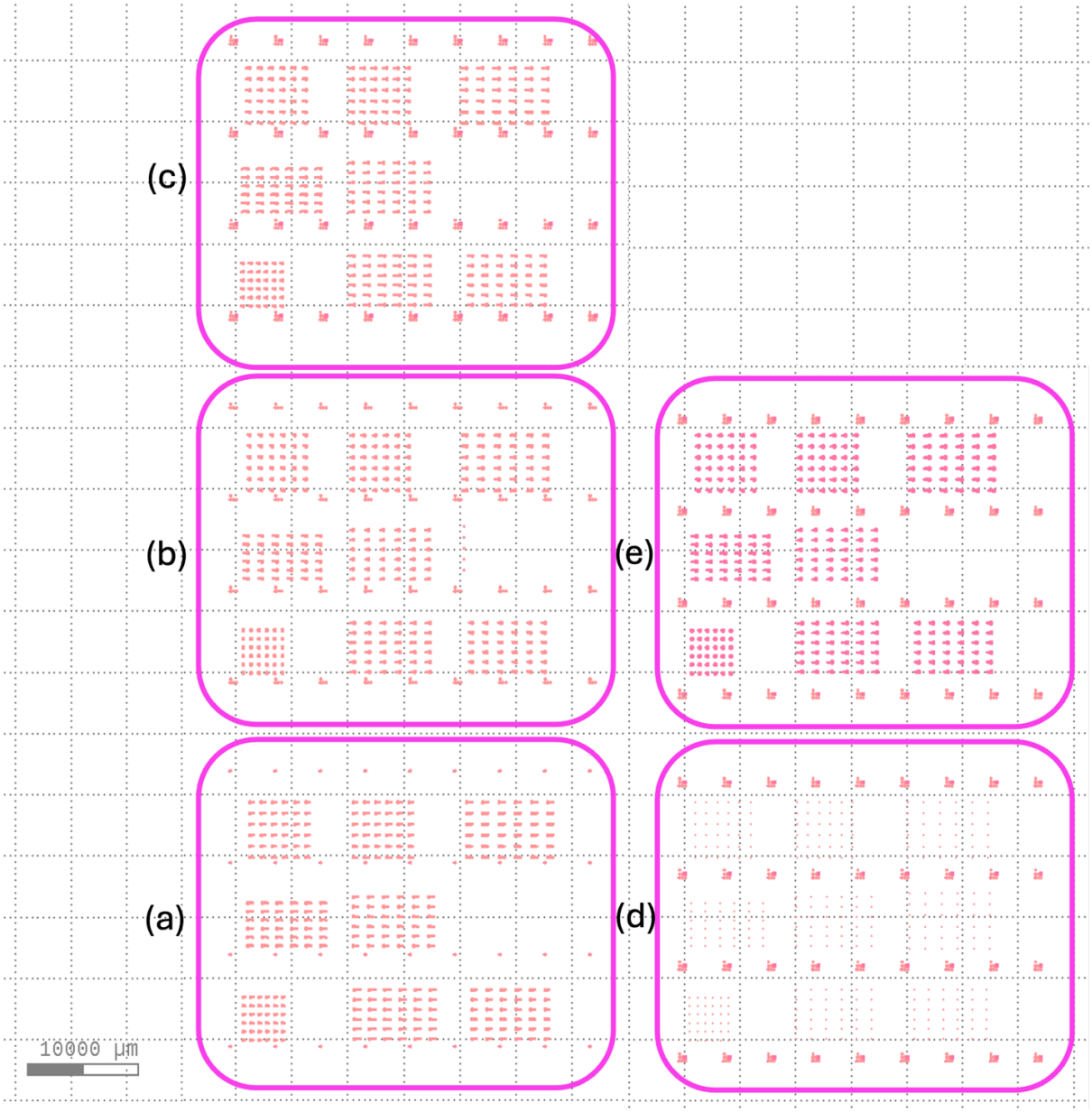


Figure 4-4: L-Edit representation of photomask design used in CMUT microfabrication. (a) Mask No. 1, for bottom electrode deposition. (b) Mask No. 2, for sacrificial layer deposition. (c) Mask No. 3, for top electrode deposition. (d) Mask No. 4, for bonding pad deposition. (e) Mask No.5, for membrane deposition.

Each mask design employed in the CMUT fabrication process is presented in detail in Section 4.3.

Photolithography challenges

During the lithography optimization process, several factors contribute to inconsistencies in the photoresist layer, leading to defects that impact pattern transfer. Issues such as improper spin-coating, uneven solvent evaporation, surface contamination, and poor adhesion between the resist and substrate result in defects like bubbles, peeling, and incomplete pattern formation. Figure 4- 5 shows some of these challenges during this fabrication.

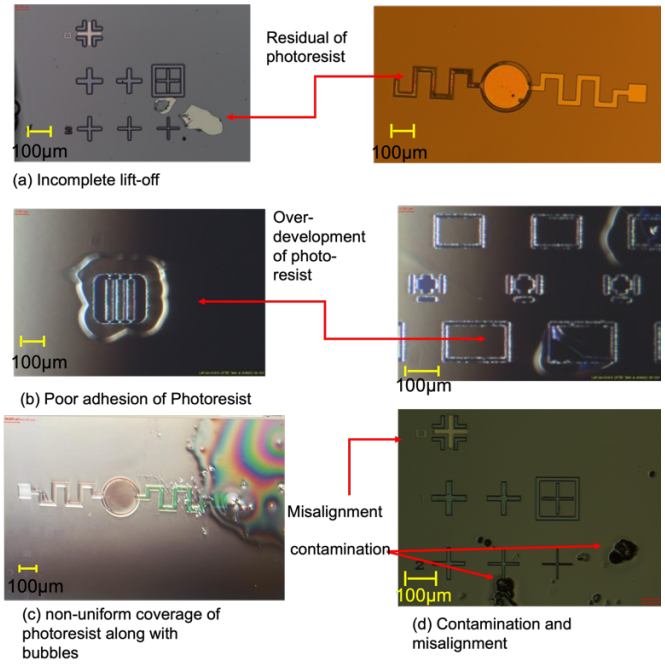


Figure 4-5: Microscopic images illustrating common defects and challenges in the photolithography process: (a) Incomplete lift-off and residual photoresist resulting from insufficient temperature during the lift-off step. (b) Poor photoresist adhesion caused by inadequate surface preparation, contamination, or insufficient baking. (c) Non-uniform photoresist coverage with visible bubbles, attributed to improper spin-coating, surface contamination, or solvent evaporation inconsistencies. (d) Presence of surface contamination and misalignment of alignment markers, leading to inaccurate pattern transfer.

Figure 4-5 (a) illustrates the presence of incomplete lift-off and residual resist on the sample surface. Such issues commonly arise from factors like insufficient development time, a weakened developer solution, or, as in this case, the lift-off temperature. The temperature was increased from 50 °C to 80 °C to resolve the problem. However, the remaining resist can interfere with the lithography process by hindering accurate pattern transfer, which may result in defects during subsequent etching or deposition steps.

Figure 4-5 (b) shows the impact of poor adhesion of the photoresist on the sample, evident from the irregular resist coverage and detachment from the substrate. This issue arises due to inadequate surface preparation, contamination, or insufficient baking, leading to defects such as peeling, incomplete pattern transfer, and edge roughness. Weak adhesion results in unwanted lift-off during development or etching.

Figure 4-5 (c) highlights the challenge of non-uniform photoresist coverage and bubble formation. These issues arise from improper spin-coating, solvent evaporation inconsistencies, or surface contamination, leading to variations in resist thickness and trapped air pockets. Bubbles within the resist create voids, causing incomplete exposure and development.

Figure 4-3(d) highlights the challenges of contamination and misalignment, both of which significantly affect pattern accuracy. Contaminants such as particles and residues can disrupt

the interaction between the photomask and substrate, hindering precise pattern transfer during exposure.

Addressing these challenges requires careful optimization of process parameters. This includes refining spin speed, exposure settings, development and baking conditions. Additionally, improving resist handling, substrate cleaning, and using adhesion promoters contribute to better uniformity and pattern fidelity. Maintaining a controlled, clean environment and employing degassing techniques—such as vacuum or ultrasonic methods—further minimize defects.

4.1.2 Etching

The etching process, Figure 4-6, in microfabrication, follows a structured sequence of steps to achieve precise patterning on the substrate.

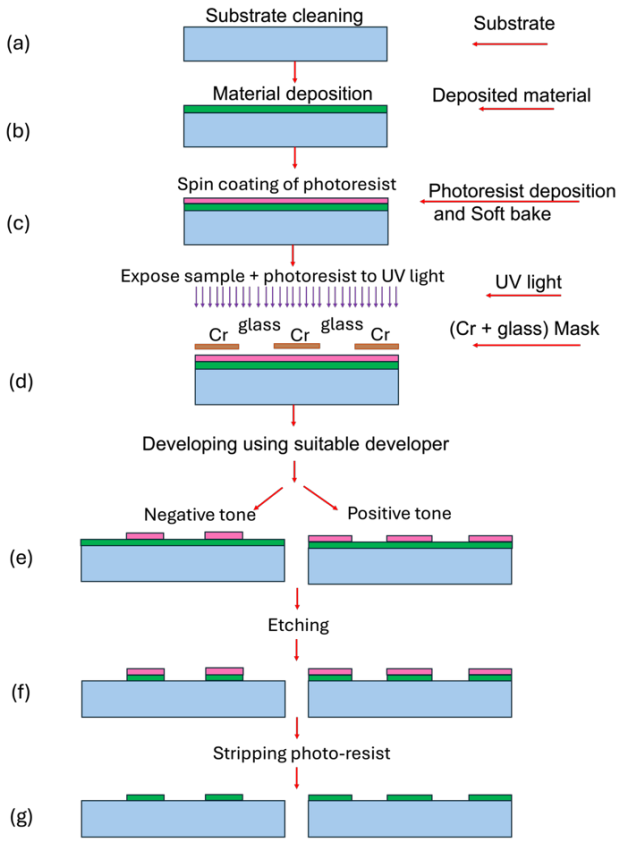


Figure 4-6: Process flow for pattern transfer using photolithography and etching.

The process begins with (a), where the substrate is cleaned. In (b), a film of material is deposited onto the substrate using techniques such as PVD, CVD, or atomic layer deposition (ALD), depending on the application. In (c), a uniform layer of photoresist was applied to the substrate using spin coating, ensuring even coverage across the surface. This was followed by a soft bake on a calibrated hot plate to remove residual solvents and improve adhesion for

subsequent processing. Following this, the photoresist-coated wafer is exposed to ultraviolet (UV) light through a quartz photomask, which defines the desired pattern on the surface. The exposure modifies the solubility of the photoresist, enabling selective removal of either the exposed or unexposed regions during the development step, depending on whether a positive or negative resist is used. Once the pattern is defined in (e) with the development of the sample, (f) focuses on the etching step, where the unprotected regions of the deposited material are selectively removed. This can be achieved through wet etching or dry etching. Finally, in (g), the structured pattern is revealed on the substrate by removing the remaining photoresist, ensuring that only the patterned material remains intact

4.1.3 Lift-off

The lift-off process in microfabrication, Figure 4-7, is especially advantageous for materials that are challenging to etch such as metal interconnects in integrated circuits.

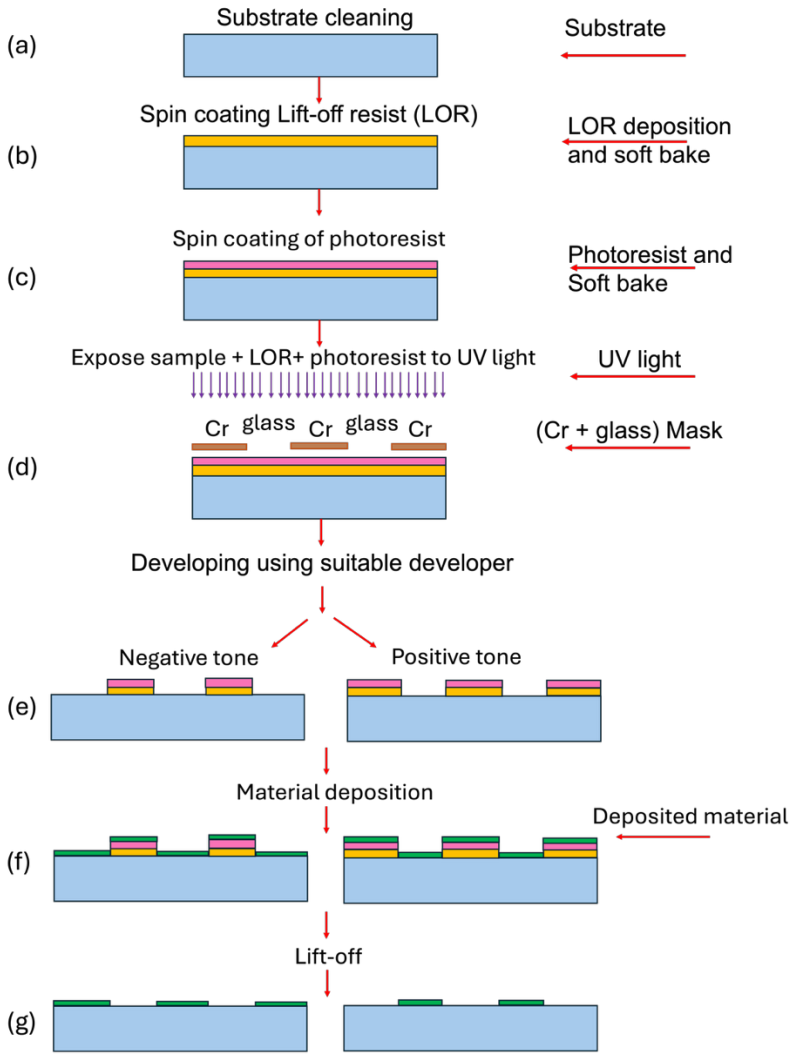


Figure 4-7: Process flow for pattern transfer using photolithography and Lift-off.

The process begins with substrate cleaning, (a), followed by photoresist coating and soft bake, (b) and (c), where a lift-off resist (LOR) layer and a photoresist layer are sequentially applied using spin coating. Each layer is individually baked to remove residual solvents and enhance adhesion. During the exposure step, (d), UV light is projected onto the photoresist, preparing it for the next step. The development process, (e), is carefully controlled to create an undercut profile, ensuring that the deposited material does not adhere to the resist sidewalls. Once the pattern is defined, a film is deposited across the wafer in step (f). In the final step, (g), the wafer is immersed in a solvent that dissolves the photoresist, lifting off the material deposited on top of it. This leaves only the material that was deposited directly onto the exposed substrate.

The distinction between the lift-off and etching techniques lies in their material removal approaches. Lift-off removes the sacrificial photoresist layer along with any unwanted material on top, whereas etching selectively removes portions of a deposited film through chemical or physical means. Due to its precision and control, lift-off is often the preferred method for applications requiring well-defined patterning without damaging underlying layers.

4.2 Material Selection

Material selection in CMUT fabrication, Figure 4-8, is a structured process that significantly impacts device performance, durability, and process compatibility.

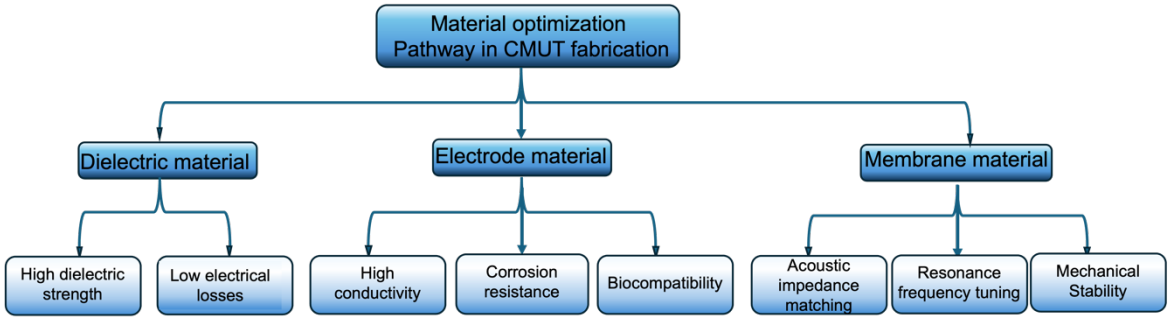


Figure 4-8: Material optimization pathway for CMUT fabrication.

Each component must be carefully optimized to ensure efficiency and reliability. Material selection is particularly crucial in determining process compatibility and structural integrity. The choice of materials must prioritize both selectivity and compatibility with subsequent fabrication steps. Selectivity refers to how well a material remains intact during an etching process while another is selectively removed. This characteristic is especially important in sacrificial layer techniques, where precise material removal through wet or dry etching dictates the overall fabrication flow. For instance, Si_3N_4 exhibits distinct selectivity properties in HF

vapour release compared to SiO_2, making it a preferred dielectric material in CMUT fabrication [163], [164].

Beyond selectivity, functional properties also play a role in CMUT performance. A key consideration is the dielectric layer, which insulates electrodes while enabling efficient capacitance modulation. Dielectric materials must exhibit high dielectric strength to withstand electrical stress while maintaining low energy losses to ensure stable capacitance modulation. Si_3N_4 and SiO_2 are widely utilized due to their excellent dielectric strength, minimal electrical losses, and robust mechanical properties [165]. Electrode materials must provide excellent conductivity for signal transmission, corrosion resistance for long-term reliability, and biocompatibility for biomedical applications. Au, Platinum (Pt), and Titanium (Ti) have been extensively studied for their conductivity and biocompatibility. Among these, Pt exhibits the highest electrical conductivity, followed by Ti and Au [166]. These properties make Pt an ideal material for medical devices [167]. The combination of Pt's biocompatibility and CMUT technology has further expanded its use in biomedical imaging [168].

The membrane material is integral to the CMUT's acoustic and mechanical properties, necessitating precise acoustic impedance matching, resonance frequency stability, and mechanical robustness to endure operational stress. The selection of membrane material has a significant impact on CMUT performance [169]. It must possess mechanical properties to ensure the desired resonance frequency and achieve efficient acoustic impedance matching. Different materials, including Si, Si_3N_4, polysilicon, and emerging options such as indium phosphide (InP), have been studied for CMUT membranes [169], [170] . SiC has gained attention in MEMS due to its exceptional mechanical resilience, thermal stability, and chemical durability [171]. SiC membranes have demonstrated superior Young's modulus, fracture toughness, and theoretical strength compared to conventional MEMS materials [172]. Polymer-based CMUTs offer advantages such as cost-effective fabrication and mechanical flexibility, but they are constrained by material limitations [73], [173]. Low-temperature fabrication methods have facilitated the integration of CMUTs with electronic circuits, enabling their use on diverse substrates [132].

In addition to these technical considerations, the final selection of materials and processes was also constrained in the work reported here by the availability of materials, fabrication techniques, and equipment in the James Watt Nano-Fabrication Centre (JWNC), University of Glasgow. These constraints require a balance between ideal material properties and practical feasibility within the available fabrication infrastructure.

4.3 Fabrication of CMUTs

As illustrated in Figure 4-9, the fabrication of CMUTs involves a multi-step process. Typically, it begins with the deposition of dielectric and electrode layers, followed by precise patterning, etching, and sacrificial layer removal to form the transducer cavities. A detailed breakdown of these steps is provided in the following sections.

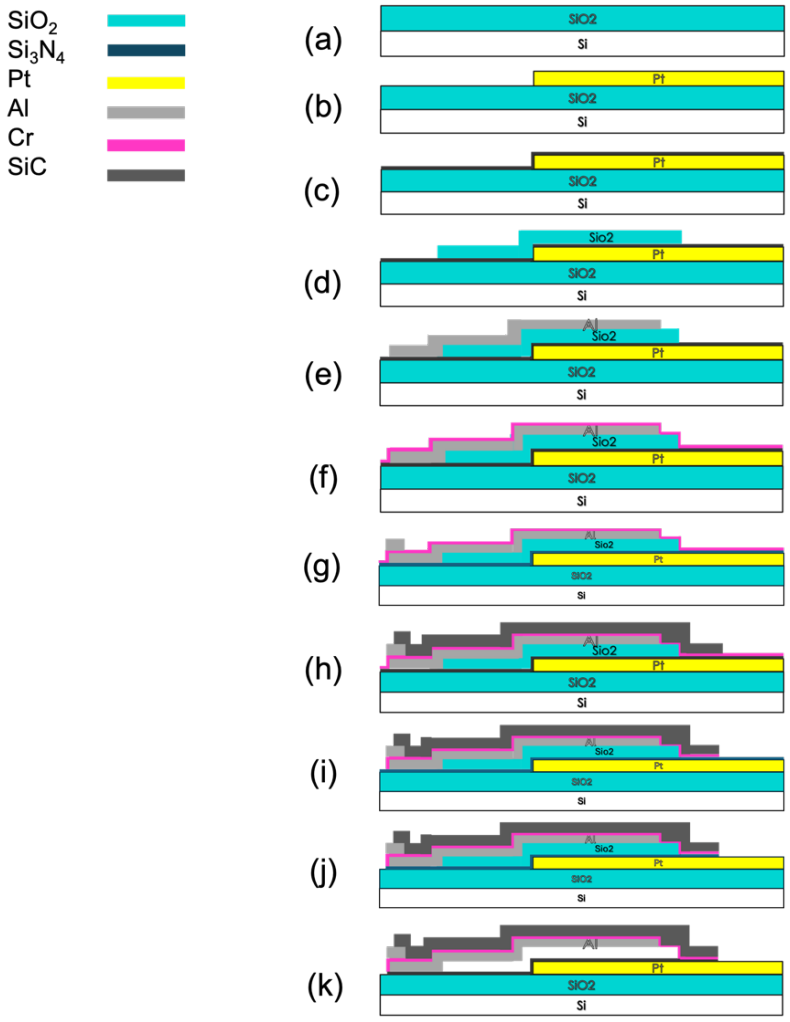


Figure 4-9: Step-by-step cross-sectional view of the CMUT fabrication process. (a) Substrate cleaning followed by SiO_2 dielectric deposition using PECVD. (b) Pt bottom electrode deposition using EVAP7. (c) Si_3N_4 dielectric layer added via PECVD. (d) SiO_2 sacrificial layer deposited by RF sputtering. (e) Al top electrode added by sputtering. (f) Cr barrier layer deposited by sputtering. (g) Al bonding pad added similarly. (h) SiC membrane layer formed by sputtering. (i) Cr layer removed by wet etching. (j) Si_3N_4 etched using RIE. (k) Final structure completed by vapour HF dry release of the SiO_2 sacrificial layer.

Figure 4-9 (a) illustrates this step, which begins with thorough cleaning. Initially, the sample is rinsed with reverse osmosis (RO) water for one minute. Following this initial rinse, ultrasonic cleaning is performed, in acetone for five minutes, followed by Isopropyl alcohol (IPA) for five minutes, and a final sonication step in RO water for an additional five minutes. To eliminate any residual moisture, the Si sample is then dried using Nitrogen (N_2) gas. The sample

then undergoes an additional cleaning step to ensure complete removal of any remaining contaminants in ASHER. This step involves applying a cleaning recipe of 200 W for 60 sec, optimizing surface purity and preparing the silicon substrate for subsequent fabrication processes. The sample then undergoes a dehydration bake on a hot plate at 200°C for 5 min. This step is essential for eliminating any residual moisture that may be present on the sample surface. Removing moisture is crucial to ensuring strong adhesion of subsequent layers in the fabrication process. After the dehydration bake, SiO_2 is deposited as a dielectric layer using high-rate Plasma - Enhanced Chemical Vapour Deposition (PECVD) to achieve efficient and uniform film growth. The deposition is carefully controlled with a gas mixture of 750 sccm of silane (SiH_4) and 800 sccm of nitrous oxide (N_2O). SiH_4 serves as the silicon source and N_2O provides the oxygen to facilitate film deposition. The process is carried out at a temperature of 300°C, optimizing film quality, adhesion, and uniformity. With a deposition rate of 728 nm/min, the process is maintained for approximately three minutes, resulting in a 2 µm thick SiO_2 layer.

Film stress significantly affects the structural integrity and functionality of MEMS devices. It arises due to thermal expansion differences, material compatibility, and deposition conditions, leading to either tensile or compressive stress. The deposited SiO_2 exhibits a compressive stress of -57 MPa, which enhances mechanical stability and minimizes the risk of cracking or delamination. Compressive stress helps reduce crack formation, while tensile stress can be beneficial for specific applications requiring flexible or strain-tolerant films. However, excess compressive or tensile stress can cause wafer deformation, cracking, or adhesion failures. To ensure stability and reliability, stress is carefully managed by optimizing temperature, pressure, and deposition rate. Additionally, the refractive index of the SiO_2 layer is measured at 1.475 at a wavelength of 632 nm, ensuring optical consistency and compatibility with subsequent fabrication steps.

4.3.1 Step 2 - deposition of Pt bottom electrode

The establishment of the Pt bottom electrode begins with deposition. As discussed in Section 4.2, Pt is chosen as the bottom electrode in MEMS fabrication due to its compatibility with cleanroom processes and excellent electrical conductivity. Its high melting point ensures excellent thermal stability and resistance to plastic deformation under elevated temperatures. The excellent resistance of Pt to corrosion and its compatibility with conventional IC fabrication techniques make it preferred for many MEMS devices [174]. Pt electrodes can be

produced through multiple techniques, such as electron beam evaporation (EBE), sputtering, and CVD. Figure 4-9 (b) illustrates this deposition process. Before deposition, a photoresist layer is applied using Mask No.1, as shown in Figure 4- 10, through lithography to achieve the required thickness for the lift-off process.

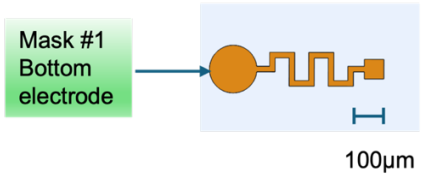


Figure 4-10: Mask No.1 used for patterning the Pt bottom electrode in the fabrication process.

As illustrated in Figure 4-7, the lift-off process ensures precise patterning. Following the preparation of the photoresist, the Electron-beam evaporation (EVAP) 7 system is used to deposit a 200 nm Pt layer. After deposition, lift-off is carried out by immersing the sample in a beaker containing SVC-14 or Micro-posit Remover 1165 (MP 1165) solvent which remove positive photoresist. The sample then is examined under a microscope to verify complete removal of residual resist. If any remains, the process parameters including photoresist deposition, baking conditions, and lift-off duration must be adjusted.

4.3.2 Step 3 - deposition of Si_3N_4 dielectric layer

As illustrated in Figure 4-9 (c), Si_3N_4 is deposited as a dielectric using a low-stress PECVD process, carefully controlled with a gas mixture of 200 sccm of SiH_4, 120 sccm of NH_3, and 1000 sccm of N_2. SiH_4 provides the Si and ammonia (NH_3) supplies N_2 to form Si_3N_4. N_2 contributes to plasma stabilization and influences film properties such as stress and refractive index. The film exhibits a compressive stress of -72 MPa, which helps prevent cracking and improves mechanical durability. The refractive index is measured at 1.987 at 632 nm, ensuring consistency in optical and dielectric performance. Fluctuations in refractive index may indicate variations in film density or composition [175]. Additionally, dielectric charging can lead to drift effects in micro-devices, impacting their long-term stability and operational performance [176]. Deposition occurs at a controlled rate of 101 nm/min, with a chamber temperature of 300°C. Precise parameter adjustment results in a Si_3N_4 layer with a thickness of 510 nm.

4.3.3 Step 4 - deposition of SiO_2 Sacrificial layer

Using Mask No.2, Figure 4-11, the lithography process is utilized to define the pattern for SiO_2 deposition, Figure 4-9 (d). The sample undergoes SiO_2 deposition via sputtering at below

200°C. Compared to methods like PECVD, sputtering offers several advantages, including the ability to produce high-density films while reducing thermal stress on the substrate [177]. Sputtering was selected for SiO_2 deposition due to its ability to provide controlled adhesion. Since the SiO_2 layer is temporary, adhesion must be carefully adjusted for efficient removal while preventing residues or damage to the patterned structure. Excess adhesion hinders the lift-off process while insufficient adhesion may cause premature peeling, disrupting the fabrication process. Unlike other deposition techniques that enhance adhesion, sputtering allows precise control over film attachment. The strength of adhesion can be tailored by modifying parameters such as substrate temperature, energetic particle bombardment, and specific deposition conditions [178]. This controlled adhesion enables elimination of unwanted material without compromising the underlying layers. The pattern of the deposited Pt bottom electrode and the SiO_2 sacrificial layer is presented in Figure 4-11. The SiO_2 deposition process was carried out with a power of 250 W, an argon (Ar) flow rate ranging from 3 - 7 sccm and a pressure of 10×10^{-3} mbar. To ensure uniform film deposition, the substrate temperature was maintained at 20°C with a rotation speed of 20 rpm. The deposition was sustained for 11,000 sec, to realise a SiO_2 film of approximately 540 nm.

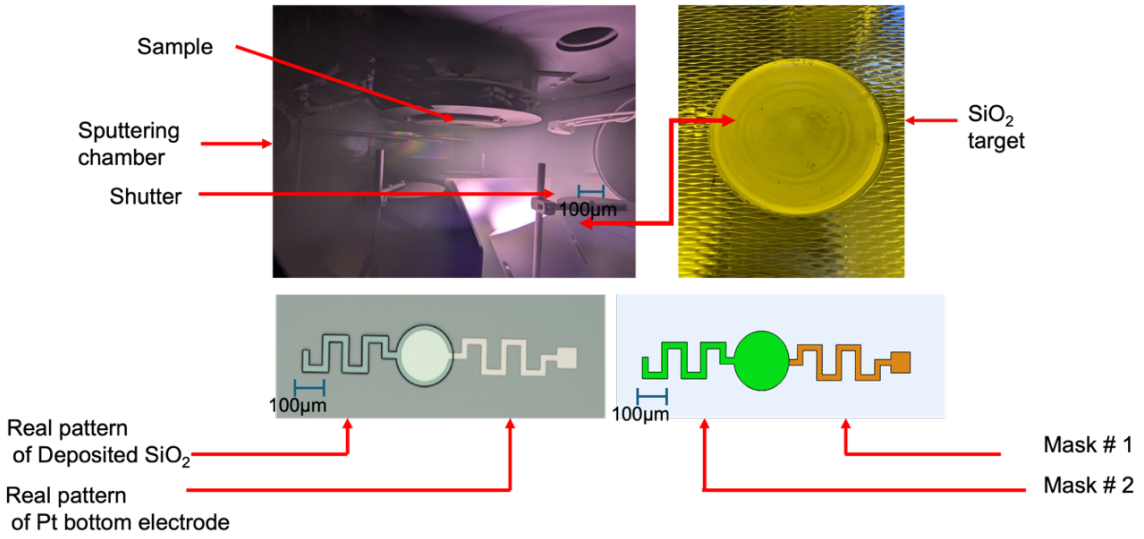


Figure 4-11: Using Mask No.2 for the deposition of a sacrificial layer in the sputtering chamber with an SiO_2 target to achieve the final pattern shown.

Once deposition is complete, the sample proceeds to the lift-off process, where SVC-14 or Micro-posit 1165 is used to remove unwanted areas.

4.3.4 Step 5 - deposition of Al top electrode

Using Mask No.3, Figure 4-13, the lithography process is utilized to define the pattern for Al top electrode deposition, Figure 4-9 (e). The top electrode, thickness 70 nm, is influenced by the step variations in the underlying layers. To ensure uniform and reliable film deposition, sputtering is preferred over EVAP because evaporation is a directional process that deposits material along a single trajectory, whereas sputtering is non-directional technique [179]. These techniques differ in their deposition mechanisms, leading to distinct film growth characteristics [180].

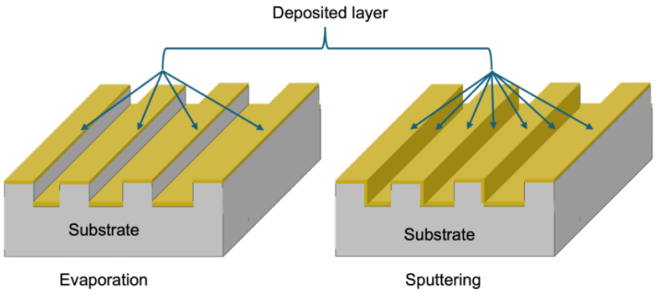


Figure 4-12: Comparison of deposition differences between EVAP and sputtering.

As illustrated in Figure 4-12, sputtered films typically provide superior step coverage and conform more effectively to surface topography than evaporated films [181]. This enhanced coverage results from the higher kinetic energy of sputtered atoms, which increases surface mobility and facilitates more effective filling of surface features [182]. Unlike EVAP, sputtering provides a more isotropic deposition process, where high-energy particles ensure that material is evenly distributed across varying topographies. This characteristic allows the deposited layer to conform more accurately to the step height variations in the underlying layers, reducing the risk of delamination. Furthermore, sputtering can minimize defect height and steepness while limiting lateral spread [183]. The process is affected by variables such as ion energy, substrate temperature, and surface rearrangement [184], [185]. Computational modelling and experimental data have shown strong agreement in predicting step coverage profiles for sputtered films, further supporting its effectiveness in achieving uniform deposition [186]. Additionally, sputtering, particularly magnetron sputtering, offers higher deposition rates and improved film characteristics compared to evaporation [187]. Sputtered Al is ideal for CMUTs, as it offers flexibility and HF vapour resistance during the release process. Unlike brittle Pt, Al withstands mechanical stress, ensuring stable and reliable performance under continuous vibration.

Using deposition parameters including a power of 120 W, an Ar flow of 3 - 7 sccm, a set pressure of 7 - 10 × 10^{-3} mbar, a temperature of 20°C, a rotation speed of 20 rpm, and a duration of 260 sec, a 70 nm Al layer, was deposited to serve as the top electrode. The applied power provides sufficient energy for Al atoms to be ejected from the target and deposited onto the substrate, while the Ar flow rate helps sustain a stable plasma. The pressure influences the mean free path of the sputtered atoms, contributing to film density and coverage. Maintaining the substrate at 20°C prevents excessive thermal stress, and sample rotation at 20 rpm promotes uniform thickness across the surface. Figure 4-13 shows the sputtering chamber during the deposition using an Al target. It also presents the pattern of the Al top electrode, along with the alignment markers utilized at this stage. Following deposition, the lift-off process involves immersing the sample in a beaker with SVC-14 or MP 1165.

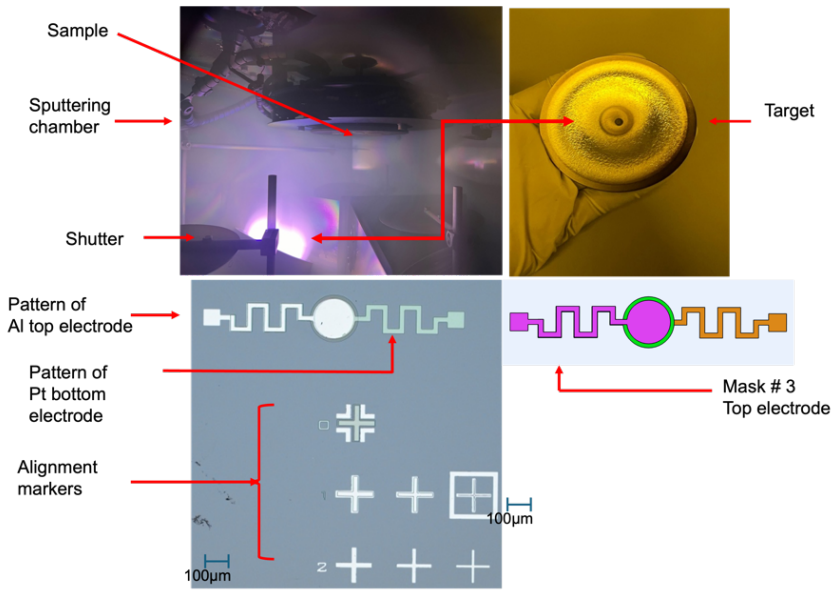


Figure 4-13: Using Mask No.3 for the deposition of the top electrode in the sputtering chamber with an Al target to achieve the final pattern shown.

4.3.5 Step 6 - deposition of Cr barrier layer

As shown in Figure 4-9 (f), chromium (Cr) was incorporated as an adhesion layer, deposited across the entire sample to strengthen the bonding between the Al top electrode and the SiC membrane. Given the critical role of the Cr layer in maintaining structural integrity, it was deposited using sputtering. Due to its low thickness of 10 nm, the process was conducted slowly to ensure high uniformity and minimize defects. The process was performed using a power of 100 W, an Ar flow rate of 3 - 7 sccm, a set pressure of 7 - 10 × 10^{-3} mbar, a substrate temperature of 20°C, and a rotation speed of 20 rpm. To ensure precise layer formation and

uniform material transfer, the deposition duration was extended to 1200 sec. Again, after deposition, the sample was subjected to a lift-off process by immersing it in SVC-14 or MP 1165. Figure 4-14 illustrates the deposited Cr layer all over the sample.

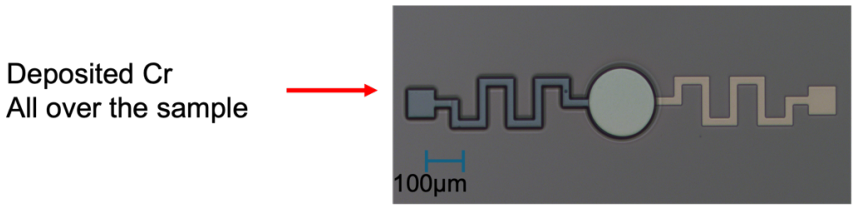


Figure 4-14: Deposition of Cr using sputtering, covering the entire sample, hence no Mask required.

4.3.6 Step 7 - deposition of Al bonding pad

As shown in Figure 4-9 (g), the Al bonding pad was deposited using Mask No.4, Figure 4-15, again by sputtering to ensure uniform thickness and strong adhesion. The deposition was carried out with the same parameters as the previous Al but for a duration of 600 seconds to achieve the thickness and surface properties for reliable electrical contact. The lift-off process was again completed using SVC-14 or MP 1165, effectively removing excess material. Figure 4-15 illustrates the pattern of the deposited Al bonding pad.

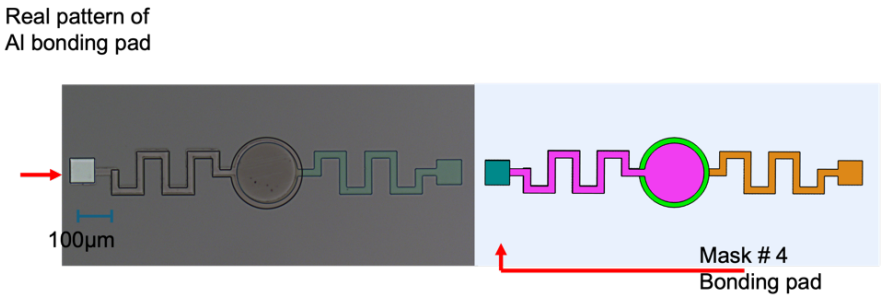


Figure 4-15: Using Mask No.4 for the deposition of the Al bonding pad in the sputtering chamber to achieve the final pattern shown.

4.3.7 Step 8 - deposition of SiC membrane

Figure 4-16 illustrates Mask No. 5, which is used during the SiC deposition process. Slit-type release holes are included in the design to enable access to the underlying SiO_2 sacrificial layer for removal during the release step. Following photoresist patterning via the lift-off process, SiC was deposited using RF sputtering, as shown in Figure 4-9 (h), with a sputtering power of 250 W. Ar gas flow ranging from 3 - 7 sccm was maintained and the chamber pressure was set at 10×10^{-3} mbar. The substrate temperature was 20°C and rotation of 20 rpm was applied. The process was sustained for 18000 sec (300 min = 5 hr) for the gradual accumulation of SiC material until the desired 1.5 µm thickness was achieved. The lift-off process for this deposition

was again carried out with SVC-14 or MP 1165, ensuring the efficient removal of unwanted material. Figure 4-16 illustrates the deposition duration of SiC, along with the actual pattern of the deposited layer, where poor adhesion of SiC on the underlying Cr layer can be observed.

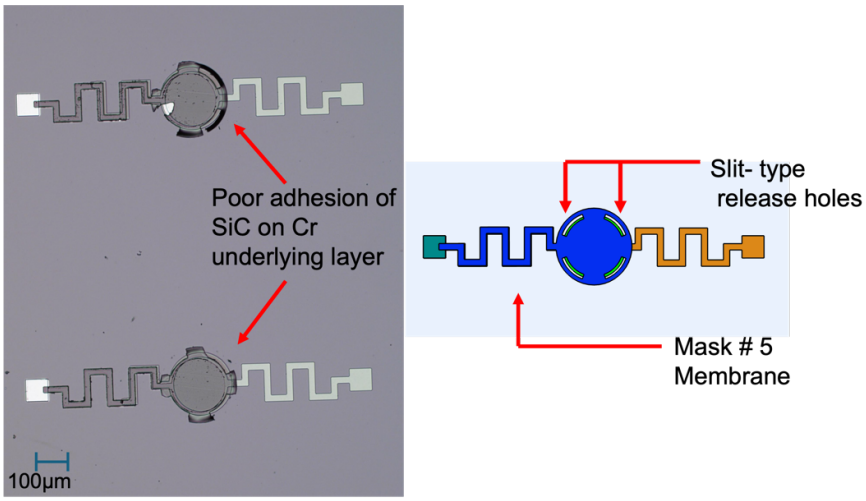


Figure 4-16: Using Mask No.5 for the deposition of the membrane in the sputtering chamber with a SiC target to achieve the final pattern shown.

Ti and Cr are frequently employed as adhesion layers to enhance the bonding of Au and other metals to various substrates [188], [189]. However, studies have shown that Ti adhesion layers exhibit stronger adhesion and improved interface stability compared to Cr [190], [191]. To address adhesion issues in future fabrication, the thickness of the barrier layer will be increased, and Cr will be replaced with Ti as the adhesion layer.

4.3.8 Step 9 - Wet etching of Cr barrier layer

Figure 4-9 (i) illustrates the steps following the deposition of SiC, where the sample undergoes the etching of the Cr barrier layer using MKCP4049 Cr etchant. In this process, a 10 nm Cr layer is removed by immersing the sample in 40 ml of MKCP4049 for 12 seconds. This is necessary to prepare for the dry etching of the Si_3N_4 layer and to expose Pt bottom electrode for later probing. Figure 4-17 presents the sample after the Cr layer has been successfully etched.

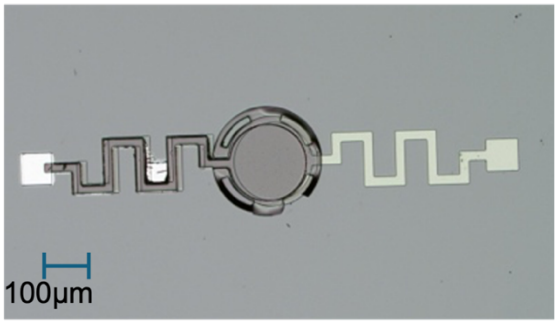


Figure 4-17: Sample after wet etching using Cr etchant (MKCP4049, Merck).

4.3.9 Step 10 - Dry etching of Si_3N_4 using RIE

This step, Figure 4-9 (j), involves dry etching of the Si_3N_4 layer to expose the bonding pad and bottom electrode for measurement. The Reactive ion etching (RIE) process is performed using a mixture of 50 sccm CH_3 and 5 sccm of O_2, with a power of 150 W, a chamber pressure of 55 mTorr, and a substrate temperature of 20°C for approximately 7 min. This process is primarily used for vertical etching of the Si_3N_4 layer, achieving an etch rate of around 80 – 90 nm per minute. Since the Si_3N_4 layer has a thickness of 510 nm, the etching duration is slightly extended, incorporating over-etching to ensure complete removal of the Si_3N_4 layer and full exposure of bottom electrode and bonding pad. Figure 4-18 presents the sample after the Si_3N_4 etching process.

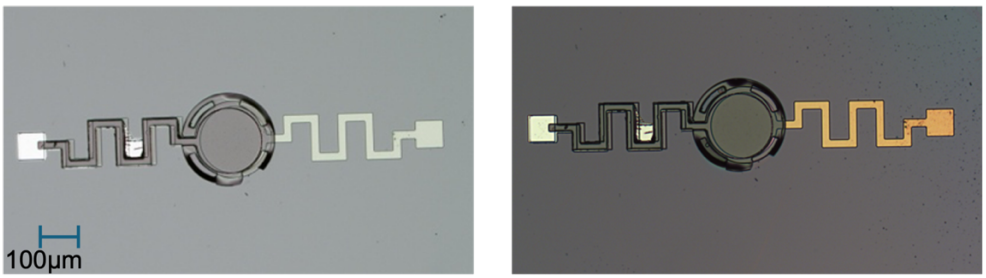


Figure 4-18: Sample before and after dry etching of Si_3N_4 using RIE.

4.3.10 Step 11 - HF vapour dry release of sputtered SiO_2 sacrificial layer

HF vapour etching is widely used for MEMS release, and Pt exhibits a certain degree of resistance to this process, contributing to its stability during fabrication [192]. Additionally, studies indicate that the etch rates of Au, Pt, and Cr in HF vapour are minimal or insignificant, further supporting their suitability for MEMS applications where controlled etching is required [193].

In this step, as shown in Figure 4-9 (k), the sample was sent to MEMSSTAR (Edinburgh, UK). The etch rates of Pt, SiC, and the Al top electrode were evaluated in the HF vapour release tool to ensure precise etching. Al and its alloys demonstrate resistance to HF vapour etching, making them well suited for integration into MEMS devices [194]. Similarly, SiC is known for its strong resistance to chemical etching, including exposure to HF vapour [195].

Although the process was designed for high accuracy, the sample underwent five cycles of HF vapour etching, Figure 4-19, to fully remove the sacrificial layer. This extended exposure resulted in over-etching, which led to damage to the first sample. This outcome highlights the need for refining the fabrication process to prevent material degradation and improve process control. The details of the operating recipe are thoroughly explained in the following section.

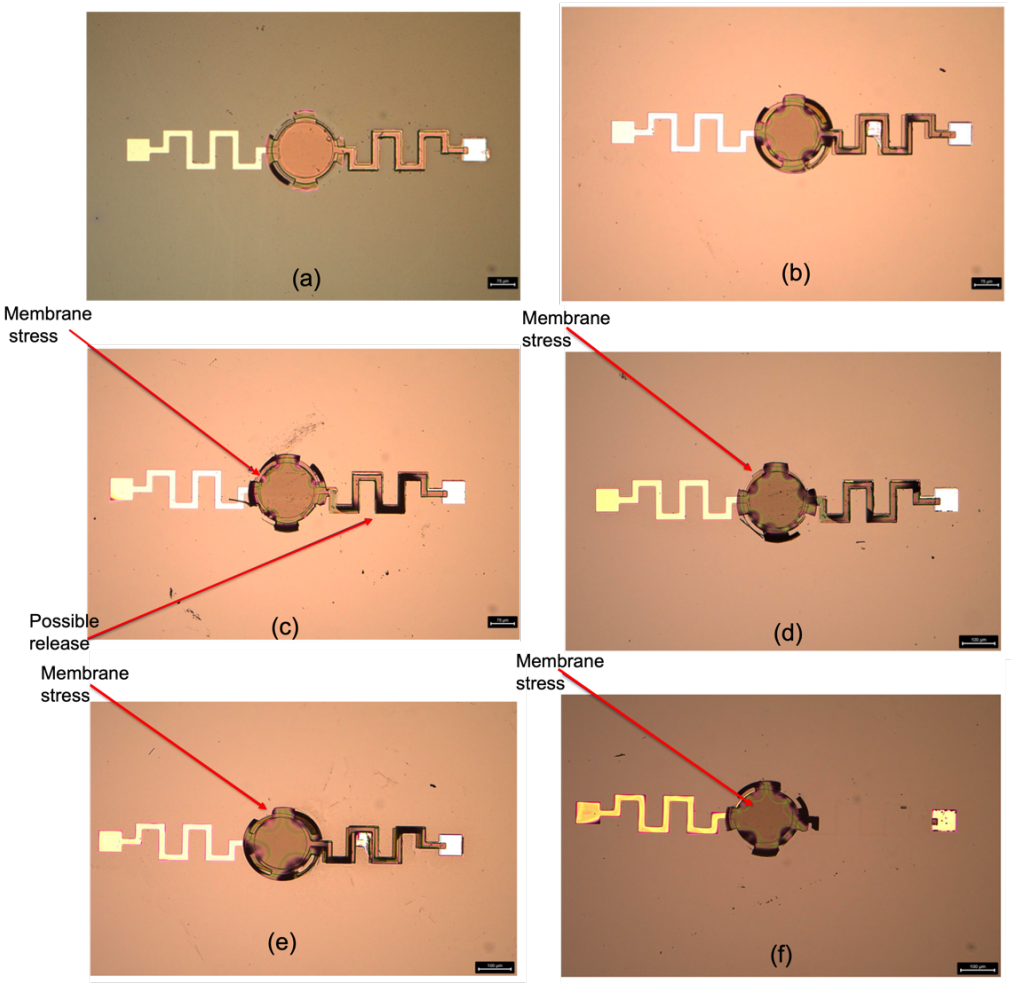


Figure 4-19: (a) First HF vapour release of the SiO_2 sacrificial layer. (b) second HF vapour release cycle. (c) Sample after subsequent annealing in second cycle. (d) third HF vapour release cycle. (e) fourth HF vapour release cycle. (f) fifth HF vapour release cycle.

First etch

First etch HF vapour dry etching for SiO_2 was carried out under controlled conditions to achieve selective material removal. An initial 10-minute etching step effectively reduced the sacrificial layer thickness, confirming successful oxide removal while preserving surrounding materials. Post-etch examination showed uniform etching, ensuring minimal under-etching or excessive material loss, validating the effectiveness of the HF vapour process in releasing the structure and informing further process optimization, as illustrated in Figure 4-19 (a).

Etch cycle (2)

After the initial 10-minute etching step, the process was extended for an additional 30 minutes to enhance material removal and facilitate structure release. As illustrated in Figure 4-19 (b), this phase of SiC etching led to the formation of a residue that affected process quality. To address this, a post-etch annealing step, Figure 4-19 (c), was implemented, where controlled heating facilitated the breakdown and vaporization of the residue. This ensured a clean surface while preserving the integrity of the surrounding materials, contributing to a more precise and reliable fabrication outcome.

Etch cycle (3)

Figure 4-19 (d) illustrates the results of the third etching process. A noticeable shift in the stress pattern was observed, gradually concentrating towards the centre of the membrane. This signified ongoing etching progression, with further undercutting occurring as the process advanced. The expansion of the undercut region confirmed effective material removal. However, despite this progress, the membrane remained intact, indicating that full release had not yet been achieved. This suggested that additional etching cycles might be required.

Etch cycle (4)

Figure 4-19 (e) presents the results of the fourth etching process. As etching progressed, the stress pattern continued shifting towards the centre, indicating an ongoing release mechanism. The expansion of the undercut further confirmed material removal, though at a controlled rate. Despite this advancement, the membrane remained partially attached, suggesting that it was still not sufficiently close to full release.

Etch cycle (5)

As illustrated in Figure 4-19 (f), the fifth etching process revealed a continued shift in the stress pattern toward the centre, indicating further undercut progression. However, during this phase,

the electrical contact fractured, ultimately leading to device failure. The structural integrity of all tested devices was compromised, suggesting that the etching process had surpassed the mechanical limits of the materials, resulting in their complete breakdown.

Overall, the etching process on the sample presented both benefits and challenges. The SiO_2 layer etched efficiently at low pressure, indicating high selectivity. However, the undercut etch rate was slower than anticipated. Unexpected etching of the SiC layer resulted in residue formation, which was removed effectively through annealing. Stress contour analysis confirmed undercut progression, but before achieving complete membrane release, the electrical contact leg delaminated across all devices, likely due to accumulated mechanical stress.

Chapter 5: Dynamic Measurement of Micromachined Capacitor

5.1 Structural characterization

To ensure proper device performance and fabrication accuracy, it is useful to examine the physical structure and surface profile of CMUTs. This process often involves tools such as the profilometer and scanning electron microscopy (SEM). The Dektak XT profilometer provides high-resolution surface measurements, enabling detailed analysis of membrane thickness, etch depths, and overall surface topography. These measurements help confirm design specifications and fabrication consistency. SEM captures high-magnification images of CMUT structures, revealing micro- and nanoscale features such as membrane shape, sidewall profiles, and surface irregularities. It is especially helpful in identifying unknown structural variations and potential fabrication defects. Combining data from profilometry and SEM provides a more complete understanding of CMUT structural characteristics.

5.1.1 Profilometry

As shown in Figure 5-1, a contact profilometer operates with a probe head and force sensor, enabling precise surface scanning. It is integrated with a Wheatstone bridge circuit connected to a digital multimeter and a computer, which collect and process the measurement data. The scanning process generates a profile, capturing surface roughness, step heights, and variations in coating thickness. This information is important for evaluating the uniformity and quality of thin films, including photoresists. The diagram also highlights different surface topographies that the profilometer can detect, assisting in the optimization of material deposition and etching processes. Additionally, the lower section of Figure 5-1 presents a measurement of a fabricated CMUT in its intermediate stages.

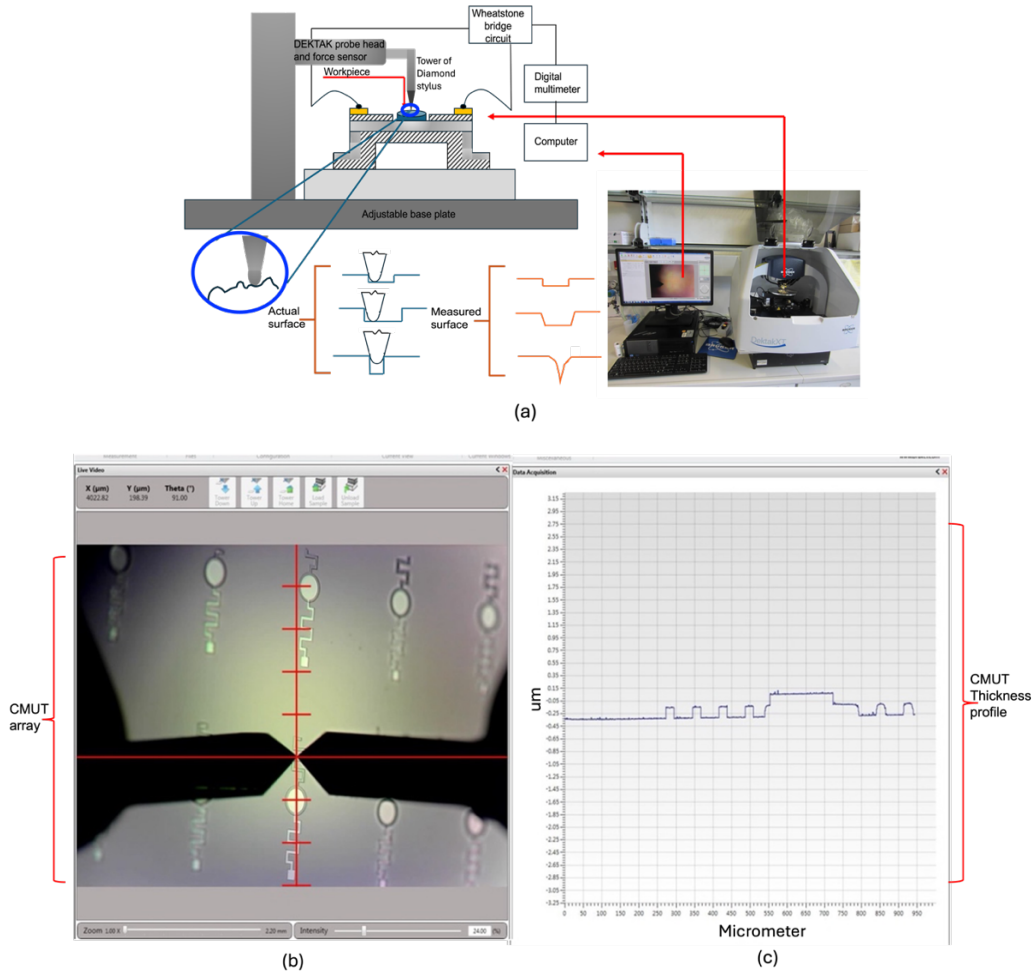


Figure 5-1: (a) Schematic and physical setup of a profilometer (Dektak XT, Bruker, USA), (b) diamond stylus on CMUT array. (c) analysis of a CMUT topography.

Quality assessment and process control in photoresist thickness measurement

Figure 5-2 presents the thickness measurement of S1818 photoresist after the developing process.

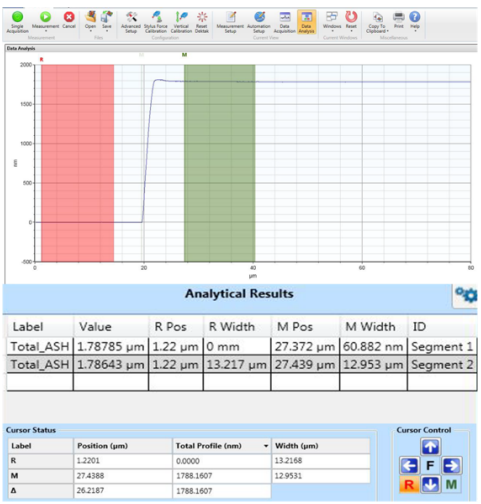


Figure 5-2: Surface profile analysis of S1818 photoresist using Dektak-XT.

The graph shows the thickness profile of the developed photoresist, with an average thickness of approximately 1.8 µm, aligning with the expected standard thickness for S1818. If the measured thickness deviates from the expected value, it may indicate inconsistencies in coating speed, resist viscosity, baking temperature, or exposure dose, all of which can affect the final lithographic pattern. In such cases, the resist must be completely stripped using appropriate solvents. Once the resist is removed, the process must be restarted from the spin coating step, ensuring that parameters such as spin speed, acceleration, and baking conditions, are properly controlled. Maintaining consistency in photoresist thickness is crucial for achieving accurate lithographic patterning and precise device fabrication. Any significant deviation can lead to pattern distortion and defects in subsequent processing steps.

5.1.2 Scanning Electron Microscopy

Figure 5-3 shows the principle of SEM, utilizing a concentrated electron beam to scan a sample's surface to generate high-resolution images.

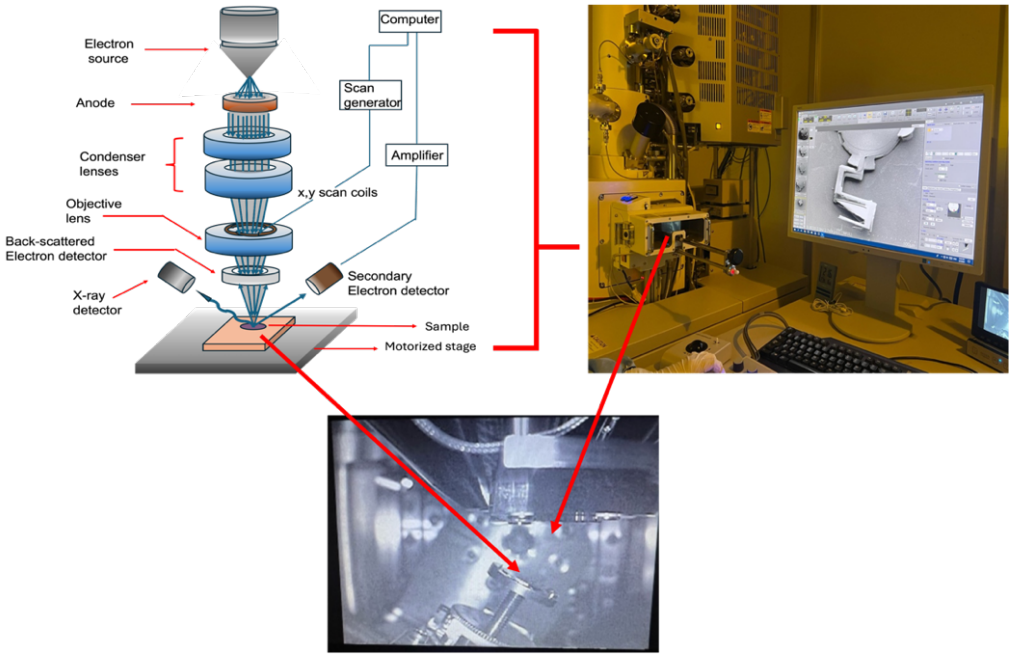


Figure 5-3: Schematic representation and physical setup of a SEM system (SU8230, Hitachi High-Technologies Corporation, Japan) used for high-resolution imaging in the present work.

As electrons interact with the material under test, secondary and backscattered electrons are emitted, allowing SEM to generate high-resolution images that capture fine surface details. This interaction provides critical insights into the nanoscale structure and composition of materials. To ensure imaging accuracy, the sample must be conductive or coated with a conductive layer to prevent charging effects. The process is performed in a vacuum to stabilize

the electron beam and eliminate interference. Different detection techniques, such as secondary electron imaging and backscattered electron imaging enhance contrast. Figure 5-4 shows SEM images of the CMUTs after the final stage of SiO_2 sacrificial layer dry release process in the present work.

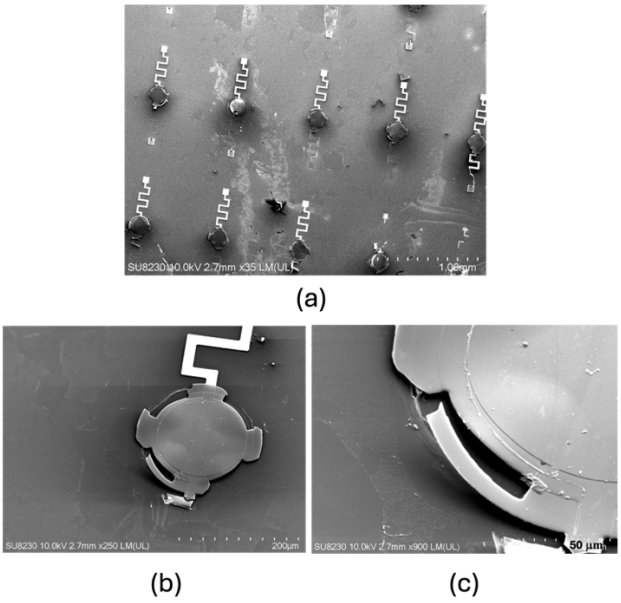


Figure 5-4: SEM images showing detailed views of the device after the final (5th) HF vapour release cycle of the sacrificial layer. (a) Overview of the CMUT array. (b) a single CMUT cell with partially released membrane. (c) High-magnification image of the membrane edge, highlighting the undercut region and released sacrificial layer.

5.2 Electrical characterisation

Capacitance measurements help assess the electrical behaviour of CMUTs and their reliability in practical applications. Two common methods used for this evaluation are C-V and C-F measurements. C-V measurements provide insight into the electrostatic response of the CMUT, revealing charge distribution and dielectric integrity. C-F measurements examine how capacitance changes with frequency, helping to identify parasitic effects such as inductive interference from bonding wires, probe connections, and measurement cables. Minimizing these effects improves the accuracy of capacitance readings.

Since the main wafer broke during the fifth HF vapour cycle, another capacitive component of the designed CMUT was completed up to the deposition of the Al bonding pad, as shown in Figure 5-5.

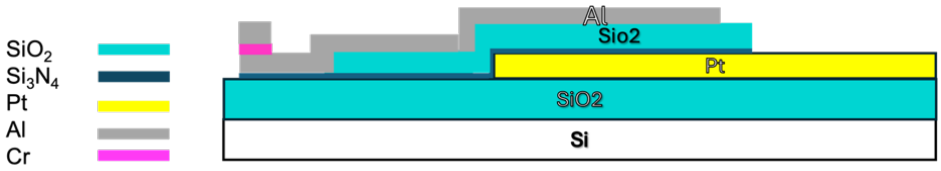


Figure 5-5: Cross-sectional view of the capacitive part of a fabricated CMUT.

Subsequently, the sample underwent wet etching of Cr and dry etching of Si_3N_4 to form the capacitive part of the CMUT for measurements. This capacitance serves as a reference for further analysis by providing insights into the structural composition and dielectric properties of the device. By analysing capacitance in relation to both voltage and frequency, the dielectric constant can be validated against expected values, and the structural integrity of the CMUT can be assessed to confirm the absence of dielectric breakdown.

5.2.1 Measurement setup

Figure 5-6 illustrates the measurement setup for assessing the capacitive part of the CMUT, incorporating a Semiconductor Parameter Analyzer (SPA), a Capacitance Measurement Unit (CMU), a probe station, and the Device Under Test (DUT). The probe station ensures precise electrical contact between the DUT and the testing instruments, with microprobes establishing direct contact with the top and bottom electrodes of the CMUT. The SPA is a versatile instrument used to evaluate the electrical characteristics of semiconductor devices, electronic components, and materials. It enables precise measurement of current, voltage, capacitance, and impedance. Capacitance measurements were performed in a controlled basement laboratory with precisely regulated vibration and humidity, timed to minimize environmental noise. A Faraday cage was employed to further reduce electromagnetic interference, ensuring accurate results. The analyser integrates multiple measurement techniques, including current-voltage (*I-V*), *C-V*, and impedance spectroscopy, allowing for comprehensive device characterization. This section examines capacitance-based measurements, specifically *C-V* and *C-F* analyses, applied to the capacitance component of an incomplete CMUT (illustrated in Figure 5-5) to evaluate its electrical behaviour.

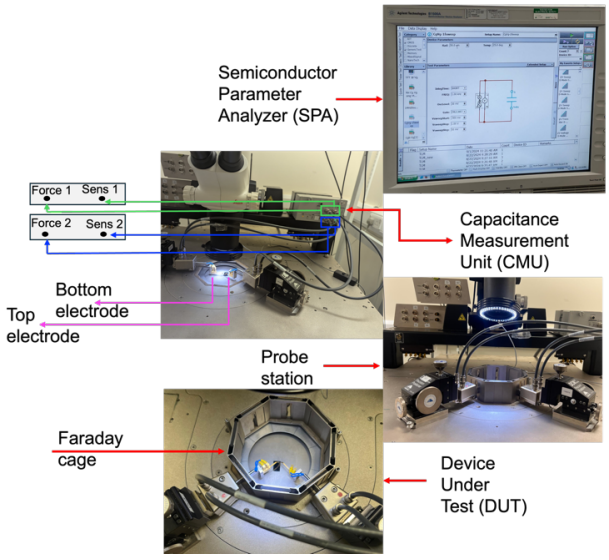


Figure 5-6: Experimental setup used for *C-V* and *C-F* measurements.

In this setup, *C-F* measurement is used to analyse the impact of parasitic inductance arising from bonding wires, cables, and connectors, while the *C-V* measurement helps assess the dielectric integrity of the sputtered SiO_2 sacrificial layer, ensuring it does not break down within the applied voltage range.

5.2.2 *C-F* Analysis

At the initial stage of the *C-F* measurement process, negative capacitance was encountered, suggesting that the conductive region of the capacitance was not fully reached. This issue indicated an under-etched Si_3N_4 layer. To address this, an additional etching of the Si_3N_4 layer was completed using the same recipe as outlined in Section 4.3.10, extending the process for an additional three minutes. Following this step, the negative capacitance issue was successfully resolved.

As Figure 5-7 illustrates, the *C-F* measurement graph presents the variation of capacitance (C_p) with frequency, in the range 1000 Hz to approximately 5 MHz, with capacitance values in the pF range.

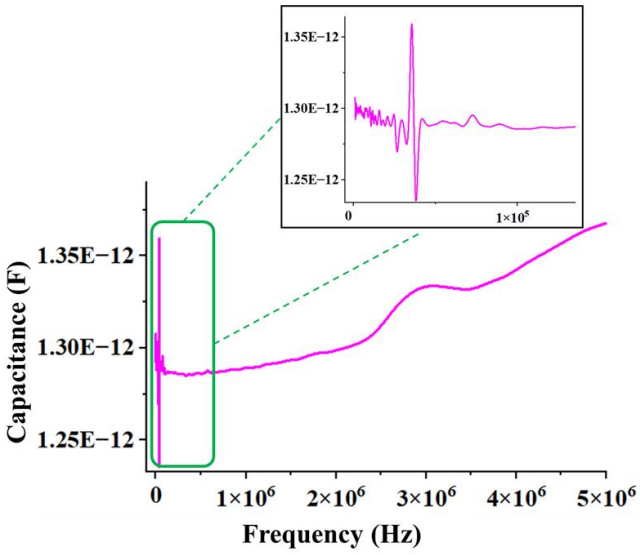


Figure 5-7: *C-F* plot of capacitance for the capacitive part of the fabricated CMUT.

The data indicates that capacitance remains relatively stable at lower frequencies, suggesting a consistent dielectric response of the CMUT structure without significant interference from parasitic effects. However, a disturbance is observed around 34 - 40 kHz, where a peak is followed by a dip. Given that complete perturbation is minor, approximately ± 0.1 pF, this fluctuation is most likely caused by electromechanical noise and the resonance of the probes rather than intrinsic device properties or external electrical parasitic.

Beyond this mid-frequency range, capacitance stabilizes again and remains consistent until higher frequencies (~1 MHz to 5 MHz), where a gradual increase is observed. This behaviour is likely influenced by minor parasitic capacitance from the probe station, measurement cables, or DUT fixture, as well as dielectric relaxation effects within the CMUT material and charge accumulation at the electrode interfaces. Overall, the capacitance values remain within a narrow range, approximately 1.25 - 1.35 pF, indicating that the CMUT device is functioning as expected with minimal external interference.

Parasitic inductance can sometimes contribute to distortions in capacitance measurements at higher frequencies by introducing reactance, but in this case, the observed capacitance does not show a strong frequency-dependent decline. Instead, the measured response is smooth apart from the minor mid-frequency fluctuation, reinforcing the likelihood that the observed resonance originates from electromechanical interactions within the probe station and not from parasitic effects in the electrical setup. Optimizing the mechanical stability of the probes and ensuring minimal movement during measurement may mitigate such minor variations in future tests.

5.2.3 *C-V* Analysis

The capacitance part of the CMUT was also measured using the setup shown in Figure 5-8, designed to analyse its *C-V* characteristics. In this setup, an ac signal is applied to the device while measuring the capacitive response. The test configuration includes a 1 MHz frequency for the excitation signal with an oscillation level of 20 mV, ensuring accurate detection of capacitance variations. An ammeter (A) measures the resulting current, and a voltmeter (V) records the voltage response. A four-terminal pair (4TP) configuration is used to minimize parasitic resistances for precise capacitance extraction. The CMUT is modelled as a parallel-plate capacitor, with G (gate) as the top electrode and Subs (substrate) as the bottom electrode. Low and high current (L_C, H_C) and low and high potential levels (L_P, H_P) connections ensure accurate separation of current and voltage measurements.

As V_{gb} (gate-to-substrate bias voltage) is swept over a voltage range of -2 V to 2 V with a step size of 50 mV, the electrostatic force influences the membrane position, altering capacitance. The chosen frequency, oscillation level, and step size allow for the measurement of electrical properties such as dielectric integrity, pull-in voltage, and charge trapping effects.

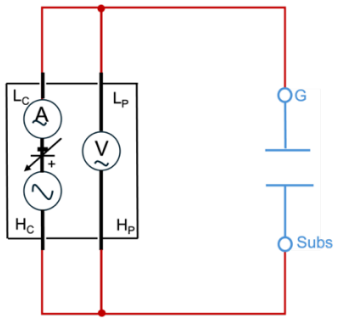


Figure 5-8: Circuit configuration for C-V measurement of CMUT: a four-terminal setup for accurate capacitance extraction.

For the *C-V* measurements, the primary concern was assessing the structural integrity of the sputtered SiO_2 sacrificial layer. If the SiO_2 layer had undergone electrical breakdown, it would have resulted in a capacitance reading of zero, indicating a short circuit between the top and bottom electrodes. However, in the specific measurement range used, this layer demonstrated sufficient dielectric strength and did not break down. This confirms the reliability of the fabrication process and the robustness of the insulating layer, ensuring proper CMUT operation within the tested voltage range.

The dielectric constant can also be validated through *C–V* measurements. As shown in Figure 5-9, the capacitance structure consists of two dielectric layers arranged in series. Therefore, Equations 5.1 and 5.2 are applied to estimate the approximate relative permittivity (ε_r) of the stacked dielectrics, based on the measured capacitance of 1.3 pF within the ±2 V range at the lowest frequency of 10 kHz. This frequency is chosen because higher frequencies introduce parasitic effects, whereas lower frequencies provide more accurate and reliable values.

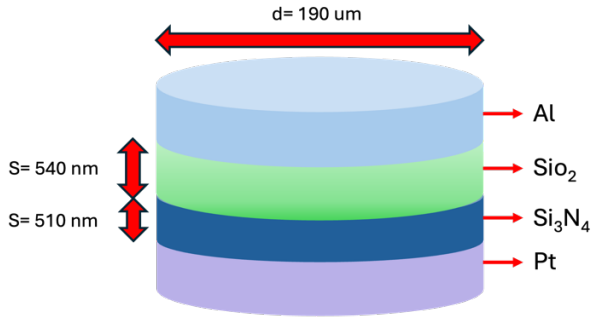


Figure 5-9:Cross-sectional view of the circular capacitive part of the fabricated CMUT

$$C = \frac{\varepsilon_0 \varepsilon_r \pi d^2}{4s} \qquad \text{Eq. 5.1}$$

$$\frac{1}{C} = \frac{1}{C_1} + \frac{1}{C_2} \qquad \text{Eq. 5.2}$$

where C represents the capacitance, $\varepsilon_0 = 8.854\times10^{-12}$ F/m is the permittivity of free space, and ε_r is the relative permittivity of the materials between the plates. The parameter d denotes the diameter of the circular plates, while s is the distance separating them.

The calculated ε_r for SiO_2 and Si_3N_4 layers were approximately 4.3 and 7.5, respectively which are in close agreement with the previously reported dielectric constant of sputtered SiO_2 [196] and PECVD Si_3N_4 [197].The deviation between the calculated and reported values may arise from factors such as fabrication variations, measurement uncertainties, or slight differences in deposition conditions.

Overall, the results confirm stable electrical behaviour in the CMUT device, with little influence from external factors. The findings demonstrate the effectiveness of the measurement approach while also suggesting potential improvements, such as reducing resonance effects caused by the microprobes and enhancing the mechanical stability of the test setup. Further refinements in fabrication processes and measurement configurations can improve accuracy, contributing to the continued reliability of CMUT devices in practical applications.

Chapter 6: Conclusions & Future Work

This research aimed at development of a CMOS-compatible fabrication process for CMUTs, optimizing an 11-step fabrication flow with five photomasks for precise patterning. These masks were designed for (1) the bottom electrode layer, (2) the sacrificial layer, (3) the top electrode, (4) the bonding pad, and (5) the membrane structure. The integration of fabrication techniques, including substrate cleaning, dielectric and electrode deposition, etching, and HF vapour dry release, resulted in a scalable and reproducible approach potentially suitable for medical imaging applications. The sacrificial release process was optimized to mitigate stiction risks, ensuring precise membrane formation while minimizing residual stress.

A comprehensive literature review explored CMUT working principles, applications in diagnostics and therapy, and comparisons with PMUTs. CMUTs demonstrated superior electromechanical coupling and frequency response, reinforcing their suitability for high-resolution medical imaging.

Analytical modelling applied Hooke's Law and Euler-Bernoulli Beam Theory to straight beams and was extended to meander structures, assessing axial and bending stiffness effects. The meander beam design was investigated as a strategy to enhance CMUT sensitivity, presenting a promising approach for performance improvements. Photolithography with photomask design using COMSOL contributed to the reproducibility and accuracy of the structures.

Experimental results confirmed stable electrical behaviour and minimal capacitance interference from parasitic effects, ensuring reliable performance across a broad frequency range. *C-F* and *C-V* measurements validated the fabrication process, confirming the integrity of the SiO_2 sacrificial layer and Si_3N_4 dielectric layer. The measured permittivity was approximately 4.3 for sputtered SiO_2 and around 7.5 for PECVD Si_3N_4.These results are in close agreement with the reported dielectric constants of 3.9 for SiO_2 and 7.22 for Si_3N_4, verifying materials consistency and fabrication precision. The HF vapour etching process efficiently removed SiO_2 but presented challenges, including slower-than-expected undercut etch rates and unintended SiC layer etching. Stress contour analysis confirmed undercut progression; however, electrical contact leg delamination occurred due to accumulated mechanical stress. Minor resonance fluctuations were attributed to electromechanical interactions in the probe station, which can be mitigated in future studies by improving mechanical stability during measurements.

Overall, this thesis marks an initial step in enhancing CMUT sensitivity through meander beam integration and continuous refinement of fabrication techniques. Future advancements will build upon these findings with a focus on advancing CMUT fabrication by refining the sacrificial release process to enhance performance and reliability. While HF vapour etching has demonstrated efficient SiO_2 removal, challenges such as slower-than-expected undercut etch rates and unintended etching of the SiC layer must be addressed. Additionally, delamination of the electrical contact leg due to accumulated mechanical stress requires further refinements to ensure structural stability. To mitigate these issues, an Al protective mask, Figure 6-1, will be incorporated to shield the underlying layers during HF vapour etching.

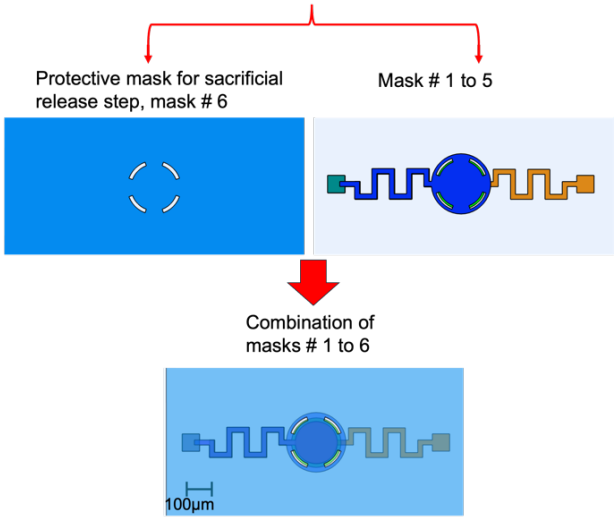


Figure 6-1: Design of Mask No. 1 to 5, along with the protective Al Mask No. 6, optimized for the HF vapour release step of the sacrificial layer in future fabrication.

This mask will cover the sample, leaving designated release holes to provide controlled access to the sacrificial layer, improving structural preservation and enabling more controlled material removal. Further enhancements will involve replacing the top electrode with Pt or Molybdenum (Mo) to facilitate integration with the Al protective mask, thereby minimizing stiction risk and ensuring a more uniform release process. Additionally, substituting SiO_2 with Aluminium oxide (Al_2O_3) as the bottom passivation layer will improve compatibility with HF vapour etching due to its higher selectivity, leading to increased device durability and reduced parasitic capacitance.

Final numerical modelling and fabrication, along with the optimized meander design, will be implemented to further enhance CMUT sensitivity and electromechanical efficiency. These refinements will expand the applicability of CMUTs in high-performance medical imaging and diagnostic systems, supporting continued innovation in CMUT technology.

Appendices

Appendix A: Clean room processes and tools

A.1 Cleaning:

Cleaning is a critical step in every fabrication process, as residual particles or organic contaminants can significantly impact the accuracy, adhesion, and overall reliability of the final structure. The cleaning process generally consists of two main steps: ultrasonic cleaning, and plasma ashing.

A.1.1 Ultrasonic cleaning:

The process begins with ultrasonic cleaning, which utilizes ultrasound waves to create cavitation cloud in a liquid medium, as Figure A-1 depicts.

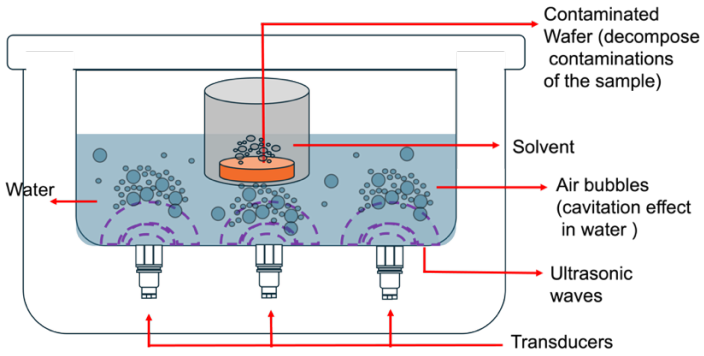


Figure A-1: Schematic diagram of the ultrasonic cleaning process, illustrating the generation of ultrasonic waves, cavitation bubble formation, and the cleaning action on submerged objects.

These bubbles dislodge and remove residual particles and contaminants from the surface of the substrate. This step is typically carried out in a sequential solvent-based cleaning cycle, beginning with five minutes in acetone, followed by five minutes in IPA, and concluding with five minutes in deionized water (DI). To minimize cross-contamination, it is recommended to use the same beaker throughout the process while sequentially replacing each solvent. The substrate should remain submerged in the beaker to avoid exposure to airborne contaminants. After solvent-based ultrasonic cleaning, it is crucial to dry the sample properly to prevent water spots, residue buildup, or oxidation. The most effective method for this is drying with N_2 gas, that removes moisture quickly and uniformly from the surface.

A.1.2 Asher

In this work, following the drying process, plasma ashing is carried out in the YES G1000 Asher to remove any remaining organic residues or surface contaminants. As shown in Figure

A-2, this process occurs in a vacuum chamber where a gas, typically O_2 or a fluorine-based compound, is ionized using RF or microwave power. The ionized gas generates reactive species that interact with the substrate, breaking down and removing microscopic organic particles. Plasma ashing prepares the substrate for subsequent fabrication steps such as deposition, lithography, or etching.

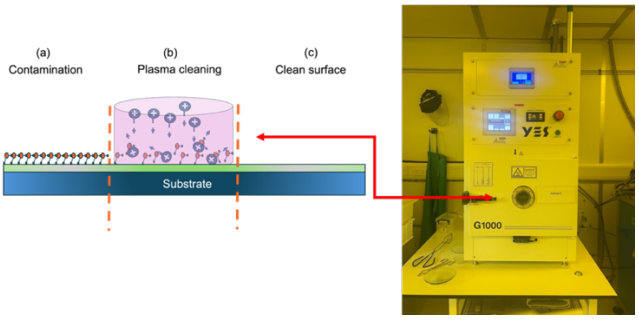


Figure A-2: Schematic representation and real-world setup of the Asher (G1000, Yield Engineering System, YES, USA) used for ashing organic materials.

In addition to its chemical reaction with organic material, plasma has a physical effect, where energetic ions lightly bombard the surface to aid in residue removal. The byproducts of this process are continuously evacuated by the vacuum system, preventing redeposition on the wafer. Asher is designed for batch processing, allowing high-throughput and uniform removal of residual photoresist. It ensures thorough cleaning of designated areas of the pattern, removing photoresist from the glass regions of the mask in positive photoresist processes and from the Cr regions in negative photoresist applications. Ensuring thorough cleaning and effective drying at each stage supports precision and consistency, ultimately improving the overall quality of the final structures.

A.2 Photolithography

A.2.1 Photoresist spin coating

Figure A-3 illustrates the process of photoresist deposition and spin coating to achieve a uniform and controlled film thickness on a substrate.

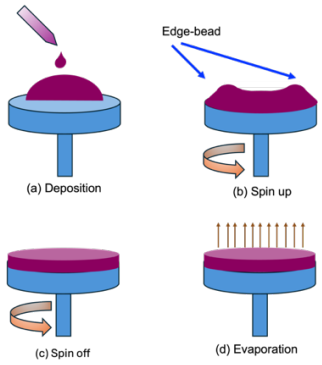


Figure A-3: General process of photoresist deposition and spin coating.

This process consists of several stages, including photoresist dispensing (a), spin coating (b & c), evaporation (d), and curing, each of which must be carefully controlled. The process begins with the deposition of photoresist using a dispenser, Figure A-3 (a), where a specific volume of photoresist is carefully dropped onto the centre of the wafer or substrate. The amount of resist dispensed plays a significant role in achieving the desired thickness, as an insufficient amount may result in incomplete coverage, while excess resist may cause issues such as material wastage and coating irregularities. As shown in Figure A-3 (b), edge bead formation in spin coating happens when excess material builds up around the edges of a substrate. This occurs because surface tension and viscosity prevent the coating from spreading evenly and cause problems like uneven film thickness, difficulties in photolithography alignment, and poor adhesion of subsequent layers. To prevent edge beads, manufacturers use techniques like Edge Bead Removal (EBR), where solvents are applied to dissolve excess material at the edges. Adjusting spin parameters, such as speed and acceleration, can also help create a more uniform coating. As the spinning continues in (c), excess resist expelled outward and make a uniform coating. The thickness of the resist layer is primarily determined by the spin speed, and viscosity of the resist. After the spinning step, solvent evaporation occurs, (d).

A.2.2 Soft bake

Figure A-4 illustrates the soft bake step on a hot plate which takes place after resist deposition. To further remove residual solvents and enhance resist adhesion, the wafer undergoes a soft bake step, typically on a hot plate at a controlled temperature.

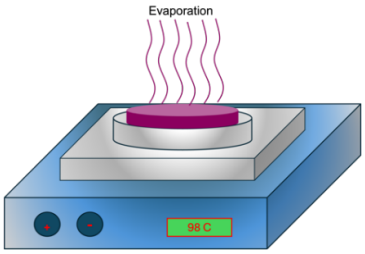


Figure A-4: Hot plate used for the baking step in photolithography.

Adjusting the soft bake temperature is essential for attaining the desired resist properties and ensuring optimal lithographic performance [198]. Overheating during soft bake can result in excessive fluidity, leading to resist overflow and uneven thickness while insufficient baking may leave residual solvents, compromising resolution. Positive resists like S1818 perform optimally at higher bake temperatures between 130-150°C [199]. Proper control of soft bake conditions prepares the photoresist effectively, minimizing defects and creating the foundation for accurate alignment, exposure, and development in the photolithography process.

A.2.3 Alignment and exposure

The mask aligner, Mask aligner 6 (MA6) in this work, features a movable chuck, which allows fine-tuned adjustments to align the new pattern with the existing features on the wafer. Figure A-5 illustrates the operation of the MA6 system in the photolithography process with clarity.

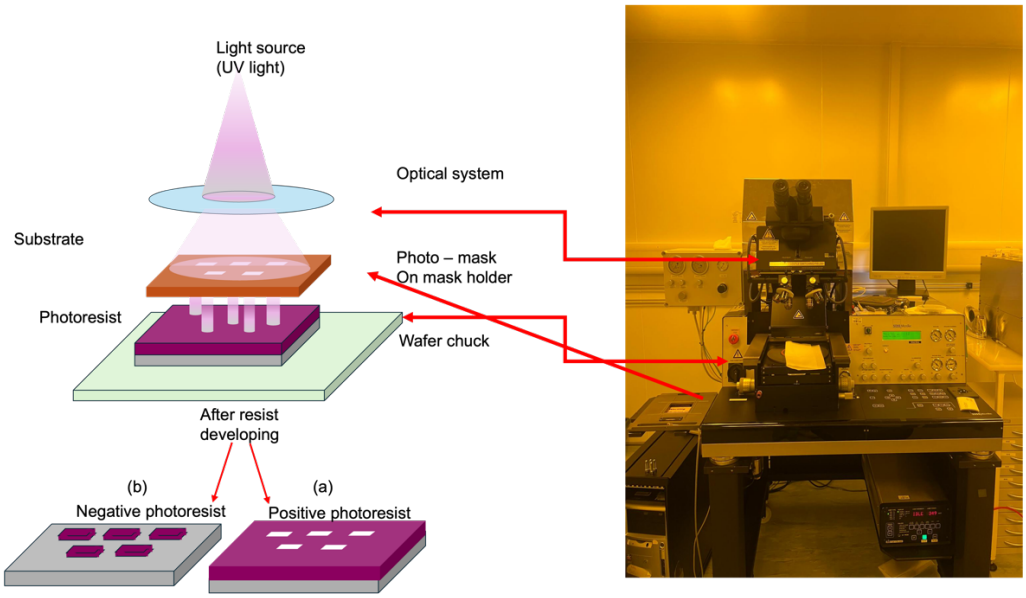


Figure A-5: A schematic representation of the role of the Mask aligner (MA6, SUSS MicroTec, Germany) in the photolithography process.

During this process, the sample and mask are carefully placed inside the mask aligner, where alignment is achieved using alignment markers present on both the sample and the mask.

Proper alignment is critical to avoid layer mismatches, which can lead to defects in the final device. Once the alignment is set, the photoresist is exposed to UV light for a specific duration known as the exposure time. This exposure chemically alters the photoresist, defining the areas that will be developed in subsequent steps depend on type of photoresist. The accuracy of this stage determines how well the intended design transfers onto the wafer. The cleanroom's yellow lighting is essential because photoresists are highly sensitive to shorter wavelengths of light. Using this lighting prevents unintended exposure before the actual photolithography process. Figure A-6 shows the alignment markers used in this work, which enable precise alignment through the MA6 system.

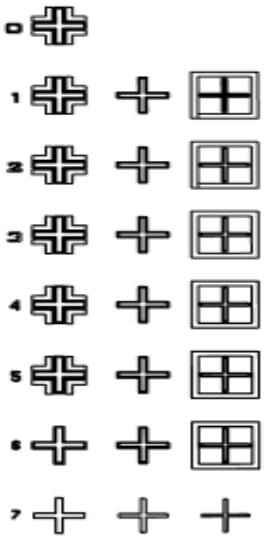


Figure A-6: Alignment markers used on the photomask for precise layer alignment in the lithography process.

Types of photoresists

Figure A-5 (a) illustrates the resulting pattern for a positive photoresist after exposure to UV light. The interaction between mask polarity and photoresist type determines how exposed and unexposed areas respond during development. In a positive photoresist process, the regions exposed to light become soluble in the developer and are subsequently removed, while the unexposed areas remain intact. The transparent sections of the mask allow light to pass through, exposing the photoresist and making it susceptible to development, whereas the Cr coated regions block light, preserving the unexposed areas. In contrast, in Figure A-5 (b), a negative photoresist process results in the exposed regions becoming chemically cross-linked, making them resistant to the developer, while the unexposed areas dissolve. In this case, the Cr portions of the mask block light, ensuring the underlying photoresist remains unexposed and removable, while the transparent glass areas allow light to expose and solidify the photoresist, keeping it on the wafer after development.

A.2.4 Development

Development process, Figure A-7, involves submerging the sample in a suitable developer solution, which selectively removes either the exposed or unexposed regions of the photoresist, depending on whether a positive or negative resist is used.

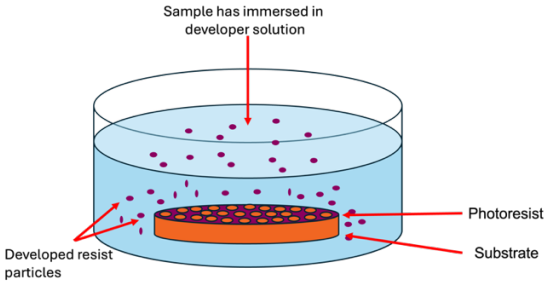


Figure A-7: Schematic representation of the general photoresist developing process in photolithography.

During development, the soluble portions dissolve, unveiling the intended pattern on the wafer. This structured pattern acts as the foundation for subsequent processes such as etching, doping, or metal deposition. The choice of developer is crucial, as each photoresist is formulated to work with a specific chemical solution. Alkaline solutions like TMAH are commonly used for developing positive-tone resists, while organic solvents are typically employed for processing negative-tone resists [200]. TMAH development generally results in a smoother surface compared to organic solvent-based methods [201]. However, some researchers have explored using TMAH for negative resists to enhance optical contrast and resolution [200]. The developer's composition, including aspects such as cation size and solvent polarity, significantly impacts resist performance [202]. Choosing an inappropriate developer can result in issues such as excessive etching, insufficient development, or contamination, potentially compromising the resolution and integrity of the final pattern. Moreover, the developer must be carefully selected to prevent adverse interactions with the underlying material. Additionally, optimizing process parameters, including development time, temperature, and agitation, is crucial for achieving high-resolution and consistent results.

A.3 Physical Vapour Deposition

PVD is a technique used to coat surfaces with thin layers of material by converting the material into a vapour and allowing it to condense onto a target surface. This process occurs in a vacuum, ensuring a clean, high-purity, and uniform coating. The two primary methods of PVD, sputtering and electron-beam evaporation, each offer unique advantages and will be explored in detail in the following section.

A.3.1 Sputtering

Sputtering is a widely used PVD technique for depositing films onto various substrates. It is valued for its ability to produce uniform coatings with strong adhesion, making it particularly effective for applications that require consistent film thickness and adhesion to sidewalls. Sputtering enables the controlled transfer of material from a target source to a substrate through ion bombardment. Figure A-8 illustrates the sputtering process, Which the Ar gas is introduced into the chamber through the gas inlet, with its flow regulated by the mass flow controller to maintain stability.

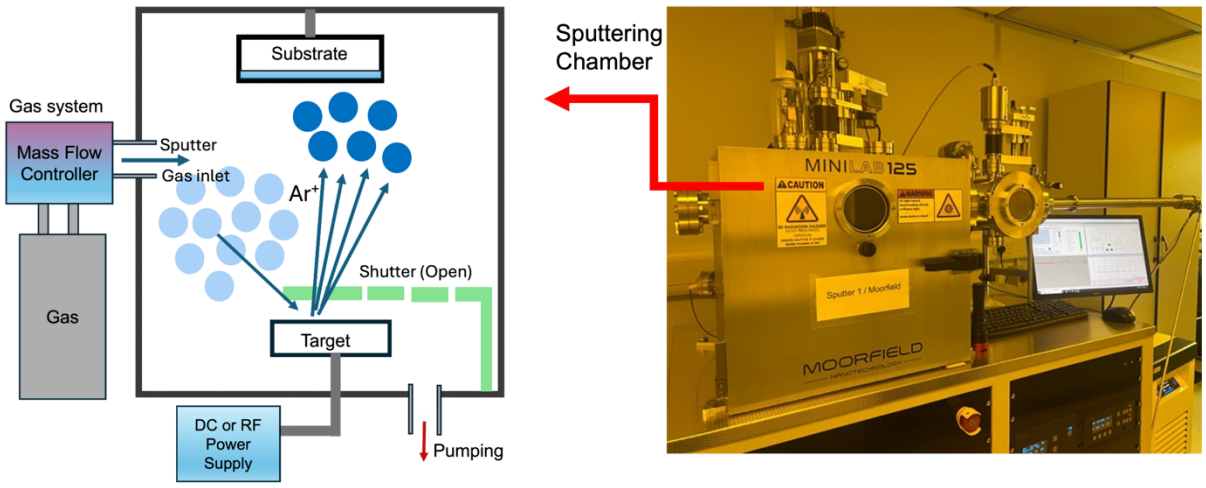


Figure A-8: Schematic representation and actual setup of a sputtering (MINILAB 125, Moorfield Nanotechnology, UK) system for thin-film deposition.

A DC or RF power supply applies a high voltage to the target material, generating a plasma that ionizes the Ar atoms. The resulting positively charged Ar ions accelerate toward the negatively charged target, where they collide with the surface, transferring momentum and causing atoms to be ejected from the target material. These ejected atoms travel through the vacuum chamber and settle onto the substrate, forming a uniform thin film. The shutter mechanism controls the deposition process, opening to allow material deposition and closing when calibration or system stabilization is required. This method is especially effective for depositing materials such as metals, oxides, and nitrides while maintaining good step coverage and uniformity across the substrate. The choice between DC and RF supplies depends on the target material, with direct current sputtering commonly used for conducting materials and RF sputtering preferred for insulating or dielectric materials.

Effect of incidence angle on deposition rate and sputtering yield (optimization in sputtering processes)

Whenever the sputtering target is changed, the deposition rate varies due to the target's angle within the chamber; therefore, re-optimization is necessary. The deposition process follows the cosine law distribution and can be expressed as:

$$R(\alpha_i) = R_0 Cos^n(\alpha_i). \quad \text{Eq. A.1}$$

where $R(\alpha_i)$ represents the deposition rate at an incidence angle α_i, R_0 is the deposition rate at normal incidence ($\alpha_i = 0$), n is a material and process-dependent factor influenced by sputtering conditions. Figure A-9 shows the arrangement of target and sample holder in sputtering chamber.

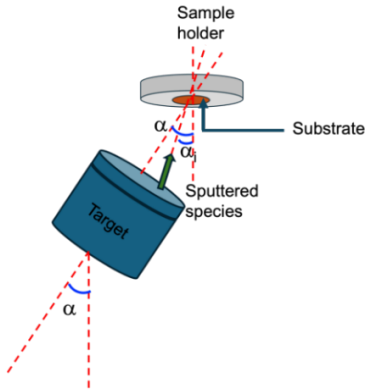


Figure A-9: Schematic representation of the target and sample holder arrangement inside the deposition chamber.

As α_i increases, fewer particles contribute to deposition due to flux changes and increased scattering, resulting in a reduced film growth rate. An increase in α_i typically results in a reduction in film thickness [203]. Research indicates that as α_i increases, the sputtering yield tends to rise, peaking within the range of approximately 70° to 85° [204], [205]. This trend is observed across different ion energies, target materials, and ion species [206]. Since, sputtering systems do not have an automated thickness control mechanism, thickness optimization must be performed manually for each material and target configuration. To optimize the process, a test deposition is conducted by placing a free substrate inside the chamber with a small area masked using tape. An estimated recipe is initially selected based on previous deposition parameters for the same material. After running the process, the thickness of the deposited layer is measured around the taped region using a profilometer. By analysing the measured thickness along with the deposition duration and flow rate, the required process time and flow rate can be adjusted to the desired thickness.

A.3.2 Electron-beam evaporator

Figure A-10 shows EVAP 7, another tool that utilizes PVD technique for thin-film coating applications.

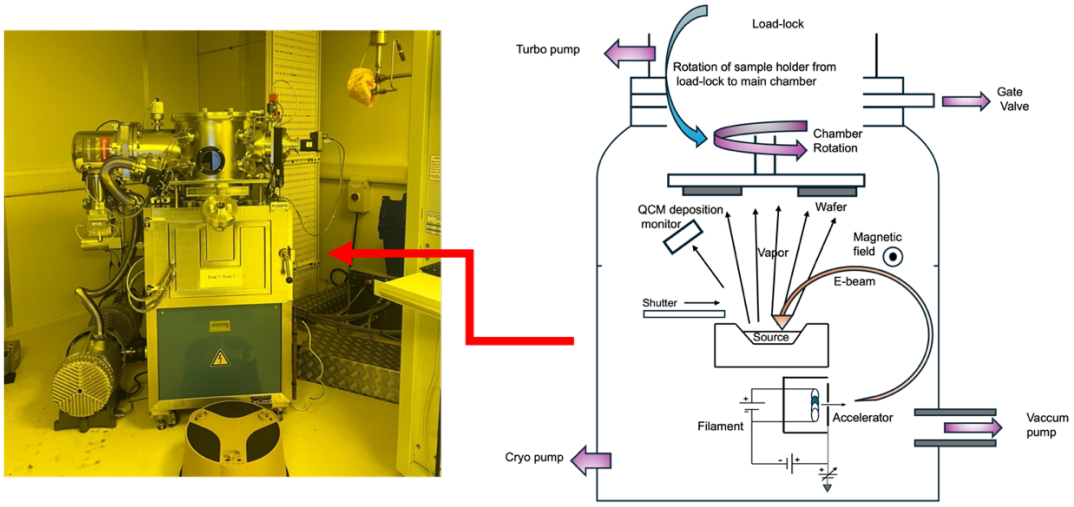


Figure A-10: Schematic representation and setup of Electron beam evaporation (EVAP 7, Plassys, France).

EVAP 7 functions by using a high-energy electron beam to heat and evaporate a target material inside a vacuum chamber. The process starts when an electron beam is generated from a heated filament and is directed towards the target material using electromagnetic fields. The energy from the electron beam causes the material to reach its evaporation point, producing a vaporized stream of atoms or molecules. These vaporized species travel in a straight-line trajectory through the vacuum and condense onto a wafer or substrate, forming a thin film. A quartz crystal microbalance (QCM) deposition monitor is used to precisely measure the deposition rate and thickness of the film in real time. A shutter mechanism is positioned between the evaporation source and the substrate, allowing precise control over when deposition starts and stops. The high vacuum environment inside the chamber is essential for minimizing contamination and ensuring that the evaporated atoms reach the substrate without colliding with residual gas molecules. Compared to other PVD methods, this method offers high deposition rates, excellent film purity, and precise thickness control.

A.4 Chemical Vapour Deposition

CVD is a technique used to deposit thin films by initiating chemical reactions of gaseous precursors on a substrate surface. This method provides precise control over film composition, thickness, and uniformity. Among the various CVD techniques, PECVD is commonly used in

this fabrication due to its ability to enhance film properties and deposition efficiency. The details of PECVD will be discussed in the following section.

A.4.1 Plasma - Enhanced Chemical Vapour Deposition

PECVD is a technology in the semiconductor and electronics industry, enabling thin films to be deposited at much lower temperatures compared to traditional methods, typically between 100–400°C [207]., which makes PECVD particularly well-suited for temperature-sensitive materials. What makes PECVD stand out is its use of plasma to initiate chemical reactions, ensuring precise and efficient material deposition. A typical PECVD system, such as the Plasma-Pro 100, Figure A-11, illustrates how this process works.

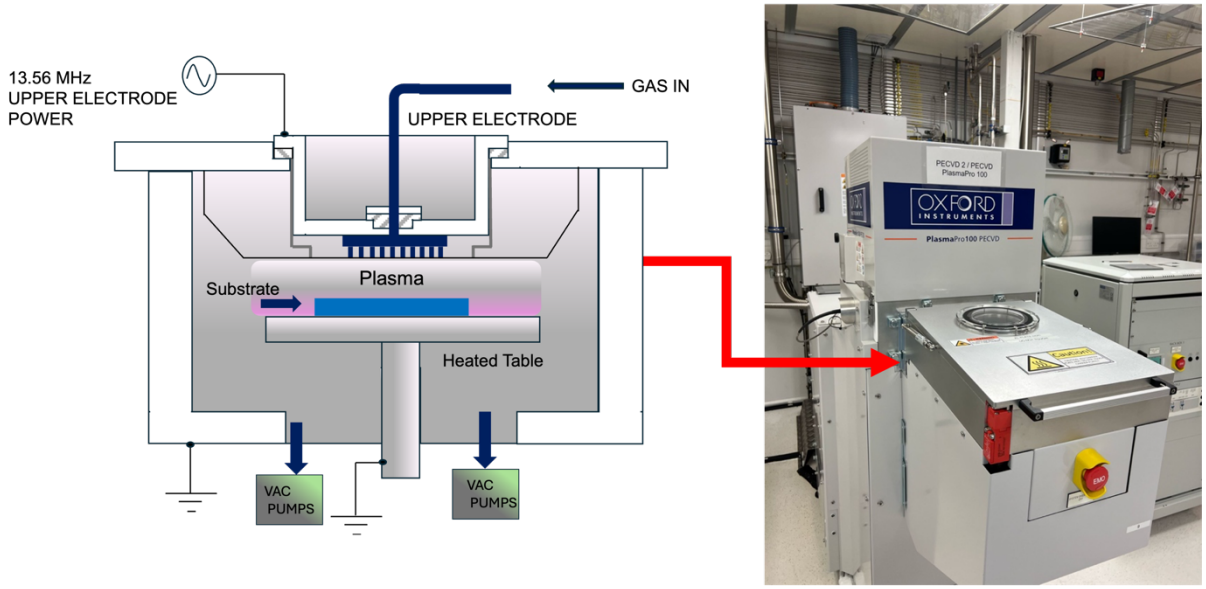


Figure A-11: Schematic representation and setup of PECVD (PlasmaPro 100, OXFORD Instrument, UK).

The process takes place inside a vacuum chamber, where gases are introduced and ionized by plasma energy. The electric field generated by RF power excites and breaks down these gases into highly reactive species. These active species then move toward the substrate, positioned beneath the plasma, where they react to form a thin film. To enhance the deposition process, the substrate is heated, optimizing material growth and properties. An essential factor in the process is the interaction between gas chemistry and plasma, which influences the characteristics of the deposited film. When depositing SiO_2, gases like O_2 or N_2O act as oxidizers, reacting with SiH_4 to form the SiO_2 layer. The reactions involved are:

$$SiH_4 + O_2 \rightarrow SiO_2 + 2H_2$$

$$SiH_4 + 2N_2O \rightarrow SiO_2 + 2N_2 + 2H_2$$

To keep the process smooth and uniform, N_2 or Ar is used as a carrier gas, helping distribute the reactants evenly.

For Si_3N_4 deposition, SiH_4 is combined with a N_2 source like NH_3. NH_3 is often preferred because it easily breaks down in plasma, creating highly reactive N_2 species that improve film formation. The chemical reactions for Si_3N_4 deposition are:

$$3SiH_4 + 4NH_3 \rightarrow Si_3N_4 + 12H_2$$

$$3SiH_4 + 2N_2 \rightarrow Si_3N_4 + 6H_2$$

As with SiO_2, N_2 or Ar helps maintain stability in the gas flow and deposition process. For amorphous Si films, SiH_4 is used, breaking down in plasma to deposit pure silicon:

$$SiH_4 \rightarrow Si + 2H_2$$

Hydrogen (H_2) is often added to fine-tune film properties, reducing defects and improving stability.

A.5 Etching methods and tools

Etching techniques and tools are broadly categorized into two main types: wet etching and dry etching, each offering distinct advantages depending on the application. Prior to examining these techniques, it is essential to establish foundational concepts, such as selectivity which influence the effectiveness and optimization of the etching process. Selectivity, defined as the ratio of etch rates between distinct materials. Figure A-12 shows the impact of material selectivity in the etching process, demonstrating how different materials react under etching conditions.

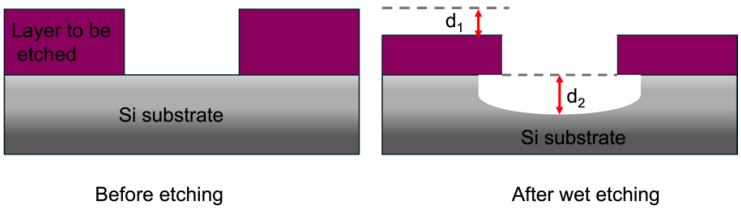


Figure A-12: Schematic illustration of selectivity in the etching process, highlighting material removal differences between the etched layer and the substrate.

The selectivity ratio is mathematically expressed as:

$$Selectivity = \frac{Etch\ rate\ of\ bottom\ layer\ (=\frac{d_2}{t_e})}{Etch\ rate\ of\ higher\ layer\ (=\frac{d_1}{t_e})} \quad \text{Eq. A.2}$$

where d_1 is the thickness of the higher layer etched over time, t_e. d_2 is the thickness of the bottom layer etched, and S_e represents the selectivity of the etching process. A high selectivity ratio ($S_e \gg 1$) indicates that the etching process predominantly removes the upper layer while leaving the bottom layer mostly intact. This is desirable in cases where a layer, such as Si_3N_4 in this work, must remain unetched while a sacrificial SiO_2 layer is removed. Conversely, a low selectivity ratio ($S_e \approx 1$) means that both materials etch at nearly the same rate, which may lead to undesirable substrate damage or excessive undercutting. In CMUT applications, selective etching is essential for shaping cavity structures while maintaining the integrity of functional dielectric layers.

The choice of etchant greatly affects both the etch rate and the resulting surface quality [208], while etching behaviour is affected by material properties such as crystallographic orientation and defect structures [209]. Etching can be either isotropic or anisotropic, with rates governed by these material characteristics and diffusion constraints [210]. In plasma etching, Etch rate and surface morphology are further shaped by process parameters such as platen power, Inductively Coupled Plasma (ICP) coil power, and working pressure [211], [212]. A thorough understanding of these factors is crucial for designing selective etching methods for different materials, including III-V semiconductors [213] and SiC [212] with wet and dry etching techniques explained in the following section.

A.5.1 Wet etching

The wet etching process, Figure A-13, where the substrate is first immersed in a chemical bath, allowing the etchant to dissolve exposed regions while preserving masked areas.

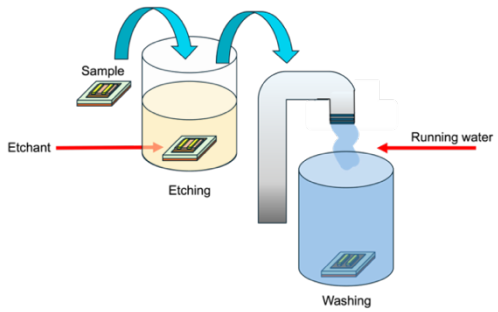


Figure A-13: Schematic representation of the wet etching process in nanofabrication.

Following etching, the substrate undergoes a rinsing step to eliminate residual chemicals, followed by a drying process to prevent adhesion-related issues, particularly in MEMS applications. Precise regulation of parameters such as temperature, solution composition, and agitation are crucial for ensuring consistent results in device fabrication [214]. Wet etching is

typically more economical and provides high selectivity; however, its isotropic nature can cause undercutting and restrict resolution [215].

A.5.2 Dry etching

Dry etching, especially RIE, provides superior anisotropy and precision, allowing for the fabrication of finer features with enhanced step definition [216]. RIE provides benefits over wet etching through its anisotropic properties and capability to create high-aspect-ratio structures [217]. This process employs plasma to produce reactive species that enable both chemical and physical etching, facilitating selective and directional material removal [218]. However, dry etching may lead to plasma-induced damage, which can degrade device performance [219]. Compared to wet etching, RIE offers greater precision in controlling critical dimensions while minimizing undercutting [215]. Etch rate, selectivity, and anisotropy can be controlled by optimizing process parameters such as gas composition, pressure, and power [210]. Working principle of Plasmalab 80, is shown in Figure A-14.

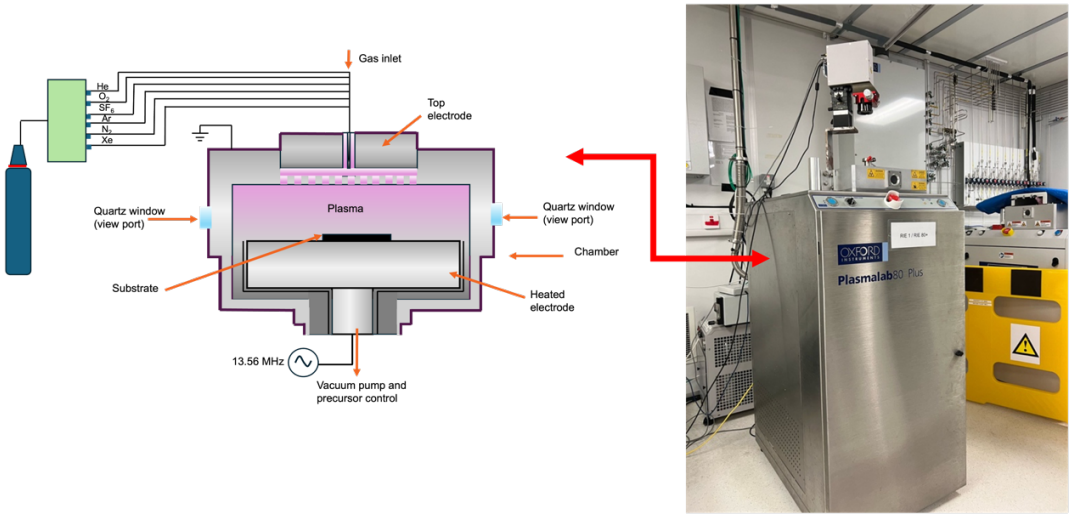


Figure A-14: Schematic representation and actual setup of the RIE system (Plasmalab 80 Plus, OXFORD Instruments, UK), used for dry etching in nanofabrication.

The RIE etching chamber operates in a controlled vacuum environment where plasma facilitates material removal. When RF power is applied to the lower electrode, plasma forms, initiating the etching process. The powered electrode, which holds the wafer or substrate, develops a negative bias, attracting positively charged ions that strike the surface and remove material in a directional manner, enabling anisotropic etching with minimal sideways erosion. Reactive gases enter the chamber through controlled inlets and break down into reactive species upon plasma excitation. These species chemically interact with the substrate, forming volatile

byproducts that are removed by the vacuum system. The choice of gases influences etching characteristics such as selectivity, speed, and profile, ensuring precision in material patterning. Fluorine-based gases, including sulphur hexafluoride (SF_6), Carbon Tetrafluoride (CF_4), and Trifluoromethane (CHF_3), are widely used for etching silicon-based materials like Si, SiO_2, and Si3N4, as they provide effective chemical reactions for material removal [220], [221]. On the other hand, chlorine-based gases such as chlorine (Cl_2) and Boron trichloride (BCl_3) are preferred for metal etching due to their ability to form volatile metal chlorides [222], [223].

Wet etch and Dry etch differences

Figure A-15 shows the isotropic and anisotropic characteristics of wet and dry etching, highlighting their impact on material removal during semiconductor fabrication.

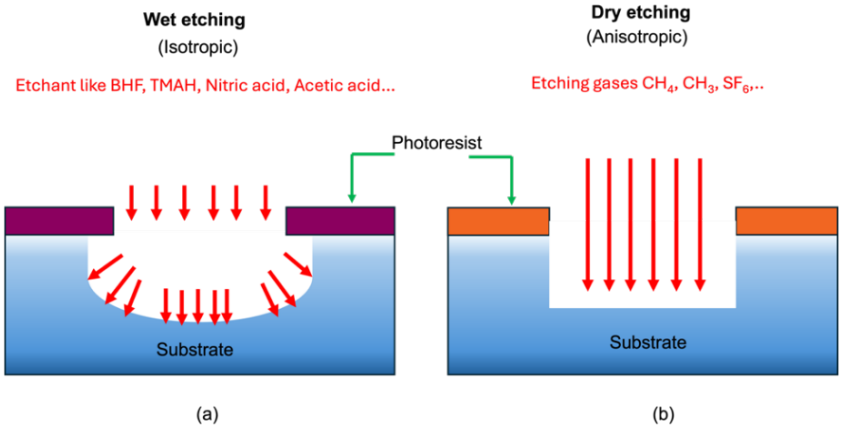


Figure A-15: Schematic illustration comparing wet and dry etching processes, highlighting their different etchants, mechanisms, and effects on the substrate.

As depicted in this figure, wet etching exhibits an isotropic nature, meaning that material is removed uniformly in all directions. This behaviour can lead to undercutting, where the etchant extends laterally beneath the masking layer, potentially compromising the precision of the etched features. In contrast, dry etching follows an anisotropic pattern, where material removal occurs predominantly in a vertical direction, minimizing lateral etching and undercutting. This characteristic allows for the fabrication of well-defined, high-aspect-ratio structures with greater precision and control over feature dimensions. Wet etching is preferred for applications requiring high selectivity and uniform removal whereas dry etching is essential for achieving precise patterning and advanced microfabrication processes [224].

A.6 HF vapour release tool

Figure A-16 (a) illustrates HF vapour release process, a reliable method for removing sacrificial layers in CMUT fabrication.

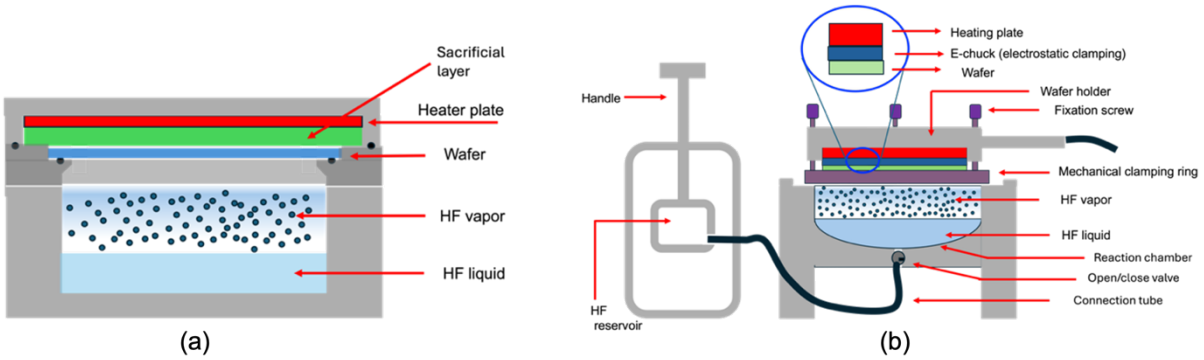


Figure A-16: Schematic representation of (a) an HF vapour release tool and (b) a VPE system used for dry etching in nanofabrication.

By converting a controlled quantity of liquid HF into vapour within a reaction chamber, this technique selectively etches sacrificial layers—typically SiO_2—beneath structural materials, eliminating the need for water rinsing and drying. It minimizes stiction, enables the release of freestanding microstructures with gap sizes as small as 50 nm [225], and supports cantilevers up to 5000 µm long [226], offering higher yields and longer detachment lengths than wet-release methods [227]. Etch rate and uniformity depend on factors such as release hole size and distribution, as well as cavity dimensions [228], with optimization enhancing release efficiency while maintaining consistent performance [229]. Compatible with IC fabrication, this method has been successfully applied to materials like phosphorus-doped polysilicon [230] and SiO_2 [231].

Figure A-16 (b) depicts a Vapour Phase Etching (VPE) system utilizing HF, comprising a reaction chamber, an etchant reservoir, and a wafer holder with an electrostatic chuck [232]. In VPE, liquid HF is vaporized under regulated conditions to interact with the wafer surface [233], providing enhanced process control and preventing stiction issues common in wet etching [234]. Like liquid-phase etching, VPE achieves selective removal between oxide and nitride layers [235]. Fine-tuning parameters such as HF and IPA flow rates, temperature, and pressure is critical to achieving high etch rates, uniformity, and efficient release of intricate MEMS structures while ensuring compatibility with IC manufacturing [226], [229].

Both HF vapour release and VPE leverage advanced vapour-phase chemistry for high-precision material removal. While HF vapour release focuses on selectively releasing sacrificial layers in CMUT fabrication, VPE represents a broader etching methodology widely used in semiconductor processing, offering versatility across applications.

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