Through Silicon Vias for the 3D Integration of Superconducting Quantum Circuits

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Abstract

The development of superconducting quantum computing has seen a rapid acceleration in recent years. The number of controllable qubits fabricated on-chip has steadily increased in the pursuit of more computational power. 3D integration has become a key enabling technology for the scalability of these larger systems due to the architectural flexibility it offers, mirroring its impact on conventional electronics. As part of this development, superconducting through-silicon vias (TSVs) have recently emerged as a method of breaking the wiring plane and routing signals through the substrate as well as for other, more novel, applications such as acting as the capacitive component of a new type of superconducting qubit.

This thesis will discuss the simulation, fabrication and measurement of superconducting TSVs. Using ANSYS HFSS electromagnetic simulation software, the geometric parameters of TSV-integrated co-planar waveguides were optimised for the transmission of microwave signals. In addition, a TSV-integrated tunable qubit coupler was simulated and the effect of the device's geometry on the various capacitances within the device, and in turn on the device's parameters, such as the charging and Josephson energies, was investigated. As a leading cause of signal degradation in electronic devices, crosstalk should be removed from devices as far as possible. Varying the number and arrangement of grounding TSVs was explored as a strategy for the mitigation of crosstalk between adjacent TSVs and it was found that using 4 ground TSVs to shield the signal TSV resulted in a dramatic reduction in crosstalk, with values of $S_{41} < -140$dB at 4GHz.

For the fabricated samples, a comparison was made of different Bosch etches used to define the TSVs and it was determined that the ICP power and total etch time were highly influential in the degree of sidewall roughness. Methods of sidewall smoothing were also investigated, with KOH wet etching found to offer near atomic-level smoothness. Finally, the fabricated samples were characterised using, among other methods, cryogenic spectroscopy. A novel application of the method of calibrated cryogenic S-parameter measurement to superconducting TSVs is also presented, with the TSV-integrated co-planar waveguide structure under test exhibiting a peak transmission of -1.44dB.

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Just as it takes a village to raise a child, it also takes a research group to complete a PhD - or in my case, two research groups and more people besides. As such, I would like to take this opportunity to extend my gratitude to the many people that made it possible for me to reach this point.

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Declaration

I certify that the thesis presented here for examination for a PhD degree of the University of Glasgow is solely my own work other than where I have clearly indicated that it is the work of others (in which case the extent of any work carried out jointly by me and any other person is clearly identified in it) and that the thesis has not been edited by a third party beyond what is permitted by the University's PGR Code of Practice. The copyright of this thesis rests with the author. No quotation from it is permitted without full acknowledgement. I declare that the thesis does not include work forming part of a thesis presented successfully for another degree. I declare that this thesis has been produced in accordance with the University of Glasgow's Code of Good Practice in Research. I acknowledge that if any issues are raised regarding good research practice based on review of the thesis, the examination may be postponed pending the outcome of any investigation of the issues.

Chapter 1

Introduction

The *qubit*, a contraction of "quantum bit", is the unit of information that is manipulated in the operations of a quantum computer. Depending on the context in which the word is used, it may refer to one of two things. Logical qubits are the theoretical ideal of a qubit, and these are the objects that are processed in algorithms for the extraction of the quantum information they represent. Physical qubits are the realisation of these logical qubits in the real world. They can take the form of superconducting circuits, arrays of atoms suspended in electromagnetic fields, photons, or other even more exotic manifestations [1–4]. Quantum computing and, therefore, qubits have been a source of excitement and intrigue for physicists and computer scientists since their conception due to the potential for exponential speed-up over classical computing. Highly publicised applications of quantum computing, such as the ability to break RSA encryption via Shor's algorithm for finding the prime factors of an integer, have drawn the eye of world governments and technology monoliths alike and with this has come an unprecedented era of funding and research, with the UK government committing £2.5 billion to quantum research over 10 years from 2024 [5, 6].

Progress in the quantum computing field has, as a result, accelerated at a startling pace. The record for the highest number of qubits in a single gate-based quantum processor is continually being broken and, at the time of writing, is held by IBM's "Condor" chip, with 1121 qubits [7]. This drive towards increasing the number of qubits on a chip represents more than just bragging rights for the company able to hold the record. Improving the scalability of fault-tolerant quantum computers is one of the key challenges facing the development of the technology [8,9]. As with classical computing, the advantages of increasing the number of bits of information that can be manipulated is clear: more information means more computational power means more utility. While classical computing had Moore's law as a guide to their progress, quantum computing faces a different set of challenges.

Large error rates in both single qubits and multi-qubit operations often prohibit the use of single physical qubits as computational units. This is pertinent for many modalities of quantum

computing, but is particularly crucial for superconducting quantum computing, which will be the modality of focus in this thesis [8, 10, 11]. The prevailing way to combat this is to use multiple physical qubits in concert with one another to form one logical qubit [10, 12].

These systems of redundancy are broadly referred to as error-correcting codes. The most prominent error-correcting method in superconducting quantum computing is the "surface-code" which, depending on the type of code used, may need 9 or even 25 physical qubits per logical qubit [10, 12]. Even very recently proposed error-correcting codes implemented in neutral atom computing use as many as 6 physical qubits per logical qubit [13]. This reduction is facilitated by the increased connectivity in this modality, which has not as yet been demonstrated in superconducting quantum computing. The requirement for redundancy, combined with the oft-referred to predication that around 1000 logical qubits will be needed for "useful" quantum computations, highlights the need for scalable methods of fabrication for these devices [8]. Given that each of these devices requires multiple electrical connections for the control and readout of qubits, the two-dimensional (2D) architectures typically used in superconducting quantum processors are severely limiting in the arrangement of devices on-chip. The three-dimensional (3D) integration of superconducting components has, therefore, emerged as a necessary step towards achieving the scalability of superconducting quantum computers [14–16].

Accordingly, various methods of 3D integration have been proposed [14, 17–21]. Novel packaging techniques such as spring-loaded pogo pins, tileable modular qubits and multilayer PCBs break the wiring plane by carrying signals off-chip, while on-chip methods such as through-silicon vias (TSVs), flip-chipping and, recently, liquid metal interconnects achieve this by incorporating additional structures into the fabricated device to provide alternative options for signal routing.

The focus of this thesis is on the development of superconducting TSVs. In particular, it aims to explore the methods of fabrication used to create these devices, including the way in which they are etched into the Si substrates and also the choice of metallisation technique and material used to coat the interior of the devices. These choices will be interrogated using cryogenic characterisation techniques that are widely used in the measurement of superconducting circuits. Further to this, a novel application of calibrated cryogenic S-parameter measurements to TSVs is also presented, which represents a step forward in the analysis of these structures.

This thesis will begin with a review of the theoretical background upon which this research is based, alongside practical experimental techniques that are used in the fabrication and measurement of the devices discussed. This includes an overview of the theory of superconductors and microwave electronics, selected topics in quantum computing and nanofabrication techniques as well as a review of methods of 3D integration currently used in superconducting quantum circuits. Following this is a discussion of TSV-integrated structures that have been simulated using ANSYS HFSS electromagnetic simulation software with the objective of optimising the

geometric parameters of these structures. Chapter 4 will then detail the practical experimental work that was carried out over the course of the project and is divided into sections on the fabrication of devices and the measurement of those devices. Finally, the findings of the thesis will be summarised and suggestions will be offered as to possible improvements and further work that could be carried out in future.

Chapter 2

Background

2.1 Superconductivity

2.1.1 Basic Theory and Properties of Superconductors

Superconductivity is a subject rich in theory and experimental work and a full treatment is far outside the scope of this work. However, it will be instructive to give an overview of some of the fundamental concepts so as to permit discussion of the ways that superconducting quantum circuits take advantage of the peculiar effects unique to superconducting materials. Superconductivity was first discovered in 1911 when it was observed that below a critical temperature, T_c, the resistance of the superconductor falls to zero [22]. Below the same T_c, they also exhibit the related property of expelling magnetic fields from the bulk of the material [23]. This is known as the *Meissner effect* and it indicates that this phenomenon is not simply a case of the material exhibiting perfect conductivity, as this would instead trap magnetic flux in the conductor. It also gives some indication of the existence of a critical magnetic field strength, above which the force responsible for this expulsion will be smaller than the pressure exerted by the expelled field, thus overcoming the Meissner effect [24]. Analogously, there exists a critical current I_c, determined by the properties of the superconductor in question, above which the superconductor will transition to a normal metal phase resulting in a sharp increase in resistivity.

The causes of these effects are explained by the consistent theories of Bardeen-Cooper-Schrieffer (BCS) and Ginzburg-Landau. BCS postulates that below T_c, electrons in the superconductor condense into pairs of opposite momentum and spin. These are known as *Cooper pairs* and are attracted to each other due to the phonon interaction between them overcoming their mutual Coulomb repulsion [25]. These are the charge carriers in superconducting material [24]. Ginzburg-Landau theory predicts that, remarkably, the entire bulk of superconductor can be described by one wave function, $\Psi = |\Psi|e^{i\phi}$, where ϕ is the collective phase of the superconductor and $|\Psi|^2$ is related to the number of Cooper pairs in the material [26].

2.1.2 The Josephson Effect

The *Josephson effect* is the key principle upon which all superconducting qubits are based [27]. Named for its discoverer, Brian Josephson, who was awarded a Nobel prize for his work, it describes the supercurrent dynamics that occur in an arrangement of two superconductors separated by a weak link, which may be an insulator, normal metal or semiconductor. This construction is named a *Josephson junction* and it allows Cooper pairs to tunnel from one superconductor to the other via a process named Andreev reflection [25]. The relations that govern the operation of the junction are:

$$I(t) = I_c \sin\phi(t) \quad (1^{\text{st}} \text{ Josephson Relation}), \tag{2.1}$$

$$V(t) = \frac{\hbar}{2e}\frac{\partial\phi}{\partial t} \quad (2^{\text{nd}} \text{ Josephson Relation}), \tag{2.2}$$

where $I(t)$ is the current through the junction, I_c is the supercurrent supported by the junction, $\phi(t)$ is the phase difference at time t between the two superconductors and $V(t)$ is the voltage across the junction [28]. Note that the 2^{nd} relation is analogous to Faraday's law of induction, which leads to the Josephson junction often being referred to as a non-linear inductor. The significance of this non-linearity will be discussed further in section 2.2.

Electrons in the superconducting electrodes of a Josephson junction are condensed into Cooper pairs when the junction is cooled below the T_c of the material used. The system can be described by two quantities: the capacitive charge $Q(t)$, and the number of Cooper pairs that have tunnelled across the junction $N(t)$. Note that if the junction is connected to a larger electrical circuit, the charge that has flown through the junction, $Q_J(t) = -2eN(t)$, may not necessarily be equal to $Q(t)$ [29].

When the leads of the Josephson junction are joined such that a loop is formed in the circuitry, a generalised flux, ϕ_J, may be used to describe the element. This is defined as the time integral of the voltage across the junction:

$$\phi_J(t) = \int_{-\text{inf}}^{t} V_J(t')dt' \tag{2.3}$$

As mentioned, this is analogous to Faraday's law, except that where the current-flux relation for a linear inductor is $I(t) = \frac{1}{L}\Phi_L(t)$, the Josephson current-flux relation is described by equation 2.1. This is the non-linear aspect of the junction and it is crucial to its use in quantum circuits [29].

2.2 Quantum Computing and Circuit Quantum Electrodynamics

A broad aim of the field of quantum computing is to build a programmable device that mimics the unique properties of a quantum system. *Circuit quantum electrodynamics* (cQED) is the mathematical formalism that quantises and thereby describes the systems of qubits and resonators that, in the superconducting modality, constitute the individual elements of that programmable device [30]. The methods used in this formalism are analogous to those used in cavity quantum electrodynamics and, in particular, a parallel can be drawn between a superconducting qubit coupled to a resonator and a Rydberg atom in a cavity, due to their characteristic frequencies both being in the GHz range. In this model, the qubit and circuit are analogous to the atom and cavity, respectively, hence the use of the name circuit QED. While the devices being considered may be large and contain many atoms, the collective degrees of freedom they possess behave quantum mechanically due to their superconducting properties. Therefore, these degrees of freedom can be engineered to take advantage of their quantum behaviours, such as superposition and entanglement [29].

2.2.1 The Cooper Pair Box and Transmon

When choosing how to construct a qubit, it seems sensible to mimic a system that has been extensively studied and is analytically solvable. One such system is the quantum harmonic oscillator. Fortunately, one of the simplest circuits it is possible to draw is one that exhibits oscillatory behaviour: the LC-oscillator. The quantum-mechanical Hamiltonian of an LC-oscillator may be written:

$$\hat{H} = \frac{\hat{Q}^2}{2C} + \frac{\hat{\Phi}^2}{2L}, \tag{2.4}$$

where $\hat{Q}$ and $\hat{\Phi}$ are the generalised charge and flux circuit coordinates, and C and L are the capacitance and inductance of the circuit, respectively [28]. To bring this closer to the language of superconducting circuits, we define the reduced flux $\hat{\phi} = \frac{2\pi\hat{\Phi}}{\Phi_0}$ and the reduced charge $\hat{n} = \frac{\hat{Q}}{2e}$, giving:

$$\hat{H} = 4E_C\hat{n}^2 + \frac{1}{2}E_L\hat{\phi}^2 \tag{2.5}$$

where $E_C = \frac{e^2}{2C}$, $E_L = \frac{\Phi_0^2}{4\pi^2 L}$ and Φ_0 is the superconducting flux quantum [28]. Note that this is analogous to the Hamiltonian of the quantum harmonic oscillator: $\hat{H} = \frac{1}{2m}\hat{p}^2 + \frac{1}{2}m\omega^2\hat{x}^2$. Therefore, we know that this describes a quadratic potential with equally spaced energy levels: $E_{k+1} - E_k = \hbar\omega_r = \frac{\hbar}{\sqrt{LC}}$. This is promising - here is a quantum electromagnetic circuit whose energy level spacing is determined by the design parameters (capacitance and inductance) and between whose energy levels transitions can be driven. However, the identical spacing between levels prevents the driving energy applied from being able to promote transitions between *spe-*

cific energy levels. An alteration to the circuit is needed so that this spacing is changed. In other words, *anharmonicity* is needed.

This is the critical problem to which the Josephson junction provides a solution. As a non-linear inductor, it may be substituted for the linear inductor in the system, shifting the energy levels of the system such that the first and second transition energies are sufficiently different so as to prevent higher energy levels being accessed. This allows the circuit to be treated as a two-level system with Hamiltonian:

$$\hat{H} = 4E_C\hat{n}^2 - E_J\cos\hat{\phi}. \tag{2.6}$$

$E_J = \frac{I_c\Phi_0}{2\pi}$ is the Josephson energy, where I_c is the critical current of the junction [28]. This describes a *Cooper-pair box* (CPB) - the simplest superconducting qubit. It is named this as it can be imagined as a superconducting island onto which Cooper pairs can tunnel, with E_C being the *charging energy* required to add each electron of the pair to the island, and E_J the *Josephson energy* - which is the proportionality coefficient of the work done in changing the phase across the junction. An illustration of the effect that the replacement of the linear inductor with a Josephson junction has on the energy levels of the circuit is given in figure 2.1.

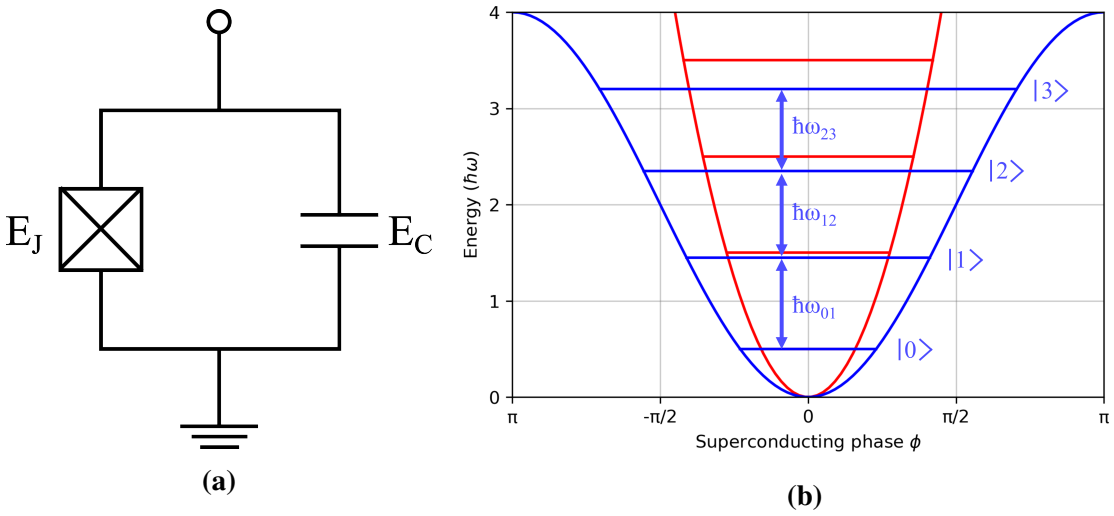


Figure 2.1: (a) Josephson junction qubit circuit diagram showing the Josephson junction and capacitor connected in parallel. (b) Energy level diagram of the quantum harmonic oscillator (red) and Josephson qubit (blue), demonstrating the anharmonicity resulting from the cosinusoidal potential.

The ratio $\frac{E_J}{E_C}$ determines the exact shape of the energy levels [31]. In the $E_C \gg E_J$ regime, the CPB is very sensitive to fluctuations in charge near the superconducting island - which leads to unwanted changes in qubit frequencies [32]. To combat this, the CPB may be capacitively shunted - thereby adding an additional capacitance and increasing the ratio $\frac{E_J}{E_C}$. This does, however, also reduce the anharmonicity of the qubit and the various parameters must be tuned to strike the correct balance [32]. This capacitively shunted CPB is called a *transmon* and is to-

day one of the most widely used types of qubit [33]. There is, of course, a zoo of different types of qubits, ranging from the CPB to more exotic ideas such as cat qubits and topological qubits [4, 34]. Discussion in this work will, however, be restricted to the more prevalent transmon.

In the example circuit described here, E_J is fixed. This can be changed, however, by replacing the single tunnel junction with two in parallel. This two junction loop is known as a *superconducting-quantum-interference-device*, or SQUID [35]. The magnetic flux through this loop can be varied, thus varying E_J. This flux-tunability is extremely useful in that it allows the qubit to be tuned in and out of resonance with other components in the system, giving the operator control over the coupling between these components and a method of executing two-qubit gate operations.

There are many sources that discuss these relations that govern the dynamics of the transmon qubit and so here they will only be stated. The frequency of the transition between the ground and first excited state of a transmon is given, approximately, by [32, 36]:

$$\omega_q = \frac{1}{\hbar}[\sqrt{8E_J E_C} - E_C]. \tag{2.7}$$

The transmon anharmonicity, α, is related to the charging energy by $E_C = h\alpha$ and is typically in the range $|\alpha| \in$ [200MHz, 300MHz] [36]. The Ambegaokar-Baratoff equation relates the critical current of the junction to its normal state resistance, R_N [36]:

$$I_c R_N = \frac{\pi}{2e}\Delta(T)\tanh\frac{\Delta(T)}{2k_B T}, \tag{2.8}$$

where $\Delta(T)$ is the temperature-dependent superconducting gap energy. At $T = 0$K, this reduces to:

$$I_c = \frac{\pi\Delta}{2eR_N} \tag{2.9}$$

allowing the expression of the Josephson energy in terms of R_N, which is simpler to directly measure and design for than I_c:

$$E_J = \frac{\Phi_0\pi\Delta}{2eR_N}. \tag{2.10}$$

One of the defining characteristics of the transmon is its large shunting capacitance and hence insensitivity to charge noise. This is manifested by designing the parameters of the qubit such that $E_J \gg E_C$; typically, $\frac{E_J}{E_C} \approx 50$. This ratio represents a trade-off between sensitivity to charge noise and a sufficiently large anharmonicity to prevent leakage to non-computational higher energy states.

2.2.2 Theory of Qubit Control, Readout and Decoherence

The *Bloch sphere*, depicted in figure 2.2, is an abstract geometrical representation of the state of a qubit that consists of a sphere centred on the origin, conventionally with the ground and excited states at the north and south pole respectively. A pure qubit state can be represented by a point on the surface of the sphere, with the polar angle representing the weighting of ground, $|0\rangle$, and excited, $|1\rangle$, states in the qubit's superposition and the azimuthal angle representing the phase of the qubit [37]:

$$|\Psi\rangle = \cos\frac{\theta}{2}|0\rangle + \sin\frac{\theta}{2}e^{i\phi}|1\rangle . \tag{2.11}$$

This is a useful tool for the visualisation of qubit activity and references are often made to rotations around the Bloch sphere when discussing the gain or loss of energy or phase by a qubit. Decoherence mechanisms are also referred to as being *longitudinal* or *transverse*, evoking the sphere [28].

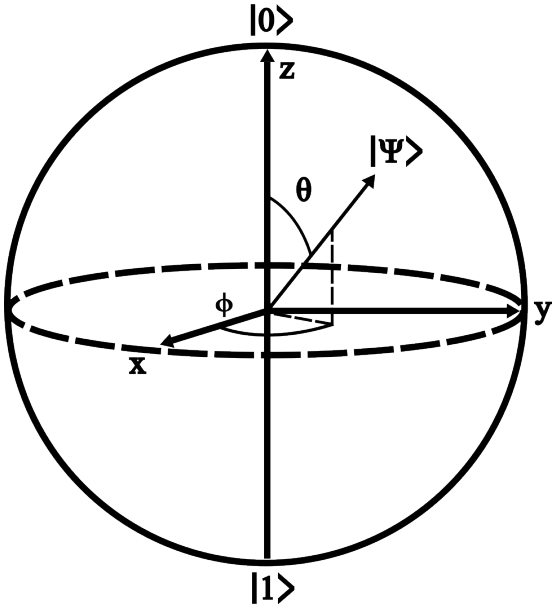


Figure 2.2: The Bloch sphere.

Transitions between qubit states are controlled by signal pulses switched on for some specified time. As the pulse is switched on at resonance, the probability that the qubit is in a given state will begin to oscillate between the $|0\rangle$ and $|1\rangle$ state at the *Rabi frequency*: $P_{0\to1}(t) = \sin^2\frac{\omega t}{2}$. So we may choose the time t, such that the qubit is in state $|1\rangle$ ($t = \frac{\pi}{\omega}$, a π-pulse) or any other superposition of states. A $\frac{\pi}{2}$-pulse gives us an equal weighting of ground and excited states [38]. Change in qubit phase, or a rotation around the z-axis of the Bloch sphere, may be obtained by detuning the frequency of the qubit with respect to the drive field, or by a composition of rotations around the x and y axes. Equivalently, a *virtual Z-rotation* may be implemented by a rotation of the coordinate axis with respect to the sphere. Physically, this is done by adding a

phase offset to the drive field for all subsequent rotations around the x and y axes [37].

Entanglement is a key feature of quantum mechanical systems that quantum computation seeks to take advantage of. There is, therefore, a need to facilitate interaction between qubits so that they become entangled, before performing operations on them. There are many methods of coupling qubits but they all rely on introducing some interaction term to the combined Hamiltonian of the two qubits. Physically, the coupling is electromagnetic and can be broken into 3 broad categories:

- Parametric driving of a mutual coupling element [39].
- Manipulating fixed-frequency qubits with microwave radiation, for example by driving one qubit at the frequency of another [33].
- Tuning the frequencies of transmon qubits near to one another by varying the flux through their dc-SQUIDs [33].

Reading the state of a qubit also presents a challenge. A simple measurement will cause the qubit wavefunction to collapse into a particular state, and thus the loss of its quantum information. Therefore, a non-destructive measurement technique is needed. A commonly used technique is *dispersive readout*. Here, a qubit of frequency ω_q is coupled to a readout resonator of resonant frequency ω_r, which is generally achieved by placing the two adjacent to one another on chip so that their fields overlap [36]. The coupling may be described by the Jaynes-Cummings Hamiltonian given in equation 2.12:

$$H_{JC} = \hbar\omega_r(a^\dagger a + \frac{1}{2}) + \frac{1}{2}\hbar\omega_a\sigma_z + \hbar g(a^\dagger\sigma^- + a\sigma^+). \tag{2.12}$$

This is where the aforementioned connection between the fields of cavity and circuit QED manifests. In cavity QED, the Jaynes-Cummings Hamiltonian describes how an atom, modelled as a two-level system, couples to a single mode of an electromagnetic field inside an optical cavity. In this context, the first term in equation 2.12 represents the energy of the electromagnetic field, with $\hbar\omega_r$ being the energy of each photon. The second term represents the atom as a spin-1/2 system, with transition energy $\hbar\omega_a$, and the third term describes a dipole interaction where an atom can absorb $(a\sigma^+)$ and emit $(a^\dagger\sigma^-)$ a photon from and to the field at a rate g [31]. The term "Rabi frequency," used in reference to the oscillation of qubit states under driving in section 2.2.2, also derives from this treatment, as this is the frequency at which energy is exchanged between the atom and cavity. In the context of circuit QED, the first term represents the energy of the resonator, the second term represents the energy of the qubit and the third term the coupling between the two.

When the detuning $\Delta = \omega_a - \omega_r$ is much larger than the coupling rate g, the system is said to be in the dispersive regime. No direct exchange of energy between qubit and resonator takes place and the measurement is, therefore, non-destructive and equation 2.12 can be approximated

as:

$$H_{disp} = \omega_r \left(a^\dagger a + \frac{1}{2} \right) + \frac{1}{2} \left(\omega_a + \frac{g^2}{\Delta} + \frac{2g^2}{\Delta} a^\dagger a \right) \sigma_z. \tag{2.13}$$

Here, the second term in the second set of brackets represents the Lamb shift in the qubit frequency due to vacuum fluctuations in the resonator and the third term represents the ac-Stark effect-induced dispersive shift in the resonator and qubit frequencies due to the mutual interaction. The response of the resonator to a probe will vary depending on the state of the qubit, which can thus be inferred [28, 33].

Decoherence times are often used as a measure of the viability of a particular qubit, and are essentially an indication of the time before the quantum information is lost from the system. Longitudinal relaxation is the result of the qubit exchanging energy with its environment and, as the name suggests, can be thought of as the qubit state rotating around a great circle on the Bloch sphere that is in plane with the z-axis. Conversely, transverse noise, caused by shifts in the qubit's frequency, results in a phase shift in the qubit state. This corresponds to a rotation around the z-axis of the Bloch sphere. Longitudinal relaxation times are denoted T_1 and transverse relaxation times are denoted T_2.

A common method of measuring T_1 begins by applying a X_π pulse, a π-pulse around the x-axis, to the qubit in its ground state. This promotes the qubit to the $|1\rangle$ state. A time τ is then allowed to pass before measuring the qubit state. The state will then be returned as $|0\rangle$ or $|1\rangle$ state with probabilities determined by the degree to which the qubit has relaxed from the excited state. This is repeated enough times to allow an expectation value of the qubit state for the chosen τ to be determined. After many different values of τ have been tested, a characteristic T_1 time can be obtained. Figure 2.3 shows a Bloch sphere representation of the measurement sequence.

T_2 may be obtained by Ramsey interferometry. In this experiment, a $X_{\frac{\pi}{2}}$ pulse is applied to the qubit, thus preparing it in a state on the y-axis. Again, a time τ is allowed to pass and a second $X_{\frac{\pi}{2}}$ pulse is then applied. During the elapsed time, the qubit will have precessed around the z-axis by some amount, therefore the application of the $X_{\frac{\pi}{2}}$ pulse will no longer shift the qubit in plane with the z-axis, but instead some parallel plane that remains normal to the x-axis. The qubit is then measured and the resultant weighting of superposition can again be inferred from the repetition of this process many times for the chosen τ and the T_2 time can be obtained from repeating this process for multiple values of τ. An illustration of the Ramsey measurement is shown in figure 2.4.

2.3 Microwave Engineering

The transition frequencies of superconducting qubits typically lie in the GHz, or microwave, range. Therefore, the signals used to manipulate the state of qubits based on current supercon-

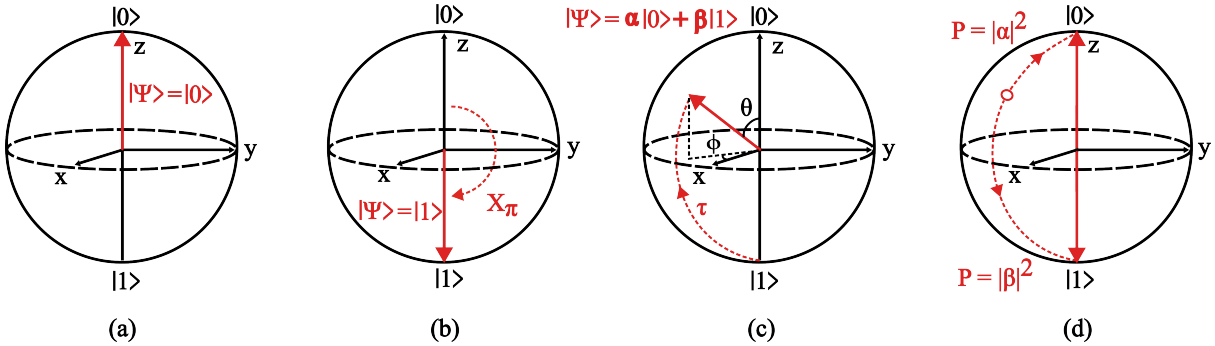


Figure 2.3: (a) Qubit is prepared in $|0\rangle$ state. (b) X_π pulse is applied to the qubit. (c) Qubit is allowed to relax for time τ. (d) Qubit is measured and collapses into either $|0\rangle$ or $|1\rangle$ state.

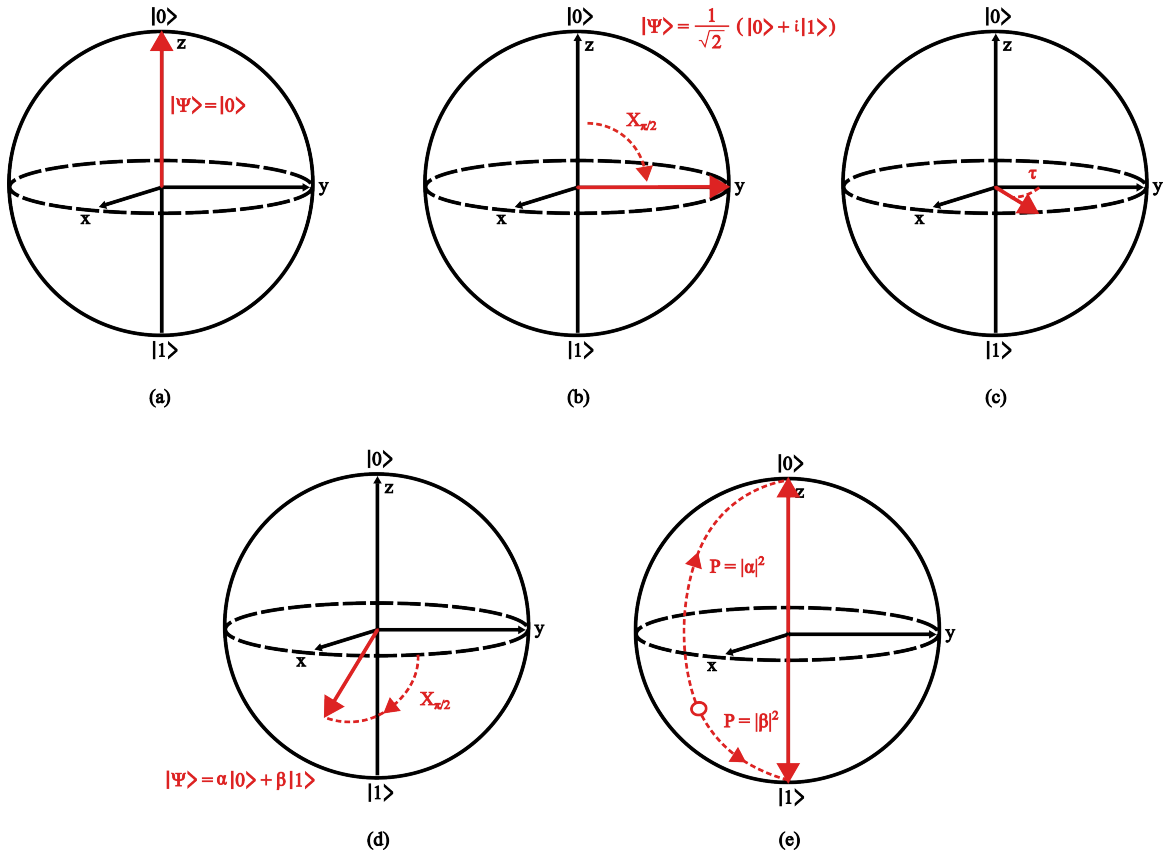


Figure 2.4: (a) Qubit is prepared in $|0\rangle$ state. (b) $X_{\frac{\pi}{2}}$ pulse is applied to the qubit. (c) Qubit is allowed to process around the z-axis. (d) A second $X_{\frac{\pi}{2}}$ pulse is applied to the qubit. (e) Qubit is measured, collapsing into either $|0\rangle$ or $|1\rangle$ state.

ducting circuit technologies must also lie in this range. This equates to wavelengths in the range 1mm - 1m, on the order of the dimensions of the circuitry itself. Interference therefore occurs on these scales and so the system becomes highly geometrically dependent [31]. The circuitry used to carry these signals to and from qubits must then be engineered for these high frequencies, as the wavelength is short enough for the voltage and current to vary over the length of the signal path [40]. This section will cover some basic concepts in microwave engineering and also introduce the topic of research: the through-silicon-via (TSV).

2.3.1 Transmission Line Theory

Coplanar Waveguides

In the case that the properties of a signal vary along its path, the carrier of the signal is referred to as a transmission line, of which there are many types. In this work, as in the majority of superconducting quantum circuits, a *coplanar waveguide* (CPW), shown in figure 2.5, is used. This consists of a central conducting strip, of width w, deposited on a dielectric substrate, with adjacent semi-infinite ground planes separated from the strip by a distance s. The waveguide supports the propagation of quasi-TEM modes, and its characteristic impedance, Z_0, is fully determined by the ratio $w : s$ and the dielectric constant of the substrate, ε_r. The commonly used standard of $Z_0 = 50\Omega$ is achievable with $w : s = 5 : 3$ and $\varepsilon_r \sim 11$, the dielectric constant of Si [26].

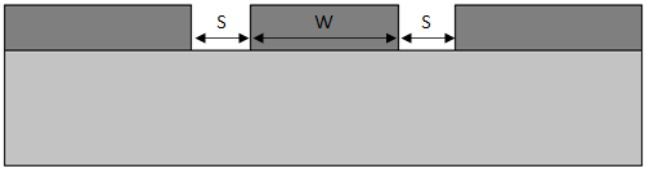


Figure 2.5: Cross-section of a coplanar waveguide, with light grey representing the Si substrate and dark grey representing the metallisation layer. w and s denote the width of the central trace and the width of the gap between the trace and the ground plane, respectively.

2.3.2 Scattering Parameters

Consider a microwave network with an arbitrary number of ports where port j is being driven with a voltage, V_j^+, and the voltage incident on all other ports is 0. Let V_i^- be the measured amplitude of the voltage wave reflected from port i. The network may be described by the *scattering matrix*, whose elements are defined [40]:

$$S_{ij} = \frac{V_i^-}{V_j^+}\Big|_{V_k^+=0\,\forall\, k\neq j}. \tag{2.14}$$

In this work, the discussion will be restricted to 2-port networks, and therefore S_{11} and S_{21} will be used as a measure of the reflection and transmission properties, respectively, of a particular line. In reciprocal networks - those containing no active devices or ferrites - the scattering matrix is symmetric [26].

2.3.3 Microwave Resonators

Resonators are ubiquitous in superconducting quantum circuits. They facilitate coupling between circuit elements and often take the form of transmission line quarter or half-wavelength resonators [41, 42]. These are strips of transmission line, open-circuited at one or both ends, respectively, of fixed length that support resonant modes whose frequency is determined by the length of the resonator, l, and the effective dielectric constant of its environment, ε_{eff}. The resonance frequency of a half-wavelength resonator is given by:

$$\frac{\omega}{2\pi} = \frac{c}{2\sqrt{\varepsilon_{eff}}l}, \tag{2.15}$$

where c is the speed of light [26].

A defining property of any resonator is its *quality factor*, or Q-factor. This can be thought of as a measure of how efficiently a resonator is able to absorb energy at a given frequency and it is defined as the frequency dependent ratio of the energy absorbed, to the power that is lost to the environment:

$$Q = \omega\frac{E_{stored}}{P_{loss}}. \tag{2.16}$$

The Q-factor of a resonator may be decomposed into components measuring the intrinsic losses of the resonator and the losses due to coupling with other circuit components: $Q_L^{-1} = Q_i^{-1} + Q_c^{-1}$. This is named the loaded Q-factor, and the components are named the internal and coupling quality factors [26].

Through-Silicon Vias

The structures mentioned so far are all patterned on the surface of a silicon substrate and are therefore restricted to two dimensions. This poses a problem for the scalability of the architecture as signal routing for control and readout circuitry becomes increasingly difficult. Moreover, the coupling of one qubit to others on the chip is, for conventional designs, restricted to nearest-neighbours [43]. A possible solution to alleviate these issues is to break the plane that the circuitry resides in and build a circuit that can route signals in three dimensions. One method of achieving this is to use through-silicon-vias (TSVs.) These consist of a conductor lined hole that is etched through the substrate, connecting circuitry on one side to the other [44]. These have been in use in the semiconductor manufacturing industry for many years, but have only recently been explored as a possible addition to superconducting quantum circuits. One reason for this is

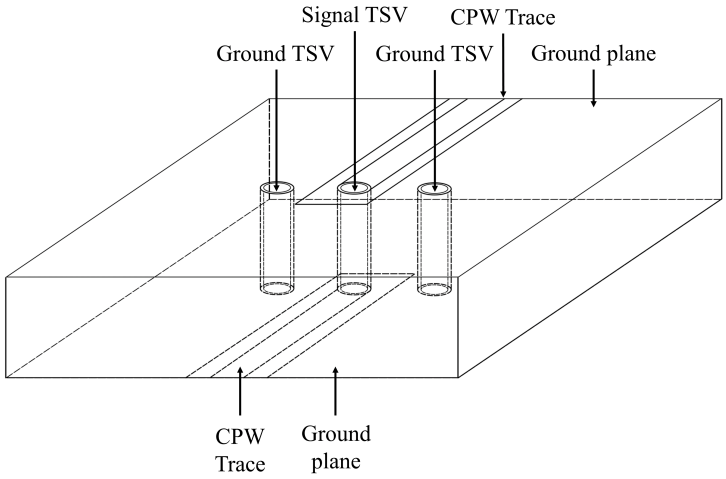


Figure 2.6: Diagram of CPWs on the top and bottom of a substrate connected by a TSV. Ground TSVs connect the parallel ground planes.

that the typical electroplating process that is used for the common Cu-lined vias is not suitable for superconducting materials [44]. Recently though, multiple techniques have been developed for superconducting TSV fabrication, increasing the viability of the component [15, 44–46]. With the objective of the introduction of TSVs being to save space on the chip, and reduce interconnect crowding, high aspect-ratio TSVs are desirable, with ratios of 10:1 being achievable.

TSVs in this case are not solitary components. In order to match the 50Ω impedance of the circuit's transmission lines, a ground-signal, or ground-signal-ground arrangement, shown in figure 2.6, is employed. The design parameters such as TSV diameter and the separation of the TSVs can be changed to tailor the capacitance (C), inductance (L), and hence impedance (Z), of the multi-TSV transition from one side of the substrate to the other according to:

$$C = \frac{\pi\varepsilon}{\operatorname{arccosh}(\frac{d}{2a})}, \tag{2.17}$$

$$L = \frac{\mu}{\pi}\operatorname{arccosh}(\frac{d}{2a}), \tag{2.18}$$

$$Z = \sqrt{\frac{L}{C}}, \tag{2.19}$$

for a ground-signal pair, where d is the distance between the centres of the TSVs, a is their radius, and ε and μ are the permittivity and permeability of the dielectric, respectively [40]. If more ground TSVs are to be added, the capacitance between the signal and ground TSVs remains approximately the same as negative charges distribute evenly between the ground TSVs. However, the inductance of the arrangement changes as there are now parallel inductance loops between each ground TSV and the signal TSV. By inserting equations 2.17 and 2.18 into 2.19, the impedance of a TSV transition of n_g ground TSVs may be expressed as a function of d and

a:

$$Z = \sqrt{\frac{\mu}{n_g \pi^2 \varepsilon} \operatorname{arccosh}^2(\frac{d}{2a})}. \tag{2.20}$$

Note that this implicitly assumes that $d \geq 2a$. A review of current superconducting TSV technologies is given in section 2.5.

Kinetic Inductance

Inductance (L) is a measure of a conductor's opposition to a change in the electrical current flowing through it. In the vast majority of discussions of inductance, it is specifically magnetic inductance (L_m) that is being referred to. This is the familiar opposition to the change in the flow of current due to the negative rate of change of the magnetic flux induced by that current flow. However, there is also another, less frequently discussed source of induction that whose origin lies in the inertial mass of the charge carriers themselves. As, for example, electrons flow through a wire, they have some kinetic energy. Therefore, if the electromotive force causing the flow were to cease, the inertia of the electrons would oppose the decrease in flow. This is called *kinetic inductance* (L_k).

To lend further support for the use of the term inductance, consider the energy associated with an electric current carried by particles of mass m, velocity v and number density n in a length of superconducting wire:

$$E = \frac{\mu}{2} \int_{\text{all space}} H^2 dV + \frac{1}{2} \int_{\text{superconductor}} nmv^2 dV, \tag{2.21}$$

where the first term accounts for the energy of the magnetic field and the second the kinetic energy of the particles. This can be rewritten:

$$E = \frac{1}{2} L_m I^2 + \frac{1}{2} \mu \lambda_L^2 \frac{l}{A} I^2, \tag{2.22}$$

using the relations $\int_{\text{all space}} H^2 dV = L_m \frac{I^2}{\mu}$ and $v = \frac{I}{enA}$, and inserting the magnetic penetration depth $\lambda_L = \frac{m}{\mu n e^2}$ [31, 40, 47]. Because both terms vary with I^2, they may both be described as inductance and the total inductance of the material is, therefore, taken as the sum of these two components:

$$L = L_m + L_k. \tag{2.23}$$

When discussing CPWs in particular, the magnetic and kinetic inductance have been shown to be:

$$L_m = \frac{\mu}{4} \frac{K(k')}{K(k)}, \tag{2.24}$$

$$L_k = \mu \frac{\lambda_L}{wt} g(s, w, t), \tag{2.25}$$

where $K(k)$ is the complete elliptic integral of the first kind with a modulus $k = \frac{w}{w+2s}$, $k' = \sqrt{1-k^2}$, t is the film thickness, w is the width of the central conductor and s is the spacing between the central conductor and the ground planes. $g(s,w,t)$ is a geometrical factor that is obtained by conformal mapping techniques and is given as [48]:

$$g(s,w,t) = \frac{1}{2k^2K(k)^2}[-\ln(\frac{t}{4w}) - \frac{w}{w+2s}\ln(\frac{t}{4(w+2s)}) + \frac{2(w+s)}{w+2s}\ln(\frac{s}{w+s})]. \tag{2.26}$$

L_k is generally much smaller in normal metals than L_m and is usually discounted. However, in superconductors it often plays a more important role. To see this, consider these expressions for resistance and kinetic reactance of a wire of length l and cross-sectional area A:

$$R = [(\frac{m}{ne^2})(\frac{l}{A})]\frac{1}{\tau}, \tag{2.27}$$

$$\omega L_k = [(\frac{m}{ne^2})(\frac{l}{A})]\omega, \tag{2.28}$$

where m, n and e are the mass, number density and charge of the charge carriers, respectively, and τ and ω are the electron collision time and signal frequency. Reactance will dominate when $\omega > \frac{1}{\tau}$. In a superconductor, $\tau \to \infty$ and therefore ωL_k may dominate R at any frequency [47]. Note that from equation 2.25, it can be observed that the kinetic inductance varies inversely with the cross-sectional area and so becomes more significant in the case of thin films.

2.4 Fabrication Techniques

One of the chief reasons that superconducting qubits are such a popular modality is that the nanofabrication techniques used to create them are well researched and developed due to their applications in the semiconductor industry [33]. An overview of the techniques used in the fabrication of the devices discussed in this work is given here.

2.4.1 Cleaning

Substrate cleaning is an imperative step in the processing of silicon wafers. Contamination on the surface of the wafer can be extremely detrimental to the results of the fabrication procedures used to create devices. These contaminants can take the form of films, discrete particles or adsorbed gases [49]. Due to the scale of the fabricated devices, even particles or residues on the order of nanometers in size may disrupt the intended pattern or function of a device. Contaminating particles may affect the device in myriad ways, but some common effects are creating electrical shorts between components that are supposed to be disconnected, unwanted chemical reactions between the contaminant and substances used during processing, provision of nucleation points for unwanted material deposition and masking during lithography, etching or depositions [50]. Contaminant films can similarly cause unwanted chemical reactions or further issues such as poor adhesion of photoresist or other deposited films.

Solvent Cleaning

The simplest way in which silicon wafers are cleaned is by by ultrasonic agitation while immersed in a series of organic solvents, often acetone, methanol and IPA, followed by a rinse with deionised water. These solvents are effective in removing organic residues from the surface of the substrate. The ultrasonic agitation helps to liberate these residues and lifts particulates from the surface of the wafer. Cleaning with multiple different solvents prevents residues from the solvent in the prior cleaning step remaining on the wafer.

Piranha Solution

Piranha solution is a mixture of sulphuric acid (H_2SO_4) and hydrogen peroxide (H_2O_2), in a 7:1 ratio in this work, and is so named for its ability to rapidly dissolve organic compounds. It can therefore be used as a potent remover of organic contaminants from Si substrates. When mixed, the reactants form Caro's acid (H_2SO_5) which is an active etchant for organics [50]. Moreover, in a secondary reaction between the two species, free oxygen radicals are produced, which dissolves carbon compounds.

Plasma Ashing

Plasma ashing is a technique that is often used to remove organic residues or photoresist from samples. In an asher, O_2 gas is excited to form atomic oxygen, which is then able to break down organic compounds. Two types of asher were used in this work: a barrel asher and a downstream asher. The difference in these tools is found in where the plasma is generated and how it reaches the sample. In a barrel asher, the chamber is cylindrical in shape. After the sample is placed inside the chamber, a plasma is formed and surrounds the sample. In a downstream asher, the plasma is formed in an area separate from the location of the sample and the atomic oxygen is carried towards the sample. This process allows charged particles contained in the plasma time to recombine and prevents them from reaching the sample surface where they may cause damage. As well as cleaning or resist stripping, plasma ashing may also be used to remove unwanted resist residue that may have been redeposited into resist trenches formed after development. This is known as descumming and helps to produce a sharper resist mask pattern. It is done at a lower plasma power, generally 100W, so as to not strip the entire resist mask.

2.4.2 Photolithography

The word *lithography*, derived from the Greek "lithos" meaning "stone" and "gráphō" meaning "to write," is a technique used for the serial production of art, writing or sheet music. It is accomplished by first drawing a design into a wax-coated limestone tablet and treating the newly exposed areas with a mixture of nitric acid and gum-arabic, turning them hydrophilic. After the removal of the wax, the tablet is coated with an oil-based ink, which is preferentially attracted to the areas not treated with the acid/gum-arabic mixture. The design can then be reproduced by pressing the tablet onto another medium, such as paper [51].

Photolithography is the modern successor to this technique and inherits its principle of successive selective exposures of a material to various treatments. A substrate, most commonly Si, is first coated with a viscous photosensitive liquid called *photoresist*. Regions of the photoresist are then selectively removed by exposure to UV light and dissolution in a developer, leaving behind areas of exposed substrate in the form of the desired pattern. These exposed areas can then be either directly etched or have material deposited into them. A diagram of this process is given in figure 2.7. This binary process of either selective addition or subtraction of material from the substrate surface may be used multiple times in succession to build up layers of circuitry [52, 53]. This technique can be incredibly effective at mass-producing extremely densely packed circuitry, with a minimum feature size on the order of tens of nanometres, depending on the variation of the technique used. For this reason, it is the most commonly used method of producing such circuits in the electronics industry today. This feature size is limited by the smallest image that may be projected onto the resist as well as the resolving capability of the resist.

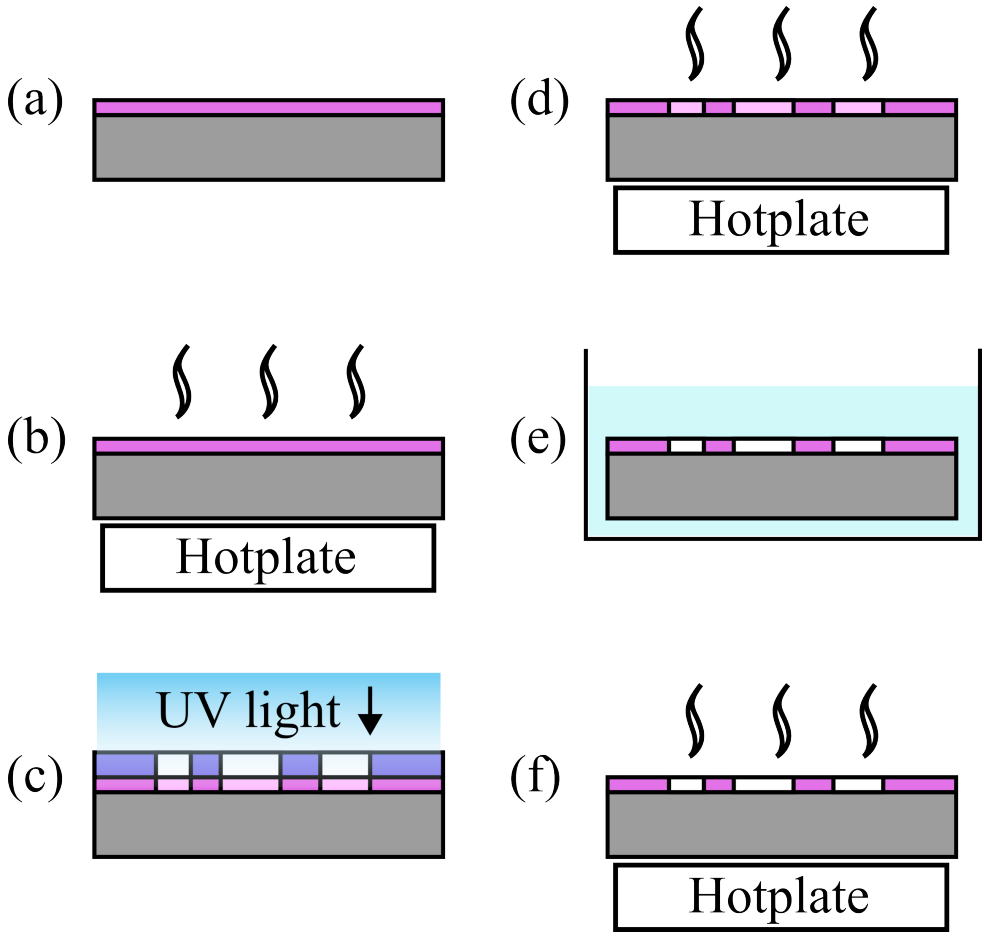


Figure 2.7: Diagram of the photolithography process. (a) Photoresist is spun onto the substrate. (b) Softbake is performed. (c) Photoresist is exposed through photomask. (d) Post-exposure bake. (e) Photoresist is developed in a beaker filled with developer. (e) Photoresist is hardbaked.

Priming

In order for photolithography to be as effective as possible, the photoresist layer must be as uniform as possible. It is therefore imperative that the substrate is free of any contamination in the form of particulates or films on its surface. Should contamination of these types be allowed to remain on the surface prior to the application of the photoresist layer, then defects in the form of "comets" or regions of poor adhesion will form in the resist, resulting in poor pattern transfer [52].

Contamination is impossible to remove entirely, but there exists a variety of techniques that can be used to improve the condition of the substrate. Particulates and organic residues are removed by the cleaning processes described in section 2.4.1. Water adsorbed onto the wafer surface is also detrimental to the adhesion of the resist to the substrate [52, 54]. A baking step in order to dehydrate the surface is often performed on the substrate immediately prior to the application of the resist. The surface may also be treated with an adhesion promoting primer after this baking step. There are a number of commercially available primers that contain

hexamethyldisilizane (HMDS) which replaces hydroxyl groups bonded to the silicon surface with a more hydrophobic functional group, thereby preventing delamination of the resist during the development step.

Spinning

There are various ways in which resist may be applied to a substrate, such as spray-coating or lamination, but a simple, yet highly effective, method of achieving a uniform film is by pouring some volume of resist onto the substrate surface and then spinning the wafer on top of a vacuum chuck to spread the applied resist over the surface [52–54]. Excess resist is flung off the sample and the solvent portion of the resist is evaporated, increasing the viscosity of the resist. As the sample is spun, centrifugal forces, proportional to the resist's mass, cause it to spread towards the sample edge. Friction between the resist and the surface opposes this and as solvent is evaporated from the resist, the resulting increase in viscosity causes an increase in friction, eventually stopping the mass flow in the resist [52, 54]. The evaporation of the solvent is crucial. Without this, the resist would tend towards being completely removed from the sample surface. However, due to the loss of solvent and the cooling effect of the evaporation, the increase in viscosity leads to the resist forming a film of a well-calibrated thickness for a given spin speed [53]. This final resist thickness is virtually independent of the spin time and the volume of resist poured onto the sample, provided there is enough to cover the surface, and varies inversely with the square root of the spin speed [54]. Photoresists generally only operate within a range of spin speeds - too low a speed creates difficulty in controlling the thickness of the resulting film and too high a speed causes turbulent airflow over the resist, limiting uniformity of the film [52, 54].

A drawback of the spinning application process is the formation of an *edge-bead* around the edge of the sample, which may also creep onto the backside of the sample. This is formed by the surface tension at the resist-air interface pointing perpendicularly downwards towards the wafer surface. Across the majority of the wafer, this causes no issue. However, at the edge of the sample, this force points towards the centre of the sample, causing resist to accumulate [52, 54]. This edge-bead can be 20-30x thicker than the rest of the resist film and should be removed for two reasons: first, after drying it may flake off and contaminate the sample, and second, it may lead to "wedge errors" during the exposure step of the photolithography [52–54].

Softbake

After the resist is applied to the substrate, there is generally still a significant volume of solvent remaining in the film. This affects the diffusion of photoactive compounds in the resist, the chemistry in the subsequent processing steps and also increases the development rate of unexposed resist. *Softbaking* the resist drives off this solvent, densifying and stabilising the resist.

This also has the effect of improving adhesion of the resist to the substrate and drying the resist, making it less prone to contamination [52–54].

Hotplates are preferred to ovens for this step as the heating is more easily controlled and generally more uniform. On a hotplate, the heat is transferred to the bottom of the resist film through the substrate, thereby driving the solvent upwards through the resist. In contrast, in an oven heat is transferred to the resist from the substrate/resist boundary and from the air/resist boundary. If too high a temperature is used, this can result in a skin forming on the outer surface of the resist, preventing solvent from evaporating from the film. Trapped vapours may then form bubbles which affect pattern transfer in subsequent processing. Conversely, if too low a temperature is used, the time needed for the bake increases considerably [52, 53]. Ideally, the cooling of the wafer should also be controlled so as to prevent uneven cooling and defects forming in the film, cracks for example [52, 54].

Exposure

To transfer a pattern to the resist, UV light is shone through a *photomask*. This is a plate made of a UV-transparent material such as quartz or soda-lime and covered, in those areas through which the lithographer does not wish light to impinge on the substrate, in an opaque material, often chromium. The materials used to construct photomasks are chosen for their degree of transparency to UV light and thermal expansion properties. Quartz, as was used for all masks in this work, has higher transparency to UV light in the region of interest and lower thermal expansion coefficient than other commonly use materials, such as soda-lime or borosilicate glass [53].

In the case of contact lithography, used in this work, the pattern on the mask itself is a 1:1 scale reproduction of the circuit design and it is placed directly in contact with the resist surface. Contact aligners are beneficial as they allow large areas to be exposed at once at a high resolution and without concern for focusing errors. They are also less sensitive to errors caused by the mask not being exactly parallel to the substrate surface, called wedge errors. As mentioned previously, however, these may still appear if the photoresist edge-bead is not removed and the mask is tilted as it makes contact with the sample. Contact lithography does necessitate the cleaning of the mask after each run to remove any photoresist that may have stuck to it during contact. In this work, this was done by gently wiping the mask face with a sponge soaked with RBS 25, a multipurpose alkaline detergent, and then rinsing with deionised water. This exposes the mask to potential damage, though this is unlikely as long as care is taken during the process.

Whether the open or covered regions on the mask form the circuitry that will be built on the substrate depends on the type of photoresist and pattern transfer process used. There are two broad categories of resist: positive and negative. In negative resists, solubility is decreased by exposure and the exposed areas, therefore, remain on the sample after it is developed. Conversely,

exposure increases solubility for positive resists and exposed areas are removed from the sample by development. The photoresists considered in this work are named S1828, manufactured by DuPont, and SPR220-7, manufactured by Rohm and Haas [55, 56]. Both of these photoresists are of the positive type. The majority of positive photoresists are based on the same chemistry, which relies on the interaction between novolak resin and diazonaphthoquinone (DNQ). This chemistry has very high contrast, which allows for vertical photoresist sidewalls and well-defined features. This, therefore, enforces a requirement for the light used in the exposure to be as uniform as possible to avoid any variation in the solubility of the exposed areas of the resist.

Post-Exposure Bake

The reflection of the exposure light from the surface of the substrate may be a source of variation in solubility throughout the photoresist film due to interference with the incident light creating standing waves and thus regions of higher or lower light intensity. This may result in roughened sidewalls of the trenches in the photoresist after development, which can be detrimental for some applications. This is called the *standing wave effect*. Anti-reflective coatings may be applied to the surface of the substrate prior to exposure to combat this, though employing a *post-exposure bake* also lessens the effect by increasing the diffusion of the soluble products of the photoreaction throughout the film [52, 53]. The standing wave effect did not have a noticeable affect on this work, perhaps because a post-exposure bake was used for all samples. It may be expected that the increased diffusion of photoreaction products throughout the film would cause a loss of pattern definition, however this effect is reduced due to the gradient in photoactive compounds being much larger in the vertical direction than it is laterally [54]. This rate of diffusion is affected by the temperature and duration of the softbake. The more solvent that remains in the film, the higher the diffusion rate. For example, after the post-exposure baking of the SPR220-7 resist, it was necessary to wait at least 45 minutes before development to allow water evaporated during the bake to be reabsorbed.

Development

Development is the step in the photolithography process in which the exposed areas are removed (for positive resists). This is often done by immersing and gently agitating the sample in a basic solution in which the products of the photoreaction are soluble. Tetramethylammonium hydroxide (TMAH) is commonly used as it does not contain any metal ions that may contaminate the sample. The development process is stopped by removing the sample from the solution and rinsing it with de-ionised water, followed by drying it with a stream of N_2 [53, 54].

Hardbake

A *hardbake* may be employed as a final step in the formation of the photoresist film. This involves baking the sample on a hotplate once more, this time at a higher temperature in order to cross-link the resin polymer in the resist and thus make it more thermally stable and vacuum resistant. Driving off excess water, solvent and other low-molecular weight materials in this step prevents them from outgassing when the etching chamber or load-lock of the etcher are pumped down. The temperature required for this bake is often too high for the photoactive compounds in the resist to withstand and it is therefore left until after development. If too high a temperature is used, some pattern degradation may occur [52, 54].

2.4.3 Etching

Dry Etching

Etching is a process in which selected regions of metals or dielectrics are removed. The ratio of the etch rates of the material to be removed and the material to remain is called selectivity:

$$\text{Etch selectivity} = \frac{\text{Etch rate of material to be removed}}{\text{Etch rate of material to remain}}. \tag{2.29}$$

High selectivity is generally desired as it decreases the likelihood of etching occurring in unwanted areas [52]. One of the most common etching methods is named *dry etching*. After a resist layer is deposited on a substrate and patterned, the substrate is placed in a vacuum chamber. From here, two broad types of reaction can occur, depending on the process: *physical sputtering*, or *chemical etching*. Physical sputtering is a process in which ions, originating from a plasma generated in the chamber, are accelerated towards the substrate and knock atoms out of the lattice after colliding with the surface. This is generally an anisotropic process due to the directionality of the ions but suffers from low selectivity and re-deposition. On the other hand, during chemical etching, reactants are pumped into the chamber and interact chemically with the substrate molecules, removing them from the crystal lattice, before they are then pumped out of the chamber. This method is often faster and more selective than physical sputtering but is isotropic and very temperature dependent. A combination of the two can also be used, where sputtering ions create reaction sites for chemical etchants by breaking reaction blocking bonds. This significantly increases the etch rate of sites that have been attacked by ions, making the process more anisotropic [57].

The Bosch Etch

Since the initial work on the development of superconducting TSVs, the use of TSVs for quantum computing applications has been explored by many groups, with as many variations in fabrication processes [15, 44, 46, 58]. However, all share the same method of etching the TSVs

into the Si substrate: the Bosch etch [59]. The Bosch etch allows one to etch high-aspect ratio, vertical structures into a substrate. This is achieved through alternating cycles of isotropic chemical etching and passivation of the etched area. First, a chemical etch is used to remove a small layer of substrate. Second, a polymer that resists the chemical etchant is deposited into the etched trench, covering the bottom and sidewalls. This passivation layer is then removed from the bottom of the etched structure by directional ion sputtering, without affecting the polymer covering the sidewalls. The bottom surface is then exposed for another round of etching and the cycle repeats [57]. An illustration of the process is shown in figure 2.8.

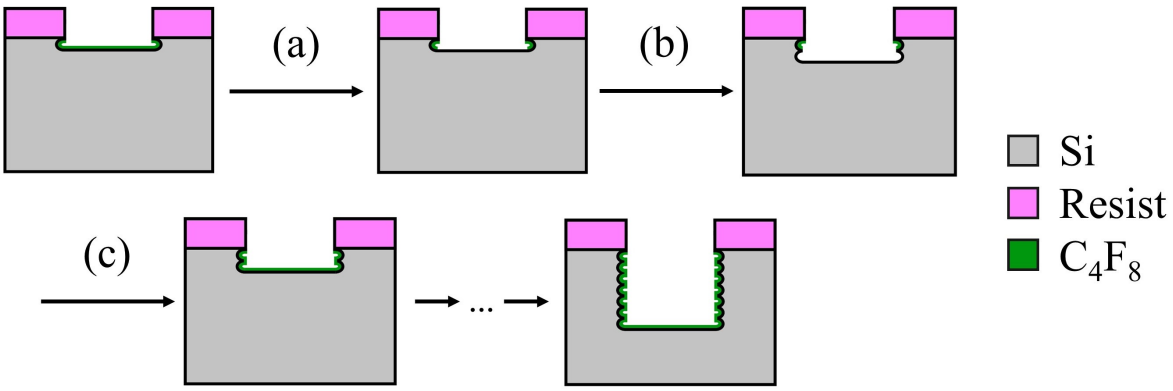


Figure 2.8: Diagram of a typical Bosch etch process showing the breakthrough (a), etch (b) and deposition (c) steps. Scallops can be seen to have formed on the TSV sidewalls in the last image.

The cyclic nature of this process creates so-called "scallops" in the sidewalls of the TSVs, which can be detrimental to film adhesion and uniformity within the TSV, particularly if the deposition method is at all anisotropic, due to the shadowing effects caused by the scallops. Furthermore, the scallop-induced surface roughness also promotes the concentration of stress and electric fields at points along the sidewall [60]. These qualities may affect the electrical properties of the device and the removal of these scallops is therefore of concern and will be discussed in section 4.1.5. Another ancilliary effect that one should be aware of when dealing with any deep Si etch is the notion of *aspect-ratio dependent etching* (ARDE). As the aspect ratio of a given structure increases, there is a reduction in the rate at which material from the bottom of the structure is removed. This is largely due to the hindrance of etchants accessing the bottom region of the structure and also the removal of volatile etch-byproducts. ARDE prevents, for example, TSVs of different diameters from achieving identical etch depths in the same number of etch cycles and they must, therefore be taken into account when calibrating a Bosch process.

Wet Etching

The other category of etching processes that is widely used in the creation of nanofabricated devices is *wet etching*. As the name suggests, this is the use of liquid phase reactants for the

removal of material from a sample. It may be used with an etching mask for the selective removal of areas of the sample or without one, for example as a method of stripping sacrificial layers or cleaning substrates. Wet etches can be much simpler to execute than dry-etch processes as they do not require the expensive and complex equipment that is often needed to control gas-phase reactions. They also offer advantages in terms of parallel processing, with many samples able to be treated simultaneously [53]. Two wet etch processes that were used in this work shall now be briefly discussed: the etching of SiO_2 with HF and the etching of Si with KOH.

HF is widely used to etch SiO_2, not least because it is the only known liquid chemical that can isotropically etch SiO_2 at a reasonable rate. It does so in the reaction: $SiO_2 + 6HF \rightarrow H_2SiF_6 + 2H_2O$. NH_4F is often mixed with the HF solution as a buffering agent in order to maintain the concentration of F ions and thus a constant etch rate. This also has the added benefit of increasing the overall etch rate by the addition of the highly reactive HF_2^- ions [61]. The reaction is terminated by the transfer of the sample to deionised water and further rinsing. Extreme caution must be exercised when undertaking processes using HF due to its high reactivity and toxicity. For the fabrication of TSVs used in this report, HF is used for two purposes: first, the removal of the sacrificial SiO_2 etch-stop, and second, the smoothing of the sidewalls of TSVs, which is discussed further in section 4.1.5.

In contrast to isotropic nature of this HF etch, the KOH etching of Si is highly anisotropic. The etch rate of KOH acting on Si is strongly dependent on the Si crystal plane that is exposed to the etchant, as well as factors such as etchant concentration and temperature [53]. The etching reaction for the [111] plane has a much higher activation energy than for the [100] and [110] planes and these planes are, therefore, selectively etched at a much higher rate than the [111] plane. A diagram of the [100], [110] and [111] planes is given in figure 2.9. The reaction may be described as: $Si + 2OH^- + 2H_2O \rightarrow Si(OH_4) + H_2 \rightarrow SiO_2(OH)_2^{2-} + 2H_2$ and, as with the HF reaction previously described, this is also used to smooth the sidewalls of TSVs and further discussion will be left to section 4.1.5 [61].

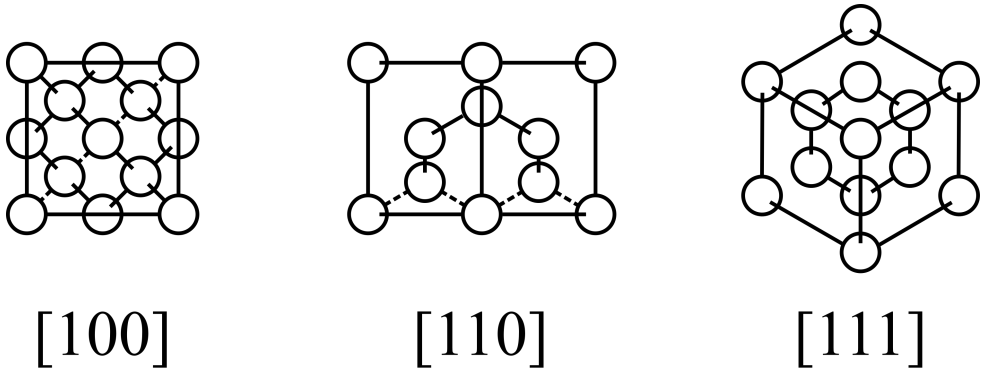


Figure 2.9: Diagram of the [100], [110] and [111] crystal planes of Si.

2.4.4 Deposition

Etching comprises the body of subtractive techniques that are used in the fabrication of nano-scale devices. On the other side of the coin is the plethora of additive techniques that are used in these processes. The deposition of material films generally proceed in two ways. They may be deposited on top of a substrate, after which they can undergo lithographic patterning followed by etching to remove unwanted regions. Alternatively, they may be deposited on top of a resist layer which is subsequently removed, leaving the deposited material remaining in the regions which were not coated by the resist layer. This process is called lift-off. A variety of deposition techniques were used in this work and the following section shall be an overview of the main concepts of each.

Sputtering

Sputtering is one of the most widely used deposition techniques in use today. It falls within the category of physical vapour deposition, which describes methods for which a vapour of the material to be deposited is formed by physical, as opposed to chemical, means before being directed towards a sample. A wide variety of insulating and conductive materials may be deposited by this method and, as such, the applications for sputtering are numerous. It may be used for the deposition of coatings that resist wear, corrosion or have certain optical or electrical properties [62]. In this work it will be used for the deposition of superconducting nitrides for the metallisation of TSVs.

To perform the deposition, a sample is loaded into a vacuum chamber such that there is a clear line of sight to a target made of high purity material attached to an electrode. The chamber is then filled with a gas, often Ar due to its inertness and high mass, which is ionised. The ions in the chamber bombard the target, causing the ejection of atoms which travel across the chamber and deposit on the sample. If the target material is conductive, then a DC source may be used to attract the ions towards the target. Conversely, if the target is insulating, then an RF source is used in order to prevent the charging of the target leading to undesired effects such as low deposition rate and arcing of the target, resulting in contamination of the deposited film or damage to the system.

In modern sputtering tools, a magnetron configuration is used such that magnets are arranged with one polarity in the centre surrounded by a ring of the opposite polarity. This causes a large increase in the probability of an ionising collision between electrons and atomic species resulting in an increased plasma density and thus ion bombardment of the target. With this in place, much higher deposition rates are possible at lower pressures and voltages, giving purer deposited films with less energy-intensive and safer systems. Reactive sputtering is also possible. This leverages the plasma in the deposition chamber by flowing a reactant gas into the chamber during the deposition which reacts with target material to form a compound film on

the sample surface. The tool used for the deposition of films in this work was a Plassys magnetron sputtering tool with both DC and RF capabilities, a load-lock to reduce contamination and pump-down times, and five material targets, each shielded to prevent their contamination while one is in use. Process-specific details will be discussed in sections 4.1.3 and 4.2.2.

Chemical Vapour Deposition

Chemical vapour deposition (CVD) is a category of processes in which a solid material film is deposited on a substrate surface by the chemical reaction of vapour phase reactants on or near the substrate surface [63]. Generally, the reaction occurs in three steps: first, the reactant gases are introduced to the chamber and are transported to the surface of the substrate; second, the film is formed by reactions on or close to the surface after the dissociation of the reactants, their adsorption to the substrate and migration to reaction sites; and third, the reaction by-products are removed from the chamber [53]. Reactions that occur on and above the substrate surface are called heterogeneous and homogeneous reactions, respectively. Homogeneous reactions are generally undesirable as the deposited material poorly adheres to the surface and may result in films of low density and uniformity that are susceptible to defects such as pinholing [53, 63]. Process parameters used in the deposition, such as gas flow, process pressure, temperature are tightly controlled so as to promote the appropriate reaction and hence film properties.

Plasma-enhanced chemical vapour deposition (PECVD) is a subset of CVD process in which a plasma is used as a source of non-thermal energy for the reaction. High-energy electrons interact with pre-cursor species and cause them to dissociate at much lower temperatures than would be required without the presence of the plasma. This may be crucial if the film is being deposited on a device with a strict thermal budget, for example to prevent excessive mechanical stress on the wafer or a large variation in thermal expansion between film and substrate [53].

The reactive nature of the CVD process distinguishes it from more physical deposition methods, such as sputtering. This presents a number of advantages, such as a greater degree of conformality in the deposited films due to the reduced directionality inherent in the deposition. Further, a huge variety of materials may be deposited by CVD - around 70% of the elements in the periodic table have been deposited in one form or another using this method. Material properties such as stoichiometry and crystal structure can be controlled and the rate of deposition may be adjusted by tailoring the deposition parameters to suit the specifications of the process. This wide variety of options leads to many application areas for the technology, such as semiconductors, MEMS, metallurgy and even exotic uses like the coating of nuclear fuel to contain fission products [63].

Atomic Layer Deposition

A particular type of CVD process which is of special interest in this work is named *Atomic layer deposition* (ALD). It takes its name from its promise of atomic monolayer control over the thickness of deposited films. This is achieved by the self-limiting nature of the reaction that takes place on the surface of the substrate in the reaction chamber. A diagram of this reaction is shown in figure 2.10. Initially, a precursor gas is pumped into the chamber which adsorbs to the substrate surface. This precursor is often, as is the case in this work, a metal-ligand complex. These molecules may bond to sites on the substrate, but do not bond to each other at a given temperature, resulting, in theory, in a monolayer of adsorbed precursor at the termination of the first step of the reaction. In practice, islands of material are generally formed as nucleation sites on the substrate are limited and it is the marker of a superior ALD process that a fully conformal film is produced. After the purging of the excess precursor gas, a reactant gas is introduced which, by a plasma-enhanced or purely thermal reaction, undergoes a substitution reaction with the ligand molecules of the adsorbed precursor, forming a continuous film. This step of the process is also self-limiting as the reacting gas may only at available sites represented by the ligand molecules. The excess gas and volatile reaction by-products are subsequently purged, after which the steps are repeated and the film is grown layer by layer [64].

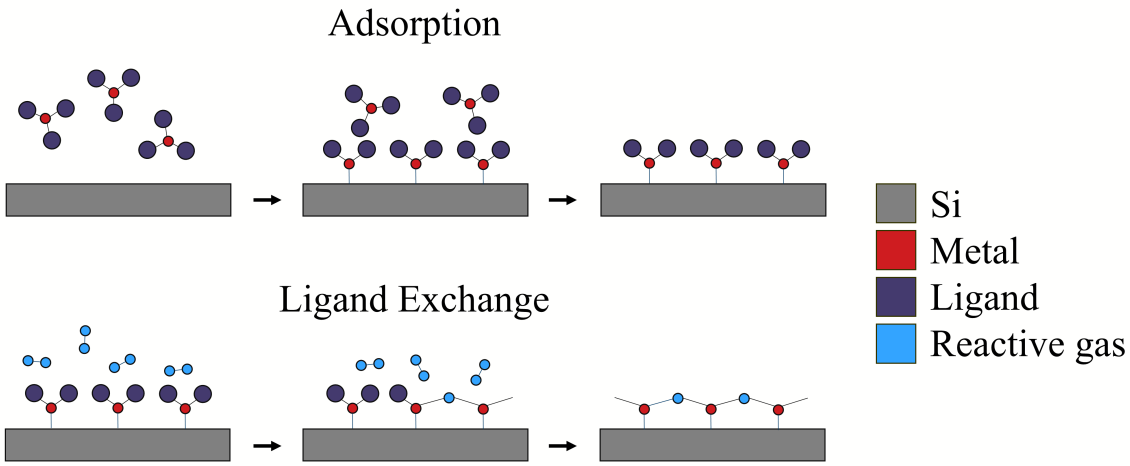


Figure 2.10: Diagram of the ALD process.

This growth pattern allows for precise control over the thickness of the deposited film. The self-limiting nature of the reaction is key to the other advantages offered by the technique. This prevents excess material from depositing in one location when compared to another and thus promotes excellent uniformity in the process. It also lends itself to greater film conformality. In the case of a more anisotropic technique like, for example, sputtering, the film will grow thicker in regions that are perpendicular to the direction of the movement of the species to be deposited. Whereas, with ALD, this is avoided and a process in which the deposition parameters have been well-tuned can result in a film that fully conforms to the topography of the substrate. As with

other PECVD processes, there is a wide parameter space that may be explored in order to vary properties of the film, such as film density, residual stress and grain size. One disadvantage of note is the propensity of ALD films to become contaminated with species that are present in their own precursor and are not removed in the purging of the chamber. This can, of course, result in a variation from targeted material parameters and is therefore undesirable. The myriad of chemical reactions that occur during any particular ALD process is difficult to control, or even to fully determine, precisely and it is therefore very challenging to mitigate this contamination [64, 65].

2.4.5 Metrology

Scanning Electron Microscopy

Scanning electron microscopy (SEM) is a technique ubiquitous in the analysis of nanofabricated samples. High resolution, ease of use and few restrictions on the nature of the sample make it an attractive method for imaging structures on the micro- or nano-scale [66]. In fact, it is an attractive group of methods, as the term scanning electron microscopy encompasses a variety of techniques such as scanning transmission electron microscopy, x-ray photoelectron spectroscopy, and the focus of this section and the most frequently used technique in this work: *secondary electron microscopy*.

In secondary electron microscopy, confusingly also abbreviated as SEM, a beam of electrons is accelerated towards the sample to be imaged inside a vacuum chamber. The electrons penetrate the sample and are scattered in a small, pear-shaped region below the surface. This scattering causes the liberation of so-called *secondary electrons* from the sample, some of which are emitted from the surface and strike the surface of a detector inside the chamber. The unique response of the sample to the electron beam due to its composition and topology allows a magnified image of the sample to be constructed [66–68]. As the depth of the electron's penetration into the sample is relatively shallow and the liberated secondary electrons have lower energy than the incident electrons, the constructed image only contains information about the surface of the imaged sample [66, 67].

Various parameters are available to the SEM operator to change on the fly to allow them to optimise the output image. The two of primary consideration are the accelerating voltage and beam current. The SEM tools used in this work (Hitachi SU8230 and SU8240) have maximum accelerating voltages of 30kV. As the operator increases this voltage, the spot size of the electron beam incident on the sample decreases, which is in general a method of increasing the resolution of the final image. However, by increasing this voltage, the interaction volume inside the sample is also increased, resulting in a loss of detail in the image [67, 68]. It may also exacerbate the charging effect in the sample or cause damage to the specimen. The probe current may also be adjusted. As this is increased, so is the signal to noise ratio of the image, which affects the smoothness or graininess of the image. As probe current increases, however, so does the

diameter of the electron beam. Higher currents are also more likely to cause damage to the sample. The operator must find the sweet-spot for both accelerating voltage and current to achieve the optimal output image [68]. This is indeed true for many other parameters under the control of the operator, such as the working distance between the sample and the electron emitter, an increase in which results in a greater depth of field but larger spot size, or the size of the aperture through which the beam passes before striking the sample, which when decreased gives higher resolution and a greater depth of field but can result in a grainy image due to the reduction in signal intensity.

As mentioned, the technique is applicable to a variety of samples. Sample size is only restricted by the size and range of movement of the sample stage and the angle by which the electron beam may be deflected by the lenses in the beam column. Thus a full 6“ Si wafer can be imaged, if desired. Insulating samples can present some difficultly during imaging. Electrons from the incident beam may build up locally in the region being scanned and cause distortion in the final image. This can be alleviated by coating the sample in a thin layer of conductive material, typically Pt or Au, such that the topology of the sample is preserved. Grounding the sample well to prevent the build up of charge is also an important way of reducing image artifacts [68]. An ideal SEM image is obtained by taking all of these factors, and more besides, into consideration and finding their optimal configuration.

Ellipsometry

The change in polarisation of a beam of light reflected from a thin film may be used to determine the thickness and optical constants of that material. This technique, known as *ellipsometry*, dates back to the 19$^{\text{th}}$ century, when it was used by Paul Drude, and it is still widely used today. It is both non-destructive and can be carried out on the fly during the fabrication process [69, 70]. The resulting information can be used to infer the composition or structure of a material [69].

To perform the measurement, light is emitted from a source held at an angle above the sample surface and penetrates the film. It is then reflected by the film/substrate interface and subsequently interferes with the light reflected by the top surface of the film and the resultant beam is is detected and analysed. The ratio of the amplitude of the linear polarisation components of the light is measured, as is their difference in phase [69]. As there are 2 measured quantities and 3 unknown quantities, (the thickness of the film and the real and imaginary parts of the complex coefficient of refraction, $\tilde{N} = n - ik$) the data must be fit to a model of the material known prior to the measurement [69, 70]. Multiple measurements are also often performed, with each one being taken with the emitter and detector held at various angles to the sample surface or at different wavelengths, in order to provide more data for the fitting.

Ellipsometry offers excellent sensitivity when measuring films and can be used on films from tens of micrometers thick to monolayers of material [71]. It does, however, have limita-

tions. Most obviously, only films that are both sufficiently thin and have a sufficiently low extinction coefficient for the incident light to penetrate and escape the material may be measured. For very thin and absorbing films, there is also a strong correlation between film's thickness and its optical constants, which may prevent unique solutions [69, 70]. In practice, though, this still leaves a large variety of samples to be analysed using the technique. The ellipsometer used for the measurement of film thicknesses in this work was the M-2000, manufactured by J. A. Woollam Co.

Profilometry

Surface topology is often of critical concern in the performance of nanofabricated devices. Whether measuring the roughness of a surface or the profile of an etched or deposited layer, precise and accurate techniques are extremely valuable in assessing the viability of the sample and the process used to make it. These types of measurements are named *profilometry*.

There are two categories of profilometric techniques: contact and non-contact, both of which were used in this work. By far the most common method of profilometry is a contact method named stylus profilometry, which as the name suggests, involves dragging a diamond-tipped stylus mounted on a cantilever across the surface of the sample [72]. The vertical displacement of this stylus is measured as it passes over features on the sample and a two dimensional cross-section of the surface is created [73]. There is a suite of non-contact profilometric methods available to the metrologist, for example atomic force microscopy and scanning tunnelling microscopy. The technique opted for in this work was optical profilometry. This utilises an interferometric apparatus and a digital camera sensor to map an area of interest on the sample as opposed to a single cross-section [74].

There are advantages to both techniques and cases where one may be more suitable than the other. Contact profilometers are often less expensive than their optical counterparts and the scans are generally faster to carry out and simpler to set up. However, the tip does have the potential to damage the surface of the sample to be measured. They also suffer from the fact that their resolution is limited by the diameter of the stylus tip and that the profile generated by the system is a convolution of the surface topology and the shape of the tip [72, 73, 75]. This was relevant in this work as it was impossible to measure the true depth of TSVs using the contact method because the stylus diameter was larger than that of the TSV and it, therefore, could not touch the bottom of the structure. Here, the optical method was much more effective. Aberrations in the surface map can occur due to beam shape, performance of the camera and surfaces that are at steep angles to the beam, though as a method of determining the depth of the TSVs, it was more than adequate [72, 74]. The contact and optical profilometers used in this work were the DektakXT and ContourGT-X, respectively, which were both manufactured by Bruker.

2.5 3D Integration Technologies for Quantum Computing

3D integration has long been used in the semiconductor industry as a way to provide scalable, small form-factor architectures and a broader design space. A large amount of research has, in the past decade, been focused on transferring these techniques to quantum devices to enhance their potential for scalability. A brief review of the various directions this research has explored will now be presented. They have been grouped into four categories, namely: through-substrate via, flip-chip architectures, airbridges and, multilayer and 3D wiring. This review will focus on the technologies applicable to superconducting quantum circuits.

2.5.1 Through-Substrate Vias

Through-substrate vias have been used in semiconductor electronics to provide high quality interconnects and isolation between circuit components. This nomenclature describes any hole through a given substrate, whether it be made of a polymer as in printed circuit board (PCB) manufacturing, Si, as in integrated circuits, or another material, that is lined with a conductor to facilitate signal routing between circuit layers. The vast majority of the research done with superconducting circuit applications in mind is based on through-silicon vias, as this is the most common substrate onto which these circuits are patterned, but as will be seen later, other materials have also begun to be explored.

To the author's knowledge, the first superconducting TSVs were developed in 2017 by Rigetti Computing [44]. These utilised sputtering as a method of metallisation and, to facilitate this, they were of a conical design, shown in figure 2.11 (a), which allowed the directional deposition to succeed. They followed a fabrication process similar to those used in the semiconductor industry, involving the etch of the TSV, followed by the deposition of the metal layer and then the removal of a layer of Si remaining on the backside of the wafer to expose the metal deposited into the bottom of the TSV trench. These devices demonstrated the feasibility of the superconducting TSV, with a measured T_c of 1.2K - that of the Al they were metallised with - and were an important first step for the technology.

This was quickly followed by work from MIT's Lincoln Lab which sought to integrate TSVs with quantum components [15,76]. Here, the TSVs were fabricated as vertical, high-aspect ratio structures, shown in figure 2.11 (c) with dimensions of 10x20x200μm and vertical sidewalls. This was enabled by the use of a conformal PECVD metallisation method. In these works, the use of TSVs for control and readout of superconducting qubits and the fabrication of qubits on the surface of a chip containing TSVs was demonstrated, proving that the two technologies are indeed compatible. A diagram of this device adapted from the work is shown in figure 2.11 (b). Critical currents large enough to support flux-biasing of qubits were shown and the high-aspect ratio of the TSVs leant into the theme of scalability by minimising the on-chip footprint

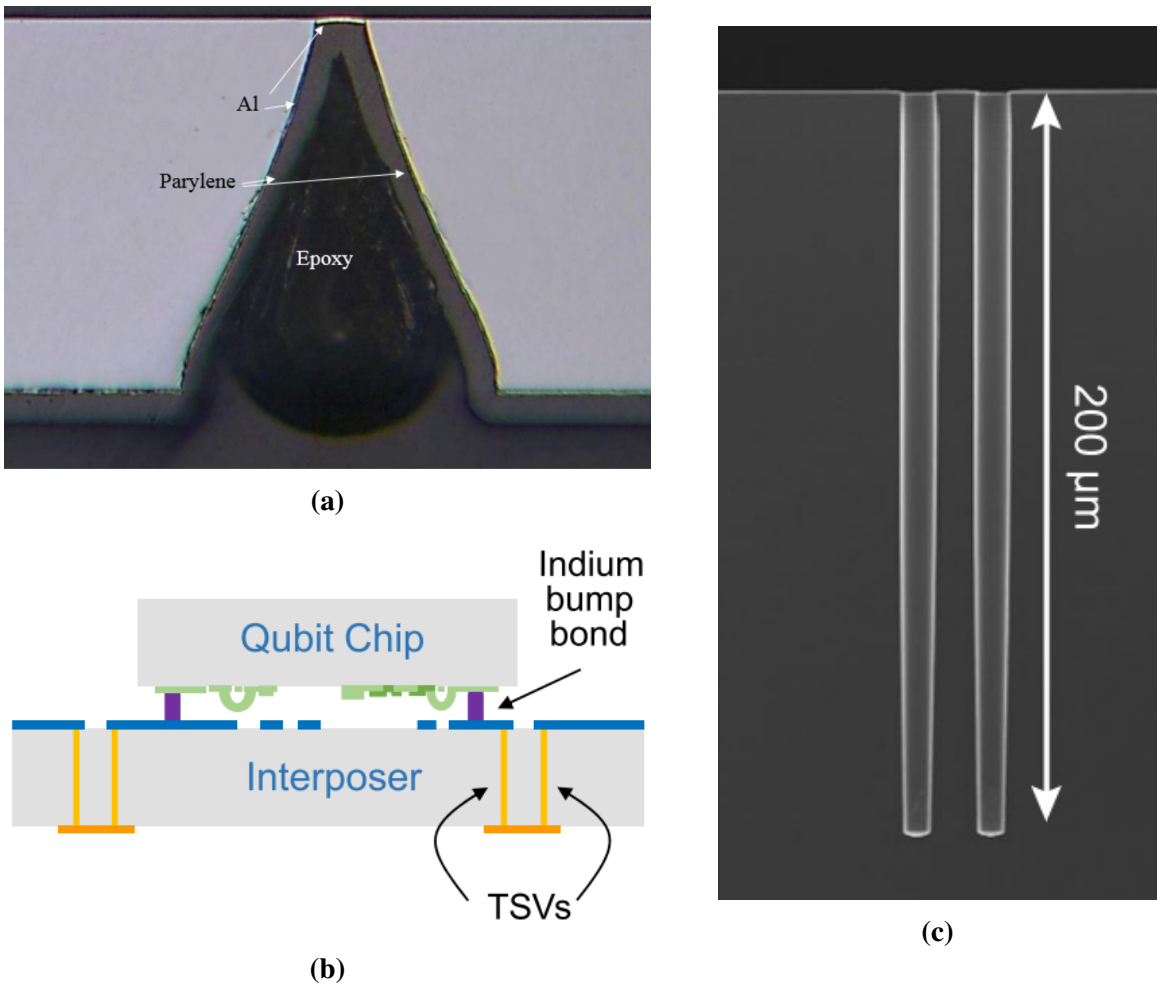


Figure 2.11: (a) Cross-sectional SEM image of a conical superconducting TSV (adapted from [44]). (b) Diagram of TSVs integrated with a qubit chip (adapted from [15]). (c) Cross-sectional SEM image of high aspect-ratio TSVs (adapted from [15]).

of the interconnects. High uniformity across the wafer on which the TSVs were fabricated was shown and resonators with TSVs embedded at various points were fabricated and measured, demonstrating the suitability of the concept to large scale fabrication and its versatility [77].

Alternative profiles of TSVs have been explored to further highlight the variety of fabrication process that are available for TSVs. One of these is the hour-glass shaped TSV (figure 2.12) which, like the conical TSV, allows for better TSV metallisation when using sputtering as a deposition technique [46]. Low single-TSV resistivity and a T_c of 1.27K confirmed the suitability of this type of TSV as interconnects [78].

ALD has emerged as a popular method of metallisation, owing to its conformal nature and precise thickness control [45, 58]. This coincided with the demonstration of TiN and others as materials of consideration for TSV fabrication. The concept of using TSVs as a method of stitching ground planes on opposite sides of the substrate has also been shown and resonator quality factors of 10^6 were measured on chips fabricated in this way [58]. This application

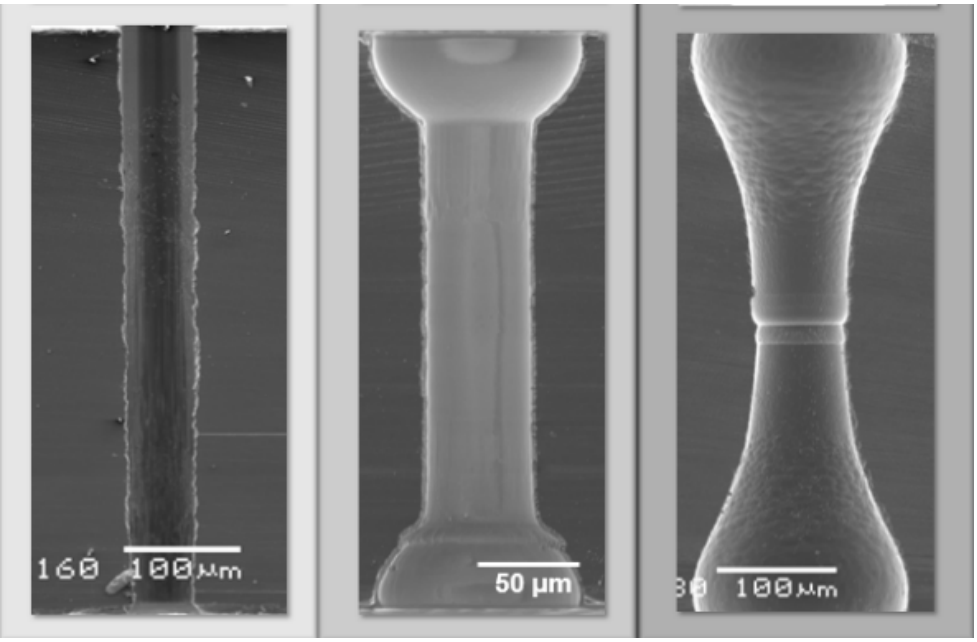


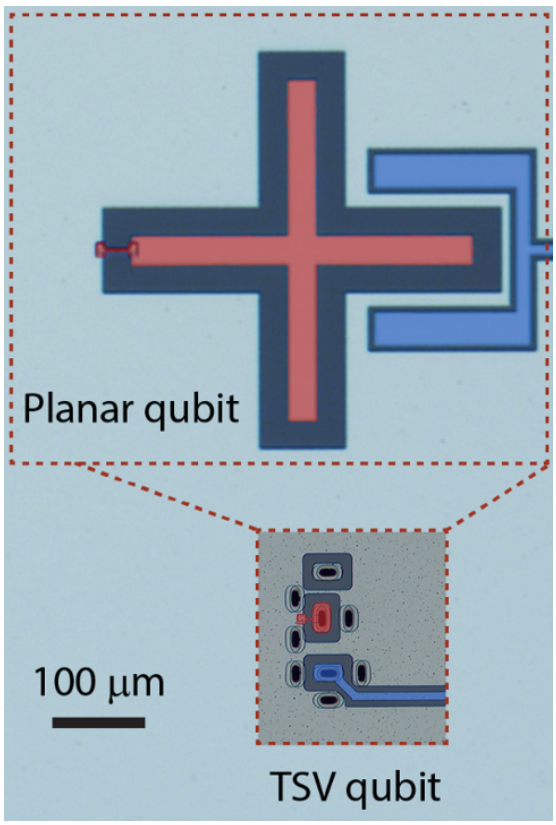
Figure 2.12: Cross-sectional SEM images of TSVs of vertical and hour-glass profiles (adapted from [78]).

of TSVs, which pushes the frequencies of substrate modes outwith the region of interest for quantum devices, is crucial for moving to larger devices.

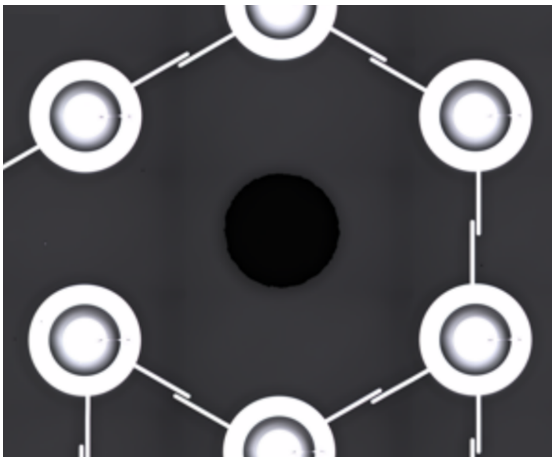
Methods of the control of the sidewall roughness of TSVs have also been a topic of research. Two key techniques, which will be explored in section 4.1.5, are the wet etching of the TSV sidewall with KOH and the use of cycles of oxidation and removal of the oxidised layer [60, 79]. These were promising steps towards the tighter control and reproducibility of fabricated TSVs, allowing for better adhesion of metallisation layers. In particular, the KOH etch method promises atomic level smoothness at the minor costs of using substrates of particular crystal orientation and requiring the TSVs to be of rhomboidal cross-section, due to the technique relying on the selective etching of the $\left[100\right]$ and $\left[110\right]$ planes over the $\left[111\right]$ plane. Record aspect ratios of 28:1 were demonstrated using this technique, further reducing the footprint of the TSVs.

Outgrowing their image as purely an interconnect, the incorporation of TSVs as capacitive elements in qubits and resonators was demonstrated in 2023 [80]. The large capacitance of the TSVs allowed for a 15x smaller footprint than a conventional transmon, as shown in figure 2.13 (a) which generally utilises large capacitive paddles on the surface of the substrate. This could allow for denser tiling of qubits on chip and thus increasing the computing power per area - a fundamental goal of scalability. It also opens the door on a suite of other potential applications for TSVs and enables, for example, the consideration of new error correction codes for use in quantum circuits.

All of the work mentioned so far has been on through-silicon vias. However, as the currently



(a)



(b)

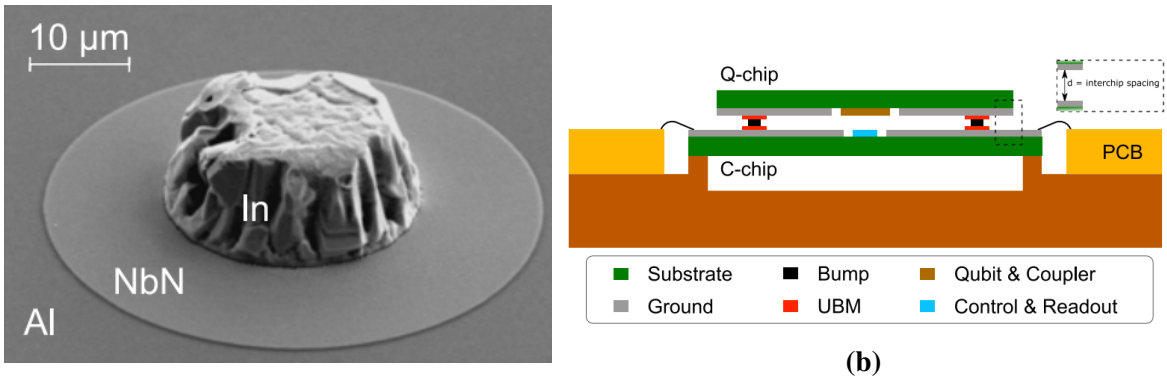
Figure 2.13: (a) False-coloured SEM image of TSV qubit in comparison with conventional transmon. Capacitive element is highlighted in red and the control line is highlighted in blue (adapted from [80]). (b) SEM image of micromachined through-sapphire via surrounded by concentric transmon qubits (adapted from [81]).

held record for superconducting transmon coherence time was achieved on samples fabricated on sapphire substrates, there has also been interest in whether the technology could be extended to this material. In 2024, this question was answered by researchers from Oxford Quantum Circuits, who presented a through-sapphire via fabrication process [81]. As sapphire is notoriously difficult to etch using deep reactive ion etch techniques, these researchers forwent this and instead utilised a CNC micromachining process to drill holes into the sapphire substrate. These through-sapphire vias were not used as interconnects, but instead as inductive shunts for the suppression of substrate modes. However, this research did demonstrate that this technique was compatible with qubit operation, with the sapphire chip integrated with a 32-qubit QPU. An example from the work is given in figure 2.13 (b). This shows that TSVs are not restricted to one substrate type and are therefore not limited to Si, which, while still the most popular substrate due to the vast knowledge base from semiconductor fabrication that can be exploited, may not be the most suitable for superconducting qubits in the long term. It is also worth noting that the CNC micromachining process used here may also be applied to Si substrates, as demonstrated by work from the universities of Oxford and Southampton [82]. The drawback to using this

technique for TSVs, however, is the large TSV diameters relative to those achievable by deep Si etching.

2.5.2 Flip-Chip Architectures

Similarly to TSVs, flip-chip architectures are a common 3D-integration technique in semiconductor manufacturing. Two chips with circuitry fabricated on their surfaces are bonded so that the circuit layers are facing each other. This allows a modular approach in the fabrication of integrated circuits and, with each chip being fabricated separately, the fabrication restrictions of one, for example thermal budgets, do not restrict the fabrication processes used for the other. It also allows greater yield in the final device as only components that meet requirements are kept and used in bonding. Along with the advantages that are common to all 3D integration techniques, such as an expansion of architectures available to circuit designers, which are directly transferable to quantum circuits, flip-chipping allows the separation of wiring layers, that may contain lossy dielectrics, from the loss-sensitive quantum components.



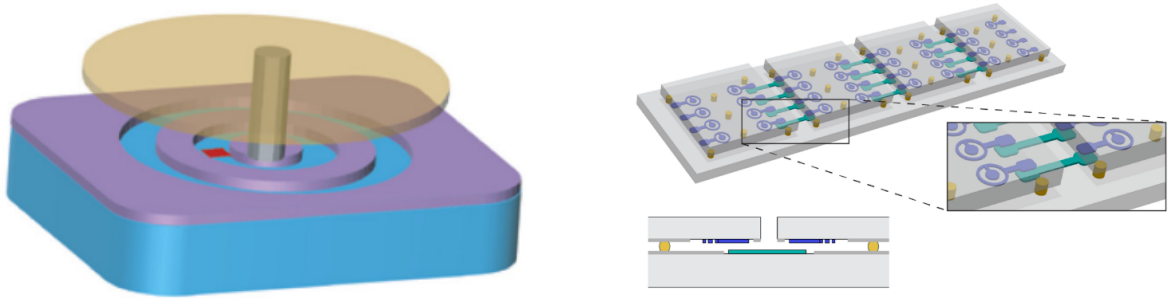
(a) **(b)**

Figure 2.14: (a) SEM image of an In bump-bond with a NbN under-bump metallisation layer (adapted from [83]). (b) Diagram of bump-bonded qubit device and packaging (adapted from [83]).

The first demonstration of flip-chip technology with superconducting quantum circuits in mind was in 2018, where an In bump-bonding process was demonstrated to be compatible with these circuits [20]. The fabrication process involved the deposition of small In bumps, an SEM image of which is shown in figure 2.14 (a), which are used to bond the top and bottom chips together via compression bonding. Between the Al and In layers, a NbN barrier layer was deposited to prevent the diffusion of the In into the Al. Chains of In bump bonds and Al CPWs were fabricated and measured. This showed the bump bonds to be high-yield and fully superconducting, with the T_c of the structure being limited by the Al. The I_c supported by the bump bonds was an order of magnitude higher than currents typically used for the flux biasing of qubits, demonstrating their use as a method of plane-breaking wiring.

The development of In bump-bonding continued, with many studies demonstrating their applicability to qubit control [76, 83–86]. Both transmon and fluxonium type qubits have been measured on flip-chip devices. Coherence times of >90μs and single qubit gate fidelities >99% have been achieved and qubit performance has been shown to not degrade as a result of their 3D integration [83, 86]. A diagram of the package used in [83] is given in figure 2.14 (b). Qubits have also been distributed across both the top and bottom chips, a so-called "flipmon," with studies demonstrating the feasibility of the device. Here, each capacitor pad is fabricated on opposing chips. The architecture seeks to take advantage of the large electric field participation ratio for the vacuum gap between the pads resulting in less dielectric loss in the device, with coherence times of up to 60μs being demonstrated. This is an indication of the versatility of the technology and asks what other architectures and applications may be possible. A diagram of the flipmon is shown in figure 2.15 (a) alongside a diagram demonstrating how multiple qubit chips may be bonded to one carrier substrate in figure 2.15 (b).

In is not the only material that has been explored for this application. Using photoresist as an adhesive to bond the two chips has also been demonstrated, in an effort to circumvent the expensive fabrication tools required for In bonding [87]. Coupling between superconducting circuits and qubits on separate dies has been shown using this method, as has full vector control of those qubits. The low bonding force needed for this technique may also be advantageous for delicate samples. In 2024, another novel material was investigated as a bonding material: Ga alloy [21]. Resonators on chips connected by this liquid metal achieved quality factors of over 10^6 and the Ga presents the advantage of being able to separate the two chips without destroying either of them - a potentially useful quality for the testing of devices.



(a) **(b)**

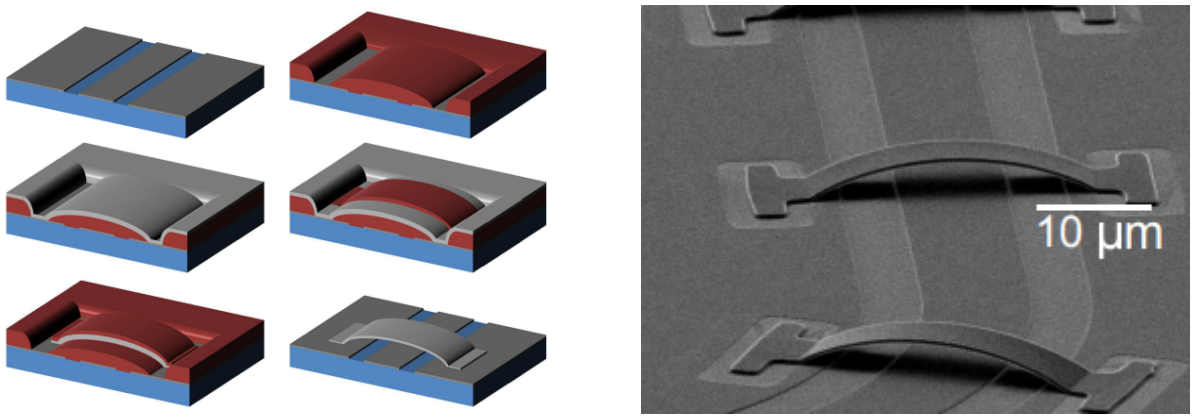
Figure 2.15: (a) Diagram of a flipmon, with the Josephson junction coloured red and the yellow capacitive pad being attached to the top chip (adapted from [85]). (b) Diagram of bump-bonds (yellow) integrated with a qubit chip. Qubits and couplers are coloured in blue and teal, respectively (adapted from [84]).

The tilt between the two chips in this type architecture must be minimised in order to prevent the capacitance between components across the chips varying from the designed value. This

prevents variation in parameters such as resonance frequency or coupling rate across the device. To this end, strategies such as the use of spacers, made of In, photoresist, or other materials, have been explored [88]. Tilt deviations of below 80μrad have been demonstrated, leading to resonance frequency variation of less than 50MHz across the chip.

2.5.3 Airbridges

Another form of plane-breaking interconnect that has received increased attention over the last decade is airbridges. As the name suggests, these are metal structures that are attached to the surface of the chip at either end, forming a bridge over a region of wiring. They have two primary functions: as interconnects that jump over circuitry to provide alternative signal routes, or to connect ground planes at either side of a CPW in order to effectively equalise the potential on either side, preventing the propagation of spurious parasitic modes. Wirebonds have often be used for this second function; however, it has been shown that, due to their small cross-section, they possess an inductance too high to provide an effective current path for this purpose [89,90]. Furthermore, as quantum components increase in scale, the addition of wirebonds becomes an unreliable process that takes a large amount of time to carry out. Whereas, because the airbridges are fabricated alongside the rest of the device, the number of airbridges can easily be scaled with the size of the device [90]. An example of an airbridge fabrication process is shown in figure 2.16 (a) alongside an SEM image of an airbridge produced by such a process.



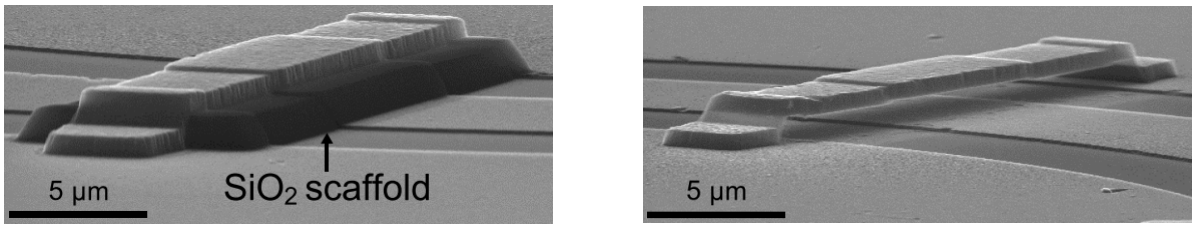
(a) **(b)**

Figure 2.16: (a) Diagram of the airbridge fabrication process using photoresist as a scaffold. Blue: Si substrate, red: photoresist, grey:Al (adapted from [90]). (b) SEM image of an Al airbridge connecting the ground planes of a CPW transmission line (adapted from [90]).

In the first study done on airbridges with a view to incorporating them into quantum devices, they were fabricated by forming a photoresist scaffold, onto which an Al layer was deposited. A second photoresist layer was deposited on top of this and patterned such that the airbridges could

be etched out of the Al layer, after which both the scaffold and mask layers were removed, leaving the free-standing airbridges [90]. This first study succeeded in reliably fabricating airbridges with a span of up to 50μm and showed an increase in loss of 1.2×10^{-8} per airbridge exhibited by resonators over which the airbridges were erected, which was attributed to TLS induced loss caused by the remnants of the photoresist scaffolding layer [90]. As research has progressed on this technology, the increase in loss on measured test resonators has remained, though it has been reduced. This small increase in loss is viewed as a worthwhile trade-off for the mitigation of spurious modes in the circuitry and the increased design flexibility that airbridges bring.

Further work sought to find alternative fabrication procedures that may be viable. One such was the use of a sacrificial scaffold made not of photoresist, but of SiO_2. This SiO_2 layer was removed after the airbridges were defined by an HF, N_2 and ethanol vapour, which did not attack the other materials in the devices. This brought the advantage of allowing the airbridges to better withstand the aggressive ultrasonic cleaning techniques that are used on devices of this type that often causes airbridges released from photoresist scaffolding to collapse. It also allowed airbridges manufactured with this technique to span larger distances, with spans of up to 70μm reported [91]. While the loss introduced per airbridge was slightly larger in this study, at 3.8×10^{-8}, they were shown to be fully compatible with Josephson junction-based qubits, with airbridges being incorporated into the design of one qubit, which coupled to another by jumping over the second qubit. There was no observable difference in the coherence times of the qubits that were coupled with and without airbridges - an important demonstration of the applicability of this technology to quantum circuit design [91]. Images of the airbridges before and after removal of the SiO_2 scaffold are shown in figures 2.17 (a) and (b), respectively.



(a) **(b)**

Figure 2.17: (a) SEM image of an airbridge prior to the removal of the SiO_2 scaffold (adapted from [91]). (b) SEM image of an airbridge after the SiO_2 scaffold has been removed (adapted from [91]).

Improvements to the loss per airbridge for structures fabricated using photoresist scaffolding have been shown since the earliest work on the topic. Utilising a greyscale electron-beam lithography technique to define the resist scaffolding, airbridges with a span of up to 100μm and a loss per bridge of 10^{-8} were fabricated by Janzen *et al.* in 2022 [92]. These were also integrated with Josephson junction-based circuits and while the resistance of the junctions did

increase as a result of the bake used for the resist, it did so in a predictable way and so could, in theory, be accounted for in future fabrication runs [92]. Further adjustments to the fabrication process have also been proposed, with Nb airbridges being fabricated on top of Al scaffolding which may subsequently be removed by selective wet etching [93]. This produced record-low loss of 5×10^{-9} due to the absence of lossy dielectrics and the more complete removal of the photoresist layer that was used to support the Al scaffold. The decrease in loss per airbridge was also a consequence of the Nb used to construct the airbridges, which brought with it an increase in T_c and superconducting gap relative to Al airbridges and thus a reduction in quasi-particle induced loss. This rapid progress in airbridge fabrication is a promising avenue to the 3D integration of quantum devices and one that has already demonstrated clear advantages.

2.5.4 Multilayer and 3D Wiring

The last category of 3D integration techniques can loosely be grouped into multilayer and 3D wiring. Multilayer wiring is achieved by embedding multiple layers of wiring into a substrate, often with the inclusion of other 3D structures such as resonant microwave cavities. This is considered as a flexible way to break the wiring plane and increase the density of wiring and the variety of circuit architectures. As these multilayer devices are often fabricated with layers of lossy dielectrics, quantum components susceptible to this loss are generally fabricated separately and integrated with these dense wiring layers by, for example, bump-bonds. As the scale, and hence complexity, of quantum devices increases, these types of solutions are of great importance to simultaneously maintain the high quality factors of resonators and coherence times of qubits while also allowing for the incorporation of complex signal routing structures to a device.

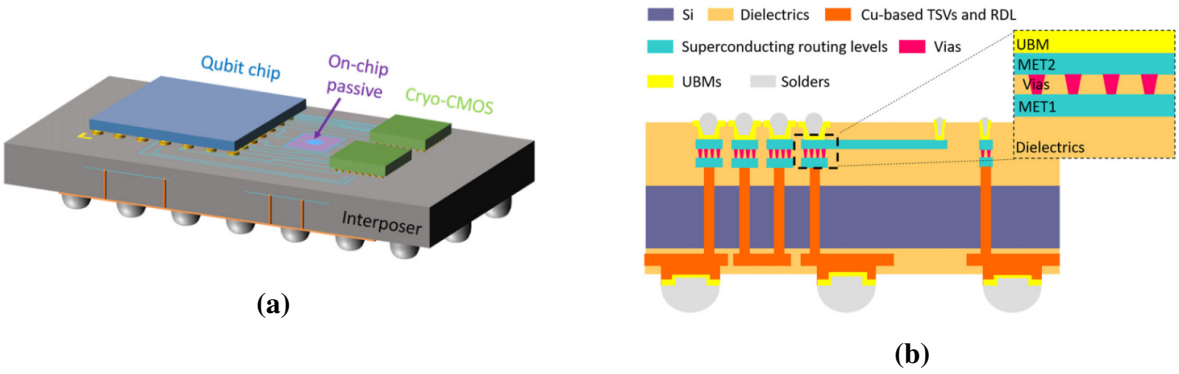


Figure 2.18: (a) Diagram of multilayer wiring platform with integrated TSVs and bump-bonded qubit and cryo-CMOS chips (adapted from [94]). (b) Cross-sectional diagram of the same device (adapted from [94]).

This approach was proposed by Brecht et al. in 2016 in a work in which they described the advantages of dividing the device into sub-systems, namely that crosstalk between components

could be minimised and that circuit elements could be engineered and fabricated separately. They also fabricated a proof of concept 3D micromachined resonator with planar multilayer coupling [95]. This concept was further developed in 2022, when a multi-layer routing platform was fabricated and integrated with a spin qubit device. It consisted of the base interposer chip, into which the wiring layers were embedded alongside TSVs to provide connection between them, two cryo-CMOS chips and one spin qubit chip that were bump-bonded to the interposer. Measurements confirmed the suitability of the circuitry to maintain signals in the GHz range and the device showed compatibility with the incorporated spin qubits [94]. A diagram of this system is shown in figure 2.18. This work is a demonstration of the combination of multiple 3D integration techniques and offers a view to the devices which will become the standard for future quantum processors.

The category of 3D wiring offers novel approaches to the packaging of quantum devices. Here, this term is used to refer to off-chip wiring that makes contact with the surface of the device by extending downwards towards it. This allows, for example, devices to be swapped to and from the packaging for rapid testing, or the use of modular, tileable architectures [14,17,96]. An example of this is shown in figure 2.19. These technologies have been demonstrated with spring-loaded pogo pins and have shown compatibility with qubits, with coherence times of 149μs and >99% gate fidelity achieved using this type of wiring [17]. This concept is extensible to large numbers of qubits and highlights the important role packaging plays in the development of quantum computing technologies.

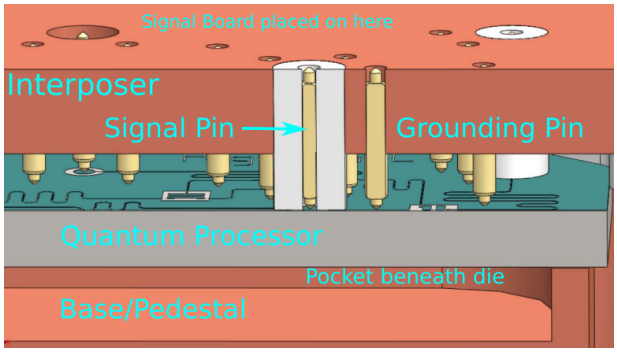


Figure 2.19: Example of 3D wiring used as part of the packaging for a quantum processor (adapted from [14]).

Chapter 3

Simulation of TSV Structures and Devices

3.1 Design of TSV Structures

Prior to the fabrication and measurement of TSVs, it is necessary to first understand the behaviour of these structures at the microwave frequencies used in the control of superconducting qubits. High-frequency simulation software is an invaluable tool in this regard as it allows one to test how varying the geometric parameters of a TSV affects these microwave properties. With this aim in mind, a series of TSV-integrated CPW structures were designed and simulated using ANSYS HFSS 3D electromagnetic simulation software to determine circuit geometries that provide the required impedance, and transmission and reflection profiles [97]. Half-wavelength resonators, both planar and 3D variants that incorporate TSVs into their length, were also simulated. These 3D resonators were included to test their viability as both a space-saving method and a possible way of transferring resonant signals from one side of the substrate to the other [77, 80].

The first of the designs to be simulated was a CPW that was interrupted by two TSV transitions, each made up of a single central signal TSV and two adjacent ground TSVs, diagrams of which are shown in figures 3.1 and 3.2. The contact pads included at both ends of the CPW were of a design that preserves the 50Ω impedance of the CPW. Ground planes were added to the top and bottom of the 5x5mm, 250μm thick intrinsic Si substrate. All metallic structures were modelled as infinitely thin perfect conductors. Wave ports were placed in contact with the side of the substrate and the edges of the contact pads and both ground planes. The structure was simulated between 2-10GHz at intervals of 20MHz, a frequency range commonly used in the measurement of quantum integrated devices. A broadband meshing technique was employed over the simulated frequency range, which allows HFSS to determine the appropriate frequencies at which to adapt the mesh. The iterative solve was carried out until there was a 2% variation in the solution between passes.

The aim of the analysis is to find a set of geometric parameters that give the highest signal

transmission and lowest reflection. There are, of course, an infinite number of combinations of geometric parameters that could be simulated and so a choice must be made as to the range of parameters that the analysis should be limited to. The TSV radius (R_v) was fixed at 20μm. This choice of radius was made at the outset with a view to the eventual fabrication of the TSVs. As they would be etched through the total thickness of the substrate, TSVs of $R_v = 20\mu$m were chosen to limit the effect of aspect-ratio dependent etching (ADRE) during device fabrication. The other parameters to be considered were the centre to centre separation distance between the signal TSV and the ground TSVs (S), the TSV pad radius (R_p) and the TSV anti-pad radius (R_a). 27 total parameter combinations were trialed, with $S \in \{0.090\text{mm}, 0.094\text{mm}, 0.098\text{mm}\}$, $R_p \in \{0.028\text{mm}, 0.030\text{mm}, 0.032\text{mm}\}$ and $R_a \in \{0.040\text{mm}, 0.042\text{mm}, 0.044\text{mm}\}$. These were to conform to three design specifications: that the anti-pad radius is larger than the pad radius ($R_a > R_p$), so as to not short the pad to ground; that the ground TSV did not make contact with the pad ($S > R_v + R_p$); and that the ground TSV was in contact with the ground planes ($S + R_v > R_a$).

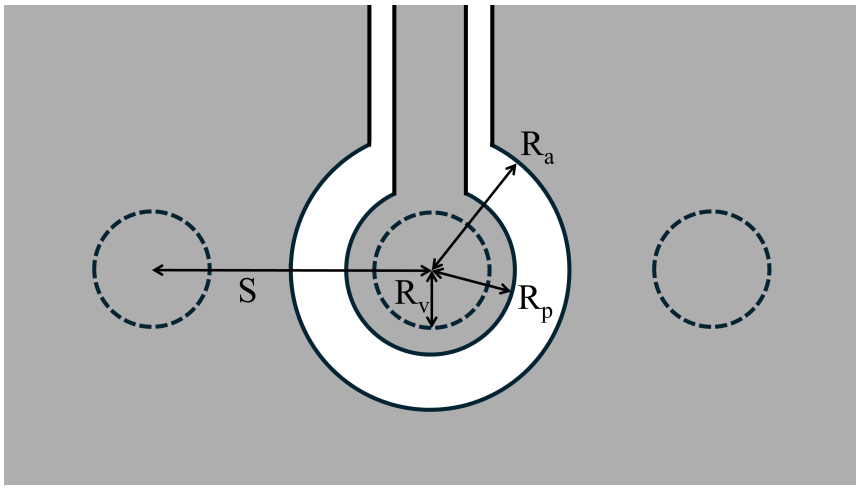


Figure 3.1: Diagram of a top-down view of a TSV transition with dimensions that were varied in the simulation included. Metallised regions are coloured grey and the Si substrate is coloured white. The central CPW trace extends downwards from the top, terminating with the TSV pad. TSVs are defined with dashed lines to highlight their position below the metal layer. A ground plane covers the majority of the rest of the area. R_v = TSV radius, R_p = pad radius, R_a = anti-pad radius, S = TSV separation.

It was found that, for all simulated frequencies and parameter combinations, $|\text{S}_{11}| < -11.9\text{dB}$ and $|\text{S}_{21}| > -0.3\text{dB}$, as shown in figure 3.2 (a) and (b). The parameter combinations that gave the highest transmission at lower frequencies also gave the lowest transmission at higher frequencies and vice versa. The choice was, therefore, made to proceed with a combination of parameters that fell within the middle of the spread. These were: $R_a = 0.042\text{mm}$, $R_p = 0.03\text{mm}$ and $S = 0.094\text{mm}$. An image of the simulated structure, with the wave ports removed for clarity, is shown in figure 3.2 (c). Though there is a characteristic shape to the S_{21} curves, they all fall within a reasonably narrow range of S_{21} values. The values for S_{11}, however, fall over a much

broader range, with local maxima at 3.80GHz and 9.98GHz and a minimum at 7.26GHz. These extrema are a result of resonance conditions related to the size of the chip and are discussed further in section 3.3.

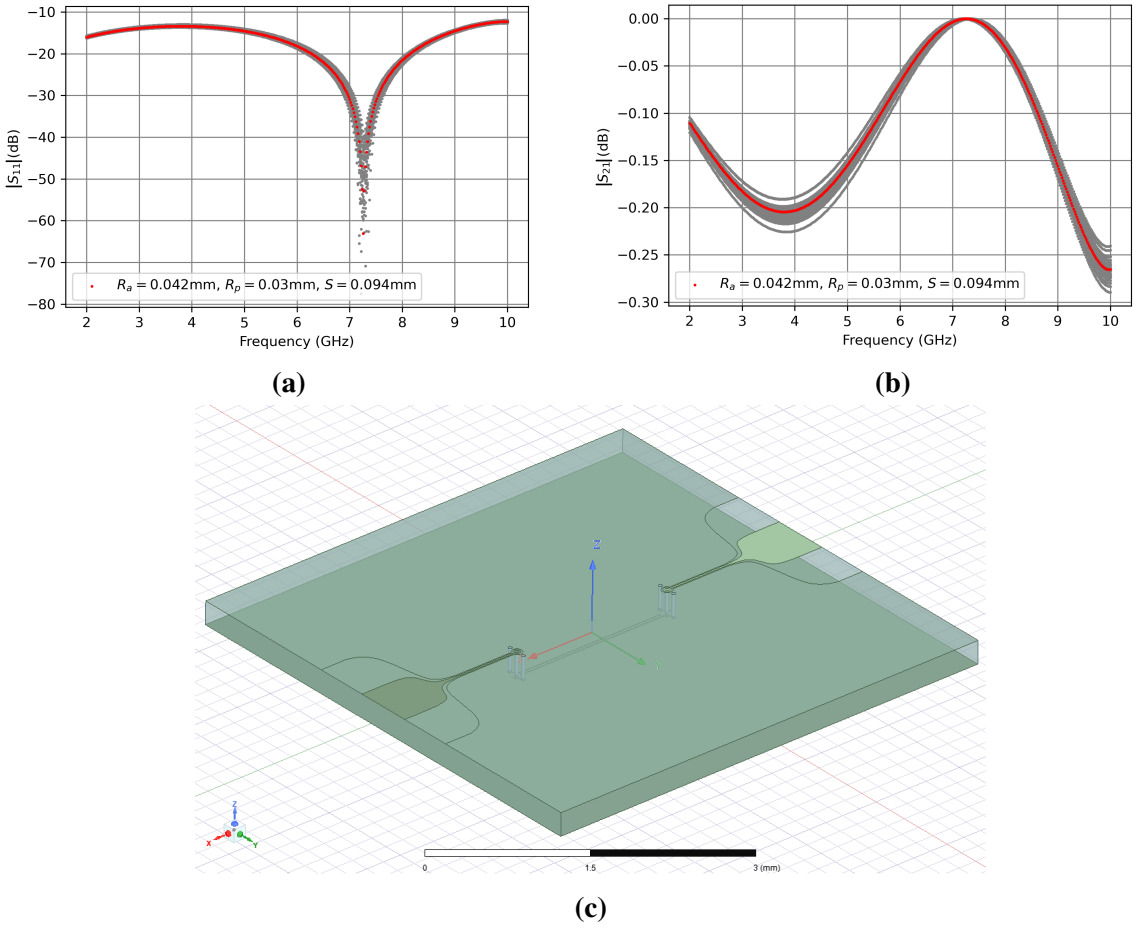


Figure 3.2: Simulated S_{11} (a) and S_{21} (b) of a CPW interrupted by two TSV transitions for various parameter combinations. The highlighted curve represents $R_a = 0.042$mm, $R_p = 0.030$mm, $S = 0.094$mm, the parameter combination chosen for all following simulations. (c) Image of the simulated structure.

After this initial simulation, ground TSVs flanking the CPW were added to the structure. These are often used to connect the top and bottom ground planes of the structure to allow current flow between them and therefore reduce the formation of chip modes in the device. All simulated variables were kept the same for this simulation. The resulting S_{11} profile of the structure was similar to the structure without the ground TSVs, though the minimum appeared to shift to 7.90GHz for the majority of tested parameter combinations. S_{11} was also slightly higher towards the end of the frequency range. The overall shape of the transmission profile changed correspondingly, with a peak at 7.90GHz, though the transmission was very slightly lower as the frequency approached 10GHz. These results and an image of the simulated structure are given in figure 3.3.

As with the previously simulated structure, there was a gradual shift in the S-parameter re-

sponse as the geometric parameters were varied. However, in contrast to the previous simulation, two of the simulated parameter combinations ($R_a = 0.040$mm, $R_p = 0.028$mm, $S = 0.094$mm and $R_a = 0.040$mm, $R_p = 0.032$mm, $S = 0.094$mm) resulted in a larger shift in the response. Curiously, this shift was not continuous with respect to R_p as the combination $R_a = 0.040$mm, $R_p = 0.030$mm, $S = 0.094$mm (the same combination that was highlighted in figure 3.2) did not lie between the other two, as would perhaps have been expected.

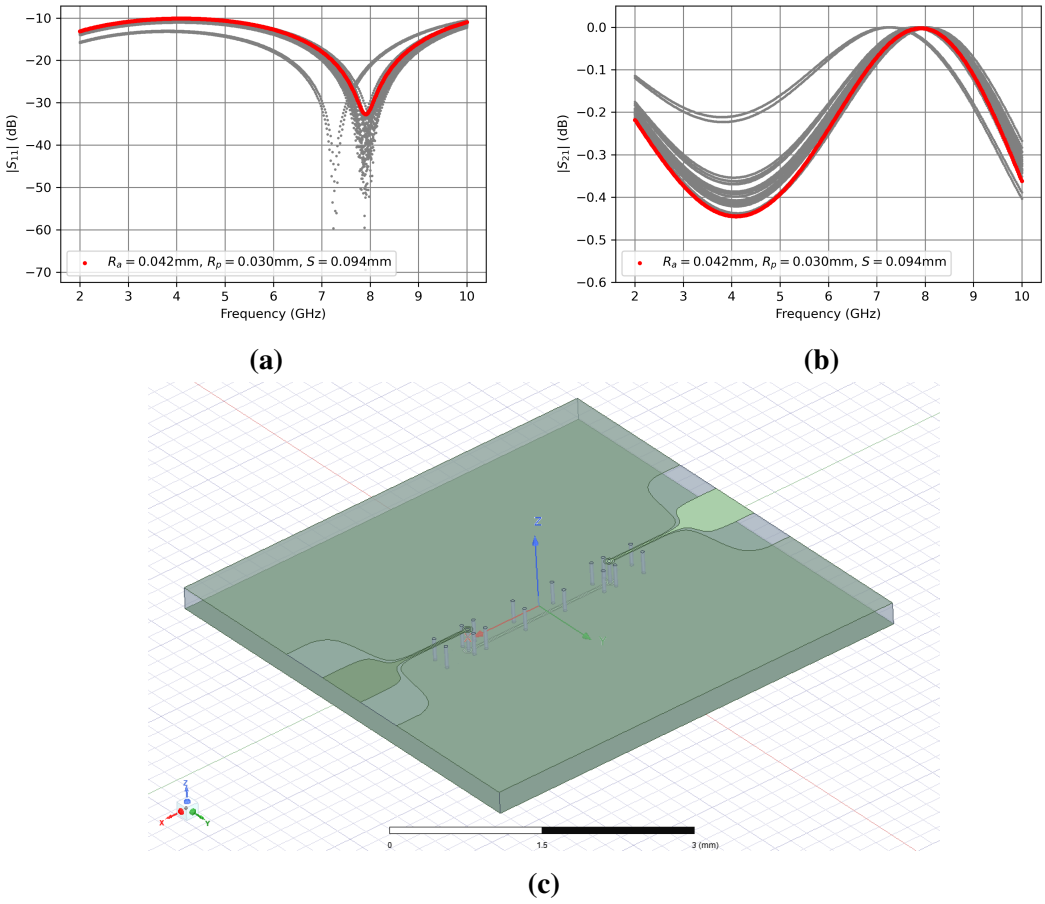


Figure 3.3: Simulated S_{11} (a) and S_{21} (b) of a CPW interrupted by two TSV transitions and flanked by TSVs connecting the ground planes. (c) Image of the simulated structure.

To determine the effect of increasing the number of TSV transitions along the CPW, a device was also simulated with six TSV transitions, with all other geometrical and simulation parameters kept the same. The results are displayed in figure 3.4. A peak in transmission and minimum in reflection was observed at 6.2GHz. The shape of the two profiles was again very similar to those observed in the previous simulations, though showed a slight decrease in transmission at lower frequencies and an additional local minimum was observed at 9.6GHz. It is possible that this minimum would exist at a frequency beyond 10GHz in the previous two simulations and that the negative shift in the positions of the extrema demonstrates a decrease in the oscillation period of the response.

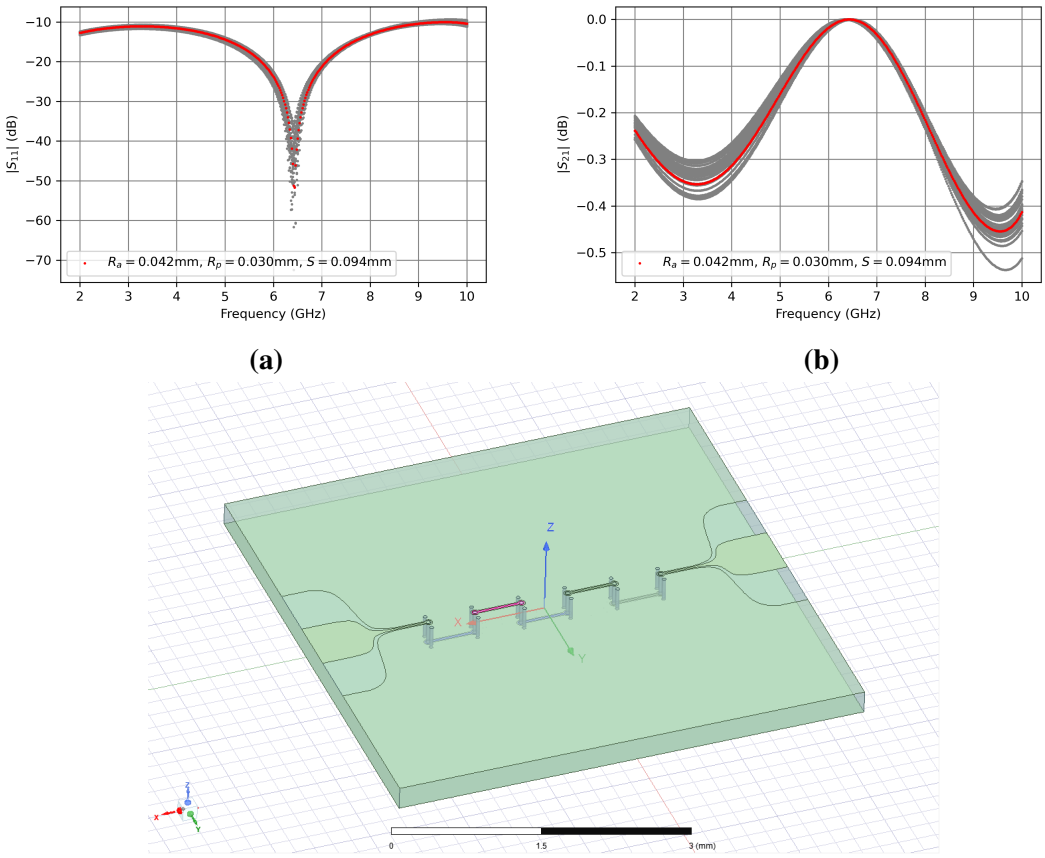


Figure 3.4: Simulated S_{11} (a) and S_{21} (b) of a CPW interrupted by six TSV transitions. (c) Image of the simulated structure.

The final simulated device was identical to the one shown in figure 3.2, save for the inclusion of two TSV-interrupted CPW resonators capacitively connected to the central CPW line. These resonators were designed such that portions of the meandered CPW part were positioned on the top and bottom of the substrate and connected by TSVs. Each resonator was designed to be of different lengths and therefore different resonance frequencies. The geometric parameters chosen for the TSVs in this device were the same as were highlighted in the previous examples: $R_a = 0.040$mm, $R_p = 0.030$mm, $S = 0.094$mm. The results of these simulations are shown in 3.5. An S-Parameter simulation was performed and the frequencies of the two resonances were determined to be 5.87GHz and 7.42GHz. These structures were designed to test the feasibility of incorporating TSVs into CPW resonators in the interest of reducing the footprint of said resonators and with a view to the future fabrication of these devices.

In figure 3.6 the simulated S-parameters for all of the devices discussed in this section are compared for the geometric parameters chosen for the fabricated samples ($R_a = 0.042$mm, $R_p = 0.030$mm, $S = 0.094$mm). The return and insertion loss profiles of the devices for this set of parameters were deemed sufficient to proceed with the fabrication. $S_{11} < -10$dB at all

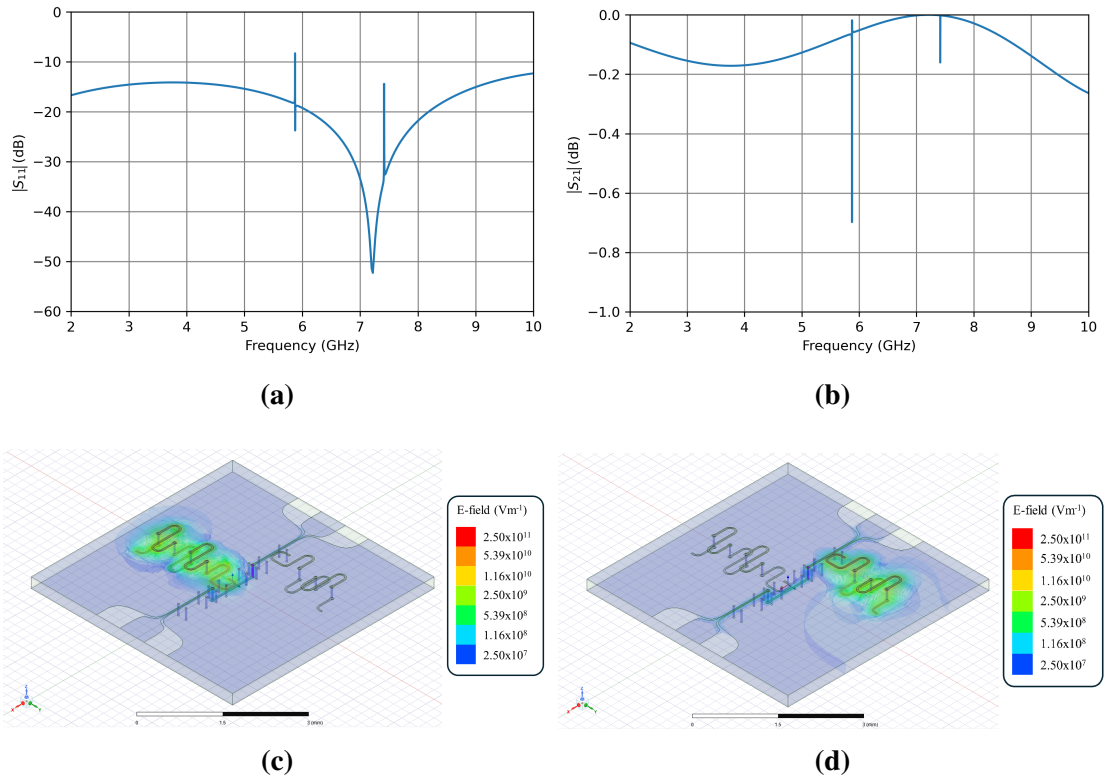
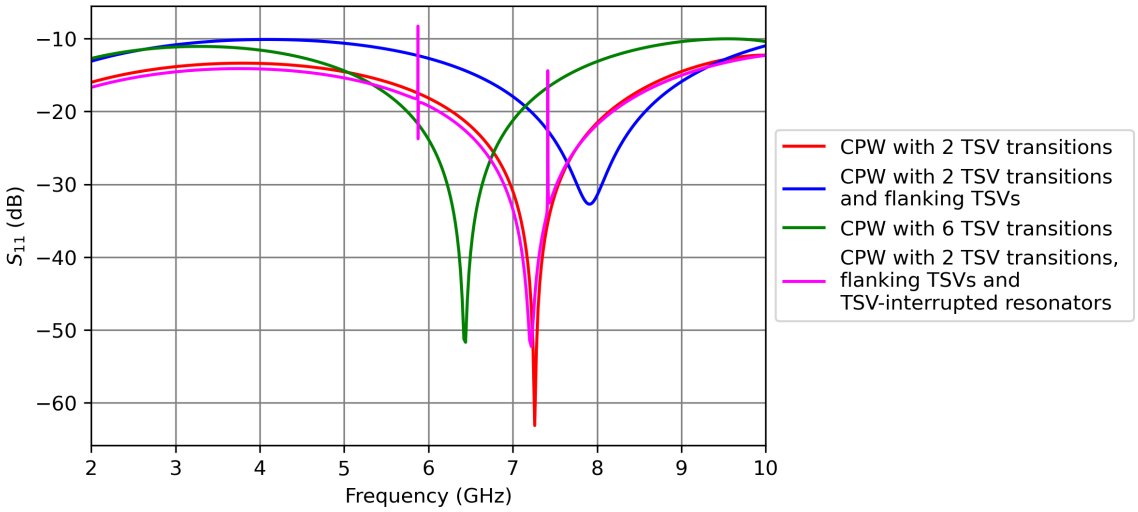
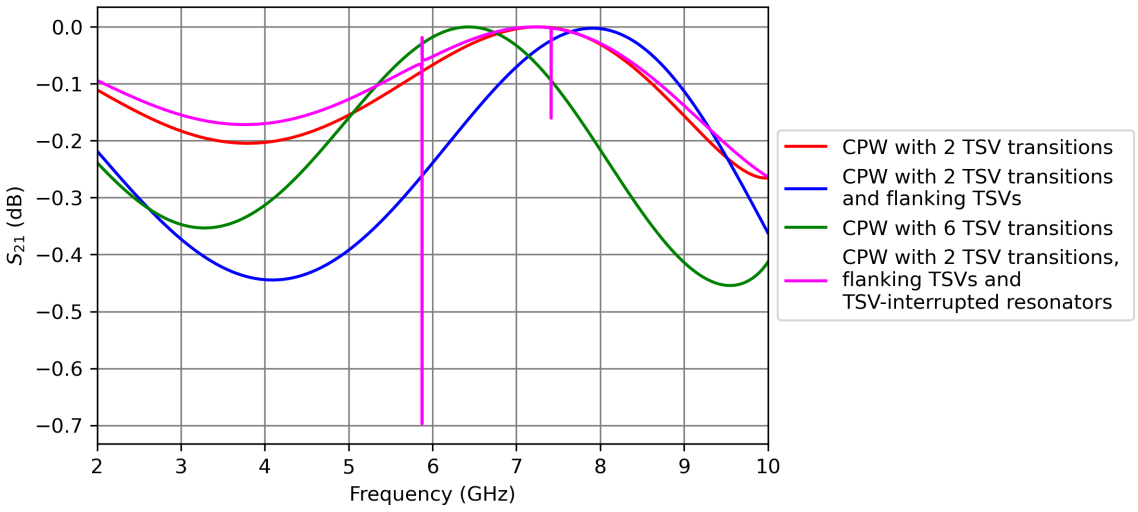


Figure 3.5: Simulated S_{11} (a) and S_{21} (b) of a CPW interrupted by two TSV transitions and capacitively coupled to a TSV-interrupted half-wavelength CPW resonator. Colour plot representations of electric field strength at the resonance frequencies of 5.87GHz (c) and 7.42GHz (d). The substrate has been made partially transparent so that the TSVs may be viewed.

frequencies for all the devices tested, which is a reasonable benchmark. Similarly, aside from the local minimum caused by the resonator, $S_{21} > -0.5$dB for all devices at all frequencies.



(a)



(b)

Figure 3.6: Comparison of the simulated S_{11} (a) and S_{21} (b) of the devices discussed so far for geometric parameters $R_a = 0.042$mm, $R_p = 0.030$mm, $S = 0.094$mm.

3.2 Design of TSV-Integrated Tunable Coupler

The overarching goal of 3D integration of superconducting circuits is to expand the variety of architectures available to designers and thereby allow for the creation of larger and more densely packed circuits. The most common use of TSVs in this respect is to break the 2D wiring plane and to allow the routing of signals through the substrate as well as across it. While this is an undoubtedly useful application of the technology that has the potential to greatly increase the number of addressable qubits on a chip, for example, the true potential of TSVs in quantum circuits may only have just begun to be explored. Instead of merely using them as interconnects, the number of applications of TSVs may expand dramatically if they were instead considered as elements of the quantum devices themselves. Recent work from MIT Lincoln Lab has shown that TSVs may be used as the capacitive element in a transmon qubit [80]. With circuit scalability at its core, the idea behind this innovation is that the on-chip area of the high-aspect ratio TSV is much smaller than that of the large capacitor pads of the standard transmon qubit. The replacement of these pads with TSVs across a whole chip has the potential to save a large proportion of the area per qubit and thereby allow for an larger number of qubits per chip.

Taking inspiration from this work, this chapter will describe a tunable coupler based on the TSV-transmon. The advantage of such a coupler is two-fold. First, as tunable couplers generally take the form of qubits themselves, with slight adjustments to their parameters, the area saved on chip will be as large as for a standard transmon qubit. Second, as the coupler is 3 dimensional, it opens possibilities for the connection of qubits through the substrate or across its bottom side, opening the door to, for example, the coupling of qubits beyond their nearest neighbours.

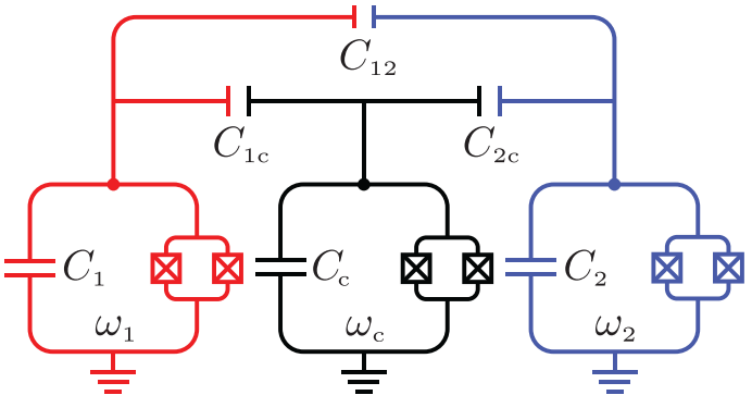


Figure 3.7: Qubit-coupler-qubit schematic with associated capacitances (adapted from [98].)

In this initial study, the operating principles of the designed coupler will be based on the works of F. Yan and Y. Sung from 2018 and 2021, respectively [98,99]. The simulation software ANSYS Q3D will be used to simulate the mutual capacitances of a qubit, coupler, qubit three-body system and the critical device parameters will then be calculated to show the feasibility of

the scheme. The two qubits that are to be coupled together will initially take the form of standard planar Xmon qubits in order to simplify the design of the device. To begin, following [98], the theory on which the scheme is based will be restated in order to provide a framework for the following discussion. The two-level Hamiltonian of the coupled three-body system, a diagram of which is shown in figure 3.7, may be stated:

$$H = \sum_{j=1,2} \frac{1}{2}\omega_j \sigma_j^z + \frac{1}{2}\omega_c \sigma_c^z + \sum_{j=1,2} g_j(\sigma_j^+ \sigma_c^- + \sigma_j^- \sigma_c^+) + g_{12}(\sigma_1^+ \sigma_2^- + \sigma_2^- \sigma_1^+), \tag{3.1}$$

where σ_λ^z, σ_λ^+ and σ_λ^- $(\lambda = 1,2,c)$ are, respectively, the Pauli-Z, raising and lowering operators defined in the eigenbasis of the corresponding mode. Assume that both qubits are negatively detuned from the coupler, $\Delta_j \equiv \omega_j - \omega_c < 0$ and that the coupling is dispersive $g_j \ll |\Delta_j|$, $(j = 1,2)$. The negative detuning is key to the function of the coupler, as will be shown later, and the dispersive coupling suppresses leakage to the coupler's higher excited states.

The virtual exchange interaction between the qubits mediated by the coupler can be approximated by the Schrieffer-Wolff transformation (SWT) $U = \exp\left\{\sum_{j=1,2} \frac{g_j}{\Delta_j}(\sigma_j^+ \sigma_c^- + \sigma_j^- \sigma_c^+)\right\}$, which decouples the coupler from the system up to second order in $\frac{g_j}{\Delta_j}$, resulting in an effective two-qubit Hamiltonian:

$$\hat{\tilde{H}} = \hat{U}\hat{H}\hat{U}^\dagger = \sum_{j=1,2} \frac{1}{2}\tilde{\omega}_j \sigma_j^z + \left(\frac{g_1 g_2}{\Delta} + g_{12}\right)(\sigma_1^+ \sigma_2^- + \sigma_2^- \sigma_1^+), \tag{3.2}$$

where $\tilde{\omega}_j = \omega_j + \frac{g_j^2}{\Delta_j}$ is the Lamb-shifted qubit frequency and $\frac{1}{\Delta} = \frac{1}{2}(\frac{1}{\Delta_1} + \frac{1}{\Delta_2}) < 0$. Assume also that the coupler remains in its ground state at all times. The combined coupling term represents the total effective qubit-qubit coupling, $\tilde{g}$. Here is where the significance of the negative detuning is made clear. As g_1, g_2 are both dependent on ω_c and $\frac{1}{\Delta} < 0$, there must exist some value of ω_c such that the effective coupling $\tilde{g} = 0$ and the coupling between the qubits is thus turned off. The coupling can be made negative or positive by decreasing or increasing ω_c, respectively. This allows the experimentalist to choose the strength of the coupling and also when it is switched on and how long for.

Consider a three mode circuit (ω_1, ω_c, ω_2), depicted in figure 3.7, in which the three devices are pairwise capacitively connected. Each mode represents a superconducting quantum nonlinear oscillator formed by a dominant capacitance (C_1, C_2, C_c) and a non-linear inductance in parallel. These capacitances are of the same order of magnitude. The qubit-qubit, C_{12} and qubit-coupler, C_{jc} $(j = 1,2)$, capacitances are small compared to C_1, C_2 and C_c, so the couplings are perturbative. Equation 3.1 is obtained by quantizing the circuit, with coupling terms. A full treatment of this can be found in [98]:

$$g_j \approx \frac{1}{2}\frac{C_{jc}}{(C_j C_c)^{\frac{1}{2}}}(\omega_j \omega_c)^{\frac{1}{2}}, (j = 1,2), \tag{3.3}$$

$$g_{12} \approx \frac{1}{2}\Big(\frac{C_{12}}{(C_1C_2)^{\frac{1}{2}}} + \frac{C_{1c}C_{2c}}{(C_1C_2C_c^2)^{\frac{1}{2}}}\Big)(\omega_1\omega_2)^{\frac{1}{2}}. \tag{3.4}$$

The qubit-qubit coupling, g_{12} has two contributions. The first term in the brackets in equation 3.4 is from the direct capacitive connection between the qubits. The second term is from the indirect capacitive connection via the intermediate capacitance network formed by C_{12}, C_{2c} and C_c.

The weak anharmonicity of transmon qubits allows the generalisation of the model by including multilevels and counter-rotating terms. The effective qubit-qubit coupling can be obtained:

$$\tilde{g} = \frac{1}{2}\Big(\frac{\omega_c}{2\Delta}\eta - \frac{\omega_c}{2\Sigma}\eta + \eta + 1\Big)\frac{C_{12}}{(C_1C_2)^{\frac{1}{2}}}(\omega_1\omega_2)^{\frac{1}{2}}, \tag{3.5}$$

where $\eta = \frac{C_{1c}C_{2c}}{C_{12}C_c}$, $\frac{1}{\Sigma} = \frac{1}{2}(\frac{1}{\Sigma_1} + \frac{1}{\Sigma_2})$ and $\Sigma_j = \omega_j + \omega_c$. The four terms in the bracket represent the virtual exchange interaction via the $|010\rangle$ state (indirect qubit-qubit coupling), the virtual exchange interaction via the $|111\rangle$ state (indirect qubit-qubit coupling), the capacitive coupling via the intermediate capacitance network (direct qubit-qubit coupling, indirect connection) and the direct capacitive coupling between nodes (direct qubit-qubit coupling, direct capacitive connection). The qubit-qubit capacitive connection is usually much weaker than the qubit-coupler coupling ($C_{12} \ll C_{1c}, C_{2c}$). However, since the virtual interaction is a second-order effect, these four terms have the same order of magnitude in their strength.

Since the qubits are negatively detuned from the coupler, we have that $\frac{\omega_c}{2\Delta} - \frac{\omega_c}{2\Sigma} + 1 \leq 0$ (resulting from the combined effect of the first three terms just discussed), where the equality holds when the coupler frequency goes to infinity. Therefore it can again be seen that there exists some value of ω_c for which the coupling factor $\tilde{g} = 0$.

3.2.1 Impedance of TSV Transition

The first element of the design that should be fixed is the form of the TSV transitions that make up the capacitive elements of the proposed coupler. Ideally, these should maintain the 50Ω impedance of the CPW lines to which they are connected in order to reduce reflections as far as possible and maintain signal integrity. This requires the inclusion of ground TSVs that flank the central TSVs connected to the inductive element of the coupler [100]. It has been shown that using four ground TSVs in this way most effectively prevents the signal TSV from coupling to resonant modes located elsewhere on the device. An image of the simulated structure is shown in figure 3.8.

The impedance of the structure is determined by its geometry. As in section 3.1, there is an infinite parameter space to choose from. The first parameter that should be considered is the radius (R_v) of each of the five TSVs in the transition. This is fixed at 10μm. This value is chosen as it results in an aspect ratio of 25:1, given the 500μm thick substrate, which is at the top end of

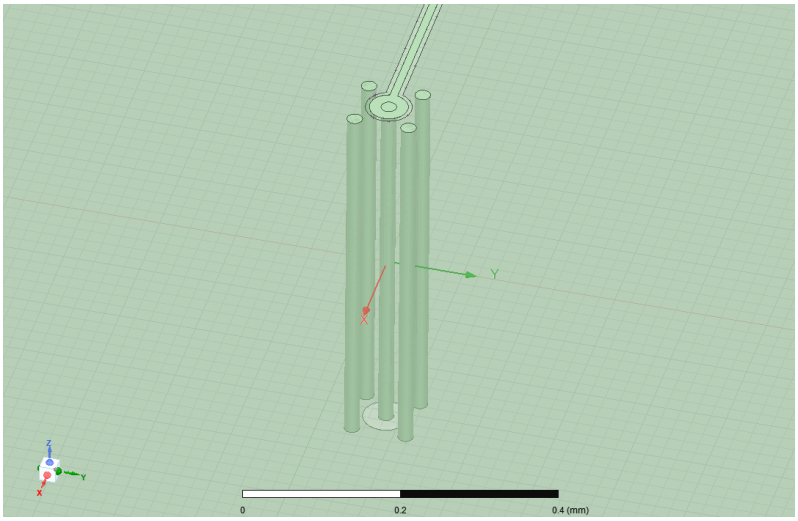


Figure 3.8: Image of the structure simulated to extract the impedance of the TSV transition. A CPW line runs from the edge of the chip to the TSV transition in the centre. Wave ports are placed at the end of the CPW line and the TSV transition. The Si substrate has been made partially transparent and the wave ports have been removed for clarity.

current literature values, yet is still achievable in terms of fabrication. The remaining parameters that were considered were the centre to centre separation distance between the signal TSV and the ground TSVs (S), the TSV pad radius (R_p) and the TSV anti-pad radius (R_a). Generally, it is best to minimise this separation of the signal and ground TSVs as it reduces radiative loss from the signal TSV and also pushes the frequencies of resonant modes between the ground TSVs outwith the operating range of the device [100, 101]. The initial set of parameter combinations were as follows: S from 0.025mm to 0.05mm in steps of 0.005mm, R_p from 0.01mm to 0.045mm in steps of 0.005mm and R_a from 0.015mm to 0.05mm in steps of 0.005mm. This results in a list of 384 parameter combinations, however after applying the restrictions that $2R_v < S$, $R_p < R_a$ and $R_p < S - R_v$, so as to avoid the intersection of the simulated objects, this list was reduced to 132 combinations. 19 of the simulations did not converge to a solution and so there were 113 total combinations that gave a result. Of these, 8 resulted in an impedance value that was fell within a range of $50\Omega \pm 1\Omega$. These are displayed in table 3.1.

The impedance of the TSV transition was determined by following the method described in [102]. A single TSV transition was embedded in the centre of a 500μm thick Si substrate and attached to a 50Ω CPW line running from the edge of the substrate. The capacitance and inductance of the structure were simulated in the ANSYS Q3D extractor both with and without the central signal TSV and the difference between the two results for capacitance and for inductance were found and assumed to be the incremental capacitance and inductance of the TSV. The CPW was included in the simulation as the capacitance and inductance values depend on the surrounding structures as well as on the shape of the TSV itself. The solution frequency was set to 10GHz. This value was selected as it is the highest frequency in the range of interest

Table 3.1: Simulated TSV transition parameter combinations that resulted in an impedance closest to 50Ω.

R_a **(mm)**	R_p **(mm)**	**S (mm)**	$L_{incremental}$ **(nH)**	$C_{incremental}$ **(fF)**	**Z (Ω)**
0.03	0.025	0.05	0.055	219.61	50.17
0.03	0.025	0.045	0.607	236.34	50.34
0.02	0.01	0.045	0.588	230.42	50.52
0.03	0.02	0.05	0.514	210.89	49.38
0.015	0.01	0.045	0.599	232.84	50.73
0.04	0.03	0.05	0.582	225.97	50.75
0.045	0.02	0.045	0.564	218.78	50.76
0.04	0.025	0.05	0.561	216.27	50.91

and as it is sufficiently high for the TSV to fall under the influence of the skin effect, meaning there is no significant difference between the simulated values for solid and hollow TSVs [102]. The simulated TSVs were solid cylinders due to meshing requirements in the Q3D extractor, whereas in practice they are formed by a thin metal layer lining the hole etched into the substrate. The desired solution accuracy was set to 0.1%. The values of incremental capacitance and inductance were then used to calculate the impedance using equation 3.6

$$Z = \sqrt{\frac{L}{C}}. \tag{3.6}$$

One advantage of this method of determination of TSV impedance is that it allows for the inclusion of the kinetic inductance (L_k) of the TSV in the calculation of impedance. The TSVs are assumed to be metallised with TiN and the L_k of TiN was taken to be 22.2pH/□ [103]. Multiplying this value by the ratio of the TSV's length to its circumference gives a total kinetic inductance of $L_k = 197.47$pH. This is of the same order as the simulated values of geometric inductance and therefore kinetic inductance and will, therefore, have a significant impact on the impedance of the transition and should not be neglected. The values of impedance calculated including and excluding kinetic inductance are shown in table 3.2.

It can be seen that the inclusion of kinetic inductance in the calculation of the impedance of the structure significantly alters the combination of parameters that result in an impedance closest to 50Ω. Note that the first four parameter combinations in this list violate at least one of the three stipulations previously mentioned. Therefore, the parameters chosen for the remainder of the simulations carried out are therefore: $R_a = 0.035$mm, $R_p = 0.025$mm and $S = 0.05$mm, giving an impedance of $Z = 49.78\Omega$.

Table 3.2: Simulated via transition parameter combinations that resulted in an impedance closest to 50Ω when L_k is included in the calculation.

R_a **(mm)**	R_p **(mm)**	**S (mm)**	$L_{incremental} + L_k$ **(nH)**	$C_{incremental}$ **(fF)**	**Z (Ω) inc.** L_k
0.04	0.02	0.035	0.746	298.34	50.01
0.045	0.025	0.045	0.554	221.16	50.06
0.035	0.03	0.05	0.565	226.83	49.93
0.035	0.02	0.045	0.584	232.06	50.17
0.035	0.025	0.05	0.532	214.61	49.78
0.025	0.01	0.045	0.574	227.49	50.24
0.04	0.015	0.045	0.567	229.42	49.73
0.05	0.03	0.05	0.553	218.88	50.28

3.2.2 Simulation of Component Capacitance

Note on Capacitance Extracted from the ANSYS Q3D Solver

ANSYS Q3D can display a Maxwell capacitance matrix (equation 3.7) or a SPICE capacitance matrix (equation 3.8). Here, the values extracted from the SPICE matrix are used.

$$\begin{bmatrix} C_{11}^M & C_{12}^M & C_{13}^M \\ C_{12}^M & C_{22}^M & C_{23}^M \\ C_{13}^M & C_{23}^M & C_{33}^M \end{bmatrix} = \begin{bmatrix} C_{11}+C_{12}+C_{13} & -C_{12} & -C_{13} \\ -C_{12} & C_{12}+C_{22}+C_{23} & -C_{23} \\ -C_{13} & -C_{23} & C_{13}+C_{23}+C_{33} \end{bmatrix}, \tag{3.7}$$

$$\begin{bmatrix} C_{11} & C_{12} & C_{13} \\ C_{12} & C_{22} & C_{23} \\ C_{13} & C_{23} & C_{33} \end{bmatrix}, \tag{3.8}$$

where the capacitances, C_{ij}, $i, j \in \{1,2,3\}$, represent the capacitances illustrated in figure 3.9. Furthermore, Q3D allows one to reduce the capacitance matrix by introducing a floating voltage at infinity. Float at Infinity disconnects the circle in figure 3.9 from ground at infinity; the C_{ii} capacitors still connect to one another at the sphere with unknown voltage, a dependent variable determined by the charge on the other conductors. This enables one to use the local ground as a reference. The simulated capacitances in this report will be taken from the original SPICE matrix.

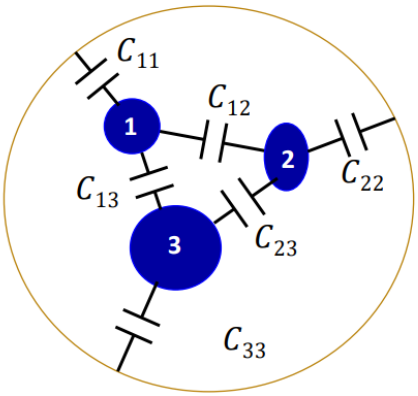


Figure 3.9: Diagram of capacitances between objects in ANSYS Q3D solver, where C_{ij} are capacitances between arbitrary objects in the model. Adapted from [104].

Note on Coupler Design

As previously addressed, the TSV transitions in the coupler should be as close to 50Ω as possible to mitigate losses. The simulated coupler design will, therefore, include the four ground TSVs, as described above. In the current chip design, the qubits to be coupled together are in the form of Xmons, with large planar capacitive elements. The majority of the mutual capacitance between the coupler and the qubits will, therefore, come from the meandered planar element of the coupler, with relatively little coming from the TSV section. However, if the qubits to be coupled together were to also use TSVs as their capacitive elements, some attention will have to be paid as to whether enclosing the signal TSVs from all three devices in these TSV cages will affect this capacitance. It may then be beneficial to investigate other arrangements of ground TSVs. However, for now the TSV transition will be designed as a signal TSV enclosed with four ground TSVs with a view to comparing it to other options in future.

Self and Mutual Capacitance of Circuit Elements.

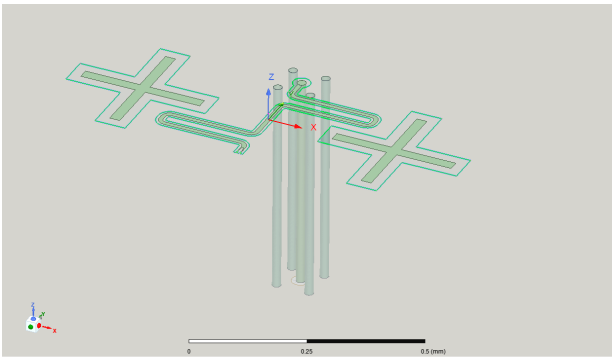


Figure 3.10: Structure used to simulate the capacitances of the coupler and qubits. The top ground plane has been made partially transparent for clarity.

An image of the simulated design is shown in figure 3.10. Ground planes are added to the top and bottom surfaces of a 500μm substrate and two crosses representing the capacitive elements of Xmon type qubits are placed in plane with the top ground. In between these qubits is the coupler, which is formed by a CPW transmission line connected to a central signal TSV. Surrounding this TSV are four ground TSVs embedded into the substrate, connecting the top and bottom ground planes. All conductors, including the sidewall metallisation of the TSVs, are modelled as 100nm thick perfect conductors as this circuit is assumed to operate in a superconducting state. The large meander in the design is used to increase the mutual capacitance between the coupler and the qubits, while allowing for a sufficiently large distance, and therefore small mutual capacitance, between the two qubits. The coupler and each of the qubits were assigned as signal nets to allow the simulation of capacitances between the structures. The ground TSVs and the top and bottom ground planes were assigned as a single ground net as it is assumed that the chip will be well connected and grounded. The solution frequency was set to 10GHz and the convergence limit per pass was set to 0.1%. The simulated capacitances can be seen in table 3.3. The remaining qubit parameters may now be evaluated, beginning with the charging energies, using the relation $E_c = \frac{e^2}{2C}$. The evaluated energies are shown in table 3.4. The anharmonicities of the qubits fall within a range typical for transmons. The coupler anharmonicity, however, is significantly lower [99].

Table 3.3: Simulated capacitances between the coupler, the qubits and ground.

C_1 (fF)	C_{12} (fF)	C_{1c} (fF)	C_2 (fF)	C_{2c} (fF)	C_c (fF)
75.631	0.025	1.069	75.650	1.049	371.105

Table 3.4: Calculated charging energies of simulated devices.

	Qubit 1	**Qubit 2**	**Coupler**
$\frac{E_c}{h}$**(GHz)**	0.251	0.251	0.052

As all three structures are transmons, the frequencies will depend on the charging and Josephson energies as in equation 2.7. A choice must, therefore, be made as to whether the resonance frequencies of the qubits and coupler are fixed, from which E_J is obtained, or a target E_J is fixed, from which the resonance frequencies are obtained. As Josephson junctions have not been included in the simulation and their parameters vary significantly as a result of fabrication processes, it is reasonable to choose target resonance frequencies, from which the remaining qubit parameters can be calculated. The resonance frequencies are chosen to be $\omega_1 = \omega_2 = 5$GHz and $\omega_c = 6$GHz. The resulting Josephson energies are given in table 3.5. Note that as the coupler is flux-tunable, the value for ω_c is nominal and the coupler's associated Josephson energy is tunable according to $E_{J\Phi} = 2E_J \cos \pi \frac{\Phi}{\Phi_0}$ [28]. The value given in table 3.5 is for E_J, as opposed to $E_{J\Phi}$.

The values of the ratio $\frac{E_J}{E_c}$ for the simulated qubits are typical for transmon qubits. The ratio for the coupler is much higher, necessitated by a smaller anharmonicity.

The coupling strengths between the components may now be evaluated using equations 3.3 and 3.5. Notice here that all the constraints of the design have been adhered to: $\Delta_j < 0$, $g_j \ll |\Delta_j|$ (j = 1,2) and $C_{12} \ll C_{1c}, C_{2c}$.

Table 3.5: Calculated Josephson energies and ratio of Josephson to charging energy of simulated devices.

	Qubit 1	**Qubit 2**	**Coupler**
$\frac{E_J}{h}$**(GHz)**	13.7	13.7	88.5
$\frac{E_J}{E_c}$	54.5	54.5	1701.9

Table 3.6: Calculated coupling coefficients of simulated devices.

g_{1c} **(MHz)**	g_{2c} **(MHz)**	$\tilde{g}$ **(MHz)**
17.47	17.14	0.60

3.3 Simulation of TSV Crosstalk

Crosstalk, or the unwanted parasitic absorbance of energy from one object by the other, is always of concern for circuit designers. An electrical environment in which signals are only transmitted through the channels for which they were intended is plainly beneficial for circuit operation. The design of TSVs is no exception [105–107]. In this section, the crosstalk between neighbouring TSVs is simulated using ANSYS HFSS. In particular, different arrangements of grounding TSVs were modelled and the arrangement which demonstrated the lowest crosstalk was sought.

In a similar fashion to the previous simulations detailed in this section, TSVs were embedded in a 5x5mm Si substrate, each with a 100nm thick perfectly conducting layer coating their interior. 100nm thick perfectly conducting ground planes were added to the top and bottom of the substrate, from which anti-pads were cut around the ends of each TSV. Contact pads were added to the ends of each TSV, as shown in figure 3.11.

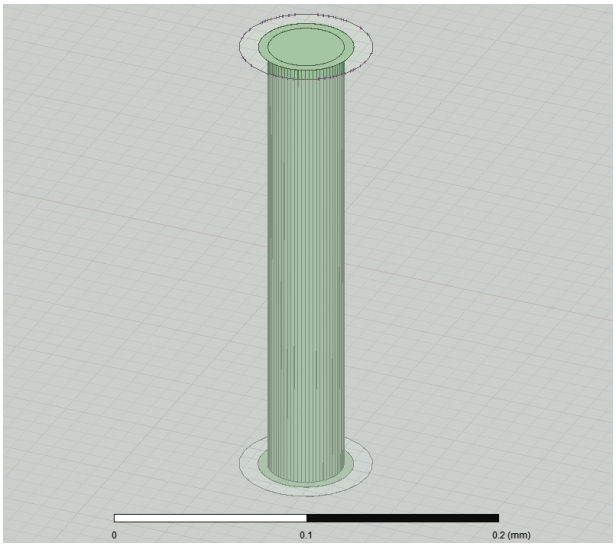


Figure 3.11: HFSS model of a single TSV with pad and anti-pad visible at the top and bottom of the structure. The substrate has been made partially transparent for clarity.

The dimensions of the pads and anti-pads were $R_p = 25\mu$m and $R_a = 35\mu$m, respectively, and the radii of the TSVs was fixed at $R_v = 20\mu$m. Ports were places at each end of the TSVs and the driven terminal solution type was used where the meshing frequency was 5GHz and the iterative solve was carried out until there was <1% variation in the solution between passes. The structures were simulated at 41 points between 4-8GHz.

Four different arrangements of TSVs were analysed. First, two solitary TSVs, with one acting as the signal TSV and the other as the parasitic TSV, were placed 500μm apart, each with ports placed at both ends. The ports on the signal TSV were numbered 1 and 2, and the ports on the parasitic TSV were numbered 3 and 4. S_{41} was used as a measure of the crosstalk between the TSVs. In the same way, two different arrangements of 3-TSV transitions, one with all six TSVs arranged collinearly and one with the two transitions arranged in parallel were simulated,

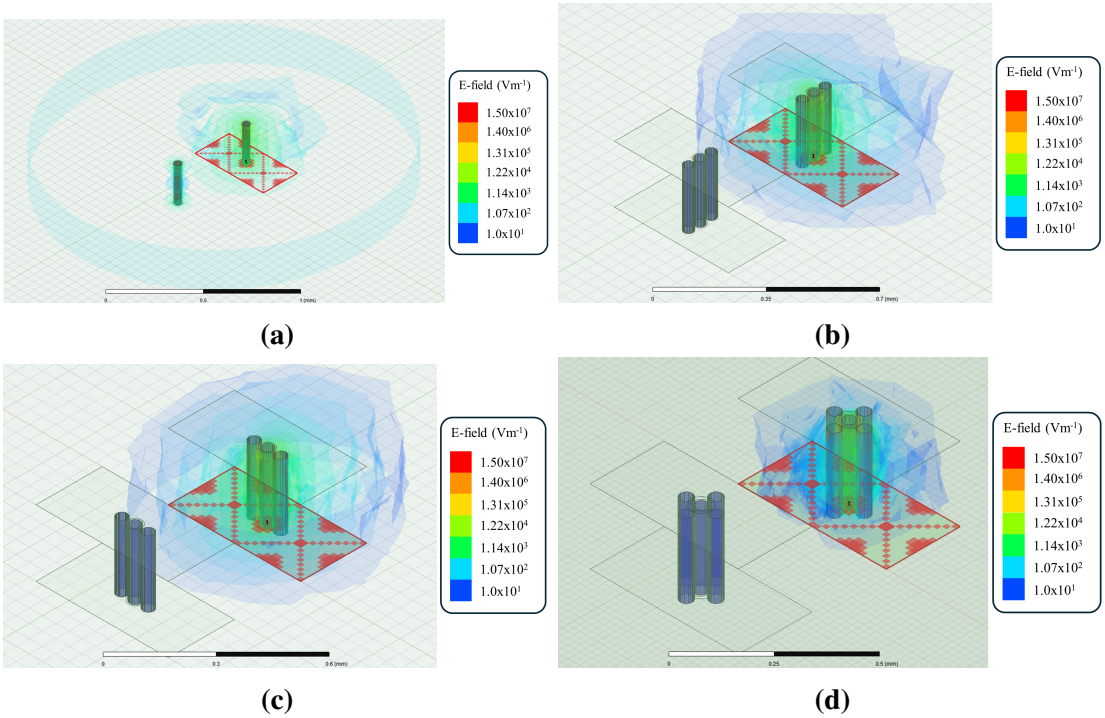


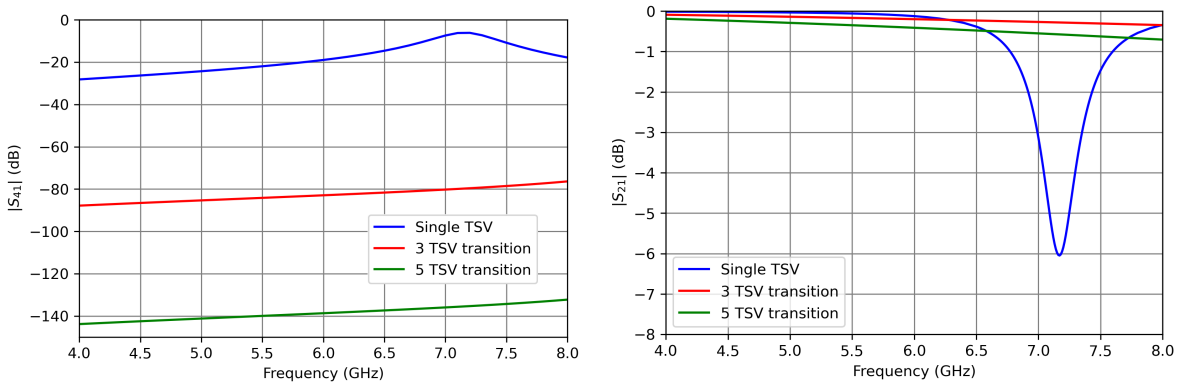
Figure 3.12: (a) Simulated electric field distribution for two single TSV transitions. (b) Simulated electric field distribution for two collinear 3-TSV transitions. (c) Simulated electric field distribution for two parallel 3-TSV transitions. (d) Simulated electric field distribution for two parallel 3-TSV transitions. Port 1 is highlighted in red and green in each image and the other ports have been made semi-transparent. The substrate has also been made partially transparent for clarity. Each pair of signal TSVs are placed 0.5mm apart.

as was a pair of 5-TSV transitions. These structures can be seen in figure 3.12, where they are shown with their simulated electric field distribution plotted.

This demonstrates qualitatively that, as would be expected, the inclusion of additional grounding TSVs confines the electric field to a smaller radius around the signal TSV, thus preventing the coupling of the signal TSV to the parasitic TSV. This is confirmed by the simulation of S_{41}, the results of which are shown in figure 3.13 (a), where a clear decrease in crosstalk is observed as the number of grounding TSVs is increased. The results for the two orientations of 3-TSV transitions were indistinguishable at this scale and they have, therefore, both been represented by the same curve on the plot.

In figure 3.13 (b), a comparison of the S_{21} for the four configurations is shown and a large resonance is present at 7.2GHz in the curve representing the response of the single TSV. This was suspected to be due to coupling of the TSV to substrate modes supported by the chip geometry. Therefore a further simulation was carried out in which the length and width of the substrate was changed and the frequency of the resonance did indeed shift as a result. This shift is shown in figure 3.14.

Eigenmode simulations of the substrate with the TSV removed were also performed for



(a) **(b)**

Figure 3.13: Comparison of simulated S_{41} (a) and S_{21} (b) of various TSV transition arrangements. 41 equally spaced points between 4GHz and 8GHz were simulated.

each of the three substrate dimensions shown in figure 3.14. These determined the fundamental modes for substrates of side length $w = 2.5$mm, 5.0mm, 7.5mm to be 10.3GHz, 7.16GHz and 6.28GHz, respectively, which correspond to the resonances seen in figure 3.14. It is clear from the 3 and 5 TSV transition curves in figure 3.13 that the inclusion of grounding TSVs helps to prevent the coupling of the TSV transitions to these substrate modes.

The collinear and parallel arrangements of the 3-TSV transition were investigated further. As viewed at the scale necessary to capture the full response of the other simulated structures, no observable difference in results could be discerned. However, from figures 3.12 (b) and (c), one can see that the electric fields are largely attenuated over the 0.5mm distance between the two signal TSVs and so it is plausible that if this distance were to be reduced, the degree of crosstalk exhibited by each structure would diverge.

It has been shown that the distance (D) between the signal and parasitic TSVs is a major determining factor in the amount of crosstalk between them and that as this distance is increased, the crosstalk decreases [106]. The simulation of the two orientations of the three-TSV transitions were, therefore, repeated with the distance between the two transitions varied in order to determine whether these different orientations do indeed affect the crosstalk between the TSVs and how that effect varies with the inter-TSV distance. The simulated data is shown in figure 3.15. Ten different inter-TSV distances were chosen, increasing by 0.05mm up to 0.50mm and by 0.50mm thereafter, with the exception of the largest distance, 3.30mm, which was included to negate the possibility of the occurrence a resonance condition in the equally spaced variation.

The data appears to show a general, though not strict, increase in crosstalk for decreasing D. For the five largest distances, the crosstalk does indeed follow this trend. However, as the distance is decreased from 0.50mm, the crosstalk either increased or decreased. This could be due to certain resonance conditions being met in the structure. It could also have been caused by interaction between the fields around the ports at each end of the two transitions, which

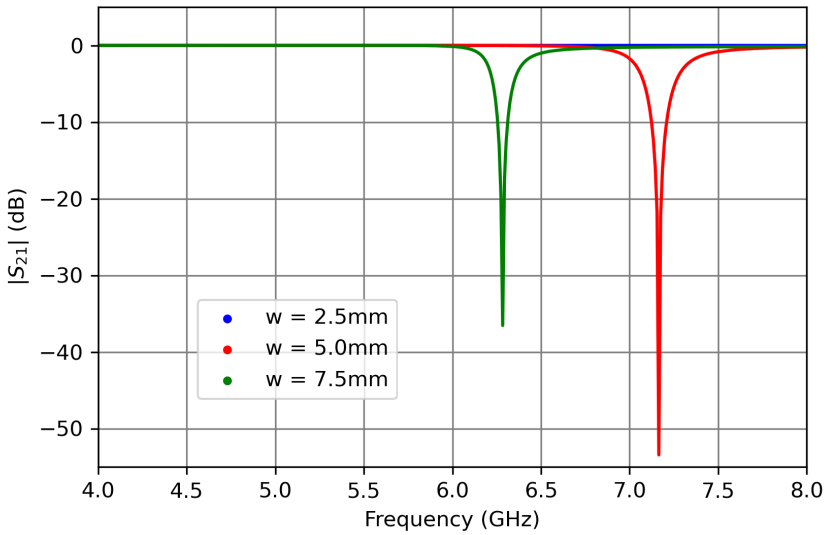


Figure 3.14: Simulated S_{21} of a single TSV for various substrate widths. 188 points were simulated between 4GHz and 8GHz with a denser sweep around the two resonances.

extend outwards from the width of the transition, as shown in figure 3.12. There is also a monotonic increase in S_{41} with frequency for all arrangements and distances. This is due to the small increase in the magnitude of the electric field at a given radius around the signal TSV as frequency increases. An example of this is shown in figure 3.16, where a dominant TM_{00} mode is shown propagating radially from the signal TSV, through the substrate [108].

With the exception of the $D = 0.25$mm and $D = 0.30$mm cases, for which there is a large disparity in the simulated crosstalk of the two TSV transition arrangements, it is difficult to discern the difference in crosstalk between the collinear and parallel structures from figure 3.15. In order to better understand the behaviour of the two arrangements, the difference between the simulated S_{41} values was also plotted in figure 3.17.

The data for four of the simulated distances ($D = 0.35$mm, $D = 0.40$mm, $D = 0.45$mm and $D = 0.5$mm) lie entirely above the line $S_{41,collinear} - S_{41,parallel} = 0$, implying that the crosstalk for these distances is higher for the collinear orientation than the parallel orientation. For the rest of the simulated distances, either all or the majority of the data points fall beneath this line, indicating that the crosstalk was higher for the parallel arrangement. Overall, it appears as if the collinear orientation is slightly preferable to the parallel orientation with respect to crosstalk. However, it is clear that the precise geometry of any particular circuit design will have to be simulated to determine any necessary adjustments in order to reduce the crosstalk as far as possible. Factors such as substrate dimensions and the presence of other TSVs or metal layers will affect the electromagnetic environment of the system and there is, therefore, likely no infallible design rule that may be universally applied to achieve the lowest possible crosstalk.

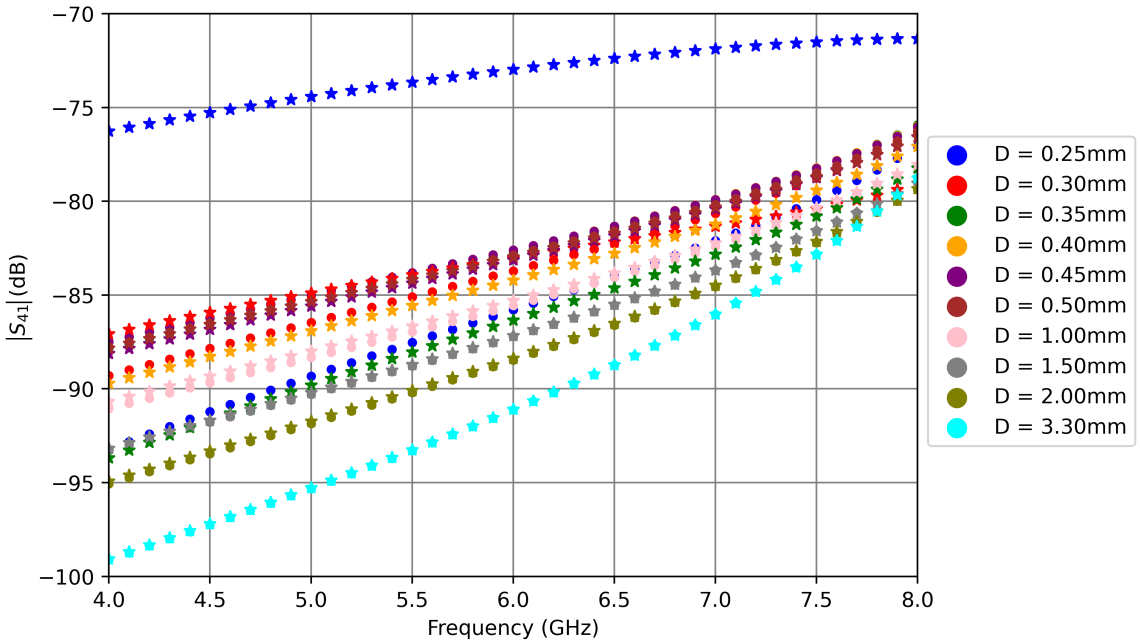
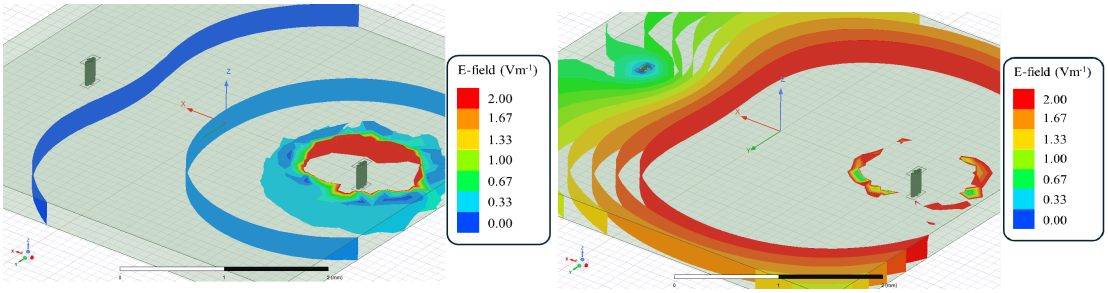
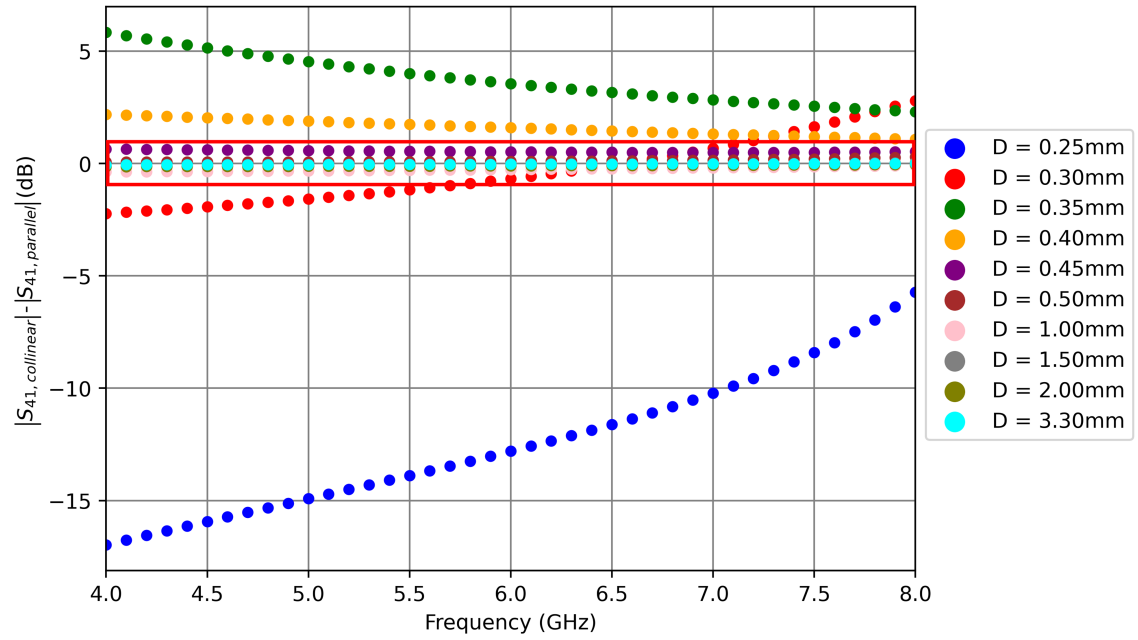


Figure 3.15: Simulated variation of S_{41} with frequency for various inter-TSV distances (D) for each of the two arrangements of the 3-TSV transition. Circular dots represent the data for the transition arranged collinearlly and stars represent the data for the transitions arranged in parallel.

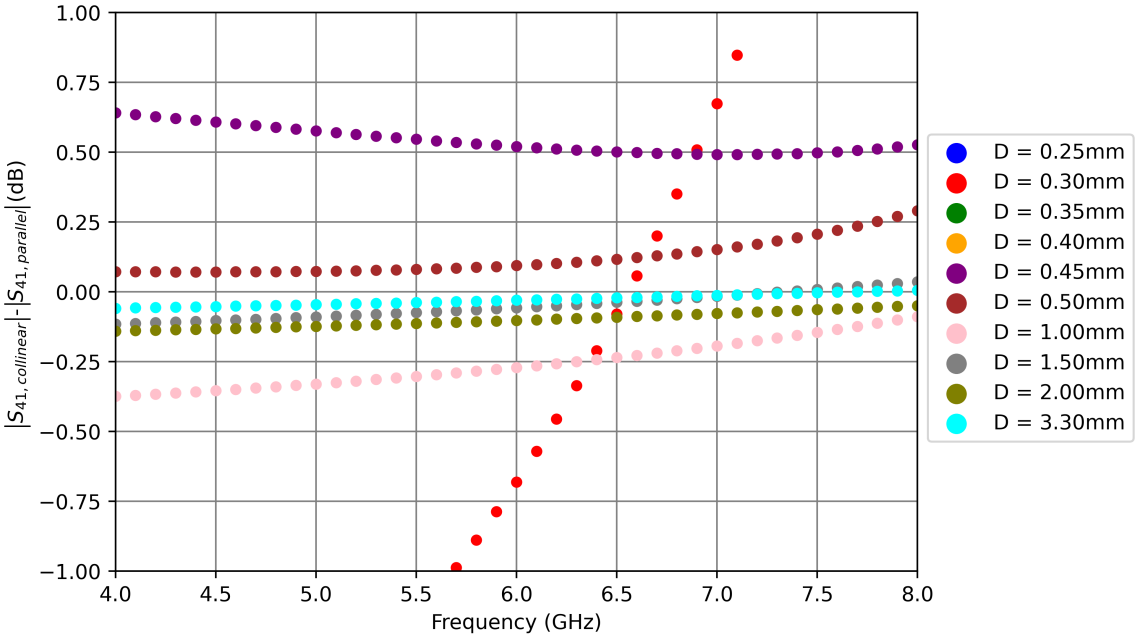


(a) **(b)**

Figure 3.16: (a) Simulated E-field emitted from 3-TSV transition in parallel configuration at 4GHz. The displayed field strengths were limited to 0-2Vm^{-1} to better illustrate the change across the substrate. The true maximum field strength was 3×10^5Vm^{-1}. (b) The simulated E-field for the structure at 7.5GHz.



(a)



(b)

Figure 3.17: (a) Simulated difference in S_{41} between the collinear and parallel arrangements of the TSV transitions for varying frequency and inter-TSV distance (D). Area highlighted in red is shown in (b) to better illustrate the points grouped around $S_{41,collinear} - S_{41,parallel} = 0$.

Chapter 4

Fabrication and Measurement of TSVs

4.1 Fabrication

The fabrication process for the TSV test samples may be broken down into three basic steps. First, the TSVs are patterned by photolithography and etched into the Si substrate using a Bosch etch. Second, layers of a superconducting nitride (TiN or NbN) are deposited on the top and bottom surfaces of the substrate by ALD, and finally, patterns are defined on both nitride layers by photolithography and then etched in a dry-etch process. Each of these steps will be discussed in the following sections. A diagram of the process is shown in figure 4.1 and a full recipe may be found in appendix A.

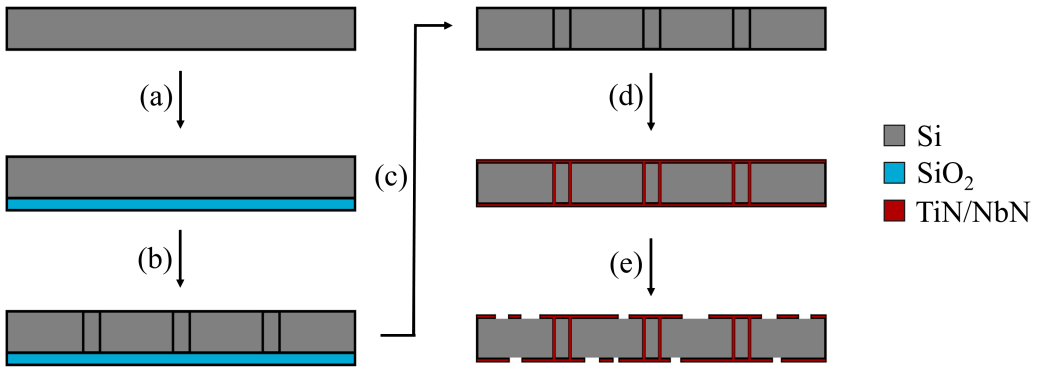


Figure 4.1: Diagram of the fabrication process used. (a) Deposition of SiO_2 etch-stop. (b) Bosch etch of TSVs. (c) Removal of SiO_2 etch-stop by HF wet-etch. (d) Deposition of nitride layer. (e) Dry-etch of nitride layer.

4.1.1 Etch-Stop Deposition

The fabrication process begins with a bare, 4" diameter, 275μm thick intrinsic Si wafer. A 2μm layer of SiO_2, to be used as an etch-stop, was deposited on the reverse side of the wafer by

PECVD in an SPTS Delta deposition system. TSVs fabricated by the Bosch process are often susceptible to *notching*, or the lateral etching of the TSV at its bottom. This can be exacerbated by the use of insulating etch-stops due to charging effects causing the deflection of etching species at the Si-insulator interface. However, the view was taken that the mechanical support provided by a thicker, insulating, etch-stop would be more beneficial than the notch-preventing capabilities of, for example, a thin metallic etch-stop [109]. This etch-stop also prevented contamination of the TSVs with the Santovac pump oil used to bond the substrate to its carrier during the etch [110]. The sample was subsequently cleaned with organic solvents followed by piranha solution and water and was blow-dried with N_2 gas. The wafer was then exposed to an O_2 plasma to remove any organic solvent residues [111].

4.1.2 Bosch Etch

The TSV locations were defined on the top side of the wafer using a 7μm layer of SPR220-7 photoresist which was exposed to UV light through a quartz photomask and developed with the TMAH-based developer, MF-CD-26. In this work, two types of spinners were used to apply photoresist to the sample: manual and automatic. When using the manual spinner, the wafer was placed on a vacuum chuck and the photoresist was applied to its surface with a syringe. The edge-bead was not removed for this application method. The automatic spinner used (SUSS MicroTec RCD8), on the other hand, applied a fixed volume of photoresist through a nozzle, spun the wafer, and then sprayed the edge of the still-spinning wafer with a fine jet of acetone to remove the edge-bead. This edge-bead was added back to the sample using the same tool after the photoresist was exposed in order to protect the edge of the wafer during the etch step. This prevented cracks from forming along the crystal planes of the silicon and reaching the interior of the sample. In both cases the maximum spin speed used was 3500rpm, resulting in a photoresist thickness of 7μm.

The samples were softbaked at a temperature of 115°C after the application of the photoresist. It was found that the 7μm SPR220-7 films were prone to cracking after their removal from the hotplate due to rapid cooling and so the samples were transferred from the 115°C hotplate to a 90°C hotplate to prevent this. This method was found to reduce the number of cracks appearing in the films. Allowing the photoresist used in the later nitride etching step to cool on a watch glass inside a LAF cabinet was sufficient for uniform cooling of these thinner films.

The etching tools used for the Bosch etch step of the process employed electrostatic clamps to hold samples in place. These were designed to hold samples of 6" diameter and for this reason, it was necessary to temporarily bond the 4" diameter sample substrates to a 6" carrier wafer. The method of bonding the sample to its carrier wafer was found to be critical in achieving a good quality Bosch etch. Santovac 5(P) oil was used as the bonding agent for the wafers and, initially, a small amount was applied to the carrier wafer using a pipette dropper, after which the

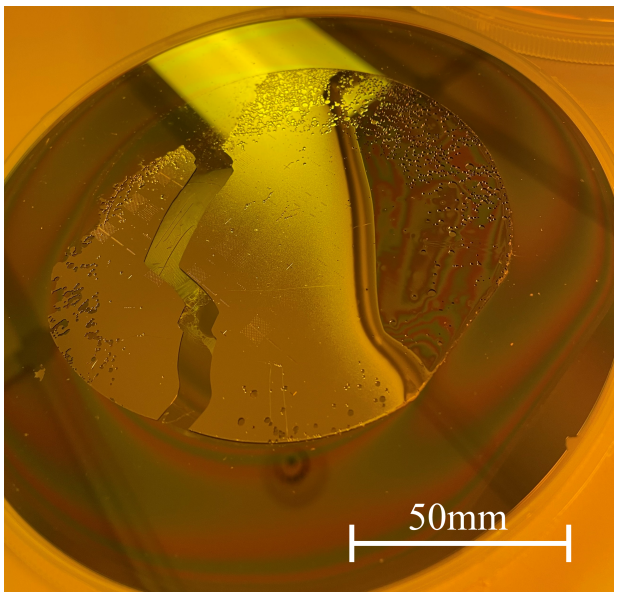


Figure 4.2: Example of the effect of run-away heating due to poor thermal conduction. The left half of the sample has debonded from the carrier wafer whereas the right half still has photoresist remaining on its surface.

sample was placed on top. It was found, however, that this method did not result in a bond with sufficient thermal conductivity for the transference of heat between the sample and the carrier. This is necessary as the carrier is cooled from below by He_2 gas inside the reaction chamber. When heat transfer was inadequate, the areas of the sample locally heated by the etch were found to etch faster, which further increased the rate of heating in these areas, and so on until the sample became badly over-etched. The application of the Santovac at room temperature, while it was still viscous, also encouraged the formation of bubbles in the oil. As the Santovac spread between the sample and the carrier, so did these bubbles, creating regions underneath the wafer where there was very poor heat transfer. These bubbles may also have lead to the bowing of the sample, exacerbating the problem [112]. An example of the effect of the run-away heating described is shown in figure 4.2, where it can be seen that part of the sample has completely de-bonded from the carrier.

Furthermore, the imprecise method of using the pipette dropper to apply the oil resulted in a variation in the volume applied from run to run. As the thermal conductivity of Santovac is $\sim 1000\times$ lower than that of Si, a consistently thin layer between the wafers is required for adequate heat transfer. The bonding process was therefore standardised as follows: the Santovac was heated to $95°C$ and 75μl of the liquid was measured using a pipette and placed onto the carrier. The sample was then placed on top of the carrier and both were placed on a hotplate and heated to $80°C$ for 2 minutes, allowing the Santovac to spread. This slight change in practice was found to make the etch much more predictable in terms of etch rate, and eliminated the occurrences of run-away over-etching.

After bonding the substrate to a Si carrier wafer, the TSVs were etched using one of two tools: an Oxford Instruments Estrelas etcher or an SPTS Rapier DRIE tool. Between these two tools, three Bosch etches with different etch parameters were tested and the resulting qualitative and quantitative differences in the TSVs produced were compared. An example of the TSVs produced by a Bosch etch can be seen in figure 4.3. After the etch, the sample was exposed to an O_2 plasma to remove the remaining C_4F_8 passivation layer on the TSV sidewalls and photoresist. The SiO_2 etch-stop layer was then removed using a 20min wet-etch in 6:1 BHF solution, which had the additional benefit of removing any native Si oxides present on the sample [113]. The nitride layers were then deposited on the top and bottom surfaces of the sample, which will be discussed in section 4.1.3. An investigation into the details of the Bosch etches used and, in particular, their affect on the sidewall roughness of the TSVs will be carried out in the next section.

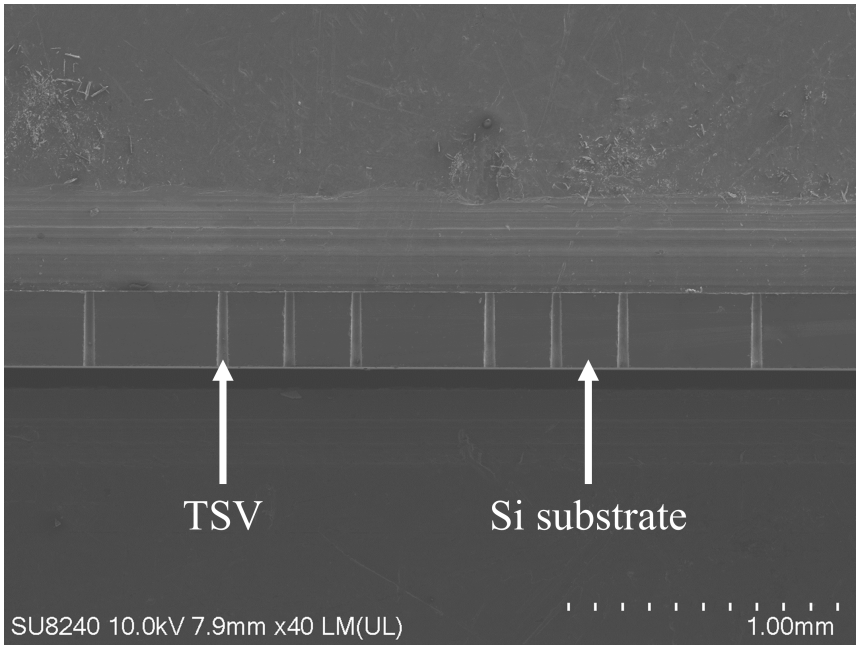


Figure 4.3: SEM image of the cross-section of a Si substrate with multiple etched TSVs.

Analysis of TSV Sidewall Roughness

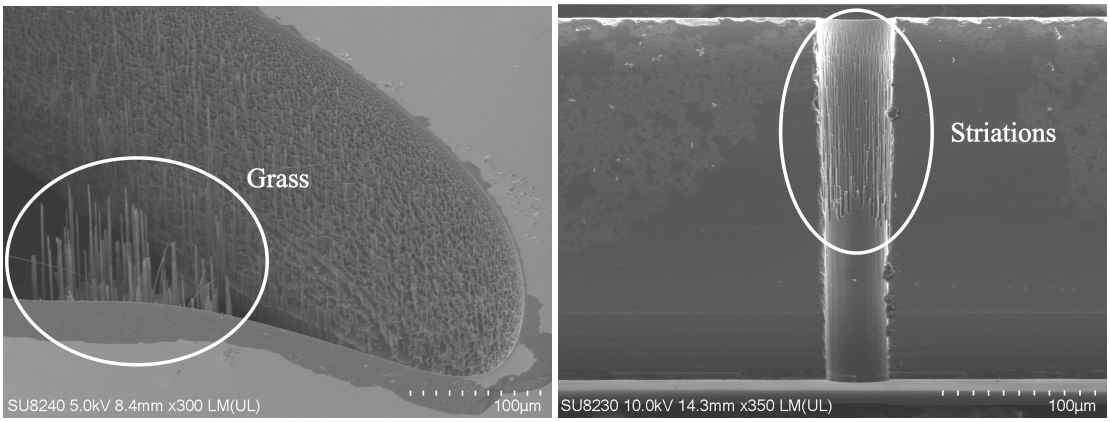
Three commonly referenced indicators of quality in a Bosch etch are sidewalls 90° to the substrate surface, smooth sidewalls and a lack of notching at the bottom of the TSV. 90° sidewalls are sought after as the two openings of the TSVs are necessarily of the same size and, therefore, take up the same amount of lateral space on either side of the chip, reducing the TSV's footprint as far as possible. Eliminating notching similarly reduces this footprint and also helps to prevent incomplete coverage of any metallisation subsequent to the Bosch etch. Reproducibility of results is fundamental to the success of any nanofabrication process and the three properties listed here all contribute to more repeatable processes.

Table 4.1: Selected key process parameters for etches 1, 2 and 3. Etch steps D, B and E are the deposition, breakthrough and etch steps, respectively. D1, D2, B1 and B2 are used to indicate where there was more than one deposition or breakthrough step per cycle. Values given for etch 1 are the parameter value at each of the four stages of the etch. Values given for etches 2 and 3 are parameter value at the start and end of the linear ramp. These recipes were developed by James Watt Nanofabrication Centre staff.

Etch step	Etch number	1				2		3	
	Etch tool	Estrelas				Rapier		Rapier	
	Stage/Ramp	1	2	3	4	Start	End	Start	End
D1	ICP Power (W)	1500				2500		2500	
B1	ICP Power (W)	1800				2500		2500	
B2	ICP Power (W)	-				-		2500	
E1	ICP Power (W)	1800				2500		2500	
D2	ICP Power (W)	-				-		2500	
D1	Pressure (mTorr)	50				40		40	
B1	Pressure (mTorr)	30.0				15.0	26.0	7.5	13.0
B2	Pressure (mTorr)	-				-		15	26
E1	Pressure (mTorr)	35				35		35	
D2	Pressure (mTorr)	-				-		55	
D1	SF_6 flow rate (sccm)	10				1		1	
B1	SF_6 flow rate (sccm)	200				250		288	333
B2	SF_6 flow rate (sccm)	-				-		300	
E1	SF_6 flow rate (sccm)	200				400		400	
D2	SF_6 flow rate (sccm)	-				-		1	
D1	C_4F_8 flow rate (sccm)	200				300		300	
B1	C_4F_8 flow rate (sccm)	10				1		1	
B2	C_4F_8 flow rate (sccm)	-				-		-	
E1	C_4F_8 flow rate (sccm)	10				1		1	
D2	C_4F_8 flow rate (sccm)	-				-		350	
D1	Time (s)	1.75	1.85	1.95	2.05	1.00		0.50	
B1	Time (s)	1.00	1.10	1.20	1.30	1.00	1.10	0.50	
B2	Time (s)	-				-		0.90	1.10
E1	Time (s)	2.50				2.00	2.20	1.90	2.10
D2	Time (s)	-				-		0.50	
Cycle	Time (s)	5.25	5.45	5.85	5.85	4.00	4.30	4.30	4.70

In this section, three different Bosch etches on two different dry etch tools are compared to determine the effect that changing both process variables and the number of etch cycles in a particular etch had on the sidewall roughness of the TSV produced. Etch 1 was performed on an Oxford Instruments Estrelas and etches 2 and 3 were performed on an SPTS Rapier. Differences in the process chamber, loading process and other environmental conditions will have arisen from performing these etches on different tools and these could have had some effect on the etch results. These effects are, however, difficult to assess when more dominant etch parameters have been changed simultaneously - as is the case here - and they will, therefore, be neglected.

Due to the etch rate of any Bosch etch being aspect-ratio dependent, it is useful to vary the etch parameters as the etch progresses and the aspect-ratio of the TSV increases. The etches performed on the Estrelas and Rapier tools are structured slightly differently in this respect. Recipe 1, performed on the Estrelas, is divided into four stages, each with a slightly modified set of parameters that repeat for an operator-specified number of etch cycles. In contrast, the parameters for recipes 2 and 3 performed on the Rapier are linearly ramped over a number of cycles from a starting to an ending value. A further structural difference between the etches is that, while etches 1 and 2 follow a standard Bosch structure of a deposition, breakthrough and etch step (D1, B1, E1), etch 3 splits the deposition and breakthrough steps into two (D1, B1, B2, E1, D2), where certain parameters are modified from step to step. This was to allow for better pressure control and synchronisation of various parameters. Aside from these overarching structural differences, there are also differences in the parameter values used for each etch. A table of selected parameters from the three etches is given in table 4.1. The plasma power, pressure, gas flow rates and step times have been listed as these parameters have been shown to dominate the properties of the resulting etch [114].



(a) **(b)**

Figure 4.4: (a) Example of grass formation emanating from the bottom of an over-etched portion of a Si sample. (b) Example of roughened band striations formed at the top of a TSV.

At this point, it is useful to more precisely define certain terms that will be used in the description of the TSV etch. There are multiple types of TSV surface roughness. The first of these is scalloping, the process of formation of which was described in section 2.4.3. *Striations* refer to long pillars that may run vertically along the TSV, constituting another form of roughness. These come in two types that are related but of slightly different origin. The first of these, *grass*, is a formation of narrow pillars that protrude upwards, often from the bottom surface of the TSV. This is generally formed by either the incomplete removal of the passivation layer prior to the etch step or the redeposition of etch byproducts. Thus, a micromasking effect is created which causes the grass to be etched into the TSV bottom [114]. As the passivation layer will tend to not be removed from the pillar sidewall in subsequent etch cycles, these pillars tend to perpetuate as

the Bosch etch progresses. The second type of striation is the so-called *roughened band*, which extends downwards from the top edge of the TSV. This is caused by the uneven erosion of the photoresist surrounding the TSV as the etch progresses, known as *pullback*, transferring to the Si substrate below. Examples of grass and roughened band striations are shown in figure 4.4.

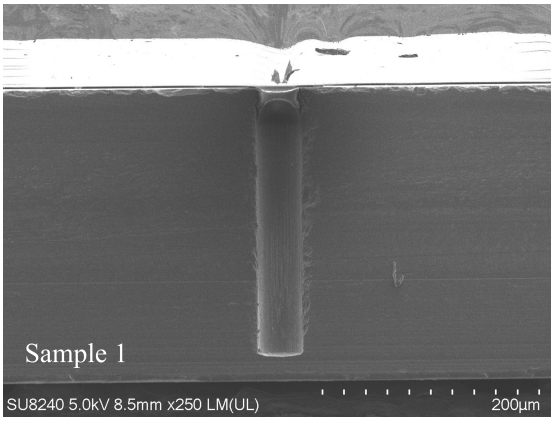
Table 4.2 lists the samples discussed in this section alongside the recipe used to etch them, the number of etch cycles they were exposed to and a qualitative assessment of the degree of striation and notch size observed in TSVs etched into each sample.

In figure 4.5, the results of etch 1 on samples 1-4 are shown, with each having undergone a different number of etch cycles. From the roughness apparent in the TSVs featured in figure 4.5 and noting the number of etch cycles used for samples 1-4, detailed in table 4.2, it can be observed that, as may be expected, the degree of striation tends to increase with the number of cycles and total etch time. The only parameters that were increased from stage to stage in etch 1 were the times allowed for the deposition and breakthrough steps. It is, therefore, likely that the increase in total etch time is the chief reason that the roughness increased.

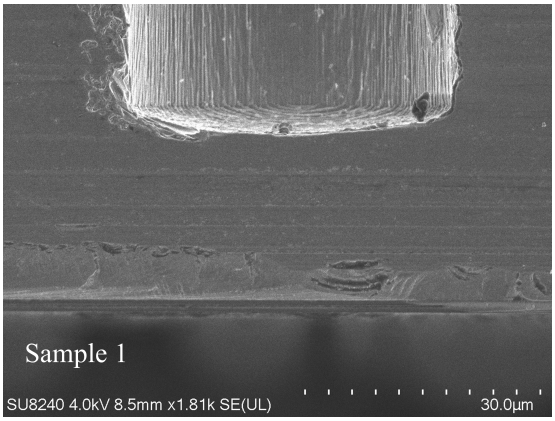
It is notable that samples 2 and 3 were etched for the same total number of cycles and the same time overall, but that the etch of sample 2 was split into an initial main etch and a top-up

Table 4.2: Etch performed on each sample and the resultant degree of striations observed. Numbers of etch cycles listed in square brackets indicate the number of cycles at each of the four parameter sets used in the Estrelas etch. Two sets of brackets indicate a main etch and a top-up etch were performed. Etches given as a number used ramped parameters and an addition sign indicates that a top-up etch was used, where the second set of cycles also started from the beginning of the parameter ramp. (EP) indicates that the etch parameters used for the full number of cycles to which it is adjacent were the end parameters of the ramp.

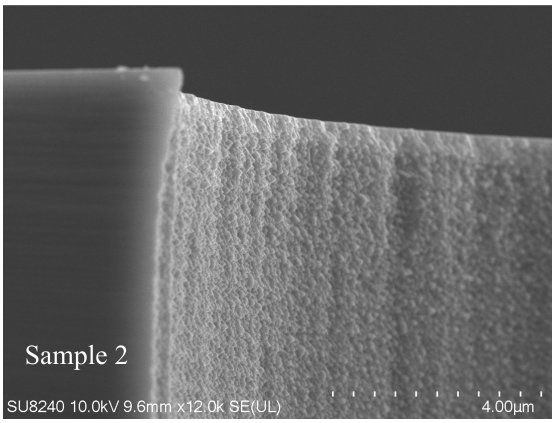
Sample number	Etch tool	Etch recipe number	Number of etch cycles	Total etch time (s)	Degree of striation	Notch size
1	Estrelas	1	[167,167,168,169] + [1,1,1,147]	4634.85	Very small	N/A
2	Estrelas	1	[205,205,205,205] + [1,1,1,97]	5176.00	Small	N/A
3	Estrelas	1	[206,206,206,302]	5176.00	Medium	Medium
4	Estrelas	1	[252,252,252,369]	6329.25	Large	Large
5	Rapier	2	857 + 100	3971.55	Large	None
6	Rapier	2	957	3971.55	Small	Small
7	Rapier	3	640 + 200 (EP)	3820.00	Large	None
8	Rapier	3	840	3780.00	Large	None


Sample 1
SU8240 5.0kV 8.5mm x250 LM(UL)
200µm

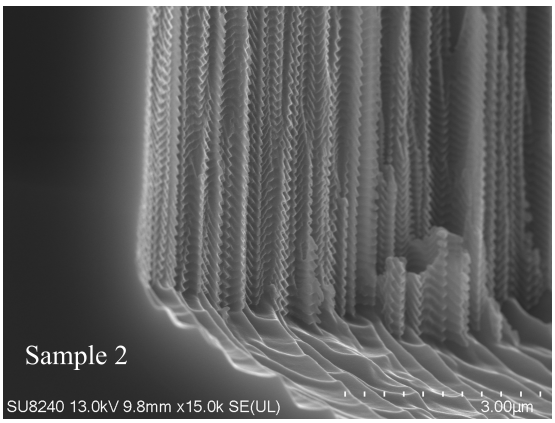
(a)


Sample 1
SU8240 4.0kV 8.5mm x1.81k SE(UL)
30.0µm

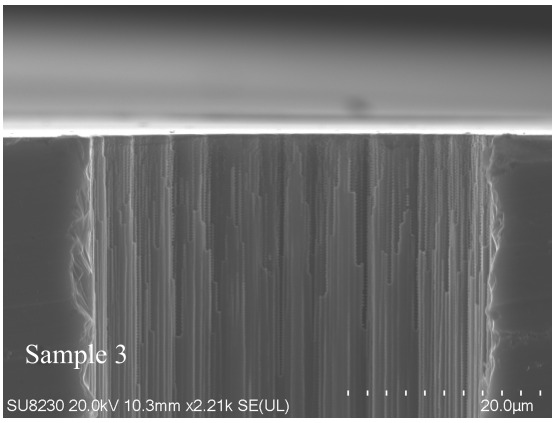
(b)


Sample 2
SU8240 10.0kV 9.6mm x12.0k SE(UL)
4.00µm

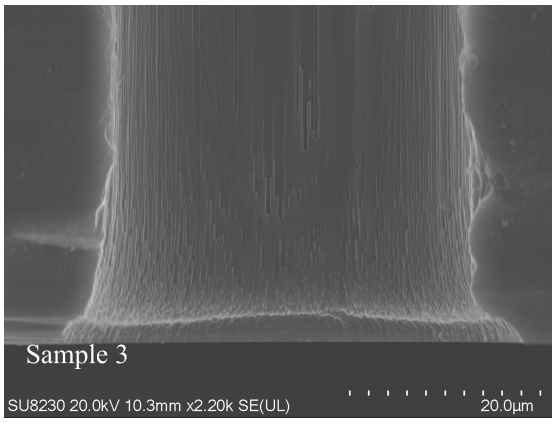
(c)


Sample 2
SU8240 13.0kV 9.8mm x15.0k SE(UL)
3.00µm

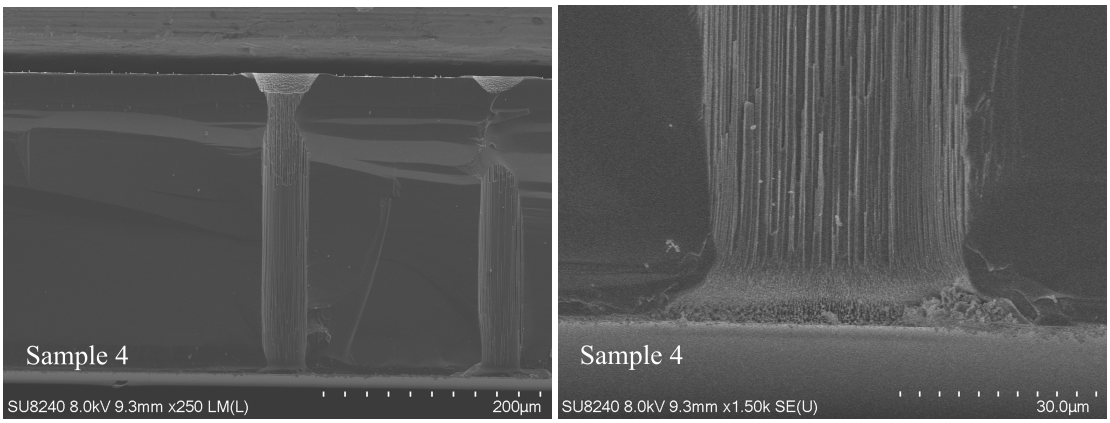
(d)


Sample 3
SU8230 20.0kV 10.3mm x2.21k SE(UL)
20.0µm

(e)


Sample 3
SU8230 20.0kV 10.3mm x2.20k SE(UL)
20.0µm

(f)



(g) **(h)**

Figure 4.5: Cross-sectional SEMs of TSVs etched using etch 1. (a) Full view of TSV etched into sample 1. (b) Bottom of a TSV etched into sample 1. (c) Top edge of TSV etched into sample 2. (d) Bottom of a TSV etched into sample 2. (e) Top edge of TSV etched into sample 3. (f) Bottom of TSV etched into sample 3. (g) Full view of TSV etched into sample 4. (Note that the apparent constriction near the top of the TSV is likely due to the sample not being cleaved precisely through the centre of the TSV.) (h) Bottom of TSV etched into sample 4.

etch. This was done as the number of cycles necessary for the etch to reach the bottom of the substrate was unknown a priori. There were four days between the initial and top-up etches of sample 2, which could have allowed time for contamination of the sample or degradation of the photoresist mask. However, it appears as though this interval between etches did not have a detrimental effect on the roughness of the sidewall of sample 2, with significantly fewer striations present at the top of the imaged TSV. Comparing the bottom end of the TSVs in samples 2 and 3, it is apparent that the etch of sample 2 did not etch through the substrate entirely. This was confirmed by optical profilometer measurements, which measured a depth of 268μm into a 275μm thick substrate. In contrast, not only did the etch of sample 3 reach the bottom of the substrate, but it was also long enough for a sizeable notch to form at the foot of the TSV. This indicates that continuously etching the sample lead to an increased overall etch-rate. One possible cause of this is the heating of the sample during the etch, which would have been preserved during the continuous etch, thereby increasing the overall etch rate. The degree of striations in the lower region of TSVs in both samples is similar, though scallops are clearly much more defined in sample 2.

Moving now to a discussion of etch 2, samples 5 and 6 were, in a similar manner to samples 2 and 3, etched for the same number of cycles and total time, but the etch of sample 5 was split into a main etch and a top-up etch. From figure 4.6, it is apparent that sample 5 suffered far worse striations than sample 6. The lithography process for both samples was the same and resulted in photoresist films that were determined to be very similar when inspected optically. There was a 14 day interval between the two etches of sample 5 which could have had a detrimental effect on

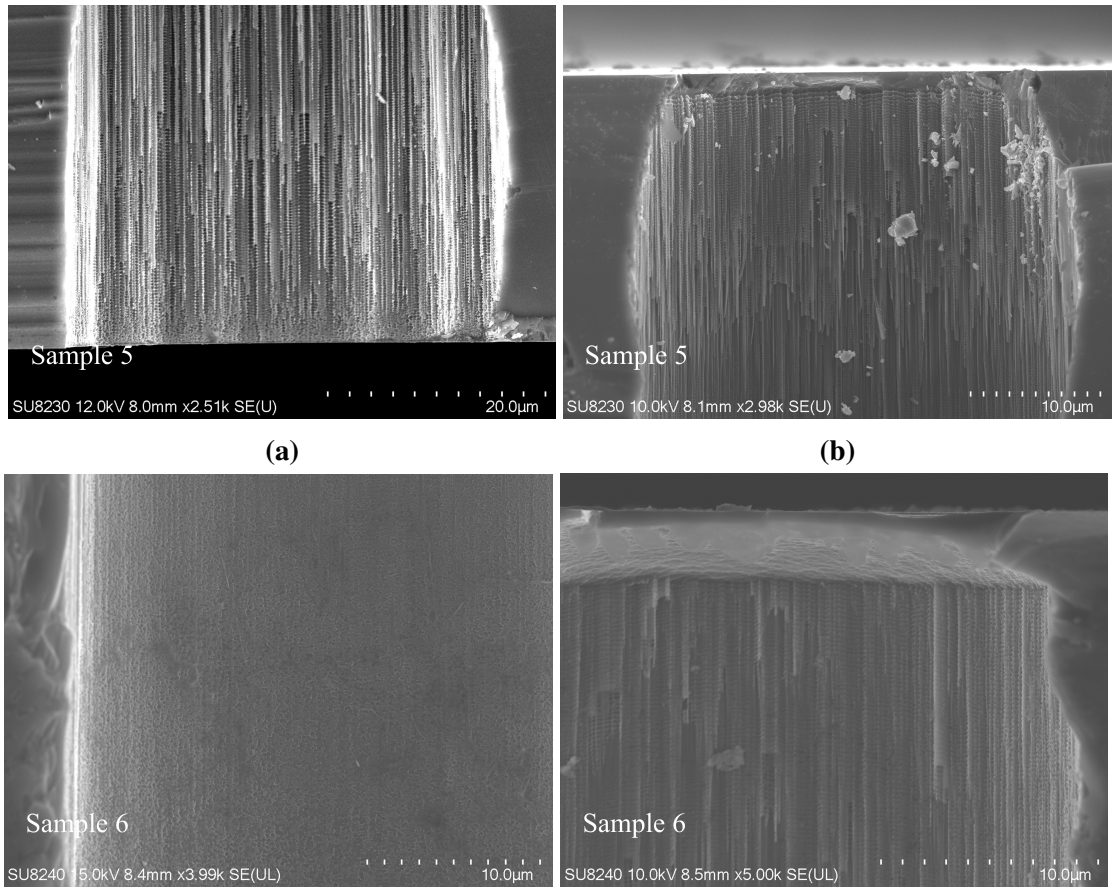


Figure 4.6: Comparison of striations present in samples etched using etch recipe 2. (a) SEM image of the top edge of a TSV from sample 5. (b) SEM image of the bottom of a TSV from sample 5. (c) SEM image of the top edge of a TSV from sample 6. (d) SEM image of the bottom of a TSV from sample 6.

the final quality of the etch. The total etch depth achieved for the TSVs on the two samples was very similar, with TSVs on both samples being measured as 277μm deep. Comparing figures 4.6 (b) and (d), it appears that there is a small (1-2μm) layer of Si that has not been removed from the bottom of sample 6, whereas the TSV from sample 5 has been etched to the full depth of the substrate. It is possible, though, that this layer did in fact remain on sample 5 as well and that it was destroyed during the process of dicing the sample prior to imaging. The fact that the scallops on the sidewall of sample 5 appear to stop a short distance from the sample surface supports this idea.

As an aside, it should be mentioned that the etch variables in the case of sample 5 were ramped linearly from their start to end points for both the main and top-up etches. This implies that the values of a given variable used during the etch of sample 5 were a combined set of 857 values equally spaced between the start and end points (inclusive) of the ramp and 100 values

equally spaced between the start and end points of the ramp. This set of values may not have been identical to the set of 957 equally spaced points between the starting and ending values of the ramp used during the etch of sample 6. This is unlikely to have had a significant effect due to the differences between the pairs of values being so slight, but is noted for completeness.

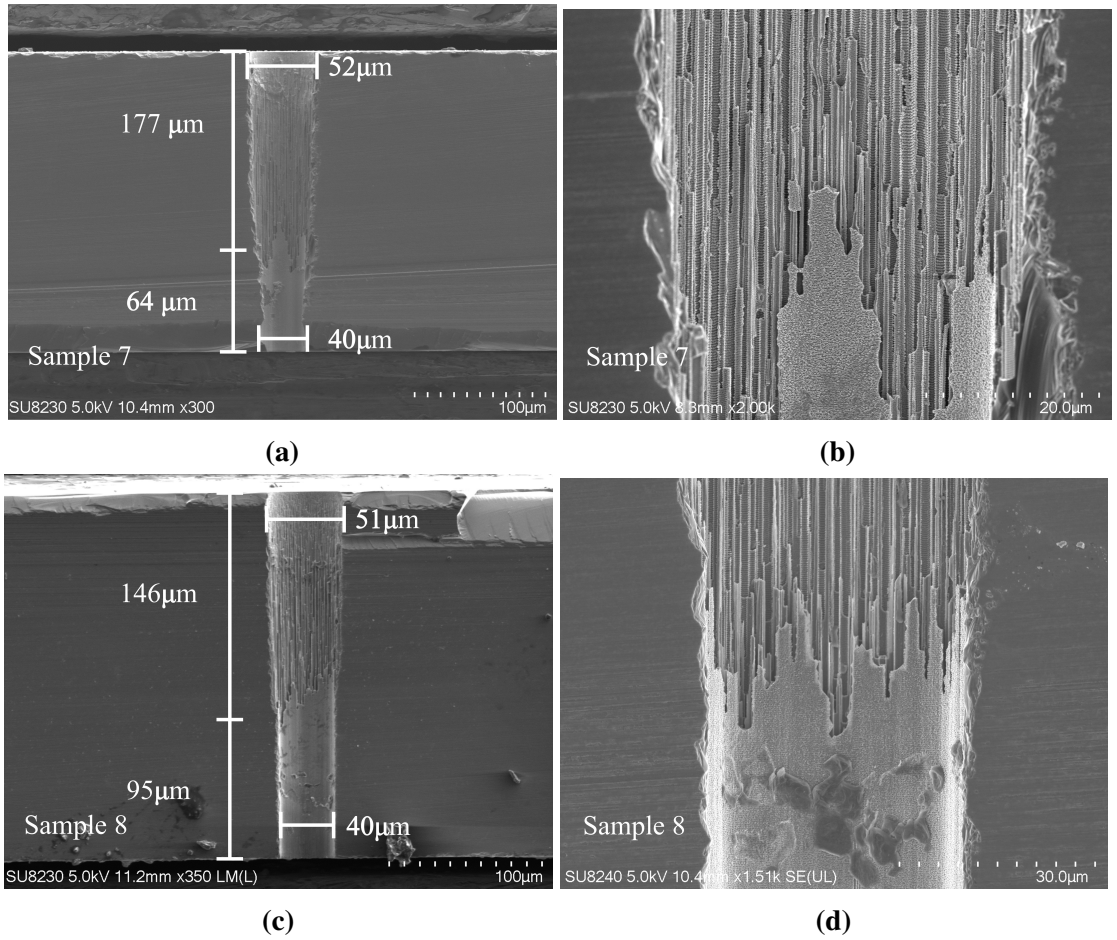


Figure 4.7: Comparison of striations present in samples etched using etch recipe 3. (a) SEM image of a TSV from sample 7. (b) SEM image of the roughened band boundary from a TSV from sample 7. (c) SEM image of a TSV from sample 8. (d) SEM image of the roughened band boundary from a TSV from sample 8.

The etch processes for samples 7 and 8 were similar to those of 5 and 6 in that they consisted of the same number of etch cycles, but that the etch used on sample 7 was split into 2 parts. The difference here is that the parameters of the second etch performed on sample 7 were not ramped from the starting to the ending values, but were instead fixed at the ending parameters. This had the effect of deepening the roughened band of sample 7 relative to sample 8, as shown in figure 4.7. The severity of the striations in each sample was, however, approximately the same. There was also an almost identical increase in width of the top opening of the TSVs of both samples

relative to the lithographically defined 40μm diameter. Neither sample, though, exhibited any notch formation at the bottom of the etched TSVs. This could be due to the fact that the number of etch cycles was well timed to stop as the etch reached the full depth of the substrate.

A comparison will now be made between the two etches that were performed on the Rapier system, namely etches 2 and 3. It would clearly have been preferable to change only one parameter at a time in order to isolate the effects that a change in that parameter would have had on the resulting etch. Unfortunately, the switch from etch 1 to etch 2 was made due to a fault with the Estrelas etching tool that required it to undergo lengthy repairs. The move from etch 2 to etch 3 was made due to the Rapier tool experiencing high levels of power reflected to the LF generator and the recipe was, therefore, altered to reduce the risk of damage to the tool. This confluence of parameter changes makes it difficult to draw specific conclusions about which of them may have brought about a given change in the outcome of the etch or which was more significant in the formation of the final TSVs. Nevertheless, it is possible, through comparison with the literature, to suggest what the origin of various TSV features may have been.

From the previous set of comparisons, it is apparent that the use of a top-up etch has the potential to affect on the outcome of the etch overall. Therefore, it is most appropriate to use samples 6 and 8 when comparing etches 2 and 3. Although there is an approximately 13% increase in the number of cycles between the two etches, the total etch time varies by much less - about 5%. Very similar 40μm diameter TSV depths of 278μm and 275μm were achieved for etches 2 and 3, respectively. As the Si wafers used as substrates were nominally 275μm thick, this was taken as evidence that the TSVs had etched through the full thickness of the substrate. From figure 4.6 (d), however, it is clear that this was not the case. The propensity for the etch 2 to produce notches cannot, therefore, be determined from this sample. It is worth noting that 20μm diameter TSVs were also present on the samples. These were also measured with the optical profilometer and the resulting measurements suggested that etch 2 had a very similar and, if anything, slightly higher etch rate than etch 3, with depths of 202μm and 196μm being reached, respectively. This is in contrast to the observations from the 40μm diameter TSVs. Of course, there is a possibility that the wafers were of different thicknesses. They were, however, obtained from the same supplier and taken from the same batch, making this unlikely.

Comparing the roughness induced by the two etches, it is clear that etch 2 produced much smoother surfaces than etch 3 overall. Curiously, the bottom section of the TSVs from both samples were similarly smooth, yet the roughness of the top section of the TSVs from sample 8 was very high, compared to the relatively smooth upper surface of the sample 6 TSVs.

To interrogate the origin of these differences, the process parameters shall be discussed, beginning with the chamber pressure. The depth of the roughened band has been shown to decrease with increasing pressure due to a decrease in the average ion angle of incidence [115]. However, this is caused by the pressure during the etch step specifically, which was identical for

etches 2 and 3. Increasing process pressure also decreases the rate at which etch by-products are removed from the reaction chamber and thus increases the likelihood that these by-products adsorb to the TSV sidewall or bottom. This adsorption can prevent the subsequent breakthrough step from completely removing the barrier layer and thus encourages sidewall damage or the formation of grass [114,115]. As the concentration of SiF_x by-products in the chamber is higher during the deposition step than the breakthrough step and thus redeposition is more probable, the fact that the pressure in the deposition step was increased in etch 3 as compared to etch 2 is more significant to the formation of grass than the decrease in pressure in etch 3's breakthrough step. Therefore, this increase in pressure during the deposition step of etch 3 was likely a contributing factor to the increase in sidewall roughness observed.

The increase in flow rates of both SF_6 and C_4F_8 from etch 2 to etch 3 would have acted as a partial counterbalance to this effect, as this would have increased the rate of removal of the byproducts of the etch. High SF_6 flow rates have, however, been associated with grass formation [114]. Moreover, an increase in the C_4F_8 flow rate promotes the deposition of the passivation layer, possibly preventing the proper removal of the fluorocarbon layer.

The length of the etch step in etch 3 was shorter than that of etch 2. This, along with the difference in the number of cycles each sample was exposed to, resulted in a cumulative etching time of 2010s for sample 6 and 1680s for sample 8. Conversely, the total breakthrough times were 1005s and 1260s for samples 6 and 8, respectively. This gave very similar total material removal times of 3015s and 2940s. The total length of time that the Si is exposed to the etching plasma is known to increase the depth of the roughened band and so, considering this factor in isolation, one would expect the roughened bands of both samples to be similar [114]. However, the increase in the ratio of the breakthrough and etching times to the deposition time has been reported to cause an increase in the rate of removal of the photoresist mask from the surface of the substrate as the protective barrier layer is more rapidly removed [114]. This could have increased the photoresist pullback around the top edge of the TSV, promoting the formation of the roughened band in sample 8.

Taking all of these factors into consideration, it can be suggested that the greater pressure in the deposition step of etch 3 and its larger SF_6 flow rate created an environment in which there existed a large degree of micromasking of the exposed Si due to the redeposition of etch byproducts and also aggressive etching of the Si substrate, exacerbating and deepening the formation of grass and striations on the TSV sidewalls. Photoresist pullback and, therefore, roughened band formation was also likely more severe in etch 3 due to the larger ratio of the sum of breakthrough step time and etch step time to deposition time.

Moving now to a comparison of etches 1 and 2, figure 4.5 shows that the number of etch cycles performed on a sample has a large effect on the sidewall roughness of the etched TSVs, even in the absence of any other parameter changes. Care should, therefore, be taken when

comparing etch 1 and etch 2, given that the number or structure of etch cycles performed on samples 1-4 and samples 5 and 6 was changed and produced TSVs of varying sidewall roughness for etches of otherwise identical parameter choices.

With this in mind, it is perhaps most appropriate when assessing the etches to compare the etch results of sample 1 with those of sample 5, due to this pair being closest in total etch time. The etch rate of etch 1 is clearly less than that of etch 2, given the thicknesses of Si remaining at the bottom of each of the TSVs, where sample 1 has an approximately 20μm thick layer compared to sample 5's layer of 0-2μm, depending on whether it was removed by the dicing process, as previously discussed. What is certainly clear is that the TSVs of sample 1 had significantly smoother sidewalls than those of sample 5.

The slower etch rate of etch 1, while of course affected by all parameter choices, is most likely a consequence of the reduced ICP power for this etch and thus the reduced ionisation and dissociation of SF_6 molecules in the chamber [114, 116]. The reduced etch step time as a proportion of total cycle time is also a likely contributor to the reduced etch rate. Lower ICP power is generally associated with a decrease in overall surface roughness as seen in the results of these two etches [116]. The increase in SF_6 flow from etch 1 to 2 could also be a contributing factor to the increase in grass formation seen in figure 4.6 (a) [114]. Counteracting these effects is the decrease in process pressure of etch 2 compared with etch 1. As discussed in the comparison between etches 2 and 3, the decrease in pressure increases the rate at which etch byproducts are removed and therefore decreases the redeposition of those byproducts. This aught to be particularly true in the case of an increased gas flow rate, though it is clearly not as significant a factor in this case as the power applied during the etch. When considering the time differences between the two etches, it can be observed that the overall etch time for sample 1 was shorter than for sample 5 and correspondingly, the roughened band depth was reduced. This is in keeping with established behaviour of Bosch etches [114].

Overall, etch 1 produced TSVs of higher quality than etch 2. The primary factor that has driven this appears to be the reduced power of etch 1, with much smoother surfaces as a result. When considering parameters combinations for further testing, powers closer to the 1500-1800W range would be an obvious starting point. Increasing the gas flow rates of etch 1 and keeping all other parameter choices may be a way of increasing the etch rate of the etch, while retaining etch 1's superior results in terms of sidewall roughness.

4.1.3 Nitride Deposition

After the TSVs are etched, superconducting nitride layers are deposited on the top and bottom surfaces of the sample, simultaneously coating the sidewalls of the TSVs. In particular, both TiN and NbN were tested on separate samples. These are attractive materials for quantum circuits due to particular material properties that lead them to exhibit lower loss than other commonly

used superconductors. They are chemically stable against the formation of native oxides, the bulk and interfaces of which are known to have a propensity for containing a high number of two-level systems - a leading source of loss in quantum circuits [42, 117, 118]. These nitrides also have a higher superconducting gap energy than Al [119, 120]. This reduces the likelihood that quasiparticles will form in the superconductor - another leading loss mechanism in these systems [120]. A further reason that nitrides are appealing for TSV fabrication specifically is that they may be deposited by ALD, which provides the conformality to the steep TSV sidewalls that is required for the process discussed here in order to maintain galvanic contact and hence signal integrity through the TSVs.

Two ALD processes were utilised here - one for the deposition of TiN and one for the deposition of NbN. The TiN films were deposited using an Oxford Instruments FlexAl deposition tool at the University of Glasgow and the NbN films were deposited in a PlasmaPro ASP tool at the Oxford Instruments site in Yatton. The primary difference between the tools used for the two depositions was that the PlasmaPro ASP tool had substrate biasing functionality. This is another degree of freedom with which to tune the energy of the ions incident on the sample surface, resulting in more control over the material properties of the deposited film. Alongside an increase in deposition rate, substrate biasing has also been shown to reduce film resistivity, increase film density and increase the thickness uniformity of the film across the surface [121]. Sputtering was also tested as a method of TiN deposition for the TSVs. Its higher deposition rate and higher purity films due to the lack of contamination from e.g. ALD precursors are attractive properties that made this technique worthy of investigation. However, being a highly anisotropic deposition method, it was suspected that the resultant films would not be sufficiently conformal to the TSV sidewalls to maintain galvanic contact over the whole TSV.

The TiN ALD process began with a precursor dose step, during which 0.9mg of tetrakis-(dimethylamido)titanium (TDMAT) precursor was flowed for 1s and the chamber was held at a pressure of 40mTorr. In the following 30s plasma step, 15sccm of N_2 gas was introduced and the plasma was ionised at a power of 200W. The sample was heated to 250°C during the process. Due to the sub-monolayer deposition rate per cycle, the overall time for the deposition of the 62nm film was approximately 12 hours. This low deposition rate is the trade-off for the monolayer thickness control the technique offers. It should be noted, however, that one quarter of this time was spent pre-conditioning the chamber in order to reduce contamination of the sample, resulting in a deposition rate of 0.12nm/min. In the NbN deposition process, tris(diethylamido)(tert-butylimido)niobium(V) (TBTDEN) was used as a precursor and the sample was heated to 320°C. The substrate biasing in this process resulted in a significantly higher deposition rate of 0.67nm/min, with the 121nm film being deposited in 3 hours.

To begin, the sheet resistance (R_s) of two ALD films and one sputtered film were measured using a Jandel 4-pt probe station and their resistivities (ρ) were subsequently calculated using

equation 4.1:

$$\rho = R_s t = 4.532 \frac{V}{I} t, \tag{4.1}$$

where the coefficient 4.532 is a result of the geometry of the probes, and V, I and t are the measured voltage, current and film thickness, respectively. Each film was unpatterned and deposited on a Si substrate. IV measurements were performed on both the top and bottom films, as they were deposited in separate deposition runs, and the film thicknesses were measured using an ellipsometer. Dense, well-ordered films with minimal contamination are likely to exhibit both low resistivity and a higher T_c with a reduced likelihood of, for example, non-superconducting regions in the film. The calculated resistivities are listed in table 4.3.

Table 4.3: Comparison of resistivities of sputtered and ALD TiN and NbN films.

Material	Deposition Method	Film Thickness (nm)	ρ_{bottom} ($\mu\Omega$cm)	ρ_{top} ($\mu\Omega$cm)
TiN	Sputtered	47	3770	2950
TiN	ALD	62	380	430
NbN	ALD	96	240	220

The resistivities of the ALD films compare favourably with values published in the literature, which range from approximately 130-2000$\mu\Omega$cm for TiN and 170-3100$\mu\Omega$cm for NbN [103, 121–127]. However, there is clearly a large disparity between the resistivities of the sputtered and ALD TiN films. In general, sputtering tends to produce films of lower resistivities than ALD, with reported values falling between 23$\mu\Omega$cm and 780$\mu\Omega$cm, depending on deposition conditions [128–131]. However, in the films deposited here, the calculated resistivities are an order of magnitude larger than those of the ALD films.

There are a number of possible causes of this disparity. The resistivity of a material is influenced by its phase composition, temperature and defects in its structure [128, 130]. In the case of TiN, the N content of the film has a large impact on its resistivity. As the N concentration increases from 0% (pure Ti), the resistivity increases as N atoms occupy interstitial positions in the lattice, causing a decrease in grain size and lattice order. As the concentration is increased further and the BCC ε-TiN phase begins to dominate, the number of defects reduces and the resistivity decreases [128, 130, 131]. A higher N concentration may be achieved by a higher N partial pressure during the deposition [131].

Parameters used in the TiN sputtering process are compared with parameters from processes reported in the literature in table 4.4 with the proviso that the properties of the films resulting from each deposition process are influenced by a range of factors including, but not limited to, the deposition system geometry, achievable base pressure, sputter target condition, pre-treatment of substrates and control of contaminants. Therefore, the parameters listed may not be solely responsible for the resulting resistivities. It can be observed from the two samples reported by Ponon et al. that a larger N_2 partial pressure, and hence N_2 concentration in the film, decreases

Table 4.4: Comparison of the resistivities of selected sputtered TiN films. The highest and lowest resistivity value reported in each work is recorded. An omission of a value indicates that parameter was not recorded in the reference and a range or list of values indicates the values were present in the reference, but that they were not ascribed to a particular sample. Flow rates marked with * are given in terms of the ratio of gas flows, as opposed to values in sccm.

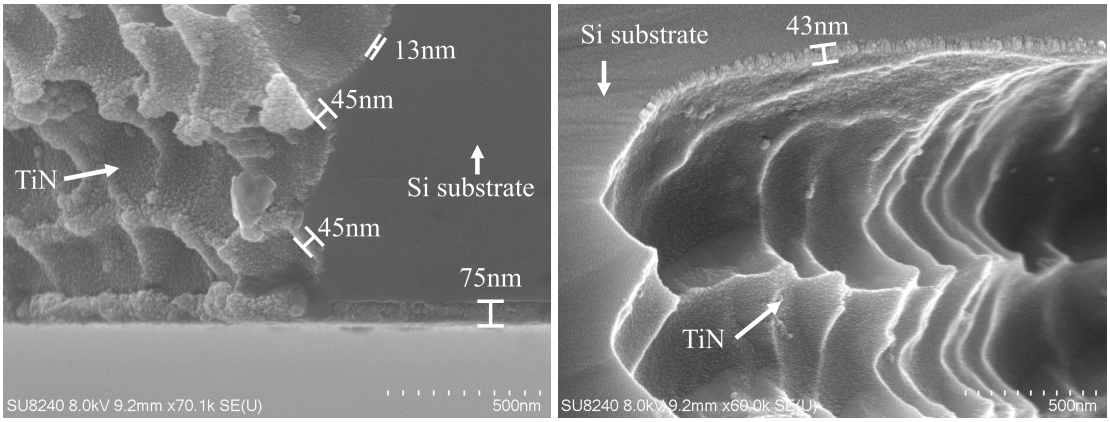
Authors (Year Published)	Method	Substrate	Ar:N_2 flow (sccm)	Process Pressure (mTorr)	Deposition Temperature (°C)	Process Power (W)	Film Thickness (nm)	ρ ($\mu\Omega$cm)
This work (2025)	R.F. sputtering	Si	20:5	2.9	25	275	60	2950
This work (2025)	R.F. sputtering	Si	20:5	2.9	25	275	62	3770
Vaz et al. (2005) [128]	D.C. sputtering	steel or Si	23:7.2	3.0	250	-	1700-4200	40
Vaz et al. (2005) [128]	D.C. sputtering	steel or Si	23:1	3.0	250	-	1700-4200	190
Yeh et al. (2008) [129]	D.C. sputtering	N-type Si	40:4	0.975	300	400	500-1000	23
Yeh et al. (2008) [129]	D.C. sputtering	N-type Si	40:4	4.875	300	400	500-1000	160
Ponon et al. (2015) [130]	D.C. sputtering	SiO_2 on Si	1:19*	3.75	250	800	170	80
Ponon et al. (2015) [130]	D.C. sputtering	SiO_2 on Si	4:1*	3.75	250	800	130	265
Kearney et al. (2018) [131]	R.F. sputtering	fused SiO_2	1:20*	3.0	600	-	58	70.2
Kearney et al. (2018) [131]	R.F. sputtering	fused SiO_2	1:20*	3.0	25	-	78.2	780

resistivity. However, it has been reported that deposition at higher temperatures has been shown to be the most critical parameter for achieving films with low resistivity [131]. This is clearly borne out here as the highest resistivity of samples reported in the selected references belonged to the only sample for which the deposition was performed at room temperature. While this sample, deposited at 25°C by Kearney et al., is still reported as having a lower resistivity that the samples produced in this work, it was metallised using an Ar:N_2 flow rate of 1:20 - a much larger proportion of N_2 than in the case of the samples deposited here. Therefore, the large resistivities of the samples deposited here can likely be largely accounted for by a combination of operating at too low a temperature and with insufficient N_2 partial pressure during deposition. In addition, it has been shown, by Yeh et al., that a decrease in the chamber pressure during the deposition results in films of lower resistivity. They attribute this effect to the increase in average ion energy, and thus the surface mobility, of the deposited atoms which results in denser films [129]. Increased film density is also noted as being beneficial in terms of resistivity by Kearney et al., which indicates that total pressure is another parameter that could be considered in future to achieve a lower resistivity.

While a small degree of film oxidation has been shown to have little impact on the resistivity of the film, it should still be limited as far as possible because as the degree of oxidation increases, it begins to significantly impact resistivity [130, 131]. Given that oxidation initially occurs at the surface of the film and the resistivity measurement was made by placing the probes in contact with the surface, it may be possible that the measurement was made through a layer of oxidised material and that the resistivity of the bulk is lower than the final measured value.

Though this is made less likely by the expectation that the tungsten probes would be able to penetrate the oxide layer, it may provide an explanation for the difference in the observed resistivities of the top and bottom-side films. The bottom-side film (higher ρ) was deposited a number of days prior to the deposition of the top-side film (lower ρ), after which their resistivities were both measured. Oxidation occurring in the intervening days could, therefore, be responsible for the difference in the measured values, despite the identical deposition conditions.

The conformality of the sputtering process was also shown to be insufficient for coating the entire TSV sidewall, as can be seen in figure 4.8. Sputtered films have previously been used to metallise TSVs, however the deposited films are often made very thick, or the vertical sidewall of the TSV is forgone in favour of a sidewall profile which is oblique enough to the direction of ion flux that a film may be grown [46].



(a) **(b)**

Figure 4.8: SEM images of the conformality of the sputtered TiN films. (a) The film at the edge of the TSV nearest the sputter target. (b) Film approximately 50μm deep into the TSV. The film can be seen to have only grown on surfaces that were facing towards the sputter target.

The conformality of the TiN and NbN films is shown in figure 4.9, with the top edges and cross-sections of the sidewalls of metallised samples presented. The thicknesses of the top and bottom NbN films were 121nm. However, from figure 4.9 (d), one can see that the thickness of the film on the TSV sidewalls was measured to be approximately 20% greater than this. This can be explained by the fact that the TSVs were etched all the way through the substrate prior to metallisation. Therefore, with the TSVs being open at both ends, their interior surfaces were exposed to both the deposition of the top surface film and the bottom surface film.

As can be seen from the ellipsometer measurement in figure 4.10 (a), the TiN ALD process provided excellent uniformity, with the film thickness only varying by a few nm across a 4" wafer, excluding the narrow region around the edge of the wafer. Figure 4.10 (b) shows an ellipsometer measurement of a witness sample which was placed into the ALD chamber alongside a TSV sample. This witness sample was a 2×2mm, 500μm thick Si chip with a 400nm PECVD SiO_2 layer deposited on the top surface. This SiO_2 layer enables a more accurate determination

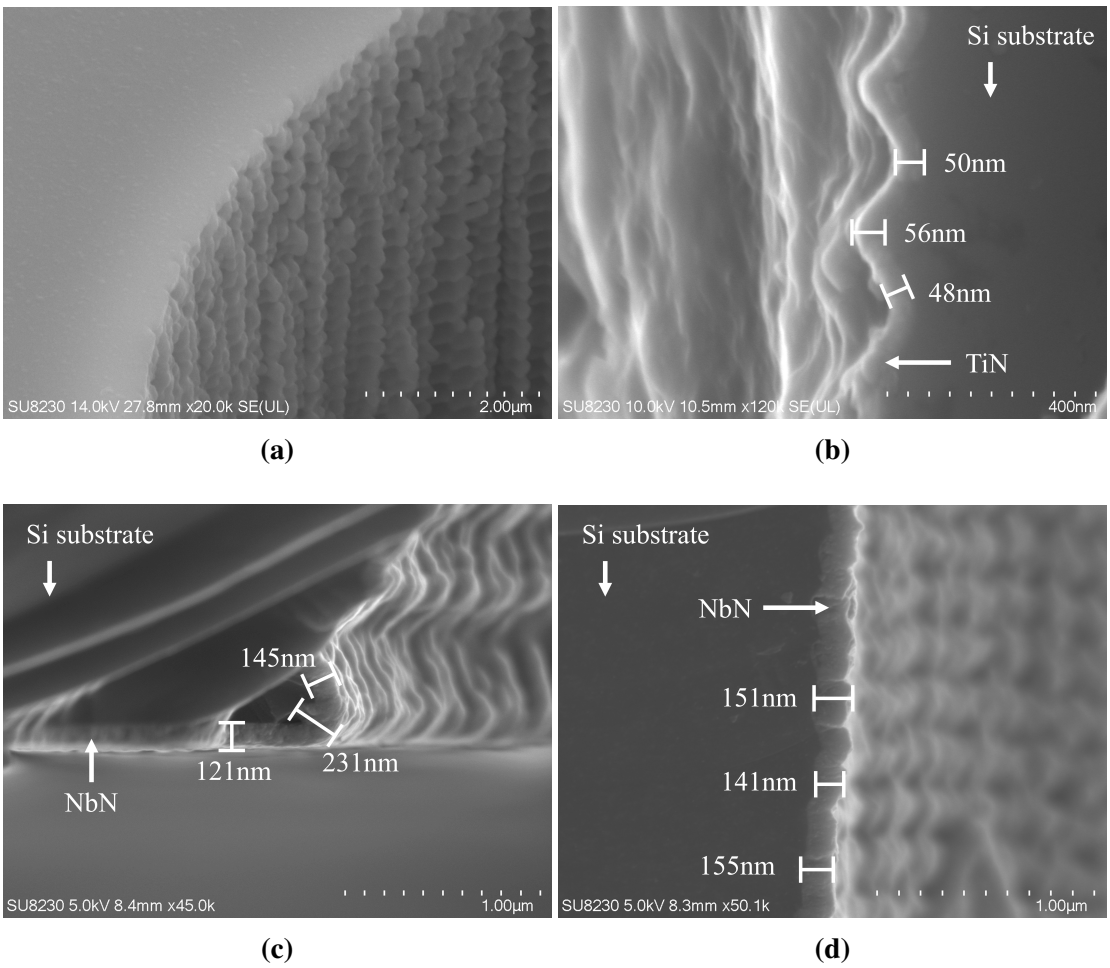
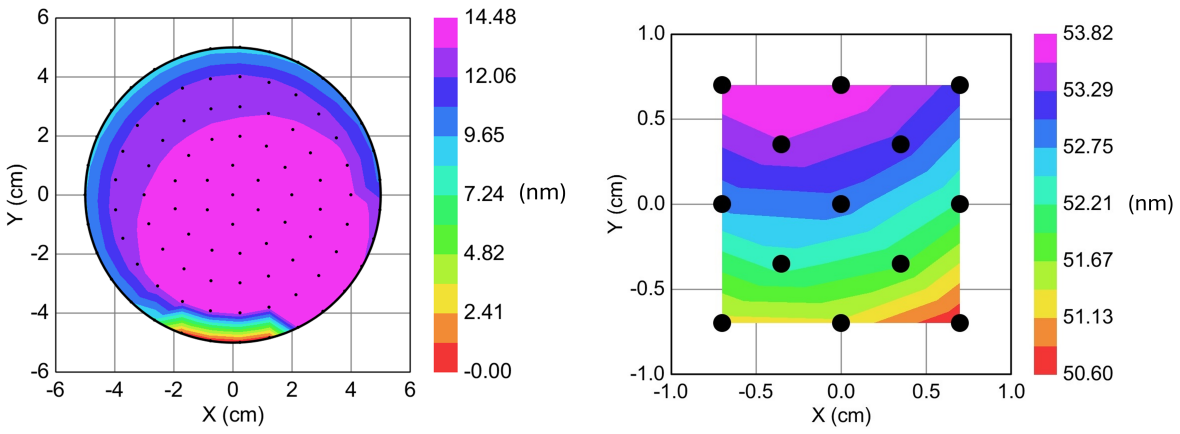


Figure 4.9: SEM images of a TSV demonstrating the conformality of the ALD method. (a) Top edge of TSVs metallised with TiN. (b) Cross-sectional image of TSV sidewall metallised with TiN. (c) Cross-sectional image of the bottom edge of a NbN TSV. (d) Cross-sectional image of TSV sidewall metallised with NbN.

of the thickness of the film as it serves to break the correlation between the optical properties of the metal film and its thickness by interference enhancement, enabling a unique solution to be obtained [132]. Again, only a small thickness variation of approximately 6% is observed. Uniformity measurements of the deposited NbN films, performed by operators at the Oxford Instruments lab, determined that the variation in film thickness was similar, at $< 6\%$ across a 6" test wafer.

4.1.4 Nitride Etch

The final step in the fabrication of the TSV samples was the dry-etch of the top and bottom sides of the wafer to define the planar circuitry. This was done in an Oxford Instruments Plasma lab 80+ using gas flows of 10sccm CF_4 etchant and 5sccm Ar. A chamber pressure of 30mTorr was maintained during the etch and an plasma power of 200W was applied. CF_4 is a commonly used etchant for TiN and NbN and this recipe in particular was found to be reliable in previously



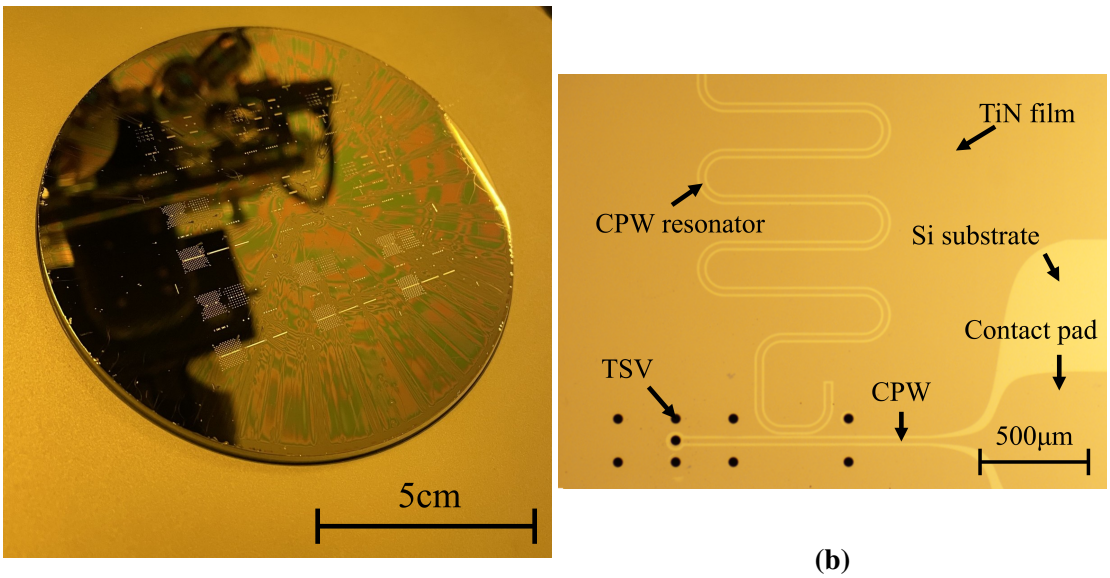
(a) **(b)**

Figure 4.10: (a) Ellipsometer measurement of TiN film uniformity on a 4" Si wafer. (b) Ellipsometer measurement of TiN thickness from a separate deposition on a 2×2cm Si witness sample, with a 400μm SiO_2 barrier layer between the film and substrate.

conducted experiments [133, 134].

The application of photoresist prior to the etch presented some difficulties. Usually, a wafer is held in place on the spinner by a vacuum chuck. In this process though, the TSVs had already been etched through the sample, perforating it, and the wafer was, therefore, unable to be held by vacuum.

Two methods were tested to overcome this. First, the wafer was be bonded to a carrier wafer which was then held in place by the vacuum chuck. This was done using Santovac 5(P) oil, as in the Bosch etch. This presented further issues, though, as the Santovac rose upwards through the TSVs and onto the top surface of the wafer, preventing uniform application of the resist and leading to unsatisfactory lithographic patterning on the samples. Moreover, as both sides of the wafer were etched sequentially, the side patterned first was placed face-down onto the carrier while the second side was being etched. The face-down side was, therefore, exposed to potential damage caused by contact with the carrier wafer surface. Initially, the barrier of the Santovac oil was thought to be sufficient to prevent this. However, it was noticed upon removing the sample from the carrier that the quality of the film had degraded. This could have been because of physical contact with the carrier in regions where Santovac was absent, or possibly due to the bowing of the wafer during the etch. This method was, therefore, discarded due to the litany of additional practical processing issues it introduced. A wafer chuck with four clamps around its circumference was found to provide a much more straightforward solution to the problem. However, care needed to be taken not to over-tighten the clamps as the wafers were very brittle and so could snap with minimal pressure. This chuck could not be installed on the automatic spinner and so the manual spinner was used for the second and third lithography steps of the



(a) (b)

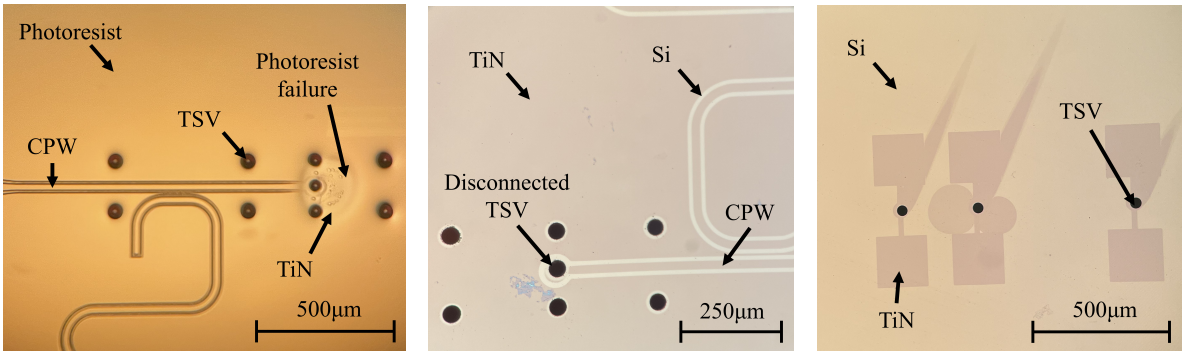
Figure 4.11: (a) Image of a Si substrate with etched TSVs and an S1818 photoresist layer prior to exposure . (b) Examples of structures etched into a TiN film.

fabrication process. An image of a Si wafer with photoresist applied after the Bosch etch step and a micrograph of structures successfully etched into a TiN sample is shown in figure 4.11.

A further issue that arose during this lithography step was the photoresist draining into the TSVs. The photoresist around the edge of the TSVs was, therefore, thinned and could not withstand the full etch duration. This, in turn, caused the conductive layer around the edge of the TSV to be etched away and thus galvanic contact between the connecting CPW and the TSV sidewall was lost. Using a viscous resist provided more protection for the metallisation layer as it was able to form a floating layer over the opening of the TSV (an example of this can be seen in figure 4.5 (a)). However, it was found that the more viscous the resist was, the less uniform its application over the non-planar sample surface became. Examples of the effects of these lithographic issues are shown in figure 4.12. It was found that spinning S1828 resist at 4000rpm, which resulted in a 2.8μm thick layer, was sufficiently viscous to prevent the disconnection between the TSV and CPW, while still being able to flow over the wafer surface.

4.1.5 Sidewall Smoothing

TSV sidewall roughness has been linked with a reduction in the performance of TSVs as interconnects [135]. These effects will be investigated in more detail in section 4.2.2, but for now it suffices to say that the achievement of a smooth TSV sidewall is beneficial to the operation of the device. In this section, two different methods of post-Bosch etch sidewall smoothing are explored.



(a) **(b)** **(c)**

Figure 4.12: Micrographs of examples of problems incurred as a result of poor lithography process. (a) Santovac contamination causing poor resist uniformity around TSVs. (b) TSV disconnected from transmission line due to poor resist coverage. (c) Result of non-uniform resist coverage post-etch. Streaks seen are due to TSVs creating thicker areas of resist coverage during spinning.

The first smoothing process consisted of thermally oxidising the Si substrate, followed by the removal of this oxide layer with a BHF solution. In the second process, the Si was directly etched by immersion in a KOH solution. The results of these processes are both compared to TSVs that have not been smoothed, but have otherwise been fabricated using the same processes.

The oxidation smoothing process was carried out by first oxidising the substrate in an atmosphere of steam at 800°C for 7.5 hours, resulting in a 1μm SiO_2 layer on all of the exposed surfaces of the sample, including the interior of the TSVs. When the scallops on the TSV sidewalls are oxidised, the depth of Si consumed is larger at the peak of the scallop than at the trough. Therefore, a smoothing effect is produced when the sample is immersed in BHF solution and the oxide layer is removed [136].

For the second smoothing process, the sample was immersed in a 40% potassium hydroxide (KOH) solution at 50°C for 15 minutes. These samples were then cleaned of residual K particles by a dilute HCl solution. The smoothing effect produced is due to the preferential etching of the [100] and [110] planes of the Si crystal. Therefore, if one defines the TSVs such that the [111] planes of the Si are perpendicular to the wafer surface, one can in theory obtain perfectly smooth TSV sidewalls [60]. This technique has been named the "Michelangelo etch" for the renaissance artist Michelangelo Buonarroti, whose famous line:

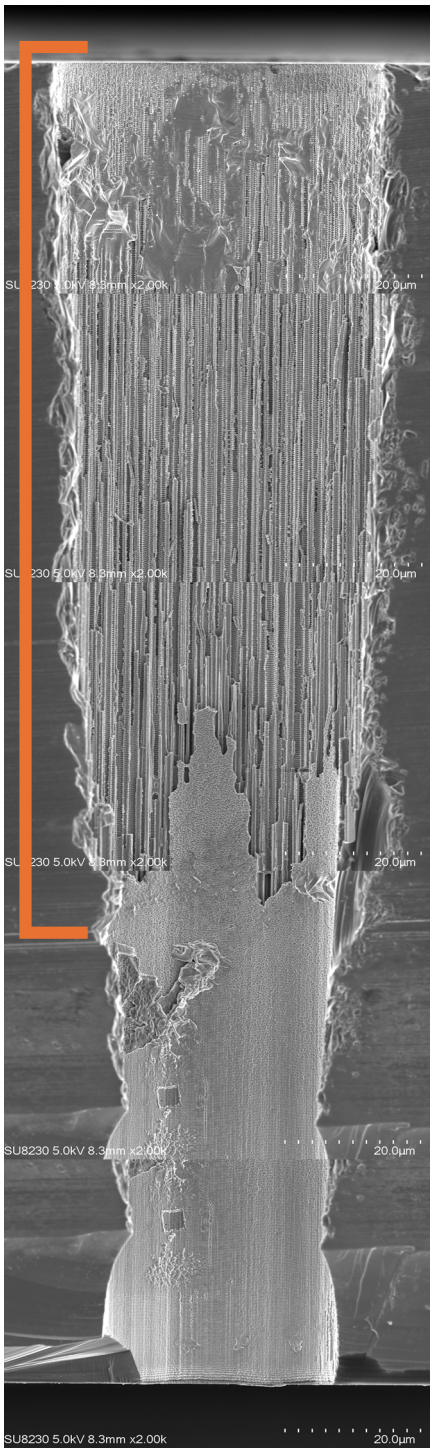
> The sculpture is already complete within the marble block, before I start my work.
> It is already there, I just have to chisel away the superfluous material.

is evidently as applicable to silicon as it is to marble.

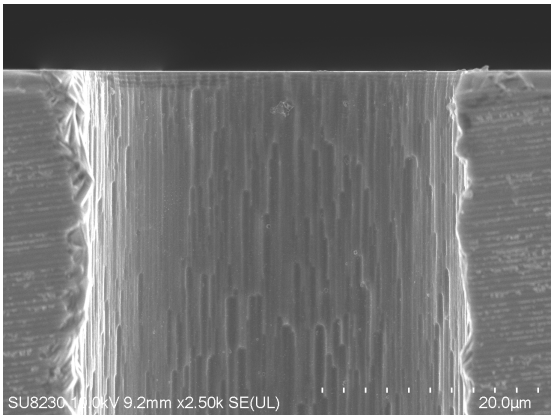
Both methods of sidewall smoothing were highly effective. It is clear from figure 4.13 (a) that there was significant lateral over-etching during the initial Bosch etch of the TSV. A

roughened band formed by large striations in the sidewall developed more than halfway down the TSV, widening the diameter of the TSV near the top surface from 40μm to approximately 50μm. This was likely caused by photoresist pullback, as discussed in section 4.1.2. However, it can be seen from figures 4.13 (b) and (c) that both smoothing methods significantly reduced this roughness.

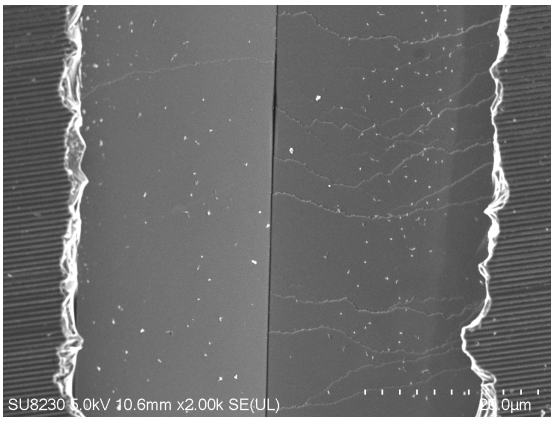
Remnants of the striations from the roughened band left after the oxidation smoothing process can be seen in figure 4.13 (b). Though these remnants do constitute roughening of the TSV interior, the difference between these and the extreme roughness of the unsmoothed TSVs is clear. Moreover, the oxidation and oxide removal process can be repeated as many times as necessary to further reduce this residual roughness. Increasing the depth of the oxide grown on the sample would have a similar effect. The KOH smoothing process by comparison creates even smoother sidewalls. Again, hints at the rough profile of the sidewall prior to smoothing are present in the form of "cliffs" running down the sidewall, which can be seen in figure 4.13 (c). This process does have a number of drawbacks when compared to the oxidation process. First, the wafer itself must be of [110] orientation. This may be prohibitive to certain processes due to a reduction in SiO_2 quality [60]. Second, it produces TSVs of rhomboidal cross-section due to the orientation of the [111] planes which, while not necessarily a hindrance, does limit design flexibility when employing the technique. Finally, given that the KOH solution etches the [100] and [110] planes of the Si much more rapidly, only the vertical [111] planes remain smooth after the etch. The top and bottom surfaces of the sample are therefore roughened by the etch and measures are needed to prevent or rectify this. One such solution could be the use of an SiO_2 hard mask for the Bosch and subsequent KOH etch. Another could be to polish the affected surfaces after the smoothing process. It is notable that SiO_2 hard masks have also been shown to reduce the depth of the roughened band caused by the Bosch etch [114].



(a)



(b)



(c)

Figure 4.13: (a) Composite SEM image of an unsmoothed TSV with the roughened band highlighted in orange. Comparison of the effects of the oxidation (b) and KOH (c) smoothing methods.

4.2 Measurement

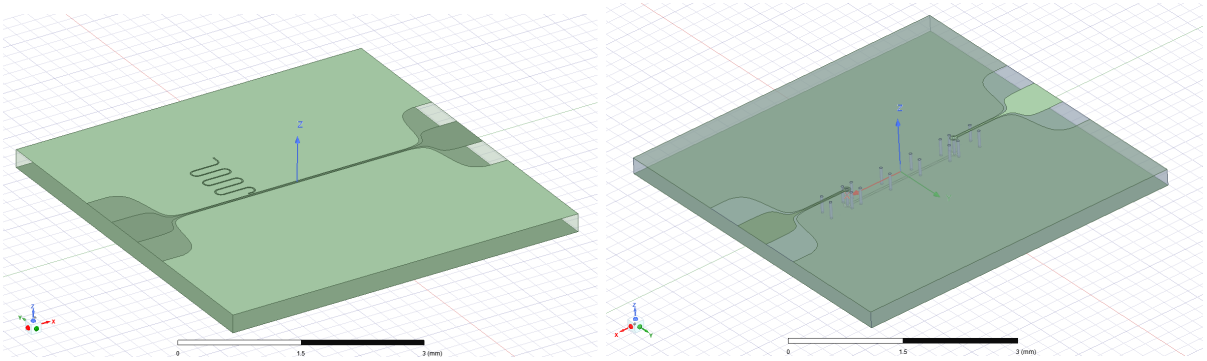
This section will discuss the room temperature and cryogenic measurement of the samples fabricated by the methods previously described. The impact of the inclusion of TSVs in a superconducting CPW will be assessed, as will the material choice for metallisation of TSVs. Finally, a calibrated S-parameter measurement of TSVs will be presented. A short summary of the various measured samples is given in table 4.5.

Table 4.5: Summary of the samples measured in the following section. All samples were 5x5mm chips fabricated on high resistivity Si substrates. Wafer number is used to indicate samples that were fabricated on the same substrate and subsequently diced for measurement. CBKR refers to cross-bridge Kelvin resistor structures, which are discussed in section 4.2.2.

Sample number	Design	Material	Deposition method	Wafer number	Section(s)	Measurement(s) performed
1	Planar CPW with CPW resonator	Nb	Sputtered	1	4.2.1	Cryogenic S-parameter
2	Two TSV transition CPW with flanking TSVs	TiN	PEALD	2	4.2.1, 4.2.2	Cryogenic S-Parameter
3	CBKR	TiN	Sputtered	4	4.2.2	Single TSV resistance
4	CBKR	TiN	PEALD	2	4.2.2	Single TSV resistance
5	CBKR	NbN	Substrate-biased PEALD	3	4.2.2	Single TSV resistance
6	Two TSV transition CPW	NbN	Substrate-biased PEALD	3	4.2.2	Cryogenic S-Parameter and temperature sweep
7	Two TSV transition CPW with flanking TSVs and TSV-interrupted CPW resonators	TiN	PEALD	2	4.2.3	Cryogenic calibrated S-parameter
8	Six TSV transition CPW	TiN	PEALD	2	4.2.3	Cryogenic calibrated S-parameter

4.2.1 Impact of TSVs on the Transmission of a CPW Line

It is first prudent to analyse how the insertion of TSVs into a CPW line affects the transmission profile of that line. To do this, cryogenic spectroscopy was carried out on two samples. The first sample, which shall be called sample 1, consisted of a CPW line that was coupled to a $\frac{\lambda}{4}-$resonator adjacent to the line with a simulated resonance frequency of 5.449GHz. Two large contact pads, which maintained the 50Ω impedance of the CPW, were positioned at each end of the line to allow for wire-bonding. The other sample, sample 2, was formed of a 50Ω CPW line with 2 TSV transitions, each with one signal TSV connecting the CPW lines on the top and bottom of the sample and two parallel ground TSVs to provide a return path for the current. The CPW in sample 2 also had 6 TSVs running along each of its sides that connected the ground planes on the top and bottom of the device. Samples 1 and 2 were metallised with 50nm sputtered Nb and ALD TiN, respectively. The substrate for both samples was a 5x5mm, 250μm thick Si chip. Images of models of samples 1 and 2, created in ANSYS HFSS, are shown in figure 4.14 (a) and (b), respectively.



(a) **(b)**

Figure 4.14: (a) ANSYS HFSS model of sample 1, with a CPW line and resonator. (b) ANSYS HFSS model of sample 2, with a CPW line interrupted by 2 TSV transitions.

Each sample was mounted in an oxygen-free Cu (OFC) sample box, shown in figure 4.15. This is used to make electrical connection to the sample and to provide a clean electromagnetic environment, preventing coupling to spurious modes [137]. Two SMA connectors were attached to opposite sides of the box and their central pins were soldered to the central tracks of two 50Ω microstrip PCBs, which were bonded to the sample box using Ag paste. These microstrips were then wire-bonded to the contact pads on the device under test. The chip itself was held in place by GE varnish applied to two parallel platforms on either side of the interior of the sample box. Between these platforms was a small cavity preventing the central track of the CPW patterned on the reverse side of the chip shorting to the adjacent ground planes. The frequencies of the cavity modes of this region were calculated and were found to fall outside the frequency span of the measurement.

The samples were characterised using two different measurement lines of the same dilution refrigerator. Both were mounted in the mixing chamber stage and were probed using a VNA through a chain of attenuators, amplifiers, and filters. Diagrams of the apparatus used are shown in figures 4.16 (a) and (b). On the input line of the setup used to measure sample 1, there were three -20dB attenuators. With an additional -10dB loss due to the cabling used, this resulted in a total attenuation of -70dB. Following the sample in the chain was a microwave switch, used to switch between multiple samples mounted in the refrigerator, a 4-8GHz circulator, to prevent reflected signals on the output line from reaching the sample, a 3.4-9.9GHz high-pass filter, and a 4-16GHz high-electron-mobility transistor amplifier (HEMT) with 42dB gain, followed by another amplifier at room temperature with a gain of 40dB. This resulted in a total gain of 12dB along the whole chain. Sample 2, on the other hand, was measured using an input line with a total attenuation of -72dB. The components on the output line were the same as used to measure sample 1, except for the HEMT, which was substituted for one with 36dB gain. The total gain through the chain was, therefore, 4dB. The samples were measured in separate refrigerator cooldowns and the substitution of the HEMT was due to a fault in the component

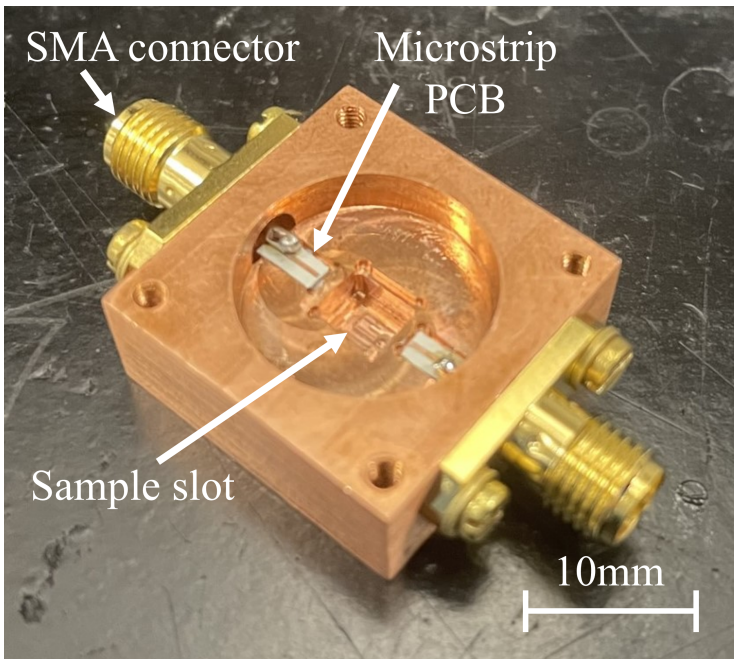


Figure 4.15: Sample box used for mounting chips for cryogenic measurement. The box is closed with a flat OFC lid.

used to measure sample 1 that occurred in the intervening period. Both samples were measured at a temperature of 20mK.

The results of transmission spectroscopy of the two devices are given in figure 4.17. Taking into account the approximately 8dB difference in gain in the measurement setups used to measure the two samples, there was an average increase in loss of 10dB, or 5dB per transition, in the 4-6GHz range, decreasing to 0dB at frequencies approaching 8GHz, as a result of the addition of the two TSV transitions into the design. This implies 32% power loss in each transition in this frequency range - much higher than desired for an interconnect. The performance of the two devices converges at frequencies beyond 6GHz. Therefore, at these frequencies, it appears as though the losses due to the packaging or the materials in the device are as significant as the losses due to the inclusion of the TSVs.

The resonance of the CPW resonator coupled to the line in sample 1 can be seen at 4.965GHz. The ripples observed in the transmission profiles of both samples most likely indicate the presence of impedance mismatches at points along the measurement chain, though an effort was made to reduce these as far as possible. The observed average oscillation periods of 0.181GHz and 0.307GHz of the ripples in the data taken for samples 1 and 2, respectively, indicates that these impedance mismatches occurred at interconnects in the measurement chain of lengths on the order of 10cm - most likely the cabling from the VNA to the samples.

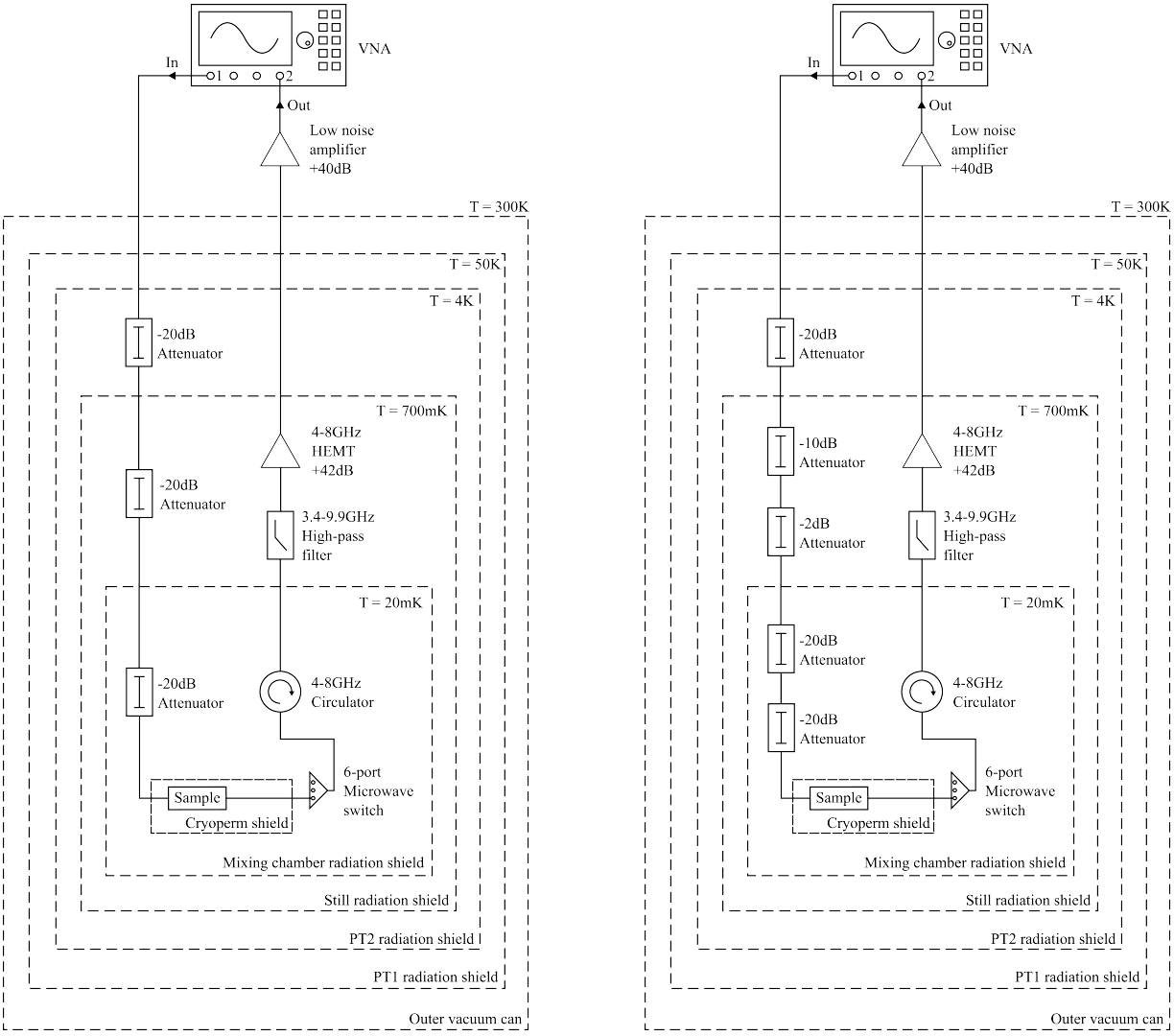


Figure 4.16: (a) Diagram of wiring used in measuring sample 1. (b) Diagram of wiring used in measuring sample 2. 10dB additional loss can also be assumed from the cabling used in both setups.

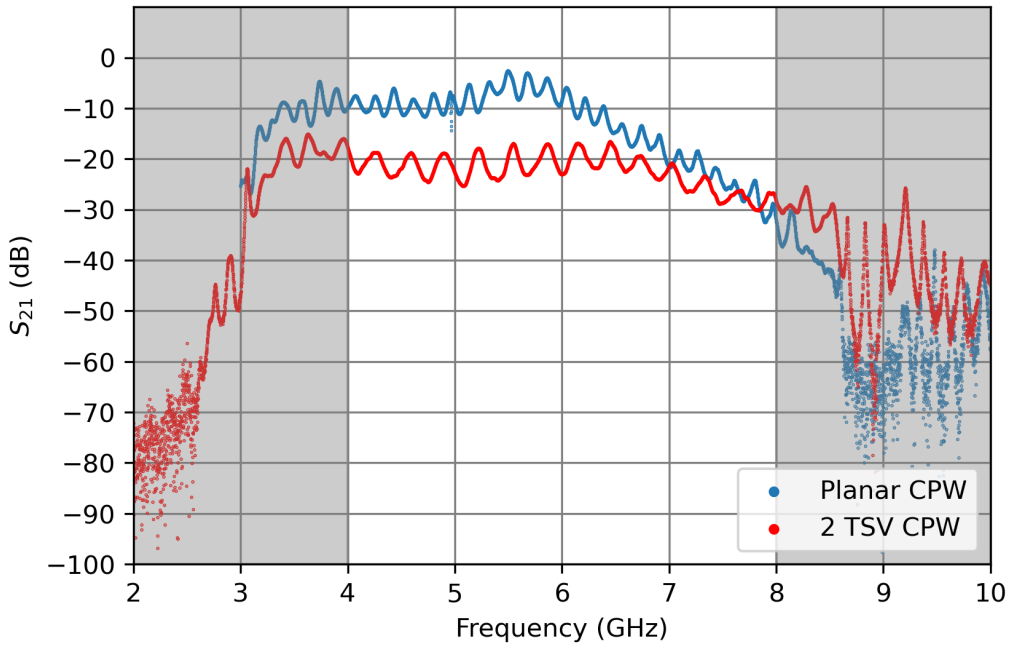


Figure 4.17: Comparison of S_{21} measurements of sample 1 (planar CPW, blue) and sample 2 (2 TSV CPW, red). The VNA power was set to -10dBm for both measurements. Regions outwith the frequency span of the narrowest band microwave component in the measurement chain are shaded grey. The data for samples 1 and 2 presented here has been plotted after taking into account the gains of 12dB and 4dB, respectively, of the measurement setups used for each sample. This is to allow for a more direct comparison of the two samples.

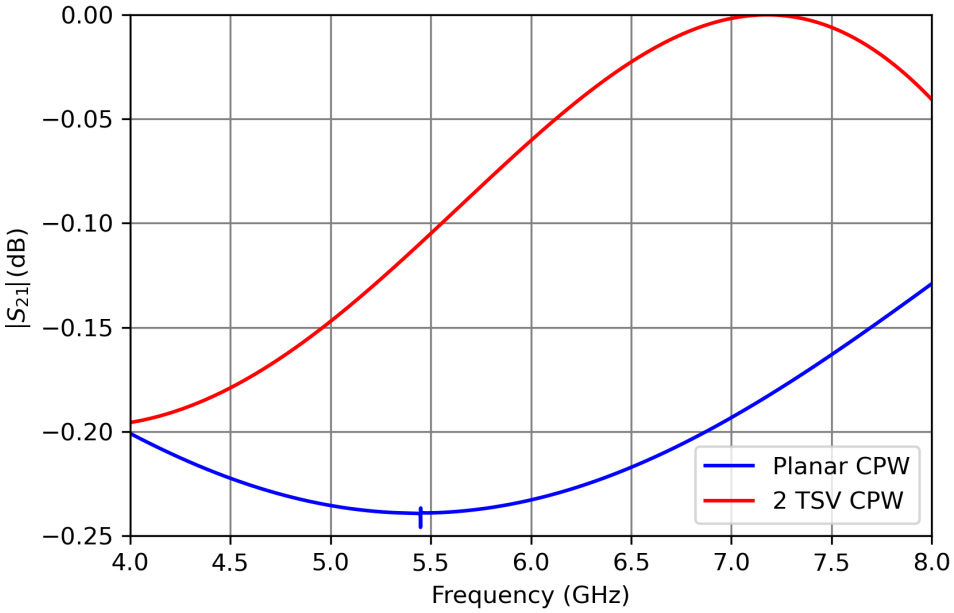


Figure 4.18: Comparison of the simulated S_{21} parameters of sample 1 (planar CPW, blue) and sample 2 (2 TSV CPW, red) from 4-8GHz. A dip in the transmission of the simulated sample 1 due to the CPW resonator coupled to the feedline is present at 5.449GHz.

Prior to their fabrication, simulations of the S-parameters of the two devices were carried out in ANSYS HFSS. This was done in order to ensure that the devices exhibited characteristics suitable for their purpose as interconnects and to serve as a comparison with the experimental data. The conducting layers in the simulated devices were modeled as perfect electrical conductors. Broadband adaptive meshing between 2-10GHz was used with a maximum parameter variation of 1% per pass of the adaptive solver allowed. The devices were simulated between 4-8GHz at 1MHz spacing. The simulated results are shown in figure 4.18.

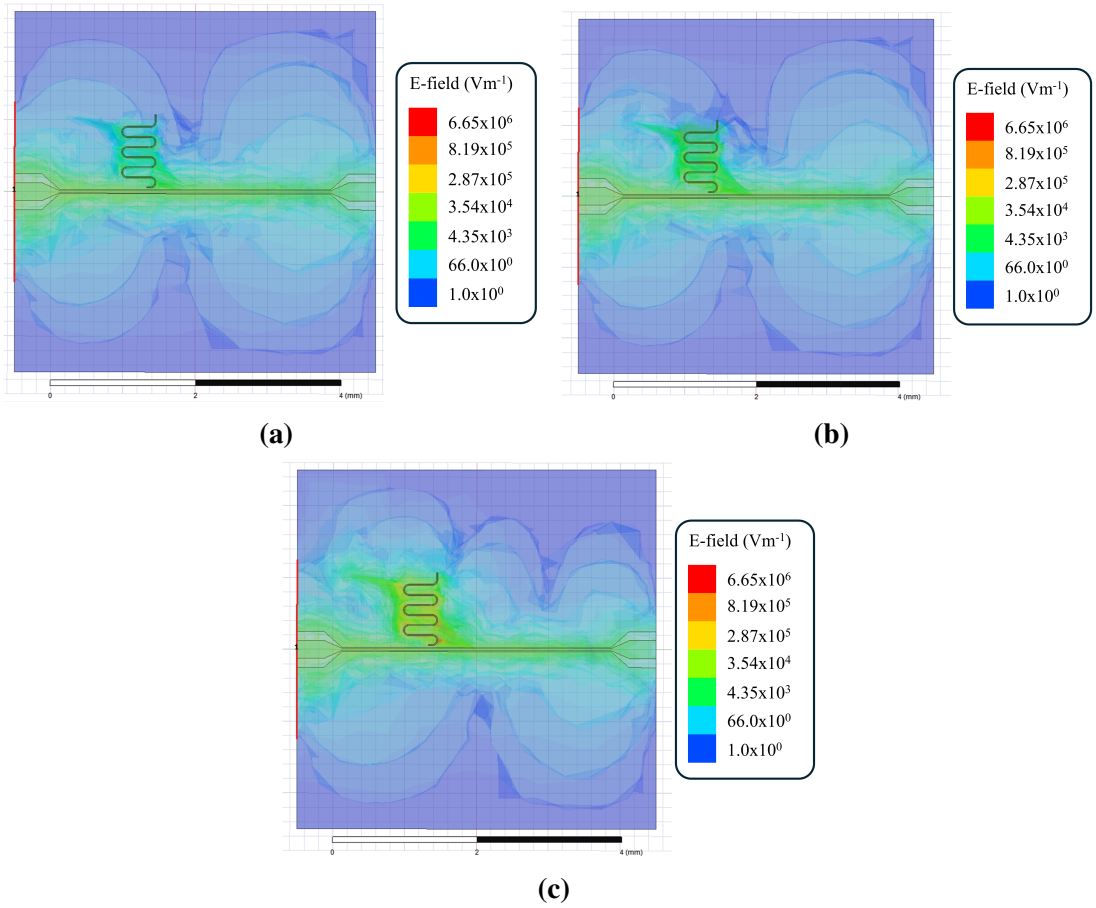


Figure 4.19: Plots of the simulated magnitude of the electric field for the model of the planar CPW at (a) 5.4GHz, (b) 5.445GHz and (c) 5.449GHz. The power leaking to the resonator can be seen to be increasing as the resonance frequency is approached.

The simulations of both designs showed excellent transmission and they were, therefore, deemed satisfactory for fabrication. Perhaps surprisingly, the planar CPW showed a lower transmission over the simulated frequency range than the design that incorporated TSVs. This was caused by the input power leaking to the resonator in sample 1. This is supported by the observation that the transmission approaches a minimum at the resonance of 5.449GHz and also the plots of electric-field strength in the region of the resonator increasing in magnitude as the resonance frequency is approached from above and below, shown in figure 4.19. The deviation

from the simulated resonance frequency value in the measured sample could be explained by the kinetic inductance of the Nb film, which is not taken into account in the simulation of the device, increasing the total inductance of the resonator and therefore decreasing its resonance frequency.

This reduction in frequency may be used to determine the kinetic inductance of the film. The measured and simulated resonance frequencies of the resonator may be described, respectively, as:

$$f_{r,m} = \frac{1}{2\pi\sqrt{(L_m + L_k)C}}, \tag{4.2}$$

$$f_{r,s} = \frac{1}{2\pi\sqrt{L_m C}}, \tag{4.3}$$

where L_m, L_k and C are the magnetic inductance, kinetic inductance and capacitance of the resonator. Combining these two equations gives an expression for the kinetic inductance:

$$L_k = \frac{1}{2\pi C}\left(\frac{1}{f_{r,m}^2} - \frac{1}{f_{r,s}^2}\right). \tag{4.4}$$

By simulating the resonator chip in ANSYS Q3D, the capacitance of the CPW resonator was determined to be 473.99fF. Inserting this value and the two previously determined resonance frequencies into equation 4.4 gives $L_k = 2.27$nH, or 0.65pH/μm.

Clearly, the fabricated devices performed significantly worse than the simulations predicted. However, the simulations can be taken as evidence that the unexpected results are not the fault of the designs themselves. This indicates the loss observed in both samples originates from fabrication or packaging related sources. This will be discussed in further detail in section 4.2.2.

4.2.2 Comparison of TiN and NbN Films in TSVs

In this section, the performance of TSVs from three samples, named samples 3, 4, and 5 metallised with sputtered TiN, PEALD TiN and substrate-biased PEALD NbN, respectively, is compared. The details of the depositions of each film may be found in section 4.1.3. The electrical resistance of individual TSVs was measured using a 4-pt probe on a Cascade Microtech® Summit 12000 Semi-Automatic Wafer Prober. IV measurements of cross-bridge Kelvin resistor (CBKR) structures were made and the resistance of a single TSV was extracted using the dimensions of the sample and the measured resistivity of the top and bottom TiN or NbN films. A diagram of the CBKR structure and the results of the measurements are shown in figures 4.20 and 4.21, respectively. These test structures are most commonly used to determine contact resistance in transistors, however they have also seen application in TSV characterisation in recent years [78, 138–140]. With reference to figure 4.20, the CBKR structure is designed such that current is forced between points I^+ and I^-, and the voltage drop across the central TSV is mea-

sured by probes placed on the contact pads labelled V^+ and V^+. The resistance of the central TSV can then be calculated from: $R_{TSV} = \frac{V^+ - V^-}{I}$, where I is the forced current [78, 139].

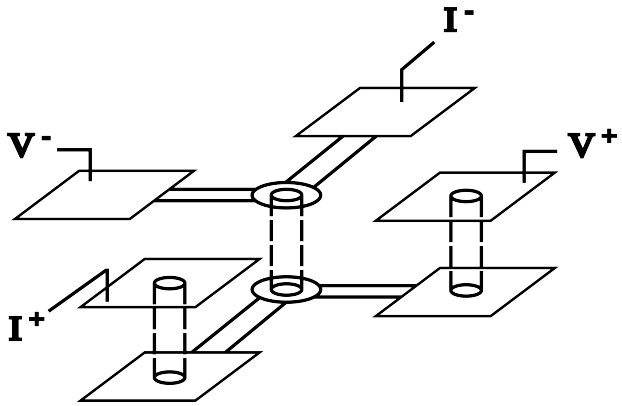


Figure 4.20: Cross-bridge Kelvin resistor structure used to measure the resistance of individual TSVs.

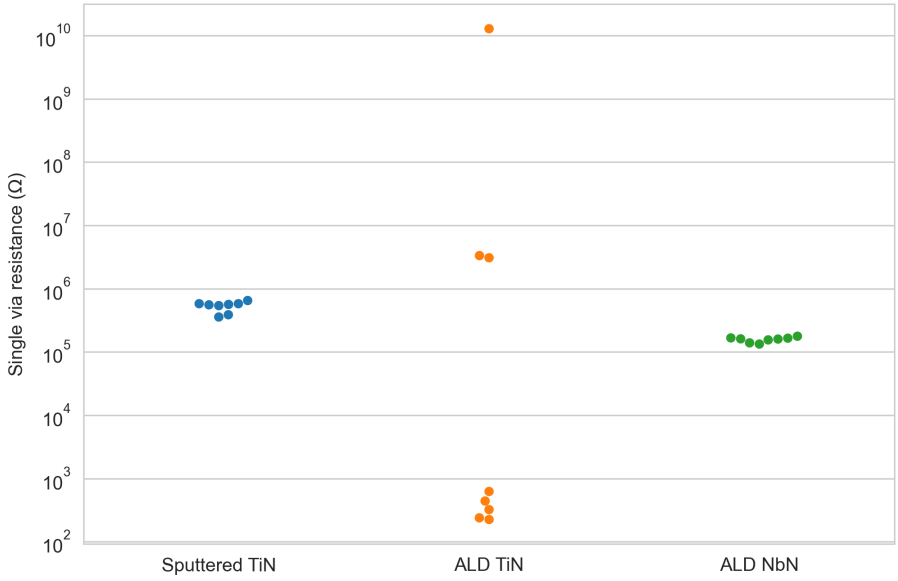


Figure 4.21: Measurement of the room temperature resistance of single TSVs, grouped by fabrication procedure. Sputtered TiN, ALD TiN and ALD NbN were used on samples 3, 4 and 5, respectively.

Each of the data points on the chart represent a measurement of a single CBKR structure for which the IV response was approximately linear. It is clear that the extracted resistance for the structures fabricated from ALD TiN sample span a large range. However, it is likely that the data at the lower end of this range are closer to the true resistance of the TSV. The much larger values are either due to the very high hardness of the TiN film making it challenging to obtain good contact between the probes and the film, or could indicate insufficient film coverage inside the TSVs incorporated into these structures.

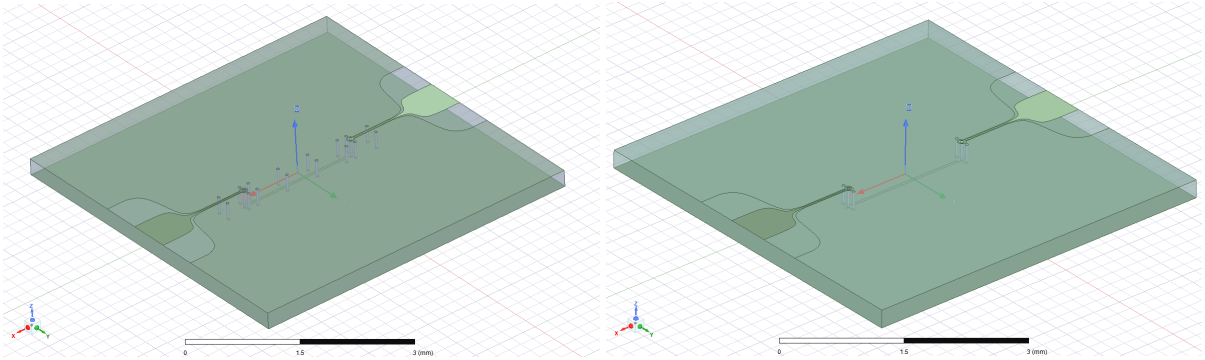
Given the measured resistivities of the ALD TiN films and the geometry of the structures, the expected resistance of single TSVs fabricated this way was calculated to be between 1.5kΩ and 3.3kΩ at room temperature. The majority of measurements for TSVs of this type fall within this expected range, showing that there is likely good galvanic contact through these TSVs.

However, for a given NbN CBKR structure, the maximum expected resistance was approximately 1.2kΩ. The measured resistances are on the order of 100x greater than these expected values. This points to the probe current flowing through the Si substrate. The resistance of the volume of Si between the two contact pads of the measured structures was estimated to be 14kΩ. This is an order of magnitude less than the measured value, which may again point to poor contact between the probes and the NbN film. It is instructive that in the work by Sowa et al., pads fabricated from In (a comparatively very soft metal) were pressed directly onto the NbN surface in order for the probes used to measure the resistivity of the film to make better contact with the surface [126]. This is perhaps an improvement that could be made to future experiments of this type.

Cryogenic S-parameter measurements were carried out on a sample consisting of a TSV-interrupted CPW line metallised with 121nm thick NbN, which shall be referred to as sample 6. The results of this measurement were compared with the results of the measurement of sample 2, which was metallised with 62nm TiN, discussed in section 4.2.1. Sample 6 was of the same design as sample 2, except that it had no flanking ground TSVs running along the CPW line. Images of these two designs are shown in figure 4.22. A comparison of the simulated S-parameters of these two devices is shown in figure 4.23. For a true comparison of the relative performances of the two materials, it would have been preferable for both structures to have been of identical design. However, from the simulated data, it can be seen that the inclusion of these flanking TSVs results in very little expected difference between the performance of the devices.

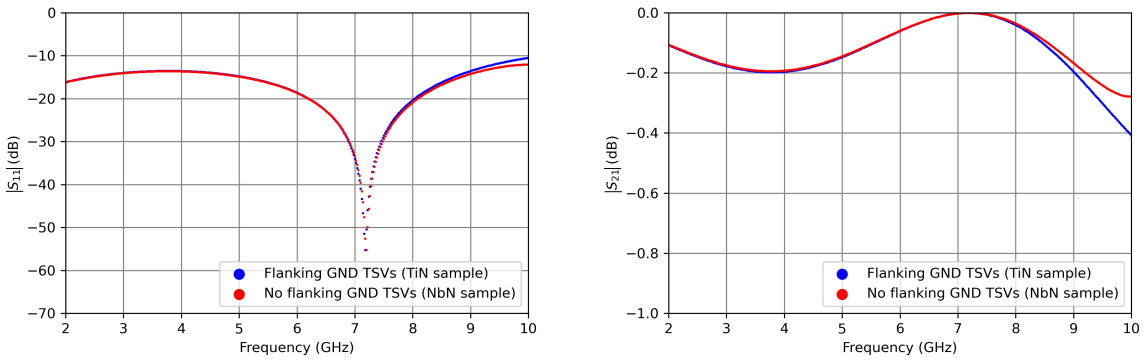
Sample 6 was measured in an Oxford Instruments ProteoxMX dilution refrigerator with 70dB attenuation on the input line and a 4-8GHz circulator, 4-8GHz isolator, 4-8GHz HEMT with 35dB gain, and an 35dB room temperature amplifier on the output line. This resulted in 0dB gain along the whole line. Samples 2 and 6 were both measured at 20mK. A diagram of the setup used for the measurement is shown in figure 4.24. As was the case with the comparison of samples 1 and 2 in section 4.2.1, it would have been preferable for samples 2 and 6 to have been measured using the same RF lines in the same refrigerator in order to remove any systematic differences from the results such that a more direct comparison could be achieved.

The results of the cryogenic spectroscopy of the two samples are shown in figure 4.25. The NbN sample (sample 6) showed higher reflection than the TiN sample (sample 2) across the frequency range of interest. There was also significantly more noise in the measurement than the equivalent measurement of the TiN sample. Over the frequency span, the less than 20dB



(a) **(b)**

Figure 4.22: ANSYS HFSS model of CPW structures. (a) CPW interrupted by 2 TSV transitions with flanking TSVs connecting the ground planes (sample 2). (b) CPW interrupted by 2 TSV transitions without flanking TSVs connecting the ground planes (sample 6).



(a) **(b)**

Figure 4.23: Comparison of S_{11} (a) and S_{21} (b) simulations of CPW transmission lines with (sample 2) and without (sample 6) flanking TSVs connecting the ground planes.

return loss indicates that either there was no significant impedance mismatches in the system or that the reflected energy was absorbed by the lossy structure. The transmission profiles of both samples was very similar, with both demonstrating losses of approximately 20dB. This implies that approximately 1% of the incident energy was transmitted through the chips.

In the transmission profile of sample 6, a large resonance occurs at 7.62GHz. Taking the ε_r of the Si substrate to be 11.9 and using equation 2.15 to calculate the characteristic length for such a resonance returns a value of 5.7mm. Given that the sum of the lengths of the CPW line and the two TSVs is 5.5mm, it is reasonable to propose that this resonance was due to the trace itself. This does, of course raise the question of why similar resonances were not observed in the measurements of any of the other samples containing two TSV transitions discussed in this

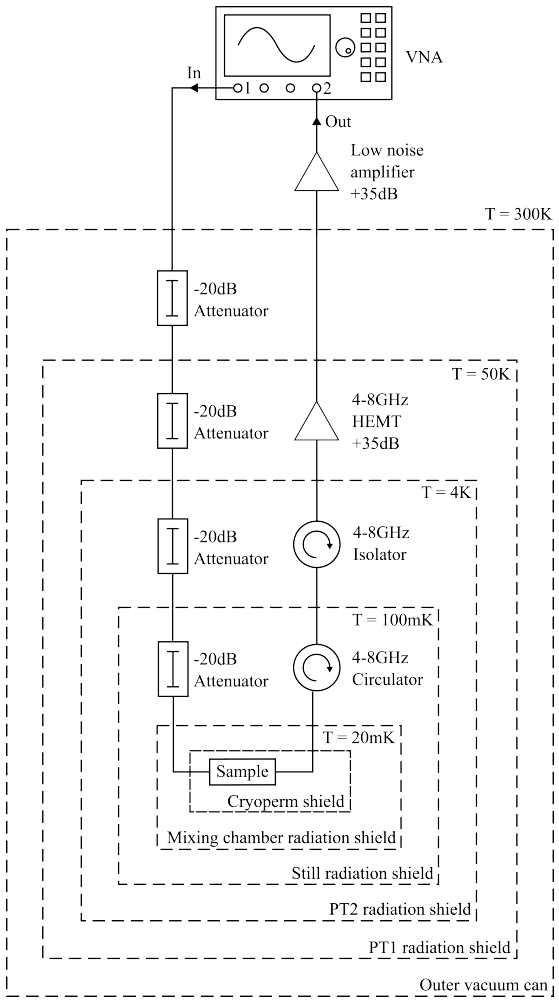
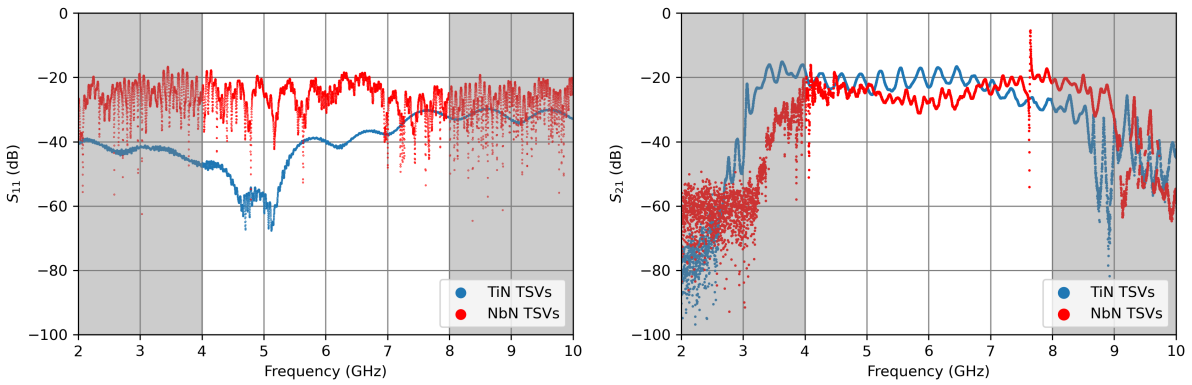


Figure 4.24: Wiring diagram of the setup used to measure sample 6.

work, which all featured CPW traces of the same length. As sample 6 was fabricated from NbN, it could be possible that the impedance mismatch between the wirebonds at the sample contact pads was larger than that of the TiN samples. This could also go some way towards explaining the larger reflected power exhibited by this sample.

Given the low transmission of the samples, it is reasonable to ask whether the signal is being transmitted through the samples at all. To do this, a measurement of the transmission of the sample was performed while varying the temperature of the dilution refrigerator. If the signal is indeed being transmitted through the sample, a sharp decline in transmission should be observed as the refrigerator is heated past the critical temperature (T_c) of the NbN film. T_c values of NbN vary depending on deposition method, film thickness, film quality and a variety of other factors, but are generally $\sim$14K. The temperature of the refrigerator was therefore steadily increased to a neighbourhood of this value.

Figure 4.26 shows that the transmission of the sample decreased when its temperature was increased past 12K. This is, therefore, taken as the approximate T_c of the sample and evidence that the microwave probe signal is indeed being transmitted through the sample.



(a) **(b)**

Figure 4.25: Comparison of S_{11} (a) and S_{21} (b) measurements of TSV-interrupted CPWs metallised with TiN and NbN. The data has been corrected for the gain in the respective measurement lines, which was 4dB and 0dB for samples 2 and 6, respectively. The VNA power was set to -10dBm for all four measurements. Regions outwith the frequency span of the narrowest band microwave component in the measurement chain are shaded grey.

There are a multitude of possible causes of the loss seen in these results. It is extremely difficult to disentangle these sources in order to declare one more dominant than the other, particularly given that neither the structures, nor the measurements performed on them were designed to probe these losses. Nevertheless, loss mechanisms shall be proposed in an attempt to explain the observed results, as will possible improvements to the fabrication of the devices in order to lessen the effects of these mechanisms.

Given that the resistivities of the two ALD films appear to be, while perhaps not the lowest achieved for these particular materials, still within an acceptable range for superconducting circuits, it is doubtful that the losses seen in the previous experiments can be entirely explained by the quality of the films. It could also be possible that there exists an open circuit in the interior of the measured TSVs. Indeed, the measurements of the single TSV room temperature resistance shown in 4.21 would appear to support this, particularly in the case of the NbN TSVs. However, as evidenced in figure 4.9, it appears as if the ALD films are conformal along the full length of the TSV. There should, therefore, be galvanic contact throughout the TSV.

One explanation for the loss that could be posited is that the TSV sidewall roughness has adversely affected the signal transmission through the structure. An example of this roughness is shown in figure 4.13 (a). It has been shown by Nakamura et al. that scalloping is linked to an increase in leakage current between adjacent TSVs [135]. In this work, the TSVs were filled with Cu and lined with a SiON barrier layer. The leakage current was linked to the scalloping causing stress concentrations in the barrier layer leading to tensile cracks. It is, therefore, doubtful that this mechanism could be directly translated to the samples discussed here. However, it is possible that, in a similar way, stress in the film caused by the rough surface could result in

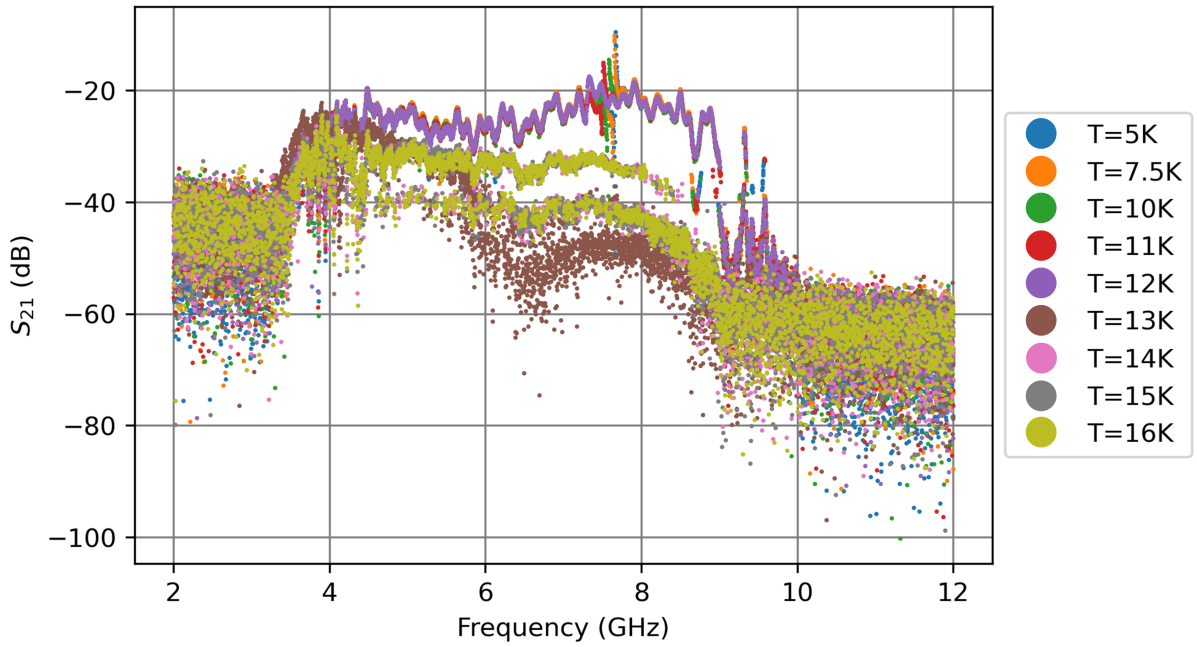


Figure 4.26: Measurement of transmission of sample 6 at various temperatures.

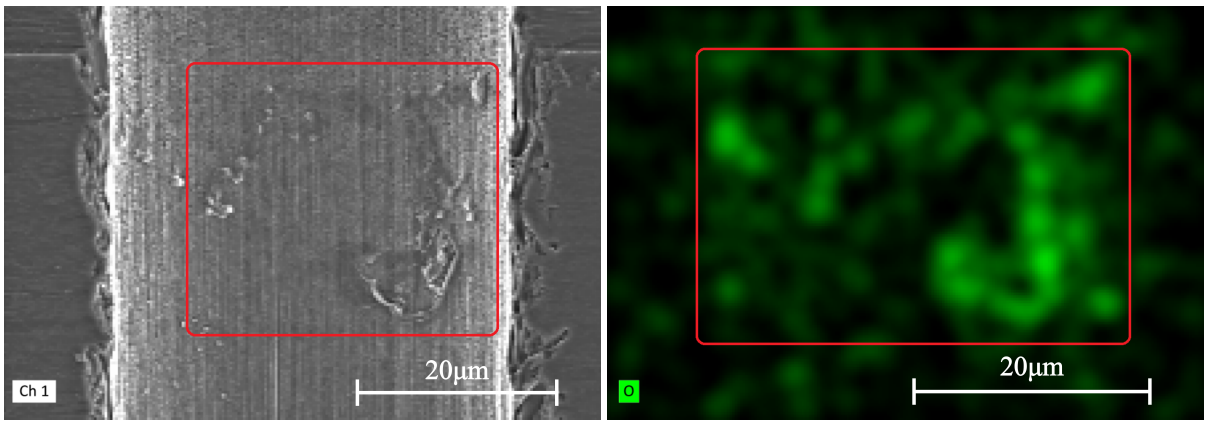
cracks in the metallisation layer, leading to reduced transmission.

High-frequency modelling of normal metal TSVs has also determined that sidewall roughness causes an increase in the electrical resistance of the TSV and hence a decrease in transmission [141]. This is due to the roughness of the TSV being of similar dimension to the skin depth of the material. In the case of the samples analysed here, there should ideally be no electrical resistance, due to their superconductive properties. It may, however, be the case that there are non-superconducting regions in the film that are subject to this effect.

Perhaps the most convincing proposition for the mechanism behind the roughness-induced loss is that described by Wisbey et al. [142]. They suggest that the increase in the area of the interface between the metal layer and the Si substrate caused by the surface roughness is the source of loss. In particular, it has been shown by these authors and a host of others that two-level systems (TLS) reside at the metal-substrate interface (as well as at the metal-air, substrate-air interfaces and in bulk dielectrics) and are a dominant loss mechanism in superconducting quantum circuits [42, 142–148]. The exact nature of these TLS is still a matter of debate, however, the proposed mechanism is that one or more atoms present at the site of a defect in the material will tunnel to another adjacent site, absorbing energy which is re-emitted as a phonon [42, 146, 148]. Each TLS will only absorb energy at, or near to, its characteristic frequency. However, because they originate from the random defects that occur in a given material, the energy spectrum of the TLS is thought to be uniform [146, 148]. They could, therefore, be a source of loss across the frequency span of the measurement. TLS loss tends to dominate the losses seen by resonant circuits at the single photon limit, which is the limit in which the above experiment was

performed [42, 142].

SiO_2 is known to be a major source of TLS in superconducting circuits that are fabricated on Si substrates [143]. The propensity for rougher surfaces to have a higher concentration of SiO_2 than smooth surfaces is demonstrated in figure 4.27. Here, an energy dispersive X-ray spectroscopy (EDX) scan of the cross-section of a TSV was made and the region of highest oxygen concentration was clearly seen to be the region of increased roughness. This could indicate a link between the increased roughness of the TSV sidewall and the exposure of the signal to TLS as a result of the larger concentration of SiO_2 adjacent to the nitride film.



(a) **(b)**

Figure 4.27: (a) Cross-sectional SEM image of a TSV prior to metallisation with a region of increased roughness highlighted by a red box. (b) EDX map of the same region showing its oxygen content. The area of the highest oxygen content can be seen to correspond the region of increased roughness.

A variety of other sources of loss exist in superconducting microwave circuits. One that has been shown to be dominant in circuits made from high kinetic inductance (L_k) materials, in particular TiN, is quasiparticles [144]. These are thought to be generated by exposure to external microwave, infra-red or optical radiation, ionising radiation from radioactive materials in the environment or even cosmic rays [149]. Multi-photon absorption and quasiparticle recombination can result in the emission of phonons, which in turn may generate further pair-breaking [148, 150, 151]. Increased disorder in superconducting films has been shown to decrease the quasiparticle recombination time, though more investigation into the degree of order of the films studied herein would need to be undertaken to understand this effect in relation to these films [152]. The samples in all experiments are well shielded to mitigate these processes, however, they cannot be eliminated entirely and so quasiparticles remain a concern in superconducting circuits.

Other sources of loss in the system could include vortex loss, radiation loss, slotline loss and many others. However, further experiments would be needed in order to elucidate the degree to

which each of sources these play a role in the reduced transmission seen in the experimental data. Generally, one would need to measure the reduction in quality factor of a microwave resonator and how this varies with power to determine the proportion of loss attributable to TLS. The variation in resonance frequency that results from a change in the complex conductivity of the material may also be used to determine the quasiparticle loss [152].

There are possible solutions to the reduction in transmission that could be explored. Primarily, incorporating the post-Bosch etch sidewall smoothing techniques mentioned in 4.1.5 in order to reduce the surface roughness of the interior of the TSVs. In a similar vein, one could look to optimise the Bosch etch itself, such that it produces TSVs of smooth, vertical sidewalls. Furthermore, dipping the sample in HF prior to metallisation has been shown to reduce the number of TLS at the metal-substrate interface [147]. A number of other methods may be employed to reduce the exposure to TLS, such as etching trenches into the gap between the central trace and ground planes of the CPW line or increasing the width of the central trace. However, it would appear that these are perhaps solutions that should be explored after the TSV fabrication process has been perfected. As a result of the factors discussed in this section, it is not possible to declare here that either TiN or NbN is a superior material for the fabrication of superconducting TSVs. Both are similar with respect to fabrication challenges and both have shown similar performance in the experiments conducted here. The one major difference between the two that is certainly apparent from this work is the much higher T_c of NbN, which allows it to be used in settings without, for example, access to cryostats with the capability to reach the lower temperatures required to reach the T_c of TiN. It could, therefore, perhaps be a more practical choice for superconducting TSVs.

4.2.3 Calibrated S-Parameter Measurements

When quantum integrated devices are measured inside a dilution refrigerator, the signal must pass through a long chain of lossy cables, attenuators, amplifiers, circulators, isolators and other microwave components. This makes it difficult to extract the true behaviour of the device under test (DUT) as the response measured by, for example, a VNA will have been distorted by this component chain. One can of course attempt to account for these components, however commercially available options are often not tested for operation at cryogenic temperatures and, therefore, their performance, while likely remaining similar, will change at least somewhat due to changes in material properties, such as dielectric constant or resistivity [153, 154]. To obtain a true measurement of the S-parameters of a DUT inside a dilution refrigerator, it is therefore beneficial to de-embed the DUT from this external circuitry. This may be done through the use of a calibration scheme. In the case of interconnects, such as TSVs, it is of particular interest to have as direct a measure as possible of the transmission and reflection profiles of the device. Calibration schemes also have the advantage of removing systematic errors in the measurement

apparatus from the S-parameter measurement.

Here, to the author's knowledge for the first time, superconducting TSVs are measured using such a calibration scheme at mK temperatures. A thru-reflect-line (TRL) calibration technique was used, which requires the measurement of transmission standards of differing electrical lengths (thru and line) as well as a pair of reflect standards [155]. The calibrated S-parameters of the device at mK temperatures are found by measuring the uncalibrated S-parameters of the device and the standards, after which the offline calibration scheme is applied. The TRL calibration scheme is chosen over, for example, a SOLT calibration scheme as there is no need for a 50Ω load in the measurement and those calibration standards that are required do not need to be precisely characterised. The two reflect standards should, however, be identical. This is advantageous as characterising these standards at cryogenic temperatures is challenging [154–156].

The setup used for the calibration is shown in figure 4.28. This consisted of two 8-port microwave switches, each with one port connected to the thru, line and reflect standards and one port connected to each DUT. SMA adapters were needed to connect the sample boxes to the coaxial cables used in the measurement and so the DUT could be more precisely considered to be the combination of the sample box and the adapter. Given the high quality of the components used, these adapters would have introduced very little attenuation to the measurement but this is noted for completeness. The switches are commercially available pulse-latched switches which are switched by 10ms, 5V pulses. These allow all of the calibration standards and the DUTs to be measured in one thermal cycle of the dilution refrigerator, which reduces the risk of drift and random errors from affecting the calibration [154]. There is a small increase in the temperature of the refrigerator after the pulse is applied to the switch, but the effect on the calibration is negligible.

The thru standard was a zero-length through connection of the coaxial cables. 3.5mm coaxial male short standards manufactured by Maury Microwave were used as reflect standards. Air lines were used to connect the switch ports to the standards and DUTs in order to prevent the adverse affects that may be brought about by the properties of the dielectric contained within standard coaxial cable changing at mK temperatures. The whole arrangement was attached to a Cu mount, which was then installed at the mixing chamber stage of the refrigerator in order to adequately thermalise the setup. These measurements were conducted at the National Physical Laboratory by Manoj Stanley on samples fabricated in the James Watt Nanofabrication Centre at the University of Glasgow by the author.

The first of the samples measured, which shall be named sample 7, consisted of a CPW transmission line interrupted by two TSV transitions, with two rows of TSVs flanking the CPW that connected the top and bottom ground planes and broad contact pads for wirebonds at each end. Adjacent to the CPW were two resonators that were split over the top and bottom layers and interrupted by 3 and 4 TSVs, respectively. These had nominal resonance frequencies of

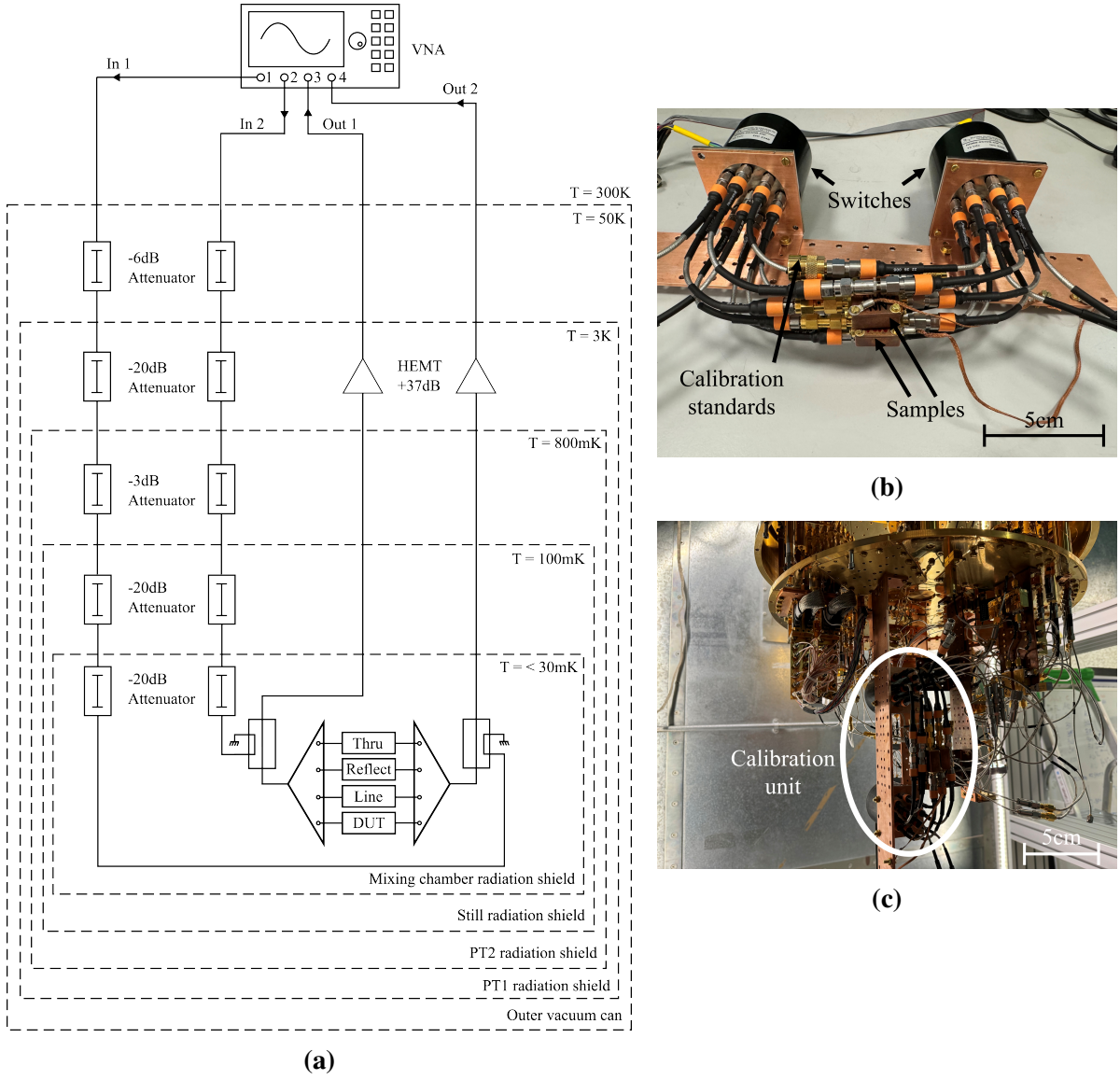
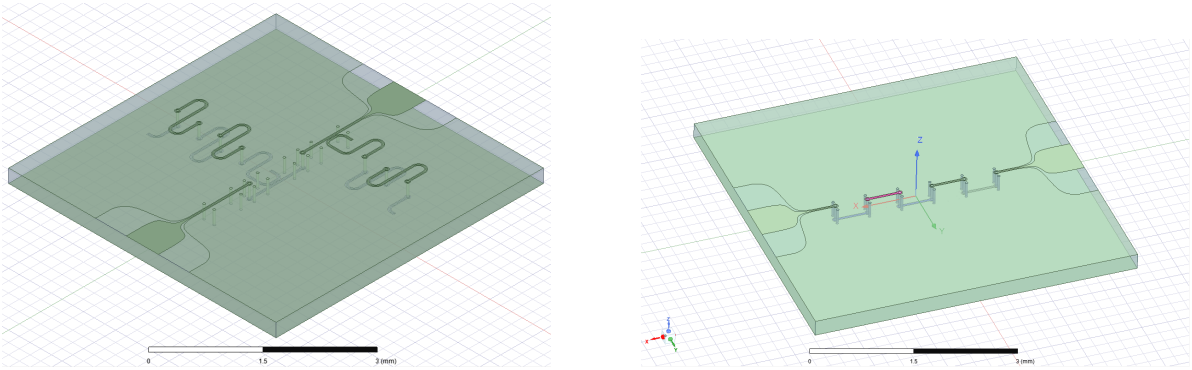


Figure 4.28: (a) Diagram of calibrated S-parameter measurement setup. (b) Sample mounted between switches before being installed in dilution refrigerator. (c) Switch setup and sample installed in dilution refrigerator.

6.09 and 8.07GHz. The second measured sample, named sample 8, consisted of a CPW line interrupted by 6 TSV transitions. These transitions are each made up of a single signal TSV and two adjacent ground TSVs. The CPW also had two contact pads at each end. Both samples were fabricated on the same wafer, which was metallised with 62nm TiN and both were mounted in identical Cu sample boxes, with the ground planes wirebonded to the box. Diagrams of the two samples are shown in figure 4.29.

The results of sample 7, shown in figure 4.30 (a) clearly show a much higher reflection and lower transmission than desired. The measurements were conducted between 4-8GHz as this was the frequency span of the amplifier used in the measurement. The lowest transmission (-



(a) **(b)**

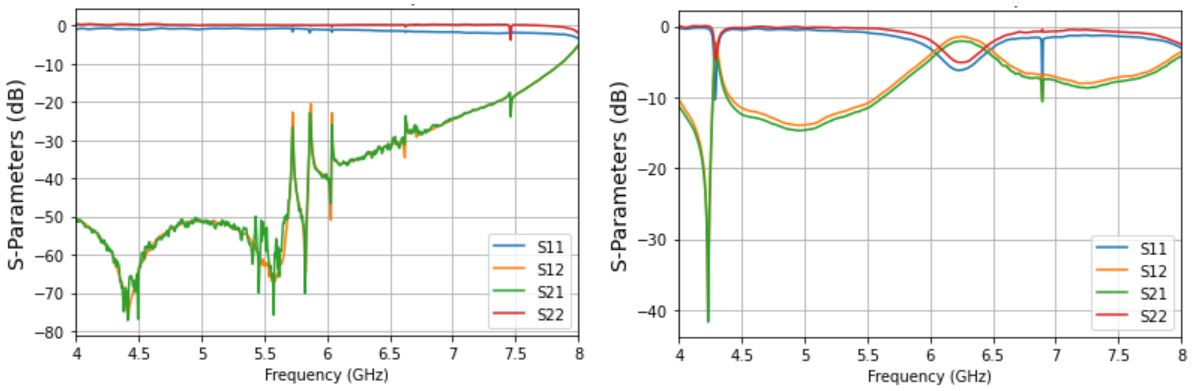
Figure 4.29: Diagrams of sample 7 (a) and sample 8 (b). White regions represent those areas of the sample that were metallised. Blue and red features are etched into the top and bottom layers of the device, respectively. TSVs are represented as small purple circles.

76dB) was seen at around 4.5GHz and the highest was seen at 8GHz, the limit of the frequency span of the measurement. The performance of the device does improve with frequency so it is possible that at frequencies beyond the span of the measurement the transmission could increase further. However, it is clear that there is an issue with the device that is causing this behaviour. There may be a disconnection or narrowing of the film at some point along the CPW trace, though from SEM images of other devices from the same wafer, this appears unlikely. The discussion of loss mechanisms present in the TSVs from 4.2.2 is also applicable to the devices measured here. Due to the profile of the transmission and reflection of the device, it is difficult to declare whether the expected resonances appear. There is a large resonance at 6.03GHz, which is very close to the expected 6.09GHz. However, the kinetic inductance of the film must also be taken into account as this could result in a shift in the resonance frequency of the resonators. The nominally 8.07GHz resonance is beyond the span of the measurement though, again, the kinetic inductance of the film may reduce this nominal frequency.

Sample 8, the results of the measurement of which are shown in figure 4.30 (b), gave slightly better results, though suffers from the same general issue of giving higher than desired reflections and lower than desired transmission. Here though, there are some regions of the frequency span in which the transmission is within the acceptable range for an interconnect. Notably, at 4.3GHz, $S_{12} = -2.21$dB and $S_{21} = -3.48$dB. At this frequency, $S_{11} = -9.23$dB and $S_{22} = -4.73$dB, which is still relatively high. At 6.3GHz, there is also a peak in transmission, with the S-parameters measured to be: $S_{11} = -6.13$dB, $S_{12} = -2.08$dB, $S_{21} = -1.44$dB and $S_{22} = -5.07$dB. The S-parameters of both devices were simulated between 2-10GHz prior to fabrication and the transmission was found to be > -0.5dB for each, with a maximum reflection (aside from resonant frequencies) of -14dB for sample 7 and -10dB for sample 8.

There is also a slight non-reciprocal behaviour in both of the devices. The VNA power for

these measurements was set to 10dBm, with 80dB attenuation on the input lines and it is possible that this input power saturated the amplifier, causing the non-reciprocity.



(a) **(b)**

Figure 4.30: Calibrated S-parameter measurements of TSV samples 7 (a) and 8 (b). Resonances due to TSV-interrupted resonators in sample 7 were expected to occur at 6.09GHz and 8.07GHz.

Chapter 5

Conclusions and Outlook

The aim of this thesis was to develop superconducting TSVs compatible with superconducting qubits. This included the simulation of these structures as well as establishing a process for their fabrication and characterising the performance of the resulting TSVs. These would have ideally exhibited low loss at mK temperatures, such that if they were integrated into quantum circuits, they would not act as an additional source of decoherence.

These aims were met with mixed success. TSVs were fabricated and characterised at mK temperatures, however the losses measured would likely preclude their use as interconnects for qubit applications. This is not to say that nothing was gained in the course of the project, however. Simulation results determined the optimal configuration of grounding TSVs for the minimisation of crosstalk. Techniques for the smoothing of the sidewalls of TSVs were explored and compared, and a demonstration of the measurement of the S-parameters of superconducting TSVs using a calibrated setup was presented for the first time.

Designs for various TSV test structures were simulated and an optimal combination of parameters was found for the characterisation of the TSVs using these structures. Further to this, a design for a TSV-integrated tunable coupler for use in qubit circuits was simulated, including the determination of relevant parameters, such as the capacitances and coupling strengths. This is a concept that emphasises the space-saving and hence scalable properties of 3D-integrated structures for quantum applications. As mentioned, the effect that the configuration of grounding TSVs has on the crosstalk between neighbouring signal TSVs was also investigated by simulation. It was determined that using 4 ground TSVs to shield the signal TSV results in a dramatic reduction in crosstalk, with values < -140dB at 4GHz. Different arrangements of 3-TSV transitions were also compared and it was shown that the overall structure of the device is a crucial factor in the optimal configuration of such a structure.

In terms of TSV fabrication, various TSV-defining Bosch etches were compared and their affect on the roughness of the sidewall of the resulting TSVs was explored. It was posited that,

in line with available literature, parameters such as the ICP power and total etch time were highly influential in this respect. The occurrence of micromasking and thus grass and striation formation was shown to also be dependent on the etching gas flow rate and the chamber pressure during the etch. Furthermore, it was shown that it is beneficial, in terms of roughness at least, to complete the etch in one run and avoid any top-up etches- something that would be natural if the process were to be applied to the fabrication of devices on a large scale.

Following on from these results, post-Bosch methods of smoothing the TSV sidewalls were investigated. It was determined that the theoretical atomic level smoothness offered by the use of KOH to etch the TSV interior was the superior method in terms of smoothing capability, but that the prerequisites imposed on the sample and resulting TSVs, such as crystal orientation and the shape of the TSV cross-section, may be drawbacks that process designers should consider prior to incorporating this technique into their fabrication. The oxidation method presents an attractive alternative in this respect as it is not bound by these restrictions and can be used repeatedly to smoothen surfaces to the designer's desire.

In the first portion of the TSV characterisation, at room temperature and using a cryogenic measurement apparatus, the losses exhibited by the TSVs made it clear that these particular devices would be unsuitable for quantum applications. However, an origin of these losses was proposed as the sidewall roughness induced prevalence of TLS at the interface between the metallisation layer and the Si. The films themselves were unlikely to be the cause due to their favourable comparison to others reported in the literature in terms of resistivity. Moreover, a subset of the ALD TiN TSVs measured for their single-TSV room temperature resistance fell within the expected range, demonstrating that the fabrication process did indeed produce TSVs through which a current path was formed. The same measurement of ALD NbN TSVs was inconclusive as it is likely that the contact between the probes and the film was insufficient for an accurate measurement. Additional measurements of, for example, resonator structures would be required for the precise determination of the dominant loss mechanisms in the TSVs.

The use of the calibrated S-parameter measurement apparatus resulted in more promising results. While the bandwidth of the TSVs measured was narrow, they did exhibit a peak transmission of -1.44dB, which is in line with values expected for an interconnect. Taken as a whole, the application of this measurement technique to superconducting TSVs is a demonstration of a characterisation method that could be incredibly useful in isolating the performance of these devices.

Looking to the future, there are a number of improvements to the fabrication process that could be explored in order to increase its reliability and the performance of the TSVs it produces. The substrates used in this work were 4", 275μm thick Si wafers. After the first Bosch etch step, these substrates were effectively perforated by rows of TSVs, due to the pattern of the chips on the photomask. This made the wafers very susceptible to breakage, decreasing the yield of

the process. Using thicker substrates of smaller diameter would help to mitigate this, though to preserve the same TSV aspect ratio, a change in the TSV diameter would be necessary.

The Bosch etch itself could have also been optimised more thoroughly. This would include further investigation of the effect of changes to the parameters of the etch itself, with a focus on the use of less aggressive etch parameters in order to limit TSV sidewall roughness. One process modification that is particularly promising is the use of a SiO_2 hard mask. This has been shown to reduce the roughness of TSV sidewalls and would also have prevented the transference of defects in the photoresist mask to the surface of the substrate. This is generally of less significance in shallow Si etching, but in deep Si etching, when the mask is exposed to the etching plasma for an extended period of time, it is more of a concern and, in this work, often resulted in substrates becoming particularly brittle.

It would have also been instructive to have included test structure designs in the photomask that would have allowed for the assessment of properties of the deposited films- planar resonator structures, for example. Metallisation of TSVs smoothed by the oxidation and KOH wet etches followed by their measurement and comparison with unsmoothed TSVs would also be a useful investigation into the applicability of these processes to devices intended for quantum circuit applications. It is the author's belief that carrying through these processes would lead to TSVs of a higher quality that would be demonstrable using the characterisation techniques discussed in this thesis. More lofty goals such as the fabrication of the proposed TSV-integrated coupler and integration of TSVs into qubit fabrication processes could then be attempted and the myriad benefits of the 3D integration of quantum circuits could be demonstrated.

As a final word, the development of quantum computing, even in the short time span of this project, has been astounding and this speaks to the faith that has been put into this technology. It is impossible to make predictions with certainty as to the direction and speed that this research will follow, but it is clear that 3D integration has been a key part the development thus far and will, in future, continue to be crucial to the realisation of a truly scalable and useful quantum computer.

Appendices

Appendix A

Through-Silicon Via Fabrication Process

Etch-stop deposition:

1. Clean sample using acetone, methanol and IPA sequentially for 5min each in ultrasonic cleaner. Rinse for 5min with RO water and blow-dry with N_2.
2. Deposit 2um PECVD SiO2 on backside of wafer.

Bosch etch:

1. Clean sample using acetone, methanol and IPA sequentially for 5 mins each in ultrasonic cleaner. Rinse for 5min with RO water and blow-dry with N_2.
2. 1 min, 100W O2 ash in plasma asher.
3. Dehydration bake on vacuum hotplate for 5min at 190°C. Allow to cool for 3min.
4. Spin SPR220-7 at 3500rpm max. spin speed for 30s.
5. Wait at least 10min for solvent loss/relaxation.
6. Softbake on vacuum hotplate for 3min at 118°C. Transfer to 90°C hotplate for 30s. Remove and allow to cool completely on a watchglass.
7. 26s UV-light exposure on contact mask aligner.
8. Wait 45min for H_2O reabsorption (necessary for photoreaction).
9. Bake on hotplate for 3min at 118°C. Transfer to 90°C hotplate for 30s. Remove and allow to cool completely on a watchglass.
10. Develop with mild agitation in MF-CD-26 for 2 mins, then rinse for 5min in RO water. Blow-dry with N_2.
11. Bond wafer to 6" carrier wafer:
    - Heat Santovac 5(P) oil to 95°C.
    - Measure 75μl Santovac 5(P) using a pipette and place in the cetre of the carrier

wafer.

- Place sample on top of carrier
- Heat carrier and sample on hotplate for 2min at 80°C.

12. Perform Bosch etch using chosen parameters.

Post-etch:

1. Check etch depth on optical profilometer..
2. De-bond sample from carrier wafer by heating to 80°C on hotplate and gently sliding the sample off.
3. Remove any remaining photoresist and C_4F_8 polymer from TSV sidewalls by 10 min O_2 ash in plasma asher.
4. 20 min 6:1 BHF dip to remove SiO_2 etch-stop.
5. Check that etch-stop has been fully removed using ellipsometer.

Metallisation:

1. ALD of nitride film on topside of wafer using chosen parameters.
2. ALD of nitride film on backside of wafer using chosen parameters.

TiN etch frontside:

1. Clean sample using acetone, methanol and IPA sequentially for 5min each in ultrasonic cleaner. Rinse for 5min with RO water and blow-dry with N_2.
2. Dehydration bake on vacuum hotplate for 5min at 190°C.
3. Spin S1818 photoresist on topside of sample at 4000rpm max. spin speed for 60s.
4. Softbake on hotplate 135s @ 115°C. Allow to cool to room temperature on a watchglass.
5. 14s UV-light exposure on contact mask aligner.
6. Bake on hotplate 135s @ 115°C. Allow to cool to room temperature to avoid thermal shock in developer.
7. Develop with mild agitation in MF319 for 75s. Rinse in RO water for 5min and blow-dry with N_2.
8. Dry-etch using 10sccm CF_4 and 5sccm Ar in plasma etch tool for approximately 5min. Use interferometer to determine end point of the etch.

TiN etch backside:

1. Clean sample using acetone, methanol and IPA sequentially for 5min each in ultrasonic cleaner. Rinse for 5min with RO water and blow-dry with N_2.
2. Dehydration bake on vacuum hotplate for 5min at 190°C.

3. Spin S1818 photoresist on backside of sample at 4000rpm max. spin speed for 60s.
4. Softbake on hotplate 135s @ 115°C. Allow to cool to room temperature on a watchglass.
5. 14s UV-light exposure on contact mask aligner.
6. Bake on hotplate 135s @ 115°C. Allow to cool to room temperature to avoid thermal shock in developer.
7. Develop with mild agitation in MF319 for 75s. Rinse in RO water for 5min and blow-dry with N_2.
8. Dry-etch using 10sccm CF_4 and 5sccm Ar in plasma etch tool for approximately 5min. Use interferometer to determine end point of the etch.

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Ki becomes important transmission line parameter as the cross-section of a superconductor decreases. Electrode thickness < magnetic penetration depth => KI is enlarged and dominates magnetic inductance.
KI may be affected by heating, normal current injection and optical irradiation.
Paper gives analytical expression for KI/length of SCPW using conformal mapping. Temperature dependence of resonant frequency verify thisexpression. Can also use this measurenment

to obtain magnetic penetration depth.
2. Expressions for Transmission Line Parameter of Thin Superconducting Coplanar Waveguide:
Authors consider SCPW where centre conductor width < transmitted wavelength. This allows a quasi TEM mode to propagate. This is what allows the use of conformal mapping. Assume that the conductor can be modelled as perfect (B-field parallel to surface). Assume that film thickness is smaller than twice the magnetic penetration depth and that the current density is uniform across the thickness. Give KI fraction in eqs 1,2,3. Note that Lk is proportional to magnetic penetration depth squared.
3. Experimental:
They verify their expression by examining the temperature dependence of the resonance frequency, and hence KI, of a CPW resonator.
Magnetic penetration depth depends on temp, so Lk must depend on temperature. Lm changes slightly with temp becase the B-field penetrates through the thin electrode. But this dependence is much smaler than that for Lk, so it's neglected.
As the only temperature dependent variable in the expression for Lk is the magnetic penetration depth, they set out to find this dependence. Each superconductor will have a unique dependence, so they choose the BCS local limit of NbN for this work.
Measured the temperature dependence of resistivity of various sample of different dimensions using 4-point probe method.
They correct for resonance-frequency reducing effect of losses in the resonator, by considering the loaded q-factor.
4. Results:
Resonant frequencies are constant in the low temperature region and decrease quickly when temp approaches Tc.
Uniform current density assumption breaks down for 400nm thick films and leads to discrepancies in results.

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