Novel Surface Termination for Advanced Diamond Electronics

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Abstract

Diamond is an interesting semiconductor for high-power and high-frequency devices due to its ultra-wide bandgap, high carrier mobility, and superior thermal conductivity. However, traditional doping is limited by the deep energy levels of most impurities, which limit carrier activation at room temperature. As a consequence, despite its exceptional intrinsic properties, relatively few reproducible and high-performance diamond field-effect transistors have been reported in recent literature. This motivates the exploration of alternative doping strategies, such as hydrogen-terminated diamond with surface transfer doping.

Hydrogen-terminated diamond provides a conductive two-dimensional hole gas (2DHG) with low activation energy and relatively high carrier mobility, making it highly attractive for electronic devices. At the same time, the surface conductivity of H-diamond is highly sensitive to surface chemistry, oxide interfaces, and fabrication processes, posing significant challenges for achieving stable and controllable device operation.

In this work, different surface terminations have been explored for negative electron affinity (NEA) and positive electron affinity (PEA), to clarify their respective roles in enabling surface transfer doping or suppressing surface conductivity. Subsequently, the behaviour of different contact metals on H-diamond was examined, with emphasis on their ability to form reliable ohmic contacts. The influence of different oxide layers and deposition methods on H-diamond transfer doping was studied, revealing that thermal ALD HfO_2 can enhance the 2DHG by promoting transfer doping, whereas electron-beam–deposited Al_2O_3 with prior in-situ annealing effectively suppresses surface conductivity without degrading the hydrogen termination.

Building on these findings, accumulation-channel hydrogen-terminated diamond MOSFETs were successfully fabricated using an optimised and reproducible process flow. The devices exhibit normally-off, enhancement-mode operation with an I_{on}/I_{off} ratio of 10^7, achieving drain current densities exceeding 35 mA/mm at room temperature.

These results demonstrate a viable pathway towards stable and controllable diamond MOSFETs, addressing key technical barriers that have limited progress in the field. A stable and reproducible Au-based fabrication process was established for hydrogen-terminated diamond devices, providing a robust contact platform for the demonstrated enhancement-mode MOSFETs.

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Declaration

With the exception of chapters 1, 2 and 3, which contain introductory material, all work in this thesis was carried out by the author unless otherwise explicitly stated.

Associated Publications

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Conferences

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Contents

1. Introduction

Diamond, as a wide-bandgap semiconductor material (5.47 eV), enables the potential development of next-generation electronic devices. It has high carrier mobility (reported values for holes and electrons range between 2000-2250 $cm^2/V \cdot s$ and 2200-2750 $cm^2/V \cdot s$, respectively) [1.1], high saturation velocity (electrons: 2.7×10^7 cm/s and holes: 1.1×10^7 cm/s), high thermal conductivity (up to 22 W/cm·K), high breakdown voltage (10 MV/cm), as well as remarkable chemical inertness and radiation hardness [1.1,1.2]. These properties potentially enable diamond material to maintain stable operation under extreme conditions of high voltage, high power, and high temperature [1.3].

The development of diamond substrates for electronics is limited by the high resistivity, and the strong O-bonding between adjacent carbon atoms in the diamond lattice makes traditional doping of diamond complicated, requiring alternative processes [1.4]. High-energy ion implantation is a strategy frequently employed to induce substitutional doping in the diamond lattice; however, this often results in the graphitisation of the diamond surface and causes extensive lattice damage [1.5]. It is important to note that although high boron doping concentrations can achieve lower resistivity, high doping concentration can reduce mobility substantially (down to 1 to 10 $cm^2/(V \cdot s)$). Additionally, more surface states are created on the diamond surface by oxygen termination after strong acid cleaning or partial gate oxide coverage, which reduces the expected control effect of the applied electric field on carrier charge in the device channel.

Surface transfer doping provides an alternative doping strategy to traditional doping of diamond [1.6]. Prior work in the ASMaD (Advanced Semiconductor Materials and Devices) group at the University of Glasgow has successfully applied surface transfer doping of diamond, enabled by the hydrogen-terminated diamond surface, to induce p-type conductivity [1.7-1.9]. Basically, a suitable surface termination can change the surface dipole sufficiently to raise the conduction band minimum (CBM) above the vacuum energy level (E_{vac}), which can induce upward band-bending at the material interface and give rise to a negative electron affinity (NEA is -1.3eV) [1.10]. The net transfer of electrons from the surface to an adsorbed surface electron acceptor material results in p-type surface conductivity due to the formation of a subsurface hole accumulation layer, which is a two-dimensional hole gas (2DHG). In contrast, oxygen termination tends to increase in work function, resulting in positive electron affinity (PEA is 1.7eV) [1.11], where additional energy is needed to remove electrons from the surface.

Despite the significant progress achieved in hydrogen-terminated diamond and transfer-doped diamond devices, several key challenges remain. In particular, the reliable and reproducible control of surface conductivity and gate modulation is still strongly dependent

on surface termination stability, oxide selection, interface quality, and processing conditions. Variations in oxide deposition methods and pre-deposition treatments can significantly influence the interfacial electronic properties, often leading to instability of the 2DHG and inconsistent device performance. These limitations hinder the realisation of robust enhancement-mode diamond MOSFETs suitable for scalable electronic applications.

Building on the challenges outlined above, while hydrogen-terminated diamond MOSFETs and transfer-doped diamond devices have been widely reported, the original contribution of this thesis lies in the optimisation of the accumulation-channel hydrogen-terminated diamond MOSFET design through oxide engineering, with a particular focus on the role of oxide deposition method and pre-deposition treatment.

Specifically, this work demonstrates that a pre-annealed single-layer oxide can provide improved electrostatic control and interface stability compared with conventional electron-beam-evaporated Al_2O_3 and atomic-layer-deposited (ALD) Al_2O_3 gate dielectrics. By decoupling oxide-induced interface effects from hydrogen termination stability, this approach enables effective suppression and re-accumulation of the 2DHG without degrading the surface chemistry.

In addition, this thesis provides a comparative experimental framework linking surface termination, oxide-induced transfer doping modulation, contact resistance, and carrier mobility extraction using de-embedded electrical methods, including the transmission line method (TLM) and split C–V analysis. These results offer practical design guidelines for achieving enhancement-mode operation and improved performance consistency in diamond MOSFETs, contributing to the development of scalable diamond-based electronic devices.

The aim of this thesis is to investigate and optimise hydrogen-terminated diamond-based electronic devices by controlling surface transfer doping, oxide–diamond interfaces, and metal contacts, to enable stable accumulation-channel enhancement-mode diamond MOSFET operation.

This thesis starts with a summary of the fundamental properties of diamond in Chapter 2, followed by Chapter 3, which reviews the development of transfer-doped diamond devices and establishes the background for this research.

Chapter 4 describes in detail the fabrication processes developed for diamond devices, including sample preparation, lithography, metallisation, oxide deposition, and different surface treatments. Chapter 5 introduces the electrical characterisation techniques and associated equipment technologies, with a particular emphasis on the principles of Hall effect measurements, the transmission line method, as well as the electrical characterisation of diamond devices.

Building on this foundation, Chapter 6 investigates the performance of different surface terminations, including hydrogen, oxygen, fluorine, and selected metal terminations, in modulating transfer doping and surface conductivity. Furthermore, the role of various oxide layers on H-diamond is examined, showing that certain oxides can enhance transfer doping. In contrast, electron-beam-evaporated Al_2O_3 can suppress the 2DHG without damaging the hydrogen termination.

Chapter 7 focuses on the challenge of forming reliable ohmic contacts on H-diamond, which is essential for reducing contact resistance and enabling high-performance devices. Both as-deposited contacts and annealed metal carbides are investigated as stable ohmic contacts.

Chapter 8 reports the fabrication process and electrical characterisation of accumulation-channel enhancement mode hydrogen-terminated diamond MOSFETs. Devices' transfer and output characteristics are analysed to understand the devices' behaviour. The Split C-V method is used to extract the carrier mobility and concentration.

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2. Background: Diamond material theory

Diamond, an ultra-wide band gap semiconductor material (5.47eV), has many properties that make it an interesting candidate for electronic material applications. The focus of this chapter is to introduce the physics behind diamond as a potential electronic material. Firstly, starting from the structure of the carbon atom and the crystal lattice structure of diamond, the properties of diamond materials are introduced and compared with other semiconductor materials. The synthetic growth methods for diamond are briefly introduced. Next, the methods of diamond doping are discussed, and the challenges of diamond material doping are summarised. The surface transfer doping mechanism of diamond is proposed, which is the most critical technology used in this work. Finally, this chapter covers the physics analysis of metal-semiconductor and metal-oxide-semiconductor interfaces, which are useful for producing field-effect transistors.

2.1 Diamond structure and characteristics

Carbon exists in many forms in nature, and carbon with different structures exhibits distinctive characteristics. The form carbon adopts is determined by the bonding configuration of individual carbon atoms with their neighbouring atoms. The atomic number of carbon is 6, and the carbon atom has electrons in a $(1s)^2\ (2s)^2(2p)^2$orbital configuration and can have up to 4 covalent bonds [2.1]. The carbon atom has two unpaired electrons in its outer shell, which are used for bonding; however, orbital hybridisation of the 2s and 2p orbitals can occur. The bonding ability of four electrons can be detected in the 2p state, so it is easy to excite an electron from the 2s state to the 2p state. In the presence of an external disturbance, such as a disturbance with hydrogen nearby, the energy difference can be overcome [2.2]. This results in four new hybrid orbitals consisting of one S orbital and three p orbitals. Sp^3 bonded carbon forms a diamond lattice configuration in which each carbon atom has a tetrahedral configuration with bond lengths of 1.54 Å and a bond angle of 109.5° [2.3]. The schematic diagram of the diamond lattice structure is shown in Figure 2.1.1 [2.4].

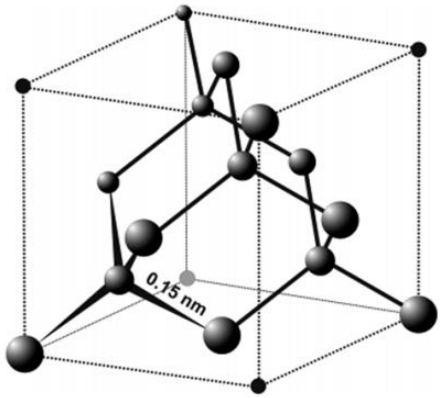

Figure 2.1.1 The schematic diagram of the lattice structure of diamond [2.4].

Diamond exhibits three principal crystal face orientations, namely (100), (110), and (111), as shown in Figure 2.1.2 [2.5]. Diamond surfaces with (001) and (100) represent equivalent crystal orientations in diamond, resulting in identical structural arrangements and properties. Diamonds with the (100) crystal orientation offer the lowest cutting difficulty and minimal surface roughness, making it advantageous for mechanical processing and device fabrication. In chemical vapour deposition (CVD) of diamond, the (100) surface is the most commonly used orientation, as it enables large-area epitaxial growth with uniform morphology [2.6].

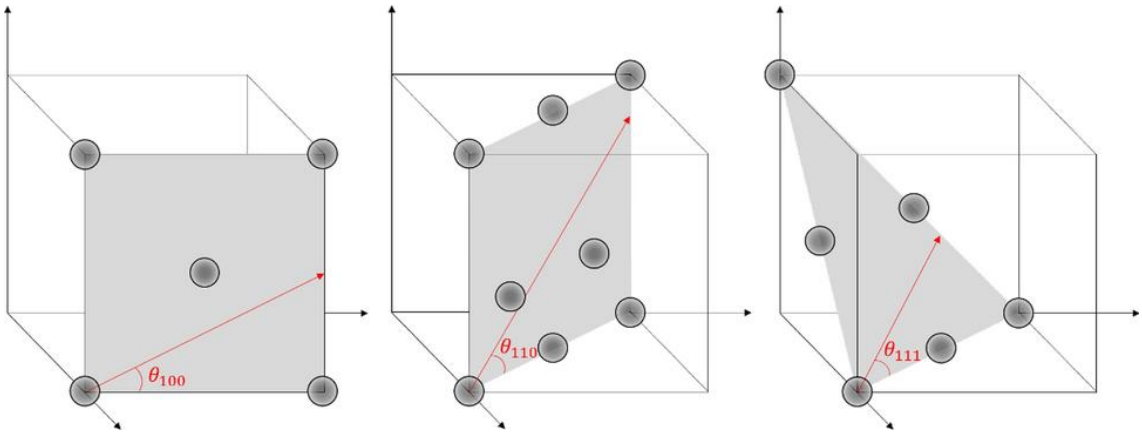

Figure 2.1.2 Diamond crystal face orientations with (100), (110), and (111) [2.5].

The arrangement of C atoms in the diamond structure is highly symmetrical, with each C atom at the centre of a regular tetrahedron, and the other four C atoms that bond with it are at the four vertices of the regular tetrahedron. In this case, all valence electrons around the C atom of the diamond are involved in bonding, and there are no excess free electrons. Therefore, diamond has the characteristics of high hardness.

Graphite is another allotrope of carbon. Unlike diamond, covalent bonds are formed between C atoms in graphite crystals in the form of sp^2 hybridisation. The sp^2 bonding of

carbon atoms gives rise to graphene formation, where each carbon atom is bound to its three nearest neighbours. Graphene is conductive because it has one remaining electron, which does not participate in bonding with other carbon atoms. Graphite has two-dimensional planar layers of benzenoid rings whose carbon atoms are 1.42 Å apart with bond angles of 120°; the interlayer distance is 3.35 Å [2.7]. Hence, the difference in the structure of hybrid orbitals is one of the main reasons for the huge difference in the electrical properties of diamond and graphite. Under certain conditions, the sp^3 hybridised bonds in diamond can transform into sp^2 bonds, leading to graphitisation. For example, direct heating of the (111) surface above 1373 K in vacuum leading to several graphene layers parallel to the surface, while annealing in vacuum at 1073 K for 5 min with a sputtered Ni film can induce the same transformation at a much lower temperature [2.8,2.9]

Diamond has very low phonon scattering due to its stiffness and short bond length, which, together with the periodicity of the diamond lattice, contribute to the quick movement of the phonons through the material. This results in diamond having the highest thermal conductivity of any three-dimensional material, up to 24 W/(m·K) [2.10], allowing for efficient heat dissipation during device operation.

The bandgap of diamond is related to its lattice structure as well. Diamond has a wide bandgap due to its tightly packed lattice of carbon atoms arranged in a tetrahedral crystal structure. This lattice configuration creates a large energy gap between the valence band, where electrons are bound to atoms, and the conduction band, where electrons can move freely. The strong covalent bonds between carbon atoms in the diamond lattice require a significant amount of energy to break, resulting in a large bandgap (5.47eV) [2.11].

The breakdown electric field of diamond, which is from impact ionisation and subsequent avalanche breakdown, exhibits the highest predicted breakdown electric field of semiconductors, with values in the range of 5–10 MV/cm [2.12]. A high electric breakdown field is desirable because it allows the device to sustain higher voltages for a given layer thickness. Conversely, for a targeted breakdown voltage, thinner layers and more compact device geometries can be realised, which is advantageous for power device integration.

In high electric fields, the maximum velocity carriers are limited because carriers lose energy to the crystal lattice by emission of optical phonons, as well as other scattering events. Therefore, high optical phonon energies tend to give a high saturation carrier velocity. Diamond has the highest optical phonon energy (≈160 meV) among

semiconductors, corresponding to the zone-centre (Γ-point, k = 0) optical phonon mode [2.9]. The saturation velocity of holes and electrons is 0.85–1.2 × 10^7 cm/s and 1.5–2.7 × 10^7 cm/s respectively [2.11].

Diamond exhibits both high electron and hole mobilities at room temperature, which is immensely attractive. The highest electron and hole mobilities of about 4500 $cm^2/(V{\cdot}s)$ and 3800 $cm^2/(V{\cdot}s)$ have been reported, respectively [2.11]. However, most of the measured mobilities for diamond investigated are in the range 2000–2250 $cm^2/(V{\cdot}s)$ for holes and 2200–2750 $cm^2/(V{\cdot}s)$ for electrons [2.13]. The potential of diamond is obvious by comparing its properties with those of competing wide band gap materials for high-frequency and high-power electronic device applications. The intrinsic material properties of diamond compared to other semiconductors are shown in Table 2.1.1 [2.11,2.14].

		Si	4H-SiC	GaN	Ga_2O_3	Diamond
Bandgap E_g $[eV]$		1.10	3.20	3.45	4.9	5.47
Saturation velocity v_S [×10^7 cm/s]	Electron	1.1	1.9	2.5	2	2.7
	Hole	0.8	1.2	-	-	1.2
Carrier mobility μ [$cm^2/(V{\cdot}s)$]	Electron	1500	1000	1500	300	2750
	Hole	450	120	200	-	2250
Breakdown field E_{Max} [MV/cm]		0.3	2.8	5	8	5-10
Dielectric constant ε_r		11.9	9.66	8.9	9.93	5.7
Thermal conductivity λ [W/(cm·K)]		1.5	4.9	1.3	0.23	22

Table 2.1.1 The intrinsic material properties of diamond compared to other common semiconductors.

As listed in Table 2.1.1, diamond exhibits comparable electron and hole mobilities primarily due to its highly symmetric crystal structure and strong sp^3 covalent bonding. The conduction and valence bands of diamond both originate from carbon sp^3 hybridised orbitals, resulting in relatively similar band curvature and effective masses for electrons and holes. In addition, the wide bandgap and strong covalent bonding lead to high phonon energies, which suppress phonon scattering at room temperature. As a result, both electrons and holes experience similarly weak lattice scattering, allowing high mobilities for both carrier types. This contrasts with many conventional semiconductors, where asymmetry between the conduction and valence band structures leads to significantly lower hole mobility compared to electron mobility.

2.2 Synthetic diamond

Before the advent of synthetic diamond production, acquiring diamonds was restricted to natural diamond mines. However, natural diamond reserves are finite, rendering their extraction challenging and costly. These limitations constrain the ability to meet the demands of large-scale industrial production and growing market needs. Consequently, significant research efforts have been directed toward developing synthetic diamond growth methods.

So far, high temperature and high pressure (HTHP) and Chemical Vapour Deposition (CVD) are two primary methods to grow diamond. The HTHP method was first developed by Bundy et al. at GE in 1955 [2.15]. This process, which often employs the temperature gradient method, has been widely employed in the production of Type I_b (containing isolated nitrogen atoms), Type II_a (nitrogen-free, high-purity), and Type II_b (boron-doped, electrically conductive) single crystals. The pressures and temperatures required for this process are typically around 5 to 6.5 GPa and 1300 to 1700°C [2.15]. When a diamond is synthesised by the HPHT method, the diamond is in the atmospheric environment, and the vast majority of the air is nitrogen. This results in HPHT diamonds containing large amounts of N impurities, which are usually yellow [2.5]. Limited by the quality of the crystal, HPHT diamond is not preferred for direct device fabrication. However, with the continuous improvement of HTHP technology, the concentration of impurities is gradually decreasing, which is enhancing the feasibility of using HTHP diamonds in device fabrication.

CVD is another growth method developed after the success of HTHP diamonds. Early work by Soviet research groups synthesised it from pure CH_4 at pressures of 13 to 40Pa and temperatures from 950 to 1050 °C [2.5]. The main principle of the CVD diamond process is to inhibit the growth of graphite through a mixture of H_2 and CH_4 or other hydrocarbon gases. In addition to providing CH_x free radicals in the reaction gas, the hydrogen atoms are also highly reactive with sp^2 carbon and maintain the sp^3 structure of the diamond. The etching rate of graphite by a hydrogen atom is much higher than that of diamond, which significantly improves the growth rate and growth quality of diamond.

Diamond CVD growth methods are generally classified into two types according to the excitation method: thermal CVD and plasma-enhanced CVD (PECVD). Different from the heating gas method, plasma can be produced by various forms of electrical discharge or induction heating. The plasma can produce hydrogen atoms for the reaction process and the appropriate carbon precursors for the growth of the diamond. Under the

discharge and exothermic action of the plasma, hydrogen molecules (H_2) are dissociated into atomic hydrogen mainly through electron impact. Although the H-H bond energy is 4.5eV, the mass difference between the electron and the hydrogen molecule results in less electron kinetic energy being transferred. Consequently, more than 9.5eV of electron energy is required for effective dissociation. The dissociation of hydrogen molecules reaches its peak at an electron energy of 25eV [2.16]. Therefore, atomic hydrogen produced in plasma usually has a higher kinetic energy compared to the thermal-assisted CVD process. In a typical plasma, about 1% of molecules are converted into neutral radicals and about 0.01% into ions. Neutral molecules such as CH_4 require high Gibbs free energy for decomposition and therefore contribute little directly to diamond growth. Consequently, the growth rate of a diamond film in PECVD is primarily determined by the concentration of neutral free radicals [2.5]

The CVD single-crystal diamond samples, which have been used in this project, were procured commercially from Element Six. Figure 2.2.1 shows 4.7mm x 4.7mm x 0.5 mm example single-crystal diamond substrates.

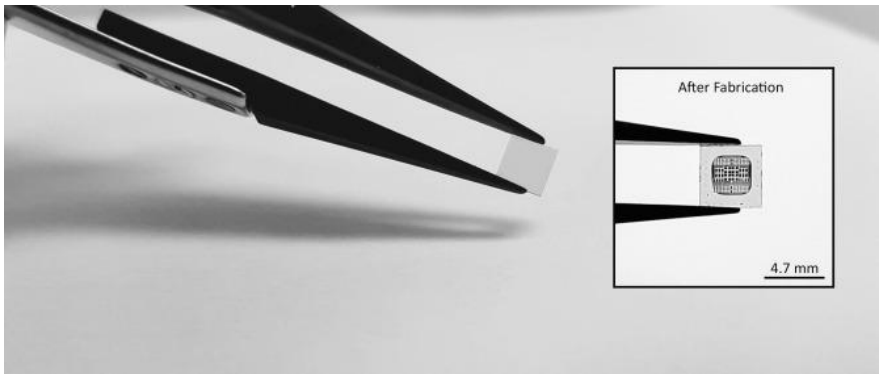

Figure 2.2.1 Single-crystal CVD diamond substrates before and after fabrication [2.19].

2.3 Doping diamond

Since intrinsic diamond is an electrical insulator, *enabling and controlling its electrical conductivity* is a prerequisite for developing diamond-based electronic devices. To enhance the density of mobile charge carriers in semiconducting material, doping is typically utilised. This process introduces additional charge carriers into the lattice of the material, usually by introducing impurity atoms. For n-type doping, these impurities can contribute an additional electron to the lattice, whereby the Fermi level will shift towards the conduction band. For p-type doping, these impurities will accept an electron from the lattice, thereby generating an additional hole and moving the Fermi level towards the valence band. Basically, these impurity atoms replace intrinsic atoms in the lattice. Doping methods include ion implantation, diffusion and growth during CVD. In ion

implantation, ions of the desired dopant are accelerated to high energies and implanted into the semiconductor material. This method offers relatively good lateral control of dopant placement via masking and beam focusing. However, achieving precise vertical control of the dopant depth profile is challenging. In diffusion doping, dopant atoms are introduced to the surface of the semiconductor material and allowed to diffuse into the crystal lattice through high-temperature annealing. This method is effective for introducing dopants uniformly throughout the material, but it also leads to the difficulty of high-concentration doping. In in-situ CVD doping, dopant-containing precursors are introduced together with carbon precursors during growth, enabling dopants to be incorporated directly into the lattice.

However, due to the strong tightness of C bonding in diamond, it is difficult to introduce impurities into the diamond crystal under conditions which will make them act as donors or acceptors. Ion-implantation is complicated in the case of diamond by bond breakage during the slowing-down process of the implanted ions, resulting in the formation of point defects and defect complexes that are difficult to remove by post-implantation annealing [2.17]. In most cases, the unannealed defects can introduce electrical conduction that is unrelated to the electrical activation of an implanted potential dopant. Besides, doping during growth permits the introduction of the desired impurities into the growing diamond. For the case of CVD diamond growth, this is achieved by including the required dopant atoms (in a suitable molecular form) into the growth gas mixture. This method has been successfully applied for the introduction of Nitrogen (N), Boron (B), and Phosphorus (P) into diamond. Figure 2.3.1 shows the main dopant impurities of diamond and their corresponding impurity levels.

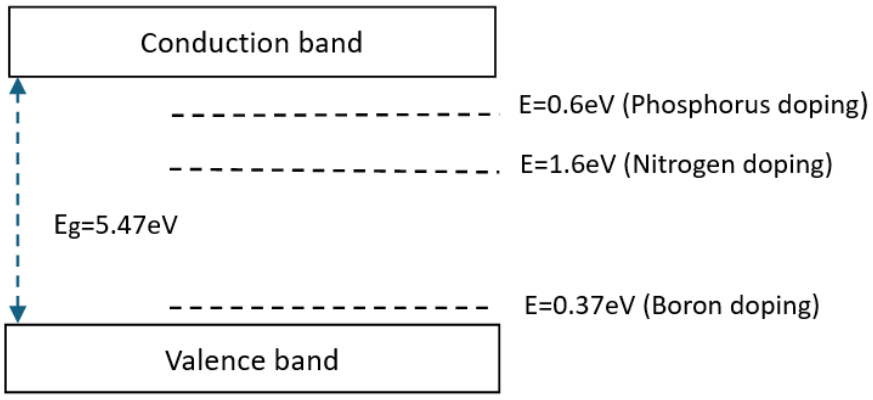

Figure 2.3.1 Common donor and acceptor energy levels represented within the diamond bandgap.

Natural diamonds sometimes contain B introduced during the geological formation of the crystal. Therefore, B can be introduced as part of the gas phase during growth via CVD, which will produce boron-doped polycrystalline or single-crystal diamond material. The doping of diamond by the introduction of B into substitutional sites by the abovementioned techniques has been achieved in the laboratory and widely used as a dopant for obtaining p-type diamond. Figure 2.3.2 shows the activation energy of the conductivity as a function of doping concentration room temperature resistivity as a function of doping concentration [2.18].

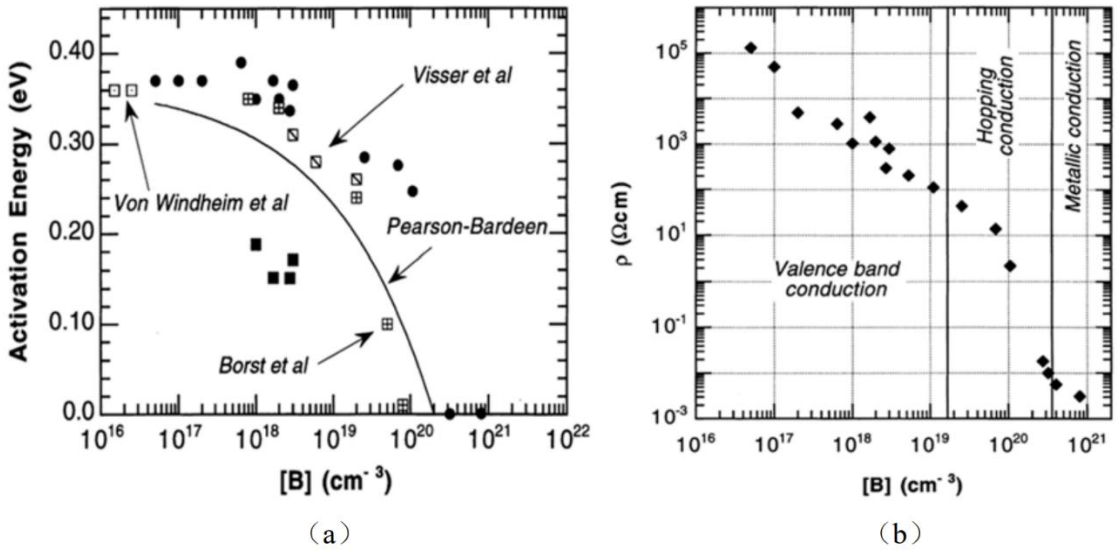

Figure 2.3.2 The relationship of Boron doping concentration and (a) activation energy, (b) room temperature resistivity [2.18].

This B doping renders the diamond conductive, with a relatively deep acceptor level with an activation energy of 0.37 eV [2.17]. The high activation energy results in a B activation rate of less than 0.1% at room temperature, so the resistivity of B-doped diamond is relatively high for low doping concentrations. With the increase of B concentration and temperature, hole mobility has been shown to decrease significantly, which also leads to the poor temperature stability of diamond devices using B-doped diamond as conductive channels [2.19]. When the concentration of B is lower than 10^{19} cm^{-3}, the working mechanism is valence band conduction. As the concentration of boron increases, the wavefunctions of neighbouring acceptor states begin to overlap. Instead of electrons being excited to the conduction band, hole transport occurs via hopping between boron atoms, giving rise to hopping conduction [2.20]. At this time, the impurity conductance dominates, and the resistivity continues to decline. When the B concentration is increased to more than 10^{20} cm^{-3}, the diamond becomes a degenerate semiconductor,

showing metal conductivity and superconductivity at room temperature and cryogenic temperatures, respectively [2.20].

A potential solution proposed to the issue of reduced mobility is delta doping [2.21]. Delta doping has been explored to alleviate the decline in mobility associated with increased dopant concentration by forming a thin (several nanometres), highly boron-doped (≥ $5\times10^{20}cm^{-3}$) layer between two intrinsic layers in diamond. As a result, carriers form a two-dimensional gas in the plane of the delta layer, the latter playing the role of a quantum well for them. A significant amount of carriers, therefore, reside in dopant-free material. As a result, carrier mobility may be enhanced in comparison with homogeneous doping [2.22]. At the same time, high-energy boron doping techniques, such as ion implantation, can also cause extensive damage to the diamond crystal lattice, thereby reducing the substrate quality and hindering the manufacture of devices.

In many semiconductors, n-type doping is generally associated with higher mobilities than p-type doping due to the lower effective mass of electrons compared with holes. In diamond, however, electron and hole mobilities are relatively comparable, so the motivation for achieving n-type doping lies primarily in enabling complementary doping schemes that allow the fabrication of bipolar devices. Unfortunately, realising stable and efficient n-type doping in diamond remains much more challenging than p-type doping. The exceptionally strong carbon–carbon bonding prevents conventional thermal diffusion methods, while the small lattice constant and short atomic spacing make it difficult to recover implantation-induced damage. Moreover, apart from nitrogen, most potential donor atoms have a significantly larger atomic radius than carbon, hindering their incorporation into substitutional lattice sites.

For n-type dopants like phosphorus and nitrogen, the activation energies are 0.6eV and 1.6eV, respectively [2.23]. Nitrogen is commonly found in natural diamonds in varying concentrations, either as isolated substitutional atoms replacing carbon in the lattice or as aggregated complexes. The impurity level of nitrogen in diamond is relatively deep, located about 1.6 eV below the conduction band minimum. This means that only a small fraction of electrons can be thermally excited into the conduction band at room temperature.

Phosphorous-doped diamond shows n-type conductivity with a donor level 0.6eV below the conduction band. Similarly, the activation energy is so large that the carrier concentration at room temperature is typically limited to $10^{11}cm^{-3}$ [2.20]. One difficulty is that the phosphorus incorporation is obtained only on (111) oriented surfaces of diamond crystals, and the homoepitaxy on such substrates requires unusual growth

conditions, low methane concentration (0.1%) and high temperature (900 °C) [2.24]. Moreover, because of the high ionisation energy of phosphorus, the carrier concentration in the conduction band is very low and the resistivity very high.

Beyond these, n-type doping with Sulphur, a group VI element, has been reported but is still controversial [2.17]. The first report that sulphur incorporated during CVD growth in diamond shows a shallower donor level (0.37 eV) and exhibits good room temperature electron mobility (600 $cm^2/(V \cdot s)$) [2.25]. The possible cause of n-type conduction is the co-doping effect that occurs when S and B are present together in the diamond crystal as donors.

In summary, the implementation of bulk-doped diamond channels for high-performance power devices is still facing challenges. For p-type material, boron doping can provide high conductivity at sufficiently high concentrations, but it also reduces carrier mobility. In contrast, potential n-type dopants such as nitrogen or phosphorus exhibit low ionisation efficiency at room temperature, resulting in extremely low carrier densities. These limitations highlight the difficulty of achieving simultaneously high conductivity and stable performance in bulk-doped diamond.

2.4 Surface termination and surface transfer doping of diamond

As an alternative to traditional bulk doping methods, surface transfer doping provides a non-destructive method for inducing charge carriers in the near-surface region of diamond. This relies on electron exchange between a semiconductor and dopants on its surface and is referred to as surface transfer doping. The transfer doping mechanism mainly considers that molecular adsorbents in the air play the role of the electron acceptor and on hydrogen-terminated diamond causes the surface band bending, and a two-dimensional hole gas (2DHG) appears [2.26].

Different chemical surface terminations of diamond result in distinct energy band structures. Figure 2.4.1 shows the surface atomic distribution diagrams of diamond surface, hydrogen-terminated diamond surface and oxygen-terminated diamond surface, as well as the corresponding energy band diagrams, are shown [2.27].

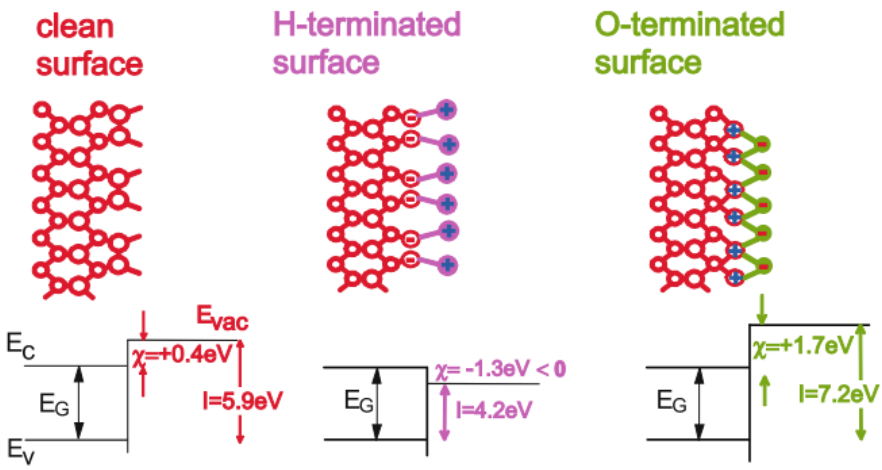

Figure 2.4.1 The surface atomic distribution diagram of diamond surface, hydrogen-terminated diamond surface and oxygen-terminated diamond surface and corresponding energy band diagrams [2.27].

The intrinsic carrier concentration in undoped diamond at room temperature is almost negligible. However, as mentioned in section 2.2, CVD diamond typically results in films with hydrogen-terminated surfaces after being treated by hydrogen plasma, and then the diamond surface shows good conductivity. Hydrogen termination is usually stable at room temperature in normal atmospheric conditions. However, the hydrogen termination can be removed by strong acids or by exposing the surface to high temperatures (above 230°C) in a normal atmosphere [2.28]. In these cases, the hydrogen is usually replaced with oxygen from the atmosphere, leading to an oxygen-terminated surface.

A clean non-terminated diamond surface in vacuum has an ionisation potential (IP) of 5.9 eV, this being the energy required to remove an electron from the valence shell of an atom and ionise it [2.27]. Electron affinity (χ) is used to characterise the energy range of a semiconductor material from the bottom level of the conduction band to the vacuum level, as shown in formula 2.1.

$$\chi = E_{vac} - E_c \tag{2.1}$$

where E_{vac} means the vacuum level, and E_C means the bottom level of the conduction band. Negative electron affinity (NEA) means that the bottom energy level of the conduction band of the semiconductor material is higher than the vacuum level. When the electrons are motivated to the conduction band, the electrons can easily escape to the vacuum. If EA is positive, the electrons in the conduction band can only be motivated to the vacuum level by absorbing a certain amount of energy. For a clean non-terminated diamond surface, EA is +0.4 eV, this being the energy required to remove one electron

from the conduction band [2.27]. Oxygen termination increases the EA of the diamond surface to ~1.7eV. Hydrogen termination results in the EA becoming negative decreasing to -1.3eV.

For hydrogen termination, in general, to act as an acceptor, the adsorbed substance must have an unoccupied electron energy level lower than the diamond valence band. As mentioned, H-terminated diamond has -1.3eV NEA, so the lower limit of the electron affinity energy of the adsorbed is required to be 4.2eV (the sum of diamond band gap and electron affinity energy).

Takagi et al. investigated the electronic structures of H-terminated diamond with (100) surface by the adsorption of NO_2 and H_2O. Hole carriers are generated through electron transfer from the H-terminated diamond to the physically adsorbed molecules. The extent of this electron transfer is primarily determined by the energy offset between the valence band maximum (VBM) of the H-terminated diamond and the unoccupied molecular orbital levels of the adsorbates. A lower unoccupied molecular orbital energy level results in greater electron transfer. Figure 2.4.2 shows the schematic diagram of the transfer doping process at the hydrogen-terminated diamond surface and the adsorbate molecule.

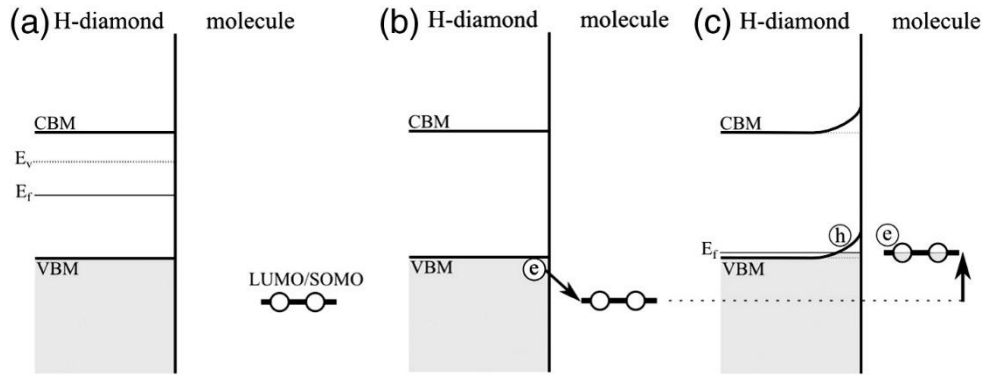

Figure 2.4.2 The schematic diagram of the transfer doping process at the hydrogen-terminated diamond surface and adsorbate molecules [2.28].

In general, the effective surface transfer doping of diamond has to meet two prerequisites. First, for p-type doping, the lowest unoccupied molecular orbital (LUMO) of the adsorbate must lie close to or below the semiconductor VBM; for n-type doping, the highest occupied molecular orbital (HOMO) of the adsorbate must be close to or above the semiconductor conduction band minimum (CBM). Second, the excess holes or electrons generated by interfacial charge transfer must be delocalised in the near-surface region and able to move parallel to the surface to serve as effective charge carriers.

The delocalisation of carriers generated from the valence band maximum (VBM) arises from the intrinsic band nature of diamond rather than from localised molecular states. When electrons are transferred from the VBM of hydrogen-terminated diamond to acceptor adsorbates, the remaining holes reside in extended valence-band states of diamond. These holes are therefore delocalised within the diamond lattice and are free to move parallel to the surface. The interfacial charge transfer induces an electrostatic potential that bends the bands upward near the surface, confining these delocalised valence-band holes within a narrow near-surface region. As a result, a two-dimensional hole gas (2DHG) is formed, in which carrier motion is restricted perpendicular to the surface but remains delocalised and conductive in the lateral direction.

Under the electric field generated by interfacial charge separation, these carriers are confined in the direction perpendicular to the interface, forming a narrow space-charge layer with a thickness of several nanometres [2.24]. However, it is important to note that while holes on the diamond surface are generally mobile and conductive, the electrons transferred to the acceptor material are not necessarily mobile, depending on its band structure and defect states.

However, the hydrogen termination is not stable under certain conditions, particularly at elevated temperatures. At room temperature in ambient air, H-terminated diamond supports a two-dimensional hole gas (2DHG) with typical sheet carrier densities of 10^{12}–10^{13} cm^{-2}, mobilities of 50–200 $cm^2/(V \cdot s)$, and sheet resistances ranging from a few to several tens of kΩ/□, depending on surface preparation and measurement conditions [2.26]. Hydrogen termination can be readily replaced by oxygen, which eliminates the surface conductivity, suppresses interfacial charge transfer, and ultimately shifts the surface polarity towards a positive electron affinity (PEA). Oxidation of diamond can be induced by a variety of processes, including O_2 plasma exposure, UV–ozone treatment in air, strong acid treatment, thermal annealing in air, or electrochemical oxidation [2.30].

2.5 Electron acceptors on H-diamond

The reliance on air-borne acceptor species and the sensitivity of the H-diamond surface to the ambient environment, however, remains a significant limiting factor in the development of surface transfer-doped diamond electronic devices. Factors such as surface morphology, uniformity of hydrogen termination, surface contamination, composition of naturally occurring atmospheric adsorbates, and variations in substrate quality can all affect device performance.

To address the limitations associated with the choice of electron acceptor layers, a variety of alternative surface acceptor materials have been investigated. Organic molecular acceptors, such as the fullerene molecule C_{60}, its fluorinated derivative $C_{60}F_{48}$, and F4-TCNQ [2.31], have been demonstrated to induce surface transfer doping on H-terminated diamond. In addition, high electron affinity oxides, including V_2O_5 and MoO_3, are highly effective in generating a two-dimensional hole gas (2DHG) at the H-diamond surface [2.32, 2.33]. When brought into contact with the diamond surface, these oxides produce hole densities significantly higher than those obtained from simple exposure to ambient air. The following section will discuss in more detail the mechanisms by which both molecular species and metal oxides act as electron acceptors on hydrogen-terminated diamond.

Strobel demonstrated that p-type surface doping of diamond could also be achieved with fullerene (C60) and fluorinated fullerenes (FFs, $C_{60}F_x$, x = 18, 36, 48) as surface acceptors, where doping is achieved by the transfer of an electron to the LUMO of $C_{60}F_x$ [2.34,2.35]. The model for surface transfer doping of hydrogen-terminated diamond by molecular fullerene adsorbates is shown in Figure 2.5.1.

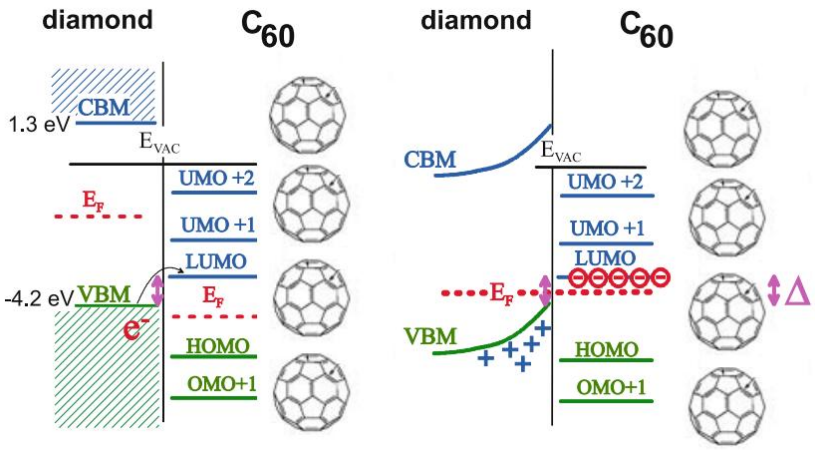

Figure 2.5.1 Illustration of the surface transfer doping of H-diamond by fullerene molecules [2.27].

The alignment of the energy levels of the fullerene surface acceptors with those of the diamond has a characteristic activation energy *ΔE* for electrons to be excited from the diamond to the adsorbate system. This activation energy plays for the surface transfer doping process the role that the acceptor ionisation energy has in the conventional bulk doping mechanism. Under the non-equilibrium situation, the Fermi levels of the diamond and the adsorbate layer deviate. As soon as contact is allowed, electrons will flow from the diamond side to the adsorbate side until the Fermi levels are equalised. The EA of C_{60} is 2.7eV [2.36]. However, it is still lower than the 4.2eV threshold. The introduction of

the strongly electronegative fluorine atoms induces a large electron affinity in the fluorinated fullerenes, allowing an electron-hole pair for each $C_{60}F_x$ acceptor. With increasing fullerene coverage, ΔE decreases, and the C_{60} electron affinity increases by 1.3 eV and reaches a saturation value for coverages exceeding 3–4 monolayers, which means the EA increases by 1.3 eV when going from a single C_{60} molecule to a C_{60} solid [2.34]. And the EA of FFs increases with fluorination and reaches 4eV for $C_{60}F_{48}$ as the highest fluorinated species synthesised so far [2.37]. Unfortunately, fullerene molecules lack thermal stability on diamond surfaces [2.38], so the encapsulation and passivation of fullerene doping layers on H-diamond would be mandatory for an electronic application in field effect transistors (FETs).

The EA of isolated F_4-TCNQ molecules is around 4.4 eV, which still matches the ionisation potential of hydrogenated diamond, thereby allowing surface transfer doping [2.31]. Furthermore, the existence of anion molecular species, as well as the gap states associated with partially occupied LUMO, suggests significant charge transfer to F_4-TCNQ. Summary of the reported empirical conductivity of various molecular species on H-diamond is shown in Figure 2.5.2.

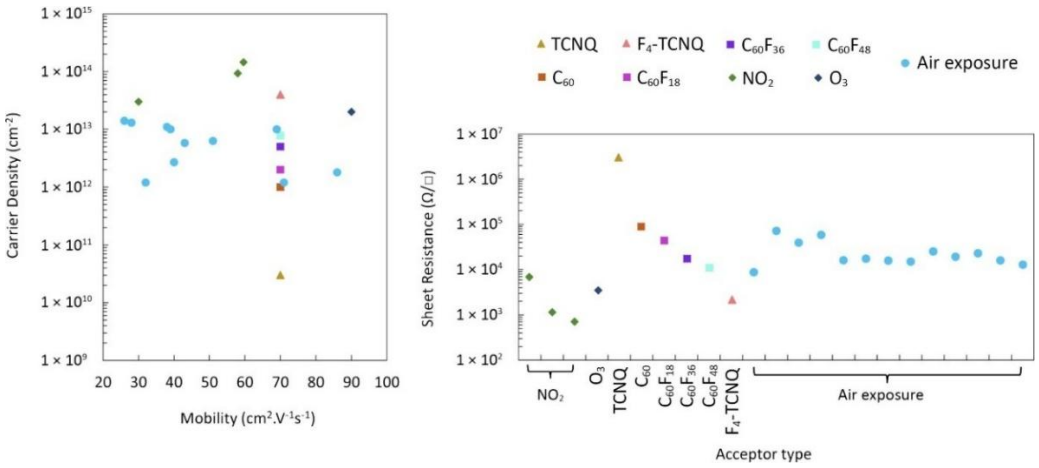

Figure 2.5.2 Summary of the reported empirical conductivity of various molecular species on H-diamond [2.19].

To enhance the stability of surface conductivity in hydrogen-terminated diamond, various solid encapsulation materials have been investigated as an alternative to these molecular species, with metal oxides being the most commonly studied. The influence of oxides on the transfer doping of H-diamond, as one of the focuses of this study, will be discussed in further detail in Sections 3.1 and 6.2.

2.6 Metal-Semiconductor interface

To utilise semiconductor materials in electronic device applications, it is essential to understand the nature of the metal–semiconductor interface, as the electronic properties of the contact strongly influence device performance. When a metal film is brought into direct contact with a semiconductor, charge transfer occurs until the Fermi levels on both sides align, resulting in energy band bending at the interface. In this study, hydrogen-terminated diamond behaves as a p-type semiconductor, therefore, only p-type metal–semiconductor interfaces are considered here.

Due to the low density of surface pinning states, hydrogen-terminated diamond approximately follows the Schottky–Mott rule, exhibiting an unpinned Fermi level. This allows its energy bands to align directly with those of the contacting metal, making the barrier height predictable from the difference in work functions [2.39].

The work function (ϕ) of metals (ϕ_m) or semiconductors (ϕ_s) is the energy required to remove an electron from the Fermi level to the vacuum level. Based on the relative values of these work functions, two main types of contacts can form between a metal and a semiconductor: Schottky contacts and Ohmic contacts. In addition, metal-oxide-semiconductor (MOS) will introduce the working principle of FETs.

Schottky Contact

Metal–semiconductor contacts can generally be divided into Schottky and ohmic types. Schottky contacts are characterised by rectifying behaviour that arises from a potential barrier at the interface. For a p-type semiconductor, when the metal work function is lower than that of the semiconductor, charge transfer depletes holes near the surface, resulting in a depletion region and an interfacial barrier. This barrier suppresses carrier transport in one direction, producing an asymmetric current–voltage characteristic: the current rises exponentially under forward bias, while only a small leakage current flows under reverse bias. In contrast, ohmic contacts also involve an interfacial barrier, but it is sufficiently thin or low that carriers can tunnel through or surmount it efficiently, leading to a nearly linear current–voltage characteristic. Figure 2.6.1 shows the Schottky contact energy band diagram with a p-type semiconductor before and after equilibrium.

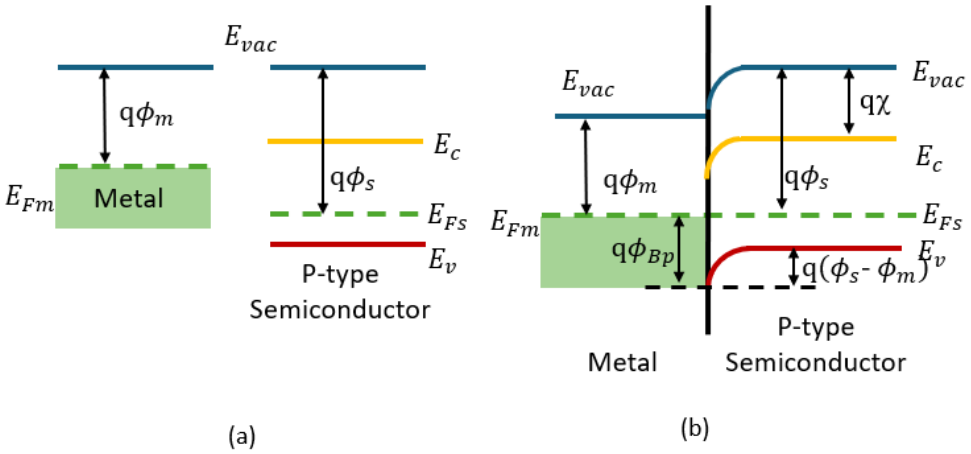

Figure 2.6.1 Energy band diagram of a p-type semiconductor forming a Schottky contact, (a) before contact, (b) after contact.

Here, ϕ_{B_P} is defined as the ideal barrier potential from the metal. The expression of barrier potential is given by equation 2.2, where E_g is the bandgap energy.

$$q\phi_{B_P} = E_g - (q\phi_m - q\chi) \tag{2.2}$$

Schottky contacts exhibit rectifying behaviour due to the potential barrier formed at the metal–semiconductor interface. Under forward bias, the effective barrier height for majority carrier transport is lowered, the depletion region narrows, and holes can more readily flow from the semiconductor into the metal. Under reverse bias, the barrier height remains essentially fixed, while the depletion region widens, thereby strongly suppressing hole transport across the junction. Figure 2.6.2 illustrates the corresponding energy band diagrams for a Schottky contact on a p-type semiconductor under forward and reverse bias.

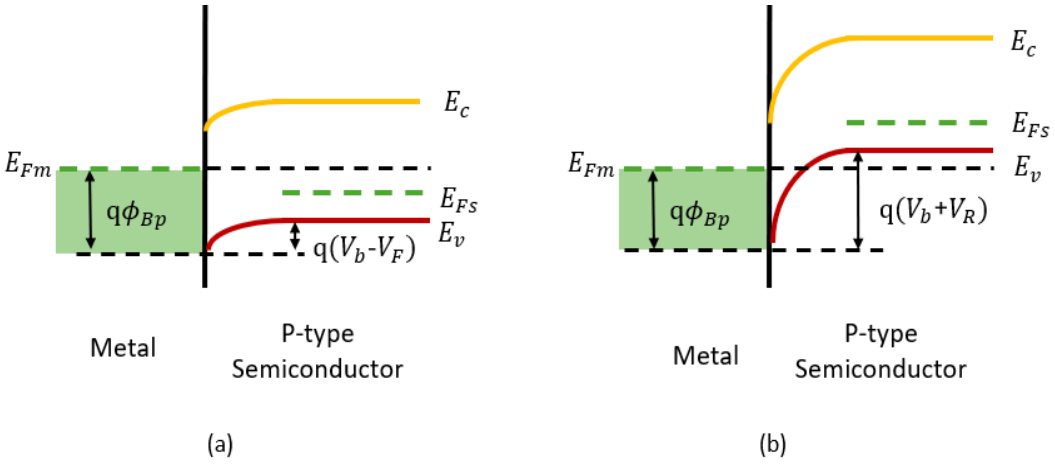

Figure 2.6.2 Energy band diagram of Schottky contact on p-type semiconductor (a) with forward bias, (b) with reverse bias.

When bias is applied, the electronic compensation on the metal side is fast, so the Fermi levels in the metal usually remain uniform and balanced. However, on the semiconductor side, due to the change of the depletion layer, the energy band will bend. In this case, the quasi-Fermi level on the semiconductor side will no longer match the Fermi level on the metal side.

In Schottky contacts, carriers cross the barrier in the following three ways, corresponding to thermionic emission, field emission and thermionic-field emission [2.40].

1) Thermionic emission (TE): refers to the situation where carriers have sufficient thermal energy to overcome the barrier height at the semiconductor-metal interface, highly dependent on temperature (above 300 K).
2) Field emission (FE): occurs when carriers tunnel through the potential barrier at the Fermi level. When the potential barrier is very thin, carriers can directly quantum tunnel. It depends on the carrier concentration at the interface and the barrier potential and has a relatively weak temperature dependence.
3) Thermionic-field emission: a process combining TE and FE, where carriers gain sufficient thermal energy to occupy states above the Fermi level and then tunnel through the potential barrier under the influence of the electric field. Both temperature and electric field contribute to carrier transport in this mechanism.

Ohmic contact

In an ideal ohmic contact, the potential barrier formed at the metal–semiconductor interface is very low or extremely thin, allowing carriers to flow in both forward and reverse directions symmetrically and providing a linear current response when a voltage is applied. For p-type semiconductors, ohmic behaviour is most readily achieved when the metal work function is larger than that of the semiconductor, as this minimises the barrier for hole injection. However, this condition is not strictly required, since sufficiently thin or low barriers can still permit efficient carrier transport through tunnelling or thermionic emission, resulting in ohmic-like characteristics. Figure 2.6.3 shows the energy band diagram of a p-type semiconductor before and after forming an Ohmic contact.

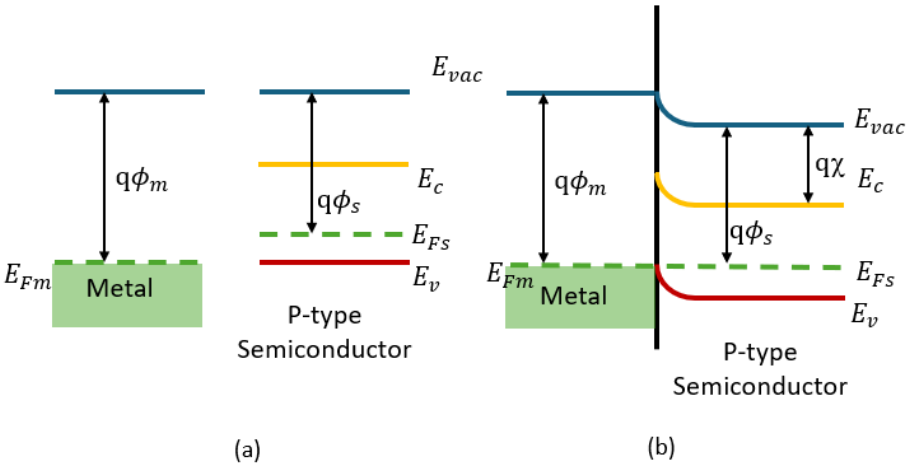

Figure 2.6.3 Energy band diagram of a p-type semiconductor forming an Ohmic contact (a) before contact, (b) after contact.

When the interface Fermi level is unpinned and the metal work function exceeds that of the p-type semiconductor, electrons will flow from the semiconductor to the metal until the Fermi levels align. This results in upward bending of the valence band edge with minimal barrier to hole transport. To form the Ohmic contact, the barrier height needs to be low enough to allow efficient carrier injection. If the barrier height cannot be further reduced, minimising the barrier width, by narrowing the depletion region, can enhance quantum tunnelling and thereby achieve ohmic contact.

MOS contact

Metal-oxide-semiconductor (MOS) contact is of great significance in this study. The quality of MOS contact will directly determine the performance of MOS devices. The analysis of MOS devices will be carried out in the next section. An ideal MOS interface can be regarded as a parallel plate capacitor, with the gate metal as the upper plate and the semiconductor as the lower plate. The MOS structure schematic diagram is shown in Figure 2.6.4.

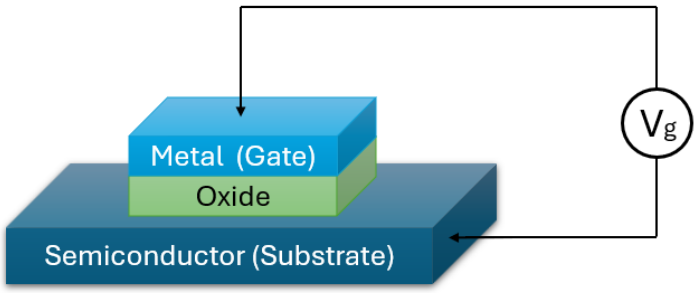

Figure 2.6.4 MOS structure schematic diagram with applied gate bias between the metal (gate) and the semiconductor (substrate).

In this research, H-diamond (p-type semiconductor) is taken as an example for analysis. When the applied bias is 0V, the band diagram of the MOS contact is shown in Figure 2.6.5. This schematic represents an idealised flat-band condition, in which the work-function difference between the metal and the semiconductor is assumed to be negligible, and the Fermi level of the metal is aligned with that of the semiconductor. In practical devices, a limited work-function difference exists, resulting in band bending in the semiconductor and a deviation from the flat-band condition. For the p-type H-terminated diamond MOS structures considered in this work, this situation is more associated with upward band bending at the semiconductor surface.

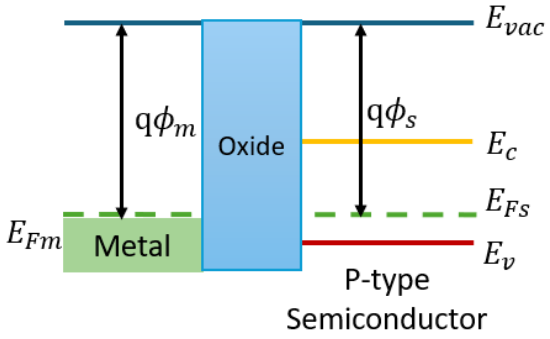

Figure 2.6.5 MOS contact with p-type semiconductor interface band diagram when bias is 0 volts.

When a negative bias is applied to the metal side, the oxide layer is equivalent to a parallel-plate capacitor being charged, establishing an electric field between the metal and the semiconductor surface. Electrons start to accumulate on one side of the metal. At this point, the top of the valence band of a p-type semiconductor bends upward, and the valence band is closer to the Fermi level. The majority carriers (holes) in the p-type semiconductor are generated at the interface between the oxide and the semiconductor and form a hole accumulation layer. As shown in Figure 2.6.6(a).

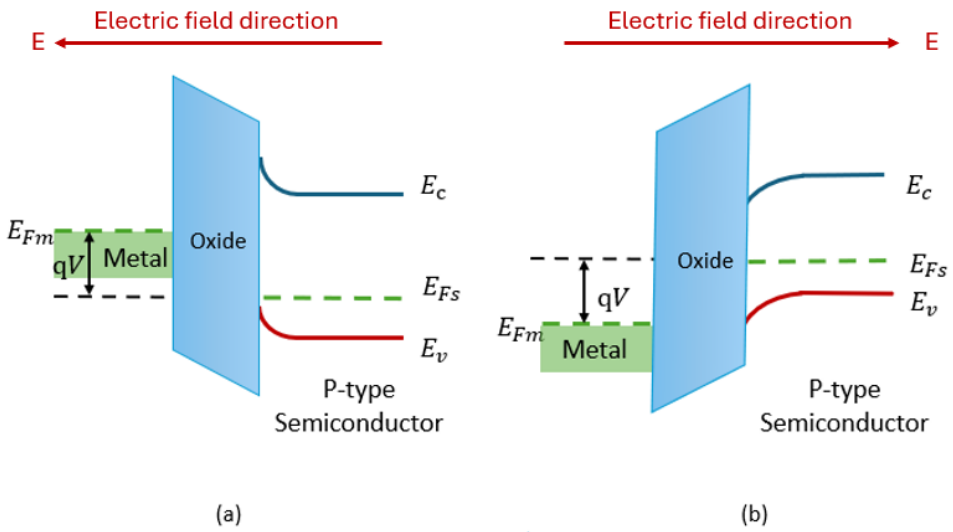

Figure 2.6.6 Energy band diagram of MOS contact on p-type semiconductor

(a) with negative bias, (b) with positive bias.

When a positive bias is applied to the gate metal, the electric field direction is reversed compared with the negative-bias case, and the energy bands at the semiconductor surface bend downward. In conventional bulk p-type semiconductors, this results in hole depletion at the oxide–semiconductor interface and the formation of a space-charge region of ionised acceptors. With further increase of the positive bias beyond the threshold voltage, the conduction band may approach the Fermi level, and, provided that a source of electrons is available, an inversion channel can form. This gives rise to a sharp increase in electron concentration at the semiconductor surface, as illustrated in Figure 2.6.6(b).

This description reflects the standard Si MOSFET model. In hydrogen-terminated diamond, the conductivity is from surface transfer doping rather than bulk acceptors, so depletion does not leave ionised charges in the same manner, and the conditions for inversion channel formation are not automatically met.

2.7 Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) Operation

Metal–oxide–semiconductor field-effect transistors (MOSFETs) are voltage-controlled devices that effectively operate as switches. As mentioned, H-diamond devices rely on 2DHG, that is, the carriers in the channel are holes. Therefore, in an H-diamond MOSFET, the gate bias modulates the density of this pre-existing 2DHG, thereby controlling the channel conductivity.

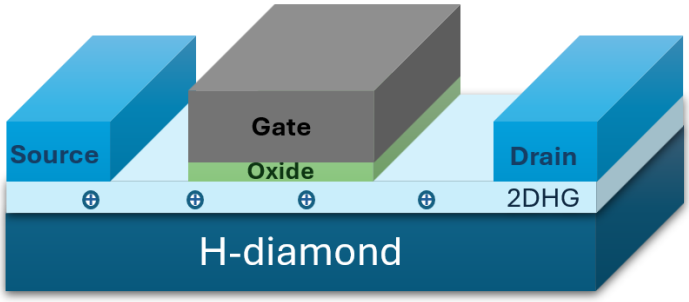

Figure 2.7.1 The schematic of a H-diamond MOSFET cross-section diagram.

As shown in Figure 2.7.1, the channel region is defined by the 2DHG, the source and drain act as ohmic contacts to this 2DHG, while the gate modulates the hole density in the channel via the electric field through the dielectric oxide. The H-diamond MOSFETs can be further classified into enhancement mode and depletion mode, depending on the operation.

1) Depletion Mode: At zero gate bias, the 2DHG density is high enough for the device to be conductive. Applying a positive gate bias reduces the hole density in the 2DHG, depleting the channel and eventually turning the device off.
2) Enhancement Mode: At zero gate bias, the 2DHG density is not enough for high conductivity. Applying a negative gate bias increases the surface band bending in the valence band, enhancing hole accumulation in the 2DHG channel and turning the device on.

The performance of MOSFETs can be further determined by analysing the DC performance under different biases. The output characteristics of MOSFETs (drain current vs. drain-source bias) can be used to evaluate the on-resistance of the device, on-current (I_{on}), and determine the reliable operating voltage of the device. A standard output characteristic IV curve of a depletion mode H-diamond MOSFET is shown in Figure 2.7.2.

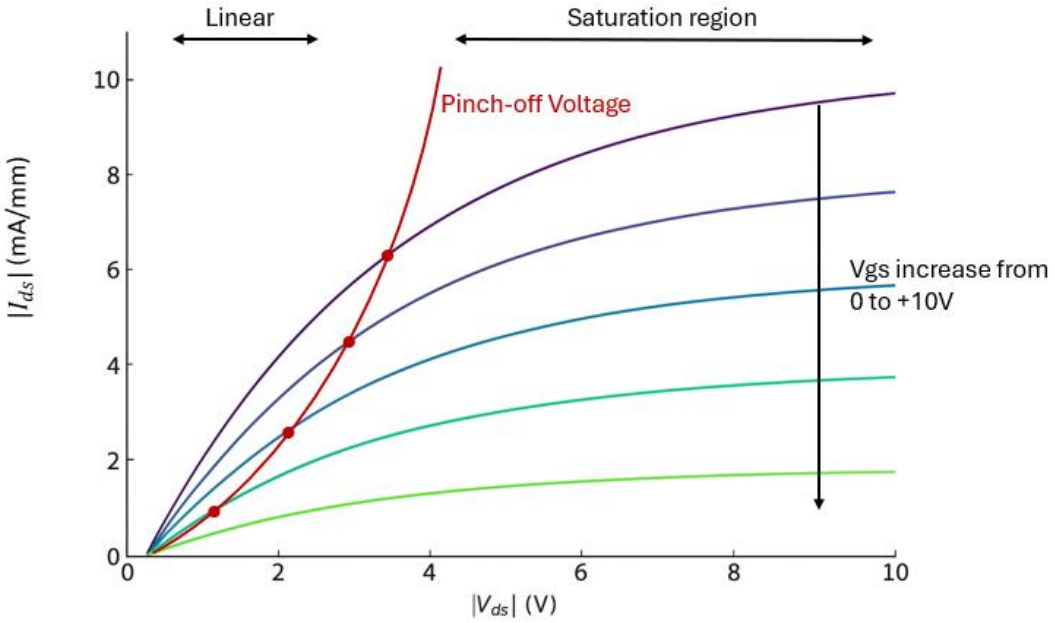

Figure 2.7.2 The schematic diagram of the output characteristics of a p-channel depletion-mode H-diamond MOSFET, the device conducts at V_{gs} = 0V, confirming depletion-mode operation.

Figure 2.7.2 can be explained with:

1) Cut off region: When V_{gs} is sufficiently positive, the 2DHG beneath the gate is almost entirely depleted, and the drain current is essentially zero apart from leakage.
2) Linear region: As V_{gs} becomes less positive and approaches V_{th}, a conductive 2DHG channel forms beneath the gate. For small drain–source voltages $|V_{ds}| < |V_{gs} - V_{th}|$, the channel behaves as a voltage-controlled resistor, hence, in this region, I_{ds} increases nearly linear with V_{ds}.
3) Saturation region: As V_{ds} increases to $V_{ds,sat}$=$|V_{gs} - V_{th}|$, two effects may occur: (a) the carrier velocity in the 2DHG approaches saturation due to the high electric field, and (b) the 2DHG near the drain is pinched off, which means beyond this point, further increases in $|V_{ds}|$ will not cause an increase or only a small increase in I_{ds}.
4) Breakdown: If V_{ds} exceeds the breakdown voltage of the device, the strong electric field will cause impact ionisation and avalanche breakdown in the depletion region, eventually leading to the device breakdown. When V_{gs} exceeds the maximum voltage that the gate dielectric layer can stand, gate dielectric breakdown or tunnelling leakage, which will damage the gate structure [2.38].

The specific DC performance analysis and related calculation methods will be presented in Section 5.2.

2.8 Summary

This chapter provides a brief explanation of the physical foundation of diamond materials, ranging from diamond structure to diamond surface transfer doping technology. On this basis, the analysis of the band structure and electrical characteristics of the metal-semiconductor interface was carried out. Through the content of this chapter, the reasons for using diamond as an electronic material have become clear, providing theoretical guidance for the construction of high-performance FETs on diamond.

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3. Literature Review

This chapter provides a comprehensive review of surface transfer doping strategies for hydrogen-terminated diamond and explains how a two-dimensional hole gas (2DHG) is formed. Various diamond surface termination techniques are reviewed, such as hydrogen-termination, oxygen-termination, scandium-termination, and silicon-termination. Ohmic contact strategies on H-diamond are explored. Subsequently, the performance of field-effect transistors (FETs) with different surface terminations is compared.

3.1 Surface transfer doping

As mentioned in Section 2.3, due to the wide bandgap and tightly packed carbon lattice of diamond, it is difficult to obtain shallow energy level dopants from impurity doping mechanisms at room temperature. Traditionally, boron doping provides the most effective conductive p-type diamond. However, it was found that a high boron concentration would lead to a significant decrease in hole mobility, even with the delta doping strategy [3.1-3.3]. Alternatively, surface transfer doping offers an effective doping method which relies on the exchange of interfacial charge between the diamond valence band and atmospheric molecules on the diamond surface [3.4].

A single-crystal diamond film grown by Plasma CVD without any impurity doping has been first reported with a relatively low resistivity of $10^6 \Omega \cdot \mathrm{mm}$ by Landstrass et.al in 1989 [3.5]. The initial explanation of this theory is that hydrogen diffuses into the diamond surface, leading to shallow acceptor states [3.5]. In 1996, evidence of a hole accumulation layer underneath the H-diamond surface was verified using X-ray photoelectron spectroscopy (XPS) and Kelvin probe measurements [3.6]. Under this mechanism, electrons from the diamond valence band can transfer into unknown acceptor states. Gi et al. also demonstrated the formation of a p-type surface conductive layer on deposited diamond films [3.7].

Negative electron affinity (NEA) on hydrogen-terminated diamond was first observed by Himpsel et al. in 1979. They implied that the vacuum level at the surface is below the conduction band minimum of diamond, and NEA enables the emission of electrons from the H-diamond surface [3.8]. Based on the NEA properties of H-diamond, Maier et al. proposed that the adsorbed aqueous layer on the H-diamond surface undergoes redox reactions and can serve as an active surface acceptor species for the formation of a hole accumulation layer [3.4]. This charge transfer will continue until the Fermi level of the

diamond aligns with the Fermi level of the surface acceptors. After equilibration, the H-diamond energy band bends upwards, as shown in Figure 3.1.1.

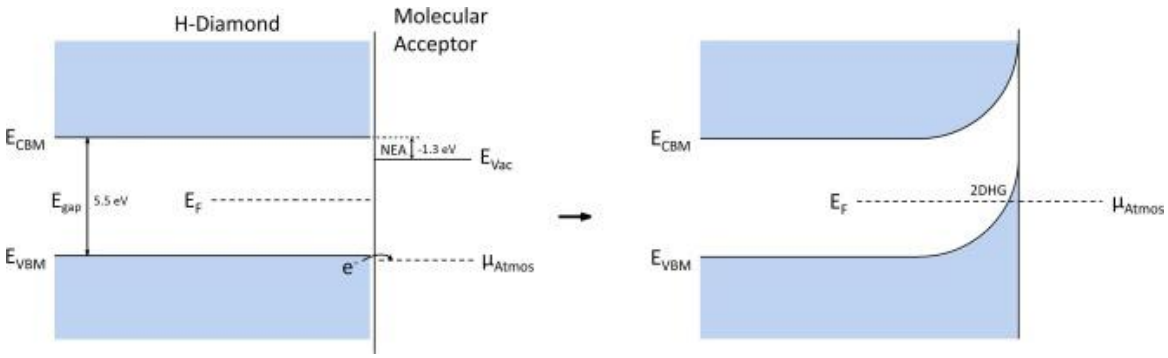

Figure 3.1.1 Energy band diagram illustrating the formation of a two-dimensional hole gas in hydrogen-terminated diamond when exposed to ambient air [3.9].

Although Maier's concept of the transfer doping mechanism is convincing, subsequent experimental work indicated that oxygen-ion acceptor species are the exact reason for the observed conductivity at the H-diamond surface in the atmosphere [3.10]. In 1999, Gi et al. carried out the Hall Effect measurements of the surface conductive layer of undoped diamond under the atmosphere of NO_2 and NH_3. They clarified that the mechanism of resistance variation is from the surface conductive layer, which was generated by adsorbing NO_2 and O_3, ultimately leading to the reduction of holes [3.11,3.12].

In 2013, the lowest sheet resistance of H-diamond achieved to date was 719.3 Ω/□ for a (111) oriented surface, as reported by Sato et al. [3.13]. This was achieved by exposing the H-diamond surface to highly concentrated NO_2, resulting in an extremely high carrier density up to 1.5×10^{14} cm^{-2}. This result aligns with a detailed study by Takagi et al. [3.14], which, based on first-principles calculations and experimental measurements, investigated various air-borne species to establish the transfer doping capabilities. Their work figured out that the hole concentration (p_s) depends on the species of adsorbate molecules. Using the highest occupied molecular orbital (HOMO), the lowest unoccupied molecular orbital (LUMO), and the single occupied molecular orbital (SOMO) of the isolated inorganic molecule and the valence band maximum (VBM) and the conduction band minimum (CBM) of (100), (110), and (111) H-terminated diamond surface to compare with, as shown in Figure 3.1.2. The first group of molecules includes NO_2, O_3, NO, and SO_2, which have LUMO/SOMO levels below or around the VBM of H-terminated diamond, leading to an increase of p_s. While the second group of adsorbates, such as N_2O, CO_2 and water, has little or no influence on p_s.

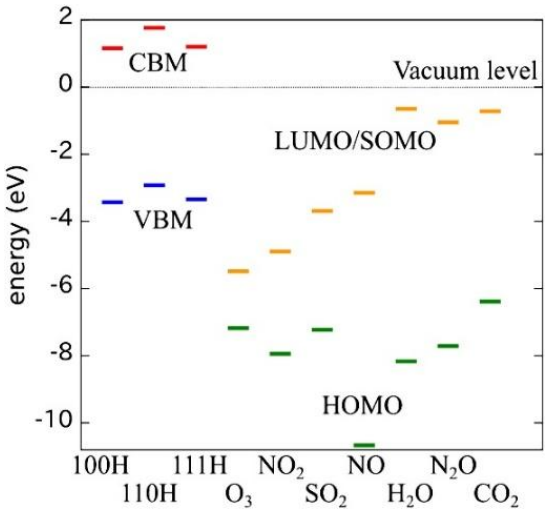

Figure 3.1.2 Energy level of occupied molecular orbital with the VBM and CBM of H-diamond [3.14].

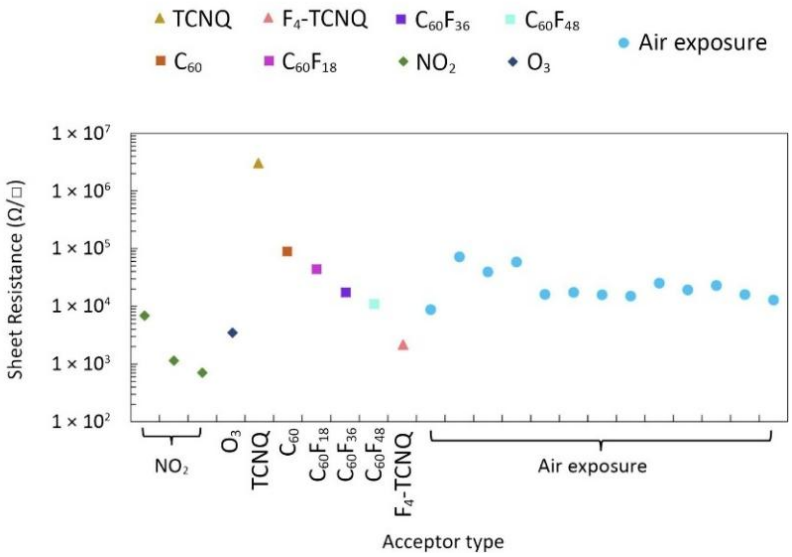

Figure 3.1.3 Different molecular species found to induce transfer doping of H-diamond [3.9].

In addition, molecules with high electronic affinity, such as C_{60}, $C_{60}F_{xx}$, and F_4-TCNQ, can be deposited on the surface of H-diamond, replacing the atmospheric adsorption layer and initiating surface transfer doping [3.15-3.18]. The summary of different molecular species found to induce transfer doping of H-diamond is shown in Figure 3.1.3.

These organic molecules offer an alternative way for surface transfer doping in H-diamond, however, they cannot provide sufficient operational stability for H-diamond electronic devices when exposed to atmospheric conditions or changing temperature environments. This has motivated the exploration of various types of solid encapsulation

materials, such as metal oxides. In 2013, Russell et al. reported that molybdenum trioxide (MoO_3) induced transfer doping, which increased the carrier concentration of the 2DHG in H-diamond from 1×10^{13} cm^{-2} to 2.16×10^{13} cm^{-2} [3.19]. The electron affinity of MoO_3 is 6.7 eV, which means that the conduction band minimum (CBM) of MoO_3 lies more than 2.8 eV below the valence band maximum (VBM) of H-diamond, hence, the electrons are more likely to transfer from H-diamond to MoO_3, as shown in Figure 3.1.4.

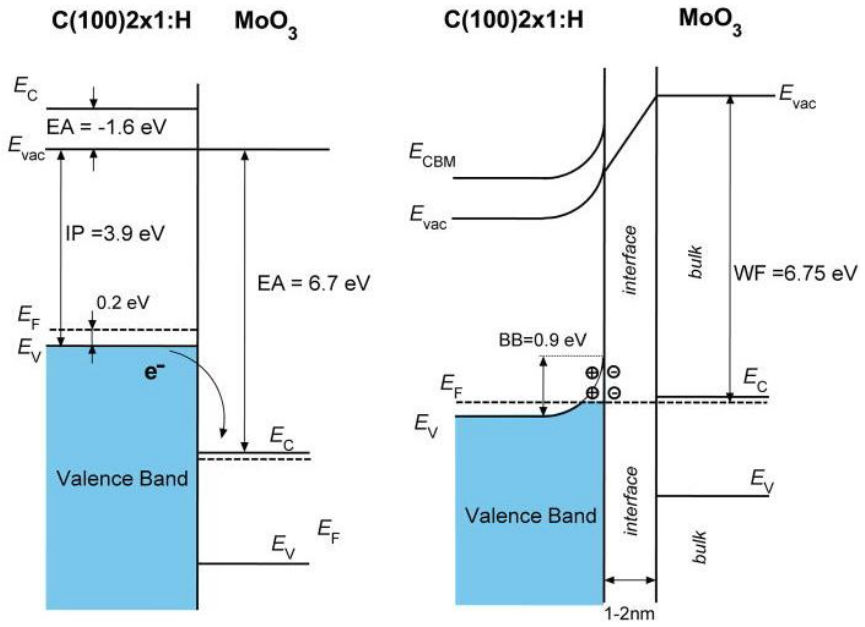

Figure 3.1.4 Energy band diagram of surface transfer doping process in hydrogen-terminated diamond using MoO3 as a surface acceptor [3.19].

When the electron affinity (EA) of the surface acceptor is high enough, the surface electron acceptor CBM sits below the VBM of H-diamond. As the Fermi levels align, the energy band bends upward, resulting in the formation of 2DHG beneath the H-diamond surface. Transition metal oxides (TMOs) such as vanadium pentoxide (V_2O_5) [3.20], rhenium trioxide (ReO_3) [3.21], tungsten trioxide (WO_3) [3.21], niobium pentoxide (Nb_2O_5) [3.22], and chromium trioxide (CrO_3) [3.23] have been reported following the success of MoO_3.

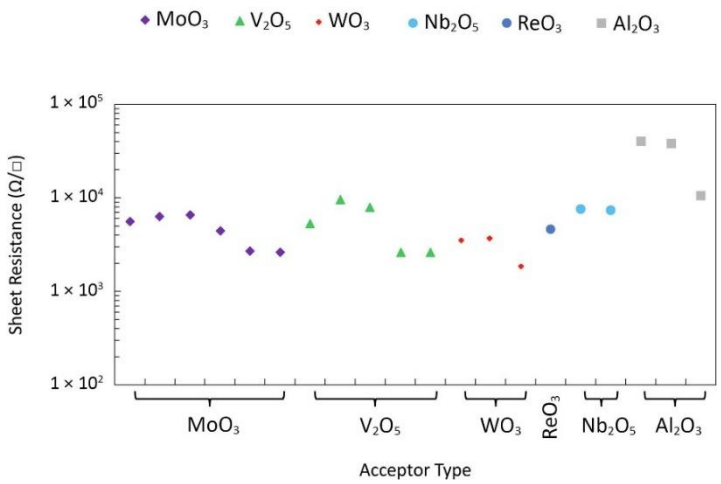

Figure 3.1.5 Reported H-diamond conductivities with transfer-doped metal oxides [3.9].

Therefore, compared to molecular species such as C_{60} or NO_2, TMOs are a more attractive solution for electron acceptors, as they exhibit higher stability over a wider temperature range [3.9]. Before the work of high EA TMOs, Hiraiwa et al. reported in 2012 the use of Al_2O_3 on H-diamond to encapsulate and stabilise the surface conductivity [3.24]. The Al_2O_3 film was formed on the diamond surface by the atomic layer deposition (ALD) with H_2O oxidant at 450 °C, which achieves highly reliable passivation. The protected 2DHG survived under air annealing at 550 °C for one hour, enabling the 2DHG device to achieve stable high-temperature operation. However, Al_2O_3 does not have a particularly high electron affinity, which is different from the transfer doping mechanism of high EA TMOs. The comparison of the CBM for TMO materials in relation to the diamond bandgap is shown in Figure 3.1.6.

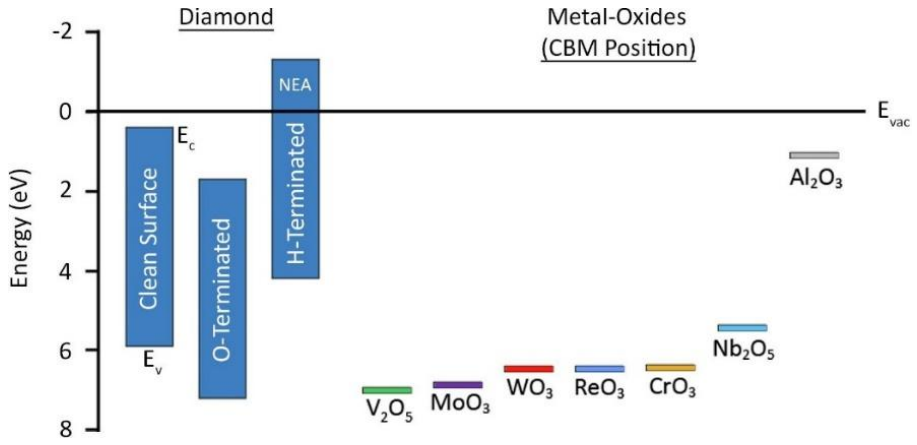

Figure 3.1.6 Electron affinities of various metal oxides relative to the diamond bandgap [3.9].

Kawarada et al. then demonstrated that air exposure is not important for achieving conductivity in H-diamond with an ALD Al_2O_3 encapsulation layer [3.25]. Later supported

by Yang et al. [3.26]. Ren et al. reported ALD Al_2O_3 with a large band offset of 3.3 eV on H-diamond. The O/Al ratio of the Al_2O_3 film indicates that there are interstitial O and Al vacancy defects beneath the H-diamond VBM, which may act as electron acceptors [3.27]. However, the transfer doping mechanism entirely relies on the ALD growth process parameters. Consistent with the process-dependent nature of Al_2O_3-induced transfer doping, Verona et al. reported that the sheet resistance of H-diamond with Al_2O_3 deposited by electron-beam evaporation is several times greater (from 16.5 kΩ/□ to 40 kΩ/□) than that reported for H-diamond with ALD Al_2O_3 [3.22]. Importantly, the absence of an in-situ anneal before the e-beam deposition may have encapsulated residual surface adsorbates, thereby lowering the hole density. This highlights the critical role of pre-deposition surface preparation and raises the possibility that in studies lacking in-situ annealing, the observed conductivity changes may not arise from genuine transfer doping by the encapsulating oxide but instead from trapped adsorbates.

3.2 Novel diamond surface termination

Most studies on the surface termination of diamond start with hydrogen termination and oxygen termination. It has been reported that other alternative chemistries can also be used to modify the surface for different applications [3.28]. As mentioned above, when the diamond surface is terminated with hydrogen atoms, it exhibits an NEA of approximately -1.3 eV. However, due to a reversed surface dipole, the electronegativity of oxygen is greater than that of carbon, leading to the electrons being drawn towards the surface. In this case, holes are depleted near the surface, resulting in a positive electron affinity (PEA) [3.29]. The energy band diagrams for the clean reconstructed surface, the O-diamond and the H-diamond surface are shown in Figure 3.2.1.

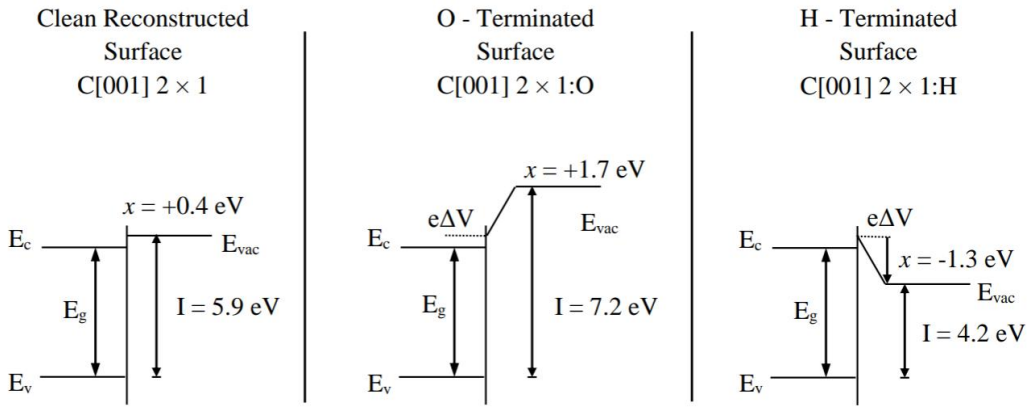

Figure 3.2.1 Energy band diagrams for clean reconstructed surface, Oxygen-Terminated Surface and Hydrogen-terminated surface [3.30].

The oxygen termination of diamond is typically achieved through various methods, such as exposure to O_2 plasma, UV ozone exposure, treatment with strong acids, and thermal annealing in air [3.28]. Among these methods, UV ozone oxidation at room temperature can achieve high oxygen coverage on diamond surfaces while maintaining structural integrity, as reported by Yang et al. [3.31].

The oxidation method determined which types of bonds form between oxygen and the diamond carbon atoms. These different bonding methods generally encompass the formation of ketone (C=O), bridging ether (C–O–C) and hydroxyl (C–OH), their relative concentrations are substantially altered by the particular oxidation method used [3.28]. The schematic diagrams of different carbon-oxygen bonding obtained through various oxygen treatment methods, along with the corresponding percentages, are shown in Figure 3.2.2.

Furthermore, the observed differences in the work function values of the four oxygen-terminated diamond surfaces range from 4.65 eV to 5.79 eV, which is significantly influenced by the oxygen-containing functional groups [3.28].

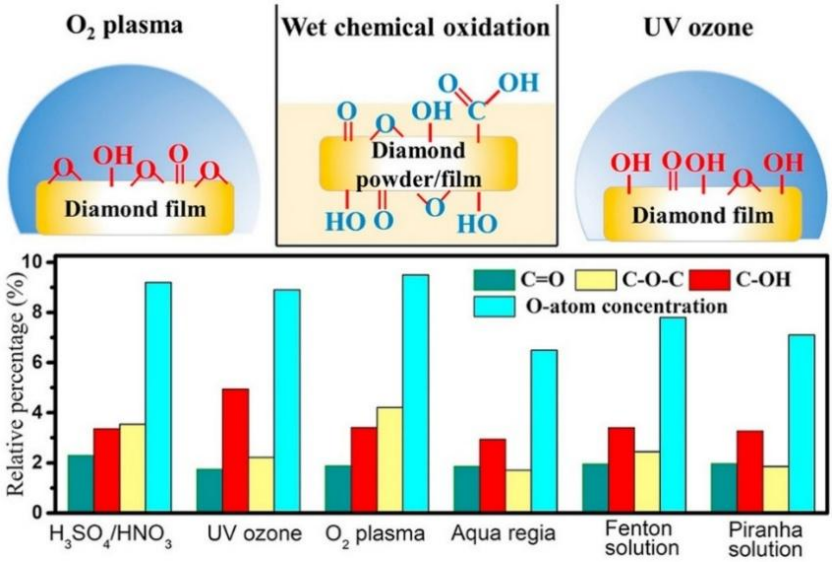

Figure 3.2.2 The schematic diagrams of different carbon-oxygen bonding obtained through various oxygen treatment methods, along with the corresponding percentages [3.32].

It is worth noting that due to the extremely low surface free energy of H-diamond, and because the completely hydrogen-terminated diamond surface has only very weak van der Waals interactions with water molecules, this results in the surface being hydrophobic [3.33]. However, when the surface consists of oxygen functional groups, the surface becomes polar and interacts with other polar medium like water [3.33]. Therefore, the

diamond surface with oxygen terminations is hydrophilic and has a high surface free energy. The variation of contact angle for the UV ozone treated H-diamond as a function of treatment time is shown in Figure 3.2.3.

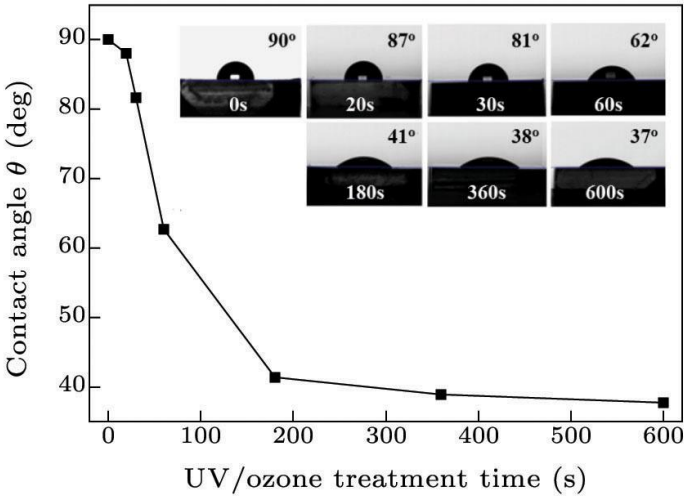

Figure 3.2.3 Variation of contact angle for the UV ozone treated H-diamond as a function of treatment time [3.32].

By investigating the hydrogen termination and oxygen termination of diamond surfaces, it was found that the essence of different terminated surfaces lies in controlling the EA and work function of the diamond surface.

Similar to the p-type transfer doping observed in H-diamond, if there is a significant PEA on the diamond surface and appropriate electron donor species can be deposited, it is theoretically possible to induce n-type conductivity on diamond. Therefore, efforts were made to explore other termination methods in order to achieve performance-type transfer doping, especially fluorine termination, which has received increasing attention.

Sen et al. used first-principles calculations to analyse the effects of fluorine termination on the stability and bonding structure of diamond (111) surfaces and compared them with hydrogen termination in 2009. They found surface F atoms, similar to H, formed sp^3 bonding with C atoms, which resulted in a stable 1x1 configuration [3.35]. The surface of the F-termination is more stable in a larger phase space than that for H-termination. This is due to the formation of strong ionic C–F bonds and the development of attractive forces between large F atoms, leading to close packing of F atoms. As a result, the diamond surface with an F terminal exhibits greater chemical inertness [3.35].

A variety of techniques have been reported for preparing F-terminated diamond surfaces with varying degrees of success. These have been based on the exposure of surfaces to atomic fluorine or molecular F_2 in its (compound) gaseous phase, and more recent

efforts have used fluorine-containing plasma to achieve this with CF_4, XeF_2, CHF_3, C_4F_8, SF_6 [3.36-3.40]. A large PEA of 2.56 eV for a plasma fluorine-terminated diamond surface was reported by Rietwyk et al. in 2013. Figure 3.2.4 shows the band diagram corresponding to these measurements [3.41]. Hence, F-terminated diamond also exhibits hydrophobic properties with a contact angle of 103° [3.42].

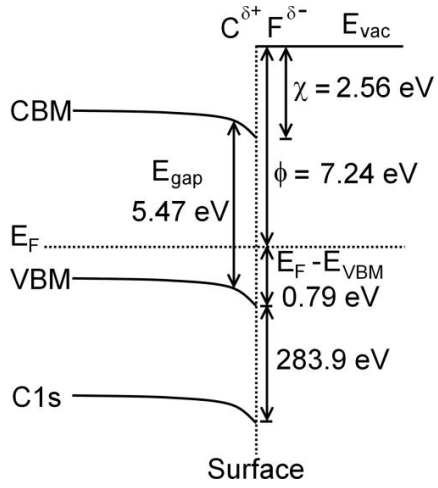

Figure 3.2.4 The schematic energy level diagram of the F: C (100) – (2 × 1) surface [3.41].

In recent years, researchers have been constantly exploring and developing alternative diamond terminations which have a larger NEA and remain stable at high temperatures. The most straightforward method for preparing the NEA surface on diamond is to deposit an element (usually a metal with Pauling electronegativity < 2.6) onto the diamond surface [3.43]. The diamond surface has to be heated to remove any existing surface termination, and then the metal is deposited by evaporation or sputtering. Then, the surface is annealed at high temperature under a vacuum to allow the metal to react with carbon and directly bond to the surface. Monolayer or sub-monolayer coverage is preferred because thicker layers would affect the electronic structure of the surface due to the influence of bulk adsorbates [3.43].

Silicon has a cubic crystal structure similar to that of diamond, and it is expected to form an ordered surface termination structure with diamond. According to spontaneous polarisation theory, the dipole of C-H and C-Si has similar differences in electronegativity (C-H is 2.5:2.1, C-Si is 2.5:1.8) [3.44]. Schenk et al. reported that silicon termination of diamond can be formed by depositing a monolayer of silicon on the (100) H-diamond surface and subsequently conducting in-situ vacuum annealing at 920℃ for 15 min [3.45-3.47]. The NEA of Si-terminated diamond in a vacuum was -0.86 eV. It decreased to -0.25 eV after exposure to air, as silicon termination is very easy to oxidise [3.45-3.47].

Later, Qiao et al. demonstrated that Si termination can also induce a two-dimensional hole gas (2DHG). However, the resulting hole density ($3.92\times10^{10}cm^{-2}$) is about two orders of magnitude lower than the typical values reported for H-terminated diamond ($\sim10^{12}$ cm^{-2}) [3.48]. Their results showed that the Fermi level is 0.2 eV above the VBM of the surface, the work function is 4.89 eV, and the band diagram of the Si-terminated diamond surface is shown in Figure 3.2.5.

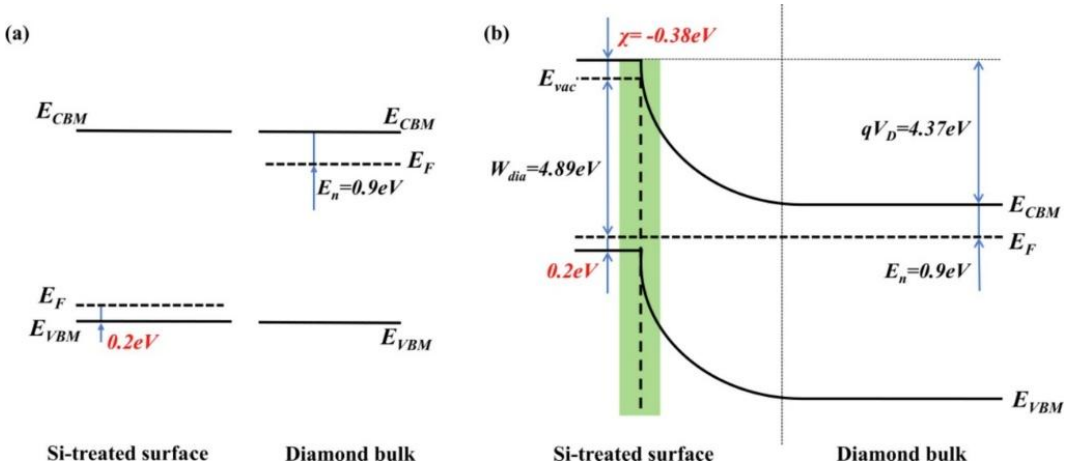

Figure 3.2.5 (a) Energy level diagram of Si-treated surface and diamond bulk. (b) Energy band diagram of Si-treated diamond surface [3.48].

The lower NEA value of Si termination reduces its ability to drive electron transfer and maintain surface hole accumulation, which fundamentally explains the substantially lower 2DHG density compared with H-terminated diamond.

Zulkharnay et al. considered scandium as another likely NEA candidate due to its relatively small ionic radius (0.75 Å), electropositive character (electronegativity is 1.36) and easy to form a highly charged cation [3.49]. They demonstrated that the NEA of 0.25 monolayer Sc-terminated bare diamond with −1.45 eV and −1.13 eV for the diamond (100) and (111) surfaces, respectively [3.50]. Geometries of 0.25,0.5,1 monolayer C-Sc bonding are shown in Figure 3.2.6.

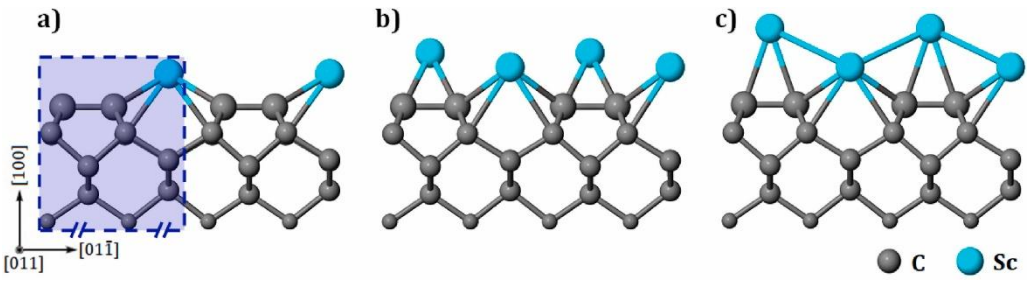

Figure 3.2.6 Sc-adsorbed bare diamond (100) surface of the lowest-energy optimised geometries of (a)–(c) 0.25, 0.5 and 1 monolayer, respectively [3.49].

In conclusion, the surface termination determined the electronic properties of diamond, particularly in terms of their electron affinity and the alignment of interface energy bands. Each termination has its unique advantages: H-termination can form 2DHG, the O-termination and the F-termination show PEA and stability. In contrast, NEA terminations have attracted great interest for their ability to enable efficient electron emission, which is the basis for cold-cathode applications operating at low temperatures. Further exploration of different diamond terminations, therefore, creates opportunities for both electronic and vacuum electronic device design.

3.3 Ohmic contact metal and carbide formation on H-diamond

Ohmic contacts are one of the important research topics in the application of diamond materials in electronic devices. Compared with other semiconductor materials, diamond has unique characteristics because it does not have a natural oxide layer. Therefore, the properties of the metal contact on diamond strongly depend on the termination of the diamond surface [3.51].

For boron-doped single-crystal diamond with a bandgap of 5.5 eV, the reported specific contact resistances range from above 10^{-3} Ω·mm down to the lowest published value of 10^{-7}Ω·mm [3.52]. Achieving such low-resistance ohmic contacts typically requires high-temperature annealing (>500 °C), which imposes constraints on fabrication processes and device design [3.52]. There are two main strategies used to obtain a relatively low-resistance ohmic metal contact of transfer-doped H-diamond. In 1994, Aoki et al. explored the characteristics of the as-grown CVD diamond surface in contact with various metals [3.53]. Their research results indicated a strong correlation between the interface Schottky barrier height and the work function of the deposited metal on the H-diamond [3.53]. This was because the H-termination provided a low density of states, which, by reducing the Fermi level pinning, made the diamond surface sensitive to the metal work function [3.9]. Therefore, high work-function metals exhibit linear ohmic contact on hydrogen-terminated diamond, while low work-function metals show Schottky barrier contact [3.54]. Alternatively, a carbide interface can be formed on the diamond, and it is suitable for operation at higher temperatures. However, the formation of the carbide requires a high-temperature annealing process at 600°C or above [3.51,3.55].

Au has been the most commonly used as an ohmic contact on H-diamond due to its high work function (ϕ_M: 5.1 eV) [3.56]. The reported lowest contact resistance of Au is 0.9 Ω·mm, and the more common contact resistance of Au is around 5 Ω·mm [3.57, 3.58]. The other high work function metals have also been proven to form linear ohmic contact

on H-diamond, such as Pd (ϕ_M:5.12eV) and Pt (ϕ_M:5.65eV) [3.56, 3.59-3.63]. The band diagram at the interface of metal/H-diamond is shown in Figure 3.3.1.

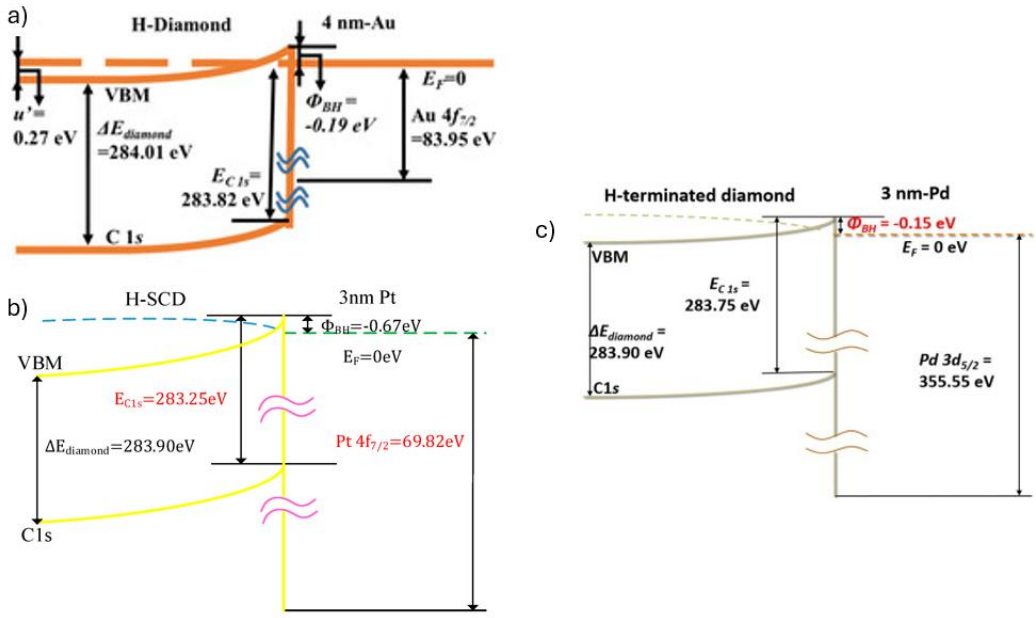

Figure 3.3.1 The band diagram at the interface of a) Au/H-diamond, b) Pt/H-diamond, and c) Pd/H-diamond [3.59,3.62,3.63].

It is worth noting that many studies on ohmic contacts of H-diamond have used the specific contact resistance (Ω.cm²), which makes it challenging to compare with the reported values in units of Ω·mm, as the information required for conversion between these two units is often unavailable. The specific contact resistance utilises the transfer length and the area where the metal edge current accumulates. The unit width contact resistance (Ω·mm) normalises the resistance with the contact width, without considering transfer length. In the transfer-doped H-diamond, the surface conductivity caused by the transfer doping largely depends on the adsorbates or high EA oxides on the surface of H-diamond. Therefore, the measured sheet resistance within the active region between ohmic contacts will almost certainly be different from the sheet resistance of the H-diamond beneath the contact metal, thereby resulting in errors when measuring the transfer length value using this method.

The most common carbide-based contact reported is TiC, with a contact resistance (width-normalised) of around 9 Ω·mm reported by Jingu et al [3.55] on H-diamond. In their research, TiC pads were selectively fabricated on O-terminated diamond surfaces and annealed for one hour under a H atmosphere at 600 °C. After carbide formation, the remnant O-terminated surface was subjected to H-radical irradiation for hydrogen termination [3.55]. In this process, atomic hydrogen radicals, generated by thermally

dissociating molecular hydrogen in a hot-filament source, react with surface oxygen species, leading to their removal (primarily as H_2O) and the formation of stable C–H surface bonds. The TiC layer is proposed to intrude into the diamond and forms shallow side contacts with the hole accumulation layer, as shown in Figure 3.3.2.

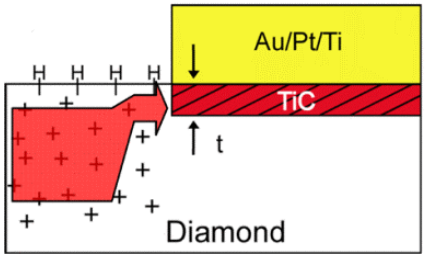

Figure 3.3.2 Schematic of cross-sectional view of TiC/diamond interface on H-diamond [3.55].

Leroy et al. searched for stable carbides in the metal-carbon binary phase diagram and chose molybdenum (Mo) as a good candidate because it is relatively insensitive to oxygen [3.64]. They found that some impurities in the annealing atmosphere entered the Mo lattice and occupied the interstitial sites. These interstitial sites are conducive to the diffusion of carbon atoms and thus are very important during the formation of carbides [3.64]. Therefore, the more interstitial sites occupied by elements other than carbon, the greater the difficulty in forming the carbide phase and the higher the temperature required for carbide formation [3.64]. Later, Okotrub et al. reported that the result of single-crystal diamond covered with Ti and Mo films was annealed in an ultra-high vacuum at temperatures of 500℃ and 800℃. XPS results showed that a clear MoC peak appeared at 500℃, while the TiC peak was observed at 800℃, as shown in Figure 3.3.3.

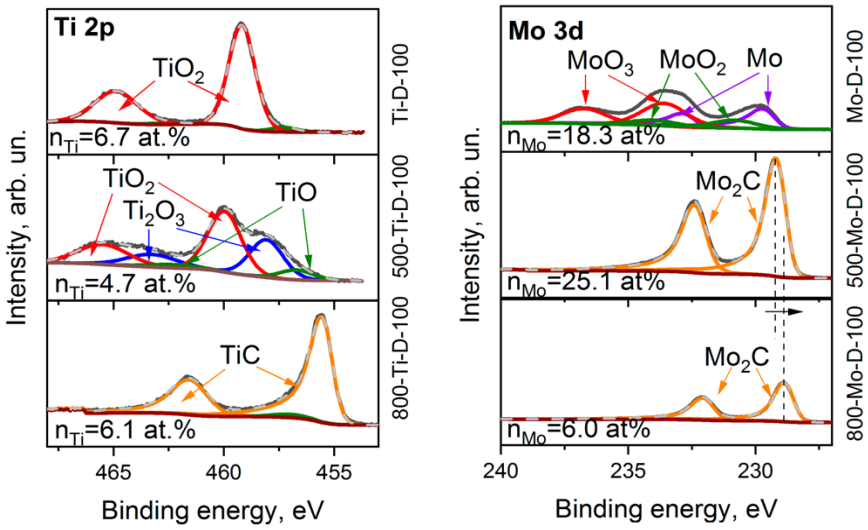

Figure 3.3.3 XPS Ti 2p spectra and Mo 3d spectra before and after annealing at 500℃ and 800℃ [3.65].

This conclusion is consistent with the theory of Leroy et al., which suggests that MoC can be formed at a lower temperature than TiC.

Overall, achieving high-quality ohmic contacts is crucial for the high-performance operation of H-diamond devices. High work function metals such as Au, Pd, and Pt can achieve low contact resistance without damaging the H-termination, demonstrating excellent linear I-V characteristics. Additionally, TiC contacts exhibit good ohmic properties but often require high-temperature annealing and subsequent post-hydrogen termination, leading to challenges in process compatibility.

3.4 Field-Effect Transistors

As mentioned previously, H-diamond with 2DHG created the unique possibility for the fabrication of lateral electronic devices in diamond. The concept of H-diamond MESFET was first demonstrated by Kawarada in 1994, and its structure is shown in Figure 3.4.1 [3.66]. In their work, a CVD-grown H-diamond substrate (100) is transfer-doped with air exposure. As a high work function metal, Au is used as an ohmic contact for the source and drain. Low work function metal Al is used as a gate metal.

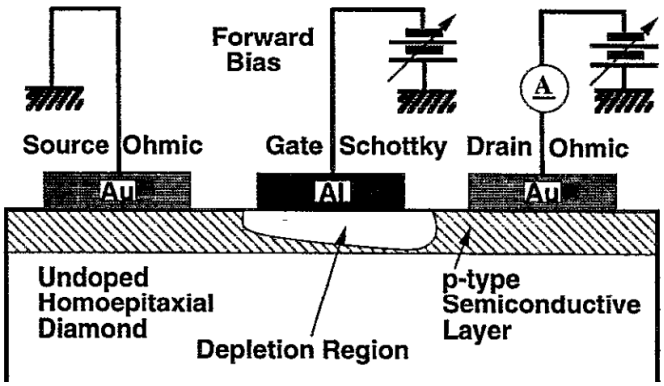

Figure 3.4.1 Structure of the original H-diamond MESFET [3.66].

The gate length of this device is 10 μm, operating in enhancement mode, exhibiting a modest maximum drain current of 1.6 mA/mm and an extrinsic transconductance of 200 μS/mm [3.66]. Since then, through improvements in the quality of the synthetic diamond substrate and optimisation of the FET geometry and device processing, the performance of H-diamond FETs has been gradually improved significantly.

In 2006, Ueda et al. demonstrated a diamond FET with a gate length of 100nm fabricated on high-quality polycrystalline diamond. The DC characteristics of the FET showed a drain current value of 550 mA/mm and a maximum transconductance of 143 mS/mm, the output characteristic as shown in Figure 3.4.2(a) [3.67]. Russell et al. reported an H-diamond MESFET using Al as the gate contact and optimised the gate length down to

50 nm in 2012 [3.58]. A maximum drain current of 295 mA/mm and the extrinsic transconductance peak of 78 mS/mm were measured, as shown in the output characteristic in Figure 3.4.2 (b). However, the gate leakage has a peak value of 0.02 mA/mm across the inspected bias range.

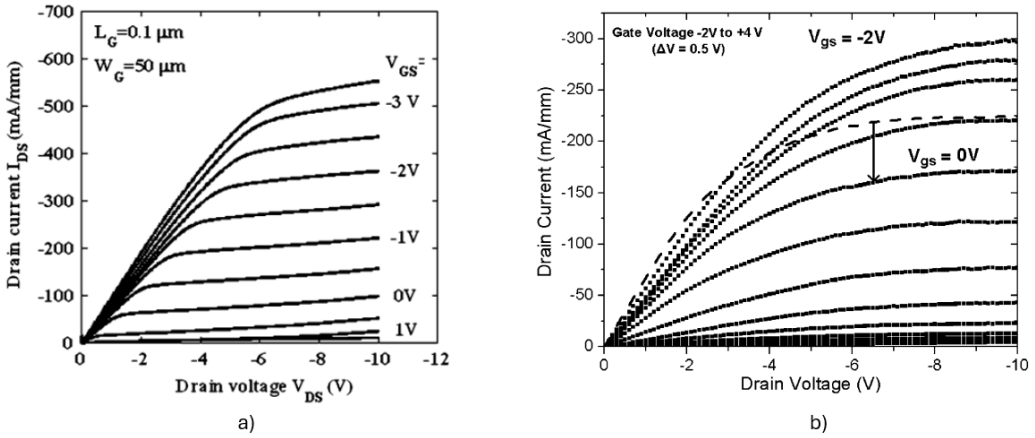

Figure 3.4.2 Reported output characteristics of (a) 100nm gate length H-diamond FET, (b) 50nm gate length H-diamond MESFET [3.67, 3.58].

As mentioned in Section 3.1, the electron acceptor layer on the diamond surface can induce the transfer doping and lead to the formation of 2DHG. Based on this mechanism, a lot of research has been conducted with MISFETs. Various dielectric materials were introduced beneath the gate metal of the device, which aim to increase the breakdown voltage and reduce the leakage current passing through the gate contact [3.9]. Verona et al. first reported the development of a new type of MISFET with vanadium pentoxide (V_2O_5) as the insulating material, fabricated on single-crystal H-diamond in 2016. The schematic cross-section diagram is shown in Figure 3.4.3.

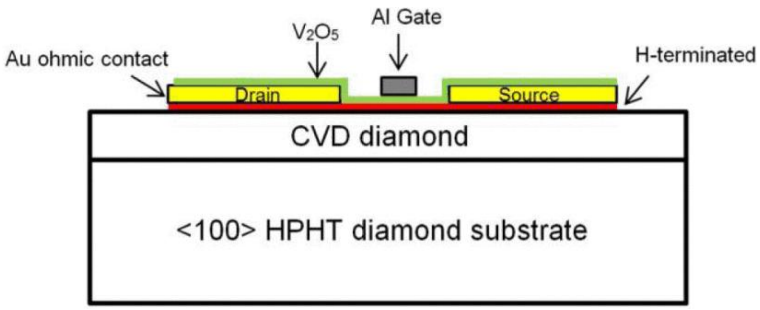

Figure 3.4.3 Schematic cross-sectional view of H-diamond MISFET with V_2O_5 gate dielectric [3.68].

Figure 3.4.3 illustrates that V_2O_5 acts as the gate dielectric, the V_2O_5 layer also extends across the source/drain access regions, covering the entire channel surface [3.68]. Their experiment results show that V_2O_5 can increase the carrier concentration compared to

the initial carrier concentration in air. Subsequently, the diamond sheet resistance dropped from 13.5 kΩ/□ to 2.7 kΩ/□. The device performs well in terms of conductivity, long-term stability, and resistance to high temperatures up to 200℃. Consistent with the transfer-doping mechanism enabled by V_2O_5, the maximum drain current of the 2 μm gate MISFET reached 280 mA/mm, about 80 mA/mm higher than that of MESFETs with the same gate length [3.68].

Later, Crawford et al. optimised the gate length to 50 nm, and instead of using V_2O_5 as an encapsulation layer covering the entire device, as shown in Figure 3.4.4. Their device exhibited a peak drain current of 700 mA/mm and a peak transconductance of 150 mS/mm in 2020 [3.57]. However, because V_2O_5 encapsulates the entire device rather than being confined beneath the gate, the transistor does not show complete turn-off behaviour, as can be seen in the output characteristics of Figure 3.4.4(b).

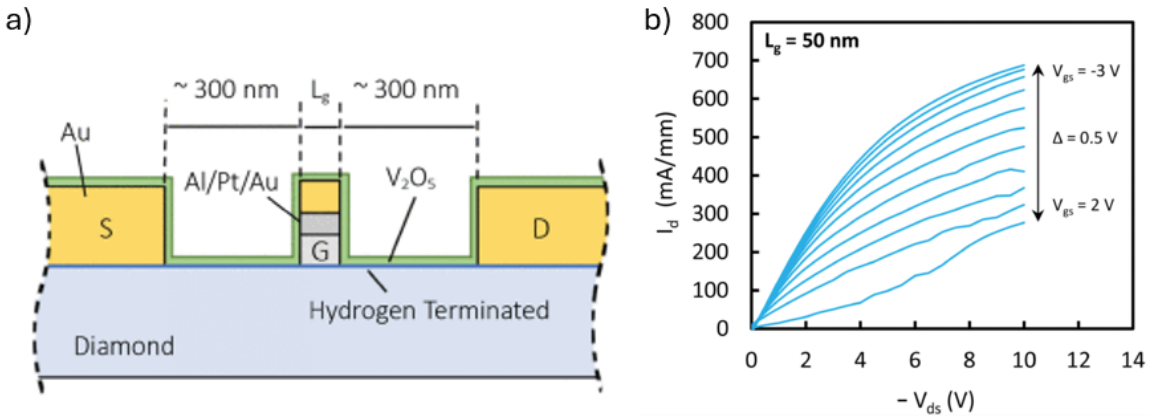

Figure 3.4.4 (a) Schematic cross-sectional view of H-diamond MESFET with V_2O_5, and (b) the output characteristics of a H-diamond MESFET with V_2O_5 [3.57].

In parallel, diamond MOSFETs with MoO_3 dielectric directly deposited on the H-diamond surface have also been tested by Ren et al. in 2017. The device structure is shown in Figure 3.4.5. Typical characteristics of this device with a gate length of 4 m include saturation drain current of 33 mA/mm and transconductance of 29 mS/mm [3.69]. However, the leakage current of the devices with a 10nm MoO_3 layer is similar to that of similar devices fabricated with a 3nm Al_2O_3 layer under the gate [3.69,3.70]. This implies that enhancing the quality of MoO_3 or depositing another high-k dielectric layer on top of the MoO_3 layer is necessary to improve the device performance.

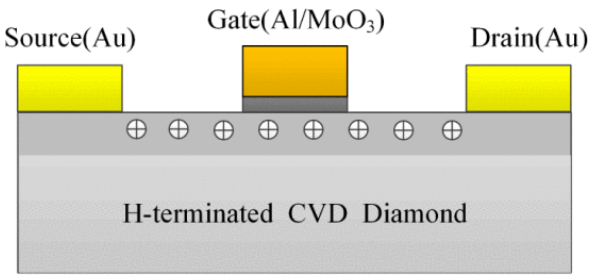

Figure 3.4.5 Schematic cross-section view of the diamond MOSFET with MoO_3 [3.69].

With the same electric field, the gate oxide with higher dielectric constant values can provide a greater hole density for MOS electronic devices [3.71]. Therefore, many oxides are used as gate oxides, such as Al_2O_3, HfO_2, and SiO_2. The maximum drain current achieved for H-diamond FETs to date for a 0.4 μm gate is 1.35 A/mm, as obtained with NO_2 adsorption and the Al_2O_3 passivation layer [3.73]. Hirama et al. indicated that due to the presence of NO_2 adsorbates, a large number of hole carriers will accumulate near the H-diamond surface, and the Al_2O_3 passivation layer can stabilise these hole carriers. Since Al_2O_3 has a relatively high potential barrier for hole carriers on the H-diamond surface, the Al_2O_3 passivation layer under the gate can confine and control the high concentration of hole carriers, thus enabling the application of a higher forward bias without significant gate leakage current [3.72].

A normally-off H-diamond FET using HfO_2 as gate oxide was first demonstrated by Liu et al in 2013. The HfO_2 gate oxide has a bilayer structure, which is fabricated by a sputter-deposition (SD) technique on a thin buffer layer prepared by an atomic layer deposition (ALD) technique. The leakage current density of the SD-HfO_2/ALD-HfO_2/H-diamond structure is smaller than 1.1×10^{-4} A cm^{-2} [3.74]. The HfO_2-gated FET has a p-type channel and normally-off characteristics. The maximum drain current of the FET with a gate length of 4 μm is −37.6 mA/mm [3.73]. This finding has encouraged the development of H-diamond normally-off type devices. They demonstrated that the SD-oxide/ALD-oxide stack structure is effective in developing the high-k/H-diamond MOSFET. This method can effectively prevent damage to the H-type diamond surface during SD deposition and solve the problem of the lack of suitable precursors for high-k materials prepared by ALD technology [3.74].

Kitabayashi et al. exhibited normally-off operation of a partial C-O channel C-H diamond MOSFETs with ALD-Al_2O_3 with more than 2000 V breakdown voltage [3.75]. The structure of the device is shown in Figure 3.4.6. They demonstrated that a partial C-O channel can control the threshold voltage, however, more advanced methods for surface oxidation need to be developed. At room temperature, the maximum drain current for

15μm gate length device is 20 mA/mm, and the drain off-current was well suppressed to 10^{-11} A/mm, and the on-off ratio was eight orders of magnitude [3.75].

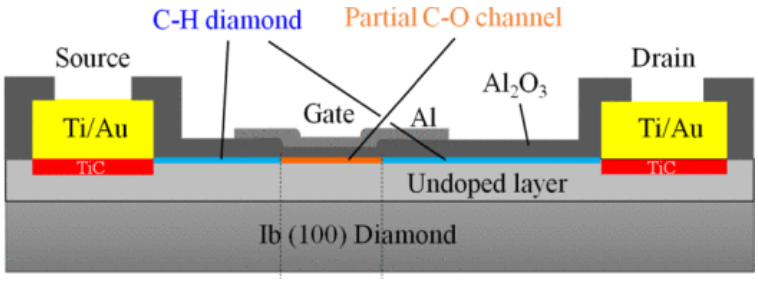

Figure 3.4.6 Schematic diagram of the C-H diamond MOSFET with partial C-O channel [3.75].

Some of the key performance parameters of various diamond FETs reported in the literature have been extracted and categorised in Table 3.4.1.

Year	Gate length (um)	Gate dielectric	$I_{d,\ max}$ (mA/mm)	Gm (mS/mm)	V_{th} (V)	f_T (GHz)	f_{max} (GHz)
1994	10	/	1.6	200	-2		
2006	0.1	/	550	143		45	120
2007	0.25	Al_2O_3 3nm	–790		-0.9	45	
2012	0.05	/	295	78 (extrinsic)		90 (intrinsic)	53 (extrinsic)
2012	0.4	Al_2O_3 17nm	1.35	135 (intrinsic)	11	15	33
2013	4	HfO_2 (SD 30.1 nm / ALD 4.0 nm	–37.6	11.2 (extrinsic)	-1.3	/	/
2013	10	$LaAlO_3$ (26.8 nm, SD) / Al_2O_3 (4.3 nm, ALD)	–7.5	2.3	-3.6	/	/
2016	2	V_2O_5 10nm	280	80 (extrinsic)	0.8	2.1	5.3
2017	4	MoO_3 10nm	33	29	0.70	/	/
2017	5	ALD-Al_2O_3 200 nm	18.2	1.2	–2.5	/	/
2025	1	E-beam+ALD-Al_2O_3 50nm	80	35 (intrinsic)	<-6	/	/

Table 3.4.1 A summarised table of key performances of different reported diamond FETs.

From a device-structure perspective, early hydrogen-terminated diamond FETs mainly exhibited normally-on behaviour due to the surface conductivity induced by the transfer

doping mechanism, which enables channel formation at zero gate bias. Subsequent developments focused on improving device performance through scaling of gate length, optimisation of contact materials, and the introduction of insulating or high-k dielectric layers to suppress gate leakage and enhance electrostatic control. As reviewed above, these efforts led to substantial improvements in drain current density, transconductance, and high-frequency performance, particularly in MESFET and MISFET configurations employing surface transfer doping. However, many of these high-performance demonstrations relied on device structures which lack the complete channel pinch-off, thereby limiting the realisation of stable and reproducible normally-off operation.

It is noteworthy that, despite the promising intrinsic properties of diamond and the significant performance improvements demonstrated over the past decades, relatively few recent studies have reported substantial and reproducible breakthroughs in diamond FETs performance. As listed in Table 3.4.1, many of the highest reported drain current densities, transconductance values, and high-frequency metrics were achieved prior to 2017, with subsequent progress largely characterised by incremental improvements rather than sustained scaling trends. More recent work has shown that further advances are possible through alternative device concepts, such as accumulation-channel hydrogen-terminated diamond FETs. However, such demonstrations remain limited in number. This apparent scarcity of recent high-performance devices does not reflect a lack of research interest, but instead highlights the considerable technical challenges associated with diamond device fabrication, including the extreme sensitivity of hydrogen-terminated surfaces to processing conditions, the difficulty of achieving stable and low-leakage gate dielectrics, and the challenge of realising stable normally-off operation. These limitations underscore the need for improved control of surface termination, oxide–diamond interfaces, and overall process stability, which form the central motivation for the experimental investigations presented in the subsequent chapters of this thesis.

3.5 Application context and potential uses of diamond FETs

Owing to its wide bandgap, high breakdown electric field, exceptional thermal conductivity, and intrinsic radiation hardness, diamond has long been regarded as a promising semiconductor material for electronic devices operating in extreme and harsh environments [3.76, 3.77]. In particular, diamond-based field-effect transistors (FETs) are well suited for applications where conventional silicon devices are limited by excessive leakage currents, thermal instability, or premature breakdown under high electric fields and elevated temperatures [3.76, 3.78].

One of the primary application domains for diamond FETs lies in high-temperature and high-power electronics. Diamond's superior thermal conductivity enables efficient heat dissipation at the device level, thereby mitigating self-heating effects that commonly degrade the performance and reliability of power transistors [3.76, 3.77]. Consequently, diamond FETs have been proposed for use in power conversion systems for aerospace and automotive platforms, as well as for downhole and geothermal electronics, where ambient temperatures can exceed the safe operating limits of conventional semiconductor technologies [3.78].

In addition to high-temperature operation, the radiation hardness and chemical inertness of diamond make diamond FETs attractive for space, nuclear, and defence-related applications [3.76, 3.77]. Diamond-based devices have demonstrated resilience to high-energy particle irradiation and harsh chemical environments, which is critical for electronics deployed in space missions, nuclear instrumentation, and radiation-rich sensing and control systems [3.76, 3.77]. For defence and radar applications, diamond FETs are also of interest for high-frequency and high-voltage radio-frequency (RF) electronics, where high breakdown fields and low parasitic effects are essential for achieving high output power density and long-term operational stability [3.25, 3.58, 3.79].

When compared with other wide-bandgap semiconductors such as silicon carbide (SiC) and gallium nitride (GaN), diamond offers distinct advantages in terms of thermal management capability and theoretical breakdown performance [3.76, 3.78]. While SiC and GaN technologies are more mature and currently dominate commercial high-power and RF markets, diamond is often viewed as a niche but enabling material for applications that demand extreme reliability, ultra-high power density, or operation under combined electrical, thermal, and radiation stress [3.80]. As a result, diamond FETs are not intended to universally replace SiC or GaN devices, but rather to complement existing wide-bandgap technologies in specialised application spaces [3.76, 3.80].

Despite this strong application potential, the widespread deployment of diamond FETs remains constrained by several technological challenges. In particular, reliable control of surface conductivity, stable gate modulation, low gate leakage currents, and reproducible normally-off operation are critical requirements for industrial and defence-oriented electronics [3.9, 3.26, 3.71]. These application-driven constraints directly motivate the research focus of this thesis on oxide–diamond interface engineering, surface transfer doping control, and the optimisation of accumulation-channel hydrogen-terminated diamond MOSFETs [3.9, 3.71]. Addressing these challenges is essential for bridging the

gap between laboratory-scale demonstrations and practical diamond-based electronic devices suitable for harsh-environment applications [3.76, 3.80].

3.6 Summary

This chapter has reviewed diamond-based electronics from both a fundamental and application-oriented perspective. Section 3.1 introduced the surface transfer doping mechanism, which is crucial for inducing a two-dimensional hole gas (2DHG) on hydrogen-terminated diamond surfaces, thereby enabling conductivity without traditional impurity doping. Section 3.2 explored alternative surface terminations, such as oxygen and fluorine, which can be engineered to produce either positive or negative electron affinity. Section 3.3 examined strategies for forming low-resistance ohmic contacts on H-diamond, including the formation of metal carbides at the interface to enhance thermal stability. In Section 3.4, various field-effect transistor architectures, including MESFETs, MISFETs, and MOSFETs, were discussed. This section also covered the evolution of H-diamond devices from the perspectives of device architecture and the dielectric materials used to enhance performance and stability.

Overall, this review highlights that while substantial progress has been made in demonstrating high-performance H-diamond FETs for high-temperature, high-power, and harsh-environment applications, several critical research gaps remain. In particular, reliable control of surface transfer doping, stable gate modulation, and reproducible normally-off operation are still strongly dependent on oxide selection, surface termination, and processing conditions. Moreover, relatively limited attention has been given to the long-term stability and reproducibility of diamond device fabrication processes, despite their importance for scalable and industrially relevant applications. These identified gaps directly motivate the subsequent chapters of this thesis, which focus on oxide–diamond interface engineering, process optimisation, and stability-aware device design to enable robust accumulation-channel hydrogen-terminated diamond MOSFETs.

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4. Fabrication process

In the field of semiconductor fabrication, sample preparation is a crucial fundamental step, as any contaminants on the sample surface (such as dust, organic residues, and metal ions) may be amplified in subsequent processes, leading to pattern defects or device leakage. Therefore, a strict sample preparation process can effectively ensure the stability of fabrication.

This chapter provides a detailed introduction to the preparation of diamond samples, including basic methods for cleaning and recycling, as well as the fabrication process based on photolithography and electron beam lithography (EBL). In the final section of this chapter, the entire process flow of fabricating diamond MOSFETs will also be presented.

4.1 Sample preparation

In this research, CVD-grown (100) single-crystal diamond samples were purchased from Element Six, the main sample sizes used are 3 mm x 3 mm and 5 mm x 5 mm, with roughness under 2nm RMS. The diamond sample preparation process is shown in Figure 4.1.1. The Atomic Forces Microscope (AFM) is an effective method to measure the surface roughness before and after all the steps during the sample preparation process. AFM theory will be introduced in detail in Chapter 5.3.

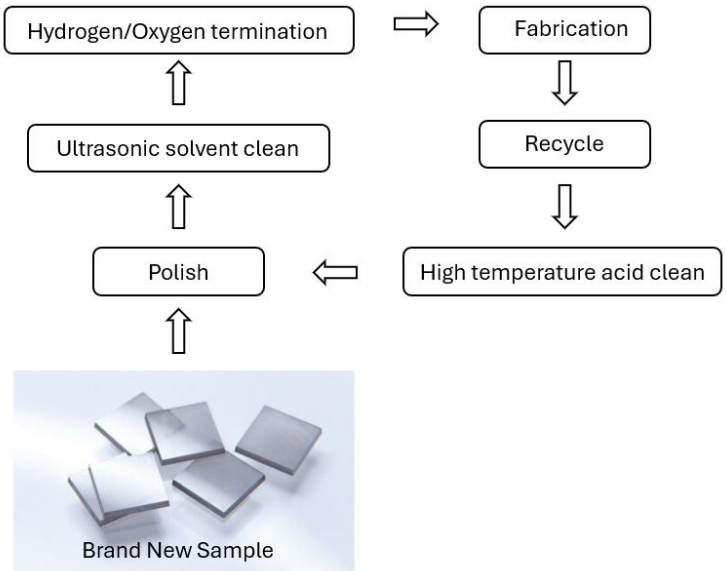

Figure 4.1.1 Diamond sample preparation process flow.

A rough surface with defects will trap more charges and enhance the scattering phenomena, which will lead to a relatively low mobility [4.1,4.2]. Hence, the polishing

process is necessary to reduce the surface roughness, and the ideal surface roughness of a polished diamond sample is under 1nm. The polishing was done by Technical Diamond Polishing in this research. A standard AFM scan result of a polished diamond surface is shown in Figure 4.1.2.

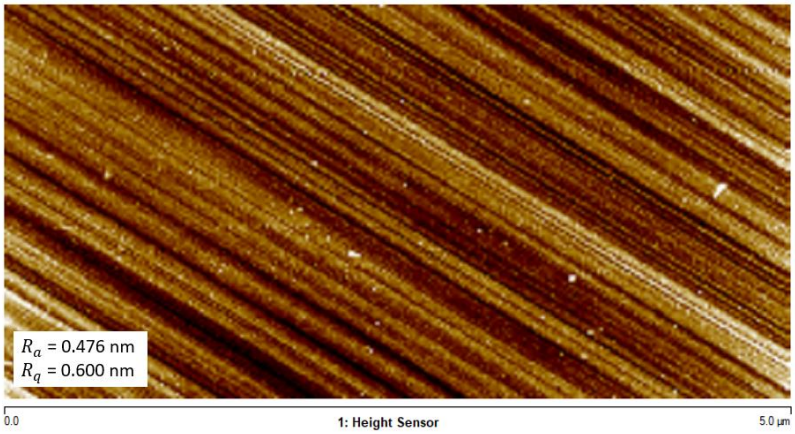

Figure 4.1.2 AFM result of a polished diamond surface.

From the scan, the polish trace is clearly visible, and some small white dots here are considered contamination from polishing and the transferring process. The main roughness result obtained from the AFM scan is the average roughness. R_a and root mean squared roughness R_q (RMS). As shown in Figure 4.1.2, both R_a and R_q can be controlled under 1nm after polishing.

The next step is ultrasonic solvent cleaning with acetone and isopropyl alcohol, which is useful for removing small contaminants from the transfer process and the surrounding air environment. The ultrasonic cleaning process involves three sequential stages. First, a 5-minute ultrasonic rinse in acetone to remove any unexpected surface contaminants. Next, the sample has to be cleaned in isopropyl alcohol (IPA) using ultrasonics for additional 5 minutes. This step ensures the removal of residual acetone from the initial stage. Crucially, the sample must be transferred to IPA after the acetone rinse to avoid acetone evaporation on the surface. If acetone dries on the surface, it will leave non-ideal residues, which will affect subsequent fabrication steps. The final step is to rinse the sample in R.O. water for 30 seconds to remove all the chemicals left on the surface and then dry the sample properly.

For various experimental purposes, diamond samples usually require different surface termination treatments, such as hydrogen termination and oxygen termination. The specific surface termination processes will be discussed in Chapter 6. Following these terminations, the diamond substrate needs to be characterised before any fabrication

process, as the surface roughness is influenced during the termination process [4.3, 4.4]. An AFM scan is essential to compare the changes in roughness before and after termination, as mentioned above. Additionally, Hall measurements are carried out to confirm surface conductivity, ensuring that hydrogen/oxygen termination has been achieved. Hall measurements will be explained in Chapter 5.1. The final step is to clean the sample once again to ensure it is in good condition for the subsequent fabrication process.

4.2 Sacrificial layer on H-diamond

H-diamond exhibits high surface conductivity through a surface transfer doping mechanism, which depends on the presence of 2DHG on the surface and atmospheric adsorbents. However, this termination is highly sensitive to nanofabrication processes, such as resist spinning, plasma etching, and solvent exposure [2.24]. To protect the hydrogen termination in these steps, a sacrificial layer is usually exploited immediately after the sample preparation stage.

The sacrificial layer, serving as a temporary surface protective barrier, prevents damage from oxygen plasma, photoresist solvents, and reactive etching while maintaining surface conductivity. It can also be selectively removed without affecting the hydrogen termination. Common sacrificial materials include thin gold (Au) films and residue-free dielectric layers, such as ALD Al_2O_3.

Gold thin films, typically 50 nm thick in this research, were deposited by e-beam evaporation, and due to their good chemical inertness, gold can effectively protect the H-terminated surface from damage during subsequent plasma treatment and lithography. Gold can be selectively etched off by potassium iodide/iodine (KI/I_2) solution. The mechanism of gold removal by KI/I_2 solution is based on an oxidation–reduction reaction. Molecular iodine (I_2) oxidises gold to Au^+ ions, which subsequently form soluble AuI_2^- complexes in the presence of iodide (I^-). This reaction can proceed smoothly in aqueous solution at room temperature. The simplified reaction can be expressed as:

$$Au + I_2 + I^- \rightarrow AuI_2^- \tag{4.2.1}$$

This reaction process is gentle and exhibits good chemical compatibility with the H-diamond surface. However, if the gold is not completely removed, it may result in poor adhesion during the metallisation step, impacting the film-forming quality of the ohmic electrode.

Another sacrificial layer used in this study was the residue-free ALD Al_2O_3 with a thickness of 15-20nm. The deposition process is typically carried out in a high vacuum

and at temperatures below 200°C, ensuring high consistency and coating quality while providing good protection for the H-diamond surface. Its main advantages are high cleanliness, no residue after removal, and no negative impact on subsequent electrode deposition and device performance. ALD films can be removed by wet chemical etching, using either buffered oxide etchant (BOE) or diluted hydrofluoric acid (HF).

Importantly, sacrificial layers usually need to be replaced or renewed at different stages of fabrication. This is because a single sacrificial layer cannot offer continuous protection throughout the entire process flow. For example, after oxygen plasma cleaning or metal deposition, the original sacrificial layer may be partially damaged, contaminated, or no longer compatible with subsequent steps. Therefore, it is necessary to remove the previous sacrificial layer and deposit a new one for the next stage of fabrication. This layer-by-layer replacement strategy ensures surface cleanliness, device reliability, and compatibility with subsequent processing steps.

4.3 Resist spinning & baking

Photolithography is a fundamental fabrication technique for transferring patterns onto substrates with high precision and accuracy. The spin coating of photoresist plays a crucial role in this process, as it determines the resolution, uniformity, and reliability of the subsequent patterning [4.5]. Spin coating is a widely used technique for applying a thin, uniform resist film to a substrate. Photoresists are broadly categorised into positive and negative photoresists [4.6]. For positive photoresist, the exposed regions become more soluble in the developer because of a photochemical reaction that breaks down the polymer chains. This type provides better resolution and is commonly used in delicate patterning. Conversely, for negative photoresist, the exposed areas become less soluble due to cross-linking caused by exposure. It is more resistant to etching and is frequently employed for thicker or mechanically stronger resist layers. In this research, thick photoresists, such as the SU-8 series and Electron beam resists like PMMA, are mainly used.

The process involves dispensing a liquid resist onto the centre of the wafer, which is then rapidly spun at high speed. Centrifugal force spreads the resist outward, and solvent evaporation during spinning leads to the formation of a uniform film, as shown in Figure 4.3.1.

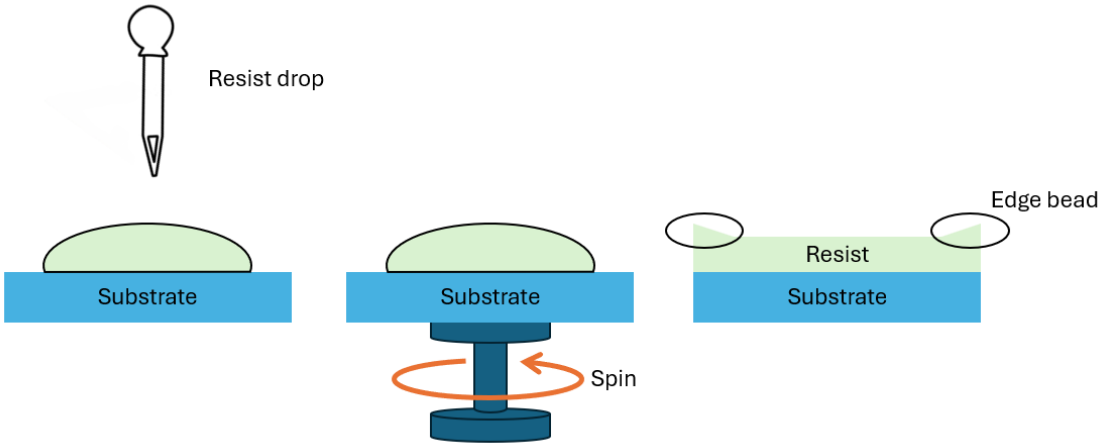

Figure 4.3.1 Resist spinning process.

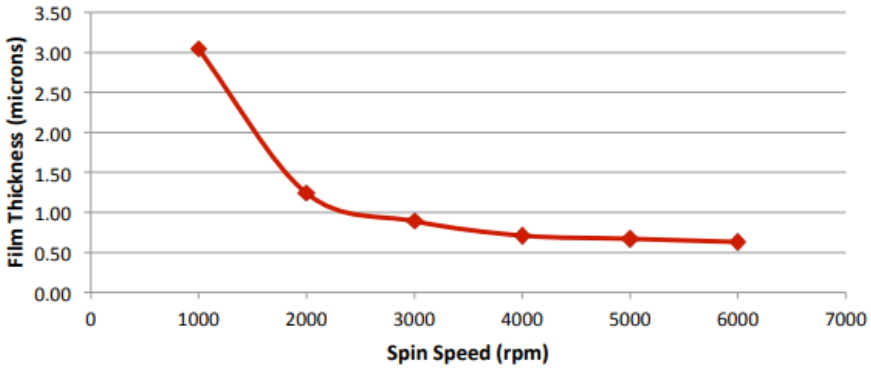

Figure 4.3.2 Example relationship curve between photoresist thickness and spin coating speed [4.7].

The photoresist thickness (t) depends on spin speed, resist viscosity, spin duration, acceleration profile, ambient temperature, and humidity in the cleanroom [4.6].

The relationship curve between photoresist thickness and spin coating speed is shown in Figure 4.3.2. As the spin coating speed increases, the thickness of the photoresist decreases. The commonly used recipes in this research will be presented in Appendix A.

After spinning, the resist layer undergoes a baking step to remove residual solvents, enhance adhesion, and ensure film uniformity. This heat treatment is typically performed on a hot plate, with the baking temperature and duration depending on the type of resist and substrate. Proper baking can stabilise the photoresist film, reduce the formation of edge beads, and increase its resistance to flow or deformation during subsequent exposure [4.6]. However, excessive baking may decrease the sensitivity of the photoresist, while insufficient baking will leave residual solvents that can interfere with the clarity and development of the pattern.

Apart from its primary role in pattern transfer, photoresist can be applied in multiple layers to support the metal lift-off method during device fabrication. After lift-off or other resist-based processes, the remaining resist has to be thoroughly removed to avoid contamination or interference with subsequent steps. To achieve this, acetone and isopropanol (IPA) are commonly used for cleaning or dissolving residual resist. For clearer removal, especially in cases of stubborn or cross-linked resists, specialised strippers such as SVC-14 and Micro-posit Remover 1165 are typically used.

4.4 Photolithography exposure

Photolithography exposure is a fundamental step in the microfabrication process that enables the precise transfer of patterns from a mask to a photoresist-coated substrate using UV light. The photomask is a core component used for pattern transfer in the photolithography process. Its main function is to transfer the required micro-patterns to the surface of the photoresist in the form of light-blocking and light-transmitting areas during the exposure process. As a kind of "template", the mask defines the geometry, size and arrangement of the final graphic. During the photolithography exposure process, UV light shines on the photomask and can only penetrate through the transparent area to the photoresist layer. Depending on the type of photoresist (positive or negative), solubility changes will occur in the exposed area, thereby achieving the transfer of the pattern. The schematic diagram of the UV light exposure process is shown in Figure 4.4.1.

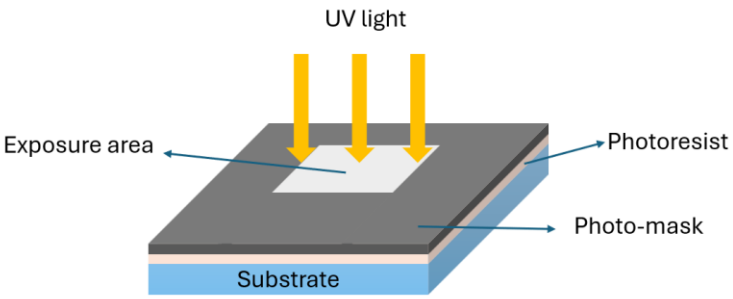

Figure 4.4.1 A schematic diagram of pattern transfer using UV exposure and photomask.

In this research, the Mask Aligner 6 (MA6) is mainly used for pattern transfer. MA6 is a manual mask alignment exposure machine. The mask will be held on the chuck by vacuum, and the tray can be replaced according to the mask size. After confirming that the pattern to be transferred is facing down, turn on the vacuum to hold the mask with the tray and place them on the stage. The MA6 system is shown in Figure 4.4.2.

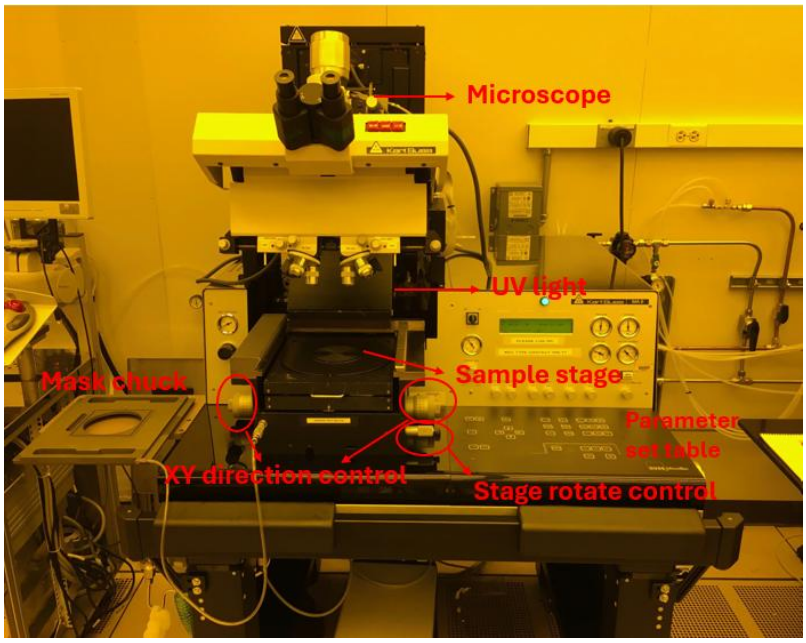

Figure 4.4.2 MA6 photolithography exposure system.

Based on the requirements of device design, multi-layer geometric alignment is usually required. The alignment markers on the mask and the sample are observed through a microscope. The XY direction and rotation angle are manually adjusted for fine-tuning to make the patterns precisely overlap. This is particularly crucial in the manufacturing of devices involving multi-layer structures. The alignment process is shown in Figure 4.4.3.

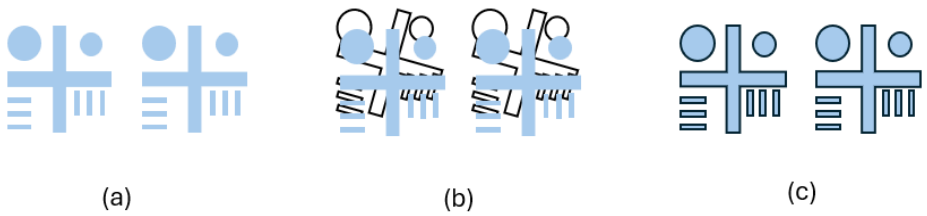

Figure 4.4.3 Alignment process (a) patterns on the sample, (b) dynamic process of how to align the patterns on the sample with the alignment markers on the mask, (c) final aligned markers and patterns.

Whether photolithography or electron beam exposure (EBL), alignment accuracy directly affects the integrity of the device structure, electrical performance. Used in photolithography systems, it performs graphic positioning by recognising the preset alignment mark on the wafer, and the general accuracy in this research can reach 2 microns.

After the alignment, the mask will come into hard contact with the sample, offering high resolution but also potentially damaging the mask. Therefore, the alignment gap needs

to be strictly controlled, as an overly large alignment gap can also lead to misalignment. The exposure time of photoresist is determined by its response intensity to ultraviolet light during the photolithography process, thereby affecting key parameters such as resolution, line width, and edge roughness of the pattern [4.6]. Different types of photoresists have different requirements for exposure time due to their varying photosensitivity, thickness, absorption coefficient and chemical reaction efficiency [4.6]. The specific photoresist and the recipe for standard exposure times are presented in Appendix A.

4.5 EBL exposure

Electron beam lithography (EBL) is a high-resolution, maskless lithographic technique that utilises a focused electron beam to write patterns directly onto electron-sensitive resists. Owing to its exceptional resolution, EBL has become a critical tool in nanofabrication and the development of advanced research devices. Similar to photolithography, positive EBL resists (such as PMMA) undergo polymer chain scission upon electron exposure, thereby increasing their solubility in developer solutions. In contrast, negative EBL resists (such as HSQ) experience cross-linking, which reduces solubility in the exposed regions. Since EBL is a direct-write, maskless process, it offers the design flexibility and is particularly well-suited for small-batch production, complex geometries, and iterative design cycles. The standard EBL process flow is illustrated in Figure 4.4.1.

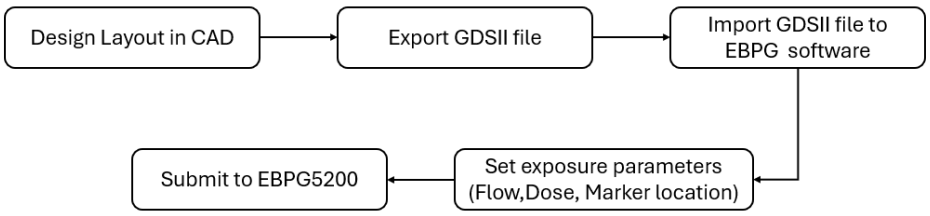

Figure 4.5.1 EBL design and exposure process flow.

The final exposure step was performed by staff at the James Watt Nanofabrication Centre (JWNC), utilising the Raith EBPG5200 electron beam lithography system. The EBPG5200 utilises a thermal field emission gun (FEG) to generate a highly coherent electron beam, with an adjustable beam energy typically ranging from 20 keV to 100 keV. The electron beam is accelerated and focused by a series of electromagnetic lenses, which reduces the beam spot size and enables nanoscale resolution [4.8]. A simplified schematic of the EBPG5200 system is shown in Figure 4.5.2.

Different from photolithography, which relies on projection through a photomask, the EBPG5200 draws patterns directly onto the resist using either raster or vector scanning modes. The beam deflection is controlled via a high-speed digital-to-analogue converter (DAC), which directs the beam to trace the desired layout as defined in the input GDSII file [4.9].

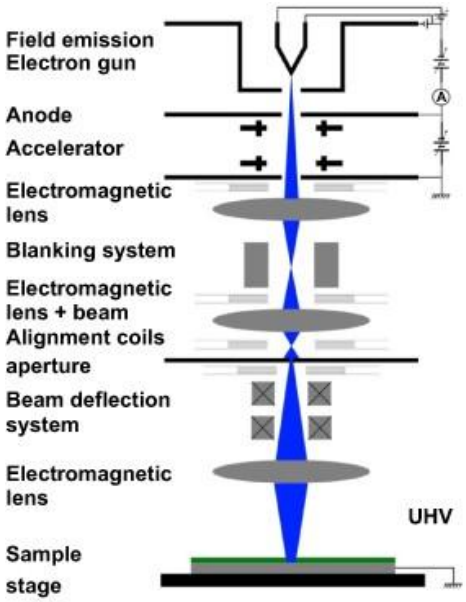

Figure 4.5.2 Simplified EBPG electron beam lithography system [4.8].

The EBPG5200 also features a fully automated alignment and calibration system, which operates using predefined alignment markers embedded in the GDSII layout. As shown in Figure 4.5.3, each corner of the sample contains a 20 μm square alignment mark. During alignment, the system reads the coordinates of these fiducials and adjusts the beam position accordingly to ensure precise overlay. To enhance the visibility of alignment marks in the electron image, high atomic number metals, such as gold (Au), are typically used due to their higher backscattered electron yield.

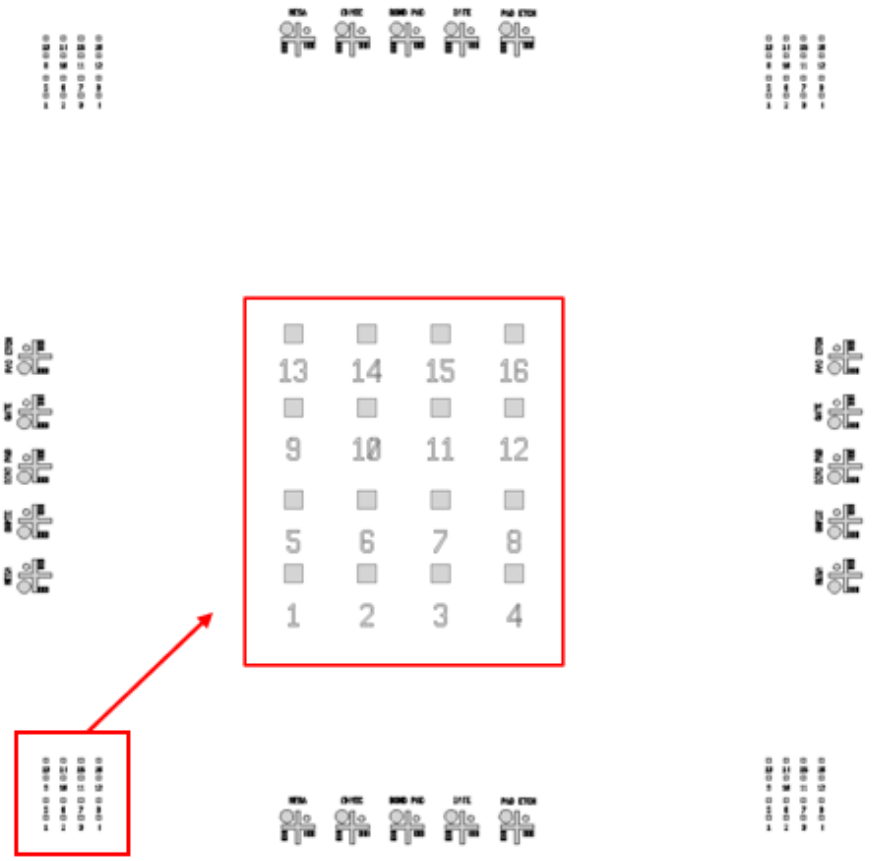

Figure 4.5.3 EBL alignment markers.

4.6 Resist development

After exposure, the resist undergoes a development process to selectively remove either the exposed or unexposed regions, depending on the resist, resulting in the formation of physical patterns on the substrate. As mentioned in the previous chapters, the polymer chains of positive photoresist (such as PMMA) break after exposure to the electron beam; hence, it is more soluble in the developer solution and can be removed after development.

The quality of the pattern transfer is highly sensitive to the interaction among the exposure dose, the chemical properties and concentration of the developer, and the development time. These parameters must be carefully balanced to ensure appropriate image contrast, resolution and feature retention. Different photoresists require specific developers, and their dissolution strength and interaction with the exposed photoresist area vary, for example, for PMMA, the standard developer used in this experiment is MIBK: IPA (1:2.5). Increasing the proportion of MIBK (a stronger solvent) can accelerate the development, but it will reduce the contrast and cause rough line edges. The exposure dose determines the amount of energy deposited into the photoresist. For

positive photoresists, a higher dose or a longer developing duration will increase the breakage of polymer chains, thereby making the photoresist more soluble. Therefore, the developing time must match the exposure dose. Insufficient exposure and too short developing time can lead to incomplete pattern formation and residual photoresist. Overexposure and longer development can cause the pattern to widen or result in the loss of small features. The development process is shown in Figure 4.6.1. The specific resist development recipe is presented in Appendix A.

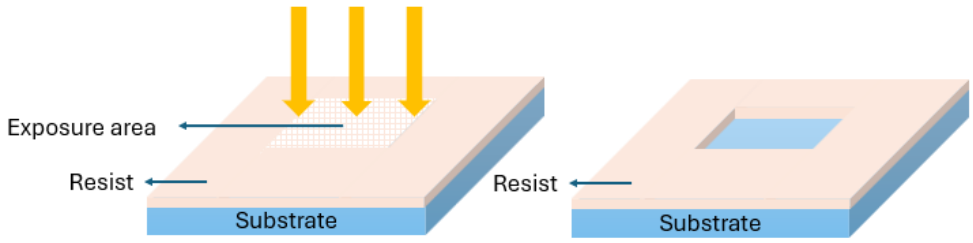

Figure 4.6.1 Positive resist development process.

After development, rinsing is essential to terminate the developer's activity and prevent overdevelopment of the resist pattern due to residual chemicals on the surface. It is important to note that different photoresists require different rinsing protocols. For instance, PMMA resists must be rinsed with isopropyl alcohol (IPA), which effectively halts the development reaction and preserves high-resolution features. In contrast, IPA is incompatible with the development chemistry of the S1800-series positive resists, such as S1805. Its use may lead to pattern deformation. Instead, these resists require rinsing with R.O. water to ensure clean and stable pattern profiles.

Following development and pattern transfer, resist removal becomes a critical step. Wet stripping methods using solvents such as acetone or photoresist removers are widely applicable; however, they may introduce problems, including incomplete removal, organic residues, or particle contamination. As an alternative or complement, plasma ashing is commonly applied after the resist developing process. This technique uses oxygen plasma to oxidise the organic components of the photoresist into volatile byproducts such as CO_2 and H_2O [4.10]. Plasma ashing is particularly effective in removing hard-baked or crosslinked resist residues, which are otherwise resistant to wet solvents. However, plasma ashing cannot directly act on the surface of hydrogen-terminated diamonds because plasma bombardment would damage the hydrogen termination.

4.7 Metallisation & Lift-off

Metallisation is a fundamental process in device fabrication, involving the deposition of conductive metal films onto substrates. In this experiment, the main purpose of metallisation is to form contact electrodes. The metallisation process introduces a conductive layer, typically defined by the photolithography-patterned region. This enables selective electrical connections between device components or between devices and external circuits. Metallisation is usually achieved through physical vapour deposition (PVD) technology. In this work the electron beam evaporation method is mainly used. The schematic diagram of the electron beam evaporation chamber is shown in Figure 4.7.1.

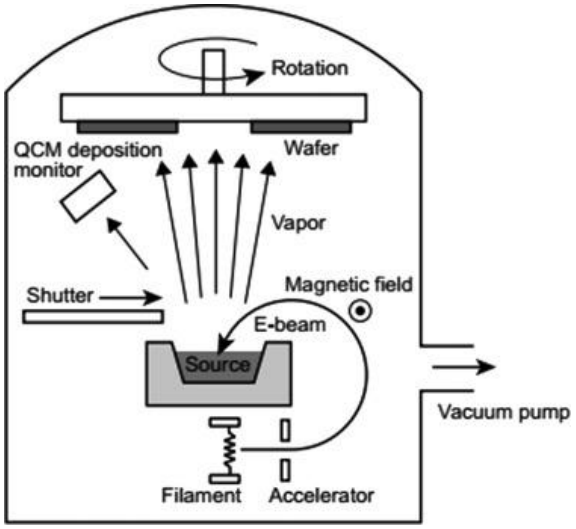

Figure 4.7.1 Schematic diagram of the Electron beam evaporation chamber used for metallisation [4.11].

Before deposition, the sample is mounted onto a holder stage, which ensures secure positioning and thermal contact during the evaporation process. To minimise contamination and preserve vacuum integrity, the sample is transferred into the main deposition chamber via a load-lock system. This intermediate chamber allows sample exchange without exposing the high-vacuum environment to atmospheric pressure. Once pumped down to an appropriate pressure, the load lock opens, allowing the sample to be introduced into the evaporation chamber, where it is aligned beneath the source, and deposition proceeds under controlled conditions.

During the electron beam evaporation process, the source material is placed in a crucible within a high vacuum (under $1 \times 10^{-6}\mathrm{mbar}$) chamber. The electron beam produced by the thermal-electron emitter and focused by the electromagnetic lens is directed towards the surface of the target material. The intense local energy causes the material to melt

and evaporate. Subsequently, the vapour travels in a straight line and condenses onto the substrate at a lower temperature, forming a film. The sample holder stage continues to rotate to ensure uniform deposition.

As mentioned in the previous section, bilayer photoresist or e-beam resist can be used for the metallisation process and liftoff. The process of metallisation and liftoff is shown in Figure 4.7.2.

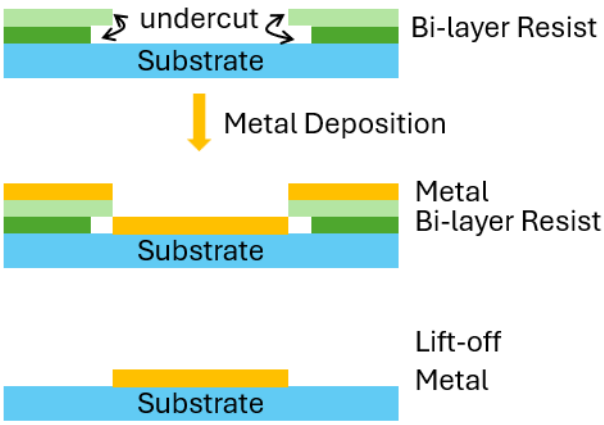

Figure 4.7.2 Metallisation and liftoff process.

Undercut refers to a lithographic resist profile in which the bottom portion of the resist layer is laterally recessed relative to the top, forming an overhanging sidewall. This structure is deliberately engineered to facilitate clean metal lift-off, ensuring that deposited metal only adheres to the substrate in the desired regions while minimising unwanted metal edge connection. In bilayer lithography, the pattern is entirely defined by the exposure of the top resist layer, which is sensitive to UV light in photolithography or to electrons in EBL. The bottom resist layer is typically either non-sensitive to radiation or only weakly responsive, and it has a faster dissolution rate in the developer. This differential development results in a lateral undercut beneath the exposed top layer, even though the bottom resist was not directly exposed. Because the metal is deposited over the developed profile, only the regions where the top resist was exposed and removed allow direct contact between the metal and the substrate. The undercut profile prevents continuous metal coverage over the resist sidewalls, which is essential for successful lift-off. In this study, bilayer lithography was employed using LOR-series resists (such as LOR 3A) as the bottom layer under a positive photoresist layer such as S1805. The LOR resist provides reliable undercut (0.5-1 microns) in this research.

Liftoff is used to selectively remove undesired metal materials after deposition, thereby defining patterned metal films. Metal will deposit on the entire surface of the sample, covering the exposed substrate and the areas covered by the resist. Finally, the sample is immersed in the specific solvent. The solvent will dissolve the resist, peel off the metal film along with the resist, and leave only the metal in the designed patterns. In this experiment, the photoresist is typically dissolved in SVC14, while the e-beam resist is usually dissolved in acetone. After soaking the sample in the solvent, it needs to be placed in a water bath at 50 degrees for at least two hours to ensure that the metal can be lifted off successfully.

4.8 Oxide deposition

In nanofabrication, oxide films play a crucial role in devices, such as gate dielectric layers, hard masks, and sacrificial layers. Oxides can be deposited with atomic layer deposition (ALD) and PVD, each offering advantages depending on the specific application requirements.

ALD is a gas-phase thin-film growth technique based on sequential, self-limiting surface reactions [4.12]. The process involves alternately pulsing precursor vapours onto the substrate surface, where each precursor chemically adsorbs or reacts with available surface functional groups [4.13]. Inert gas purging steps are inserted between pulses to remove excess reactants and by products, preventing gas-phase reactions. Precursors play a crucial role in ALD, as they have to be volatile, thermally stable, and highly reactive toward the surface species. Depending on their chemical form, precursors can be gaseous, liquid, or solid. Crucially, each precursor reacts only until the surface is saturated, enabling precise monolayer formation in a self-limiting manner [4.13]. This mechanism enables atomic-scale control over film thickness and the application of uniform, conformal coatings, even on complex structures. An example of the ALD Al_2O_3 deposition cycle is shown in Figure 4.8.1.

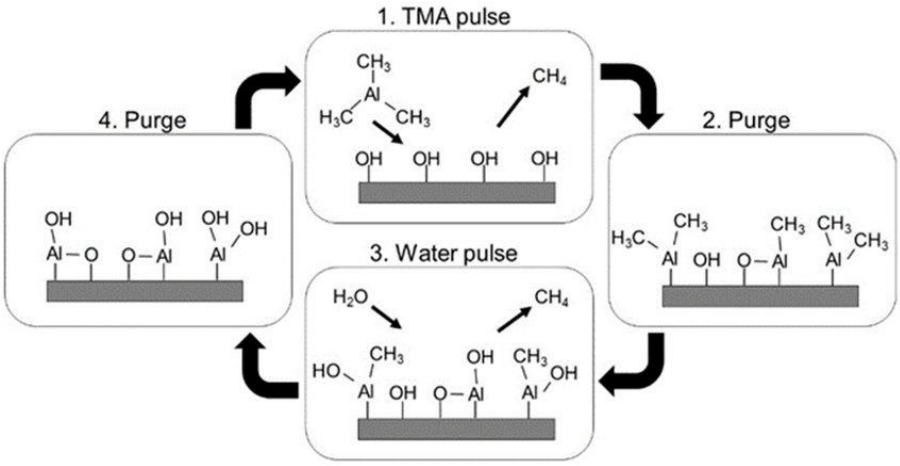

Figure 4.8.1 ALD deposition cycle of Al_2O_3 process [4.14].

In this process, TMA reacts with surface hydroxyl groups to form surface-adsorbed Al-CH_3, releasing methane in the process. After purging, H_2O is introduced and reacts with Al-CH_3 to form Al-OH, and further forms aluminium oxide. Approximately one atomic layer of aluminium oxide is deposited in each cycle. Based on this self-limiting feature, ALD has extremely high film uniformity and is suitable for high-k dielectric constant materials (such as Al_2O_3 and HfO_2). However, the disadvantage is that the deposition rate of ALD is relatively slow, it relies on high-purity precursors, and the cost is relatively high.

As mentioned in Section 4.7, physical vapour deposition (PVD) forms films by vaporising solid material in a vacuum, causing atoms or molecules to condense on the substrate. This category includes thermal evaporation and electron beam evaporation. In contrast, dielectric layers such as oxides and nitrides are commonly deposited using chemical vapour deposition (CVD) techniques. Among these, atomic layer deposition (ALD) is an advanced variant of CVD, which provides superior conformality and precise thickness control compared to line-of-sight PVD methods.

During the thermal evaporation process, the oxide solid material is placed in a crucible and heated by an electric current to raise its temperature above the evaporation point. The evaporated atoms travel in a straight line towards the cooler substrate and condense on its surface to form a film [4.15]. The entire process needs to be carried out under high vacuum (10^{-6} Torr) to prevent atoms from colliding with gas atoms to reduce the risk of contamination [4.15].

Similarly, electron beam evaporation is another high-vacuum PVD method. Focusing a high-energy electron beam on a solid oxide target causes local evaporation of the target

material. Under high vacuum conditions, the vapour deposits on a cooler substrate surface. The electron beam is generated by the thermal emission cathode and focused onto the surface of the target material in the crucible by a magnetic lens [4.15]. This method offers the advantages of a faster deposition rate compared to ALD and a more straightforward process. However, it is worth noting that, similar to thermal evaporation, the oxide films produced by electron beam evaporation also exhibit discontinuity and poorer uniformity compared to the ALD process.

As shown in Figure 4.8.2, ALD is a conformal process based on surface reactions, which can uniformly coat all exposed surfaces, including the vertical and even concave (bottom cut) side walls of photoresist patterns. Therefore, ALD films cannot be selectively removed by dissolving photoresist and thus are fundamentally incompatible with the stripping process. PVD evaporates the oxide to the substrate in a relatively linear trajectory. This leads to a significant discontinuity between the deposited film and the side walls of the photoresist, allowing the solvent to penetrate and lift the photoresist beneath.

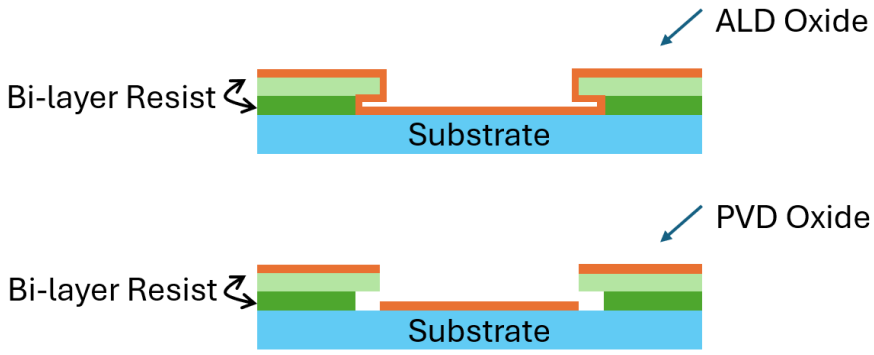

Figure 4.8.2 Schematic diagram showing coverage of PVD and ALD oxide deposition processes.

After the oxide deposition, the pattern of the thin film usually requires precise etching techniques. These methods are mainly divided into two categories: wet chemical etching and dry plasma etching. The choice of method depends on the thin film material, etching selectivity, resolution requirements and substrate compatibility. Wet etching refers to immersing the sample in a liquid chemical solution that selectively dissolves the oxide layer. Due to its simple operation and low equipment cost, it is widely used. Dry etching utilises ions and active free radicals generated by plasma to remove dielectric layers. It offers anisotropic etching profiles and superior pattern resolution, enabling a more precise definition of the area to be etched [4.18]. BOE is mainly used in this research to wet etch oxide layers due to its high selectivity and compatibility with photoresist.

On H-diamond, due to the influence of the surface transfer doping mechanism, the deposition of dielectric materials such as Al_2O_3, SiO_2 and HfO_2, will significantly affect its surface conductivity. This is because oxide deposition usually leads to the replacement or removal of atmospheric surface adsorbents. In addition, the charge changes at the interface between the oxide and H-diamond may lead to the suppression of hole accumulation. It is also worth noting that surface damage or alteration caused by high-energy substances or heating may destroy the hydrogen termination. The influence of different oxides on the hydrogen terminal will be elaborated in detail in Chapter 6.

4.9 Summary

This chapter outlines the fabrication process of H-diamond devices, focusing on both fundamental techniques and specific process flows. Beginning with the importance of maintaining a clean, uncontaminated surface. Subsequent sections describe the sequential fabrication steps, including resist spinning, photolithography exposure, and EBL exposure, which are employed to define features on the diamond surface. The development and removal of resist materials were discussed in terms of the critical formation of pattern profiles, undercut structures, and metal lift-off processes. Special attention was given to the role of sacrificial layers in protecting the hydrogen-terminated diamond surface throughout the fabrication. Furthermore, key processes such as metallization, dielectric deposition, and pad etching were introduced to achieve the specific design purpose. The chapter concluded with the full process flow for fabricating an accumulation-channel mode H-diamond MOSFET device, integrating all previously introduced steps.

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5. Characterisation Methods

This chapter describes the various techniques used to characterise processed diamond substrates, including Hall effect measurement theory for measuring carrier concentration, carrier mobility, and sheet resistance. Transmission line measurement (TLM) is used to calculate the contact resistance and sheet resistance between semiconductor materials and metals. Atomic force microscopy (AFM) is widely used to examine the roughness of diamond surfaces. Scanning electron microscopy (SEM) achieves high-resolution characterisation of the surface morphology and composition of materials by focusing an electron beam to scan the sample surface and collecting signals. In the following sections, the fundamental theories and calculation methods of diamond device analysis will also be introduced.

5.1 Surface characteristics

5.1.1 Hall effect measurements

The Hall Effect is one of the most critical methods for measuring carrier concentration, carrier mobility, and sheet resistance in semiconductors. It is widely used as a fast and straightforward measurement technique. The Hall effect was first discovered by Edwin Hall in 1879, which describes the difference in potential voltage that occurs on an electrical conductor in the presence of a magnetic field [5.1]. The theory of Hall effect measurement assumes that there is a flat and uniform conducting sample, and the current of carriers flows parallel to both sides of the sample. When a magnetic field B is applied perpendicular to the sample surface, the charge carriers will be deflected by the Lorentz force. The moving charge carriers will redistribute and create an electric field, at which point the lateral Lorentz force will be compensated. In the state of equilibrium between the electric field and the transverse Lorentz force, the transverse current through the sample surface is zero, and the Hall voltage can be measured between the symmetric sides of the sample. The schematic diagram of the Hall effect is shown in Figure 5.1.1.

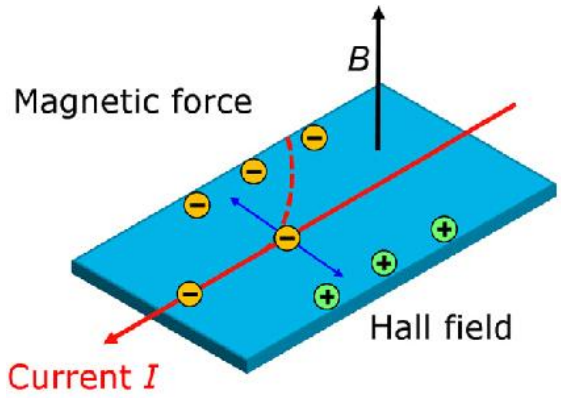

Figure 5.1.1 Schematic diagram of Hall Effect theory [5.2].

The Hall voltage is given by:

$$V_H = \frac{R_H I B}{d} \tag{5.1.1}$$

Where d is the thickness of the film, I is the current, B the magnetic field strength and the Hall coefficient can be defined as

$$R_H = \pm\frac{r}{q n_s} = \pm r\rho\mu \tag{5.1.2}$$

where r is the Hall scattering factor, which is normally defined as 1. $R_H > 0$ if the majority of carriers are holes (p-type) and $R_H < 0$ if the majority of carriers are electrons (n-type), q is the unit charge, n_s is carrier concentration [5.2-5.4]. Hence, the majority carrier concentration and the mobility can be calculated according to equations (5.1.3) and (5.1.4) when V_H and sheet resistance R_{sh} is known.

$$n_s = \frac{1}{q R_H} \tag{5.1.3}$$

$$\mu = \frac{R_H}{R_{Sh}} \tag{5.1.4}$$

The Van der Pauw (VDP) method was first proposed by Leo J. van der Pauw in 1958 [5.5]. It is a technique for the electrical characterisation of a given material that utilises the Hall effect. The sheet resistance R_{sh} of a sample that is homogeneous, isotropic, and of uniform thickness can be measured. Besides, the shape of the sample can be arbitrary, which means that when a sample has four different theoretical point ohmic (linear) contacts on its circumference, it can be characterised with the VDP method [5.6].

The basic principle is to apply a current and measure the voltage using four ohmic contacts of equal spacing on the material surface. Due to the symmetry of the design,

when applying a current between two adjacent contacts, for example, from 1 to 2, the corresponding voltage between 3 and 4 will create a symmetrical resistance around the structure. VDP measurement of different kinds of contact is shown in Figure 5.1.2.

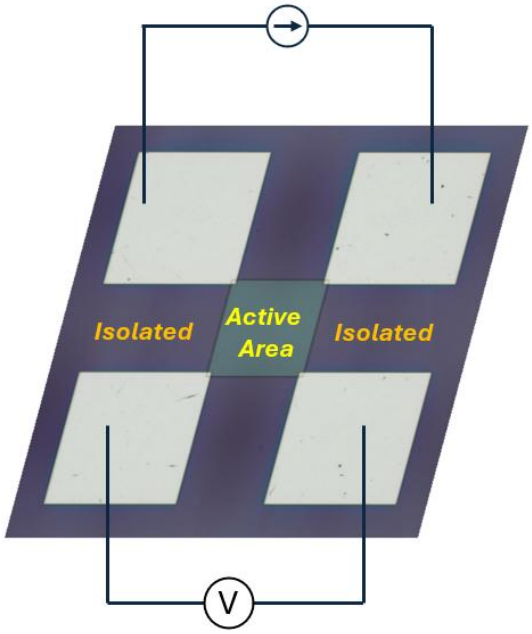

Figure 5.1.2 VDP measurement contact method.

Using Ohm's law,

$$R = \frac{V_{43}}{I_{12}} \tag{5.1.5}$$

Therefore, to calculate the sheet resistance,

$$R_{Sh} = \frac{\pi R}{ln2} \tag{5.1.6}$$

where R_{sh} is sheet resistance, and R is the measured resistance.

In addition to the contact method above, by applying a current between two non-adjacent contacts, the potential voltage difference between the two remaining contacts is then measured. In contrast, when a magnetic field B is applied perpendicular to the sample surface, this potential difference is the Hall voltage V_H. Therefore, referring back to equations (5.1.3), (5.1.4), and (5.1.6), the majority carrier concentration, carrier mobility, and sheet resistance can be calculated.

In this work, all the Hall measurements were carried out with the "Nanometric HL5500PC Hall measurement system". It is a station with four-probe micromanipulators and a fixed magnet with field reversal. The Hall kit system is shown in Figure 5.1.3.

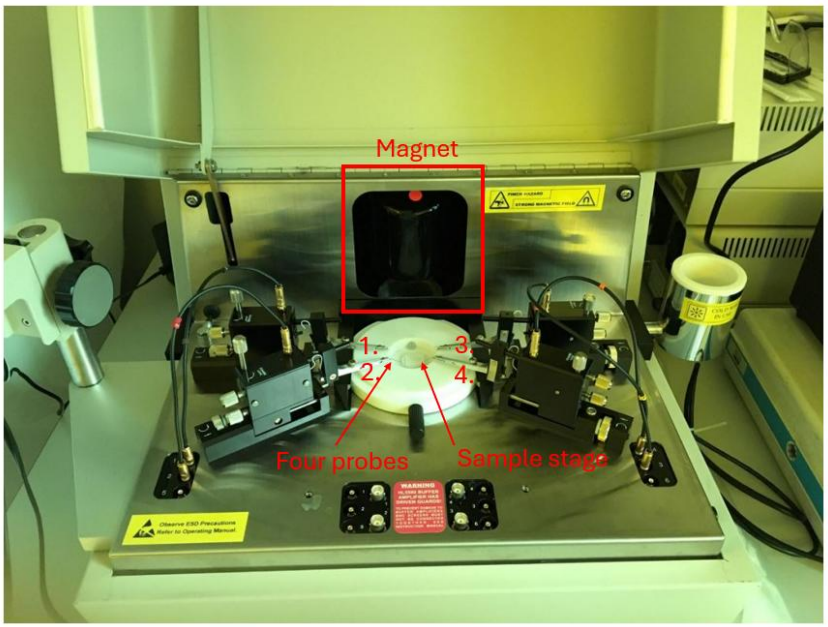

Figure 5.1.3 Nanometric HL5500PC Hall measurement system.

The VDP technique is essential for characterising materials because the current that a semiconductor can transmit is determined by the amount of charge that passes through a region per unit time. At the same time, the VDP technique is also the first step in analysing the diamond substrate in this work.

5.1.2 Transmission line measurements (TLM)

The ohmic contact between a metal and a semiconductor is an essential component of semiconductor devices. The contact resistance can be characterised as R_c and specific contact resistivity ρ [5.8]. Accurate measurement of contact resistance is crucial for understanding its impact on device performance.

Transmission line measurement (TLM) was proposed initially by Shockley [5.9]. The method consists of a series of metal contacts, with the distance between them increasing linearly. The schematic diagram is shown in Figure 5.2.1. In this example, the metal contacts have the same area and are spaced from L_1 to L_5. A potential difference is applied between two metal contacts with a known gap distance. The current between two contacts was measured, and the resistance was calculated according to Ohm's law. The dependence of the resistance on the contact gap is shown in Figure 5.1.6.

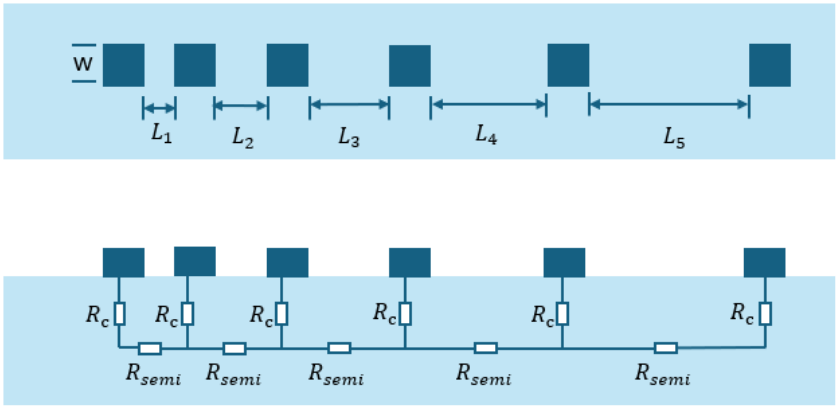

Figure 5.1.6 TLM structure with increasing gap distance between metal contact pads.

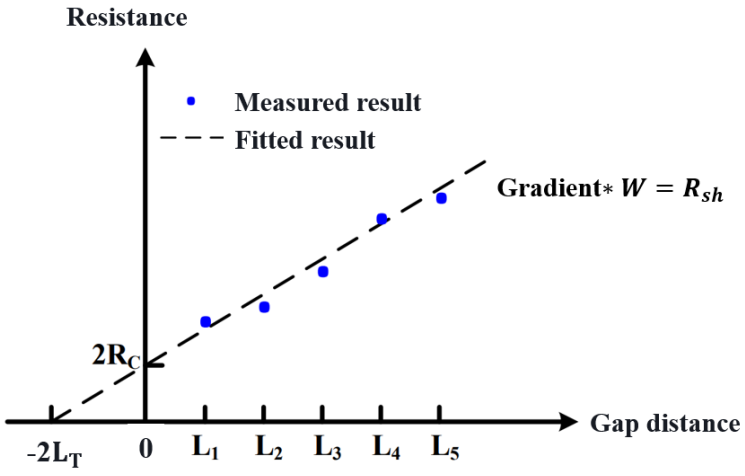

Figure 5.1.7 Example plot of measured total resistance with different gap lengths of TLM structure.

According to the TLM structure, the transfer length (L_T) represents the maximum length that the carrier travels in the semiconductor below the contact pad before flowing into the contact pad. Therefore, the effective conductive area of the contact is L_TW, the contact resistance is

$$R_c = \frac{\rho_c}{L_T W} = \frac{R_{sh} L_T}{W} \tag{5.1.12}$$

The total resistance R_T is

$$R_T = R_{semi} + 2R_c = \frac{R_{sh}}{W}(L + 2L_T) \tag{5.1.13}$$

As shown in Figure 5.1.7, the fitting line can be intended to be merged back to a distance of 0, which would be the case where the theoretical distance between two ohmic contacts is zero, which means $2L_T$ can be obtained from the intercept of the fitted curve and the X-axis, and the contact resistance R_c can be obtained from the intercept of the Y-axis. In addition, the sheet resistance R_{sh} of the substrate can be calculated from the slope of the fitted curve.

In this work, the ohmic contact resistance is reported as a width-normalised contact resistance with units of Ω·mm. This quantity represents the contact resistance per unit contact width and should be distinguished from the specific contact resistivity, which has units of Ω·m² and describes the intrinsic resistivity of the metal–semiconductor interface.

The width-normalised contact resistance (Ω·mm) does not represent a bulk or interfacial resistivity; rather, it is a practical metric widely used in lateral device structures to enable comparison of contact performance independent of contact geometry. This normalisation is particularly appropriate when the sheet resistance beneath the ohmic contact differs from that of the exposed channel region, as is commonly observed in hydrogen-terminated diamond due to its surface-conductivity-dominated transport.Therefore, in this work, contact resistances are consistently normalised to contact width and reported in units of Ω·mm to avoid assumptions regarding uniform sheet resistance beneath the contacts.

Compared to regular TLM structures, the circular TLMs (CTLM) offer a more straightforward approach for the rapid selection of suitable ohmic contacts, as they do not require an isolation stage to define the electrically active geometry of the TLM. CTLM uses a ring metal pad with the same radius but different radius differences from the contact; the schematic diagram is shown in Figure 5.1.8. The ring structure metal contact can effectively prevent the larger errors caused by leakage current, thereby improving the accuracy of the test. In this structure, current flows between the inner and outer metal pads.

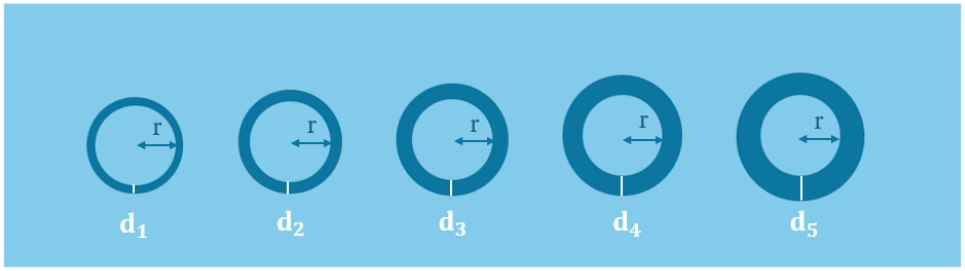

Figure 5.1.8 CTLM structure with increasing gap distance.

In theory, all ohmic contact resistances remain constant, while the channel resistance between the centre pad and the outer ring pad depends on the spacing between them (i.e., the difference in their radii). Similar to the TLM measurement method, a voltage is applied across a pair of pads with a defined spacing, and the resulting current flowing through the channel between the inner circle and the outer ring can be measured. The specific contact resistance R_c and sheet resistance can be obtained from the following equations [5.10].

$$R = \frac{R_{sh}}{2\pi}\left[\ln\left(\frac{r+d}{r}\right) + L_T\left(\frac{1}{r+d} + \frac{1}{r}\right)\right] \quad (5.1.14)[5.10]$$

where R is the resistance measured when a voltage is applied to the contact, R_{sh} is the sheet resistance, r is the inner diameter of the ring, and d is the radius difference, L_T is the transfer length.

As with the TLM analysis method, plotting the measured resistance with different gaps of CTLM structure gives a linear plot, the slope is $\frac{R_{sh}}{2\pi}$ and the intercept is $2R_c$.

In CTLM, the correction factor is used to account for deviations from ideal assumptions in the calculations of contact resistance and sheet resistance. This factor adjusts the resistance value of the measurement to provide more accurate measurement results that better reflect the actual material properties [5.11].

Correction factor c can be described by

$$c = \frac{r}{d} \cdot \ln\left(\frac{r+d}{r}\right) \quad (5.1.15)[5.11]$$

Since r and d are designed for known values, therefore, the correction factor can be calculated. Here, take $r = 50\mu\text{m}$ For example, the correction factors for different gap spacings are shown in Table 5.1.1.

Radius difference d [μm]	Correction factor
2	0.981
4	0.962
6	0.944
8	0.927
10	0.911

Table 5.1.1 Correction factors for different gap spacing, take $r = 50\mu\text{m}$ as example.

The experimentally measured CTLM data should be divided by these correction factors to obtain a value that can be used for linear fitting. Without these correction factors, the specific contact resistance would be underestimated.

5.1.3 Atomic Force Microscopy (AFM) technology

The atomic force microscope (AFM) belongs to a series of scanning probe microscopes invented in the 1980s, with the last product in this series being the AFM, developed by Binnig [5.12]. AFM shows a wide range of applications in studying the physical properties of surfaces. It is capable of imaging down to the sub-nanometre level to construct three-dimensional morphologies. With the right equipment and conditions, AFM technology can even image at atomic resolution [5.13]. Free from vacuum constraints, surfaces can be inspected in air and water environments, allowing the surface to be visualised in its usual or operating environment [5.14]. In this work, AFM plays a crucial role in characterising diamond samples, as it can measure the surface roughness with high resolution.

The two most common imaging modes of AFM are contact mode and tapping mode. There are two general approaches to contact mode imaging: constant height and constant force. The constant force is the most widely used [5.15]. In constant-force contact mode AFM, when the probe tip scans the surface, it encounters surface areas with different heights, resulting in a change in the deflection of the cantilever. The feedback loop then adjusts the height of the probe to maintain a constant deflection and force between the probe and the sample. This height variation is used to generate topographic information in the image [5.14]. In tapping-mode AFM, the cantilever oscillates near its resonant frequency, and as the tip approaches the sample, the oscillation is affected by tip–surface interactions [5.15]. A schematic of the AFM system is shown in Figure 5.1.9 [5.16].

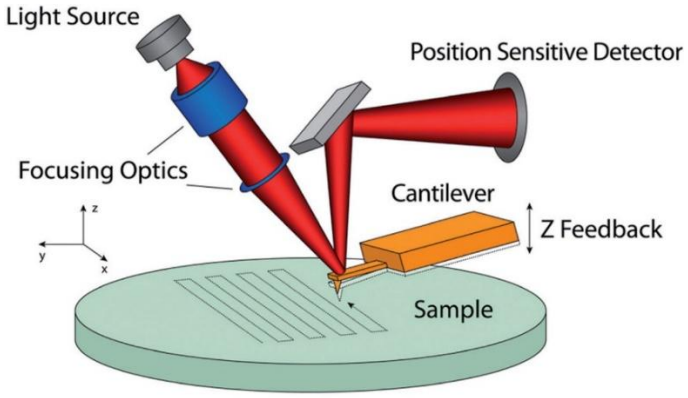

Figure 5.1.9 The schematic system of an AFM [5.16].

Because roughness changes the surface area that can be contacted, it plays a key role in determining the extent and nature of contamination on the surface of the sample. This means that the smoother the surface of the sample, the smaller the contact area with contamination. In this work, the main parameter is the roughness average R_a and root mean squared surface roughness R_q (RMS). The roughness average R_a represents the simple average of the mean absolute deviation from the mean sample height on the measured area, R_q can be defined as the root mean square of the height deviations taken from the mean line or surface.

It is important to note that these two values are affected by the scan size, and for larger scan sizes, larger surface features may become visible, resulting in a larger range of feature heights included in the scan, which adds to the statistical description of height changes [5.13]. Here is an example of an AFM scan result of a clean diamond surface, shown in Figure 5.1.10.

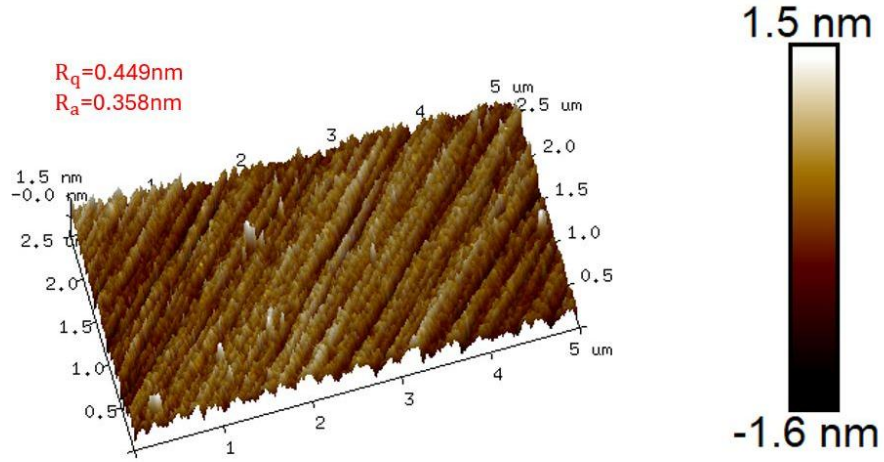

Figure 5.1.10 Example surface roughness result from AFM.

By definition, the root mean square (R_q) is always greater than or equal to the arithmetic mean (R_a) for any set of non-identical numbers. This stems from the quadratic mean-arithmetic mean inequality, where $R_q \geq R_a$. Real surfaces always exhibit variability in height deviations. The squaring process in R_q amplifies the influence of larger peaks and valleys, ensuring $R_q > R_a$. This makes R_q a more sensitive metric for detecting surface irregularities.

5.1.4 Scanning Electron Microscopy (SEM) technology

The Scanning Electron Microscope (SEM) is a high-resolution microscopic technique that uses the interaction between the electron beam and the sample to generate various

signals (such as secondary electrons, backscattered electrons, X-rays, etc.) to obtain the surface morphology, composition distribution and crystal structure of the sample. The resolution range of SEM instruments is from 1 nanometre to several nanometres.

SEM emits electrons through an electron source. After being accelerated by high voltage (1k eV to 30k eV). The electrons form an electron beam with uniform energy. The electron beam is converged through the condenser lens. The focused electron stream is projected and scanned onto the sample surface, and various signals generated are collected using a dedicated detector. The electrons in the electron beam interact with the atoms in the sample, generating various signals that can be used to obtain information about the surface morphology and composition. The position of the electron beam is correlated with the intensity of electrons captured by the detector using software, and the images can be viewed in real-time on an external monitor. The schematic of the SEM working system is shown in Figure 5.1.11.

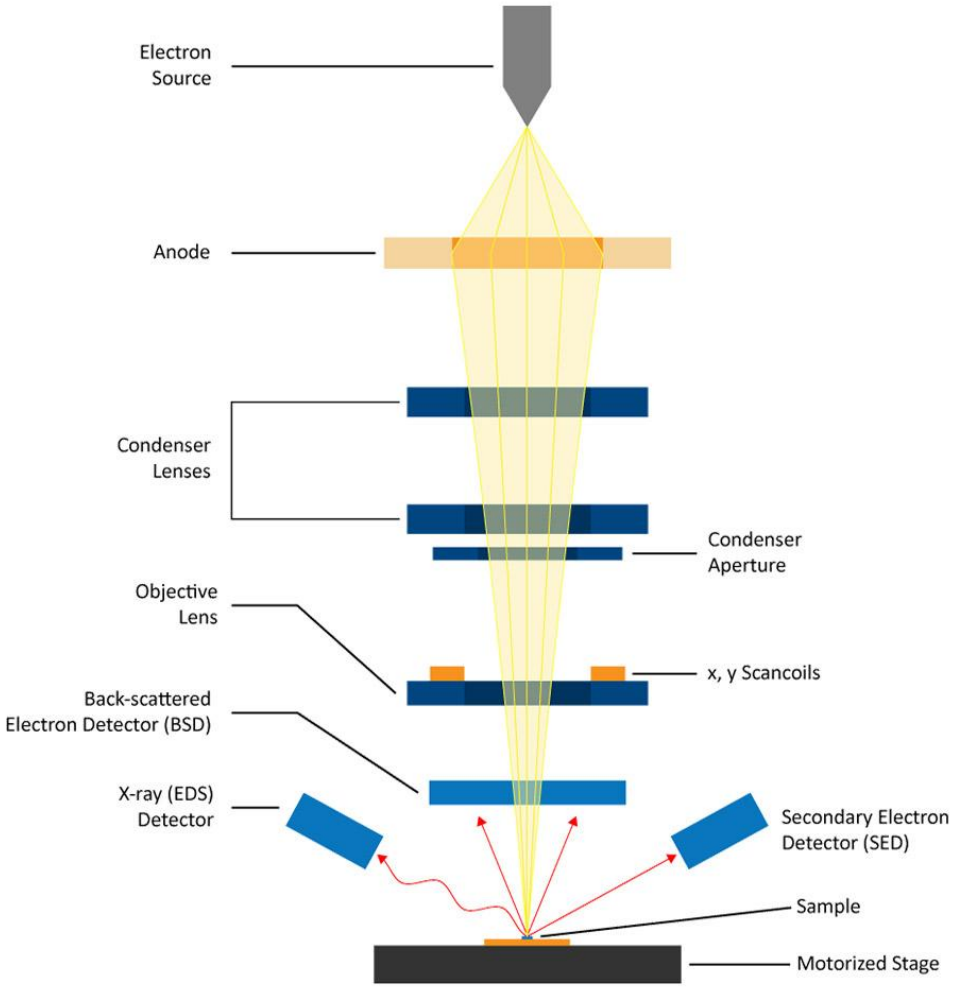

Figure 5.1.11 Schematic of SEM working system [5.17].

It is worth noting that the contrast in SEM images is influenced by the surface conductivity of diamond. Insufficiently conductive surfaces can accumulate charge under the electron beam, leading to image distortion or dark contrast. An example of this contrast is illustrated in Figure 5.1.13, where the marker area corresponds to the O-terminated marker areas appear darker due to their insulating nature, while the H-terminated regions show brighter contrast as the conductive 2DHG suppresses charging.

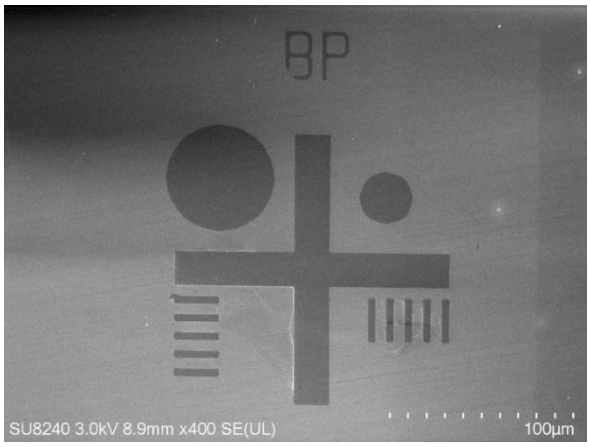

Figure 5.1.13 SEM scan of a marker pattern: O-terminated (dark) vs. H-terminated diamond (bright).

5.2 Field-effect transistor characteristics

5.2.1 DC characteristics

To characterise the electrical performance of the FET, measuring the I-V characteristics of the device can effectively extract key parameters such as output characteristics and transfer characteristics. Next, this subsection will be divided into two parts to introduce the measurement and analysis methods of output characteristics and transfer characteristics. A simplified FET cross-section diagram is shown in Figure 5.2.1.

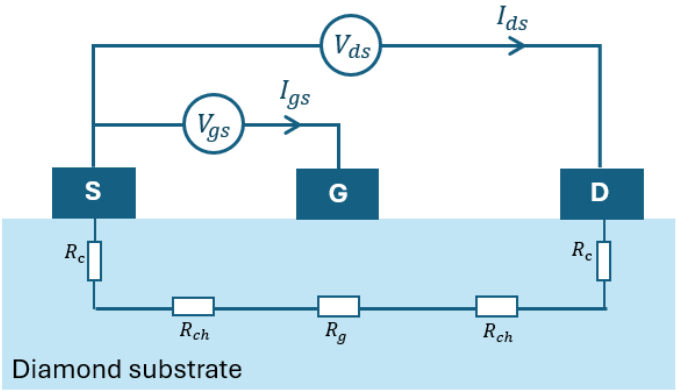

Figure 5.2.1 Simplified FET cross-section diagram.

In measurement, three probes are usually used. Among them, the source is grounded, and the other two probes are connected to the gate and drain, respectively, which are used to control the source-drain voltage (V_{ds}) and the source-gate voltage (V_{gs}).

Output characteristics

The output characteristic is used to represent the relationship between the V_{ds} and the drain current, $I_{d,}$ under certain conditions V_{gs}. In this case, the drain is analysed as the output terminal of the device, and thus it is referred to as the output characteristic. As mentioned in section 2.7, the output characteristic $I_d V_{ds}$ curve can explain the device's performance and divide it into different operating regions, which involve the cut-off region, the linear region, the saturation region, and the breakdown region. An example of a diamond MOSFET output characteristics IV plot is shown in Figure 5.2.2

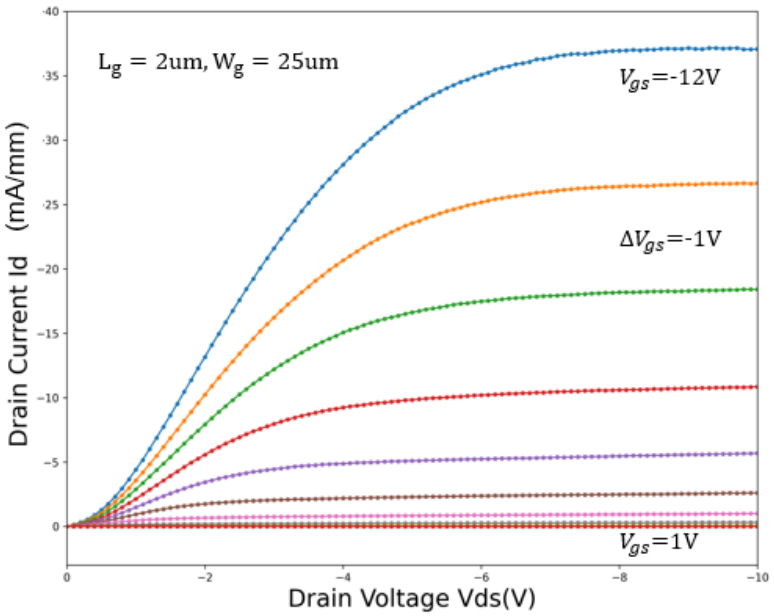

Figure 5.2.2 Example output characteristics IV plot of H-diamond MOSFET.

Analysing the output characteristics of the device enables an intuitive analysis of the on-resistance (R_{on}) of the device in the linear region, as the device operates like a resistor in this case. As shown in Figure 5.2.1, R_{on} can be defined as

$$R_{on} = 2R_c + 2R_{ch} + R_g \tag{5.2.1}$$

where R_c is the contact resistance, R_{ch} is the channel resistance, and R_g refers to the resistance of the gated channel region.

TLM measurement can provide the result of R_c, while both VDP and TLM measurements can generate the sheet resistance result, which can be used to calculate the resistance in the channel R_{ch}.

In addition, as V_{ds} keeps increasing, the lateral electric field near the drain becomes sufficiently large that the drain current no longer increases linearly with V_{ds} but tends to saturate at a nearly constant value, and the I_{dsat} can be defined as

$$I_{d,sat} \approx \upsilon_{sat} W C_{eff} (V_{gs} - V_{th}) \tag{5.2.2}$$

Where υ_{sat} represents the hole velocity, W is the channel width, C_{eff} is the effective gate capacitance per unit area. This behaviour may originate from either carrier velocity saturation or channel pinch-off. Further increasing V_{ds} beyond the saturation region will eventually lead to high-field effects such as impact ionisation or dielectric breakdown, which behave as a sudden increase in drain current and mark the breakdown limit of the device.

Transfer characteristics

The transfer characteristic is used to analyse the relationship between the drain current and V_{gs} under a fixed V_{ds}. In this case, what is emphasised is the response when a voltage is applied at the gate and the current is transferred to the drain side. Therefore, it is called the transfer characteristic, known as $I_{ds}V_{gs}$ curve.

As mentioned in Section 2.7, FETs perform as a voltage-controlled switch, which means that a FET needs a specific voltage to turn on or off. Therefore, the definition of threshold voltage (V_{th}) is introduced. In the measurement of the device, the parameters related to the V_{th} can be effectively extracted through the analysis of the transfer characteristics, so as to determine when the device is on and when it is off. There are three methods to extract V_{th},

1) Constant-current method: Plot I_d–V_{gs} at a fixed small V_{ds} in the linear region, and define V_{th} as the value of V_{gs} at which I_d reaches a predefined constant current (typically normalised to the device geometry).
2) Square-law method: Plot $\sqrt{I_{ds}}$ V_{gs}, perform linear fitting in the saturation region and extend it to the x-axis, then V_{th} is equal to V_{gs} where $\sqrt{I_{ds}}$ is 0.
3) Linear region method: Plot $I_d V_{gs}$, find a small V_{ds} and perform linear fitting in the linear region and extend it to the x-axis, then V_{th} is equal to V_{gs} where I_d is 0.

4) Transconductance peak method: Transconductance (g_m) is used to describe the rate of change in I_d caused by a small change in V_{gs} at a specific drain voltage ($V_{ds} > V_{th}$). In this case, V_{th} is equal to V_{gs} where g_m reach the maximum. Ideally, intrinsic g_m^* can be defined as

$$g_m^* = (\frac{dI_{ds}}{dV_{gs}})_{V_{ds}} \tag{5.2.3}$$

However, in actual measurement, considering the voltage drop between the source and the gate, that is, the transconductance is affected by parasitic resistance. Extrinsic i.e. as measured transconductance g_m can be defined as:

$$g_m = \frac{g_m^*}{1+g_m^* R_s} \tag{5.2.4}$$

Where R_s represents the source resistance. It considers the voltage drop between the source and the gate contacts. R_s is the sum of the sheet resistance in the channel and the contact resistance under the contact.

$$R_s = R_{ch} + R_c \tag{5.2.5}$$

An example plot of the diamond FET transfer characteristic is shown in Figure 5.2.3.

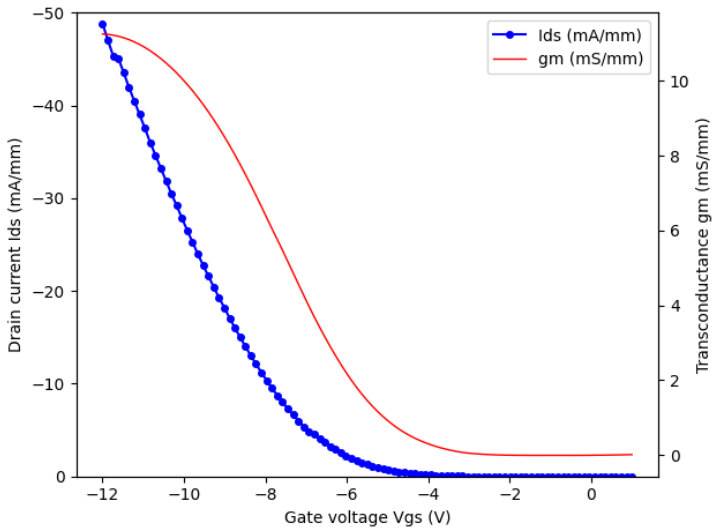

Figure 5.2.3 Example transfer characteristics IV plot of H-diamond MOSFET.

In addition, by plotting $log_{10}(I_{ds})V_{gs}$, the subthreshold swing (SS), which presents the rate of the change in I_d caused by V_{gs} when $V_{gs} < V_{th}$ can be determined. Specifically, it describes the increment of gate voltage required to increase or decrease the leakage current by an order of magnitude. That is, the switching steepness of the device from the "completely off" to the "weakly conducting" region, which is used to measure the sensitivity of the leakage current in the off state varying with the gate voltage.

$$SS = \frac{dV_{gs}}{dlog_{10}I_{ds}} \ [mV/dec] \tag{5.2.6}$$

The on-state current and off-state current ratio (I_{on}/I_{off}) can be generated from transfer characteristics as well. This ratio is an important figure of merit, as a high I_{on}/I_{off} indicates strong gate control over the channel, low leakage current in the off state, and efficient switching behaviour of the device.

Gate leakage

The gate leakage current is used for evaluating the quality of the gate dielectric and its interface with the hydrogen-terminated diamond surface. Ideally, the gate current should remain several orders of magnitude lower than the drain current, ensuring that the gate maintains effective control over the 2DHG. In practice, however, several leakage mechanisms may occur. Direct tunnelling may arise if the dielectric layer is too thin, while the defects and interface states can also contribute significantly to leakage. In addition, the non-uniformity of gate dielectrics deposition may lead to leakage as well.

Extreme gate leakage has a negative impact on device performance. It increases the off-state current, thereby reducing the I_{on}/I_{off} ratio, which is essential for device switching. Moreover, leakage current through the dielectric will accelerate device degradation under high-field operation, eventually leading to dielectric breakdown and compromising long-term device reliability. To minimise these effects, high-dielectric constant (high-k) oxides such as Al_2O_3 and HfO_2 are typically used. These materials enable a greater physical thickness under the same equivalent oxide layer thickness which suppresses tunnelling leakage, while maintaining a large gate capacitance through their high-k.

5.2.2 CV characteristics

In addition to DC characteristics, capacitance-voltage (CV) testing is an important method for characterizing the gate dielectric material and channel electrical performance. Extracting parameters such as the capacitance of the gate oxide layer can provide important information for optimizing the device process. Different to Si MOSFET, H-diamond forms a 2DHG just beneath the diamond surface through surface transfer doping, so in CV test of H-diamond MOSFET, the focus is on the extraction of capacitance, mobility and 2DHG carrier density. An example CV curve is shown in Figure 5.2.4.

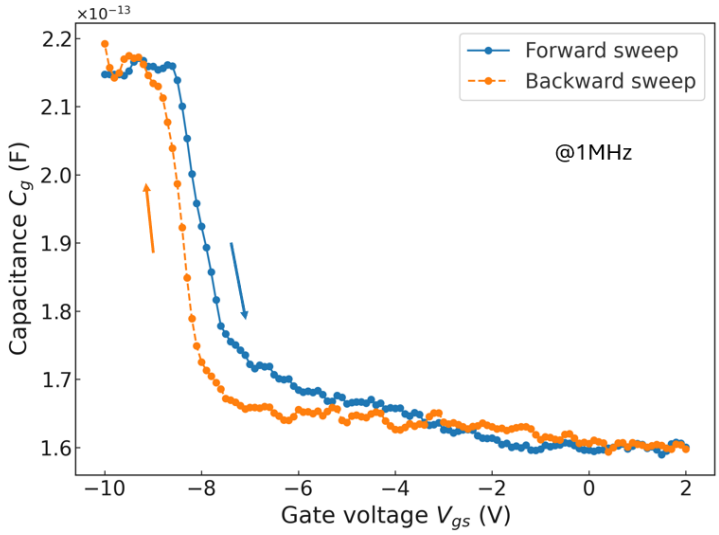

Figure 5.2.4 Example CV curve of 1um gate length accumulation channel H-diamond MOSFET.

As shown in Figure 5.2.4, there are three regions in the CV plot,

1) Off/depleted region: when $V_{gs} > 0$, 2DHG has been blocked or extremely weak, the channel is in the off state. In this regime, the measured capacitance saturates at a constant level primarily determined by the parasitic capacitance, which appears effectively in series with the gate oxide and depletion capacitances.
2) Depletion region: when $V_{th} < V_{gs} \leq 0$, holes are not fully depleted, and the equivalent capacitance increases as the gate bias becomes more negative.
3) Accumulation region: when $V_{gs} \leq V_{th}$, 2DHG has accumulated, a channel is formed, and the measured capacitance approaches its maximum value. Ideally, the capacitance per unit area is close to the oxide capacitance, which can be expressed as

$$C_{ox} = \frac{\varepsilon_0 \varepsilon_{ox}}{t_{ox}} \tag{5.2.7}$$

Where ε_0 is vacuum permittivity, ε_{ox} is the dielectric constant of oxides, t_{ox} It is the thickness of the oxide. In practice, however, the effective capacitance is slightly lower than C_{ox} because it also includes the contribution of the diamond between the oxide/diamond interface and the centroid of the 2DHG charge distribution.

5.3 Chapter Summary

This chapter introduces the key technologies for characterising diamond materials and devices. Firstly, the Hall effect measurement theory was explained, which is used to

determine the carrier concentration, mobility, and sheet resistance. Secondly, the Transmission Line Measurement (TLM) method was introduced, which can separate and quantify the contact resistance and sheet resistance. Subsequently, the application of atomic force microscopy (AFM) in evaluating the surface roughness of diamond was explained. It was then explained how scanning electron microscopy (SEM) achieves high-resolution imaging of the surface morphology and composition of materials by focusing an electron beam to monitor and capture secondary and backscattered electron signals. In the second section, the theoretical framework and calculation methods for the electrical analysis of FETs are presented, including DC characteristics and CV characteristics. The working range of the FET is introduced, laying the foundation for device design and performance optimisation.

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6. Novel Surface Terminations and Transfer Doping Performance

In this chapter, the impact of different diamond surface terminations as hydrogen (H), oxygen (O), fluorine (F), silicon (Si), and scandium (Sc) will be explored. These terminations were experimentally introduced and characterised via the Hall effect and DC tests. The following section focuses on the transfer doping performance of H-diamond under the influence of various oxide layers. The specific oxide materials and deposition mechanisms were tested to verify the mechanism of enhancement and suppress of the two-dimensional hole gas (2DHG) in H-diamond. By examining the relationship between hydrogen termination and surface oxides, there is an aim to provide insights into the stability and modulation of 2DHG, which is critical for device applications such as diamond-based field-effect transistors.

6.1 Surface terminations

The difference in electrical properties of different terminations of the diamond surface is mainly due to the difference in electron affinity (EA). EA refers to the energy difference between the vacuum electron level and the bottom energy level of the conduction band. It reflects the difficulty of electrons moving from the conduction band to the vacuum level to become free electrons, that is, the strength of the atom or material's ability to attract electrons. For surface termination of diamond, the greater the electron affinity of the surface termination, the stronger the ability to attract electrons, and more difficult it is for electrons to escape from the diamond surface. Hence, the diamond surface charge is also more difficult to control. Novel surface termination research on diamond offers more possibilities for the development of negative EA (NEA), or low work function conditions, in wide-bandgap materials, which play a crucial role in the development of effective field-effect transistors (FETs).

In this chapter, the surface treatment process of hydrogen termination is carried out in collaboration with Prof. Alastair Stacey from RMIT University in Australia. The silicon termination and scandium termination were conducted in collaboration with Prof. Paul May’s group from the University of Bristol; our main tasks involved electrical measurements and processing development of these terminated surfaces.

Hydrogen termination

In this research, polished single-crystal CVD diamond substrates were purchased from Element Six with a (100) surface orientation, and the dimensions are 4.5 mm x 4.5 mm.

As the standard preparation process for hydrogen termination of the ASMaD group at the University of Glasgow, diamond samples have to be acid-cleaned to remove any potential surface contamination. The two-stage high-temperature acid clean steps are:

1) Soak the sample in mixed HNO_3: HCl in 1:1 ratio and boiling at 120 °C for 20 mins.

2) Soak the sample in mixed HNO_3: H_2SO_4 in 1:3 ratio and boiling at 250°C for 20 mins.

Sheet resistance measurements were performed using a Nanometrics HL5500PC Hall Effect measurement system. Four probes from the Hall kit were directly landed on the sample surface in a square geometry. All acid-cleaned samples exhibited insulating behaviour, indicating that the surfaces were most likely oxygen-terminated. Acid-cleaned diamond samples were packaged and shipped to Australia for hydrogen termination. In this work, all hydrogen-terminated diamond samples were stored and transported in a sealed box to minimise exposure to ambient air and moisture. This procedure helps preserve the hydrogen termination and maintain surface conductivity before electrical characterisation. The details of diamond hydrogen termination parameters provided by Prof. Alastair Stacy are shown in Appendix A.

As discussed in Chapter 4, Hall effect measurements and surface roughness analysis are two of the most fundamental characterisation techniques, as they offer direct evaluation of the electrical and physical surface quality, respectively. Selected results for hydrogen-terminated diamond samples obtained in this study are summarised in Table 6.1.1.

Sample	Sheet resistance (kΩ/□)	Mobility ($cm^2/V{\cdot}s$)	Concentration (cm^{-2})	Roughness Before H-term (nm)	Roughness After H-term (nm)
SC15	17.4	69.5	$+5.16 \times 10^{12}$	0.72	0.58
SC17	22.6	61	$+4.53 \times 10^{12}$	0.68	0.54
SC18	18.2	74	$+4.62\times 10^{12}$	0.92	0.85
SC22	15.8	50.1	$+7.9\times 10^{12}$	0.39	0.53
SC34	10.5	52.5	$+1.13\times 10^{13}$	0.60	0.71

Table 6.1.1 Results of H-diamond samples, including conductivity and roughness.

The typical sheet resistance of H-diamond in this study ranges from 10 kΩ/□ to 50 kΩ/□, depending on the surface quality and air exposure. The hole concentration is generally on the order of 10^{12} to 10^{13} cm², while the hole mobility lies between 40 and 120 cm²/V·s.

The surface roughness, as measured by AFM, is typically below 1 nm for high-quality CVD diamond substrates.

Oxygen termination

To investigate the role of oxygen termination on diamond surfaces, several oxidation techniques were employed to introduce oxygen-containing functional groups and replace the original C-C and C-H surface bonding. The following three methods were used for the oxygen termination of diamond:

1) High-temperature acid clean:
   As mentioned before, the two-stage high-temperature acid clean recipe included immersing diamond samples in a 1:1 mixture of concentrated HNO_3 and HCl, followed by boiling at 120°C for 20 minutes. This step was followed by immersion in a 1:3 mixture of HNO_3 and H_2SO_4 and boiling at 250 °C for an additional 20 minutes. This method can remove organic contaminants and introduce carboxyl, hydroxyl, and carbonyl groups onto the diamond surface. It is known to result in a strongly oxygen-terminated diamond surface with high chemical stability [6.1].
2) Oxygen plasma ashing:
   Oxygen plasma treatment was performed using a YES G-1000 plasma asher. The aim is to remove the hydrogen termination bonds on the diamond surface and introduce oxygen-containing groups on the surface. This treatment mainly has a chemical modification effect rather than a physical etching. In this study, the oxidation parameters were set to 300 W RF power with an oxygen flow of 20 sccm for 2 minutes.
3) UV-ozone treatment
   UV-ozone treatment was employed to achieve oxygen termination on the diamond surface, using ambient oxygen as the source gas. This technique allows for gentle and controllable surface oxidation, minimising physical damage while providing high surface uniformity [6.2]. In this study, the process was performed using a UVOCS (Ultraviolet Ozone Cleaner System), in which the samples were loaded 5–6 cm below the quartz-mercury vapour lamp. This low-pressure lamp emits ultraviolet light at wavelengths of 254 nm and 185 nm, which interact with ambient oxygen to generate ozone and atomic oxygen [6.3]. Prior to treatment, the system was preheated for 30 minutes to stabilise the ozone generation environment. The samples were then exposed to UV-ozone for 5 minutes to finish the surface oxidation.

The high-temperature acid clean recipe and oxygen plasma treatment recipe were previously calibrated by the ASMaD group members. UV ozone treatment was carried out in this study.

As mentioned, the evaluation of O-diamond surfaces was primarily based on Hall effect measurements. However, this approach was not sufficiently effective in distinguishing between various oxidation methods, as all oxygen-terminated samples exhibited insulating behaviour. The lack of surface conductivity alone could not provide insight into the effectiveness of each oxidation process.

To address this limitation, water contact angle (WCA) measurements were introduced as a supplementary characterisation method. Since oxygen termination significantly changes the surface hydrophilicity, the WCA provides indirect but reliable evidence of surface functionalisation. A lower contact angle generally indicates a more hydrophilic surface, which correlates with a higher density of oxygen-containing groups. Therefore, the WCA serves as a convenient and non-destructive indicator for comparing the extent and uniformity of surface oxidation among different treatment techniques.

Figure 6.1.1 shows the stability of the hydrophilicity of O-terminated diamond by UV ozone. This figure illustrates the changes in the WCA of the O-diamond surface after UV ozone treatment at various time durations. This indicates that the oxygen termination formed by UV-ozone is not fully stable and will react or desorb after being exposed to the air for a period of time. For example, the increase in water contact angle may result from the transformation of oxygen functional groups from strongly polar species such as C=O to less polar ones like C–O–C. This behaviour has been widely reported in the literature. According to previous studies, the increase in water contact angle may be associated with an evolution of surface oxygen configurations from strongly polar species (such as C=O) to less polar bonding arrangements (for example, C–O–C), as well as partial desorption or rearrangement of oxygen functional groups on the diamond surface [6.2]. Additionally, surface contamination and the influence of ambient air or humidity can also contribute to the degradation of surface hydrophilicity. However, although the WCA increases over time, it does not fully return to its original hydrophobic state after 1 day.

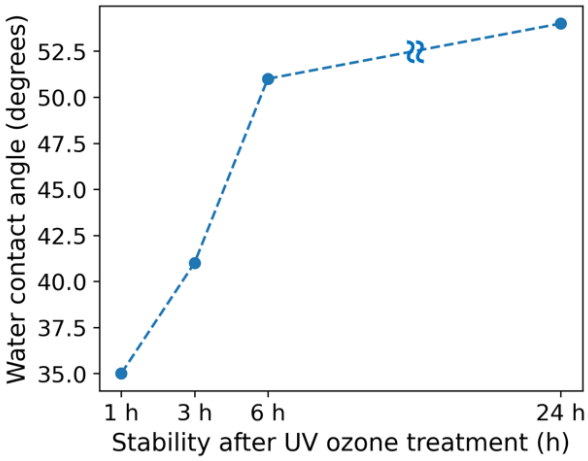

Figure 6.1.1 Stability of water contact angle of O-terminated diamond by UV ozone.

Silicon-termination diamond experiment

As mentioned in the previous chapter, H-termination is relatively unstable under oxidation or high-temperature conditions. O-termination typically behaves as insulating. To explore further possibilities for NEA on diamond surfaces, silicon termination (Si-termination) has emerged as a promising alternative. Explored surface terminations of diamond and their reported electron affinities are listed in Table 6.1.2.

Termination	Hydrogen termination	Oxygen termination	Silicon termination	Scandium termination	Fluorine termination
Bonding	C-H	C-O	C-Si	C-Sc	C-F
EA (eV)	-1.3	1.7	-0.86	-3.02	2.56

Table 6.1.2 Bonding of Novel surface terminations of diamond and their electronic affinity [6.4].

Similar to hydrogen-termination, Si termination is considered to exhibit NEA and form a 2DHG in diamond. The results revealed a Fermi level of 0.2 eV above the valence band maximum (VBM), work function of 4.89 eV, and NEA is -0.86eV [6.5].

To investigate the potential of Si termination, this experiment was collaborated with Paul May's group at the University of Bristol. Acid-cleaned, oxygen-terminated single-crystal diamond samples were provided for silicon deposition. Before deposition, diamond samples were treated with oxygen plasma to be oxygen-terminated. The surface condition was verified via AFM and Hall effect measurements.

Silicon deposition was carried out by electron beam (e-beam) evaporation using a single-crystal silicon rod as the source material. The process was conducted under ultra-high vacuum (UHV) conditions within a nano ESCA system. The system is equipped with an

integrated quartz crystal microbalance (QCM), which allows for precise in-situ thickness measurements of the deposited Si layer. The deposition rate and conditions have been calibrated to achieve sub-monolayer (sub-ML) accuracy.

In the present experiment, two coverage levels of 1.0 ML and 0.5 ML were investigated. Here, 0.5 ML refers to a surface coverage where only half the number of silicon atoms required for a complete monolayer are deposited across the diamond surface. The deposited Si atoms are assumed to be distributed over the surface, although the precise atomic arrangement cannot be confirmed within this study. On bare diamond surfaces, the number of available bonding sites for Si atoms is limited. While Si atoms ideally tend to form four bonds, it is unlikely that all surface carbons are fully coordinated with Si. The remaining surface carbons are likely to restructure or interact with adjacent atoms to reduce dangling bonds, but incomplete passivation or partial oxygen termination of the surface cannot be excluded.

In contrast, oxidised diamond surfaces offer more opportunities for Si atoms. An O-terminated diamond surface features a variety of functional groups, including hydroxyl (–OH), ether (–C–O–C–), carbonyl (C=O), and lactone structures. This leads to a bigger range of possible bonding configurations for the Si atoms. In this study, two parameters are mainly considered in evaluating the silicon-functionalised diamond surfaces: the thickness of the Si layer (in monolayers) and the bonding configuration between Si and surface carbon atoms (C–Si and C–O–Si).

Experiment One: Si Deposition on O-Diamond Surfaces

Two O-diamond samples, ES12 and ES15, were subjected to the following sequential treatments:

1. Initial annealing: Both samples were annealed at 250 °C for 1 hour in vacuum (1×10^{-9} mbar) to remove surface adsorbates.
2. Silicon deposition:
    - Sample ES12: Deposited with 1ML of silicon by e-beam evaporation at room temperature. The deposition duration was 7 minutes 30 seconds.
    - Sample ES15: Deposited with 0.5 ML of silicon under the same conditions, with a deposition time of 3 minutes 45 seconds.
3. Post-deposition Annealing: Both samples were subsequently annealed at 600 °C in vacuum (1×10^{-9}mbar) to promote interfacial reaction and surface reconstruction.

Firstly, a four-probe Van der Pauw (VDP) measurement was carried out to extract the sheet resistance, mobility, and concentration using the Hall system. Table 6.1.3 lists the results after the Si-termination.

Sample	Sheet resistance (Ω/□)	Mobility ($cm^2/(V·s)$)	Concentration (cm^{-2})
ES12	3129	0.217	9.196×10^{15}
ES15	3428	0.312	5.842×10^{15}

Table 6.1.3 Hall measurement results after Si-termination.

Both Si-terminated samples exhibit sheet resistances in the range of approximately 3.1–3.4 kΩ/□, which follows the typical region reported for p-type conductivity on the H-diamond surface. Although these sheet resistance values appear promising, the extracted carrier densities (~10^{15} cm^{-2}) and mobilities (<0.4 $cm^2/(V·s)$) are physically unreasonable when compared with values typically reported for H-terminated surfaces. It indicates that, while Si-termination leads to measurable conductivity, the underlying origin of the observed electrical behaviour cannot be conclusively determined from the present results.

To further investigate the origin and stability of the observed surface conductivity, a thermal stability experiment was conducted. After initial Hall measurements, each sample was heated to 80 °C for 10 minutes on a hot plate in ambient air, and subsequent Hall measurements were repeated to monitor any changes in sheet resistance, mobility, and carrier concentration. This experiment was based on the idea that heating a substrate will perturb surface transfer-doped samples in air, which are highly sensitive to atmospheric conditions and temperature, since both these factors can influence the nature and number of surface adsorbates available to accept electrons at the diamond surface.

In the case of H-diamond, such perturbations are typically reversible at temperatures below 200 °C [6.6]. Thermally desorbed adsorbates tend to re-adsorb upon cooling, allowing the sample to recover its original conductivity. However, this reversibility is not expected if the observed conductivity originates from, for example, a graphitic surface layer. The electrical characteristics of graphitised surfaces typically remain stable upon low-temperature heating (such as 80 °C), as their conduction mechanism does not rely on ambient-dependent surface states [6.7].

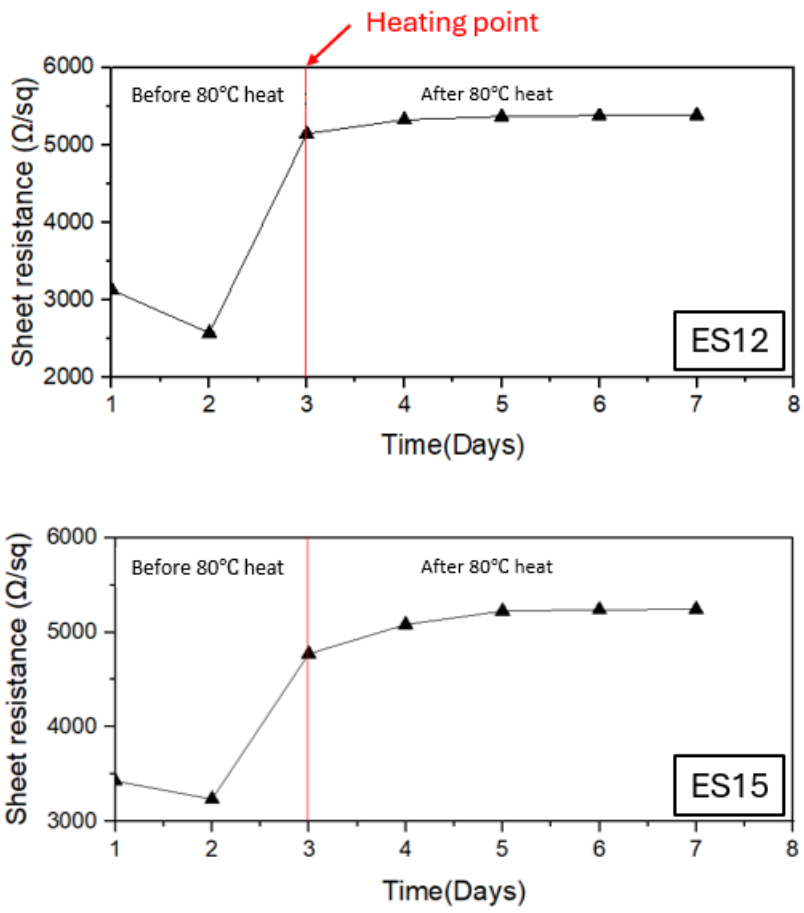

Figure 6.1.2 Hall measurements result over time before and after 80 °C heat.

Figure 2.1.3 shows the results of sheet resistance stability before and after 80 °C heat. It is interesting to note that after heating, the sheet resistance increased from 2.5 kΩ/□ to 5 kΩ/□. To assess the stability of the surface conductivity over time, the sample was left exposed to ambient air and re-measured daily over the following four days. During this period, the sheet resistance remained and did not return to its original value of 2.5 kΩ/□.

Importantly, this elevated resistance remained stable over the following days of ambient exposure, without recovering to its original value. Such behaviour contrasts with that of transfer-doped H-diamond surfaces, where conductivity changes induced by low-temperature heating (<200 °C) are typically reversible due to re-adsorption of surface adsorbates. The lack of recovery observed here indicates that the conductivity is unlikely to originate from conventional surface transfer doping. Instead, the stable post-heating resistance suggests a conduction mechanism more consistent with sp^2 carbon or other defect-related states that are not sensitive to atmospheric re-adsorption processes.

Experiment Two: Comparison of Pre-Annealing Effects on Si-Terminated Surfaces

This experiment aimed to investigate the influence of pre-annealing on silicon bonding behaviour by comparing samples with different initial surface conditions. The two samples, EX01 and ES03, received the following treatments:

1. Pre-Annealing Conditions:
    - Sample EX01: Pre-annealed at 1000 °C for 1 hour in vacuum (1x10^{-9} mbar), which is intended to remove the oxygen surface termination.
    - Sample ES03: Pre-annealed at 300°C for 1 hour in vacuum, consistent with the process in Experiment One, to remove surface adsorbates while preserving the oxidised surface termination.
2. Subsequent Si deposition and annealing: both samples then underwent 1ML of silicon deposition and 600 °C vacuum (1x10^{-9} mbar) annealing using the same conditions described in Experiment One.

In this context, sample EX01, which underwent high-temperature vacuum annealing (1000 °C) before Si deposition, is expected to exhibit C–Si bonds at the interface, as high-temperature vacuum annealing has been widely reported to effectively remove oxygen-related surface species from diamond surfaces [6.6,6.10]. To evaluate the electrical properties, Hall measurements were performed on sample EX01 and ES03. The results of the hall measurement are listed in Table 6.1.4.

Sample	Sheet resistance (Ω/□)	Mobility ($cm^2/(V·s)$)	Concentration (cm^{-2})
EX01	2.1x10^4	7.15	4.144×10^{13}
ES03	Not measurable	Not measurable	Not measurable

Table 6.1.4 Hall measurement result of Si-terminated diamond under pre-annealing.

Sample EX01, which was pre-annealed at 1000 °C, demonstrated clear surface conductivity, attributed to potential C–Si interfacial bonds. In contrast, sample ES03 has O-termination and is expected to form C–O–Si bonding configurations after Si deposition. Although Hall measurements were performed under identical conditions, no measurable conductivity was detected in ES03 using the standard four-probe Van der Pauw method. To confirm this result and exclude potential contact artefacts, silver DAG was applied at the sample corners, no electrical shorting was observed across the edges, and both sides of ES03 remained non-conductive.

This observation indicates that residual oxygen-related species or the formation of a silicon oxide interlayer suppresses the direct formation of C–Si bonds, thereby preventing charge transfer and the establishment of a conducting surface channel. By comparison, high-temperature vacuum annealing, as applied to EX01, is therefore identified as a critical condition for removing oxygen species and enabling C–Si interfacial bonding, which is associated with the emergence of hole conduction.

Although EX01 exhibited a relatively high carrier concentration, its mobility was limited to approximately 7 $cm^2/V{\cdot}s$, which is significantly lower than the typical values reported for hydrogen-terminated diamond (50-200 $cm^2/V{\cdot}s$). This suggests that, while the potential C–Si bonding enables charge transfer, additional scattering mechanisms or partial graphitisation may still dominate carrier transfer. Moreover, the observed colour change of the surface after high-temperature annealing raises the possibility of partial graphitisation, as shown in Figure 6.1.3.

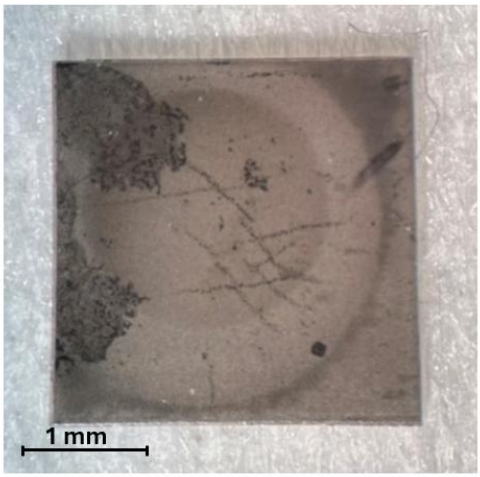

Figure 6.1.3 Sample EX01 after Si-termination with pre-annealed at 1000 °C for 1 hour in vacuum.

However, such a conclusion cannot be established from electrical data alone and requires complementary structural characterisation, such as Raman spectroscopy or XPS, to be confirmed. Overall, this comparison clearly demonstrates the influence of pre-annealing conditions on the interfacial bonding configuration and the resulting electronic properties of Si-terminated diamond.

Scandium-termination diamond experiment

To identify a better NEA surface termination candidate, Paul May's group from the University of Bristol conducted a computational study of the Scandium termination, providing predicted values of EA and work function (WF) for the undoped diamond (100)

surface. For the Sc-terminated bare diamond surface, these values were extremely dependent upon the surface coverage and position of the Sc adsorbates, with the most NEA (−3.02 eV) and work function of 1.98 eV for a 0.25 ML coverage. These values show that these two Sc–diamond surfaces have the highest NEA for a metal adsorbed onto bare diamond measured to date, as well as being thermally stable up to 900 °C [6.8].

Diamond samples with O-termination for Sc termination were provided to Bristol group. Before metal deposition, both samples were acid-cleaned and subsequently treated with UV-ozone for 5 minutes to ensure the removal of contaminants and to stabilise the surface O-termination.

Experiment process:

- Sample ES02: H-plasma treated to achieve the H-terminated surfaces, annealed at 900 °C for 1 hour.
- Sample ES13: Treated with UV ozone in ambient air to form the O-terminated surface, followed by annealing at 400 °C for 1 hour.

A 0.25 monolayer (ML) Sc was deposited on both surfaces, followed by a post-deposition anneal at 400 °C for 15 minutes. X-ray photoelectron spectroscopy (XPS) and ultraviolet photoelectron spectroscopy (UPS) were performed to characterise the surface termination. Subsequently, both samples were extracted from the UHV system and left exposed to ambient atmosphere in the laboratory for 9 days.

The results show that both Sc-terminated and Sc-O-terminated surfaces keep NEA with air exposure. For the Sc–diamond surface, the NEA changed from −0.92 eV to −0.74 eV, indicating a slight degradation. In contrast, the Sc–O–diamond surface showed an improvement in NEA, with the EA shifting from −0.26 eV to −0.86 eV after air exposure. This suggests that the surface may have undergone further oxidation during exposure to air. The post-exposure oxidation enhanced the surface dipole required for NEA.

As shown in Figure 6.1.4, both samples exhibit visible colour changes after scandium deposition. These colourations are not intrinsic, as the diamond substrate is single-sided polished and optically transparent, and bulk scandium is silvery white in appearance. Instead, the observed colours are most likely due to thin-film interference effects, which vary with film thickness. To explore whether the visible colour changes are from optical interference effects, a solvent cleaning step was first performed to remove potential surface contaminants. AFM was then used to characterise surface roughness, the results are shown in Figure 6.1.5. Both samples exhibited a surface roughness (R_q) of around

43 nm, which is much rougher than before (under 1nm). According to the measured surface roughness values. It infers that the actual thickness of scandium on the sample surface is significantly greater than 0.25 ML, as designed.

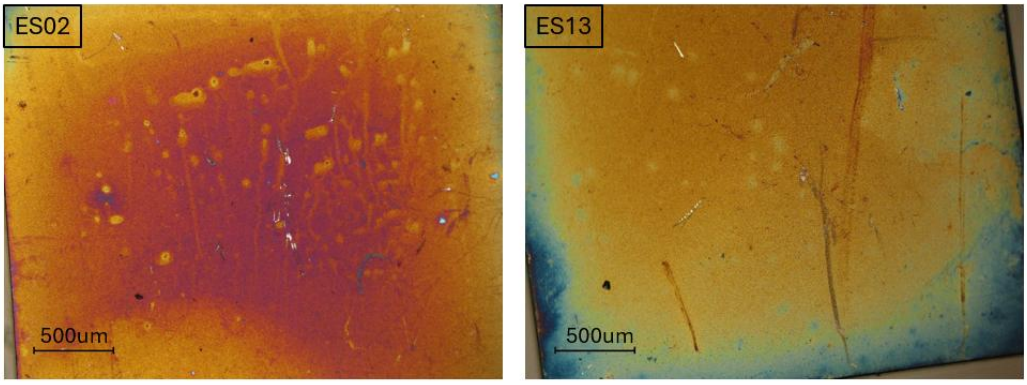

Figure 6.1.4 Optical images of sample ES02 and ES13, respectively.

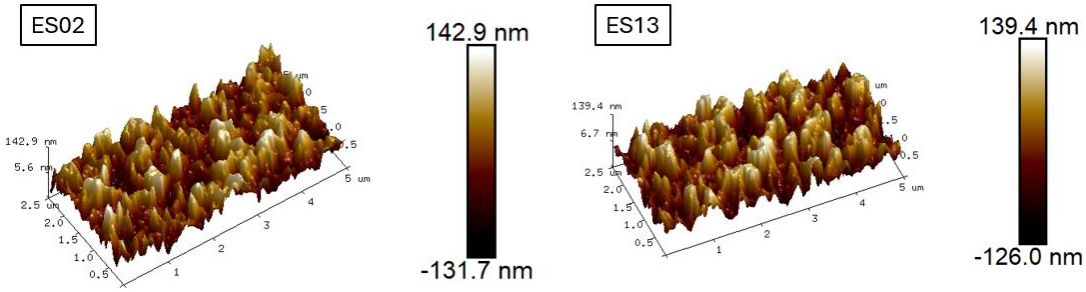

Figure 6.1.5 Surface roughness 3D image of AFM, sample ES02 and ES13, respectively

Given the visible colour change observed on the surface and the possibility of residual metallic species, which infers that the surface might exhibit measurable conductivity. To test this, Hall measurements were carried out on both samples (ES02 and ES13), and the results are summarised in Table 6.1.5. Both samples exhibited very low sheet resistance and high sheet carrier concentrations, on the order of 10^{17} cm^{-2}, compared to the H-termination. The high conductivity suggests that the sample surface may contain metallic species.

Samples	Sheet resistance (Ω/□)	Mobility ($(cm^2/V{\cdot}s)$)	Concentration (cm^{-2})
ES02	509.3	0.025	$+4.902 \times 10^{17}$
ES13	584.2	0.064	$+1.667 \times 10^{17}$

Table 6.1.5 Hall measurement results after Sc-termination.

To verify this hypothesis, scanning electron microscopy (SEM) with EDX is used to investigate the surface elemental composition. At the same time, weakly bonding or adsorbed species were selectively removed while protecting the stable surface terminations. The samples were treated with 37% hydrochloric acid (HCl) solution for 2 minutes. After etching, SEM-EDX measurements were repeated on both samples to evaluate changes in surface composition. SEM-EDX spectrum results are shown in Figure 6.1.6.

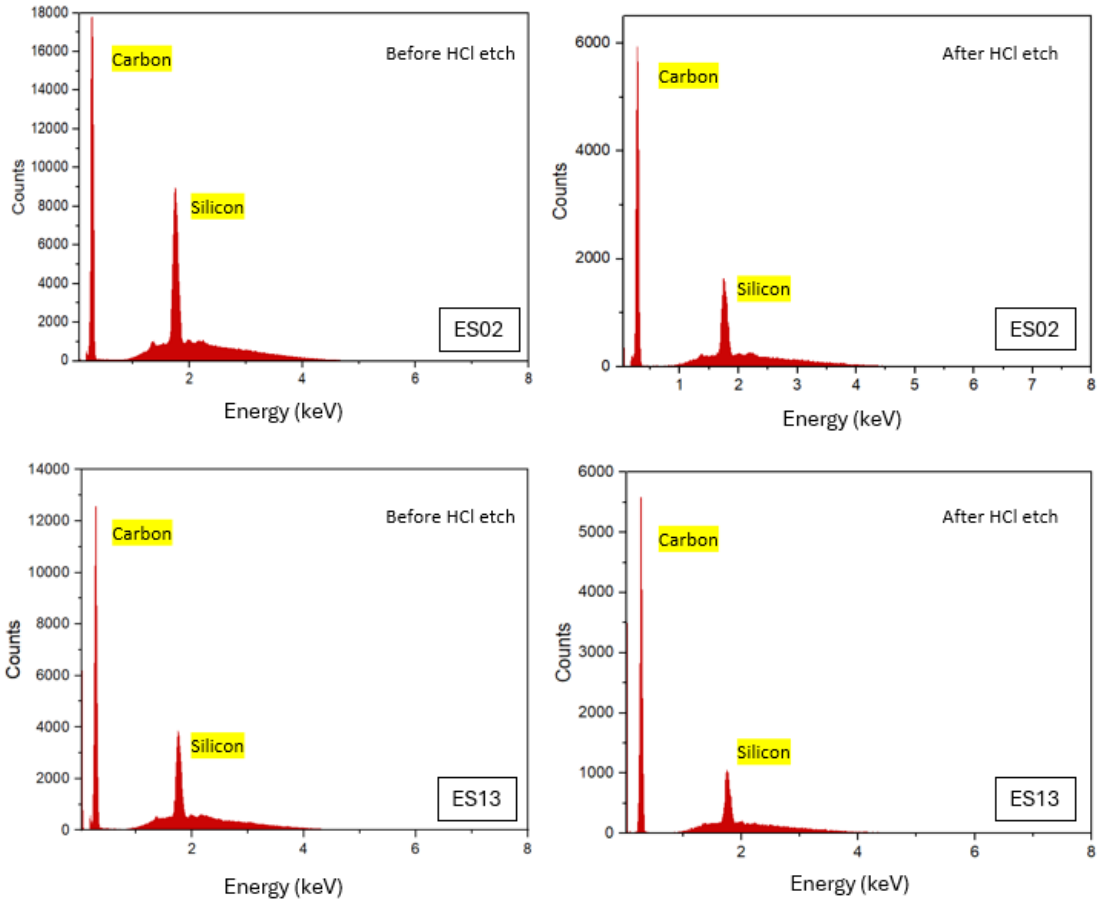

Figure 6.1.6 SEM-EDX spectrum results before and after HCl etch.

It should be noted that silicon was not intentionally deposited on these samples, and its presence is attributed to surface contamination, most likely originating from previous processing steps, handling, or environmental exposure before scandium deposition. The SEM–EDX spectra shows the Si signals on both ES02 and ES13 before the acid treatment, which decrease after a 2-minute 37% HCl dip, consistent with the removal of Si-containing surface contaminants such as silicon oxides. No Sc peaks (~4.09 keV) are detected before or after etching. However, this non-detection does not preclude the presence of Sc because the 0.25 ML is far below the typical EDX detection limit on a carbon substrate, the coverage is likely non-uniform (AFM gives R_q≈43 nm), and acid

exposure can further remove Sc-oxide species. Together with the visible colouration and the Hall measurement results, the data indicate the formation of a conductive surface layer of uncertain composition rather than the sub-monolayer Sc termination. In short, the colour change, roughening, and high conductivity are attributed to an undesired surface overlayer, while the absence of an EDX Sc signal is consistent with the expected detection limits. Further clarification of the surface composition would require Sc-sensitive techniques such as XPS or Raman spectroscopy, as well as temperature-dependent transport measurements.

Fluorine-termination diamond experiment

The significant contrast in electronegativity between fluorine and carbon results in a highly polar C-F bond. This dipole layer can modify the surface band structure, potentially leading to the confinement of electrons within a two-dimensional plane near the surface. This bond exhibits a notably high, positive EA, even compared to that of O-terminated diamond. After vacuum annealing to 350 °C, a clean, monofluoride-terminated C (100): F surface was obtained for which a PEA of 2.56 eV was measured [6.4]. The formation and characterisation of a 2DEG on fluorine-terminated diamond surfaces present significant challenges. Therefore, the ASMaD group is working on setting up a recipe for fluorine-terminated diamond within the JWNC.

Creating a fluorine termination on a diamond surface involves chemically modifying the surface to replace hydrogen or oxygen atoms with fluorine atoms. The unterminated diamond surface needs to be activated to make it more receptive to fluorine bonding. In this study, a clean oxygen-terminated diamond surface is prepared by performing acid cleaning followed by UV–ozone treatment, as detailed before. There are several established methods to introduce fluorine atoms onto diamond surfaces. A commonly used approach is to expose the activated diamond to fluorinated precursor gases, such as SF_6 or C_4F_8, which decompose in plasma to release reactive fluorine species.

Here, a recipe for a fluorine termination process using the Oxford Instruments Plasma Pro System 100 ICP300 Cobra etch tool was tested. This tool offers a temperature-controlled stage with a high-density ICP source that enables anisotropic and uniform plasma exposure. The specific process recipe used in this work is summarised in Table 6.1.6.

Sample	Precursor gas	Gas flow rate	ICP power	Platen power	Chamber pressure	Duration
EXN	SF_6	50 sccm	300W	25W	22.5 mTorr	120s

Table 6.1.6. Fluorine termination recipe with ICP plasma tool.

Because both O-terminated and F-terminated diamond are not expected to exhibit surface conductivity in air, the electrical measurements alone cannot distinguish between the two terminations before and after the treatment. Hence, the surface properties were investigated by water contact angle analysis. In principle, the surface WCA is strongly influenced by the type of surface termination. As mentioned before, hydrogen-terminated diamond is typically hydrophobic, whereas oxygen-terminated surfaces tend to be hydrophilic. The fluorine termination, due to its strong surface dipole and low surface energy, is expected to be even more hydrophobic than H-terminated diamond and hence should show a larger contact angle.

The WCA results exhibit a substantial increase from 37.4° (pre-treatment) to 90.9° (post-treatment). This dramatic increase in hydrophobicity strongly indicates the replacement of oxygen-containing surface groups with fluorine terminations, which are known to lower the surface energy and induce a non-polar, hydrophobic character. To evaluate the surface termination stability, a second measurement was performed after 2 hours. The contact angle exhibited a minor fluctuation (89°±1°), which may be attributed to either measurement error or slight adsorption of atmospheric species. After 24 hours of ambient exposure, the WCA remained stable.

This indicates that the hydrophilicity of the oxygen-terminated diamond surface has undergone a significant change after the fluorine termination process, providing us with considerable confidence in completing the fluorine termination process. However, it is important to note that WCA alone cannot serve as conclusive evidence of successful fluorine termination, as similar hydrophobic behaviour may arise from other surface modifications or residual contaminants.

6.2 Transfer Doping Performance

Hydrogen-terminated diamond has demonstrated exceptional surface conductivity and promising device characteristics, making it a strong candidate for high-frequency, high-power, and quantum electronic applications. However, the major limitation of the 2DHG instability is believed to originate from surface transfer doping via air-adsorbed species. As discussed in Chapters 2 and 3, hydrogen-terminated diamond exhibits a NEA,

typically around −1.3 eV. The key requirement for the transfer doping mechanism is that the Fermi level or conduction band minimum (CBM) of the acceptor material lies below the valence band maximum (VBM) of the H-diamond. In this case, electrons from the diamond surface can be transferred to the acceptor material, resulting in the formation of a 2DHG layer.

Based on these theoretical considerations, the focus is to explore the interaction between hydrogen-terminated diamond (H-diamond) and various oxide materials with different electron affinities (EA) and work functions (WF). Prior work from the ASMaD group has demonstrated that certain high-WF transition metal oxides, such as MoO_3 and V_2O_5, can effectively enhance surface transfer doping and significantly reduce the sheet resistance of H-diamond surfaces. Oxides with a high EA typically exhibit a lower CBM, making them more likely to behave as electron acceptors. Therefore, even in the absence of a high work function, materials with sufficiently large electron affinity can still facilitate effective transfer doping and enable 2DHG formation on H-terminated diamond. In this study, the focus is on investigating the influence of oxides with varying EA instead of high WF.

ALD HfO_2 comparison

The schematic band configurations for different ALD oxides on H-diamond are shown in Figure 6.2.1. To investigate how different ALD parameters influence the surface conductivity of H-terminated diamond, the first test focuses on ALD-deposited HfO_2 films. ALD techniques vary in parameters, including plasma or thermal deposition method, precursor types, deposition temperature, and film thickness. A summary of the initial test parameters is shown in Table 6.2.1.

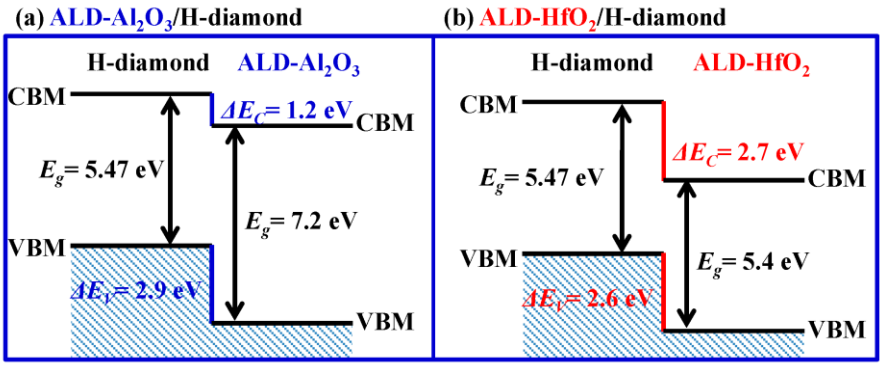

Figure 6.2.1 Schematic band configurations reported for different oxides on H-diamond [6.9].

Samples	Material	Recipe	Temperature	Thickness	Cycles
EX02	HfO_2	Plasma-TDMAH	290℃	20nm	110
ES11	HfO_2	Plasma-TDMAH	290℃	30nm	170
ET02	HfO_2	Thermal - TEMAH	290℃	30nm	170

Table 6.2.1 ALD oxide deposition experiment recipe details with deposition temperature and thickness.

Three 3 mm × 3 mm diamond samples were cleaned and hydrogen-terminated in Australia. In this study, blanket deposition was performed, and Hall measurements were taken before and after deposition to evaluate the effects. For the post-deposition measurements, electrical access to the underlying conductive area was achieved by scratching through the oxide layer at the four corners of the sample, thereby exposing the conductive surface for contact formation. The initial Hall measurements of these samples are listed in Table 6.2.2.

Sample		Sheet resistance (kΩ/□)	Mobility ($cm^2/(V·s)$)	Concentration (cm^{-2})
EX02	Before HfO_2 deposition	23	69.4	$+3.891\times10^{12}$
	After HfO_2 deposition	/	/	/
ES11	Before HfO_2 deposition	15	90.9	$+4.59\times10^{12}$
	After HfO_2 deposition	/	/	/
ET02	Before HfO_2 deposition	16	81.7	$+4.61\times10^{12}$
	After HfO_2 deposition	11	62.1	$+8.6\times10^{12}$

Table 6.2.2 Initial results of Hall measurement for ALD HfO_2 experiment.

After ALD HfO_2 deposition, samples EX02 and ES11, which were using plasma-enhanced ALD with TDMAH precursors, exhibited non-conductive surfaces, indicating the loss of 2DHG conductivity. In contrast, sample ET02 fabricated using thermal ALD with TEMAH precursors showed enhanced surface conductivity, with sheet resistance decreasing from 16 kΩ/□ to 11 kΩ/□. This suggests that thermal ALD helps preserve or even improve the transfer doping effect.

As shown in Figure 6.2.1, the CBM of HfO_2 typically lies at approximately –2.7 eV relative to the vacuum level. Given that the VBM of H-diamond is situated around –4.2 eV, the CBM of HfO_2 remains higher than the diamond VBM, suggesting that direct electron transfer from H-diamond to the oxide should not occur. However, a decrease in resistivity with ALD HfO2 deposition was observed. This behaviour may arise from interface dipoles or defects, which can lower the oxide CBM or mid-bandgap states that act as electron acceptor states. Therefore, although HfO_2 does not have an essentially high EA, it may still contribute to partial hole accumulation.

In addition, to determine whether the observed reduction in conductivity was due to the oxide layer itself or damage caused by plasma exposure during deposition, 10:1 BOE etching was performed to selectively remove the HfO_2. Hall measurements were then repeated. For thermally deposited HfO_2, the sheet resistance of the sample recovered to 16 kΩ/□ from 11 kΩ/□ after oxide removal, implying that the oxide contributed to improving the 2DHG via surface transfer doping. In contrast, for plasma-treated samples, conductivity did not recover after oxide removal, suggesting that the H-termination had been damaged by plasma exposure.

Importantly, previous studies have reported that HF/BOE treatment does not leave detectable fluorine residues nor significantly degrade the H-terminated diamond surface [6.10]. This is consistent with observations that after BOE removal of thermally deposited oxides, the surface conductivity returned to the pre-deposition level, confirming that the BOE process itself does not adversely affect the H-termination conductivity.

Al_2O_3 deposition method comparison

Previous reports have shown that in-situ vacuum annealing prior to oxide deposition can effectively remove air adsorbates from the diamond surface [6.11]. Consequently, when oxide layers are deposited immediately after in-situ annealing, the observed changes in surface conductivity can be attributed more directly to the oxide material and the deposition process itself, rather than to uncontrolled interface impurities. Based on this idea, a comparative study is focus on the Al_2O_3 to evaluate how different deposition techniques (E-beam vs. thermal ALD) and pre-annealing conditions influence the transfer doping behaviour of H-diamond. Single-crystal, 3 mm × 3 mm diamond samples were cleaned and hydrogen-terminated in Australia.

Ebeam Al_2O_3 with pre-anneal process:

1. In-situ 300 °C anneal for 1hour in vacuum (10^{-7}mbar)
2. Cool down to room temperature without breaking the vacuum

3. E-beam Al_2O_3 deposition - 15nm thick

Hall measurements were carried out before and after the Al_2O_3 deposition and the results are listed in Table 6.2.3. The sheet resistance significantly increased from 31.2 kΩ/□ in the air to 867.6 kΩ/□ after deposition, indicating that the accumulation of holes was significantly suppressed. However, the conductivity partially recovered to 54.6 kΩ/□ after BOE etching, suggesting that the suppression of transfer doping was not due to permanent degradation of the H-terminated surface, but rather the result of energy level change introduced by the Al_2O_3 overlayer.

	Before Al_2O_3	After Al_2O_3	After BOE etch
Sheet resistance (kΩ/□)	31.2	867.6	54.6

Table 6.2.3 Comparison of sheet resistance values of H-diamond before and after 15nm E-beam-evaporated Al_2O_3 and after BOE removal of Al_2O_3.

Despite performing a high vacuum anneal (1 ×10^{-6}mbar, 300 °C, 1 h) to remove surface adsorbates, the subsequent deposition of Al_2O_3 led to a significant suppression of hole conduction, in contrast to the enhancement observed with MoO_3. Importantly, E-beam evaporated Al_2O_3 induced only weak transfer doping on H-diamond, as reflected by the relatively high sheet resistance (~870 kΩ/□) compared with the much stronger doping effect of MoO_3.

Since the Al_2O_3 films deposited by E-beam evaporation may differ in their interfacial properties from those prepared by ALD, thermal ALD deposition was also tested as a comparison technique, which is known to produce conformal oxide layers. In this set of experiments, an additional control group without in-situ annealing was included to more directly assess the influence of potential residual air adsorbates on transfer doping behaviour. This comparison enables an evaluation of how Al_2O_3 affect the transfer doping mechanism via different deposition methods.

Thermal ALD Al_2O_3 with pre-anneal process:

1. In-situ 400 °C anneal for 1hour in vacuum (10^{-6}mbar)
2. Cool down to 200 °C under the vacuum
3. Thermal ALD Al_2O_3 deposition - 20nm thick

Compared with the E-beam process, the ALD experiments employed a higher annealing temperature (400 °C). This difference arose from the equipment constraints: the plasma tool used for E-beam oxide deposition is most stable at ~350 °C, whereas the ALD system allows annealing at higher temperatures. A 400 °C anneal is known to be more

effective in removing adsorbates from the H-diamond surface and therefore provides a cleaner interface [6.11]. Following annealing, the substrate was cooled to 200 °C, which corresponds to the ALD growth window, rather than to room temperature. Hall measurements were carried out before and after the Al_2O_3 deposition. Hall measurement results are listed in Table 6.2.4.

Sheet resistance (kΩ/□)	Before Al_2O_3 deposition	After Al_2O_3 deposition	Day1	After BOE etch
No pre-anneal	48	900k	189	39
Pre-anneal	39	unmeasurable	2600	42

Table 6.2.4 Hall measurements result of ALD Al_2O_3.

For the sample without in-situ annealing, the sheet resistance increased significantly from 48 kΩ/□ to 900 kΩ/□ immediately after oxide deposition, indicating a strong suppression of 2DHG. Over time, the conductivity partially recovered, and the resistance decreased to 189 kΩ/□ after one day. It suggests a slow recovery, potentially due to the relaxation of interface states and slow charge trapping and releasing within the Al_2O_3 layer. After the Al_2O_3 layer was removed by BOE etching, the resistance returned to 39 kΩ/□, close to its original value, confirming that the suppression was reversible and not caused by permanent damage to the hydrogen termination.

In contrast, the sample subjected to pre-annealing at 400 °C in a vacuum (10^{-6} mbar) exhibited better performance in suppressing 2DHG. The conductivity dropped below the measurable limit immediately after ALD Al_2O_3 deposition, and the sheet resistance reached 2.6 MΩ/□ after one day. Following oxide removal, the sheet resistance recovered to 42 kΩ/□, nearly identical to the pre-deposition value of 39 kΩ/□. This indicates that in-situ annealing effectively removes air adsorbates and stabilises the surface, but in the present case, the Al_2O_3 films deposited at 200 °C did not enable effective transfer doping.

ALD Al_2O_3 on H-terminated diamond has been reported to support stable transfer doping, thereby sustaining or even enhancing the 2DHG. Nevertheless, other studies have demonstrated that the ability of ALD Al_2O_3 to induce transfer doping is highly dependent on the deposition conditions and the interface quality. For example, Yang et al. showed that when plasma-enhanced ALD was performed without sufficient protection of the H-termination or appropriate surface cleaning, the C 1s core level shifted from ~284.1 eV to ~285.1 eV and the surface resistance increased from ~30 kΩ to ~3 MΩ, leading to a pronounced suppression of surface conductivity [6.12]. This degradation is consistent

with plasma-induced damage to the H-terminated surface, which has also been verified in the ALD HfO_2 experiment.

Several studies have reported that the transfer doping behaviour of ALD Al_2O_3 on H-terminated diamond is strongly dependent on the deposition temperature and interface quality. Yu et al. suggested that deposition temperatures above 400 °C are generally required to achieve stable transfer doping [6.13]. Without sufficient interface cleaning by in-situ annealing, residual adsorbates are likely to hinder charge transfer, even at elevated deposition temperatures. The present results are therefore consistent with the view that both growth temperature and interface preparation are critical, although the precise mechanism may vary with growth conditions and film quality.

While some reports indicate that transfer doping in hydrogen-terminated diamond can be achieved with Al_2O_3 deposition at temperatures around 200 °C, our experiments under similar conditions did not yield effective doping, regardless of pre-annealing treatment. This discrepancy can be understood from a fundamental electronic structure perspective: the electron affinity of Al_2O_3 is approximately 1.2 eV, positioning its conduction band minimum above the valence band maximum of diamond. As a result, the band alignment does not satisfy the condition for direct electron transfer from diamond to the oxide, which is essential for transfer doping to occur.

In this study, samples deposited at 200 °C exhibited a clear degradation in electrical properties. Without pre-annealing, the sheet resistance increased sharply from 48 kΩ/□ to 900 kΩ/□. Even with pre-annealing—which preserved a relatively clean H-diamond surface conductivity was still lost after Al_2O_3 deposition. These results underscore that both deposition temperature and interface preparation are critical. However, the absence of doping here points to an inherent limitation in the band alignment.

It is worth noting that earlier reports of successful transfer doping under similar conditions may have been influenced by defects introduced during the ALD process, such as those related to precursor purity or chamber conditions. In contrast, with our current optimised ALD system where such extrinsic defects are minimised, the intrinsic electronic structure dominates, and no transfer doping effect is observed. This supports the conclusion that achieving transfer doping with Al_2O_3 on H-diamond is not feasible under well-controlled conditions, due to the misalignment of the band structures.

Low-temperature ALD Al_2O_3 films may contain fixed or trapped charges; however, no high-temperature post-deposition annealing was applied in this work, and the observed device behaviour is primarily interpreted in terms of oxide–diamond interface effects.

Post-deposition annealing of Al_2O_3 may be explored in future work to tune oxide fixed charge and interface trap density, although the annealing temperature must be carefully limited to avoid degradation of the hydrogen termination.

6.3 Summary

In this chapter, a variety of surface terminations—hydrogen (H), oxygen (O), fluorine (F), silicon (Si), and scandium (Sc) and their influence on the surface conductivity and transfer doping behaviour of single-crystal diamond were investigated. Hydrogen termination serves as the baseline due to its well-established NEA properties and 2DHG formation, while other terminations were explored for their stability and potential to modulate surface electronic properties.

Oxygen-terminated surfaces can be prepared via high-temperature acid cleaning, oxygen plasma treatment, and UV-ozone treatment, all of which exhibit insulating behaviour. Water contact angle measurements are used to infer the degree of surface oxidation. Fluorine termination also significantly increased surface hydrophobicity.

From these results, an important lesson is that surface chemical stability alone is insufficient to enable transfer doping; the presence of a suitable surface dipole and favourable band alignment is essential for sustaining conductive surface channels on diamond.

Although silicon and scandium terminations were explored as promising routes to achieve NEA and transfer doping on diamond, the experimental results indicate that both approaches remain highly challenging in their current forms. While high-temperature annealing promoted conductivity on the Si-deposited surface, the measured sheet resistance and carrier concentrations suggest that the observed electrical behaviour may not result from ideal C–Si bonding, but rather from partial graphitisation. This highlights a key limitation of metal-based or hybrid surface terminations: processing conditions required to activate conductivity may inadvertently compromise surface integrity, undermining device reliability.

Finally, the transfer doping effects through oxide deposition on H-terminated diamond were explored. Previous studies have shown that ALD Al_2O_3 can promote transfer doping on H-diamond only under specific conditions, such as with in-situ pre-annealing and deposition temperatures above 250 °C. In agreement with these reports, optimised 200°C deposited ALD Al_2O_3 films did not enhance conductivity, regardless of pre-annealing, but instead suppressed the 2DHG. By contrast, thermal ALD HfO_2 deposition has been reported to enhance transfer doping, consistent with our observation of

improved conductivity in this case. These observations demonstrate that oxide material selection and deposition strategy play a decisive role in determining whether transfer doping is promoted or suppressed at the oxide–diamond interface.

Overall, the key lesson from this chapter is that effective control of surface conductivity in diamond devices requires a holistic approach combining stable surface termination with carefully engineered oxide interfaces. By selecting oxide materials and deposition strategies, the H-diamond surface can be tuned to either enhance 2DHG formation or suppress hole conduction. This understanding directly informs the device design strategies adopted in subsequent chapters, enabling the realisation of both normally-on transfer-doped diamond FETs and normally-off enhancement-mode diamond MOSFETs.

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7. Ohmic contact and carbide formation on H-diamond

Achieving low-resistance ohmic contacts is critical for high-performance H-diamond devices, as it directly influences output current, on-resistance, transconductance, and overall device performance. However, forming reliable contacts on H-diamond remains a challenge due to the surface termination characteristics.

High work function metals, such as gold (Au), are commonly used to form ohmic contacts on H-diamond. However, Au exhibits poor adhesion to the hydrogen-terminated surface and cannot form stable interfacial compounds, which can lead to contact degradation under thermal and possibly electrical stress. To overcome these limitations, metal carbide contacts, such as titanium carbide (TiC), have been explored. Ti can react with diamond to form conductive and adherent TiC layers during high-temperature annealing [7.1]. The metal/metal carbide contacts show improved adhesion, thermal stability, and lower contact resistance compared to conventional Au contacts [7.2].

This chapter focused on identifying more stable, low-resistance ohmic contacts on hydrogen-terminated diamond using as-deposited metals and investigating the formation of metal carbide interfaces to enhance device performance and ensure stability under high-temperature operation.

7.1 As-deposited metal ohmic contacts

To achieve low-resistance ohmic contacts on H-diamond, high work-function metals are typically preferred. Table 7.1.1 summarises the reported work function values of the metals investigated in this study [7.3].

Metal	Work function
Gold (Au)	5.1-5.47
Palladium (Pd)	5.22-5.6
Molybdenum (Mo)	4.36-4.95

Table 7.1.1 Work function of contact metals.

To evaluate the as-deposited metal contact behaviour on H-diamond, both Transmission Line Model (TLM) and Circular Transmission Line Model (CTLM) structures were fabricated on single-crystal, polished (100) diamond substrates. The diamond samples have been acid-cleaned to remove surface contamination, as described in the previous chapter. Subsequently, the samples were hydrogen-terminated by hydrogen plasma

treatment performed in Australia. A schematic of the fabrication flow is shown in Figure 7.1.1.

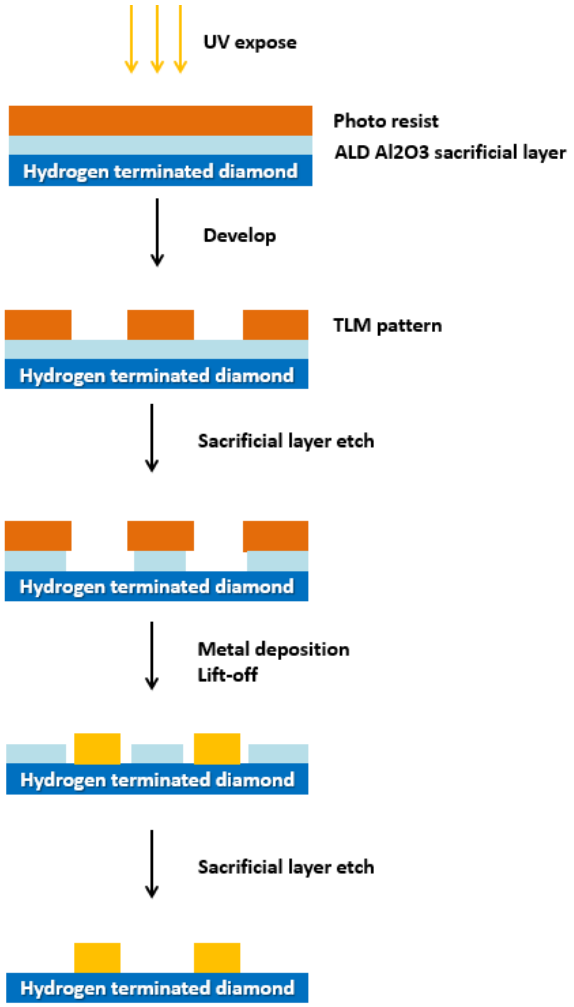

Figure 7.1.1 A schematic of the fabrication flow of the TLM/CTLM structure.

An ALD Al_2O_3 layer was deposited on the H-diamond surface as a sacrificial layer to protect the hydrogen termination during the photolithography process and metal patterning steps. A bi-layer photoresist stack including LOR series and S1805 was used for photolithography. Detailed parameters of the photolithography process are provided in Appendix A.

For Au contacts, a TLM structure consisted of rectangular pads (100 μm × 100 μm) patterned at spacings ranging from 2 to 8 μm was fabricated using 150 nm of Au. Because TLM measurements require electrically isolated regions between contacts to avoid parasitic current paths, fabricating TLM structures for multiple metals on the same sample would require additional isolation steps and repeated e-beam lithography exposures, making the process complex and time-consuming. Therefore, the Au TLM

structure was fabricated on a dedicated isolated sample, while subsequent experiments employed CTLM in order to allow testing of multiple metals on the same sample.

Hence, Pd and Mo contacts were characterised using CTLM structure. The CTLM approach does not require substrate isolation and can be readily defined by photolithography using a mask, which enables multiple contact metals to be patterned and directly compared on the same sample. Pd (140 nm) and Mo (30 nm Mo / 30 nm Pt / 80 nm Au) contacts were sequentially deposited in two steps. A protective Pt/Au capping layer was employed to prevent Mo oxidation during ambient exposure and to ensure a comparable total thickness with the Pd stack.

The CTLM structures consisted of concentric circular contacts with an inner radius of 50 μm and varying gap sizes from 2 μm to 10 μm. Following metal deposition, lift-off was carried out, and the sacrificial Al_2O_3 layer was selectively etched using BOE solution to expose the hydrogen-terminated diamond surface between the contacts. BOE etching is a standard method for selectively removing oxides without significantly damaging the H-terminated diamond surface conductivity, as discussed in section 6.2. The optical images of fabricated TLM/CTLM structures are shown in Figure 7.1.2.

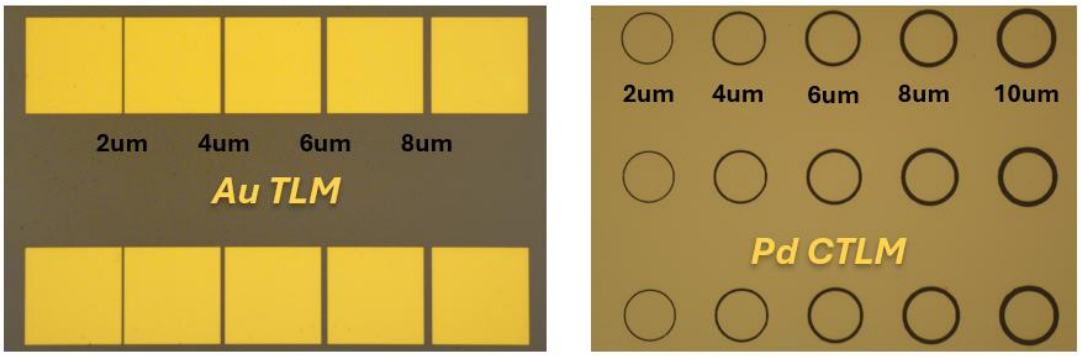

Figure 7.1.2 The optical images of TLM/CTLM structures.

The electrical measurements were performed using a two-probe setup, where each probe contacted one of the metal pads adjacent to the gap in either the TLM or CTLM structure. The voltage sweep (−10 V to +10 V) was applied across the gap, and the resulting current was recorded to extract the total resistance between the contacts. All measurements were conducted in air at room temperature. A linear fitting of the total resistance with the gap distance was performed, and the slope of the fitted line represents the sheet resistance, while the intercept represents twice the contact resistance. The calculation equations of the TLM and CTLM structures were introduced in Chapter 5.

Figure 7.1.3 shows the IV result of the TLM measurement for the Au contact. Figure 7.1.4 shows the linear fit result of each gap. A clear linear relationship was observed between the measured resistance and gap spacing, indicating a uniform sheet resistance and contact geometry. From the linear fit, the contact resistance of the as-deposited Au contact is 2.21 Ω·mm. This result suggests that Au can form a relatively low-resistance ohmic contact without annealing.

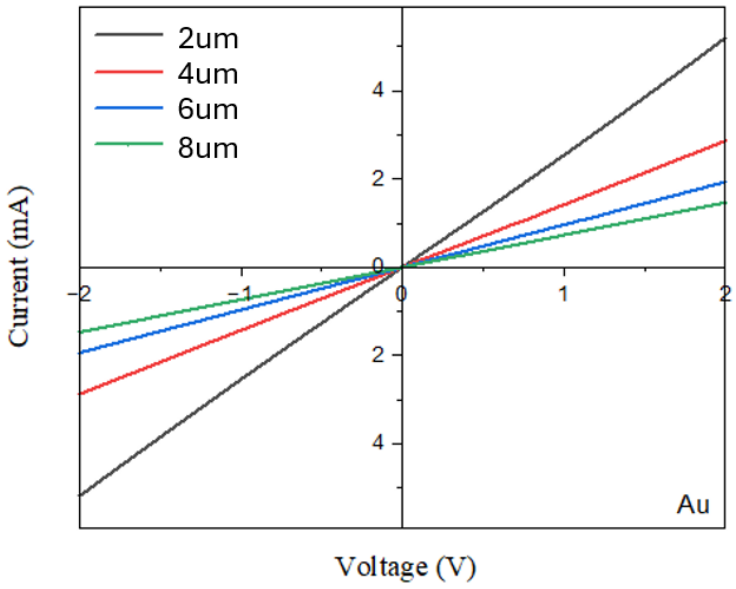

Figure 7.1.3 IV results of TLM measurement, Au as ohmic contact metal.

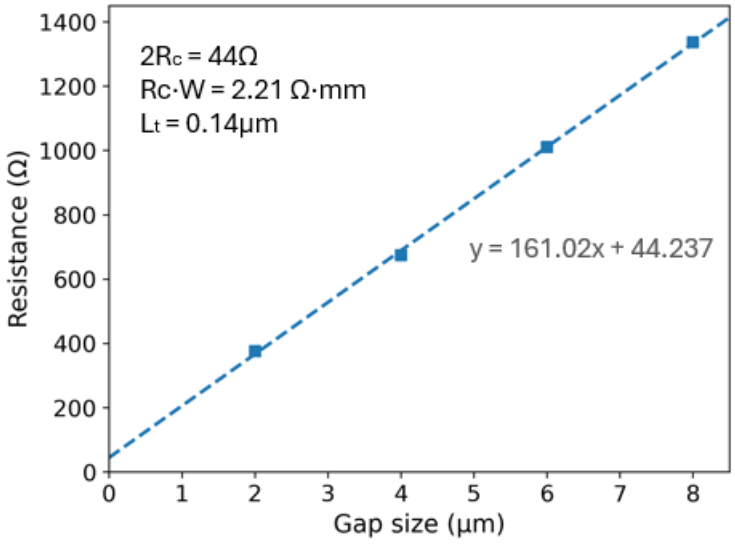

Figure 7.1.4 TLM measurement linear fit result, Au as ohmic contact metal.

The IV results from the CTLM measurements for Pd and Mo contacts are presented in Figure 7.1.5, and the linear fit for each gap is shown in Figure 7.1.6. The extracted corrected contact resistances were 6.83 Ω·mm for Pd and 5.96 Ω·mm for Mo,

respectively.

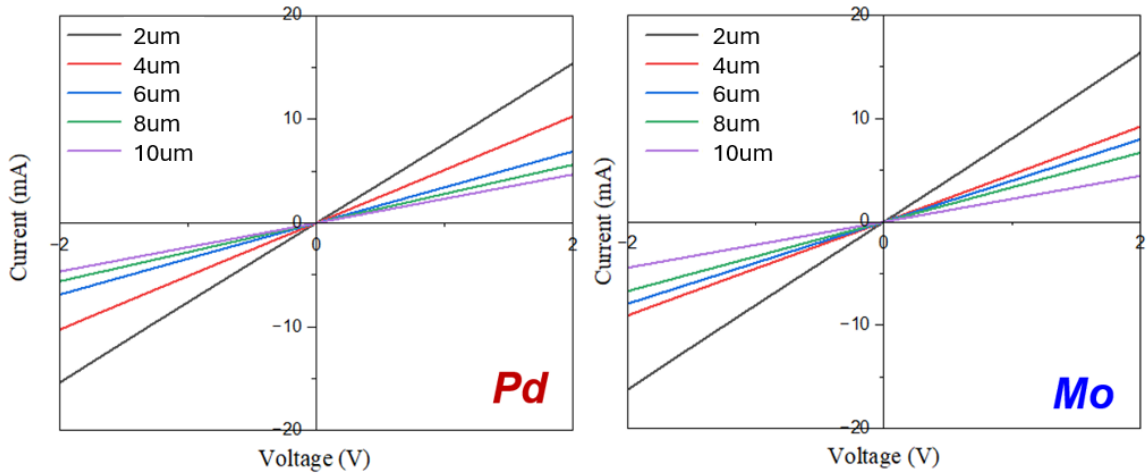

Figure 7.1.5 IV results of CTLM measurement, Pd and Mo as ohmic contact metal.

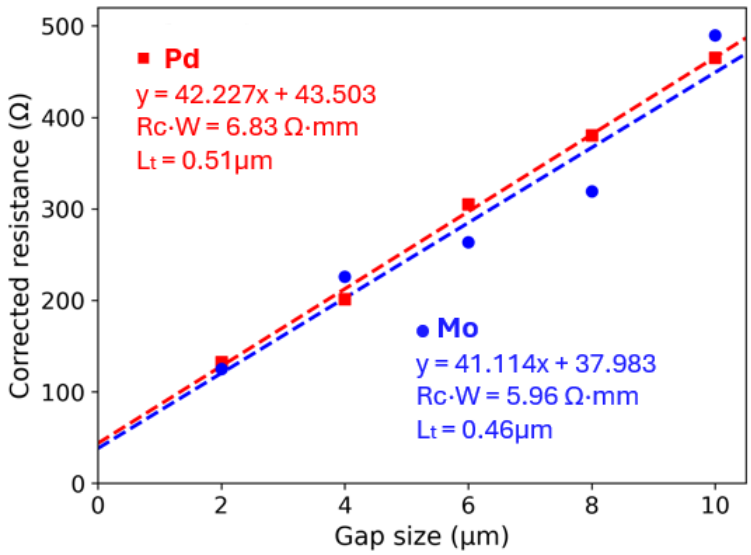

Figure 7.1.6 Pd and Mo as ohmic metal: CTLM measurement results.

Although Pd has a higher work function (5.22- 5.6 eV) than Au (5.1- 5.47 eV) and is theoretically expected to form better ohmic contacts to H-terminated diamond, the measurements indicate that Au exhibits the lowest contact resistance among the three metals tested. It should also be noted that contact resistance is often related to the sheet resistance (R_{sh}) of the H-diamond as well, lower R_{sh} generally results in lower contact resistance. In these experiments, the initial R_{sh} of the Au sample was approximately 16 kΩ/□, while the Pd sample exhibited a lower R_{sh} of 10 kΩ/□. However, the results showed that Au exhibited a lower contact resistance than Pd, which highlights that the relationship between work function, sheet resistance, and practical contact behaviour may not be straightforward. Both Pd and Mo contacts demonstrate linear IV behaviour

and relatively low resistance, confirming their ability to form good ohmic contacts on H-diamond.

Theoretically, Au typically interacts via weak van der Waals forces, meaning its adhesion relies primarily on surface tension and mechanical coverage rather than actual chemical bonding. In contrast, density functional theory calculations suggest that Pd can partially chemisorb at the diamond surface, forming stronger interfacial interactions than Au [7.4]. Such chemisorption is predicted a more favourable alignment of the Pd Fermi level relative to the diamond valence band maximum, thereby reducing the hole injection barrier and improving adhesion compared with Au. This makes Pd a more promising candidate for forming reliable ohmic contacts to H-terminated diamond devices.

However, this experiment discovered that Pd also suffers from adhesion issues on H-diamond. In some cases, Pd patterns exhibited peeling behaviour that was even more severe than that of Au. This might be caused by multiple factors. Although the poor adhesion of Au is mainly due to its weak interfacial interaction, since it does not attempt to chemically bond with the substrate, its behaviour is relatively less affected by minor surface contamination. In contrast, Pd is more chemically “active” and tries to interact with the substrate. Hence, its adhesion is perhaps more sensitive to the substrate conditions. For instance, although Pd may initially adhere well to a clean H-diamond surface, its adhesion is highly sensitive to subsequent fabrication steps. During photoresist stripping or the lift-off process, Pd is easier to peel. This suggests that Pd may form stronger adhesion with neighbouring materials, such as resist residues or subsequently deposited metals, than with the diamond surface itself. Moreover, Au can relieve intrinsic stress through deformation and is therefore regarded as a low-intrinsic-stress metal. This implies that although Au films often exhibit poor adhesion, they are rarely stress-driven delaminating. In contrast, Pd films are mechanically stronger and tend to accumulate higher stress, which makes them more sensitive to stress-induced peeling or cracking [7.5]. An example of an optical image is shown in Figure 7.1.7.

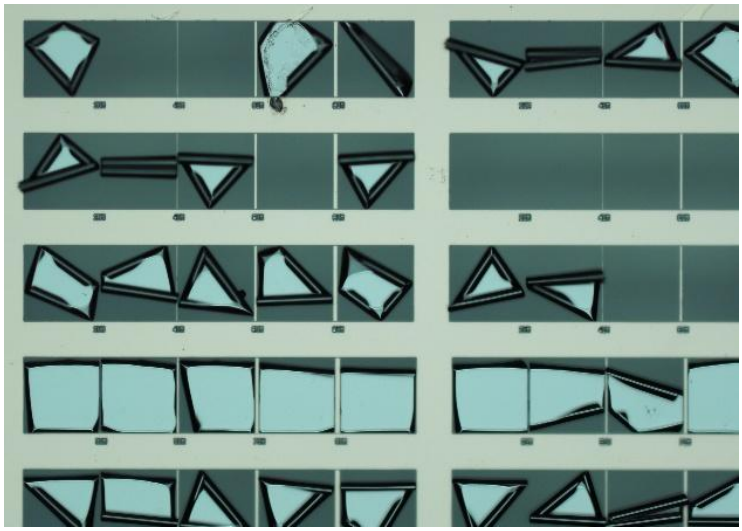

Figure 7.1.7 Optical image of Pd film peeling after lift-off.

The as-deposited Mo contact in this work exhibited a contact resistance of 5.96 Ω·mm. However, whether Mo can form a stable ideal ohmic contact to H-diamond needs further discussion. Theoretically, the reported work function of Mo ranges from 4.36 eV to 4.95 eV, depending on the crystal orientation and metal film condition. This range lies near or slightly below the VBM of H-diamond, making Mo a challenging candidate for ohmic contact formation. The ohmic contact behaviour of Mo in this experiment may be explained by the following ideas.

First, the electronic properties of Mo films are known to be sensitive to deposition parameters. Crystalline orientation and surface roughness can lead to variations in the practical work function. Secondly, the interface effect may also play a role in reducing the barrier. This could result in a Schottky barrier height that is lower than the theoretically calculated value, thereby achieving more efficient hole injection [7.6].

In addition, oxidation of the Mo surface during processing has to be considered. In this fabrication, the metal deposition chamber did not support in-situ Mo/Pt/Au deposition. Consequently, the sample was shortly exposed to ambient air during the transfer from Mo to Pt/Au deposition, introducing the possibility of a thin MoO_3 interlayer at the interface of Mo and Pt. However, the deposited Mo layer was 30 nm thick, and the sample exposure to air was minimised immediately after deposition. Therefore, while the formation of a very thin native oxide at the Mo/Pt interface cannot be entirely ruled out, the observation of clear ohmic behaviour indicates that any such oxide must be extremely limited and discontinuous and cannot dominate the current transport. The primary conduction is still considered to be provided by Mo. Further XPS or TEM studies

would be valuable to verify the exact interfacial chemistry and clarify the potential influence of such an ultrathin oxide layer.

7.2 Carbide formation

Achieving low-resistance and thermally stable ohmic contacts remains a major challenge for H-diamond devices. While as-deposited metals such as Au and Pd can exhibit ohmic behaviour, their poor adhesion and limited thermal robustness pose reliability concerns for long-term operation or high-temperature processing. This motivates the exploration of alternative contact strategies instead of the as-deposited metal contact.

Metal carbides, such as titanium carbide (TiC), offer a promising solution to these limitations. Carbide-based contacts are known for their excellent thermal stability, strong adhesion to diamond surfaces, and robust interfacial bonding. Several studies have reported that TiC can form at the metal–diamond interface through high-temperature annealing, typically in a hydrogen environment. Jingu et al. reported that TiC-based source/drain contacts in H-diamond FETs achieved a specific contact resistance of 9 Ω·mm, demonstrating the electrical viability of this approach [7.1].

In this section, the focus is on the conditions under which metal carbide can be formed on diamond. Several process parameters, including annealing atmosphere, temperature, and surface protection, are investigated to assess their impact on carbide formation, interface uniformity, and electrical performance.

Based on the comparison of the recipes from the literature, it has been found that some key conditions are necessary for the formation of stable metal carbides on diamond. First, hydrogen termination is usually reintroduced after carbide formation to restore the surface conductivity of H-diamond, as reported in previous studies [7.1]. Second, the Ti layer must be protected during annealing to prevent unwanted oxidation or reactions with ambient gases, which may affect the carbide formation. Third, the annealing atmosphere will also affect the carbon diffusion from the diamond lattice to the Ti.

Due to the absence of post hydrogen-termination capability in the lab and the safety concerns associated with high-temperature hydrogen annealing, the strategy relies on the pre-hydrogen-terminated diamond substrates. All following experiments were conducted on (100)-orientation single-crystal H-diamond samples that have undergone the hydrogen plasma treatment in Australia before carbide processing. The following experiments also use the CTLM method to evaluate the performance of the metal contact, the structure as shown in Figure 7.1.2.

To reduce the degradation of the hydrogen termination and protect the Ti film, the experiment was conducted with a metal stack (Pt/Au) to cap the Ti layer. After patterning Ti/Pt/Au CTLM structures on the H-diamond, a conformal ALD Al_2O_3 film was deposited to cover the whole sample. This layer was intended to prevent hydrogen desorption and contamination during the high-temperature annealing to form the carbide contacts. Meanwhile, the annealing was carried out at 700°C under high vacuum conditions (3×10^{-6} mbar) for 30 minutes. The schematic of the fabrication process with ALD Al_2O_3 protective layer is shown in Figure 7.2.1.

After annealing, the ALD Al_2O_3 layer was selectively removed using BOE. A two-probe DC I–V sweep measurement was performed to evaluate the electrical characteristics of the metal contacts. The voltage was swept from −10 V to +10 V, and Figure 7.2.2 shows the I–V characteristics of Ti/Pt/Au CTLM structures before and after vacuum annealing at 700 °C for 30 minutes.

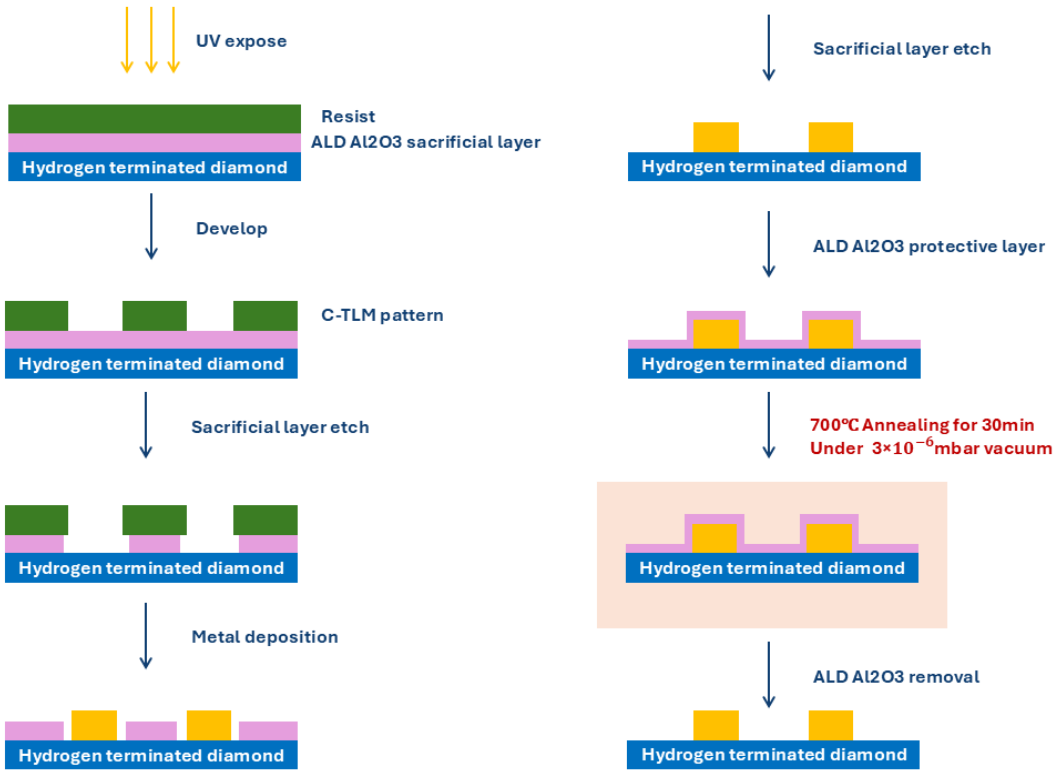

Figure 7.2.1 Fabrication process of carbide formation with ALD Al_2O_3 protective layer.

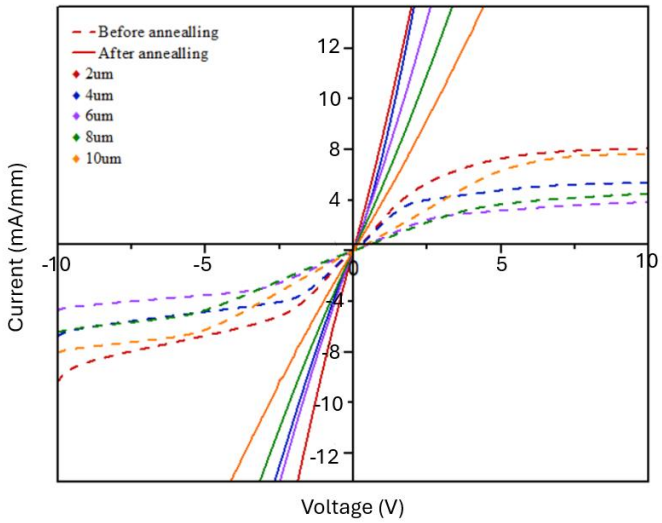

Figure 7.2.2 I–V characteristics of Ti/Pt/Au contacts on H-diamond before and after 700 °C annealing.

As shown in Figure 7.2.2, before the annealing (dashed lines), the IV curves exhibited Schottky-like behaviour, with current strongly suppressed near zero bias and increasing slightly at higher voltages. The currents were relatively low, and the scaling was not proper with the gap spacing. After annealing (solid lines), the IV curves showed significant improvement. All gaps displayed more symmetric and nearly linear characteristics over the measured voltage range, indicating a partial transition to ohmic behaviour. The currents increased significantly for all the gaps, which also proved the possibility of TiC formation. These results implied that thermal annealing encouraged the interfacial reaction between Ti and the diamond surface, leading to the possible formation of a TiC layer. However, the curves are not perfectly linear over the whole voltage range, which also suggests that TiC formation may still be incomplete or non-uniform under the current annealing conditions.

To further evaluate the role of Al_2O_3 encapsulation, the previously fabricated Mo/Pt/Au structure without encapsulation (introduced in Section 7.1) was employed here as a comparative reference. Both the Al_2O_3 encapsulated Ti/Pt/Au and the non-encapsulated Mo/Pt/Au samples were annealed at the same time under identical conditions. Although the comparison involves different metal stacks, it still provides evidence that the absence of an Al_2O_3 capping layer will lead to the degradation of H-diamond under high-temperature annealing. In addition, as mentioned in section 7.1, although Mo exhibited ohmic behaviour in the as-deposited, pre-annealed state, its interfacial contact stability after annealing remains uncertain. It has been reported that Mo can form molybdenum carbide (MoC) when annealed on diamond at high temperatures, which may influence

both contact resistance and long-term reliability. Therefore, this experiment can further provide evidence to support the possibility of Mo as an ohmic contact. Figure 7.2.3 shows the CTLM results of Ti/Pt/Au (with Al_2O_3) and Mo/Pt/Au (without Al_2O_3) contact before and after the anneal.

The two-probe DC measurements of the CTLM structures were carried out. As shown in Figure 7.2.3, the slope of the linear fit in each case corresponds to the sheet resistance (R_{sh}) of the H-diamond active area, which enables observing more directly the changes in H-termination before and after annealing.

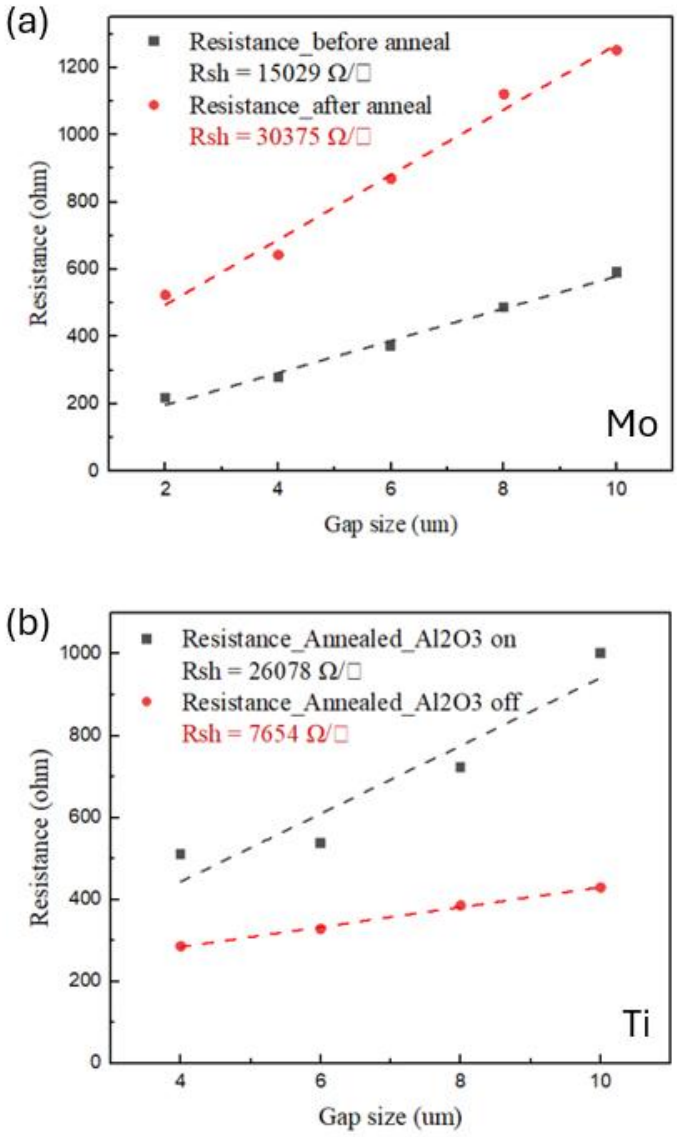

Figure 7.2.3 Annealing results of CTLM structures under different encapsulation conditions, (a) Mo fabricated Mo/Pt/Au structure without Al_2O_3 encapsulation, (b) Ti/Pt/Au with Al_2O_3 encapsulation.

For the Mo contact, the sheet resistance increased significantly from 15 kΩ/□ to 30 kΩ/□ after annealing. This clear increase in R_{sh} indicates degradation of the H-termination, which is caused by high-temperature annealing without surface encapsulation. The contact resistance (R_c) also increased, rising from 15.9 Ω·mm before annealing to 47.4 Ω·mm after annealing. Despite the Mo contact showing nearly ohmic characteristics in the as-deposited state, annealing did not provide any improvement in contact resistance. The possible reason is in the case of higher sheet resistance, the extracted R_c values are affected, since increased R_{sh} intensifies current crowding and spreading resistance at the contact edge, leading to an apparent overestimation of R_c [7.7]. Secondly, Mo is known to react with diamond at elevated temperatures, and the possible formation of a thin, discontinuous MoC layer at the interface may further increase R_c [7.8].

In contrast, due to the Schottky-like behaviour of the initial Ti contact, reliable sheet resistance could not be extracted before annealing. To address this, a Pd CTLM structure was fabricated on the same sample before annealing, which was used to calculate the initial sheet resistance of the H-terminated diamond surface. The Pd contacts exhibited linear I–V characteristics, and the sheet resistance is 10.2 kΩ/□. Ideally, the Pd CTLM should have been re-measured after annealing to evaluate the effect of high temperature on the hydrogen termination. However, due to poor adhesion of Pd, the contacts were no longer stable after Ti/Pt/Au fabrication, and electrical measurements could not be performed. Nevertheless, by comparing the Ti CTLM result after annealing and Al_2O_3 removal, which showed the sheet resistance of 7.6 kΩ/□, with the initial Pd-based result of 10.2 kΩ/□, it can be inferred that the hydrogen termination has not been damaged. The reduction in R_{sh} is possibly attributed to the time-dependent recovery of the 2DHG after removing the sacrificial Al_2O_3 in BOE. Once the gap region is exposed to ambient air, the surface adsorbate layer gradually recovers, enhancing transfer doping and thereby lowering R_{sh}. In addition, the non-uniformity of H-termination and minor variations in post-etch surface condition can further contribute to differences. Since the annealing was performed with the Al_2O_3 encapsulating over the whole surface, the R_{sh} change is unlikely to be caused by anneal-induced desorption; instead, it reflects differences in the post-BOE recovery state of the 2DHG. This supports the conclusion that the ALD Al_2O_3 capping layer effectively protected the H-terminated diamond surface during the high-temperature annealing.

Moreover, combining the IV characteristic results as shown in Figure 7.2.2, the electrical behaviour of the Ti contacts clearly improved from the initial result to a more linear I–V characteristic, supporting the possibility of TiC formation at the interface. This suggests that the annealing process not only preserved the hydrogen termination but also enabled

the carbide formation at the interface of Ti/H-diamond. The extracted contact resistance was approximately 29 Ω·mm, which is higher than the reported TiC ohmic contacts on H-diamond (9 Ω·mm) [7.1]. This indicates that while the initial annealing process promoted the carbide formation, the reaction may have been incomplete or non-uniform.

To improve both the uniformity of TiC formation, the following experiment was designed with a high annealing temperature. Given that the previous results verified ALD Al_2O_3 can be used as a protective layer for the hydrogen termination and redeposited a conformal ALD Al_2O_3 film over the entire sample again to protect the H-diamond surface for the following more aggressive annealing. Rapid thermal annealing (RTA) was selected as the heating method to provide a fast, high-temperature process. The Al_2O_3 layer also served to block any undesired effects from the N_2 environment in the RTA system. A second annealing step was performed on the same sample at 825 °C for 1 minute. The CTLM measurement results before and after RTA anneal are shown in Figure 7.2.4. Both datasets in Figure 7.2.4 correspond to contacts annealed with the Al_2O_3 encapsulation. After annealing, the oxide was selectively removed by BOE and all CTLM measurements were performed on the de-encapsulated surface.

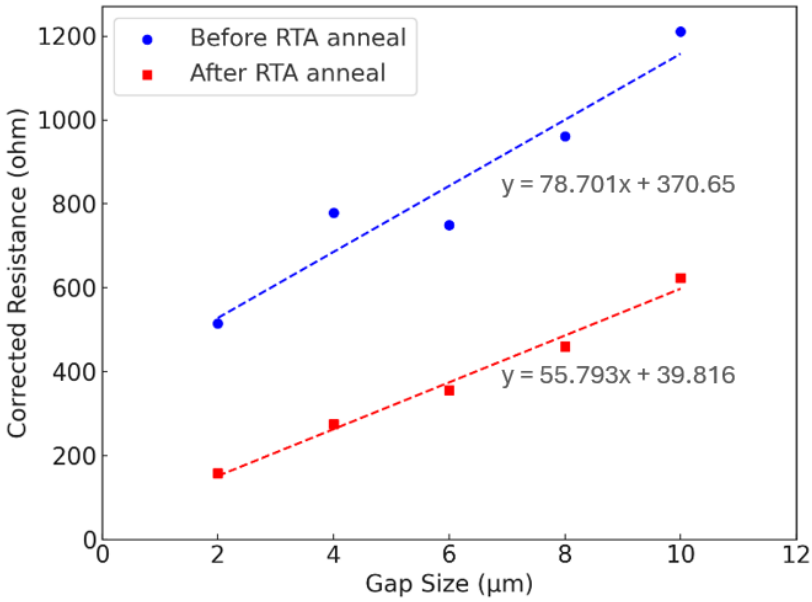

Figure 7.2.4 CTLM measurement result of Ti/Pt/Au contact before and after the subsequent 825 °C RTA anneal.

As shown in Figure 7.2.4, the blue data points exhibit the results before the 2nd anneal, suggesting that although the fitted line is linear, the original data points are relatively scattered, showing a coefficient of determination (R^2) of 0.90. In contrast, the red data points collected after the second RTA run show a much tighter fit with $R^2 = 0.99$, indicating

enhanced contact uniformity and more stability across all the gaps. In addition, the contact resistance drops dramatically from 29 Ω·mm before RTA annealing to 6.5 Ω·mm after RTA annealing. This result supports the assumption that TiC formation became more uniform and complete after the second, high-temperature annealing step.

However, while the electrical data suggest enhanced carbide formation, direct microstructural evidence, such as transmission electron microscopy (TEM), would be required to confirm the presence and continuity of the TiC layer. Ideally, a dedicated sample should be fabricated with a Ti/Pt/Au stack and directly subjected to RTA under ALD Al_2O_3 encapsulation for structural characterisation. Unfortunately, due to limitations in sample availability and fabrication time, this confirmation could not be completed within the current timeline of the study.

7.3 Summary

This chapter has investigated the formation of ohmic contacts on H-diamond using both as-deposited metal structures and metal carbide formation based on thermal annealing. The extracted contact resistance values are discussed in the context of representative literature reports to assess their relative performance within the field. Key findings are summarised as follows:

- As-deposited contacts: Among the tested metals, Au exhibited the lowest contact resistance (2.21 Ω·mm) on H-diamond in its as-deposited state, despite its known weak adhesion. This value is a typical A-based contact resistance reported for H-diamond, which is commonly in the range of 0.9-5.5 Ω·mm [7.9]. Pd also showed a moderate ohmic behaviour (6.83 Ω·mm), attributed to its higher work function and chemical bonding capability. Mo demonstrated a contact resistance of 5.96 Ω·mm. It should be noted that most literature reports for metal contacts on hydrogen-terminated diamond provide specific contact resistivity values (ρ_c), rather than normalised contact resistance (Ω·mm), and direct conversion is not possible without detailed structural parameters. Based on representative reported ρ_c values for Pd contacts, the corresponding normalised contact resistance is generally inferred to be from a few to a dozen Ω·mm [7.10]. On this basis, the Pd contact resistance achieved in this work compares favourably with prior studies. To the best of the author's knowledge, no published contact resistance values have been explicitly reported for Mo on hydrogen-terminated diamond, preventing direct literature comparison. It should be noted that variations in H-diamond sheet resistance across different samples also affect the extracted contact resistance values, as discussed above.

- Metal carbide formation contacts: The Ti/Pt/Au contact stack, when annealed at 700 °C and subsequently at 825 °C with ALD Al_2O_3 encapsulation, showed significant improvements in both contact resistance and I–V characteristic. The final contact resistance reached 6.5 Ω·mm, which is comparable to or lower than previously reported TiC-based contacts (~9 Ω·mm) [7.1]. These results suggest the formation of a conductive TiC layer at the metal–diamond interface, with improved uniformity after high-temperature RTA.
- Protective Encapsulation: The role of ALD Al_2O_3 as a hydrogen-termination preservation layer was shown to be critical. Comparative experiments between Ti/Pt/Au (with Al_2O_3) and Mo/Pt/Au (without Al_2O_3) confirmed that the encapsulated structure retained lower sheet resistance and contact integrity after annealing, demonstrating the effectiveness of this encapsulation strategy. This capability is essential for enabling high-temperature processing steps that are otherwise incompatible with H-terminated diamond.
- Limitations and further works: While electrical measurements strongly support the formation of TiC, the absence of direct microstructural evidence remains a limitation. Due to equipment and resource limitations, techniques such as TEM, could not be employed. Future work will prioritise structural characterisation and the inclusion of additional control samples to verify the property and quality of the carbide interface fully.

In conclusion, this chapter highlights the potential of metal-carbide as a strategy for achieving low-resistance ohmic contact on H-diamond. It identifies key process parameters, especially surface protection and annealing conditions. Moreover, it presents a practical approach to preserving hydrogen termination under high-temperature processing. These findings lay the foundation for further optimisation of H-diamond electronic devices.

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8. Accumulation channel H-Diamond MOSFETs

As discussed in the previous chapters, a series of studies on various surface terminations, ohmic contacts, and gate oxide materials have been conducted to establish the foundation for the fabrication of high-performance diamond-based transistors.

In this chapter, the focus shifts to the accumulation channel mechanism in H-diamond MOSFETs. Building on the findings regarding oxide applications from Chapter 6, the aim is to clarify how the interaction of surface termination and gate dielectric enables the realisation of accumulation-mode, normally off operation in H-diamond devices.

Section 8.2 provides a detailed flow of the device design and fabrication process. Furthermore, Sections 8.3 and 8.4 will present the direct current (DC) and CV performance of H-diamond accumulation channel MOSFETs, respectively. Through detailed characterisation and analysis, the potential and challenges of these devices for advanced electronic applications will be discussed.

8.1 Accumulation channel mechanism

As introduced previously, the hydrogen-terminated diamond surface exhibits p-type surface conductivity due to the formation of a 2DHG layer beneath the surface, typically enabled by ambient air adsorbates. However, when the H-diamond surface is annealed in vacuum to remove air adsorbates, the surface transfer doping mechanism is largely suppressed. This results in a significant reduction of the 2DHG, as illustrated in Figure 8.1.1(a). It's worth mentioning that the Fermi level on the H-diamond surface is largely unpinned [8.1, 8.2]. Therefore, it allows the Fermi level in close proximity to the surface to be modulated with respect to the band structure by an externally applied gate bias. As shown in Figure 8.1.1 (b), when a gate voltage is applied to such a structure, holes can be attracted to the gate region.

This causes the valence band edge to bend upwards under the gate, re-establishing a surface accumulation layer of holes. The result is the formation of a conductive channel between the source and drain. This working principle forms the basis of an accumulation-channel mode MOSFET, which also behaves as normally off when no gate bias is applied.

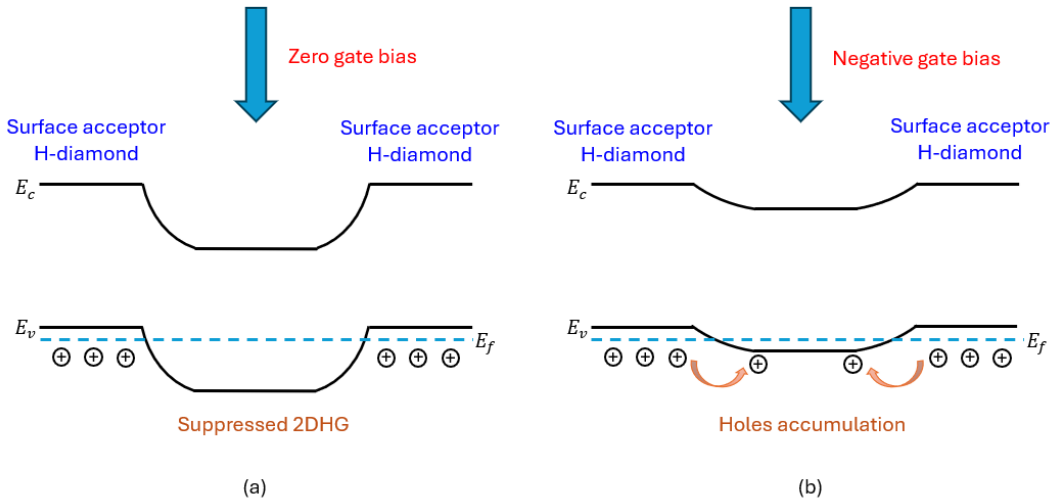

Figure 8.1.1 Energy band diagram between the gate channel and source-drain area for an accumulation channel H-diamond FET with (a) no gate bias, (b) when a negative gate bias is applied.

To experimentally verify this behaviour, the influence of Al_2O_3 deposited by ALD as a gate dielectric on H-diamond was investigated. As discussed in section 6.2, ALD Al_2O_3 can significantly suppress the surface conductivity of H-diamond. For the sample without pre-annealing, the sheet resistance increased from 48 kΩ/□ to 900 kΩ/□. For the pre-annealing oxide experiment, the sample was annealed in situ at 400 °C for 1hour in vacuum (10^{-6} mbar), the sheet resistance increased from 39 kΩ/□ to the measurable limitation, indicating that the 2DHG was completely suppressed. Importantly, after BOE etching to remove the Al_2O_3 layer, the sheet resistance of both samples returned to values close to the original (around 40 kΩ/□), confirming that the suppression in conductivity was reversible and attributed to the presence of the oxide layer.

8.2 Fabrication process

This section presents the fabrication process of H-diamond accumulation channel MOSFET devices. The device structure of this device relies on suppressing the transfer doping mechanism on the hydrogen-terminated surface to accumulate holes under the gate, forming a conductive channel upon application of a sufficiently negative gate bias. The entire fabrication process includes substrate cleaning, sacrificial layer deposition, mesa isolation, ohmic contact, bond pad, oxide dielectric deposition, gate deposition, and pad etch. A simplified schematic diagram of the fabrication process is shown in Figure 8.2.1.

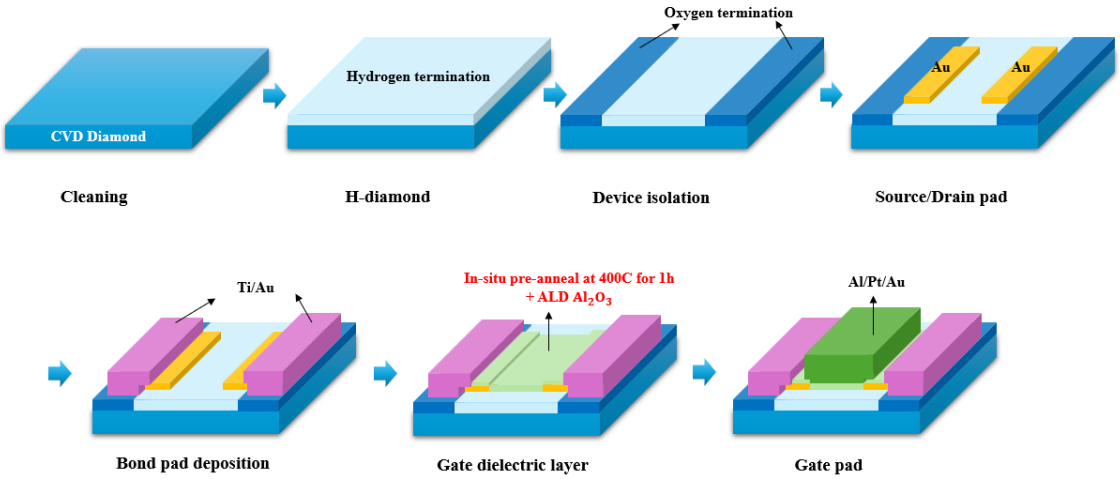

Figure 8.2.1 A simplified schematic diagram of the Accumulation Channel H-diamond FET fabrication process.

Sample preparation and sacrificial layer

A 4.5 mm × 4.5 mm, (100) orientation, single-crystal diamond substrate, single-side polished, was purchased from Element Six. To ensure a clean surface, the sample underwent a thorough cleaning process, including high-temperature acid cleaning and solvent cleaning. The high-temperature acid cleaning process is listed in Appendix A. The cleaned substrate was then sent to the collaborator in Australia, where hydrogen termination was performed under hydrogen plasma conditions. These H-terminated diamond samples need to be solvent cleaned again to remove any contamination from transport and subsequently exposed to ambient air for several days to allow the surface conductivity to stabilise. During this period, the surface conductivity was monitored by Hall measurement. Once the diamond sample reached a stable and optimal conductivity, a 20 nm thick sacrificial layer of ALD Al_2O_3 was deposited to protect the hydrogen-termination for subsequent processing steps.

Markers and isolation

Defining alignment markers and isolation levels is crucial for ensuring the integrity of devices and maintaining the accuracy of multi-layer lithography alignment. A double layer of PMMA is used for the fabrication of the lift-off marker. After spinning and baking, a thin layer of 10 nm Al is deposited on top of the sacrificial layer as a charge conduction layer (CCL) to prevent pattern distortion. The marker layers in the design file are uploaded to EBPG5200.

After the EBL exposure, the CCL is removed with CD26 for 2min. Subsequently, the sample is developed in developer (MIBK: IPA 1:2.5) for 45 seconds, followed by a 30-second rinse in IPA. Due to the sensitivity of the developer to temperature, a water bath is used to warm up the solvent to 23°C before development. As the bottom layer of PMMA is more sensitive to the electron beams, an undercut is formed after the development.

After confirming the resist development, residual resist was removed by a 200 W, 1-minute oxygen plasma ashing. The sacrificial Al_2O_3 layer was subsequently etched for 40 s at room temperature in a 10:1 BOE solution, followed by a 300 W, 2-minute oxygen plasma treatment to replace the hydrogen termination with oxygen, thereby enhancing the adhesion of subsequently deposited metals. An 80 nm Pd layer was then deposited by E-beam evaporation to define as the marker material. The metal patterns were defined by liftoff in acetone at 50 °C for at least two hours.

The fabrication of the isolation level is similar to the marker level. Alignment with the previous step was ensured by submitting the coordinates of the four corner markers to the EBPG system, which located the marker positions through backscattered electron detection from the Pd markers and diamond substrate. Then, the machine can locate the marking position by detecting the backscattered electrons from the metal marker and the diamond substrate. After development and sacrificial layer etching, the isolation zone was exposed to the air. Subsequently, a 300W 2-minute oxygen plasma was used to replace the exposed hydrogen termination with oxygen, thereby creating an insulating surface. Two isolation test structures are located at the bottom left corner and the top right corner of the sample. The design of the fabrication is shown in Figure 8.2.2, which shows the markers and the isolation structures.

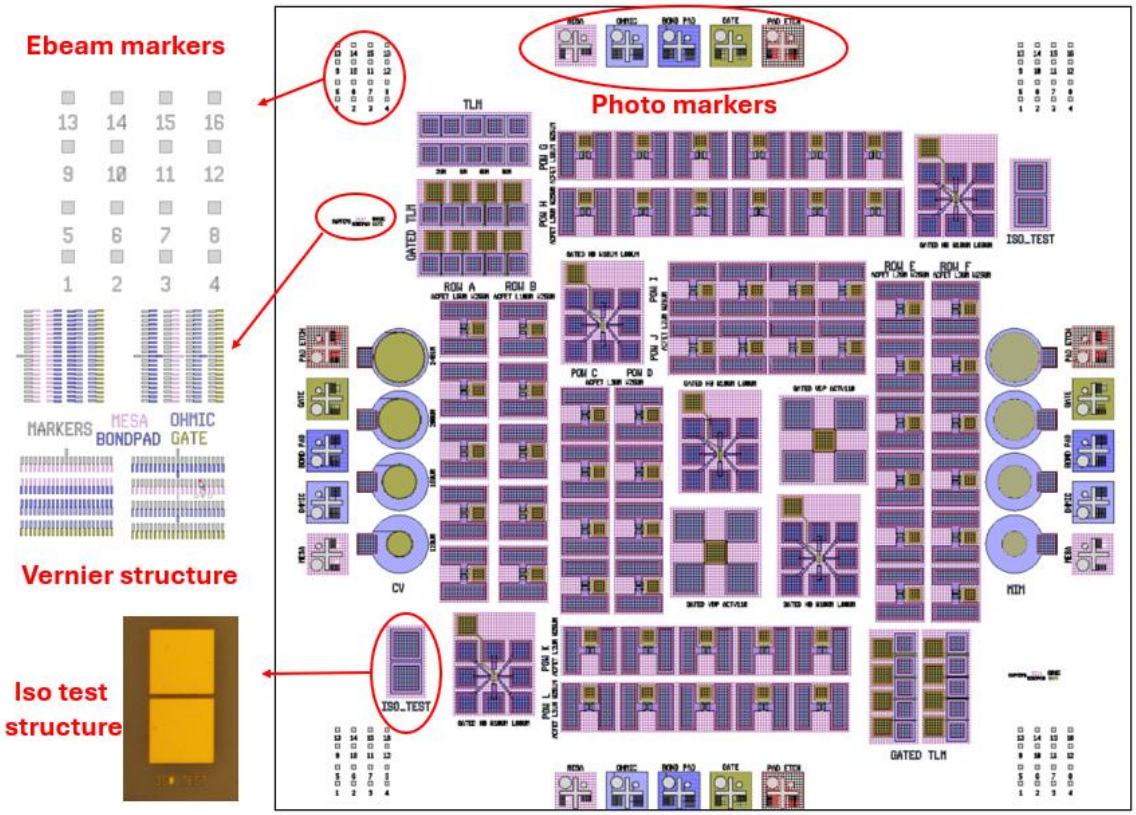

Figure 8.2.2 The L-edit design of MOSFETs and images of isolation and marker structure.

Ohmic contacts

To define the ohmic contact level, a bilayer PMMA resist is spun on top of the existing sacrificial layer, creating an undercut profile during development. A thin layer of 10 nm Al is subsequently deposited as a CCL to mitigate charging effects during EBL exposure. The sample is then patterned using an EBPG system to expose the source and drain contact regions. After exposure, the Al CCL is removed, and the bilayer resist is developed to form a well-defined undercut profile, which is essential for a clean lift-off process. A selective etch step is applied to remove the sacrificial layer only within the exposed contact windows, ensuring that the ohmic metal is deposited directly onto the H-terminated diamond surface. Subsequently, 150 nm of gold is deposited by PVD to form the contact pads. To complete the lift-off, the sample is immersed in acetone overnight in a 50°C water bath. An optical image of a lift-off gold ohmic contact is shown in Figure 8.2.3.

After the ohmic contact fabrication is completed, it is necessary to remove the original sacrificial layer and deposit a fresh one before proceeding to subsequent fabrication steps. This requirement arises from the fact that the ohmic contacts are defined directly within the active area of the device, including the source, drain, and the channel region

between them. During the lift-off process used for metal patterning, an undercut profile is introduced by the development of the e-beam resist, which inevitably causes partial removal or disruption of the sacrificial layer above the channel. As a result, the original sacrificial layer no longer provides continuous protection to the hydrogen-terminated surface across the entire active region. Hence, a new conformal ALD Al_2O_3 sacrificial layer has to be deposited to ensure complete surface coverage and protection during subsequent process steps, such as gate definition.

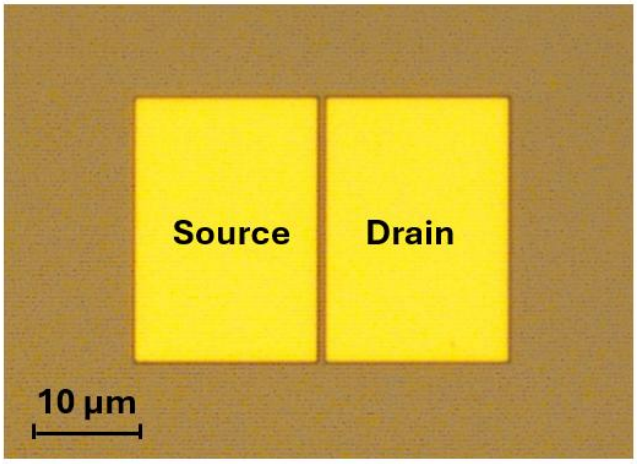

Figure 8.2.3 Optical image of a lift-off gold ohmic contact.

Bond pad

Bond pads serve as enlarged metal contacts designed to protect the ohmic contacts during subsequent electrical measurements by probing. The fabrication process of bond pads closely parallels that of the ohmic contact level. A bilayer of PMMA resist is spin-coated onto the device surface, followed by the deposition of a 10 nm Al CCL. EBL exposes the bond pad patterns. After exposure, the aluminium CCL is removed, and the resist is developed with well-defined undercut profiles. The sacrificial layer within the exposed bond pad regions is selectively removed. To enhance adhesion between the metal and the exposed diamond surface, the sample is treated with an oxygen plasma ashing step (300 W, 2 minutes). A metal stack of 20 nm titanium, followed by 200 nm gold (20 nm Ti/200 nm Au), is deposited by PVD, where titanium promotes stronger adhesion to the diamond surface. Finally, the lift-off is carried out overnight in acetone in a 50°C water bath. An optical image of a lift-off Bond pad is shown in Figure 8.2.4. The final step in the bond pad level is to entirely remove the sacrificial layer using a 10:1 BOE for 1 minute.

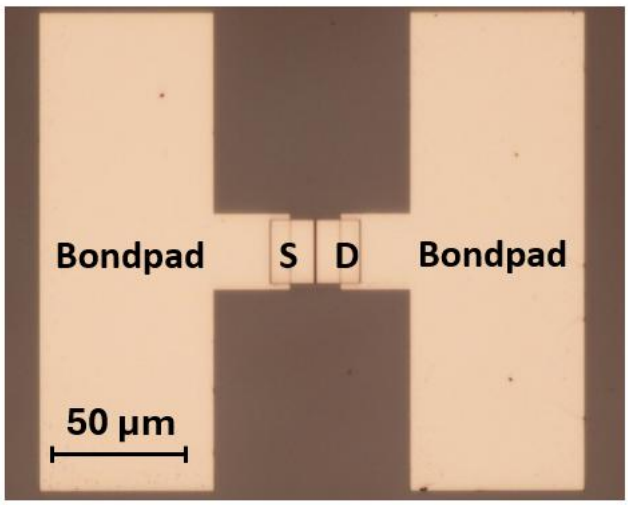

Figure 8.2.4 Optical image of bond pad level.

Oxide deposition

The gate dielectric is a key component in H-diamond FETs, enabling gate control over the channel. In this process, a 15 nm thick Al_2O_3 film was deposited using thermal ALD as the gate dielectric. Prior to deposition, the sample underwent a pre-annealing step at 400 °C for 1 hour under 10^{-6} mbar vacuum condition. This annealing process will remove surface adsorbates and suppress surface transfer doping.

After annealing, the sample was cooled in situ to 200°C before initiating the ALD process. The Al_2O_3 film was deposited via thermal ALD using trimethyl aluminium (TMA) and H_2O as the precursor. The deposition rate is 0.083 nm/cycle. This technique provides atomic-level thickness control and conformal coverage, which is essential for gate dielectric uniformity.

Gate

The gate metal defines the electrostatic control terminal of the FET device and must be patterned on top of the gate dielectric. A bilayer PMMA resist was spun onto the sample. A 10nm Al CCL is deposited to reduce charging, and exposure is performed using the EBPG system. After exposure, the CCL is removed, and the gate pattern is developed. Since the gate is deposited directly on top of the Al_2O_3 dielectric layer, no sacrificial layer removal is required at this step. Prior to metal deposition, a 200W, 1-minute oxygen plasma ashing process is applied to remove resist residue. The gate metal stack consists of 20 nm of Al, 20 nm of Pt, and 200 nm of Au. The metals are deposited sequentially via PVD. Finally, the lift-off is carried out overnight in acetone within a 50°C water bath. An optical image of a fabricated FET device is shown in Figure 8.2.5.

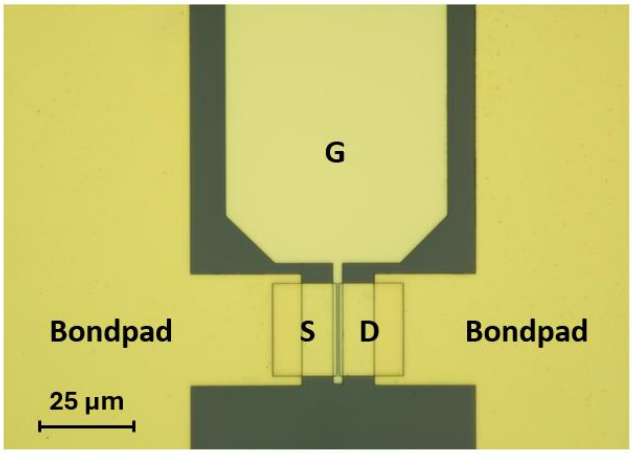

Figure 8.2.5 An optical image of a fabricated FET device.

Pads etch

After the gate dielectric deposition steps, the entire device surface, including bond pads and metal contacts, is covered by the oxide. To enable electrical probing, it is necessary to selectively remove the oxide above the bond pads through a pad etching process. This step exposes the underlying metal, allowing for reliable electrical contact during measurement by probing. A window is defined over the bond pad region by EBL. After development, a 10:1 BOE solution is used to remove the oxide layer in the exposed areas selectively. This approach ensures that only the oxide above the pads is removed, while the rest of the device remains protected. The alignment must ensure that the window is opened precisely above the bond pad without damaging adjacent features. An optical image of the pad etch level is shown in Figure 8.2.6. Since the thin layer of Al_2O_3 is nearly transparent, only the relative contrast is visible.

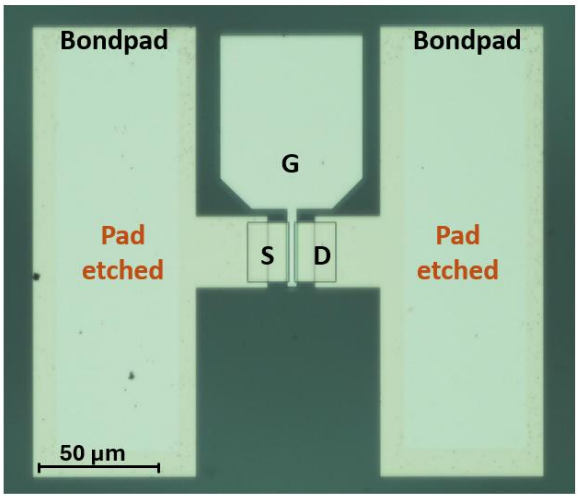

Figure 8.2.6 An optical image of the completed Accumulation Channel H-diamond FET including pad etch level.

8.3 MOSFET measurement

As introduced above, the source and drain pads are formed by Au to form ohmic contacts on H-diamond. The gate dielectric is 15 nm pre-annealed Al_2O_3 deposited by ALD, which effectively suppresses the transfer doping mechanism of H-terminated diamond surfaces. Ti/Au layers are overlapped on top of the ohmic pads for further electrical probing measurement. The schematic diagram of the H-diamond accumulation channel MOSFET structure is shown in Figure 8.3.1.

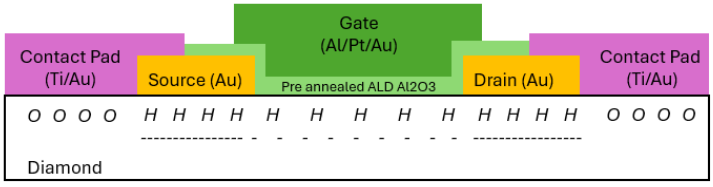

Figure 8.3.1 The schematic diagram of the cross-section H-diamond accumulation channel device structure.

To further investigate the impact of channel length on device performance, a series of H-diamond accumulation channel MOSFETs with varying channel lengths (1 μm, 2 μm, 3 μm, 5 μm, and 10 μm) were designed and fabricated. All devices share a uniform channel width of 25 μm and identical layer structures as described above. Importantly, the gate overlaps the source and drain regions on both sides by 1 μm, ensuring robust control and minimising parasitic resistance. In the following analysis, the electrical performance of the accumulation channel MOSFET with a 1 μm channel length will be analysed in detail as a representative example. Comprehensive DC characterisation, including output, transfer, leakage, breakdown, and contact properties, will be presented for this device. Subsequently, a comparative summary of the key performance across devices with different channel lengths will be provided, highlighting the scaling effects and trends observed in H-diamond accumulation channel MOSFETs.

Output Characteristics and Hysteresis

To establish the basic operation of the fabricated H-diamond MOSFETs, the output characteristics were first measured. Figure 8.3.2 shows the output characteristics of the H-diamond MOSFET with L_g=1 μm, W_g=25 μm, measured at various gate voltages from 0 V to –12 V in steps of –1 V. The device demonstrates clear p-type accumulation-channel behaviour, with the drain current I_{ds} increasing significantly as the gate bias V_{gs} becomes more negative. This behaviour reflects the modulation of the channel potential by the gate bias, leading to the formation of a hole accumulation layer at the diamond surface. The current saturation suggests that the channel carriers are effectively confined

and controlled by the gate field. The maximum drain current reaches over 35 mA/mm at V_{gs}= -12V and V_{ds}= -10V, which highlights the good conductivity of the 2DHG channel. The curves also exhibit an obvious saturation and linear region, which is consistent with classical MOSFET operation.

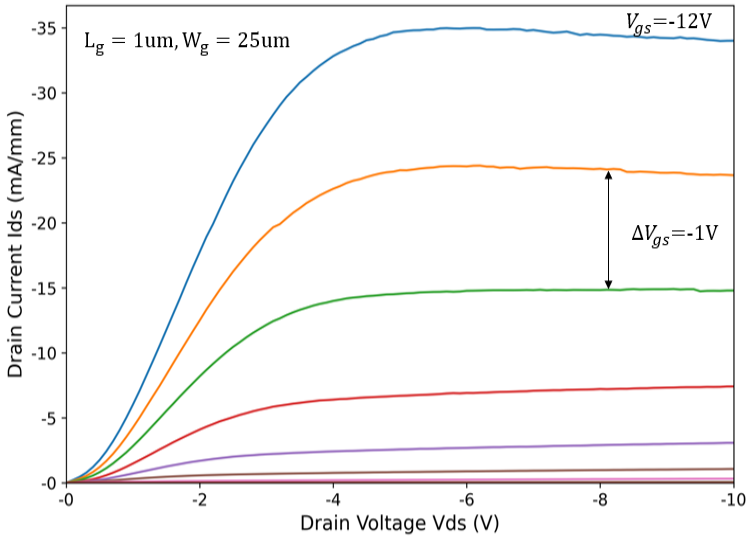

Figure 8.3.2 The output characteristic of a 1μm gate/channel length accumulation channel H-diamond FET.

At low drain bias, the output characteristics exhibit a slight curve at the turn-on region, rather than entering a perfectly linear region as seen in traditional MOSFETs. This non-ideal turn-on region may be attributed to the following reasons. At relatively low gate bias, the 2D hole density has not yet reached a saturated or high level. As a result, the drain current increases slowly with increasing V_{ds}, leading to the non-linear turn on. In addition, the interface traps at the gate dielectric/diamond interface can weaken the ability of the gate to modulate channel carriers [8.3]. The accumulation of channel carriers is not as rapid as the increase in V_{gs}, resulting in a curved turn-on. Meanwhile, since the curved turn-on behaviour is maintained under larger negative gate bias, it is also likely that a potential barrier is formed in the ohmic contact region, which limits carrier injection and contributes to the observed non-linearity.

Following the basic output characteristic measurements, a double-sweep hysteresis test was performed to further evaluate the stability and reliability of the accumulation channel H-diamond MOSFET. By sweeping the gate voltage forward and backwards across the operation range, it can be directly observed that the charge trapping, interface quality, and memory effects in the device. To ensure safe and reliable characterisation, the V_{gs} sweep was applied from the on-state (V_{gs} at -12V) to the off-state (V_{gs} at 0V), then

reversed the sweep direction. In this case, the device turns on in a fully accumulated, highly conductive state and then gradually depletes carriers, minimising the risk of sudden current increase or breakdown. The hysteresis characteristic result is shown in Figure 8.3.3.

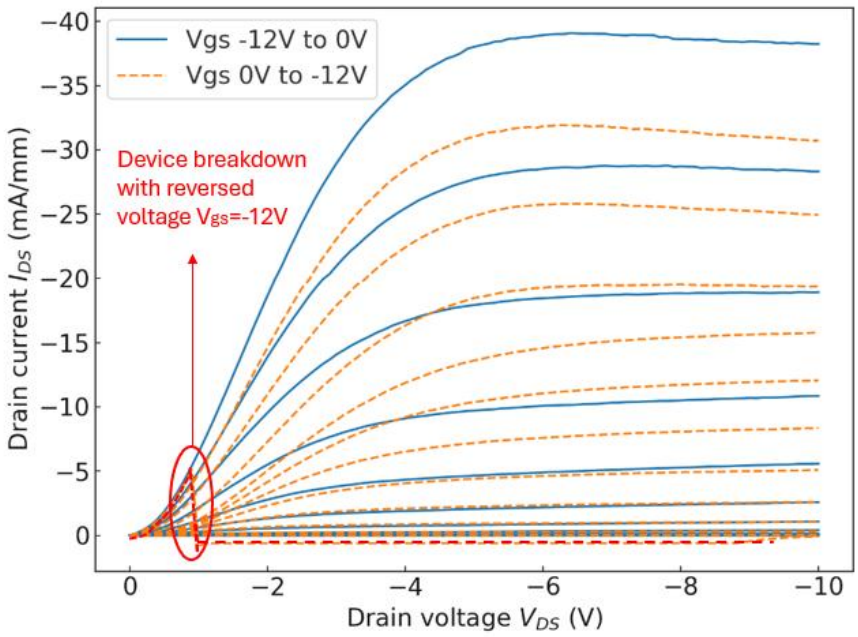

Figure 8.3.3 The hysteresis performance of a 1μm gate/channel length device.

As shown in Figure 8.3.3, the double-sweep output curves exhibit a hysteresis in which the drain current during the reverse sweep (from off-state to on-state) is higher than in the forward sweep. This phenomenon is attributed to the trapping and gradual release of charges at the gate dielectric/diamond interface. When the device is initially biased in the on-state, interface traps can become filled, and these trapped charges are only slowly released as the gate voltage is swept back toward the off-state, resulting in enhanced channel conductivity during the reverse sweep. During the reverse gate voltage sweep, device breakdown was observed when V_{gs} reached its most negative value (V_{gs} at -12V). This suggests that under these conditions, the channel is maximally accumulated, and a large number of carriers released from previously filled traps are present at the interface and within the channel. Consequently, these lead to device breakage.

Transfer characteristic

The transfer characteristic of the accumulation channel H-diamond MOSFET when V_{ds} at -10V is shown in Figure 8.3.4. The drain current increases by more than seven orders of magnitude as V_{gs} sweep from 0V to -12V, indicating the good gate control.

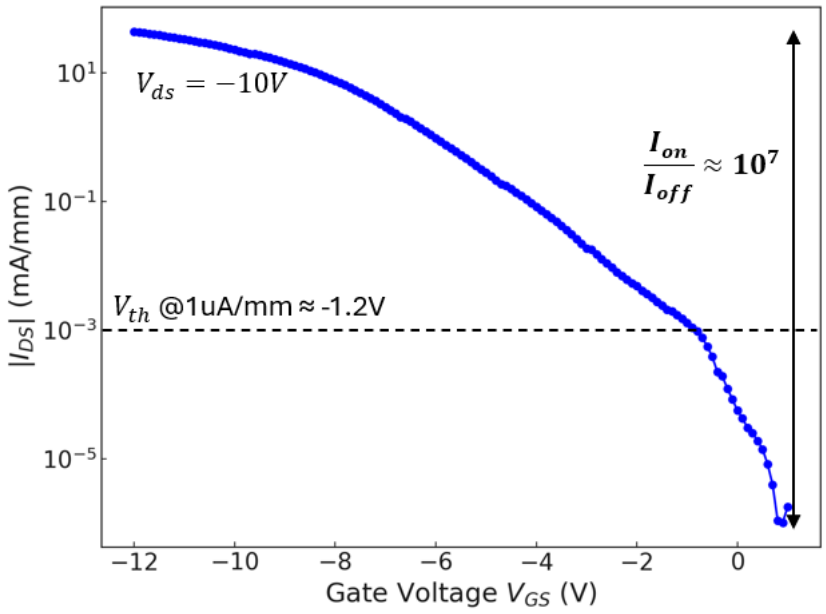

Figure 8.3.4 Transfer characteristic of 1μm gate/channel length accumulation H-diamond FET.

In this work, the threshold voltage (V_{th}) is extracted using a fixed current criterion, defined as the gate voltage at which the normalised drain current reaches 1 μA/mm. For this device, the V_{th} is around -1.2 V, as indicated in Figure 8.3.4.

It should be noted that, although the fixed-current method is less commonly used for conventional inversion-mode MOSFETs, it is intentionally adopted here for the accumulation-mode H-diamond device. In this structure, the channel forms gradually under gate bias rather than through an abrupt inversion process. The selected current level, therefore, defines a practical boundary below which the drain current is dominated by deep subthreshold transport and trap-assisted conduction, rather than by a continuous accumulated channel. Accordingly, the V_{th} extracted using the constant-current method is interpreted as an effective device turn-on voltage, marking the onset of measurable channel conduction from the subthreshold regime.

In addition to the constant-current method, the V_{th} can also be extracted by linear extrapolation at the point of peak transconductance (g_m), which is a widely adopted method for MOSFETs and high-performance FETs. Figure 8.3.5 shows the transfer characteristics with the g_m curve. In this approach, the point of g_m peak is approximately 12 mS/mm from the transconductance curve. As highlighted in Figure 8.3.5, the V_{th} value obtained by the linear extrapolation method is approximately -8V. The V_{th} obtained value by this method reflects the most sensitive range of the device switch under the gate control.

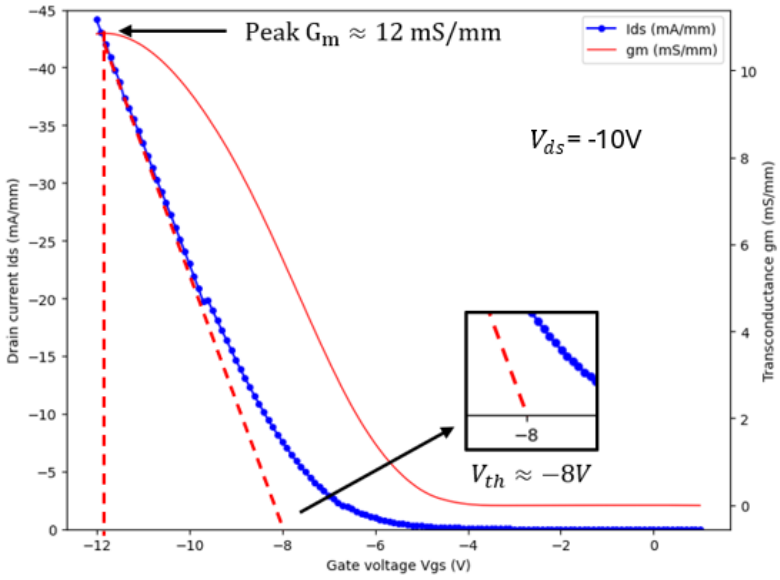

Figure 8.3.5 Transfer characteristics with g_m curve of 1 μm gate/channel length accumulation H-diamond FET.

It should be noted that the threshold voltage values extracted by the constant-current method and by the linear extrapolation at peak g_m can differ significantly. In this device, the constant-current method shows the V_{th}≈−1.2V, which is more relevant to the practical device turn-on. In contrast, the peak-g_m linear extrapolation method yielding $V_{th} \approx -8$V highlights the formation of a strongly accumulated channel rather than the initial turn-on condition. The physical distinction between these two extracted values is now explicitly clarified.

Off-state breakdown and Leakage

The off-state breakdown was measured by fixing the gate voltage (V_{gs}) at zero volts and sweeping the drain bias (V_{ds}) from 0 to -25V, while recording both the drain current (I_{ds}) and the gate current (I_g), as shown in Figure 8.3.6. At lower V_{ds} (0 to -16V), the I_{ds} and I_g relatively remain at the noise floor. As V_{ds} keep decreasing, a clear rise in current is

observed, and both I_{ds} and I_g showed the same growth trend. It indicates that the breakdown is more likely associated with the 15 nm thick ALD Al_2O_3 layer between the gate and ohmic contacts.

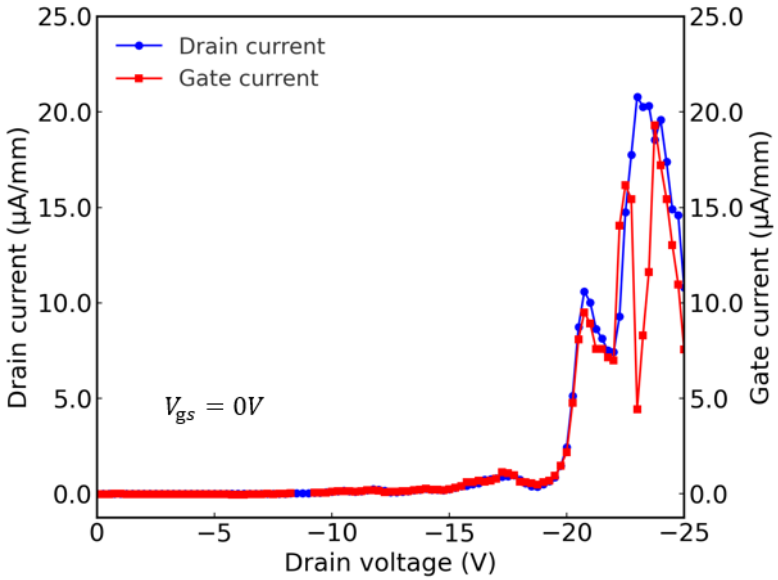

Figure 8.3.6 Off-state breakdown measurement for 1 μm gate/channel length accumulation H-diamond FET.

To characterise the intrinsic gate leakage behaviour of the gate, I_gV_g curve was performed at V_{ds}= 0V. As shown in Figure 8.3.7, the leakage remains low until the V_{gs} reaches -8V, after which it increases steadily. As V_{gs} keeps decreasing, the I_g exhibits a significant increase in μA/mm range, which also suggests the breakdown is associated with the thin dielectric layer under the gate, is the primary leakage path under high negative gate bias.

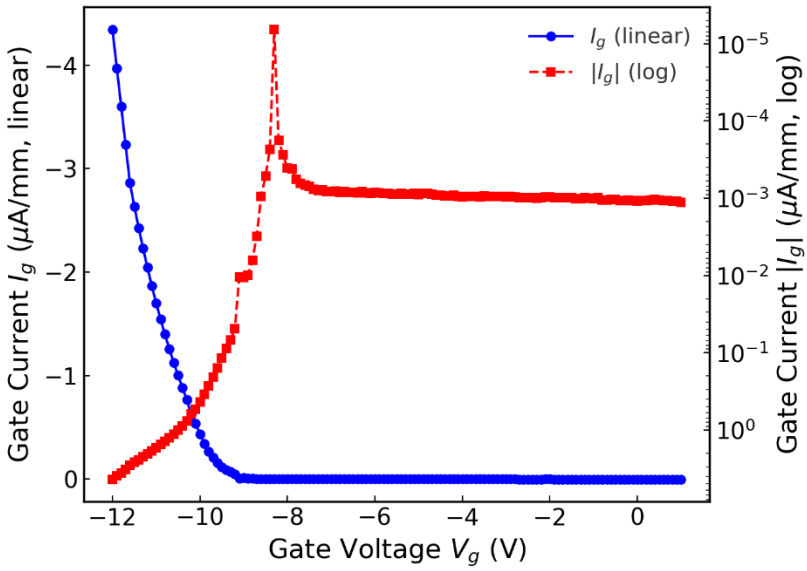

Figure 8.3.7 Off-state gate leakage measurement for 1μm gate/channel length accumulation H-diamond FET.

Based on the reported breakdown field value of thermal ALD Al_2O_3 deposited is approximately 5±0.8 MV/cm [8.4]. The maximum theoretical breakdown voltage for a 15-nm-thick thermal-ALD Al_2O_3 is around 8.7V under the assumption. This calculated value matches quite well with the gate-leakage behaviour. This provides the evidence that the intrinsic breakdown of the 15nm Al_2O_3 layer leads to the leakage and breakdown behaviour under high field. The uniformity of the ALD-grown Al_2O_3 film will also affect the effective breakdown voltage, which may indicate the difference between the theoretical value and the observed breakdown behaviour.

TLM

To evaluate the ohmic contact quality at different stages of device fabrication, TLM measurements were performed both immediately after the ohmic level fabrication, as shown in Figures 8.3.7 and 8.3.8. After the 400 °C annealing (used immediately prior to oxide deposition), the TLM IV curves exhibit nonlinearity over the full voltage range (from -10 V to 10 V). This behaviour contrasts obviously with the pre-annealing measurements, where the contacts demonstrated good linearity over a wide bias range.

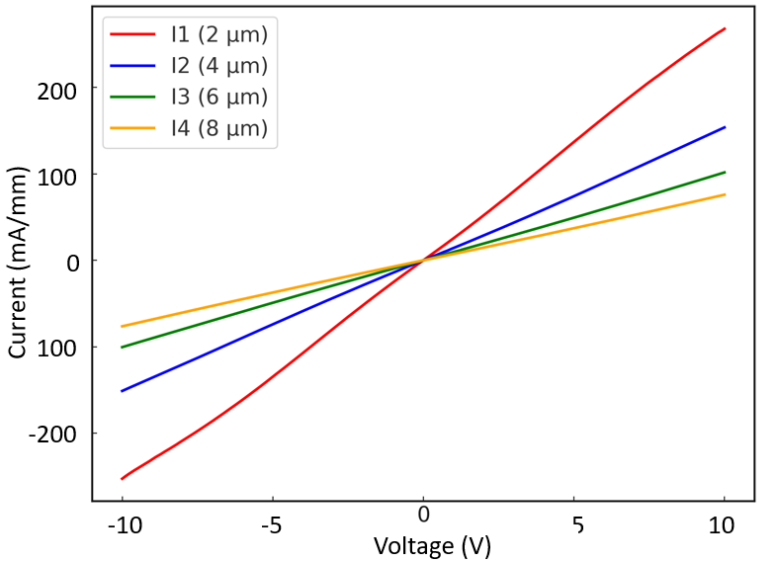

Figure 8.3.7 TLM IV results after ohmic level fabrication with full voltage range (-10V to 10V).

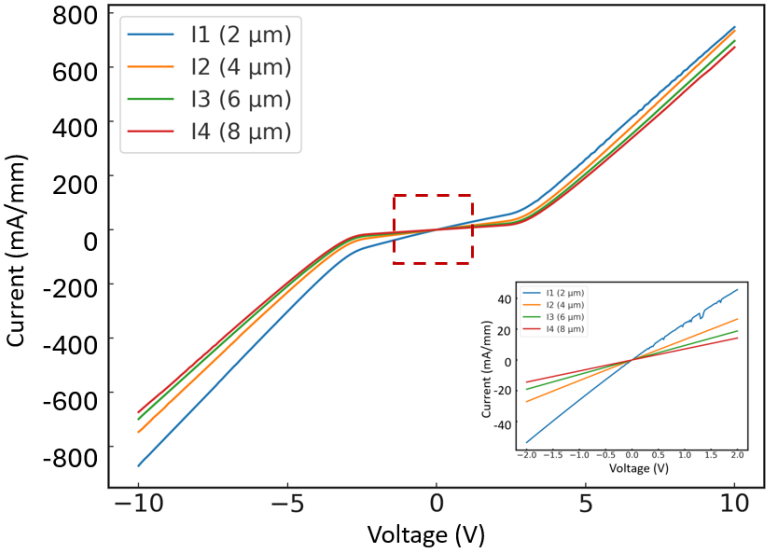

Figure 8.3.8 TLM IV results after whole device fabrication with full voltage range (-10V to 10V) and a zoomed-in region (-2V to 2V).

As shown in Figure 8.3.9, the linear fits to the resistance versus gap size data show the contact resistances (R_c) of 2.21 Ω·mm after ohmic level fabrication ("Before") and 3.95 Ω·mm after the entire device fabrication process ("After"). However, due to the absence of a clearly linear range post-annealing, the post-anneal R_c could only be extracted within a narrow window of −2 V to 2 V as shown in Figure. 8.3.8. However, the extracted R_c values may lack reliability, since the contacts no longer behave as ideal ohmic.

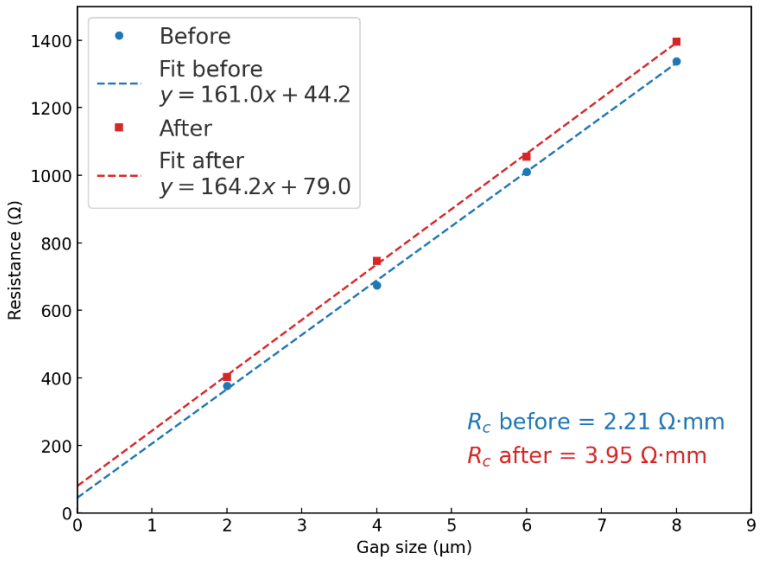

Figure 8.3.9 TLM results after ohmic level and after whole device fabrication.

In addition, as discussed in Section 8.2, there is also a factor from the fabrication process that may affect the ohmic behaviour of the device. After the formation of Au ohmic contacts, an additional Ti/Au bond pad layer was deposited to overlap the ohmic pads, aiming to improve long-term measurement stability. However, the gate oxide deposition was performed after the bond pad step, which required a thermal anneal at 400°C for 1 hour to remove surface adsorbates from the H-terminated diamond. As a result, both the Au ohmic layer and the Ti/Au bond pads were subjected to this high-temperature treatment. This thermal exposure could have induced diffusion or alloy formation between Ti and Au, modifying the original metal–semiconductor interface. Even in the absence of Ti-induced reactions, gold tends to diffuse to release the metal internal stress, leading to the defects [8.5]. In this case, the effective contact area degrades the electrical quality of the interface, resulting in increased contact resistance and nonlinear IV behaviour.

To obtain a more realistic contact resistance, the produced FET devices with different gate/channel lengths were used as equivalent to TLM structures with varying source–drain spacings, given that all devices were fabricated with the same structure and the same process. In principle, this allows the extraction of R_c using the same linear extrapolation method as in the TLM analysis. Specifically, devices with gate lengths of 1, 2, 3, and 5 μm were characterised in the on-state to determine their total on-resistance. The on-resistance for each device was extracted the low-drain-bias, approximately linear region of the output characteristics at V_{ds}= -1V and V_{gs}= -12V, ensuring strong channel accumulation. Based on the output characteristics, the $I_{ds}-V_{ds}$ relationship remains approximately linear around this bias point, prior to the onset of pronounced quasi-

saturation behaviour, and therefore $V_{ds} = -1\text{V}$ is taken as a representative low-field operating condition for $\mathrm{R_{on}}$ extraction.

It should be noted that the sheet resistance R_{sh} may vary slightly across different locations on the sample due to non-uniform hydrogen termination or processing-induced variations. However, it is a common assumption in contact resistance extraction to treat R_{sh} as approximately constant for devices fabricated on the same sample under identical conditions. Under this assumption, the slope of the R_{on} versus gate length relation represents sheet resistance, while the intercept corresponds to the contact resistance. It should be emphasised that the extracted $\mathrm{R_{on}}$ represents an effective low-drain-bias on-resistance suitable for relative comparison and contact resistance extraction, rather than an absolute power-device figure of merit. Figure 8.3.9 shows the extraction of contact resistance at V_{ds}= -1V and V_{gs}= -12V.

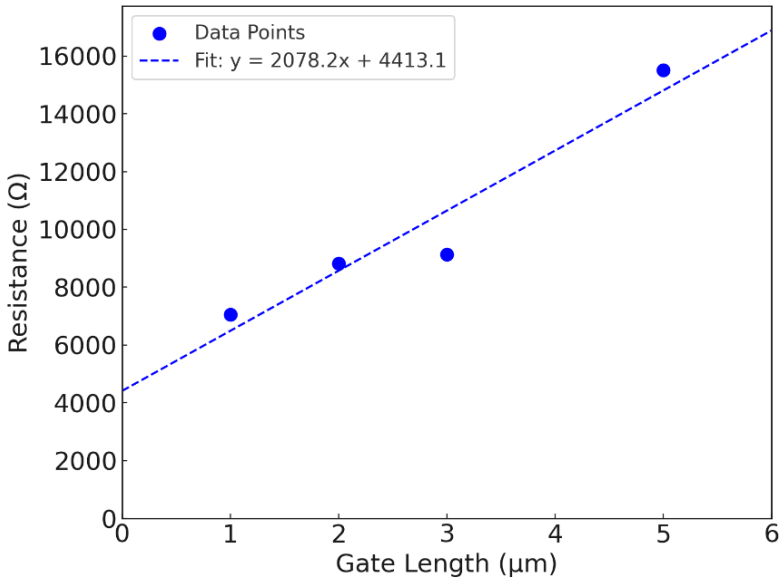

Figure 8.3.10 R_{on} extracted from different gate length devices at V_{ds}= -1V and V_{gs}= -12V.

As shown in Figure 8.3.10, the linear fitting of R_{on} extracted from devices with gate length spacings ranging from 1 μm to 5 μm. The data point at 10 μm shows an abnormally large resistance and deviates significantly from the expected linear trend, which is most likely due to additional parasitic effects and non-uniformities rather than the intrinsic channel scaling. From the slope of the linear fit, the normalised contact resistance is calculated to be large at 55.15 Ω·mm.

Scaling output and transfer characteristics for all gate lengths

In these sections, the electrical characteristics of the accumulation channel H-terminated diamond MOSFETs were analysed using the device with a gate comparison across all fabricated gate lengths, highlighting the impact of lateral scaling on the output and transfer characteristics. Figure 8.3.10 and Figure 8.3.11 show the output characteristic and transfer characteristic for all H-diamond accumulation channel devices with varying gate lengths.

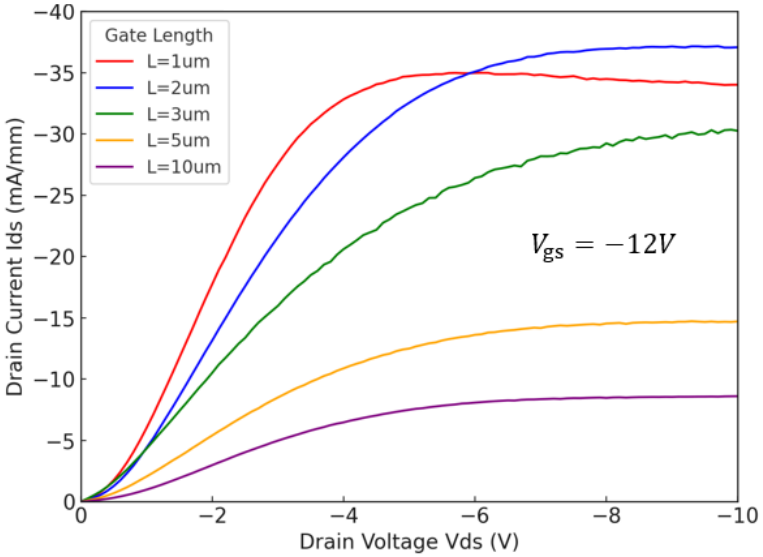

Figure 8.3.10 Max current for all gate length H-diamond accumulation channel devices at V_{gs}= -12V.

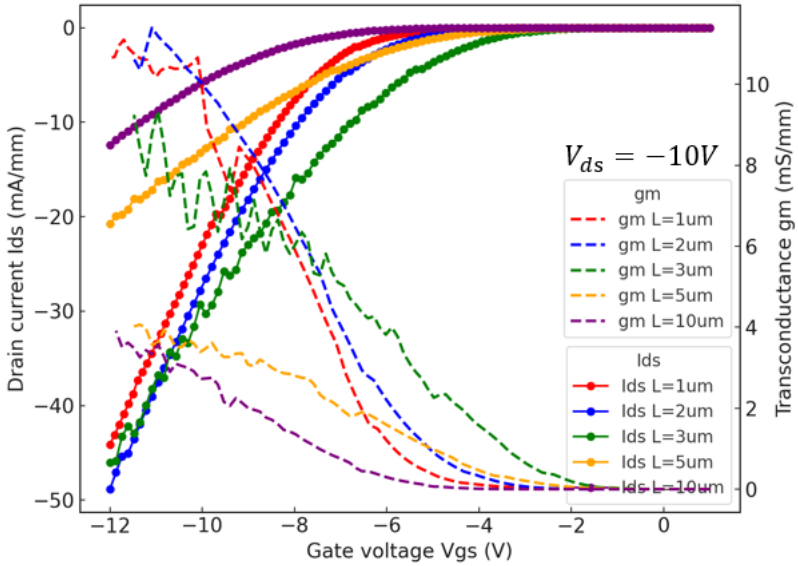

Figure 8.3.11 Transfer curve and transconductance for all gate length H-diamond accumulation channel devices at V_{gs}= -12V.

The saturation drain current extracted from the output characteristic curve at V_{gs}= -12V increases with decreasing gate length, from 8.6 mA/mm at 10 µm to 35 mA/mm at 1 µm. A similar trend is observed for the maximum drain current transfer characteristic curve. In principle, both transfer and output measurements under the same bias conditions should behave as identical current values. However, in practice, this device shows a slight difference, with the transfer curves giving consistently higher drain currents. This discrepancy is attributed to trap-related effects, during the transfer measurement at fixed V_{ds} = –10 V, as V_{gs} is swept from 0 V to –12 V, surface or interface traps at the hydrogen-terminated diamond can be gradually filled, thereby effectively enhancing the channel charge density. In contrast, the output characteristics measured at fixed V_{gs} = –12 V do not involve such a progressive trap filling process, leading to a slightly lower extracted saturation current.

In the output characteristics, the 1 µm device exhibits a slight reduction in drain current compared to the expected scaling trend, which is combined with a lower knee voltage. Here, the knee voltage is defined as the V_{ds} at which the output characteristic departs from the linear region and begins to exhibit current saturation. If the drain current in this device could continue to increase with V_{ds} over a broader range before reaching saturation, its scaling behaviour would align more closely with the proportional trend observed for the 2–10 µm devices. Under the present conditions, only the longer-channel devices (2–10 µm) exhibit more linear scaling of the drain current.

The onset of current saturation at lower V_{ds} in the 1 µm device can be attributed to several factors. The high lateral electric field in the short channel induces velocity saturation of the hole carriers at lower drain bias. This velocity saturation is often described as an effective mobility degradation, since the carrier velocity no longer increases linearly with the applied field. As a consequence, the drain current increase is limited and the transition to saturation occurs earlier.

From the transfer characteristics, the threshold voltage and the transconductance were extracted for each gate length. As expected from channel length scaling, g_m shows a clear upward trend as L_g is reduced, reflecting enhanced gate control and reduced channel resistance. The threshold voltage values, on the other hand, exhibit only partial scaling behaviour between 10 µm, 5 µm, and 3 µm channel lengths, and a negative shift is observed. However, the 1–2 µm devices deviate from this trend. Such deviation is most likely associated with the increasing influence of parasitic resistances, combined with high-field effects such as velocity saturation. The corresponding V_{th} values for all

gate lengths are reported in the summary table at the end of this chapter (Table 8.4.1), which provides a complete overview of the extracted parameters.

In the output characteristics, the $L_g = 1$ μm device exhibits a slight reduction in drain current after the onset of saturation, deviating from the monotonic scaling trend observed in the longer-channel devices. This behaviour is accompanied by a reduced knee voltage, defined as the drain voltage at which the output characteristic departs from the linear region and enters saturation.

This current reduction at high | V_{ds} | is attributed to short-channel effects under strong lateral electric fields. In the 1 μm device, the high drain bias leads to significant drain-induced depletion extending towards the source, effectively reducing the gate-controlled channel length. In accumulation-mode H-diamond FETs, this results in partial depletion of the accumulated hole channel near the source region, weakening channel continuity rather than sustaining a constant saturation current.

In addition, velocity saturation and field-induced mobility degradation become more pronounced in the short-channel device, further limiting the drain current at high | V_{ds} |. Self-heating effects at high power density may also contribute secondarily to the observed current reduction. For the $L_g = 2$ μm device, similar mechanisms are expected to occur at higher drain voltages; however, within the measured bias range, the effective channel length remains sufficient to suppress a pronounced current roll-off.

8.4 Split CV and mobility extraction

Following the analysis of the DC measurement results, this section focuses on investigating the device characteristics using split CV measurements. The capacitance–gate voltage response is discussed, after which the influence of parasitic capacitance is removed to accurately extract the variations of hole density and sheet resistance as a function of gate voltage. These parameters are then used to estimate the dynamic behaviour of the carrier mobility. Finally, based on the extracted mobility and resistance values, both the transconductance and the intrinsic transconductance are analysed, providing a more comprehensive understanding of the device operation and performance limitations.

Split CV

In this section, the CV measurement was carried out with the gate voltage (V_{gs}) first swept from −10V to +2V (forward sweep) and then reversed to −10V to record the hysteresis effects. In practical devices, the measured gate capacitance is not simply determined by

the intrinsic channel capacitance (C_{gc}), which scales with the gate area. In addition, it also includes many parasitic capacitance contributions that are largely independent of gate length, such as the gate–source overlap capacitance (C_{gs1}), the gate–drain overlap capacitance (C_{gd1}). Figure 8.4.1 illustrates the distribution of both intrinsic and parasitic capacitances in the studied device structure. While these parasitic capacitances constitute only a minor ratio in long-gate devices, their relative contribution becomes significant as the gate length decreases, since the intrinsic capacitance shrinks proportionally with the gated area. This results in an apparent accumulation capacitance that deviates from the actual channel capacitance, thereby introducing errors in the extraction of sheet carrier density and mobility if left uncorrected.

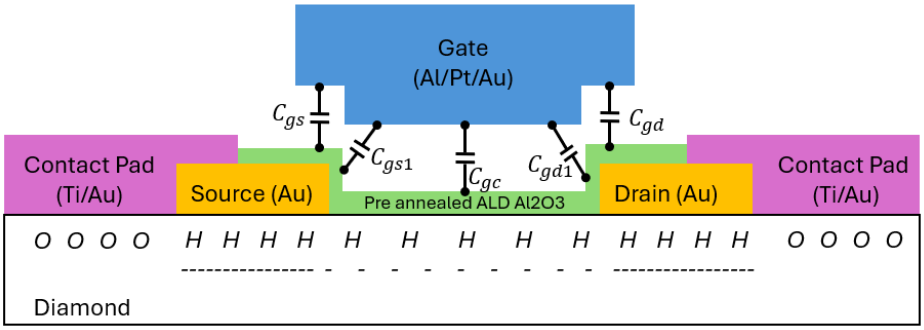

Figure 8.4.1 The distribution of gate capacitance in the accumulation channel H-diamond FET.

As shown in Figure 8.4.2, the CV characteristics measured at 1 MHz are presented for devices with different gate lengths. It can be observed that the apparent accumulation capacitance increases as the gate length decreases. However, the 2 μm device exhibits an accumulation capacitance of approximately 5×10^{-12} F, which is significantly larger than that of the 3–10 μm devices (on the order of 10^{-13} F) and deviates from the expected gate-length dependence.

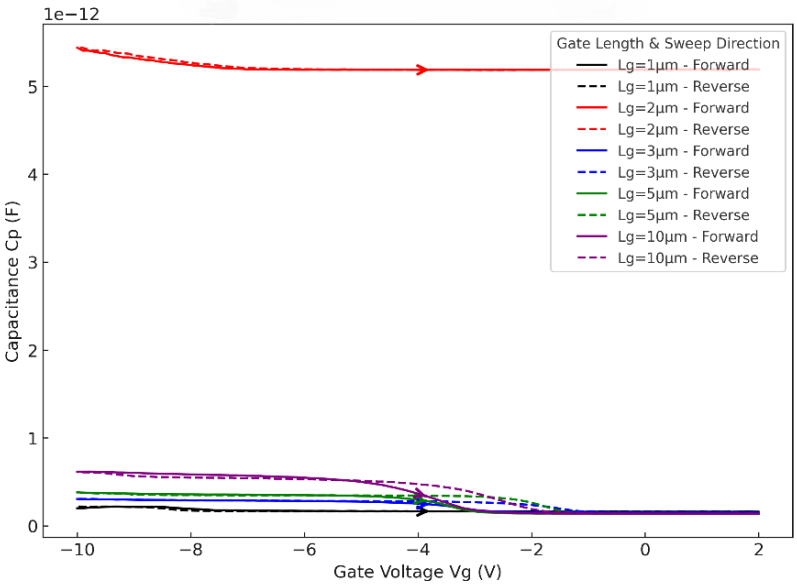

Figure 8.4.2 The CV characteristics measured at 1 MHz for different gate length accumulation channel H-diamond FETs.

Although the 2 μm device exhibits an obvious difference in the C–V measurement, its DC characteristics remain well-behaved and comparable to the other gate length devices. This indicates that the deviation does not originate from the intrinsic channel conduction, but rather from parasitic effects specific to the high-frequency capacitance measurement. In particular, the relatively small intrinsic gate capacitance of the 2 μm device makes the measurement more sensitive to the parasitic capacitances, which have a negligible impact under DC bias conditions but can dominate the AC response. For this reason, the 2 μm C–V data were excluded from the parasitic extraction, while its DC performance was still considered valid. The CV characteristics measured at 1 MHz for the other gate lengths are shown in Figure 8.4.3.

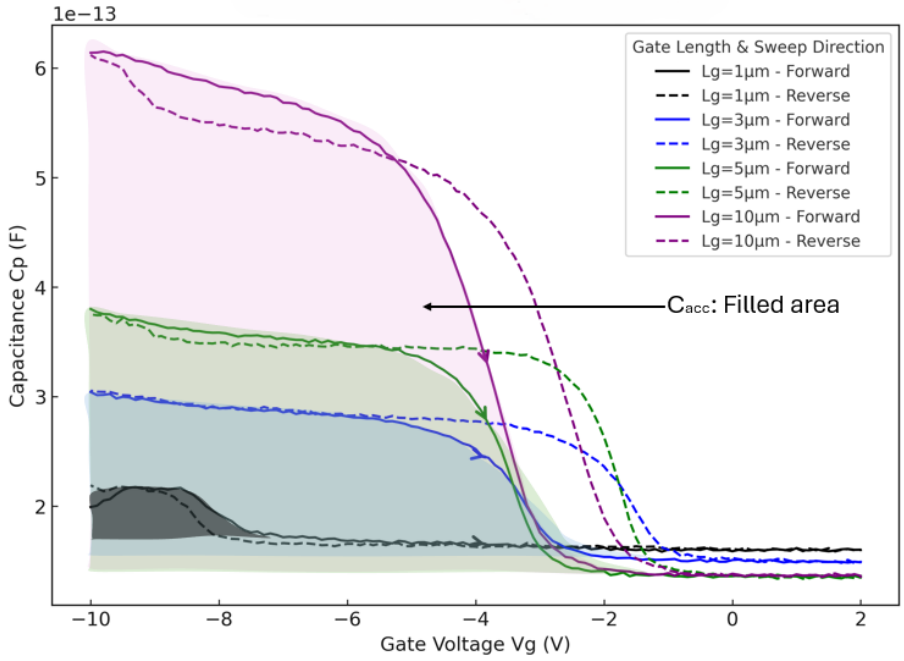

Figure 8.4.3 The CV characteristics measured at 1 MHz for different gate length accumulation channel H-diamond FETs, 2 μm device removed.

As shown in Figure 8.4.3, the CV characteristics at 1 MHz are presented for devices with gate lengths ranging from 1 μm to 10 μm (excluding the 2 μm device). In the accumulation region, the capacitance increases with gate length, consistent with the expected proportionality of capacitance to gate area. At the same time, the hysteresis between forward and reverse sweeps exhibits clear gate-length dependence: the 1 μm device shows nearly overlapping curves with minimal hysteresis, whereas the 3–10 μm devices display more pronounced deviations, indicating that interface charge trapping and release processes become more evident in longer-channel devices. By contrast, the 10 μm device exhibits a minor influence from parasitic capacitances and demonstrates a stable accumulation capacitance.

To quantitatively separate the intrinsic channel capacitance from the parasitic contributions, the accumulation capacitance (C_{acc}) of devices with different gate lengths (L_g) was analysed. Here, each C_{acc} data point was extracted from the CV characteristics where the capacitance values were in the strong accumulation region, and each parasitic capacitance (C_{par}) was extracted from the floor region. Figure 8.4.4 shows that C_{acc} increases approximately linearly with L_g, which is expected since the effective channel area scales proportionally with the gate length.

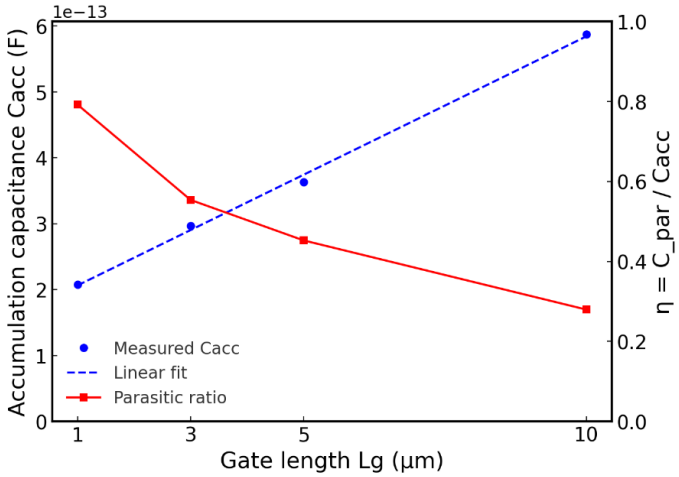

Figure 8.4.4 Gate-Length scaling of accumulation capacitance and parasitic fraction.

To further evaluate the influence of parasitic capacitance, the parasitic ratio (η) can be defined as

$$\eta = \frac{C_{par}}{C_{acc}} \tag{8-1}$$

as also shown in Figure 8.4.4 (red curve). The results indicate that η increases as the gate length decreases, highlighting that shorter gate length devices suffer from a stronger parasitic contribution (parasitic ratio=0.8). In contrast, devices with longer gate (L_g=10μm) exhibit the smallest parasitic ratio (0.28), making them more suitable candidates for subsequent carrier density and mobility extraction. Figure 8.4.5 shows the CV characteristics measured at different frequencies for a 10 μm gate length accumulation channel H-diamond device.

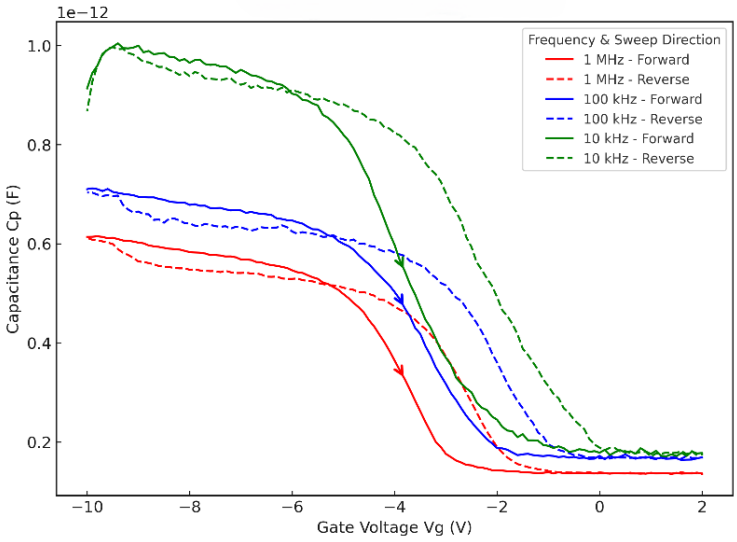

Figure 8.4.5 The CV characteristics measured at different frequencies for a 10μm gate length accumulation channel H-diamond FETs

As shown in Figure 8.4.5, CV measurements were performed at 10 kHz, 100 kHz, and 1 MHz. The accumulation of capacitance progressively decreases from 10 kHz to 1 MHz, and the hysteresis between forward and reverse sweeps becomes less pronounced. At low frequency (10 kHz), the accumulation capacitance is significantly elevated and exhibits a large hysteresis, indicating that the slow interface and the traps can respond to the sweeping bias and contribute additional measurable capacitance. At 100 kHz, this effect is partially suppressed. At high frequency (1 MHz), however, the slow traps are essentially "frozen," resulting in the lowest accumulation capacitance, minimal hysteresis, and a value approaching the theoretical oxide capacitance. The clear and distinct transition region observed at 1 MHz, along with the consistency with the expected oxide capacitance values, confirms that only intrinsic channel carriers can respond at this frequency, and even rapid interface states cannot follow the AC signal. In contrast, at 100 kHz and 10 kHz, the transition region is broader and shifts toward more negative gate bias, with an increase in accumulation capacitance, reflecting the contribution of traps and interface states that can respond under lower-frequency modulation. Therefore, in this study, the 1 MHz data of 10 μm gate length are used for the extraction of hole density and mobility.

In theory, the capacitance from the gate oxide layer can be calculated in the following equation,

$$C_{ox} = \frac{\varepsilon_0 \varepsilon_{ox} A}{t_{ox}} \tag{8-1}$$

Where the ε_0 is 8.854 × 10^{-12} F/m, A is the parasitic overlap area (50μm^2), t_{ox} is the thickness of the oxide (15nm). As shown in Figure 8.3.14, the average parasitic capacitance at the floor is 1.71 x 10^{-13} F. Hence, a dielectric constant around 5.8 was calculated using equation 8-1. The typical dielectric constant of ALD Al_2O_3 is reported between 7 to 9. However, the dielectric constant is reported to decrease as the thickness of the Al_2O_3 film decreases and is also affected by growth temperature. Hence, the dielectric constant of Al_2O_3 may be as low as 5.9, which is close to this result [8.6].

Mobility Extraction

As discussed above, the measured gate capacitance consists of both the effective channel capacitance and parasitic capacitances. By subtracting the parasitic contribution, the intrinsic channel capacitance can be obtained as

$$C_{eff} = C_g - C_{parasitic} \tag{8-2}$$

By integrating the area between the effective capacitance and the charge density (Q_i) can be determined as:

$$Q_i = \int C_{eff} d(V_{gs}) \tag{8-3}$$

The corresponding 2D hole density is then given by:

$$p_s = \frac{Q_i}{q} \tag{8-4}$$

The sheet resistance (R_{sh}) was extracted from the measured transfer characteristic at a fixed V_{ds} chosen within the linear operation region (V_{ds}=-1V). By extracting the turn-on resistance and the contact resistance, the channel resistance can be obtained according to

$$R_{ch} = R_{on} - 2R_c \tag{8-5}$$

The contact resistance was calculated from the TLM measurements, which is 55.15 Ω·mm. Subsequently, the sheet resistance is calculated using

$$R_{sh} = \frac{R_{ch}}{W \times L} \tag{8-6}$$

where W and L expressed the channel length and width, respectively. Figure 8.4.6 shows the relationship between the extracted 2D hole density and sheet resistance with V_{gs}.

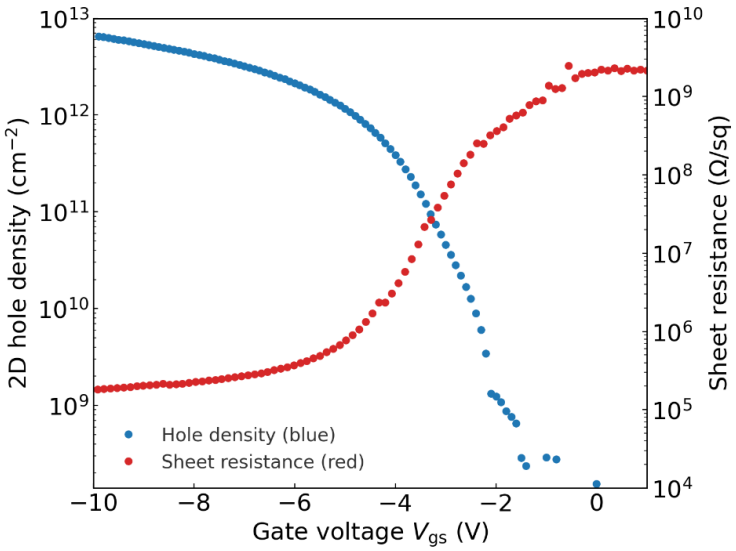

Figure 8.4.6 Accumulation Channel 2D hole density and sheet resistance versus V_{gs} for 10 μm gate/channel length accumulation channel H-diamond FETs.

At V_{gs} is 0V, the device is in the off-state, and the hole density is effectively 0 (less than 10^9cm^{-2}). The sheet resistance exceeding 10^{10} Ω/□ indicates the depletion of the 2DHG.

As the gate bias is swept to more negative values, holes were gradually accumulated at the channel under the gate control, leading to a rapid increase in 2D hole density and a corresponding decrease in sheet resistance. When V_{gs} = -10V, the hole density is approaching 6.5 x 10^{12} cm^{-2}. At the same time, the R_{sh} decreased to 10^5 Ω/□, recovering the conductive behaviour characteristic of the H-diamond surface before 2DHG suppression. This trend demonstrates the effective modulation of the 2DHG in accumulation channel H-diamond MOSFETs. With the calculated carrier density, the effective carrier mobility can be deduced using the following equation:

$$\mu_{eff} = \frac{1}{n \cdot q \cdot R_{sh}} \tag{8-7}$$

Figure 8.4.7 shows the carrier mobility versus V_{gs} for a 10 μm gate/channel length device.

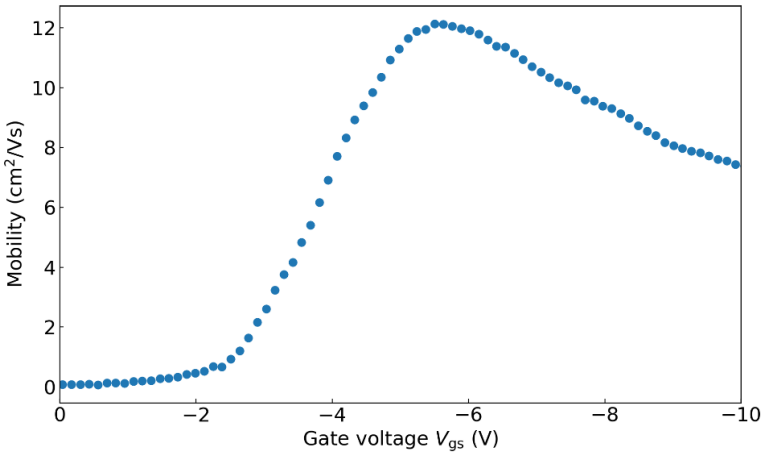

Figure 8.4.7 Accumulation Channel carrier mobility versus V_{gs} for 10 μm gate/channel length device.

It should be noted that contact resistance does not intrinsically degrade the channel mobility, as mobility is governed by carrier transport and scattering mechanisms within the gated channel. However, a large contact resistance can lead to an underestimation of mobility if it is extracted directly from extrinsic I–V characteristics, because the effective channel bias and the measured transconductance are reduced. In this work, the contact resistance is explicitly de-embedded based on TLM analysis, and the mobility is extracted using split C–V-derived carrier density together with corrected channel resistance. Therefore, the mobility shown in Fig. 8.4.7 predominantly reflects intrinsic channel transport rather than contact-limited effects.

The extracted mobility with gate bias exhibits a characteristic that reflects the progress of the 2DHG density and scattering mechanisms. At low V_{gs} region (V_{gs} <-2V), the 2DHG is strongly suppressed, resulting in extremely low carrier density and maximum sheet

resistance. Under these conditions, the channel is not formed, and the extracted mobility is nearly zero and does not represent intrinsic carrier transport mechanisms. As V_{gs} becomes more negative, the 2DHG density increases, the channel is formed, and the sheet resistance decreases rapidly. Therefore, the mobility is increasing and reach 12cm^2/V·s as the V_{gs} being more negative. However, with further negative bias (over -6V), the stronger perpendicular electric field confines the 2DHG closer to the interface, which enhances interface scattering. As a result, the mobility decreases gradually to approximately 7−8cm^2/(V·s).

In this study, the peak channel mobility is only about 12 cm^2/(V·s), which is significantly lower than the commonly reported values of 50-100 cm^2/(V·s) for H-diamond. This reduction can be attributed to the interfacial conditions. A vacuum annealing was performed at 400℃ for 1 h to effectively remove air adsorbates, thereby suppressing the transfer doping mechanism. While this treatment reduces Coulomb scattering from adsorbates, it also decreases the intrinsic 2DHG density, requiring more negative gate bias to re-establish conduction. Subsequent deposition of ALD Al_2O_3 further suppresses the 2DHG by preventing the reformation of surface acceptor layers, while its fixed charges and interface states. In addition, the high-k dielectric contributes to the phonon scattering. At more negative bias, the perpendicular electric field pushes the 2DHG closer to the Al_2O_3/diamond interface, enhancing phonon scattering. In this case, the vacuum annealing and oxide capping cooperatively reduce the initial hole density and enhance interface-related scattering, thereby explaining why the measured channel mobility in this work is lower than the values typically observed in H-terminated diamond.

Transconductance

The transconductance g_m is a key parameter that characterises the gate controllability of a field-effect transistor. The transconductance provides a more sensitive investigation of variations in interface charge, effective gate capacitance, and carrier mobility, making it useful for evaluating the impact of oxide thickness, contact resistance, and interfacial scattering on device performance. In this section, a detailed analysis of both extrinsic and intrinsic transconductance is presented, complemented by split CV and extracted mobility data.

The extrinsic transconductance g_m was directly extracted from the I_dV_{gs} curves. However, the extrinsic g_m includes the influence of parasitic source resistance. These resistances reduce the effective voltage applied to the channel, leading to an underestimation of the intrinsic channel modulation efficiency. As introduced above, the contact resistance was extracted from the linear fitting of R_{on} with different gate/channel

lengths. Based on the extracted R_c, the intrinsic transconductance g_m^* can be calculated with the following equation:

$$\text{Intrinsic transconductance, } g_m^* = \frac{g_m}{1 - g_m R_c} \tag{8-8}$$

Extrinsic and intrinsic transconductance curves (g_m & g_m^* vs V_{gs} at V_{ds}=-10V) are plotted for comparison in Figure 8.4.8. The intrinsic transconductance (g_m^*) reaches a peak value of approximately 34.2 mS/mm at V_{gs} =-12 V, whereas the extrinsic transconductance (g_m) exhibits a much lower maximum of about 12 mS/mm, with the two curves diverging significantly in the strong accumulation regime and gradually decreasing toward zero near V_{gs}= -6V.

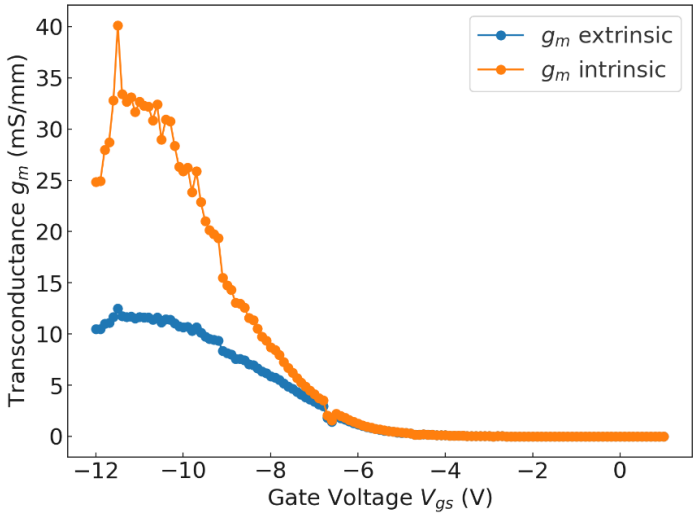

Figure 8.4.8 Extrinsic transconductance (g_m) & Intrinsic transconductance (g_m^*) extracted from 1 μm gate/channel length accumulation channel H-diamond FET.

This large discrepancy indicates that the extrinsic g_m is strongly suppressed by contact resistance. As discussed in section 8.3, the contact resistance is significantly higher due to fabrication-related issues. Hence, the intrinsic g_m^* is over three times of the extrinsic g_m.

For comparison, the accumulation-channel devices with a gate length of 1 μm and a thicker oxide layer of 50 nm, previously reported by the ASMaD group, exhibited the extrinsic g_m of 25 mS/mm and an intrinsic g_m^* of 35 mS/mm. Ideally, with the oxide thickness reduced to 15 nm in the present devices, a proportional increase in the gate capacitance would lead to three times increase in the intrinsic transconductance g_m^*. In practice, however, although the correction for contact resistance raises intrinsic g_m^* by approximately three times, the resulting intrinsic g_m^* was only similar compared to the transconductance of the devices that the ASMaD group previously published, and it was

not three times as much. This is because the intrinsic g_m^* depends on both the gate capacitance and the carrier transfer properties, hence, it is limited by velocity saturation, interface scattering, and the effective capacitance.

To provide a clear comparison of the device performance at different gate lengths, the key electrical parameters have been summarised in Table 8.4.1. The table includes the maximum drain current ($I_{d,max}$), gate leakage current (I_g), transconductance (g_m), intrinsic transconductance (g_m^*), on-resistance (R_{on}), on/off current ratio (I_{on}/I_{off}), threshold voltage (V_{th}), and the maximum capacitance ($Cap_{,max}$). This summary highlights the trends of the accumulation-channel H-diamond MOSFET.

Gate length (μm)	1	2	3	5	10
$I_{d,max}$ (mA/mm)	35.1	37.2	30.3	14.7	8.6
$I_{g\ leakage}$ (μA/mm)	4.3	0.6	3.1	4.3	3.9
Peak g_m^* (mS/mm)	12.5	10.6	9.5	4.1	3.9
Intrinsic g_m (mS/mm)	34.2	25.5	19.9	5.3	4.9
R_{on} (kΩ)	7.1	8.8	9.1	15.5	43.4
I_{on}/I_{off}	10^7	10^{10}	10^5	10^5	10^5
V_{th} (V)	-8	-7.6	-7	-6	-8.2
$Cap_{,max}$ (F)	2.19×10^{-13}	5.4×10^{-12}	3.05×10^{-13}	3.8×10^{-13}	6.15×10^{-13}

Table 8.4.1 Summary of key performances of accumulation-channel H-diamond MOSFETs with different gate lengths.

As summarised in Table 8.4.1, the device performance parameters exhibit the scaling trends with gate length but also some deviations. The maximum drain current ($I_{d,max}$) generally increases as L_g is reduced, consistent with enhanced gate control and reduced channel resistance, but the values for the 1–2 μm devices are significantly higher than expected from linear scaling. This deviation may be associated with increased parasitic resistance and non-uniformities in the longer-channel devices, which limit the achievable current. The leakage current (I_g) also varies non-monotonically, with the lowest value obtained for the 2 μm device. Since gate leakage is strongly influenced by local oxide thickness variations, interface traps, and processing defects, device-to-device variation is more pronounced here. These variations also affect the extracted I_{on}/I_{off} ratio, explaining the exceptionally high value of 10^{10} for the 2 μm channel device. Similarly, the threshold voltage does not follow a perfectly monotonic trend, which can be attributed to geometric variation in interface state density and trap occupation across different devices.

Overall, while the main scaling trends are consistent with short-channel behaviour, the observed inconsistency with highlight the strong sensitivity of H-diamond MOSFETs to interface and process variations.

8.5 Summary

In this chapter, the accumulation-channel H-diamond MOSFETs were investigated, from device fabrication to electrical characterisation. Through an in-situ 400℃ anneal for 1h under vacuum to remove the majority of the air adsorbates on H-diamond prior to 15 nm ALD Al_2O_3 layer deposition.

The maximum drain current of 35 mA/mm was extracted with a channel length of 1 μm and a width of 25 μm. The threshold voltage was approximately -1.5V, taken at a drain current of 1 μA/mm and the transconductance is around 12 mS/mm. The I_{on}/I_{off} ratio exceeding 10^7 was extracted from the transfer characteristics.

Using split CV measurements, the carrier concentration and mobility were extracted as 6.5 x 10^{12} cm^{-2} and 12 $cm^2/V{\cdot}s$, respectively. The effective gate capacitance was found to be strongly limited by interface traps and parasitic capacitance, particularly in short-channel devices where parasitic effects dominate. These results explain the relatively lower intrinsic transconductance of the present devices, despite employing a thinner 15 nm Al_2O_3 gate dielectric compared to previous accumulation channel devices produced in the group using a 50 nm thick Al_2O_3 oxide.

Overall, the analysis demonstrates that both extrinsic and intrinsic transconductance are limited by different mechanisms: extrinsic transconductance is strongly suppressed by high contact resistance, while intrinsic transconductance is constrained by interface scattering and the reduced effective capacitance. Future improvements in ohmic contact fabrication, interface quality, and dielectric thickness represent promising directions for enhancing accumulation channel H-diamond MOSFET performance.

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9. Conclusions and Future Work

9.1 Conclusions

Diamond has long been known as a material with attractive electronic properties, including its ultra-wide bandgap high thermal conductivity, large breakdown electric field. These characteristics make diamond promising for next-generation high-power, high-frequency, and high-temperature electronics. In particular, hydrogen-terminated diamond enables the formation of a two-dimensional hole gas (2DHG) at the surface, offering a unique platform for field-effect transistor (FET) applications. In this work, the primary motivation for diamond research is to explore the performance of diamond-based FETs. To achieve this, a series of studies have been carried out, including surface termination, transfer doping oxide, ohmic contact and the MOSFETs characterisation, with a strong emphasis on developing stable and reproducible fabrication processes suitable for device integration.

In Chapter 6, the significance of surface terminations for diamond electronics was first established. Terminations that induce negative electron affinity (NEA), such as hydrogen, enable stable hole accumulation, whereas other terminations that lead to positive electron affinity (PEA), including oxygen and fluorine, exhibit no surface conductivity. On this basis, further investigations were carried out on hydrogen-terminated diamond to explore transfer doping effects introduced by oxide layers. It was shown that Ebeam and ALD Al_2O_3 with in-situ pre-anneal can suppress the 2DHG associated with the removal of air adsorbates, whereas ALD HfO_2 enhances conductivity. Hence, it demonstrates that oxide deposition can effectively tune the interfacial electronic properties of H-diamond.

The focus of Chapter 7 is placed on the challenge of achieving reliable ohmic contacts on hydrogen-terminated diamond, which is a critical requirement for reducing contact resistance and enabling high-performance devices. Comparisons were made between as-deposited metal contacts and carbide-formation approaches. High work function metals such as Au and Pd exhibited ohmic behaviour in their as-deposited state, however, their poor adhesion to the H-diamond surface makes the formation of stable contacts challenging. Within the scope of this work, Au was shown to form low-resistance and reproducible ohmic contacts on hydrogen-terminated diamond without requiring aggressive post-deposition treatments, demonstrating its viability as a contact metal for H-diamond devices.

In contrast, metal-carbide formation on H-diamond provides alternative methods for reliable ohmic contact with low contact resistance by high-temperature annealing process. In addition, a useful finding in this research is ALD Al_2O_3 can be used as a protective capping layer to reduce the damage of hydrogen-termination during the high-temperature annealing process. By optimising this approach, the contact resistance of TiC was achieved as low as 6.5 Ω·mm. Together, these results highlight both Au-based contacts and carbide formation as viable and complementary strategies for achieving efficient and stable ohmic contacts on H-diamond.

In Chapter 8, the most important results of this research are presented: the fabrication and characterisation of normally-off, accumulation-channel, enhancement-mode hydrogen-terminated diamond MOSFETs. Devices with varying gate length of 1 µm, 2 µm, 3 µm, 5 µm, and 10 µm with fixed gate width of 25 µm, and a 15 nm thermal ALD Al_2O_3 gate dielectric were successfully fabricated. By employing in-situ annealing (400 °C for 1 hour) prior to Al_2O_3 deposition, the 1µm gate length FET accomplish a maximum drain current of 35 mA/mm, a threshold voltage of –1.5 V, a transconductance of 12 mS/mm, and an I_{on}/I_{off} ratio exceeding 10^7. Split C–V analysis extracted a carrier concentration of 6.5 × 10^{12} cm^{-2} and a mobility of 12 $cm^2/(V·s)$. These results demonstrate that the combination of oxide engineering and the Au-based ohmic contact fabrication process enables stable enhancement-mode operation in hydrogen-terminated diamond MOSFETs, providing a scalable platform for future diamond electronic devices.

9.2 Future work

Building on the studies in this work, several directions for further research can be identified. For the investigation of novel diamond surface terminations, although different methods were employed to evaluate surface conductivity, further techniques are required to clarify the electron affinity and thermal stability of these terminations. In particular, advanced spectroscopic and microscopic characterisation methods such as Raman spectroscopy, XPS, and TEM can be applied to identify the influence of sp^2 carbon, interface dipoles, and defect states on 2DHG formation. In addition, oxide-induced transfer doping remains a promising route for interface engineering. Beyond the pre-annealing process of oxide deposition temperature studied here, the choice of ALD precursors and alternative oxide materials is also worth comparing with e-beam evaporation, such as e-beam HfO_2. It deserves further investigation to gain a deeper understanding of the transfer doping mechanisms on H-diamond surfaces.

Regarding the ohmic contact study on H-diamond, the lowest contact resistance of TiC achieved in this work was 6.5 Ω·mm. However, this result was obtained through a two-step annealing process (vacuum anneal followed by RTA). It would be valuable to investigate whether a single-step RTA anneal process, combined with an ALD Al_2O_3 protective layer, could achieve comparable results, as the Al_2O_3 capping has been shown to mitigate hydrogen-termination damage during high-temperature annealing. In addition, other carbide-forming metals, such as tantalum, represent promising candidates for achieving low-resistance and thermally stable contacts. To advance this field further, detailed interfacial studies using cross-sectional TEM and related techniques will be essential to confirm carbide formation directly and to correlate the microstructural evolution with electrical behaviour.

For the accumulation-channel H-diamond MOSFETs investigated in Chapter 8, further improvements are needed to address the performance limitations identified in this work. A key priority is to reduce the high contact resistance, which strongly suppresses the extrinsic transconductance. Future work should therefore explore the integration of optimised carbide-based ohmic contacts, as developed in Chapter 7, into the MOSFET process flow. The intrinsic transconductance was also shown to be limited by interface scattering and reduced effective capacitance, pointing to the importance of improving the oxide/diamond interface. Possible approaches include the use of higher-permittivity dielectric materials, interface passivation layers, or optimised ALD processes to lower interface defect densities. Scaling the gate length below 1 µm would further allow the evaluation of short-channel effects and the high-frequency capability of these devices. Beyond room-temperature operation, it will also be significant to extend device characterisation across a wider temperature range. Reliability testing under high temperature will be essential for assessing suitability in high-power and high-temperature environments. Cryogenic measurements could provide additional insight into carrier transfer mechanisms. Moreover, pulsed I–V measurements would be valuable for distinguishing trapping effects.

Appendix A

Hydrogen termination process:

Steps	Hydrogen termination process
1	Sample load and pump chamber to vacuum
2	Stage heats up to 800°C
3	Hydrogen plasma strike
4	Stage cools down to 700°C
5	Stop the hydrogen plasma
6	Chamber cool down to room temperature
7	Chamber venting

Table A. Hydrogen termination process provided by Dr. Alastair Stacy from Australia.

Appendix B

Two-stage high-temperature acid clean process:

Two-stage high-temperature acid clean	
Step1	Mix 65% HNO_3 and 37% HCl in the ratio of 1:1
Step2	Heat the acid mixture to 120°C
Step3	Soak samples in the boiled acid for 20 minutes
Step4	Rinse samples in RO water to clean off the acid residue
Step5	Mx 65% HNO_3 and 95%H_2SO_4 in the ratio of 1:3
Step6	Heat the acid mixture to 250°C
Step7	Soak samples in the boiled acid for 20 minutes
Step8	Rinse samples in RO water to clean off the acid residue

Table B. Two-stage high-temperature acid clean process in this work.

Appendix C

Parameters for the resist used in this work:

	LOR3A	S1805	PMMA (50k 12%)	PMMA (200k 4%)
Spinning	5000rpm 45s	5000rpm 45s	5000rpm 60s	5000rpm 60s
Baking	180°C 5mins	115°C 3mins	180°C 5mins	180°C 5mins
Development Solvent	2.5%TMAH CD26	1:1 Microposit: R.O. water	1:2.5 MIBK: IPA	1:2.5 MIBK: IPA
Development duration	35-40s	75s	23°C 45s	23°C 45s
Ashing	300W, 2mins		200W, 1min	

Table C. Parameters for the resist used in this work. LOR3A stands for lift-off resist, S1805 is a photoresist, and PMMA is an e-beam resist. LOR is not sensitive to either UV light or e-beam; however, it can be lifted off and etched by TMAH.

Appendix D

Extraction of Contact Resistance from TLM Measurements:

Au contact, the plot is shown in Figure 7.1.4

For a linear TLM structure with two identical ohmic contacts separated by a gap length $L$and having contact width W, the measured total resistance between the two pads can be written as

$$R_{\mathrm{tot}}(L) = \frac{R_{\mathrm{sh}}}{W} L + 2R_c,$$

where:

- $R_{\mathrm{tot}}(L)$is the measured resistance between the two contacts (Ω),
- R_{sh} is the sheet resistance of the semiconductor/channel region (Ω/□),
- W is the contact width (m, or μm as used consistently),
- L is the spacing (gap length) between contacts (m or μm),
- R_c is the resistance of a single contact (Ω),
- $2R_c$ is the combined resistance contribution from both contacts (Ω).

The measured Au TLM data is shown in Table D.

Gap size (um)	Averaged resistance (Ω)
2	375.795
4	673.9671
6	1010.438
8	1337.083

Table D.1 The initial averaged resistance measured from Au TLM contact.

Hence, the equation of the fitted line is y = 161.02x + 44.237.

$$\mathrm{R_c} \approx \frac{44.24}{2} = 22.12\Omega.$$

The gap-size axis intercept (the intercept on the L-axis when $R_{\mathrm{tot}} = 0$),

$$2\mathrm{L_t} \approx -\frac{44.24}{161.02} = -0.275\mu\mathrm{m}.\ \mathrm{L_t}=0.14\mu\mathrm{m}.$$

Because contact resistance is reported normalised to the contact width, the width-normalised contact resistance is defined as:

$$R_cW = R_c \cdot W,$$

where R_c is in Ω and W is in mm, giving units of $\Omega \cdot$ mm.

Here,

$$W = 100\mu\text{m} = 0.1\text{mm}$$

Therefore,

$$\text{R}_\text{c}\text{W} \approx 22.12 \times 0.1 = 2.21\ \Omega \cdot \text{mm}$$

Extraction of Contact Resistance from CTLM Measurements:

Pd and Mo contact, the plot is shown in Figure 7.1.6

The measured Pd TLM data is shown in Table D.1

Gap size (um)	Averaged resistance (Ω)	Correction factor	Corrected
2	129.8265684	0.98052	132.4061273
4	193.7364182	0.96201	201.3864837
6	287.9408006	0.94441	304.8909989
8	352.9905935	0.92763	380.5315525
10	423.9886932	0.91161	465.0999044

Table D.1 The initial averaged resistance measured from Pd CTLM contact.

The measured Mo TLM data is shown in Table D.2

Gap size (um)	Averaged resistance (Ω)	Correction factor	Corrected
2	122.5541752	0.98052	124.9892369
4	217.3736062	0.96201	225.9570327
6	249.1248639	0.94441	263.7900862
8	295.9096634	0.92763	318.9970658
10	446.3351993	0.91161	489.6131946

Table D.2 The initial averaged resistance measured from Pd CTLM contact.

For the CTLM structure:

- Inner diameter = 100 μm, the inner radius

$$\text{r} = 50\ \mu\text{m} = 0.05\ \text{mm}$$

- Gap spacing d is varied (here $\mathrm{d} = 2{,}4{,}6{,}8{,}10\ \mu\mathrm{m}$).

For a circular contact, the effective contact width is the circumference:

$$W_{\mathrm{eff}} = 2\pi r$$

Numerically:

$$\mathrm{W_{eff}} = 2\pi(50\ \mu\mathrm{m}) = 314.16\ \mu\mathrm{m} = 0.31416\ \mathrm{mm}$$

The width-normalised contact resistance is defined as:

$$R_c W = R_c \cdot W_{\mathrm{eff}}$$

To extracted R_c:

The equation of the fitted line for Pd is y = 42.227x + 43.503, and the equation of the fitted line for Mo is y = 41.114x + 37.983

- Pd:

$$R_{c,\mathrm{Pd}} = \frac{43.5032}{2} = 21.7516\ \Omega$$

- Mo:

$$R_{c,\mathrm{Mo}} = \frac{37.9829}{2} = 18.9915\ \Omega$$

Use the CTLM circumference normalisation:

$$R_c W = b\pi r \text{ with } \pi r = \pi(0.05\ \mathrm{mm}) = 0.1570796\ \mathrm{mm}$$

- Pd:

$$R_{cW,\mathrm{Pd}} = 43.5032 \times 0.1570796 = 6.83\ \Omega \cdot \mathrm{mm}$$

- Mo:

$$R_{cW,\mathrm{Mo}} = 37.9829 \times 0.1570796 = 5.96\ \Omega \cdot \mathrm{mm}$$

To extracted L_t:

- Pd:

$$L_{T,\mathrm{Pd}} = \frac{43.5032}{2 \times 42.2266} = 0.515\ \mu\mathrm{m}$$

- Mo:

$$L_{T,\mathrm{Mo}} = \frac{37.9829}{2 \times 41.1144} = 0.462\ \mu\mathrm{m}$$