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Gallium Nitride Transistors for Power Switching Applications

Sahalu Hassan

Submitted in fulfilment of the requirements for the Degree of Doctor of Philosophy

James Watt School of Engineering, Electronics and Nanoscale Engineering

Supervised by

Prof. Edward Wasige

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Abstract

The growing demand for compact, robust, and energy-efficient power electronic systems has driven intensive research in gallium nitride (GaN) transistor technology over the past two decades. While GaN devices offer superior material properties for high-power and high-performance applications, their widespread adoption in power switching applications has been hindered by reliability concerns, operational mode limitations, and challenges in achieving reliable high-voltage capability.

This thesis investigates strategies to enhance GaN device performance, focusing on improved voltage handling capability, reliable enhancement-mode operation, and mitigation of trap-assisted degradation to reduce on-resistance in both lateral and vertical device architectures.

A combined approach of experimental characterization and TCAD-based device simulation was employed in this project. Experimentally, the role of channel and nucleation layer thicknesses in buffer-free AlGaN/GaN high electron mobility transistors (HEMTs) on silicon carbide substrates were analysed. Wafer 2, featuring a thicker GaN channel, delivered the highest drain current density but suffered from increased off-state drain leakage and pronounced dynamic threshold instability at high bias. In contrast, Wafer 3, incorporating a thicker AlN nucleation layer, achieved a more balanced performance with moderate current enhancement, reduced gate leakage, superior breakdown voltage, and improved dynamic stability.

In parallel, a novel vertical GaN field-effect transistor was proposed and studied through rigorous TCAD simulations to achieve enhanced electrostatic control and improved breakdown performance. The device incorporates a vertical fin channel fully surrounded by a conformal gate, enabling efficient carrier confinement and transport. Simulation results demonstrate a breakdown voltage of ~1430 V, a threshold voltage of ~1.3 V, and improved forward conduction current, compared to conventional vertical GaN FinFETs with ~840 V breakdown and ~1.0 V threshold voltage. Moreover, the proposed architecture offers a simplified fabrication process compared to the conventional Vertical GaN FinFET.

Overall, the findings of this thesis provide valuable insights into design and engineering strategies for both lateral and vertical GaN devices, advancing their potential for next-generation, energy-efficient, and high-performance power electronics.

List of Publications

a. Journal Articles

[1] Karami, K., Hassan, S., Taking, S., Ofiare, A., Dhongde, A., Al-Khalidi, A., and Wasige, E. (2023). *Comparative Study of Al_2O_3 and HfO_2 as Gate Dielectric on AlGaN/GaN MOSHEMTs*. International Journal of Electronics and Communication Engineering, 17(2), pp. 47–50.

[2] Hassan, S., Karami, K., Ofiare, A., Wasige, E., and Al-Khalidi, A. (2025). *Impact of Channel and Nucleation Layer Thicknesses on Buffer-Free AlGaN/GaN HEMTs*. (Under review).

[3] Hassan, S., Cheng, Z., Al-Khalidi, A., and Wasige, E. *Enhanced Electrostatic Control and Breakdown Voltage in a Gate Wrap-Around Vertical GaN FinFET: A TCAD Study*.(Under preparation).

b. Conference Contributions

[1] Hassan, S., Kadandani, N. B., Karami, K., Dwidar, M., Wasige, E., and Al-Khalidi, A. (2023). *Evaluation of DC Performance of Buffer-Free AlGaN/GaN HEMT on SiC Relative to the Thickness of AlN Nucleation Layer*. 14th International Renewable Energy Congress (IREC 2023), pp. 8–11. doi: 10.1109/IREC59750.2023.10389436

[2] Kadandani, N. B., Hassan, S., and Al-Khalidi, A. (2023). *An Overview of the Role of Solid-State Transformers in Extreme Fast Charging of Electric Vehicles*. 14th International Renewable Energy Congress (IREC 2023). doi: 10.1109/IREC59750.2023.10389423

[3] Hassan, S., Karami, K., Afesomeh, O., Wasige, E., and Al-Khalidi, A. (2024). *Impact of Channel Layer Thickness in Buffer-Free AlGaN/GaN High Electron Mobility Transistors on SiC Substrates*. UKNC 2024, 10 January 2024.

[4] Hassan, S., Cheng, Z., Iloke, J. I., Al-Khalidi, A., and Wasige, E. (2024). *Vertical GaN FinFET with Linearly Doped Drift Layer for High-Power Switching Applications*. UK Semiconductors 2024, 8–9 July 2024.

[5] Hassan, S., Cheng, Z., Iloke, J. I., Al-Khalidi, A., and Wasige, E. (2025). *Electrostatic Control and Breakdown Enhancement in a Gate-Enclosed Vertical GaN FinFET: A TCAD*

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Finally, I dedicate this thesis to my late parents. Their endless sacrifices, unconditional love, and lifelong prayers have been the true foundation of all my achievements. This accomplishment is a tribute to them.

Chapter 1

Introduction

1.1 Background

Modern electronic technology is fundamental to enhancing efficiency, reliability, and flexibility across critical sectors like power systems, renewable energy, transportation, and computing. In power systems, it optimizes performance at the transmission, distribution, integration, and consumption levels. Power electronics are also indispensable in electric vehicles (EVs), aerospace systems, and industrial automation. Within telecommunications and computing, they enable energy-efficient data centers, high-speed networking, and reliable power conversion for digital infrastructure, supporting advanced energy management and sustainability. Global power consumption continuously rises, driven by population growth, industrialization, urbanization, economic development, and the proliferation of digital technologies, all requiring high-performance electronic systems. To ensure power systems meet this demand without overstretching, improvements in efficiency, reliability, and capacity are essential. High-temperature electronics are also in demand across sectors such as aerospace, automotive, military, industrial systems, deep-sea oil and gas exploration, where conventional device technology fails under extreme conditions. These challenges underscore the urgent need for more robust solutions in power electronics.

For decades, silicon (Si) has been the cornerstone of semiconductor technology due to its abundance, cost-effectiveness, and well-established manufacturing processes. While silicon has been effective across many applications, its fundamental material limits now restrict further progress [1]. Its relatively narrow bandgap leads to performance degradation at high frequencies, high power, or extreme temperatures. Silicon devices are typically reliable only below 150 °C, and beyond this threshold they become prone to failure [2]. Additionally, controlling switching and conduction losses becomes increasingly difficult at higher power levels and switching speeds, with cooling requirements escalating correspondingly [3]. These constraints render silicon less viable

for next-generation power electronics and have shifted research focus to wide bandgap (WBG) semiconductors (Eg > 3 eV), such as silicon carbide (SiC), gallium oxide (Ga_2O_3), and gallium nitride (GaN). Among these, GaN has emerged as the most promising candidate for power-switching applications. It offers superior performance over Si, including higher efficiency, faster switching speeds, and a smaller form factor. GaN also possesses distinct advantages over SiC, such as ultra-high switching speeds (~150 V/ns) [4] and zero reverse recovery losses [5], [6] (in technologies like HEMTs and FinFET), and lower switching energy [3], [6].

Figure 1.1 illustrates the comparative power-handling capabilities and operational frequency ranges of various semiconductor device technologies, including silicon (IGBTs and MOSFETs), SiC, and GaN [7]. The performance disparity among these materials is evident. GaN devices can operate at frequencies exceeding 5 MHz while maintaining power levels around 10 kW, whereas Si and SiC devices are typically limited to below 100 kHz and 500 kHz, respectively, under similar conditions. Furthermore, GaN devices could exhibit more than 50% lower switching energy compared to SiC [5], [8], leading to substantially reduced power loss. This exceptional combination of high frequency, high efficiency, and power density establishes GaN-based electronics as a key enabler for next-generation high-performance, sustainable, and resilient power systems.

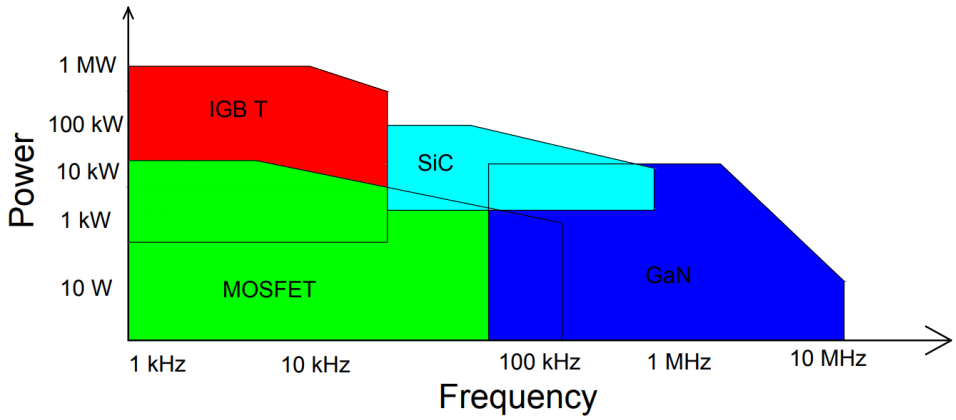


Figure 1.1 Comparing power handling capabilities against operational frequencies for GaN, Si and SiC frequencies for GaN, Si and SiC. At 10kW, GaN is shown to operate at 5 MhZ while Si and SiC are limited to frequencies below 1 MhZ at the the same power level [7].

1.2 Gallium Nitride (GaN): Crystal Structure and Material Properties

Gallium nitride (GaN) is a wide-bandgap III-V semiconductor that has attracted extensive research and industrial interest owing to its exceptional electrical, thermal, and

mechanical (hardness, elastic modulus, and thermal elasticity) properties. These characteristics make it particularly well-suited for high-power, high-frequency, and optoelectronic applications. Structurally, GaN is a binary compound composed of gallium (Ga) and nitrogen (N). Under ambient conditions, it crystallizes primarily in the thermodynamically stable wurtzite phase, while the zinc blende structure can be achieved under specific epitaxial growth conditions.

1.2.1 Wurtzite Crystal Structure

The wurtzite structure, which is thermodynamically stable for GaN at room temperature and atmospheric pressure, crystallizes in a hexagonal lattice with space group $P6_3mc$. In this structure, as shown in Figure 1.2, each gallium atom is tetrahedrally coordinated by four nitrogen atoms, and vice versa. The inherent anisotropy of the wurtzite lattice gives rise to pronounced polarization effects (spontaneous and piezoelectric) which play a central role in the operation of GaN-based high electron mobility transistors (HEMTs) and other device architectures. The lattice constants of wurtzite GaN are approximately a = 3.189 Å and c = 5.185 Å, yielding a c/a ratio close to 1.625, which is near the ideal value for hexagonal close packing [9].

In contrast, the zinc blende phase of GaN adopts a cubic structure but it is metastable and typically grown on lattice-matched cubic substrates such as GaAs under non-equilibrium conditions [10], [11]. While zinc blende GaN lacks the strong polarization fields found in wurtzite, it is less commonly used due to growth complexities and reduced thermal stability.

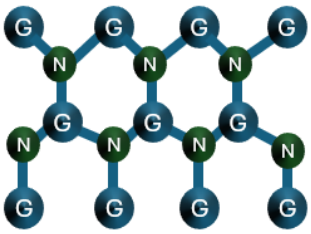


Figure 1.2 Crystal structure of wurtzite GaN showing the tetrahedrally strong polar covalent bonding of GaN and N atoms [9].

1.2.2 Material Property of Semiconductor

Semiconductors exhibit unique material properties that distinguish them from conductors and insulators. Their electrical conductivity lies between the two and can be precisely controlled by doping and external stimuli such as temperature, light, or electric

field. Key properties include bandgap energy, carrier concentration, mobility, and dielectric constant, all of which directly influence device behavior and performance. Table 1.1 summarises the key material properties of the state-of-the-art semiconductor materials.

Table 1.1 Properties of some state-of-the-art semiconductor materials [1], [12]

MATERIAL PROPERTY	UNIT	SEMICONDUCTOR MATERIAL				
		Si	***GaAs***	***Ga_2O_3***	***SiC***	***GaN***
Energy Band Gap	eV	1.12	1.43	4.85	3.26	3.44
Relative Dielectric Constant	-	11.9	12.5	10	9.7	9.5
Thermal Conductivity	W/mK	150	54	300	400	130
Breakdown Electric Field	MV/cm	0.3	0.4	8.0	3.0	3.3
Saturated Electron Velocity	cm/s	1×10^7	1×10^7	2×10^7	2×10^7	2.5×10^7
Electron Mobility	$cm^2/V.s$	1500	8500	300	700	1000

1.2.2.1 Energy bandgap

The bandgap of a semiconductor is the energy difference between the top of the valence band (where electrons are bound to atoms), and the bottom of the conduction band, where they are free to move. This fundamental property governs the electrical and optical behavior of every semiconductor material. A wider energy bandgap (E_g), such as that of GaN, enables the material to withstand significantly higher electric fields before breakdown, allowing operation at much higher voltages and power densities. GaN's wide bandgap results in a much lower intrinsic carrier concentration compared to Si. At room temperature (300 K) [9][13], [14], the intrinsic carrier concentration (n_i) of GaN is approximately 10^{-12} cm^{-3}, whereas Si exhibits a much higher n_i of about 10^{10} cm^{-3}. This low intrinsic carrier concentration helps GaN devices maintain stable conductivity modulation under typical operating conditions. However, with increasing temperature, n_i rises exponentially due to thermal excitation of electrons across the bandgap as shown in equation (1.1). In Si, this leads to a sharp increase in leakage currents and eventual device failure at junction temperatures around 150°C (without effective heat sink) [15]. In contrast, GaN's wider bandgap greatly suppresses thermal carrier generation, enabling reliable operation at temperatures exceeding 400°C [16], [17]. This thermal resilience makes GaN particularly well-suited for harsh environments, including those found in power conversion systems, electric vehicles, aerospace applications, and deep-sea exploration.

$$n_i = \sqrt{N_c N_v} \exp\left(-\frac{E_g}{2kT}\right) \tag{1.1}$$

where;

N_v - Effective density of states in the valence band (cm^{-3}).

E_g - Energy bandgap (eV).

k - Boltzmann constant ($\approx 1.38 \times 10^{-23}$ J/K or 8.617×10^{-5}eV/K).

T - Absolute temperature (Kelvin, K).

Another major advantage of GaN is its ability to undergo bandgap engineering through alloying with elements such as aluminium (Al) and indium (In), forming a ternary

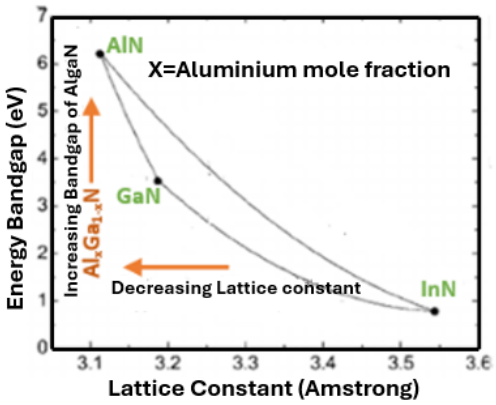


Figure 1.3 Energy bandgap modification of AlGaN with aluminium mole fraction[12]

compounds such as AlGaN and InGaN. This approach allows for the tailoring of electronic and optical properties for a specific semiconductor device application.

To obtain aluminium gallium nitride ($Al_xGa_{1-x}N$) of a specific alloy composition, the bandgap can be continuously tuned between that of GaN (E_g =3.4 eV) and aluminium nitride (E_g =6.1 eV) by varying the aluminium mole fraction (x). This compositional adjustment not only modifies the bandgap but also alters the ma terial's lattice constant, as illustrated in Figure 1.3. As a result, the energy bandgap of $Al_xGa_{1-x}N$ is always larger than that of pure GaN for any non-zero aluminium content. The precise value of the bandgap for a given composition can be estimated empirically from Equation (2).

$$E_g(x) = xE_g(AlN) + (1-x)E_g(GaN) - bx(1-x) \tag{1.2}$$

where $Eg(GaN)$ = 3.4eV, $Eg(AlN)$ = 6.1eV, x is the aluminium mole ratio and b is the bowing parameter.

1.2.2.2 Critical electric field

Critical electric field (E_{crit}) of a semiconductor is the maximum electric field that the material can withstand before it breaks-down (i.e when the material loses its insulating properties and allows uncontrolled current flow). It is a fundamental property that determines how much voltage a semiconductor device can handle before failure.

The high critical electric field strength is a crucial parameter in power semiconductor devices, as it directly determines the maximum voltage the device can block when it is turned-off. GaN, with a critical electric field of approximately 3 MV/cm, significantly outperforms Si, which has a critical field of only 0.3 MV/cm. This nearly tenfold enhancement in E_{crit} enables GaN devices to sustain approximately ten times higher voltages than silicon devices of the same drift region width. The relationship is quantitatively represented by the breakdown voltage expression in equation (1.3):

$$\mathrm{V_{BR}} = \frac{1}{2}\left(E_{crit} W_{drift}\right) \tag{1.3}$$

where

$\mathrm{V_{BR}}$ is the breakdown voltage of the device,

E_{crit} is the critical electric field of a semiconductor material,

W_{drift} is the width of the drift region of the device.

According to equation (1.3), the breakdown voltage is directly proportional to both the critical electric field and the drift region thickness. Therefore, for a given W_{drift}, selecting a material with a higher E_{crit}, such as GaN, ultimately allows for a much higher $\mathrm{V_{BR}}$, or conversely, enables device miniaturization without compromising voltage-blocking capability.

The ability to scale down device size while maintaining high-voltage operation offers several key advantages. These include reduced device dimensions leading to increased power density and lower parasitic elements (such as junction capacitance, and interconnect inductance), which in turn minimize switching losses and enable faster charge and discharge cycles. This enhanced performance allows for the development of more compact and efficient power conversion systems. Furthermore, higher integration

density per chip reduces manufacturing costs by allowing more devices to be fabricated on a single wafer, improving overall scalability and economic viability.

1.2.2.3 Electron mobility

Electron mobility (μ) is a fundamental parameter in semiconductor physics, representing the ease/speed with which electrons can traverse a material under the influence of an electric field. It significantly influences both the electrical conductivity and the dynamic performance of semiconductor devices. High electron mobility implies a reduced carrier scattering within the crystal lattice, thereby enabling rapid carrier transport. This results in faster device response times and improved overall efficiency, particularly in high-frequency and power applications. The drift velocity v_d of electrons, which is directly proportional to the applied electric field E_{crit},, is given by the relation in equation (1.4).

$$v_d = \mu E_{crit} \tag{1.4}$$

Where

μ is the carrier mobility and

E_{crit} is the critical electric field of the semiconductor material

This equation describes the importance of high mobility in achieving greater carrier velocities under a given field, which translates into faster switching behavior.

GaN exhibits relatively high electron mobility, typically ~700-1400 $cm^2/V.S$ in its bulk form (depending on the purity) [18]. However, when a heterojunction is formed by growing a thin epitaxial layer of materials such as Aluminium Gallium Nitride (AlGaN), Aluminium Nitride (AlN), or Indium Aluminium Nitride (InAlN) on a thicker GaN substrate, a two-dimensional electron gas (2DEG) is formed at the interface due to polarization effects. In this confined 2DEG region, electrons are spatially separated from donor impurities and thus experience significantly reduced Coulomb scattering. This leads to an enhanced mobility value, often exceeding 2000 $\frac{cm^2}{V}.S$, depending on the heterostructure composition and quality [13].

The high electron mobility in GaN-based heterostructures enables rapid electron transport, thereby reducing carrier transit time. The reduced transit time results in

increased current density (J_e) and lower on-state resistance $\mathrm{R_{DS(on)}}$, which collectively minimize conduction losses and enhance overall device performance and efficiency. As expressed in Equations (1.5), these interrelated characteristics collectively result in higher power density and faster switching speed enabling GaN devices to deliver greater output power within a smaller footprint.

$$\mathrm{R_{DS(on)}} = \frac{4V_{BR}^2}{E_{cr}^3 e_o e_r \mu_r} \tag{1.5}$$

where

$R_{DS(on)}$ - On-state resistance

V_{BR} - Breakdown voltage

E_{cr} - Critical electric field

ε_0 - Permittivity of free space

ε_r - Relative permittivity

μ_n - Electron mobility

$$J_e = en\mu_r E_{cr} \tag{1.6}$$

where;

J_e - Electron current density at the critical electric field.

e - Electron charge ($\approx 1.602 \times 10^{-19}$ coulomb).

n — Electron concentration or carrier density in the semiconductor.

μ_n - Electron mobility (same as above).

E_{cr} - Critical electric field (same as in Equation 1.5).

1.2.2.4 Thermal Conductivity

Thermal conductivity is a critical material property that quantifies a semiconductor's ability to conduct heat. It is especially important in high-power and high-frequency semiconductor devices, where significant heat is generated due to Joule heating. Efficient heat dissipation is essential to prevent elevated junction temperatures, which can degrade carrier mobility, shift threshold voltages, accelerate material degradation, and ultimately lead to thermal runaway and catastrophic device failure. Moreover, poor thermal management contributes to increased power losses, limiting the energy

efficiency and reliability of the system. GaN, owing to its wide bandgap and strong covalent bonding, exhibits relatively good thermal conductivity, typically around 130 $W/m.k$. The actual thermal conductivity value depends on several factors, including crystalline quality, defect concentration, doping levels, and the type of substrate used. The ability of a material to conduct heat can be described by Fourier's Law of heat conduction [12]:

$$q = -k\nabla T \tag{1.7}$$

where q is the heat flux vector (W/m^2), k is the thermal conductivity (W/mK), and ∇T is the temperature gradient across the material.

In this context, a higher thermal conductivity allows more effective heat removal under a given thermal gradient.

Substrate selection plays a vital role in overall thermal management. For instance, while GaN-on-Si is cost-effective and widely used, its thermal conductivity is significantly lower than that of GaN-on-SiC. Silicon carbide (SiC), with a thermal conductivity of ~400 W/mK, provides superior heat spreading, making it an optimal substrate for high-power GaN devices. Therefore, engineering thermal pathways, through material choice, device layout, and heat sink integration, is fundamental to harnessing GaN's full potential in power applications.

1.2.2.5 Polarization effects

As discussed earlier, in the wurtzite crystal structure of group III-nitride semiconductors, Ga and N atoms are arranged in a tetrahedral coordination, forming strong polar covalent bonds. The significant electronegativity difference between Ga and N leads to a non-centrosymmetric charge distribution, giving rise to an intrinsic spontaneous polarization [13]. This polarization is a consequence of the lack of inversion symmetry in the wurtzite lattice and manifests as a built-in electric field oriented along the c-axis ([0001] direction) of the crystal. The spontaneous polarization is typically negative in sign and increases in magnitude from GaN to InN and AlN due to increasing ionicity and bond asymmetry [19], [20]. In III-nitride materials, the internal electric fields arising from spontaneous

polarization can reach up to 3 MV/cm [21], significantly influencing electronic properties such as carrier distribution and band bending.

In addition to spontaneous effects, piezoelectric polarization arises in strained heterostructures, such as those found in AlGaN/GaN high-electron-mobility transistors (HEMTs). When a thin layer of AlGaN is epitaxially grown on a thicker GaN buffer layer along the c-axis (as shown in Figure 1.4), the difference in lattice constants introduces biaxial strain in the AlGaN layer. Since AlGaN has a smaller lattice constant than GaN, it undergoes in-plane tensile strain to accommodate the larger GaN lattice beneath it. This strain, coupled with the piezoelectric nature of III-nitrides, induces an additional polarization component along the growth direction. The resulting piezoelectric polarization is additive to the spontaneous component and further enhances the internal electric field at the heterojunction interface [4]. The total polarization P_{total} in such heterostructures is given by the sum of spontaneous and piezoelectric polarization components expressed in equation (1.8).

$$P_{total} = P_{sp} + P_{pz} \tag{1.8}$$

where P_{sp} is the spontaneous polarization (C/m^2), and P_{pz} is the piezoelectric polarization induced by strain (C/m^2).

The abrupt change in polarization across the AlGaN/GaN interface gives rise to a polarization-induced charge, which attracts free electrons from the surrounding material and forms a high-density two-dimensional electron gas (2DEG) at the interface without intentional doping. This phenomenon is fundamental to the operation of GaN-based HEMTs, enabling high electron mobility and carrier confinement critical for high-speed, high-power device applications [9].

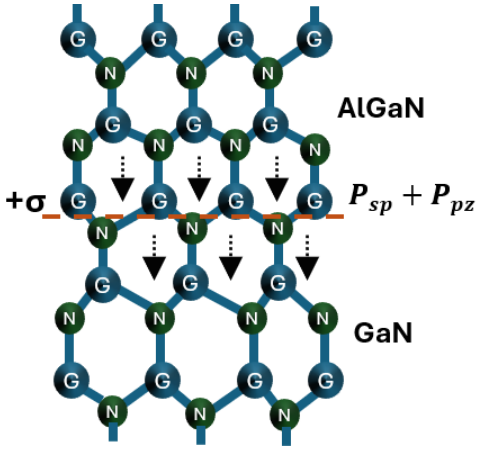


Figure 1.4 Charge-Induced Effects in AlGaN/GaN Layered Structure[13]

1.3 Key Challenges in GaN Power Device Development

While GaN devices were originally developed for optoelectronic applications, recent advancements have firmly established GaN as a strong contender to replace silicon in high-power switching technologies. GaN-based power transistors have demonstrated significant improvements in efficiency, switching speed, and thermal handling, making them well-suited for emerging applications. Despite these promising developments, several problems remain unsolved, and researchers are in the pursuit of exploring GaN's capabilities in power switching application spaces. The key technical challenges are discussed in the following sections.

1.3.1 Lack of robust, high-power GaN transistors

While significant progress has been made in demonstrating high-voltage (>1 kV) GaN transistors at the research level, their commercial penetration into high-power switching applications has been relatively slow. Most of the high-power systems such as electric traction powertrains (30-350 kW) [14], onboard fast battery chargers (3.3-21 kW), PV inverters (0.3-5 kW), wind turbines, transmission and smart grid systems are still dominated by silicon IGBTs (insulated gate bipolar transistor), MOSFETs (metal oxide semiconductor field effect transistors), GTOs (gate turn off thyristors) and SCRs (silicon-controlled rectifiers). Commercialized Si IGBT technology has developed over the past 35 years, and within this period, its power density has been increased from 35 kW/cm^2 to about 250 kW/cm^2 [22], [23]. While discrete SiC transistors (IGBTs and MOSFETs) covering operating voltages between 600 to 1700 V [24] have been adopted in the market

(for applications such as hybrid and electric vehicle traction inverters), GaN devices of 900 V [25] and 1200 V [26] are only recently presented by vendors such as GaNPower, and the widely commercialized GaN devices are within voltage classes of 15 to 650 V [27] in applications such as data centers, lidar systems, power supplies, fast chargers, and in consumer electronics that are low power markets, typically within 10 W to 3 kW in power spectrum, areas that SiC can also rival effectively. The lack of commercial adoption is largely due to some critically unsolved technical and economic constraints. The economic constraints include high cost and smaller sizes (< 8 inches) of native GaN wafers, and the economic viability of integrating GaN processes into the established manufacturing workflows (commonly available for Si technology).

1.3.2 Lack of robust over-voltage withstand capability

One of the critical limitations of GaN-based high electron mobility transistors (HEMTs) is their inherently poor over-voltage tolerance due to the absence of a robust avalanche breakdown mechanism. Unlike silicon or silicon carbide power devices, which typically incorporate a P-N junction or body diode that can safely absorb transient over-voltages through avalanche conduction, GaN HEMTs lack such intrinsic protection. As a result, they are highly susceptible to catastrophic failure when subjected to voltage transients that exceed their dynamic breakdown threshold [22], [23].

This limitation presents a significant reliability concern in practical applications, where inductive switching transients, load dump conditions, or poor circuit layout can cause voltage spikes. To mitigate the risk of failure, manufacturers often derate GaN devices, i.e., specify operational voltage levels significantly below their nominal breakdown voltage [28]. While this conservative design approach helps improve device robustness and reliability, it also imposes serious technical and economic trade-offs. Device derating leads to underutilization of the device's theoretical capabilities, requiring larger devices or parallel configurations to meet power demands. This, in turn, increases the system's physical footprint and cost, while decreasing power density (negating some of the key advantages GaN technology offers over silicon). Consequently, improving the over-voltage ruggedness of GaN devices through structural innovations (e.g. active clamping, or integration of protection circuits) remains an active area of research and development aimed at expanding their reliability envelope for high-power applications.

1.3.3 Premature breakdown due to electric field crowding

During the off-state operation of GaN HEMT, a strong electric field develops within the device, particularly concentrating near the gate edge on the drain side. This non-uniform distribution, known as electric field crowding, can lead to premature breakdown, especially when the local electric field exceeds the critical breakdown threshold of the GaN material.

To mitigate this, field plate structures are commonly introduced. These are metal extensions connected to the gate or source that extend over the passivation layer towards the drain [29]. Field plates help redistribute the electric field more evenly across the gate-drain spacing, effectively shifting the field peak away from the gate edge to the field plate edge, thereby enhancing breakdown voltage and device reliability [29]. However, longer or more extensive field plates increase parasitic capacitance, notably the gate-drain capacitance (C_{gd}), which in turn slows the switching transients. This trade-off between breakdown robustness and switching speed leads to increased switching losses, reduced overall system efficiency, and potentially larger and more complex power management circuits due to slower switching dynamics.

Therefore, optimizing field plate design is crucial in GaN power device engineering to balance voltage handling capability, efficiency, and switching performance.

1.3.4 Time-dependant failure in MIS-HEMT and p-GaN gate HEMTs

In metal insulator semiconductor (MIS)-AlGaN/GaN HEMTs, a gate dielectric layer is deposited over the AlGaN barrier to suppress quantum mechanical tunnelling of electrons through the Schottky gate, thereby reducing gate leakage current. Common dielectric materials used in GaN-based devices include silicon nitride (SiN_x), aluminium oxide (Al_2O_3), and hafnium oxide (HfO_2). However, the introduction of a dielectric layer over the AlGaN barrier increases the overall barrier thickness, reinforcing the device's normally-on (depletion-mode) nature. Moreover, high electric field stresses the dielectric over time, leading to gradual degradation and reduced device lifetime due to phenomena such as time-dependent dielectric breakdown (TDDB) [30], [31].

1.3.5 Dynamic instability of on-resistance

Dynamic on-resistance caused by trapping and de-trapping of carriers within the device structure results in current collapse leading to undesirable conduction losses [32]. This instability phenomenon has severe effects on the performance of GaN devices, and for over a decade, researchers developed various methods of suppressing this problem in GaN HEMTs. Surface treatments and systematic epilayer design remain the common approaches to minimizing the phenomenon of dynamic on-resistance [32]. Dynamic on-resistance is discussed in detail in section 2.1.4.1.

1.3.6 Threshold voltage shift

Threshold voltage (V_{th}) shift is a time-dependent instability phenomenon that arises from changes in the pinch-off mechanism of a GaN HEMT when the device is subjected to prolonged electrical stress, particularly during off-state or gate bias stress conditions. These shifts directly impact the device's switching behavior and long-term reliability [33].

V_{th} shifts can occur in both the positive and negative directions, depending on the type and location of charge trapping within the gate dielectric, barrier layer, or at their interfaces [30], [24]. A positive V_{th} shift increases the gate voltage required to turn the device on, which can lead to elevated on-resistance (R_{ON}) and, in severe cases, premature or incomplete turn-on. On the other hand, a negative V_{th} shift lowers the turn-on voltage threshold, potentially resulting in subthreshold leakage currents or unintended (false) turn-on events. In high-power switching applications, such false triggering can cause catastrophic system-level failures, including short circuits or damage to downstream components.

Understanding and mitigating V_{th} instability is essential for ensuring the safe and predictable operation of GaN power devices in demanding environments. This is particularly important for enhancement-mode HEMTs, where precise control of the threshold voltage is critical for fail-safe performance.

1.3.7 Instability due to output capacitances

Losses due to output capacitances are other setbacks of GaN HEMT in high-frequency high-power applications [34], [35]. An output capacitance primarily consists of an

intrinsic and extrinsic form of capacitance. The intrinsic capacitance arises basically from the semiconductor material itself, and an inherent device structure influenced by the gate-source and gate-drain access regions (in GaN HEMT) which vary with the device geometry and the bias conditions. Both capacitors charge and discharge in every switching cycle. In theory, these capacitors should ideally be lossless, however, studies show a considerable power loss during the off-state switching cycle in GaN HEMTs, though significantly higher in other power devices such as SiC MOSFETs and Si super-junction devices [34]. The loss is found to increase with increasing frequency and could dominate the total device losses in soft-switching converters at megahertz frequencies [34] .

1.3.8 Normally-off operation

Normally-off operation refers to the transistor being in off-state by default when no voltage is applied across its gate-source terminals. GaN HEMT is by default a normally-on device, however, in power switching applications, a high threshold (>3V) enhancement-mode (e-mode) device is desired due to the following reasons:

1.3.8.1 Safety

Normally-off transistors provide inherent safety benefits since they do not conduct current until they are actively driven into the conduction state by applying a voltage at their gate-source terminals, which reduces the risk of an unintended current flow preventing potential hazards in the case of system malfunction or maintenance activity. In depletion mode devices, a gate driver is designed to keep the transistor in off-state, failure of the driver presents a potential hazard.

1.3.8.2 Enhanced reliability and reduced power loss

Since normally-off transistors are by default in a non-conduction state, they exhibit reduced subthreshold and gate leakage losses at off-state. This is important in applications where power efficiency is critical such as power conversion systems in transmission, renewables, electric vehicles and automotive, etc, that handle power in gigawatt level. Secondly, they are less stressed at stand-by or idle state compared to depletion mode devices which could extend their lifetime, thus enhancing reliability.

1.3.8.3 Lesser complexity

Normally-off devices simplify the overall system design by requiring less complex gate driver circuitry. Unlike normally-on devices, which need specialized driver circuits to maintain the transistor in a non-conductive state during standby, normally-off devices inherently remain off at zero gate bias, eliminating the need for additional negative or complex gate drive voltages. This reduction in driver complexity translates to lower system cost and improved reliability.

1.3.8.4 Limitations of the currently commercialised E-mode GaN HEMTs

Although enhancement-mode (e-mode) GaN devices have been commercialized through cascode HEMT and p-GaN gate architectures, each approach presents challenges. Cascode configurations integrate a silicon MOSFET along with the GaN HEMT, and consequently, inherit limitations typical of silicon devices, such as higher turn-on/turn-off losses and increased switching losses, which constrain their performance in high-efficiency power applications. On the other hand, p-GaN gate e-mode GaN HEMTs face significant reliability concerns, including threshold voltage instability, gate leakage, and time-dependent dielectric breakdown, that continue to limit their widespread adoption[36].

1.3.9 Difficulty in achieving effective p-type doping

Effective p-type doping in GaN remains a significant challenge due to intrinsic material properties and dopant behaviour. Despite magnesium being the primary acceptor dopant, its deep energy level and low ionization efficiency limit hole concentration, hindering the performance of GaN-based devices that rely on p-type conductivity [37], [38].

1.3.9.1 Mg dopant ionization challenges in GaN

Magnesium (Mg) is the most used acceptor dopant for achieving p-type conductivity in GaN. However, Mg introduces a relatively deep acceptor level, approximately 200 to 250 meV above the valence band edge. This deep level requires substantial thermal energy to ionize the Mg atoms and release free holes, resulting in low ionization efficiency at room temperature. Consequently, only a small fraction of the incorporated Mg atoms actively contributes to hole conduction, making effective p-type doping in GaN challenging [37], [38].

1.3.9.2 Low hole mobility

Even when p-type doping is achieved in GaN, the hole mobility remains inherently low, typically less than 30 $cm^2/V{\cdot}s$. This low mobility leads to high resistivity in the p-type layers, which adversely affects device performance, especially in vertical device architectures and normally-off transistors that rely on efficient current spreading through the p-type regions [37], [38].

1.3.4 Challenges Addressed in This Thesis

The challenges outlined in Sections 1.3.1–1.3.9 highlight the multifaceted barriers limiting the widespread adoption of GaN power devices in high-power and high-reliability applications. This thesis addresses a selected subset of these open challenges through targeted device design, simulation, and structural optimization, with particular emphasis on enhancement-mode operation, reduced on-resistance and breakdown voltage enhencement.

Specifically, this work addresses the following key challenges:

- **Challenge 1.3.1 – Lack of robust, high-power GaN transistors:**

This thesis contributes to this challenge by investigating both lateral and vertical GaN device architectures focusing at improving voltage handling capability and power robustness. In particular, vertical GaN FinFET structures are explored as a scalable pathway toward high-voltage and high-power operation beyond the limitations of conventional lateral HEMTs.

- **Challenge 1.3.3 – Premature breakdown due to electric field crowding:**

This thesis investigates advanced gate and device geometries in vertical GaN FinFET structures to enhance electrostatic control and improve breakdown voltage capability. The proposed designs mitigate premature breakdown by redistributing peak electric fields more uniformly within the device.

- **Challenge 1.3.5 – Dynamic instability of on-resistance:**

Trap-assisted degradation and current collapse phenomena are investigated in lateral GaN HEMT through epitaxial layer design, which is shown to significantly influence carrier

trapping effects. Mitigation of these mechanisms stabilizes the dynamic on-resistance, thereby improving conduction efficiency under high-voltage switching conditions..

- **Challenge 1.3.6 – Threshold voltage shift:**

Threshold voltage stability is examined as a key reliability concern, particularly for enhancement-mode devices. This thesis investigates the influence of epitaxial layer design in lateral GaN HEMTs and device geometry in vertical GaN FinFETs on threshold voltage stability.

- **Challenge 1.3.8 – Normally-off (enhancement-mode) operation:**

Achieving reliable normally-off operation is a primary objective of this work. This thesis explores advanced device concepts, particularly the vertical GaN gate wrap-around FinFET architecture, to enhance and stabilize enhancement-mode device operation.

The remaining challenges discussed in this chapter, such as over-voltage avalanche robustness (Section 1.3.2), output capacitance losses (Section 1.3.7), and fundamental limitations of p-type doping in GaN (Section 1.3.9), are acknowledged as important but beyond the direct scope of this thesis.

1.5 Research Objectives and Methodology

1.5.1 Research goals

The primary objective of this research is to explore and enhance the performance of GaN-based power electronic devices by addressing key material and device-level challenges. This includes improving epitaxial layer quality, achieving normally-off operation, optimizing device architectures, and evaluating reliability under high-power conditions. The study aims to contribute to the development of a robust and efficient GaN transistors suitable for next-generation power applications. To achieve these objectives, a combination of theoretical analysis, numerical simulations, and experimental validation is employed.

1.5.2 Methodological approach

The research methodology involves an in-depth review of current GaN technologies, simulation-based design optimization, and the fabrication and characterization of

prototype devices. This multi-faceted approach ensures a comprehensive understanding of both material properties and device performance.

The work was planned to be achieved through the following objectives:

- Design and fabrication of robust lateral high voltage GaN HEMT for power switching applications.
- Design of GaN epitaxial wafer for vertical GaN transistors.
- Design and simulation of robust vertical GaN transistor for high-power switching applications.
- Measurements and characterization of the fabricated transistors.

1.6 Structure of the Thesis

This thesis has been structured into 7 chapters each addressing a specific aspect or research.

Chapter 1 provides background knowledge on the use of GaN in high power switching applications. It highlights some critical challenges of GaN transistors which should be overcome.

Chapter 2 presents a comprehensive review of prior research on GaN devices, detailing their operational principles and highlighting advancements in device design and performance that address the evolving demands of modern high-power, high-frequency applications.

Chapter 3 describes the standard fabrication and characterization techniques and the associated tools employed for GaN device processing at the James Watt Nanofabrication Centre (JWNC), University of Glasgow.

Chapter 4 investigates the influence of channel and nucleation layer thicknesses on the electrical and structural performance of buffer-free AlGaN/GaN HEMTs.

Chapter 5 presents the modelling and simulation approaches used to analyse and optimize semiconductor devices, with emphasis on Silvaco ATLAS as the primary tool.

Chapter 6 presents a comprehensive TCAD-based investigation of a novel gate wrap-around (GW) vertical GaN FinFET architecture aimed at addressing key limitations of conventional GaN power devices.

Chapter 7 provides the summary of the entire work and chapters, highlights on the nobility and the future work

1.7 Summary

This chapter introduced GaN as a contending wide bandgap semiconductor material for enhanced power electronics applications. It outlined the material's key physical properties, including energy bandgap, critical electric field, electron mobility, and thermal conductivity, which collectively contribute to its superior performance in power electronic applications. The discussion also highlighted inherent challenges in GaN technology, such as doping limitations, reliability concerns, and difficulties in achieving normally-off operation. Furthermore, the chapter established the motivation for this research, defined the key objectives, and described the methodological approach used to investigate and address the technical barriers.

Chapter 2

GaN-based Power Electronic Devices

Gallium Nitride (GaN) devices are revolutionizing the field of power electronics due to the material property discussed in the previous chapter. With a high breakdown voltage, low on-resistance, and fast switching capabilities, GaN-based transistors enable compact, efficient, and high-performance power systems. These advantages make them ideal for modern power applications. By enabling higher switching frequencies and reduced energy losses, GaN devices support the development of smaller, lighter, and more efficient power electronic systems crucial for meeting the increasing demands of next-generation energy technologies. GaN transistors can be broadly categorized based on structure into either lateral or vertical, depending on the mode of current flow.

Lateral and vertical GaN transistor architectures represent complementary solutions for a wide spectrum of power electronic applications. In the lateral GaN devices, the gate, drain, and source electrodes are fabricated on the same plane, and current flows horizontally from drain to source. In the vertical structure, drain and source electrodes are placed on the top and bottom sides of the substrate, hence, current flows vertically from drain to the source terminals.

2.1 Lateral GaN HEMTs

The lateral GaN devices are well-suited for high-frequency systems, low- to medium-voltage ($\approx < 200$ V up to ≈ 600 V) [39], [40], because at higher voltages, they become bulkier (due to increase in the access regions) thereby compounding the R_{ON} and distorting switching frequency, while vertical GaN devices are more suited to address the needs of high-voltage, high-power applications where efficiency and compactness are critical. As substrate technologies and fabrication techniques advance, vertical GaN devices are expected to play an increasingly significant role in next-generation power systems. Lateral GaN devices are predominantly realized as High Electron Mobility Transistors (HEMTs), owing to the formation of a high-density two-dimensional electron

gas (2DEG) at the AlGaN/GaN heterointerface, which provides superior carrier mobility and conductivity.

2.1.1 Formation of 2DEG in lateral GaN HEMT

The formation of a two-dimensional electron gas (2DEG) at the AlGaN/GaN heterojunction is one of the most distinguishing and advantageous features of GaN-based high electron mobility transistors. Unlike traditional silicon MOSFETs, where carriers are introduced through intentional doping, the 2DEG in GaN HEMTs arises spontaneously, driven by inherent polarization effects in the material system as described in Chapter 1 and illustrated in Figure 2.1.

In making GaN based heterojunction device, such as AlGaN/GaN high electron mobility transistors, a thin layer of AlGaN is epitaxially grown on the thicker GaN layer (Figure 2.1). Because the two materials have large difference in the energy bandgap and lattice parameters, when they are thermally in contact, the thinner layer (AlGaN in this case) exhibits another form of polarization known as piezoelectric polarization due to tensile stress.

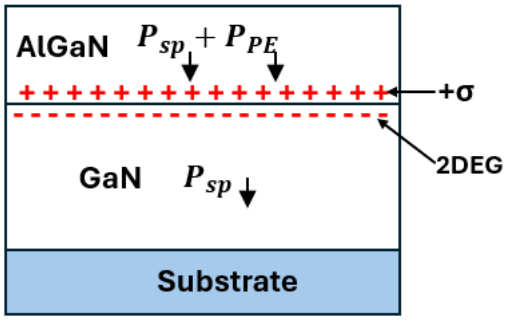


Figure 2. 1 Formation of 2DEG in AlGaN/GaN heterostructure due to polarization effects.

The spontaneous (P_{SP}) and piezoelectric (P_{PE}) polarizations will result in a fixed positive charge density at the AlGaN layer closer to the interface as expressed in equation (2.1) *[19]*.

$$\sigma = [P_{SP}(\text{AlGaN}) + P_{PE}(\text{AlGaN})] - [P_{SP}(\text{GaN}) + P_{PE}(\text{GaN})] \quad (2.1)$$

Where

σ is the sheet polarization charge density

$P_{SP}(\text{AlGaN})$ is the spontaneous polarization of the AlGaN layer

$P_{PE}(\text{AlGaN})$ is the piezoelectric polarization of the AlGaN layer

$P_{SP}(\text{GaN})$ is the spontaneous polarization of the GaN layer, and

$P_{PE}(\text{GaN})$ is the piezoelectric polarization of the GaN layer

Due to the large difference in the energy bandgaps and electron affinities (qX_1 and qX_2) of AlGaN and GaN, as illustrated in Figure 2.2, a significant conduction band offset ΔE_c is formed at their heterojunction, as shown in Figure 2.3. This discontinuity in the conduction band causes polarization-induced positive charges to accumulate at the AlGaN barrier near the interface. To maintain charge neutrality, free electrons from the GaN layer move toward this interface and become confined within the potential well created by the conduction band offset. These electrons are spatially confined in the z-direction but remain free to move in the $x - y$ plane, resulting in the formation of the two 2DEG at the AlGaN/GaN interface, as illustrated in Figure 2.3. This confinement reduces electron scattering, resulting in an exceptionally high electron mobility of up to 2000 $cm^2/V{\cdot}s$, and a high sheet carrier density of approximately $1\times10^{13}\,cm^{-2}$. The density of the 2DEG is primarily influenced by the aluminium mole fraction (x) in the $A_{lx}GaN_{1-x}N$, alloy, and to some extent, by the thickness of the AlGaN barrier layer [41], [42], [43].

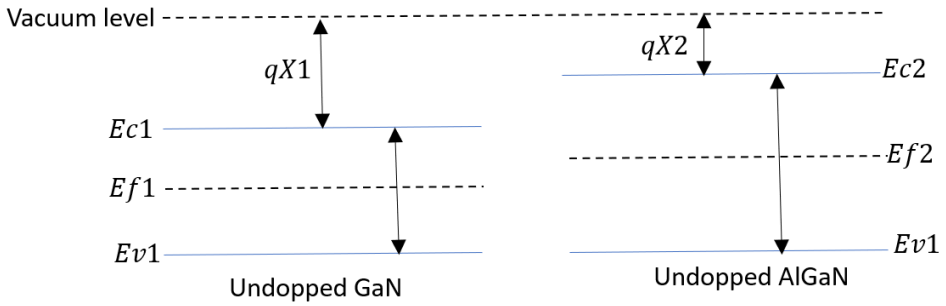


Figure 2. 2 Energy band diagram of undoped AlGaN and GaN crystals

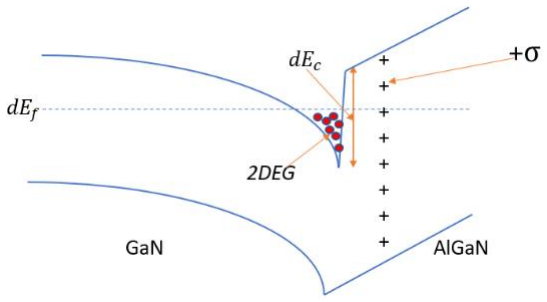


Figure 2. 3 Band diagram of the AlGaN/GaN heterostructure formation of 2DEG in the potential well

The free carriers in the 2DEG exhibit behaviour distinct from those in metals or conventional semiconductors. In metals, conductivity decreases with increasing

temperature due to enhanced electron–phonon scattering, while in semiconductors, conductivity typically increases with temperature as more carriers are thermally excited across the bandgap [44], [45]. At very low temperatures, semiconductors show reduced conductivity because of insufficient ionized carriers and reduced mobility. In contrast, the 2DEG in AlGaN/GaN heterostructures behaves differently: its carrier density is primarily governed by polarization-induced charges at the interface rather than thermal excitation, and its mobility is only weakly temperature-dependent. As a result, both carrier density and mobility remain relatively stable across a wide temperature range, leading to conductivity in the 2DEG channel that is largely insensitive to extreme thermal conditions [44], [45].

2.1.2 Basic structure and operational principle of lateral GaN HEMTs

A basic cross-sectional view of a GaN HEMT is illustrated in Figure 2.4. The device structure typically begins with a thick GaN buffer layer (usually >2 μm) epitaxially grown on a substrate (typically sapphire or Si), followed by a thin AlGaN barrier layer. At the AlGaN/GaN heterojunction, a 2DEG is naturally formed.

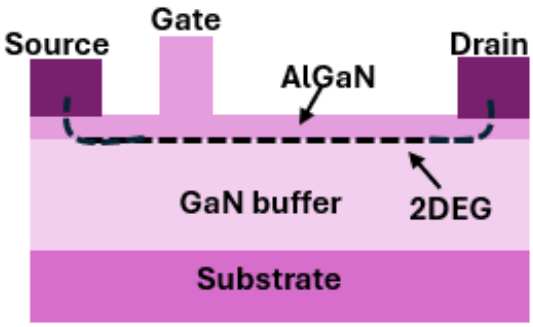


Figure 2. 4 Basic structure of GaN HEMT

Source and drain electrodes are fabricated to form low resistance ohmic contacts with the GaN channel, while a Schottky gate is placed over the AlGaN barrier to modulate channel conductivity. A thin GaN cap layer (typically 1–2 nm thick) is often deposited atop the AlGaN barrier to suppress surface oxidation, reduce the surface electric field, and facilitate the formation of low-resistance ohmic contacts. Additionally, when GaN is grown on a foreign substrate (such as Si or SiC), a nucleation layer, typically of a thin AlN-based material, is inserted between the substrate and the GaN buffer to mitigate lattice mismatch and thermal stress (due to coefficient of thermal expansion (CTE) mismatch). To minimize gate leakage current, especially under high gate bias, a thin dielectric layer

(commonly SiO_2, Si_3N_4, or a high-κ material) is sometimes introduced between the metal gate and the AlGaN barrier (in MIS-HEMTs). This dielectric must be carefully optimized to avoid introducing interface traps or compromising device reliability under operating conditions. Discussion on the optimization of GaN epitaxy through layer engineering is detailed in sections 2.1.5 and 2.1.6.

When a forward drain-source voltage (V_{DS}) is applied, electrons flow from source to drain, resulting in current flow into the external circuit. A gate-source voltage (V_{GS}) controls the conduction state of the transistor, effectively turning the device ON or OFF as demonstrated in Figure 2.5. Due to the polarization effects inherent in the AlGaN/GaN heterostructure, GaN HEMTs operate naturally in depletion mode, meaning the device conducts by default and requires a negative gate voltage (below the threshold voltage, V_{th}) to turn OFF. As discussed in Chapter 1, this normally-on behavior presents significant challenges in power switching applications, where fail-safe operation often requires normally-off (enhancement-mode) devices. This characteristic is regarded as one of the primary limitations of conventional GaN HEMTs. Consequently, significant research efforts over the past decades have been dedicated to enabling enhancement-mode (normally-off) operation. The following sections explore various approaches developed to achieve this functionality.

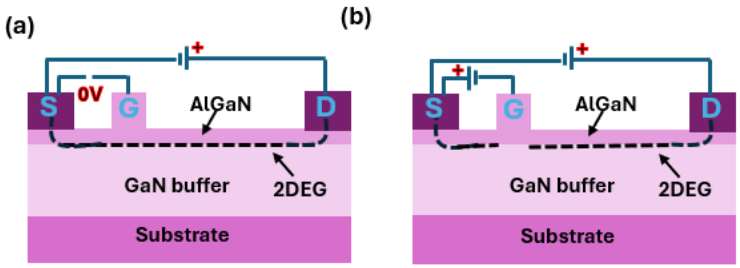


Figure 2. 5 Biasing of AlGaN/GaN HEMT (a) conducts at $V_{GS} \geq 0$ V, and (b) channel depleted at $V_{GS} < V_{th}$.

2.1.3 Enhancement mode GaN HEMTs

Achieving enhancement-mode (E-mode) operation in GaN HEMTs is a critical requirement for their widespread adoption in power electronics applications. Some of the developed approaches have matured to the point of commercialization and are now widely implemented across the power electronics industry.

2.1.3.1 Cascode configuration

The cascode configuration is a direct circuit-level solution to achieve E-mode behavior using a depletion-mode GaN HEMT. It combines a low-voltage silicon (or Si-based) MOSFET with a high-voltage GaN HEMT to produce a normally-off composite switch suitable for power electronics. The cascode structure is made such that the depletion mode GaN HEMT is connected to the low voltage N-channel enhancement mode Si-MOSFET in cascode mode, as shown in Figure 2.6. The drain of the Si-MOSFET is connected to the source of the HEMT and the source to the gate of the GaN HEMT such that when the MOSFET is off, no current flows and the composite device is off. When it is turned on, the gate of the HEMT is driven and the transistor is turned-on [46].

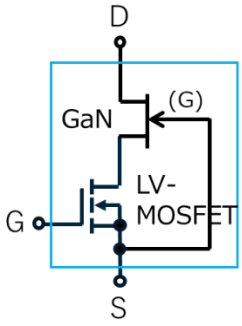


Figure 2. 6 Cascode configuration for normally-off GaN HEMT [47].

The highly matured high-speed 25–30 V Si MOSFETs, are cost effective due to the technology push by modern computer CPUs. Its breakdown voltage, operation speed, ON-resistance, and current levels when used at the low voltage side of the composite makes them a perfect match to > 600 V GaN devices. The core concept behind the composite architecture is to harness the fast-switching capability of the silicon MOSFET to drive the high-voltage GaN FET at similar speeds, thereby enabling normally-off (enhancement-mode) behavior. Simultaneously, the MOSFET facilitates high-speed control, while the GaN FET conducts the high power that the MOSFET alone could not efficiently handle at such frequencies. This configuration has been adopted by several companies such as Transphorm, Exagan, Texas instrument etc. However, the cascode structure still have some limitations, such as capacitance mismatch, increased parasitic inductance and thermal mismatch risks, potential failure modes due to interaction between the devices, and higher packaging complexity and cost [48], [49].

2.1.3.2 Recessed gate enhancement mode device

Recessed gate enhancement mode GaN HEMT is achieved by recessing the gate electrode deep into the AlGaN layer, thus the AlGaN layer beneath the gate region is thinned such that the amount of the piezoelectric field generated is reduced proportionally [50]. The AlGaN layer is etched away thus reducing the positive polarization charges under the gate electrode. When the electric field of the Schottky gate metal is larger than that generated by the piezoelectric field beneath the gate, the 2DEG will be eliminated with zero bias on the gate shown in Figure 2.7. When a positive bias voltage is applied to the gate, electrons will be attracted to the interface, thus restoring the 2DEG channel and so creating an electrical path between the source and drain electrodes.

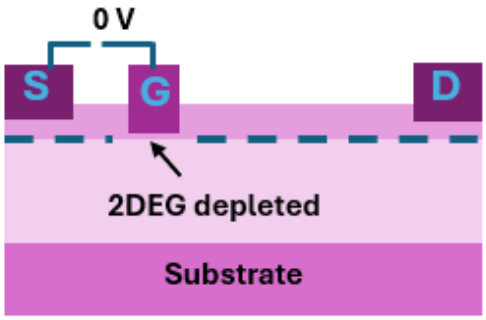


Figure 2. 7 Gate recessed into the AlGaN layer depletes 2DEG at Vgs=0 V

Recessed-gate E-mode devices face several shortcomings, including etch-induced damage, poor process uniformity, and increased on-resistance. These issues, among others, collectively restrict their commercial adoption despite the advantage of normally-off operation [50].

2.1.3.3 Fluorine ion implanted e-mode device

In this method, fluorine ions are implanted into the AlGaN layer [51]. The fluorine ions create negative ions in the layer which repel the 2DEG negative electrons thereby breaking the source-drain electrical connection. A Schottky gate is placed on top of the implanted fluorine layer as illustrated in Figure 2.8. When a positive voltage is applied on the Schottky gate, the 2DEG channel is reconstructed. Although this approach enables normally-off operation, it suffers from several disadvantages: fluorine ions may diffuse or redistribute over time, leading to threshold voltage instability; implantation-induced

lattice damage can degrade channel mobility; and reliability concerns such as gate leakage and long-term performance degradation limit its commercial viability [52].

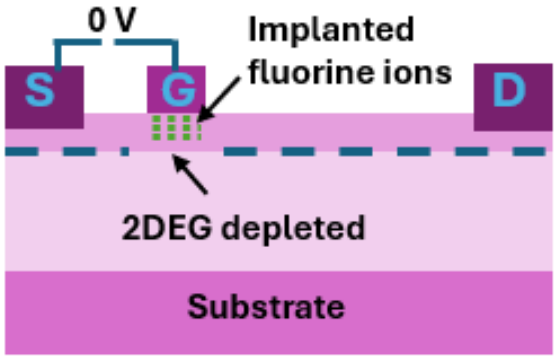


Figure 2. 8 Fluorine ions implanted into the AlGaN layer beneath the gate, depletes 2DEG at Vgs=0V

2.1.3.4 p-GaN Gate e-mode device

Another method of realizing normally OFF operation is to use a p-type doped GaN layer between the AlGaN barrier and gate electrode as shown in Figure 2.9. With appropriately designed doping level and thickness of the p-GaN layer, sufficient negative charges in the p-GaN layer would be able to deplete the 2DEG underneath. The Mg-doped pGaN layer lifts-up the potential of the heterojunction only below the gate to achieve the normally off operation of the device [31]. Table 2.1 shows the various metal/p-GaN structures reported in the literature for normally off device operation consisting of distinct doping densities and the thickness of the p-GaN layer and the threshold voltage achieved. This gating technique provides a reasonable threshold voltage (V_{th}) for normally off operation.

Table 2.1: Example of some design parameters to achieve a p-GaN E-mode HEMT.

Schottky Gate Metal stack	p-GaN thickness (nm)	p-GaN doping concentration	V_{th} (V)	V_{BR} (V)	Ref
Ni/Au	70	1e18	1.6	1300	[53]
Ni/Au (20/20nm)	100	4e19	3.6-8.2	620	[54]
Ni/Au (20/300nm)	50	3e18	0.48		[55]
Ni/Au (25/120)	60	3e19	1.7-2.1	256	[56]
Ti/Au	100	1e19	2.44	-	[57]
W	100	2e17	3.0	-	[58]
TiN	80	1e18	1.6	200	[59]

In p-GaN/AlGaN/GaN heterostructure typical thickness of the AlGaN barrier layer is in the range of 10–15nm, while the Al mole fraction is in the order of 15–20%. The active p-GaN doping densities required to deplete the 2DEG at the AlGaN/GaN interface is typically above 10^{18} cm^{-3}. A major limitation of p-GaN E-mode HEMTs is the poor activation efficiency of Mg p-type dopants, which leads to a low hole concentration in the p-GaN layer. This limits the depletion capability over the 2DEG and results in a relatively low or capped threshold voltage. Another major reliability concern in p-GaN HEMTs is the time-dependent breakdown of the AlGaN–p-GaN/metal gate stack, often attributed to avalanche-induced degradation. Additional reliability issues include material defects, back-gate effects, gate leakage, and bias-stress-induced instabilities. Fabrication-related challenges, such as etch-induced damage and the inherent difficulty of simultaneously achieving low on-resistance and high breakdown voltage also represent significant limitations. [60], [61], [62].

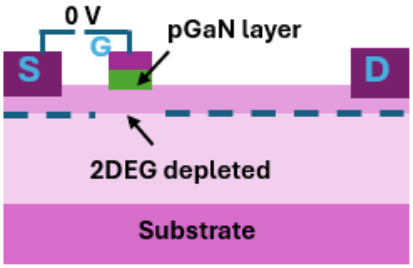


Figure 2. 9 pGaN layer regrown beneath the gate depletes 2DEG at Vgs=0 V.

2.1.4 Reliability issues and degradation mechanisms in lateral GaN HEMTs

Despite the advantages of lateral GaN HEMTs, long-term reliability remains a critical concern, as device performance can degrade under electrical, thermal, and environmental stresses. Understanding the degradation mechanisms is essential for ensuring stable operation in power electronics in harsh-environment applications, enabling the design of a robust GaN devices capable of withstanding real-world operating conditions. This section explores the primary degradation mechanisms that affect device stability over time, including trapping effects, hot electron degradation, gate leakage, and dynamic on-resistance (R_{DSon}) increase. These reliability issues often stem from imperfections in the epitaxial layers, surface states, or defects introduced during fabrication.

2.1.4.1 Dynamic on-resistance

The dynamic R_{ON} is the on-resistance of a GaN HEMT measured immediately after switching from a high OFF-state bias to the ON-state. Following this OFF–ON transition, the resistance is initially elevated due to charge trapping and then gradually relaxes toward its static value. This phenomenon, commonly known as current collapse, is one of the most critical reliability concerns in GaN power devices. It arises from charge trapping at surface states or within buffer layers under high-voltage switching, as illustrated in Figure 2.10, leading to a transient increase in on-resistance. The result are a reduced efficiency, and long-term reliability issues [63], [64], [65].

The electrons captured by these traps are unavailable for conduction when the device switches ON, leading to a temporary increase in on-resistance and a corresponding drop in drain current. The gradual recovery process, known as de-trapping, defines the time scale of current collapse [48], [66], [67].

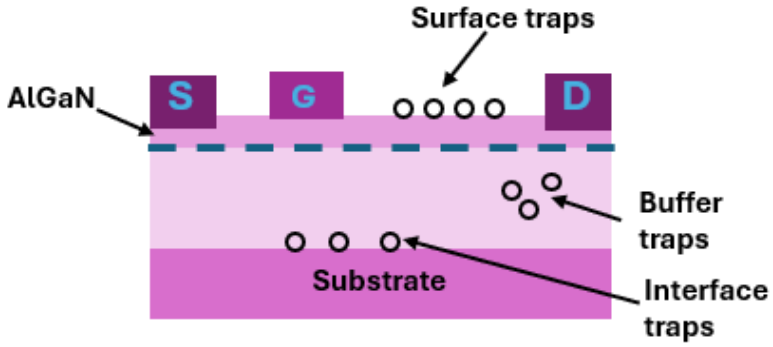


Figure 2. 10 Various trap sites in GaN HEMT

Dynamic on-resistance can be effectively reduced through optimized surface passivation and field plate engineering.

2.1.4.2 High electric field stress

The lateral geometry concentrates high electric fields at the drain-side gate edge, which can induce trap generation, hot electron effects, and eventually lead to gate leakage or premature breakdown. This is mitigated using field plates. It is worth noting that the gate field plate not only enhances breakdown voltage but also suppresses current collapse. By redistributing and reducing the peak electric field at the gate edge, the gate field plate alleviates this trapping effect, thereby mitigating current collapse while simultaneously improving breakdown performance [68].

2.1.4.3 Self-heating effect

GaN devices exhibit high power density, and the relatively low thermal conductivity of substrates such as sapphire or silicon exacerbates localized self-heating. This leads to elevated channel temperatures, accelerating degradation of contacts, metallization layers, and dielectric materials.

2.1.4.4 Hot carrier injection

High-energy electrons accelerated by strong lateral electric fields can affect the AlGaN barrier or create defect states, leading to permanent degradation of mobility and transconductance [69].

2.1.4.5 Gate leakage and instability

Gate stacks (Schottky or MIS structures) are prone to leakage due to tunnelling, trap-assisted conduction, or dielectric breakdown. These instabilities manifest as threshold voltage shifts and increased gate current over time [70].

2.1.4.6 Gate dielectric breakdown (in MIS-HEMTs)

In metal–insulator–semiconductor GaN HEMTs, dielectric reliability is a key challenge. Defects in the insulator or poor interface quality can cause time-dependent dielectric breakdown (TDDB), limiting lifetime [71].

2.1.5. Substrate selection

Substrate selection plays a crucial role in determining the structural integrity and performance of GaN-based devices, including HEMTs. While GaN-on-GaN substrates offer the best lattice and thermal match resulting in low defect densities and superior device performance, their high cost and limited availability make them less practical for large-scale production. Consequently, GaN-on-silicon remains the most widely adopted approach due to its affordability and compatibility with mature silicon fabrication infrastructure. Alternative substrates include sapphire and silicon carbide (SiC), each offering distinct advantages and trade-offs in terms of thermal conductivity, lattice matching, and cost. However, this approach is not without challenges. The significant lattice and thermal expansion mismatches between GaN and foreign substrates introduce a high density of defects, dislocations (Figure 2.11), and cracks in the epitaxial layers. These structural imperfections increase the susceptibility of the device to high vertical electric fields, which can accelerate device breakdown at elevated voltages.

Table 2.2 presents the lattice and thermal mismatches of GaN on commonly used substrates. To address these issues, complex transition and buffer layers (comprising AlN, graded AlGaN, or superlattice) are introduced to relieve mechanical stress and reduce defect propagation from the substrate. These layers, described in the coming sections, serve to enhance electrical isolation and improve breakdown characteristics.

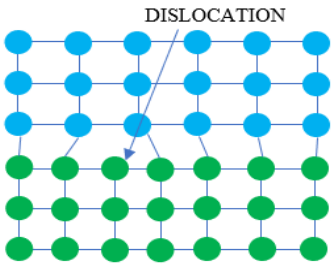


Figure 2. 11 Dislocation due to lattice mismatch.

To reduce the effects of lattice and thermal mismatches in GaN HEMTs, researchers have developed a variety of innovations in epitaxial design, buffer layer engineering, device architecture, growth methodologies, and substrate selection, aiming to balance cost-effectiveness, device performance, and long-term reliability in advanced power and RF applications. Table 2.2 compares the lattice mismatch and thermal mismatches of common substrates used in the manufacture of GaN devices, highlighting the structural and thermal compatibility challenges that influence strain, defect formation, and heat dissipation in GaN-based device operations.

Table 2.2 Lattice and thermal mismatches of GaN on Substrates

Material	Lattice parameters (Å)	Lattice mismatch with GaN	Thermal Conductivity w/m-K	Coefficient of thermal expansion (CTE) (10^{-6} k-1)	Thermal Mismatch
AlN	$a = 3.112$ $c = 4.982$	2.48%	200	4.2	34%
InN	$a = 3.548$ $c = 5.7034$	-10.1%	80	3.8	32%
GaN	$a = 3.1891$ $c = 5.1855$	0%	130	5.59	0%
Sapphire	$a = 4.765$ $c = 12.982$	16%	30	7.5	-23%
SiC	$a = 3.081$ $c = 15.117$	3.51%	490	4.2	30%
Si	$a = 5.431$	-17%	130	3.59	55%

2.1.6 Epitaxial layer optimization for GaN HEMTs

The performance and reliability of GaN HEMT are strongly determined by the quality and design of the epitaxial layers. Careful optimization of the buffer, channel, and barrier structures is essential to improve key parameters such as electron mobility, breakdown voltage, thermal stability, and 2DEG density. Critical factors including dislocation density, interface roughness, polarization effects, and strain management directly influence the electrical characteristics and robustness of the device. Each layer must therefore be precisely engineered to minimize defects, control strain, and maximize electron transport, while maintaining stability under high-power and high-temperature operation. Through such material engineering, trapping effects can be mitigated, dynamic performance enhanced, and overall device lifetime extended.

This section discusses the design of epitaxial layers in GaN HEMTs and how engineering the epitaxial stack enables the realization of high-performance and reliable devices.

2.1.6.1 Nucleation layer

GaN epilayers are typically grown at elevated temperatures > 1000°C using the metal-organic chemical vapour deposition (MOCVD) technique. As the material cools to room temperature, substantial tensile stress (approximately 1 GPa) [72] develops within the film. This stress arises because the CTE mismatch between the foreign substrate (such as Si, Sapphire) being much lower than that of GaN. As a result, if the GaN layer thickness exceeds a few hundred nanometers, the likelihood of cracking increases significantly.

A nucleation layer (NL) is typically deposited between the substrate (such as Si, SiC, or sapphire) and the GaN buffer to facilitate the epitaxial growth of GaN. This layer's main function is to promote the formation of a stable GaN film that minimizes defects and dislocations, which are detrimental to device performance. Due to its excellent thermal stability and ease of use, AlN is commonly employed as the initial buffer layer for growing GaN on some foreign substrates.

2.1.6.2 GaN buffer layer

In GaN power devices, the buffer layer is a thick, semi-insulating epitaxial layer grown between the active GaN channel and the substrate. Its primary function is to electrically isolate the channel from the substrate, suppress vertical leakage currents, accommodate lattice and thermal mismatch, and sustain high electric fields during off-

state operation [73]. In conventional lateral AlGaN/GaN HEMTs, the buffer is commonly doped with deep acceptors such as iron or carbon to increase resistivity and improve breakdown voltage. The thickness of the GaN buffer layer typically 1 to 3 μm, depending on the target breakdown voltage, substrate type, and device architecture [73].

Despite its benefits, the buffer layer is also a major source of reliability and performance limitations, as deep-level traps within the buffer contribute to current collapse, dynamic on-resistance degradation, and threshold voltage instability. Additionally, thick semi-insulating buffers increase epitaxial growth time, cost, and wafer bow, while complicating thermal management due to their relatively low thermal conductivity. These drawbacks have motivated the development of buffer-less (or buffer-free) GaN device designs, in which the conventional semi-insulating buffer is eliminated or significantly thinned.

2.1.6.3 AlGaN barrier layer

The AlGaN barrier layer is essential in forming the 2DEG at the AlGaN/GaN heterointerface. The aluminium composition and thickness of the AlGaN layer determine the 2DEG density, carrier mobility, and overall device performance. Proper control of these parameters is crucial for optimizing HEMTs.

2.1.6.4 GaN cap layer

The GaN cap layer is a thin layer of GaN grown on top of the AlGaN barrier layer in AlGaN/GaN HEMT structure. Though often only a few nanometers thick (typically 1–3 nm), the cap layer plays a vital role in stabilizing device surface properties, enhancing reliability, and improving ohmic contact formation. Its inclusion is particularly important in advanced GaN HEMT designs where surface states and leakage currents critically influence device behaviour. AS AlGaN surface is susceptible to oxidation, the cap layer acts as a barrier that improves chemical stability especially under high humidity and high voltage conditions.

2.1.6.5 Step-graded AlGaN buffer layer

Step graded AlGaN buffer layer (Figure 2.12) is primarily engineered to gradually relax the strain caused by the lattice mismatch between the GaN material and the underlying substrate. The graded composition of AlGaN allows for a smooth transition in both the lattice constant and CTE mismatch between the GaN layer and the substrate. By gradually increasing the aluminium content from the substrate side, the buffer layer

helps relieve strain in a controlled manner, thus reducing the occurrence of dislocations and defects in the GaN buffer and active regions of the HEMT device. This technique improves epitaxial quality and enhances breakdown voltage.

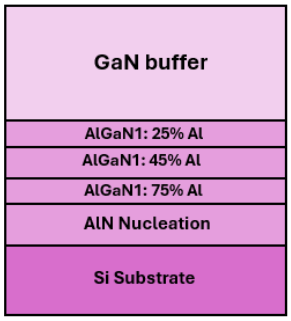


Figure 2. 12 Example of graded AlGaN buffer layer on a Si substrate

2.1.6.7 Passivation layer

The passivation layer serves several essential functions in enhancing the performance of GaN HEMTs, especially in high-power and high-frequency applications. It is a layer of insulating material typically SiNx in AlGaN/GaN HEMT deposited on the surface of the device, to provide an active barrier against moisture, chemical exposure, mechanical damage, and oxidation that can degrade performance and the lifetime of the device. The surface of GaN typically contains trap states that can capture and release charge carriers leading to degradation of electrical performance of the device. Effective surface passivation is essential to neutralize these traps and improve stability and reliability.

2.1.6.8 Iron- and carbon-doped GaN for power electronics

Semi-insulating buffer layers are essential in GaN power devices to suppress leakage current, improve breakdown voltage, and mitigate current collapse under high electric fields. Iron-doped (Fe:GaN) [74] and carbon-doped (C:GaN) [75] materials are the two most widely adopted approaches to achieve high resistivity in GaN epitaxial buffers for power electronic applications. Iron acts as a deep acceptor, compensating unintentional n-type background doping and effectively reducing vertical leakage, which is beneficial for high-voltage operation. However, Fe-related deep traps can introduce memory effects and dynamic instabilities under high-frequency switching [76]. Carbon doping, typically introduced during metal–organic chemical vapor deposition, also creates deep acceptor states and offers improved control over buffer resistivity and electric-field distribution [75]. Compared to Fe-doped buffers, C-doped GaN often exhibits reduced trap-induced dispersion and improved dynamic on-resistance stability, making it increasingly

attractive for both lateral and vertical GaN power devices. Nonetheless, excessive carbon incorporation can lead to increased trapping and reliability trade-offs, requiring careful optimization of doping concentration and layer thickness [77].

2.2 GaN-based Vertical Transistors

Unlike lateral device architectures where current flows parallel to the wafer surface, vertical devices conduct current perpendicularly, from the drain to the source. In this configuration, the source and gate electrodes are typically located on the top surface of the wafer, while the drain electrode is positioned on the bottom side.

Several vertical GaN transistor architectures have been proposed and demonstrated in the literature, each offering unique advantages for high-performance power applications. Notable design geometries include the Current Aperture Vertical Electron Transistor (CAVET), Trench Metal-Oxide-Semiconductor Field-Effect Transistor (Trench-MOSFET), Fin Field-Effect Transistor (FinFET), Junction Field-Effect Transistor (JFET), and the in-situ Oxide GaN Interlayer-Based Vertical MOSFET (OG-FET). These device structures summarised in the following sections.

2.2.1 Current aperture vertical electron transistor (CAVETs)

CAVET design was first reported by Ben-Yaacov *et al*. [78] in 2004. The primary motivation behind this architecture was to mitigate the detrimental effects of large surface electric fields at the gate's drain-side edge, which limited the high-voltage performance of lateral HEMTs. Since its inception, numerous CAVET-based design variations have been proposed [78].

The basic structure shown in Figure 2.14 which comprises of an intentionally doped-GaN layer grown on substrate followed by implantation of two adjacent (Mg-doped) p-GaN or (Fe-doped) insulation layers creating an aperture with an undoped GaN layer grown on the top. These implanted regions define a narrow undoped region known as the current aperture (where current can flow between the drain and the source as shown in Figure 2.15), above which an undoped GaN channel layer is subsequently grown. The implanted regions are now commonly referred to as the Current Barrier Layer (CBL). Their

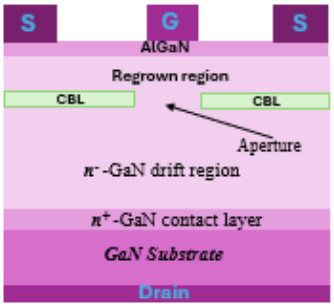


Figure 2. 13 Cross sectional view of GaN CAVET showing the main device layers.

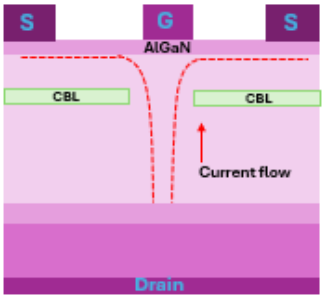


Figure 2. 14 Current Flow Path in Vertical GaN Current Aperture Vertical Electron Transistor (CAVET)

primary function is to confine current conduction to the aperture region directly beneath the gate. A thin AlGaN barrier layer is subsequently grown atop the undoped GaN channel for the formation of 2DEG at the AlGaN/GaN interface. The gate modulates electron flow through this confined aperture, enabling vertical conduction from the channel into the drift region, thereby achieving controlled current flow.

CAVETs require epitaxial regrowth that increases the complexity and fabrication cost and owing to the polarization in AlGaN/GaN heterojunction, it is difficult to realize a normally off CAVET with a reasonable normally-off threshold voltage. For fail-safe power switching applications, devices with reasonable thresholds of 3-5 V [79] are required and that could easily be significantly achieved with other design topologies such as MOSFET, discussed in the next section.

2.2.2 Trench MOSFET and OG-FET

The first enhancement mode vertical GaN trench MOSFET was demonstrated in 2007 by H. Otake *et al.* [80] schematically shown in Figure 2.16. The device consists of four layers grown on sapphire substrate by low pressure metal organic vapor phase epitaxy (MOVPE). The layers were silicon doped 0.5 μm n^+-GaN drain layer, 0.1 μm n^-GaN drift, 0.5 μm n^+-

GaN source layer and 0.6 µm Mg-doped p-GaN for the channel. A trench gate width of 560 µm made from Ni/Au (10/125) was deposited between the source and drain. Using two different gate dielectrics, SiO_2/Si_xN_y and SiO_2 applied separately, a threshold voltage of 25.5 V and 5.1 V were respectively observed and with a channel mobility of 133 cm^2/Vs. Fully vertical GaN trench MOSFET on GaN substrate was demonstrated in 2008 by H. Otake *et al* [81] upon which similar threshold voltages as reported with sapphire substrate were obtained. Various vertical GaN based trench MOSFETs achieving very high voltages through appropriate design of the thickness of the drift layer, doping concentration, high quality GaN substrate, modification in the geometry of the device structure or modified growth technique, were reported [82][83], [84].

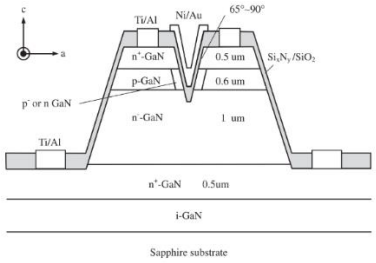


Figure 2. 15 Schematic of trench-MOSFET [80]

Although the vertical GaN trench MOSFETs were demonstrated to have high breakdown and reasonable threshold voltages, they have poor electron mobility [85] in the p-GaN channel resulting in very high on-resistance which is a critical drawback in high power applications. Another issue is the difficulty of the source electrodes to form good ohmic contacts with the buried p-GaN channel layer causing the threshold voltage to shift negatively at high drain biases [86], [87].

To improve the channel conductivity and reduce on-resistance of the conventional trench MOSFET, an Oxide-GaN trench MOSFETs (OG-FETs) structure was introduced [85], [88], [89]. In 2016, C. Gupta *et al*. [90] reported a novel OG-FET structure of vertical trench MOSFET. In the conventional trench MOSFET structure, gate dielectric is deposited on the trench structure and the current flows from source to drain through the p-GaN inversion layer at the dielectric/p-GaN interface which results in the poor mobility and high on-resistance. In the improved structure with sapphire substrate shown in Figure 2.17, an MOCVD-regrown GaN interlayer was inserted between the n-p-n trenched

structure and the dielectric which yielded a significant reduction of on-resistance ($3.8 m\Omega cm^2$) compared to the similar devices demonstrated without the interlayer.

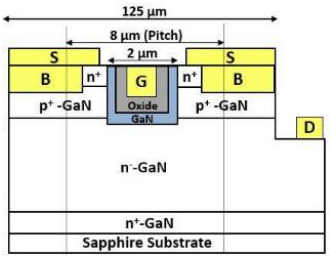


Figure 2. 16 Schematic of OG-FET [90]

2.2.3 Fin field effect transistors (Fin-FETs)

To address some of the limitations associated with conventional GaN vertical devices—such as CAVETs and trench-based MOSFET structures—GaN FinFET architectures have been proposed and demonstrated.. Depending on how many sides of the fin are electrostatically controlled by the gate, GaN FinFETs can be implemented in dual-gate, tri-gate, or gate-all-around configurations, enabling stronger gate control and reduced short-channel effects compared to planar structures. [91], [92]. FinFETs offer key advantages over trench MOSFETs and CAVETs because they avoid material regrowth steps and do not rely on a p-GaN layer to achieve normally-off operation. The device was first introduced by Sun *et al.* [87] in 2017, and consisted entirely of GaN epitaxial layers. The structure included an n^+-GaN layer (0.2 µm, Si: 2×10^{18} cm^{-3}) grown on a 2-inch bulk GaN substrate, an n-GaN drift region (8 µm, Si: 2×10^{16} cm^{-3}), and an n^+-GaN cap layer (0.3 µm, Si:$4\times10^{18}cm^{-3}$), as illustrated in Figure 2.18.

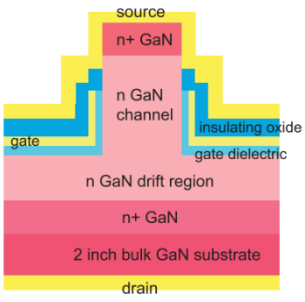


Figure 2. 17 Schematic of Vertical GaN Fin-FET [87].

To achieve normally-off operation, the width of the vertical fin channel enclosed by the gate metal must be scaled to the submicron regime. The gate region comprises a dielectric–metal stack formed along the fin sidewalls, while the source and drain electrodes are located at opposite ends of the device—the source making an ohmic

contact to the n^+-GaN cap layer at the top, and the drain connected through the bottom of the substrate. Due to the work-function difference between GaN and the gate metal, electrons in the vertical fin channel are depleted V_{GS}=0, resulting in normally-off behavior. When a positive gate bias is applied, the depletion width reduces, allowing a conduction channel to form within the fin.

The fabricated device demonstrated promising performance, achieving R_{ON} of 0.38 mΩ·cm^2, a threshold voltage (V_{th}) of 1 V, and a breakdown voltage (V_{BV}) of 800 V for a fin width of 450 nm. Further improvements in wafer design, electric-field management, and ohmic-contact processing, reported later in 2017 by the same research group, enhanced the device performance even more, reducing R_{ON} to 0.2 mΩ·cm^2, maintaining V_{th} at 1 V, and increasing V_{BR} to 1200 V. [93]. n 2019, the device structure was further modified to study the impact of capacitances, charge distribution, and power-switching figures of merit (FOMs). The updated device featured an active area of 0.23 mm^2 and a total footprint of 0.45 mm^2 including pads (Figure 2.19). Argon-implant edge termination was introduced beneath the gate-pad edges to improve electric-field distribution and switching behavior [94]. These modifications resulted in improved performance metrics, including an R_{ON} of 2.1 mΩ·cm^2, a threshold voltage of 1.3 V at a drain current of 2 mA, and a breakdown voltage of 1200 V [70]. The device delivered a drain current of 5 A at an on-state resistance of 0.9 Ω, and its switching speed was estimated to be approximately 3.5 MHz.

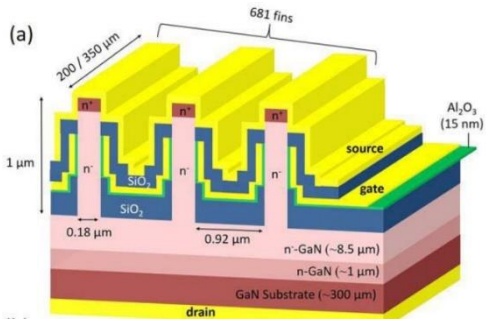


Figure 2. 18 Cross-sectional view and 3D view of GaN vertical Fin-FET demonstrated by [93]

Despite the remarkable performance, the device did not achieve commercial adoption, primarily due to the high substrate cost (estimated at $50–$100 per cm^2) and the limited wafer size (2-inch) [93]. To address this limitation, A. Zubair *et al.* demonstrated a GaN

vertical power FinFET fabricated on a Quasi-Substrate Technology (QST)-engineered substrate with a matched thermal expansion coefficient (TEC), enabling the realization of high-power yet low-cost vertical GaN devices [95]. The device structure comprised a 2-µm drift layer (N_D=$10^{17}cm^{-2}$), 0.1µm channel layer (N_D=$2x10^{17}cm^{-}2$) and 0.1µm source layer (N_D=$10^{19}cm^{-}2$), epitaxially grown on the substrate by MOCVD. The device exhibited excellent performance, achieving of R_{on} =2.1 mΩcm^2, V_{th} =1.5V, V_{BV} =1200V and drain current of 5A were reported. A schematic illustration of the GaN vertical power FinFET on the QST-engineered substrate is shown in Figure 2.20.

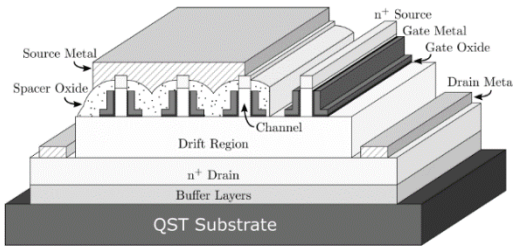


Figure 2. 19 Schematic of vertical GaN Fin-FET on Engineered substrate [95]

Several normally off FinFET devices with voltages up to 1.2 kV were reported in the literature [96], [97], [98]. More recently, an ultra-wide bandgap based Ga_2O_3 power Fin-FETs have been reported with a V_{BR} exceeding 1kV [99], 1.6 kV[100], and 2.6kV [101].

2.3 Advancing GaN Transistor Technology for High-Power Applications

High-power electronic systems demand devices capable of sustaining high breakdown voltages in the kilovolt range, large current densities, and simultaneously maintaining very low on-state resistance [102], [103]. At present, most commercially available GaN power transistors are limited to around 650 V, primarily based on lateral GaN HEMT technology. While research prototypes have achieved breakdown voltages exceeding 1700 V [104], they remain off-market due to challenges in reliability, fabrication complexity, and cost. This gap underscores the pressing need for ongoing researches to advance GaN devices with higher voltage and current capabilities, alongside improvements in reliability, manufacturability, and cost-effectiveness.

Lateral GaN devices, particularly HEMTs, have demonstrated remarkable performance due to their high-mobility 2DEG channel, which enables low R_{ON} and high switching speeds. However, their suitability for high-power applications is limited by several

intrinsic constraints. Achieving breakdown voltages above 1 kV requires increased gate-to-drain spacing, which inherently raises R_{ON}. Maintaining low R_{ON} under these conditions necessitates wider device structures, resulting in bulky designs. Additionally, the lateral geometry positions the active region near the surface, complicating electric-field management and making devices prone to dynamic on-resistance effects, such as current collapse. While passivation layers and complex field-plate structures can mitigate these effects, they introduce additional parasitic capacitances and increase fabrication complexity.

Threshold voltage (V_{th}) presents another challenge. In power applications such as automotive electronics, robust operation typically requires threshold voltages greater than 3–5 V. Lateral GaN HEMTs, however, V_{th} is typically under 1.5 V. Moreover, they lack avalanche breakdown capability since they do not incorporate bulk p–n junctions. This limitation requires designers to introduce wide safety margins above the rated voltage to prevent destructive breakdown, which increases cost and reduces efficiency. Thermal management is also problematic, as current in lateral HEMTs flows through narrow surface channels, leading to localized hotspots that degrade reliability at high current densities. For these reasons, lateral GaN HEMTs are generally better suited for low- to mid-power applications.

Vertical GaN devices, by contrast, address many of these shortcomings. By carefully designing drift regions with appropriate doping density and thickness, vertical structures can sustain blocking voltages well above 1 kV and handle large currents without significant increases in R_{ON}. Because voltage blocking occurs within the bulk material, electric fields are more evenly distributed, reducing susceptibility to dynamic R_{DSON}. Current conduction through the bulk also provides a more uniform path for heat dissipation, significantly improving thermal management. Vertical device architectures further offer greater flexibility in achieving normally-off operation, with threshold voltages in the range of 2–7 V demonstrated in devices such as trench-MOSFETs and FinFETs. Literature reports vertical GaN devices with operating voltages exceeding 1.2 kV and achieving higher current densities [54], [58], [105].

Several vertical GaN transistor designs have been discussed previously. Among these emerging architectures, vertical GaN FinFETs have demonstrated the greatest potential.

The architecture combines high breakdown voltage, low on-resistance, and excellent thermal performance. Early prototypes achieved breakdown voltages around 800 V with on-resistances as low as 0.38 $m\Omega \cdot cm^2$ [87], and subsequent demonstrations have pushed performance beyond 1200 V, with switching frequencies above 3 MHz and high Baliga's figure of merit (BFOM) [106].

Table 2.3 shows the performance data of various vertical GaN devices including the Baliga's Figure of Merit (BFOM). The results clearly indicate that FinFET consistently demonstrate the highest BFOM values among all device types. For instance, a GaN FinFET reported in 2017 achieved a BFOM of 7.2 GW/cm^2 [107], while a later demonstration on a Ga_2O_3 substrate reached an extraordinary 280 GW/cm^2 [101], far surpassing other device designs. These values illustrate the FinFET's ability to combine high breakdown voltages with extremely low on-resistance.

In contrast, CAVETs, while capable of achieving high breakdown voltages above 1 kV, generally exhibit lower BFOM values (typically around 0.3–1.0 GW/cm^2). This limitation arises from higher on-resistance and fabrication complexities associated with p-GaN layers and regrowth processes.

Trench FETs occupy an intermediate position, with BFOM values generally below those of FinFETs. While some trench structures report BFOMs close to 2–3 GW/cm^2 (e.g., 2.89 GW/cm^2 for a V-groove FET in 2016), most remain significantly below FinFET benchmarks, reflecting challenges in achieving both low R_{ON} and high blocking voltage simultaneously. Overall, the figure of merit comparison underscores that, while CAVETs and trench FETs provide useful demonstrations of vertical GaN capability, FinFETs dominate in performance. Their exceptionally high BFOM values confirm their strong potential as the most promising architecture for next-generation, high-power GaN devices.

Despite these advances, challenges remain with the state of the art GaN FinFETs. Electron transport in the fin sidewalls is less efficient than in the drift region, limiting mobility and increasing R_{ON}. Large gate areas introduce high parasitic capacitances, and long-term reliability issues, including dielectric breakdown and gate oxide robustness, remain active areas of research. Long-term reliability issues remain, including dielectric breakdown, gate-oxide degradation, and charge trapping, which can shift threshold

voltage over time. FinFET structures require precise nanoscale etching and conformal gate deposition, increasing manufacturing difficulty and cost.

Table 2.3 Performance comparison of various vertical GaN transistor structures.

Device type	Substrate	V_{BR}(V)	$R_{on,sp}$ (Ωcm^2)	V_{th}(V)	$N_{D,drf}$ (cm^{-3})	t_{drf} (μm)	Growth Method	V^2_{BR}/R_{ON} (GW/cm^2)	Year	Ref
VHFET	GaN	672	7.6	-1.1	7e15	5	MOVPE		2010	[108]
CAVET	GaN	500	0.37	-	-	3	MOCVD	0.68	2014	[109]
CAVET	GaN	1500	2.2	0.5	1e16	15	MOCVD	1.0	2014	[110]
CAVET	GaN	20	0.4	-7	NA	3		-	2015	
VC-JFET	GaN	1260	5.2	0.8	1e16	11	MOCVD	0.31	2015	[111]
LC-JFET	GaN	1320	1.7	1.0	1e16	11	MOCVD	1.0	2015	[111]
Trench FET	GaN	1200	1.8	3.5	9e15	13	-	0.8	2015	[82]
V-Groove	GaN	1700	1.0	2.5	1e16	13	MOCVD	2.89	2016	[112]
Trench FET	GaN	1200	3.4	-	8e15	13	MOCVD	0.42	2016	[113]
Trench FET	GaN	600	1.7	4.8	2e16	8	MOCVD		2016	[86]
Trench FET	GaN	600	0.97	3.0	6e16	8	MOCVD	0.37	2016	[114]
VFET	GaN	450	0.84	0.5	2e16	8	-	0.24	2016	[115]
Trench FET	GaN	450	0.47	4.0	5e18	10	TCAD-SIM	0.43	2016	[115]
OG-FET	GaN	990	2.6	0.8	1e16	8	MBE	0.38	2017	[88]
FinFET	GaN	800	0.36	1.0	2e16	8	MOCVD	1.8	2017	[87]
V-Trench	GaN	600	0.3	16	2e16	8	MBE	-	2017	[105]
FinFET	GaN	1200	0.2	1.0	3e15	7	MOCVD	7.2	2017	[116]
OG-FET	GaN	320	4.4	1.0	8e15	10	MOCVD	0.02	2017	[89]
OG-FET	GaN	1400	2.2	4.7	5e15	15	MOCVD	0.89	2017	[117]
Fin-MISFET	GaN	513	0.4	-	6e15	7	MOCVD	0.66	2017	[118]
OG-FET	GaN	700	0.98	2.5	9e15	10	MOCVD	0.5	2018	[119]
CAVET	GaN	880	2.7	0.1	5e15	15	MOCVD	0.29	2018	[120]
Trench FET	Silicon (111)	645	6.8	3.3	2e16	4	MOCVD	0.06	2018	[121]
MISFET	Ga_2O_3 (001)	1057	18	2.2	2e16	10	HVPE	0.06	2018	[98]
VC-JFET	GaN	600	6.4	0.8	10e16	11	TCAD-SIM	0.056	2018	[122]
FinFET	GaN	1200	2.1	1.3	4e15	9.5	MOCVD	0.69	2019	[123]
FinFET	Ga_2O_3 (001)	2660	25.2	>1.5	2e15	10	HVPE	280	2019	[124]
FinFET	E-Substrate	1200	-	-	1e17	2	MOCVD	-	2020	[125]

Figure 2.21 presents a comparison of breakdown voltage (BV) versus threshold voltage (V_{th}) for different GaN device architectures, namely MOSFETs (grey), CAVETs (yellow), and FinFET (blue), reported in the literature. From the distribution of points, most devices cluster around threshold voltages between 0 and 3 V, with breakdown voltages spanning

a wide range from a few hundred volts up to nearly 2800 V. MOSFETs (grey) are spread broadly, with several devices achieving breakdown voltages exceeding 1500 V, though their threshold voltages vary widely. Some MOSFETs even operate with negative threshold voltages, indicating normally-on behaviour, which is less desirable for fail-safe power applications. CAVETs (yellow) show similar trends, with high breakdown voltages above 1 kV but threshold voltages often at or below zero. The negative V_{th} values highlight the challenge of achieving robust normally-off operation in CAVET architectures, despite their strong blocking capability. FinFET (blue) exhibit a more compact distribution, with breakdown voltages ranging from around 600 V to over 1600 V, while maintaining positive threshold voltages close to 1–3 V. This demonstrates their ability to combine high breakdown voltage with desirable normally-off behaviour, making them attractive candidates for high-power applications.

Overall, the chart illustrates the trade-off between threshold voltage and breakdown strength in various types of GaN device. While MOSFETs and CAVETs can achieve higher breakdown voltages, they often face challenges with on-resistance and threshold voltage respectively. FinFET, by contrast, demonstrates a better balance between BV and V_{th}, and exceptionally, an on-resistance, supporting their potential as the most promising vertical GaN architecture for next-generation power devices.

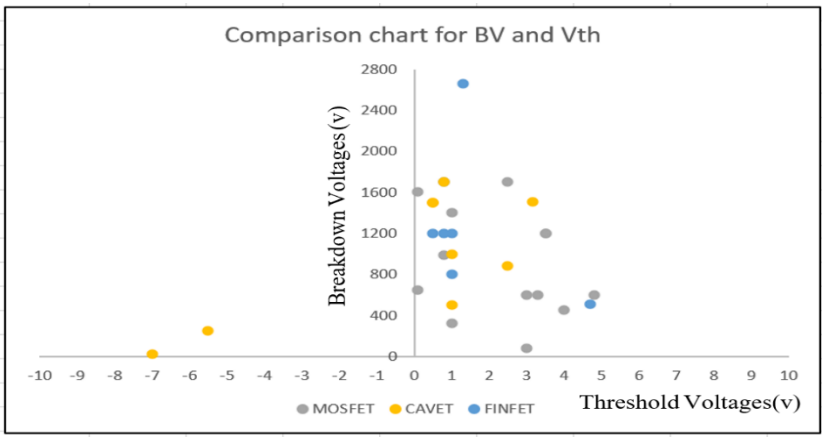


Figure 2.21 Breakdown Voltage vs. Threshold Voltage Characteristics of Different GaN Device Architectures

2.5 Commercial GaN Technologies

Commercial gallium nitride (GaN) technologies have matured significantly in recent years and are now widely adopted in power electronics and high-frequency applications.

Commercial GaN devices for power electronic applications are typically implemented as enhancement-mode high-electron-mobility transistors (e-mode HEMTs) and are currently available in voltage classes ranging from approximately 100 V to 650 V (table 2.4), and in rare cases up to 900 V (table 2.4). These devices are used in applications such as fast chargers, data-center power supplies, power converters, and electric-vehicle onboard chargers. Several semiconductor manufacturers have successfully commercialized GaN power devices, including Infineon Technologies (CoolGaN series), Navitas Semiconductor (GaNFast power ICs), Efficient Power Conversion (EPC eGaN FETs), GaN Systems, Transphorm, and Texas Instruments. Table 2.2 presents selected devices currently available from some of these manufacturers. Many of these devices are fabricated using GaN-on-silicon (GaN-on-Si) technology, which enables cost-effective large-scale manufacturing on silicon wafers [126].

Table 2.4. Commercially Available GaN Power Transistors

Manufacturer	**Part No.**	**R_{ON} (mΩ)**	**Voltage (V)**	**Ref**
Efficient Power Conversion (EPC)	EPC2034C	8	200	[127]
Efficient Power Conversion (EPC)	EPC2218	~3.2	100	[128]
GaN Systems	GS66508T	50	650	[129]
Transphorm	TP65H050WS	50	650	[130]
Transphorm	TP90H180PS	180	900	[131]
Infineon Technologies	IGO60R070D1	70	600	[132]

2.6 Summary

This chapter reviewed the fundamental device architectures, operating principles, and technological challenges of GaN-based power transistors. It began with an introduction to lateral GaN HEMTs, describing the formation of the 2DEG, their basic operation, and the various methods used to achieve enhancement-mode behaviour, including cascode configuration, recessed gate, fluorine implantation, and p-GaN gate techniques. Reliability issues such as dynamic on-resistance, hot-carrier effects, gate leakage, and dielectric breakdown were discussed alongside strategies for epitaxial layer optimization and substrate selection to improve device performance.

The discussion then moved to vertical GaN power devices, covering CAVETs, trench MOSFETs, and vertical FinFET, with emphasis on their ability to support higher breakdown voltages and improved scalability compared to lateral devices. Design considerations for

the fin (of FinFET) and drift regions were highlighted, as well as recent innovations aimed at enhancing electrostatic control and reducing conduction losses.

Overall, the chapter established a comparative perspective on GaN device technologies, showing the distinction between lateral and vertical architectures, the challenges in achieving reliable normally-off operation, and the potential of vertical FinFET as a pathway toward next-generation high-power GaN electronics.

Chapter 3

Overview of Fabrication and Characterization Techniques of GaN Transistors

The fabrication of GaN devices relies on a diverse set of sophisticated tools designed to precisely manipulate materials at the micro- and nanoscale. These tools enable critical process steps such as lithography, etching, deposition, and thermal treatment, each contributing to the formation of high-performance semiconductor structures. Lithography systems, including photolithography and electron beam lithography, are used to define device patterns with high accuracy. Etching tools such as inductively coupled plasma (ICP) and reactive ion etching (RIE) enable controlled material removal with high anisotropy and selectivity. Deposition tools, including metal evaporation and chemical vapor deposition systems, facilitate the growth of thin films and metal contacts. Additionally, annealing furnaces and rapid thermal processing units are employed for alloying ohmic contacts, dopant activation and stress relief. The integration and precise control of these fabrication tools are essential for achieving the desired device geometries and electrical characteristics, forming the foundation of successful GaN device manufacturing. All fabrications in this project were carried out in the James Watt Nanofabrication Centre (JWNC) of the University of Glasgow.

After fabrication, characterization of semiconductor devices is carried out to evaluate their electrical, physical, and reliability performance and to verify compliance with design specifications. This process involves measuring key parameters such as current–voltage (I–V) characteristics, capacitance–voltage (C–V) behavior, threshold voltage, leakage current, gain, and switching speed. Characterization helps identify fabrication defects, assess process consistency, and ensure that the devices will operate reliably under intended operating conditions.

3.1 Fabrication Techniques

3.1.1 Epitaxial material growth

Epitaxy is a crystal growth technique in which a thin film is deposited on a single-crystal substrate, and the film's crystal structure is aligned with that of the substrate. Epitaxial growth is a fundamental initial step in the fabrication of GaN devices, involving the growth of high-quality crystalline layers on the prepared substrate. The most used epitaxial techniques for GaN devices are Metal-Organic Chemical Vapor Deposition (MOCVD) and Molecular Beam Epitaxy (MBE), each offering unique advantages in terms of layer control, uniformity, and scalability.

During epitaxial growth, precursor gases or elemental sources are introduced into a reactor chamber under precisely controlled temperature, pressure, and ambient conditions. These parameters influence the crystalline quality, thickness, doping profiles, and interface sharpness of the GaN layers. Typically, the growth starts with a low-temperature nucleation layer to improve adhesion and accommodate lattice mismatch between the substrate and the GaN layer, followed by a high-temperature buffer and the active device layers, such as undoped GaN, AlGaN barrier layers, and doped layers for source, drain, and gate regions.

The epitaxial growth process also involves in-situ monitoring techniques, such as reflectometry or pyrometry, to ensure uniformity and reproducibility. Precise control over doping concentration during growth enables the tailoring of electrical properties essential for device operation. High-quality epitaxial layers exhibit low dislocation densities and smooth surfaces, which are crucial for minimizing leakage currents and enhancing device reliability.

3.1.2 Lithographic processes

Lithography involves the transfer of geometric patterns onto a substrate and is a critical step in device fabrication. It serves as the foundation for both micro- and nanofabrication in semiconductor manufacturing. The two primary lithographic techniques are optical lithography, commonly referred to as photolithography, and electron beam lithography (e-beam lithography). Photolithography is widely used due to its simplicity, speed, and cost-effectiveness, and offers alignment precision around 1 μm, making it suitable for

fabricating features as small as 1 μm. In contrast, e-beam lithography provides much higher resolution, with alignment accuracy reaching 0.5 nm and the capability to define features as small as 3 nm. However, it is significantly slower, more costly, and involves more intricate processing steps compared to photolithography. Photolithography was the primary patterning technique used in the fabrication of the lateral GaN devices, whereas electron beam lithography (EBL) was employed for the fabrication of the vertical GaN Fin structures described in Chapters 4 and 6 respectively.

3.1.2.1 Photolithography

Photolithography operates by transferring a geometric mask pattern onto a light-sensitive photoresist layer through ultraviolet (UV) light exposure. The process begins with the uniform spin-coating of photoresist onto the wafer surface, followed by a soft bake to remove solvents and improve adhesion. A photomask containing the desired pattern is then aligned over the wafer, and UV light is projected through the mask to selectively expose the photoresist.

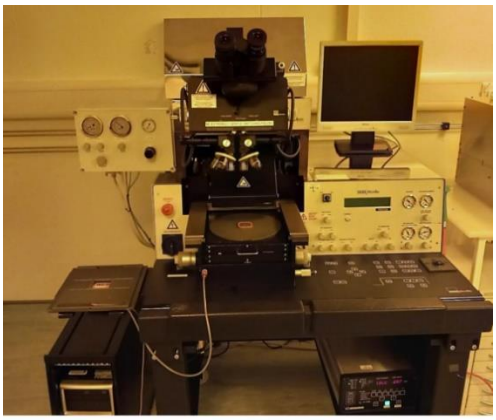


Figure 3. 1 Suss Mask Aligner (MA6) in JWNC for photolithographic patterning

Depending on the type of photoresist used – positive or negative – the exposed or unexposed regions become soluble during the subsequent development step, revealing the intended pattern. The resulting photoresist pattern serves as a mask for subsequent processing steps such as etching or metallisation. Critical process parameters such as exposure time, alignment accuracy, and development time must be carefully optimized to achieve high-resolution pattern transfer. Photolithography remains a key enabling technology in GaN device fabrication due to its scalability, precision, and compatibility with various material systems and device architectures. The required UV exposure time

varies depending on the thickness and type of the photoresist, as it influences how effectively the light penetrates the resist layer.

In this project, UV exposure was carried out using a SUSS Mask Aligner (MA6), shown in Figure 3.1, which operates at a wavelength of 365 nm. The tool supports six different mask-to-substrate contact modes: proximity, soft, hard, low vacuum, vacuum, and flood exposure. In proximity contact mode, a predefined gap is maintained between the mask and the substrate. While this reduces the risk of mask damage, it comes at the cost of lower resolution—typically around 2.5 µm. Soft contact mode applies gentle mechanical pressure to bring the mask and substrate into contact, improving the resolution to approximately 1 µm. Hard contact mode uses increased pressure, further enhancing resolution to 1 µm.

In both low vacuum and vacuum contact modes, the air gap between the mask and substrate is evacuated to improve contact uniformity. These modes offer the highest resolution, achieving features as small as ~1 µm. The processes of resist exposure for pattern definition and substrate etching are illustrated in figure 3.2.

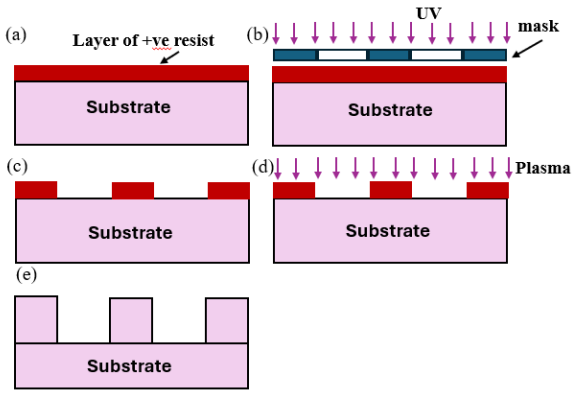


Figure 3.2 Lithographic process flow from resist coating to pattern transfer

(a) Resist coating

A thin layer of resist is spin-coated onto the surface of a clean wafer. This forms a uniform coating that will be used to define micro-scale features.

(b) Exposure

The resist is selectively exposed to UV light through a hard-mask, or electron beams lithography, which defines the desired pattern. Depending on whether the resist is positive or negative, the exposed or unexposed areas will become soluble in the developer.

(c) Development

The wafer is then developed using a chemical developer solution, which removes the exposed (or unexposed) regions of the resist depending on the resist tone, revealing the patterned areas of the wafer beneath.

(d) Etching

With the remaining resist acting as a mask, the wafer is subjected to selective etching, which removes material from the exposed areas of the wafer.

(e) Resist removal

After etching, the resist is stripped, leaving behind the final patterned features on the wafer.

3.1.2.2 Electron beam lithography

E-beam lithography uses a focused beam of high-energy electrons to directly write patterns onto an electron-sensitive resist layer, typically polymethyl methacrylate (PMMA), without the need for a physical mask. The electron beam scans across the substrate in a raster or vector fashion, locally modifying the solubility of the resist depending on exposure dose and resist chemistry. After exposure, the wafer undergoes a development process where the exposed or unexposed regions of the resist are selectively removed, depending on whether a positive or negative resist is used. This process enables feature definition down to the nanometre scale, often below 10 nm, with extremely high alignment precision. Figure 3.3 shows an image of Raith 100 kV EBPG 5200 electron beam lithography tool used in the JWNC.

Figure 3. 3 An image of Raith 100 kV EBPG 5200 electron beam lithography tool in the JWNC

The column is the central component of an e-beam lithography system, where the electron beam used for pattern writing is generated, as shown in Figure 3.4. Positioned at

the top of the column is the electron gun, typically a thermionic or field emission source engineered specifically for e-beam lithography. The emitted electron beam is guided through a series of magnetic condenser lenses, which focus and shape the beam. By adjusting the magnetic field strength of these lenses, the beam current, typically between 1 nA and 100 nA, can be precisely controlled to meet the desired exposure conditions. The focused beam then passes through deflection coils, which steer it across the writing field. These coils can deflect the beam by approximately 1 mm, though this range is constrained by aberration limitations. To write over larger areas, the sample stage is moved mechanically. Consequently, large patterns are divided into smaller regions known as fields, with each field exposed sequentially. The stage incorporates a high-precision interferometer with sub-nanometre resolution, allowing for system calibration and alignment with positioning accuracy better than 1 nm.

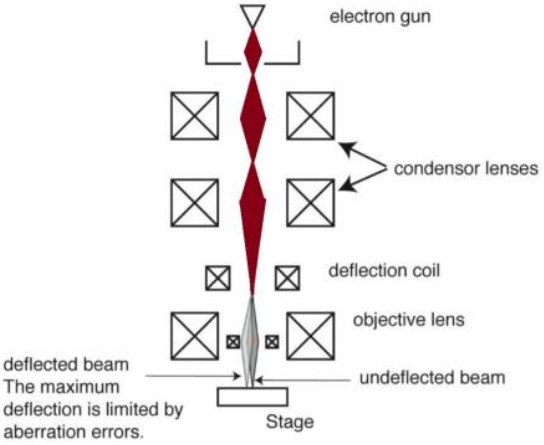


Figure 3.4 Schematic illustration of the column in an electron beam lithography (EBL) system, showing key components such as the electron gun, magnetic condenser lenses, deflection coils, and sample stage [133].

3.1.2.3 Mask design for lithographic processes

The design and preparation of photo and e-beam masks are critical steps that define the geometry of device features and determine the spatial precision of the fabrication process. In this stage, the intended device structures, such as contacts, gate fingers, isolation mesas, and alignment marks etc, are laid out using specialized CAD software compatible with the lithography system in use. The layout must conform to the resolution, overlay, and feature density constraints of the chosen lithographic technique.

For photolithography, masks are typically designed to accommodate micron-scale features, with minimum critical dimensions generally around 2 μm. The photomask is a high-resolution chrome-on-glass template that contains the positive or negative image of the pattern to be transferred onto the photoresist-coated substrate. Multiple levels are created corresponding to different fabrication steps, such as etching and metallization, with strict alignment tolerances between successive masks.

E-beam lithography masks, or more precisely, direct-write e-beam exposures, require a different design paradigm. Because of the sub-micron and even nanometre resolution capabilities of e-beam lithography, the layout must be optimized for proximity effect correction and writing time efficiency. Unlike photomasks, e-beam systems can directly write patterns without the need for physical masks, but the design still follows hierarchical and rule-based structures.

In this project, the LEDiT software platform was used to design the mask layouts for both photolithography and e-beam lithography. For the photolithography, photomasks were fabricated by Compugraphics. Both photo and e-beam mask designs must include alignment marks to ensure accurate layer-to-layer registration during the lithography sequence. Design verification, and layout-versus-schematic (LVS) checks, are typically conducted prior to mask generation to avoid process errors. The finalized layout is then exported in standard formats such as GDSII or OASIS and submitted for mask writing or direct patterning, forming the blueprint for all subsequent fabrication steps.

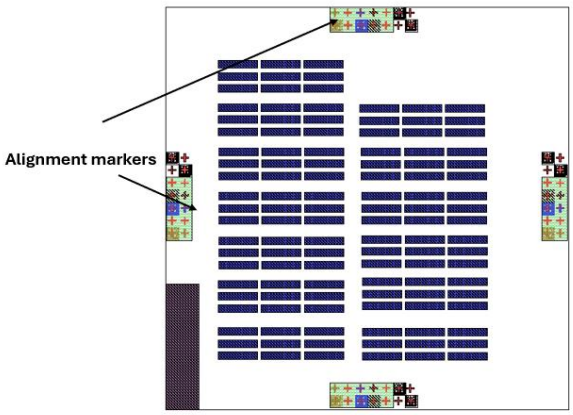


Figure 3.5 Layout of a 10 × 10 mm cell with patterns alignment makers designed in L-Edit.

Figure 3.5 presents a 10 × 10 mm cell layout designed in L-Edit, highlighting the patterned structures and strategically placed alignment markers for accurate layer registration,

while Figure 3.6 illustrates different marker configurations demonstrating proper alignment as well as translational and rotational misalignments.

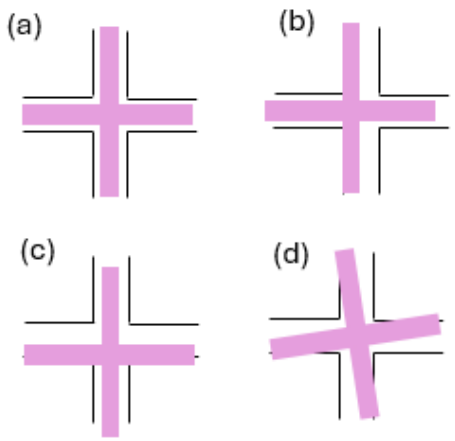


Figure 3.6 showing (a) properly aligned marker (b) Translational misalignment along x-axis (c) Translational misalignment along Y-axis and (d) Rotational misalignment.

3.1.3 Dry etching

Inductively Coupled Plasma (ICP) is a key anisotropic dry etching technique employed for pattern transfer in GaN device fabrication. In this step, material is selectively removed from the substrate in defined areas, such as the isolation mesas or active regions, based on the lithographically patterned resist or hard mask. ICP combines high plasma density generated by an inductively coupled source with independent RF biasing on the substrate, providing precise control over etch anisotropy, depth, and selectivity. Etch depth is a critical parameter determined by both the device design and the underlying layer structure. In GaN-based devices, for instance, etching down to a specified layer, such as the GaN buffer, AlGaN barrier, or a specific heterojunction interface, is essential for achieving proper isolation and device functionality. The depth is typically monitored through time-based etching, in-situ end-point detection, or profilometry after processing.

In this work, the dry etching process for our vertical GaN-based structures was carried out using an ICP etcher employing a BCl_3/Cl_2 gas mixture with flow rates of 25 sccm and 15 sccm, respectively. The process was optimized at an ICP power of 500 W and a platen (bias) power of 105 W, under a chamber pressure of 5 mTorr. The substrate temperature was maintained at 10 °C, with helium backside cooling pressure of 10 Torr to ensure uniform temperature control and prevent thermal damage. This recipe provided stable

plasma conditions with anisotropic profiles suitable for device fabrication, yielding an etch rate of approximately 100 nm per second.

Selectivity refers to the ratio of the etch rate of the target material (e.g., GaN) to that of the masking material (e.g., SiO_2, photoresist, or Ni). High selectivity is crucial to prevent degradation or erosion of the mask during prolonged etching, especially for deep or fine-feature patterns. The BCl_3/Cl_2 plasma chemistry used was optimized to maximize etch rate and directionality while minimizing mask damage and surface roughness

Overall, ICP enables well-defined, vertical sidewalls and high aspect ratio features necessary for advanced GaN device structures. Process parameters such as ICP power, RF bias power, chamber pressure, and gas flow rates are carefully calibrated to achieve desired outcomes while maintaining process repeatability and surface integrity.

3.1.4 Metal deposition and lift-off techniques

The two most common techniques used for metal deposition in GaN device processing are evaporation (electron beam and thermal) and sputtering. In the electron beam and thermal evaporation, a metal source is heated under high vacuum until it vaporizes and condenses onto the wafer surface. E-beam evaporation provides high purity films and precise control over deposition rates, making it suitable for multilayer contact stacks like Ti/Al/Ni/Au, which are widely used for forming ohmic contacts in GaN HEMTs. In this project, electron beam evaporation tools were used in the deposition of hard mask and contact layers.

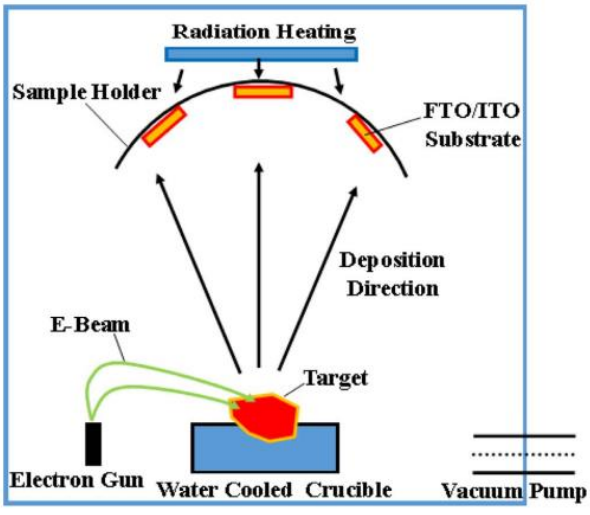


Figure 3. 7 Illustration of metal deposition using electron beam evaporation[134]

In the process, as illustrated in Figure 3.7, the metal to be deposited is placed in a water-cooled crucible. A hot filament, usually tungsten, emits electrons through thermionic emission when heated. These electrons are accelerated using a high-voltage potential and directed as a focused electron beam toward the surface of the source material. The kinetic energy of the electrons is converted into thermal energy upon impact, leading to localized heating and subsequent vaporization of the material. The vaporized atoms rise through the vacuum chamber and condense onto the cooler substrate positioned above the source, forming a uniform thin film. The vacuum environment, maintained by a vacuum pump, ensures that the vapor reaches the substrate without scattering due to collisions with air molecules.

A quartz crystal microbalance (QCM) is often integrated into the system to monitor the deposition rate and film thickness in real time. This is achieved by detecting frequency shifts in the quartz crystal as mass accumulates on its surface, allowing precise control over the deposition process. Since evaporated metal is deposited in a largely directional manner, it coats all exposed surfaces vertically. This characteristic allows for the use of a lift-off process to define precise metal patterns on semiconductor substrates. In this project, a bilayer resist approach is employed to facilitate clean lift-off. The bilayer structure creates a necessary undercut profile, which enables the resist remover to reach and dissolve the lower resist beneath the unwanted metal regions.

Figure 3.8 is an illustration of the lift-off process used in this project. Details of the individual process steps are described below.

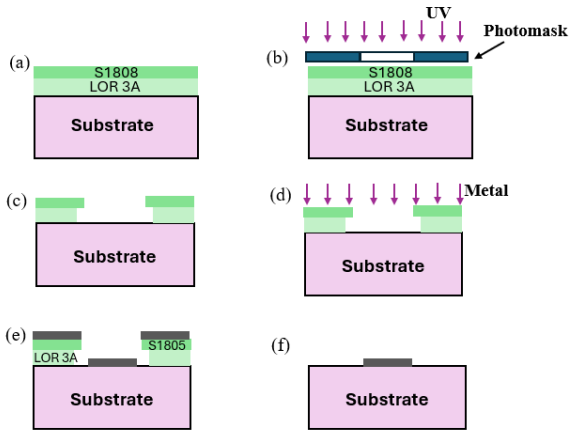


Figure 3. 8 Metal lift-off process

(a) The process starts by coating the substrate with a bilayer resist. First, a lift-off resist (LOR 3A) is spun onto the substrate. Then, a positive photoresist (S1808) is applied on top of the LOR. This bilayer stack is used because it enables the formation of an undercut profile after development, which is important for a clean lift-off.

(b) Next, the resist stack is exposed to ultraviolet (UV) light through a photomask. The photomask defines the pattern for the metal deposition. The UV light passes through transparent areas of the mask and exposes the positive photoresist below. Since it is a positive resist, the exposed areas become soluble in the developer solution.

(c) After exposure, the photoresist is developed. The exposed photoresist dissolves away in the developer. At the same time, the underlying LOR is partially dissolved, creating an undercut beneath the remaining photoresist. This undercut prevents metal from forming continuous sidewalls during deposition, facilitating easy lift-off.

(d) Then, the metal layer is deposited over the entire surface, typically by evaporation. The metal covers both the exposed substrate areas and the top surface of the resist stack, including the overhang created by the undercut.

(e) After metal deposition, the wafer is immersed in a solvent. The solvent dissolves the bilayer resist, lifting off the resist and the metal deposited on top of it. Because of the undercut, the metal on the substrate remains intact without any unwanted metal connecting the patterned areas.

(f) The final result is a clean metal pattern left on the substrate in the areas defined by the photomask. This lift-off process avoids the need for metal etching and allows precise patterning of metal features with well-defined edges.

3.1.5 Post-deposition annealing

Following metal deposition, annealing is often necessary to form low resistance ohmic contacts (in GaN devices) by promoting interdiffusion and alloying between the metal layers and the semiconductor surface. In GaN device fabrication, rapid thermal annealing (RTA) is commonly used due to its ability to deliver precise, high-temperature pulses over short durations, minimizing thermal budget while enabling effective interface

reactions. Typical annealing temperatures range from 700°C to 900°C depending on the metal system and desired contact characteristics.

In this project, the rapid thermal annealing process was performed at a temperature of 800 °C for 30 seconds in an N_2 atmosphere [135]. The samples were placed on a Si carrier wafer to ensure uniform heat distribution, with a temperature ramp rate of approximately 50–100 °C/s to minimize thermal stress. Cooling was performed under continuous N_2 flow to maintain surface integrity.

3.1.6 Thin film deposition of dielectric materials

Thin film deposition of dielectric materials is a critical step in the fabrication of GaN devices, as dielectric layers serve essential roles such as insulation, surface passivation, and gate dielectric formation. These layers influence device performance, reliability, and overall electrical characteristics. Common dielectric materials used include silicon dioxide (SiO_2), silicon nitride (Si_3N_4), and aluminium oxide (AL_2O_3), each offering distinct electrical and physical properties tailored for specific device requirements.

Several deposition techniques are employed depending on the desired film quality, thickness uniformity, and conformality. Plasma-enhanced chemical vapor deposition (PECVD) is widely used for depositing silicon-based dielectrics due to its relatively low processing temperatures and good film uniformity, making it suitable for temperature-sensitive substrates. Atomic layer deposition (ALD) offers atomic-scale thickness control and excellent conformality over complex device topographies, which is advantageous for high-k dielectrics such as AL_2O_3. Physical vapor deposition (PVD) methods, including sputtering and evaporation, provide alternative approaches for depositing dielectric films with different stoichiometries and densities.

3.1.7 Stylus profilometry

A stylus profiler (Bruker Dektak XT) was employed in this project for accurate measurement of thin film thickness, step height, and surface topography after various fabrication processes such as etching and deposition. The Dektak XT operates on the principle of contact profilometry, in which a diamond-tipped stylus is mechanically scanned across the sample surface under a controlled vertical force (typically in the

range of 10–150 μN). As the stylus traverses surface features, vertical displacements are recorded with nanometer-level resolution, generating a precise surface height profile.

In this study, Dektak XT was used to measure etch depths, film thicknesses, and to verify surface step heights after patterning and rapid thermal processing. The measurements were performed over scan lengths ranging from 6 μm to 560 μm, depending on feature size, with data acquisition controlled through the Vision64 software platform.

3.2 Material Characterization

Physical and structural characterization involves analysing the material composition, crystalline quality, surface morphology, and layer thicknesses of semiconductor materials and devices to ensure that fabrication processes meet design specifications. These techniques are critical for identifying defects, verifying doping profiles, and assessing interface quality, all of which directly influence device performance and long-term reliability.

In this research, structural analysis was carried out using Scanning Electron Microscopy (SEM) and Transmission Electron Microscopy (TEM), which provide a high-resolution imaging of surface and cross-sectional features at the nanoscale, enabling the identification of defects such as dislocations, voids, and layer discontinuities. Atomic Force Microscopy (AFM) could also be employed to measure surface roughness and topography with nanometre precision, an essential parameter for ensuring thin-film uniformity and the reliability of gate dielectrics.

The following subsections provide a detailed description of some of the characterization methods.

3.2.1 Atomic Force Microscopy (AFM)

Atomic Force Microscopy (AFM) is a high-resolution surface characterization technique used to investigate the topography and roughness of semiconductor materials at the nanometre scale. It operates by scanning a sharp tip mounted on a flexible cantilever across the sample surface. As the tip interacts with the surface features, deflections in the cantilever are detected using a laser beam reflected into a position-sensitive photodetector, allowing precise mapping of surface contours. AFM can operate in different modes, including contact mode, tapping mode, and non-contact mode,

depending on the nature of the sample and the desired resolution. Tapping mode is commonly used in semiconductor applications to minimize damage to delicate surfaces while maintaining high-resolution imaging.

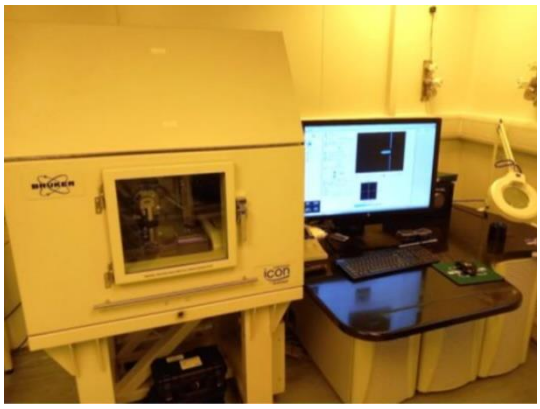


Figure 3. 9 Atomic force microscopy (AFM) kit in the JWNC.

The technique provides quantitative data such as root mean square (RMS) surface roughness, peak-to-valley height, and grain size distribution. Figure 3.9 shows the AFM equipment located in the JWNC.

3.3.2 Scanning Electron Microscopy (SEM)

Scanning Electron Microscopy (SEM) is a powerful imaging technique used to analyse the surface morphology and microstructural features of semiconductor materials with high spatial resolution. It operates by directing a focused beam of high-energy electrons onto the sample surface. As the electrons interact with the atoms of the material, they generate various signals, including secondary electrons, which are collected to produce detailed images of the surface. SEM provides excellent lateral resolution typically ranging

Figure 3. 10 Scanning Electron Microscopy (SEM) equipment in the JWNC.

from a few nanometres to tens of nanometres, making it ideal for examining fine surface details such as edge profiles, grain boundaries, micro-cracks, etch patterns, and structural defects. Figure 3.10 shows the SU8240 Hitachi SEM located in JWNC and used in this project.

3.2.3 Transmission Electron Microscopy (TEM)

Transmission Electron Microscopy (TEM) is an advanced imaging technique used to examine the internal microstructure of semiconductor devices at atomic or near-atomic resolution. In TEM, a high-energy electron beam is transmitted through an ultra-thin specimen, typically less than 100 nanometres thick. As electrons pass through the sample, they interact with its atomic structure, creating contrast based on thickness, composition, and crystallographic orientation. TEM provides detailed information about crystal lattice arrangements, defects such as dislocations and stacking faults, interface quality, and layer thickness with sub-nanometre precision. It is particularly valuable for analysing epitaxial layers, gate oxides, heterostructures, and metallization interfaces in semiconductor devices.

Sample preparation for TEM is complex and time-consuming, involving precise mechanical thinning followed by ion milling or focused ion beam (FIB) techniques to achieve electron transparency. The TEM imaging and analysis for this project was conducted at the Kelvin Nano-characterization Centre, University of Glasgow, and was performed by the facility's technical staff.

3.3 Summary

This chapter presented a comprehensive overview of the fabrication techniques and characterization methods employed in the processing of GaN-based devices at the James Watt Nanofabrication Centre (JWNC), University of Glasgow. It outlined the standard step-by-step procedures and tools used throughout the fabrication process, including lithographic patterning, dry and wet etching, metal deposition and lift-off, rapid thermal annealing, and dielectric layer deposition.

Post-fabrication treatments and metrology techniques, such as film thickness and etch depth measurements, were also described to ensure process accuracy and reproducibility. In addition, the chapter introduced the material characterization

methods utilized in this work, namely Atomic Force Microscopy (AFM), Scanning Electron Microscopy (SEM), and Transmission Electron Microscopy (TEM), which provided essential insights into surface morphology, structural integrity, and defect distribution within the fabricated structures.

Collectively, these processes and analytical techniques establish the experimental foundation for the device fabrication and performance analysis discussed in the subsequent chapters.

Chapter 4

Buffer-free AlGaN/GaN HEMTs

4.1 Introduction

This chapter describes the fabrication, characterization and analysis of the performance of buffer-free AlGaN/GaN HEMTs with varying channel and nucleation layer thicknesses, investigating their suitability for medium-voltage switching applications. By eliminating the conventional buffer layer, these structures aim to reduce material complexity while enhancing thermal handling, minimizing trapping effects, and maintaining high breakdown voltage, all critical for reliable device operation.

A comprehensive structural and electrical evaluation of three buffer-free AlGaN/GaN HEMT wafers was conducted to assess the impact of epitaxial design and defect distribution on device performance and reliability. Cross-sectional TEM and SEM imaging were used to obtain a physical view of the quality of the material wafer. DC and pulsed-IV measurements were employed to investigate the behaviour of the devices under various bias conditions. It was found that the GaN channel and AlN nucleation layer thickness play a fundamental role in defining the trapping behaviour, self-heating response, and electrical robustness of GaN HEMT devices. This chapter describes and discusses these findings.

4.1.1 Motivation for buffer-free HEMT design

Conventionally, the epitaxial layer structure for GaN HEMTs is grown on non-native substrates, usually Si or Sapphire, using MOCVD technique and includes a thick GaN channel layer, typically ~1 μm, to minimize defect density, and a thick (typically ~1-2 μm) GaN/AlGaN buffer layer to accommodate lattice mismatch and optimize strain within the substrate. The buffer layer is usually doped with carbon or iron acceptor impurities to minimize buffer leakage [136], [137].

Recently, epitaxial layer design for AlGaN/GaN HEMT structures without the buffer layer have been demonstrated [138], [139]. These buffer-free structures offer several important

advantages including reduced growth material requirements, lesser growth complexity and processing time, improved device performance not hampered by buffer-related imperfections (due to reduced trapping effects) and improved thermal management by positioning of the GaN channel layer closer to the substrate. Thus, buffer-free HEMTs employ a more sustainable growth approach and can enable higher power operation, longer device lifetimes, and enhanced reliability.

Buffer-free AlGaN/GaN structures on Si are just emerging, but are more developed for SiC substrates where the *hot-wall* MOCVD growth technique is used [139] Hot-wall MOCVD is a high-temperature chemical vapor deposition technique (typically 1400–1650°C for SiC, or lower for oxides) in which the entire reactor chamber is heated, rather than just the substrate. This approach ensures highly uniform, high-quality epitaxial layer growth for materials such as AlN and GaN by reducing thermal gradients, minimizing wafer bowing, and improving precursor distribution.[138], [140]. The ability to grow a high-quality AlN nucleation layer with this technique has made it possible to successfully eliminate the thick GaN buffer, which had been very challenging prior to its introduction. Their epitaxial layer structure comprises an AlGaN barrier layer grown on a thin GaN channel layer, typically between 200 nm and 265 nm in thickness and AlN nucleation layer of tens of nanometers, typically 60 nm [141], [142], [143]. This epi-structure provides device performances comparable to the best conventional devices with buffer layers.

Recently, a study into buffer-free structures with even thinner channel layers, down to 150 nm, was conducted [144]. Such devices benefit from the AlN nucleation layer as a back barrier and so help with better confinement of the 2-2DEG channel and would be ideally suited for highly scaled sub-100nm short channel devices by minimizing the short channel effects. While such configurations have been predominantly explored for radio frequency (RF) applications, this study focuses on their potential in power switching devices.

In this study, we compare the electrical performance of AlGaN/GaN HEMT devices fabricated on three otherwise identical wafer structures but with different GaN channel (250 nm vs 500 nm) and AlN nucleation layer (60nm vs 100nm) thicknesses. The aim is to integrate power-device-optimized design to enhance breakdown voltage – critical for medium-voltage applications – while simultaneously utilizing the inherent advantages of buffer-free architecture, such as improved thermal management, minimized trapping

effects, and reduced leakage paths, all contributing to superior dynamic performance and device reliability.

4.2 Wafer Structure

This study investigated three buffer-free AlGaN/GaN HEMT epitaxial structures grown by hot-wall MOCVD on semi-insulating SiC substrates, grown by SweGaN as shown in figure 4.1. Each wafer consists of a 2 nm GaN cap layer and a 23 nm $Al_{0.24}Ga_{0.76}N$ barrier layer. Wafer 1 serves as the reference and includes a 250 nm GaN channel and a 60 nm AlN nucleation layer. Wafer 2 has a thicker GaN channel of 500 nm, while Wafer 3 features a thicker AlN nucleation layer of 100 nm.

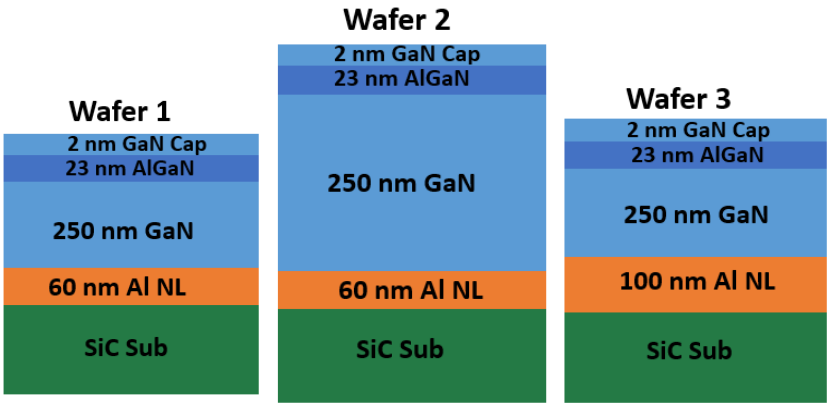


Figure 4. 1 showing wafer structures with Wafer 1, the reference wafer (channel: 250 nm, AlN NL: 60 nm); Wafer 2, thicker channel layer (500 nm); Wafer 3, thicker AlN NL (100 nm).

To assess the transport properties of the 2DEG, contactless Hall and Eddy current measurements were performed by the grower. The extracted values of sheet carrier concentration (n_s), mobility (μ), and sheet resistance (R_{sh}) are summarized in Table 4.1. The results show a very close n_s values across all wafers, with moderate variations in μ and R_{sh} due to the changes in channel and nucleation layer thickness.

Table 4.1: 2DEG Properties of Wafers 1, 2 and 3.

	Wafer 1	Wafer 2	Wafer 3
n_s [/cm^2]	8.68e12	8.49e12	8.7e12
μ [cm^2/Vs]	2012	2091	1963
R_{sh} [Ω/sq]	380	364	365

The 4-inch wafers were diced into 10 mm x 10 mm samples using a precision automated dicing saw equipped with a diamond-coated blade to ensure clean, crack-free separation. Prior to dicing, epitaxial side of the wafers were coated with ~3 μm layer of S1818 photoresist to prevent surface abrasion or damage while dicing, then mounted on

adhesive-backed dicing tape to maintain mechanical stability and prevent chipping during the process. Parameters such as blade speed, feed rate, and coolant flow were carefully optimized to minimize mechanical stress and contamination.

The transparent nature of the sample and its double-side polished nature, makes visual identification of the epi-side impractical. To identify the epitaxial layer side, a simple continuity test was performed. The dicing resist was first removed by immersing the sample in Microposit 1165 resist remover at 50 °C for several hours to ensure complete dissolution of the protective resist layer. After resist removal, the sample was thoroughly rinsed with reverse osmosis (RO) water and dried using a nitrogen gun. A subsequent soft bake for 3 minutes at 180°C was performed to eliminate any residual moisture from the sample surface. To identify the epitaxial layer side, a two-probe resistance measurement was conducted using the Keysight B1500A Semiconductor Device Analyzer. For the test, two probes were gently placed on one side of the sample, and the resistance was measured. A significantly lower resistance was recorded when the probes were in contact with the epitaxial side. In contrast, the SiC substrate side exhibited a very high resistance and significantly low conducting current due to the semi-insulating nature of the substrate. To prevent misidentification in subsequent processing steps, the substrate side was carefully marked using a diamond scribe, providing a clear visual reference for proper sample orientation throughout the remaining fabrication process.

4.3 Fabrication Process

The fabrication of AlGaN/GaN HEMTs involved a series of precisely controlled steps, including ohmic contact formation, mesa isolation, gate definition, and pad metallization. Each step was optimized for material compatibility, pattern fidelity, and electrical performance to ensure reliable and repeatable device operation. A brief description of the process is provided in this section, the detailed description can be found in appendix I.

The device structure features a two finger-HEMT design, comprising a gate with a length (L_g) of 3 µm, separated by 2 µm from the source (L_{gs}) and 4 µm from the drain (L_{gd}) as shown in Figure 4.2.

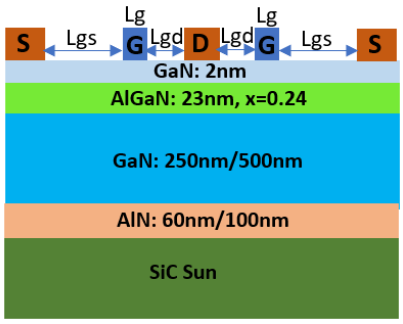


Figure 4. 2 Cross-sectional view and dimensions of the 2-finger HEMT

The wafer surface first underwent thorough cleaning and pre-treatment to eliminate native oxides, organic residues, and other contaminants. The sample was immersed in a plastic beaker containing acetone and subjected to ultrasonic agitation for 5 minutes to ensure complete removal of surface contaminants, followed by rinsing with isopropyl alcohol (IPA) and reverse osmosis (RO) water, then dried using a nitrogen gun.

The fabrication process began with a soft bake at 180 °C for 3 minutes to remove surface moisture, followed by the application of a bilayer resist stack (LOR 3A/S1818) to achieve a clean undercut profile for reliable metal lift-off to define ohmic contacts and alignment markers. LOR 3A was spin-coated and baked at 150 °C, then overlaid with S1818 photoresist, which was baked at 115 °C. The wafer was exposed to UV light through a photomask and developed in MF319 to reveal the alignment markers and ohmic contact patterns. Oxygen plasma descum and dilute HCl cleaning were performed to remove residual resist and native oxides. A Ti/Al/Ni/Au (30/180/20/100 nm) ohmic metal stack was then deposited by electron-beam evaporation followed by lift-off process in heated Microposit 1165 (50 °C for 2 hours) to removed excess metal and resist, producing well-defined alignment markers and ohmic contacts for subsequent device fabrication.

Figure 4.3 shows a micrograph of the deposited ohmic contacts prior to and after high temperature annealing which was carried out at 800 °C for 30 seconds in a nitrogen ambient to alloy the Ti/Al/Ni/Au metal stack and reduce contact resistance. This process enhanced metal–semiconductor interdiffusion, improved adhesion and thermal stability, and resulted in low-resistance ohmic contacts essential for reliable, high-performance AlGaN/GaN HEMTs.

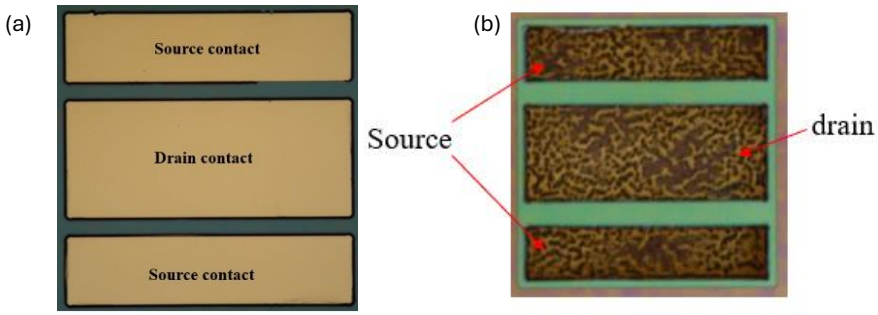


Figure 4. 3 (a) Ohmic contact after deposition of Ti/Al/Ni/Au (30/180/20/100 nm), (b) after annealing at 800 ℃ for 30 s.

Next, mesa isolation carried out to electrically separate individual device regions by selectively removing semiconductor material surrounding the active areas. The process involved spin-coating and patterning S1818 photoresist to define the mesa regions, followed by ICP etching using Cl_2/Ar gases for 50 seconds at 200 W ICP power, 100 W RF bias, and 5 mTorr pressure. The etch rate of approximately 100 nm/min ensured complete removal of the AlGaN/GaN layers down to the buffer layer. After etching, the resist was stripped in Microposit 1165 at 50 °C and the wafer rinsed and dried. The resulting mesas exhibited smooth, well-defined sidewalls that effectively isolated the devices and minimized leakage. Figure 4.4 presents the completed isolated device along with an illustration depicting the mesa isolation profile.

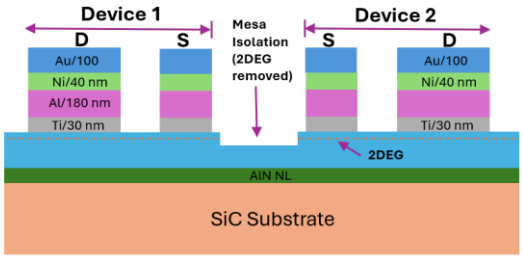


Figure 4. 4 Outline of mesa isolation after the etching process.

Gate definition (Fig. 4.5) began by the application of a bilayer resist stack (LOR 3A/S1805) to achieve a clean undercut profile for reliable metal lift-off. The resist layers were spin-coated, baked, exposed to UV light through a photomask, and developed to form ~3 µm gate openings with high precision. Metal deposition was performed by electron-beam evaporation of a Ni/Au (20/200 nm) stack, where Ni acted as the Schottky contact layer and Au ensured chemical stability. The lift-off process in heated Microposit 1165 (50 °C) removed excess metal, producing sharp, well-defined gate electrodes. This process

yielded precise gate structures essential for effective control of the 2DEG channel and high-performance HEMT operation.

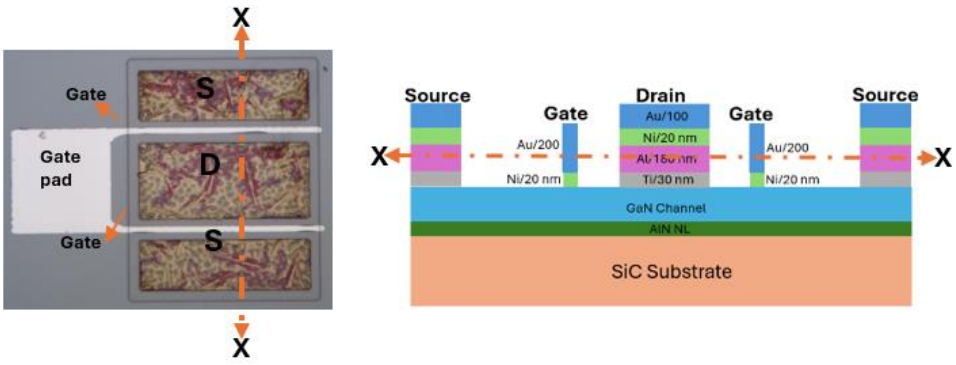


Figure 4. 5 (a) Gate profile after deposition Ni/Au (20/200 nm) gate stack (b) Cross-sectional view of the contacts

Finally, metal bond-pad processing was performed to create large-area contacts suitable for probing. The pad dimensions were designed to accommodate the ~50 µm pitch tungsten probe tips of the Keysight B1500A analyser, ensuring stable electrical contact.

A bilayer resist stack (LOR 10A/S1818) was used for precise pattern definition and clean metal lift-off. After spin-coating, baking, exposure, and development, a Ni/Au (20/200 nm) metal stack was deposited via electron-beam evaporation. The lift-off process in heated Microposit 1165 (50 °C) removed excess metal and resist, resulting in smooth, well-defined bond pads optimized for reliable probing. The layout of the final device structure is shown in Figure 4.6.

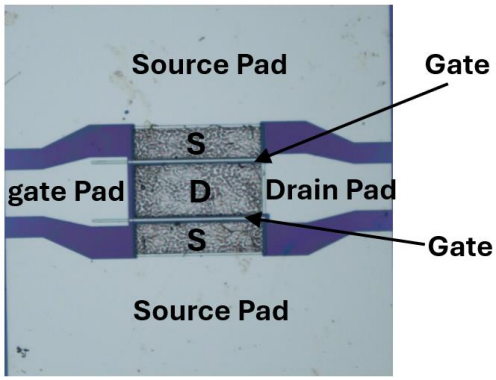


Figure 4. 6 Complete structure of 2-finger HEMT device

4.4 Device Characterization

Following fabrication, the AlGaN/GaN HEMT devices were characterised using the Keysight B1500A Semiconductor Device Analyzer under ambient conditions, employing

both two-probe and four-probe configurations depending on the specific test requirements.

4.4.1 DC characterization

DC characterization was used to evaluate key electrical parameters such as threshold voltage (V_{th}), drain current (I_{DS}), transconductance (G_m), on-resistance (R_{ON}), and breakdown voltage and gate leakage behaviour as detailed below.

Figures 4.7 (a) and (b) show the output characteristics (I_{DS}-V_{DS}) and gate leakage current measurements for devices fabricated from the three wafers. The measured saturated drain current (I_{DS}) at V_{GS} = 0 V was 327 mA/mm, 411 mA/mm, and 368 mA/mm for wafers 1, 2, and 3, respectively. Thus, both Wafers 2 and 3 exhibit 26% and 11% increase in I_{DSS} compared to the reference wafer (wafer 1). As shown in Figure 4.7(b), Wafer 2 demonstrated significantly lower gate leakage current (~0.076 µA/mm at V_{GS} = -6V) compared to ~7.0 µA/mm and ~0.72 µA/mm for Wafers 1 and 3 respectively.

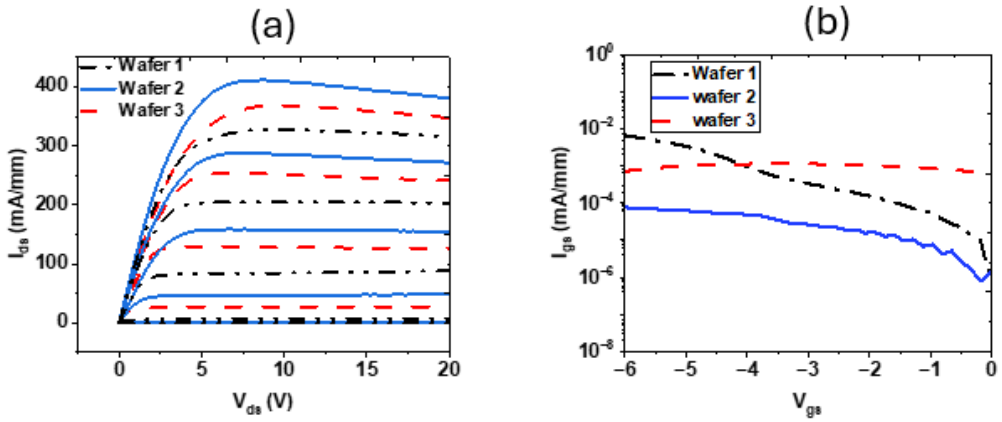


Figure 4. 7 (a) Output characteristics: the gate-source voltage (VGS) from -4 V to 0 V in -1 V steps. the drain-source voltage (VDS) from 0 V to +20 V; (b) Gate leakage current of all 3

Figure 4.8 shows the off-state drain leakage currents or breakdown voltage (V_{BR}) measurements which were conducted by applying a high negative gate bias of -8 V to fully turn off the transistor and then sweeping the drain voltage (V_{DS}) from 0 V to +200 V. Wafers 1 and 3 demonstrated a breakdown voltage (presumably) exceeding 200 V (the measurement limit of our equipment is 200 V); Wafer 2 exhibited hard breakdown at ~200 V; the leakage drain current was taken at 1 mA/mm threshold in all 3 cases. For V_{DS} under 100 V, Wafer 2 showed several orders of magnitude lower off-state leakage current. However, its leakage rises steeply with increasing V_{DS}, leading to premature run-away around

200 V. In contrast, Wafers 1 (250 nm GaN, 60 nm AlN) and 3 (250 nm GaN, 100 nm AlN) both sustain breakdown voltages exceeding 200 V, with Wafer 3 showing lower leakage than Wafer 1.

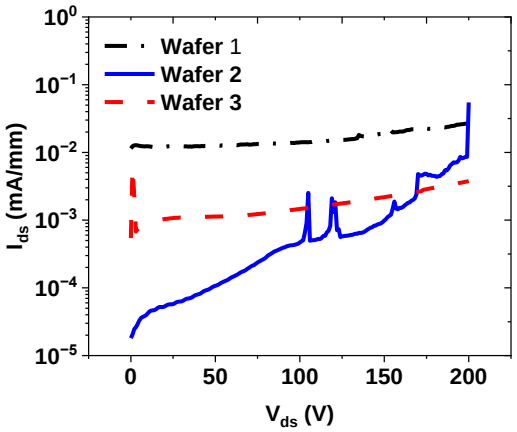


Figure 4. 8 Breakdown voltage characteristics of wafers 1, 2 and 3.

From the I_{DS}–V_{GS} transfer characteristics in Figure 4.9, the extracted threshold voltages (V_{TH}) were approximately –3.7 V, –3.3 V, and –2.9 V for Wafers 1, 2, and 3, respectively.

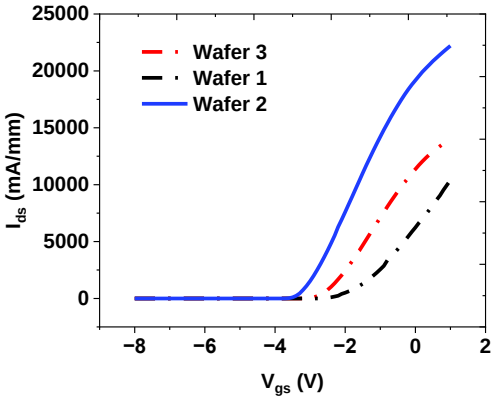


Figure 4. 9. transfer characteristics at VDS =10 V of devices from the 3 wafers

The DC transconductance (Gm) versus gate voltage (V_{gs}) curves for the three wafers are presented in Figure 4.10. Transconductance quantifies how effectively the gate voltage modulates the drain current, defined as the ratio of the change in drain current to the change in gate voltage($gm = Ids/Vds$). Higher DC transconductance in FETs indicates stronger voltage-to-current gain, which translates to faster switching speeds and lower power consumption [145], [146].

From the graphs (Figure 4.10), Wafer 2 exhibits the highest peak Gm, reaching approximately 95 mS/mm at Vgs≈−1.5 V. Wafer 3 shows a slightly lower peak of around 70 mS/mm at the same gate voltage, while Wafer 1 has the lowest peak of approximately 42 mS/mm. Additionally, Wafer 2 displays a broader high-Gm region compared to Wafer 3, suggesting stronger current-driving capability.

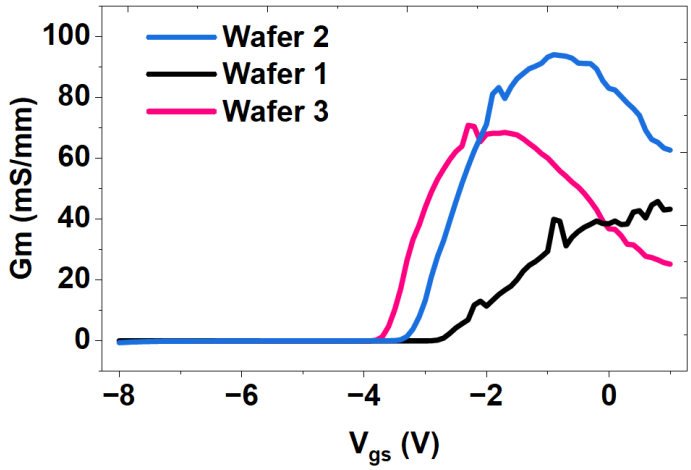
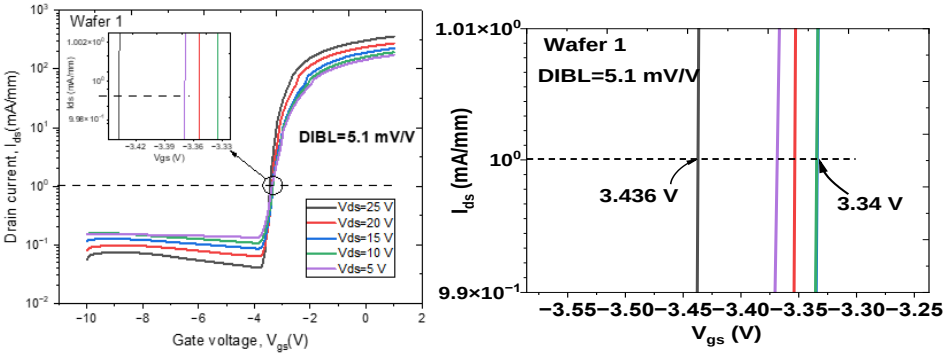


Figure 4.10: DC transconductance of the 3 wafers

In Figure 4.11, drain induced barrier lowering (DIBL) characteristics of the 3 wafers measured under varying drain-source voltage from 5 V to 25 V at a step of 5 V, with a threshold voltage (V_{th}) defined as the gate voltage at drain current density of 1 mA/mm are shown. The insert-graph shown in Figure 4.12 presents wafer 2 having a lower V_{th} shift of 1.05 mV/V against wafer 1 with wider shift of 5.6 mV/V, which makes IDBL effect lower in wafer 2. The off-state drain leakage current density of wafer 1 (56 µA/mm) at V_{gs}=-10 V and V_{ds} of 5 V is 100× higher than that of wafer 2 (0.56 µA/mm).



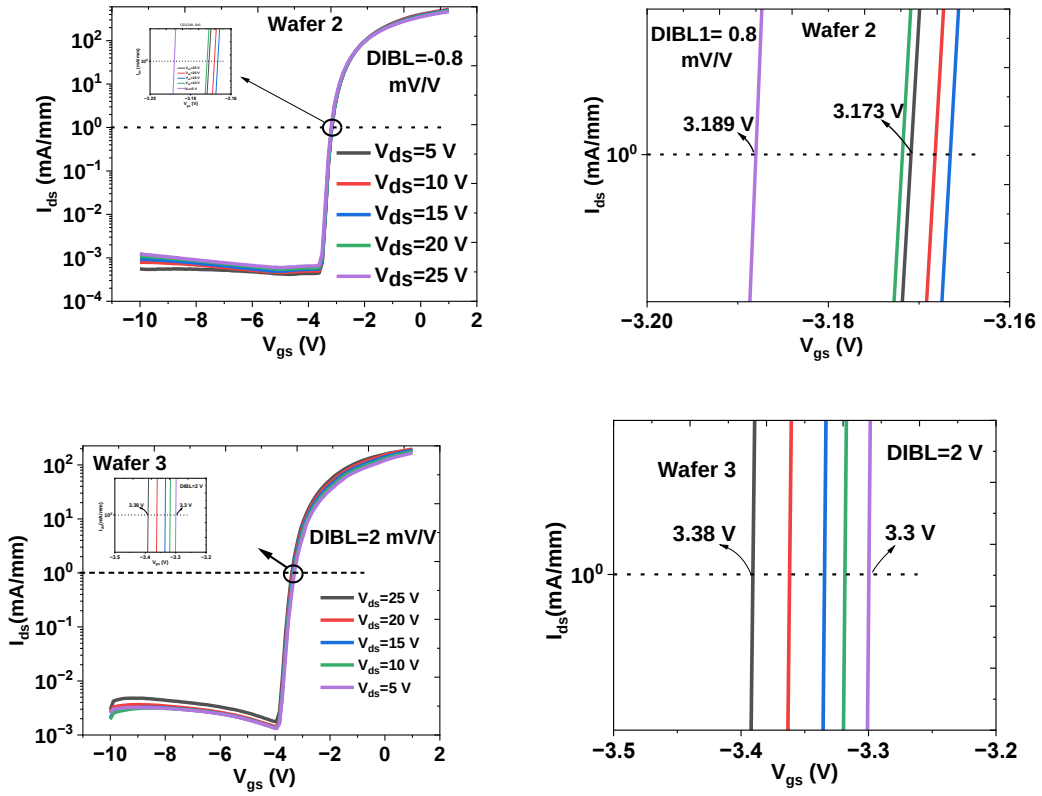


Figure 4. 11 Drain induced barrier lowering (DIBL) for wafer 1 and 2.

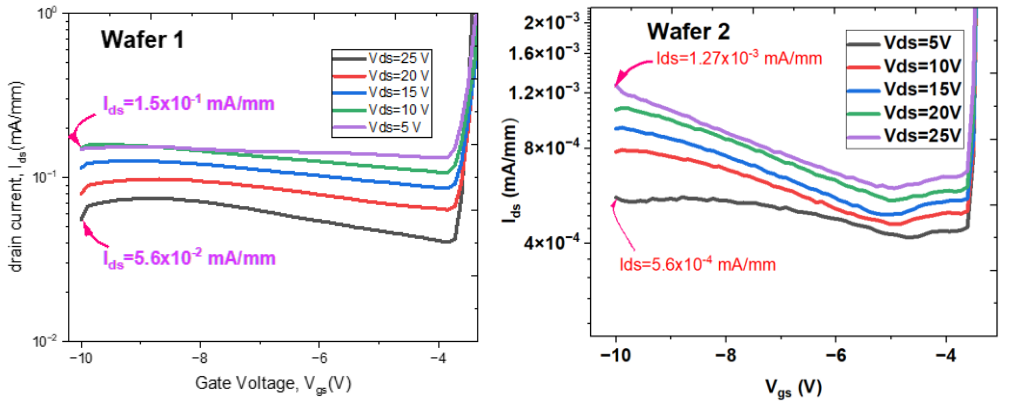


Figure 4. 12 DIBL characteristics showing the off- state drain leakage current densities of wafer 1 and 2.

4.4.2 Characterization of self-heating

A pulsed I–V method serves as an effective technique for investigating self-heating effects in AlGaN/GaN HEMTs by isolating thermal influence from intrinsic device behaviour. Using short pulse widths and low duty cycles reduces the on-time of the device, thereby minimizing heat accumulation in the channel and surrounding layers. This enables more accurate characterization of the device under near-isothermal conditions. In contrast,

static DC I–V measurements allow for continuous power dissipation, leading to a rise in lattice temperature and corresponding performance degradation. The difference between pulsed and DC curves reveals the degree of self-heating , which can significantly impact current handling, efficiency and reliability [147].

Measurements were performed on the 2×100 µm two-finger HEMT devices using a Keithley 4200A-SCS parameter analyser. The quiescent biases for both gate and drain were set at 0 V, and the pulse width and period were 1 µs and 100 µs, respectively. The output characteristics for each wafer are presented in Figure 4.13 (a–c). In each case, the pulsed I–V curves reach significantly higher drain current levels than their DC counterparts, clearly illustrating the impact of thermal buildup during static operation. As the lattice temperature increases under DC stress, reductions in thermal conductivity, bandgap, and especially the mobility of 2DEG carriers occur, resulting in observable current drop.

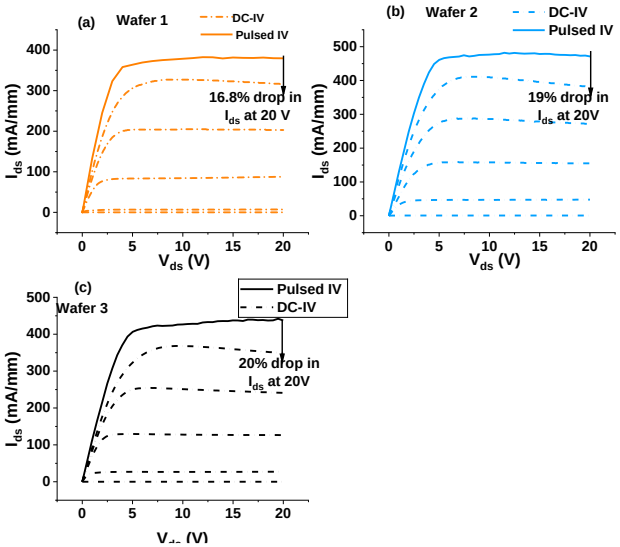


Figure 4. 13 Pulsed and static IV characteristics measured under quiescent biases {Vgs,q, Vds,q} = {0, 0} at Vgs of to -4 V and Vds of 0 to 20 V. Pulse duration set to 1 µs with a period of 100 µs, for self-heating characterization.

For Wafer 1, the drain current drops by approximately 16.8% under DC conditions relative to pulsed operation. Wafer 2 exhibits a larger drop of 19%, while Wafer 3 shows the highest reduction at 20%. The larger current drop in Wafer 2 is attributed to the increased thermal resistance introduced by the thicker GaN channel layer [148], which positions the heat-generating region farther from the thermally conductive SiC substrate, thereby reducing heat dissipation efficiency. In contrast, the heat dissipation degradation in Wafer 3 is linked to the elevated thermal barrier resistance resulting from its thicker (100

nm) AlN nucleation layer, which impedes vertical heat conduction despite its advantages in dislocation suppression [40]. While Wafer 1 is still affected by self-heating, its thermal degradation is less severe than in the other two wafers, attributed to its thinner GaN channel and reduced thermal path length to the SiC substrate (due to closer proximity of the active region to the substrate) [148].

4.4.3 Characterisation of trap states

Pulsed I–V measurements were conducted to investigate the influence of trap states on drain current recovery and transient device behaviour. The following three quiescent bias conditions were employed to isolate different trapping mechanisms:

Q1 (0 V, 0 V) – cold, stress-free state, the reference state

Q2 (–10 V, 0 V) – gate-stressed condition, used to assess gate lag

Q4 (0 V, 30 V) – drain-stressed condition, used to evaluate drain lag

Figure 4.14 shows pulsed IV curves of the gate and drain lagging phenomena due to stresses induced by gate and drain quiescent biases. In Wafer 1, the drain current under cold-state conditions (Q1) peaks at approximately 368 mA/mm. When subjected to gate stress (Q2), the current drops to 309 mA/mm, corresponding to a gate lag of approximately 16%. This significant degradation indicates a high density of electron traps located near the AlGaN/GaN interface or at the surface, likely associated with threading dislocations and other structural defects. Under drain-stressed conditions (Q4), the drain current decreases to 340 mA/mm, resulting in a drain lag of around 7.6%. This suggests the presence of moderate trap activity within the buffer or gate-drain access region. Therefore, the dominant degradation observed under gate stress in Wafer 1 points to surface/interface-related trapping as the primary mechanism of current dispersion.

In Wafer 2, the cold-state drain current (Q1) reaches approximately 455 mA/mm. Under gate-stressed conditions (Q2), it decreases only slightly to 445 mA/mm, resulting in a gate lag of about 2.2%. This minimal degradation indicates excellent interface integrity and low trap density near the AlGaN/GaN interface or surface region. However, under drain-stressed conditions (Q4), the drain current drops significantly to 366 mA/mm, corresponding to a drain lag of approximately 19.6%. This substantial reduction suggests strong trap activation deeper in the structure, likely within the GaN buffer or at the

AlN/SiC interface, triggered by the high electric field at the drain. Although Wafer 2 exhibits well-controlled gate-related trapping behavior, its pronounced drain lag highlights limitations in buffer quality and vertical heat or charge dissipation pathways, which compromise its transient performance under high-field operation.

Wafer 3 exhibits a cold-state drain current of approximately 410 mA/mm. Under gate-stressed conditions (Q2), the current drops slightly to 406 mA/mm, yielding a gate lag of just ~0.98%—the lowest among all three wafers. This minimal degradation indicates highly effective surface and interface passivation, consistent with the clean and well-ordered GaN/AlN interfaces. However, when subjected to drain-stressed conditions (Q4), the drain current decreases to 365 mA/mm, corresponding to a drain lag of approximately 10.98%. While this is an improvement over Wafer 2, it remains a notable reduction, suggesting that trap states located deeper in the structure—possibly within the thicker AlN nucleation layer or at the AlN/SiC interface—are being activated under high drain bias. Despite the superior surface quality, this result highlights that vertical transport and buffer-layer engineering remain critical to fully mitigate field-induced dispersion effects

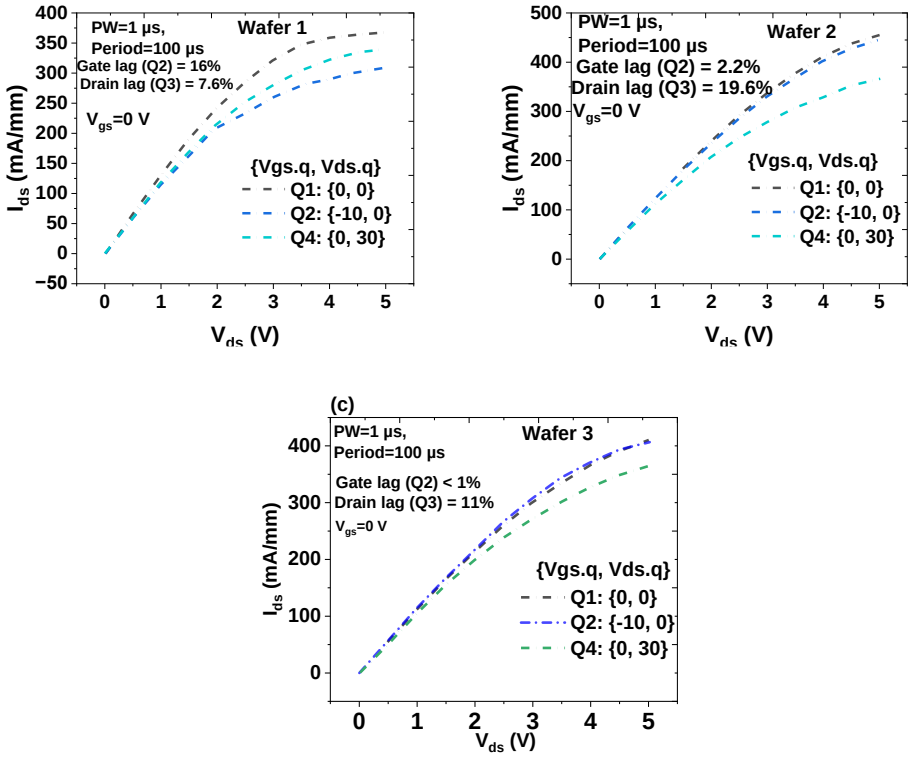


Figure 4. 14 Pulse IV curves showing gate and drain lagging phenomena due to stresses induced by gate and drain quiescent biases

Changes in the threshold behavior were analysed under various quiescent gate and drain bias conditions to assess field-induced trapping effects. The gate quiescent bias ($V_{gs,q}$) was fixed at –6 V to ensure the device remained fully turned off during the quiescent phase, while the drain quiescent bias ($V_{ds,q}$) was incrementally increased from 5 V to 40 V in 5 V steps. This configuration produced the pulsed transfer characteristics shown in Figure 4.15 for all three wafers. The characteristic curves reveal a systematic positive threshold voltage shift across all three wafers. Threshold voltage values extracted at I_{ds}=20 mA/mm indicate that wafer 1 exhibits a shift from ~2.9 V under cold-state conditions to ~2.7 V at $V_{ds,q}$ of 40 V. Similarly, wafer 2 shows a shift from ~3.6 V in the cold state to approximately 3.4 V at $V_{ds.q}$=40 V, while wafer 3 shifts from ~3.4 V to ~3.2 V under the same bias conditions.

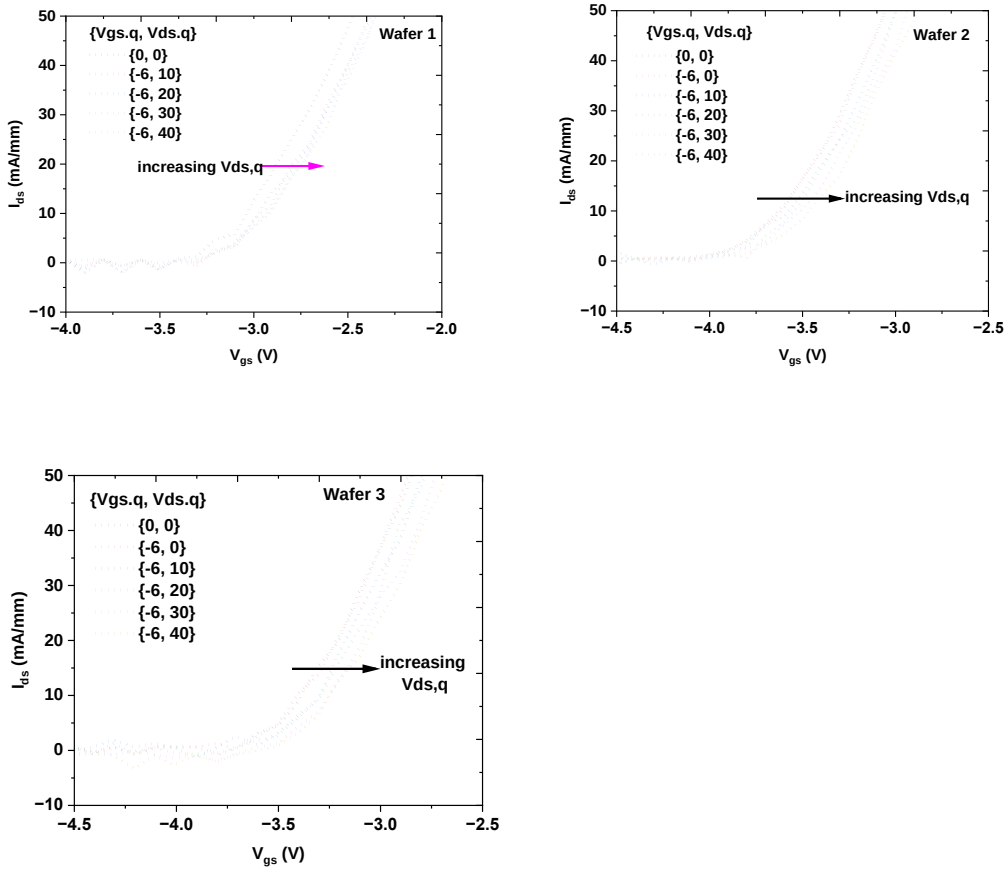


Figure 4. 15 Pinch-off characteristics at various drain quiescent stress voltages from 0 to 40 V.

The uniform threshold voltage shift observed across all wafers under quiescent drain bias suggests a common, bias-induced trapping mechanism. The limited magnitude of the

shift indicates relatively stable gate control; however, the reproducibility of the effect points to charge trapping at the surface or gate interface as a contributing factor that warrants further investigation. Although the magnitude of the threshold voltage shift is small (~0.2 V), its persistence across multiple wafers implies a systematic reliability-related phenomenon that could influence long-term device stability under high-field operation.

4.5 Material Characterization

Transmission electron microscopy (TEM) analysis of the samples was carried out to assess the growth quality of the epitaxial layer. Figure 4.16 shows TEM micrographs for Wafers 1, 2 and 3 from which relative fewer threading dislocations in Wafer 2 and 3 may be seen.

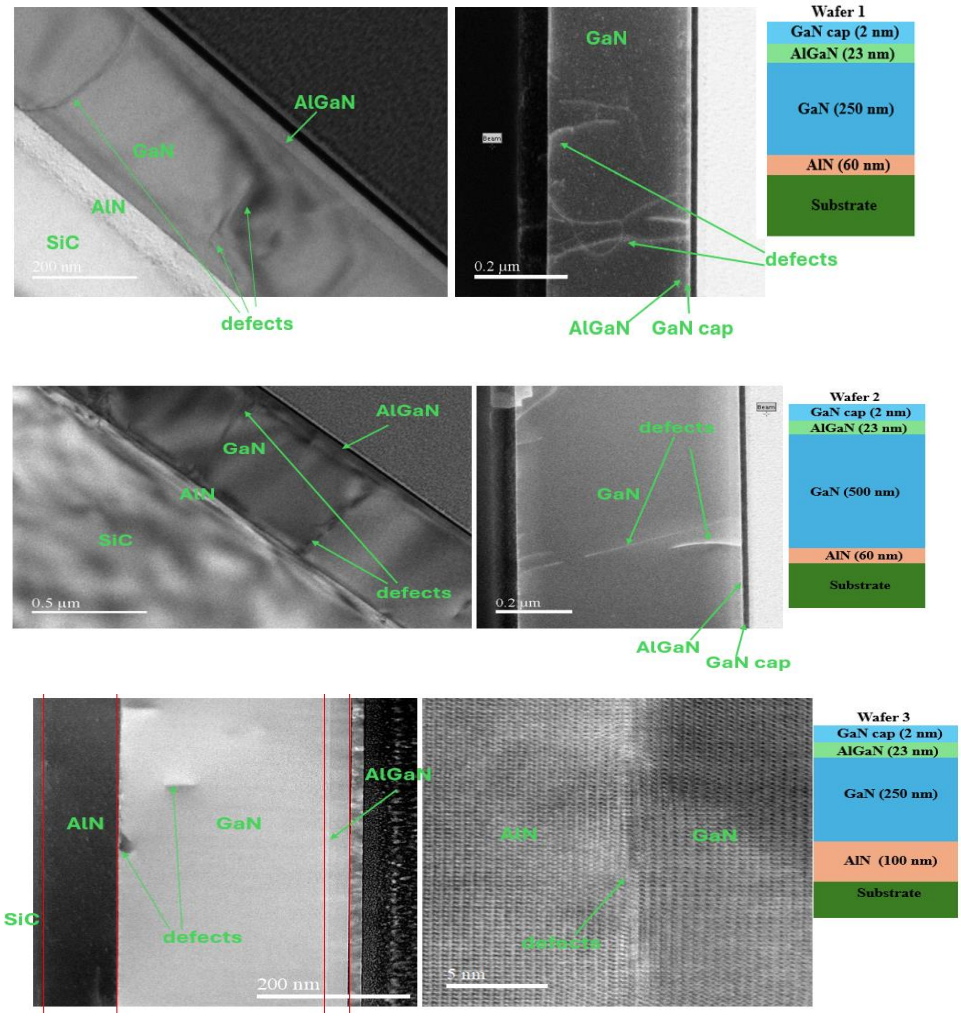


Figure 4. 16 TEM images for Wafers 1, 2 and 3. Threads of dislocations are seen to emanate from the SiC/AlN interface. Some of the threads extend through the GaN channel and the AlGaN barrier layers to the surface.

The cross-sectional TEM images of Wafers 1, 2, and 3 reveal significant differences in crystalline quality and defect propagation, which can be directly linked to their respective epitaxial designs. These variations arise primarily from changes in the thickness of the GaN channel and AlN buffer layers, which influence dislocation filtering, strain relaxation, and overall material integrity.

Wafer 1 consists of a 250 nm GaN channel over a 60 nm AlN nucleation layer grown on a SiC substrate. The images show that numerous threading dislocations propagate vertically from the substrate through the AlN buffer and into the GaN channel, with many extending up to the AlGaN interface. These defects suggest limited dislocation filtering efficiency, likely due to the relatively thin AlN layer and the short distance available for dislocation bending or annihilation. The presence of such extended defects through the active channel and the AlGaN/GaN layer can introduce trap sites and degrade the structural quality at the interface, resulting in higher gate and buffer leakage, and reduce carrier transport.

In Wafer 2, the GaN channel is increased to 500 nm while retaining the same 60 nm AlN buffer. The TEM images indicate that many of the dislocations bend or terminate within the thicker GaN layer, suggesting improved dislocation filtering compared to Wafer 1. The thicker GaN layer provides a greater vertical distance for threading dislocations to interact, bend, or annihilate, resulting in fewer defects reaching the AlGaN/GaN interface. This suggests a better structural quality at the AlGaN/GaN interface, and could be the reason for lower gate leakage compared to wafer 1.

Wafer 3 introduces a thicker 100 nm AlN buffer while maintaining a 250 nm GaN channel. This structural change results in the most notable reduction in defect propagation among the three samples. The TEM cross-sections reveal a highly ordered lattice structure with minimal visible dislocations traversing into the GaN region. The thicker AlN nucleation layer appears to serve as an effective filter, reducing the threading dislocation density and promoting higher crystal quality in the subsequent GaN growth.

Although transmission electron microscopy (TEM) provides direct, high-resolution visualization of structural defects, the localized nature of TEM observations limits their statistical representativeness. Consequently, TEM imaging alone is insufficient to draw

definitive conclusions regarding the overall crystalline quality, defect density uniformity, or device-relevant material performance. A comprehensive assessment therefore requires the integration of TEM imaging with complementary TEM-based analytical techniques and macroscopic characterization methods.

The scanning electron microscopy (SEM) images shown in Figure 4.17 for Wafers 1, 2, and 3 reveal differences in surface morphology through physical observation.

Wafer 1 exhibits a visibly rough and defect-laden surface, with several dark regions indicating large surface pits or voids and a high density of microstructural irregularities distributed across the field of view. These features are typically associated with high densities of threading dislocations propagating to the surface and can arise from poor

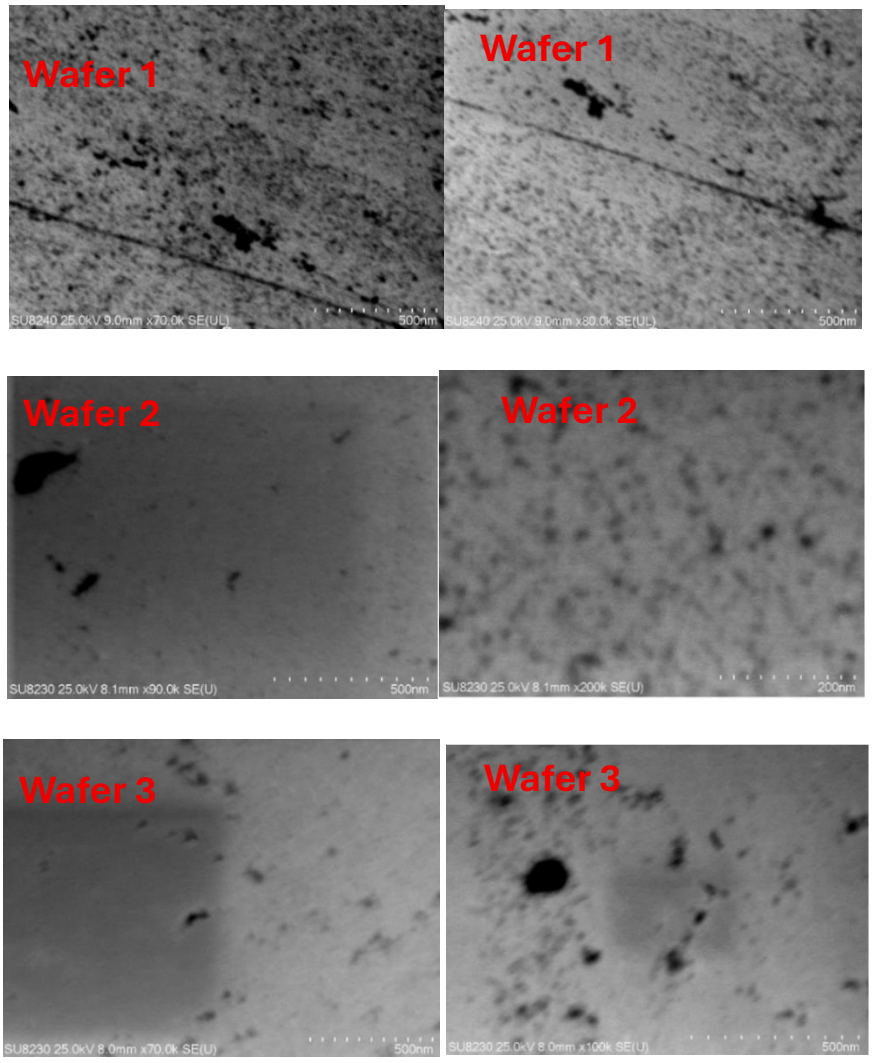


Figure 4. 17 SEM images for Wafers 1, 2 and 3. Threads of dislocations are seen to emanate from the SiC/AlN interface. Some of the threads extend through the GaN channel and the AlGaN barrier layers to the surface.

lattice matching or inadequate nucleation layer engineering. Such defects are known to promote surface states that contribute to gate leakage, current collapse, and increased surface-related trapping phenomena.

In contrast, Wafer 2 presents a markedly smoother surface with significantly fewer visible pits or structural anomalies. The visibly reduced density of surface defects suggest improved epitaxial uniformity, which aligns with the better dislocation filtering through the underlying thicker (500 nm) GaN channel layer. This quality surface morphology is indicative of reduced surface trap density, which would help minimize gate leakage and suppress gate lag behaviour.

Wafer 3 shows an intermediate surface quality. While some regions appear smooth and relatively defect-free, there are also localized areas with clusters of larger voids or pits, particularly in the right-hand image.

4.7 Conclusion

Buffer-free AlGaN/GaN HEMT architectures present several key advantages for medium-voltage power applications. Removing the conventional doped buffer layer simplifies the epitaxial structure, reduces growth time, and mitigates deep-level trap formation and buffer-related leakage. By positioning the GaN channel closer to the thermally conductive substrate, heat dissipation is significantly improved – an essential factor for devices operating under high current densities. Additionally, the absence of carbon- or iron-doped buffers minimizes trapping effects that typically degrade dynamic performance, resulting in enhanced switching efficiency and long-term reliability.

The results demonstrate that both GaN channel and AlN nucleation layer (NL) thicknesses critically influence the DC and dynamic performance of buffer-free AlGaN/GaN HEMTs on SiC substrates. Devices with a thicker 500 nm GaN channel (Wafer 2) achieved the highest drain current density (411 mA/mm) and exhibited a 100× reduction in gate leakage current compared to the reference wafer. However, the same wafer exhibited premature off-state drain leakage at high drain bias (VDS ≈ 200 V). In contrast, the wafer incorporating a thicker 100 nm AlN NL (Wafer 3) provided a balanced performance, with moderate current enhancement (368 mA/mm), suppressed gate leakage, and superior breakdown characteristics (>200 V). Pulsed-IV measurements

further revealed distinct transient responses among the wafers. The thicker GaN channel device exhibited the most pronounced threshold and pinch-off voltage shifts with increasing quiescent drain bias, indicative of drain-induced trap charging and dynamic threshold instability. Conversely, the wafer with the thicker AlN NL showed improved trap immunity and stable threshold behavior. Overall, the findings highlight a clear trade-off between current density, leakage suppression, and dynamic stability in buffer-free AlGaN/GaN HEMTs, guiding epitaxial design optimization for both RF and high-voltage power applications.

Chapter 5

Modelling and Simulation Methodology for Vertical GaN FinFETs

5.1 Introduction

Modelling and simulation constitute a vital stage in the design and optimization of advanced semiconductor devices, enabling accurate prediction of device performance prior to fabrication. This is particularly essential for GaN power transistors, where high material cost, complex epitaxial structures, and stringent process requirements make experimental trial-and-error approaches difficult. Through a physics-based simulation framework, designers can explore the influence of structural, electrical, and material parameters on device operation, thereby guiding the development of efficient, reliable, and scalable GaN-based technologies.

In this chapter, a comprehensive modelling and simulation methodology is presented for the Vertical GaN FinFET architecture. The chapter discusses on the theoretical foundation, numerical formulation, and implementation of semiconductor transport models within a Technology Computer-Aided Design (TCAD) environment. Emphasis is placed on the self-consistent solution of the fundamental semiconductor equations, Poisson's equation, carrier continuity, and drift–diffusion transport models, along with critical physical effects such as carrier mobility degradation, recombination mechanisms, impact ionization, and self-heating.

Furthermore, the TCAD modelling workflow, encompassing device structure definition, physical model selection, meshing strategy, and calibration, is systematically discussed. The simulation was carried out using Silvaco Athena for process and structural modelling, followed by Silvaco Atlas for electrical characterization under various biasing conditions. Material parameters and physical models relevant to GaN and dielectric layers (AL_2O_3, SiO_2) are described to ensure accurate representation of real device behaviour.

The outcomes of this modelling process serve as a validated predictive tool for analysing key performance metrics, such as threshold voltage, on-resistance, breakdown voltage, and electrostatic control, for the device performance evaluation presented in Chapter 6.

5.2 Objectives

This section outlines the primary objectives of simulation-driven investigations in the context of power transistor development.

5.2.1 Understanding physical behaviour at the nanoscale

Semiconductor device simulations enable the visualization and quantification of internal physical phenomena, such as electric field distribution across junctions and interfaces, carrier transport dynamics such as drift, diffusion, and velocity saturation, as well as charge trapping, recombination, and leakage mechanisms etc. By capturing these microscopic effects, simulations provide both intuitive and quantitative insight into how fundamental physical processes influence macroscopic performance metrics such as on-resistance (R_{on}), threshold voltage (V_{th}), and breakdown voltage.

5.2.2 Performance evaluation of the device architecture

Technology computer-aided design (TCAD) simulations allow systematic assessment of structural variations such as gate length, fin width, and trench depth. By providing a virtual platform for prototyping, TCAD accelerates innovation and reduces the need for costly trial-and-error fabrication.

5.2.3 Optimization of key performance metrics

Through iterative parameter sweeps (i.e. systematically varying input variables such as voltage, thickness, or doping level), simulations enable the optimization of critical device characteristics, including on-resistance (R_{ON}), breakdown voltage (V_{BR}), threshold voltage

(V_{th}), and gate capacitance. Such optimization is essential for achieving the right balance between efficiency, size, and reliability in power applications.

5.3 Fundamental Semiconductor Equations

Accurate modelling of semiconductor devices requires the self-consistent solution of fundamental physical equations that govern electrostatics, carrier transport, and recombination–generation phenomena. The device physics underlying GaN FinFET operation is governed by a system of coupled partial differential equations that describe these phenomena. The behaviour of charge carriers in semiconductor devices is fundamentally described by a coupled set of semiconductor transport equations such as Poisson's equation, the carrier continuity equations, and the drift–diffusion transport model. Collectively, these equations define how the properties such as electrostatic potential, carrier concentrations, and current densities evolve within the semiconductor under applied bias conditions. These governing equations, implemented within Technology Computer-Aided Design (TCAD) tools such as Silvaco ATLAS, form the mathematical backbone of the device simulation process.

5.3.1 Poisson's equation

Poisson's equation describes the relationship between the electrostatic potential and the local charge density. In a field-effect transistor (FET), the gate electrode does not conduct current into the channel, instead, it electrostatically controls the flow of carriers (electrons or holes) between the source and drain by modifying the electric field and potential distribution inside the channel region. The relationship between the electrostatic potential $\phi(x, y, z)$ and the charge density ρ in the device is governed by Poisson's equation expressed as follows [149]:

$$\nabla \cdot (\varepsilon \nabla \psi) = -\rho \tag{5.1}$$

where

$$\rho = q(p - n + N_D^+ - N_A^-) \tag{5.2}$$

ψ : electrostatic potential (V)

ε : permittivity of the semiconductor (F/cm)

q : electronic charge $(1.6 \times 10^{-19}\mathrm{C})$

n, p : electron and hole concentrations (cm^{-3})

N_D^+, N_A^-: ionized donor and acceptor ↓ zentrations (cm^{-3})

Solving Poisson's equation provides the spatial potential profile within the device, which directly determines the electric field distribution, carrier confinement, and threshold voltage of the transistor.

5.3.2 Carrier continuity equation

The continuity equations express the principle of charge conservation for electrons and holes. They describe how carrier densities change with time due to current flow, generation, and recombination processes. The equations are expressed as follows [149];

For electrons:

$$\frac{\partial n}{\partial t} = \frac{1}{q}\nabla \cdot \mathbf{J}_n + G_n - R_n \tag{5.3}$$

For holes:

$$\frac{\partial p}{\partial t} = -\frac{1}{q}\nabla \cdot \mathbf{J}_p + G_p - R_p \tag{5.4}$$

where:

n and p = electron and hole concentrations (cm^{-3})

$\mathbf{J}_n$ and $\mathbf{J}_p$ = current density vectors for electrons and holes $(\mathrm{A/cm}^2)$

q = electronic charge $(1.6 \times 10^{-19}\mathrm{C})$

G = carrier generation rate $(\mathrm{cm}^{-3} \cdot \mathrm{s}^{-1})$

R = carrier recombination rate $(\mathrm{cm}^{-3} \cdot \mathrm{s})$

In the FET devices, the continuity equations are solved in conjunction with Poisson's equation within the device. This coupled system determines critical operating characteristics such as channel current, leakage behaviour, and transient response.

5.3.3 Drift-diffusion equations

Carrier motion follows drift–diffusion transport model, which is one of the most widely used frameworks for describing charge carrier motion in semiconductor devices. It accounts for two fundamental mechanisms of carrier transport [149]:

1. Drift, caused by the electric field, and
2. Diffusion, caused by spatial gradients in carrier concentration

The total current density $\mathbf{J}_n$ for electrons:

$$\mathbf{J}_n = qn\mu_n\mathbf{E} + qD_n\nabla n \tag{5.5}$$

and for holes:

$$\mathbf{J}_p = qp\mu_p\mathbf{E} - qD_p\nabla p \tag{5.6}$$

where μ_n and μ_p are mobilities, D_n and D_p are diffusion coefficients, and $\mathbf{E} = -\nabla\phi$ is the electric field.

5.3.4 Carrier mobility equations

Carrier mobility (μ) defines how easily charge carriers move through a semiconductor in response to an electric field. It depends strongly on factors such as doping concentration, lattice temperature, electric field strength, and crystal quality. In device simulations, mobility is often described by empirical models that account for both low-field and high-field effects.

5.3.4.1 Low-field mobility

Low-field mobility characterizes how readily charge carriers (electrons or holes) move through a semiconductor under low electric field conditions, where their drift velocity remains linearly proportional to the applied electric field. In this regime, carrier transport is predominantly limited by scattering mechanisms such as lattice (phonon) scattering, ionized impurity scattering, and, in certain materials like GaN, piezoelectric scattering arising from polarization effects in the crystal lattice. The behaviour is commonly modelled using empirical equations like Caughey–Thomas model expressed in equation

5.7 [150]. The model captures the reduction in carrier mobility with increasing doping concentration due to enhanced impurity scattering.

$$\mu(N) = \mu_{\min} + \frac{\mu_0 - \mu_{\min}}{1 + \left(\frac{N}{N_{\text{ref}}}\right)^{\alpha}} \tag{5.7}$$

where

μ_0 = low-field mobility at low doping,

$\mu_{\min}$ = minimum mobility at high doping,

N = doping concentration,

N_{ref} = reference doping concentration, and

α = empirical fitting parameter.

5.3.4.2 High-field mobility

High-field mobility refers to the behaviour of charge carriers in a semiconductor when subjected to strong electric fields, under which their drift velocity no longer increases linearly with the field. At these elevated field strengths, carriers gain excess energy, leading to carrier heating and increased scattering, particularly through interactions with optical phonons. As a result, the drift velocity approaches a saturation limit, and the effective mobility becomes dependent on the electric field, in contrast to the constant mobility observed under low-field conditions. This phenomenon is modelled using a field dependent mobility relation, such as the Caughey-Thomas velocity saturation model [149]:

$$\mu(E) = \frac{\mu_0}{\left[1 + \left(\frac{\mu_0 E}{v_{\text{sat}}}\right)^{\beta}\right]^{\frac{1}{\beta}}} \tag{5.8}$$

where

v_{sat} = saturation velocity,

β = empirical constant describing the sharpness of transition between low-field and highfield regimes, and

E = local electric field.

5.3.5 Carrier recombination

Carrier recombination is a fundamental process in semiconductors that directly influences carrier lifetime and the trap-related leakage currents. Among the various recombination mechanisms, Shockley–Read–Hall (SRH) and Auger recombination are particularly important for determining the steady-state and transient behaviour of devices such as GaN-based FinFETs.

5.3.5.1 The Shockley-Read-Hall (SRH) recombination

This mechanism describes carrier annihilation through defect or trap states located within the semiconductor bandgap. These trap states, often arising from crystal imperfections, impurities, or dislocations, act as intermediate energy levels that facilitate recombination between electrons and holes. In GaN devices, SRH recombination is often dominant due to the relatively low intrinsic carrier concentration and the presence of defect states introduced during epitaxial growth or processing. The recombination model is expressed as [149]:

$$R_{\mathrm{SRH}} = \frac{np - n_i^2}{\tau_p(n + n_1) + \tau_n(p + p_1)} \tag{5.9}$$

where

n and p are the electron and hole concentrations,

n_i is the intrinsic carrier concentration,

τ_n and τ_p are the electron and hole lifetimes, and

n_1 and p_1 correspond to the equilibrium carrier concentrations when the trap level is at the Fermi energy for electrons and holes, respectively.

5.3.5.2 Auger recombination

Auger recombination is a three-particle interaction process in which the energy released during electron-hole recombination is transferred to a third carrier instead of being emitted as a photon. This process becomes significant at high carrier densities, such as during heavy injection or under high current operation. As carrier density increases, Auger recombination contributes to efficiency degradation and increased heat generation, which are concerns in high-power and high frequency GaN devices.

The Auger recombination rate is given by:

$$R_{\text{Auger}} = \left(C_n n + C_p p\right)(np - n_i^2) \tag{5.10}$$

where

C_n and C_p are the Auger recombination coefficients for electrons and holes, respectively.

5.3.5.3 Impact ionization

Impact ionization is a high-field phenomenon in semiconductors where energetic charge carriers gain sufficient kinetic energy from the electric field to generate additional electron–hole pairs through collisions with the crystal lattice. This process leads to carrier multiplication and can result in avalanche breakdown if the generated carriers further accelerate and trigger successive ionization events. In the vertical GaN FinFETs, impact ionization plays a crucial role in determining the breakdown voltage and high-field reliability. The model is empirically represented in equation (5.11) [149].

$$\alpha = A \exp\left(-\frac{B}{E}\right) \tag{5.11}$$

where

$\alpha =$ impact ionization coefficient (cm^{-1}),

$E =$ local electric field ($\mathrm{V/cm}$),

A and $B =$ material-dependent fitting parameters determined experimentally.

From equation (5.11), it is evident that when the impact ionization coefficients attain sufficiently high values, even a small initial current can generate a significant number of electron–hole pairs. Under an applied electric field, these newly generated carriers are accelerated, contributing to an increased current density. This elevated current further enhances the rate of impact ionization, initiating a positive feedback loop. Once this process becomes self-sustaining, the current rapidly escalates beyond controllable limits, ultimately leading to avalanche breakdown in the device.

5.3.6 Thermal effects and self-heating

Thermal effects play a critical role in determining the performance, reliability, and efficiency of modern semiconductor devices. In high-power and high-frequency transistors such as vertical GaN FinFETs, substantial self-heating can occur due to high current densities and electric fields within confined device geometries. When charge carriers move through a semiconductor under bias, they dissipate energy as Joule heating, which manifests as local temperature rise within the device. The power density of heat generation per unit volume is given by:

$$H = \mathbf{J} \cdot \mathbf{E} \tag{5.12}$$

where

H = heat generation rate $(\mathrm{W/cm^3})$,

$\mathbf{J}$ = total current density vector $(\mathrm{A/cm^2})$,

$\mathbf{E}$ = electric field vector $(\mathrm{V/cm})$.

This localized heating alters carrier mobility, threshold voltage, and saturation current, creating a strong electrothermal coupling that must be solved self-consistently with the electrical transport equations.

5.4 TCAD Modelling and Simulation

This section describes the TCAD-based modelling and simulation of a vertical GaN FinFET, developed and calibrated against the structure reported by Y. Zhang et. al [116] and illustrated in Figure 5.1.

5.4.1 Device structure

The structure shown in Figure 5.1 comprises of two main semiconductor layers: a heavily doped n^+-GaN cap layer and a lightly doped GaN drift layer. The n^+-GaN cap, with a thickness of 0.3 µm and a doping concentration of 3×10^{18} cm^{-3}, serves as the top contact region to ensure low contact resistance. Beneath it lies the 9 µm GaN drift layer, doped to 3×10^{15} cm^{-3}, which supports the main voltage drop during device operation and governs the breakdown characteristics. Table 5.1 presents the parameters reported by Y. Zhang et al. [116], which were used for modeling the conventional FinFET structure.

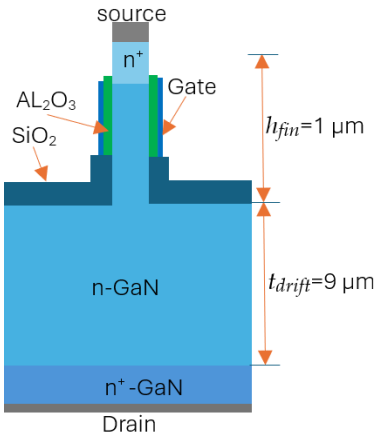


Figure 5. 1 Structure of the vertical GaN FinFET [103].

Table 5.1: Parameters Used for Modelling the Conventional FinFET

Parameter	Symbol	Value	Unit
Fin height	h_{fin}	1.0	μm
Gate length	l_g	0.2	μm
Gate oxide thickness	t_{ox}	0.3	μm
GaN drift thickness	t_{drift}	9.0	μm
GaN drift doping conc	-	$2x10^{15}$	cm^{-3}
GaN Cap layer thickness	-	0.3	μm
GaN Cap doping conc	-	$3x10^{18}$	cm^{-3}

5.4.2 Simulation models and methodology

The two-dimensional device structure of the GaN FinFET was developed using the Silvaco Athena process simulator and subsequently evaluated for electrical performance using Silvaco Atlas. The physical layout and doping profiles were initially constructed using Silvaco Athena, emulating standard fabrication steps for vertical device structures as reported in [116], then subsequently into Silvaco Atlas for electrical and physical characterization under various biasing conditions.

The material parameters for GaN and the dielectric layers used in simulating the device are presented in Table 5.2. These values represent key physical properties required for accurate TCAD modelling of the FinFET. For GaN, a bandgap energy of 3.4 eV was used, slightly overriding the default value of 3.45 eV specified in the Silvaco material library, to better align with reported experimental data. The electron mobility was set to 900 $cm^2/V{\cdot}s$ to capture the efficient transport characteristics of electrons in GaN, while the hole

mobility was fixed at 10 $cm^2/V{\cdot}s$ to reflect the intrinsic asymmetry between electron and hole transport. The effective density of states in the conduction and valence bands was defined as Nc = 2.3 × 10^{18} cm^{-3} and Nv = 1.8 × 10^{19} cm^{-3}, respectively, which govern intrinsic carrier concentrations and statistical behavior. A thermal conductivity of 130 $W/m.k$ was adopted to account for heat dissipation and self-heating effects, both of which are critical in high-power GaN devices.

For the dielectric layers, Al_2O_3 and SiO_2 were used as gate insulators mimicking what was reported in [116], and their wide bandgaps were set to 9 eV and 8.9 eV, respectively, which ensure strong carrier confinement and low gate leakage. Their dielectric constants were set to ε_r = 10.2 for Al_2O_3 and ε_r = 3.9 for SiO_2, values that directly influence gate capacitance and electrostatic control. Both materials exhibit comparatively lower thermal conductivities than GaN, with 35 $W/m.K$ for Al_2O_3 and 1.4 $W/m.K$ for SiO_2 but remain suitable for a thin insulating layers where electrical isolation is prioritized over thermal conduction.

Table 5.2: Material parameters for GaN and for dielectric materials [151] [152]

Parameter	**GaN**	**Al_2O_3**	**SiO_2**
Bandgap (E_g)	3.4 eV	9 eV	8.9 eV
Electron affinity (χ)	4.1 eV	1.0 eV	0.95 eV
Permittivity (ε_r)	8.9	10.2	3.9
Electron mobility (μ_n)	900 $cm^2/V{\cdot}s$	—	
Hole mobility (μ_p)	30 $cm^2/V{\cdot}s$	—	
Effective density of states (N_C, N_V)	N_C = 2.3e18 cm^{-3}, N_V = 1.8e19 cm^{-3}	—	
Thermal conductivity (κ) (W/mK)	130	35	1.4

To capture localized physical effects with high accuracy, a refined mesh was applied in the critical regions surrounding the fin channel, gate dielectric interfaces, source, and drain terminals as shown in Figure 5.2. Coarser meshing was used in less sensitive regions of the drift layer to reduce computational overhead, thereby achieving an optimal balance between numerical accuracy and simulation efficiency. A comprehensive set of physical models was activated to capture the unique properties of GaN and the FinFET

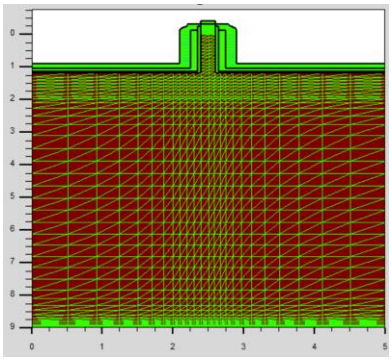


Figure 5.2. Mesh distribution along X and Y directions of the vertical GaN FinFET.

geometry accurately. These included field-dependent (FLDMOB) and concentration-dependent (CONMOB) mobility models to account for carrier mobility degradation under high electric fields and heavy doping concentrations. The doping-dependent mobility model (CONMOB) captures impurity scattering that becomes significant at high doping concentrations, while the high-field mobility model (FLDMOB) represents velocity saturation effects that occur under strong electric fields, especially relevant in high-voltage switching devices. Shockley–Read–Hall (SRH) recombination, thermal generation, and bandgap narrowing (BGN) models were used to represent realistic recombination mechanisms and temperature-dependent effects. Additionally, high-field saturation and carrier transport models suited for wide bandgap semiconductors were incorporated to capture GaN's behaviour under extreme conditions. To simulate avalanche breakdown behaviour, the Selberherr impact ionization model was employed. This enabled accurate prediction of breakdown voltage by capturing the onset of carrier multiplication in high-field regions, such as near the gate edges or trench terminations.

The simulation models enabled in the TCAD simulator are summarized in table 5.3. The models listed in the table are standard built-in physical models available in the Silvaco ATLAS simulation library [153]. Although default parameter values for these models are provided in the ATLAS manual, the simulator also allows users to specify or adjust certain parameters in order to better represent the physical behavior of a particular device or material system. In this work, some parameters were modified from their default library values to achieve appropriate calibration of the device characteristics. Specifically, the carrier lifetimes and trap energy level in the Shockley–Read–Hall recombination model, the coefficients of the Auger recombination model, and the parameters of the impact ionization model were adjusted to suitable values. These adjustments enable the

simulation to more accurately capture recombination processes, high-field carrier effects, and breakdown behavior, as reflected in the parameter values presented in the table.

Table 5.3:Physical models used in the simulation

Model Type	Model Name	Setting / Value	Purpose
Mobility	Doping-dependent (CONMOB)	Enabled: MOBILITY CONMOB	Accounts for impurity scattering
	High field (FLDMOB)	Enabled: MOBILITY FLDMOB	Models' velocity saturation
	Temp-dependent (CVT)	Enabled: MOBILITY CVT	Includes lattice scattering
Recombination	SRH	RECOMB SRH $\tau_n = \tau_p$ = 1e-6 s Trap Energy = 0.6 eV below CB	Bulk & interface traps
	Auger	RECOMB AUGER $C_n = C_p$ = 1e-31 cm^6/s	Needed in high-injection regions
Impact Ionization	SELBERG	IMPACT SELB A = 3.3e6 cm^{-1} B = 1.0e7 V/cm	For breakdown voltage estimation
Bandgap Narrowing	BGN	BGN $\Delta Eg \approx 0.01–0.02$ eV for ND > 1e18 cm^{-3}	Narrows bandgap in highly doped regions
Statistics	Fermi	FERMI	Accurate carrier distribution at high doping
Interface Charge	Fixed Charge	INTERFACE CHARGE = 1e12 cm^{-2} (GaN/oxide)	Affects Vt and leakage
Lattice Heating	Thermal Model	Enabled: Lat.temp	Models self-heating / Joule heating

The Shockley–Read–Hall (SRH) recombination, with lifetimes of $\tau_n = \tau_p$ = 1 μs and trap energy levels set 0.6 eV below the conduction band, accounts for bulk and interface traps which dominate in GaN-based structures. Auger recombination was included with coefficients of $C_n = C_p = 1\times10^{-31}$ cm^6/s to capture non-radiative recombination processes that become important under high carrier injection conditions.

Avalanche breakdown behavior was modelled using the Selberherr impact ionization formulation. This model accurately predicts the onset of carrier multiplication in high-field regions, enabling reliable estimation of breakdown voltage.

To account for band structure modifications at high doping, the bandgap narrowing (BGN) model was activated, with ΔE_g in the range of 0.01–0.02 eV for doping concentrations above 1×10^{18} cm^{-3}. This effect is critical for capturing realistic carrier concentrations and threshold voltage behavior. Carrier statistics were modeled using the Fermi–Dirac distribution (FERMI), which provides improved accuracy over the Maxwell–Boltzmann approximation under high doping levels typical of GaN power devices.

Interface effects were included by specifying a fixed charge density of 1×10^{12} cm^{-2} at the GaN/oxide interface, which directly influences threshold voltage stability and gate leakage characteristics. Additionally, the temperature-dependent CVT model incorporates lattice scattering, ensuring that thermal effects on carrier transport are accurately represented. Together, these models provide a realistic description of carrier dynamics under varied operating conditions. Finally, lattice heating was invoked by enabling the self-heating or Joule heating command (LAT.TEMP), allowing the thermal coupling between electrical power dissipation and device temperature rise to be resolved. This is essential for evaluating reliability and performance under high-power operation.

This methodology enabled the extraction and analysis of key device characteristics such as transfer and output behaviour, breakdown voltage, short-channel effects like drain induced barrier lowering (DIBL), and gate control efficiency, providing comprehensive insight into the electrostatic and transport performance of the GaN FinFET. To ensure accuracy and reliability of the simulation, the results obtained from the modelled device were calibrated against experimental data reported in [116], and the comparative results are presented in the output characteristics (I_{ds}–V_{ds} and I_{ds}–V_{gs} curves) in Figures 5.3 and 5.4. All values are normalized to the fin area of the devices of 2×10^{-9} cm^2.

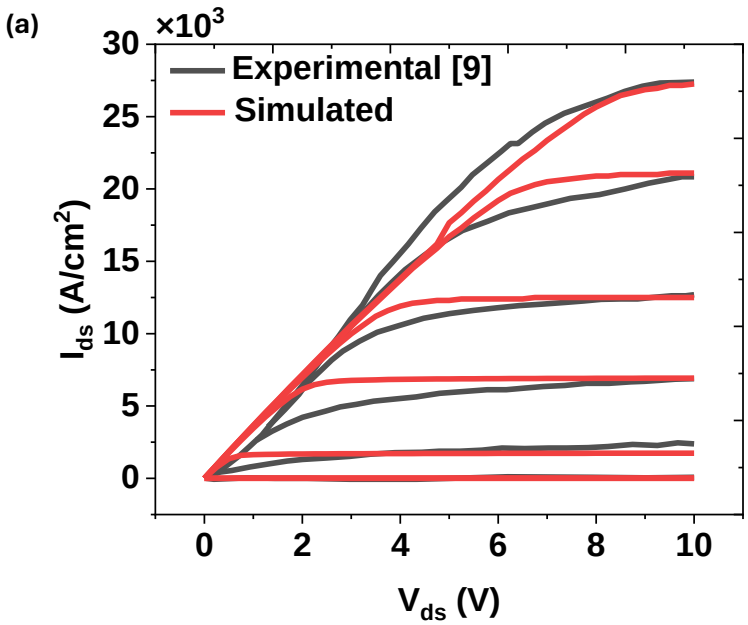


Figure 5.3. Calibration of simulated Ids–Vds characteristics against experimental measurements reported in [116]

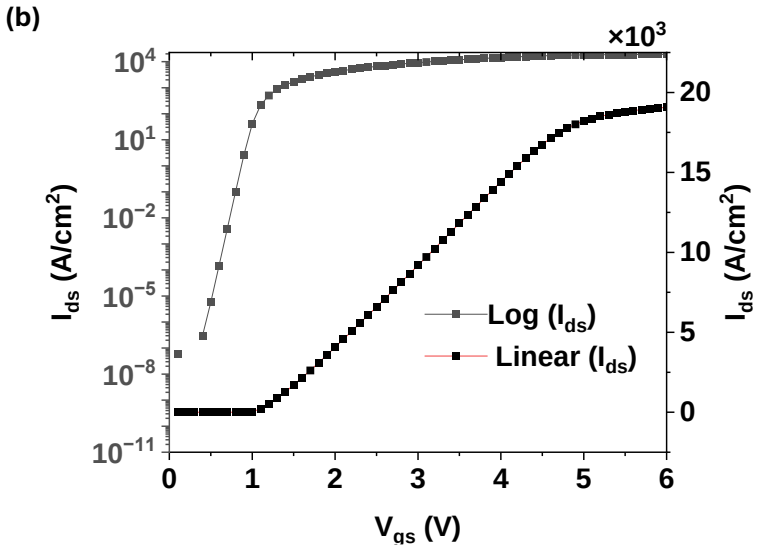


Figure 5. 2 Calibration of simulated Ids–Vgs characteristics against experimental measurements reported in [116]

5.5 Summary

Owing to the high fabrication cost and material challenges associated with GaN devices, simulation-based approaches were employed to predict device behaviour and optimize performance before experimental fabrication. This chapter presented a detailed framework for the modelling and simulation of the of the vertical GaN FinFET structure with a reference to an experimentally fabricated device.

The chapter stated the objectives of simulation-driven analysis, which include understanding nanoscale physical behaviour, evaluating architectural variations, and optimizing key performance metrics such as threshold voltage, on-resistance, and breakdown voltage. Fundamental semiconductor equations forming the basis of TCAD simulations were then discussed. These include Poisson's equation for electrostatics, carrier continuity equations for charge conservation, and drift–diffusion models for current transport. Supplementary models for carrier mobility (both low-field and high-field regimes), recombination mechanisms (Shockley–Read–Hall and Auger), impact ionization, and thermal effects were detailed, emphasizing their importance in accurately predicting device operation under various bias and temperature conditions.

Subsequently, the chapter described the implementation of the simulation methodology within the Silvaco TCAD environment, including structure development in Athena and

electrical characterization in Atlas. The simulated device consisted of an n^+-GaN cap layer and a lightly doped GaN drift region, with material parameters carefully chosen and tabulated for GaN and dielectric layers (Al_2O_3 and SiO_2).

A wide range of physical models were activated to capture realistic device physics — including field-dependent and doping-dependent mobility (FLDMOB, CONMOB), recombination models (SRH, Auger), impact ionization (Selberherr model), bandgap narrowing, Fermi–Dirac statistics, and self-heating effects. Interface fixed charges were also considered to account for gate oxide interactions.

Finally, model calibration was performed by comparing simulated transfer (I_{ds}–V_{gs}) and output (I_{ds}–V_{ds}) characteristics with reported experimental data, demonstrating strong agreement and validating the accuracy of the developed simulation framework.

Overall, this chapter established a robust and physics-based TCAD modelling methodology that provides a predictive foundation for analysing, optimizing, and validating the Vertical GaN FinFET architecture discussed in the next chapter.

Chapter 6

Gate Wrap-around Vertical GaN FinFET: A TCAD Study

6.1 Introduction

This chapter presents a comprehensive TCAD-based investigation of a novel gate wrap-around (GW) vertical GaN FinFET architecture aimed at addressing key limitations of conventional GaN power devices. The motivation for this study arises from the need to achieve superior electrostatic control, higher breakdown voltage, and enhanced device reliability, all of which are critical for high-power switching applications.

The TCAD simulation framework is described, and simulation results are analysed in detail, including drain current–voltage characteristics, breakdown voltage behaviour, threshold voltage stability, and drain-induced barrier lowering (DIBL) effects. The performance of the GW-FinFET is benchmarked against that of a conventional vertical FinFET, demonstrating the advantages of the wrap-around gate in improving gate control, and achieving higher breakdown resilience. A description of the fabrication process for the fin structure is also provided.

6.2 Proposed GW GaN FinFET

The conventional vertical GaN FinFET typically consists of a vertical fin-shaped channel etched into the GaN layer, with a gate positioned adjacent to the sidewalls of the fin [116]. This configuration offers a certain level of electrostatic control over the channel, however, its low threshold voltage increases the risk of unintended turn-on due to thermal fluctuations and noise in practical applications. Enhancing gate modulation requires further thinning of the fin channel, however, this exacerbates access resistance and intensifies self-heating effects, potentially degrading overall device performance. Moreover, though this structure has demonstrated high breakdown voltage and low on-resistance, further optimization and electric field management could lead to enhanced breakdown performance.

Here, we propose a novel gate wrap-around (GW) vertical GaN FinFET (GW-FinFET) architecture, wherein the gate electrode fully surrounds the vertical fin channel with a conformal geometry. By extending the gate coverage to the top and all sidewalls of the fin, the proposed design ensures uniform and stronger electrostatic coupling across the entire channel. This enhanced gate control enables more precise modulation of the channel potential, leading to an improved threshold voltage characteristic, reduced leakage currents, and enhanced blocking capability

Similar concepts, such as gate-all-around (GAA) and wrap-around-gate structures, have been investigated in planar silicon and GaAs devices [154], [155], [156], [157], [158]. To the best of our findings, the proposed device geometry has not been reported in vertical GaN FinFET. Using TCAD simulations, the proposed structure is comprehensively analysed and benchmarked against the conventional vertical GaN FinFET (Conv-FinFET). Key electrical parameters including breakdown voltage, threshold voltage, and forward conduction current are extracted and compared. The simulation results demonstrate that the GW -FinFET gate structure yields a better threshold and breakdown voltage performance compared to Conv-FinFET.

6.2.1 Motivation and research objective

Gate-all-around (GAA) and wrap-around-gate architectures have demonstrated significant improvements in electrostatic control for planar silicon and GaAs technologies, yet such concepts remain largely unexplored in vertical GaN FinFET designs. This gap in research presents an opportunity to develop innovative device structures that exploit GaN's material advantages while overcoming the limitations of existing architectures. The objective of this research, therefore, is to evaluate a novel gate wrap-around vertical GaN FinFET (GW-FinFET) architecture in which the gate electrode fully envelops the fin channel, ensuring stronger and more uniform electrostatic coupling. The successful demonstration of this will establish it as a promising candidate for future GaN-based power electronic applications.

6.2.2 Device target specifications

The development of the proposed GW-FinFET is guided by stringent target specifications that address the requirements of high-performance power electronic applications. The

device is designed to achieve a breakdown voltage exceeding 1200 V, thereby ensuring robust blocking capability under medium- to high-voltage operation. A well-controlled threshold voltage in the range of 1–2 V is targeted to provide stable switching margins and reduce the risk of parasitic turn-on. In addition, low specific on-resistance is pursued to minimize conduction losses while maintaining high efficiency, complemented by an enhanced forward current capability compared to conventional vertical GaN FinFETs.

6.3 Structure of the GW-FinFET

The proposed structure shown in Figure 6.1 retains the fundamental concept of the conventional design discussed in Chapter 5, while introducing key innovations in geometry and fabrication methodology. In the novel vertical GaN GW-FinFET, the etched fin is completely enclosed by a conformal gate stack. The proposed device maintains the same geometric dimensions and doping profile as the conventional FinFET summarized in Table 5.1, including the fin height (h_{fin}) drift region thickness (t_{drift}), doping concentrations of the n+-GaN cap layer and the GaN drift layer, as well as the corresponding layer thicknesses. However, unlike the conventional structure, a bilayer of Al_2O_3 dielectric is deposited in two distinct stages, as described in Section 6.1. This dielectric conformally wraps around the entire fin structure, followed by the deposition of the gate stack on top, as illustrated in Figure 6.1.

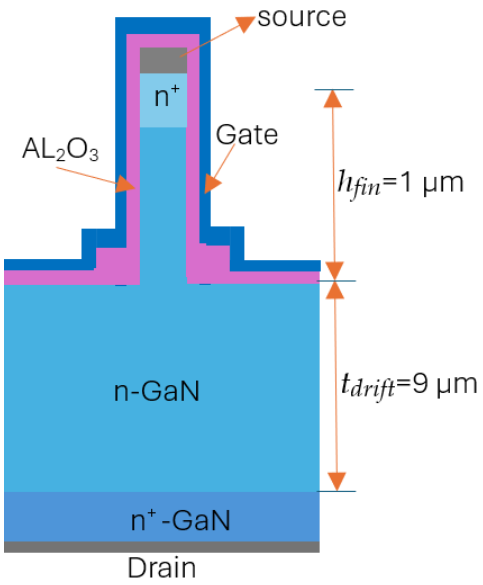


Figure 6. 1 is the proposed structure of the GW GaN FinFET showing various layers and dimensions.

In addition to the performance improvements predicted by the simulation results presented in the following sections, this structure also offers a simplified fabrication approach as illustrated in figure 6.13. The proposed process eliminates several etch-back and deposition steps typically required during gate and dielectric formation, thereby improving process simplicity and enhancing fabrication reproducibility.

6.4 Modelling and Simulation of the GW-FinFET

The modelling and simulation framework of the conventional vertical GaN FinFET described in Chapter 5 was used to model and simulate the proposed GW-FinFET device. All models, material properties, physical parameters, and bias conditions were kept the same to those used in Chapter 5 (Table 5.2) to ensure consistency and enable an accurate comparison of the characteristics and performance of the two device structures.

6.4.1 Output characteristics of the GW-FinFET

The drain current saturation characteristics of the conventional and proposed GaN FinFET were obtained by sweeping the drain-to-source voltage (V_{ds}) from 0 to 10 V, while increasing the gate-to-source voltage (V_{gs}) from 0 to 6 V in 1 V steps. This biasing scheme allowed the extraction of output characteristics under progressively stronger channel inversion. Figures 6.2 and 6.3 show the simulated current-flow line contours of the conv-FinFET and the GW-FinFET respectively, which reveal the distribution of carrier transport from source to drain through the fin channel and into the drift region. At V_{gs} = +6 V, the results indicate pronounced current crowding along the fin sidewalls in both structures, where the gate exerts the strongest electrostatic control, while the current density at the fin centre remains comparatively weaker. As the carriers exit the fin, the current streamlines expand and spread into the drift region, reflecting vertical current spreading and resistance-limited conduction typical of vertical GaN FinFET structures.

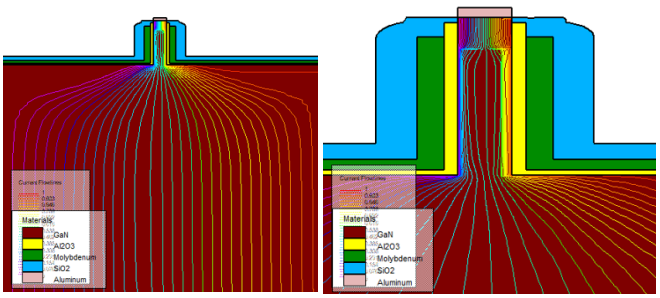


Figure 6.2 2D Cross-section of the simulated conventional GaN FinFET structure showing current flow line contours. The vertical current flows from the drain electrode beneath to the source as captured in this image.

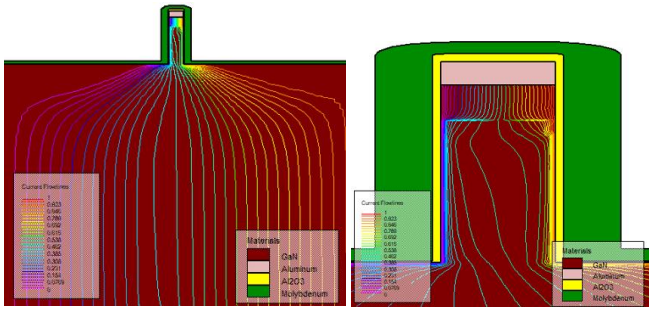


Figure 6.3 2D Cross-section of the simulated GW- GaN FinFET structure showing current flow line contours. The vertical current flows from the drain electrode beneath to the source as captured in this image.

Figure 6.4 presents the simulated I_{ds}–V_{ds} characteristics of the conventional and GW vertical GaN FinFETs. The GW-FinFET demonstrates a slightly higher drain current compared to the conventional design, indicating improved carrier conduction and enhanced current drive capability under bias.

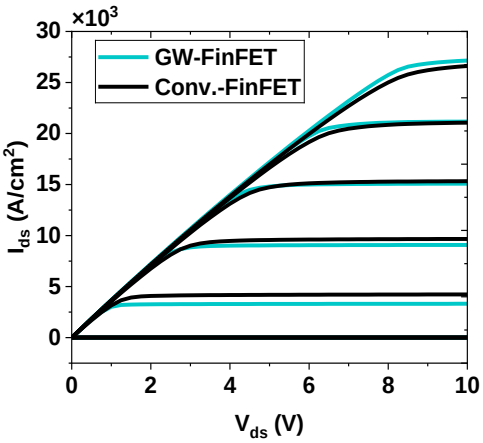


Figure 6.4 Comparison of Ids–Vds Characteristics for Conventional FinFET and GW-FinFET for a Vds swept from 0 to 10 V at various Vgs from 0 to 5V. The Ids for the GW-GaN FinFET is slightly higher than the conventional GaN FinFET

Figure 6.5 (a) and (b) shows the electron mobility profiles across the fin channel for both the conventional and GW FinFET which help to clarify this behavior. In both devices, the peak mobility occurs at the center of the fin channel, where the carrier concentration is lower, and scattering is minimal. Toward the fin sidewalls adjacent to the gate oxide and near the heavily doped cap layer, the mobility gradually decreases due to enhanced carrier scattering and impurity-related effects. This degradation is consistent with field-induced and doping-induced scattering mechanisms that typically dominate near high-field or heavily doped regions.

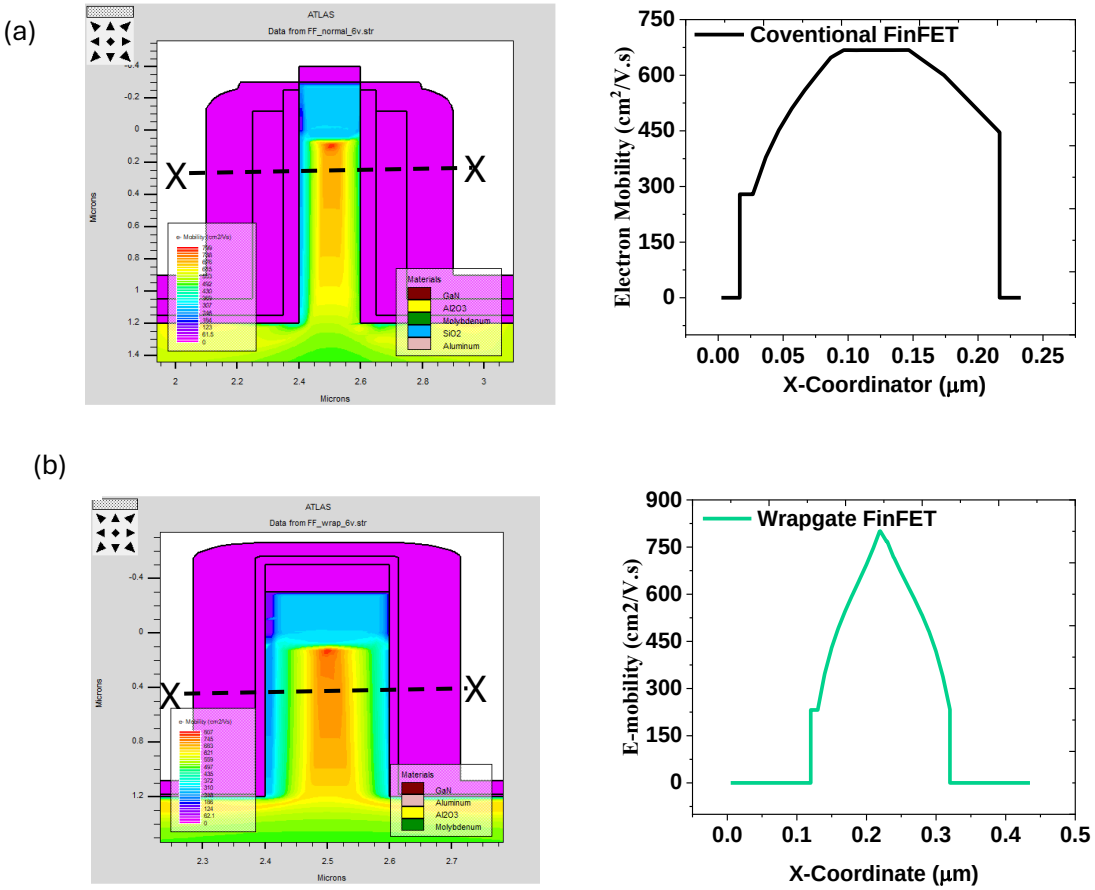


Figure 6.5. Electron mobility profiles for (a) conventional FinFET and (b) GW-FinFET structures. The X–X cross-section illustrates the variation of electron mobility across the fin width. In both devices, mobility decreases near the fin sidewalls and reaches its maximum near the center. The electron mobility in the GW-FinFET appears to be higher (~800 cm²/V.s) than in the conventional FinFeT (~700 cm²/V.s)

It can be noted from figure 6.5a and b that the GW-FinFET exhibits a modestly improved peak mobility profile (~800 cm²/V.s) relative to the conventional device (with ~680 cm²/V.s). We attribute this improvement to the gate wrap-around geometry, which

reduces localized field crowding, and suppresses excessive carrier scattering at the fin sidewalls. The resulting enhancement in mobility contributes to its superior performance, enabling more efficient carrier transport through the channel under applied bias. This observation, as illustrated, confirms that the GW-FinFET achieves improved transport efficiency compared to its conventional counterpart.

6.4.2 Threshold voltage and DIBL effect

Figure 6.6 shows the transfer characteristic curves of the conventional and proposed device obtained by sweeping V_{gs} from 0 to 6V at fixed V_{ds} of 1 V. The proposed GW GaN FinFET shows a slightly higher threshold voltage of ~1.3 V, whereas that of the conventional device is 1.0 V. This ~0.3 V shift in turn-on voltage is a direct reflection of the enhanced gate control provided by the gate geometry which aligns with the fundamental design goals of next-generation GaN FinFET architecture intended for power electronic applications.

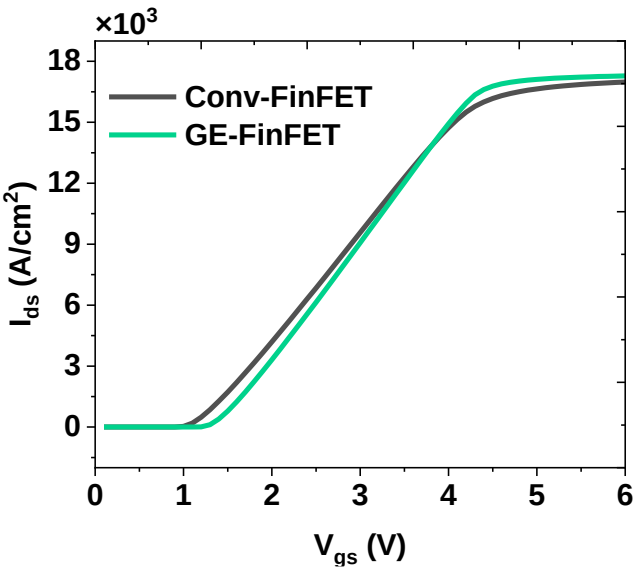


Figure 6.6 shows the transfer characteristics curves of conventional and GW vertical GaN FinFETs obtained by sweeping Vgs from 0 to 6 V at Vds=1 V. A slightly higher threshold voltage of ~1.3 V was obtained for the GW-FinFET against the conventional with Vth of ~1 V.

To analyse the stability of the threshold voltage under high-stress conditions, a drain induced barrier lowering (DIBL) behaviour of the GaN FinFETs were evaluated using transfer characteristics (I_{ds}-V_{gs}) across a range of drain-source voltages (V_{ds}) from 5 V to 25 V, with the gate-source voltage (V_{gs}) swept from –3 V to 6 V. The results are shown in Figure 6.7 and offer insight into the electrostatic integrity and short-channel effects of the

device. In the GW-FinFET, the threshold voltage (V_{th}) exhibited a minor shift approximately corresponding to a DIBL of ~ 2.5 mV/V. This small shift indicates strong electrostatic gate control and minimal influence of the drain field on the channel. In comparison, the conventional vertical GaN FinFET demonstrated a larger shift in V_{th} resulting in the DIBL of ~7.5 mV/V, nearly three times higher than that of the GW-FinFET. This result highlights the enhanced threshold voltage stability and superior short-channel effect suppression achieved by the gate-wrapped architecture.

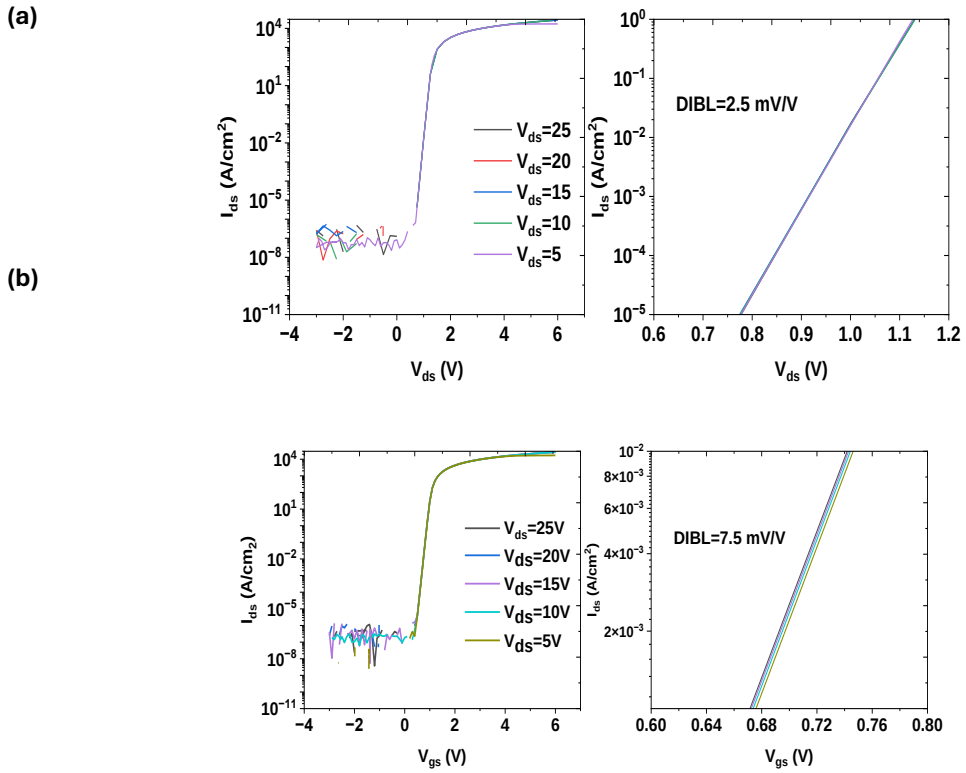


Figure 6. 7. Ids-Vgs transfer curves comparing DIBL and drain leakage characteristics for the (a) GW-FinFET and (b) conventional FinFET measured across a range of drain-source voltages (V_{ds}) from 5 V to 25 V, with the gate-source voltage (V_{gs}) swept from –3 V to 6 V. The extracted DIBL values for the GW-FinFET and the conventional FinFET are approximately 2.5 mV/V and 7.5 mV/V, respectively, indicating significantly improved gate control in the GW-FinFET architecture.

To further investigate device robustness, both structures were subjected to elevated drain voltages ranging from 100 V to 800 V while maintaining the same gate–source voltage sweep from –3 V to 6 V. The results, shown in Figure 6.8(a) and (b) for the GW-FinFET and the conventional FinFET, respectively, reveal no significant additional shift in threshold voltage compared to that observed at lower drain voltages (5–25 V). This indicates that both devices, preserve strong electrostatic integrity and exhibit stable

operation even under extreme high-voltage stress conditions. However, it is important to note that at such high drain biases, the observed stability must be interpreted cautiously, as effects like impact ionization or punch-through could become non-negligible in practical implementations. Furthermore, the discussion of elevated drain voltages must be considered within the limits of the modelling framework established in Chapter 5. The TCAD model was calibrated against experimental data within a defined drain-voltage range (V_{ds}=0 to 10 V), and the extracted physical parameters (e.g., mobility models, impact ionization coefficients, trap parameters, and contact resistances) are therefore validated only within that bias window. Extrapolation to significantly higher drain voltages (V_{ds}>100 V) may introduce increasing uncertainty, particularly in regimes where high-field effects such as enhanced impact ionization, self-heating, dynamic trapping, or premature breakdown mechanisms become dominant. Since these effects were not independently calibrated beyond the validated voltage range (V_{ds}=0 to 10 V), the predictive capability of the model under extreme bias conditions should be interpreted qualitatively rather than quantitatively. Consequently, conclusions drawn at elevated drain voltages indicate trends and physical insight but should not be regarded as fully validated predictions without additional high-voltage experimental calibration.

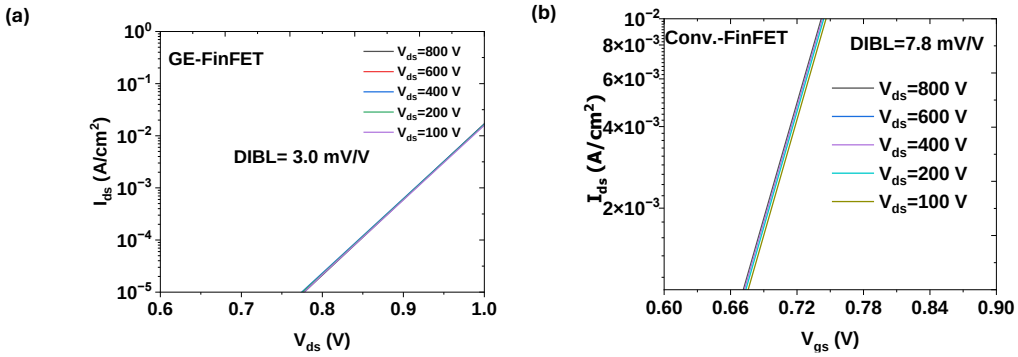


Figure 6.8 Idss-Vg transfer characteristics swept at higher Vds (100-800 V) for the (a) GW-FinFET and (b) conventional FinFET to investigate the DIBL effect at higher voltages. As shown in the curves, no significant differences is obtained compared to measurements taken at lower voltages (0-25 V) as shown in figure 6.7

6.4.3 C-V Characteristics

Figure 6.9 shows the capacitance–voltage (C–V) characteristics of two distinct vertical GaN FinFET structures which provide information on gate control efficiency and channel modulation behaviour. In the GW-FinFET structure, the capacitance remains nearly

constant at approximately 2.5 μF/cm^2 from V_{gs}=0 V to ~3.5 V, indicating that the device remains in a non-conductive or subthreshold regime. In this range, the gate voltage is insufficient to significantly form a conduction channel, and the capacitance is primarily dominated by depletion effects, with minimal variation in response to the gate bias. At around V_{gs}= 3.5 V, a sharp rise in capacitance is observed, peaking at approximately 22 μF/cm^2 by V_{gs}= 4 V. This increase reflects strong electrostatic coupling between the gate and the channel, resulting in effective carrier accumulation and enhanced channel conduction. The steep slope in the C–V curve during this transition highlights the effectiveness of the gate-engineered structure in modulating the channel potential. In contrast, the conventional vertical GaN FinFET exhibits a significantly lower initial capacitance of about 0.27 μF/cm^2, which remains nearly flat up to V_{gs}= 3.8 V. The subsequent increase in capacitance is more gradual, peaking at ~3 μF/cm^2 by V_{gs}= ~4.3 V. This behaviour indicates weaker gate-channel coupling and reduced electrostatic control over the channel. Beyond the transition region, both devices reach a saturation stage, where the capacitance flattens. Any further increase in gate voltage will no longer significantly affect the channel charge. In this regime, the total capacitance approaches the geometric or insulator capacitance limit of the device. Notably, the GW-FinFET

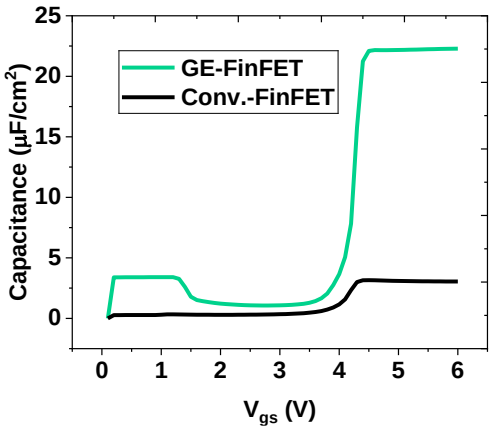


Figure 6. 9. presents the capacitance–voltage (C–V) characteristic curves of the GE- and conventional vertical GaN FinFET measured at a fixed drain-source voltage of 5 V with gate voltage swept from 0 to 6 V. In the GW-FinFET, the capacitance stays nearly constant (~2.5 μF/cm²) from VGS=0V_{GS}=0VGS=0 to ~3.5 V, reflecting a subthreshold regime where depletion effects dominate and channel formation is minimal. Beyond ~3.5 V, the capacitance increases sharply, reaching ~22 μF/cm² at VGS=4V_{GS}=4VGS=4 V, indicating strong gate–channel coupling, carrier accumulation, and effective channel conduction.

achieves more-than sevenfold saturation capacitance (~22 μF/cm^2) of the conventional structure (~3 μF/cm^2). This highlights the enhanced electrostatic control offered by GW-FinFET.

6.4.4 Breakdown voltage

Figure 6.10 (a) and (b) show the electric field distribution contours for the two distinct structures with V_{ds} swept to 2000 V while the gate bias held at -10 V. They reveal localized field crowding at the gate–dielectric interface, particularly at the sharp bottom corners of the gate. These regions act as hotspots where avalanche breakdown is most likely to initiate. Figure 6.11 shows the breakdown voltage characteristics of both the conventional and the proposed GW-GaN FinFETs for V_{ds} from 0 to 2000 V under a high negative V_{gs} of -10 V to ensure complete channel pinch-off. The GW-FinFET demonstrates a markedly higher breakdown voltage, approximately 70% greater, achieving 1430 V as opposed to 840 V for the conventional structure, as illustrated in Figure 6.12. This significant improvement is attributed to the superior electrostatic control provided by the wrap-around gate geometry, which enforces more uniform modulation of the channel potential and promotes even redistribution of the electric field along the fin sidewalls and drift region.

Cross-sectional electric field profiles along the X–X axis, shown in Figures 6.12 (a) and (b), further highlight the differences between the two architectures. While both devices exhibit localized peaks near the oxide–semiconductor interface at the gate corners, the GW-FinFET effectively suppresses the intensity of these peaks. This reduction in field concentration mitigates premature avalanche generation and enables the device to sustain higher voltages before breakdown occurs.

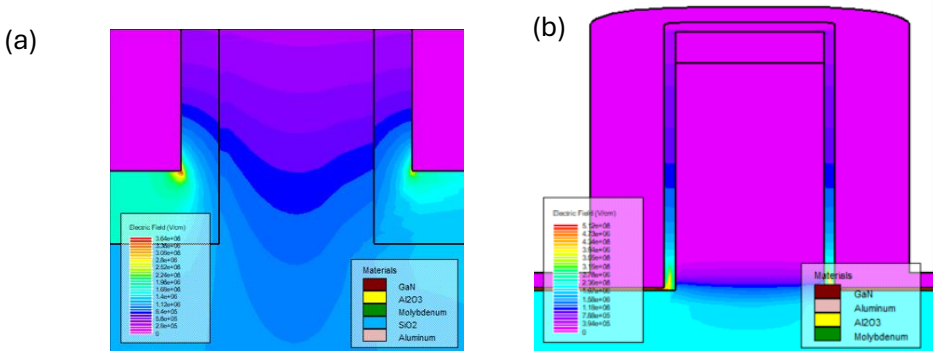


Figure 6.10. Electric field profile of (a) Conventional FinFET and (b) GW-FinFET structures

This observation is supported by electric field contour plots extracted from the GE-FinFET at intermediate voltages below its breakdown threshold (870 and 1430 V). At 870 V, the extracted electric field peak was approximately 0.7 MV/cm. For V_{ds}=1200 V, below the final breakdown voltage, the peak field increased to 2.6 MV/cm, and at breakdown (1430 V) it reached 4.8 MV/cm. In contrast, the conventional device, at its maximum breakdown

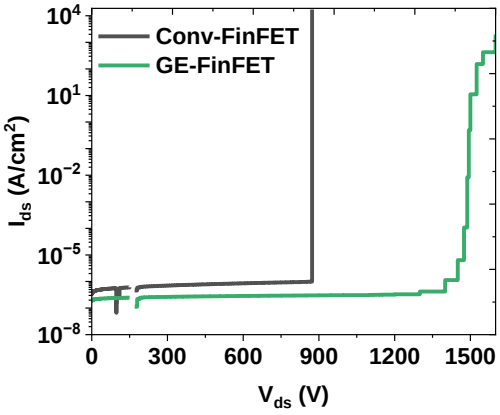


Figure 6. 11. Breakdown voltage curve of the conventional and the GW-FinFETs measured by sweeping Vds from 0 to 2000 V at high Vgs of -10 V to completely turn-off the devices. A significantly much higher breakdown voltage of ~1430 V was obtained from the GW-FinFETs against 870 V obtained from the conventional FinFET.

voltage of 840 V, exhibited an electric field peak of approximately 3.6 MV/cm, more than 5× the field strength seen in the GE-FinFET at around the same voltage. This comparison, as illustrated in Figure 6.12 (a) and (b), highlights the superior field management capabilities of the gate-enclosed design, which contributes to its higher voltage-blocking performance under high-stress conditions.

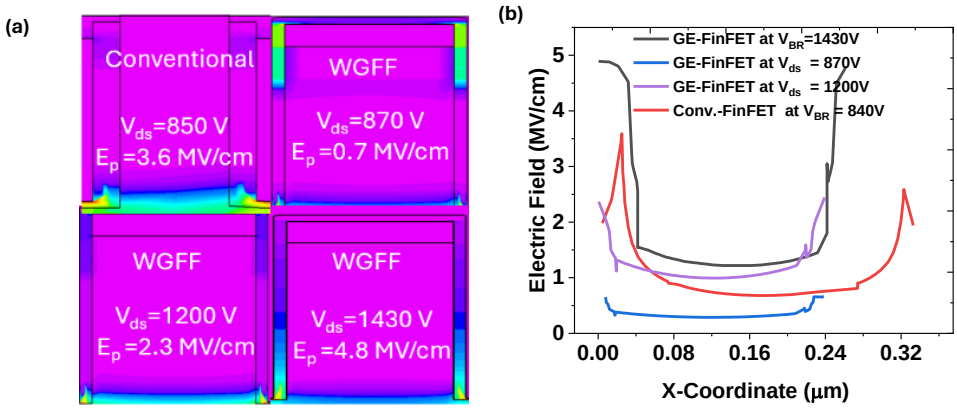


Figure 6.12. Diagram (a) and (b) comparing the electric field peaks (Ep) of conventional GaN FinFET at its maximum breakdown voltage with that of wrap-around-gate Vertical GaN FinFET structure at voltages before breakdown and at breakdown.

6.5 Proposed Fabrication Process for the GW-FinFET

The fabrication process of the proposed Gate Wrap-around FinFET (GW-FinFET) is similar in principle to that of the conventional vertical GaN FinFET but is significantly simplified by eliminating the need for precision-timed resist trimming steps. In this architecture, the fin channel is entirely enveloped by a conformal gate stack, allowing uniform gate coverage across the top and sidewalls of the fin. The simplified process flow is illustrated in Figure 6.13 and is described as follows.

The process begins with fin definition and etching, where a vertical fin channel is patterned and etched from the GaN epitaxial structure to form the active conduction path. This is followed by the deposition and patterning of the first Al_2O_3 dielectric layer, which serves both as a gate insulator and an initial isolation barrier. Once the dielectric is established, source contacts and pads are formed to provide electrical access to the source terminals, along with the definition of gate and source pad regions for subsequent metallization.

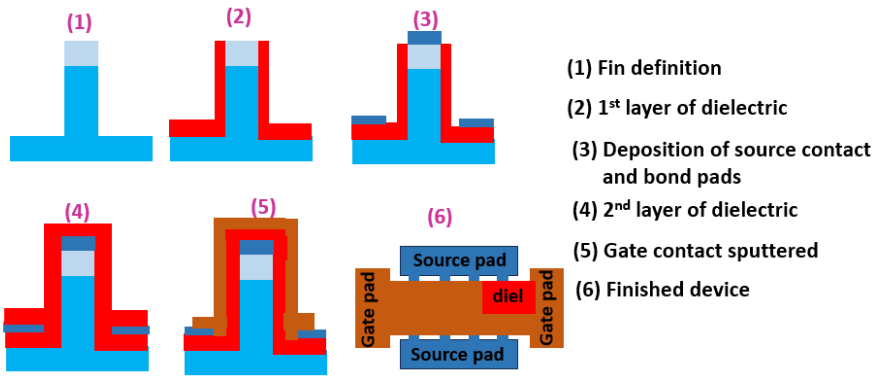


Figure 6. 13. Proposed fabrication steps for the GW-FinFET

A second Al_2O_3 dielectric layer is then deposited to further reinforce electrical insulation between the gate and source regions, ensuring stable device operation and mitigating parasitic leakage. Following dielectric deposition, the source metal contacts are evaporated to establish robust ohmic connections to the source regions. Finally, the gate metal is sputtered, fully wrapping around the fin structure and conformally covering its top and sidewalls to complete the gate wrap-around geometry.

The resulting structure incorporates distinct source and gate pads, symmetrically arranged around the fin channel, ensuring both reliable electrical isolation and efficient access for testing.

6.6 Fabrication of Fin Structure Using a Hard Mask as Etch Mask and Source Contact

In the conventional fabrication method of a GaN FinFET, a hard mask (e.g., Ni, Cr, or NiCr) is used to etch and define the fin geometry. Afterward, the mask is removed, followed by the deposition of a conformal gate layer and the source contact. In this scheme, however, the hard mask is intentionally left in place and repurposed as the source contact.

To demonstrate this concept of a dual-purpose etch mask (simultaneously defining the fin during etching and functioning as the source contact) preliminary experiments were conducted to fabricate the fin-shaped structure as shown in figure 6.14. A Ti/Al/NiCr (30/400/50 nm) metal stack was deposited, where Ti served as an adhesion layer to GaN, Al enabled the formation of a low-resistance ohmic contact, and NiCr acted as a protective capping layer, a durable etch mask and the source contact.

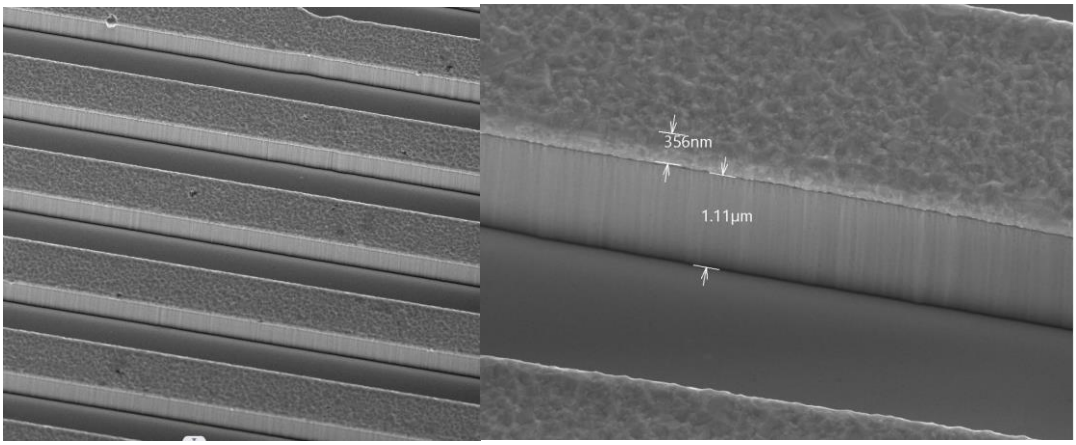


Figure 6.14 SEM image of self-aligned dual purpose source contact for GW-FinFET

The inclusion of NiCr in the stack offers significant advantages: its high hardness and resistance to Cl-based etch chemistries improve selectivity during anisotropic etching, and its stability under high plasma power helps maintain pattern fidelity. However, potential drawbacks include increased series resistance compared to established metal capping layers.

Fin definition was performed using photolithography on a Mask Aligner 6, followed by anisotropic dry etching with a BCl_3/Cl_2 plasma, in which the NiCr layer functioned as the primary hard mask while the underlying Ti/Al contributed to ohmic behaviour. Post-etch a TMAH surface treatment at 75 °C was employed to reduce plasma-induced damage, smoothen the fin sidewalls, and ensure reproducibility. The SEM image of the fabricated fin structure is presented in Figure 6.14, provides a visual confirmation of the defined geometry achieved through the concept.

It should be noted that this proof-of-concept experiment demonstrates only the feasibility of employing the hard mask as a dual-purpose layer for fin definition and source contact formation. It does not confirm the electrical performance of the device, which can only be assessed after full device fabrication and subsequent electrical characterization.

6.7 Conclusion

The proposed GW-FinFET architecture offers several key benefits for advancing GaN-based power electronics. Simulation results showed enhanced gate coupling, lower leakage currents, and higher the blocking voltage. In addition, the proposed structure, potentially reduces fabrication complexity, and so improves manufacturability and scalability. In summary, the GW-FinFET is potentially a strong candidate for next-generation power electronic systems.

Chapter 7

Thesis Summary

This thesis has explored the design, fabrication, characterization, and modelling of GaN-based power electronic devices, with emphasis on understanding material properties, device architectures, influence of epitaxial layer and strategies for achieving reliable device operation. Across the seven chapters, a comprehensive study has been presented that integrates both experimental and simulation approaches to advance the state of GaN power electronics.

7.2 Process Achievements

i. Systematic analysis of GaN material properties and device-level challenges within various power electronic application spaces.

ii. Comparative evaluation of different enhancement-mode techniques (recessed gate, fluorine implantation, p-GaN gate) and their reliability trade-offs.

iii. Experimental fabrication and characterization of buffer-free AlGaN/GaN HEMTs with optimized epitaxial designs.

iv. Development of a TCAD-based framework for studying GaN device architectures, calibrated against experimental data.

v. Proposal and validation of a novel gate wrap-around vertical FinFET structure, demonstrating significant improvement in electrostatic control and breakdown voltage, featuring a simplified fabrication process.

vi. Initial experimental steps toward practical fabrication of vertical FinFETs using innovative processes.

7.3 Novelty of the Thesis

This thesis makes significant contributions to the field of GaN-based power electronics through two original research directions:

1. Impact of channel and nucleation layer thicknesses on buffer-free AlGaN/GaN HEMTs

A significant contribution of this research lies in its systematic investigation of the impact of channel and nucleation layer thicknesses on buffer-free AlGaN/GaN high electron mobility transistors (HEMTs). The research focuses on understanding how variations in the nucleation and channel layer thickness influence key device performance parameters. Through a combination of carefully controlled fabrication processes and comprehensive electrical and structural characterization, the study establishes clear and quantitative correlations between epitaxial design choices and resulting device metrics, including current conduction, breakdown voltage, and thermal stability. The findings not only deepen understanding of epitaxial optimization for high-performance HEMTs but also highlight the potential advantages of simplifying wafer structures. This approach offers promising routes toward improved thermal management, enhanced device reliability, and reduced manufacturing complexity in GaN HEMT technology.

2. Gate wrap-around vertical GaN FinFET: A TCAD study

Vertical device architectures are widely regarded as the next frontier in high-power GaN electronics, offering superior scalability and power-handling capabilities compared to their lateral counterparts. Nonetheless, these devices continue to face significant challenges, including limited gate control, pronounced short-channel effects arising from the pursuit of e-mode operation, and increased fabrication complexity.. In this context, this thesis introduces and investigates, for the first time, a gate wrap-around (GW) vertical GaN FinFET structure using advanced TCAD simulations. Simulation results show that the GW-FinFET architecture exhibits markedly improved electrostatic control, and enhanced breakdown voltage capability relative to conventional vertical FinFET

designs. The novel device concept also features a potentially simplified fabrication process, reducing overall complexity, manufacturing time, and cost.

7.4 Future Work

Building upon the findings of this thesis, several directions for future research are proposed:

1. For buffer-free lateral GaN HEMTs, future work will focus on further optimization of the fabrication process. Devices will be fabricated from the best-performing wafer structures identified in this study, extending the investigation to both RF and power device applications. This will allow a comprehensive evaluation of how optimized epitaxial designs translate into enhanced performance metrics such as high-frequency response, output power, efficiency, and breakdown capability.
2. For vertical GaN FinFETs, the fabrication and characterisation of gate wrap-around FinFETs and benchmarking against state-of-the-art GaN power devices.
3. Applications – Integration of optimized GaN devices into power converter systems to evaluate switching efficiency, thermal stability, and system-level performance.

Appendices

Appendix I

Key Fabrication Steps

The fabrication of AlGaN/GaN HEMTs involved a series of precisely controlled steps, including ohmic contact formation, mesa isolation, gate definition, and pad metallization. Each step was optimized for material compatibility, pattern fidelity, and electrical performance to ensure reliable and repeatable device operation.

Surface Cleaning and Pre-treatment of the wafers

Prior to metal deposition processing, the wafer surface underwent thorough cleaning and pre-treatment to eliminate native oxides, organic residues, and other contaminants. This step is critical to ensuring optimal metal adhesion and minimizing contact resistance. In this work, a combination of solvent cleaning, acid etching, and plasma or UV-ozone treatments was employed. Specifically, the sample was immersed in a plastic beaker containing acetone and subjected to ultrasonic agitation for 5 minutes to ensure complete removal of surface contaminants, followed by rinsing with isopropyl alcohol (IPA) and reverse osmosis (RO) water, then dried using a nitrogen gun.

Deposition of Alignment Markers and Ohmic Metal Stack

The process began with a soft bake of the sample at 180°C for 3 minutes to eliminate any residual moisture from the substrate surface. A bilayer resist stack was then employed to facilitate a clean and well-defined lift-off profile. First, a layer of LOR 3A (lift-off resist) was spin-coated at 4000 rpm for 30 seconds, resulting in a thickness of approximately 300 nm. This was followed by a soft bake at 150°C for 2 minutes to solidify the layer, enhance adhesion to substrate and ensure stability during subsequent processing.

Next, a layer of S1818 positive photoresist was spin-coated at 4000 rpm for 30 seconds, yielding a thickness of around 1.8 µm. A soft bake at 115°C for 3 minute was then performed to remove residual solvents and ensure strong adhesion between the resist layers and the substrate.

The use of a bilayer resist system (LOR 3A/S1818) is essential for achieving an undercut profile during development, which enables clean metal lift-off. The LOR layer dissolves more rapidly than the top resist during development, creating a re-entrant profile that prevents metal from forming continuous sidewalls, thereby facilitating a reliable and residue-free lift-off process.

Using a mask aligner (MA6), the wafer was exposed to ultraviolet (UV) light for 6 seconds through a photomask containing the alignment marker and ohmic contact patterns. This exposure selectively altered the solubility of the photoresist in the exposed regions. Following exposure, the wafer was developed in MF319 developer for approximately 2 minutes to dissolve and remove the exposed areas of the S1818 resist, thereby revealing the underlying semiconductor surface for subsequent metal deposition. After development, the sample was thoroughly rinsed in RO water to halt the development process and remove any residual developer, then dried using a nitrogen gun to prevent watermarks or contamination. Prior to metal deposition, resist descum were carried out using the G-1000 Asher, which provided mild oxygen plasma treatment to remove residual resist and improve metal-to-semiconductor contact quality. Dilute HCl/RO water (1:4) treatment was carried out to remove native oxides and chemical residues.

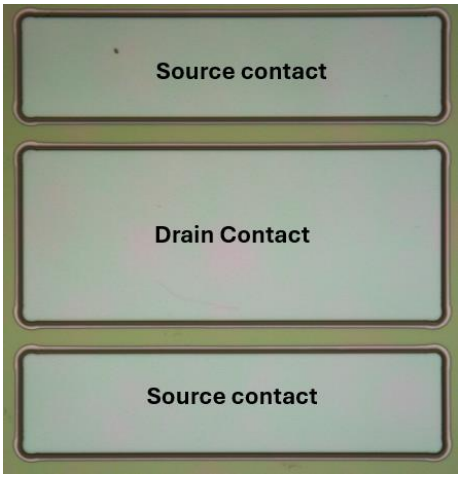


Figure 6.4 Defined ohmic contact pattern after development before metal deposition

Subsequently, the multilayer Ti/Al/Ni/Au ohmic metal stack was deposited onto the patterned wafer using an electron-beam evaporation. The choice and sequence of metals are critical to achieving low contact resistance and stable thermal performance.

The titanium layer promotes adhesion, aluminium provides good contact with the semiconductor, while nickel and gold serve as diffusion barriers and protect against oxidation.

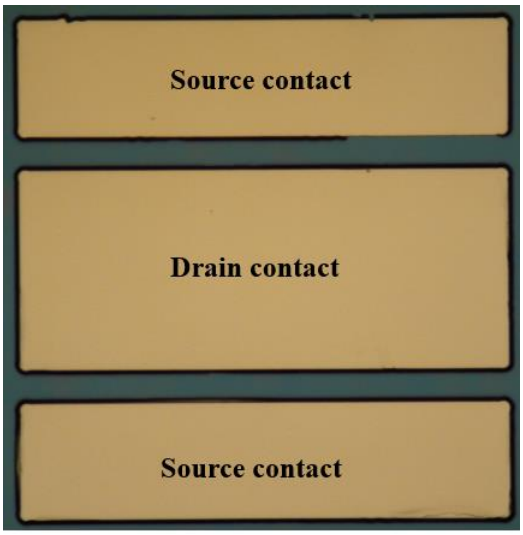


Figure 6.5 Ohmic contact after metal deposition before thermal annealing

Following metal deposition, the lift-off process was performed by immersing the wafer in a bath of Microposit remover 1165 maintained at 50 °C for approximately 2 hours. This allowed the underlying photoresist and unwanted metal to dissolve and lift away, leaving behind only the desired metal features adhering directly to the wafer surface. Gentle agitation or brief ultrasonic treatment was applied to facilitate the removal of any residual metal flakes or resist, ensuring sharp and well-defined pattern edges. Upon completion of the lift-off, the wafer was rinsed with RO water and dried with a nitrogen gun. This process successfully defined both the alignment markers and the ohmic contact regions required for further device fabrication.

Rapid Thermal Annealing and Contact Resistance Optimization

Rapid thermal annealing (RTA) was performed to alloy the ohmic metal stack and optimize the contact resistance of the AlGaN/GaN HEMT devices. The samples were annealed at a temperature of 850°C for 30 seconds under a nitrogen ambient to promote interdiffusion and formation of low-resistance ohmic contacts. This high-temperature, short-duration annealing enhances metal-semiconductor interaction, reduces contact resistance, and improves adhesion and thermal stability of the contacts. Optimizing

these parameters is critical for achieving reliable, high-performance HEMTs with minimal parasitic losses and improved current injection efficiency.

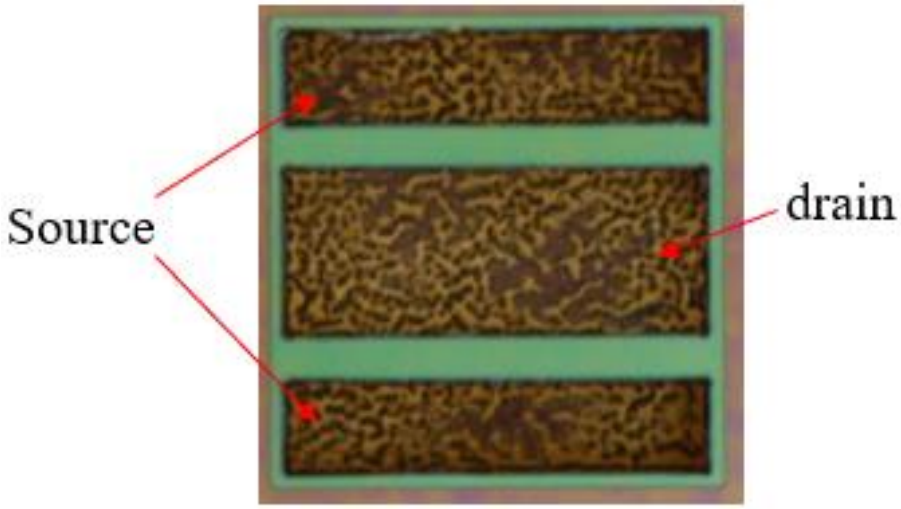


Figure 6.6 Ohmic contacts after metal deposition
and high temperature thermal annealing

Mesa Isolation Etch

Mesa isolation etching was performed to electrically isolate device regions by selectively removing the semiconductor material around the active areas.

The mesa isolation process began with spin-coating a layer of S1818 positive photoresist at 4000 rpm for 30 seconds, resulting in a uniform resist thickness of approximately 1.8 μm. The coated wafer was soft-baked at 115 °C for 3 minute to remove residual solvents. Using a mask aligner, the sample was then exposed to UV light through a photomask defining the mesa regions, followed by development in MF319 developer for 90 seconds. This step removed the exposed resist, creating the desired mesa pattern openings.

Following resist patterning, inductively coupled plasma (ICP) dry etching was carried out using the ICP-180 system with a Cl_2/Ar chemistry for 50 seconds. The etch recipe utilized 20 sccm of Cl_2 and 10 sccm of Ar, which provided an optimal balance between chemical etching and physical sputtering for smooth, anisotropic profiles. The chamber pressure was maintained at 5 mTorr. An ICP power of 200 W and an RF bias power of 100 W were applied to generate a high-density plasma and control ion energy for directional etching.

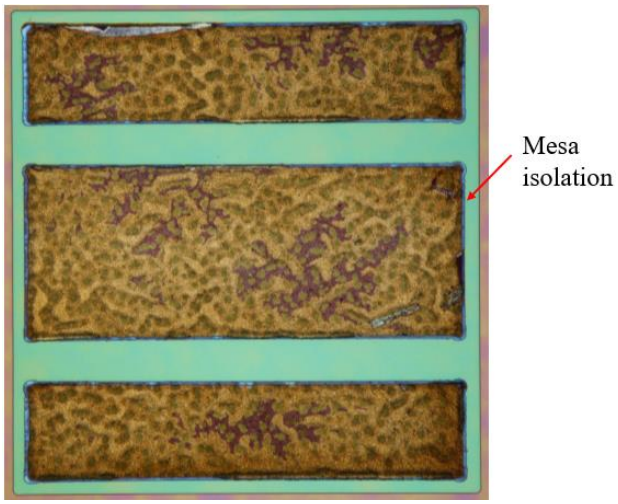


Figure 6.7 Outline of Mesa Isolation profile after Etching Process

The etch proceeded at a rate of approximately 100 nm/min, with the etch depth calibrated to ensure complete removal of the AlGaN/GaN layers down to the insulating buffer layer, thereby electrically isolating each device mesa. After etching, the remaining photoresist was stripped using Microposit 1165 remover at 50 °C, followed by RO water rinsing and nitrogen blow drying. This process defined well-isolated mesas with clean sidewalls, critical for minimizing leakage and ensuring reliable device operation.

Gate Formation

The gate formation process is a critical step in AlGaN/GaN HEMT fabrication, as it directly influences the device's threshold voltage, transconductance, and overall performance. This step involves precise patterning and metal deposition to define the gate electrode between the source and drain contacts, ensuring proper control of the two-dimensional electron gas (2DEG) channel.

Lithography and Gate Definition

After initial cleaning, the 2 and 3 um gate patterning process commenced with a substrate soft bake at 180 °C for 3 minutes to eliminate any residual surface moisture, ensuring optimal resist adhesion. A bilayer resist stack was then applied to enable clean metal lift-off and high-resolution gate definition. The process began with spin-coating LOR 3A lift-off resist at 4000 rpm for 30 seconds, resulting in an underlayer thickness of approximately 300 nm. This was followed by a soft bake at 150 °C for 2 minutes to enhance resist adhesion.

Next, a layer of S1805 positive photoresist was spin-coated at 4000 rpm for 30 seconds, producing a uniform top resist layer approximately 500 nm thick. The sample was then soft-baked at 115 °C for 3 minutes to remove residual solvents and enhance resist performance during exposure. Gate patterns were defined using UV exposure through a photomask in a mask aligner, with an exposure time of 2.5 seconds. The exposed sample was developed in MF319 developer for 90 seconds, revealing the gate openings in the resist stack.

The use of a bilayer resist system, with LOR 3A beneath S1805, resulted in a desirable undercut profile, critical for clean metal lift-off and preventing unwanted metal bridging at the gate edges. S1805 was specifically chosen for this step due to its capability to resolve fine features in the 2–3 µm range, ensuring precise gate definition required for high-performance HEMT operation.

After patterning, the sample was inspected under an optical microscope to confirm resolution and alignment prior to gate metal deposition.

Metal Gate Deposition and Liftoff

Metal deposition was carried out using electron beam evaporation (plassys IV) to ensure uniform coverage and high film purity. A bilayer metal stack of Ni/Au was deposited, with typical thicknesses of 20 nm for Ni and 200 nm for Au. Nickel serves as the adhesion and Schottky contact layer, while gold provides low resistivity and chemical stability. After deposition, the lift-off process was performed by immersing the sample in heated Microposit 1165 remover at 50 °C for several hours. The bilayer resist structure facilitated clean separation of unwanted metal, leaving behind well-defined gate electrodes with sharp edges. The sample was then rinsed with RO water and dried with a nitrogen gun, completing the gate formation process.

Metal Bond-pad processing

Pad metallization was carried out to form large-area metal contacts for probing and wire bonding. Proper pad sizing was carefully considered to ensure compatibility with the probe station used during electrical characterization. Specifically, the pads were designed to accommodate the tungsten probe tips of the Keysight B1500A Semiconductor Device Analyzer, which typically have tip diameters of ~50 µm. Sufficient

pad area is essential to ensure stable contact, reduce measurement variability, and prevent damage during repeated probing.

Lithography and Liftoff Process

Pad metallization began with the application of a bilayer resist stack to facilitate clean lift-off and ensure well-defined metal patterns. First, LOR 10A was spin-coated at 4000 rpm for 30 seconds, producing an underlayer approximately 1 μm thick. This was soft-baked at 150 °C for 2 minutes to improve adhesion and thermal stability. Next, S1818 positive photoresist was spin-coated at 4000 rpm for 30 seconds, resulting in a top resist layer about 1.8 μm thick, followed by a soft bake at 115 °C for 3 minutes.

The pad patterns were defined using UV exposure through a photomask and developed in MF319 developer for 90 seconds, creating the bilayer undercut profile critical for lift-off. Subsequently, a metal stack, typically Ti/Al/Ni/Au, was deposited by electron beam evaporation. After metal deposition, the lift-off process was performed by immersing the sample in Microposit 1165 remover at 50 °C, removing unwanted metal and resist and leaving well-defined pad contacts suitable for wire bonding and probing.

Appendix II

Test Structures

Test structures are critical for isolating and quantifying specific electrical parameters that cannot be independently extracted from a fully fabricated device. In HEMTs, for example, the contact resistance and the sheet resistance of the 2DEG are electrically in series, making it impossible to separate their effects using conventional measurements on the complete device. Minimizing both is essential to reduce parasitic losses and improve device performance. To independently extract these resistances in GaN HEMT, a Transfer Length Method (TLM) structure is employed. The TLM (Figure 2.13) consists of a series of ohmic contacts deposited on a continuous 2DEG channel, with each contact pair separated by incrementally increasing distances. By measuring the total resistance

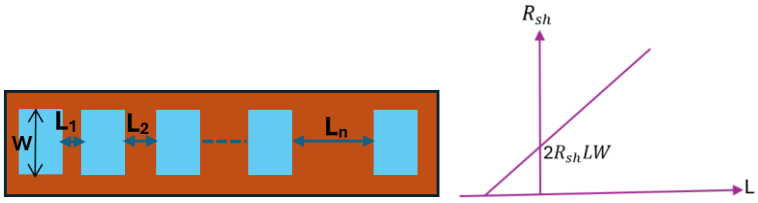


Figure 2. 20 Typical TLM structure for contact resistance extraction in GaN HEMTs

between contact pairs at various spacings, the contact resistance and 2DEG sheet resistance can be extracted. When the measured resistance is plotted against contact separation as shown in Figure x, the y-intercept corresponds to twice the contact resistance, while the slope of the linear fit yields the sheet resistance of the 2DEG. Extrapolating the line to the negative x-axis provides twice the transfer length (the characteristic length over which current laterally spreads from the semiconductor into the metal contact).

The transfer length is determined by the relative values of the contact and sheet resistances and represents the effective depth within the contact over which the majority of current injection occurs. As the current penetrates laterally under the contact metal, both the local current density and potential drop exponentially, forming a spatial potential distribution that can be analytically modelled. The TLM technique thus provides a reliable and widely used approach for evaluating contact and sheet resistances in GaN-based semiconductor devices.

Appendix III

Design of Vertical GaN FinFET

In vertical FinFET power devices, the two main regions of interest are the fin and the drift region. The fin provides control of current conduction, while the drift region plays the role in sustaining high voltages. Their design must be carefully optimized to balance conduction performance with breakdown voltage capability.

2.4.1 The fin region

The fin in a FinFET is the narrow, vertical semiconductor (GaN) structure that forms the transistor channel. Its geometry (fin height, width, and pitch) affects the current density, gate control, and electrostatic integrity. A multi-fin structure increases current drive capability, while narrower fins improve short-channel effects. Its role is to maintain strong gate control and low leakage.

2.4.2 The drift region

The drift region in a FinFET structure determines the high-voltage performance of the device. It is designed primarily to withstand large electric fields and sustain the blocking voltage when the device is in the off state. To perform this function, the drift region is doped much more lightly than other regions of the device. This light doping reduces the electric field concentration and increases the depletion width, both of which are necessary for achieving a high breakdown voltage. However, the light doping leads to higher resistivity of the drift region, introducing a fundamental trade-off between conduction loss and voltage blocking capability.

The breakdown voltage of the drift region can be expressed as a function of its doping concentration. For a semiconductor with dielectric constant ε_s, electronic charge q, and critical electric field E_{cr}, the maximum breakdown voltage is given by equation (2.2) [159],

$$V_B = \frac{\varepsilon_s E_{cr}^2}{2qN_D} \tag{2.2}$$

where N_D is the donor dopant concentration in the drift layer. This equation shows that the breakdown voltage increases as the doping concentration decreases. To sustain such a voltage, the physical thickness of the drift region must be comparable to or larger than

the depletion width that develops under reverse bias conditions. This depletion width is expressed as [159]

$$L_N \approx w_d = \sqrt{\frac{2\varepsilon_s V_B}{qN_D}} \tag{2.3}$$

indicating that a thicker drift layer is required as the breakdown voltage rises. In practical FinFET designs, this means that high-voltage devices must be fabricated with drift regions that are both lightly doped and physically extended in dimension.

The presence of a thick, lightly doped drift region has direct implications on the resistance of the device. The total resistance of the drift region can be written as

$$R = \rho \frac{L_N}{A} \tag{2.4}$$

where *A* is the effective cross-sectional area of the conduction path and ρ is the resistivity of the material. Since resistivity is the inverse of conductivity, and conductivity is proportional to the product of charge, mobility, and doping concentration, the drift region resistance becomes

$$R_{SP} = \rho L_N = \frac{L_N}{q\mu_n N_D} \tag{2.5}$$

where μ_n is the electron mobility in the drift layer. This indicates that reducing the doping density to increase breakdown voltage unavoidably raises the specific on-resistance of the device. By combining the above equations, one arrives at equation (2.6) which presents a more fundamental trade-off relationship:

$$R_{SP} = \frac{4V_B^2}{\varepsilon_s \mu_n E_{cr}^3} \tag{2.6}$$

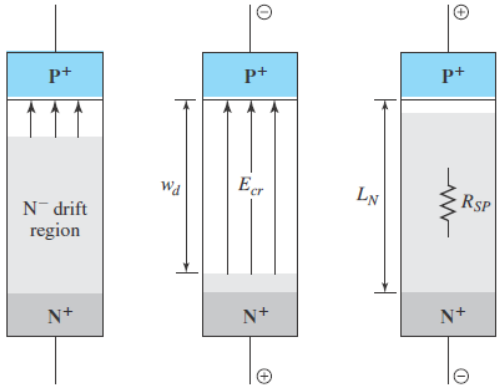


Figure 2.22 Relationship between resistance R and drift region [2]

This equation illustrates the inherent limitation faced in drift region design, where higher blocking voltages demand a disproportionate increase in resistance (Figure 2.22). The parameter that emerges from this relationship, $\frac{V_B^2}{R_{sp}}$ is known as the Baliga figure of merit (BFOM). It is a material-dependent figure that emphasizes the importance of the critical electric field E_{cr}.

In the specific case of FinFET, the geometry of the device introduces further complexity. Since the conduction path is formed along the narrow fins, the effective cross-sectional area A is much smaller than in planar devices. As a result, the resistance contribution of the drift region can be more pronounced in FinFET, particularly when the drift length must be extended to support kilovolt-range breakdown voltages. To mitigate this, designs can often resort to material innovations, such as employing wide bandgap semiconductors that allows the drift region to sustain the required breakdown voltage while minimizing the persistence of on-resistance. Table 2.4 shows how the on-resistance is strongly influenced by the intrinsic material properties, particularly the critical electric field, dielectric constant, and carrier mobility.

Table 2.4 Comparison of on-resistance of the state-of-the-art semiconductor materials at 1kV

Semiconductor Material	**Critical Electric field (E_{cr}) V/cm**	**Dielectric constant (ε_s)**	**Electron mobility (μ_r) cm²/Vs**	$R_{sp} = \frac{4V_{BR}^2}{E_{cr}^3 \varepsilon_s \mu_r}$	**Comparison of R_{sp}**
Silicon	0.3×10^6	11.9	1500	9.37×10^{-2}	Baseline (100%)
SiC	3×10^6	10.1	700	2.37×10^{-4}	400 times lower than silicon
GaN	3.3×10^6	9.0	1000	1.40×10^{-4}	670 times lower than silicon

Ga_2O_3	8×10^6	10.2	300	2.88×10^{-5}	3250 times lower than silicon

Ultimately, the drift region in a FinFET embodies the most critical design compromise: achieving a low doping concentration and a sufficiently thick depletion layer to provide high breakdown voltage, while simultaneously ensuring that the resistance does not render the device impractical for power applications. This balance defines the performance limits of vertical FinFET and explains why the migration toward wide bandgap materials has become essential in modern high-voltage transistor technologies.

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