Optimisation of Resonant Tunnelling Diodes for Terahertz Applications

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Abstract

Resonant Tunnelling Diodes (RTDs) are a prominent technology in THz emitter research. This thesis explores the suitability of these devices for future adoption as THz emitters, primarily focusing on communications applications. Through the establishment of a more accessible fabrication process, critical analysis of the literature, and a systematic analysis of RTD epitaxial structures, some of the challenges of realising these devices in practice have been addressed.

For mass manufacturing capabilities in the future, the RTD fabrication process must be as time and cost-effective as possible while still delivering high-performance devices. A process is developed here with this in mind, keeping the number of steps to a minimum, and using commonly available tools and chemicals to make this process as accessible as possible. High current density RTD devices are fabricated and electrically characterised with this process.

The predictability of RTD device performance will be a key aspect of future designs. Establishing reliable figures of merit to characterise device performance and designing devices to achieve these figures of merit, will be key to producing RTDs for a range of applications. A critical analysis of results from the literature is performed to detect trends in device performance and, using the IRE, comparisons of these historical devices are made. The IRE allows for optimisation of the electrical characteristics of the device. An investigation into the effects of the epitaxial structure on the device performance is also done.

For optimisation of RTD devices, the epitaxial structure requires close examination. A systematic analysis is performed, with small changes made to key epitaxial parameters – including the thicknesses and positions of active layers – resulting in a clearer perception of the effect these parameters have on the device performance. Comparisons with literature and simulation work are done, and conclusions about the epitaxial optimisation of RTD devices are formed.

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List of Outputs

[1] R. Baba, K.J.P. Jacobs, B.J. Stevens, B.A. Harrison, A.P. Watt, T. Mukai, “Resonant Tunnelling Diodes for next generation THz systems”, 2018 IEEE British and Irish Conference on Optics and Photonics (BICOP), London, UK, (2018)

[2] M. Cito, D. Cimbri, D. Childs, R. Baba, B.A. Harrison, A. Watt, T. Mukai, E. Wasige, R.A. Hogg, “Micro-PL analysis of high current density resonant tunneling diodes for THz applications”, Applied Physics Letters, Vol. 119, Issue 7, (2021)

[3] M. Cito, R. Baba, D. Childs, B.A. Harrison, A. Watt, T. Mukai, R.A. Hogg, “Micro-photoluminescence characterization of structural disorder in resonant tunneling diodes for THz applications”, SPIE Nanoscience + Engineering, San Diego, USA, (2021)

Table of Contents

List Of Figures

List Of Tables

Declaration

I hereby declare that all work presented in this thesis was carried out by the author unless otherwise explicitly stated. This work has not been presented in any previous application for a degree at this or any other institution.

Chapter 1 : Background

1.1 Introduction

Resonant tunnelling diodes (RTDs) are a promising technology in the realm of terahertz (THz) emitters. These devices have existed for over 50 years, and the technology has advanced to a stage where potential applications in the telecommunications industry, in particular, are more feasible than ever. As we approach 6G and 7G wireless telecommunication standards, the demand for higher frequency emitters grows and grows. RTDs are the most suitable technology for emission at these frequencies, and it is vital for more research to be done into these devices, to achieve the power and frequency outputs necessary for practical use in wireless networks everywhere.

In this chapter, a background of RTDs is given through the context of the literature, and the physical description of how these devices operate. Firstly, a literature review of the discovery of tunnel diodes is detailed, followed by the discovery of resonant tunnelling 17 years later. Following this, a description of the operation of an RTD is provided with regards to both the electrical characteristics, and the emission of high-frequency signals. Then, the advances in technology which led to improvements in RTD performance are described all the way up to the present day. A comparison of RTDs with other THz technologies is then performed to demonstrate why RTDs are the most promising candidate for THz emitters in the future. Finally, gaps in the knowledge of RTD research are explored, followed by an outline of the work done in this thesis.

1.2 Terahertz (THz) Technology

The THz region of the electromagnetic spectrum is the focus of much study in the photonics and electronics areas. At THz frequencies, a range of applications are possible. In telecommunications [1], as we strive for higher data rates and lower latency, we require higher bandwidths. To achieve this, we must look to higher frequencies i.e. the THz region. Free space communications in particular are the application this work focuses on, and further details of this are given later in this section. In addition, THz offers a non-ionising alternative to x-rays which has applications in medical imaging - as THz waves are absorbed by water, they can detect differences in water content. This is a useful property for detecting diabetic foot syndrome, for example [2]. In security applications, THz radiation can be used to detect concealed weapons or illegal substances as they pass through clothing, luggage and other non-metallic materials. Some of the illegal substances have characteristic spectra in the THz region, allowing them to be identified also [3]. Reviews of other applications in spectroscopy and imaging are given in [4] [5]. Therefore, developing practical technologies is of very high importance. In particular, the research done in this thesis pertains to THz emitters. There are considerable challenges to be overcome in the THz region, leading to the existence of the "THz gap" – a frequency range in which there are a lack of practical devices capable of emission.

Edholm's law [6], shown in Figure 1-1, states that the three telecommunications categories – wireless, nomadic and wireline - can be plotted as linear relationships between data rate and time. Wireless technologies can be accessed freely as the user moves about e.g. mobile telephony; nomadic describes systems which can be used from place to place like Wi-Fi hotspots; and wired systems are connections like Ethernet that are fixed to a certain location. When extrapolated, this graph predicts that the data rates of wireless and nomadic technologies will converge around the year 2030. Edholm's law predicts that the data rates for telecommunications will continue to increase, and therefore THz technology is required to meet this demand. At THz frequencies, much larger

bandwidths will be available, and progress on more data-intensive applications such as Internet of things (IoT) [7] will be possible.

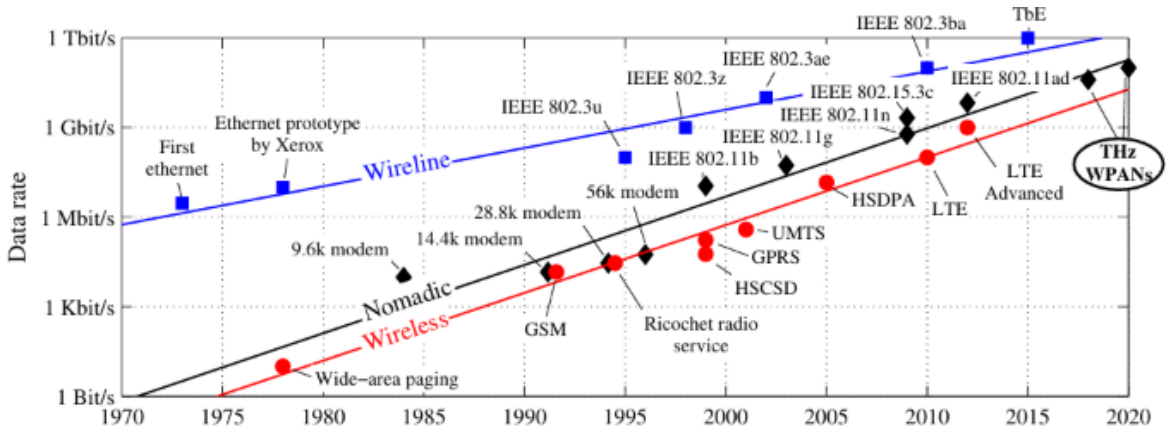

***Figure 1-1**: Edholm's law of bandwidth. Wireline (or wired) technologies currently offer the fastest data rates but by the year 2030, nomadic and wireless technologies are expected to catch up, from [8], adapted from [6].*

A significant problem encountered in the THz region is with atmospheric attenuation. At frequencies above 1GHz, atmospheric attenuation starts to become a significant limiting factor on the range of waves. This is due to the presence of absorption peaks of common compounds such as oxygen (O_2) and water (H_2O). Therefore, the operating frequency of any THz emitter must be carefully engineered to avoid these attenuation peaks. A plot of the attenuation is shown in Figure 1-2 based on a model from the International Telecommunications Union (ITU) [9].

Looking at the standard plot in Figure 1-2, suitable frequencies to choose for THz communication could lie between 200-300GHz, around 350GHz, 410GHz, 650GHz and 850GHz. At even higher frequencies - up to 10THz – more attenuation peaks occur, so that the suitable frequency windows become a lot narrower. In addition, the attenuation continues to increase so that the range of the signals drops significantly. To overcome this unavoidable atmospheric attenuation, a number of new technologies are required.

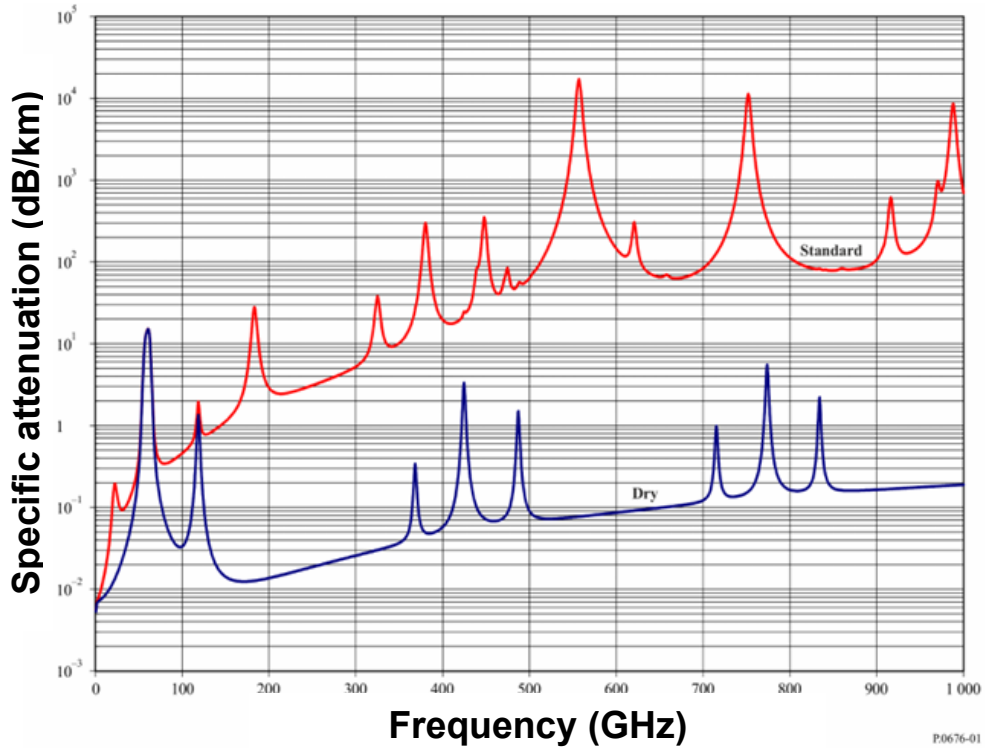

Figure 1-2: *Two plots of specific attenuation (dB/km) against frequency (GHz) from 0 to 1THz. Standard conditions are T = 15°C and P = 1013 hPa (sea level). A water vapour density of 7.5g/m^3 is present for the top plot and a dry atmosphere for the bottom one. Adapted from ITU-R P.676-13 [9].*

Firstly, higher power emitters are needed to output a signal with enough range at the necessary frequency bands. This is the main focus of this work, and will be covered in detail in the following sections. One way to increase the capacity of a wireless communications system is to use multiple-input and multiple-output (MIMO) technology. MIMO systems use multiple antennas on both the transmitting and receiving ends, demultiplexing a high data rate signal into several lower data rate signals for transmission, and then multiplexing them at the receiver to reconstruct the original signal. The number of antennas used correlates to the increase in capacity of the system. For use at higher frequencies, with higher bandwidths, ultra-massive MIMO (UM MIMO) has been posited as a potential solution [10]. These can have as many as 1024 antenna elements at each end of the link.

As the range will unavoidably decrease at these frequencies, improving the directivity of the beam is another way to increase the efficiency of the signal and reduce loss. Beamforming is the technique used to achieve this, and has been used for many years. In beamforming, multiple elements of an antenna array are

combined so that their signals interfere with each other, resulting in a directional signal, as shown in Figure 1-3.

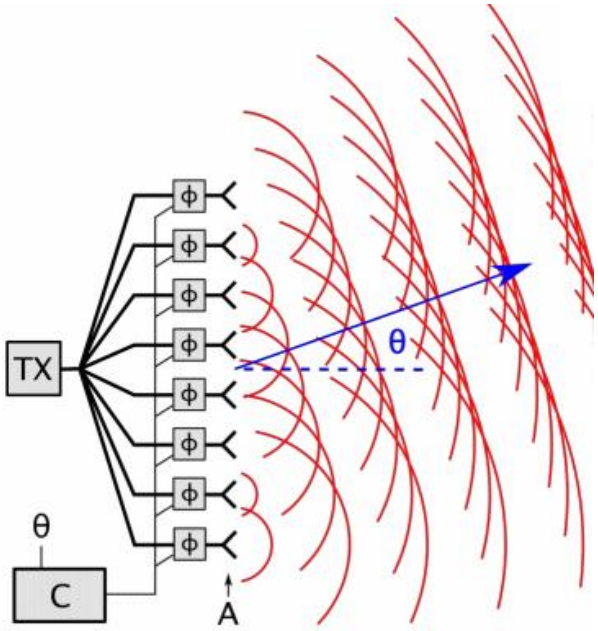

***Figure 1-3**: A phased array demonstrates how beamforming works. The signal from each element (A) is shifted slightly in phase (ϕ) controlled by a computer (C). This results in constructive and destructive interference which causes a directional beam at an angle (ϑ)*

Analogue and digital beamforming techniques both have advantages and disadvantages for transmitting data, particularly when the number of antenna elements approaches that required for MIMO and UM MIMO. Therefore, a hybrid system is required to optimise the complexity and cost of the systems whilst maintaining the integrity of the data. Details of this are given in [11] and [12].

The “THz gap” is a region lying between 0.1 THz & 10 THz which holds a lot of potential for high speed and high bandwidth communication. However as of yet, a suitable technology has not been found that meets the requirements for a realisable device. As well as the technical factors like frequency and power outputs, devices must be mass-manufacturable meaning the manufacturing process must be kept simple and cost-effective. There are a range of devices being researched to bridge the “THz gap”, but each have their own drawbacks and

technological limitations. These devices will be discussed later in this section, and by comparison, the advantages of RTDs will be explained.

As previously mentioned, the THz gap represents a real challenge for researchers. This is an area where the lowest frequency optical devices and the highest frequency electrical devices have not covered under normal operating conditions. Although some devices have been created to operate in this region, they always suffer from drawbacks such as substantial size or cooling. These disadvantages make the devices infeasible as commercial products and more work must be done to create a suitable device. A summary of the power and frequency values obtained by some of these devices is shown in Figure 1-4.

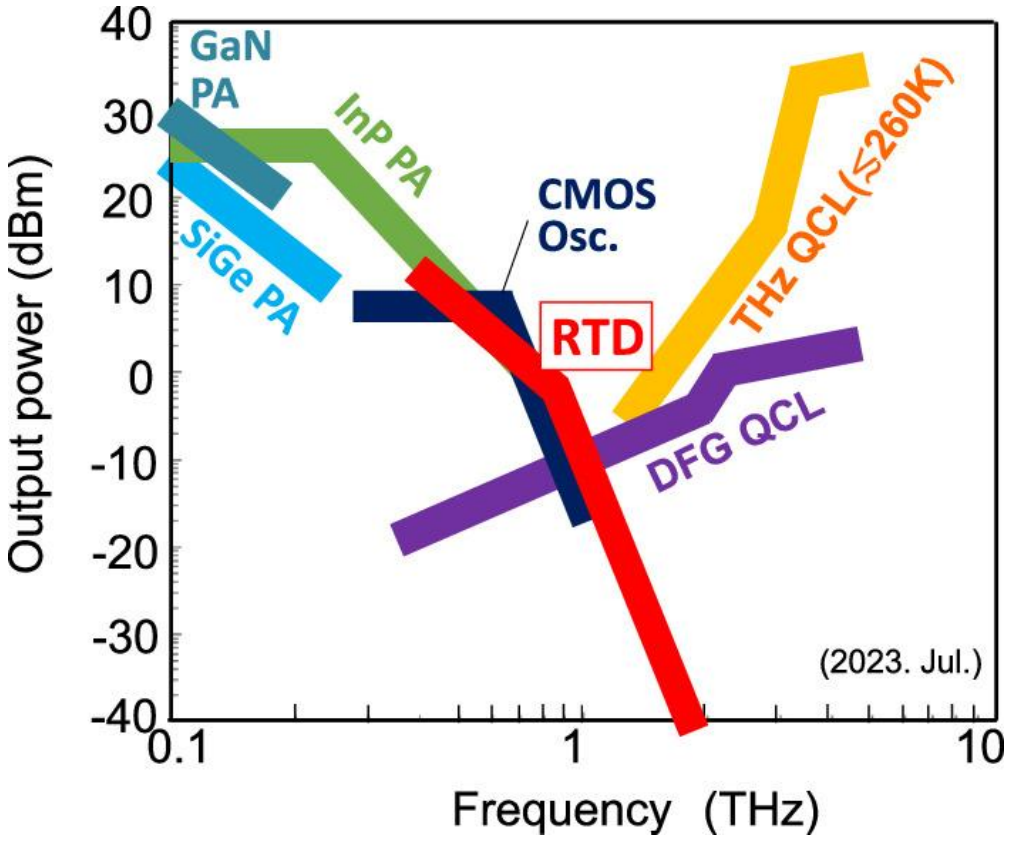

***Figure 1-4**: Plot of a number of technologies being researched in the THz region, with their respective power and frequencies plotted, from Suzuki & Asada [13].*

Solid state devices tend to suffer from large drops in power as their operating frequencies reach the lower boundary of the THz gap. Impact ionisation avalanche transit-time (IMPATT) diodes have been shown both experimentally and through simulation, to operate in the THz gap and emit high power signals [14] [15]. However, the operation of these devices relies on the avalanche breakdown phenomenon which has inherent high phase noise [16]. Gunn diodes have produced

THz waves [17], although the frequency of these is limited by the length of the transit region. Oscillations at 307 GHz with a power of 28μW have been recorded [18], however obtaining higher frequencies appears problematic. Furthermore, high electron mobility transistors (HEMTs) and heterojunction bipolar transistors (HBTs) are capable of THz emission also [19] [20]. However, the cut-off frequency limits these devices to the lower end of the THz gap and power outputs tend to be low. These devices are most commonly integrated in monolithic microwave integrated circuits (MMICs) which are difficult to fabricate, limiting the manufacturability of these devices [21].

Laser-based systems, like quantum cascade lasers (QCLs) and p-Ge lasers, have demonstrated operation at the upper end of the THz gap and produce very high power outputs. However, these devices require cooling and are not suitable for room temperature operation.

Some other possible THz solutions are: Schottky chain multipliers [22] [23] which are only available as tabletop packages and thus impractically large for use as a commercial THz emitter; difference frequency generation (DFG) of two mid-infrared (IR) QCLs has been demonstrated to provide 7μW at 80K and 300nW at 300K, which is too low a power for THz emission [24]; and RTDs which have displayed the potential to operate within the THz gap with 1.98 THz achieved at room temperature [25] though have problems with output power at these frequencies (in the range of μW) [26] [27].

1.3 Epitaxial Growth & Heterostructures

The QW structure is integral to the operation of the RTD device. The epitaxial design will have significant impact on the performance of the device, which can be visualised through energy band diagrams, as seen in Figure 1-9. A number of design considerations must be addressed including the growth method, material selection, and layer thicknesses in order to optimise device performance.

Firstly, two main methods for growing wafers must be considered: molecular beam epitaxy (MBE) and metalorganic vapour-phase epitaxy (MOVPE).

In MBE operation, layers of material are deposited onto the substrate to gradually build up the intended structure under high vacuum conditions. In the example of gallium arsenide (GaAs), the individual elements, Ga and As, are heated separately until sublimation occurs. The resultant gases will then condense on the wafer where reaction between them can occur to form GaAs. The term “beam” in MBE arises as these gases do not interact before reaching the wafer, due to the long mean free paths of the atomic elements. During this deposition process, a technique called reflection high-energy electron diffraction (RHEED) is used to monitor the growth. In RHEED, an electron gun sends electrons to strike the wafer at a very acute angle relative to the wafer surface, which then diffract due to the atoms on the surface, and then form an interference pattern on a detector. From these patterns, details about the crystal structure can be determined.

In an MOVPE system, chemical reactions between precursor gases are used to deposit the required layers. For indium phosphide deposition, for example, trimethylindium ($(CH_3)_3In$) and phosphine (PH_3) are used. When these gases reach the heated semiconductor surface, the bonds within these compounds break and the In and P elements absorb onto the wafer surface. Methane (CH_4) is removed from the chamber as a byproduct from the reaction. The MOVPE process is a much faster one than for MBE, due to the nature of the deposition process. In addition, the MBE process requires high or ultra-high vacuum conditions, and the chamber must be kept very clean. However, the inclusion of in-situ monitoring in MBE (RHEED monitor) represents an advantage over MOVPE processes. Generally, MOVPE is more suitable for high-volume production with a faster process and higher throughput whereas for wafers requiring a greater degree of control and precision, MBE is better suited.

Using either of the two above processes, wafers can be grown. If layers of the same material are grown, even with different doping levels throughout, it is known as a homostructure, and the boundaries between layers of different doping concentrations are known as homojunctions. If different materials are

used, the structure is a heterostructure and the boundaries are called heterojunctions. The difference in energy band gaps of different materials allows for applications in semiconductor lasers [28], solar cells [29], transistors [30], and as shown in this work, RTDs. There are three main types of heterojunctions, shown in Figure 1-5.

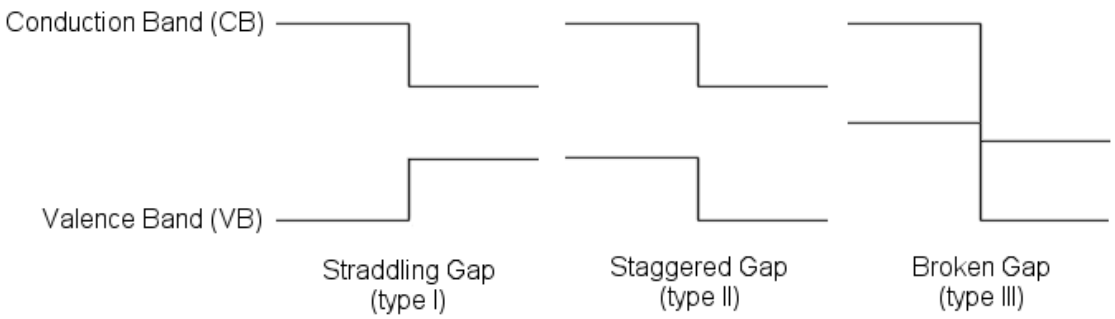

***Figure 1-5**: Band diagrams of the three possible heterojunction structures. The vertical axis represents the energy if the conduction and valence bands, and the horizontal axis is the physical length of the materials*

Type I occurs when the valence band for one of the semiconductors is higher, and the conduction band is lower. This means the band gap must be larger. Type II heterojunctions occur when both valence and conduction bands are higher for one semiconductor, and the band gap can be smaller or larger. For Type III structures, the same conditions are true as for Type II, except there is an overlap between the valence band of one semiconductor and the conduction band of the other.

QWs consist of a low bandgap material sandwiched by two barriers of high bandgap material. When the low bandgap material is of a length approaching the de Broglie wavelength of the particles, these particles within the well become confined to discrete energy levels. Several parameters affect the position of these energy levels within the QW including the width of the QW layers and the bandgap of the QW materials.

When deciding on the materials for a heterostructure, it is important to consider the matching of the crystal lattices. The lattice constant for cubic crystal structures, a, represents the distance between atoms. If a material with different lattice constants is grown on a substrate, the crystal is stretched or compressed to fit the substrate lattice. This is known as strain. If the strain becomes too large, dislocations will occur, caused by missing or dangling bonds

in the heterojunction. Strain can be compressive or tensile, depending on the lattice constants of the respective materials. Strain balancing can be achieved by compensating a tensile strained structure with compressive layers to balance the strain of the overall structure. Details of this are given in [31]. Strain can cause changes to the band structure, as seen in [32], and so can improve or worsen the electrical properties of a fabricated device.

For the RTDs in this work, an InGaAs/AlAs QW material system is used, grown on an InP substrate. When the InGaAs Indium composition is 53%, the lattice constant matches that of InP (a=5.869Å), and so it is said to be lattice matched (LM). The lattice constants of AlAs (a=5.6605Å) and InGaAs with higher In compositions (a=5.9773Å for $In_{0.8}Ga_{0.2}As$), are not lattice matched, and so contribute strain to the overall structure. As the lattice constant of AlAs is lower than for LM-InGaAs, the lattice must stretch and thus, the structure experiences tensile strain. Conversely, the $In_{0.8}Ga_{0.2}As$ layer will undergo compressive strain. The dimensions of these layers can be chosen to enable a fully strain balanced structure or only a partial strain balanced structure, as is used in this work.

AlAs provides a high barrier height due to its high bandgap (E_g = 2.16eV) compared to that of $In_{0.53}Ga_{0.47}As$ (E_g = 0.507eV) and $In_{0.8}Ga_{0.2}As$ (E_g = 0.503eV), thus forming the QW structure. The doping of the RTD layers in this work is done with Si (n-type doping). The contact layer is highly doped to reduce contact resistance, and the current path layer is also highly doped to reduce the resistance along this path, thus increasing the current flow.

1.4 Quantum Tunnelling and the Tunnel Diode

Quantum tunnelling occurs through potential barriers due to the wave-particle duality of matter, proven by the double-slit experiment, conducted by Thomas Young [33]. Louis de Broglie demonstrated that all matter exhibits wave-like behaviour [34]. This behaviour can be represented by a wavefunction. Erwin Schrödinger developed the wave equation [35] as a way of calculating these wavefunctions. A probability density can be found as the square of the amplitude

of the wavefunctions (known as the Born rule), representing the probability of a particle being measured at a certain position.

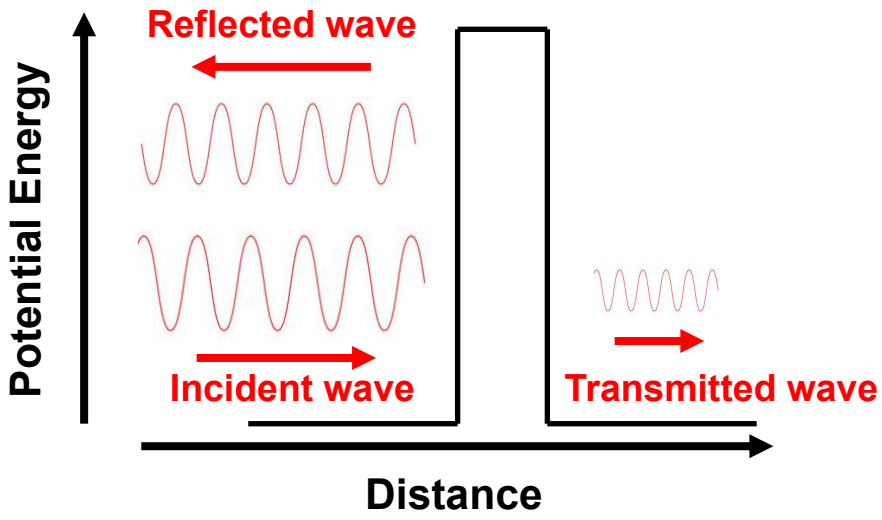

***Figure 1-6**: Simplified diagram of quantum tunnelling through a single barrier.*

In the classical case, a particle incident on a barrier would not be able to pass through and would instead reflect the way it came. In quantum mechanics, this particle is represented as a probability wave. As this wave reaches the barrier, a small part of the wavefunction can pass through the barrier if the barrier is thin enough, shown in Figure 1-6. The majority of the wavefunction is still reflected as the tunnelling probability is low but there is a non-zero probability of the particle tunnelling through. Factors affecting the tunnelling probability are barrier width, the barrier height, and the particle size.

The first tunnelling diode was invented in 1957 by Leo Esaki [36] when he fabricated very thin germanium (Ge) p-n junctions with high doping concentrations on each side. By increasing the doping concentrations, the junction width i.e. the barrier width, decreased. The reverse breakdown voltage of these p-n junctions became zero, and an odd I-V graph was obtained, with an area where the current appeared to decrease with increasing voltage. This occurs due to the misalignment of conduction and valence bands and is a very similar process to that which occurs in RTD devices. This will be discussed in more detail later in this chapter. This is called the negative differential resistance (NDR) region, and it allows RTD devices to be used as oscillators, and therefore, THz emitters.

Following on from this discovery, the tunnel diode was demonstrated on silicon (Si) p-n junctions [37], with wider NDR regions possible due to the greater bandgap on Si compared to Ge, although this factor in addition to the larger effective mass of Si resulted in a lower tunnelling current [38]. NDR regions were also discovered on metal-oxide-semiconductor (MOS) junctions [39]. Al-Al_2O_3-SnTe (or GeTe) material systems were chosen, with the increase in barrier height as bias is applied attributed to the NDR region.

Research into practical applications for this unique I-V characteristic continued, and the phenomenon of resonant tunnelling became a very promising research area.

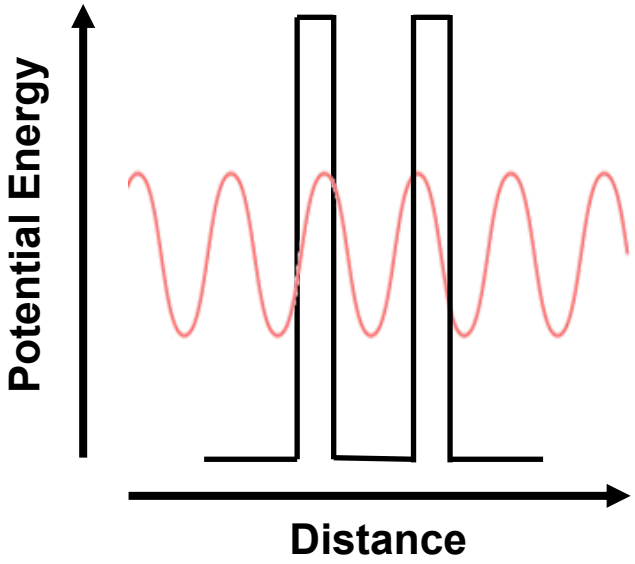

***Figure 1-7**: Simplified diagram of resonant tunnelling through a double barrier structure.*

Resonant tunnelling occurs when there is a double-barrier structure forming a QW, shown in Figure 1-7. When the energy of the incident waveform matches the energy of a quasi-bound state within the well, the waveform fully transports through the double-barrier structure i.e. the transmission probability is 1. As tunnelling is a very fast process, this allows for very fast devices to be made. These are detailed in Section 1.5.

1.5 The Resonant Tunnelling Diode (RTD)

Chang, Esaki and Tsu fabricated the first double barrier RTD in 1974, demonstrated by the presence of peaks in the current at the appropriate resonance energies [40]. The quantum well (QW) consisted of $Al_{0.7}Ga_{0.3}As$ barriers and a GaAs well, grown using molecular beam epitaxy (MBE). The fabrication process and device design were detailed in [41].

Resonant tunnelling occurs when two very thin high-potential barriers exist with a QW lying between them. A QW is a structure which confines an electron to only two dimensions of movement by limiting the width of the other dimension down to around the de Broglie wavelength. This confinement creates discrete quasi-bound energy levels within the QW. When electrons are incident on the QW, a number of transport mechanisms are possible. These are summarised in Figure 1-8.

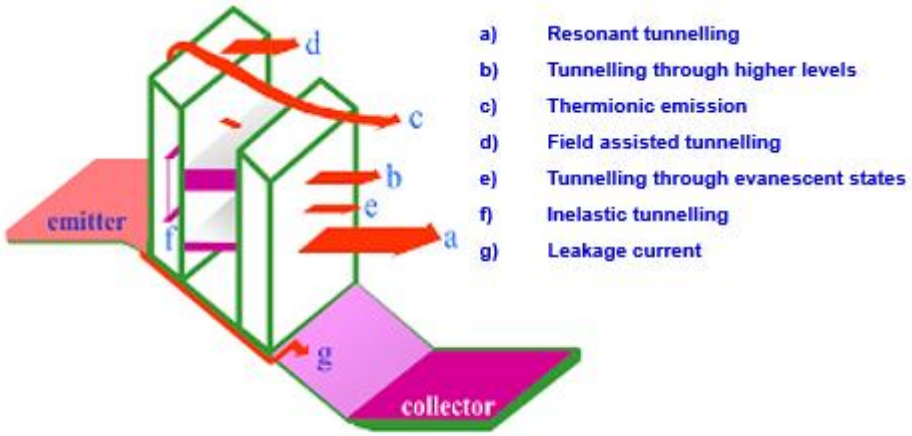

***Figure 1-8**: Diagram of transport mechanisms through a double barrier structure, adapted from [42] and [43]*

In addition to resonant tunnelling, it is also possible for incident electrons to tunnel through higher quasi-bound states in the QW. Thermionic emission occurs when electrons acquire high enough energies to travel over the barriers. By applying a voltage, an electric field is created, and the conduction bands of the QW structure are no longer flat. This reduces the energy required for electrons to tunnel through the system (d). It is also possible for electrons to tunnel through the QW without occupying the quasi-bound states, instead occupying evanescent

states. Inelastic tunnelling can occur in several ways. An electron may absorb or emit a phonon (from the vibrations of the crystal lattice), to increase or decrease its energy to match that of the quasi-bound state. Other inelastic tunnelling can be caused by impurities in the material, or roughness at the interface between different materials or a few other scattering methods. Leakage current describes any current that flows through the device through an alternate path. This is a result of the fabrication process and should be minimised to improve device performance.

The resonant tunnelling transport mechanism occurs when the Fermi level of the electrons on the emitter side aligns with the quasi-bound state in the QW. This leads to a device I-V with the shape shown in Figure 1-9.

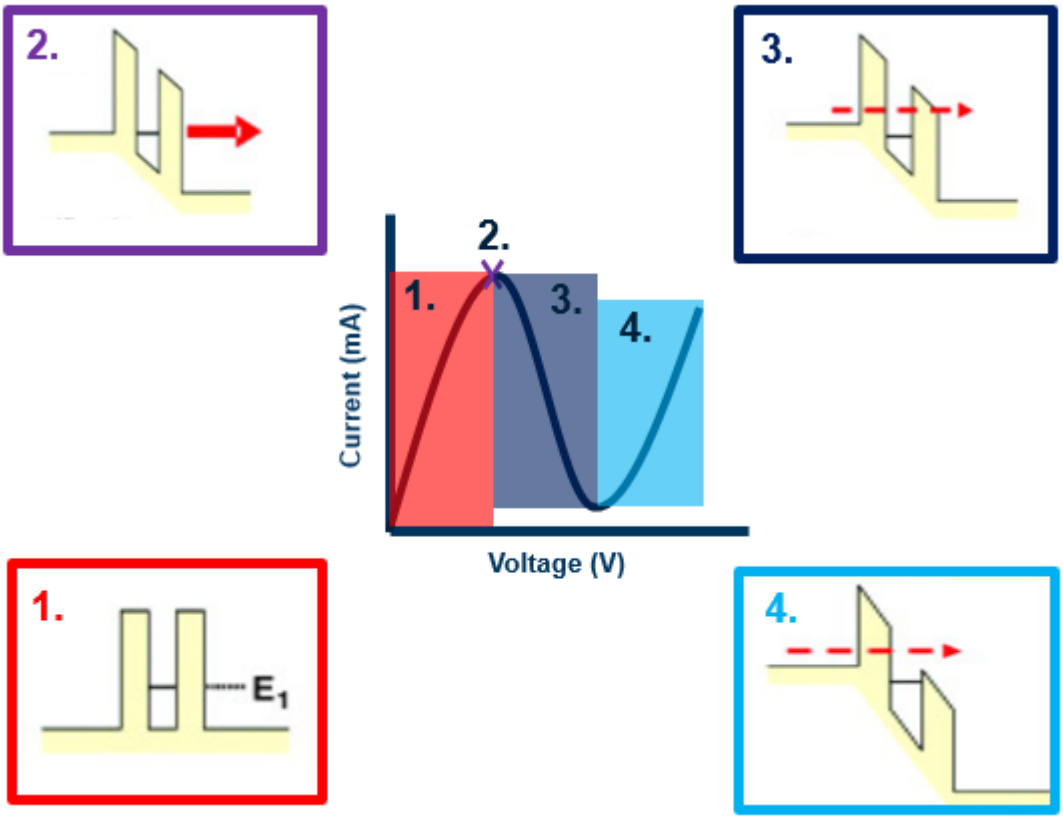

Figure 1-9: *Typical shape of an I-V graph of an RTD (centre). The I-V is split into 4 parts as the bias increases, with simplified conduction band diagrams shown for each section. From zero bias (bottom-left) up to the peak current (top-left), then the NDR region (top-right) and the subsequent PDR region (bottom-right).*

Initially, when no bias is applied, the Fermi level of the emitter conduction band lies below the E_1 state in the well. When a voltage is applied across the device, the Fermi level approaches E_1, and more electrons can tunnel through the double barrier structure, resulting in an increase in current. This continues up to

the peak current, which is achieved when the emitter side aligns with E_1, and resonant tunnelling occurs. This phenomenon results in almost all the electrons tunnelling through the double-barrier structure to the collector at the output, as the transmission probability approaches one.

When the bias voltage is further increased, the emitter becomes misaligned with E_1, the resonant tunnelling decreases, and so does the current. This decrease in current, coinciding with an increase in voltage, creates the NDR region on the I-V curve. The device is biased in this region to extract THz oscillations. Further increasing the voltage causes the current to start increasing again after reaching a minimum (called the valley current). This occurs since the electrons now have enough energy to travel over the potential barriers, or to tunnel through higher quasi-bound states in the QW. Additional states can result in another NDR region, although this depends on the work function in the QW i.e. the energy difference between the energy level and the conduction band energy of the barrier material. Other transport mechanisms - such as thermionic emission - over the barriers, will begin to dominate over resonant tunnelling through the quasi-bound state, as the electron energy increases. Thermionic emission is dependent on the temperature of the device and can be minimised by operating the device in a cryostat [44]. This will improve the efficiency of the device as it reduces the contribution of non-resonant tunnelling transport. Conversely, at higher temperatures, thermionic emission is expected to increase until the NDR region no longer exists. Further research is required into this upper temperature limit for RTD devices. However, for practical operation, we require devices to operate at room temperature. An alternative approach to reduce thermionic emission is to increase the separation between the E_1 and E_2 levels in the QW, which requires consideration in the epitaxial design phase.

The first oscillation results from an RTD device were obtained by Sollner *et al.* [45]. This device consisted of an undoped GaAs QW with thin AlGaAs barriers. A coaxial resonant cavity was used to extract the signal, with the QW mesa at one end of the cavity. A frequency value of 18GHz and a power value of 5μW was obtained.

An example of free space emission of an RTD in a slot antenna is shown in Figure 1-10. In a slot antenna, applying voltage across the slot results in a current flow round the edges of the slot. An electric field is established across the slot, resulting in a capacitive effect, and due to the longer path lengths for the current around the slot, an inductive effect is also present. As the length of the slot approaches half of the free-space wavelength (λ_o), resonance is obtained from these capacitive and inductive effects and the structure will radiate a wave perpendicular to the plane. The frequency of this radiated signal is dependent on the slot length. To sustain oscillations, the NDR resistance must be larger than the radiation loss of the antenna.

For practical extraction of a signal from a device like this, a number of other circuit components are required. A shunt resistor is required to suppress low-frequency parasitic oscillations. Capacitive coupling is required both to geometrically define the length of the slot, and to provide a low impedance path at the high frequencies targeted for these devices. Metal-insulator-metal (MIM) reflectors are chosen for this coupling. Furthermore, for focusing of the signal onto an appropriate THz detector, a lens is required. Most of the radiated signal is transmitted through the substrate [46], so attaching the lens to the substrate is a common solution to retrieve the signal [47].

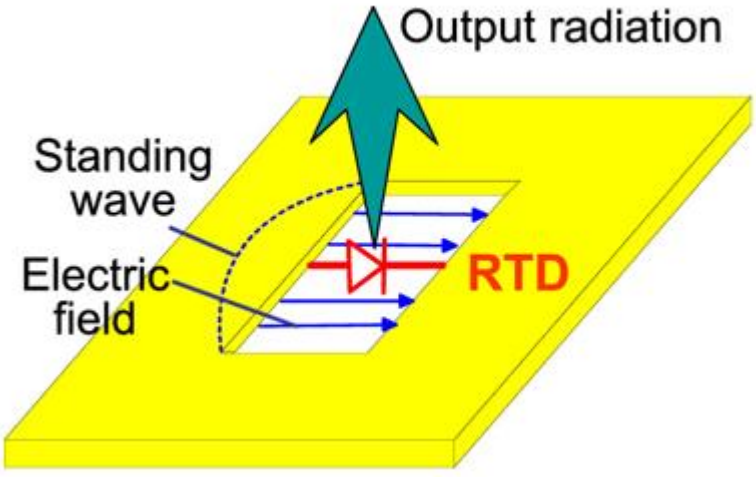

Figure 1-10: *RTD device inserted in a metal slot antenna structure which acts as a resonator to emit a high frequency signal, adapted from [13]*

The basic operation of RTD devices has been described in this section, with regards to the physics, I-V characteristics, and the signal output. Over the last 50

years, there have been significant advances in this field of research, and in Section 1.6, this research will be detailed, up to and including the state of the art today.

1.6 Advances in RTD Design

As mentioned in Section 1.5, GHz emissions were first obtained from RTD devices by Sollner *et al.* in 1984 [45], at 200K. This was limited by the external circuitry, as well as several aspects of the epitaxial and device structures. Future research was able to improve on this, allowing for steadily improving frequency and power output values. In 1987, Brown *et al.* [48] demonstrated oscillations up to 56GHz with a 60μW power output, at room temperature. This was done mainly by improving the epitaxial structure of the device. The barrier width was reduced to 1.5nm compared to 5nm from [45], increasing the current density, and therefore, the power. The barrier material was different, with AlAs used instead of $Al_{0.35}Ga_{0.65}As$. AlAs has a much larger barrier height, reducing thermionic emission [49]. Also, by having a lower doping concentration of the GaAs outside of the barriers, the capacitance of the device is reduced. This is caused by an increase in both the width of the depletion region and the required bias voltage and allows for higher frequency signals to be obtained [48]. In 1988, Brown *et al.* [50] improved their measured frequency output up to 200GHz, primarily by using smaller waveguides to extract signals of higher frequencies. Theoretical frequency values of up to 600GHz were also proposed.

Several material systems have also been explored for RTD devices and some of these are summarised in Table 1-1. In 1990, Mehdi & Haddad [51] fabricated devices on the $In_{0.53}Ga_{0.47}As$/InAlAs and the $In_{0.53}Ga_{0.47}As$/AlAs systems. The InAlAs barriers have a lower electron effective mass in comparison to the AlGaAs system, improving the current density through the device. In addition, InAlAs and AlAs barriers have higher barriers than AlGaAs, which reduces thermionic emission and thus improves device performance. InGaAs (μ_e=9000cm^2/V.s) also features higher electron mobility than GaAs (μ_e=9000cm^2/V.s), and is easier to form ohmic contacts on, both considerable advantages when it comes to fabricating RTD

devices. Brown *et al.* [52] also demonstrated oscillations up to 712GHz on InAs/AlSb RTDs, in 1991. In this material system, electrons can tunnel through barriers more easily due to the staggered (Type II) band structure, compared to the Type I structure for GaAs/AlAs, resulting in a greater current density. Electron mobility in InAs (μ_e=40000cm^2/V.s) is also higher than in GaAs, which increases the potential frequency output. The power of the 712GHz signal was measured as 0.3μW, demonstrating the difficulty in increasing both power and frequency in these devices. The InAs/$In_{0.53}Ga_{0.47}As$/AlAs material system was demonstrated by Smet *et al.* [53] in 1992 to produce devices with very high peak to valley current ratios of 50. InAs was used as a sub-well within the QW structure, allowing for the QW to be narrower while keeping the E_1 quasi-bound state low.

***Table 1-1**: Table displaying electron mobility, effective mass and bandgap for a number of well and barrier materials used in the literature*

Material		*μ_e (cm^2/Vs)*	m_e^*/m_0	E_g (eV)
Well	GaAs	8500 [54]	0.067 [55]	1.42 [54]
	$In_{0.53}Ga_{0.47}As$	11500 [56]	0.041 [57]	0.75 [58]
	$In_{0.8}Ga_{0.2}As$	21900 [59]	0.032 [60]	0.50 [58]
	InAs	30000 [61]	0.023 [60]	0.36 [58]
	InSb	78000 [62]	0.014 [63]	0.17 [64]
Barrier	AlGaAs	1530 [54]	0.092 [54]	1.86 [54]
	AlAs	200 [54]	0.15 [65]	3.10 [66]
	$In_{0.52}Al_{0.48}As$	4500 [67]	0.072 [60]	0.7 [66]
	AlSb	250 [68]	0.14 [66]	2.39 [66]

In 1997, Reddy *et al.* [69] reported oscillations of 650GHz from a 64-element array of RTD devices with Schottky collector contacts, though power values for this array were unable to be obtained due to limitations with the instrumentation. However, a 16-element array was found to emit signals at 290GHz with 28μW of power. Orihashi *et al.* [70] integrated the RTD into a slot antenna and achieved 587GHz output with 8μW of output power. Calculated values of 90μW at 1THz were found to be possible for these devices, from optimisation of the device structure, and theoretical frequencies of up to 3THz were determined for the RTD itself. This demonstrated the potential of RTD devices and prompted another wave of research into their properties.

By steadily improving this slot antenna device structure, the operation frequency gradually increased to 831GHz [71], then 915GHz [72], before breaking the THz barrier with oscillations at 1.04THz [26]. This trend continued with oscillations obtained at 1.31THz [73], 1.40THz (with a patch antenna structure) [74], 1.42THz [75], 1.55THz [76] and up to 1.92THz [27]. Izumi *et al.* [25] demonstrated 1.98THz oscillations, the highest frequency achieved for a single oscillator at room temperature. To achieve this record frequency, small adjustments were made to the device structure, in particular the antenna electrode. These devices operate with a slot antenna structure and the limiting factor on frequency was determined to be the losses of the antenna, caused by the air bridge and antenna electrode resistances. In [27], Maekawa *et al.* optimised the air bridge resistance and so, the antenna electrode resistance became the main limiting factor. To reduce this, the thickness of the electrode is increased to 2μm from the original 50nm, overcoming the skin effect (Au skin depth at 2THz = 60nm) thus reducing the electrode resistance, and increasing the frequency of the emitted signal. No power value was quoted for this result.

There have been considerable developments in enhancing the power outputs of RTD devices also. Many high-frequency feature power on the level of tens of μWs, when mWs are required for the any practicality. In 2010, Hinata *et al.* [77] obtained 200μW from a single RTD device operating at 443GHz, by offsetting the position of the RTD in the slot antenna structure. Shiraishi *et al.* [78] extracted 420μW at 548GHz by grading the indium percentage of the InGaAs on the emitter side and reducing the barrier thickness, to improve the RTD performance with the same antenna structure. A power of 1mW was achieved at 260GHz by Al-Khalidi *et al.* [79] in 2019 by increasing the device area. To compensate for the ensuing increase in capacitance, the inductance was reduced with a microstrip short stub resonator to still achieve frequencies in the THz range.

Arrays of RTDs have been demonstrated to achieve higher power outputs. Suzuki *et al.* [80] obtained powers of 610μW, 270μW, and 180μW, at frequencies of 620GHz, 770GHz and 810GHz respectively for a 2-element array. In [81], an 89-element array produced 730μW at 1.01THz. However, the outputs from the devices were not coherent, and so the structure was not optimised. In 2022, Koyama *et*

al. [82] constructed a 36-element array to give an 11.8mW output at 450GHz. The device design is shown in Figure 1-11.

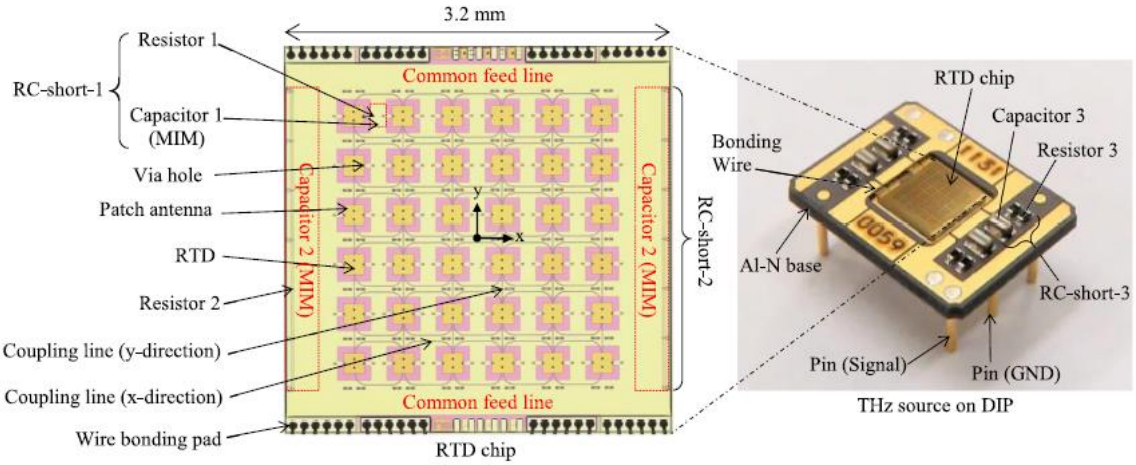

***Figure 1-11**: 6x6 array of RTD devices with patch antenna structures and external circuitry, from Koyama* et al. *[82].*

This represents the state of the technology today. Research is ongoing to optimise both single RTD devices and arrays, in terms of power and frequency output. For applications in communication, certain power and frequency targets must be reached for the devices to be viable. For 5G systems nowadays, frequency bands up to 71GHz [83] are being used. For 6G, there are no set frequency bands chosen yet although the expectation is to look towards the sub-THz region (90-300GHz) for very high data rate applications. Beyond 6G, frequencies in the THz region must be used. As shown in Section 1.2, atmospheric attenuation limits the range of signals as the frequency increases. For 5G, ranges up to 600m can be achieved [84] so in the 6G case, with at least a factor of 10 increase in attenuation, ranges up to 60m could be targeted. To achieve this, power values in the mW range will be required from THz emitters. Optimising the power output from these devices will allow for greater ranges and therefore make the technology more feasible in practice. As has been seen from the literature in this section, the values that have been obtained are approaching the required parameters for applications as a THz emitter.

1.7 Gaps in Knowledge

The work summarised above illustrates the wealth of research that has been done into RTDs since their invention in 1974. Devices have been made with a large variety of materials and structures for a wide range of applications. The primary application concerned in this work is for THz communication, and for THz emission, in particular. Therefore, it is necessary to find some way to optimise the design and fabrication of RTD devices to allow for these applications to be realised in the near future.

Several device designs and fabrication processes have been demonstrated in the literature with very specific aims of minor increases in frequency and power. However, for RTDs to become a more practical technology, the fabrication process requires simplicity in combination with performance. It is important to develop a process which is relatively cost and time-effective, while still producing devices which meet the requirements for a THz emitter. Therefore, the construction of these devices must be broken down into steps with each step optimised accordingly. In this work, the fabrication of the electrical component of the RTD will be investigated, with the aim of producing working devices with comparable electrical characteristics to those found in the literature, but a simplified development process. To do this, some method of comparison with the literature is required.

The RTD literature consists of 50 years of work across the world, with a vast range of devices optimised for different purposes. The optimisation of RTD devices requires a figure of merit (FoM) which can be extracted from these devices in the literature and compared across them all. In 2016, Baba *et al.* [85] introduced an FoM, to be later named the intrinsic resonant efficiency (IRE), which allowed for a way to analyse the electrical characteristics of a device regardless of structure. Simulation work was then performed to determine how the IRE could be optimised [86] by altering the epitaxial structure. A full critical review, based on results from the literature, would provide an alternate method of optimising this FoM. By looking back and analysing older research and a large variety of device structures, trends in electrical characteristics can be identified, and the impact this has on

the IRE can be visually represented to allow for optimisation of device design in the future.

Following on from this, investigating the perceived trends through a systematic analysis is also required. By fabricating devices with identical epitaxial structures except for the parameter being investigated, the number of variables in the experiment can be drastically reduced. Fabricating these devices in parallel also reduces variations and allows for a more accurate assessment of the effects caused by small changes to the device structure. This systematic analysis validates the critical analysis work done, as clear trends should be visible following device characterisation. In this thesis, these gaps in the knowledge will be addressed.

1.8 Thesis Outline

In this thesis, the task of realising RTD devices in practice will be investigated. Firstly, a fabrication process is developed in Chapter 2 with the aim of establishing a simple, quick method to manufacture these devices. Keeping the process as simple as possible lowers the barriers to adoption of these devices for applications in the future. Electrical characterisation of these devices is also done, with the values obtained vital to the optimisation of RTD devices.

In Chapter 3, these electrical characteristics are properly investigated. A critical analysis of the literature is performed, aiming to identify trends across a wide variety of different device designs and structures. The IRE is analysed, within the context of its suitability as an FoM for the electrical characteristics of the devices.

Following this, Chapter 4 demonstrates the need for a systematic investigation into the effect of the epitaxial parameters on the RTD performance. Several QW structures are explored, and more reliable conclusions about the IRE can be drawn from this type of analysis.

In Chapter 5, the work done in this thesis is summarised, and conclusions are drawn based on the results obtained. A list of future work is given, as this thesis represents the start of an important step in realising RTDs as practical, produceable devices for THz emission in the near future.

Chapter 2 : Development of Fabrication Process

2.1 Motivation

In this chapter, the process developed to fabricate RTD devices will be detailed. The aim is to establish a fabrication process which can produce devices in a quick and cost-effective manner. For a quick process, the number of steps must be minimised, whilst still delivering a high quality of device. For a cost-effective process, not only is a quick process helpful, but also the choice of tools and chemicals used. This process will use chemicals and tools that are likely to be available in any cleanroom facility for micro or nanofabrication, so that these steps can be reproduced as easily as possible. These considerations are intended to aid future fabrication processes for mass production of RTD devices. The process detailed in this chapter was adapted from an existing process, introduced by K. Jacobs [87]. This is called a dual-pass structure, as the current must flow through the RTD QW layers twice between the metal contacts. This device structure was chosen as it simplifies the fabrication process, with details of this in Section 2.3 below.

Firstly, the device structure is described, with the motivation behind the choice of both device and epitaxial structures explained. Then, the minimisation of the contact resistance of the devices is investigated – an important parameter to consider for high-frequency devices as it can limit device performance. Following this, the fabrication process is broken down into its three main steps, with each of these steps fully detailed. Descriptions of some of the challenges faced and the work done to optimise the process are given also. Penultimately,

the electrical characteristics of some fabricated devices are shown, demonstrating the effectiveness of this fabrication process to produce RTD devices. Finally, possible improvements to the process are given, and future work required to realise these improvements is discussed.

2.2 RTD Figures of Merit

A figure of merit is a measure of the performance of a device. They are extremely useful as they allow comparisons to be made and thus, optimisation of device designs and structures. There are normally several different FoMs for any given device which provide measurements for various aspects of the device performance. The needs of the user will determine which FoMs are the most important and require optimisation.

As we are considering the application of an RTD as a THz emitter in this thesis, the most important output parameters to consider are the power and frequency. The RTD device can effectively be split into two parts: the resonator and the antenna. In this thesis, we focus on the resonator design, comprising of the epitaxial structure, and the device structure and dimensions. To optimise the output from the whole device, it is important to first optimise the output from the resonator. Therefore, an investigation into the I-V characteristics is required. From the I-V characteristics, we can measure and calculate several FoMs, shown in Table 2-1.

***Table 2-1**: List of RTD characteristics which can be measured directly, and those which can be calculated using these measurements.*

Measured	*Calculated*
J_{PK} – Peak current density	PVCR – Peak-to-valley current ratio
J_V – Valley current density	IRE – Intrinsic resonant efficiency
V_{PK} – Peak voltage	G_{RTD} – RTD conductance
V_V – Valley voltage	C_d – Device capacitance
P_{OUT} – Output power	P_{MAX} – Maximum theoretical output power
f_{OUT} – Output frequency	f_C – Maximum theoretical output frequency

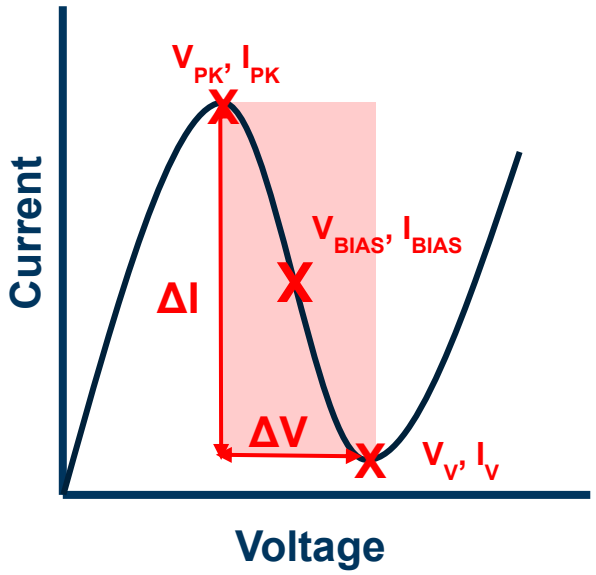

***Figure 2-1**: Example of an RTD I-V graph with the NDR region shaded in red. Important current and voltage values are also denoted.*

The peak and valley values are taken directly from the I-V characteristics, as shown in Figure 2-1. The area of the device must be known to find the current density values. A higher peak current density, J_{PK}, means more electrons pass through the RTD structure, and translates to a higher power output. The peak voltage, V_{PK}, would ideally be minimised to reduce the power required to operate the device. The valley current density, J_V, consists of non-resonant transport mechanisms through the double barrier structure such as scattering caused by interface roughness or impurities, phonon scattering, and thermally assisted tunnelling through higher quasi-bound states. Minimising these processes allows for greater efficiency in the device. The valley voltage, V_V, occurs due to electrons

tunnelling through higher energy levels in the QW. Therefore, the gap between energy levels determines V_V, and should be maximised to increase the size of the NDR region and reduce the RTD conductance, G_{RTD}. The PVCR is calculated by:

$$\boldsymbol{PVCR = \frac{J_P}{J_V}} \quad (1)$$

Where J_P and J_V are the peak and valley current densities, respectively. The RTD conductance is given by:

$$\boldsymbol{G_{RTD} = \frac{3\Delta I}{2\Delta V}} \quad (2)$$

Where ΔI and ΔV are the current and voltage ranges within the NDR region, as shown in Figure 2-2. The IRE, which is investigated in more detail in Chapter 3, is expressed as:

$$\boldsymbol{IRE = \frac{P_{MAX}}{P_{BIAS}}} \quad (3)$$

Where P_{MAX} is found from [88]:

$$\boldsymbol{P_{MAX} = {}^{3}/_{16}\,\Delta I \Delta V} \quad (4)$$

And:

$$\boldsymbol{P_{BIAS} = I_{BIAS} V_{BIAS}} \quad (5)$$

I_{BIAS} and V_{BIAS} represent the bias current and voltage of the device, which is generally set to the midpoint of the NDR region. An estimate for the output frequency of the device can be found from [88] to be:

$$\boldsymbol{f_c \cong \frac{1}{2\pi C_0}\sqrt{\frac{G_{RTD}(1 - G_{RTD}R_C)}{R_C}}} \quad (6)$$

Where C_0 is the capacitance of the device, given by:

$$C_0 = \frac{\varepsilon A}{d} \quad (7)$$

And R_C is the device contact resistance, given by:

$$R_C = \frac{\rho_C}{A} \quad (8)$$

Where ε is the permittivity, A is the device area, d is the length of the QW structure, and ρ_C is the specific contact resistivity. The actual output power and frequency can only be found once the antenna structure has been fabricated. The antenna structure adds more variables, and thus optimisation of power and frequency are more difficult. Furthermore, for the critical analysis of the literature performed here, there is more material available of just the resonator structure without the antenna, and so the analysis is concerned with only this section. Further analysis is required for the antenna structures in the literature.

The focus of this analysis will be on the PVCR and IRE, both derived from the relationship between the peak and valley points of the I-V curve. P_{NDR} is used interchangeably with P_{MAX} here, as it is calculated from the spans of the NDR region. This applies to the simplified ideal RTD, ignoring parasitic elements and higher harmonics of the voltage as well as approximating the I-V characteristics to a cubic equation. The input power to the device, P_{ELEC}, is equated to P_{BIAS}, which is chosen as the midpoint of the NDR region of the I-V curve. From [47], this is the optimal bias point for maximising power output as it maximises the possible voltage swing. The IRE can therefore be defined as:

$$IRE = \frac{P_{NDR}}{P_{ELEC}} \quad (9)$$

Where P_{NDR} is defined the same as P_{MAX} from Equation 4, and P_{ELEC} is the same as P_{BIAS} in Equation 5. The parameters for calculating IRE are shown on the I-V graph in Figure 2-2.

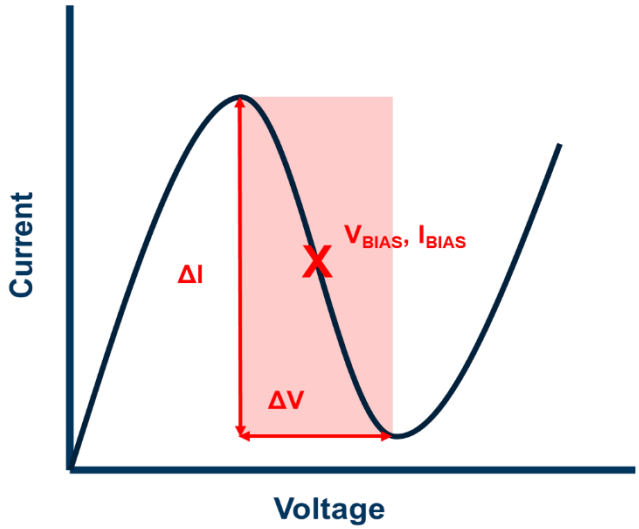

***Figure 2-2**: Example of an RTD I-V curve, with pertinent points for calculating IRE indicated.*

The PVCR has been used as a FoM for a long time, as an indicator of the quality of the epitaxial structure. However, the IRE is a more recently defined FoM [85] and is a ratio of the theoretical output power, P_{MAX}, to the supplied input power at the bias point in the middle of the NDR region. Optimising the IRE is important for increasing the overall power output of the device.

Several different equivalent circuits have been used to represent the behaviour of an RTD, representing different operating modes of the device. In Figure 2-3, a lumped circuit model of an RTD is shown.

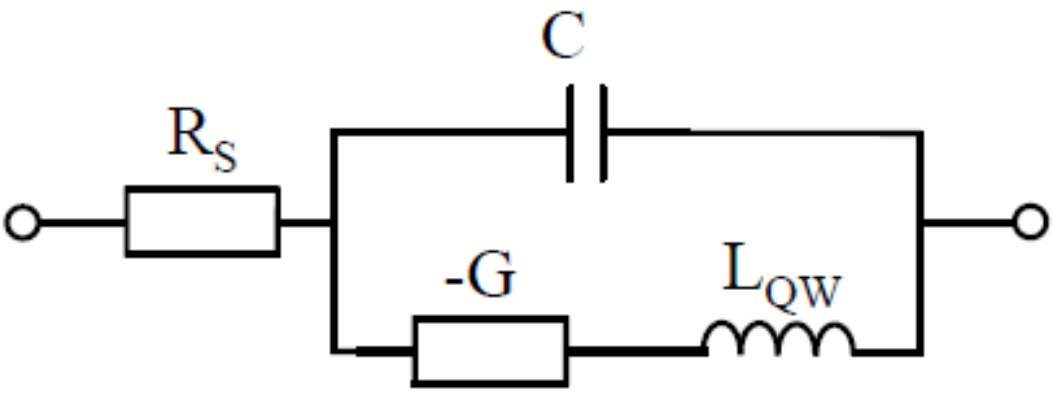

***Figure 2-3**: Small-signal equivalent circuit of an RTD.*

The negative differential conductance (NDC) of the RTD, G, is calculated as shown in Equation 2. This is in series with L_{QW}, an inductance which represents the time taken for electrons to travel through the QW. There is a delay between

applying the voltage across the device, and the electrons travelling through the QW, so an inductor most accurately represents this behaviour. The capacitance, C, accounts for the "charging" and "discharging" behaviour which occurs in the depletion regions on either side of the QW, and R_S is the series resistance which is an accumulation of the parasitic resistances present in the materials used to make the device.

The resonator and antenna structures will also have equivalent circuits which affect the equivalent circuit of the RTD, and it is important to analyse these when trying to optimise the overall emitter performance. However, they will not be covered in this thesis. In addition to the electrical characteristics, the conduction band structure, shown in Figure 2-4 also provides useful information related to the performance of the device.

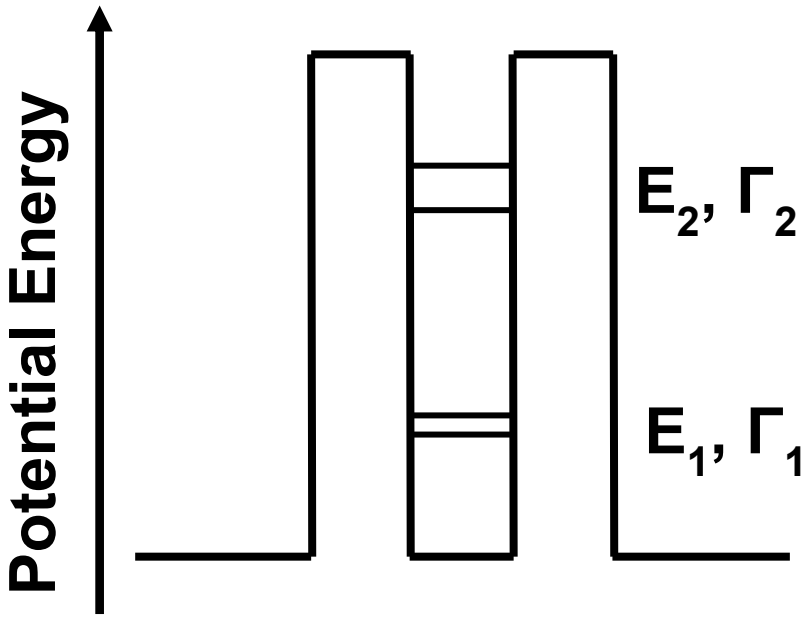

***Figure 2-4**: Conduction energy band diagram of the QW structure. Values for the quantised energy levels and linewidths in the QW, are labelled.*

Within the QW, the E_1 and E_2 levels, along with their respective linewidths, Γ_1 and Γ_2, dictate the nature of the NDR region. Wafer characterisation techniques such as photoluminescence spectroscopy are required to ascertain values for these, but the relative values between different device structures can be inferred from the I-V characteristics.

2.3 Dual-Pass Process

The process for fabricating RTDs was established based on the dual-pass structure proposed by K. Jacobs *et al.* [87]. The name dual-pass originates from the fact the current will pass through the RTD structure twice when bias is applied, as opposed to the more conventional RTD fabrication process [90] where only a single pass is required, as one side of the device is etched past the QW structure. The dual-pass structure allows for metallisation to be completed in one step (as opposed to two for the 'standard' process), meaning the contact resistances of both electrodes will be the same, low value. This simplifies the fabrication process and as the metal is deposited before any etching occurs, the risk of damaging the surface is mitigated, and the reproducibility of the process is improved. In addition to this, greater control over the device area is permitted by taking I-V measurements during the final etch step of the fabrication process. In single-pass structures, a second metallisation step is required following the etching step, and so the I-V measurements cannot be taken until the device is fully fabricated. The device structure is shown in Figure 2-5.

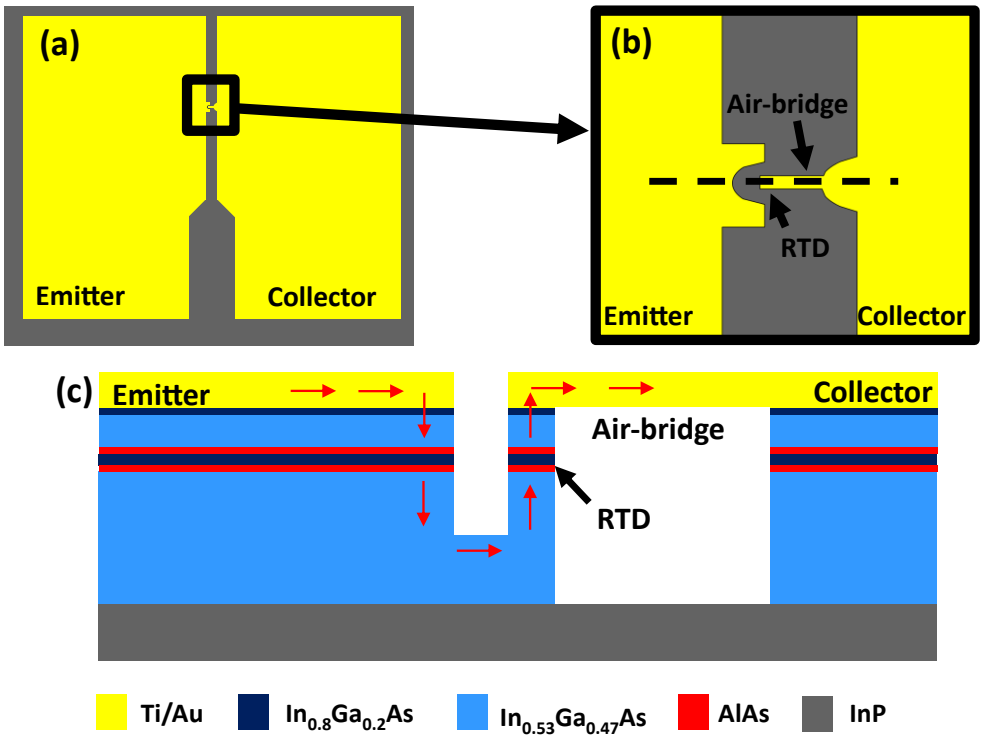

Figure 2-5: *Layout of device dual-pass structure. (a) shows the top-down view of a single RTD device, (b) shows a close-up view of the RTD bridge structure, and (c) provides a cross-section of the RTD area – the red arrows represent the direction of electron flow when in forward bias*

The total device area, visible in Figure 2-5(a), is 1mm x 1.3mm with large collector and emitter contacts on each side. This large area was chosen to allow for direct probing of the contacts when IV testing is done. Although certain geometric parameters of the device vary across the mask, the base design features a 20μm wide channel between the contacts and the critical device feature - the air-bridge structure - has a length of 8μm and width of 1.5μm. This width was chosen to be as small as possible while still allowing for reliable photolithography results. Narrower width air-bridges (1.25μm) were also present on the mask but could not be consistently achieved with the photolithography process. The cross-section of this critical feature is shown in Figure 2-5(c), illustrating the profile of the air bridge structure. The red arrows represent the flow of current when the device is biased for 1st quadrant operation. In this structure, RTD characteristics are obtainable in both forward and negative bias, although the I-V measurements will differ in each case according to the thickness of the spacer layers on either side of the QW. The epitaxial structure is shown in Figure 2-6. The wafers used in this thesis were grown by MOVPE at the National Epitaxy Facility at the University of Sheffield.

Thickness	Material	Doping (cm^{-3})
8nm	$In_{0.8}Ga_{0.2}As$	$2x10^{19}$:Si
15nm	$In_{0.53}Ga_{0.47}As$	$2x10^{19}$:Si
25nm	$In_{0.53}Ga_{0.47}As$	$3x10^{18}$:Si
20nm	$In_{0.53}Ga_{0.47}As$	Undoped
1.1nm	AlAs	Undoped
4.5nm	$In_{0.8}Ga_{0.2}As$	Undoped
1.1nm	AlAs	Undoped
2nm	$In_{0.53}Ga_{0.47}As$	Undoped
200nm	$In_{0.53}Ga_{0.47}As$	$3x10^{18}$:Si
400nm	$In_{0.53}Ga_{0.47}As$	$2x10^{19}$:Si
200nm	$In_{0.53}Ga_{0.47}As$	Undoped
100nm	InP	Undoped
InP substrate		

***Figure 2-6**: Example of the epitaxial structure of an RTD wafer. Layers are colour coded to match the material, although doping concentrations vary.*

The QW region is represented by the two red barriers, and the navy well region. The barrier (1.1nm) and well (4.5nm) widths are very narrow. The substrate thickness of InP is 350μm, and the rest of the layers only add up to around 1μm. Lattice-matched (LM) InGaAs i.e. $In_{0.53}Ga_{0.47}As$, matches the lattice constant of InP. This is used for the structure, minimising the risk of defects in the structure, which could affect the properties of the device. Although LM InGaAs is the only material between the substrate and the QW, the doping level changes. The layers with greater doping permit higher currents, and so the $2x10^{19}cm^{-3}$ doped layer makes up part of the current path through the device. This layer is 400nm thick to make wet etching to this depth easier, as wet etching can present issues with non-uniformity, and difficult to control etch rates. The 2nm and 20nm spacer layers on either side of the QW are undoped, chosen to minimise capacitance in the device. Higher doped LM InGaAs layers are used once again above the QW structure to enhance current flow and, in combination with the $In_{0.8}Ga_{0.2}As$ cap layer, to reduce the contact resistance, which is a very important parameter in RTD devices.

2.4 Contact Resistance Investigation

Although contact resistance is important for most fabricated devices, it is especially vital for RTDs as it has a direct effect on the signal output from the device. To obtain high-frequency signals, resistive losses must be reduced, and the RC delay is often a limiting factor on the frequency. Other devices feature additional contributors to the device resistance which must be minimised to maximise the frequency output. For example, the channel or sheet resistances in transistor devices also affect device performance. However, for RTDs the contact resistance is the main limiting resistive factor and therefore, an investigation into minimising contact resistance has been done.

To minimise contact resistance, there are several factors to consider. We want to reduce the potential barrier between the top semiconductor layer ($In_{0.8}Ga_{0.2}As$, in our case) and the metal deposited on top. Therefore,

consideration of surface preparation of the semiconductor is required, the choice of metal, and annealing of the contact after deposition.

To determine the specific contact resistivity, test structures are required. The simplest structures are the transfer length method (TLM) structures proposed by Shockley [91], which are rectangular metal contacts deposited on the semiconductor surface, with gradually increasing separation. For each set of TLM structures, a mesa etch is required to isolate the metal contacts and prevent current spreading in the semiconductor. An example of a set of TLM structures is shown in Figure 2-7 along with a graph depicting how contact resistance is calculated.

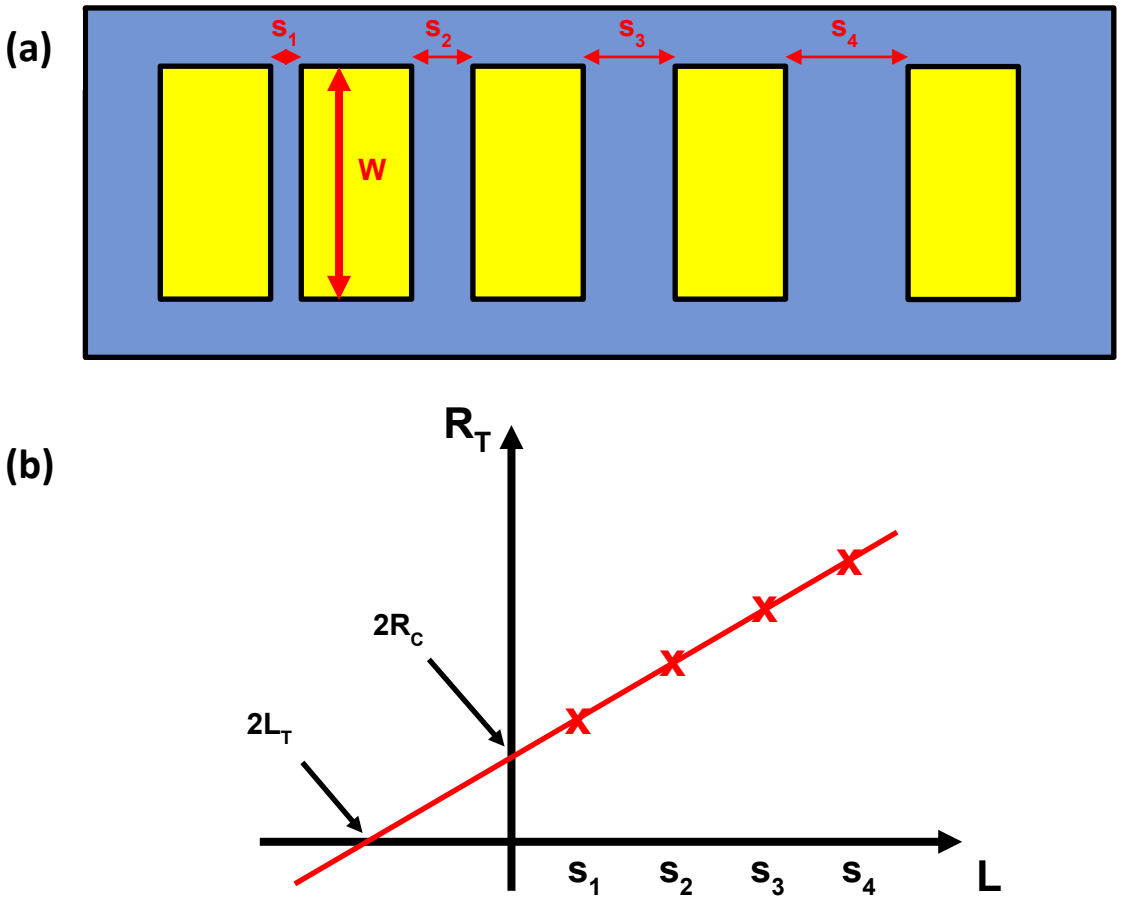

***Figure 2-7**: (a) Top-down view of the TLM structure, and (b) how values are extracted to calculate the specific contact resistivity, ρ_c.*

The resistance values are obtained from the I-Vs for each pair of contacts and plotted against the separation between each contact (s_1-s_4). The resistance

increases linearly with the current path length, and this relationship can be extrapolated through the y and x-axes to give values for the contact resistance, R_c, and the transfer length, L_T. The transfer length refers to the path length of the current under the metal contacts before it travels through the metal-semiconductor interface and into the contact. The specific contact resistivity, ρ_c, is the parameter used to compare the quality of the metal-semiconductor interface for different samples, and is calculated as shown in Equation 10.

$$\rho_c = R_c W L_T \tag{10}$$

where W is the width of the TLM structure, as shown in Figure 2-7. The circular transfer length method (CTLM) is used in this work, which uses a similar system except the test structures are circular in shape [92] [93], shown in Figure 2-8(a). CTLMs have the advantages of a simpler fabrication process, due to the removal of the mesa etch step.

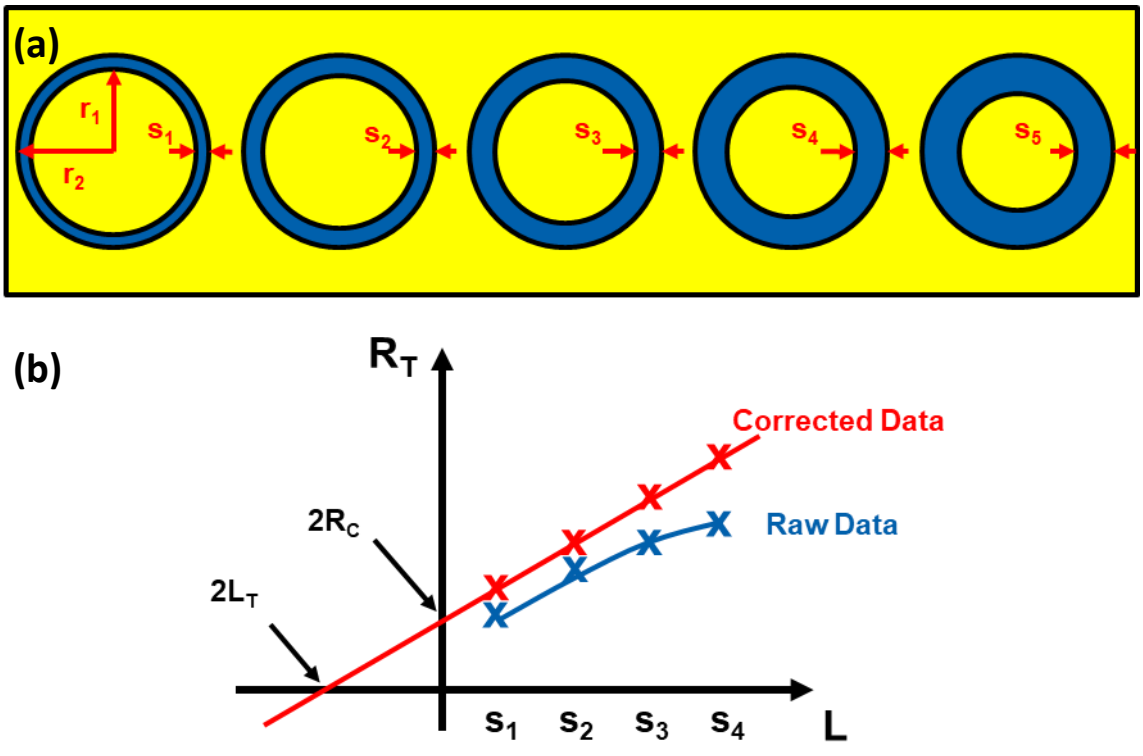

***Figure 2-8**: (a) Top-down value of the CTLM structure, and (b) how values are extracted to calculate the specific contact resistivity, ρ_c.*

A correction factor, C, is required due to the circular geometry of the CTLMs. This is given by:

$$C = \frac{r_1}{s}\ln\left(\frac{r_1 + s}{r_1}\right) \quad (11)$$

where r_1 is the internal radius of the CTLM structures, and s is the separation between the CTLM structure and the contact pad.

The CTLM structures are based on rectangular TLM structures, where the current path is gradually increased across a row of structures. Each structure is tested, and the resistance is shown to gradually increase as the path length increases. In the TLM case, these resistances can be linearly extrapolated to the y and x-axes, allowing the contact resistance and transfer length to be found, respectively. However, in the CTLM case, a correction factor calculated for each data point must be applied before linear extrapolation can be performed, shown in Figure 2-8(b). Then, the calculations follow the TLM process.

Furthermore, four-probe measurement was used to obtain the I-Vs from these test structures. This removes the effects of parasitic resistances which affect the results taken with two-probe measurement. For resistance values as low as we'd expect for n-InGaAs ohmic contacts, this parasitic resistance can have a notable effect on the values measured.

From the literature, several different techniques have been shown to aid in reducing the contact resistance. The preparation of the semiconductor surface is a vital parameter to consider, with various cleaning processes used, both dry and wet. Next, the choice of metals to be deposited in the stack is important for reducing the barrier height between the semiconductor and metal. Finally, annealing of the deposited metal can further reduce the contact resistance, with the right temperature and time settings. To minimise the contact resistance, all these factors must be investigated for the semiconductor surface being used which is n-type InGaAs in this case.

One of the most common dry cleaning processes is a combination of ultraviolet light (UV) and ozone (O_3). Several examples exist in the literature of this technique working to lower contact resistance values for samples with varying In compositions (53% to 86%) [47] [94] [95] [96], and a very low ρ_c value of $0.73\Omega\mu m^2$ is obtained by Crook *et al.* [97] with a 10 minute UV/O_3 clean as part

of the surface preparation stage. Several different wet cleaning stages are also available. These can be used to clean the surface of contaminants, but also to remove the native oxide on the semiconductor surface prior to metal deposition. These generally consist of an etching agent diluted with water to slow down the etch rate and allow only the native oxide layer to be etched without damaging the semiconductor surface itself. This has been done with hydrofluoric (HF) acid [95] [96] - called a buffered oxide etch (BOE) -, hydrochloric (HCl) acid [94] [98] [99], and ammonium hydroxide (NH_4OH) [47] [100] [101]. Crook *et al*. [97] used a 10 second NH_4OH dip to achieve the very low specific contact resistivity as mentioned previously.

The first factor to be investigated here is the surface preparation of the samples. A base sample was prepared with no surface preparation to give an idea of the specific contact resistivity values. Then a comparison with O_2 ashing, and with UV/O_3 cleaning was performed. Both processes act to remove contaminants from the surface by oxidising them and thus, desorbing them from the surface of the semiconductor. Following this, different concentrations of NH_4OH were investigated for oxide removal. Furthermore, the effect of in-situ argon (Ar) sputtering was investigated. The metallisation tool used also includes an Ar sputtering gun, for cleaning the sample in the chamber under vacuum prior to metallisation. A comparison of all these methods can be seen below in Figure 2-9. All the samples here were cleaned with acetone and isopropyl alcohol (IPA), then underwent the appropriate surface preparation, before photolithography, metallisation and lift-off were performed. They were all metallised with 20/200nm Ti/Au and measured using the four-probe technique.

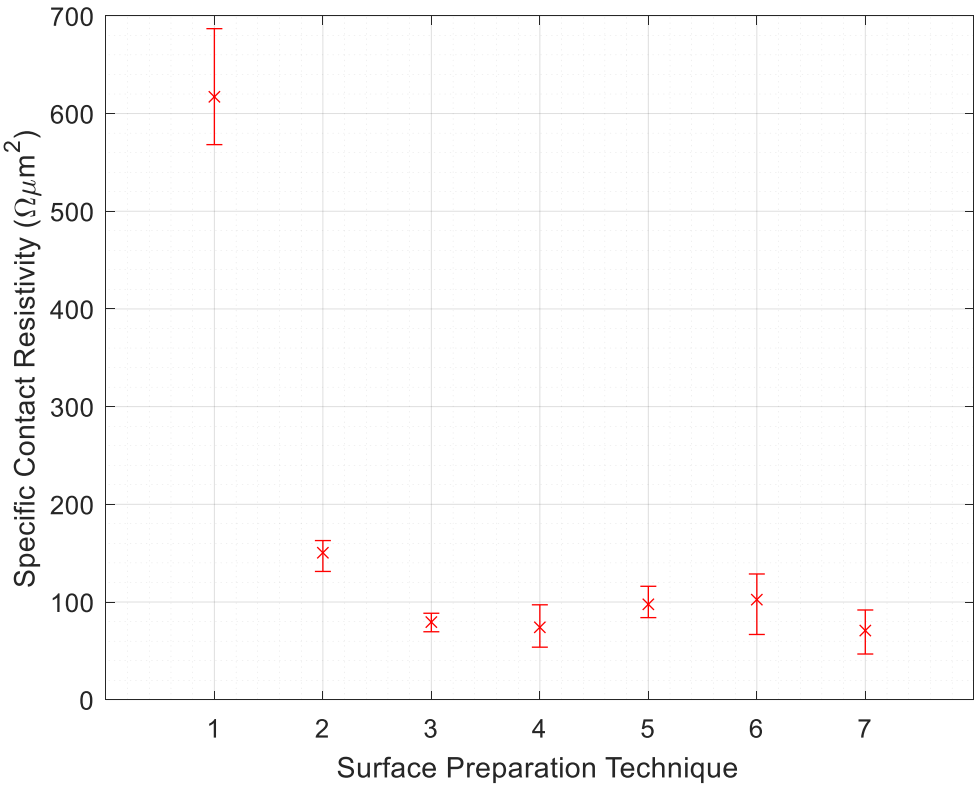

***Figure 2-9**: Graph depicting specific contact resistivity for a range of surface preparation techniques, described in Table 2-2 . Measurements are taken from several CTLM structures. The average and range of values for each technique are shown.*

***Table 2-2**: Table showing surface preparation techniques plotted in Figure 2-9, with values for the average ρc. and the calculated standard deviation, shown.*

Number	*Technique(s)*	*Avg. ρ_c ($\Omega\mu m^2$)*	*Std. Dev, σ_c ($\Omega\mu m^2$)*
1	No surface preparation	617.13	62.03
2	Ashing	150.43	16.82
3	UV/O_3	79.46	7.71
4	1:1 NH_4OH	74.12	19.38
5	UV/O_3 + 1:4 NH_4OH	97.66	13.12
6	2x UV/O_3	102.42	28.04
7	2x UV/O_3 + Ar sputter	70.77	19.07

For each surface preparation technique investigated, measurements from five sets of CTLM test structures were taken, and the average values are plotted in Figure 2-9 with error bars representing the variance of the calculated resistivities. There is a clear improvement found when any sort of surface preparation is done, with a ~4-8x reduction in specific contact resistivity compared to the no surface preparation case.

A comparison of ashing and UV/O_3 cleaning shows a notable difference in ρ_c and the standard deviation, σ_c. Both techniques were performed before spinning resist. The ashing step was 30 seconds, and the UV/O_3 step lasted 10 minutes. One of the advantages of using UV/O_3 over plasma ashing is that damage to the surface of the semiconductor is minimised. Plasma processes involve charged ions colliding and reacting with the surface of the material which can cause the displacement of atoms [102]. To avoid this damage, the asher tool must be operated at low power values which reduces the effectiveness of the surface cleaning process. From the results obtained, the UV/O_3 step results in a lower ρ_c, and σ_c, and so is preferred to ashing.

In addition to this comparison, other dry cleaning techniques are investigated. A second 10-minute UV/O_3 clean can be done before the metallisation step to remove any contaminants which may have been deposited during the lithography process on the semiconductor surface. However, on average, ρ_c is higher, and a larger spread of values is obtained. This could be caused by oxidation of the surface. Another technique explored here is the use of in-situ Argon sputtering. This capability was available as part of the metallisation tool, allowing the surface of the sample to be cleaned immediately prior to metal deposition. This significantly reduces the risk of contaminating the sample during the loading procedure. The lowest average ρ_c (70.77Ωμm^2) was obtained using the Ar sputtering step, suggesting it is very advantageous to use this as part of the surface preparation step.

NH_4OH was chosen for the wet cleaning step, with the main purpose of removing the native oxide prior to metal deposition. In addition to a 5s dip done in a 1:1 dilution with RO water, another technique combining a UV/O_3 clean with a 5s dip in 1:4 dilution was done for comparison. The sample which underwent an NH_4OH dip only, achieved the second-lowest average ρ_c of 74.12Ωμm^2, whereas the combination of UV/O_3 and NH_4OH resulted in a higher ρ_c. This is an interesting result, as we would expect both processes to work well together. However, when using NH_4OH dips, it was noted that the solution can react with the photoresist, resulting in displacement of features. This leads to photoresist scum on the semiconductor surface, and following metallisation, some of the features may not lift off, or may be completely removed. Reducing the concentration of the NH_4OH

dip was attempted, but no difference was found even at a 1:19 dilution. As a result, for a more consistent surface preparation process, the NH_4OH dip was omitted. Since a lower ρ_c was obtained without this step anyway, it is believed that the contact resistance will be low enough without the native oxide removal step.

The single lowest contact resistance found was 46.8Ωμm^2 for the surface preparation step featuring an Ar sputtering step. A thorough investigation into the removal rates of the Ar sputtering could not be done due to the failure and lengthy maintenance of this tool. The most consistent results, however, came from the sample with only the 10-minute UV/O_3 preparation, with a standard deviation of 7.71Ωμm^2. A combination of these procedures could yield even lower results. The UV/O_3 results give lower resistivity values than the O_2 asher and so UV/O_3 cleaning seems like the best dry cleaning procedure in this case.

Throughout the fabrication process detailed in Section 2.5, the Ar sputtering gun required maintenance and could not be used. Therefore, longer UV cleans were done to account for this, and to attempt to improve the cleanliness of the semiconductor surface.

Following the surface preparation of the sample, the next step to consider is the choice of metals. Within the literature, several different metals are chosen for deposition on n-type InGaAs surfaces. The simplest metal system is Ti/Au [47]. Titanium acts as an adhesive layer to the surface, while gold is chosen for its high conductivity and robustness. Alternatives to this are stacks using palladium (Pd) and platinum (Pt) as interstitial layers [95] [97] [100]. These layers also act as a diffusion barrier. Furthermore, Pd and Pt can be used as the contact layer as they can form phases with the semiconductor surface and lower contact resistivity, a process called solid phase regrowth (SPR) [103]. This is shown to be true for p-InGaAs, although Ti is still better in the n-InGaAs case. Molybdenum (Mo) has also been studied due to its high melting point [94] [104], and erbium arsenide (ErAs), which can be grown epitaxially *in-situ*, reduces the number of defects occurring at the metal-semiconductor interface [105]. The choice of metal contact is dependent on the work function of the metal, and how this aligns with the electron affinity of the semiconductor. A large difference in these values could

cause a large Schottky barrier height, increasing the contact resistance. Doping of the semiconductor can also reduce this barrier height and lower contact resistance [106].

The lowest values for specific contact resistivity were found in the literature for the Ti/Pd/Au metal stack [97], however other sources achieved higher values for the same choice of metals. Acceptable values were obtained for samples with the Ti/Au metallisation [47], and as this is the simplest, and was available on the metallisation tool used, this was chosen as the contact metallisation for the fabrication of the RTD devices in this work.

Another important technique that has been proven to reduce contact resistance is annealing of the metal contacts [97] [107]. Rapid thermal annealing (RTA) was the process used, with the sample annealed at a fixed temperature of 275°C in a nitrogen (N_2) atmosphere. The temperature was chosen as 275°C as annealing at 300°C and above has been shown to degrade the quality of the contact. Diffusion of the In from the semiconductor into the metal contact is believed to be the reason for this [108] [109]. To decide on an optimal annealing time, measurements were taken in 30 second steps and the specific contact resistivity calculated afterwards. The results are shown in Figure 2-10.

Initially, the annealing of the sample results in a reduction in ρ_C, and it hits the lowest value of 39.1Ωμm^2 after 60 seconds. It then stays roughly constant before increasing again after 2 minutes and 30 seconds. This increase can be attributed to the diffusion of In into the Au [108]. The optimal annealing time is therefore decided to be 1 minute.

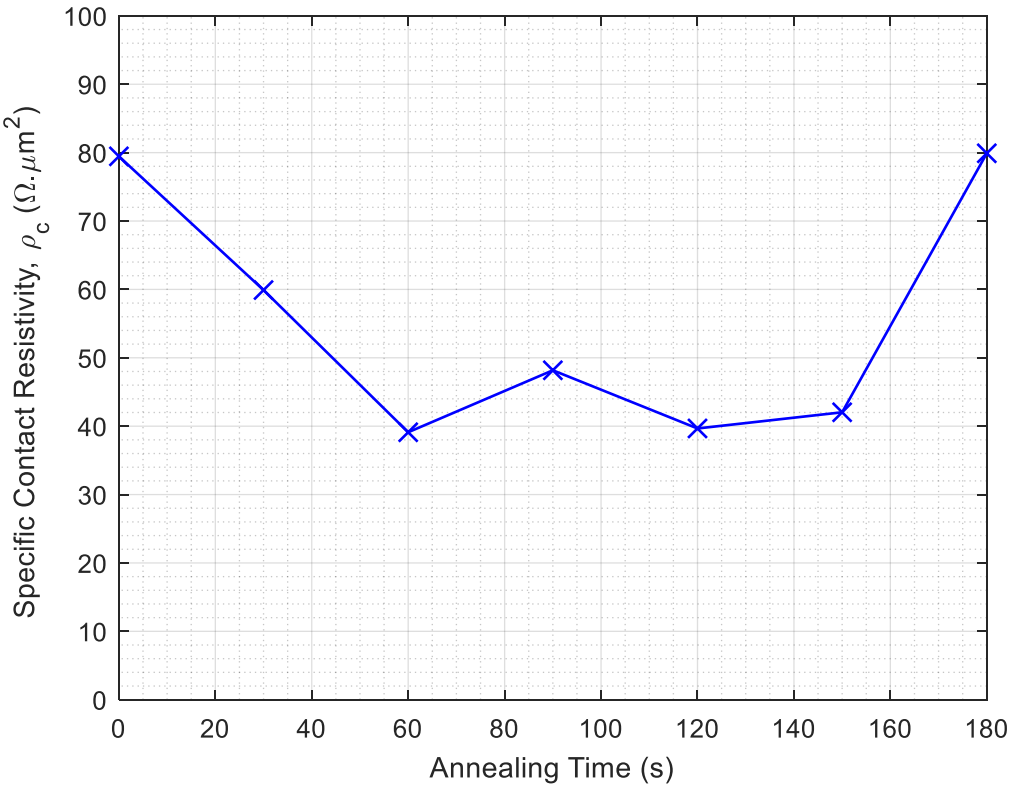

Figure 2-10: *Specific contact resistivity, ρ_c, against annealing time for a sample metallised with Ti/Au 20/200nm, and with a UV/O_3 surface preparation. The temperature was set to 275°C. The data points are averages of values calculated at six different locations on the sample.*

It is expected that a lower contact resistivity will be obtained when the Ar^+ sputtering is combined with annealing. Further future work that could be done is to properly investigate different metal stacks from the literature for a more comprehensive analysis. In comparison to the literature [97], these specific contact resistivity values differ by a factor of ~40 and so are not fully optimised for high-performance RTD devices. However, for the purposes of the work done in this thesis, the contact resistivity values are sufficient.

2.5 Fabrication Process

The full fabrication process is shown in Appendix A. A new photomask was designed for this process. The three main steps in the fabrication process are shown in Figure 2-11 - metallisation, shallow etch and deep etch.

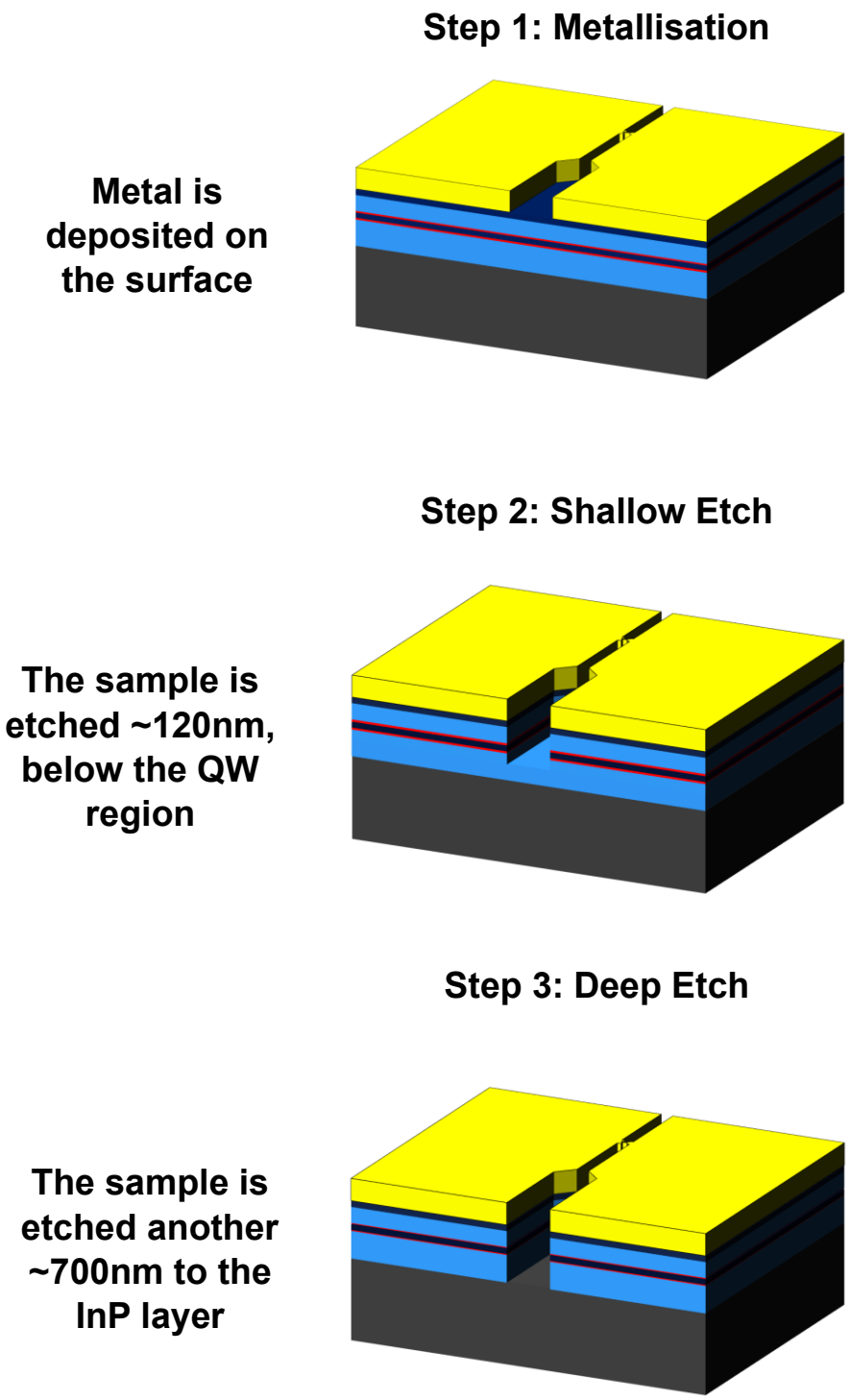

***Figure 2-11**: Overview of the main steps in the fabrication process for an RTD device.*

Compared to the dual-pass process in [87], a process using positive resist was chosen instead of a negative one due to the lack of a suitably thin, negative photoresist in the cleanroom facility. As one of the aims of this process is to be as accessible as possible, positive photoresists are more commonly used in cleanroom environments and thus were chosen for this process.

The metallisation stage consists of the cleaning of the sample, a photolithography step to transfer the pattern of the metal, and the metal deposition and subsequent lift-off. To start off, the sample is cleaned for 5 minutes each in acetone & IPA, agitated in an ultrasonic bath, before being dried with a N_2 gun. Then, it is subject to UV/O_3 cleaning for 20 minutes in an ultraviolet ozone cleaning system (UVOCS) tool [110]. The sample is then inspected to ensure the surface is clean. A dehydration bake at 200°C for 5 minutes is performed to remove any moisture from the surface of the sample before the resist is spun on. Since using a positive resist will result in an overcut resist profile which causes problems with metal lift-off, a lift-off resist (LOR) is deposited first. In this case, LOR 5A is used which gives an approximate thickness of 550nm when spun at 3000rpm [111]. The LOR is baked for 3 minutes at 150°C. S1818 photoresist is then deposited on top with a spin speed of 4000rpm, giving a thickness of around 1.8µm [112]. This is baked at 115°C for 2 minutes.

Following this, the pattern for the device is transferred using photolithography. A Karl Suss MA6 mask aligner [113] is used to expose the sample. Exposure tests were performed to determine appropriate exposure and development times to transfer the 1.5µm-wide bridges onto the sample. An image of an RTD device following the photolithography step is shown in Figure 2-12.

***Figure 2-12**: Optical microscope image of RTD air-bridge area pre-metallisation.*

Underexposure leads to some photoresist remaining in the critical features which would then lift off all the metal during the lift-off stage. Overexposure causes the edges of patterns to receive a higher dose of UV light than they should, causing rough edges and the rounding of corners. In addition to this, the development time must be optimised as this varies with exposure time. Underdevelopment has the same problems as underexposure where the resist is

not fully removed. Overdevelopment can cause the rounding of features and reduction in feature size until they are eventually removed completely at extreme development times. The optimal exposure time was found to be 8 seconds with a 40 second development time which provided the results seen in Figure 2-13. MF-319 is used for the development as this develops both the LOR and the S1818 simultaneously. Following this step, a UV/O_3 clean is performed for 10 minutes to clean the surface further (also reducing specific contact resistivity) and remove resist residues that remain from the development stage.

Metal is then deposited onto the sample. From the contact resistivity study, a Ti/Au metallisation is performed. The thickness of the metals is dictated by the thickness of the LOR to optimise lift-off. From the LOR datasheet, the LOR must be at least 1.2x thicker than the metals, so 20nm of titanium and 350nm of gold are chosen. The metals are evaporated onto the sample inside a PLASSYS MEB550S e-beam evaporation unit [114]. The sample is then lifted off in Microposit Remover 1165 [115] at 50°C and inspected to ensure the metal has lifted off correctly. Images of the metallised samples are shown in Figure 2-13.

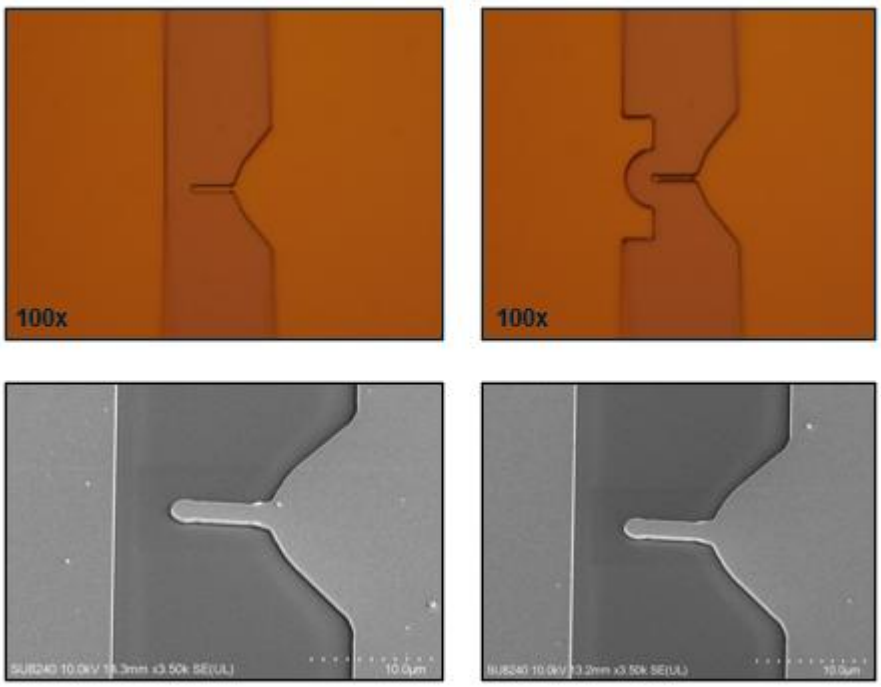

***Figure 2-13**: Two optical microscope images (at 100x magnification), and two SEM images, of the RTD device after metallisation and lift-off has occurred.*

The second step in the fabrication process is the shallow etch step. In this stage, the semiconductor is etched through the RTD structure down to the highly

doped emitter layer. This layer forms part of the current path of the device, as shown in Figure 2-5. A wet etch process is chosen for both etch steps as it is a quicker process, and dry etch processes can damage the surface of the sample [116] which is particularly problematic in smaller devices like the RTD. The wet etch process can be controlled reasonably well and give consistent results when repeated. The etchant used was a H_3PO_4:H_2O_2:RO water solution with a 1:1:38 ratio which selectively etches InGaAs over InP. An etch rate of around 120nm/minute was deduced from repeated wet etch tests although this rate can vary significantly sometimes. Therefore, the etch rate is always checked with a 30 second etch at the start of the process to ensure there are no under or over-etching problems. Before performing the etch, the sample is cleaned once again with a 2-minute Acetone and IPA clean in an ultrasonic bath, followed by a 10-minute UV/O_3 clean. The etch rate of the solution is then determined, and the sample is etched to a depth of 120nm, which should require 1 minute at the expected etch rate. The depth of the etch is measured using a DektakXT stylus profiler [117].

The third stage of the fabrication process is the deep etch stage. In this step, photoresist is patterned onto the RTD mesa area to protect that area from the subsequent wet etch. The sample is then etched down to the InP substrate to isolate the metal contacts and form the mesa of the device. Further wet etching leads to lateral etching under the bridge structure to create an air-bridge and the formation of the RTD device at the end of the bridge. An air-bridge structure reduces the parasitic capacitance of the device which can be a limiting factor for the output frequency. It also allows for greater control over the device area during the fabrication process. Figure 2-14 illustrates these steps.

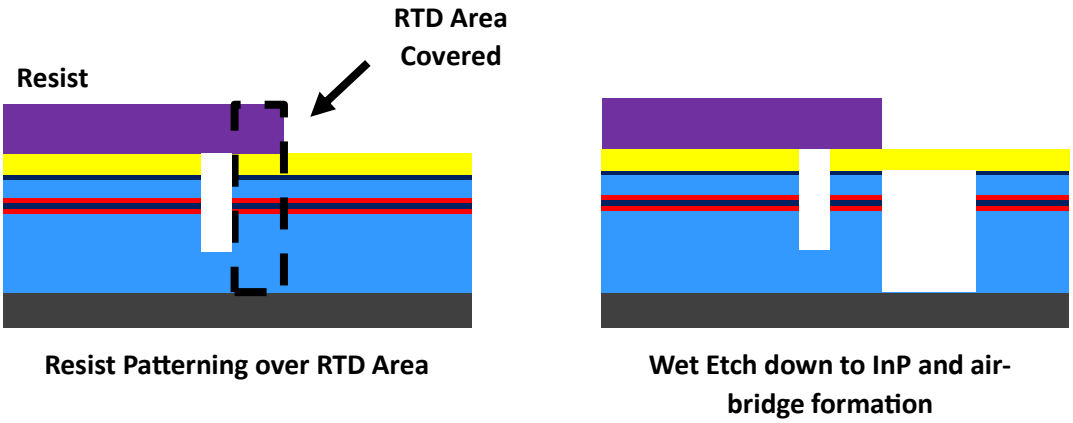

***Figure 2-14**: Deep Etch stage illustration of the device cross-section. Resist is deposited to cover and protect the end of the bridge area, and then the sample is etched down to the InP and under the metal to form an air-bridge structure.*

S1818 resist is used to cover the device area, with the same recipe as before (4000rpm, baked at 115°C for 2 minutes). It is exposed and developed for 8s and 40s respectively, the same times as before also, before a UV/O_3 clean. Images of the RTD devices with the resist coverage are shown in Figure 2-15.

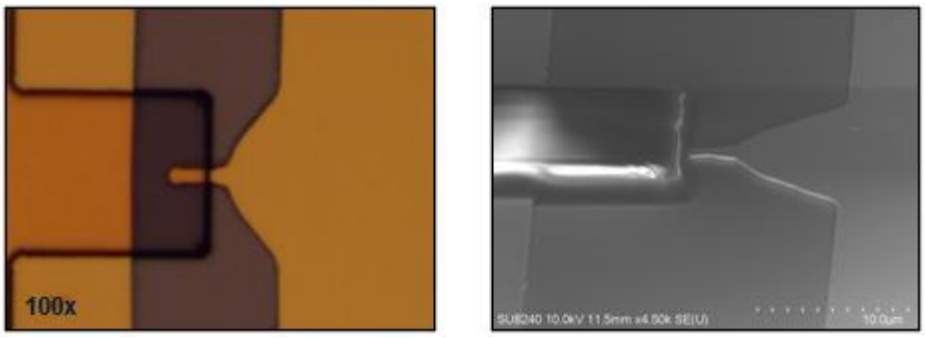

***Figure 2-15**: Optical microscope and SEM images of the RTD devices following the deposition of resist, prior to the deep etch stage.*

Then the wet etch is performed, etching a total depth of 700nm (around 5 minutes and 50 seconds at 120nm/minute) and the DektakXT is used to check when the right depth has been obtained. Following this, the sample is then I-V tested to check whether RTD characteristics are visible. If they are not, it is assumed the air-bridge has not been fully etched, and so a 30 second etch is performed. This process is repeated until RTD characteristics such as those shown in Section 2.6 are obtained. Once the etching is deemed sufficient, the resist is stripped in Microposit Remover 1165 at 50°C, and the sample is cleaned in acetone and IPA once more. Images of the etched sample before and after the resist is stripped are shown in Figure 2-16.

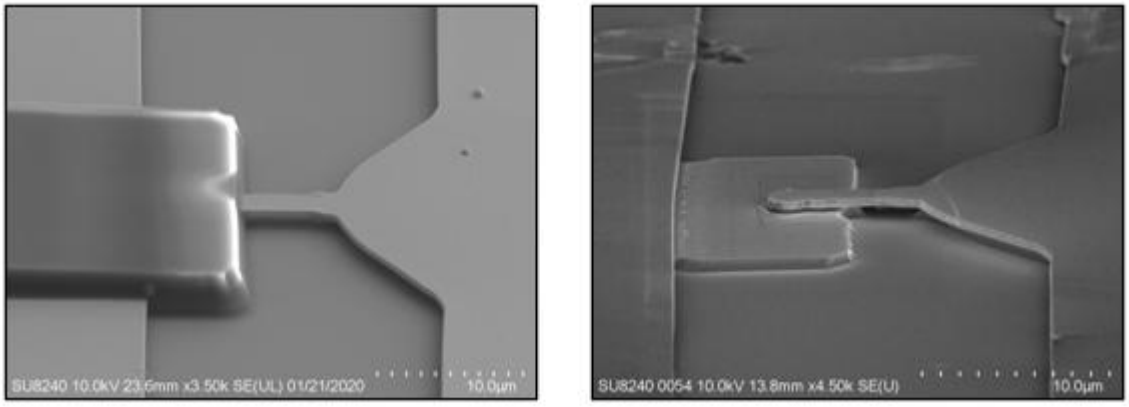

***Figure 2-16**: SEM Images of an RTD following the deep etch stage. On the left, the resist still covers the mesa area. On the right, the resist has been stripped.*

There were several issues faced, when establishing this fabrication process, and some adaptations were required before working devices could be fabricated. Firstly, when optimising the wet-etch process, some problems were encountered with the resist coverage of the device area. If too little of the bridge was covered in resist, the following etch step would etch away the device completely. Therefore, the alignment of the photoresist pattern was shifted to cover more of the bridge and ensure the device survived the wet etch. Figure 2-17 demonstrates one poor example of resist coverage and one good one.

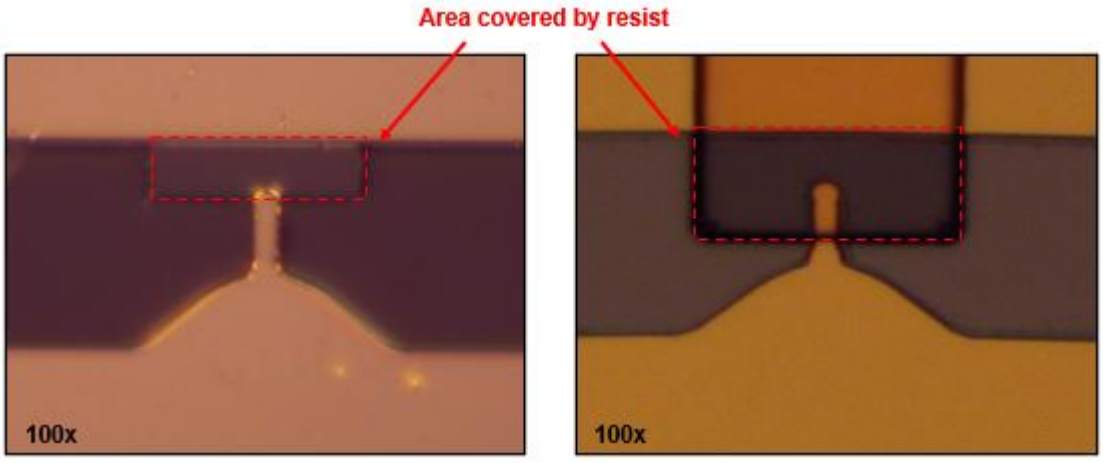

***Figure 2-17**: On the left, poor resist coverage is shown. The right-hand side shows a much better coverage of the bridge.*

On the left device in Figure 2-17, the length of the bridge covered by the resist was 0.9µm whereas 4.5µm was covered for the right-hand bridge. This led to the device on the left being etched away during the deep etch stage whereas the device on the right ended up as a working RTD. The results obtained from this device and one other are presented in Section 2.6.

Also, there were several challenges encountered with the two etching steps. The initial photolithography process has presented issues with the undercut of the LOR during development. From the data sheet [118], this undercut should not be any more than 1µm but in practice has been several µm, resulting in inaccurate features and poor lift-off. Removing the LOR layer was tried, though this made the lift-off more difficult with only an S1818 layer. This also amounted to unreliable metal depositions with flagging – metal sticking to resist sidewalls - occurring.

Another challenge came with the wet etching. The etching solution used (H_3PO_4:H_2O_2:H_2O 1:1:38) which previously gave consistent 100nm/minute etch rates, had dropped to etch rates of around 15nm/minute. To combat this, a higher concentration etch (1:1:8) was used, although this then led to issues with excessive under-etching of the RTD mesa as the etch rate was very inconsistent and difficult to control. It is believed this was caused by possible contamination or expiration issues with chemicals used in the etch solution. The extended closure of the cleanroom facility due to the COVID-19 pandemic could have led to improper storage of the chemicals which require refrigeration. Fixes to the RO water supply occurred, and new bottles of phosphoric acid and hydrogen peroxide were obtained, and this fixed this issue, returning the etch rates back to normal. In addition to this, under-etching of the RTD mesa still occurred, as shown in Figure 2-18.

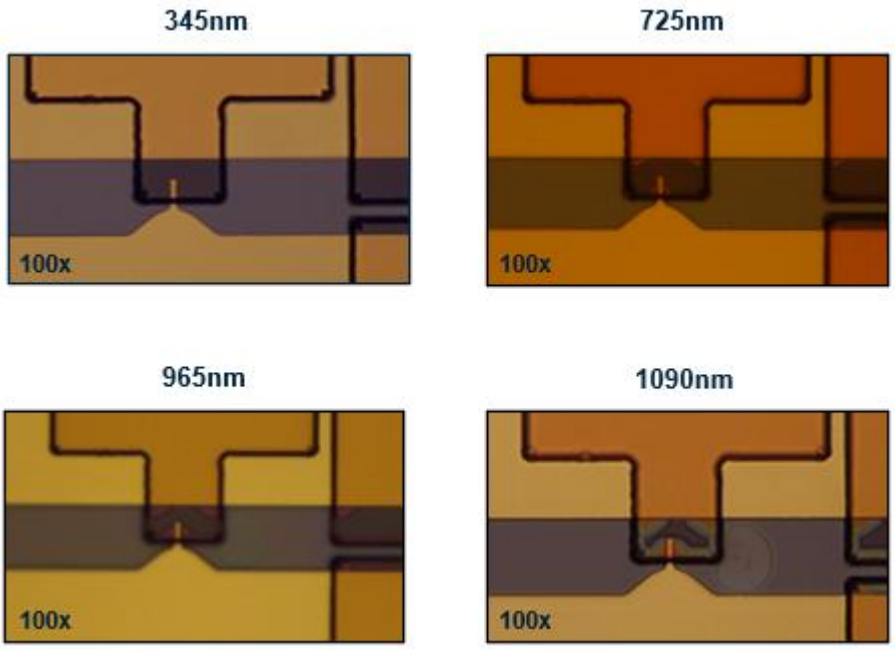

***Figure 2-18**: Optical microscope images showing the effects of underetching on the RTD mesa as the deep etch is performed.*

It was believed that this underetching occurred due to issues with the adhesion of the S1818 resist to the air-bridge structure. Different baking temperatures and times of the photoresist were investigated, although no improvement was found. Also, longer cleaning steps in acetone, IPA and the UVOCS tool were implemented prior to the resist deposition to ensure the surface was as clean as possible, in case any sort of contamination under the resist was causing an uneven profile. This underetching led to very inconsistent results across the area of one sample. Some devices were fabricated as expected, although most did not function as the RTD area was etched away. Future work on this process is required for a more reliable fabrication process. One possible idea to counter the underetching issue is to create a new mask photomask design with a larger area at the end of the air-bridge structure so that even if underetching occurs, it would not be possible to etch all the way through the RTD critical area.

2.6 Device Characterisation

As mentioned in Section 2.5, device testing can be performed during the fabrication process until the characteristic RTD I-V plot showing negative

differential resistance (NDR) is obtained. A 4-wire I-V measurement setup is used to provide accurate results as the measurement does not include the resistance of the wires, particularly important for devices with small resistances like RTDs. The testing is performed in 3rd quadrant operation (i.e. negative bias) as the V_{PK} and J_{PK} values are lower in this operation due to having a thicker spacer layer on the collector side. This reduces the chance of catastrophic self-heating and subsequent failure of the device. The following results have been obtained.

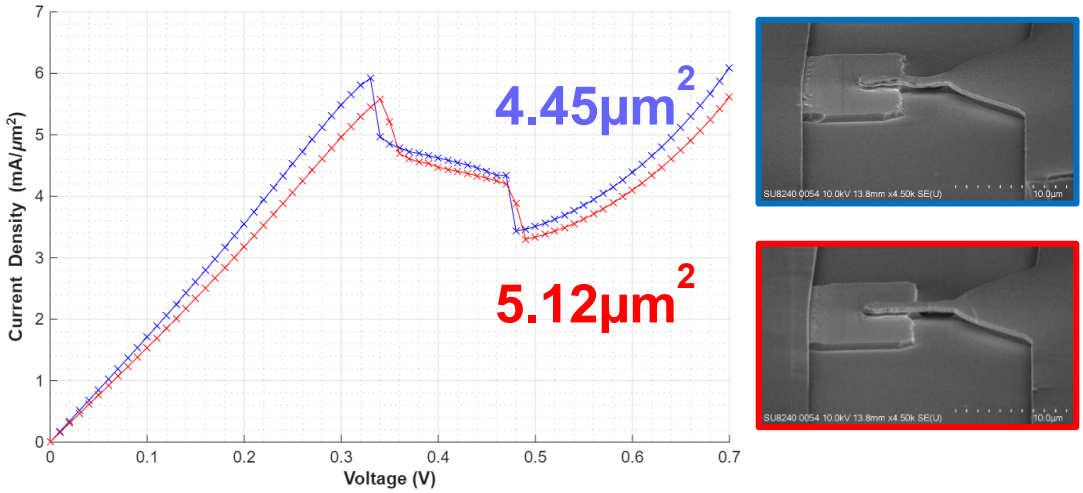

***Figure 2-19**: I-V Results of two RTD devices fabricated using the process in Section 2.5. An SEM image for each device is shown.*

In Figure 2-19, the I-V plots of two fabricated RTD devices are shown. The NDR region is apparent, lying between approximately 0.35V and 0.5V. The shape of this graph differs from the ideal graph shown in Figure 1-9, particularly in the NDR region. The peak and valley points are sharper than the curves shown previously due to the nature of the abrupt change in current caused by the conduction band misalignment. The NDR region is also not a continuous curve, due to the oscillating nature of the device in this region. Capacitive and inductive contributions combined with the NDR create an RLC circuit which, if the gain is greater than the loss of the slot antenna, results in oscillations and unstable regions are often visible in the I-V measurements [119]. Resistors are often connected in parallel to stabilise the device in this region. The measured areas of the devices were obtained from SEM images. The I_{PEAK} decreases with decreasing device area. This occurs as the tunnelling current through the RTD is proportional to the area. The area and the peak current values allow the peak current density, J_{PK}, to be calculated. For the red sample, J_{PK} = 5.58mA/μm^2, and J_{PK} = 5.92mA/μm^2

for the blue one. An equation for the maximum signal power an RTD can transmit has been derived in [88] to be:

$$P_{NDR} \approx {}^{3}/_{16} \times \Delta I \times \Delta V \quad (12)$$

where P_{NDR} is the power calculated from the NDR region; ΔI is the current range in the NDR region; and ΔV is the voltage range in the NDR region.

Therefore, the current and voltage spans in the NDR region should be maximised for maximum power output. The Peak-to-Valley Current Ratio (PVCR) is a useful measure of this span and is given by:

$$PVCR = {}^{I_{PEAK}}/_{I_{VALLEY}} \quad (13)$$

For both samples fabricated, this is found to be 1.7. This value is expected to be the same for these devices, as noted in [87]. Surface leakage currents, caused by possible dangling bonds or contamination on the surface, provide unwanted alternate paths for current to flow, and are expected to increase the I_{VALLEY} thus decreasing PVCR [120]. However, the surface leakage is too small for this structure. Ideally, both the PVCR and J_{PK} would be maximised, but as reported by Sugiyama *et al.* [121], a negative correlation appears to be the trend between these two parameters for devices with different structures. Therefore, finding ways to increase one parameter without decreasing the other is important for improving the output of RTDs in the future. The J_{PK} and PVCR characteristics of these devices also fit close to the trendline plotted in [121] so they are reasonable results.

Another key FoM is the IRE, defined by Baba *et al.* [86] as a measure of the conversion efficiency from electrical power to signal power.

$$IRE = {}^{P_{NDR}}\Big/_{P_{Chip}} \quad (14)$$

P_{NDR} is found as before, and P_{Chip} is the electrical power when biased at the mid-point of the NDR region. This bias point has been shown to be where peak THz emission occurs [47]. For the fabricated devices, IRE values of 3.5% (red) and 3.7%

(blue) were calculated. These values agree with those simulated in [86] [31] for a device with 1.1nm thick barriers, 4.5nm wide QW and $In_{0.8}Ga_{0.2}As$ as the material in the well, which fits the structure used here. An IRE value of 1.6% was calculated for a device fabricated with the initial dual-pass process by Jacobs *et al.* [87], over a factor of two smaller than the value found here. The PVCR was measured to be 1.5, also lower than the 1.7 obtained here. This highlights the improvements made in the device performance with this process, in addition to the reduced complexity and number of steps.

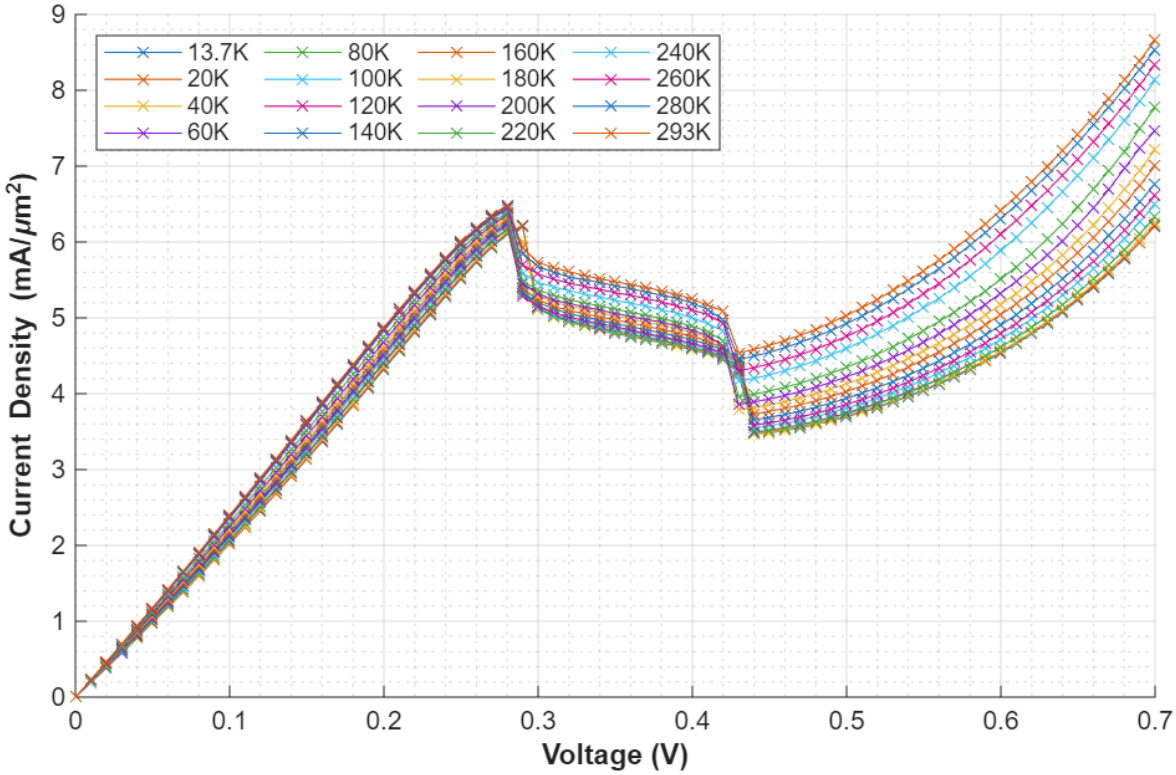

Figure 2-20: *Graph of J-V measurements taken from 13.7K up to room temperature (293K).*

Low temperature measurements were also taken to confirm the behaviour of the RTDs follows the expected trend as established by Jacobs *et al.* [44]. The RTD sample, with a device area of 5.12μm^2, was cleaved and wire bonded, before being placed in a cryostat where the temperature was reduced to a low of 13.7K. I-V measurements were taken in steps of 20K, with a temperature controller unit used to allow for accurate measurement of the temperature in the cryostat. After the measurements were taken, the data was overlaid in the graph shown in Figure 2-20.

The trend as the temperature increases is visible in Figure 2-21. As the temperature increases, the peak and valley currents both appear to rise. This is likely due to the increase in thermionic emission through the QW structure, as more electrons acquire the energy needed for this. It is noticeable that the valley current has a larger increase than the peak current values. This change is depicted in Figure 2-21. There is very little change in the voltage values, with only a marginal increase in V_{PK} and V_V at the lowest temperatures. This disagrees with the findings in [44], which featured a notable increase in V_{PK} and V_V. This was attributed to an increase in the series resistance of the external circuit.

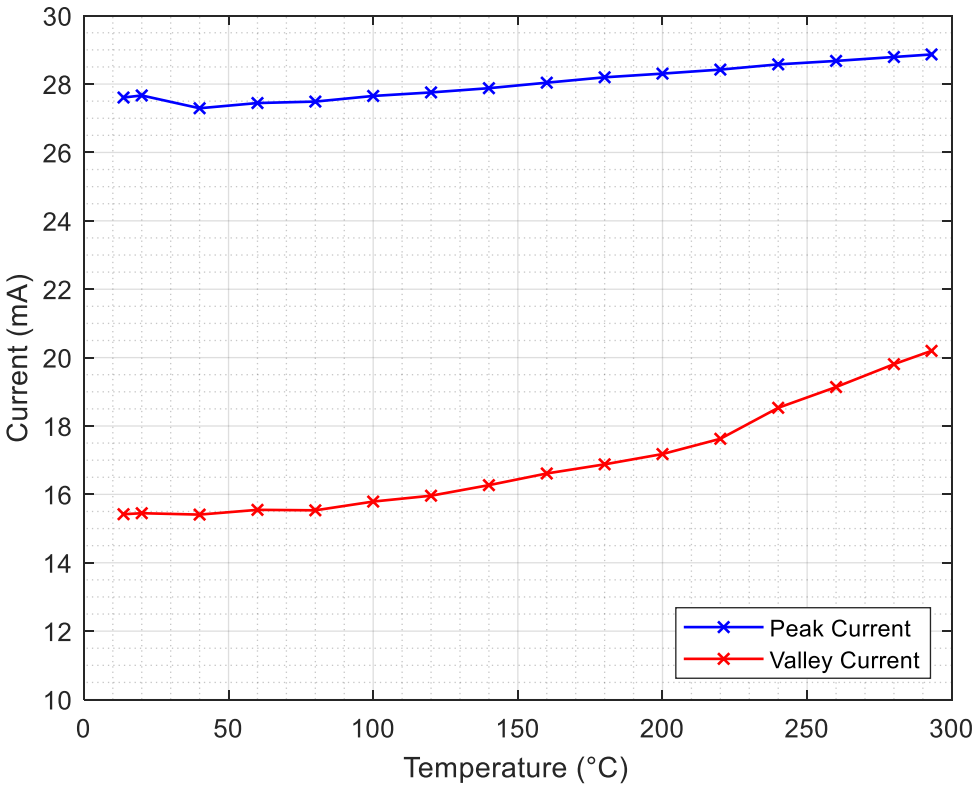

Figure 2-21: *Graph showing trends in I_P and I_V as the temperature increases.*

The valley current rises from 15.4mA to 20.2mA, a 31% increase, while the peak current increases from 27.6mA to 28.9mA, only a change of 5%. This translates to a change in PVCR from 1.79 at 13.7K, to 1.43 at room temperature (293K). If the peak and valley values are extrapolated linearly to higher temperatures, the NDR region would be expected to collapse at around 600K. This is a suitably high temperature for possible future packaging requirements. The effect of temperature on PVCR and IRE is shown in Figure 2-22. Similarly to the PVCR, there is a notable reduction in IRE from 4.4% to 2.8%.

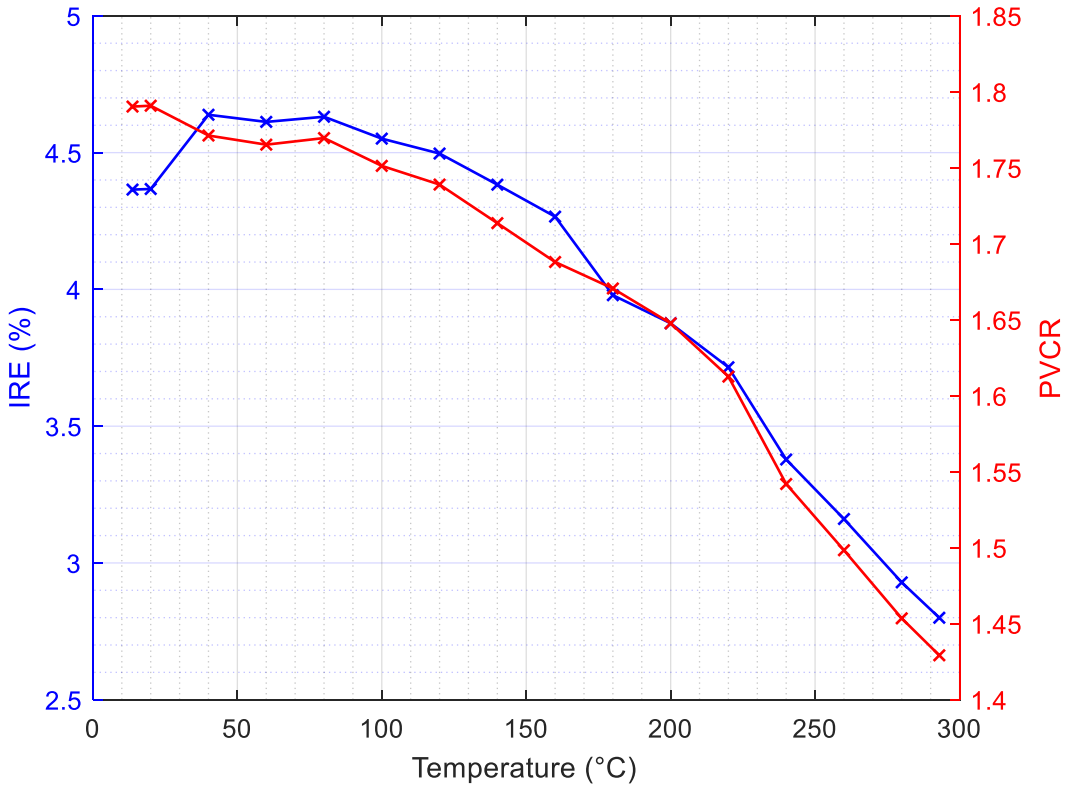

***Figure 2-22**: IRE (blue) and PVCR (red) plotted against temperature.*

As expected due to the temperature dependence of the valley current, both IRE and PVCR fall at higher temperatures. This agrees with the work done by Jacobs *et al.* [44] which stated a drop in PVCR from 1.8 to 1.4 from 20-300K. This closely matches the drop from 1,79 to 1.43 obtained here, as would be expected from devices with the same dual-pass structure, QW structure and similar device areas (5.12μm^2 here compared with ~8μm^2).

The trends in PVCR and IRE show that as the temperature increases, device performance worsens. For real-world applications, the temperature dependence of RTD devices requires further investigation. In addition to the temperature, several other parameters can affect the electrical characteristics, and therefore, the outputted signal, of RTD devices. In Chapter 3, these parameters are investigated based on results from the literature, and the trends in electrical characteristics are obtained and analysed.

2.7 Conclusions & Future Work

In this chapter, a simple, cost-effective process for fabricating RTD devices was established. The dual-pass process was chosen as an already established simplified process due to its single metallisation step, and the capability to control the device area closely. Optimisation of the contact resistance was done, with particular attention on the surface preparation, choice of contact metals, and the annealing step. Then each step of the fabrication process was described, further simplifying the existing process for dual-pass structures by breaking it down into three relatively simple steps. Devices were fabricated from this process and characterised electrically at room temperature and at temperatures down to 13.7K, demonstrating the quality of devices which were fabricated.

Some improvements can still be made to this process, and further work is required to fully optimise this. There are some issues with reliability as the yield of operational devices on a sample was quite low. This could be improved by using a different resist for the photolithography steps. This process uses LOR and an S1818 positive photoresist as it is very readily available, though the 1.5μm RTD air-bridges do not form consistently across the sample after the development step. A negative resist, as was used in [47], may provide the necessary lift-off undercut, and should be investigated. The other factor affecting the reliability is the air-bridge wet etch step. The underetching of the RTD mesa occurred despite attempts to optimise the resist mask, and full optimisation of this step is required. Different resists could be used, to investigate the resist adhesion to the surface of the device. Another possible solution is to try a different photomask for this step. The mask used results in bridge structures as shown in Figure 2-19. However, by increasing the device area at the end of the bridge, as shown in Figure 2-23, it is possible for this underetching to be overcome as the air-bridge would be etched through without eliminating the RTD column.

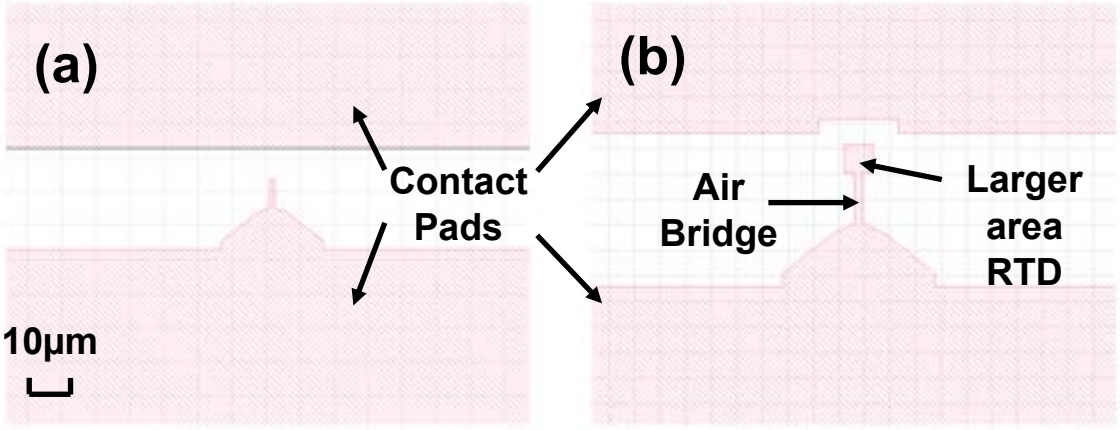

***Figure 2-23**: (a) Existing photomask design of RTD air-bridge, and (b) proposed design of RTD air-bridge to combat underetching difficulties.*

One of the main challenges facing RTD fabrication of high current density devices is the risk of failure due to overheating of the RTD column. In the process described here, I-V measurements are taken in 3rd quadrant operation as current density is lower in this direction due to the asymmetrical spacer layers on either side of the QW, as shown in Figure 2-6. However, adapting the fabrication process is another method which should be investigated to improve the thermal conductivity of the RTD device. Overgrowth of an Fe-doped InP layer, similar to that used in the substrate, onto the fabricated device is one method to aid with heat extraction. The current device relies on air to cool the device which has very poor thermal conductivity (0.03W/m.K), whereas InP has a much higher thermal conductivity (68W/m.K). This should allow higher current density RTD devices to be made, and with longer lifetimes. To evaluate the effect of this overgrowth layer, the temperature of the RTD under operation would need to be determined. A temperature map can be obtained by using scanning thermal microscopy (SThM) across the surface of the sample under operation. A full investigation into suitable deposition materials should be done to optimise the thermal conductivity. It is expected that improving the thermal conductivity of the device will decrease the effects of thermal components of the current density and voltage, thus improving the electrical characteristics, and by extension, the power and frequency outputs.

Another area for future work is to extend the fabrication process developed here to allow for THz frequencies to be extracted. MIM structures can be added to the slot antenna structure and when biased in the NDR region, a signal is output through the substrate. A hemispherical Si lens is required to focus the signal, like

in [87]. A Dielectric Resonator Antenna (DRA) is proposed as an alternate structure. DRAs have shown promise at millimetre wavelengths [122], as they do not suffer from conduction losses – increasing their radiation efficiency. The InP substrate can be used adapted into a rectangular DRA, if cleaved and thinned to the appropriate size for the frequency desired. The DRA structure removes the need for an Si lens, resulting in a more compact device and once correctly designed, should improve the radiation output from the device.

Chapter 3 : Critical Analysis of RTD I-V Characteristics

3.1 Motivation

In this chapter, a critical review of the RTD I-V Characteristics is done. This involves an analysis of the device characteristics in the literature, to find patterns and possible predictors of RTD performance. Being able to predict device performance more accurately would be very important for future production of RTD devices, as they could be engineered reliably depending on the application.

There are several figures of merit (FoMs) used to assess RTD device performance. Depending on the purpose of the device (high power, high frequency etc.), different FoMs are chosen as indicators, and can also be set as targets prior to the design and fabrication steps. The aim of the work done in this thesis is to optimise the RTD electrical characteristics with a view to maximising the power output. Therefore, an appropriate FoM, the IRE, is chosen as a measure of this.

In this chapter, a range of FoMs are listed and discussed, with a critical comparison of their suitability for assessing RTDs performed. This is done with a particular focus on the electrical characteristics, and the FoMs that relate to the power and frequency outputs of RTD devices. A prominent FoM used for RTDs is the peak-to-valley current ratio (PVCR), and this was first plotted against J_{PK} in Sugiyama *et al.* [121]. This work has been updated and analysed in this chapter, with an alternate plot of J_{PK} vs J_V proposed as a clearer representation of the current density relationship. This analysis is extended to the voltage relationship also.

A mathematical breakdown of the IRE into its constituent current density and voltage parameters is done for the first time, with analysis to determine the extent to which it can be optimised. Further analysis of the IRE is done, by considering the previously established relationships between the current density values and the voltage values. This allows a model to be made for estimation of the IRE values, and a comparison between these theoretical values and the ones calculated from the literature. The direct relationship between IRE and the peak and valley current densities was obtained, as well as the relationship with peak and valley voltages. An alternate method for predicting IRE was achieved through multiple regression analysis (MRA) which determines the effect each current and voltage parameter (and combinations of these parameters) has on the IRE value.

Finally, an investigation into the relationship between device parameters, and the electrical characteristics from the literature, is done. For barrier width, well width, In composition, and device area, the effect on current density and voltage values is analysed from the literature. From this critical literature analysis, the methods to optimise the IRE can be ascertained. This analysis demonstrates the difficulty in determining conclusive relationships due to the large variation of device parameters in the literature, and shows why a systematic study, as is performed in Chapter 4, is necessary for a fuller picture.

3.2 Electrical Characteristics Breakdown

In this section, the electrical characteristics (peak and valley values) of RTDs in the literature are studied, with the intention of identifying trends which can be used to engineer higher performance devices. This study encompasses a range of device designs, and so some variability in results is inevitable. However, all the data is taken from InP/InGaAs material structures to minimise this variability. Also, by observing and analysing outlying data, useful conclusions or topics of future research can be extracted. To measure these trends, the Pearson correlation coefficient, R, is found. This is a measure of the correlation between two variables and is calculated by:

$$R = \frac{n\Sigma xy - \Sigma x \Sigma y}{\sqrt{(n\Sigma x^2 - (\Sigma x)^2)(n\Sigma y^2 - (\Sigma y)^2)}} \times 100 \quad (15)$$

where R is the Pearson's coefficient, n is the number of data points, and x and y are the two variables. Values near 100% for R signify a near-perfect degree of correlation between the two variables. A high degree of correlation is indicated by an R value from 50-100%, a medium degree by an R between 30% and 49%, and a low degree by a value of 29% or lower. A value of 0% indicates no correlation at all. In addition to this, for variables with noticeable trends, a Theil-Sen fitted line (Appendix B) is applied to the graph. Theil-Sen regression is chosen as a more robust fitting method compared to least squares as outlying data points have less effect on the fitted line.

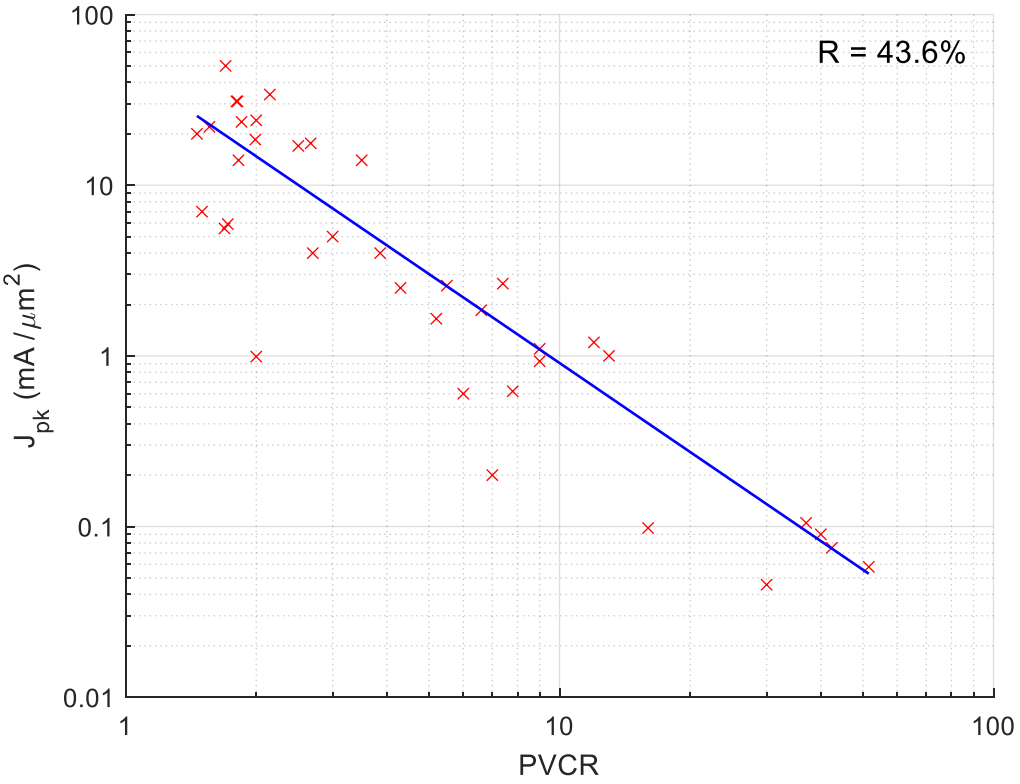

***Figure 3-1**: Graph of J_{PK} against PVCR, adapted from Sugiyama et al. [121], and Baba et al. [86]. All data points are taken from the literature [25] [27] [121] [87] [123]- [124] , and a Theil-Sen fitted line is overlaid in blue.*

In 2014, Sugiyama *et al.* [121] published a graph showing an inverse relationship between J_{PK} and PVCR, taken from data in the literature. There is a

large variation in device structures and fabrication processes represented in this dataset, and so general trends in RTD characteristics can be inferred. In Figure 3-1 this graph is recreated with additional data, from Baba *et al*. [86], and from more recent literature.

The inverse relationship is maintained between the two variables with the new data added, with a Pearson correlation coefficient, R, of 43.6%. This suggests a moderate degree of correlation. A high J_{pk} correlates to a higher power output, whereas a higher PVCR represents a higher quality of QW structure as the scattering effects and other contributors to the valley current are minimised. Therefore, there appears to exist a trade-off between the two, and further analysis is required to determine the extent to which these parameters can be optimised. As the degree of correlation is only moderate, this suggests some degree of engineering can be done to optimise both values. Ideally, values to the top right of Figure 3-1 are desired, and an analysis of device structural parameters is done later in this chapter to determine how this could be achieved. As the PVCR is a function of J_{pk}, some relationship between the two can be expected. A clearer trend is plotted in Figure 3-2. This shows the direct relationship between the peak and valley currents.

A very strong positive linear correlation can be seen, with R = 98.4%. This explains the trend seen in Figure 3-1, as a higher J_v corresponds to a lower PVCR by definition. To optimise these values, J_{pk} must be maximised, and J_v minimised. However, the strength of the correlation between these values suggests this would be a difficult task with limited results. Therefore, it is prudent to investigate the relationship between V_{pk} and V_v to assess whether they can be engineered separately. This is done in Figure 3-3.

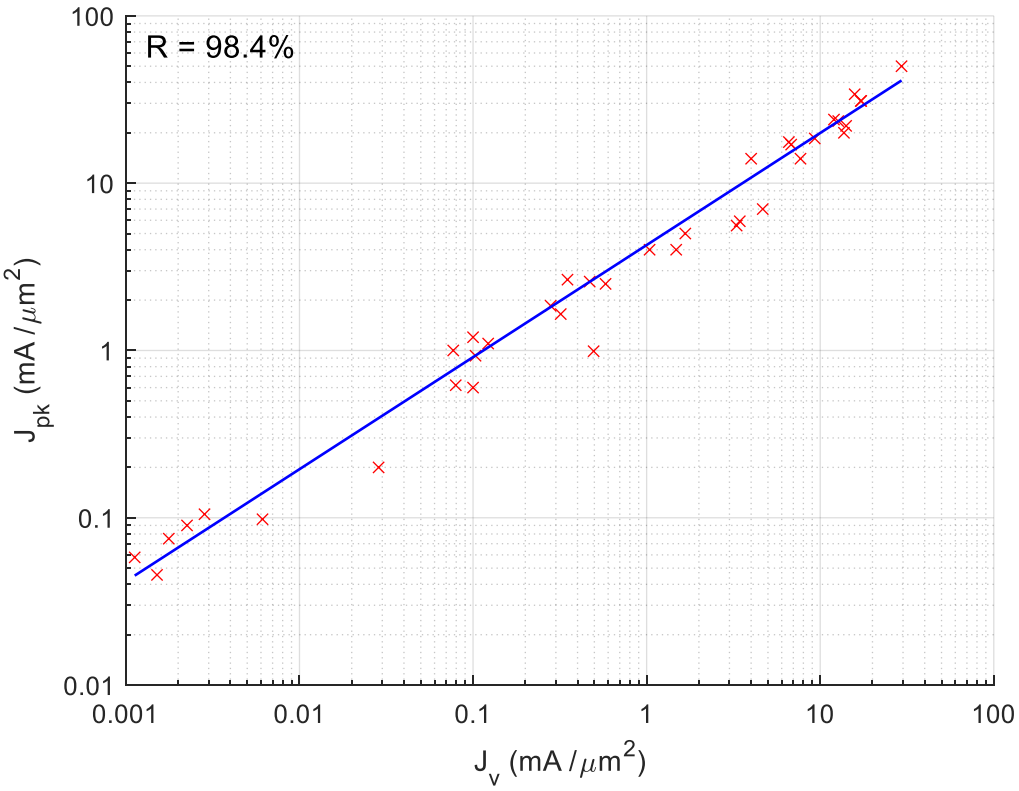

***Figure 3-2**: Peak vs valley current density values taken from the literature and plotted on logarithmic scales. The Theil-Sen line fit is shown in blue.*

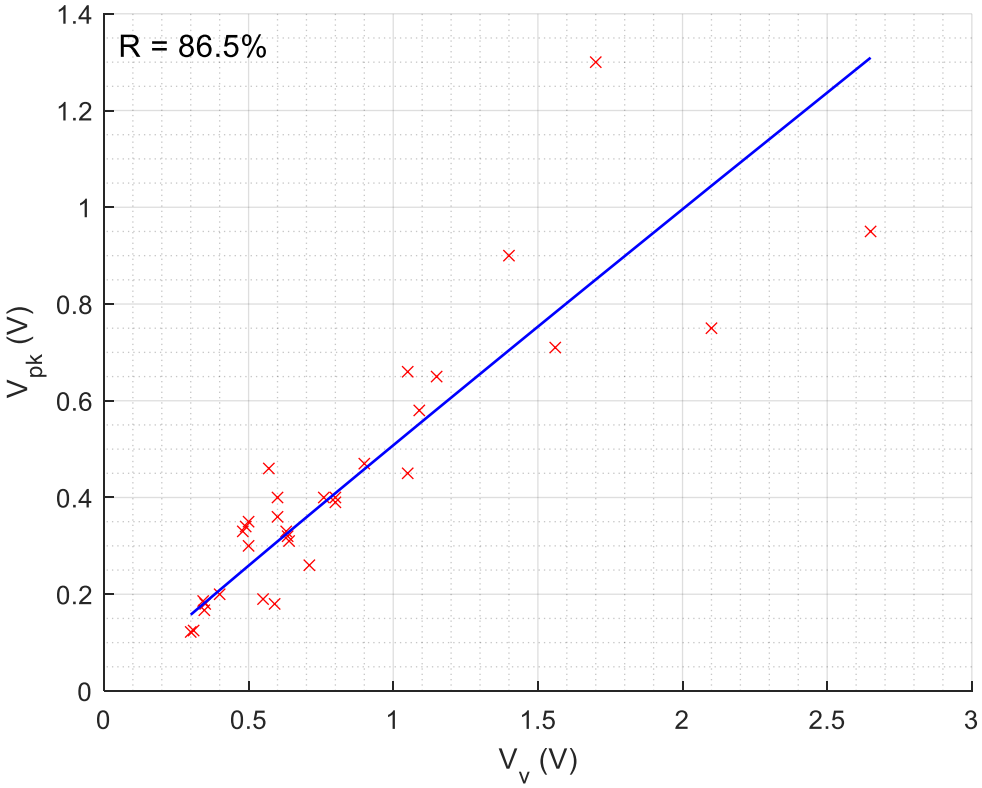

***Figure 3-3**: Peak vs valley voltage values taken from the literature. The Theil-Sen line fit is shown in blue.*

A positive correlation is also seen for V_{PK} vs V_V. A Pearson's coefficient of 86.5% is found, showing very strong correlation between the two, though not as strong as for J. Outliers are most noticeable at high V values, so further data is required to confirm the trend continues beyond ~1.2V. Similar to the case for current density, this suggests that parameters affecting V_{PK}, such as E_1 level and device resistance, have a similar effect on V_V. This makes maximising ΔV difficult, although the outliers at high V values suggest there is some optimisation that can be done.

From Figure 3-2 and Figure 3-3, the equations of the Theil-Sen fitted lines are determined to be:

$$\boldsymbol{J_{pk} = 1.8979 J_v + 0.4397} \quad (16)$$

$$\boldsymbol{V_{pk} = 0.5058 V_v + 0.0072} \quad (17)$$

These equations show the dependence the respective peak and valley values have on each other. They will be useful for the analysis of the IRE in the next section. It is important to note the errors inherent in using these equations for further analysis. Firstly, the rounding error which occurs by representing the slope and intercept of the lines to four decimal places. This results in a maximum error of 5×10^{-5} i.e. half of the lowest decimal place. The second, and larger, error, concerns how accurately the Theil-Sen line fits the data. As neither correlation is perfect (R=100%), there will be some inaccuracy in the analysis. The equation for voltage will have a higher error than that for the current density, due to its lower correlation coefficient value. Although strong correlations have been shown for the peak and valley values for both J and V, it is also worth investigating the J vs V dependence for completeness. This is shown in Figure 3-4.

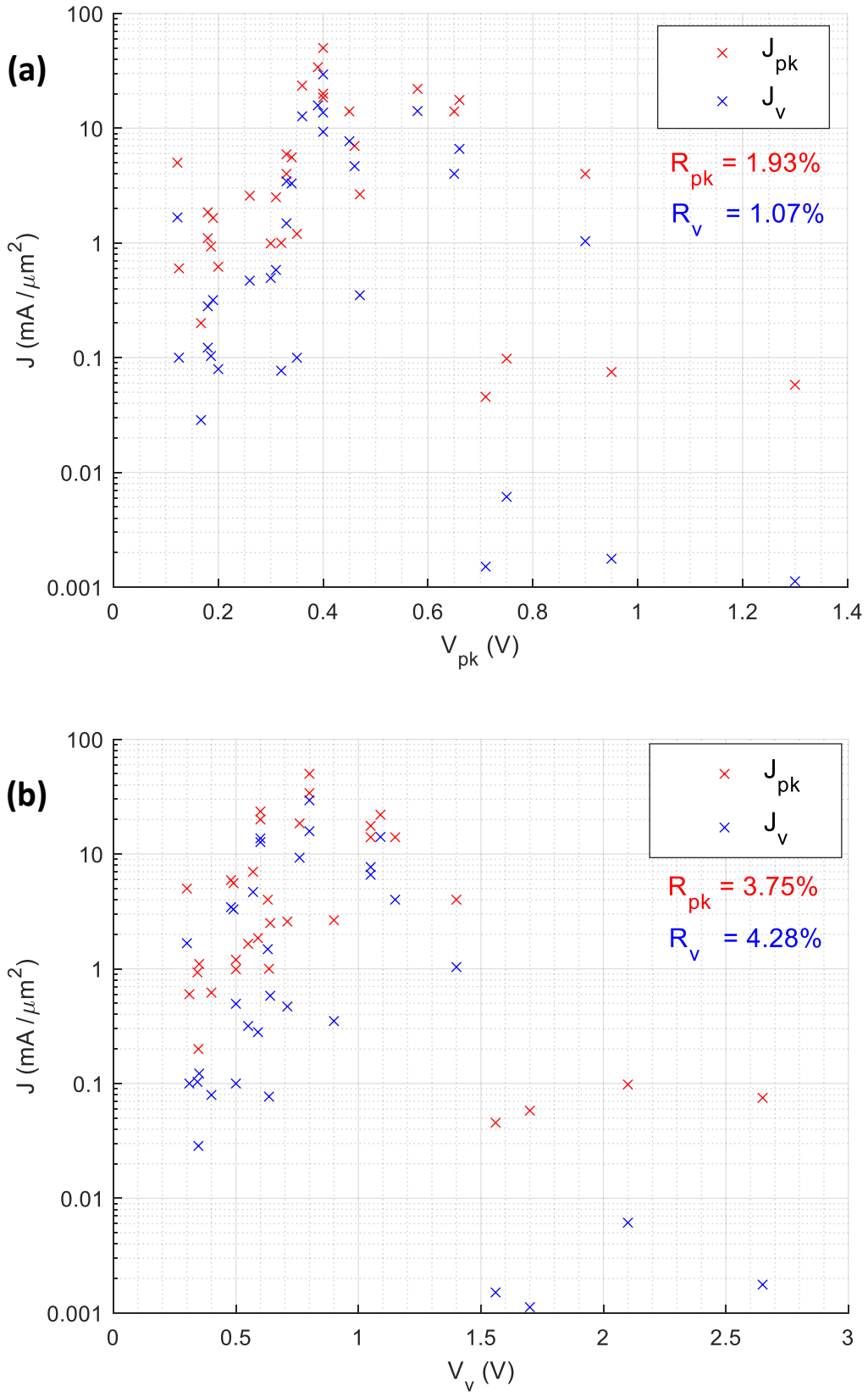

***Figure 3-4**: Graphs of peak and valley current density plotted against (a) V_{PK} and (b)V_v. J_{PK} values are shown in red, and J_v values are shown in blue.*

For all J vs V combinations, there are no clear correlations. Pearson's coefficients of 1.93% and 1.07% are obtained for J_{PK} and J_V respectively, against

V_{PK}. Against V_V, values of 3.75% and 4.28% for V_{PK} and V_V respectively, are obtained. The V_V values are marginally higher though still very low and so it can be assumed J & V are independent from each other. Another point to note from Figure 3-4 is the existence of four data points in the bottom right of each graph, with high V and low J values, relative to the rest of the data. These data points represent large-area RTD devices with thicker barrier and well widths. Although Theil-Sen regression views these data points as outliers and the Pearson coefficient does not indicate a trend, more data at higher voltages should be obtained to investigate whether there is a possible negative trend. Therefore, J & V can be engineered separately, though whether this is enough to have a significant influence on IRE requires further analysis.

3.3 Breakdown of IRE

The IRE is a relatively new FoM for RTD devices, first mentioned in Baba *et al*. [85]. It is intended as a measure of the electrical efficiency of the device, calculated as in Figure 2-2. From this definition, optimisation of the IRE would result in a direct improvement in device performance. IRE is particularly useful as it is solely a measure of the RTD and can be optimised prior to integration with other structures such as the antenna. Therefore, this section will look at the literature and assess the applicability of IRE to a wide range of RTD devices.

As introduced previously, the IRE is expressed as:

$$\boldsymbol{IRE = \frac{P_{NDR}}{P_{ELEC}} = \frac{{}^{3}/_{16} \times \Delta I \times \Delta V}{I_{BIAS} \times V_{BIAS}}} \quad (\mathbf{18})$$

Expressing the current and voltage values as peak and valley values and simplifying,

$$\boldsymbol{IRE = {}^{3}/_{16} \times \frac{(I_{PK} - I_V) \times (V_V - V_{PK})}{\left(\frac{I_{PK} + I_V}{2}\right) \times \left(\frac{V_V + V_{PK}}{2}\right)}}$$

$$= {}^{3}/_{4} \times \frac{(I_{PK} - I_V) \times (V_V - V_{PK})}{(I_{PK} + I_V) \times (V_V + V_{PK})} \quad (19)$$

I_{pk} and I_v here are interchangeable with J_{PK} and J_v, as the device area, A, would cancel out in this equation. Substituting the current densities in, and breaking the brackets gives:

$$IRE = {}^{3}/_{4} \times \frac{(V_V J_{PK} + V_{PK} J_V) - (V_V J_V + V_{PK} J_{PK})}{(V_V J_{PK} + V_{PK} J_V) + (V_V J_V + V_{PK} J_{PK})} \quad (20)$$

The left- and right-hand sides of this equation are visually represented in Figure 3-5.

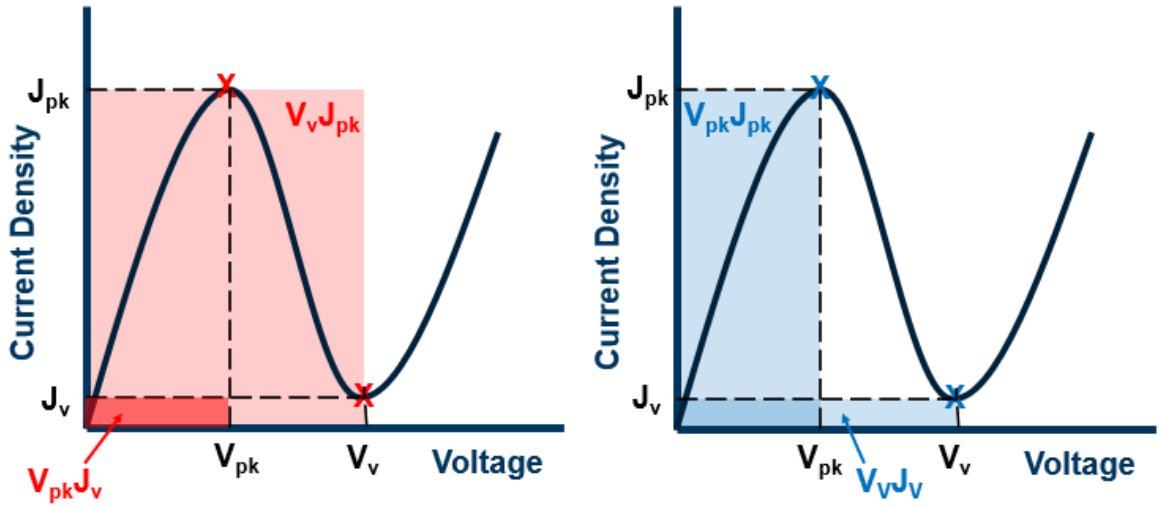

***Figure 3-5**: RTD I-V graphs with areas highlighted for IRE common terms in red, and difference terms in blue.*

To maximise IRE, the difference between the two graphs needs to be maximised. This difference is equivalent to the area of the NDR region so maximising ΔJ and ΔV is required. This translates to maximising J_{PK} and V_v, and minimising J_v and V_{PK}. However, the sum of both must be minimised also, which equates to reducing all the J and V values.

The ideal maximum case for the IRE can be determined from partial differentiation of the IRE equation. By differentiating with respect to each of the four variables, maximum or minimum IRE values can occur when any of the following twelve solutions occur:

$$\frac{\partial}{\partial V_V}: V_{PK} = 0,\ J_{PK} = J_V,\ J_{PK} = -J_V \qquad \frac{\partial}{\partial V_{PK}}: V_V = 0, J_V = J_{PK},\ J_V = -J_{PK}$$

$$\frac{\partial}{\partial J_V}: J_{PK} = 0,\ V_{PK} = V_V,\ V_{PK} = -V_V \qquad \frac{\partial}{\partial J_{PK}}: J_V = 0, V_V = V_{PK},\ V_V = -V_{PK}$$

For each variable, there are three solutions. However, four of these, represented in red, are invalid as negative values are not possible for these variables. Another four, in blue, are invalid as the NDR region disappears under these conditions. Finally, two of the solutions, in purple, are invalid, as they imply other peak and valley values are negative. Therefore, only two solutions are viable: V_{PK} = 0V, and J_V = 0mA/μm^2. When both conditions are true, the IRE equation simplifies to:

$$\boldsymbol{IRE = {}^{3}/_{4}\frac{V_V J_{PK}}{V_V J_{PK}} = 0.75\ or\ 75\%} \qquad \boldsymbol{(21)}$$

Therefore, 75% is the maximum possible value for IRE. However, partial differentiation is only applicable when all the variables are independent. As concluded in Section 3.3, the peak and valley values have a close correlation and show strong dependence on each other. Therefore, a more detailed analysis is required. To include this peak-valley dependence for both current and voltage, the equations of the Theil-Sen fitted lines from Figure 3-2 and Figure 3-3, are expressed in terms of J_V and V_{PK}, and inserted into the IRE equation:

$$\boldsymbol{IRE = {}^{3}/_{4} \times \frac{([1.8979J_V + 0.4397] - J_V)([1.614V_{PK} + 0.102] - V_{PK})}{([1.8979J_V + 0.4397] + J_V)([1.614V_{PK} + 0.102] + V_{PK})}}$$

$$\boldsymbol{= {}^{3}/_{4} \times \frac{(0.8979J_V + 0.4397)(0.614V_{PK} + 0.102)}{(2.8979J_V + 0.4397)(2.614V_{PK} + 0.102)}} \qquad \boldsymbol{(22)}$$

Plotting this equation then gives:

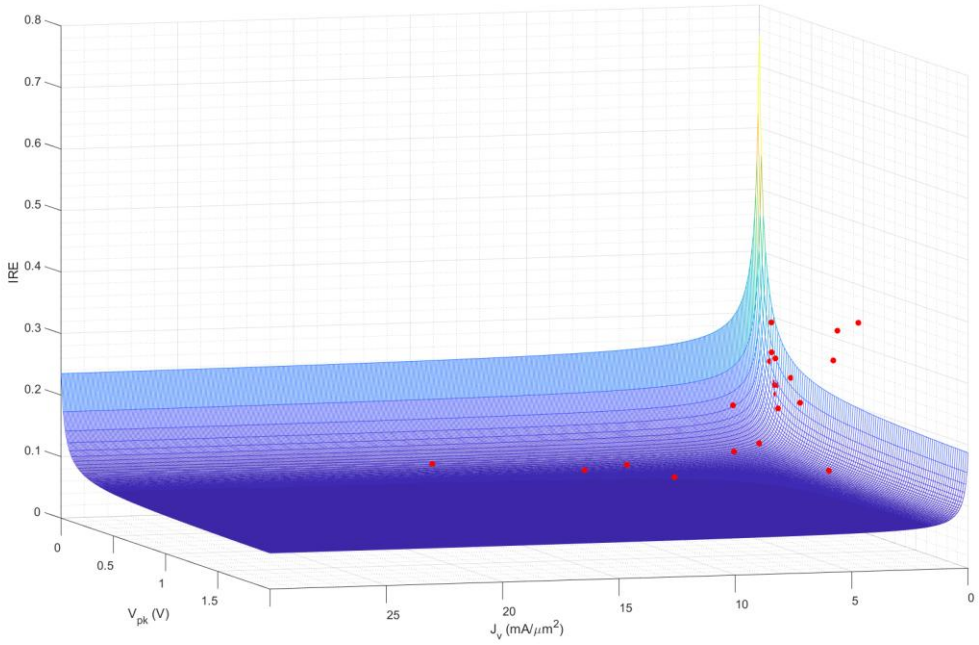

***Figure 3-6**: 3-D Plot of the IRE against J_V and V_{PK}. Data from the literature is plotted in red.*

As can be seen from Figure 3-6, the IRE peaks at 0.75 (75%) when J_V and V_{PK} are both zero and drops off quickly as these values increase. From the J_V and V_{PK} axes, there is very little change in IRE once values go beyond ~5mA/μm^2 and 0.5V respectively. The ranges for the x and y-axes are chosen to encompass the values from the literature, which are plotted to assess their agreement with the model. Most of the data points either lie below or beneath the expected IRE values. Small differences can be attributed to previously mentioned rounding and fitting errors. However, the most notable outliers are the three data points with a higher IRE value than expected. These correspond to the main outliers in the data in Figure 3-4, representing devices with high V and low J values due to their large area and thicker QW structure. More data points of similar structures should be included in the analysis to ascertain whether these high IRE values are replicable and to further tune the model used.

Therefore, to maximise IRE, the current and voltage values should be minimised as much as possible and with further analysis, Figure 3-6 will ideally allow for devices to be accurately engineered for specific IRE values. An important issue to discuss is whether it is feasible to attain current and voltage values low enough to improve IRE. In both J_V and V_{PK} cases, the maximum IRE is obtained

when the other variable is 0. Both scenarios are plotted in Figure 3-7 to investigate the extent to which the IRE value drops.

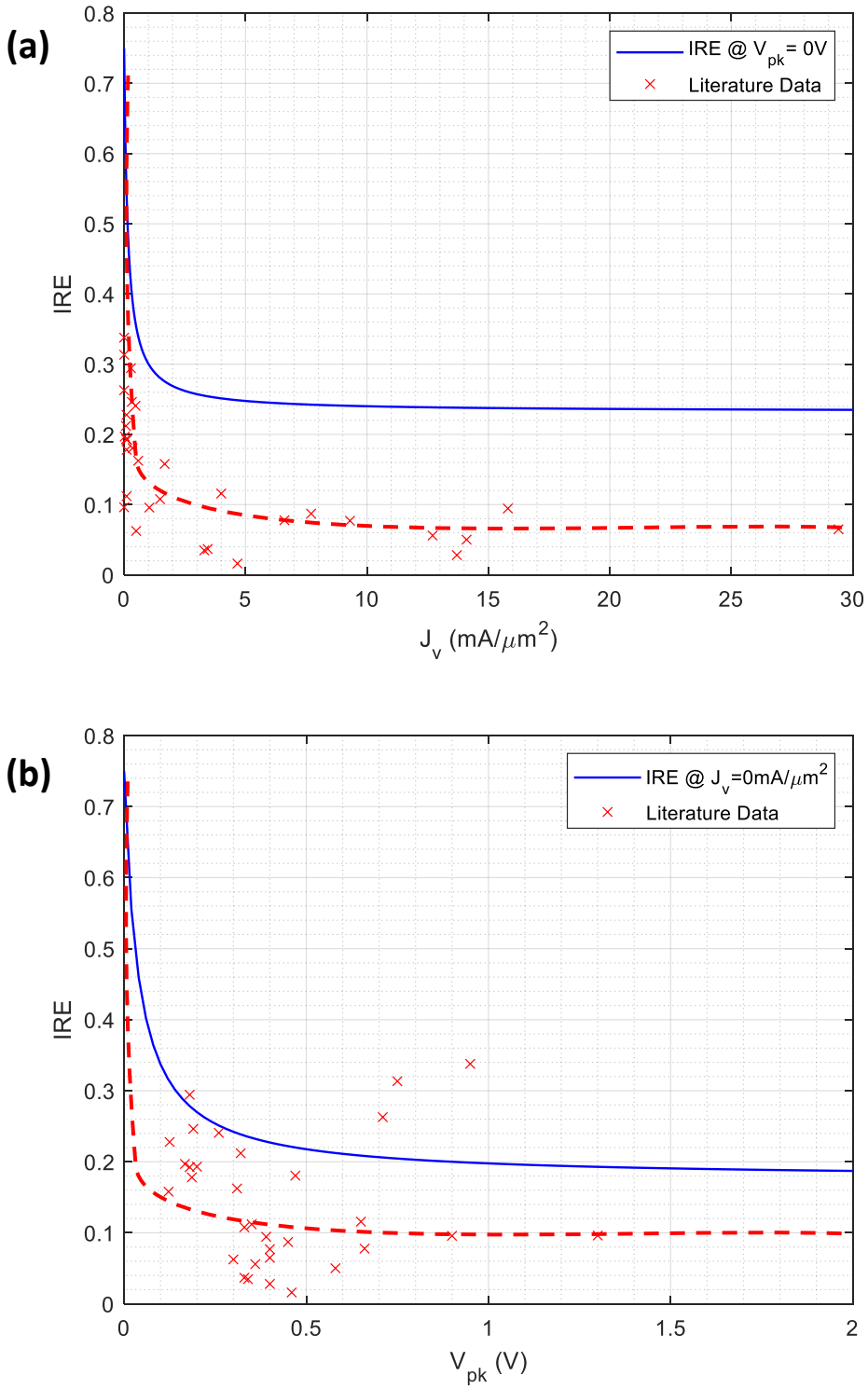

***Figure 3-7**: Individual plots of IRE against (a)J_V when V_{PK} = 0V, and (b)V_{PK} when J_V = 0mA/μm². This is taken from Figure 3-6. The blue lines represent the maximum calculated IRE values, and the dashed red lines are guides for the eye, fitted to the literature data.*

For Figure 3-7(a), all the data points lie below the 'maximum' IRE line, as expected. However, this is not true for Figure 3-7(b) as four data points lie above the line. These are the same outliers as discussed previously. The equations for the maximum IRE values plotted in Figure 3-7 are:

$$IRE_{J_V=0} = {}^{3}/_{4} \times \frac{0.614V_{PK} + 0.102}{2.614V_{PK} + 0.102} \quad (23)$$

$$IRE_{V_{pk}=0} = {}^{3}/_{4} \times \frac{0.8979J_V + 0.4397}{2.8979J_V + 0.4397} \quad (24)$$

The highest IRE value that can be obtained is 0.75 (75%). Calculating the horizontal asymptotes from these equations, it can be seen that for Figure 3-7(a), the IRE approaches 23.2% as J_V increases, and for Figure 3-7(b), it approaches 17.6% as V_{PK} increases. This suggests the current density will have a greater impact on IRE, and as such, minimising it should be a priority.

Another useful factor to consider is the gradient of the 'maximum IRE' slope. Visually, the graph when V_{PK}=0 exhibits a sharper decrease than the case when J_V=0. The 1/e values of the slopes are determined from the initial peak IRE (75%) and the respective lowest IRE values (17.6% and 23.2%) and results in values of 0.26mA/μm^2 in Figure 3-7(a) and at 0.068V in Figure 3-7(b). Examining the literature data, eleven data points lie below the J_V 1/e value, whereas in the V_{PK} case, there are no data points. This means it is more practical to engineer the current density values compared to the voltage, and this should be considered when designing future devices.

The literature data is expected to fall beneath the 'maximum IRE' curves. This holds true for most data points, although there are four outliers in Figure 3-7(b), which correspond with the four largest IRE values. It is important to note that as the IRE equation derived here is based on strong, but not 100% correlations, that there will be some inaccuracy in the calculation of maximum IRE. However, the shape of the graph is the important part for our analysis. The red dashed line shown on each graph is intended as a visual representation only, and further analysis of the relationships between IRE and the electrical characteristics is done in Section 3.5. However, this line follows a similar shape to the blue 'maximum' curve in both cases - although the outliers are ignored in Figure 3-7(b). In Figure

3-7(a), this dashed line lies at approximately a quarter of the IRE value of the blue line, and in Figure 3-7(b), it lies at roughly half the 'maximum IRE' value. This greater drop for the V_{PK} = 0V case implies it is more important to reduce J_V than V_{PK}.

The relationship between IRE and the J and V values requires further analysis. Determining the scale of the effect each of these variables has on the IRE will allow us to decide which variables to prioritise when designing our RTD devices. The IRE is presented against the peak and valley current values in Figure 3-8.

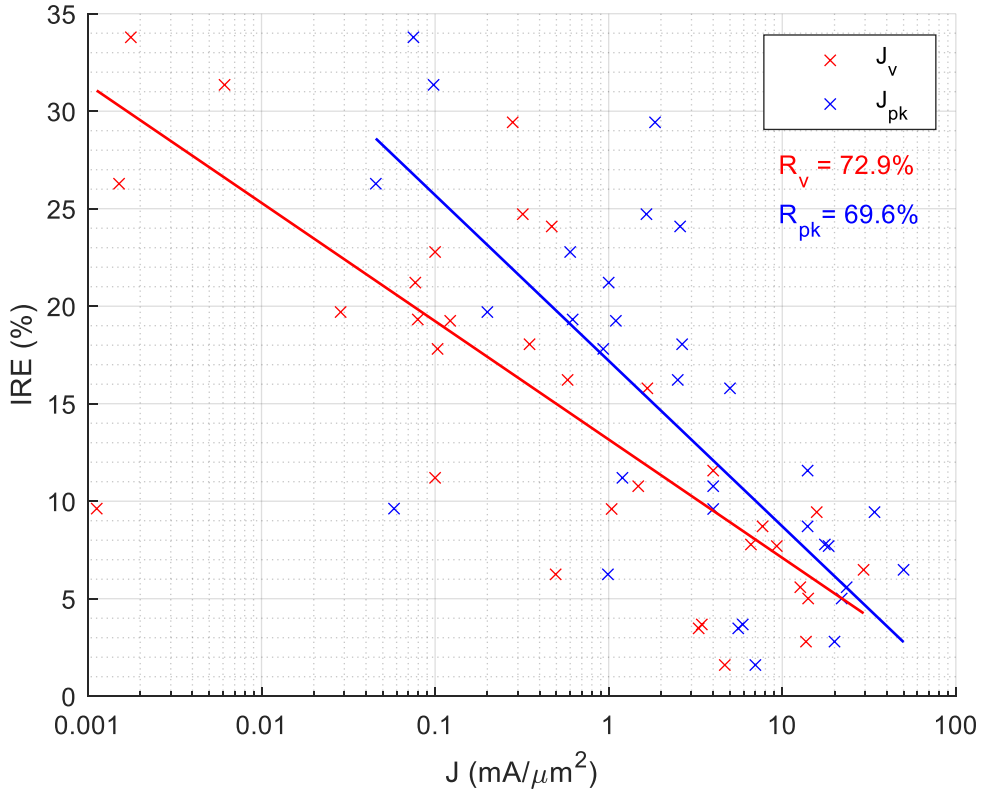

***Figure 3-8**: Plot of IRE against peak (blue) and valley (red) current densities. Theil-Sen fitted lines are plotted in the respective colours also.*

R values of 69.6% and 72.9% are obtained for the peak and valley values respectively, suggesting a moderate to strong degree of correlation. This is a negative exponential relationship with J. There is only a 3.3% difference in the correlation coefficient, as expected due to the strong correlation between J_{PK} and J_V. The fitted lines converge at higher J values, also agreeing with the J vs PVCR relationship. There is room for some optimisation, as evidenced by the spread of values around the fitted lines, and the non-perfect Pearson coefficient. The

relationship between IRE and the peak and valley voltages is also investigated in Figure 3-9.

There is a small positive correlation shown here between IRE and V_V, with an R of 33.4%. However, this correlation appears to be skewed by the three data points in the top right of this graph, and so more data points at similar V values are required to verify this. For the V_{PK}, the R value is only 3.4%, and so there is no clear correlation.

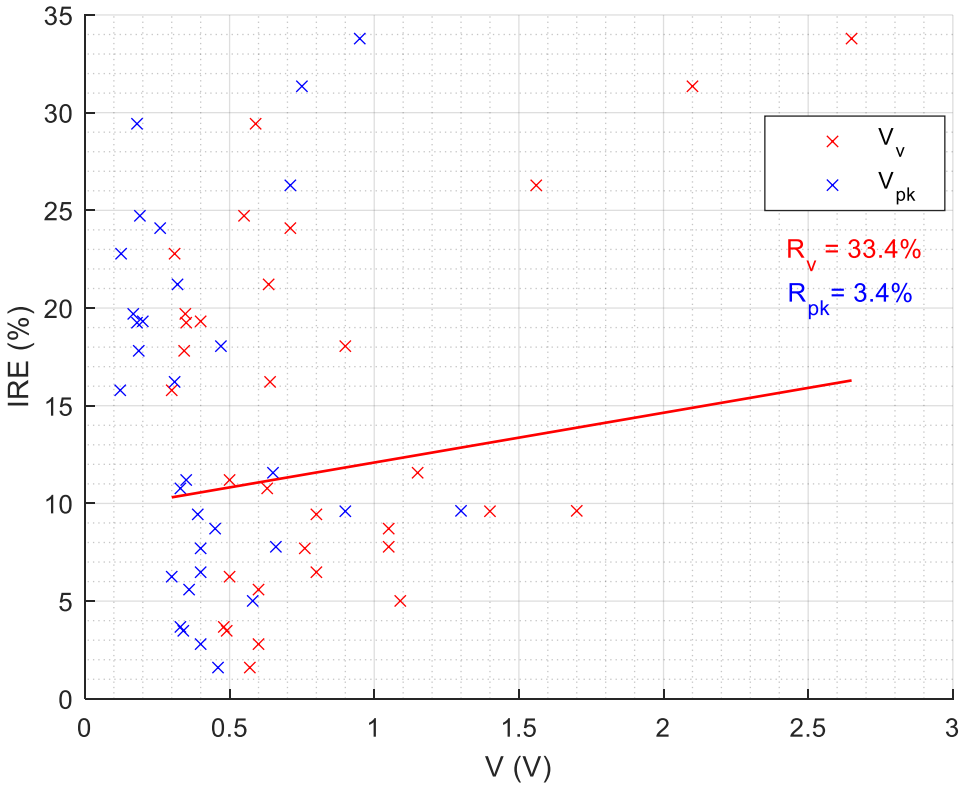

***Figure 3-9**: Plot of IRE against peak (blue) and valley (red) voltages. A Theil-Sen line is fitted for the valley values, as a minor correlation is found from the R value.*

Despite Figure 3-6 showing the peak in IRE values at low J_{PK} and V_{PK}, the real values tend to lie above the 1/e value, resulting in low IRE for all data points. This demonstrates the difficulty in engineering the IRE as it is dependent on multiple variables which conflict with each other. To determine which variables have greater impact on the IRE, MRA and measurement of the partial correlation coefficients (PCC) are done.

3.4 Multiple Regression Analysis

As shown in Figure 3-2 and Figure 3-3, the peak and valley values for both current and voltage exhibit a strong linear relationship. This presents difficulties in optimising the Δ values. The extent to which these values can be optimised is investigated by multiple regression analysis.

Multiple regression analysis (MRA) is a statistical method used to determine the relationship of a dependent variable to 2 or more independent variables. The coefficients calculated from MRA indicate the effect of each independent variable on the dependent variable, when the other independent variables are kept fixed. This builds on linear regression which observes one independent variable only. To look at multiple independent variables, more complex maths is required. The output of MRA is a series of coefficients, each corresponding to one of the independent variables, resulting in an equation of the form:

$$\boldsymbol{y_i = \beta_0 + \beta_1 x_{i1} + \beta_2 x_{i2} + \cdots + \beta_p x_{ip} + \epsilon} \qquad (25)$$

where y_i is the dependent variable; x_i are the independent variables; $ß_0$ is the y-intercept (a constant); $ß_p$ are the slope coefficients for each independent variable; and ϵ is the error term. The coefficients are found by the least-squares method. In this case, we want to ascertain how strongly the IRE depends on each of the current and voltage variables. MRA allows the IRE to be expressed as a linear equation like so:

$$\boldsymbol{IRE = 0.13 J_{PK} - 0.85 J_V - 40.17 V_{PK} + 22.31 V_V + 15.5925} \qquad (26)$$

This equation is used to estimate IRE in Figure 3-10. An R value of 86.4% is obtained, demonstrating a strong correlation between the IRE estimated by multiple regression and the real values. The positive value of the J_{PK} in the MRA equation indicates an increase in J_{PK} will result in an increase in IRE, when all other variables are controlled. Likewise, an increase in V_V would have the same impact, whereas for J_V and V_{PK}, increasing them would decrease the IRE. This agrees with the ideal case, where we want to minimise J_V and V_{PK}. There are noticeable outliers at both low, and high, IREs. Also, the predicted IRE for one of

these low IRE outliers has a value of -1.35% which is not possible to achieve in practice.

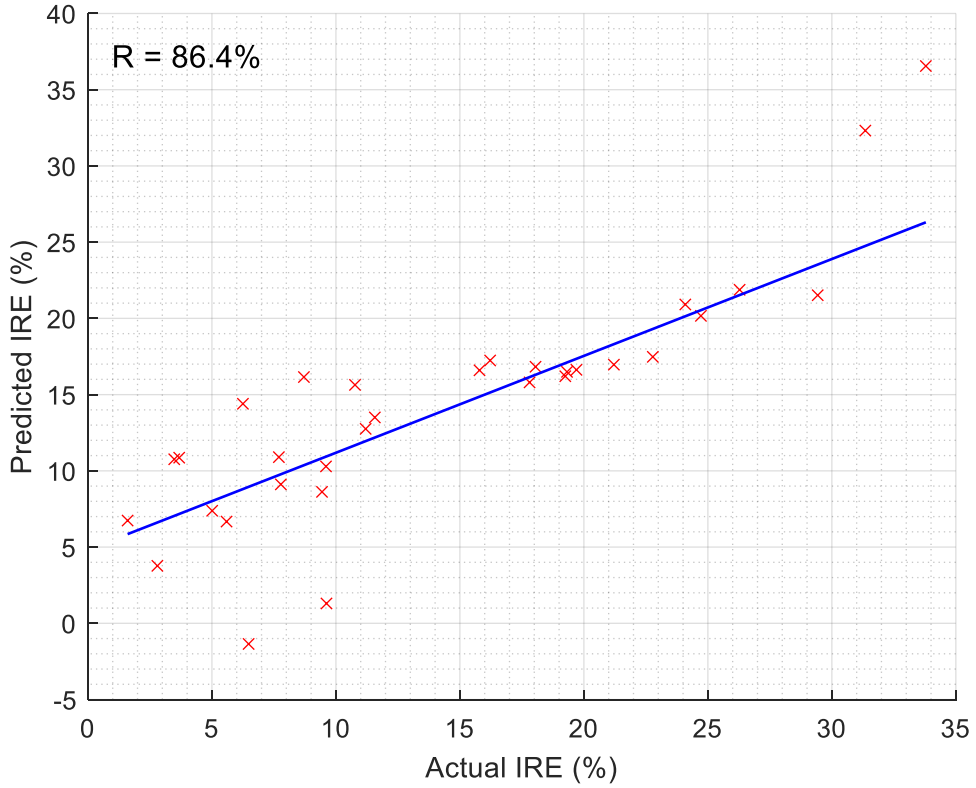

***Figure 3-10**: Plot of IRE calculated from the MRA equation, against the real IRE values of devices from the literature. A Theil-Sen fitted line is shown in blue.*

For a more accurate estimation, the interaction variables must be included also. These are all the linear combinations of J_{PK}, J_V, V_{PK}, and V_V, and represents the interdependence of the values of these variables on each other. The coefficients of this equation are represented in Table 3-1, and it is plotted in Figure 3-11.

***Table 3-1**: Coefficients of terms in the MRA equation when interaction variables are included.*

	J_{PK}	J_V	V_V	V_{PK}	$J_{PK}J_V$	$J_{PK}V_V$	$J_{PK}V_{PK}$	J_VV_V
IRE	5.01	-18.49	14.62	-33.65	0.22	5.08	-22.7	-0.76
	J_VV_{PK}	V_VV_{PK}	$J_{PK}J_VV_V$	$J_{PK}J_VV_{PK}$	$J_{PK}V_VV_{PK}$	$J_VV_VV_{PK}$	$J_{PK}J_VV_VV_{PK}$	**Error**
	44.74	4.35	-0.49	0.62	4.6	-11.81	-0.1	18.05

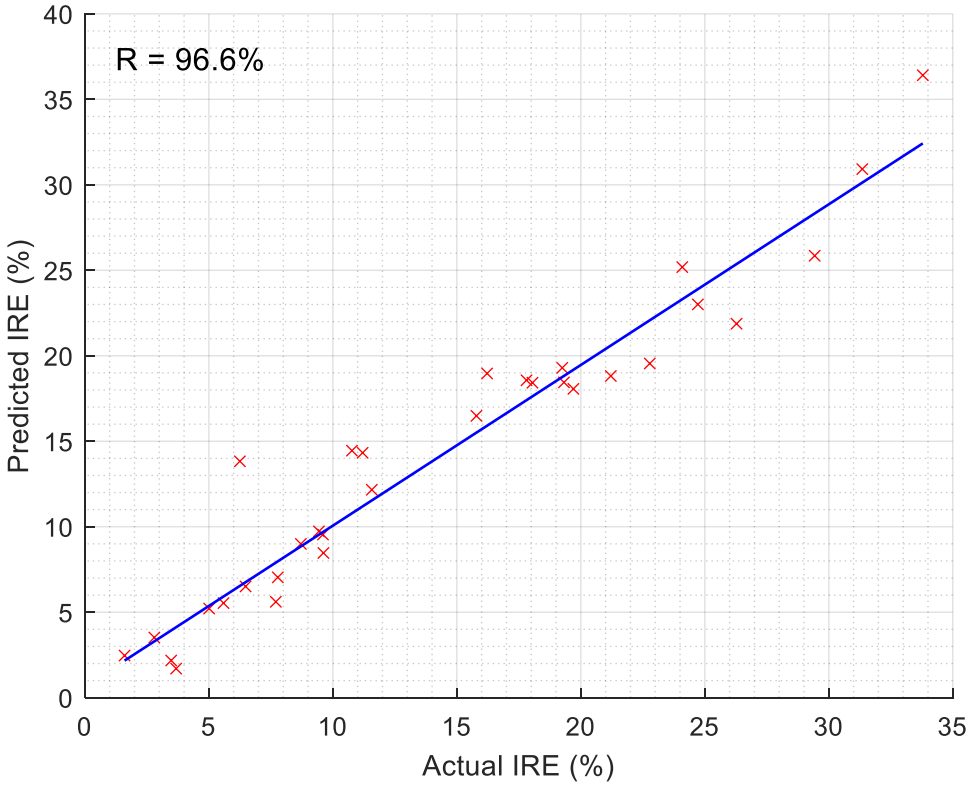

***Figure 3-11**: Plot of IRE calculated from the MRA equation with interaction variables included, against the real IRE values of devices from the literature. A Theil-Sen fitted line is shown in blue.*

This gives a more accurate fit compared to that of Figure 3-10, with an R value of 96.6% indicating a very strong correlation. The fit to the line is noticeably improved, and there are no longer any negative values calculated for the predicted IRE. Therefore, the coefficients in Table 3-1 provide a very close approximation to the real IRE values. However, it also becomes more difficult to interpret the effects of individual variables given the number of terms which now feature multiple, interacting variables. The signs of the original four variables stay the same, however the effects of combining these variables requires closer inspection. For example, although J_{PK} and J_V have opposing signs individually, $J_{PK}J_V$ has a positive value, indicating that increasing J_{PK} has a slightly greater impact on increasing the IRE, than increasing J_V has on decreasing the IRE. This also holds true in the V_VV_{PK} case. Larger effects are noticed with the $J_{PK}V_{PK}$ and J_VV_{PK} values. In particular, the term with the greatest impact on IRE is the J_VV_{PK} term, with a positive coefficient of 44.74. This appears to contradict what is known previously – that we want to minimise J_V and V_{PK}. However, by increasing J_VV_{PK}, other terms from Table 3-1 will have the opposite effect on IRE such as the individual J_V (-18.49) and V_{PK} (-33.65) terms, as well as the $J_{PK}V_{PK}$ term (-22.7), all of which have

large negative connotations for the IRE. The PCCs of the IRE for each individual term are shown in Table 3-2 along with the p-values.

***Table 3-2**: PCC values and p-values of the IRE against each of the peak and valley values.*

IRE vs …	*R^2 value*	*p-value*
J_{PK}	0.28	0.0018
J_V	0.29	0.0014
V_V	0.11	0.0619
V_{PK}	0.00	0.8524

The R^2 values for the current density terms indicate a weak correlation to the IRE. The p-values lie beneath 0.05 for both variables, so the correlation is statistically significant. However, in the case for the voltages, the V_V p-value lies just above 0.05, and is much higher for V_{PK}, suggesting these values are not significant and no correlation can be drawn between them and the IRE.

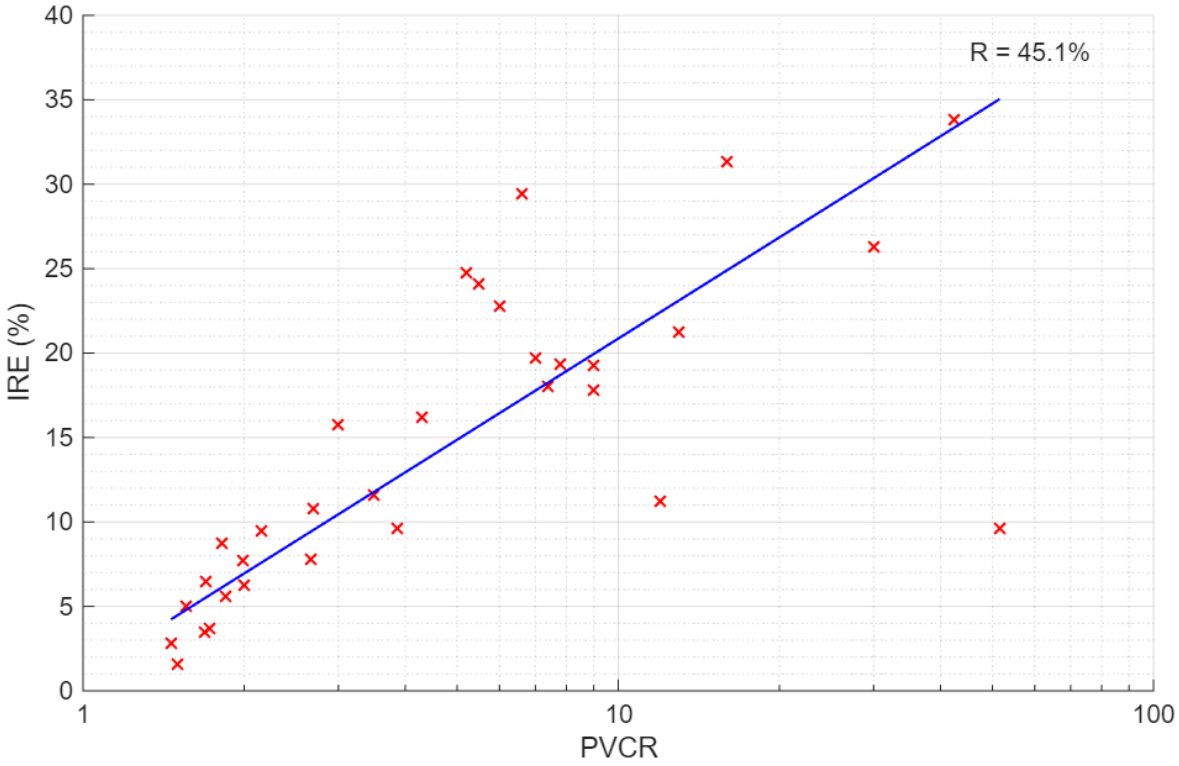

***Figure 3-12**: IRE against PVCR for devices in the literature. A Theil-Sen fitted line is shown in blue.*

The work done here tests the efficacy of the IRE to predict, and therefore, engineer the behaviour of RTD devices. As the PVCR has been used as a measure of the quality of an RTD device for many years, a comparison between the two is done in Figure 3-12. A moderate correlation is obtained between the two FoMs,

with a correlation coefficient of 45.1%. The accuracy of the fitted line is notably better at low values of IRE and PVCR, with high variation as these values increase. Since these data points represent a large range of different epitaxial structures, and device designs, a more systematic investigation is required to ascertain the exact nature of this relationship, particularly at high PVCR and IRE values. This is done in Chapter 4. However, before this, the effect of different epitaxial designs on the electrical characteristics requires close examination.

3.5 Review of Device Parameters

Although we've looked at how to analyse the IRE based on the current and voltage values taken from the I-V graph, it is also necessary to look at how these electrical values are obtained, and the parameters which influence them. In this section, we will investigate four different physical parameters which affect the device performance – barrier width, well width, In composition, and device area. By inspecting the relationships between these parameters and the I-V values obtained, it is hoped that RTD device performance can be predicted to some extent, and devices can be designed for specific FoM values. The relationships with J are shown in this chapter, and the relationships with V are included in Appendix C as the correlations are generally very weak.

Firstly, the barrier width is investigated. Figure 3-13 shows the relationship between the barrier width and the current. The relationship between barrier width and the voltage is shown in Appendix C-1.

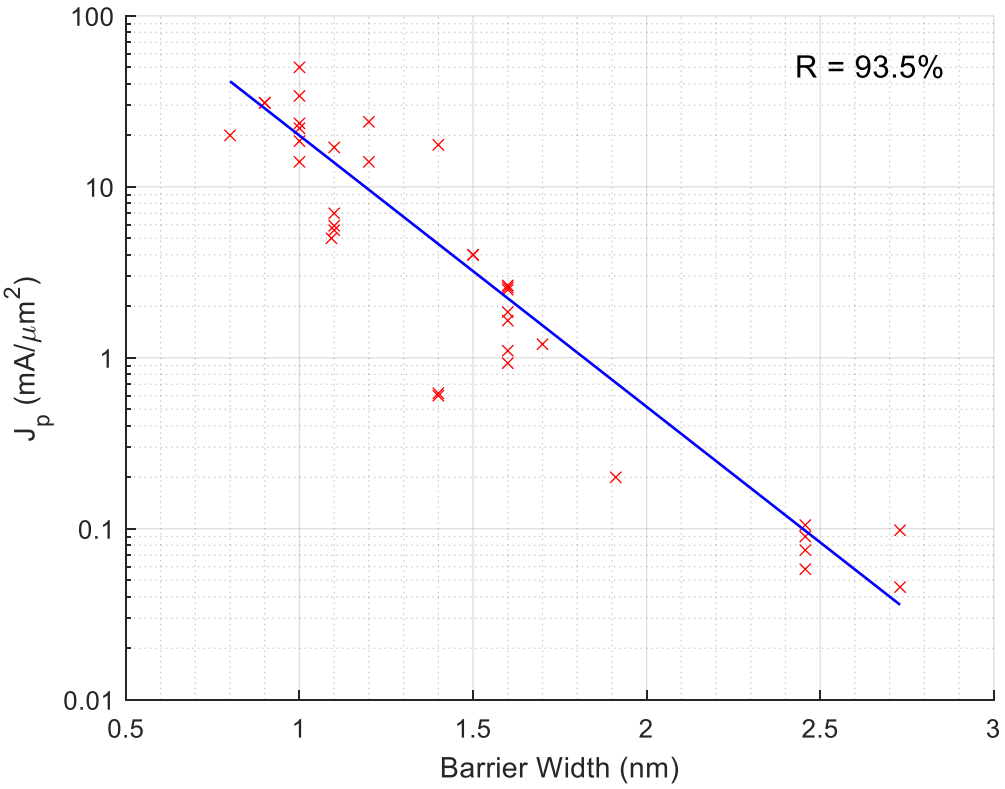

Figure 3-13: *Graph of J_{PK} against barrier width. Theil-Sen fitted line is shown in blue.*

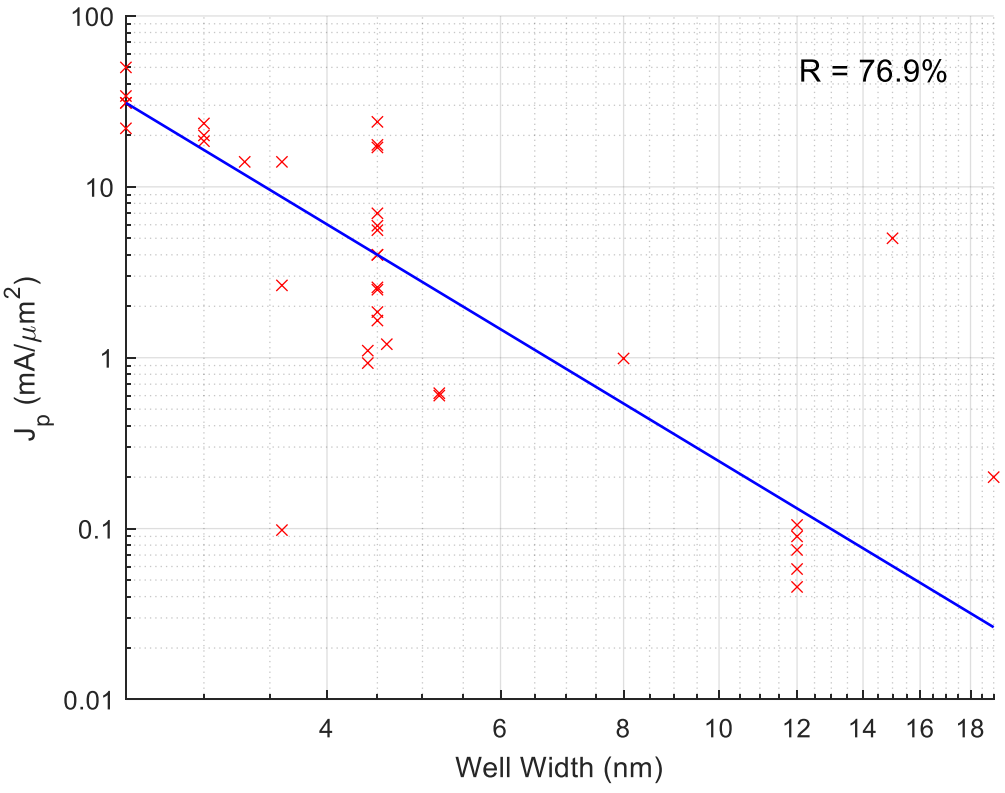

Figure 3-14*: Graphs of J_{PK} against well width. Theil-Sen fitted line is shown in blue.*

An exponential relationship is obtained from Figure 3-13, with a very strong correlation. This means decreasing the barrier width results in exponential increases in J_{PK}, and due to their relationship, J_V. The tunnelling probability is expected to increase at thinner barrier widths, and so more electrons should be able to travel through the QW structure. This trend therefore agrees with the physical expectation.

In Appendix C-1, a moderate degree of correlation is obtained in the V_{PK} case. The Theil-Sen fitted line appears to show a very weak gradient as it treats the higher V_{PK} values at higher barrier widths as outliers. With more data points at these values, this can be expected to change and the positive correlation as suggested by the Pearson's coefficient will become more noticeable. Another structural parameter to consider is the well width. This is plotted against J_{PK} in Figure 3-14.

A strong negative correlation is determined from Figure 3-14, suggesting the peak current density decreases as the well width increases. This agrees with the expected physical behaviour, as increasing the well width decreases the width of the quasi-bound energy level, thus allowing fewer electrons to tunnel through the QW structure.

In the case for V_{PK}, a very weak negative correlation is shown in Appendix C-2. This disagrees with the expected behaviour of a double barrier structure, as increasing the well width would be expected to lower E_1, and thus also lower V_{PK}. More data points are required at higher well width values for further analysis although it is also worth noting that at lower well widths, there is a high variance of V_{PK} values. The number of different device designs and structures could explain this, and a systematic review is required to obtain a more accurate analysis of this relationship.

In addition to the barrier and well widths of the QW structure, the Indium composition of the QW will also affect the device behaviour considerably. Therefore, a plot of J_{PK} against In composition is shown in Figure 3-15.

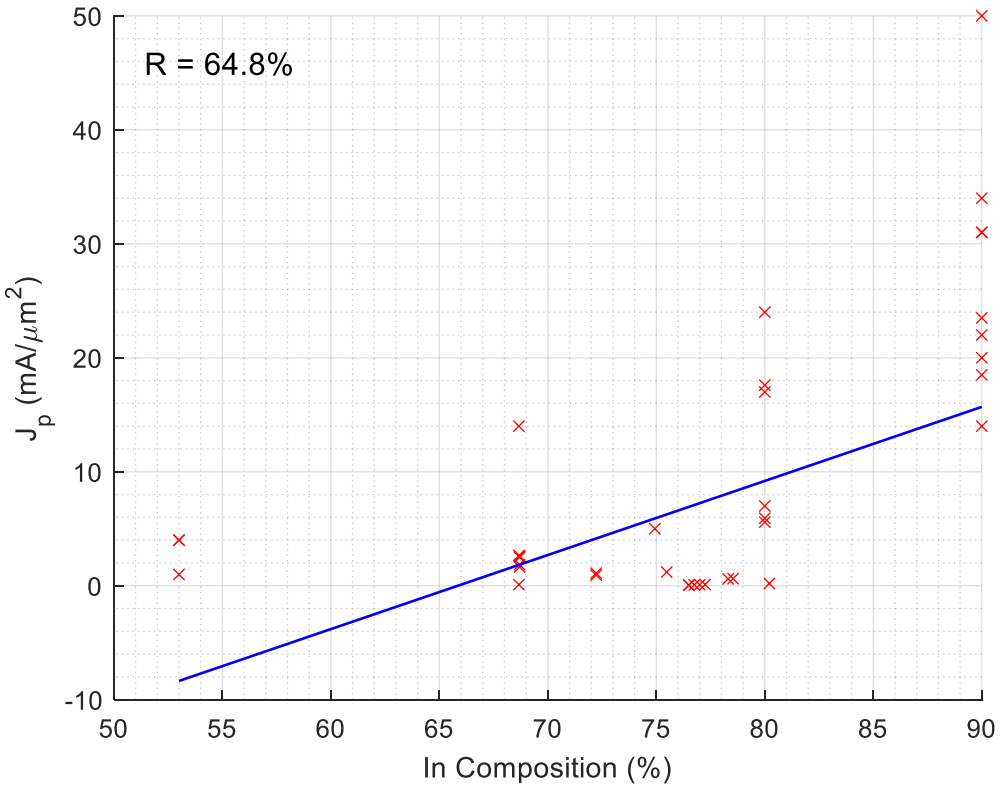

***Figure 3-15**: Graphs of J_{PK} against In composition. Theil-Sen fitted line is shown in blue.*

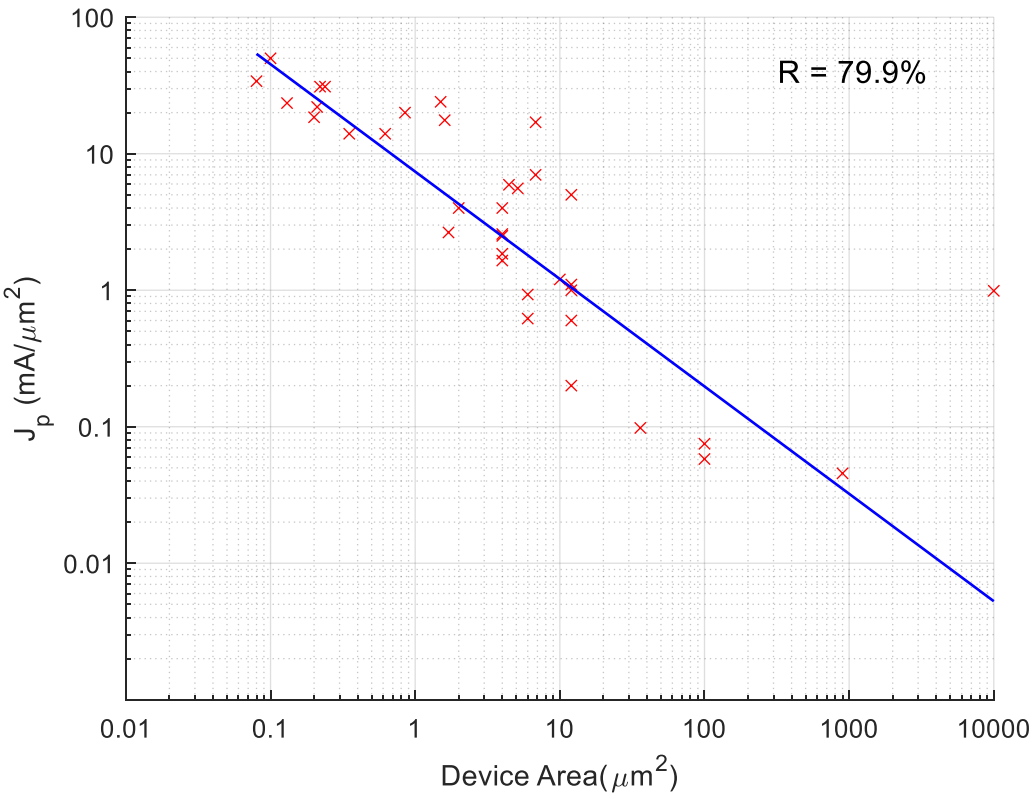

***Figure 3-16**: Graphs of J_{PK} against device area. A Theil-Sen fitted line is shown in blue.*

From Figure 3-15, a strong, positive, degree of correlation is found between IRE and J_{PK}. Increasing the In composition in the QW is expected to improve carrier confinement within the QW as the bandgap energy is decreased. This would be expected to increase the current through the device as the transmission coefficient would also increase. A more systematic approach would be expected to give a higher R-value and help clarify this relationship further.

In addition, there is no apparent trend between V_{PK} and the In composition (shown in Appendix C-3), despite an increase in In composition decreasing the bandgap of the material and reducing E_1. Once again, a reduction in V_{PK} would be expected but is not visible from the literature values studied. The approach in Chapter 4 aims to clarify the nature of these relationships by removing as many sources of variance as possible.

Another important parameter to investigate is the device area. As opposed to the other three parameters discussed, the device area is set during the fabrication process instead of during the epitaxial growth step. This allows for easier engineering of the device performance, and so its relationship with J_{PK} is also important to analyse. This is shown in Figure 3-16.

From Figure 3-16, as the device area increases, there is a noticeable decrease in J_{PK}. This is expected as the current spreads out over a larger area, thus decreasing the current density. Variation around the trendline can be explained by the effects of the other structural parameters.

There is a weak negative correlation between V_{PK} and device area, shown in Appendix C-4. This could be attributed to the electrical resistance, which is inversely proportional to the cross-sectional area. This would decrease at larger device areas, and thus a lower voltage would be required across the device. However, large variance exists again around the trendline, and a more systematic approach is required.

3.6 Conclusions & Future Work

Within this chapter, we have taken a subset of data from the literature, and performed analysis of key electrical parameters, to determine both the viability of the IRE as an FoM in a practical sense, and to demonstrate the necessity of a systematic approach to analysis if RTD devices are to be designed and fabricated reliably in the future.

Firstly, a summary of the RTD electrical FoMs was performed, with the intention to find some way of predicting, and therefore optimising, device performance before the antenna structure is fabricated. The IRE, introduced by Baba *et al.* [85], is chosen as the main FoM as it represents the power efficiency of the RTD based on the I-V characteristics alone. Optimisation of the IRE is desired as it represents an increased power output, at a lower bias. Following this, examination of the PVCR as a FoM was done, with a particular focus on work done by Sugiyama *et al.* [121], and Baba *et al.* [86]. Representing the PVCR vs J_{PK} trend as J_{PK} vs J_V shows a strong correlation which appears to limit the maximisation of the ΔJ value. Furthermore, by investigating the interdependence of the peak and valley electrical characteristics, the ΔV value also appears to be tough to maximise However, J and V values are shown to have no correlation.

Section 3.4 provides a more thorough investigation of the IRE, using data from the literature to examine trends and to analyse how much control of the IRE is possible. The ideal IRE (75%) is examined, and the largest practical values are predicted to occur when J and V values are low, with an exponential relationship found from analysis of the IRE equation. Four outlying data points with particularly thick QW structures are identified, but further analysis of similar structures is required. Multiple regression analysis is then performed in Section 3.5 to demonstrate the extent to which each variable affects the overall IRE value. The interactions between variables are found to complicate the analysis, and examination of literature trends of the IRE shows a negative correlation with J, and a weaker, positive correlation with V. The IRE is also shown to have a strong correlation with the PVCR. Finally, the relationship of the electrical characteristics with the structural parameters is investigated. The trends found here are analysed

with respect to the expected physical behaviour, with some discrepancies, particularly with the V_{PK} values, occurring. This can be put down to the range of device and epitaxial designs, fabrication processes, and variation in environments. This shows why a systematic approach is required to ascertain a more accurate analysis. This is the approach taken in Chapter 4.

In the future, this work can be extended with more data to further assess the veracity of the conclusions achieved here. The devices analysed here are all based on the InGaAs/AlAs material system, with some InAs sub-well devices also represented. Therefore, work should be done on other material systems, such as GaAs and GaN to assess the corresponding trends for each material, and for a critical comparison between them. This would allow for the optimal materials to be chosen for the appropriate RTD application. In addition, the assessment of the IRE should be carried through to the antenna construction also. An assessment of the correlation of IRE to real power and frequency outputs would establish whether its suitability as a FoM extends beyond just the electrical characteristics. A different FoM may be required for comparison of antenna structures which, when combined with the IRE, could give an overall device FoM.

Further verification of the conclusions reached here could be achieved if more systematic analyses of device structure are performed. The data obtained from these analyses will provide more clarity on the current density and voltage behaviour. By investigating these aspects thoroughly, a full systematic review into maximising the IRE can be performed. The device parameters predicted from this analysis can be tested in practice, and full optimisation of IRE can be achieved. Another source of data which would expand on the work done here is wafer characterisation techniques such as photoluminescence (PL) spectroscopy. By retrieving information on the device energy bands, the prediction of the effects of device structure can be verified, which would also contribute to the optimisation of the IRE.

Chapter 4 : Optimisation of RTD Epitaxial Structure

4.1 Motivation

In Chapter 3, it was posited that optimising the epitaxial structure will enable more efficient RTD devices. The concept of IRE was introduced as a measure of this efficiency. Within the literature, many different epitaxial structures and different device designs have been demonstrated, making comparison of the figures of merit very difficult due to the number of changing variables.

Previous work done has shown some relationship between device structure parameters and the electrical characteristics. Tsuchiya and Sakaki demonstrated the exponential relationship between barrier width and current density for the GaAs/AlAs/GaAs barrier material system [125]. This relationship is shown to be true for both the peak and valley currents. This work compares three different barrier widths and keeps all other structural parameters constant, enabling the authors to remove sources of error, and to obtain more reliable results. Other work has been done on the GaAs/AlAs/GaAs material system, with an investigation into the current dependence on well width also performed [126]. Three different well widths are compared, and near exponential relationships are found for both peak and valley current values against the well width.

In Moise *et al*. [127], a review of some parameters in the AlAs/InGaAs/InAs/InGaAs/AlAs material system is performed. This is one of the systems used in this thesis, with an InAs sub-well as part of the QW structure. The

exponential relationship between current and barrier width is confirmed, and asymmetry in the barrier width is investigated. The near exponential relationship between current and well width is demonstrated again also.

As evidenced by these examples, a systematic comparison is required for an accurate analysis of the electrical characteristics of RTD devices. Within this chapter, the number of variables is controlled by following the same fabrication method for all devices and fabricating the devices in parallel. This means errors arising from fabrication have been minimised, and so variance in some characteristics, such as contact resistance and device capacitance, will be minimised. Only the epitaxial structures differ, allowing for a fairer comparison to be done. Although some structural parameters have been systematically analysed in the literature, the work done here investigates several different parameters and uses the IRE, as well as previous simulation work done in [86], resulting in a more detailed analysis.

A summary of the experiments performed here is given in Section 4.2, including the baseline epitaxial structure, and the key differences between the structures investigated here. Four main experiments are done, comparing the well width, In composition, inclusion of a sub-well, and the sub-well position. The electrical characteristics in each case are compared and analysed with reference to the literature. Following this, the results are all analysed with respect to simulation work done by Baba *et al*. [86]. Devices were fabricated using the dual-pass process detailed in [87] and I-V measurements were obtained by Toshikazu Mukai at ROHM Co., Kyoto, Japan. The wafers were grown at the National Epitaxy Facility at the University of Sheffield.

4.2 Overview of Experiments

Four experiments have been done here on both ternary and sub-well QW structures. The first experiment compares well width and In composition for ternary QW structures, focusing on the competing effects changes to both parameters will have on the device I-Vs. Secondly, the same comparison is done

for sub-well QW structures. Following this, a direct comparison of ternary and sub-well QW devices is done at both 3.52nm and 4.5nm well widths. Finally, the position of the sub-well within the QW is investigated, comparing a central sub-well to one aligned with the emitter barrier. The base structure of the five wafers used in this investigation is detailed in Figure 4-1.

Thickness	Material	Doping (cm^{-3})
8nm	$In_{0.8}Ga_{0.2}As$	$2x10^{19}$:Si
20nm	$In_{0.53}Ga_{0.47}As$	$2x10^{19}$:Si
25nm	$In_{0.53}Ga_{0.47}As$	$3x10^{18}$:Si
20nm	$In_{0.53}Ga_{0.47}As$	Undoped
1.1nm	AlAs	Undoped
4.5nm	$In_{0.8}Ga_{0.2}As$	Undoped
1.1nm	AlAs	Undoped
2nm	$In_{0.53}Ga_{0.47}As$	Undoped
20nm	$In_{0.53}Ga_{0.47}As$	$3x10^{18}$:Si
400nm	$In_{0.53}Ga_{0.47}As$	$2x10^{19}$:Si
100nm	$In_{0.53}Ga_{0.47}As$	Undoped
1.1nm	AlAs	Undoped
4.5nm	$In_{0.8}Ga_{0.2}As$	Undoped
1.1nm	AlAs	Undoped
100nm	$In_{0.53}Ga_{0.47}As$	Undoped
200nm	$In_{0.52}Al_{0.48}As$	Undoped
200nm	InP	Undoped
InP substrate		

QW under investigation (See **Table** 4-1)

***Figure 4-1**: Example of the epitaxial structure of the RTD devices analysed in this section. This is the structure of Wafer 1 from Table 4-1, with a 4.5nm ternary QW. Two double barrier QW structures are grown on top of an InP substrate - the bottom QW is intended for wafer characterisation while the top is for device fabrication.*

***Table 4-1**: Overview of the epitaxial structures investigated in this work. For the well structures, T represents the Ternary ($In_{0.53}Ga_{0.47}As$) and I stands for InAs*

Wafer No.	*Well Structure*	*Barrier Width (nm)*	*Well Width (nm)*	*In comp.[avg.] (%)*
1	T	1.1	4.5	80
2	T	1.1	3.52	85
3	IT	1.1	1.17/2.34	100/53 [68.7]
4	TIT	1.1	1.37/1.76/1.37	53/100/53 [71.8]
5	TIT	1.1	1.17/1.17/1.17	53/100/53 [68.7]

Table 4-1 shows how the three main QW epitaxial parameters vary for the five wafers fabricated in this section. Barrier width is kept constant at 1.1nm, and all the devices fabricated had an RTD area of 1.2μm^2. However, the well structure, well width, and In composition, all vary. Therefore, the effects of these three variables on the device performance can be investigated in a systematic manner, eliminating the variance associated with the literature analysis.

The TIT samples include an InAs sub-well between two standard ternary InGaAs layers within the QW. The principal reason behind using the sub-well structure is to aid with the growth of the structure. Lattice-matched InGaAs (In composition of 53%) has a similar lattice constant (5.87Å) to AlAs (5.66Å), and thus the boundary between these two will feature fewer defects than that of the InGaAs used in the ternary QWs in this work (with In compositions of 80% and 85%). The higher the In composition, the larger the lattice constant, resulting in more defects at the barrier boundary, which will affect device performance. However, if the In composition can be matched with the inclusion of a sub-well, this problem can be mitigated, and the characteristics of the device should be like a standard ternary QW.

All the I-V results taken here are 3rd quadrant measurements, meaning electrons travel down through the RTD structure shown in Figure 4-1. This is chosen as the current density is lower in this direction due to the asymmetric 20nm/2nm InGaAs layers on either side of the QW, and thus there is less chance of device overheating, and subsequent failure.

Furthermore, wafer 3 features an asymmetric QW structure with an InAs sub-well on the barrier side (either collector or emitter depending on 1st or 3rd

quadrant operation). This asymmetry suggests the behaviour of the device and its IV characteristics will differ depending on the direction of flow of current. As the devices are measured only in the 3rd quadrant here, this comparison and subsequent analyses should be done at a future date. As the dual-pass structure requires the current to effectively pass through the QW twice, the asymmetrical QW presents additional complications. Any changes to the behaviour of the device caused by this asymmetry in the RTD area may be somewhat negated by the current passing through the QW structure the second time as the asymmetry of the QW will be flipped. Comparisons with a single-pass structure should be done later to fully investigate this.

Approximate values for the maximum power and frequency are calculated in addition to the conductance of the devices. These values do not represent the real output of the RTD devices, as the antenna structure must still be fabricated which includes large power losses and a reduction in maximum frequency. Therefore, the comparisons performed here contribute only to the optimisation of the electrical side of the device.

For each set of results, the I-V characteristics are shown. From these characteristics, the relative operation of the devices is then explained in terms of their band diagrams, and transmission coefficients. From the measured J and V values, several figures of merit (FoMs) are determined qualitatively and a comparison to the simulation work done in Baba *et al*. [86] is done.

4.3 Electrical Characterisation

The first experiment deals with wafer numbers 1 & 2. These are both ternary QW structures though they differ in QW width and In composition. Wafer 1 has a 4.5nm QW with 80% In composition, while Wafer 2 has a 3.52nm QW with 85% In composition. The I-V curves and key characteristics are shown in Figure 4-2 and Table 4-2 respectively.

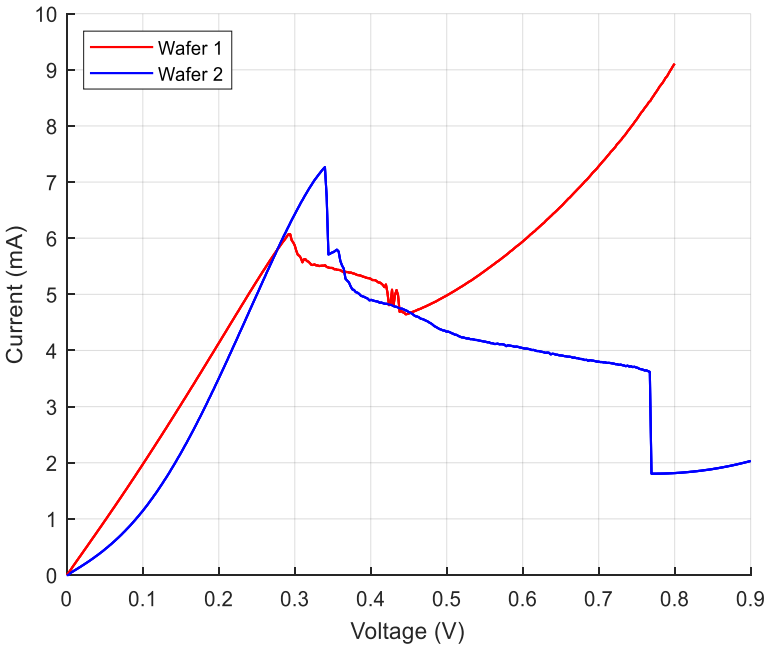

***Figure 4-2**: I-V measurements of wafer 1 (red) and wafer 2 (blue). wafer 1 has a 4.5nm QW with 80% In composition, while wafer 2 is 3.52nm wide with 85% In composition. Both devices are measured in 3rd quadrant operation.*

***Table 4-2**: J & V values extracted from Figure 4-2, and calculated PVCR and IRE from these values.*

Wafer	J_{PK} *(mA/μm²)*	J_V *(mA/μm²)*	V_{PK} *(V)*	V_V *(V)*
1	5.06	3.87	0.292	0.446
2	6.06	1.51	0.340	0.770

There are two variables in the RTD structure to consider for this experiment – the well width, and the Indium composition. Wafer 1 has a 0.98nm wider well, though a 5% lower In composition. From Schrödinger's equation for a finite well, the energy levels in the QW have an inverse square relationship with the well width. Thus, it is expected that the energy levels for wafer 1 would decrease. However, lower In composition raises the energy levels in the QW as there is an accompanying increase in bandgap energy for the InGaAs material. The combination of a wider well but lower In composition for wafer 1 will have competing effects on the energy levels, and so the results will show which of these epitaxial factors is the more decisive factor in establishing the energy levels in the QW.

To evaluate this, the V_{PK} will be analysed as this is directly related to E_1 in an RTD. An increased well width would also increase the dwell time in the QW structure which would limit the current flowing through the structure, as shown

by Kanaya *et al*. [73]. Also, a wider QW reduces the separation between E_1 and E_2, causing a higher amount of electron scattering through E_2, thus increasing J_V. Increasing the In composition decreases the effective mass, also lowering the density of states available in the QW, and thus decreases the current (J_{PK}) which can flow through. Table 4-2 shows J and V values extracted from the graph.

It can be seen then that wafer 2, with the narrower QW and higher In composition has a higher J_{PK} and lower J_V. This result is interesting when tied with the critical review in Chapter 3, in particular the J_{PK} vs J_V graph in Figure 3-2. Despite the very strong correlation between J_{PK} and J_V in the literature, these two wafers do not follow this relationship. The effect of narrowing the QW has a greater effect than increasing the In composition on J_{PK}, although only a 1mA/μm^2 difference (1.2mA) is observed. Increasing the In composition increases the separation between E_1 and E_2, thus reducing the scattering of electrons through E_2 which is one of the main components of the valley current. Therefore, a reduced valley current is measured.

Both V_{PK} and V_V are higher for wafer 2. This is explained by the raised E_1, and the increased separation between E_1 and E_2, respectively. As mentioned previously, the reduced QW width shifts E_1 up, and this effect dominates the opposing effect caused by the increased In composition. For V_V, a higher bias is required to reach E_2, which is higher due to the increased In composition.

Wafers 4 and 5 are next to be considered. Both structures feature QWs with InAs sub-wells sandwiched by lattice-matched InGaAs (In composition = 53%). The main difference between the two is the QW width – wafer 4 is 4.5nm, and wafer 5 is 3.52nm. There also exists a slight difference in In composition. For these sub-well structures, the average In composition across the QW is taken – this gives 71.8% for Wafer 4, and 68.7% for wafer 5. From the previous comparison of Wafers 1 & 2, it has been observed that the change in QW width has a greater effect on the parameters of the device, however this slight difference in In composition is important to remember. Although the same parameters are being compared here as in the previous comparison, it is useful to realise whether the sub-well structures have a similar relationship as the ternary QWs.

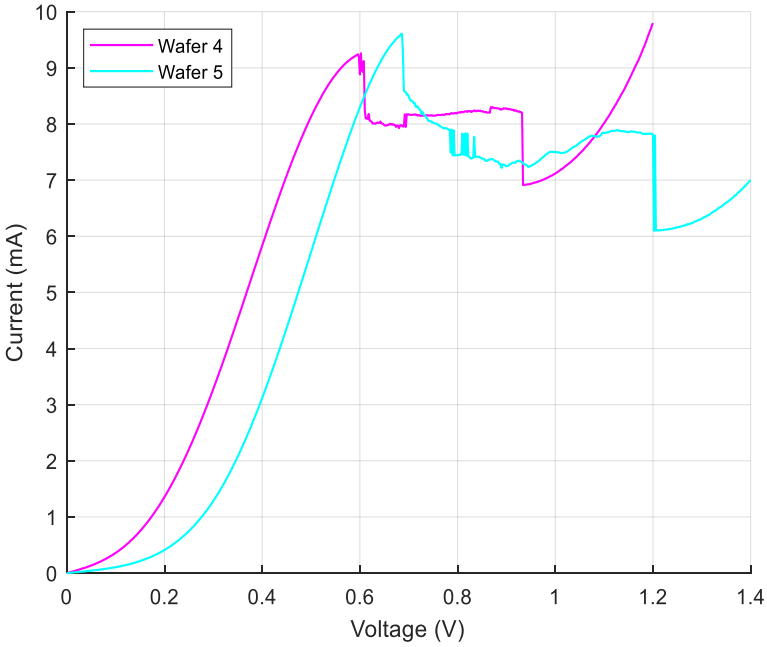

***Figure 4-3** : I-V characteristics of devices fabricated on wafer 4 (purple) & wafer 5 (cyan). Both QW structures feature an InAs sub-well between layers of $In_{0.53}Ga_{0.47}As$. The wafer 4 QW is 4.5nm wide, with a 1.37/1.76/1.37nm structure, and wafer 5 is 3.51nm wide with a 1.17/1.17/1.17nm structure. Both devices are measured in the 3rd quadrant.*

***Table 4-3**: Peak and valley values extracted from Figure 4-3*

Wafer	J_{PK} *(mA/μm²)*	J_V *(mA/μm²)*	V_{PK} *(V)*	V_V *(V)*
4	7.72	5.76	0.602	0.934
5	8.01	5.08	0.686	1.206

Figure 4-3 shows the I-V characteristics of wafers 4 & 5. It is immediately apparent that the relationship between these two sub-well structures differs from that of the ternary QWs. The difference in J_{PK} is a lot less pronounced, and the PVCR is more similar for both samples here. There is still a notable difference though, as the narrower QW (wafer 5) has a slightly higher J_{PK}, lower J_V, and higher V_{PK} and V_V. This agrees with the relative values from the previous comparison, however the differences between the sub-well samples are smaller.

The J_{PK} difference can once again be explained by the reduced dwell time in the QW for the narrower well sample, wafer 5. At the same time, the separation between E_1 and E_2 is increased, resulting in a lower J_V and increased V_V. V_{PK} is also increased as E_1 is higher, as expected. Although the In composition difference is only 3.1%, it is still worth commenting on its effect on the I-V characteristics. Contrary to the ternary samples, the sample with the wider QW has a higher In

composition in this case. Therefore, as opposed to the ternary samples, the higher In composition and wider QW both result in a lower J_{PK}. These factors also both contribute to a reduced E_1, and thus V_{PK}. However, when considering E_2, increasing In composition and increasing well width have opposing effects. This explains why J_V does not differ as much for the sub-well structures compared to the ternary ones.

The next comparison is done between devices with an InAs sub-well vs purely ternary QW devices. For this investigation, comparisons at two different QW widths – 3.52nm and 4.5nm – are performed. Wafers 2 and 5 both have 3.52nm QWs and wafers 1 and 4 have 4.5nm QWs. Although ideally, we'd like to only change one variable (the inclusion of the sub-well), the In composition is also affected as the structure of the QW changes. Therefore, the difference in In composition must also be accounted for in our analysis. By including two different QW widths, discrepancies due to In composition and other differences in device quality will be minimised.

Table 4-4 shows the effect of an InAs sub-well. In both cases, the devices with the sub-well (wafers 4 and 5) have higher peak and valley currents and voltages. Lower In compositions for both sub-well structures will contribute to this. For the 3.52nm comparison, wafer 2 has 85% In, compared to 68.7% for wafer 5, and for the 4.5nm samples, wafer 1 has 80% while wafer 4 has 71.8%. The lower In composition will increase the density of states in the QW, thus increasing the current which can flow through the device. It will also result in an increase in E_1, and therefore V_{PK}. Both expected patterns are visible in the I-V graphs of Figure 4-4.

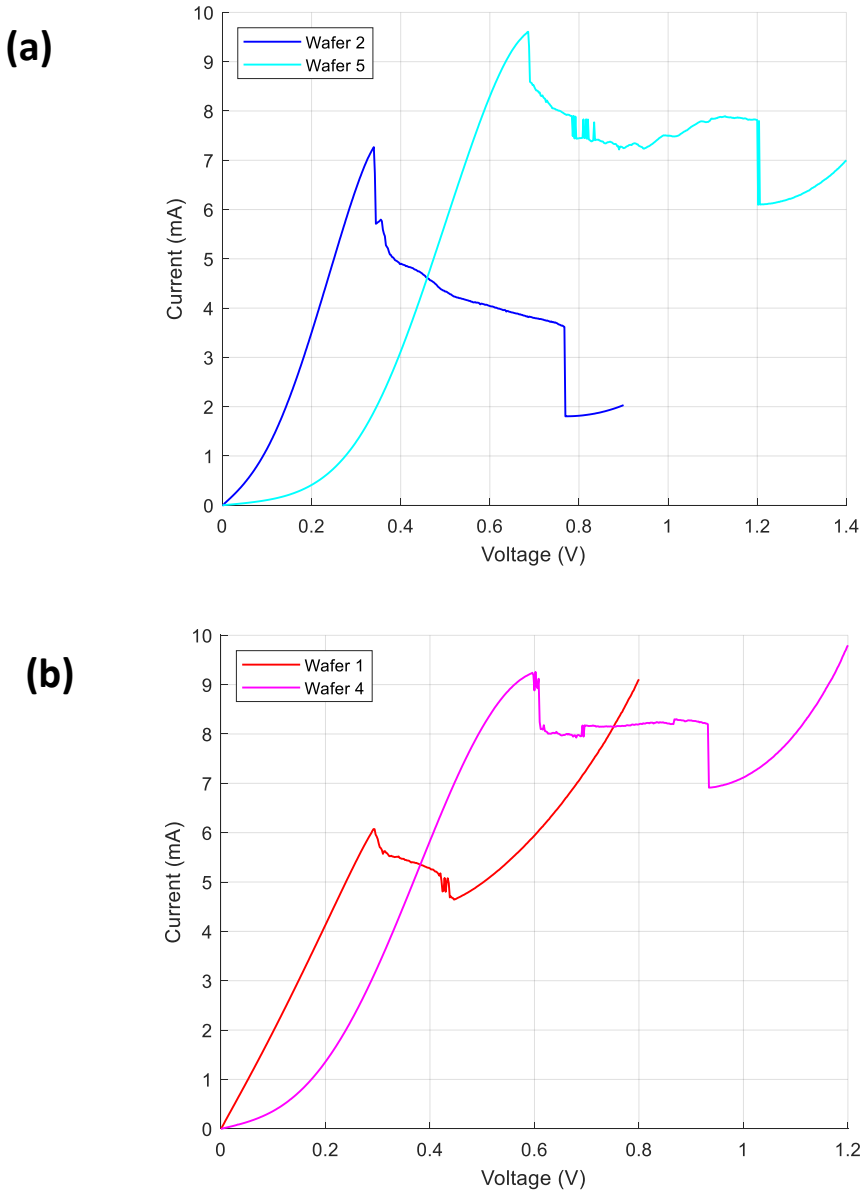

***Figure 4-4**: I-Vs comparing the ternary QW to the sub-well structure. In (a), both samples have a 3.52nm well width, comparing wafer 2 (dark blue, ternary) with wafer 5 (cyan, sub-well). In (b), both samples have a 4.5nm well width. wafer 1 (ternary) is in red, and wafer 4 (sub-well) is in magenta.*

***Table 4-4**: Table showing peak and valley values, taken from the I-V graphs in **Figure 4-4**.*

Wafer	J_{PK} *(mA/μm²)*	J_V *(mA/μm²)*	V_{PK} *(V)*	V_V *(V)*
2	6.06	1.51	0.34	0.77
5	8.01	5.08	0.686	1.21
1	5.06	3.87	0.292	0.446
4	7.72	5.76	0.602	0.934

When examining the values in Table 4-4, the most notable difference between the 3.52nm and 4.5nm samples is the valley current difference. For the 3.52nm samples, valley current differs by 3.57mA/μm^2 compared to just 1.89mA/μm^2 for the 4.5nm samples. This difference results in larger PVCR and IRE

values for the 3.52nm samples, in particular for the ternary QW sample (wafer 2). This difference can be explained by the difference in QW width, as previously discussed.

The final variation in epitaxial structure investigated here relates to the position of the sub-well within the QW. The commonest structures feature the sub-well in the centre of the QW, making a symmetric structure. However, an asymmetric structure should give different results depending on the direction of the asymmetry. Two samples with 3.52nm QWs are compared here, with equal In compositions of 68.7% (2.34nm InGaAs, 1.17nm InAs). These are from wafers 3 and 5 in Table 4-1. Wafer 3 features the asymmetric structure, with the InAs sub-well adjoining one of the barriers, while wafer 5 is a symmetric structure. The I-V characteristics of these devices are compared in Figure 4-5 below.

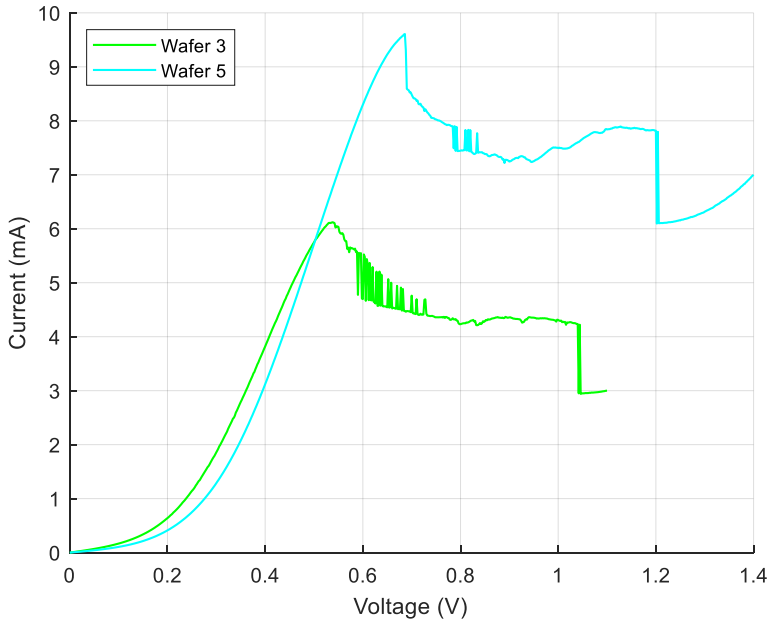

***Figure 4-5**: I-V graph of two devices, one with a centred sub-well (wafer 5, cyan), and one with an asymmetric sub-well (wafer 3, green)*

***Table 4-5:** Peak and valley I-V values obtained from Figure 4-5.*

Wafer	J_{PK} *(mA/μm²)*	J_V *(mA/μm²)*	V_{PK} *(V)*	V_V *(V)*
3	5.1	2.45	0.538	1.046
5	8.01	5.08	0.686	1.21

The graph in Figure 4-5 shows the asymmetric structure causes a significant reduction in the peak and valley currents and voltages. However, there is an

increase in PVCR and IRE. As ascertained previously, the increase in PVCR is expected as J_{PK} decreases due to the nature of the relationship between J_{PK} and J_V. The difference in IRE is mainly due to the drop in bias point (at the midpoint of the NDR region). The ΔI and ΔV values do not differ by much, though are slightly higher for Wafer 5. However, the effect of this difference is outweighed by the lower I_{BIAS} and V_{BIAS}, resulting in an IRE 1.83x larger for the asymmetric structure.

For both structures, the E_1 levels are expected to be similar as the structural parameters discussed previously in this section are the same. Therefore, it is expected that V_{PK} would be similar for both. However, this is experimentally shown to be false, with V_{PK} being 0.148V lower for the asymmetrical structure. Therefore, the sub-well position must affect the alignment of the electron energy outside the QW to the E_1 value within. This could be caused by the change to the shape of the potential energy in the well under bias conditions. A standard ternary structure would have a triangular potential well, whereas the sub-well structure may compensate for/exacerbate this depending on the direction the bias is applied. This could affect the tunnelling probability through the first barrier, affecting the bias required for resonant tunnelling to occur (V_{PK}).

The asymmetrical QW also has a much lower J_{PK}, 5.1mA/μm^2 compared to the 8.01mA/μm^2 for the central sub-well structure. This suggests that the asymmetrical structure slows the tunnelling rate of electrons. This could again be related to the shape of the potential well as explained above, possibly increasing the dwell time within the QW. The same reasoning could be applied to J_V which is also lower for the asymmetrical structure by 2.63mA/μm^2.

4.4 Comparison with Simulation

From simulation work done in Baba *et al.* [86], the effects of varying barrier width, QW width and In composition were investigated. From this work, Figure 4-6 shows how these epitaxial parameters are predicted to affect the IRE, E_1 level and transmission peaks for both ternary and sub-well structures.

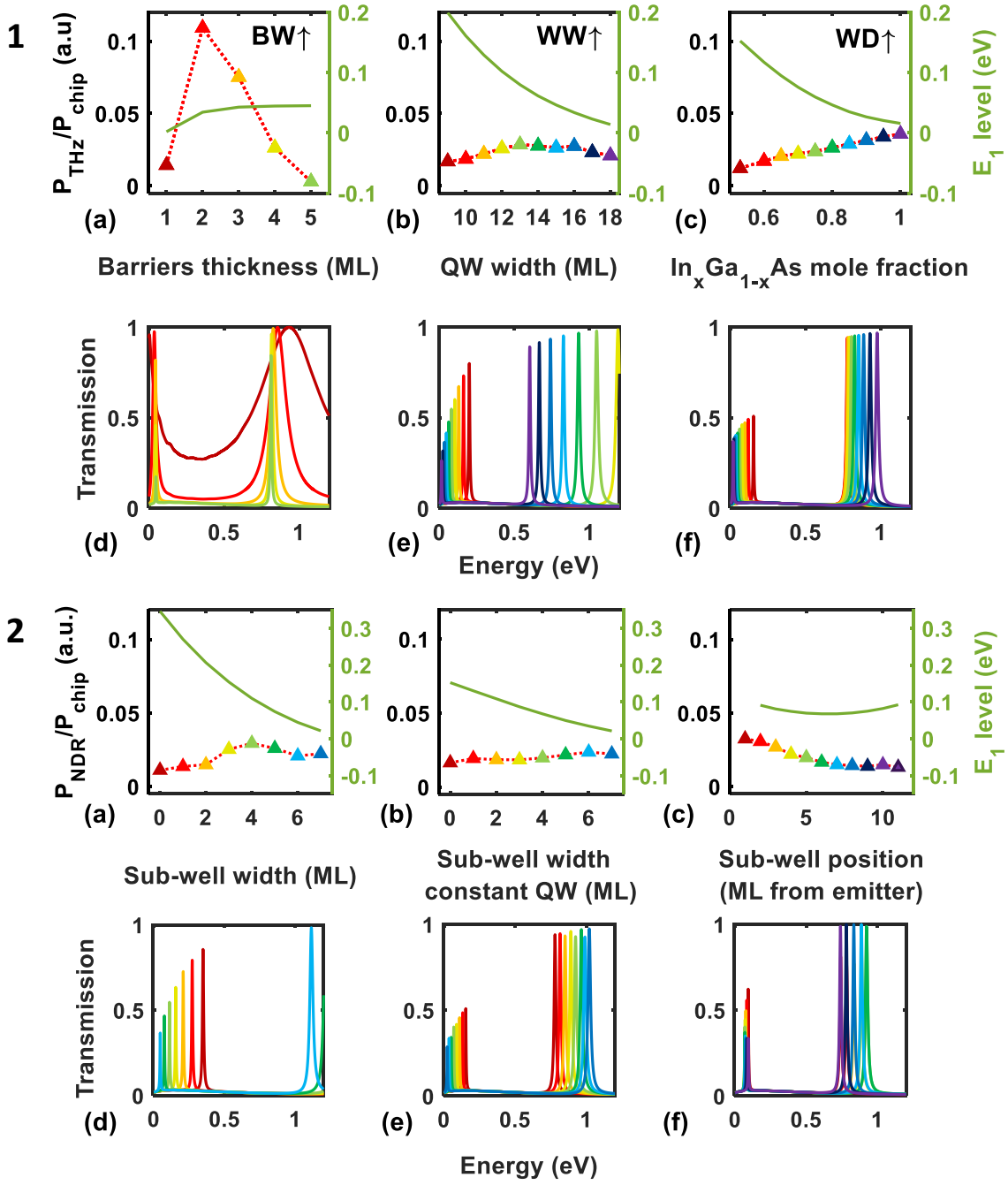

***Figure 4-6**: From Baba et al. [86], simulation results are shown to estimate IRE and transmission coefficients of RTD devices with differing structural parameters. Section 1 corresponds to the ternary QW structure, with barrier width, well width, and In composition being investigated. Section 2 represents the sub-well structure, with the QW width, the sub-well width, and the sub-well position being altered.*

***Table 4-6**: Simulated values for the energy levels, full widths at half maximum for the transmission coefficients, and the predicted IRE, for the devices characterised here, extracted from Figure 4-6*

Wafer	*E_1 (meV)*	*E_2 (meV)*	*ΔE (meV)*	*E_1 FWHM (meV)*	*E_2 FWHM (meV)*	*IRE (%)*
1	46.2	827	781	5.89	17.2	2.64
2	90.6	1220	1130	6.84	30.6	2.85
3	101	741	640	6.18	14.5	3.24
4	34.8	990	955	5.56	21.5	2.36
5	110	>1200	>1090	6.56	N/A	2.94

General trends can be established, allowing for a qualitative analysis. These graphs are based on a reference sample with 1.17nm barriers and a 4.5nm well with 80% In composition. One of these parameters is then changed in each graph to simulate a sensitivity analysis.

Table 4-6 shows extracted values for each of the structures fabricated in this work. Relative differences in IRE, E_n, and FWHM values are calculated and summed to give approximations in each case. Although some inaccuracy is unavoidable with this method, it is hoped that the general trends and scale of the differences are still useful for comparison with the practical results.

In both the ternary and sub-well cases, increasing the QW width results in a predicted reduction in E_1, E_2, ΔE and the FWHMs of both energy levels. The IRE is shown to peak at a certain width. Increasing the In composition (and analogously the sub-well width with constant QW) should also reduce E_1, though E_2, and hence, ΔE, is increased also. For the ternary case, the IRE is expected to increase linearly with the In composition, although for the sub-well case, only a very slight variation is visible. Trends in FWHM are unclear.

Wafers 1 & 2 are compared in the first experiment. These two structures feature competing changes in QW width and In composition. As V_{PK} is lower for the wafer 1, this agrees with the trend in E_1 in the simulation. Wafer 2 is expected to have a higher ΔE, proven true by the reduced J_V. The increased E_1 FWHM relates to the J_{PK} for wafer 2 as well, showing further agreement with the simulation. The real IRE value of 2.09% is slightly below the 2.64% simulated for wafer 1, and the IRE of wafer 2 is higher than wafer 1 in both simulation and real data. However, the IRE of wafer 2 is much higher in practice, at 17.5%, over 6x higher than the simulated value. The simulation therefore either underestimates the P_{NDR} or overestimates the P_{CHIP}.

Experiment 2 also dealt with two samples with differing QW widths, and slightly different In compositions, though with sub-well structures. In this case, wafer 4 is the wider QW with a slightly higher In composition in comparison with wafer 5. The E_1 level is expected to be significantly lower for wafer 4, however there is only a small difference in V_{PK}. Further comparisons are required to

determine whether this is due to an overestimation of E_1 for wafer 5, or an underestimation for wafer 4, or possibly both. Wafer 4 is also expected to have a reduced ΔE, and this is agreed experimentally due to the slightly higher J_V. Further agreement is found when considering the E_1 FWHM which is lower for wafer 4, correlated by a lower J_{PK}. The predicted IRE values for the sub-well structures are 2.36% and 2.94%, for wafers 4 and 5, respectively. The actual values are 2.36% and 4.61%. For wafer 4, the IRE is identical, suggesting good agreement between the simulation and practice. For wafer 5, a 1.67% difference in IRE is found, with the simulation underestimating the value, similar to experiment 1.

Comparisons of the two structures was done in experiment 3. At 3.52nm QW width, wafers 2 (ternary) and 5 (sub-well) were compared, and at 4.5nm width, wafers 1 (ternary) and 4 (sub-well) were compared. In addition to the structure, the In composition also varies between samples and must be taken into consideration. Firstly, in both the 3.52nm and 4.5nm cases, lower simulated E_1 for wafers 1 and 2 (ternary structures) does correctly translate to lower V_{PK}. The ΔE comparison is only possible for the 4.5nm samples, as the simulation predicts E_2 as lying above the AlAs conduction band and thus, not in the QW. The ΔE is expected to be higher for the sub-well structure (Wafer 4), however this does not correlate to a lower J_V. Instead, J_V is higher in both 3.52nm and 4.5nm cases. This suggests that less scattering occurs in the ternary case, possibly due to fewer boundaries, and hence, fewer defects in the materials, resulting in lower J_V. The simulated E_1 FWHM is lower in both cases for the sub-well structures (Wafers 4 and 5) and so lower J_{PK} would be expected also. However, J_{PK} is greater for both sub-well structures. This could be due to the difference in In composition which leads to a higher J_{PK} for the sub-well structures due to a higher density of states. The IRE values for the 4.5nm structures are relatively close to the simulated values, although the ternary IRE is slightly lower rather than higher than the sub-well case. The 3.52nm structures, however, differ significantly from the simulated values. The 3.52nm sub-well structure (wafer 5) has an IRE 1.57 times greater than the simulated value and the ternary structure (wafer 2) is 6.14 times greater. This suggests the simulated I-V requires more refinement in the 3.52nm case and is perhaps indicative of an issue with other QW widths, although further work is required to confirm this.

The final experiment investigates the position of the sub-well. Wafers 3 (asymmetrical QW) and 5 (symmetrical QW) are considered here and the pertinent simulated graphs are (c) and (f) from Figure 4-6. However, these graphs consider a 4.5nm QW and so the values extracted from them will not be accurate to the real results. It is still worthwhile to investigate the trend in values as this should apply to both 3.52nm and 4.5nm QWs. The E_1 level, for example is shown to be at its lowest when the sub-well is centred, suggesting V_{PK} will also be lower. This is not true from the practical measurements, as wafer 5 has a higher V_{PK}. It is also apparent from Figure 4-6(f) that the symmetrical well features a higher ΔE. However, again the measured results show a lower J_V, and V_V, in the asymmetrical case, implying the opposite of the simulation is true. The simulated E_1 FWHM is larger in the symmetrical case, which does translate to a higher J_{PK} in practice. Finally, the IRE values differ considerably for both structures when measured compared to the simulation. Although there is agreement that the asymmetrical device has higher IRE, the IRE value is larger by 2.6 times in the asymmetrical case, and by 1.57 times in the symmetrical case. Once again, this suggests some inaccuracies in the calculation of IRE in the software. The real values measured in this experiment differ the most from the simulation, compared with all the other experiments. Given the QW width and the In composition are kept the same, it is suggested that the effect of strain on the well structure is more complicated than the simulation suggests.

4.5 Analysis of FoMs and Literature Comparison

Using the J and V values, several FoMs can be calculated or approximated using the equations mentioned in Chapter 3. These are shown in Table 4-7 for Wafers 1 & 2.

***Table 4-7** : Figures of merit for Wafers 1 & 2. These are calculated from both the I-V values in Table 4-2, and the device structures.*

Wafer	*PVCR*	*IRE*	G_{RTD}*(mS)*	f_C*(THz)*	P_{MAX} *(μW)*
1	1.31	2.09	13.9	0.563	41
2	4.02	17.5	19.1	0.573	440

As expected from the J and V values, the PVCR and IRE are both higher for wafer 2. These are both indicators of the higher quality of the QW structure and suggest wafer 2 is a design more suited for practical applications. Calculations of f_C and P_{MAX} also confirm this, as they are both higher for wafer 2. The P_{MAX} value, is over 10x greater due to increases in both ΔJ and ΔV, caused by the narrower well and increased In composition. It is important to remember that this P_{MAX} value is the maximum theoretical power. Losses in the antenna are unavoidable and will reduce this to give the actual power output.

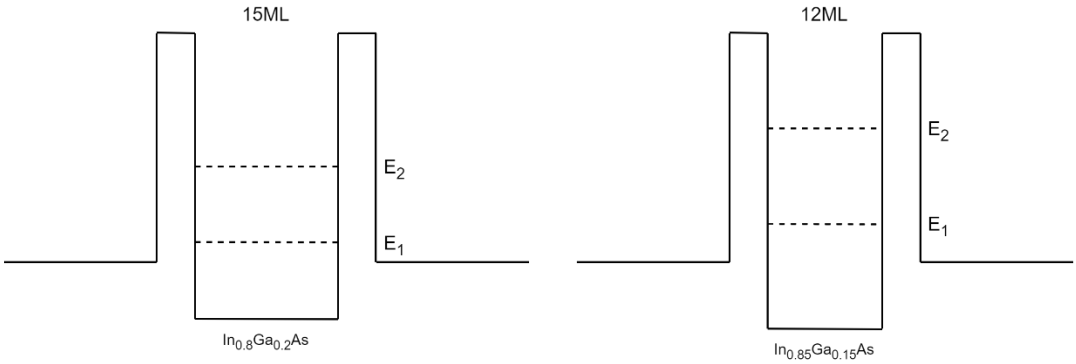

***Figure 4-7**: Simplified band diagrams for wafers 1 (left) & 2 (right) under zero bias conditions. Relative positions of E_1 & E_2 are displayed based on the I-V characteristics.*

Figure 4-7 provides a representation of the analysis performed above. V_{PK} is largely dependent on E_1 and so E_1 is lower for the 4.5nm structure. The relative position of E_2 can be determined from E_1, J_V, and V_V. The separation between E_1 and E_2 affects the amount of scattering which occurs through the E_2 level, and this, in turn, relates to the valley current. Also, the valley point represents when electrons begin to tunnel through E_2, and so V_V will scale with E_2. Therefore, for the 4.5nm sample (wafer 1), both E_1 and E_2 are shown to be lower than their respective values for the 3.52nm sample (wafer 2).

To complete the analysis of these results, a comparison with results in the literature is done, demonstrating the benefits of the systematic analysis done in this thesis. As both structures considered here have simple ternary QWs, they will only be compared with other devices with ternary QWs. Figure 4-8 and Figure 4-9 look at how the two QW parameters discussed in this section – well width and Indium composition – affect the J_{PK} of a number of devices in the literature.

An inverse relationship between J_{PK} - and consequently, J_V – and well width is apparent. The R value of 73% suggests a good correlation. This could be explained by the longer dwell time in the QW in a device with longer well width, which reduces the rate of electrons passing through the structure. The two data points ascertained in this work lie below the plotted trendline. These results were obtained in 3rd quadrant operation whereas the literature results were all obtained in 1st quadrant, which would give the higher J_{PK} seen in the graph. It is also apparent that the two results obtained in this work appear to trend contrary to the literature, with a slight positive correlation. Further work with a wider range of well widths should be performed to investigate this.

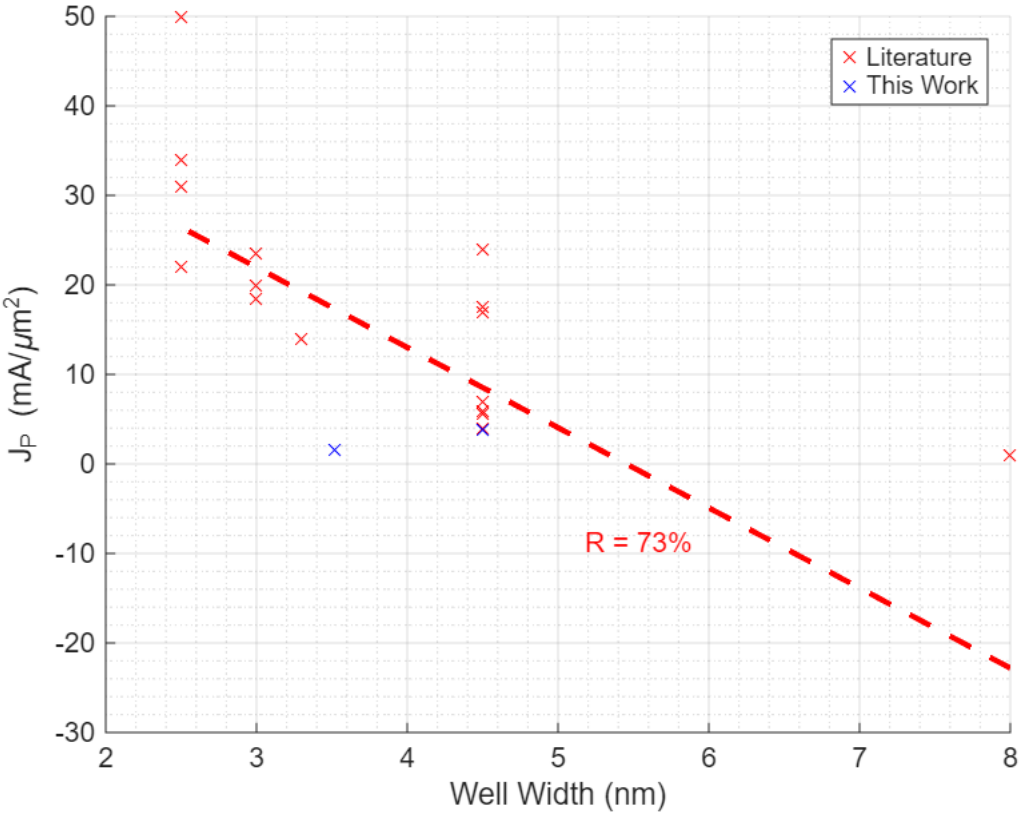

***Figure 4-8**: J_{PK} vs well width from the literature for ternary QW structures. This work is shown in blue. The line of best fit is determined by Theil-Sen regression, and the R value is shown.*

For the V_{PK} case (in Appendix D-1), there is no recognisable correlation with the well width as shown by the R value of only 9%. Increasing well width has been shown to lower E_1 in the QW, which should result in a lower V_{PK}. However, other differences in structural parameters and device designs contribute to this, making this correlation very difficult to ascertain through a literature review. The two data points representing this work again lie below the literature trendline for the same reason suggested previously. The trend in these two points, however, agrees

with the expected behaviour of the E_1 level, though further controlled measurements are required to confirm this.

Figure 4-9 shows the J_{PK} trend with changing In composition. As In composition increases, J_{PK} generally increases also, with an R of 69%. However, the data used here is limited in featuring only 3 (4, with new data) different values of In composition. Furthermore, for each of these values, there is a large variation around the trendline, suggesting a combination of other epitaxial parameters have an overall greater effect on J_{PK}. Like the case for well width, both devices in this work lie below the literature trendline due to the 3rd quadrant measurement. The new results also follow the same trend as the literature, with a slight positive relationship. Again, similarly to the well width, there is a weak correlation between V_{PK} and In composition (Appendix D-2). Despite a higher In composition lowering E_1, this does not appear to result in a lower V_{PK}. Other structural parameters, particularly the well width, must also affect this, leading to an unclear correlation.

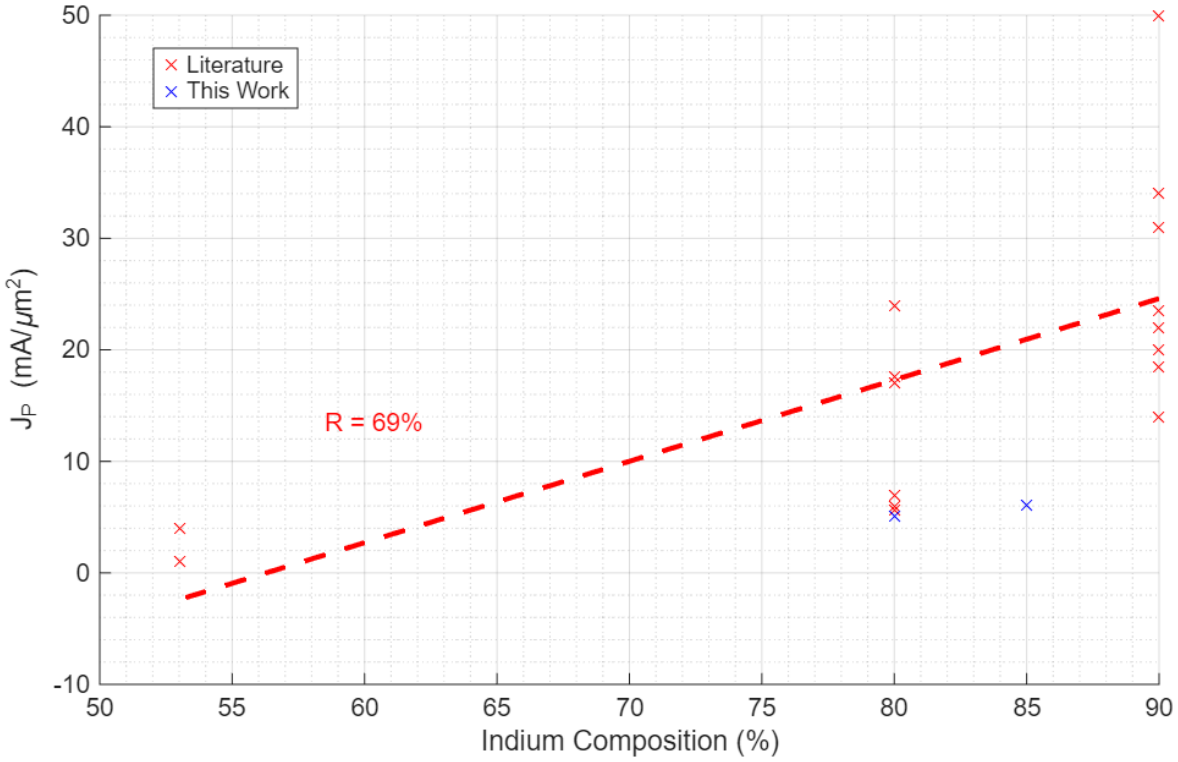

***Figure 4-9**: J_{PK} vs In composition for devices with ternary QW structures. The data points for this work are shown in blue. The best fit line is found using Theil-Sen regression and the R value is displayed next to the line.*

For the comparison of wafers 4 & 5 (w/ sub-well), the FoMs are also analysed. Once again, the effect of decreasing the QW width is to increase PVCR and IRE values. Table 4-8 shows how this affects the estimated P_{MAX} and f_C.

***Table 4-8**: Figures of merit calculated for wafers 4 & 5 from I-V measurements and device structural parameters.*

Wafer	*PVCR*	*IRE*	*G_{RTD} (mS)*	*f_C (THz)*	*P_{MAX} (μW)*
4	1.34	2.36	10.6	526	146
5	1.58	4.61	10.1	500	342

As expected, due to the improved IRE and PVCR, P_{MAX} is also estimated as over 2x higher. However, wafer 4 features a higher estimated output frequency. Whereas for the ternary QW samples discussed previously the narrower QW featured a higher frequency, the opposite is true here. This is shown by the difference in G_{RTD}, which is slightly higher for wafer 4. As G_{RTD} is determined from the ΔI and ΔV values (in particular, the ratio between the two), the most obvious difference in the two cases is the J_V value. For the ternary samples, J_V differs by more than a factor of two whereas the factor is only around 1.1x for the sub-well samples. This suggests the position of E_2 varies less in the sub-well structure than the ternary one when the QW width is changed. The predicted relative band diagrams are shown in Figure 4-10.

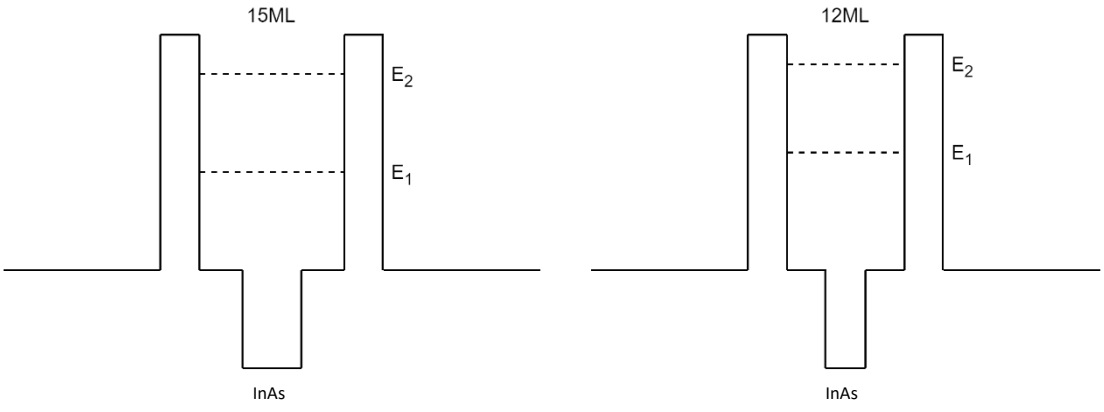

***Figure 4-10** : Relative conduction band diagrams for wafers 4 (left) and 5 (right). The values are not absolute, and the diagram is not to scale.*

The lower V_{PK} value for wafer 4 translates to a lower E_1 level. The higher J_V, and lower V_V, suggests a smaller ΔE as more scattering occurs, and less energy is required for electrons to tunnel through E_2. Therefore, E_1 and E_2 for the wider

QW sample (wafer 4) are lower than their respective values for the narrower sample (wafer 5). A literature comparison of TIT structures is performed in Figure 4-11 investigating the relationship between J_{PK} and the well width:

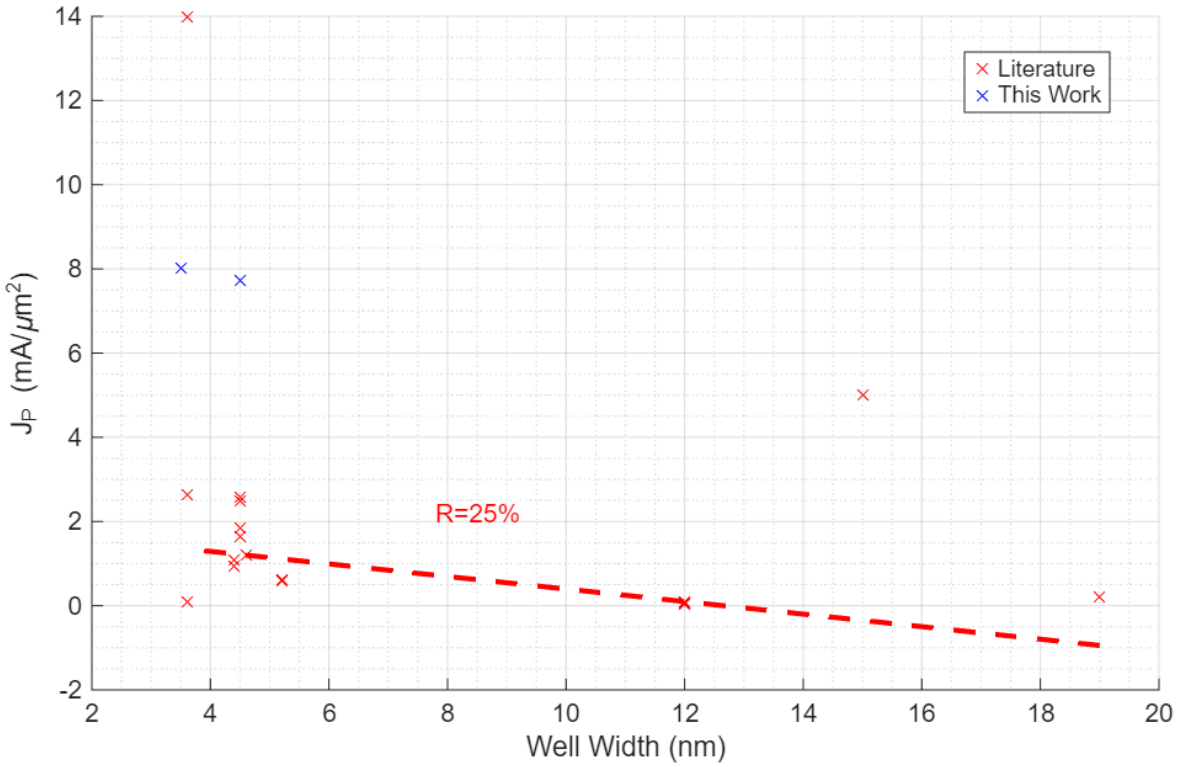

Figure 4-11: *J_{PK} vs well width, taken from a number of sources in the literature. Theil-Sen regression is used for the line of best fit, and the R value is shown next to the line. Data points from this work are shown in blue.*

For both J_{PK} and V_{PK} (Appendix D-3), a weak correlation can be seen, with an R value of 25% for the current density and only 20% for the voltage. This suggests other factors, such as barrier width, have a greater impact on the I-V characteristics. For J_{PK} this is particularly interesting, as it differs from the relationship shown previously for the ternary case. Another interesting observation is that both devices tested in this work lie above the plotted trendline for J_{PK} and V_{PK}. Contrary to the ternary case, this suggests that the sub-well devices are an improvement on devices in the literature for J_{PK} and a slight deterioration for V_{PK}. Again, this could be due to the thin barrier width as most of the devices used in the sub-well literature review have thicker barriers, consequently lowering J_{PK}. The effect of In composition on J_{PK} is explored in Figure 4-12.

Figure 4-12 shows a medium correlation between Indium composition and J_{PK} in the literature, with an R value of 44%. There is a slight negative trend in J_{PK} as the In composition increases. This disagrees with the positive trend found for the ternary QW case in Figure 4-9. The data also features noticeably large outliers, particularly at low In composition values (68.7%). The two data points representing this work also appear as outliers to the fitted line, lying well above the weak trend from the literature. These two points also show a slight negative trend but at higher J_{PK} values. More data will give a more accurate analysis of this trend but the scale of the variance in data points suggests other factors have a greater impact on J_{PK} than the In composition.

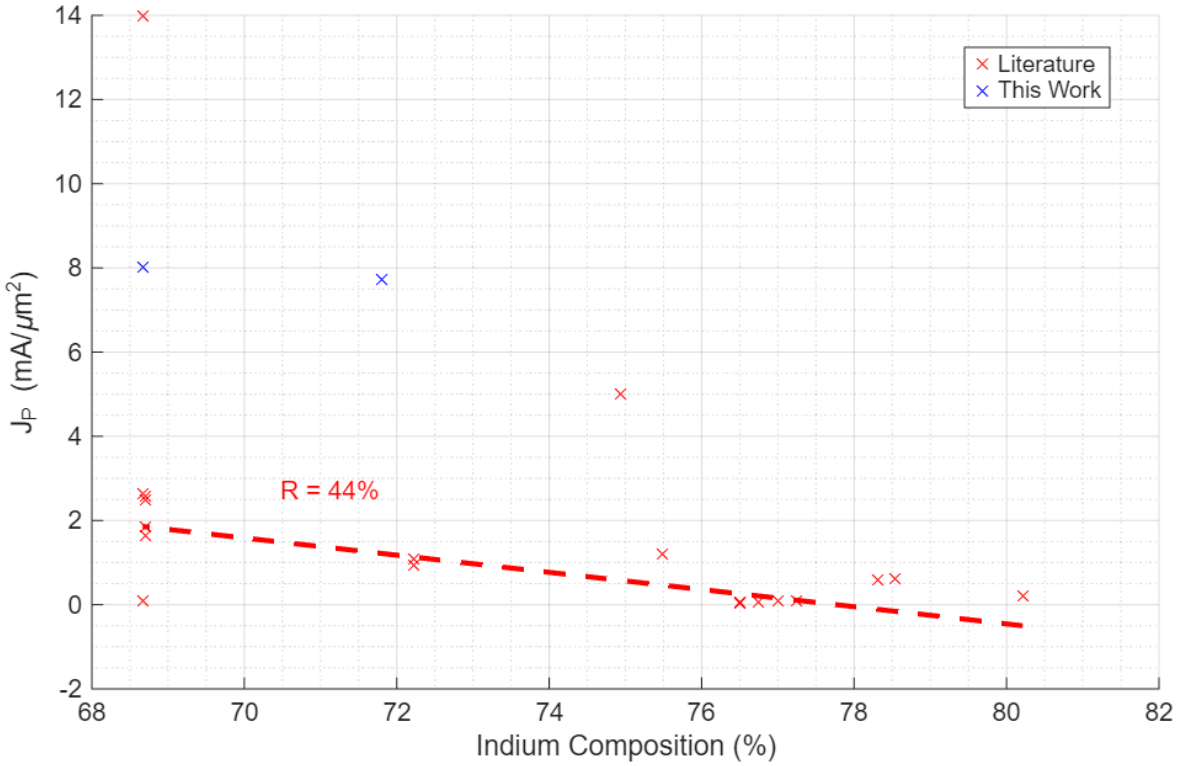

Figure 4-12: *J_{PK} vs In composition from the literature. A Theil-Sen best fit line is plotted with the R value next to it. Data from this work is shown in blue.*

There is no correlation calculated between In composition and V_{PK}, as shown in Appendix D-4. An R value of 7% demonstrates this. The two values found in this thesis, appear to show a slight negative trend, similar to the case for Figure 4-12, but the overall trend in the literature suggests this is a coincidence and other factors influence V_{PK} to greater effect.

In the ternary vs sub-well comparison, although the 3.52nm samples have higher PVCR and IRE, the relative difference in these values is also useful to

highlight. For the 3.52nm samples, wafer 2 has much higher PVCR and IRE when compared to wafer 5. However, for the 4.5nm samples, it can be seen that the sub-well sample, wafer 4, has slightly higher PVCR and IRE. Table 4-9 further explores the effect the sub-well has on the theoretical output of the device.

***Table 4-9**: Table showing FoMs for each device, calculated from the values in Table 4-4, and the structural parameters of the RTDs themselves.*

Wafer	*PVCR*	*IRE*	G_{RTD}*(mS)*	f_C*(THz)*	P_{MAX}*(μW)*
2	4.02	17.5	19.1	0.573	440
5	1.58	4.61	10.1	0.500	342
1	1.31	2.09	13.9	0.563	41
4	1.34	2.36	10.6	0.526	146

The PVCR and IRE differences between 3.52nm and 4.5nm have been analysed previously. However, the effect of the sub-well structure at each of these widths affects the PVCR and IRE differently. At 3.52nm width, the sub-well, in combination with the reduced In composition, results in ~2.5x reduction in PVCR and a ~3.8x reduction in IRE. This also means the theoretical output frequency and power are lower. Therefore, despite the added stability the sub-well structure provides to the growth process, the drop in performance makes this structure unsatisfactory for the fabrication of devices to be used in practice. However, a comparison should be performed with a sub-well structure device with an equivalent In composition to ascertain an indisputable conclusion.

This comparison differs for the 4.5nm sample. The sub-well structure leads to a marginal increase in PVCR and IRE. Again, the In composition differs significantly. However, the device with the sub-well structure (wafer 4) has a ~1.02x increase in PVCR and ~1.13x increase in IRE. This does not directly translate to increases in theoretical frequency and power, however. As expected, the trend in frequency follows the trend in conductance, so wafer 4 has a theoretical output frequency 37GHz lower than wafer 1. The P_{MAX}, on the other hand, trends in the opposite direction, with wafer 4 being 105μW higher than wafer 1. As P_{MAX} is proportional to ΔV, and G_{RTD} is inversely proportional to ΔV, this difference in trend is explained by the increased ΔV for wafer 4. Although this increase in ΔV is also seen for the 3.52nm sub-well structure, the significant decrease in ΔJ results in

the lower power we see in Table 4-9. Relative conduction band diagrams are shown in Figure 4-13.

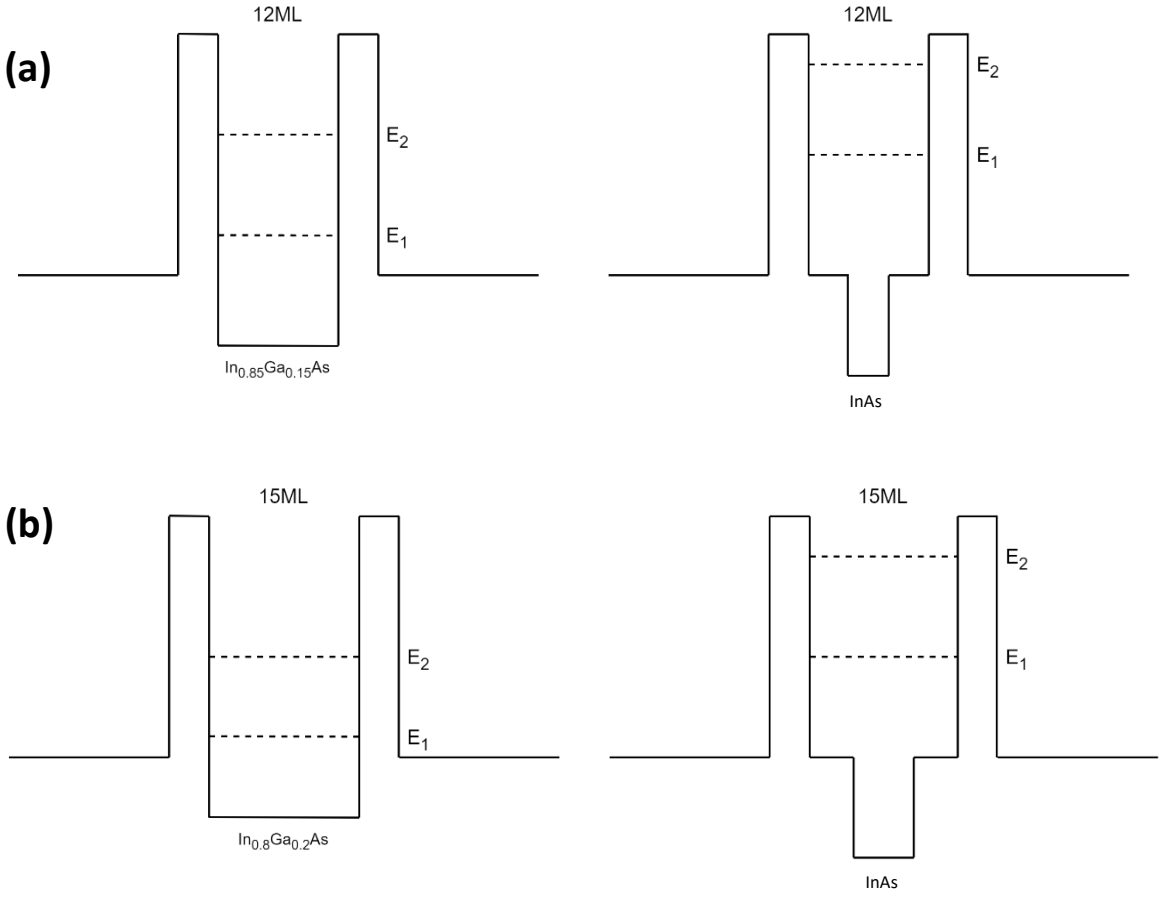

***Figure 4-13**: Conduction energy band diagrams for (a) 3.52nm and (b) 4.5nm QW widths. In each case, the ternary QW is represented on the left, and the sub-well structure on the right. The estimated relative positions of E_1 and E_2 are shown also.*

As can be seen in Figure 4-13, the sub-well structure increases both E_1 and E_2 at both QW widths. For the 3.52nm structures, the In composition difference is 16.3% compared to 8.2% for the 4.5nm ones. This difference results in ΔE_1 for the 3.52nm samples being larger than that for the 4.5nm samples. As E_1 is proportional to V_{PK}, it is expected to be higher for the sub-well structures compared to the ternary structures, and higher for the 3.52nm QW than the 4.5nm QW, as explored previously. E_2 is estimated by observing the valley and ΔV values. ΔV is higher for the 3.52nm devices and for the sub-well structures, and therefore a corresponding larger ΔE is expected to follow this trend. A comparison of ternary and sub-well structures is shown in Figure 4-14.

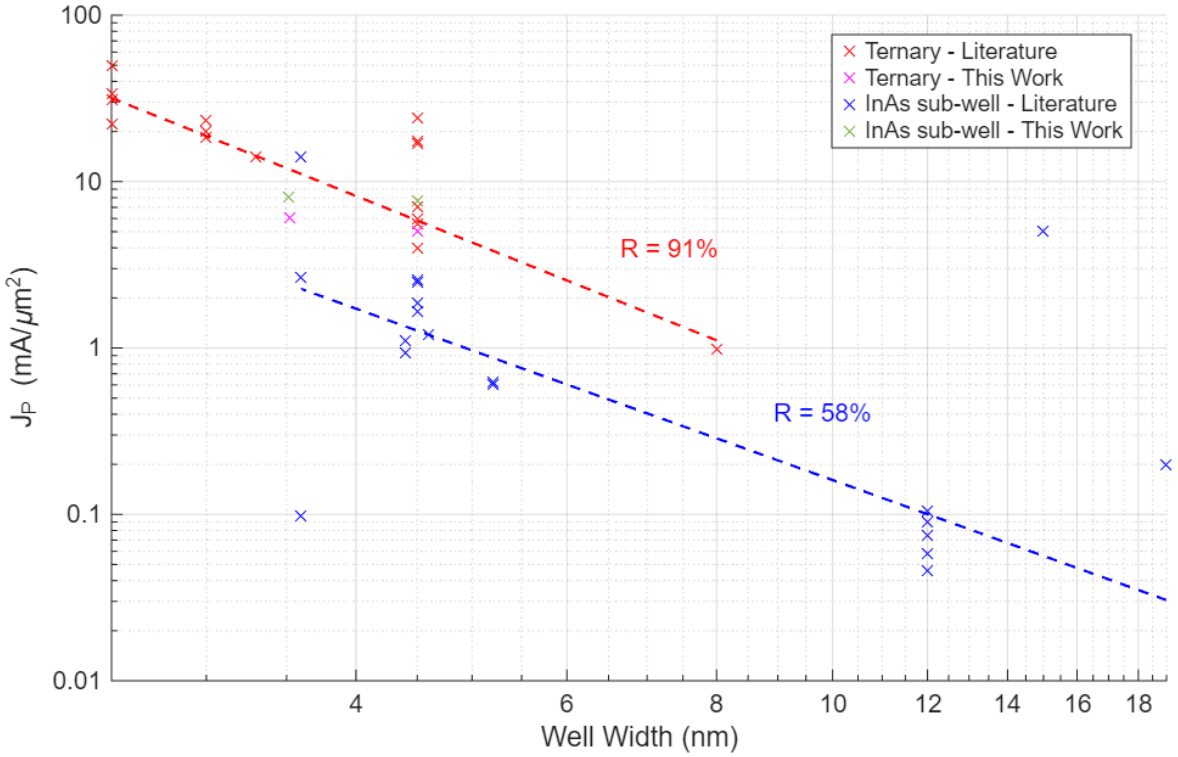

Figure 4-14: *Graph of J_{PK} vs well width, for both ternary and sub-well QW structures. The literature values are in red (ternary) and blue (sub-well), while the data points obtained in this work are magenta (ternary) and green (sub-well).*

A negative correlation is found in the J_{PK} case, with higher J_{PK} values for the ternary case. Narrower well widths are available for the ternary data in the literature, whereas the sub-well structures tend to feature wider wells. Also, the ternary results have a much stronger correlation (R = 91%), compared to the sub-well structures (R = 58%), possibly caused by other factors such as barrier width, which varies more for the sub-well data. It can also be noted that the data from this work demonstrates marginally higher J_{PK} values for the sub-well structure, in disagreement with the literature trend. This further suggests that the influence of other factors affects the perceived trends and demonstrates the need for further systematic analysis like is done here.

The V_{PK} vs well width graph in Appendix D-5 shows very little to no correlation between the two. R values of 9% and 20% for the ternary and sub-well data, respectively, suggest the well width has very little impact on V_{PK}. However, this does not agree with the expected physical change of the QW, as making the QW wider is expected to reduce E_1, and hence, V_{PK}. Therefore, by observing the new data we can see this expected behaviour, as both ternary and sub-well

structures show negative trends. Further work is required to explore the extent and exact shape of this trend. Furthermore, like the J_{PK} case, higher V_{PK} values are found for the ternary case in the literature, but this work demonstrates the opposite – the sub-well structures feature higher V_{PK}. A similar comparison is done against In composition, shown in Figure 4-15.

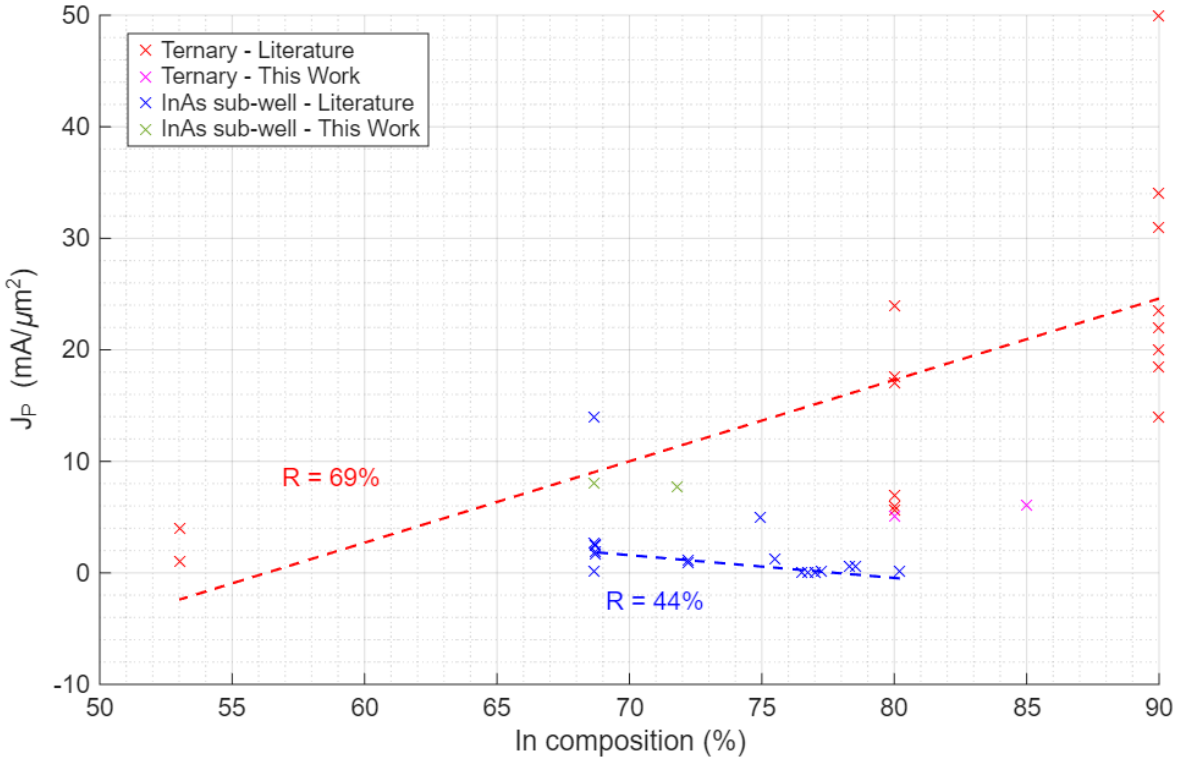

Figure 4-15: *The relationship of J_{PK} against well width is shown for both the ternary and sub-well structures. The literature values are shown in red (ternary), and blue (sub-well), and the new data from this work is shown in magenta (ternary), and green (sub-well).*

Again, a trend is visible for the J_{PK} case but not for V_{PK} (Appendix D-6). However, the J_{PK} trends are not as strong as for the well width, with R for the ternary being 69%, and 44% for the sub-well. There is also a difference in direction of the trend. The ternary case shows a positive correlation, in disagreement with the physical expectation. However, the sub-well structure does feature a slight negative trend, although from a much narrower subset of In composition values. Also, the data points corresponding to this work show that the sub-well devices (with lower In composition) have slightly higher J_{PK}, than their ternary counterparts. This agrees with the expected physical behaviour, although further data points are required to ascertain how the well structure affects J_{PK}.

For V_{PK}, both R values (21% for ternary and 7% for sub-well devices), suggest a weak correlation between In composition and V_{PK}. However, increasing the In composition should lower the E_1 level, thus reducing V_{PK}. This is visible from the new data points, although the exact shape of the trend isn't clear, and further work is required.

For the symmetrical (wafer 5) vs asymmetrical (wafer 3) QW comparison, the FoMs are calculated and shown in Table 4-10.

Table 4-10: *Calculated FoMs for the symmetrical and asymmetrical QW structures, derived from the I-V values in Table 4-5.*

Wafer	*PVCR*	*IRE(%)*	*G_{RTD}(mS)*	*f_C(THz)*	*P_{MAX}(μW)*
3	2.08	8.44	9.39	0.488	303
5	1.58	4.61	10.1	0.500	342

The reduction in peak and valley currents for the asymmetrical structure (wafer 3) results in a higher PVCR, agreeing with the trends found in the literature and the analysis carried out in Chapter 3. There is also an improvement in IRE for the asymmetric structure, as ΔI and ΔV stay roughly similar whereas the bias point is reduced. It is shown in Table 4-10 that both the frequency and power output are expected to be lower for the asymmetrical structure. As the measurements were taken in the 3rd quadrant, the sub-well would border the second barrier. Further work should be done to investigate the sub-well position at different locations in the QW, and comparisons drawn. It is expected that having the sub-well at the other end of the QW will have the opposite effect on f_C and P_{MAX}, improving the characteristics of the device. A qualitative representation of the energy band diagrams is shown in Figure 4-16.

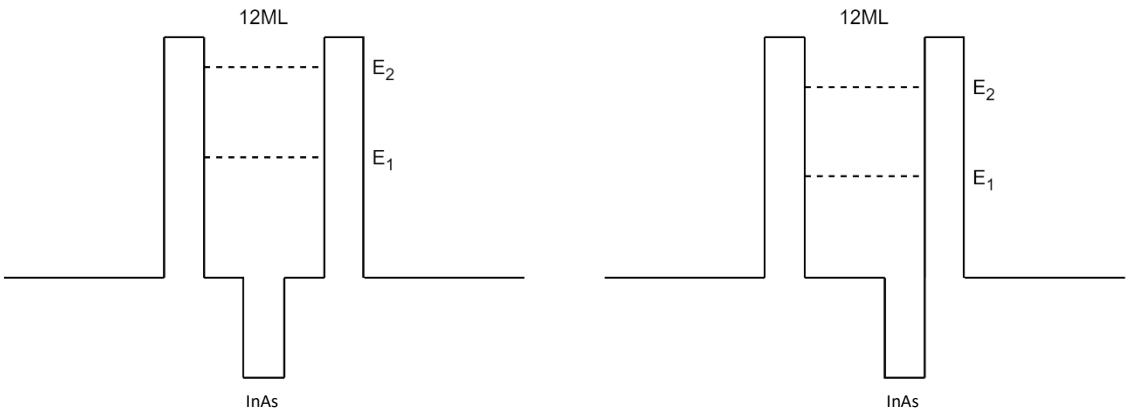

***Figure 4-16**: Estimated conduction band diagrams for the symmetric QW structure (left), and the asymmetric QW structure (right). The relative energy levels are also shown.*

In composition is the same (68.7%) for both structures. Therefore, the significant difference between J_{PK} values can only be attributed to effects of the position of the sub-well on the potential. Figure 4-16 shows the band diagrams under zero bias and at V_{PK} conditions. The change in the potential well can be seen which can explain the differences in the I-V values shown in Table 4-5.

When comparing IT to TIT, shifting the sub-well to the emitter side appears to have the same effect as lowering E_1, increasing ΔE, and decreasing the FWHM of the transmission coefficient according to the measurements taken. Given the In composition stays constant, E_1 should not be affected. V_{PK} may be lower due to scattering-assisted tunnelling caused at the interface between the 80% InGaAs and the AlAs barrier. This would also reduce the number of carriers tunnelling resonantly, which could explain the lowered J_{PK}. However, the reduced J_V suggests the scattering effects are reduced for the IT structure (or that E_2 is at a much higher level). It is also worth reiterating the possible effect of the dual-pass structure on the electrical characteristics. The second pass through the QW could lead to lower currents if it reduces the number of available states in the well. Further investigation is required here to investigate the effects of the device structure. Figure 4-17 shows the IRE vs J_{PK} plot for the sub-well devices only.

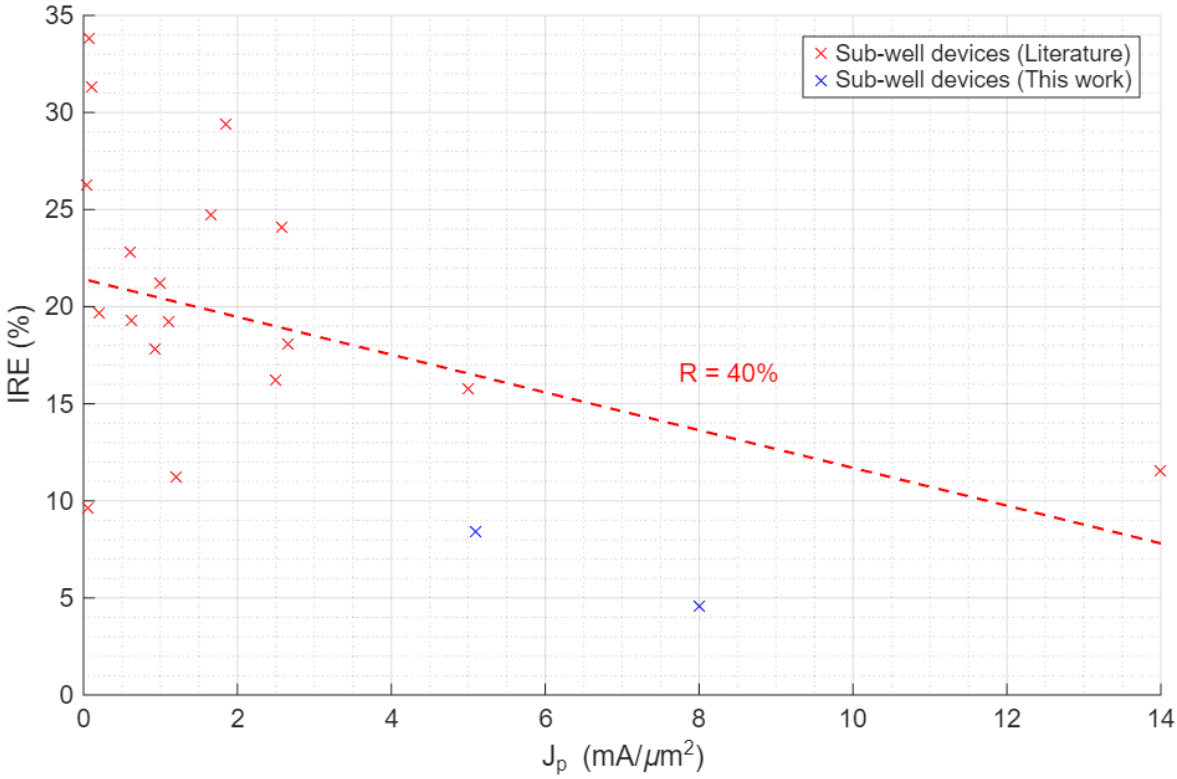

***Figure 4-17**: Plots of IRE vs (a) J_{PK} and (b) V_{PK} for sub-well structure devices. Devices in the literature are represented in red, and the devices measured in this work are in blue.*

There is a medium correlation visible between IRE and J_{PK} for the sub-well devices, with an R value of 40%. This relationship is skewed by the lack of data points at higher J_{PK} values, and so more data is required for further analysis of the exact trend. However, all the samples in the literature here feature symmetrical QW structures. The symmetrical QW device fabricated in this work has a notably lower IRE in comparison with the literature, approximately 3x smaller than the trendline would predict. The asymmetrical sample also lies below the expected literature value by a factor of ~2. However, it is noted that these two new devices do follow a similar decreasing trend to the literature values, lending more credence to the general expected behaviour of IRE against J_{PK}.

From Appendix D-7, there is no correlation found between IRE and V_{PK} (R = 0%). This suggests that in practice, the V_{PK} has no direct bearing on the IRE, most likely due to the more dominant effects of other variables, and the dependency of these variables on each other.

As the IRE has been chosen as a key FoM for RTDs here, the final comparison of the devices fabricated here is to measure it against PVCR, as seen in Figure

4-18. On this plot of IRE vs PVCR, there is a general positive correlation in the literature although a lot of variation around the trendline, giving an R value of 45%. However, for the devices fabricated in this work, shown in blue, the correlation is much stronger (R = 99%). This shows the benefits of a systematic study into the epitaxial design of RTDs. The 3.52nm ternary QW device featured the highest values for IRE and PVCR, approximately double the values for the next device, the asymmetrical sub-well structure. Then came the 3.52nm TIT structure, followed by the 4.5nm TIT structure, and finally the 4.5nm T structure. This suggests the 3.52nm structures provide better results than the 4.5nm ones, however the In composition provides no clear trend here. It is also notable that the trend is steeper than that shown for the literature, suggesting the devices in this work represent a general improvement in IRE performance.

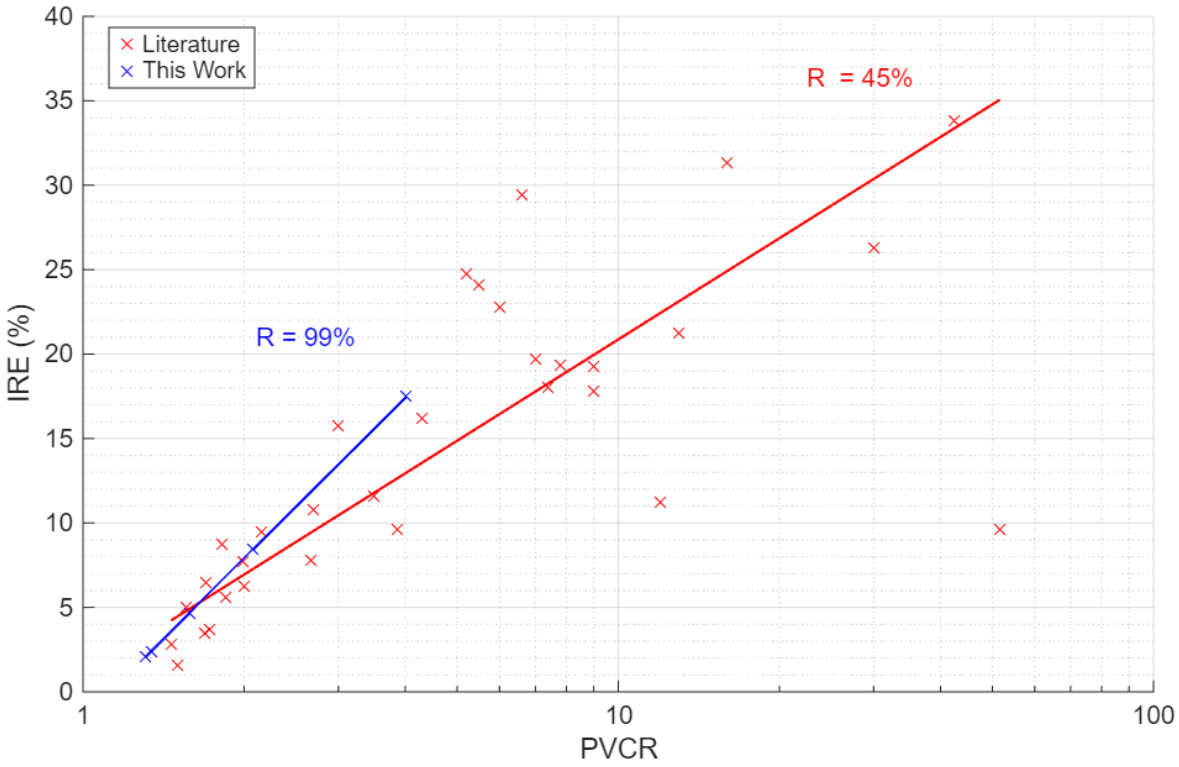

***Figure 4-18**: Graph of IRE against PVCR. Data from the literature is shown in red, while the work done here is shown in blue. Theil-Sen fitted lines have been plotted for each case.*

Figure 4-18 demonstrates the advantages of a systematic approach clearly. By removing sources of error from different device structures and fabrication processes, a much clearer relationship can be found, and therefore more reliable conclusions can be drawn. The strong IRE relationship with PVCR (and hence, J_{PK}),

suggests the IRE can be utilised as a FoM to the same extent, and, from its definition as a measure of efficiency of the RTD resonator device, is a more intuitive statistic to obtain.

It can be seen from Figure 4-18 that to optimise the IRE (and hence, PVCR), narrow well width and high In composition ternary QWs are the way to go. In this work, the 3.52nm, 85% In device provided an IRE of 17.5% and a PVCR of 4.02. Future work should investigate narrower QWs (<3nm), and increased In compositions (90%) as well as looking at barrier widths, both narrower and wider, and investigating their effect on the IRE. A possible list of experiments is given in Table 4-11. However, there are epitaxial limitations which must also be considered, as discussed in [86], as the layers must be strain-balanced during the growth process. This requires further analyses before wafers with these structures should be grown.

***Table 4-11**: Parameters of potential future experiments with the aim of maximising IRE.*

Experiment	Well width (nm)	In comp (%)	Barrier width (nm)
1. QW width	3, 3.25, 3.52	85	1.1
2. In Comp	3.52	85, 87.5, 90	1.1
3. Barrier Width	3.52	85	0.9, 1.1, 1.3

Another path to explore is the asymmetrical QW which gave the second-highest IRE and PVCR figures in this work. An investigation into the effect of the dual-pass structure on these devices should be done, by also fabricating devices with a single-pass structure, such as the one in [119] and comparing the electrical characteristics. In addition to this, an analysis of the effect of the position of the sub-well at the other side of the QW is worth exploring.

4.6 Conclusions & Future Work

Within this chapter, a systematic study of several epitaxial structural parameters of RTDs has been performed. By examining the literature, the need for a systematic study was evident - to establish the exact effects of changes in the device epitaxy. By comparing changes to well width, In composition, QW structure and the well symmetry, the I-V characteristics (and hence, the power output) can be optimised depending on the needs of the user.

It was found that a lower QW width will increase both IRE and PVCR. However, as only two well widths were used in this work, further work is needed to fully optimise the structure. The well width should be lowered until the maximum IRE can be found. In terms of the In composition, the results showed no correlation to IRE and PVCR. Further investigations could be done, comparing devices with the same QW structure and well width to verify whether this is the case, however from this work, other variables appear to have a greater impact on the device characteristics.

The inclusion of an InAs sub-well was shown to have contrasting effects on the IRE and PVCR values, depending on the QW width. The ternary QW sample at 3.52nm well width gave higher values for both FoMs than the sub-well case, but the opposite was true for the 4.5nm case. For a more comprehensive study of this relationship, the In composition should be equalised for the samples under investigation. In this case the ternary samples featured notably higher values, which affects the electrical characteristics, thus obscuring the true effect of the inclusion of the sub-well. The position of the sub-well was shown to have a significant effect on the electrical characteristics. When placed on the emitter side, higher PVCR and IRE values were obtained than from a centralised sub-well. This could also benefit from a more comprehensive review, with more positions in the QW explored including on the collector side of the well. Analysis of this data will create a clearer image of the effect of the sub-well position, allowing for further optimisation of the RTD epitaxial structure. In general, more data will give greater depth to this review and will verify the conclusions reached here, as well as allowing for a more quantitative approach to be done. Accurate predictions of

device performance should be possible as more data is obtained and analysed as in Chapter 3.

A comparison of the data obtained here with simulation results from [86] was done. The experimental results showed some agreements with the trends predicted in the electrical characteristics – derived from the energy levels and transmission coefficients graphs. There were some differences encountered which, upon further experimental work, may point to improvements required in the simulation model, particularly with the sub-well structures which did not show the expected improvement over the ternary samples. In addition, the predicted IRE values varied by less than 1% across all the samples. However, real IRE values ranged from 2.09% to 17.5%, suggesting the values obtained from the simulation require further refinement. Finally, the graph of PVCR vs IRE demonstrated the benefits of a systematic analysis, with the data from this work showing a much stronger (98%) correlation compared to that calculated from the literature values (20%).

Combining the results of this systematic analysis with results obtained from wafer characterisation techniques such as PL spectroscopy, will allow the quantitative effects of device structure on the band structure to be obtained. This will contribute to the desired capability to predict RTD performance and aid design of such devices. If specific values of FoMs can be targeted, and achieved, with a reliable fabrication and characterisation process, RTDs will become more accessible for mass production in THz emitters. Part of achieving this prediction capability is to evaluate the reproducibility and reliability of RTD devices. Therefore, full Gage Repeatability and Reproducibility (GR&R) analysis is required. Current processes for producing RTDs exhibit a large variation in device performance, evidenced by the work done in the literature. In the future, a full process must be designed which can produce RTDs with the same characteristics on subsequent process runs.

For further optimisation of the epitaxial structure, there are several other variables which would benefit from a systematic analysis. The doping concentration of both the contact and current path layers could be investigated. The contact layer has a direct impact on the contact resistance, and the current

path layer doping affects the current flowing through the device. The width of the sub-well layer relative to the QW is another parameter which requires investigation, as it is expected to be analogous to the In composition in a ternary well, but verification of this is required. Comparison of identical epitaxial dimensions on different materials also warrants investigating. There have been many advances in the development of GaN-based RTDs, and by comparing the electrical characteristics systematically, a suitable comparison of the two material systems can be done.

By systematically comparing different epitaxial parameters, the work in this chapter shows that optimisation of RTDs can be done with respect to the IRE value. Further work is required to fully optimise these devices; however, it is hoped that the work done here can contribute to realising RTDs in practical applications.

Chapter 5 : Conclusions

5.1 Summary

In this thesis, steps are taken toward the optimisation of RTD devices for future mass production in THz applications. As we approach 6G and 7G, new technologies are required to provide the bandwidths and data rates required, and RTDs are a key part to achieving that. If RTDs are to be integrated across a wide range of applications, an efficient fabrication process is required. Furthermore, the device epitaxial structure requires optimisation, and further analysis is required so that devices can be designed and fabricated accurately to meet specific FoMs. This context and the historical review of RTD devices is detailed in Chapter 1.

In Chapter 2, the details of the development of the fabrication process are given. The motivation behind the choice of the dual-pass structure is detailed, aiming to keep the fabrication process as simple as possible without sacrificing the quality of the device made. The contact resistance of the device is investigated, with three main factors – surface preparation, choice of metals, and annealing – explored to minimise the specific contact resistivity, ρ_c. Then, the three main steps in the fabrication process are described. The first metallisation step features cleaning of the device surface, then photolithography to transfer the device pattern, and finally metal deposition and lift-off. The second step is the shallow etch – this features an etch down below the active device region and establishes a path for the current to flow. The third, and final, step is the deep etch, which includes initial photolithography to protect the RTD area from the etchant, and then an etch down to the InP layer to isolate the device contacts and

also create the air-bridge structure. Characterisation of fabricated devices with different device area is then shown, at a range of temperatures down to 13.7K.

A critical literature analysis is performed in Chapter 3, to assess the trends in RTD performance over a range of different device designs and epitaxial structures. A range of existing RTD FoMs are presented, with a focus on the electrical characteristics. The IRE is highlighted as a particularly useful FoM for comparing device performance. The I-V characteristics are analysed, and very strong correlations are found between the peak and valley current values. This explains the strong trend between peak current density and PVCR in [121]. Strong correlations are also found between the peak and valley voltages; however current and voltage values were found not to correlate. The IRE is then broken down into its constituent current and voltage parts, and these are analysed through a variety of methods to determine how the IRE could be optimised. High IRE values occur at low values of both valley current density and peak voltage. The IRE is then found to have a strong correlation with the peak current density, and hence, PVCR. Finally, the effects of the epitaxial structures on device performance from the literature are analysed. The main structural parameters considered are the barrier width, well width, In composition, and the device area. Some strong correlations are found, although the variation in results demonstrates the necessity of a systematic review.

A systematic review is then performed in Chapter 4, with four main experiments to compare the effect of device epitaxial structures on the electrical characteristics. For each experiment, several FoMs are calculated, qualitative conduction band diagrams are shown, and a comparison with the literature is done. Firstly, a comparison of ternary structures is done, with alterations in the well width and In composition. These parameters have competing effects on the electrical characteristics. Secondly, the same is done for the sub-well structures. The effect of the variation in epitaxial structure is a lot less pronounced in the sub-well case. Thirdly, a direct comparison between the ternary and sub-well structures is performed, at 3.52nm and 4.5nm well widths. Both sub-well samples exhibit higher peak and valley values for both current and voltage. Finally, an investigation into the sub-well position is done, with one structure with a centralised sub-well, and another with the sub-well aligned on the emitter side.

The centralised sub-well features higher peak and valley values in this case. Following these experiments, an overall comparison to previous simulation work [86] is done, to compare results and assess the accuracy of the predicted characteristics. Some of the trends expected from the simulation model are verified with practical devices, such as the decrease in E_1 level as the well width increases. This is shown as a reduction in V_{PK} for the characterised devices. However, other aspects of the model do not concur with the practical results obtained. The IRE values of the samples feature a much larger variation than is anticipated. Also, the asymmetrical sub-well structure is expected to feature a higher E_1, and therefore V_{PK}, however this is not true for the real devices. Therefore, further tuning of the model is required, and further systematic analysis will aid in doing this.

5.2 Future Work

There are several areas covered in this work, which represent steps toward realising RTD devices in a practical capacity. Possible next steps are detailed in this section, with regards to the fabrication process, critical literature analysis, and the device optimisation.

Firstly, a fabrication process is developed with the aim of producing RTDs in a simple and cost-effective manner. Issues with reliability and reproducibility of the process suggests that further optimisation is required – perhaps in the photolithography steps by changing the resist used, or using a different device mask, similar to the one shown in Figure 2-23. Another aspect to consider with the fabrication process is the addition of MIM structures and external circuitry in order to extract THz signals. A simple process for this is described in [47]. Following this, an investigation into antenna structures should be performed. The dielectric resonator antenna (DRA) represents a promising technology to extract THz waves from the RTD device. The current structure would lose a lot of its signal in the substrate and would require a Si lens to focus the signal out, whereas a DRA, fabricated onto the bottom of the substrate, would reduce the overall size of the device and extract more power if designed correctly.

Heating of the sample is another issue to be faced, as catastrophic failure of high current density devices can occur. The overgrowth of an Fe-doped InP layer on top of the device would improve thermal conductivity, reducing the device temperature and increasing device lifetime. A process would have to be developed to ensure the RTD device is not damaged during this process. Also, measuring of the device temperature would be required to accurately ascertain the effect of this heat sinking. This could potentially be done with a linear scan using an Atomic Force Microscopy (AFM) tool although this requires further investigation.

The critical analysis done in this work aims to investigate work done across decades of RTD research and find patterns in the electrical characteristics of these devices. This is done only for devices with the InGaAs/AlAs material system, as this is most pertinent to this thesis. Similar work should be done for other material systems, such as GaAs-based RTDs, and GaN-based RTDs. Optimisation of devices on these material systems can then be done, as well as comparisons between material systems to determine which materials are the most suitable for RTD applications. This work can also be expanded by adding the output characteristics (power and frequency) of devices with completed antenna structures. The accuracy of the IRE when applied to these outputs can be analysed, and then depending on the results, another FoM could be established for the antenna section of the device. This possible FoM, in conjunction with the IRE will give an overall FoM for RTD performance. The critical analysis could also be further verified by incorporating more systematic analyses, like the one performed in Chapter 4, allowing for accurate analysis of trends in the IRE and other FoMs. The inclusion of wafer characterisation techniques could also be done, allowing characteristics such as the QW energy levels to be included, and give another dimension to the analysis.

The systematic approach taken in Chapter 4 could be expanded to cover a number of different epitaxial structures, device designs, and material systems. To add to the work done in this thesis, more data points from more devices could be taken to confirm the relationships determined here. In addition, comparing epitaxial structures with monolayer differences in just the key parameters (well width, In composition, and sub-well position) could be done. Comparison of the electrical characteristics with the wafer characteristics obtained through

photoluminescence (PL) spectroscopy would also help our understanding of the behaviour of these devices. The fabrication of antenna structures and subsequent characterisation for these devices would also provide more data for this systematic analysis and allow us to optimise devices with actual power and frequency outputs in mind, and not just the assumptions based on electrical characteristics. The systematic approach could also be extended to the antenna design as well, to optimise the power and frequency outputs.

Device designs could be created with the aim of maximising IRE. Low current density and voltage devices are required for this, so thicker barrier, wider wells, and lower In composition devices could be investigated to validate the IRE trends with these parameters. Work could also be done to try and optimise IRE at higher values of peak current density. The outlying data points in Figure 3-7 (b) demonstrate that the plotted maximum IRE line is not fully accurate, and requires further tailoring to ensure it fits for all RTD devices.

The future work detailed here will bring RTD devices closer to becoming a mass-producible device. Although there is plenty of research conducted into improving device frequency and power outputs – which are also vital for the future of RTD devices, there is little being done to make these devices an accessible technology. Therefore, the work in this thesis is a step toward achieving this, with the hope that RTDs will be at the forefront of THz technology in the very near future.

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Appendix A – Fabrication Process

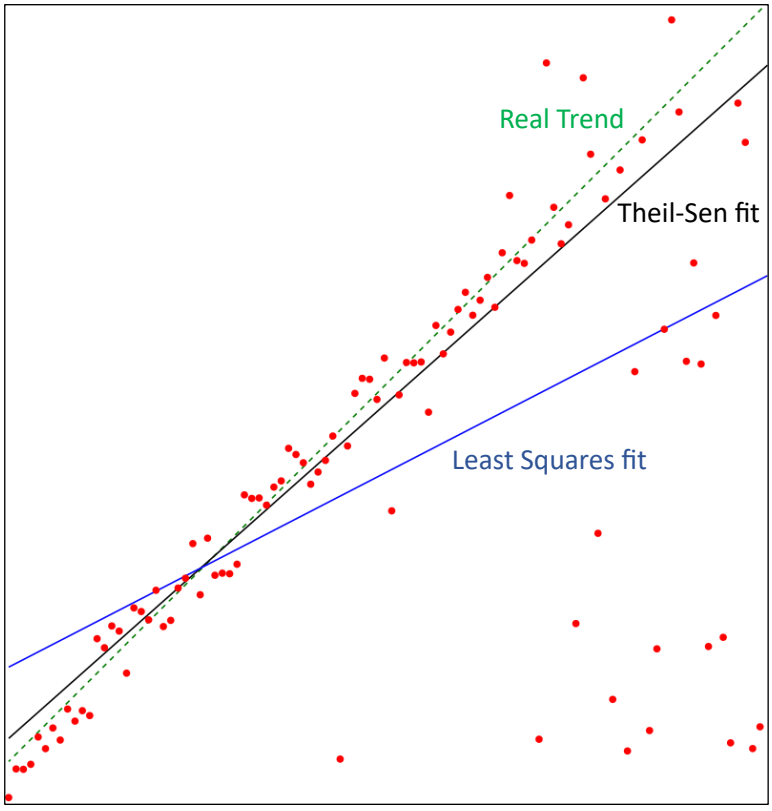
Process Module	Process Stage	Process Step	Details
1. Sample Preparation		1.1 Scribe	Rectangles, note wafer orientation
		1.2 Map	Sample Location on Wafer
		1.3 Assign Sample ID	JWNC sample database
		1.4 Solvent Clean	Acetone 5mins US, IPA 5mins US
		1.5 Dry Clean	UV/O_3 20mins, <5mm from bulb
2. Metallisation	Photoresist Patterning	2.1 Dehydration Bake	180°C for 5mins
		2.2 Resist Spin	S1818 4k rpm 30s, FT = 1.8µm, 115°C 2mins
		2.3 Exposure	Mask section "CENTRE", rotated 45° 8s
		2.4 Develop	Microposit Concentrate: RO water 1:1 40s
		2.5 Clean Developed Area	UV/O_3 10mins
	Metallisation	2.6 Metal Deposition	Ti/Au 20/200nm
		2.7 Lift-off	30mins in Microposit Remover 1165 50°C, 2mins US bath
3. Shallow Etch		3.1 Solvent Clean	Acetone 2mins US, IPA 2mins US
		3.2 Dry Clean	UV/O_3 10mins, <5mm from bulb
		3.3 Wet Etch	H_3PO_4:H_2O_2:H_2O 1:1:38 (100nm/min), Dektak, etch for 90s, Dektak
4. Deep Etch	Photoresist Patterning	4.1 Solvent Clean	Acetone 2mins, IPA 2mins
		4.2 Dry Clean	UV/O_3 10mins, <5mm from bulb
		4.3 Resist Spin	S1818 4k rpm 30s, FT = 1.8µm, 115°C 2mins
		4.4 Exposure	Mask section "DEEP ETCH", 8s
		4.5 Develop	Microposit Concentrate: RO water 1:1 40s
		4.6 Clean Developed Area	UV/O_3 10mins

	Wet Etch	4.7 Vertical Wet Etch	H_3PO_4:H_2O_2:H_2O 1:1:38 (100nm/min), Dektak, etch for 9mins, Dektak
		4.8 Lateral Wet Etch & Test	H_3PO_4:H_2O_2:H_2O 1:1:38 (100nm/min), Dektak, etch 1min, test, etch 1min, test…..
		4.9 Strip Resist	Microposit Remover 1165 30mins 50°C bath

Appendix B – Theil-Sen Regression

Theil-Sen regression uses the median of the slopes of every pair of data points to determine the slope of the fitted line. The y-intercept is also calculated as a median of the intercept values calculated using this median slope value.

This process is more robust than the typical least squares method, as outlying data does not have as large an effect on the fitted line. This is demonstrated on the example below. The blue line represents the least squares fit, the Thiel-Sen fitted line is black, and the real trendline is the dashed, green line.



Appendix C - Chapter 3 Additional Correlation Graphs

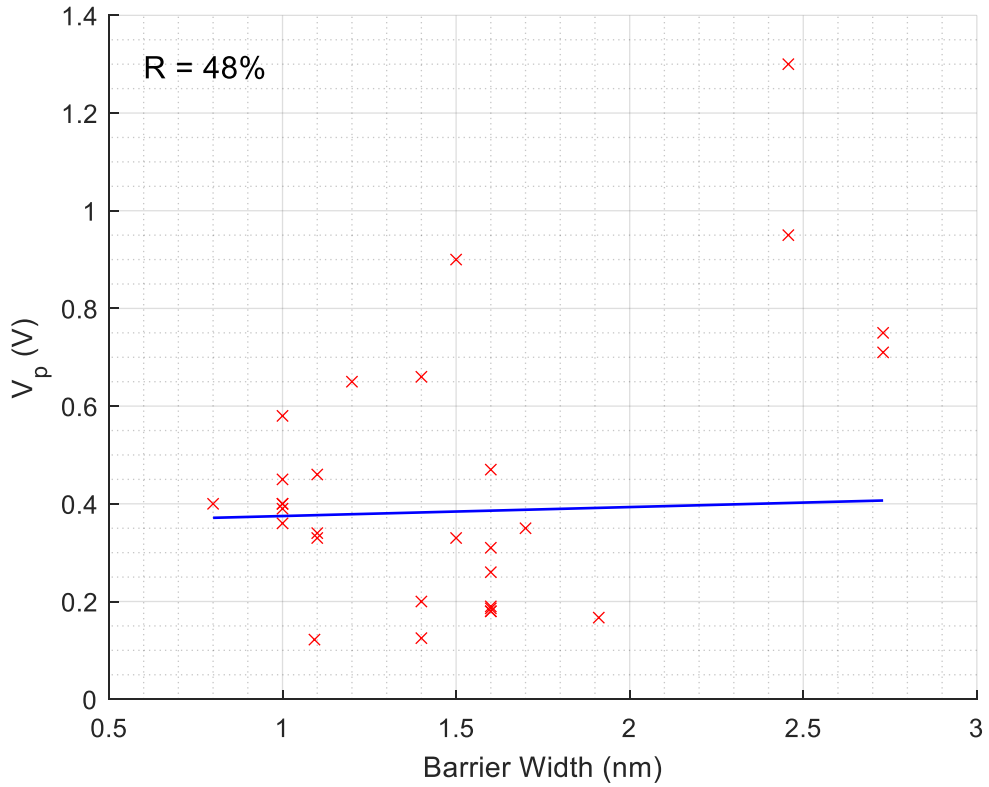


Figure C - 1: *Peak voltage plotted against barrier width for devices in the literature. The Theil-Sen fitted line is shown in blue.*

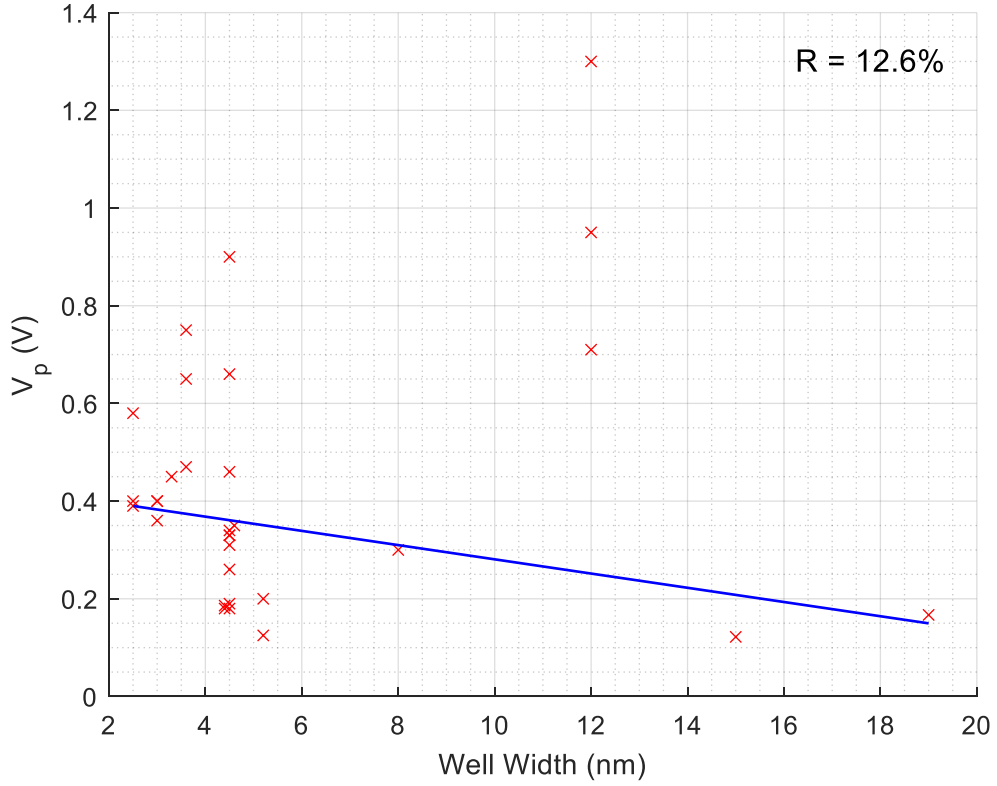


Figure C - 2: *Peak voltage against well width for devices in the literature. The Theil-Sen fitted line is shown in blue.*

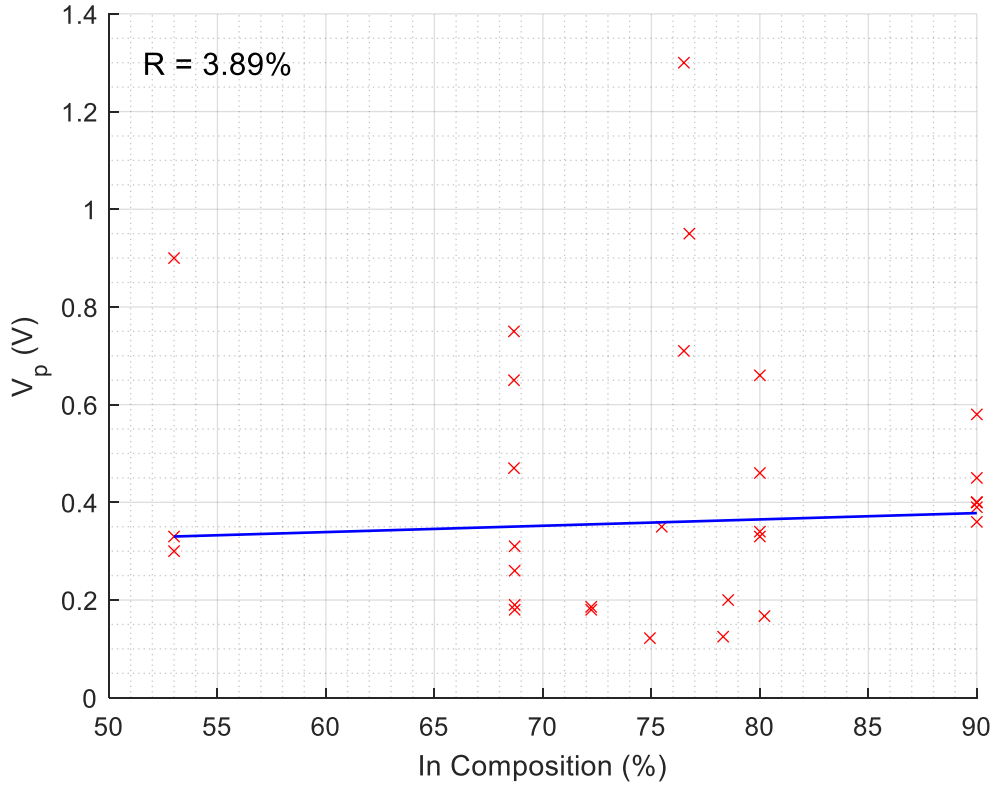


Figure C - 3: *Peak voltage against Indium composition for devices in the literature. Theil-Sen fitted line shown in blue.*

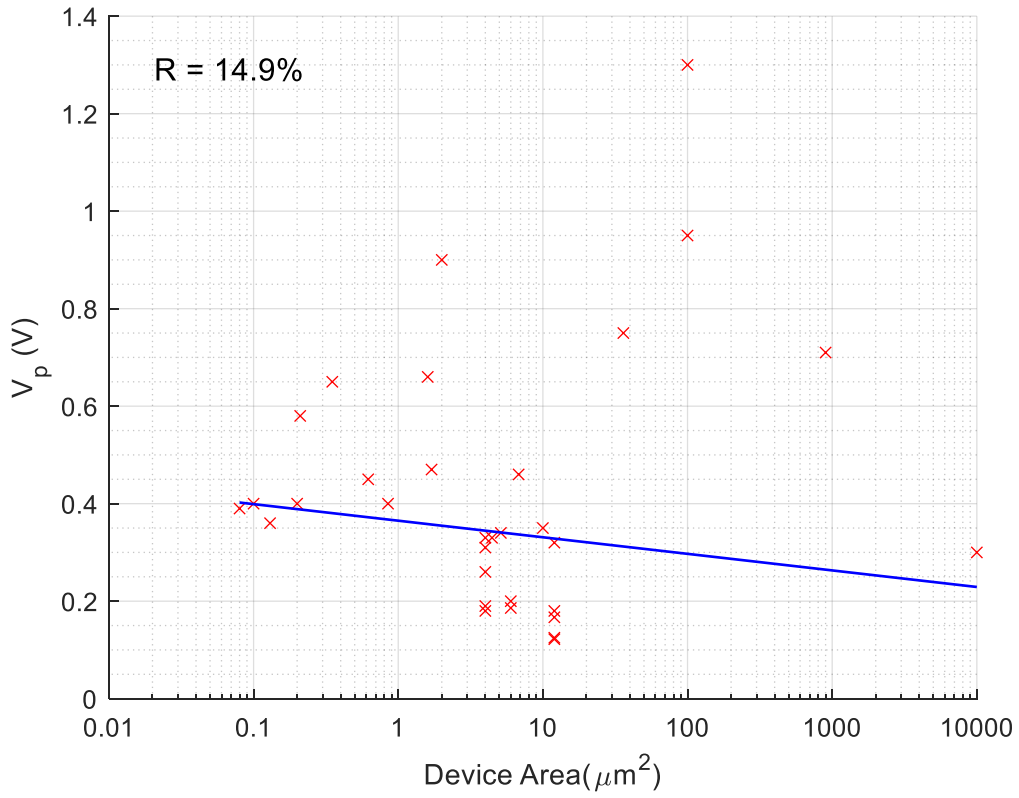


Figure C - 4*: Peak voltage against device area for devices in the literature. Theil-Sen fitted line shown in blue.*

Appendix D - Chapter 4 Additional Correlation Graphs

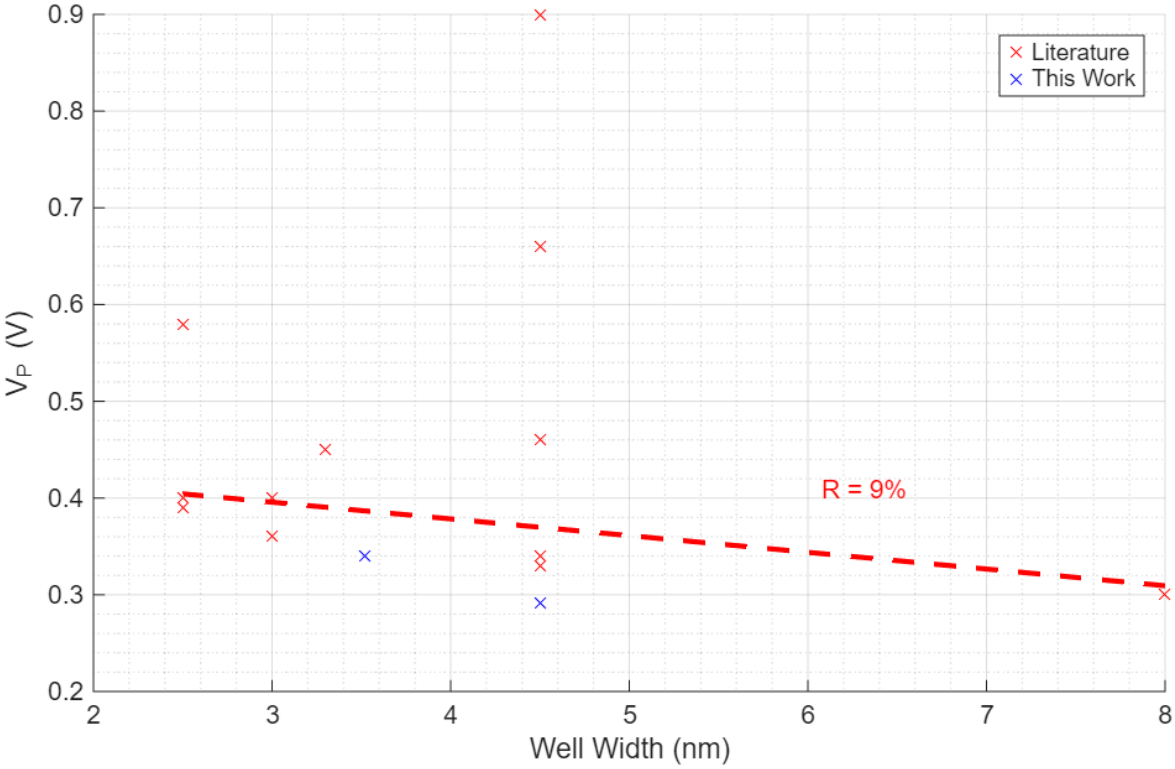


Figure D - 1: *Peak voltage against well width for ternary devices in the literature and devices fabricated in this work. A Thiel-Sen fitted line is shown in red, and the R value is shown.*

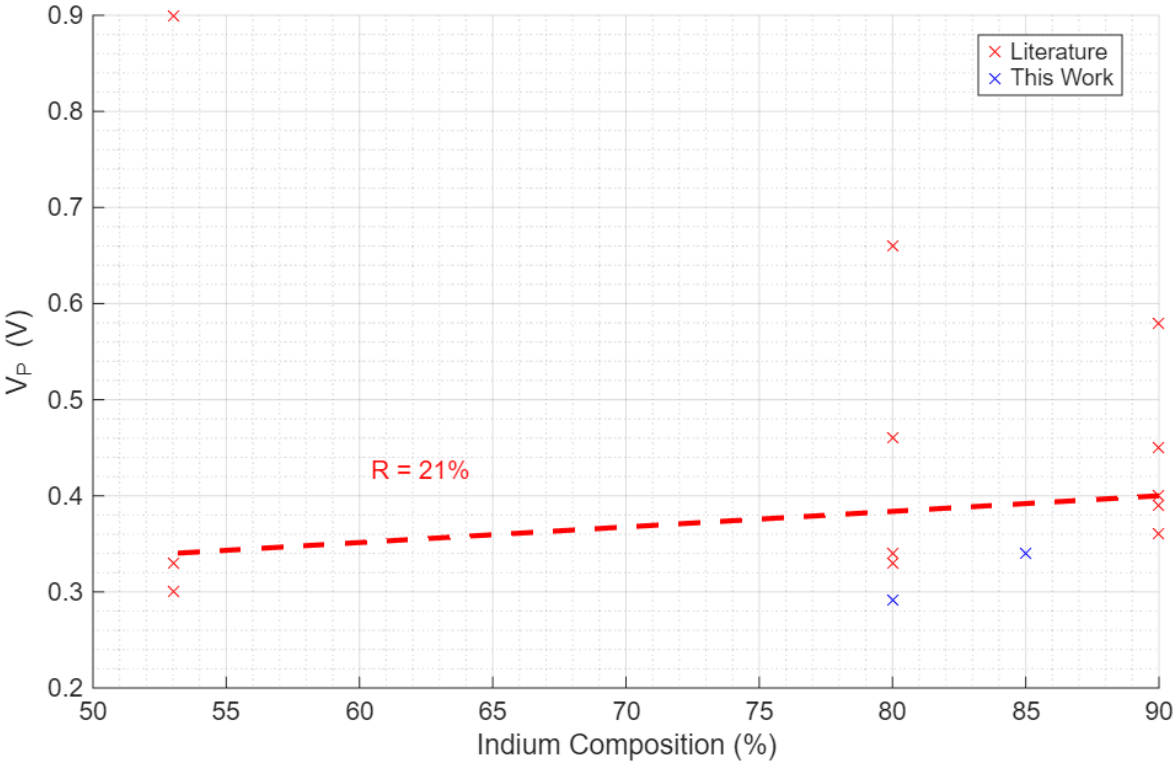


Figure D - 2: *Peak voltage against In composition for ternary devices in the literature and devices fabricated in this work. A Theil-Sen fitted line is shown in red, and the R value is shown.*

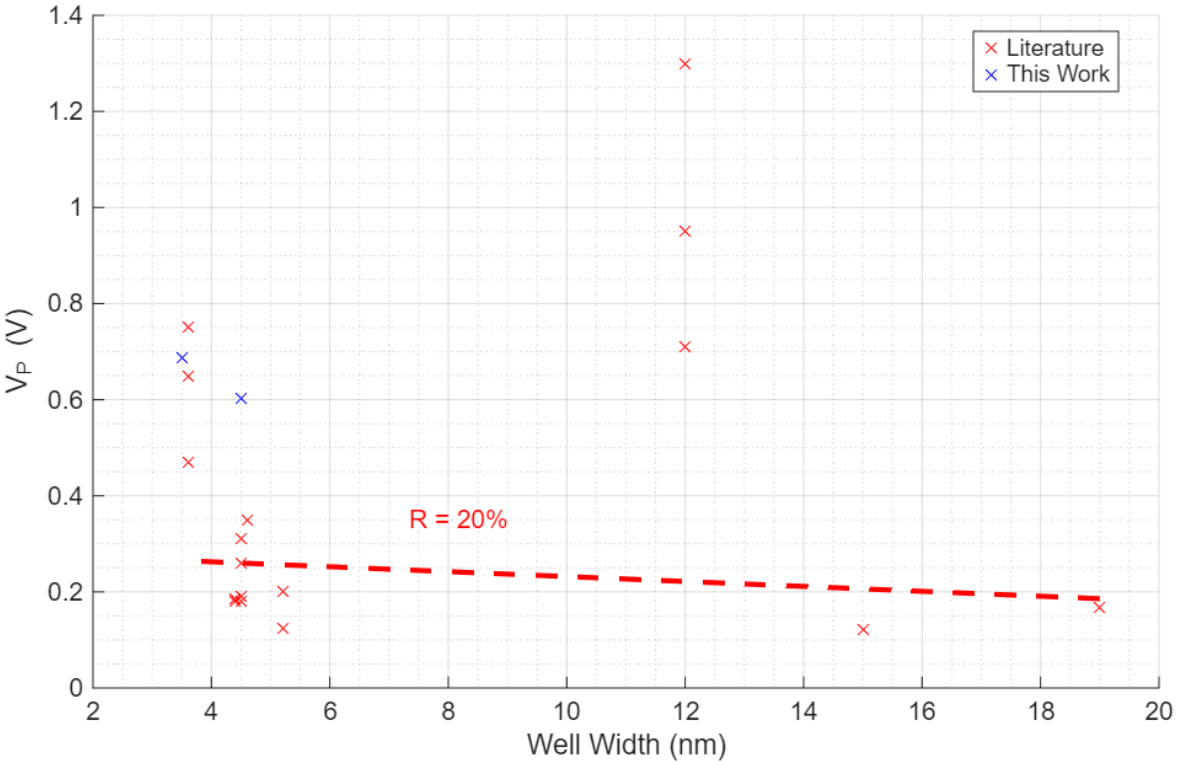


Figure D - 3: *Peak voltage against well width for sub-well devices in the literature and devices fabricated in this work. A Thiel-Sen fitted line is shown in red, and the R value is shown.*

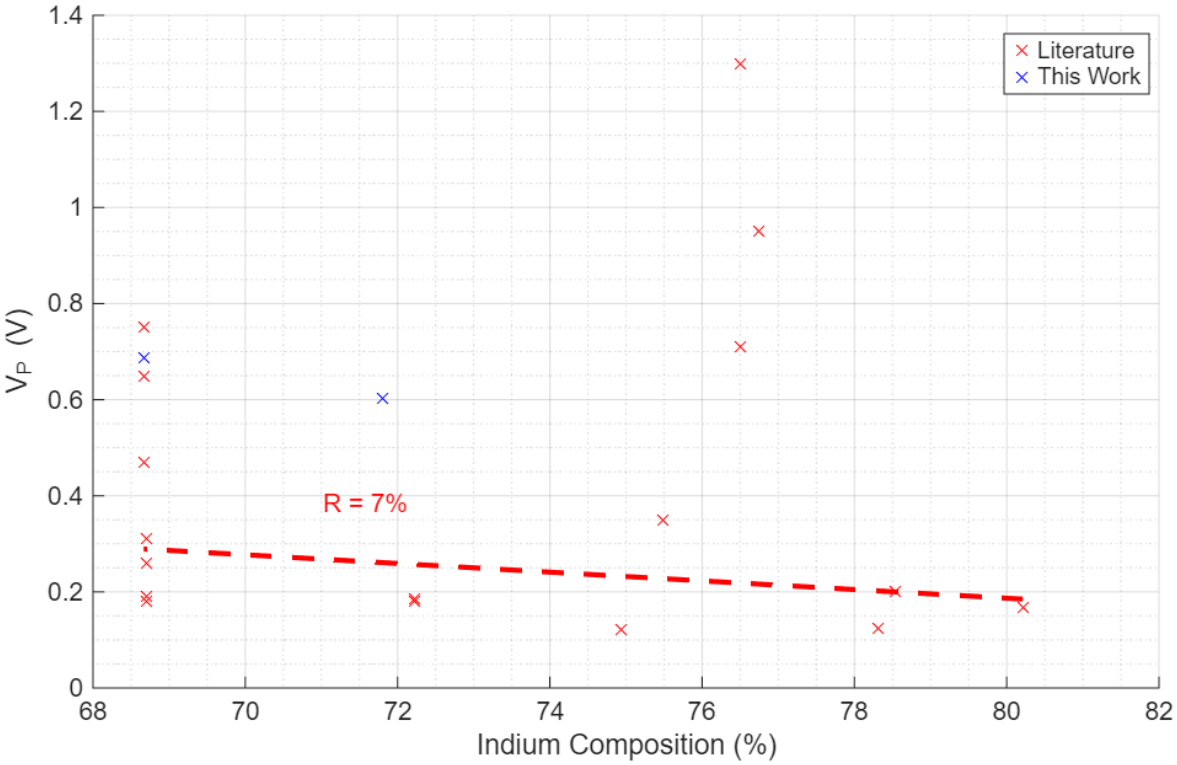


Figure D - 4: *Peak voltage against In composition for sub-well devices in the literature and devices fabricated in this work. A Thiel-Sen fitted line is shown in red, and the R value is shown.*

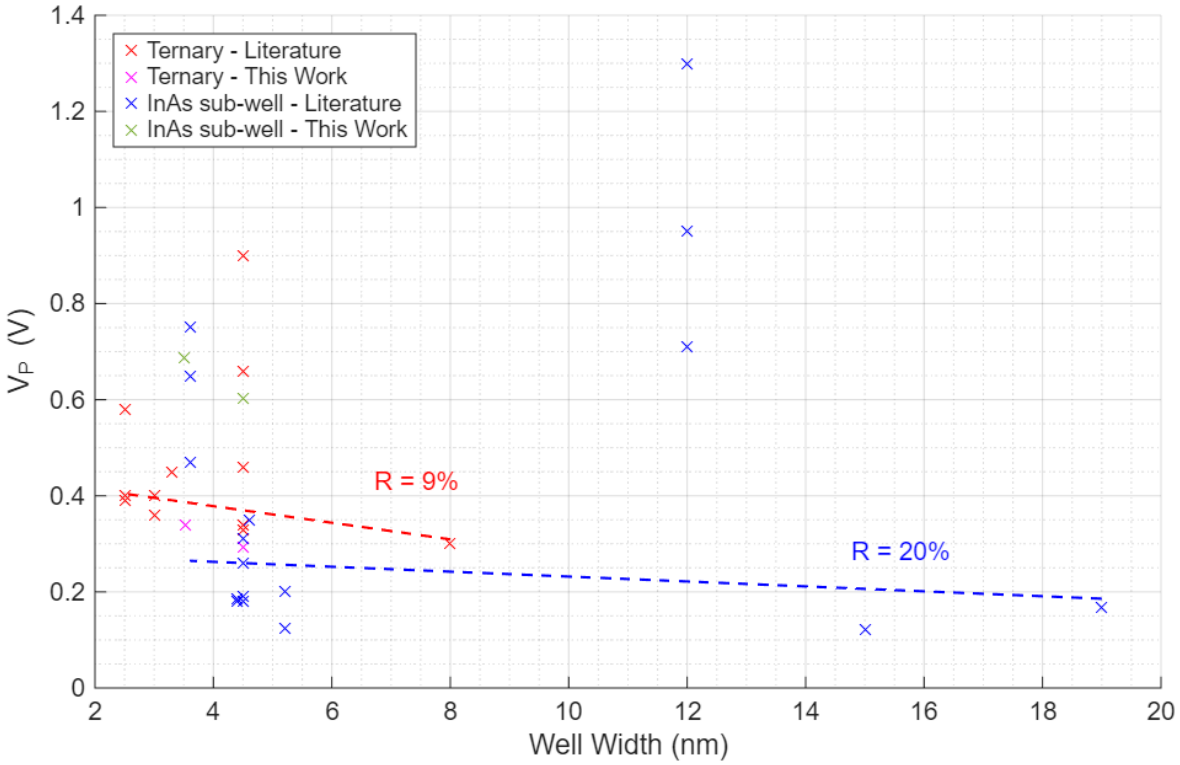


Figure D - 5: *Peak voltage against well width for ternary and sub-well devices in the literature and devices fabricated in this work. Thiel-Sen fitted lines are shown in red and blue for ternary and sub-well devices respectively, and the R values are shown.*

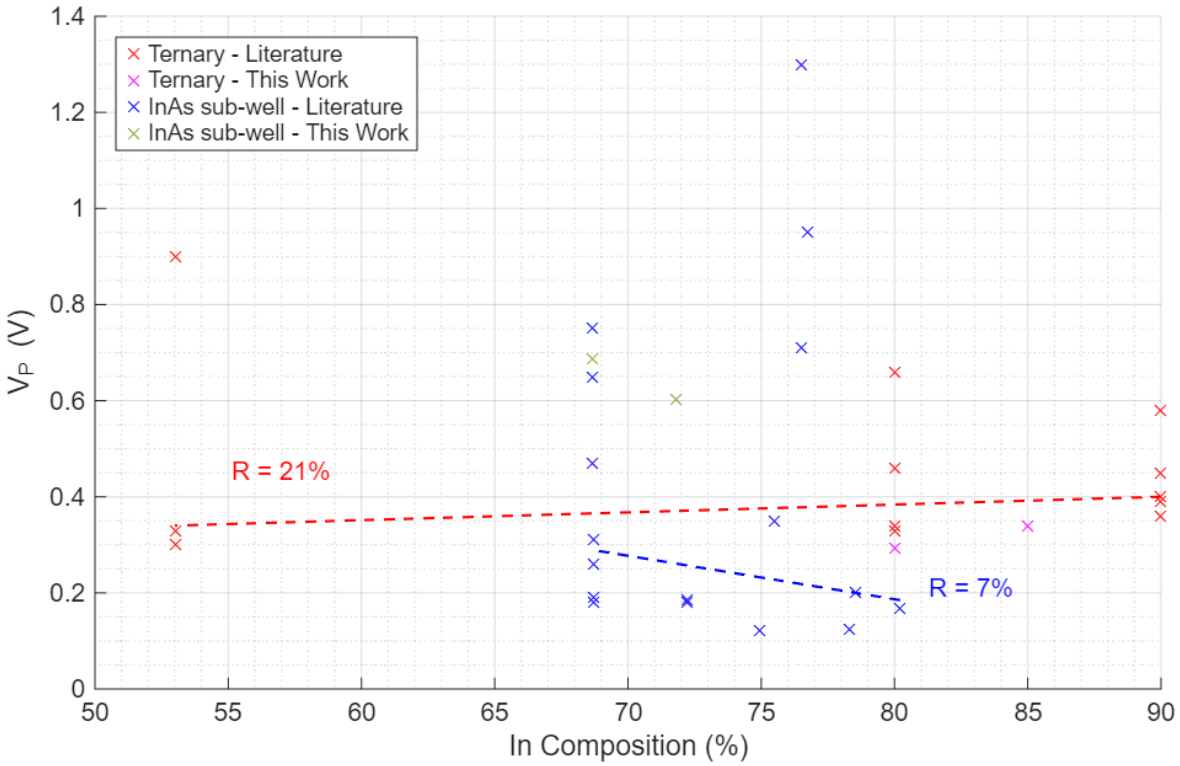


Figure D - 6: *Peak voltage against In composition for ternary and sub-well devices in the literature and devices fabricated in this work. Thiel-Sen fitted lines are shown in red and blue for ternary and sub-well devices respectively, and the R values are shown.*

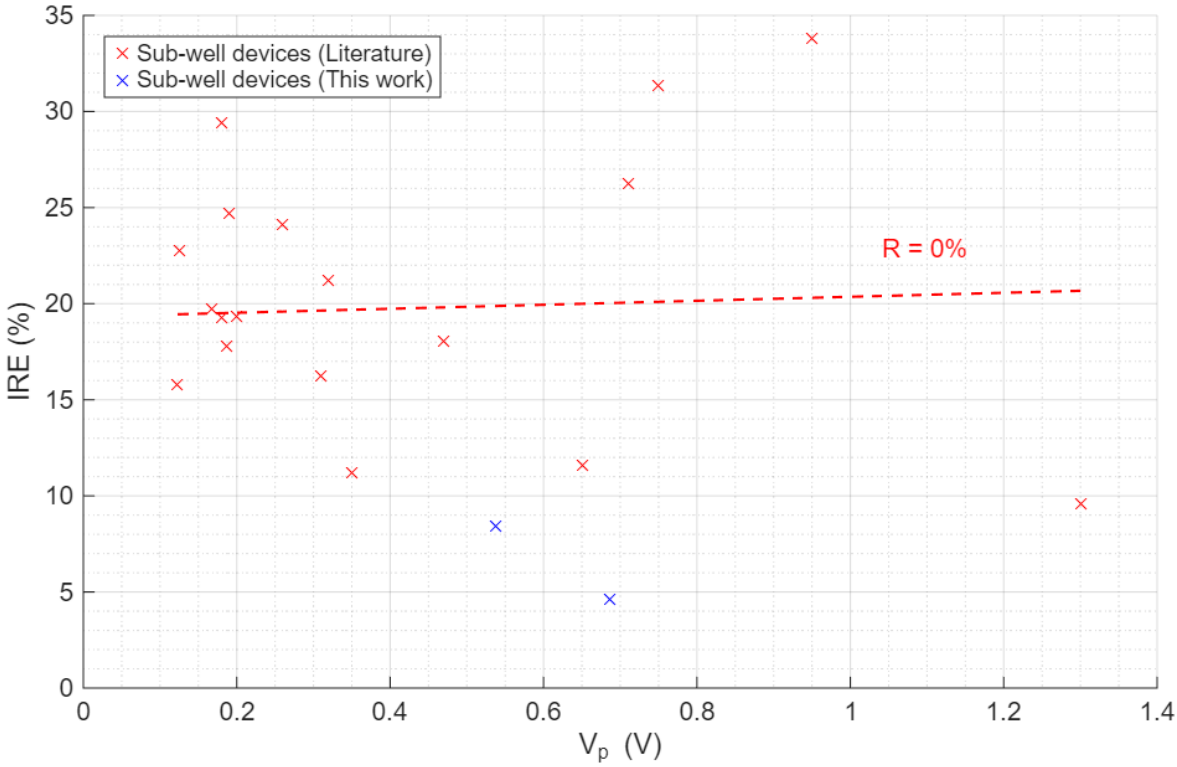


Figure D - 7: *IRE against peak voltage for sub-well structures in the literature and devices fabricated in this work. A Thiel-Sen fitted line is shown in red, and the R value shown.*