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Development of Low-Resistance Ohmic Contacts in GaN Heterostructures Using Silicon Ion Implantation

by

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A thesis submitted in fulfilment of the requirements for the degree of

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Abstract

The formation of low-resistance Ohmic contacts remains an important consideration in the development of III-nitride electronic devices. This thesis investigates approaches for reducing Ohmic contact resistance (R_c) in AlGaN/GaN and AlN/GaN heterostructures, with particular emphasis on patterned recessed Ohmic contacts, silicon (Si) ion implantation, and the relative positioning of the recess and Ohmic metallisation.

The first experimental study investigated the influence of recess patterning on Ohmic contact resistance. Localised recess patterns with dimensions of $4\ \mu m \times 150\ \mu m$ *and* $4\ \mu m \times 10\ \mu m$ were compared with a conventional planar contact without recess etching. The localised recess patterns did not provide an improvement in contact resistance compared with the conventional planar contact, which produced the lowest contact resistance of 0.81 Ω·mm among the structures investigated. These results demonstrate that, under the processing conditions used in this work, the introduction of the investigated localised recess patterns did not improve the Ohmic contact resistance

Si ion implantation was subsequently investigated as an approach for reducing Ohmic contact resistance. Blanket Si implantation was applied to GaN/AlGaN/GaN and AlN/GaN heterostructures, followed by high temperature activation and Ohmic contact formation. Low contact resistances were obtained from the implanted structures, with the implanted AlGaN/GaN heterostructure achieving R_c values of approximately $0.10–0.14\ \Omega \cdot$ mm without post metallisation annealing. For the implanted AlN/GaN heterostructure, a minimum R_c of $0.46\ \Omega \cdot$ mm was obtained following post metallisation annealing at 800 °C for 30 s. The effects of implantation activation, surface encapsulation and post metallisation annealing were also investigated as part of the process development.

Building on the blanket implantation study, a selective area Si ion implantation process was developed to enable implantation to be confined to defined Ohmic contact regions. The process was applied to an available n-doped GaN capped AlN/GaN heterostructure, allowing implanted and un-implanted regions to be directly compared on the same sample. The implanted region exhibited a contact resistance of $0.14\ \Omega \cdot$ mm, compared with $0.30\ \Omega \cdot$ mm in the un-implanted region, corresponding to a reduction of approximately 53.5%. The corresponding sheet resistance decreased from 750 to 119 Ω/□. These results demonstrate

the reduction in Ohmic contact resistance achieved through Si ion implantation and the applicability of selective area implantation to device fabrication.

The final experimental study investigated the influence of recess-to-metallisation positioning on Ohmic contact resistance using aligned, overlap and gap designs. Overlap and gap distances of 2, 3 and 5 μm were investigated. Increasing the recess-to-metallisation overlap progressively reduced the extracted contact resistance, with the 5 μm overlap producing the lowest R_c of $0.95\ \Omega \cdot \mathrm{mm}$ among the investigated designs. In contrast, introducing a gap between the recessed and metallised regions resulted in a substantial increase in contact resistance. An optimum overlap distance was not established, as R_c continued to decrease up to the maximum investigated overlap of 5 μm.

Overall, the results demonstrate that Ohmic contact resistance in III-nitride heterostructures is strongly influenced by recess patterning, Si ion implantation and recess-to-metallisation positioning. In particular, the ion implantation studies demonstrate the effectiveness of this approach for achieving low-resistance Ohmic contacts, while the development of selective-area implantation demonstrates how the implantation process can be confined to defined contact regions for integration into device fabrication. The recess studies further highlight the importance of the extent of recessing and the positioning of the Ohmic metallisation relative to the recessed region. Together, these findings contribute to the development and understanding of fabrication approaches for achieving low-resistance Ohmic contacts in III-nitride electronic devices.

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List of Publications

1. J. I. Iloke, A. Ofiare, S. Hassan and E. Wasige, *'Development of Low-Resistance Ohmic Contacts on AlN/GaN Heterostructures Using Si Ion Implantation'*, UK Semiconductors 2025, Sheffield UK, 2 – 3 July 2025

2. J. I. Iloke, A. Ofiare, A. Al-Khalidi and E. Wasige. '*Towards Low Resistance Contacts for Millimetre-wave AlGaN/GaN HEMTs Through Transfer-Length Patterning*' UK Semiconductors 2024, Sheffield UK, 8 – 9 July 2024

3. S. Hassan, Z. Cheng, J. I. Iloke, A. Al-Khalidi, and E. Wasige, *'Vertical GaN FinFET with Linearly Doped Drift Layer for High-Power Switching Applications'*. UK Semiconductors 2024, Sheffield UK, 8 – 9 July 2024.

4. S. Hassan, Z. Cheng, J. I. Iloke, A. Al-Khalidi, and E. Wasige, '*Electrostatic Control and Breakdown Enhancement in a Gate-Enclosed Vertical GaN FinFET: A TCAD Study*', UK Semiconductors 2025, Sheffield UK, 2 – 3 July 2025

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Author's Declaration

University of Glasgow

College of Science and Engineering

Statement of Originality to Accompany Thesis Submission

Name: Joel Idor Iloke

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I certify that the thesis presented here for examination for a PhD degree of the University of Glasgow is solely my own work other than where I have clearly indicated that it is the work of others (in which case the extent of any work carried out jointly by me and any other person is clearly identified in it) and that the thesis has not been edited by a third party beyond what is permitted by the University's PGR Code of Practice.

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I acknowledge that if any issues are raised regarding good research practice based on review of the thesis, the examination may be postponed pending the outcome of any investigation of the issues.

Signature: Joel Idor Iloke

Date: 24 September 2026

Abbreviations

2DEG	Two-Dimensional Electron Gas
2DHG	Two-Dimensional Hole Gas
AFM	Atomic Force Microscopy
Al	Aluminium
AlGaN	Aluminium Gallium Nitride
AlN	Aluminium Nitride
Ar	Argon
Au	Gold
BCl_3	Boron Trichloride
Cl_2	Chlorine
CTLM	Circular Transmission Line Model
CVD	Chemical Vapour Deposition
DC	Direct Current
e-beam	Electron Beam
EBPG	Electron Beam Pattern Generator
E_C	Conduction Band Energy
E_f	Fermi Level Energy
E_g	Bandgap Energy
f_{max}	Maximum Oscillation Frequency
f_t	Unity Current Gain Cut-off Frequency
Ga	Gallium
GaAs	Gallium Arsenide
GaN	Gallium Nitride
GHz	Gigahertz
g_m	Transconductance

H_2O	Water
HEMT	High Electron Mobility Transistor
HF	Hydrofluoric Acid
HVPE	Hydride Vapour Phase Epitaxy
ICP	Inductively Coupled Plasma
InAlN	Indium Aluminium Nitride
InP	Indium Phosphide
IPA	Isopropyl Alcohol
I–V	Current–Voltage
JWNC	James Watt Nanofabrication Centre
k	Thermal Conductivity
LED	Light Emitting Diode
L_G	Gate Length
L_{GD}	Gate–Drain Distance
L_{GS}	Gate–Source Distance
LOR	Lift-Off Resist
L_{SD}	Source–Drain Distance
L_T	Transfer Length
LTLM	Linear Transmission Line Model
MBE	Molecular Beam Epitaxy
MIBK	Methyl Isobutyl Ketone
MMIC	Monolithic Microwave Integrated Circuit
MOCVD	Metal Organic Chemical Vapour Deposition
N_2	Nitrogen
Ni	Nickel
n_s	Sheet Carrier Concentration
PECVD	Plasma Enhanced Chemical Vapour Deposition

PMMA	Polymethyl methacrylate
P_{PE}	Piezoelectric Polarisation
P_{SP}	Spontaneous Polarisation
q	Electron Charge
R_c	Ohmic Contact Resistance
RF	Radio Frequency
RIE	Reactive Ion Etching
RO	Reverse Osmosis
R_{sh}	Sheet Resistance
RTA	Rapid Thermal Annealing
SEM	Scanning Electron Microscope
Si	Silicon
SiC	Silicon Carbide
SiN_x	Silicon Nitride
SiO_2	Silicon Dioxide
TEM	Transmission Electron Microscope
Ti	Titanium
TiN	Titanium Nitride
TLM	Transmission Line Model
V_{BR}	Breakdown Voltage
V_{DS}	Drain–Source Voltage
v_{eff}	Effective Electron Velocity
V_{GS}	Gate–Source Voltage
V_P	Pinch-Off Voltage
v_{sat}	Saturated Electron Velocity
V_T	Threshold Voltage
W_g	Gate Width

ε	Absolute Permittivity
ε_o	Vacuum Permittivity
ε_r	Relative Permittivity
μ_n	Electron Mobility
Φ_b	Schottky Barrier
σ	Polarisation Charge

1 Introduction

1.1 Overview

Due to rapid advancements in wireless communication technologies and the growing demand for higher data rates, improved reliability, and reduced power consumption, there is increasing pressure on the already congested lower gigahertz frequency bands. As a result, future generations of wireless systems are expected to shift towards the millimetre-wave (mmWave) frequency range, typically defined between 30 GHz and 300 GHz. This spectrum offers significantly more available bandwidth, making it a promising candidate for meeting the performance requirements of emerging applications [1],[2]. Figure 1.1 illustrates the spectrum allocations for 4G, 5G, and the emerging 6G technologies, highlighting the progressive move toward higher frequencies [3]. The mmWave band is currently under active investigation for a wide range of applications, including next generation cellular networks, satellite communications, radar systems, and other high speed wireless technologies.

Silicon (Si) has traditionally been the cornerstone of the semiconductor industry, because of its availability, low production cost, and the extensive research and development it has received over the years. However, as the demand for higher frequency and high power electronic applications continue to grow, Si is approaching its limits in terms of power handling capability, switching speed, and maximum operating temperature. These limitations have created a need for alternative materials. Wide bandgap semiconductors such as gallium nitride (GaN), indium phosphide (InP), silicon carbide (SiC), and gallium arsenide (GaAs) have emerged as promising candidates, offering superior performance in terms of higher power density, faster switching, and enhanced thermal stability, enabling the development of more compact, efficient, and reliable electronic systems.

Table 1.1 shows a comparison of the material properties of GaN with other commonly used semiconductors such as Si, GaAs, InP, and SiC [4]. The table highlights key parameters including:

I. Energy bandgap: GaN has a wider bandgap of 3.4 eV compared to Si 1.12 eV. The wider bandgap means that more energy is required to excite electrons from the valence band into the conduction band, resulting in a much lower intrinsic carrier

concentration. Consequently, the thermal generation of charge carriers is suppressed at elevated temperatures, making GaN suitable for high temperature operation [5].

II. Electron mobility: while Si generally exhibits higher intrinsic electron mobility (~1500 cm^2/Vs) compared to bulk GaN (~900 cm^2/Vs), advances in the epitaxial growth of GaN based heterostructures, such as AlGaN/GaN, enable the formation of a high mobility two dimensional electron gas (2DEG) at the heterointerface, with electron mobilities exceeding 1500 $cm^2/V.s$ reported in GaN based high electron mobility transistors (HEMTs) [6].

III. Breakdown electric field: is a key parameter needed for high frequency and high-power applications and is directly related to the energy bandgap. Wide bandgap GaN has a higher breakdown electric field of 3.3 MV/cm compared to that of the low bandgap Si and other semiconductor devices of equal size.

IV. Thermal conductivity: The thermal conductivity of GaN (~1.3 W/cm·K) is considerably lower than that of SiC ~4 W/cm·K, but significantly higher than that of InP and GaAs, and comparable to that of Si. The relatively high thermal conductivity of GaN facilitates heat dissipation during device operation, helping to limit temperature rise and maintain device performance during high power operation.

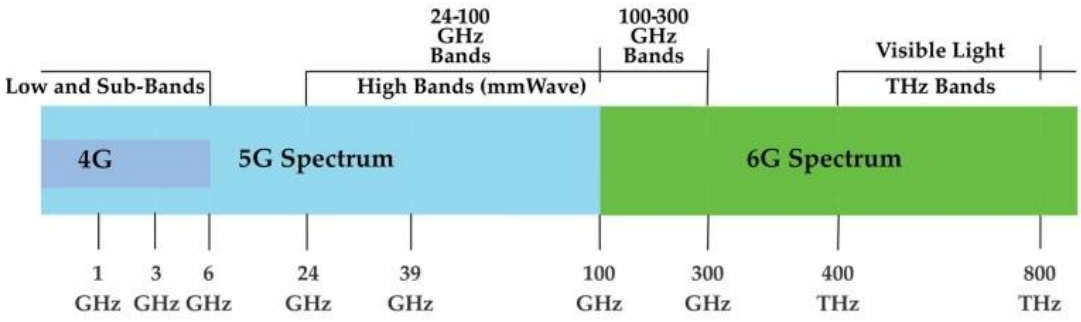


Figure 1.1 Frequency spectrum band [3].

Table 1.1 Material property comparison of GaN with other leading semiconductors.

Parameter and units	**Si**	**GaAs**	**InP**	**GaN**	**SiC**	**AlN**	**Diamond**
Energy bandgap (eV)	1.12	1.43	1.34	3.44	3.26	6.2	5.5
Thermal conductivity (W/cm. K)	1.5	0.54	0.67	1.3	4	2.85	22
Breakdown electric field (MV/cm)	0.3	0.4	0.45	3.3	3	12	10
Saturated electron velocity (10^7 cm/s)	1.0	1.0	1	2.5	2	1.7	2.7
Electron mobility μ (cm^2/Vs)	1500	8500	5400	900	700	300	4800
Relative dielectric constant (ε_r)	11.8	13.1	12,4	9.5	9.7	8.5	5.5

GaN can form heterostructures with wider bandgap materials such as aluminium gallium nitride (AlGaN) and aluminium nitride (AIN). These heterostructures result in the formation of a quantum well known as a 2DEG channel, characterised by a high electron sheet density exceeding 10^{13} cm^{-2} and high electron mobility [7]. The high carrier concentration and electron mobility, combined with other inherent properties, make GaN-based devices well suited for high power high frequency applications.

The AlGaN/GaN heterostructure is a leading material for high performance radio frequency (RF) devices. AlGaN/GaN field effect transistors have demonstrated state of the art performance achieving power densities as high as 8.7 W/mm, a current gain cut-off frequency (f_t) of 74 GHz, and a maximum oscillation frequency (f_{max}) of 140 GHz for a 150 nm gate length device [8]. Beyond the conventional AlGaN barrier, alternative heterostructures within the GaN material system have been explored, including AlN/GaN [9], AlInN/GaN [10] , and AlInGaN/GaN [11], where the AlGaN barrier layer is replaced with aluminium nitride (AlN), aluminium indium nitride (AlInN), and aluminium indium gallium nitride (AlInGaN), respectively. These variations offer potential for further optimisation of device performance.

Today, GaN based HEMTs are mainly used to realise microwave amplifiers. Figure 1.2 illustrates common application areas for GaN technology, including base stations and radar

systems, which use RF/microwave amplifiers (and MMICs), and electric vehicles, which use DC/DC converters, etc.

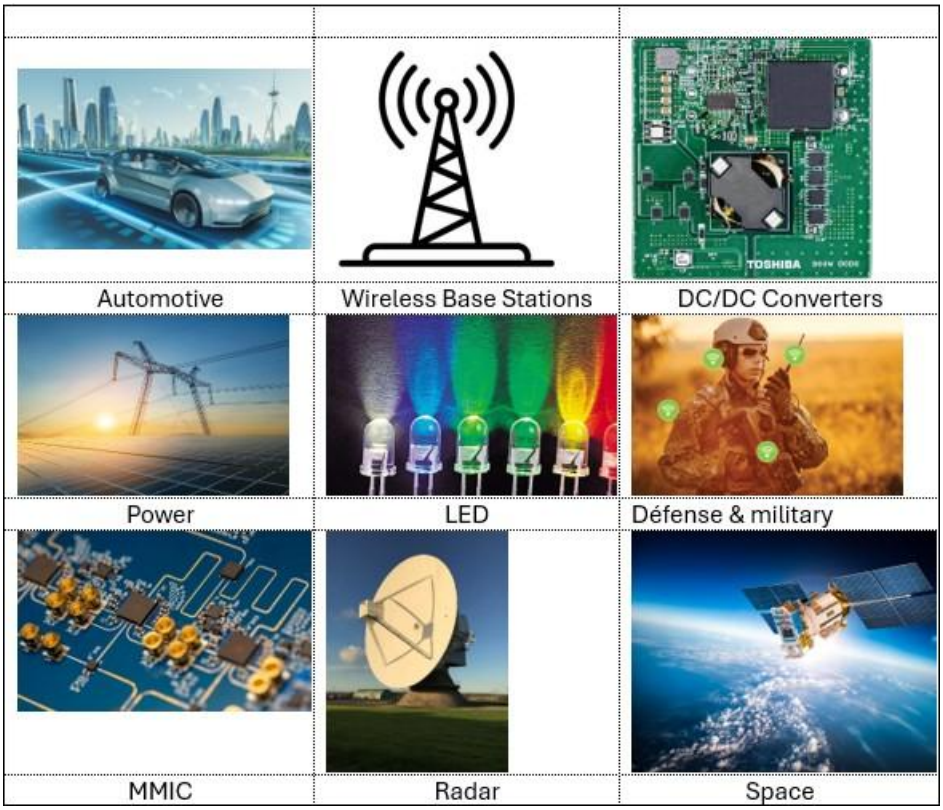


Figure 1.2 Example applications of GaN technology across RF, power, and optoelectronics.

1.2 Research Challenges

Compared to traditional semiconductor devices, GaN HEMTs offer superior energy efficiency, compact system size, and enhanced overall performance [12]. However, significant challenges remain that hinder the full realisation of its potential. Major research challenges in RF GaN HEMTs include thermal management [13], which can limit the achievable power density and device reliability, and high Ohmic contact resistances which reduce device efficiency and high frequency performance [14].

This section discusses some of these challenges and how they are addressed in this project, with a particular focus on Ohmic contact evaluation in AlN/GaN and AlGaN/GaN material systems.

1.2.1 Realisation of Low Resistance Ohmic Contacts in GaN HEMTs

The formation of low resistance Ohmic contacts is critical to the performance and reliability of GaN HEMTs. Efficient carrier injection from the metals into the semiconductor is dependent on the quality of these contacts. Consequently, the contact resistance directly affects the maximum drain current, total on resistance, and power dissipation of the device. In radio frequency applications, low Ohmic resistance is particularly important, as it enhances both the current gain cut off frequency (f_t) and the maximum frequency of oscillation (f_{max}) by reducing the source and drain series resistances.

However, achieving low resistance Ohmic contacts to GaN remains challenging due to its wide bandgap. The difficulty is even more pronounced in AlN barrier HEMTs, where the bandgap is 6.2 eV, leading to a larger Schottky barrier height at the metal semiconductor interface. The strategies for reducing Ohmic contact resistance can be divided into two categories: either lowering the barrier height, through high temperature annealing, Ohmic regrowth technique [15] and by highly doping the GaN cap layer [16] or by easing tunnelling through the barrier layer of the heterostructure, through using thin barrier layer [17] or using dry etching to reduce the barrier layer [18].

In this project, a novel technique to reduce Ohmic contact resistance in AlGaN/GaN HEMTs was explored. The method involved implementing an uneven, patterned interface within the transfer length region of the contacts. Specifically, dry etching was used to form horizontally recessed regions that extends beyond the 2DEG prior to metallisation. This is further described and discussed in chapter 4.

1.2.2 Ion Implantation for Low Resistance Ohmic Contacts

Ion implantation is one of the methods which can be used to selectively dope a semiconductor material with impurity atoms to manipulate its electrical conductivity. Ion implantation also provides precise control over the dopant concentration and depth profile, making it possible to obtain a variety of doping profiles [13]. Due to its low activation energy, Si is the most used donor dopant in GaN. Selective area Si ion implantation can be used to improve ohmic contacts by creating a heavily doped GaN surface to enhance carrier tunnelling.

Nevertheless, during ion implantation, energetic ions are introduced into the material at relatively high energies, causing substantial damage to the crystal lattice through the displacement of atoms from their lattice sites. Consequently, high-temperature post-implantation annealing is required to recover the implantation-induced lattice damage and electrically activate the implanted dopants. However, the high temperatures required for this process can cause degradation of the GaN surface, which may adversely affect device performance [19]. This presents an additional challenge in the ion implantation process and necessitates the use of an encapsulation layer to protect the GaN surface and preserve its material quality during post-implantation annealing.

Relatively few studies have demonstrated the integration of ion implantation with GaN-based HEMT fabrication. In this project, the implantation and post-implantation processes were systematically optimised to enhance dopant activation, suppress surface degradation, and successfully integrate ion implantation as a means of reducing Ohmic contact resistance in AlN/GaN and AlGaN/GaN HEMT devices.

1.2.3 Investigation of Recess – Metallisation Geometry on Contact Resistance

Recess etching of the barrier layer is an effective technique for reducing contact resistance in GaN-based HEMTs by thinning or removing the barrier between the metallisation and the 2DEG [20]. In addition to the recess depth and process conditions, the overlap geometry between the recessed region and the Ohmic metallisation plays a crucial role in determining device performance. Depending on whether the metallisation extends beyond the recessed region, or the recess extends beyond the metallisation, the relative contributions of sidewall and planar current injection mechanisms vary, thereby influencing the contact resistance and performance of the device [20]. Despite its significance, systematic investigations of recess–metallisation overlap geometry remain limited in the literature. Therefore, in this project we investigated the influence of recess–metallisation overlap geometry on Ohmic contact resistance.

1.3 Research Aim and Objectives

The primary aim of this thesis was to investigate and evaluate approaches for reducing Ohmic contact resistance in III-nitride heterostructures through patterned ohmic contacts,

silicon ion implantation, and recess-to-metallisation alignment. To achieve this aim, the following research objectives were pursued:

I. To design, fabricate, and characterise patterned Ohmic contacts in AlGaN/GaN heterostructures and evaluate the influence of recess patterning on Ohmic contact resistance.
II. To investigate Si ion implantation as an approach for reducing Ohmic contact resistance through the fabrication and characterisation of implanted III-nitride heterostructures.
III. To develop a selective area Si ion implantation process and evaluate its influence on Ohmic contact resistance through direct comparison of implanted and un-implanted regions.
IV. Investigate the influence of recess to metallisation alignment/geometry including aligned, gap and overlap designs on Ohmic contact resistance.

1.4 Thesis Structure

This thesis is organised into 7 chapters. Chapter 1 introduces the background of GaN based technology, including a comparison with other leading semiconductor technologies. It also outlines the key research challenges, as well as the aim and objectives of the project. The remainder of the thesis is organised as follows:

- Chapter 2 provides a theoretical background on GaN HEMTs, covering polarisation effects, 2DEG formation, device structure, operating principles and high frequency behaviour. It also reviews metal–semiconductor interactions and methods for extracting contact resistance.
- Chapter 3 describes the epitaxial growth techniques for GaN HEMTs and the fabrication processes relevant to this study, including photolithography, electron-beam lithography, metallisation, thermal processing, and wet and dry etching. It also covers the DC and RF characterisation methods employed in this work.
- Chapter 4 focuses on the approaches for reducing Ohmic contact resistance. It also includes experimental investigations of patterned Ohmic contacts on an AlGaN/GaN HEMT structure.
- Chapter 5 describes the optimisation of Ohmic contacts using Si ion implantation. It covers implantation physics, the use and removal of encapsulations layers, implantation

induced damage and annealing recovery. It also includes experiments and results of blanket and selective Si ion implantations demonstrating reduced contact resistance in AlGaN/GaN and AIN/GaN HEMT material systems.

- Chapter 6 investigates recessed Ohmic contact geometry in AlGaN/GaN HEMTs through systematic variation of recess - metallisation overlaps configurations. The fabrication process and characterisation of fabricated structures is also described.
- Chapter 7 concludes the thesis by summarising the key findings and suggesting directions for future work.

2 Fundamentals of GaN-based HEMTs

2.1 Introduction

This chapter discusses the key theoretical concepts relating to the operation of GaN-based HEMTs. It provides an overview of the material properties, polarisation phenomena, spontaneous and piezoelectric, that give rise to the two-dimensional electron gas (2DEG). In addition, the chapter describes the GaN HEMT device structure and its high frequency operation.

2.2 Polarisation Effects in GaN HEMTs

Gallium nitride (GaN) is a group III–V binary semiconductor with a direct bandgap, which can exist in three different structures: rocksalt, zinc-blende, and wurtzite. Among these, the wurtzite structure is the most thermodynamically stable and is therefore widely utilised for electronic and optoelectronic devices. The wurtzite GaN unit cell, illustrated in Figure 2.1, consists of alternating layers of hexagonally close-packed gallium (Ga) and nitrogen (N) atoms. A distinguishing feature of the wurtzite structure is the lack of inversion symmetry along the c-axis, which gives rise to two distinct polarities: Ga-polar (0001) and N-polar (000-1). The corresponding atomic arrangements, with arrows indicating the direction of the spontaneous polarisation dipole (P) in the GaN crystal, are shown in Figure 2.2. In most GaN-based devices, the top surface is Ga-face, corresponding to growth along the (0001) direction. However, device fabrication on N-face GaN, grown along the (000-1) direction, has also been successfully demonstrated [21],[22],[23]. Group III-V semiconductors exhibits strong polarisation fields, which can be categorised into two types: spontaneous polarisation and piezoelectric polarisation.

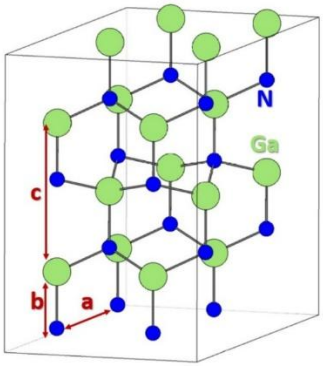


Figure 2.1 Schematic representation of GaN wurtzite structure [24].

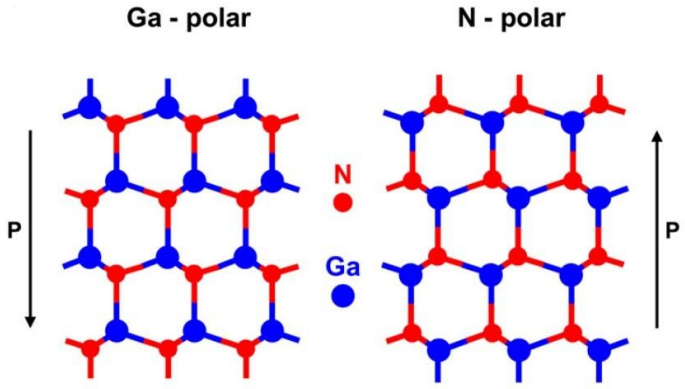


Figure 2.2 Atomic structure of Ga and N-polar GaN [25].

2.2.1 Spontaneous Polarisation

Spontaneous polarisation (P_{SP}) in GaN arises naturally when the material is grown along the c-plane of its wurtzite crystal structure. Due to the lack of inversion symmetry along the [0001] axis and the difference in electronegativity between Ga and N, a dipole moment is formed within each unit cell. Since no external field is required, this effect is termed spontaneous polarisation. P_{SP} is dependent on the Al mole fraction, x by the expression:

$$P_{SP} = (-0.052x - 0.029)\ Cm^{-2} \qquad 2.1$$

Spontaneous polarisation is therefore a direct consequence of the mixed ionic–covalent nature of Ga–N bonds and the deviation of wurtzite lattice parameters from an ideal hexagonal structure. AlN, with its larger bond length and lower c/a ratio, exhibits higher spontaneous polarisation compared to GaN [26],[27],[24].

2.2.2 Piezoelectric Polarisation

Piezoelectric polarization arises from the lattice mismatch between the barrier layer and the GaN interface, which induces compressive strain at the junction. When the crystal lattice is strained, atomic displacements occur within the lattice, generating an electric field whose magnitude depends on the level of strain. The piezoelectric polarization can be expressed as

$$P_{PE} = e_{33}\varepsilon_z + e_{31}(\varepsilon_x + \varepsilon_x) \quad 2.2$$

Where $\varepsilon_z = \frac{c-c_o}{c_o}$ represents the strain along the c-axis, and the in-plane strains $\varepsilon_x = \varepsilon_y = (a - a_0)/a_0$ are assumed to be isotropic, and a and c denotes the lattice constants of the strained layer while e_{33} and e_{31} are the piezoelectric coefficients. The strain components are related by

$$\varepsilon_z = -\frac{2C_{13}}{C_{33}}\varepsilon_x \quad 2.3$$

where $C_{13}$and $C_{33}$are elastic constants [28]. By substituting these relationships into the piezoelectric polarization equation, the polarization along the c-axis is obtained as

$$P_{PE} = 2\frac{(a - a_0)}{a_0}(e_{31} - e_{33}\frac{C_{13}}{C_{33}}) \quad 2.4$$

The total polarisation in a crystal is the sum of the spontaneous and piezoelectric polarisation components, and can be expressed as [29]:

$$P = P_{PE} + P_{SP} \quad 2.5$$

Table 2.1 summarises the lattice constants together with the spontaneous polarisation, piezoelectric constants, and elastic constants of AlN, GaN, and InN, which strongly influence strain and polarisation behaviour in III-nitride heterostructures.

Table 2.1 Lattice constants, spontaneous polarisation, piezoelectric constants, and elastic constants of AlN, GaN and InN [30], [31].

Wurtzite	**AlN**	**GaN**	**InN**
a_o (Å)	3.112	3.189	3.54
c_o (Å)	4.982	5.185	5.705
P_{SP} (C/m^2)	-0.081	-0.029	-0.032
e_{33} (C/m^2)	1.46	0.73	0.97
e_{31}(C/m^2)	-0.60	-0.49	-0.57
C_{13} (GPa)	108	103	92
C_{33} (GPa)	373	405	224

2.2.3 Two-Dimensional Electron Gas (2DEG) Formation

The combined effects of spontaneous and piezoelectric polarisation in III-nitride heterostructures lead to the formation of a high-density 2DEG at the interface between the barrier and the channel layers. In AlGaN/GaN or AlN/GaN HEMTs, the discontinuity between the total polarisation in the barrier layer and that in the GaN channel induces fixed polarisation charges at the heterointerface [32],[33],[34]. This polarisation sheet charge density, σ, at an abrupt interface of an AlGaN/GaN or GaN/AlGaN heterostructure is expressed as:

$$\sigma = P(top) - P(bottom) \qquad 2.6$$

$$= \{P_{SP}(top) + P_{PE}(top)\} - \{P_{SP}(bottom) + P_{PE}(bottom)\} \quad 2.7$$

Figure 2.3 illustrates the AlGaN/GaN heterostructure under three different conditions: (i) a relaxed AlGaN/GaN interface, (ii) a tensile strained AlGaN layer grown on relaxed GaN, and (iii) a compressively strained GaN layer grown on relaxed AlGaN. When the polarisation induced sheet charge density is positive (+), free electrons are attracted to the interface to compensate for the polarisation induced charges, whereas a negative (−) sheet charge density attracts holes. These compensating carriers accumulate at the heterointerface between the barrier and buffer layers, forming a 2DEG or a two-dimensional hole gas (2DHG), depending on the direction of the polarisation field.

In a Ga-face AlGaN/GaN heterostructure, the polarisation-induced sheet charge at the interface is positive, as illustrated in Figure 2.3a Even when the AlGaN barrier layer is relatively thick (greater than approximately 65 nm) and becomes relaxed, electrons remain confined at the heterointerface due to the difference in spontaneous polarisation between GaN and AlGaN layers. When the heterostructure is pseudo morphically grown, as shown in Figure 2.3b the tensile strain in the AlGaN barrier enhances the piezoelectric polarisation, thereby increasing the total polarisation difference $P_{AlGaN} - P_{GaN}$. This, in turn, raises both the positive sheet charge density (σ) and the resulting sheet carrier concentration (n_S) within the 2DEG channel.

In contrast, for N-face AlGaN/GaN heterostructures, the directions of spontaneous and piezoelectric polarisations are reversed compared to the Ga-face configuration, pointing away from the substrate rather than toward it. As a result, the net polarisation-induced sheet charge becomes negative, leading to the accumulation of holes at the interface, as illustrated in Figure. 2.3d and 2.3e However, in an N-face configuration where GaN is grown on top of AlGaN, the resulting interface exhibits a positive sheet charge, which can again confine electrons at the junction, as shown in Figure 2.3f [31], [35].

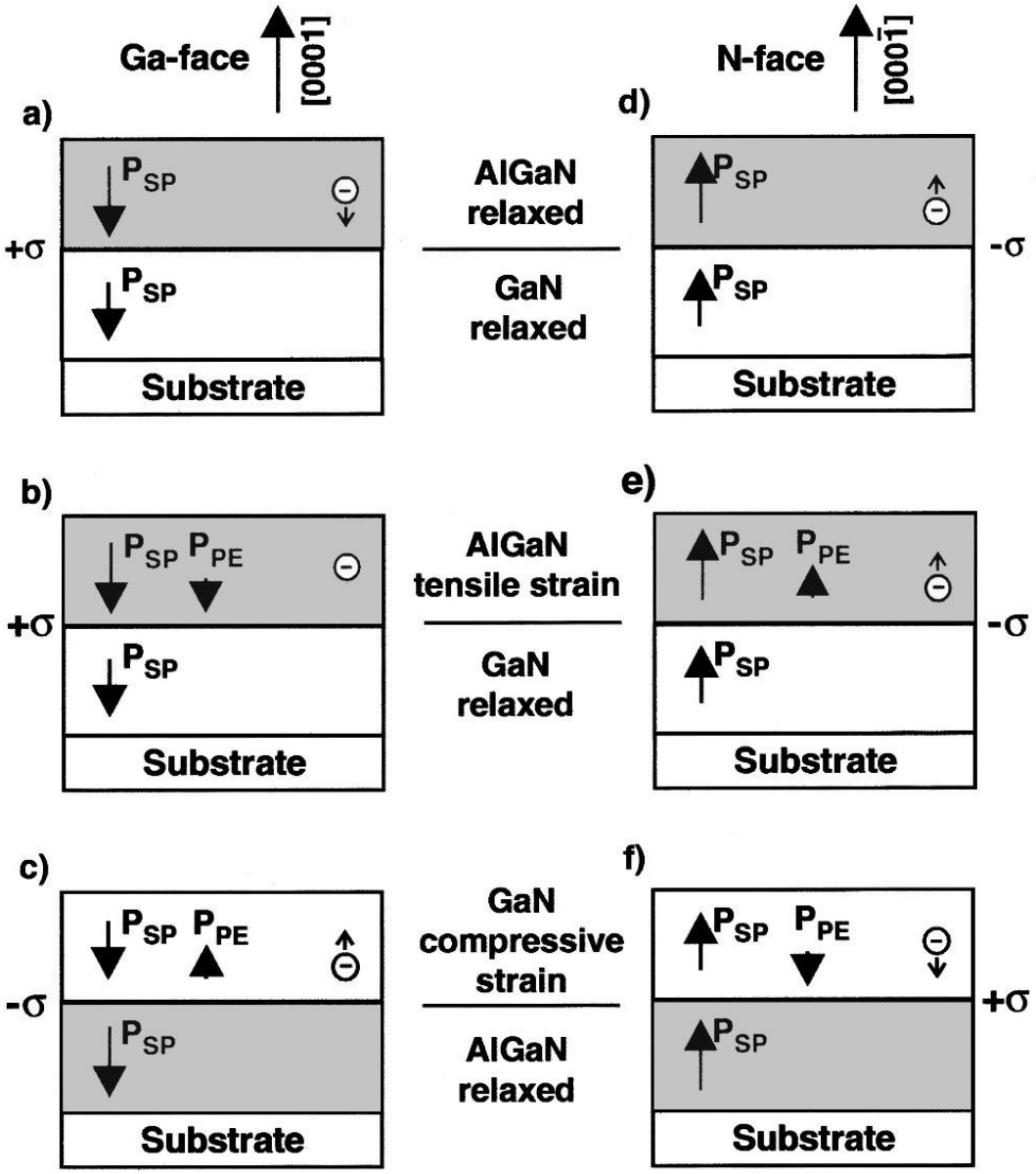


Figure 2.3 Polarisation charge density and polarisation vector orientation in strained and relaxed Ga-face and N-face AlGaN/GaN heterostructures [31].

In a conventional GaN HEMT, a strained AlGaN barrier layer is epitaxially grown on a relaxed GaN channel, as illustrated in Figure 2.3b. Under this configuration, the total polarisation-induced sheet charge density, σ, can be expressed as:

$$\sigma = P_{SP,GaN}(x) - [P_{SP,AlGaN}(x) + P_{PE,AlGaN}(x)] \qquad 2.8$$

The difference in bandgap energy between the AlGaN barrier and the GaN channel results in a large conduction band offset, denoted as ΔE_C. This offset forms a quantum well at the heterointerface, where free electrons accumulate to create the 2DEG. The corresponding energy band diagram of a conventional GaN HEMT is shown in Figure 2.4 [36]

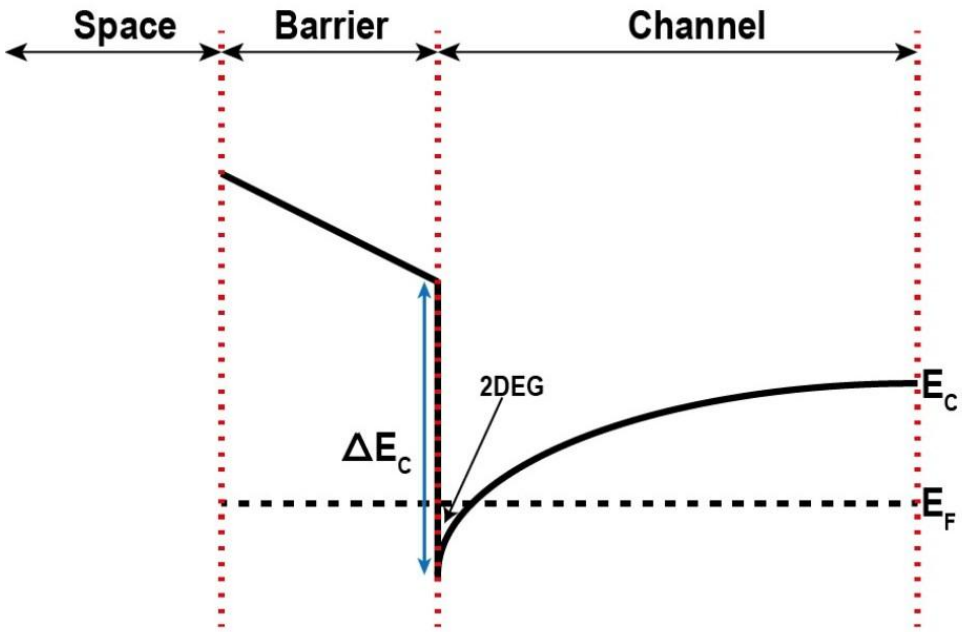


Figure 2.4 Band diagram of a conventional (Ga-face) GaN HEMT.

The maximum sheet carrier concentration, n_s, in the 2DEG can be estimated using [37]:

$$n_s(x) = \frac{\sigma(x)}{q} - \frac{\varepsilon_0 \varepsilon_r(x)}{q^2 d}[q\phi_b(x) + E_F(x) - \Delta E_C(x)]$$

where x is the aluminium mole fraction in the barrier layer, q is the electron charge (1.6×10^{-19} C), ε_0 is the vacuum permittivity, $\varepsilon_r(x)$ is the relative dielectric constant, d is the barrier thickness, $\phi_b(x)$ is the Schottky barrier height, E_F is the Fermi level relative to the GaN conduction band edge, and $\Delta E_C(x)$ is the conduction band offset at the AlGaN/GaN interface where the 2DEG is formed.

2.3 GaN HEMT Device Structure

GaN-based HEMT is a major area of interest within the field of high power and high frequency applications. The epitaxial layers that form the HEMT are sequentially grown on

a substrate from bottom to top. The structure typically comprises a nucleation or buffer layer, a GaN channel layer, a barrier layer (commonly AlGaN or AlN), and a thin GaN cap layer. The most used growth techniques are metal organic chemical vapour deposition (MOCVD) and molecular beam epitaxy (MBE). The source and drain electrodes are designed to form low resistance Ohmic contacts with the semiconductor, while the gate electrode forms a Schottky contact. A basic GaN HEMT schematic is illustrated in Figure 2.5.

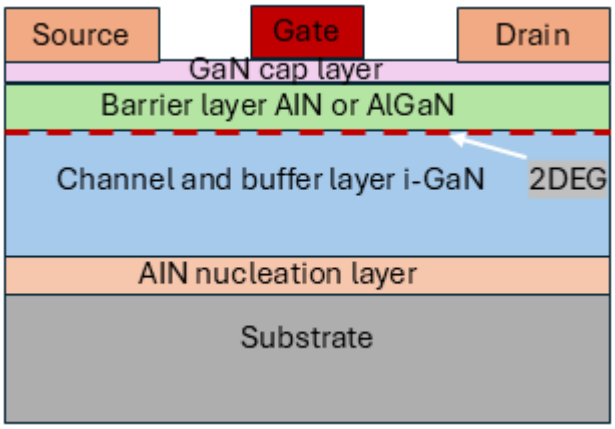


Figure 2.5 Basic GaN HEMT schematic structure.

AlGaN/GaN and AlN/GaN HEMTs differ primarily in their barrier layer material and layer thicknesses, which strongly influence device characteristics such as carrier confinement, electron mobility, and breakdown performance. To better understand the operation and performance of GaN-based HEMTs, it is important to examine the structure in detail, focusing on the composition and function of each constituent layer.

2.3.1 Substrate

GaN is typically grown on a foreign substrate because native GaN substrates are mostly available in relatively small sizes and are expensive [38]. Common substrates used for GaN-based HEMTs include Si, SiC, and sapphire (Al_2O_3), with diamond, and native GaN, also used in specialised applications.

The choice of substrate depends on factors such as lattice mismatch, thermal expansion coefficient, thermal conductivity, wafer size, and cost. Growing GaN on foreign substrates, however, comes with challenges including lattice and thermal mismatch, which can introduce defects, and cracks, in the epitaxial layers [39]. To overcome these limitations,

buffer layers are used. Despite this challenge, foreign substrates remain preferred for their cost effectiveness, scalability, and availability compared to bulk GaN. Table 2.2 lists some of the key physical and thermal properties of commonly used substrates for GaN based HEMTs [40].

Table 2.2 Material properties of typical substrates used in growing GaN HEMTs.

Property / Substrate	**GaN**	**SiC**	**Silicon**	**Sapphire**	**CVD Diamond**	**AlN**
Lattice constant (Å)	3.189	3.08	5.43	4.758	3.567	3.112
Thermal mismatch (%)	-	30	55	-23	-	34
Thermal conductivity (W/m.K)	130	400	150	35	2000	-
Thermal expansion coefficient ($1/10^6$ K)	5.59	4.3	3.59	7.3	0.8	4.15
Lattice Mismatch to GaN (%)	-	3.5	-16.9	16.08	-	2.4
Typical wafer size (inches)	2	6	6	6	4	-

GaN-on-SiC

Silicon carbide (SiC) is widely regarded as the most suitable substrate for high performance GaN based HEMTs [41], [42]. It combines a high thermal conductivity of 400 W/m.K, a small lattice mismatch with GaN of about 3.5%, and a thermal expansion coefficient of 4.3 $\times 10^{-6}$ K^{-1}. These properties significantly minimise strain and allow for low defect densities to be achieved. Due to its excellent thermal conductivity [43], SiC substrates enables improved thermal management, thereby enhancing reliability, breakdown voltage, and RF output power in high frequency applications. During epitaxy, GaN-on-SiC structures typically include an AlN nucleation layer, followed by graded AlGaN transition layers and a semi insulating GaN buffer. These designs help accommodate the residual lattice and thermal mismatch between GaN and SiC [44]. GaN-on-SiC are predominantly used for RF applications.

GaN-on-Silicon

Silicon (Si) has emerged as one of the most widely adopted substrates for GaN based HEMTs because of its low cost, large wafer availability, and compatibility with mainstream complementary metal-oxide semiconductor (CMOS) fabrication processes. One of the

primary obstacles in GaN-on-Si growth is the large lattice mismatch between the two materials. In addition, GaN and Si also has high thermal expansion coefficient mismatch [45], [46] which results in substantial tensile stress during cool down from high epitaxy temperatures, and consequently, cracks[47] which can lead to reduced yield. To address this challenge several interlayers are typically introduced to manage the mismatch strain [48]. GaN-on-Si devices are commonly used for power devices (which they employ a p-GaN gate layer).

GaN-on-Sapphire

Sapphire (Al_2O_3) is one of the earliest and most established substrates for GaN epitaxy and continues to play a significant role in GaN device development, particularly for optoelectronics and cost sensitive applications [49]. Despite the high lattice mismatch between GaN and sapphire, high quality GaN films have been demonstrated on sapphire substrates[50]. Sapphire substrates are low cost but has poor thermal conductivity which makes it unsuitable for high power applications. Although with appropriate thermal management and device geometries GaN-on-sapphire can still demonstrate competitive RF performance [47].

GaN-on-GaN

The progress of bulk GaN substrates has been driven by the laser diode market. Unlike heteroepitaxial growth on foreign substrates such as SiC, Si, or sapphire, homoepitaxial growth on native GaN substrates eliminates lattice and thermal mismatch, resulting in very low dislocation densities ($<10^6$ cm^{-2}) and superior crystalline uniformity [51], [52]. These attributes enhance carrier mobility, breakdown voltage, and reliability. Despite its advantages, the widespread commercialisation of GaN-on-GaN technology has been limited by the high cost and restricted wafer size (typically ≤2–4 inches) of native GaN substrates. Nevertheless, ongoing advances in hydride vapor phase epitaxy (HVPE) and ammonothermal method are reducing production costs and expanding wafer diameters, making GaN-on-GaN increasingly viable for high-power (vertical power devices such as GaN FinFETs) and for high-reliability applications [53],[54]

GaN-on-Diamond

Diamond has emerged as one of the most promising substrates for next generation GaN HEMTs, primarily due to its exceptionally high thermal conductivity, (2000 W/mK), the highest of any known bulk material [55]. This makes GaN-on-diamond an attractive platform

for RF power amplifiers, radar, satellite communications, and other thermal limited, high power density systems. The primary limitations of GaN-on-diamond lie in the complexity and cost of fabrication. The growth of GaN on diamond is difficult due to the large lattice mismatch and so the integration of GaN with diamond is commonly done via bonding.

2.3.2 Functional Roles of Epitaxial Layers

Nucleation layer

The nucleation layer plays a critical role in achieving high-quality GaN epitaxy, especially when GaN is grown on foreign substrates. Its primary function is to reduce the lattice mismatch between the substrate and the overlying GaN buffer, thereby preventing excessive strain, cracking, and defect formation. AlN is the most commonly used nucleation material due to its relatively favourable lattice mismatch with GaN [56] . Depending on the substrate and design requirements, the thickness of the AlN nucleation layer typically lies in the range of 20–200 nm [49], providing a transitional interface that promotes smooth, and low defect GaN overgrowth.

Buffer layer

The buffer layer is grown on top of the AlN nucleation layer, and it performs several essential functions within the GaN HEMT structure. Its primary roles include providing vertical electrical insulation, suppressing off state leakage current, enhancing the vertical breakdown voltage, and improving carrier confinement in the channel [57], [58]. To achieve the high resistivity required for proper buffer insulation, extrinsic dopants are intentionally introduced to the buffer. Among the commonly used dopants, carbon (C) and iron (Fe) are particularly effective. [59], [24],[60].

Channel layer

The GaN channel layer forms the active region of the HEMT and plays a central role in establishing the heterostructure with the barrier layer situated at the top. Because the GaN channel possesses a lower bandgap than the barrier material, this leads to the formation of the 2DEG at the GaN/barrier interface, as discussed in Section 2.2.3.

Spacer layer

In GaN based HEMT, a spacer layer is a thin layer of material incorporated between the barrier and the GaN channel to enhance electron mobility and improve overall device performance. This layer is typically a thin ~ 1nm AIN layer. It separates the 2DEG from charged impurities and alloy disorder in the barrier layer, thereby reducing alloy scattering mechanisms [61], [62], [63], [64].

Barrier layer

The barrier layer is a key component of the GaN HEMT heterostructure, responsible for generating the strong polarization fields that induce the 2DEG at the barrier/channel interface. The choice of barrier material typically AlGaN, AlN, or InAlN [65] determines the strength of the polarization charge, the 2DEG density, the interface quality, and ultimately the electrical performance of the device. In conventional AlGaN/GaN HEMTs, the barrier consists of $Al_xGa_{1-x}N$, with aluminium compositions typically ranging from 20–30%. AlGaN barrier thicknesses usually fall in the range of 20–30 nm, balancing strong polarization fields with the need to avoid strain relaxation and cracking during growth [66],[67].

AlN barriers provide some of the strongest polarization fields among III-nitride heterostructures due to their large bandgap. However, the lattice mismatch between AlN and GaN restricts the AlN barrier thickness to typically 1–5 nm, beyond which strain relaxation and defect formation are likely to occur [68], [69]. Despite their ultrathin nature, AlN barriers can induce very high 2DEG sheet densities and achieve excellent electron confinement, making AlN/GaN HEMTs highly suitable for ultra-high frequency, millimetre-wave, and high power device applications [70], [71].

Cap Layer

The cap layer is the final epitaxial layer grown in a GaN HEMT structure and is most composed of GaN. Although typically only a few nanometres (1-3 nm) thick [72], this layer plays an important role in enhancing both the electrical performance and reliability of the device. One of its primary functions is to suppress barrier relaxation, which in turn helps to reduce gate leakage current as it increase the barrier height [73], [74]. In addition, the GaN cap layer acts as a form of surface passivation, mitigating surface oxidation and increasing the 2DEG density [75]. Due to the smaller bandgap of GaN (~ 3.4 eV) compared to AlGaN and AlN, the presence of a GaN cap also facilitates improved Ohmic contact formation by lowering the effective contact resistance in the structure[76].

2.4 HEMT Operation and Characteristics

The basic structure of a GaN HEMT consists of a Schottky gate contact and two Ohmic contacts, namely the source and drain, fabricated on a GaN heterostructure. Due to strong spontaneous and piezoelectric polarization effects in III-nitride materials, a 2DEG is formed at the barrier/GaN interface without the need for intentional doping. As a result, GaN HEMTs are inherently depletion mode (normally on) devices, where a conductive channel exists at zero gate bias.

At zero gate source voltage (V_{GS}), the polarization induced 2DEG provides a low resistance path directly connecting the source and drain, allowing current to flow when a drain source voltage (V_{DS}) is applied, as shown in Figure 2.6(a). When a positive gate voltage is applied, the electron density in the 2DEG increases thereby enhancing the drain current. Conversely, applying a negative gate voltage progressively depletes the 2DEG. When the gate voltage reaches the threshold voltage (V_{th}), the 2DEG beneath the gate is fully depleted, cutting off the current flow between the source and drain, as illustrated in Figure 2.6(b).

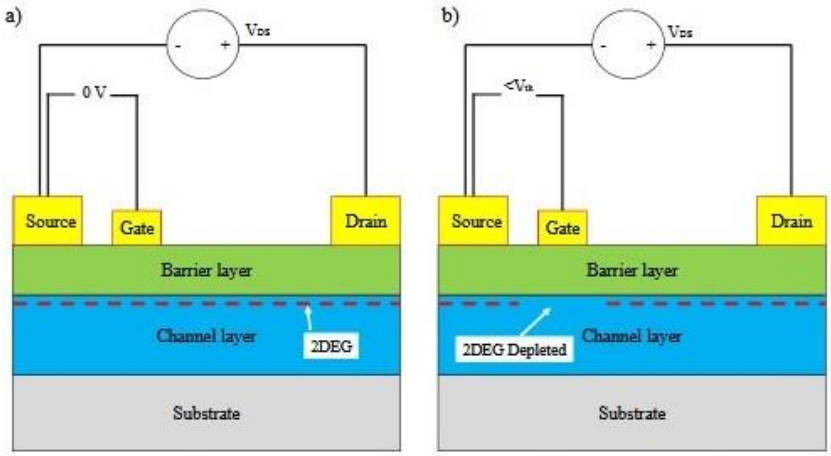


Figure 2.6 Schematic illustration of a D-mode HEMT showing (a) current flow between the source and drain at $V_{GS} = 0$ V, and (b) channel depletion and device turn off under an applied negative gate bias [77].

GaN HEMTs operate in a manner similar to conventional FETs and exhibit distinct linear and saturation operating regions. In the linear region ($V_{DS} \leq V_{GS} - V_{th}$), the drain current is determined by the total charge present in the channel (under the gate) and the time required

for electrons to traverse the gate under an applied voltage. The time taken for electrons to travel across the gate at an effective velocity v_{eff} is given by:

$$t = \frac{L_G}{v_{\text{eff}}} \tag{2.1}$$

where L_G is the gate length. The total charge under the gate can be expressed as:

$$Q = qn_s L_G W_G \tag{2.2}$$

where q is the electron charge, n_s is the 2DEG sheet carrier concentration, and W_G is the gate width. The drain current is therefore given by:

$$I_{DS} = \frac{Q}{t} = qn_s v_{\text{eff}} W_G \tag{2.3}$$

The effective electron velocity in the linear region is related to the applied electric field and electron mobility:

$$v_{\text{eff}} = \mu_n E = \mu_n \frac{V_{DS}}{L_{DS}} \tag{2.4}$$

where μ_n is the electron mobility.

As the drain voltage increases and the condition $V_{DS} \geq V_{GS} - V_{th}$ is satisfied, the device enters the saturation region. In this operating region, the electric field near the drain side of the gate becomes sufficiently high that the electron velocity reaches its saturation value due to increased scattering. This leads to pinch-off at the drain end of the channel, and the drain current becomes relatively independent of further increases in V_{DS}. Figure 2.7 shows the typical current voltage characteristics of a GaN HEMT.

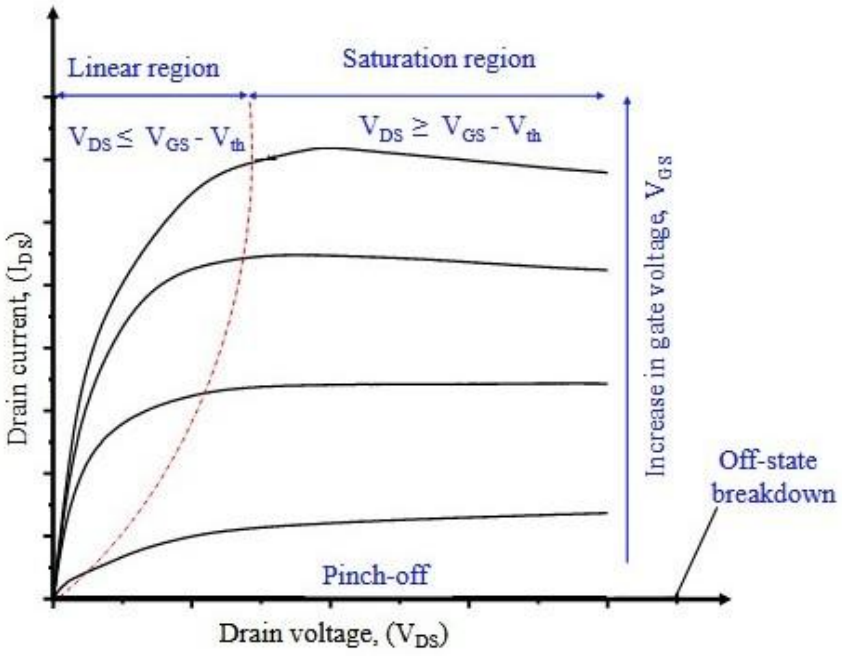


Figure 2.7 DC output drain current - voltage (I–V) characteristics of a typical GaN HEMT.

The charge under the gate can also be expressed as a function of the applied gate voltage.

$$Q = CV \tag{2.5}$$

where $C$is the gate capacitance and $V = V_G - V_{th}$ is the effective gate voltage. The gate capacitance is given by:

$$C = \frac{\varepsilon L_G W_G}{d_{\text{barrier}}} \tag{2.6}$$

where ε is the dielectric permittivity, L_G and $W_G$are the gate length and width, respectively, and d_{barrier} is the barrier thickness. Using this relationship, the 2DEG sheet carrier concentration can be written as:

$$n_s = \frac{\varepsilon_{\text{barrier}}}{q(d_{\text{barrier}} + \Delta d)}(V_G - V_{th}) \tag{2.7}$$

where Δd represents the effective distance of the 2DEG from the heterointerface. When $V_G = V_{th}$, the sheet carrier concentration becomes zero, and the channel is fully depleted.

In the saturation regime, where the electron velocity reaches the saturation velocity v_{sat}, the drain current can be expressed as:

$$I_{DS} = \frac{\varepsilon_{\text{barrier}} v_{\text{sat}} W_G}{d_{\text{barrier}} + \Delta d}(V_G - V_{th}) \tag{2.8}$$

GaN HEMTs are typically biased at high drain voltages (in the saturation region) to achieve high output powers.

Transconductance (g_m) is a key performance metric that quantifies the sensitivity of the drain current to changes in gate voltage and is defined as:

$$g_m = \frac{\partial I_{DS}}{\partial V_G} \tag{2.9}$$

In the saturation region, the transconductance becomes:

$$g_m = \frac{\varepsilon_{\text{barrier}} v_{\text{sat}} W_G}{d_{\text{barrier}} + \Delta d} \tag{2.10}$$

A high transconductance is essential for achieving high gain and high frequency performance in RF applications.

2.5 RF Performance Metrics

The high frequency behaviour of HEMTs is commonly characterised using 2-port scattering parameters (S parameters) [78]. A HEMT is a two-port network, where the input port is defined between the gate and source terminal, and the output port between the drain and source terminal when operated in a common source configuration.

Measured S-parameters form the basis for extracting key RF figures of merit, including the current gain cut-off frequency (f_T) and the maximum oscillation frequency (f_{MAX}), which together define the upper frequency limits of transistor operation. The short-circuit current gain, expressed in terms of hybrid parameters, is given by the forward transmission hybrid h_{21}. This parameter can be directly derived from the measured 2-port S-parameters (S_{11}, S_{12}, S_{21} and S_{22}) as:

$$h_{21} = \frac{I_{out}}{I_{in}} = \frac{-2S_{21}}{(1 - S_{11})(1 + S_{22}) + S_{12}S_{21}} \tag{2.11}$$

current gain cut-off frequency f_T is defined as the frequency at which the magnitude of the current gain falls to unity or 0 dB:

$$| h_{21}(f_T) | = 1 \tag{2.12}$$

Physically, f_T represents the frequency at which the transistor ceases to provide current amplification.

The maximum oscillation frequency f_{MAX} is defined as the frequency at which the transistor power gain falls to unity. It is commonly extracted using Mason unilateral power gain (U)

$$U = \frac{| S_{21}/S_{12} - 1 |^2}{2[K | S_{21}/S_{12} | - \mathrm{Re}(S_{21}/S_{12})]} \tag{2.13}$$

The maximum oscillation frequency is then given by:

$$U(f_{MAX}) = 1 \tag{2.14}$$

2.5.1 Small-Signal Equivalent Circuit

HEMTs are commonly operated in a common source configuration, where the gate and drain electrodes are biased with respect to the source. Under these conditions, a small RF signal is applied to the gate terminal, and the amplified response is obtained at the drain terminal. For a given set of bias voltages, the RF behaviour of the HEMT can be measured in terms of S-parameters and described using a small-signal equivalent circuit model, which represents a linearised approximation of the device response around its operating point [79]. This approach enables the evaluation of device performance and the identification of factors limiting high frequency operation.

The small-signal equivalent circuit provides an electrical representation of the physical HEMT structure, where each circuit element corresponds to a specific region of the device. Figure 2.8 illustrates the small signal network superimposed on the cross-sectional view of the GaN HEMT.

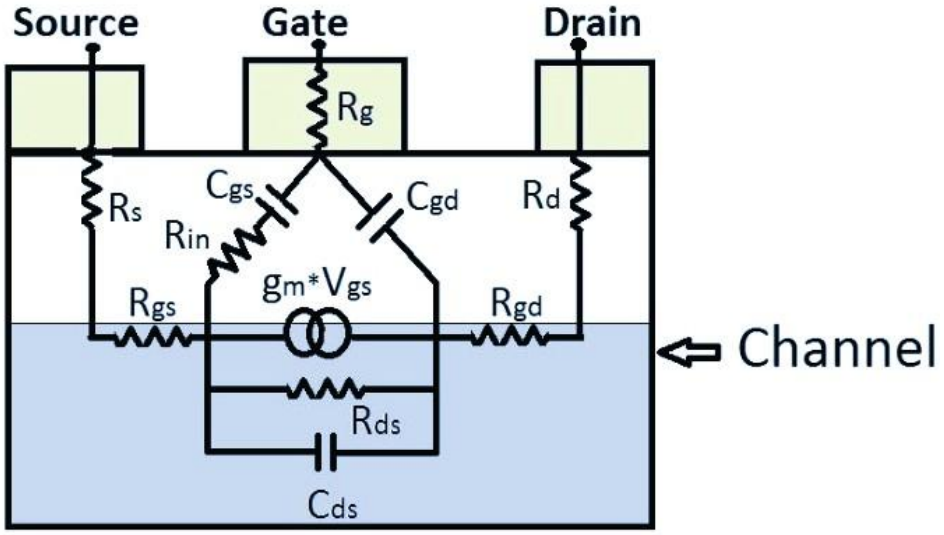


Figure 2.8 Cross-sectional schematic of the GaN HEMT with the superimposed small-signal equivalent circuit.

The small-signal model of a GaN HEMT is divided into intrinsic and extrinsic regions. The intrinsic region corresponds to the active part of the device located beneath the gate and within the channel between the source and drain, whereas the extrinsic region includes parasitic elements associated with the gate, source, and drain contacts, as well as access regions, this is illustrated in Figure 2.9. Intrinsic elements are influenced by the applied bias conditions, while extrinsic elements are largely bias independent and are determined by device geometry and layout.

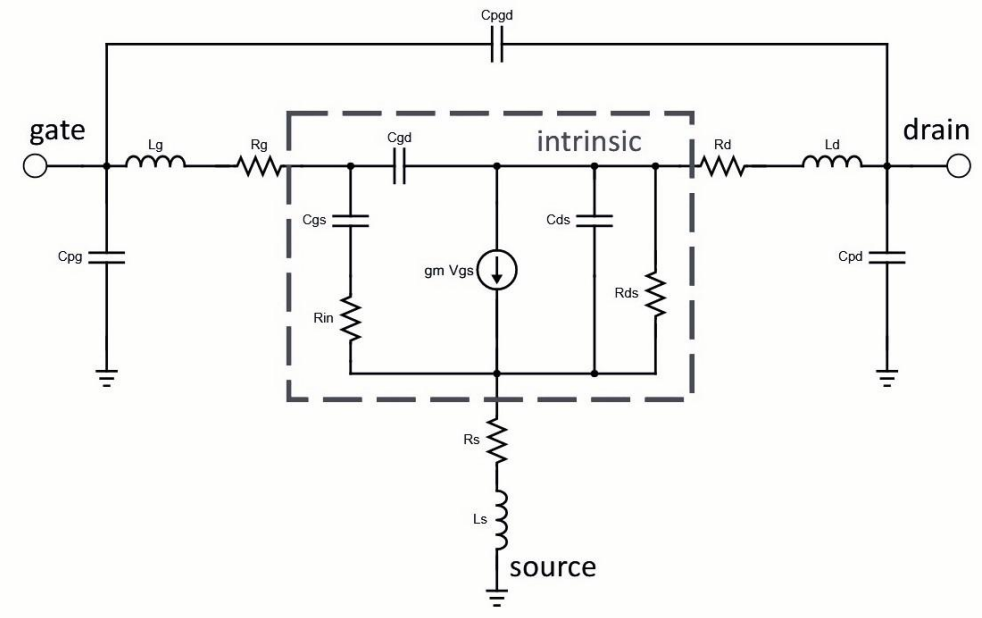


Figure 2.9 Small signal equivalent circuit of a GaN HEMT.

Gate source capacitance (C_{gs}) and gate drain capacitance (C_{gd}) represent the charge stored in the depletion region beneath the gate and towards the source and drain sides, respectively. The resistance of the semiconductor under the gate is modelled by the input resistance (R_{in}), which appears in series with C_{gs}. The gain mechanism of the HEMT is represented by a current generator $g_m V_{gs}$, where $g_m$is the transconductance and $V_{gs}$is the voltage across the gate capacitance. The finite output resistance of the device is represented by R_{ds}. The drain–source capacitance (C_{ds}) represents the capacitive coupling between the drain and source across the depleted channel region and appears in parallel with R_{ds}.

The extrinsic components of the small-signal model account for parasitic effects outside the intrinsic region. R_s, R_d and R_g are contact and access resistances of the source, drain and gate electrodes, respectively. Parasitic inductances L_g, L_d, and $L_s$originate from the contact pads at the gate, drain, and source terminals. Additionally, parasitic capacitances (C_{pg}, C_{pd}, and C_{pgd}) result from electric field coupling between metal contacts and are determined by the device layout [80].

The expressions for f_T and f_{MAX} can also be evaluated in terms of the equivalent circuit elements shown in Figure 2.9, allowing the cut-off and maximum oscillation frequencies to be calculated directly from the small-signal model parameters

$$f_T = \frac{g_m}{2\pi\left[(C_{gs}+C_{gd})\left(1+\frac{R_s+R_d}{R_{ds}}\right)+g_m C_{gd}(R_s+R_d)\right]} \tag{2.15}$$

$$f_{MAX} = \frac{f_T}{2\sqrt{\left(\frac{R_g+R_{in}+R_s}{R_{ds}}\right)+2\pi f_T R_g C_{gd}}} \tag{2.16}$$

In summary, equations 2.11, 2.13, 2.15 and 2.16 show the link between RF measurements and equivalent circuit elements of the device. Lowering the drain and source resistances, R_d and R_s, which are Ohmic contact resistances in the device, is the focus of the research described in this thesis. Therefore, a short description of the physics of these contacts is described next.

2.6 Metal–Semiconductor Interfaces

Metal–semiconductor contacts are formed when a metal is deposited onto a semiconductor, resulting in the formation of a barrier at the metal–semiconductor interface. Electrons traversing this junction encounter the barrier, which they must surmount [81]. In HEMTs, two primary types of metal–semiconductor junctions exist: Schottky and Ohmic. Schottky contacts exhibit rectifying behaviour and are commonly used as gate contacts, whereas Ohmic contacts provide low-resistance, bidirectional current flow for the source and drain.

When a metal is brought into contact with an n-type semiconductor, the Fermi levels of the two materials align at thermal equilibrium. This alignment is achieved through the transfer of electrons from the semiconductor conduction band (E_c) into the metal, provided the metal Fermi level is lower than that of the semiconductor [82]. The Fermi level is defined as the highest energy level that electrons can occupy at absolute zero temperature (0 K). Figure 2.10 illustrates the energy band diagram of a metal in contact with an n-type semiconductor.

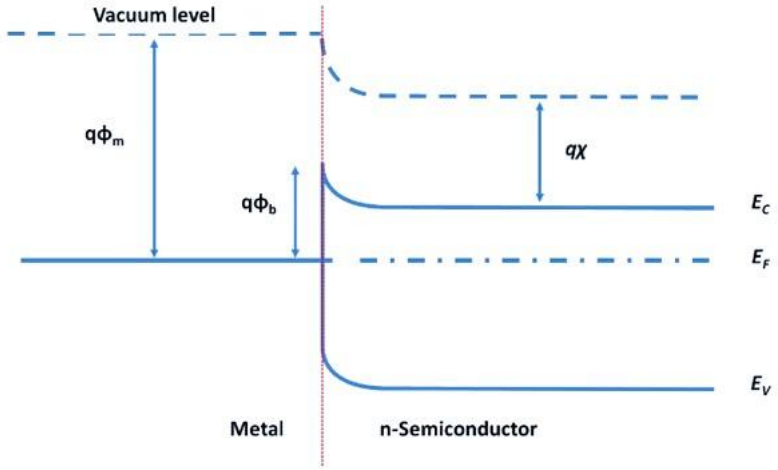


Figure 2.10 Energy band diagram of a metal–semiconductor (n-type) contact.

Band bending at the metal–semiconductor interface causes a discontinuity in the conduction bands, leading to the formation of an energy barrier known as the Schottky barrier. For an ideal contact between a metal and an n-type semiconductor, the Schottky barrier height $q\phi_b$ is equal to the difference between the metal work function ϕ_m and the semiconductor electron affinity χ, and is given by [83]

$$q\phi_b = q\phi_m - q\chi \tag{2.17}$$

Here, $q\phi_m$ is the metal work function, defined as the energy difference between the metal Fermi level and the vacuum level, while $q\chi$ is the electron affinity, defined as the energy required to remove an electron from the conduction band into the vacuum. Achieving low-resistivity Ohmic contacts with wide band-gap semiconductors is challenging due to their high electron affinity and large band-gap width [84].

2.6.1 Current Transport Mechanisms

Thermionic emission (TE), field emission (FE), and thermionic field emission (TFE) are the main conduction mechanisms by which carriers are transported across a metal–semiconductor interface. The dominant conduction mechanism depends on the semiconductor doping concentration (N_D), which determines the thickness of the space-charge region (barrier width) formed at the interface [85],[86].

Thermionic emission dominates current transport in lightly doped semiconductors ($N_D < 1 \times 10^{17}$ cm^{-3}). Field emission, which is based on quantum mechanical tunnelling, becomes the primary transport mechanism in heavily doped semiconductors ($N_D > 1 \times 10^{19}$ cm^{-3}). Thermionic field emission represents an intermediate transport mechanism, occurring for doping concentrations typically in the range $1 \times 10^{17} < N_D < 1 \times 10^{19}$ cm^{-3}.

The three transport regimes can be distinguished using the characteristic energy E_{00}, defined as

$$E_{00} = \frac{qh}{4\pi}\sqrt{\frac{N}{\kappa_s \varepsilon_0 m^*_{\text{tun}}}} = 1.86 \times 10^{-11}\sqrt{\frac{N}{\kappa_s (m^*_{\text{tun}}/m)}} \text{ [eV]} \tag{2.18}$$

where N is the doping concentration, m^*_{tun} is the tunnelling effective mass, m is the free electron mass, ε_0 is the vacuum permittivity, and κ_s is the semiconductor dielectric constant. Comparison of E_{00} with the thermal energy kT indicates that thermionic emission dominates when $kT \gg E_{00}$, thermionic field emission occurs when $kT \approx E_{00}$, and field emission dominates when $kT \ll E_{00}$, where $k$is Boltzmann's constant and T is the absolute temperature [87].

2.6.2 Schottky Contacts

A Schottky contact is distinguished by its asymmetric current voltage (I–V) behaviour, in which the current flowing through the metal–semiconductor junction differs with the polarity of the applied bias voltage. The typical I–V characteristics of a Schottky contact are shown in Figure 2.11.

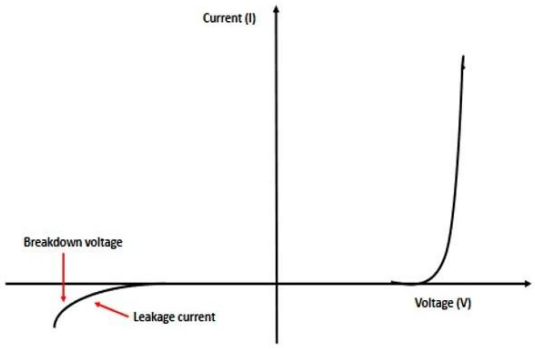


Figure 2.11 I-V characteristics of Schottky contact.

In conventional GaN based devices, Schottky contacts are used as the gate terminal, where modulation of the gate voltage controls the carrier concentration in the 2DEG. In this work, nickel (Ni) and gold (Au) are used for the Schottky contacts. For wide band gap semiconductors such as GaN, the Schottky barrier height is strongly influenced by the work function of the contact metal [88]. Consequently, metals with high work functions are generally preferred for Schottky gate fabrication in GaN based devices.

Table 2.1 lists the work functions of several commonly used metals, from which platinum (Pt) and nickel (Ni) are identified as the most suitable metals for Schottky contact formation due to their high work functions. However, Pt suffers from poor adhesion to GaN, limiting its practical use. Nickel is therefore widely adopted as a Schottky contact metal owing to its high Schottky barrier height, strong adhesion to GaN, minimal thermal reactivity with nitrogen atoms, and relatively high work function (~5.15 eV). In contrast, metals such as titanium (Ti) and aluminium (Al), which have lower work functions of 4.33 eV and 4.28 eV respectively, are typically used for Ohmic contacts [89]. The Schottky gate electrode is typically realised using a Ni/Au metal stack, where the Au layer serves to protect the underlying Ni layer from oxidation.

Table 2.3 Comparison of work-function values for different metals.

Metal	Pt	Ni	Au	Mo	Ti	Al	Ag
Work function (eV)	5.65	5.15	5.10	4.60	4.33	4.28	4.26

2.6.3 Ohmic Contacts

An Ohmic contact is characterised by a linear current voltage (I–V) relationship that is independent of the polarity of the applied bias. In an ideal Ohmic contact, the voltage drop across the metal semiconductor interface is negligible compared to that within the bulk semiconductor material, ensuring efficient carrier injection into the device[90]. Figure 2.12 illustrates the typical I–V characteristics of an Ohmic contact.

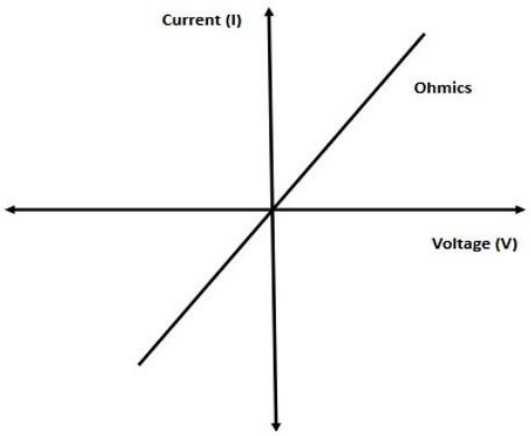


Figure 2.12 I-V characteristics for an Ohmic contact.

For GaN based HEMTs, high-quality Ohmic contacts are essential to minimise resistance at the source and drain terminals. In addition to low contact resistance, practical Ohmic contacts must exhibit good thermal stability and smooth surface morphology to ensure reliable device operation. Achieving these requirements is particularly challenging in wide bandgap heterostructures such as AlGaN/GaN and AlN/GaN, where contact performance is strongly influenced by the properties of the metal–semiconductor interface established during fabrication.

2.7 Contact Resistance Characterisation

Accurate extraction of Ohmic contact resistance is essential for assessing contact quality in GaN-based devices. Transfer length method or transmission line model (TLM) is a widely used technique for this purpose, enabling quantitative evaluation of contact resistance and specific contact resistivity through dedicated test structures [91], [92]. The TLM approach is commonly implemented in two forms: the linear transmission line model (LTLM) and the

circular transmission line model (CTLM). These models allow the separation of contact resistance from the sheet resistance of the underlying semiconductor, providing insight into the effectiveness of Ohmic contact formation.

2.7.1 Linear Transmission Line Model

The LTLM is a widely used technique for quantifying the electrical properties of semiconductor layers and their interfaces with metal contacts. Originally described by Reeves and Harrison [93], the LTLM employs a set of Ohmic contacts with uniform width (W) and varying gap spacing (L) to establish a relationship between the measured total resistance, the contact resistance, and the sheet resistance of the semiconductor. As the contact spacing increases, the measured resistance increases due to the additional series resistance contributed by the semiconductor region between the contacts. Figure 2.13 shows an SEM image of a fabricated LTLM test structure, highlighting the varying gap spacings (in μm) between adjacent contact pads.

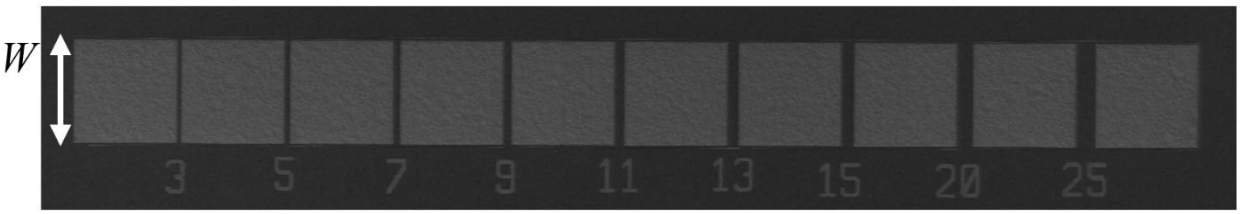


Figure 2.13 SEM image of the fabricated LTLM test structure with contact gap spacings ranging from 3 to 25 μm.

Mesa isolation is an essential step in the fabrication of LTLM structures, as it ensures well defined current paths. Without mesa isolation, fringing fields and lateral current spreading can distort the measured resistance, leading to inaccuracies in the extracted contact and sheet resistance values. By confining the current flow, mesa isolation enables more reliable determination of the contact resistance R_c and sheet resistance R_{sh}.

Electrical characterisation of TLM structures can be performed using a four-probe measurement configuration. In this method, current is applied through one pair of probes while the voltage is measured across a separate pair, thereby minimising the influence of

probe and system cable resistances. The total resistance R_T measured between two contacts separated by a distance L can be expressed as:

$$R_T = 2R_m + 2R_c + R_{semi} \tag{2.19}$$

where R_m is the resistance of the contact metal, R_c is the contact resistance at the metal–semiconductor interface, and R_{semi} is the resistance of the semiconductor material. In most practical cases, $R_c \gg R_m$, and the contribution of $R_m$can be neglected.

The semiconductor resistance is given by:

$$R_{semi} = \frac{\rho}{t}\frac{L}{W} \tag{2.20}$$

which can also be written as:

$$R_{semi} = R_{sh}\frac{L}{W} \tag{2.21}$$

where ρ is the resistivity, $t$is the thickness of the conducting semiconductor, and R_{sh} is the sheet resistance expressed in ohms per square (Ω/□). Substituting into Equation (2.19) yields:

$$R_T = 2R_c + \frac{R_{sh}}{W}L \tag{2.22}$$

A plot of the measured total resistance as a function of contact spacing, as illustrated in Figure 2.14, allows extraction of key parameters. The y-axis intercept corresponds to $2R_c$. The normalised contact resistance $R_c(\Omega.mm)$ is obtained by multiplying $R_c$by the contact width W.

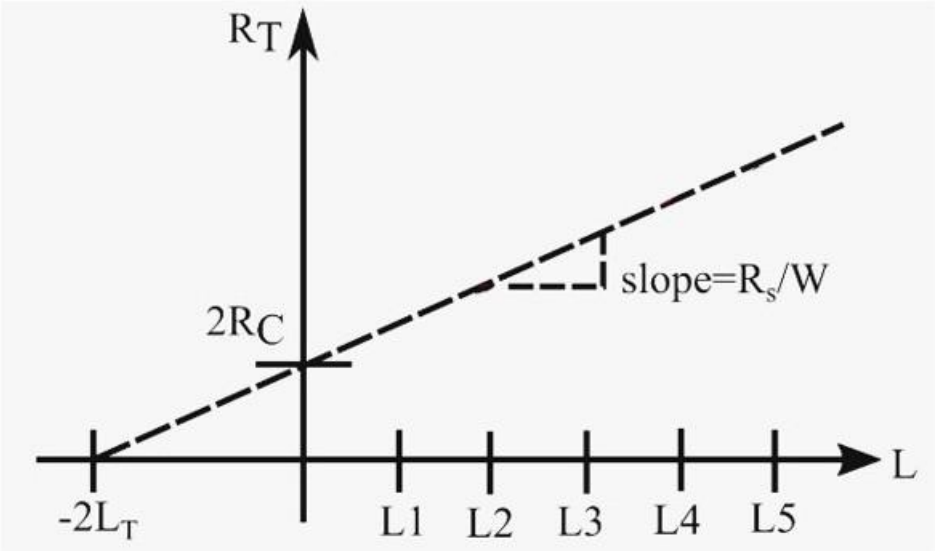


Figure 2.14 Total resistance as a function of contact spacing.

In addition, the transfer length L_T can be extracted by extrapolating to the point where the graph intercepts with the horizontal axis. The transfer length represents the effective distance over which current is transferred between the metal contact and the semiconductor. Current injection is highest near the contact edge, leading to a phenomenon known as current crowding.

The transfer length is given by:

$$L_T = \sqrt{\frac{\rho_c}{R_{sh}}} \tag{2.23}$$

2.7.2 Circular Transmission Line Model

The CTLM technique is commonly used to evaluate the electrical characteristics of Ohmic contacts. CTLM structures inherently address the problem of fringing fields. Unlike Linear Transmission Line Model (LTLM) structures, which require two lithography steps (patterning and mesa isolation), CTLM structures can be fabricated using a single lithography step. In the CTLM geometry, the inner circular contact is surrounded by the outer contact, ensuring that the current flowing between the two contacts is fully confined. Consequently, there are no fringing fields/currents, and so mesa isolation is not required for CTLM structures.

Figure 2.15 shows an SEM image of a fabricated CTLM test structure, it consists of concentric metallic contacts arranged as an inner circular contact and an outer ring, separated by a gap. The CTLM structures used throughout this thesis had an inner-contact diameter of 180 μm. The gap spacings between the inner and outer contacts were 4, 8, 12, 16, 20, 24, 32, 40, and 48 μm.

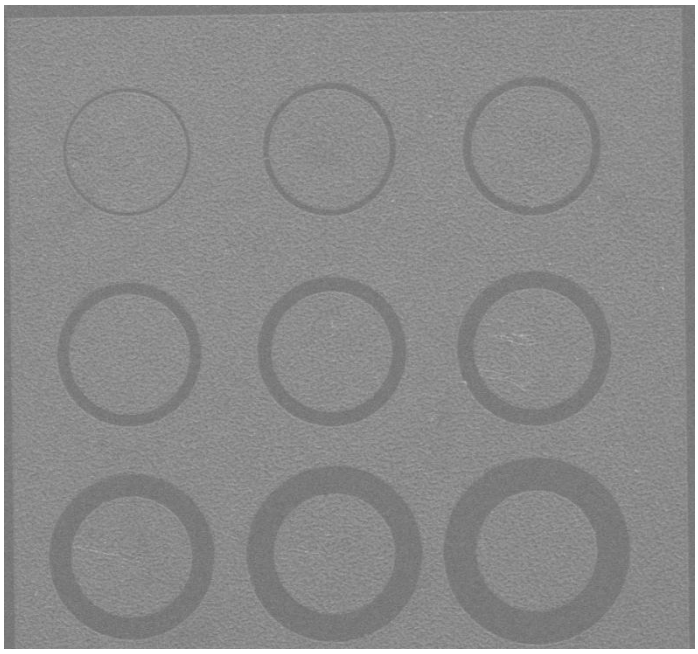


Figure 2.15 SEM image of the fabricated CTLM test structure.

The technique for extracting the contact resistance from CTLM structures is similar to that used for LTLM structures. One key difference, however, is the requirement for a correction factor to be applied to CTLM data. This correction accounts for the unequal circumferences of the inner and outer circular contacts and is necessary to obtain a linear relationship between the total resistance and the gap spacing [94]. The correction factor depends on the gap spacing and is given by:

$$C = \frac{R_1}{s} ln\left(\frac{R_1 + s}{R_1}\right) \tag{2.24}$$

where R_1 is the radius of the inner circular contact and s is the gap spacing. Correction factors calculated for $R_1 = 90$ μm are listed in Table 2.4.

Table 2.4 Correction factors for different gap spacings.

Gap spacing (μm)	4	8	12	16	20	24	32	40	48
Correction factor (C)	0.98	0.96	0.94	0.92	0.90	0.89	0.86	0.83	0.80

2.8 Summary

This chapter presented the fundamental theory of GaN HEMTs. The formation of the 2DEG was discussed, with emphasis on the role of spontaneous and piezoelectric polarization in enabling high electron density and mobility within GaN-based heterostructures. Substrate selection was reviewed, noting that due to the historical unavailability of native GaN substrates, GaN epitaxial layers are commonly grown on foreign substrates such as SiC, Si, and sapphire. The chapter also covered the device structure, operating principles, and depletion-mode operation of GaN HEMTs. Next, the small-signal equivalent circuit model was introduced as a critical tool for understanding and analysing the RF behaviour of GaN HEMTs. The extraction of key frequency figures of merit, including the current gain cut-off frequency and maximum oscillation frequency, was briefly described. Finally, a brief description of the physics of metal-semiconductor interfaces for both Ohmic and Schottky contacts was given as well as the method of extraction of the Ohmic contact resistance from measurements. Overall, this chapter established the theoretical foundation necessary for the analysis, characterisation, and optimisation of Ohmic contacts for GaN HEMTs discussed in subsequent chapters.

3 Semiconductor Growth and Fabrication Techniques

3.1 Introduction

This chapter describes the fabrication techniques used for the realisation of AlGaN/GaN and AlN/GaN HEMTs on GaN-on-SiC and sapphire substrates. The fabrication processes include sample preparation, lithography, dry and wet etching, mesa isolation, dielectric film deposition, metallisation, and post metallisation annealing, all of which are critical to achieving functional and high-performance devices. All micro- and nanofabrication work was carried out at the James Watt Nanofabrication Centre (JWNC), University of Glasgow, while ion implantation, discussed in subsequent chapters, was performed at the Surrey Ion Beam Centre. The epitaxial growth of the GaN heterostructures was undertaken externally by commercial suppliers and is therefore discussed only briefly. This chapter focuses on the practical implementation of standard cleanroom processes and outlines the fabrication flow adopted in this project, providing the technological foundation for the device structures analysed in later chapters.

3.2 Epitaxial Growth of GaN-Based Semiconductors

Epitaxial material growth involves the formation of a crystalline thin film on a crystalline substrate through controlled atomic layer deposition under carefully optimised growth conditions such as temperature, pressure, precursor concentration, and gas flow rates. When the grown layer differs from the substrate material, the process is referred to as heteroepitaxy, which is of primary relevance to the AlGaN/GaN and AlN/GaN heterostructures investigated in this work. During growth, atoms from high purity sources are transported to the substrate surface, where the optimisation of growth parameters is essential to achieve high crystalline quality, layer uniformity, and precise thickness control. The two most widely used techniques for GaN based epitaxial growth are metal organic chemical vapour deposition (MOCVD) [95], [96], [97] and molecular beam epitaxy (MBE) [98], [99], [100] both of which offer excellent control over heterostructure composition. All wafers used in this project were commercially grown, using either MOCVD or MBE.

3.2.1 Metal-Organic Chemical Vapour Deposition

MOCVD is the most widely used epitaxial growth technique in the development of GaN based technologies. Its widespread adoption is largely attributed to its relatively low cost when compared with alternative epitaxial methods such as MBE, making MOCVD particularly attractive for industrial and commercial device fabrication. For GaN based heterostructures, MOCVD typically achieves growth rates in the range of 1–3 μm/h, which are approximately twice those attainable using MBE [101]. Furthermore, MOCVD growth is generally performed at elevated temperatures exceeding 1000 °C, significantly higher than the growth temperatures commonly employed in MBE processes [102]

During the MOCVD growth process, metal organic precursors including trimethylgallium (TMG), trimethylaluminum (TMA), and trimethylindium (TMI) are delivered to the heated substrate surface using carrier gases such as hydrogen or nitrogen. For GaN epitaxy, ammonia (NH_3) is commonly used as the nitrogen source. A simplified overall chemical reaction describing GaN growth is given by:

$$TMG + NH_3 \rightarrow GaN + 3CH_4$$

where TMG $(CH_3)_3$ Ga supplies gallium, NH_3 provides nitrogen, and methane (CH_4) is produced as a byproduct of the reaction. Figure 3.1 shows the MOCVD growth chamber [103].

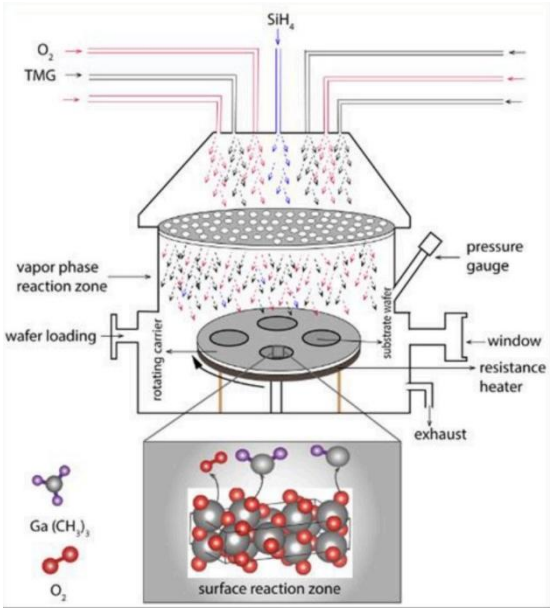


Figure 3.1 Schematic diagram showing the MOCVD reaction chamber.

3.2.2 Molecular Beam Epitaxy (MBE)

Molecular beam epitaxy (MBE) is a widely used technique for the epitaxial growth of high-quality crystalline layers on a substrate. In this process, the substrate is placed inside a high-vacuum chamber, where molecular or atomic beams of the constituent elements are directed toward the substrate surface. For GaN HEMT growth, beams of gallium and nitrogen are supplied to form the epitaxial layers.

MBE growth is typically carried out at temperatures of approximately 700 °C, which are significantly lower than those used in MOCVD. Despite this advantage, MBE is generally more expensive than MOCVD due to its relatively low growth rates, which typically range from 300 to 500 nm/h [101]. These slower growth rates prevent MBE from meeting the large-scale wafer supply demands of the GaN industry. Consequently, MBE is primarily used in research and development applications, where its ability to produce high-quality material with precise control over composition and interfaces makes it well suited for proof-of-concept studies and advanced device research, rather than high volume manufacturing. A schematic of the basic elements of an MBE growth chamber is shown in Figure 3.2 [104]

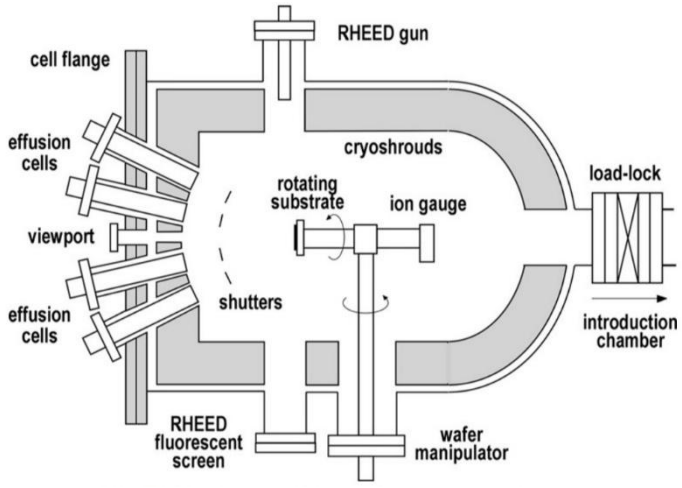


Figure 3.2 Schematic View of an MBE growth chamber.

3.3 Lithography

Lithography is a key micro- and nanofabrication process used to transfer predefined device patterns onto the surface of a substrate. It is an essential step in the fabrication of electronic devices, where accurate pattern definition and alignment are critical to device performance. Depending on the required resolution and throughput, different lithographic techniques can be used. The two most used lithography methods in semiconductor processing are photolithography and electron beam lithography (EBL).

3.3.1 Photolithography

Photolithography, also referred to as optical lithography, is the primary patterning technique used in this work for defining micrometre scale device features. Due to its high throughput, good reproducibility, and low cost per fabricated device, photolithography is widely adopted in both industrial and research-based semiconductor fabrication. In photolithography, patterns are transferred from a hard chrome photomask onto a photoresist coated wafer using ultraviolet (UV) light ($\lambda \approx 200–400$ nm). All photolithography processes in this work were carried out at the JWNC using a Karl Suss MA8 mask aligner with a minimum feature size of approximately 1 μm. Photolithography enables high throughput pattern transfer but is limited in resolution (alignment accuracy of ±1 μm) and is therefore unsuitable for submicron feature definition. Figure 3.3 shows the Karl Suss MA8 mask aligner.

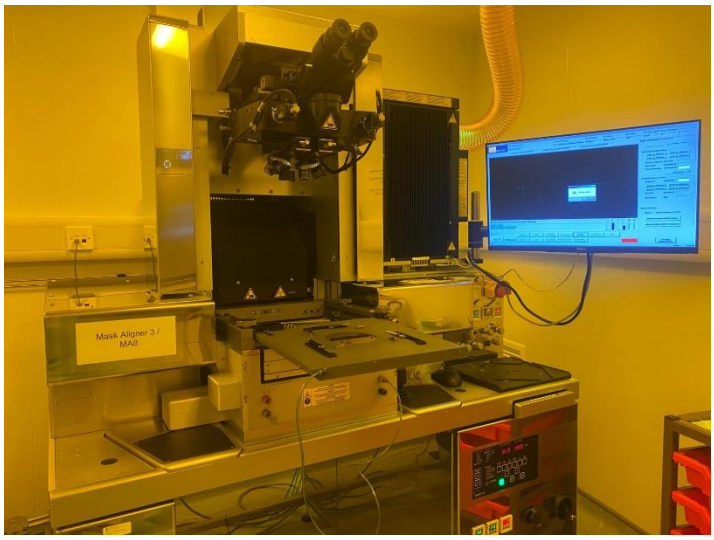


Figure 3.3 Karl Suss MA8 mask aligner.

3.3.2 Electron-Beam Lithography

Electron beam lithography (EBL) is a high resolution, maskless patterning technique that enables the direct transfer of nanoscale features onto a resist coated substrate using a focused electron beam. Because of its superior resolution and positioning accuracy, EBL is particularly suited for fabricating submicron device features, such as transistor gate foot or trench structures below 100 nm. In EBL, the desired pattern is defined in a computer aided design (CAD) file and directly written onto an electron sensitive polymer resist without the need for a physical mask. The interaction between the incident electron beam and the resist modifies its solubility, allowing selective development of exposed regions. Unlike photolithography, EBL permits the selection of different exposure doses within a single write, allowing local dose optimisation to compensate for variations in resist thickness and proximity effects. EBL processing in this work was carried out at the JWNC using a high-resolution electron beam lithography system. In this project, the Raith EBPG 5200 (shown in Figure 3.4) was used exclusively for defining the gate foot region, where feature sizes down to 200 nm were required. The system can transfer nanoscale patterns with resolutions down to approximately 3 nm and provides high alignment accuracy of ±0.5 nm.



Figure 3.4 Raith EBPG 5200 electron-beam lithography tool.

3.3.3 Photoresists

Photoresist is a polymer material that is sensitive to ultraviolet (UV) radiation and is used as a temporary masking layer during lithographic pattern transfer. The photoresist is applied

uniformly to the wafer surface, typically by spin coating, to ensure good thickness uniformity across the sample. The resist thickness is controlled by adjusting the rotation speed, and spin duration. Photoresists are broadly classified into positive and negative types based on their response to UV exposure. In positive photoresists, exposure to UV radiation breaks the polymer bonds, making the exposed regions soluble in the developer. Consequently, the exposed areas are removed during development, while the unexposed regions remain intact. In contrast, negative photoresists undergo cross-linking in the exposed regions, resulting in stronger bonds. During development, the unexposed regions are removed, whereas the exposed areas remain on the substrate. Illustrations of the exposure and development for positive and negative photoresists are shown in Figure 3.5

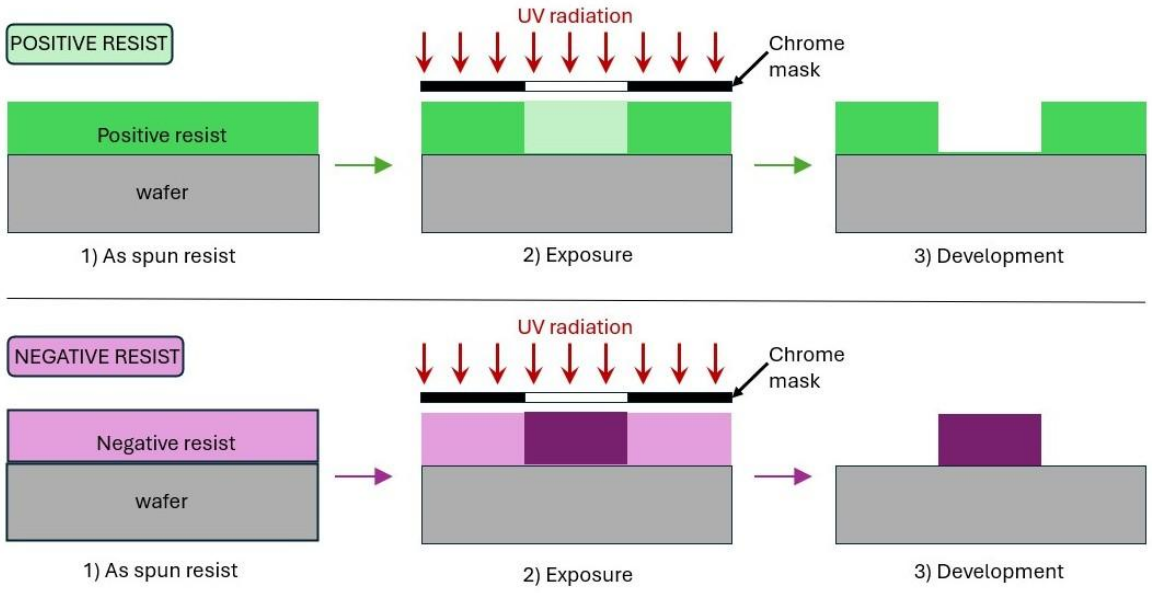


Figure 3.5 Schematic illustration of spin coating and development processes for positive and negative photoresists.

3.4 Metallisation

Metallisation is one of the most critical steps in semiconductor device fabrication, as it enables the formation of metal - semiconductor contacts required for electrical connection between the device and the external circuitry. The quality of these contacts strongly influences the overall device performance. Several techniques are available for depositing metals onto semiconductor surfaces, including electron beam evaporation, sputtering, and electroplating. In this research work, electron beam evaporation was primarily employed for metal deposition.

3.4.1 Electron-Beam Metal Evaporation

Electron beam metal evaporation is a vacuum deposition technique in which a focused electron beam is used to vaporise a solid metal source, resulting in the deposition of a thin metal film onto a substrate. The metal source is held in a water-cooled crucible, ensuring that only the surface region exposed to the electron beam evaporates. This localised heating minimises contamination from the crucible and enables the deposition of high purity metal films.

In this work, metal evaporation was carried out using the Plassys MEB 450 (Plassys IV) and Plassys Evap 7 systems. The Plassys Evap 7 system used for metal deposition is shown in Figure 3.6. These tools consist of a high vacuum chamber, an electron beam gun, a metal source, a substrate holder, and a monitoring system. Prior to deposition, the wafer is loaded into the chamber, which is then evacuated to a vacuum level typically in the range of 10^{-6} to 10^{-8} Torr. The high vacuum reduces collisions between evaporated metal atoms and residual gas molecules, enabling uniform and directional deposition [105]. The electron beam gun generates electrons via thermionic emission from a heated filament. A high voltage accelerates the electrons towards the metal source, while magnetic fields focus them into a narrow beam. Unlike resistive thermal evaporation, the crucible remains water-cooled, preventing unwanted heating and eliminating the risk of crucible material evaporation, which improves film purity. During, the initial heating stage, a shutter shields the substrate to prevent uncontrolled deposition. Once a stable evaporation rate is achieved, the shutter opens and metal deposition begins. The deposited film thickness is monitored in situ using a quartz crystal microbalance (QCM) [106], allowing accurate control of the final metal thickness. Typical deposition rates used in this work were in the range of 0.3–0.5 nm/s, providing precise thickness control. Film uniformity is enhanced by rotating or angling the substrate holder during deposition. After the target thickness is reached, the shutter is closed, and the chamber is vented before unloading the wafer. The schematic diagram for the evaporator is shown in Figure 3.7 [106]. An additional capability of the Plassys IV and Evap 7 systems is an internal argon (Ar) ion source positioned behind a secondary shutter, enabling in-situ Ar surface treatment/cleaning prior to metallisation. In this project, Ar pre-treatment was used before Ohmic metal deposition to remove native surface oxides.

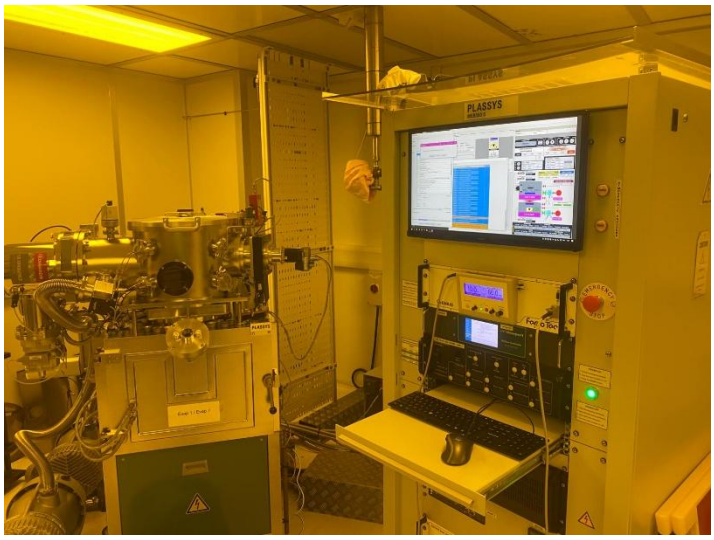


Figure 3.6 Photo of the metal evaporation tool Evap 7.

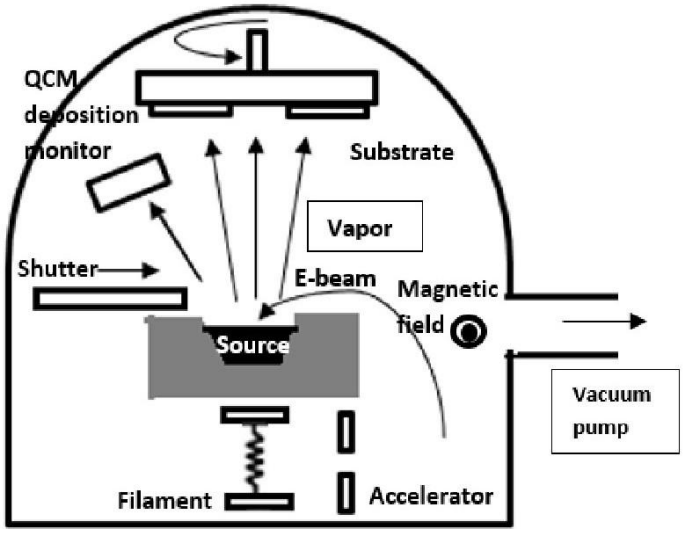


Figure 3.7 Schematic representation of the electron-beam evaporation metallisation mechanism.

3.4.2 Metal Lift-Off

The metal lift off technique is a widely used patterning method for defining metal features on semiconductor surfaces, particularly when directional deposition methods such as evaporation are used. Because evaporated metal travels predominantly in a vertical direction, it deposits uniformly on all exposed surfaces. This directional nature makes lift-off an effective approach for selectively forming metal patterns. In a typical lift-off process, a resist

layer is first applied to the semiconductor surface, and windows are opened in the resist at locations where metal deposition is required. These windows are defined using lithographic techniques either UV photolithography or e-beam lithography. After patterning, metal is blanket-deposited over both the exposed semiconductor regions and the remaining resist. The substrate is then immersed in a solvent such as acetone or a dedicated resist stripper, which dissolves the resist and removes the metal deposited on top of it. As a result, metal remains only in the previously opened windows on the semiconductor surface.

A critical requirement for a successful lift-off process is the formation of an undercut profile in the resist. The undercut ensures that the metal deposited on the resist surface is physically disconnected from the metal deposited directly on the semiconductor. This discontinuity allows the solvent to access and remove the resist underneath the metal, enabling clean lift-off without metal residues.

3.4.2.1 Lift-Off in Photolithography

In photolithography, lift-off can be achieved using either a single layer or a bilayer photoresist process. For a single layer lift-off process, photoresists such as S1805 or S1818 can be used by pre-exposing the resist to a developer (MF319) before the UV exposure step. This pre-development treatment hardens the top surface of the resist, making it less sensitive to the developer. Consequently, the lower part of the resist develops faster than the top, resulting in an undercut profile. The single layer resist lift-off procedure is illustrated in Figure 3.8(a). Alternatively, and more reliably, a bilayer photoresist system can be used. In this project, two resists with different development rates are used, LOR3A as the bottom layer and S1805 as the top layer. The bottom resist develops faster, naturally forming an undercut beneath the top resist. This bilayer configuration allows the resist stripper to easily access the resist beneath the metal, ensuring complete removal of unwanted metal during lift-off. The bilayer resist lift-off procedure is illustrated in Figure 3.8(b).

3.4.2.2 Lift-Off in Electron-Beam Lithography

For e-beam lithography, undercut profiles are typically achieved using multilayer resist systems with different molecular weights. Resists with lower molecular weight are more sensitive to electron exposure and therefore develop faster than higher molecular weight resists. By using a bilayer or tri layer resist stack where the lower layer has a smaller molecular weight an undercut profile can be formed after development. This approach is

particularly important for high resolution features and complex structures such as T-gates. The tri layer resist lift-off procedure is illustrated in Figure 3.8(c).

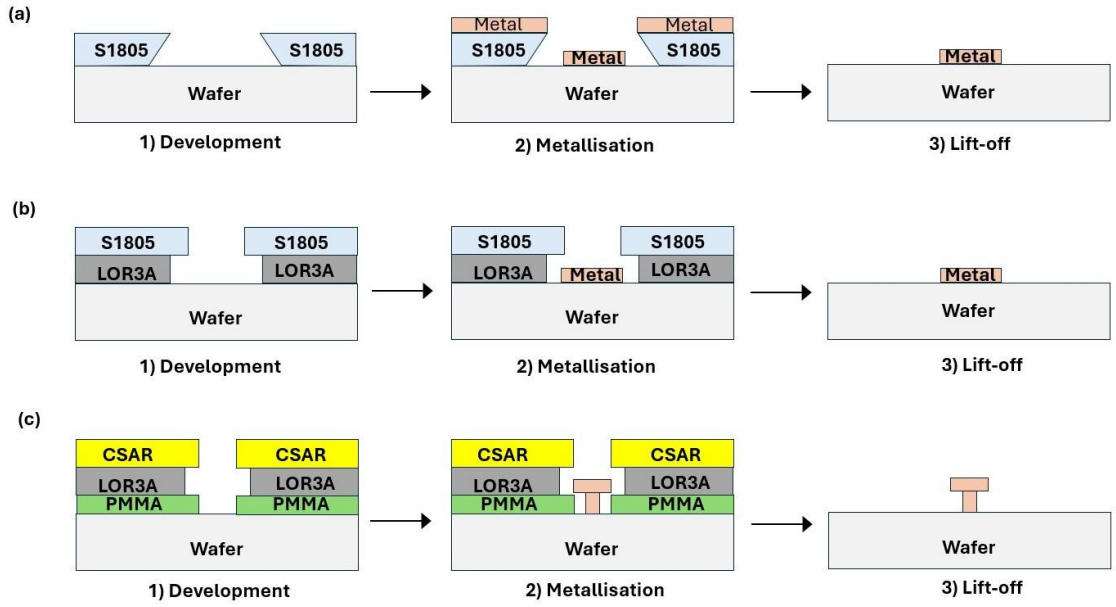


Figure 3.8 Metal lift-off process flow using (a) a single layer photoresist, (b) a bilayer photoresist, and (c) a tri layer photoresist system.

The general metal lift-off process using a bilayer photoresist can be summarised as follows:

1. Spin-coat the first (bottom) photoresist layer with a lower density or higher sensitivity to achieve an undercut profile.
2. Spin-coat the second (top) photoresist layer with higher density.
3. Expose the resist stack using UV light through a photomask corresponding to the desired metal pattern.
4. Develop the resist to remove exposed regions and reveal the patterned substrate.
5. Perform a descum step to eliminate any residual resist and ensure a clean surface.
6. Carry out surface deoxidation, which is particularly critical for ohmic contact formation.
7. Deposit the required metal stack using a directional evaporation technique.
8. Immerse the sample in a resist stripper or acetone to dissolve the photoresist and lift off the excess metal.

For reliable lift-off, the total deposited metal thickness must be less than the thickness of the bottom resist layer. This ensures the presence of a sufficient overhang and maintains metal discontinuity, which is essential for clean and reproducible lift-off results.

3.5 Rapid Thermal Annealing

Rapid thermal annealing (RTA) is a key process in semiconductor fabrication in which a wafer is heated to high temperature in a controlled ambient, such as nitrogen (N_2) or forming gas, to modify its electrical properties. In semiconductor device processing, RTA is commonly used for dopant activation and to promote interfacial reactions in metal semiconductor contacts. For GaN HEMT devices with a Ti/Al/Ni/Au metal stack, conventional Ohmic contact formation requires annealing at temperatures between 750 °C and 950 °C for 30–45 s in an N_2 ambient. This thermal treatment enables the reaction of Ti with the underlying nitride layer, forming a TiN alloy beneath the contact and facilitating electron transport into the 2DEG. For these processes, the Jipelec JetFirst 200 RTA system, shown in Figure 3.9, was used, and it was also employed for the dopant activation of silicon implanted wafers at 1100 °C (for 2 minutes).



Figure 3.9 Photo of the Jipelec JetFirst 200 RTA tool.

3.6 Etching

Etching is a material removal process used to selectively remove metals, semiconductors, or dielectric layers from a wafer. It is commonly applied in device mesa isolation, selective

material removal for device patterning, and the formation of vias connecting the front and back sides of a wafer. During etching, the etchant whether liquid or gaseous can attack both the exposed wafer surface and the masking layer. Therefore, the photoresist mask must be sufficiently thick to withstand the etching conditions. In addition to photoresists, e-beam resists, metals, and other materials such as dielectrics and polyimide can also serve as etch masks. Etching is generally classified into two methods: wet etching, where the etchant is a liquid solution, and dry etching, where the etchant is gaseous.

3.6.1 Dry Etching

Dry etching of GaN is a plasma-based process used to selectively remove material from the substrate. Plasma is generated by applying a high frequency electrical field to a gas mixture, producing reactive species that interact with the GaN surface. These species react with the material to form volatile by-products, which are subsequently removed, resulting in material removal with predominantly vertical etch profiles. The gas mixtures used typically consist of a reactive gas, such as chlorine or fluorine based species, combined with an inert gas like argon or helium [107], [108]. The choice of gas chemistry determines the selectivity of the process, allowing specific layers to be etched while stopping on underlying materials of different composition. Compared to wet etching, dry etching offers improved control over etch depth and sidewall profile due to its anisotropic nature.

In this project, dry etching was carried out using two techniques: Reactive Ion Etching (RIE) for etching dielectrics and Inductively Coupled Plasma (ICP) etching for the GaN based heterostructures. RIE employs a single RF power source that controls both ion density and ion energy, in this study, an SF_6/N_2 chemistry was used for the RIE process with typical SiN_x etch rates of approximately 7.5 nm/min. ICP etching, in contrast, utilises separate RF and DC power sources, enabling independent control of ion energy and plasma density. The Oxford Instruments ICP 180 system, shown in Figure 3.10 was used for mesa isolation and for the shallow recess etching processes used in this research. Cl_2/Ar and BCl_3/Cl_2, chemistries were utilised in the ICP system. Chlorine based ICP etching has been reported in the literature to achieve GaN etch rates of up to 1 μm/min [109]. This process was used for device isolation by etching the epitaxial layers down to the semi insulating buffer layer, corresponding to a typical etch depth of around 150–200 nm. Process parameters such as gas flow rates and chamber pressure can be adjusted to enhance etch directionality and preserve

lithographically defined features. Figure 3.11 illustrates a dry etching process performed after pattern definition using photolithography.



Figure 3.10 Oxford Instruments ICP 180 system used for dry etching of the GaN based heterostructures.

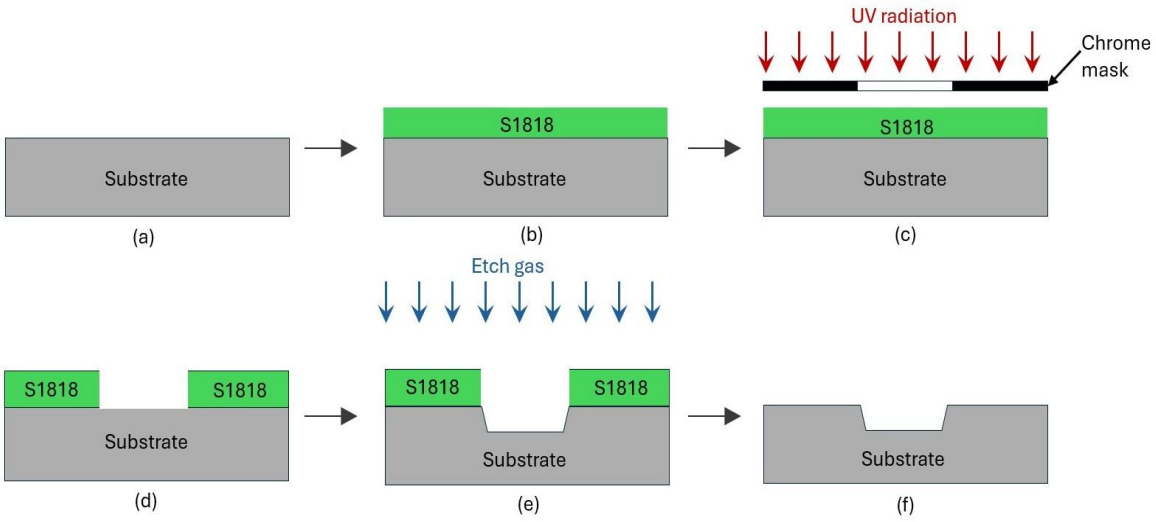


Figure 3.11 Schematic illustration of a dry etching process using S1818 photoresist.

3.6.2 Wet Etching

Wet etching is a material removal process that relies on chemical reactions between a liquid etchant and the wafer surface. One of its main advantages is that it is generally less damaging to underlying layers, reducing the risk of device degradation. However, wet etching occurs in both vertical and lateral directions, resulting in isotropic etch profiles with limited control over sidewall geometry, and wafer scale uniformity is typically limited. GaN exhibits high chemical stability, making it highly resistant to conventional wet etching. In addition, wet etching of GaN is polarity dependent, with N-polar GaN being more reactive than Ga-polar GaN. Since the epi-structures used in this work are Ga-polar, wet etching is not suitable for the removal of GaN epi-layers, and dry etching is therefore preferred for GaN processing. In this project, wet etching was used for the removal of the SiO_2 layer. Following implantation and dopant activation, the SiO_2 layer was removed using a buffered oxide etchant (6:1 BOE), composed of hydrofluoric acid (HF) and ammonium fluoride (NH_4F), commonly known as buffered HF, as detailed in Chapter 5.

3.7 Dielectric material deposition

Dielectric layers are commonly used during GaN device fabrication for electrical insulation, surface protection, masking and structural support. Several deposition techniques can be used for this purpose, including physical vapour deposition (PVD), plasma enhanced chemical vapour deposition (PECVD) and atomic layer deposition (ALD). Among these techniques, PECVD is widely used for the deposition of dielectric films such as silicon dioxide (SiO_2) and silicon nitride (SiN_x), as it ensures relatively uniform film deposition at moderate substrate temperatures.

In PECVD, precursor gases are introduced into a vacuum chamber containing the substrate and are activated using a plasma. Energetic electrons within the plasma dissociate and ionise the precursor gases, producing reactive species that react at the substrate surface to form the required dielectric film.

In this research, dielectric deposition was carried out using an Oxford Instruments PlasmaPro 100 PECVD system, shown in Figure 3.12. The tool is a load locked PECVD system capable of depositing dielectric materials including SiO_2 and SiN_x. For the ion implantation process in this research (described in Chapter 5 & 6), the SiO_2 layer was first used as a retarding layer prior to Si ion implantation and was later deposited again as an encapsulation layer before the high temperature dopant activation anneal step.



Figure 3.12 PlasmaPro 100 PECVD system used for SiO_2 and SiN_x deposition.

3.8 Summary

This chapter described the epitaxial growth techniques for GaN HEMTs, followed by an overview of the key fabrication techniques used in GaN device processing, including lithography, dielectric deposition, dry etching and metallisation. The equipment employed in this work was also presented. The process and techniques described here were used in the study of Ohmic contacts for GaN HEMTs described in the next three chapters.

4 Patterned Ohmic Contacts for GaN-based HEMTs

4.1 Introduction

Ohmic contacts are crucial for the performance of GaN based HEMTs. Low resistance Ohmic contacts enable efficient carrier injection into the 2DEG, minimise power loss, and support high frequency operation. However, owing to the wide bandgap of GaN and the resulting high Schottky barrier height at the metal semiconductor interface, achieving Ohmic contacts with low contact resistance remains a significant challenge. To reduce the Ohmic contact resistance, the effective barrier can be engineered either by reducing the barrier thickness, thereby facilitating carrier tunnelling, or by lowering the barrier height at the metal semiconductor interface [110],[111].

This chapter provides a review of approaches to Ohmic contact resistance reduction in GaN-based HEMTs followed by a study on patterned Ohmic contacts.

4.2 Approaches to Contact Resistance Reduction

The performance and reliability of GaN based HEMTs are strongly influenced by the quality of the Ohmic contacts formed at the source and drain terminals. Low Ohmic contact resistance, smooth surface morphology, and thermal stability are essential for high frequency, high temperature and high power operation [112]. In particular, low resistance Ohmic contacts enable efficient carrier transport from metal electrodes into the semiconductor, directly impacting device efficiency and power handling capability [113], [114].

Achieving low-resistance Ohmic contacts in both AlGaN/GaN and AlN/GaN HEMTs remains challenging due to their intrinsic material properties, including wide bandgap and high electron affinity. Without effective Ohmic contact technology, overall device performance and thermal stability can be severely compromised. To address these challenges, a broad range of Ohmic contact technologies has been explored, including optimisation of metal stacks and annealing conditions, surface and interface treatments, recess etching, selective regrowth and ion implantation techniques. Each approach involves trade-offs in terms of process complexity and integration.

4.2.1 Optimisation of Metal Stacks

The formation of low resistance Ohmic contacts in HEMTs plays a critical role in determining device performance. Comprehensive analyses by [85] and [115] examine the mechanisms governing Ohmic contact formation, highlighting the importance of both metal stack configuration and processing conditions. In practice, many metallisation schemes used for AIN/GaN and AlGaN/GaN heterostructures are adapted from optimised processes originally developed for GaN or n-type GaN. Early investigations into Ohmic contacts on n-type GaN explored the use of aluminium (Al) [116], titanium (Ti) [117], and titanium/aluminium (Ti/Al) bilayers [118]. Building upon this foundational work, the Ti/Al/X/Au metallisation scheme where X may be platinum (Pt), nickel (Ni), or molybdenum (Mo) emerged as a standard approach. Variants such as Ti/Al/Pt/Au [119], Ti/Al/Ni/Au [120], [121] and Ti/Al/Mo/Au [122], [123] have been widely reported in the literature. Each layer within these metal stacks serves a specific function. The roles of the individual metals, from the semiconductor interface to the top contact layer, are discussed below.

Titanium (Ti): Titanium plays a critical role in the formation of Ohmic contacts to AlGaN/GaN and AlN/GaN heterostructures. During annealing, Ti reacts with nitrogen from the AlGaN barrier to form titanium nitride (TiN), which facilitates close contact with the semiconductor and contributes to effective barrier thinning at the metal semiconductor interface [124], [125]. This interfacial reaction is a key step in ensuring Ohmic behaviour. In addition, the formation of TiN is accompanied by the creation of nitrogen vacancies in the AlGaN layer beneath the contact. These vacancies increase the electron concentration near the interface and enhancing electron transport from the metal contact into the 2DEG [126], [127].

Aluminium (Al): During annealing, Al reacts with Ti to form Al_3Ti, which help suppress oxidation of the Ti layer and preserve its reactivity at the interface [128]. This interaction supports the formation of a low resistance contact by maintaining the effectiveness of the Ti semiconductor reaction.

Nickel (Ni), Platinum (Pt), and Molybdenum (Mo): Nickel, platinum, and molybdenum are commonly used as diffusion barrier layers in Ohmic contact stacks. Their primary function is to prevent the interdiffusion of gold into the underlying layers and to limit the upward diffusion of aluminium during high temperature annealing. This diffusion control is

essential for avoiding the intermixing of Al with Au, which would result in a highly resistive alloy, and is therefore essential for maintaining consistent electrical characteristics across the contact area. In addition, these metals contribute to improved surface morphology after annealing, which is critical for reliable device performance [129].

Gold (Au): Gold is typically used as a capping layer in Ohmic contact stacks. Its primary role is to protect the underlying metal layers from oxidation during subsequent processing steps. Gold also enhances the overall conductivity of the contact and provides a robust interface for external electrical connections, such as bonding wires or probes [130].

A key advantage of metal stack optimisation is that low-resistance contacts can be achieved without intentionally modifying the semiconductor through recess etching, regrowth or implantation. The approach is also well established in GaN HEMT fabrication. However, the electrical performance and surface morphology of alloyed contacts are strongly influenced by the metal composition, thickness of the individual layers, and annealing conditions. Conventional Ti/Al-based contacts typically require high temperature annealing, which can promote interdiffusion between the metal layers and result in degradation of the contact surface morphology.

4.2.2 Regrown Ohmic Contacts

Regrowth provides a different approach to reducing Ohmic contact resistance by introducing a highly doped semiconductor layer within the source and drain contact regions. Typically, the barrier material in these regions is selectively removed and highly doped n^+- or n^{++}-GaN is subsequently regrown. The highly doped GaN provides a low-resistance path between the metal contact and the 2DEG and can enable low-resistance contacts. Regrown contacts have demonstrated some of the lowest contact resistance values reported for GaN HEMTs, with R_c as low as 0.02 Ω·mm [131].

The main advantage of regrowth is therefore the very low contact resistance that can be achieved. The technique can also avoid the high temperature post-metallisation alloying required by many conventional Ti/Al-based contacts. However, these advantages are accompanied by increased fabrication complexity because regrowth requires additional processing of the source and drain contact regions and an additional epitaxial growth step [132]

4.2.3 Recess Ohmic Contact Technology

Recess Ohmic contact technology is an approach for reducing contact resistance in GaN based HEMTs by locally modifying the barrier layer beneath the source and drain contacts [133], [134]. In conventional AlGaN/GaN and AlN/GaN heterostructures, the wide bandgap barrier separates the metal contact from the 2DEG, limiting carrier transport across the metal semiconductor interface. Recess etching addresses this limitation by partially or fully thinning the barrier prior to metallisation, thereby reducing the effective tunnelling distance [135], [136]. The performance of recessed Ohmic contacts depends critically on etch depth control and uniformity. Insufficient etching results in limited reduction of contact resistance, whereas excessive etching can damage the GaN channel or degrade the 2DEG density [137], [138]. This sensitivity is especially pronounced in AlN/GaN heterostructures, where the barrier is typically only a few nanometres thick. For example, [110] recessed a 5.5 nm AlN barrier by 2.5 ± 0.5 nm, leaving approximately 3 nm beneath the Ohmic contact. Following metallisation and annealing, the recessed contacts exhibited an average R_c of 0.7 ± 0.2 Ω·mm, with a minimum of 0.5 Ω·mm, compared with 1.6 Ω·mm for non-recessed contacts.

4.2.4 Selective Patterned Recess Technique

The concept of fabricating an uneven surface beneath the Ohmic contact in AlGaN/GaN structures is aimed at optimising contact resistance by creating specific patterns (like arrays of horizontal lines or holes) in the Ohmic contact region. This technique involves selectively etching the AlGaN layer to create regions with depleted and higher density 2DEG. Figure 4.1 illustrates a selectively patterned AlGaN/GaN structure.

The uneven surface allows the metal and the high-density 2DEG to come into closer proximity than would be possible with uniformly thick AlGaN layers, thus reducing the overall contact resistance. When electric fields at the boundary of these thin and thick regions of AlGaN bend or fringe this bending increases the effective area of interaction between the metal and the 2DEG, which is otherwise limited in uniform structures. This fringing effect, enhanced by the recessed ohmic contact, effectively brings the metal in closer contact with areas of high 2DEG concentration. By effectively shortening the path that electrons have to travel from the 2DEG to the metal, the overall resistance at the contact interface is reduced [139], [140]. Low R_c values of approximately 0.10–0.15 Ω·mm have been reported for hole-

etched Ohmic structures using Ti/Al/Ni/Au annealed at 830 °C for 30 s, compared with 0.38–0.43 Ω·mm for conventional structures investigated in the same study [141].

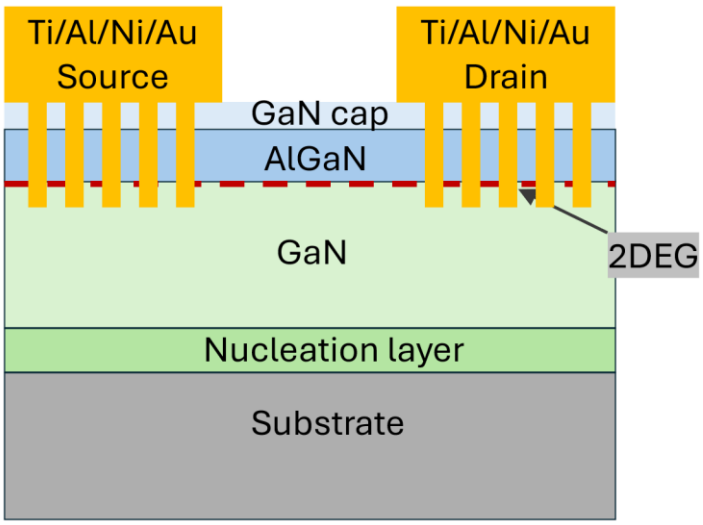


Figure 4.1 Selectively patterned recessed AlGaN/GaN structure

4.2.5 Ion-Implanted Ohmic contacts

Ion implantation is an effective method for reducing Ohmic contact resistance in GaN-based HEMTs by selectively forming highly doped regions beneath the source and drain contacts. Si is commonly used as the donor species, with implantation followed by high temperature activation annealing producing highly doped regions. The increased donor concentration reduces the depletion width at the metal–semiconductor interface, thereby enhancing carrier tunnelling and facilitating the formation of low-resistance Ohmic contacts[142],[143]

However, implantation-induced lattice damage necessitates careful optimisation of implantation conditions and thermal treatment to prevent degradation of AlGaN/GaN and AlN/GaN HEMT heterostructures.

The literature discussed above demonstrates that low-resistance Ohmic contacts have been achieved using different combinations of semiconductor modification, metallisation and thermal processing. Tables 4.3 and 4.4 summarise selected reported Ohmic contact results for AlN/GaN and AlGaN/GaN HEMTs, respectively. Since the reported structures differ in material properties, contact geometry and processing conditions, the values are presented as representative literature results rather than as a direct performance comparison between the different techniques. For each semiconductor modification approach, the lowest reported R_c among the studies considered is highlighted in bold.

Overall, Ohmic contact resistance can be reduced through optimisation of the metal–semiconductor contact, modification of the barrier within the contact region, or local enhancement of the carrier concentration. However, each approach involves different requirements in terms of fabrication complexity, thermal processing and integration with the overall device process. Consequently, this work focuses on the use of optimised metal stacks, patterned recess etching and ion implantation for low Ohmic contact development in AlGaN/GaN and AlN/GaN HEMTs.

Table 4.1 Selected reports of Ohmic contact techniques for AlN/GaN HEMTs.

Semiconductor Modification	Metal schemes (nm)	2DEG density (cm^{-2})	μ (cm^2/V. s)	RTA Conditions	R_c Ω.mm	R_{sh} Ω/□	Ref
Si Implantation	Ti/Al/Ni/Au 30/180/40/100	1.6 * 10^{13}	1600	800 °C, 30 secs, N_2	0.46	110	This work
No modification	Ti/Al/Ni/Au 30/180/40/100	-	-	800 °C, 30 secs, N_2	0.4	300	[144]
No modification	Ti/Al/Ni/Au 30/180/40/100	1.6 * 10^{13}	1450	800 °C, 30 secs, N_2	0.6	300	[144]
No modification	Ti/Al/Ni/Au 30/180/40/100	2.2 *10^{13}	1250	800 °C, 30 secs, N_2	0.49	159	[145]
Recess	Ti/Al/Ni/Au 30/200/40/10	2.5 *10^{13}	700	800 °C, 30 secs, N_2	**0.5**		[146]
No modification	Ti/Al/Ni/Au 30/175/35/60	2.5 *10^{13}	1510	950 °C, 30 secs, N_2	0.33	168	[147]
No modification	Ta/Al/Ni/Au 20/160/55/45	2.2 *10^{13}		830 °C, 60 secs, N_2	**0.08**		[148]
No modification	Ti/Al/Ni/Au	1*10^{13}	900		0.8 - 2		[149]
No modification	Ti/Al/Ni/Au	1.9 *10^{13}	965	850 °C, 60 secs, N_2	0.45		[150]
Si implantation	Ti/Al	-	-	-	0.3	-	[151]
Si implantation	Ti/Al	1.1 *10^{13}	1480	-	0.3	376	[152]
Si implantation	Ti/Al/Ni/Au 30/200/40/10			825 °C, 30 secs, N_2	**0.14**	119	This work

Table 4.2 Selected reports of Ohmic contact techniques for AlGaN/GaN HEMTs.

Semiconductor or modification	Metal schemes (nm)	2DEG density (cm^{-2})	μ (cm^2/V. s)	RTA Conditions	R_c Ω.mm	Ref
Si ion implantation	Ti/Au/Ni/	-	-	Non-alloyed	0.2	[153]
Si ion implantation	Ti/Al/Ni/Au 25/200/60/100	$1.02 * 10^{13}$	500	750 ℃, 30 s, N_2	0.44	[143]
Si ion implantation	Ti/Ni/Au/Ni	$1.15 * 10^{13}$	2050	Non-alloyed	0.2	[154]
Si ion implantation	Ti/Al/ 30/200/			550 ℃, 1 min, N_2	**0.09**	[155]
Si ion implantation	Ti/Al/Ni/Au/Ti/ Pt	-	-	870 ℃, 30 secs, N_2	0.1	[156]
No modification	Ta/Al/Ta/	$9.10 *10^{12}$	2266			[18]
Recessed	Ti/Al/Ni/Au 15/80/20/100	-	-	800 ℃, 30 secs, N_2	0.2	[133]
Recessed	Ti/Al/Ni/Au	$9.0*10^{12}$	2000	850 ℃, 30 secs, N_2	0.12	[121]
Recessed	Ti/Al/Ni/Au	$1.36*10^{13}$	1936	830 ℃, 60 secs, N_2	**0.1**	[141]
Recessed	Ti/Al/Ti	$1.07*10^{13}$	1966	550 ℃, 60 secs, N_2	0.15	[157]
No modification	Ti/Al/Ni/Au	$1.13*10^{13}$	1360	860 ℃, 30 secs, N_2	0.85	[158]
No modification	Ti/Al/Ti/Au 20/110/40/50	-	-	830 ℃, 45 secs, N_2	0.75	[159]
No modification	Ti/Al/Ni/Au 20/110/40/50	-	-	830 ℃, 45 secs, N_2	1.3	[159]
No modification	Ti/Au/Al/Ni/Au (25/20/120/40/ 50)	-	-	830 ℃, 30 secs, N_2	0.5	[160]
Regrown	Ti/Au (20/100)	$7.63 * 10^{12}$	1620	-	0.1	[161]
Regrown	Ti/Au	-	100	-	**0.06**	[132]

4.3 Experimental Investigation of Patterned Ohmic Contacts

In this study, different Ohmic recess patterns were investigated as a means of reducing the contact resistance in AlGaN/GaN heterostructures. Dry etching was used to selectively recess the AlGaN/GaN prior to metallisation, with the etched regions extending into the GaN channel. Three contact structures were investigated: a 4 µm × 150 µm horizontal recess extending across the Ohmic contact region, a 4 µm × 10 µm selective edge recess positioned on either side of the contact, and a conventional planar contact without recess etching. These structures were used to investigate the effect of the extent and position of the recess on the resulting Ohmic contact resistance and sheet resistance, with the conventional planar contact serving as a reference for evaluating the performance of the patterned recess structures.

4.3.1 TLM Fabrication

The epitaxial layer structure used in this work is illustrated in Figure 4.2**.** The wafer was grown at Qrona Technologies, USA, using the molecular beam epitaxy (MBE) technique on a 1-mm thick, single-side polished (SSP) sapphire substrate. The structure of the wafer, from the top layer down, includes a 2-nm thick GaN cap layer, a 20-nm thick AlGaN (~35%) barrier layer, a 2µm thick GaN channel layer, followed by a 0.6µm iron (Fe) doped buffer layer and a 30-nm AlN nucleation layer.



Figure 4.2 Schematic of the AlGaN/GaN HEMT.

In this project, the fabrication was carried out using the photolithography method. A mask, essential for pattern transfer, was designed using Tanner-EDA's L-edit software, as illustrated in Figure 4.3**.** This mask was divided into four sections, each containing different patterned TLM structures arranged in a repetitive sequence. Additionally, alignment markers were included in each section to facilitate the alignment of various layers during the exposure process.

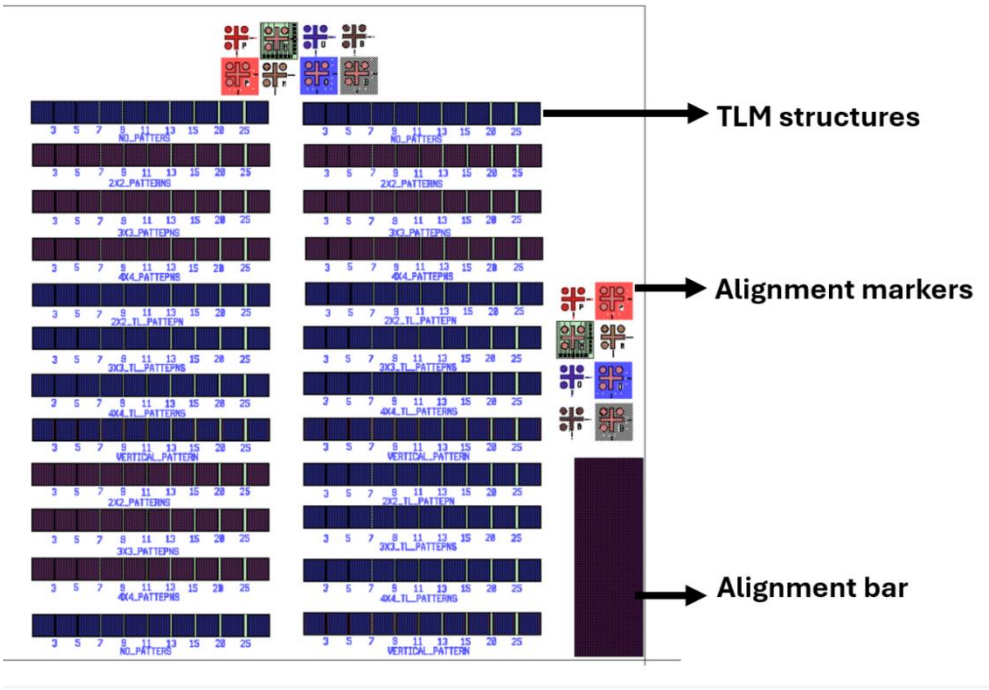


Figure 4.3 Photolithography mask with TLM structures and alignment markers.

Figure 4.4 shows micrographs of three TLM contact structures investigated in this experiment. The first pattern, shown in Figure 4.4(a), consists of horizontal recessed lines approximately 4 × 150 µm in size and spaced 4 µm apart. The second pattern, shown in Figure 4.4(b), consists of smaller horizontal recessed lines approximately 4 × 10 µm in size and spaced 4 µm apart. These recessed regions were positioned near the edges of the Ohmic contacts to investigate the effect of recessing within the transfer length region. The third structure, shown in Figure 4.4(c), consists of a conventional planar contact without recess etching, which served as a reference for evaluating the performance of the patterned recess structures. All three TLM structures used the same contact spacings of 3, 5, 7, 9, 11, 13, 15, 20 and 25 µm. The three structures were fabricated on the same sample and repeated at different locations across the sample.

The fabrication process began with cleaning the sample using acetone, isopropyl alcohol (IPA), and reverse osmosis (RO) water. Following cleaning, Ti/Pt (20/100 nm) alignment markers were deposited on the sample. These markers were used to align the subsequent lithography steps with the previously defined structures. The Ohmic recess patterns were then defined within the Ohmic contact regions and etched to a depth of approximately 32 nm using the ICP 180 system. The etch was performed at a chamber pressure of 20 mTorr using BCl_3/Cl_2 flow rates of 5/10 sccm, with ICP and RF powers of 100 and 15 W, respectively. The recess depth was selected to extend the Ohmic contact region below the 2DEG, consistent with recessed Ohmic contact approaches reported in similar research studies [162]. Mesa isolation was subsequently performed to electrically isolate adjacent structures. The mesa was etched using Cl_2/Ar flow rates of 30/15 sccm, RF/ICP powers of 75/750 W and a chamber pressure of 4 mTorr for 1 min. Prior to Ohmic metal deposition, a 45 s in-situ Ar etch was performed to remove surface contamination and native oxide from the exposed contact regions. A Ti/Al/Ni/Au (30/180/40/100 nm) metal stack was then deposited by electron-beam evaporation. Finally, the Ohmic contacts were annealed by rapid thermal annealing (RTA) at 800 °C for 30 s in a nitrogen (N_2) atmosphere.

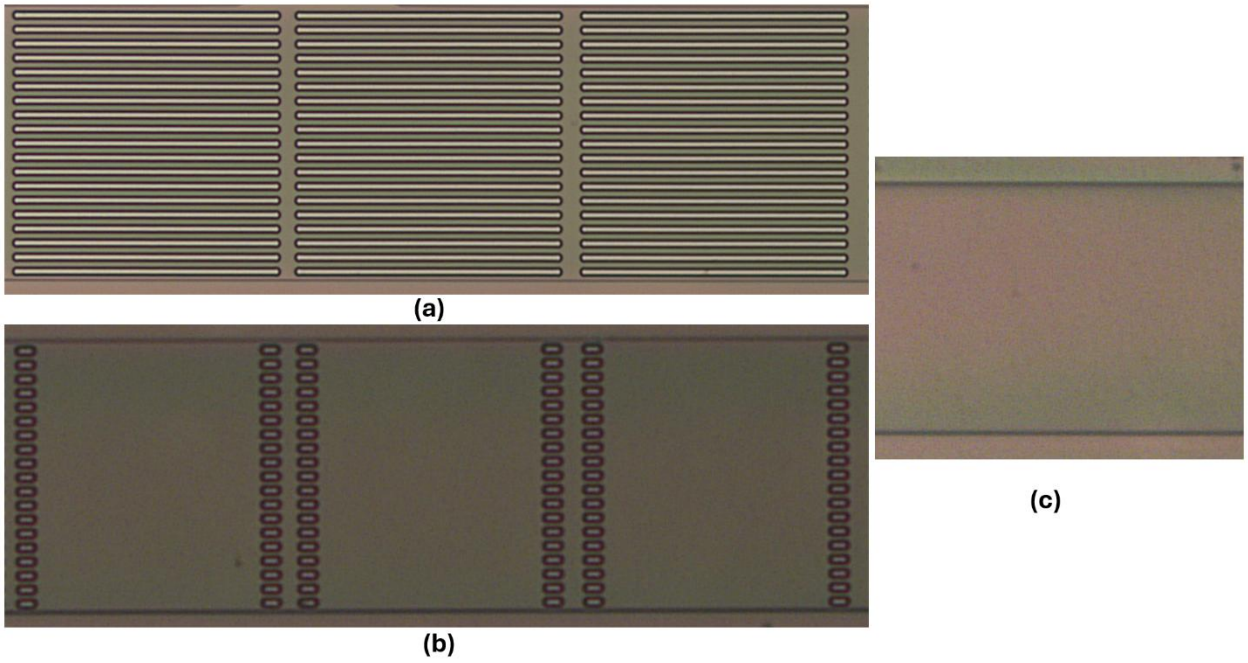


Figure 4.4 Optical microscope image of the patterned Ohmic contacts investigated: (a) horizontal pattern, (b) transfer region pattern, and (c) conventional planar contact without recess etching.

4.4 Results and Discussion

The Ohmic contact resistance of the different recess patterns was evaluated using the LTLM. Figure 4.5 shows the measured total resistance as a function of TLM gap spacing for the structures. The two selectively recessed structures produced similar contact resistance values. The 4 µm × 150 µm horizontal recess gave a contact resistance of 1.13 Ω·mm, while a slightly higher value of 1.18 Ω·mm was obtained for the 4 µm × 10 µm localised edge recess. The relatively small difference between these values indicates that reducing the patterned recess from a continuous horizontal region to a more localised region did not improve the contact resistance. In comparison, the conventional planar contact without recess etching exhibited the lowest contact resistance of 0.81 Ω·mm. This indicates that, under the fabrication conditions used in this work, the conventional planar contact provided lower contact resistance than either of the selectively recessed structures, suggesting that the introduction of the investigated recess patterns did not improve the Ohmic contact performance.

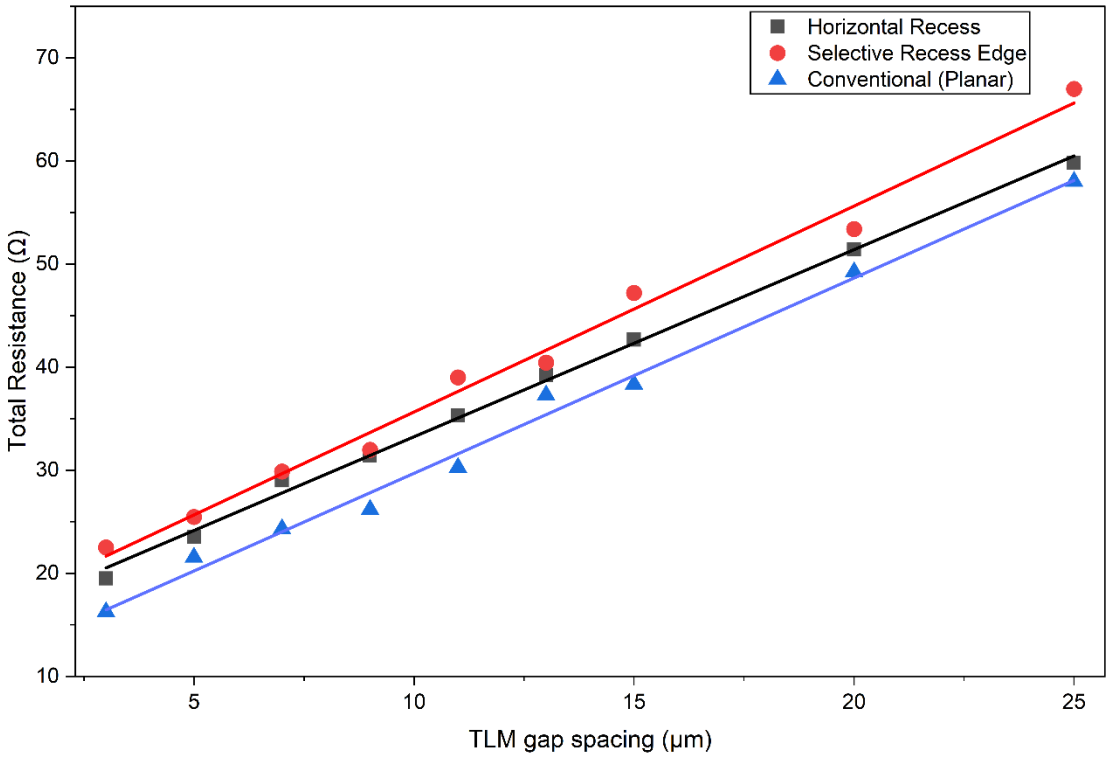


Figure 4.5 Total resistance as a function of TLM gap spacing for the horizontal recess, selective edge recess and conventional planar contact structures

This result differs from some previous studies [163], [164] in which patterned recesses produced lower contact resistance than conventional non - recessed contacts. For example, [164] reported a contact resistance of 0.18 Ω·mm for a patterned etched structure, compared with 0.46 Ω·mm for the conventional structure, and attributed the improvement to the additional metal-semiconductor interface created along the etched sidewalls. Similar improvements have also been reported for horizontal patterned recesses, where the increased sidewall contribution was proposed to improve current transport across the Ohmic contact [165].

However, the two patterned recess structures investigated in this work produced higher contact resistance than the planar (non-recessed) contact, as discussed above. This discrepancy may be associated with differences in pattern dimensions, recess depth, etching conditions and subsequent metallisation. Ion bombardment during ICP dry etching may have introduced defects and trapping states within the etched semiconductor regions, potentially degrading carrier transport towards the 2DEG. Furthermore, the directional nature of electron-beam evaporation may have resulted in nonuniform metal coverage along the recessed sidewalls, limiting the additional current injection pathways expected from patterned recessing. The absence of a dedicated post-etch wet chemical treatment, such as TMAH or KOH, may also have allowed plasma-induced surface damage to persist; such treatments can modify or remove damaged surface material under suitable processing conditions. These mechanisms provide possible explanations for the higher contact resistance observed, although their individual contributions were not experimentally verified. Under the conditions investigated in this work, patterned recessing therefore did not improve Ohmic contact resistance relative to the planar (non-recessed) contact.

4.5 Summary

This chapter discussed approaches for improving Ohmic contacts in GaN-based heterostructures. Three Ohmic contact structures were investigated: a localised recess within the transfer length region, a horizontal recess pattern, and a conventional planar contact without recess etching. The fabricated structures were characterised to determine their contact and sheet resistances and assess the influence of the different contact configurations on the characteristics. The measured contact resistances were 1.18 Ω·mm, 1.13 Ω·mm, and 0.81 Ω·mm for the transfer length region, horizontal recess, and conventional planar contact, respectively. The similar values obtained for the two localised patterns indicate that their different configurations had only a small influence on contact resistance. In contrast, the conventional planar contact produced the lowest contact resistance, indicating that the introduction of the patterned recesses did not improve the Ohmic contact resistance under the fabrication conditions investigated in this work. Overall, these results demonstrate that the performance of patterned recess contacts depends on the specific recess geometry and fabrication conditions, with the conventional planar contact providing the lowest contact resistance among the structures investigated.

5 Silicon Ion-Implanted Ohmic Contacts for GaN HEMTs

5.1 Introduction

Ion implantation is a technique used to modify the conductivity of semiconductors by introducing controlled levels of dopants. In the context of Ohmic contact formation, ion implantation enables localised doping beneath the contact metal, thereby reducing the Schottky barrier width and enhancing electron tunnelling. This chapter discusses the fundamentals of donor doping in GaN, the physics of ion implantation with emphasis on depth profiling using SRIM simulations, and the effects of implantation induced damage and post implantation annealing on Ohmic contact optimisation.

5.2 Donor Doping in GaN

N-type doping in GaN is predominantly achieved using silicon (Si) as a donor dopant. Si substitutes for gallium lattice sites and introduces shallow donor states, [166] enabling high electrical activation efficiency and electron concentrations exceeding $10^{19}\,\mathrm{cm}^{-3}$. The effectiveness of Si as a donor is attributed to its favorable incorporation on Ga sites and the formation of energetically stable Si–N bonds. As a result, Si remains the dominant n-type dopant for GaN [167]. For Ohmic contact formation, heavy donor doping near the metal semiconductor interface is critical. High donor concentrations reduce the depletion width at the interface, thereby enhancing electron tunnelling through the Schottky barrier and lowering contact resistance. Consequently, donor doping is widely used in the source and drain regions of GaN based FET to improve device performance.

Due to the strong bonding and high thermal stability of GaN, dopant incorporation by diffusion is ineffective. Ion implantation therefore provides a practical method for introducing dopants with precise control over dopant concentration as well as lateral and depth distributions [168]. Si ion implantation has been extensively used to achieve n-type doping in GaN and has been shown to enable very low Ohmic contact resistances [169]. However, high dose implantation introduces significant lattice damage, which can limit dopant activation and degrade material quality if not adequately managed.

While Si implantation in GaN has been well established in the literature, investigations targeting AlGaN/GaN HEMTs are limited, and donor implantation in AlN/GaN HEMTs

remains underexplored. As AlGaN/GaN and high barrier AlN/GaN heterostructures are increasingly adopted for high-performance GaN based devices, a detailed understanding of donor implantation, dopant activation, and implantation induced damage recovery in these HEMT structures is required.

5.3 Range and distribution of implanted ions

Ion implantation is the introduction of energetic, charged particles into a target substrate, resulting in a controlled distribution of implanted ions beneath the material surface. The implanted ion dose can vary widely depending on the application. When energetic ions enter a semiconductor substrate, they lose their energy progressively through collisions with both the electrons and nuclei of the target atoms. Eventually, the ions come to rest at some depth within the crystal lattice. The average depth at which the ions stop can be controlled by adjusting the acceleration energy of the implanted ions. The total distance an ion travels before coming to rest is called its range (R), while the projected range (R_p), is the average penetration depth measured along the original direction of the ion beam. Figure 5.1 illustrates the trajectory of ions in a substrate [170].

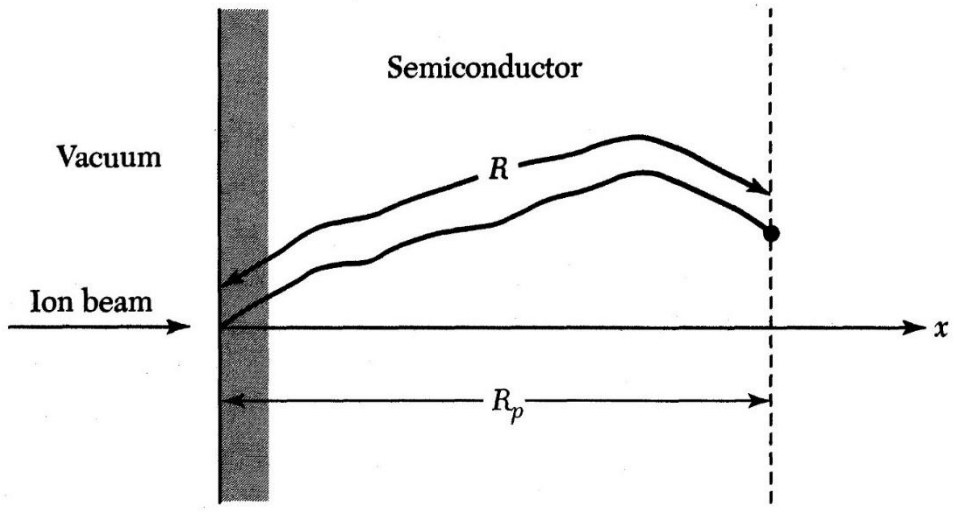


Figure 5.1 Ion incidence and trajectory within a semiconductor.

Due to statistical variations in collisions, not all ions stop at the same depth. Instead, they form a distribution that is approximately Gaussian in shape. The spread of this distribution around the projected range is called range straggle (ΔR_p).

The depth distribution, N(x), of implanted ions, normalized for an ion implantation dose is given by the expression [171]:

$$N(x) = \frac{\phi}{\sqrt{2\pi}\Delta \mathrm{R_P}} exp\left[-\frac{1}{2}\left(\frac{x - R_P}{\Delta R_P}\right)^2\right] \quad 5.1$$

The implant concentration $N(x)$represents the dopant concentration (in cm^{-3}) at a depth x. The parameter ϕ denotes the implantation dose (in cm^{-2}). The quantity $R_p$is the projected range, which corresponds to the average penetration depth of the implanted ions, while ΔR_prepresents the range straggle, or the standard deviation of the implantation depth.

The maximum (peak) concentration occurs at the depth $x = R_P$. The peak concentration is given by:

$$N(R_P) = \frac{\phi}{\sqrt{2\pi}\Delta R_P} \quad 5.2$$

This expression indicates that the peak concentration is directly proportional to the implantation dose ϕ, increasing the dose therefore increases the dopant concentration at the projected range. Figure 5.2 illustrates a typical ion implantation depth distribution.

To achieve high doping levels, sufficiently large doses are required. However, excessive implantation can introduce significant lattice damage that may not be fully removed even with high-temperature annealing.

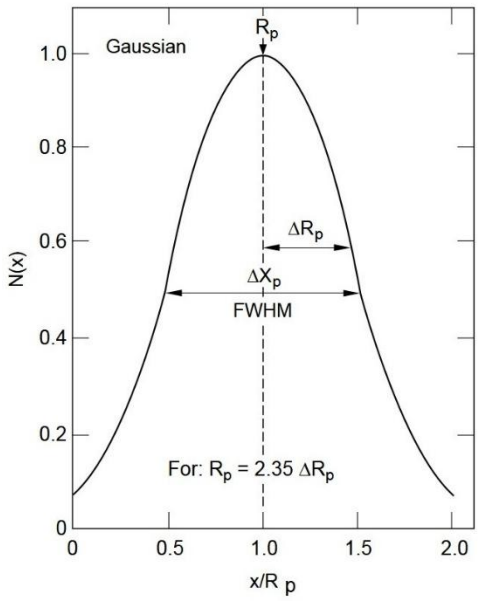


Figure 5.2 Gaussian range distribution for implanted ions with $R_P = 2.35\Delta R_P$ and a full width of half-maximum (FWHM) of ΔX_P [171]

5.3.1 SRIM Simulation of Si Ion Implantation in GaN-Based Heterostructures

Stopping and Range of Ions in Matter (SRIM) is a simulation software package used to predict the penetration and distribution of energetic ions within a target material. The calculation is based on the energy lost by an incident ion as it travels through the target, primarily through two mechanisms: nuclear stopping and electronic stopping. Nuclear stopping involves the transfer of energy from the incident ion to target atoms through elastic collisions with their nuclei, while electronic stopping involves energy loss through inelastic interactions with the electrons of the target material [172],[173]. The total stopping power, which represents the energy lost per unit distance travelled by the ion, can therefore be expressed as [174]:

$$-\frac{dE}{dx} = S_n(E) + S_e(E) \tag{5.3}$$

where E is the kinetic energy of the incident ion, $x$is the distance travelled through the target, and $S_n(E)$ and $S_e(E)$ represent the nuclear and electronic stopping powers, respectively.

SRIM uses the Transport of Ions in Matter (TRIM) Monte Carlo simulation method to calculate the trajectories of implanted ions as they undergo successive interactions with the

target atoms [175]. The energy lost and changes in direction resulting from these interactions determine the subsequent motion of each ion until it comes to rest within the target. By simulating many ion trajectories, TRIM determines the resulting implantation depth distribution, including the projected range and range straggling. Since individual ions undergo different collision sequences, they do not all come to rest at the same depth, resulting in a distribution of implanted ions rather than a single implantation depth [172],[175].

In this work, SRIM simulations were used to estimate the projected range, straggling behaviour, and depth distribution of silicon ions implanted into the GaN based heterostructures investigated. The implantation parameters used in this study were adopted from [176], where Si ion implantation was applied to GaN to improve Ohmic contact formation. SRIM simulations were therefore performed to evaluate the resulting ion distribution within the heterostructures and to confirm that the implantation profile lies within the near surface region relevant for Ohmic contact formation.

In the simulations, the layered structures were defined to represent the near surface epitaxial layers most relevant to the implantation process. Accurate representation of the SiO_2 layer, GaN cap, barrier, and channel layers was particularly important, as these layers influence the stopping behaviour and final distribution of the implanted ions. The SiO_2 layer served as both a protective cap to minimise surface damage during implantation and a retarding layer to control the projected range of the Si ions. The underlying GaN buffer layer was also included to ensure that the full ion trajectory and distribution were captured within the target structure. The material densities used in the simulations were 2.65 g/cm³ for SiO_2, 6.1 g/cm³ for GaN, and 3.26 g/cm³ for AlN. A density of 5.57 g/cm³ was used for AlGaN. Silicon ions were implanted at a tilt angle of 7° to minimise ion channelling effects, consistent with previous Si implantation studies in GaN [177]. Ion channelling occurs when implanted ions are aligned with relatively unobstructed paths between rows of atoms in the crystal lattice, allowing them to undergo fewer collisions and consequently penetrate deeper into the material than intended. Tilting the sample reduces this alignment and therefore suppresses channelling [178]. An implantation energy of 250 keV was selected based on previous Si implantation studies in GaN employing a 350 nm SiO_2 retarding layer [176]. The simulations were performed using the TRIM Monte Carlo module within SRIM The simulated implantation profile in the AlGaN/GaN structure for a 250 keV Si implantation energy is shown in Figure 5.3**.** Additional simulations were performed to determine the projected ion

ranges and straggling behaviour for the different heterostructures investigated in this research.

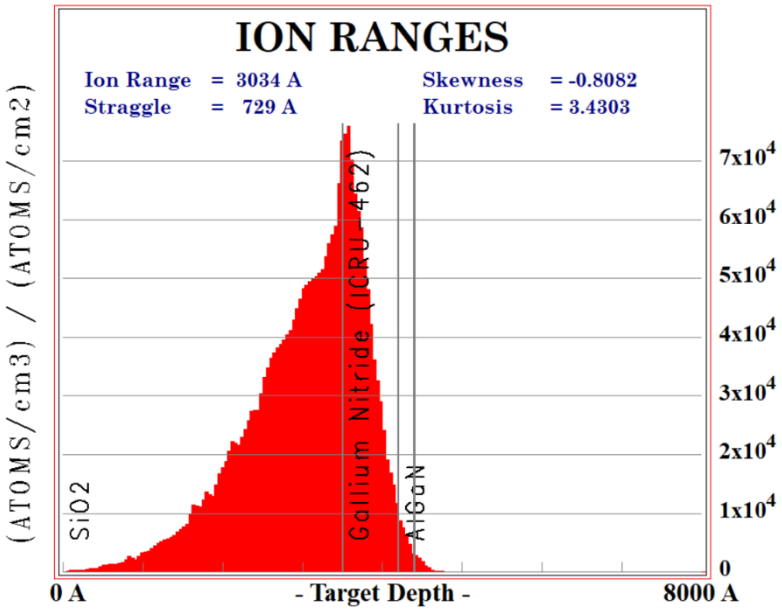


Figure 5.3 Simulated Si ion profile into AlGaN/GaN for 250 keV ion energy.

5.4 Implantation-Induced Damage and Activation Annealing in GaN

Despite the many advantages of ion implantation, the energetic ions used during implantation generate substantial damage within the crystal lattice. Therefore, a subsequent high temperature annealing step is required to restore the crystal structure and to electrically activate the implanted dopant species. A detailed understanding of implantation induced damage, and its subsequent recovery is therefore essential for the optimisation of ion implantation processes in GaN technologies.

When ions are implanted into a semiconductor, they interact with the lattice through nuclear and electronic collisions, transferring energy to the surrounding atoms. These collisions result in the formation of point defects such as interstitials and vacancies. Depending on the ion, implant temperature and implantation dose, these defects can lead to extensive crystal damage and even amorphisation of the implanted region. These defects affect the electrical behaviour of the semiconductor, as they form localised deep levels that act as carrier traps and compensate shallow donors or acceptors. In addition, the increased crystal defects provide scattering centres for charge carriers, thereby degrading electron mobility. As a

result, although ion implantation can introduce high dopant concentrations, effective electrical activation typically requires thermal annealing to repair implantation damage [179]. Therefore, post-implantation annealing is important for repairing implantation-induced damage and activating the dopant species within the crystal.

Previous studies have shown that annealing temperatures above $1000°C$ are typically required for effective electrical activation of Si donors in GaN [179] with full recovery of implantation induced damage and dopant activation requiring annealing temperatures above $1500°C$ [180]. It has however been reported that both carrier concentration and electron mobility increase with increasing ion dose and annealing temperature, reaching optimal values at around $1350°C$. For implantation doses of approximately 1×10^{15} cm^{-2}, nearly complete apparent activation has been achieved after annealing at $1350°C$ [181].

The activation of implanted dopants in AlGaN is generally more difficult than in GaN because the incorporation of aluminium increases the bond strength within the lattice. As a result, Si implanted AlGaN structures often require higher annealing temperatures to achieve similar activation efficiencies. Experimental studies have reported that activation efficiencies approaching 100% are obtained only after annealing at temperatures near $1375°C$, yielding sheet resistances as low as $74\ \Omega/\square$ for high dose implants [182]. These results highlight the significant influence of the epitaxial composition on the thermal budget required for effective dopant activation and the recovery of implantation induced defects.

Although high annealing temperatures are required to repair implantation induced damage and activate dopants, GaN surfaces become thermally unstable at elevated temperatures. Surface degradation can occur above approximately $900°C$ [183], resulting in the formation of N_2 and the consequent loss of nitrogen. To mitigate this effect, protective encapsulation layers are typically deposited prior to high temperature annealing. Commonly used materials include SiO_2, Si_3N_4, and AlN, which act as capping layers to preserve the surface morphology of GaN during annealing. However, these materials exhibit different thermal stabilities and processing challenges. For example, Si_3N_4 may begin to degrade at temperatures above approximately $1100°C$ [179], whereas, although AlN provides good thermal stability, it can be difficult to remove after annealing, which may complicate subsequent processing steps [180].

High-temperature RTA has been used successfully for implanted Si donor activation in GaN [19], [184]. Furnace annealing is also a viable approach: Dupuis et al. [185] reported Si activation and smooth surface morphology following annealing at 1150 °C for 5 minutes in N_2. In the present work, RTA was adopted as a practical activation method offering controlled high-temperature processing with a limited dwell time, while SiO_2 encapsulation was used to protect the semiconductor surface. A temperature-dependent study was therefore carried out to evaluate the effectiveness of SiO_2 as an encapsulation layer during rapid thermal annealing.

Activation annealing plays a critical role in determining the electrical performance of implanted regions. In device applications, it can also significantly reduce the contact resistance of implanted ohmic contacts. For instance, Si implantation followed by high temperature annealing has been shown to produce extremely low contact resistances of $0.097\ \Omega \cdot mm$ in GaN [186] demonstrating the strong potential of ion implantation for forming highly conductive n^+regions suitable for ohmic contacts. However, excessively high annealing temperatures can lead to unwanted effects in the device structures. For instance, [187] reported that activation annealing at 1050 °C in GaN-on-Si HEMT structures enhanced the conductivity of implanted regions but also increased the sheet resistance of the 2DEG channel, suggesting partial degradation of the heterostructure during the thermal process. These findings highlight the importance of carefully optimising annealing conditions to achieve a balance between dopant activation, defect recovery, and the preservation of device structural integrity.

5.5 Blanket Silicon Ion Implantation for Low-Resistance Ohmic Contacts

Silicon ion implantation was used as a re-growth free approach for forming low resistance Ohmic contacts on both AlGaN/GaN and AlN/GaN heterostructures. The process starts with a 350 nm PECVD deposited SiO_2 layer, used as a retarding mask to control dopant penetration during implantation. Si ions were implanted at room temperature with an energy of 250 keV, a fluence of 2.0×10^{16} cm^{-2}, and a tilt angle of 7°, at the Surrey Ion Beam Centre. Following implantation, the retarding layer was removed using buffered oxide etchant (BOE) 6:1. A fresh 200 nm 300 °C SiO_2 encapsulation layer was then deposited prior to dopant activation annealing, at 1100 °C for 120 s in N_2 ambient using RTA, after which the encapsulation layer was etched with BOE. CTLM structures were then defined using

photolithography. Prior to metallisation, an in-situ Ar plasma etch was performed for 45 seconds to remove native oxide from the samples surfaces. Ohmic contacts were formed using a Ti/Al/Ni/Au (30/180/40/100 nm) metal stack deposited by e-beam evaporation, followed by lift-off.

5.5.1 Si-Implanted Ohmics on GaN/AlGaN/GaN HEMT Heterostructure

The GaN/AlGaN/GaN HEMT structure used in this work was a commercially sourced epi-structure grown by MBE on a high-thermal-conductivity 4H-SiC substrate. The epitaxial structure consisted of an AlN nucleation layer, a 1.7 μm GaN channel, a 1 nm AlN spacer, a 20 nm AlGaN barrier, and a 70 nm undoped GaN cap layer. Hall measurements previously performed on material from the same wafer and reported in [188] yielded a 2DEG sheet carrier concentration of $2.7 \times 10^{12}\text{cm}^{-2}$ and an electron mobility of 780 $\text{cm}^2\ \text{V}^{-1}\ \text{s}^{-1}$. The GaN/AlGaN/GaN epitaxial structure and the corresponding simulated Si distribution are presented in Figure 5.4. The simulation was performed at an implantation energy of 250 keV using a 350 nm SiO_2 retarding layer. A depth of 0 nm corresponds to the surface of the GaN cap, therefore, the plotted profile represents the Si distribution within the semiconductor after passage through the SiO_2 layer. Following implantation and activation annealing, Ohmic contacts were formed on the heterostructure. The sample was subsequently diced into smaller pieces to investigate the effect of post-metallisation annealing on the contacts. One piece was retained in the as-deposited condition without further annealing, while the remaining pieces were subjected to post-metallisation annealing at 800 °C for 30 s and 850 °C for 30, 40, and 50 s.

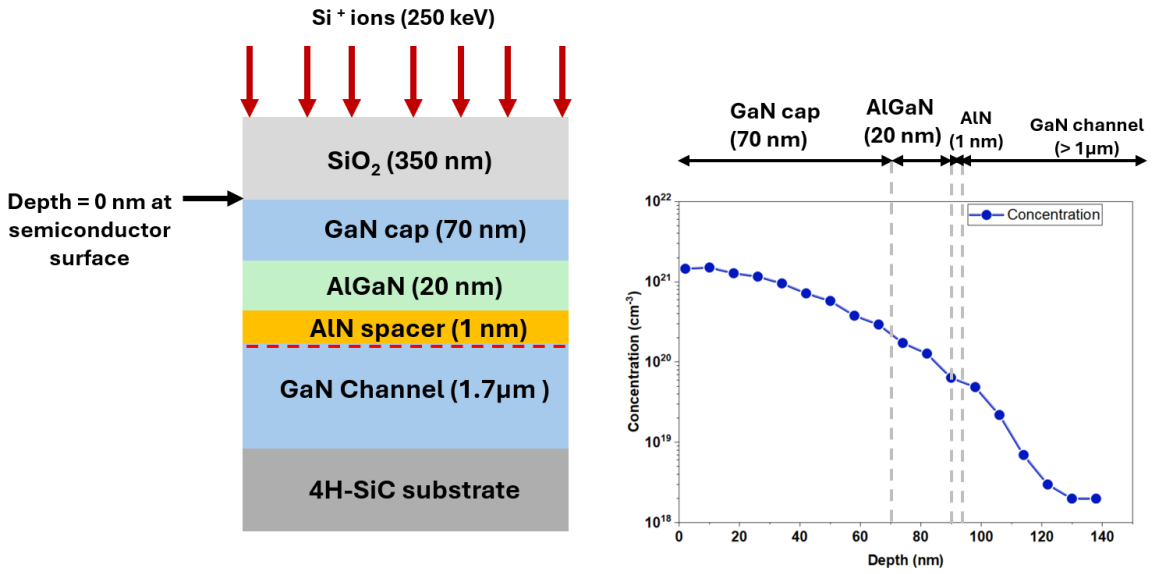


Figure 5.4 GaN/AlGaN/GaN epitaxial structure and SRIM simulated Si implantation depth profile.

The contacts were characterised using CTLM measurements. The resistance as a function of contact gap spacing, shown in Figure 5.5, exhibited a linear relationship for the non-alloyed sample, confirming Ohmic behaviour and enabling the contact and sheet resistances to be extracted. The non-alloyed sample exhibited the lowest contact resistance of 0.14 Ω·mm, with a corresponding sheet resistance of approximately 55 Ω/□. Following post-metallisation annealing, the contact resistance ranged from 0.41 to 0.73 Ω·mm, while the sheet resistance ranged from 128 to 175 Ω/□. The extracted contact and sheet resistances for all annealing conditions are summarised in Table 5.1.

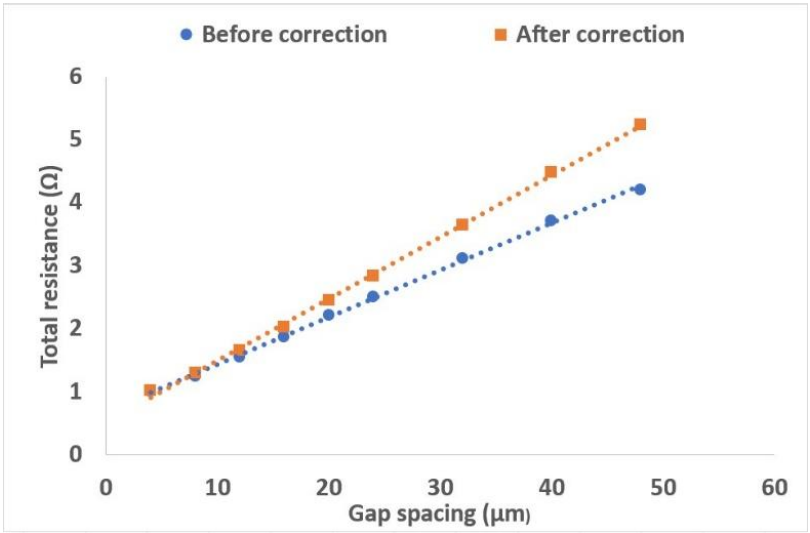


Figure 5.5 Measured resistance versus gap spacing for non-alloyed sample.

Table 5.1 Contact and sheet resistances of Si-implanted GaN/AlGaN/GaN sample under different post metallisation annealing conditions.

Annealing condition (°C)	Annealing time (s)	R_c (Ω·mm)	R_{sh} (Ω/□)
Unannealed	-	0.14	55
800	30	0.44	133
850	30	0.41	175
850	40	0.73	130
850	50	0.52	128

The results show that post metallisation annealing increased both the contact and sheet resistances relative to the unannealed samples. At 850 °C, no consistent relationship between annealing time and contact resistance was observed, with $R_c$varying from 0.41 Ω·mm at 30 s to 0.73 Ω·mm at 40 s and 0.52 Ω·mm at 50 s. Similarly, the sheet resistance was highest after annealing at 850 °C for 30 s and decreased at longer annealing times.

Overall, the unannealed condition provided the lowest R_c and R_{sh} among the conditions investigated. A possible explanation is that the high concentration of electrically active Si donors narrows the depletion region at the metal–semiconductor interface, facilitating electron tunnelling and enabling low-resistance Ohmic conduction without post-metallisation alloy annealing. However, degenerate doping and field emission dominated transport were not directly established in this study.

Atomic force microscopy (AFM) images of the annealed surface (Figure 5.6) show a generally preserved surface morphology with some localised surface pits observed after implantation and annealing. The AFM surface roughness after annealing was measured to be 1.52 nm, indicating that despite the presence of minor surface degradation, the overall surface quality remained relatively well maintained. These results demonstrate that the

combination of a high Si implantation dose and the thick GaN cap layer enable efficient Ohmic contact formation without the need for post metallisation annealing.

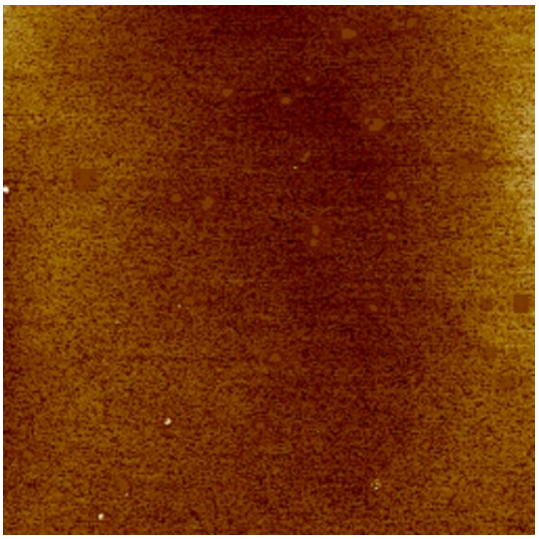


Figure 5.6 AFM image showing the surface morphology of the sample after ion implantation, annealing, and SiO_2 removal. The scan was performed over a 10 × 10 μm² area.

5.5.2 Si-Implanted Ohmics on AlN/GaN HEMT Heterostructure

The AlN/GaN heterostructure was grown by Qrona Technologies, USA, and consisted of a 2 nm GaN cap layer, 3 nm AlN barrier layer, 100 nm GaN channel layer, 1.5 μm GaN buffer layer, and an AlN nucleation layer grown on a 2-inch c-plane sapphire substrate. According to measurements provided by the grower, contactless characterisation across the wafer yielded an average 2DEG sheet carrier concentration, n_s, of 1.6×10^{13}cm^{-2} and a room-temperature electron mobility of approximately 1600 cm² V^{-1} s^{-1}.

Figure 5.7 shows the AlN/GaN epitaxial structure alongside the SRIM simulated Si implantation profile. The simulation was carried out at an implantation energy of 250 keV with a 350 nm SiO_2 retarding layer. In the plot, 0 nm corresponds to the surface of the GaN cap, after the Si ions have passed through the SiO_2 layer. The simulated Si concentration decreases with increasing depth, with the implanted ions extending through the 2 nm GaN cap, 3 nm AlN barrier and 100 nm GaN channel. Following implantation, the sample underwent activation annealing at 1100 °C for 120 s in N_2, followed by Ohmic contact formation and post-metallisation annealing at 800 or 850 °C for 30 s.

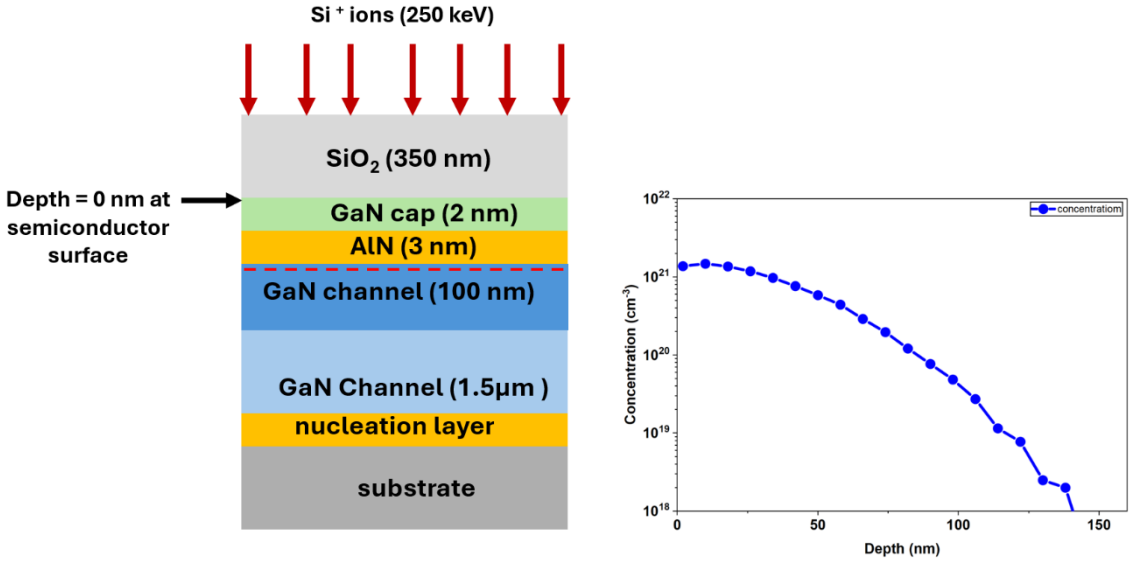


Figure 5.7 AlN/GaN epitaxial structure and simulated Si implantation depth profile.

Unlike the AlGaN/GaN study, an unannealed contact was not included in this experiment; therefore, the effect of annealing is evaluated by comparing the two annealing temperatures rather than against an unannealed reference. The resistance as a function of gap spacing obtained from CTLM measurements at 800 ℃ is shown in Figure 5.8.

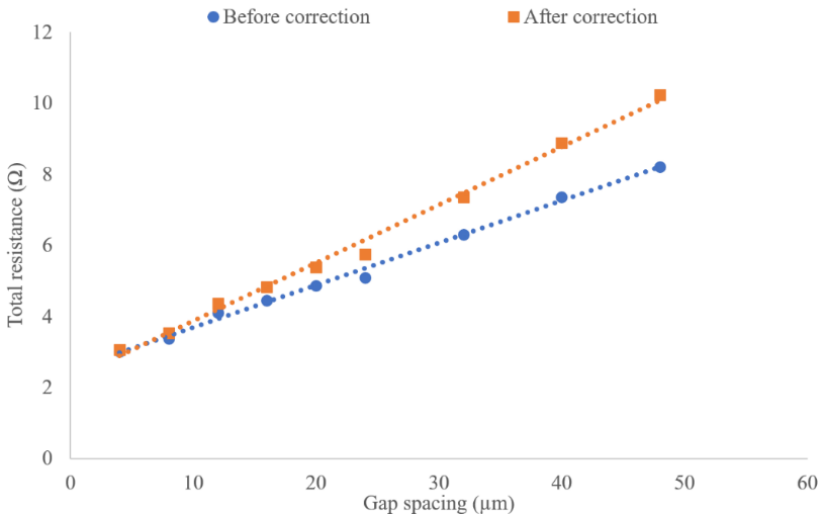


Figure 5.8 Measured resistance versus gap spacing

The linear relationship between resistance and gap spacing confirms Ohmic behaviour. For the samples annealed at $800\ ^{\circ}\mathrm{C}$, extracted contact resistances ranged from 0.46 to $0.75\ \Omega \cdot \mathrm{mm}$, with the lowest R_c of $0.46\ \Omega \cdot \mathrm{mm}$ obtained under this condition. In comparison, annealing at $850\ ^{\circ}\mathrm{C}$ resulted in R_c values between 0.64 and $0.76\ \Omega \cdot \mathrm{mm}$. The lowest contact resistance obtained at $850\ ^{\circ}\mathrm{C}$ was therefore higher than the best value obtained at $800\ ^{\circ}\mathrm{C}$. The sheet resistance remained within a relatively similar range for the two annealing conditions. Values of approximately $85 - 110\ \Omega/\square$ were measured following the $800\ ^{\circ}\mathrm{C}$ anneal, compared with approximately $88 - 94\ \Omega/\square$ following the $850\ ^{\circ}\mathrm{C}$ anneal. The lower minimum R_c obtained at $800\ ^{\circ}\mathrm{C}$, despite the broadly comparable sheet resistance, indicates that increasing the post-metallisation annealing temperature to $850\ ^{\circ}\mathrm{C}$ did not improve the contact performance under the conditions investigated.

5.5.3 Silicon dioxide (SiO2) Encapsulated Annealing

A temperature dependent study was conducted to evaluate the effectiveness of a 200 nm SiO_2 encapsulation layer in protecting GaN based heterostructures during RTA. The 200 nm thickness was selected based on previous studies in which 200 nm SiO_2 layers was used to protect GaN surface during post implantation annealing [189] The annealing was carried out in an N_2 ambient for a fixed duration of 2 minutes, with annealing temperatures of 1100 °C, 1150 °C, and 1200 °C investigated. The study was motivated by the need to protect the GaN surface during the high temperature annealing required for the recovery of implantation induced lattice damage and activation of implanted Si ions. Since GaN is susceptible to surface degradation at elevated temperatures, it was necessary to establish whether the selected 200 nm SiO_2 encapsulation layer could provide adequate surface protection under the intended post implantation annealing conditions.

The first and second sample sets used in this study are AlN/GaN heterostructures as in Figure 5.7 (Section 5.5.1). The first sample set were not implanted but were encapsulated with 200 nm SiO_2 deposited at 300 °C. These samples were annealed at 1100 °C, 1150 °C, and 1200 °C for 2 minutes to evaluate the structural integrity and protective performance of the SiO_2 encapsulation layer under these thermal conditions. Optical microscopy was used to characterise the encapsulated surfaces, with particular attention given to evidence of film degradation such as cracking, peeling, delamination, or severe surface modification. The

results showed that the SiO_2 layer remained largely continuous after annealing, with no catastrophic film failure observed across the investigated temperature range.

A second sample set consisted of selectively Si implanted regions. These were used to investigate the influence of SiO_2 deposition temperature on post annealing surface stability. The samples were implanted with Si ions at 250 keV and encapsulated with 200 nm SiO_2 deposited either at 300 °C or 350 °C. Both samples were annealed at 1100 °C for 2 minutes in an N_2 ambient.

AFM images of the selectively Si-implanted samples following activation annealing are shown in Figure 5.9. Figures 5.9(a) and (b) show the implanted and un-implanted regions, respectively, of the sample encapsulated with 200 nm SiO_2 deposited at 300 °C, while Figures 5.9(c) and (d) show the corresponding implanted and un-implanted regions of the sample encapsulated with 200 nm SiO_2 deposited at 350 °C. Numerous small dark spots are visible in the implanted region of the sample encapsulated at 300 °C, as shown in Figure 5.9(a). These features may indicate localised surface degradation, suggesting that the SiO_2 layer deposited at 300 °C did not provide sufficient protection against surface degradation during the 1100 °C post-implantation anneal.

The RMS surface roughness measured in the implanted regions decreased from 3.20 nm for the sample encapsulated at 300 °C to 1.87 nm for the sample encapsulated at 350 °C, as summarised in Table 5.2. This corresponds to an approximately 42% reduction in surface roughness following activation annealing at 1100 °C for 2 minutes. The lower surface roughness suggests that the SiO_2 layer deposited at 350 °C provided more effective surface protection under the investigated processing conditions. This improvement may be associated with increased film density and reduced porosity at the higher deposition temperature, potentially enhancing the encapsulation layer’s resistance to thermal degradation. However, further characterisation of the SiO_2 films would be required to confirm this mechanism.

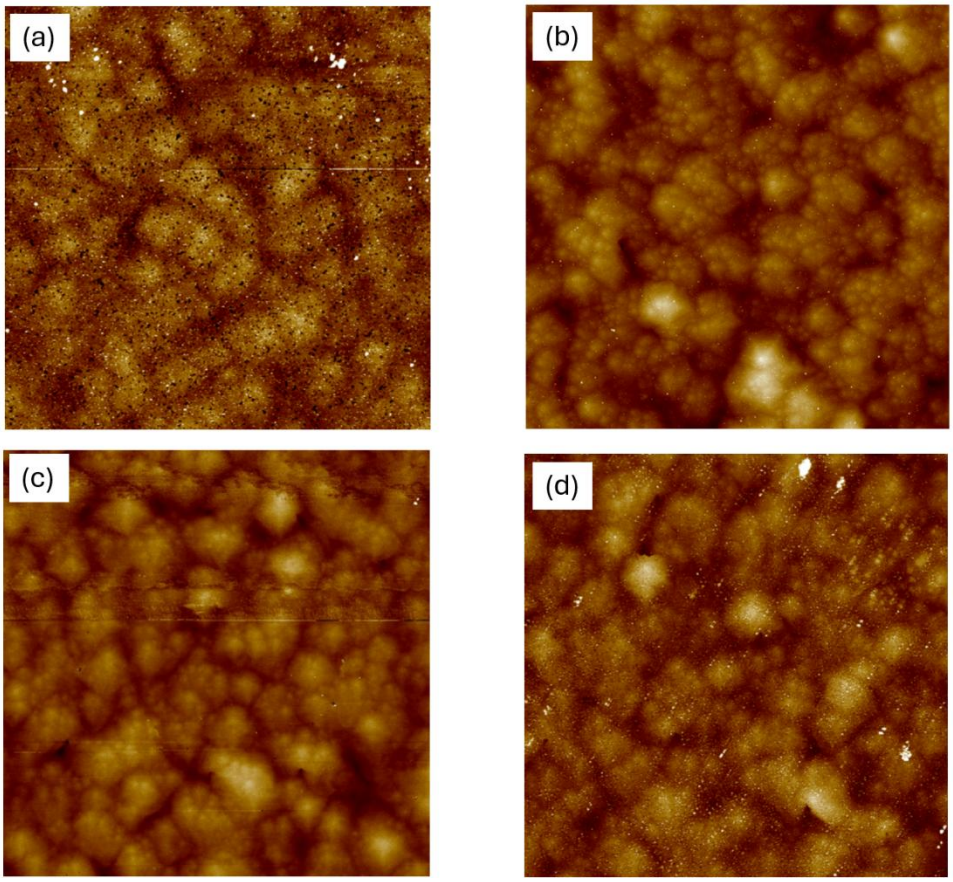


Figure 5.9 AFM images of selectively Si implanted AlN/GaN samples showing the implanted and un-implanted regions after annealing at 1100 °C for 2 minutes, with 200 nm SiO_2 deposited at 300 °C [(a) implanted and (b) un-implanted regions] and 350 °C [(c) implanted and (d) un-implanted regions].

Table 5.2 RMS surface roughness values for selectively Si implanted AlN/GaN samples annealed at 1100 °C for 2 minutes.

SiO2 deposition temperature	Annealing condition	RMS roughness (nm)
300 ℃	1100 ℃, 2 min	3.2
350 ℃	1100 ℃, 2 min	1.87

The third sample set consisted of Si implanted AlGaN/GaN heterostructures incorporating a 2 nm GaN cap layer and a 20 nm AlGaN barrier layer grown on a SiC substrate. These samples were encapsulated with 200 nm SiO_2 deposited at 350 °C and annealed at 1100 °C and 1200 °C for 2 minutes to evaluate the effectiveness of the optimised SiO_2 deposition condition under more aggressive activation annealing conditions.

Optical microscope observations revealed a clear difference between the two annealing temperatures (Figure 5.10). The implanted region of the sample annealed at 1200 °C exhibited severe surface degradation and localised burning, indicating that the 200 nm SiO_2 layer deposited at 350 °C was not sufficient to protect the implanted surface at this temperature. In contrast, the implanted region of the sample annealed at 1100 °C did not show visible burning, indicating improved thermal stability at the lower annealing temperature.

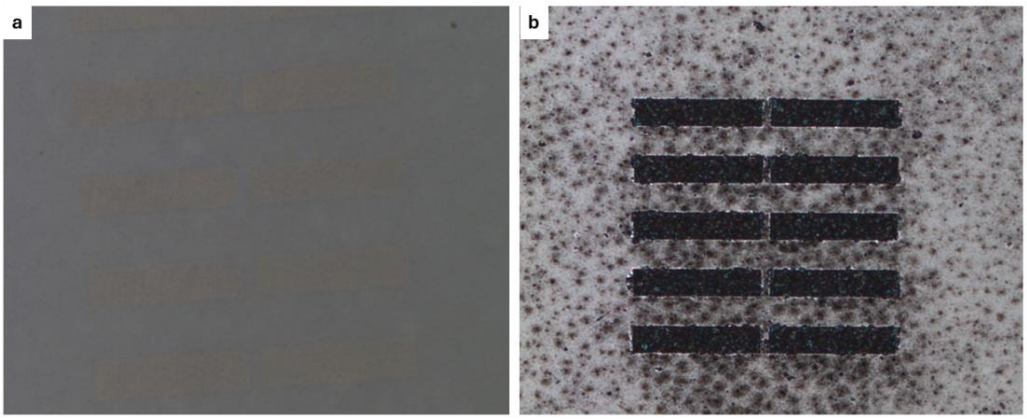


Figure 5.10 Optical microscope images of Si implanted AlGaN/GaN samples annealed at (a) 1100 °C and (b) 1200 °C for 2 minutes with 200 nm SiO_2 deposited at 350 °C.

5.6 Selective Area Si Ion Implantation Process Development

Following the investigation of blanket Si implantation, a selective-area implantation process was developed to confine Si implantation to the Ohmic contact regions while leaving the remaining regions of the heterostructure un-implanted. The implantation conditions, including the 350 nm SiO_2 retarding layer, were adopted from the process reported in [176], as previously discussed in Section 5.3.1. SRIM simulations were subsequently performed using the same conditions to evaluate the Si implantation profile within the GaN/AlN/GaN heterostructure used in this work. The simulations showed that the highest Si concentration occurred within approximately the first 10 nm of the semiconductor, followed by a gradual decrease in concentration with increasing depth. The implantation profile extended through the GaN cap, AlN barrier and GaN channel, with the low-concentration tail reaching into the underlying GaN buffer, as shown in Figure 5.11. A schematic representation of the overall process flow is shown in Figure 5.12.

A 350 nm SiO_2 layer was first deposited by PECVD at 300 °C to retard the implanted Si ions and control their penetration depth. A Ti/Ni mask stack (20/270 nm) was then deposited by e-beam evaporation and lifted off from the Ohmic regions, leaving the non-Ohmic areas protected during implantation. Si ion implantation was carried out in the exposed regions at an energy of 250 keV, with a dose of 2×10^{16} $cm^{-2}$and a tilt angle of 7°. The Ti/Ni mask effectively shielded the non-Ohmic regions from implantation. All implantations were performed at room temperature.

Following implantation, the Ti/Ni mask was removed using a sequential wet etching process. The Ni layer was first etched by pre-dipping the sample in $HCl:H_2O$ (1:6) followed by $HNO_3:H_2O$ (1:1), with intermediate RO water rinsing. The Ti layer was subsequently removed using a Ti etchant, followed by a final clean in $HCl:H_2O_2:H_2O$ (1:1:6) to eliminate residual metal contamination. The SiO_2 retarding layer was then removed using a buffered oxide etch (6:1 BOE), consisting of hydrofluoric acid (HF) and ammonium fluoride (NH_4F). A fresh 200 nm SiO_2 layer was subsequently deposited at 350 °C to serve as an encapsulation layer during activation annealing. RTA was performed at 1100 °C for 120 s in an N_2 ambient using a Jipelec JetFirst system to activate the implanted dopants. Following annealing, the SiO_2 encapsulation layer was removed using a 6:1 BOE solution.

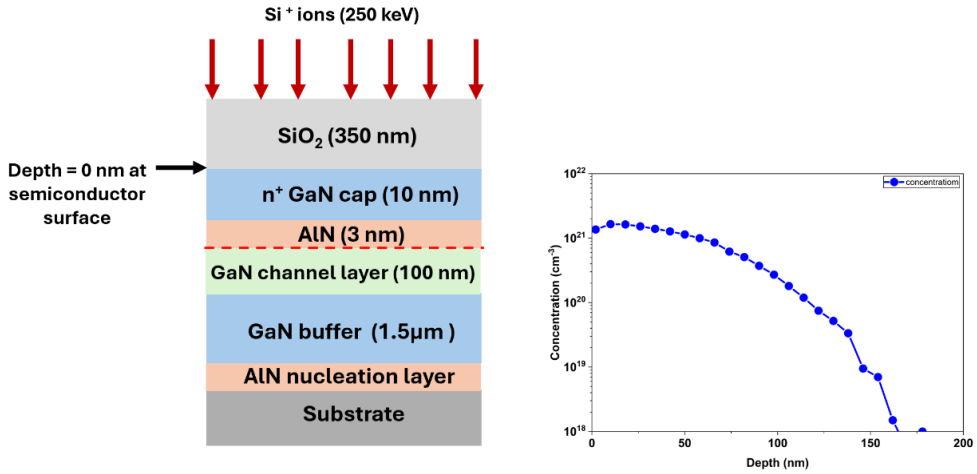


Figure 5.11 n+ GaN/AlN/GaN epitaxial structure and simulated Si implantation depth profile.

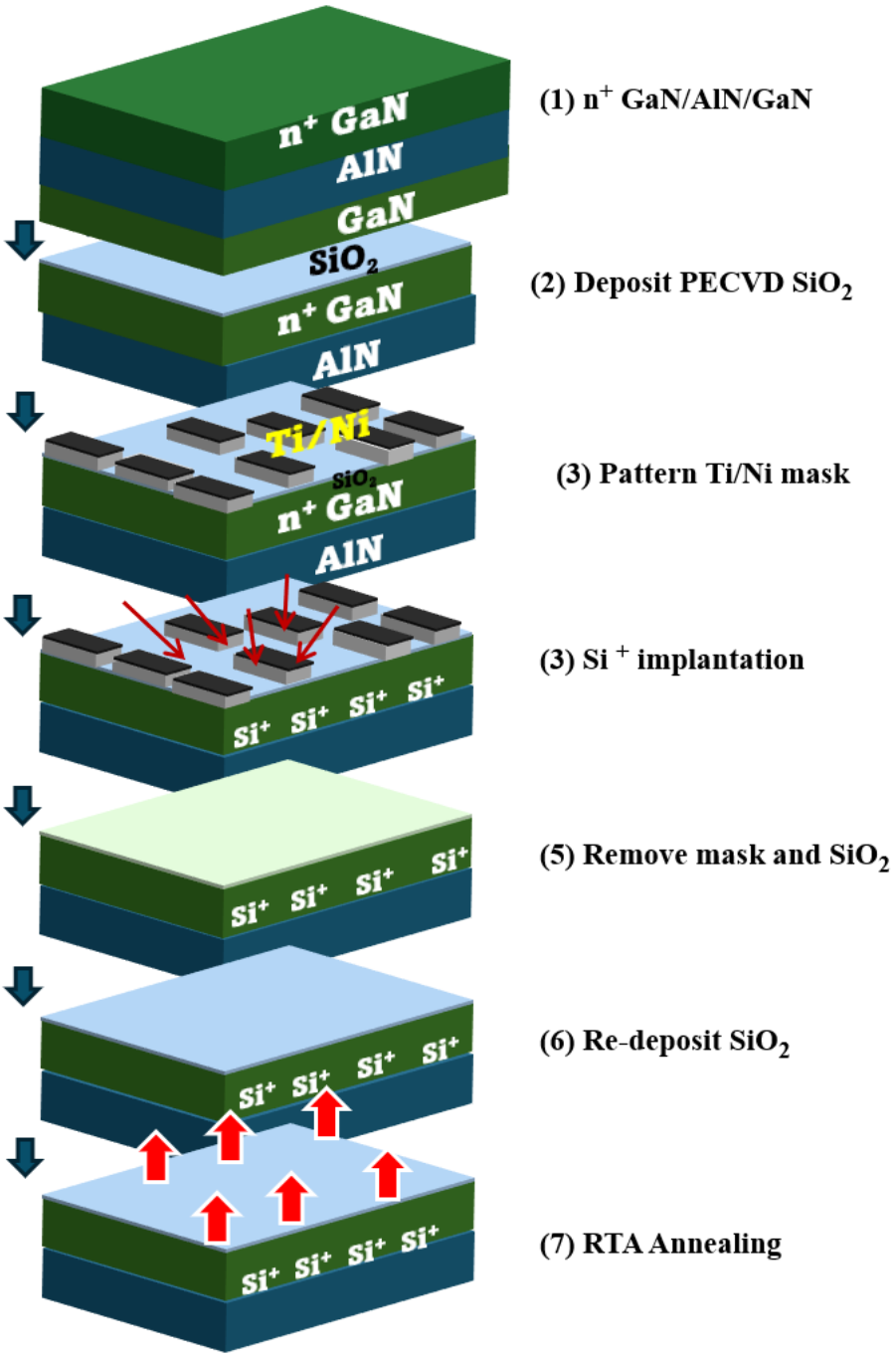


Figure 5.12 Process flow for Si ion implantation and activation in n+ GaN/AlN/GaN heterostructure

5.6.1 CTLM Fabrication and Characterisation

Following the development of the selective area Si ion implantation process, the process was applied to an available n^+ GaN/AlN/GaN heterostructure to investigate its effect on Ohmic contact characteristics. Implanted and un-implanted regions were defined on the same

sample, and CTLM structures were fabricated in both regions to allow direct comparison of the extracted contact and sheet resistances.

The n^+ GaN/AlN/GaN heterostructure was grown on a 2-inch c-plane sapphire substrate. The epitaxial structure consisted of an AlN nucleation layer, an approximately 1.5 µm GaN buffer layer, a 100 nm unintentionally doped (UID) GaN channel, a 3 nm UID AlN barrier, and a 10 nm heavily n-doped GaN cap layer with an electron concentration greater than 1×10^{20}cm^{-3}.

The sample was selectively implanted and activated using the process described in the preceding sub-section. Following activation, CTLM structures were fabricated in both the implanted and un-implanted regions using identical Ohmic contact processing conditions. A Ti/Al/Ni/Au metal stack of 20/180/40/100 nm was deposited, followed by lift off and subsequently annealing at 825 °C for 30 seconds in N_2. The fabricated CTLM structures were subsequently characterised to extract the contact resistance (R_c) and sheet resistance (R_{sh}).

5.6.2 Results and Discussion

Figure 5.13 shows the I–V characteristics obtained from the implanted TLM structures. The linear relationship between current and voltage demonstrates Ohmic behaviour over the measured voltage range.

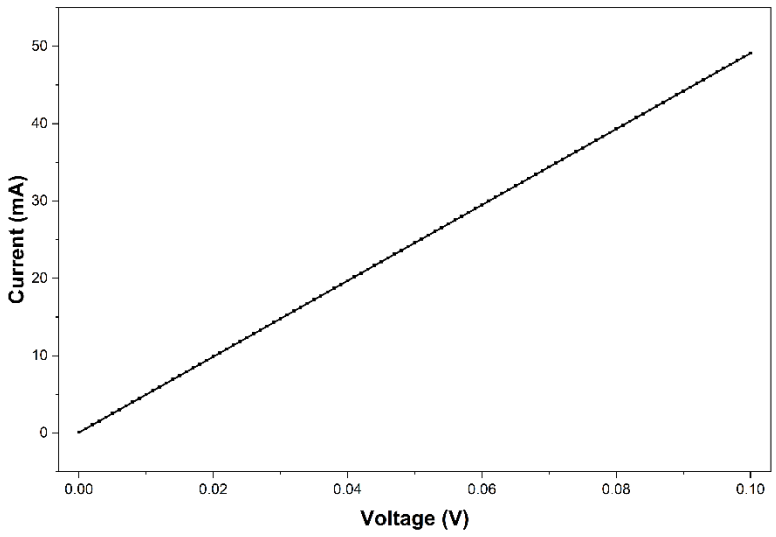


Figure 5.13 Measured I–V characteristics of the Si-implanted TLM structures

Figure 5.14 shows the measured resistance as a function of gap spacing for the implanted and un-implanted regions.

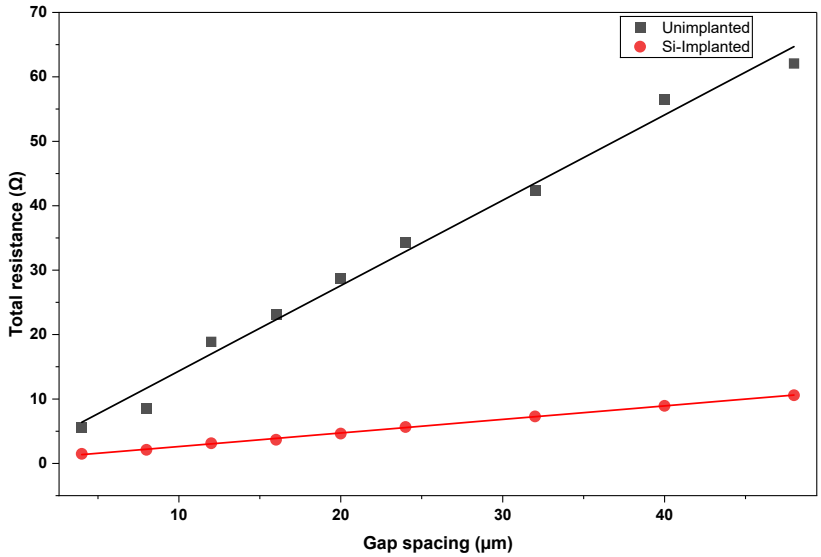


Figure 5.14 Measured resistance as a function of gap spacing for the implanted and un-implanted regions

The CTLM measurements showed that selective Si implantation improved the electrical characteristics of the n^+ GaN capped AlN/GaN heterostructure. The implanted region exhibited a contact resistance (R_c) of 0.14 Ω·mm, compared with 0.30 Ω·mm for the un-implanted region, corresponding to a reduction of approximately 53.5%. The sheet resistance (R_{sh}) also decreased substantially from 750 Ω/□ in the un-implanted region to 119 Ω/□ following implantation. The simultaneous reduction in R_c and R_{sh} indicates improved carrier transport within the implanted contact region. This improvement is notable because the heterostructure already contained an approximately 10 nm heavily n-doped GaN cap ($n > 1 \times 10^{20}$ cm^{-3}). The results therefore indicate that selective Si implantation provided an additional electrical benefit despite the presence of the highly doped cap. The improvement may be associated with electrically activated Si donors increasing the conductivity of the implanted region and facilitating carrier transport between the Ohmic contact and the channel.

5.7 Summary

This chapter investigated Si ion implantation as an approach for reducing Ohmic contact resistance in GaN-based heterostructures. The principles of donor doping in GaN, ion range and distribution, and implantation induced damage were first considered. SRIM simulations were used to examine the distribution of implanted Si and support the selection of implantation conditions. The need for high temperature annealing to activate the implanted Si and recover implantation induced lattice damage was also discussed.

Blanket Si implantation was investigated on GaN/AlGaN/GaN and AlN/GaN heterostructures. For the implanted GaN/AlGaN/GaN sample, the lowest contact and sheet resistances of 0.14 Ω·mm and 55 Ω/□, respectively, were obtained without post-metallisation annealing. Annealing between 800 and 850 °C increased both resistances, with no consistent improvement observed with annealing time. For the blanket implanted AlN/GaN sample, contact resistance values of 0.4–0.7 Ω·mm and sheet resistance values of 85–110 Ω/□ were measured across the sample.

The effectiveness of a 200 nm SiO_2 encapsulation layer in protecting the semiconductor surface during high temperature activation annealing was investigated. Following activation at 1200 °C, severe surface degradation and localised burning were observed, indicating that the 200 nm SiO_2 layer did not provide sufficient protection under these conditions. In contrast, no visible burning was observed following activation at 1100 °C. This temperature was subsequently used for the selective implantation experiments.

A selective area Si ion implantation process was subsequently developed and applied to an n-doped GaN-capped AlN/GaN heterostructure. CTLM structures fabricated in implanted and un-implanted regions of the same sample gave contact resistances of 0.14 and 0.30 Ω·mm, respectively, corresponding to a reduction of approximately 53.5% following implantation. The corresponding sheet resistance decreased from 750 to 119 Ω/□.

Overall, the chapter progressed from the investigation of Si implantation and activation to blanket implantation and the development of a selective-area implantation process. The results showed that low contact resistance could be achieved using Si implantation and that selective implantation reduced both contact and sheet resistance compared with the un-implanted region of the same heterostructure.

6 Recessed and Implanted Ohmic Contacts for GaN-based HEMTs

6.1 Introduction

Building on the Ohmic contact formation techniques and Si ion implantation discussed in Chapters 4 and 5. This chapter, focuses on investigating recessed Ohmic contact geometries specifically, evaluating how these structural changes alter overall performance. Chapter 5 demonstrated that Si ion implantation can effectively reduce Ohmic contact resistance by increasing the local donor concentration beneath the Ohmic contact region. However, further reduction in contact resistance can also be achieved through optimisation of the Ohmic contact geometry itself [190].

Beyond material and process modifications, the overlap geometry between the recessed region and the Ohmic metallisation also plays a critical role in determining device performance. In particular, the variations in the relative dimensions of the recess and the metallisation regions influences current transport mechanisms and the contact resistance. Depending on whether the metallisation extends beyond the recessed region or the recessed region extends beyond the metallisation, the current spreading behaviour and access resistance can change significantly, thereby affecting both the extracted contact resistance and the RF device characteristics. Despite its importance, systematic investigations of recess metallisation overlap geometry remain relatively limited in the literature.

Therefore, this chapter investigates the influence of recess metallisation overlap geometry on Ohmic contact resistance. Si ion implantation and barrier recess techniques are used as complementary approaches to investigate three different overlap configurations through systematic variation of the relative dimensions between the recess and metallisation regions. TLM structures are fabricated using the different overlap geometries to evaluate their influence on contact resistance.

6.2 Experimental Design

To investigate the influence of Ohmic contact geometry on contact resistance, different recess–metallisation configurations were designed and fabricated. The LTLM structures used $150 \times 150\ \mu m^2$ square contacts, with the entire contact region subjected to Si ion implantation. The contact gap spacings used were 3, 5, 7, 9, 11, 13, 15, 20 and 25 μm, as

already noted in chapter 4. The implanted area was kept constant for all structures, while the relative position of the recess and metallisation regions was varied to produce aligned, overlap and gap configurations.

In conventional recessed Ohmic contacts, the recess and metallisation regions are typically aligned such that the edge of the metallisation coincides with the edge of the recessed barrier region. However, the relative overlap between these regions can significantly alter the available current injection pathways and the effective current spreading behaviour beneath the contact. Depending on whether the metallisation extends beyond the recess region or the recess extends beyond the metallisation, the relative contributions of planar and sidewall current injection mechanisms are expected to change. Figure 6.1 shows the simplified cross section of metal/AlGaN/GaN and the resistances contributing to the contact resistance.

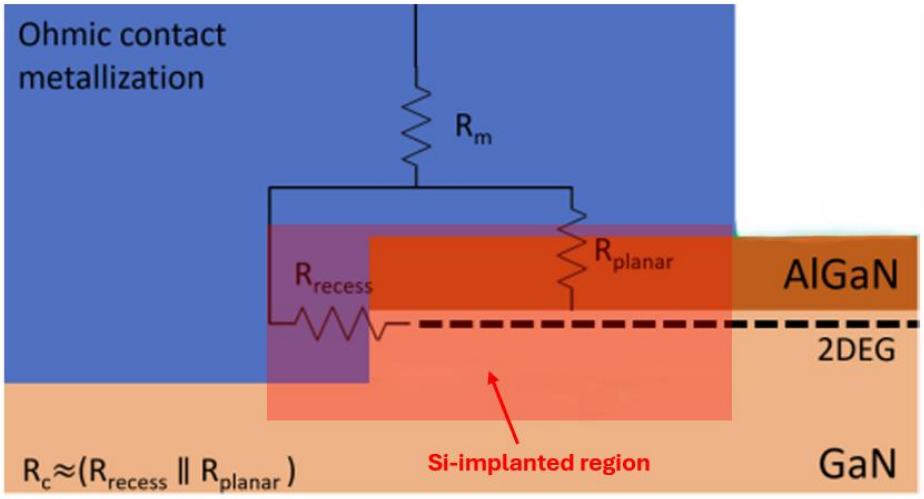


Figure 6.1 Recessed and Si-implanted Ohmic contact structure and associated resistance components (adapted from [20]).

Design A: Aligned Recess and Metallisation

In the first configuration, the recessed region and the Ohmic metallisation were aligned such that both structures possessed identical dimensions:

$$W_m = W_r \tag{6.1}$$

Where W_m represents the metallisation width and W_r represents the recess width. In this design, the edge of the metallisation coincided directly with the edge of the recessed region. This configuration represents the conventional recessed Ohmic contact structure and serves as the reference geometry for comparison with the other overlap designs.

Design B: Metallisation Wider than Recess

In the second configuration, the Ohmic metallisation extended beyond the recessed region uniformly around the entire contact perimeter. In this geometry, the metallisation dimensions exceeded the recess dimensions according to:

$$W_m = W_r + \Delta \tag{6.2}$$

Where Δ represents the overlap extension. The overlap extensions investigated in this work were: 2 µm, 3 µm, and 5 µm.

Design C: Recess Wider than Metallisation

In the third configuration, the recessed region extended beyond the Ohmic metallisation uniformly around the contact perimeter. In this case, the recess dimensions exceeded the metallisation dimensions according to:

$$W_r = W_m + \Delta \tag{6.3}$$

Where the overlap extensions investigated were: 2 µm, 3 µm, and 5 µm.

The overlap geometries investigated in this work were designed to systematically evaluate how the relative overlap between the recess and Ohmic metallisation influences Ohmic contact resistance. Figure 6.2 shows the schematic illustration of the three categories of geometries investigated.

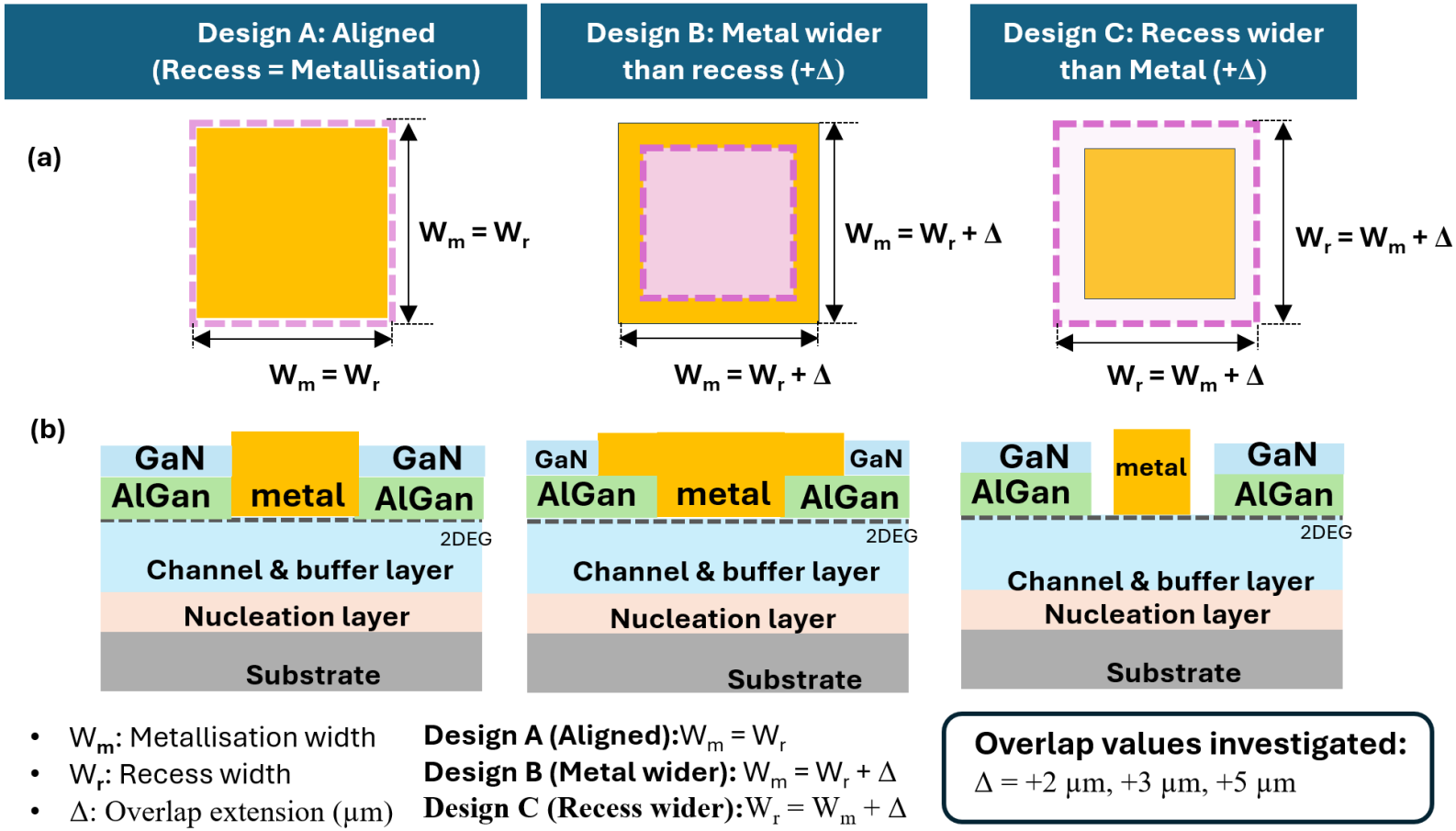


Figure 6.2 Schematic illustration of the investigated metal–recess alignment geometries for recessed Ohmic contacts in AlGaN/GaN heterostructure. Design A shows aligned metal and recess widths Design B shows metal extending beyond the recess and Design C shows the recess wider than the metallisation

6.3 LTLM Fabrication and Characterisation

The AlGaN/GaN heterostructure used for this study, was grown on a 6H-SiC substrate and comprised a 0.3 µm Fe-doped AlGaN transition layer, a 0.5 µm Fe-doped GaN buffer layer, a 1.2 µm unintentionally doped (UID) GaN layer, a 20 nm $Al_{0.3}Ga_{0.7}N$ barrier layer, and a 2 nm GaN cap layer. The implanted sample was activated by rapid thermal annealing using 200 nm SiO_2 encapsulation, as described in Section 5.6. Following activation, the SiO_2 encapsulation layer was removed using an HF based wet etch prior to fabrication of the LTLM structures. Prior to Ohmic contact formation, recessed Ohmic regions were defined using electron beam lithography followed by low bias ICP dry etching using ICP 180 system with BCl_3 and Cl_2 flow rates of 5 and 10 sccm, respectively, at a chamber pressure of 20 mTorr. The ICP and RF powers were set to 100 W and 15 W, respectively. The recess process was designed to selectively remove the barrier layer in the Ohmic contact region while minimising plasma induced damage to the underlying channel. Afterwards, mesa isolation was performed using the same tool with Cl_2/Ar gases. Following recess formation, Ohmic metallisation consisting of Ti/Al/Ni/Au/ 30/180/40/100 nm was deposited by electron beam evaporation under high vacuum conditions, prior to the Ohmic metallisation the samples were dip in HCl: H_2O and an in-situ Ar etching for 45 seconds to remove native oxide. Rapid thermal annealing was subsequently performed in N_2 ambient at 800 ℃ for 30 seconds to form alloyed Ohmic contacts.

6.4 Results and Discussion

Figure 6.3 shows the measured total resistance as a function of LTLM gap spacing for the aligned and 2, 3 and 5 µm recess–metallisation overlap designs. The aligned design produced an R_c of 8.7 $\Omega \cdot$ mm, which decreased to 4.75, 2.21, and 0.95 $\Omega \cdot$ mm for overlap distances of 2, 3 and 5 µm, respectively. This shows a progressive reduction in contact resistance with increasing recess-to-metallisation overlap

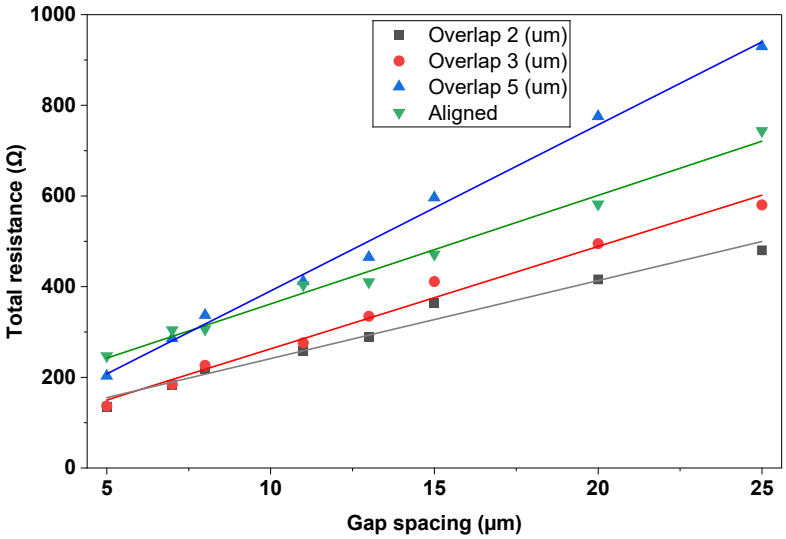


Figure 6.3 Total resistance as a function of gap spacing for the aligned and 2, 3 and 5 μm recess-metallisation overlap designs

The effect of separating the recess and metallisation regions was also investigated using the gap design. Table 6.1 summarises the extracted contact resistance for all the recess–metallisation geometries investigated.

Table 6.1 Extracted contact resistance for the different recess-metallisation designs.

Recess-metallisation design	Aligned	2 μm overlap	3 μm overlap	5 μm overlap	2 μm gap	3 μm gap	5 μm gap
R_C (Ω·mm)	8.7	4.8	2.2	0.95	74	-	78

The reference aligned design gave a high R_c of 8.7 Ω.mm which may have been due to misalignment during photolithography that created a gap. The overlap design gave lower contact resistances. However, in contrast, the 2 and 5 μm gap designs produced substantially higher R_c values of 74 and 78 Ω · mm, respectively. The similar values obtained for both designs indicate that the presence of a gap had a much greater influence on R_c than the difference between the two gap dimensions investigated. Further measurements would, however, be required to establish the dependence of contact resistance on gap distance.

The reduction in R_c with increasing overlap is consistent with the findings of Yazdani *et al* [20], who reported a decrease in contact resistance with increasing lateral recess-to-metallisation distance, with minimum resistance obtained when this distance became comparable to or greater than the contact transfer length. The optimum lateral distance was

also found to depend on the epitaxial structure and metallisation. In this study, R_c continued to decrease up to the maximum investigated overlap of 5 µm. The larger overlap distances over which this reduction was observed may reflect differences in the epitaxial structure, metallisation and corresponding transfer length. An optimum overlap distance was therefore not established, and the 5 µm overlap represents the lowest-resistance design within the investigated range.

6.5 RF HEMT Device Fabrication

In this section, we report our attempts to fabricate RF HEMT devices employing Si ion-implanted Ohmic contacts. Figure 6.4 shows a T-gate fabricated using the process developed in the group [191]. The devices shown in Figure 6.5, however, were fabricated using a different, SiN_x supported gate process. This involved blanket deposition of approximately 130 nm of SiN_x, followed by gate-foot lithography and etching of the exposed SiN_x. A separate lithography step defined the gate head, after which the gate foot and head were metallised together.

No functional RF HEMT devices were obtained using this fabrication sequence. SEM inspection revealed that the T-gates had fractured at the mesa edge, where the gate structure extended from the active device region towards the gate bond pad, as shown in Figure 6.5. This discontinuity prevented a reliable electrical connection between the gate electrode and the bond pad, thereby preventing the intended electrical characterisation of the fabricated devices.

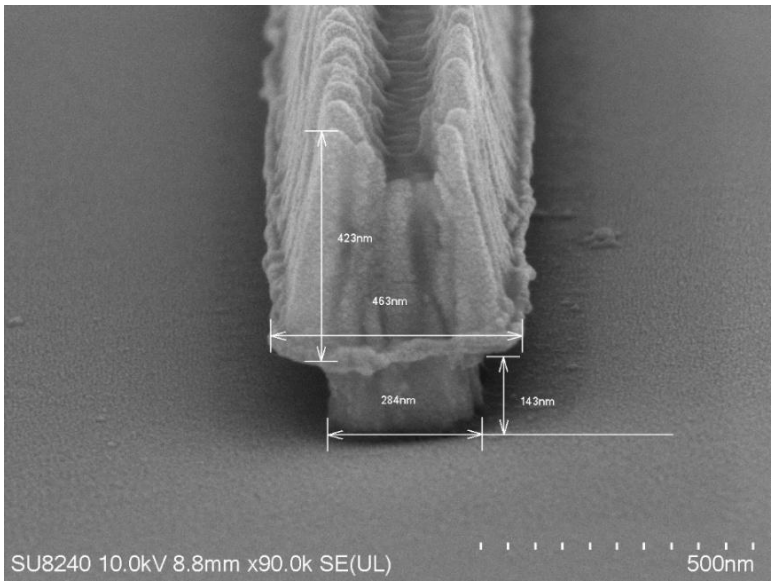


Figure 6.4 SEM image of the fabricated T-gate using the process recipe described in [191]

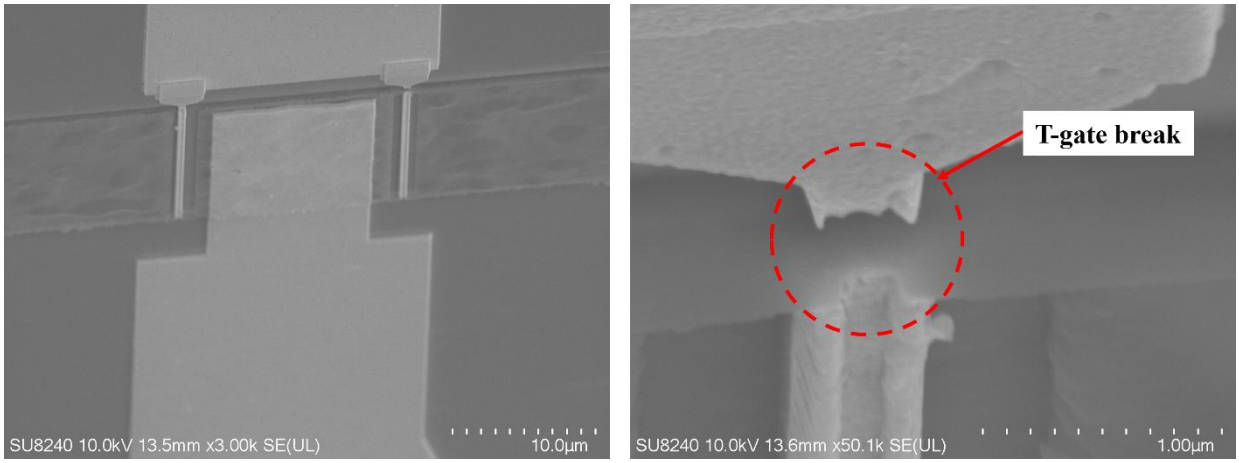


Figure 6.5 SEM of a fabricated RF HEMT with broken T-gate to bond pad connection

6.6 Summary

This chapter investigated the influence of recess-to-metallisation geometry on ohmic contact resistance. TLM structures were designed and fabricated with three configurations: aligned recess and metallisation edges, overlap distances of 2, 3 and 5 µm, and gap distances of 2, 3 and 5 µm. The electrical characterisation showed a clear dependence of contact resistance on the recess-to-metallisation geometry. The aligned structure produced an R_c of 8.7 $\Omega \cdot$ mm, which decreased to 4.8, 2.2, and 0.95 $\Omega \cdot$ mm for overlap distances of 2, 3 and 5 µm, respectively. In contrast, the 2 and 5 µm gap structures produced substantially higher R_c values of 74 and 78 $\Omega \cdot$ mm, respectively.

Overall, increasing the recess-to-metallisation overlap progressively reduced the contact resistance, while introducing a gap resulted in a substantial increase. The 5 µm overlap produced the lowest R_c among the configurations investigated; however, an optimum overlap distance was not established since R_c continued to decrease up to the maximum overlap investigated. These results demonstrate the importance of recess-to-metallisation positioning in the formation of low-resistance ohmic contacts.

7 Conclusions and Future Work

AlGaN/GaN and AlN/GaN heterostructures are attractive for high-frequency and high-power electronic devices, owing to their favourable material properties and 2DEG formed at the heterointerface. However, the resistance associated with the source and drain ohmic contacts can limit device performance, making the development of low-resistance contacts important. This thesis investigated three approaches to reducing ohmic contact resistance in these heterostructures: patterned recess structures, Si ion implantation, and recess-to-metallisation alignment. The results show that contact performance depends not only on the metal stack, but also on the modification and geometry of the semiconductor beneath the contact and its relationship with the subsequent metallisation.

7.1 Patterned Recess Ohmic Contacts

The first study investigated the influence of different recess patterns on Ohmic contact resistance. Three contact structures were considered: a $4\ \mu\text{m} \times 150\ \mu\text{m}$ horizontal recess, a $4\ \mu\text{m} \times 10\ \mu\text{m}$ recessed transfer length region, and a conventional planar contact without recess etching. The investigation was undertaken to determine whether localised patterning of the semiconductor beneath the Ohmic contact could provide lower contact resistance compared with a conventional planar contact. The $4\ \mu\text{m} \times 150\ \mu\text{m}$ horizontal recess pattern produced a contact resistance of $1.13\ \Omega \cdot \text{mm}$, while a slightly higher value of $1.18\ \Omega \cdot \text{mm}$ was obtained for the $4\ \mu\text{m} \times 10\ \mu\text{m}$ recessed structure. In comparison, the conventional planar contact produced the lowest contact resistance, with an extracted R_c of $0.81\ \Omega \cdot \text{mm}$. The results therefore show that the investigated localised patterns did not provide an improvement in contact resistance compared with the conventional planar contact, under the processing conditions used in this work.

7.2 Si Ion-Implanted Ohmic Contacts

The second study investigated Si ion implantation as an approach for reducing ohmic contact resistance in AlGaN/GaN and AlN/GaN heterostructures. Of the approaches investigated in this thesis, Si ion implantation produced the lowest contact resistance. For the blanket-implanted AlGaN/GaN heterostructure, the best contact produced R_c value of $0.10\ \Omega \cdot \text{mm}$ with a sheet resistance of $55\ \Omega/\square$, without post-metallisation annealing. Subsequent annealing at the investigated temperatures resulted in higher contact and sheet resistances,

indicating that an additional ohmic anneal was not beneficial for this structure under the conditions investigated. Blanket implantation was also investigated on an AlN/GaN heterostructure, with the contacts annealed at 800 and 850 °C for 30 s. The 800 °C condition produced R_c values between 0.46 and 0.75 Ω · mm, while values between 0.64 and 0.76 Ω · mm were obtained at 850 °C. The lowest contact resistance of 0.46 Ω · mm was therefore obtained following the 800 °C anneal. The implantation experiments therefore demonstrated low contact resistance in both material systems, although the magnitude of R_c and response to subsequent thermal processing differed. The work was subsequently extended from blanket to selective-area Si implantation, allowing implanted and un-implanted contact regions to be directly compared.

7.3 Recess-to-Metallisation Alignment

The final study investigated the influence of the relative position of the recessed semiconductor and ohmic metallisation using aligned, overlap and gap configurations. The aligned structure produced an R_c of 8.7 Ω · mm. Increasing the metallisation overlap from 2 to 3 and 5 µm progressively reduced R_c from 4.75 to 2.21 and 0.95 Ω · mm, respectively. The 5 µm overlap therefore reduced R_c by approximately 89% relative to the aligned structure. In contrast, the 2 and 5 µm gap structures produced much higher contact resistances of 74 and 78 Ω · mm, respectively. The results demonstrate that separating the metallisation from the recessed region severely degraded contact performance, whereas increasing overlap improved it over the range investigated. The study therefore establishes recess-to-metallisation positioning as an important fabrication parameter for recessed ohmic contacts. Although the 5 µm overlap produced the lowest resistance, it should not be regarded as the optimum overlap since larger dimensions were not investigated. The physical mechanism responsible for the alignment dependence also requires further investigation.

7.4 Contributions of the Research

The main contributions of this thesis are:

1. **Patterned recess contacts:** The influence of recess geometry was experimentally evaluated, showing that neither of the two patterned recess structures provided lower contact resistance than the conventional planar contact. This demonstrates that the introduction of localised recess patterns does not necessarily improve Ohmic contact

resistance and that their effectiveness depends on the specific recess geometry and processing conditions employed.

2. **Si ion implantation:** Si implantation produced the lowest contact resistance achieved in the thesis, with values approaching $0.1\ \Omega \cdot \mathrm{mm}$. The work also demonstrated the importance of activation and encapsulation. Extension to selective area implantation provided a route for evaluating the process in a device.

3. **Recess-to-metallisation alignment:** A systematic dependence of contact resistance on the relative position of the recess and metallisation was demonstrated. Increasing overlap progressively reduced R_c, while introducing a gap caused a substantial increase in resistance. This identifies lateral recess-to-metal positioning as an important fabrication consideration.

Together, these studies demonstrate that low-resistance contact formation in AlGaN/GaN and AlN/GaN heterostructures requires consideration of both the electrical modification and geometry of the semiconductor contact region, rather than the metallisation alone.

7.5 Future Work

The findings presented in this thesis have identified several areas that could be explored further to improve the understanding and development of low-resistance Ohmic contacts in III-nitride heterostructures. While the investigated approaches provided useful insight into the effects of recess patterns, Si ion implantation, and recess-to-metallisation alignment, further investigation would provide a more complete understanding of the mechanisms governing the observed contact behaviour and support further development of the associated fabrication processes.

Further work on the patterned recess contacts should investigate a wider range of recess dimensions, depths and pattern geometries. Since neither of the two localised recess patterns investigated produced lower contact resistance than the conventional planar contact, further optimisation could establish whether alternative recess geometries and etch depths can provide an improvement in contact resistance. Physical characterisation using AFM and cross-sectional TEM could also help distinguish the influence of recess geometry from surface modification, etch damage and metal coverage.

Further development of the Si ion implantation process should focus on selective area implantation for source and drain contact formation. Systematic variation of implantation dose and energy, together with Secondary Ion Mass Spectrometry (SIMS) and Hall measurements, would provide a better understanding of the relationship between the implanted Si profile, electrical activation, carrier concentration and contact resistance. The encapsulation and activation processes should also be investigated further to minimise surface degradation during high temperature activation. Evaluation across selectively implanted and un-implanted HEMTs would also allow the TLM-derived contact resistance to be correlated with device parameters such as on-resistance, drain current and transconductance, f_t and f_{max}. This would establish how improvements at the contact level translate into HEMT performance.

The recess-to-metallisation alignment study should be extended beyond the maximum overlap of 5 µm investigated in this work to determine whether contact resistance continues to decrease or eventually reaches a minimum. Future structures should also consider the relationship between the recess-to-metallisation distance and contact transfer length, rather than varying the overlap independently. Smaller gap dimensions, particularly below 2 µm, would help establish the alignment tolerance at which contact resistance begins to increase significantly. Cross-sectional SEM and AFM analysis of the recess boundary could further clarify the role of metal coverage, recess-edge morphology and lateral transport in the observed resistance dependence. Finally, the overlap configuration giving the lowest contact resistance could be incorporated into complete HEMTs to determine whether the improvement observed from TLM measurements translates into improved device performance.

Future work should focus on achieving reliable gate-metal continuity across the mesa boundary and integrating the research group T-gate process [191] with the Si ion-implanted Ohmic contacts. Further process optimisation could include developing a tapered mesa profile, refining the SiN_x gate-foot etch to ensure a continuous opening across the mesa transition, and improving the resist profile of the subsequent gate-head lithography to minimise metallisation shadowing. Dedicated metal-line test structures crossing the mesa edge, combined with cross-sectional SEM inspection and electrical continuity measurements, would help identify the origin of gate discontinuities and guide process optimisation before further RF device fabrication.

8 Appendix A

GaN HEMT Fabrication Processes

Sample Cleaning

- Immerse the sample in acetone in an ultrasonic bath for 5 minutes.
- Immerse the sample in isopropyl alcohol (IPA) in an ultrasonic bath for 5 minutes.
- Rinse with reverse osmosis (RO) water for 5 minutes.
- Blow dry with nitrogen (N_2).

A. Fabrication Using Photolithography

1. Markers

- Perform dehydration bake at 180 °C for 5 minutes.
- Spin coat LOR 3A at 3000 rpm for 60 seconds.
- Soft bake at 180 °C for 3 minutes
- Spin coat S1805 at 4000 rpm for 30 seconds.
- Soft bake at 115 °C for 3 minutes
- Expose using mask aligner (MA) 8 at a dose of 50 mJ/cm².
- Develop in MF 319 for 1 minute 45 seconds
- Rinse in RO water for 5 minutes.
- Blow dry with N_2.
- Visual inspection under microscope and take images
- Deposit Ti/Pt (20/80 nm) using a metal evaporator.
- Perform lift off in 1165 resist stripper for 10 minutes, with pipette assisted cleaning.
- Rinse in IPA for 30 seconds.
- Rinse in RO water for 5 minutes
- Blow dry with N_2.

2. Ohmic Pattern Recess

- Spin coat S1805 at 4000 rpm for 30 seconds.
- Soft bake at 115 °C for 3 min.
- Expose using the MA 8 at a dose of 50 mJ/cm² in hard contact mode.
- Develop in Microposit developer: H_2O (1:1) for 75 seconds
- Rinse in RO water for 5 minutes.
- Blow dry with N_2.
- Visual inspection under microscope and take images
- Etch using ICP 180 with BCl_3/Cl_2 = 5/10 sccm, RF and ICP power = 15/100 W, at 30 ℃ table temperature, 27℃ chiller temperature and 20 mTorr for 5 minutes.
- Remove the resist in warm 1165 overnight, followed by pipette assisted cleaning.
- Rinse in IPA.
- Rinse in RO water for 5 minutes
- Blow dry with N_2.

3. Ohmic Contact Deposition

- Spin coat LOR 10A photoresist at 6000 rpm for 30 seconds.

- Soft bake at 150 °C for 2 minutes on a hotplate.
- Spin coat S1818 photoresist at 4000 rpm for 30 seconds.
- Soft bake at 115 °C for 3 minutes on a hotplate.
- Expose using the MA 8 at 90 mJ/cm^2 in hard contact mode.
- Develop in MF319 developer for 2 minutes 30 seconds.
- Rinse in RO water for 5 minutes.
- Blow dry with N_2.
- Perform O_2 plasma ashing at 110 W for 2 min.
- Use Ar gun for 45 seconds in the electron beam evaporator
- Deposit Ti/Al/Ni/Au (30/180/40/100 nm) using the electron beam evaporator.
- Perform liftoff in 1165 resist stripper in a hot water bath for 4 hours, followed by pipette assisted cleaning.
- Rinse in RO water.
- Blow dry with N_2.
- Anneal using rapid thermal annealing (RTA) at 800 °C in an N_2 atmosphere for 30 seconds.

4. Mesa Isolation

- Spin coat S1818 at 4000 rpm for 30 seconds.
- Soft bake at 115 °C for 3 min.
- Expose using the MA 8 at 90 mJ/cm^2 in hard contact mode.
- Develop in Microposit developer: H_2O (1:1) for 75 seconds
- Rinse in RO water for 5 minutes.
- Blow dry with N_2.
- Visual inspection under microscope and take images
- Etch using ICP180 with Cl/Ar = 30/15 sccm, RF/ICP power = 65/650 W, at 4 mTorr for 60 seconds.
- Strip the resist in 1165 resist stripper in a hot water bath overnight
- Rinse in RO water.
- Blow dry with N_2.

5. Gate Contact Deposition

- Spin coat LOR 3A at 4000 rpm for 30 seconds.
- Soft bake at 150 °C for 2 minutes.
- Spin coat S1805 at 4000 rpm for 30 seconds.
- Soft bake at 115 °C for 3 minutes.
- Expose using MA 8 at a dose of 50 mJ/cm².
- Develop in MF319 for 1 minute 45 seconds.
- Rinse in RO water for 5 minutes
- Blow dry with N_2.
- Perform O_2 plasma ashing at 110 W for 1 min.
- Deposit Ni/Au (20/200 nm) using a electron beam evaporator.
- Perform liftoff in 1165 resist stripper in a hot water bath for 4hrs, followed by pipette assisted cleaning.
- Rinse with RO water.

- Blow dry with N_2.

6. Bond Pad Deposition

- Spin coat LOR 10A at 6000 rpm for 30 seconds.
- Soft bake at 150 °C for 2 minutes.
- Spin coat S1818 at 4000 rpm for 30 seconds.
- Soft bake at 115 °C for 3 minutes.
- Expose using the MA 8 at 90 mJ/cm^2 in hard contact mode.
- Develop in MF319 for 2 minutes 30 seconds.
- Rinse in RO water for 5 minutes.
- Blow dry with N_2.
- Perform O_2 plasma ashing at 110 W for 2 min.
- Deposit Ti/Au (20/400 nm) using electron beam evaporator.
- Perform lift-off in 1165 resist stripper in a hot water bath for 4 hrs, followed by pipette assisted cleaning.
- Rinse in RO water.
- Blow dry with N_2.

B. Ion Implantation

1. Etch Marker

- Spin coat AZ4562 photoresist at 4000 rpm for 60 seconds.
- Soft bake on a hotplate at 100 °C for 6 minutes 20 seconds.
- Allow the sample to rehydrate for 10 minutes prior to exposure.
- Expose using the MA6 mask aligner for 25 seconds.
- Develop in AZ400K:H_2O (1:4) for 2 minutes.
- Rinse in RO water for 60 seconds.
- Blow dry with N_2.
- Perform hard bake on a hotplate at 120 °C for 2 minutes.
- Etch using ICP180 with $BCl_3/Cl_2/Ar$ = 10/14/16 sccm, pressure = 5 mTorr, ICP/RF power = 800/200 W, for 1 minute 10 seconds.
- Strip the resist by soaking in warm 1165 resist stripper overnight.
- Rinse in IPA.
- Rinse in RO water for 5 minutes.
- Blow dry with N_2.

2. Selective Ion Implantation Mask

- Deposit a blanket layer of 350 nm SiO_2 using PECVD.
- Perform dehydration bake at 180 °C for 10 minutes.
- Spin coat AZ2020 photoresist at 4000 rpm for 30 seconds.
- Soft bake at 110 °C for 60 seconds.
- Expose using the MA8 mask aligner at a dose of 80 mJ/cm² (i-line filter, hard-contact mode).
- Perform post exposure bake (PEB) at 110 °C for 60 seconds.
- Develop in MF319 for 90 seconds, followed by two rinses in RO water for 15 seconds each.

- Deposit Ti/Ni (20/270 nm) using electron beam evaporator.
- Lift off in 1165 resist stripper in a hot water bath for 4 hours to expose the ohmic regions and mask other regions.,
- Perform ion implantation with energy of 250 keV, dose of 2×10^{16} cm^{-2}, and tilt angle of 7° (carried out at the University of Surrey).

3. Post Ion Implantation Processing

- Pre-dip the sample in HCl:H_2O (1:3) for 60 seconds.
- Rinse in RO water for 30 seconds.
- Etch Ni using HNO_3:H_2O (1:1) for 3 minutes.
- Rinse in RO water for 30 seconds.
- Etch Ti using Ti etchant for 10 seconds.
- Rinse in RO water for 60 seconds.
- Immerse in HCl:H_2O_2:H_2O (1:1:6) for 1 minute.
- Rinse in RO water for 5 minutes.
- Etch SiO_2 using buffered oxide etch (BOE 6:1) for 4 min.
- Rinse in RO water for 15 minutes
- Blow dry with N_2.
- Deposit a 200 nm SiO_2 encapsulation layer using PECVD at 350 ℃ for post implantation annealing.
- Perform RTA at 1100 °C for 120 s.
- Remove the encapsulation layer using BOE 6:1 for 5 min.
- Rinse in RO water for 15 minutes
- Blow dry with N_2.

C. Fabrication Using E-Beam Lithography

1. E-Beam Markers

- Spin coat 12% PMMA at 5000 rpm for 60 seconds.
- Soft bake at 180 °C for 5 minutes.
- Spin coat 2% PMMA at 5000 rpm for 60 seconds.
- Soft bake at 180 °C for 5 minutes.
- Expose using EBPG with dose = 825 μC/cm², beam current = 32 nA,
- Develop in IPA: MIBK (2.5:1) for 60 seconds at 23 °C.
- Rinse in IPA for 30 seconds.
- Rinse in RO water for 5 minutes
- Blow dry with N_2.
- Deposit Ti/Pt (20/80 nm).
- Perform lift off in 1165 resist stripper for 10 minutes, with pipette assisted cleaning.
- Rinse in IPA.
- Blow dry with N_2.

2. Mesa Isolation

- Spin-coat 15% PMMA at 4000 rpm for 60 seconds
- Soft bake at 180 °C for 5 minutes.
- Expose using EBPG with dose = 825 μC/cm², beam current = 100 nA,

- Develop in IPA: MIBK (2.5:1) for 60 seconds at 23 °C.
- Rinse in IPA for 30 seconds.
- Rinse in RO water for 5 minutes
- Blow dry with N_2.
- Etch using ICP180 (Cl/Ar = 30/15 sccm, RF/ICP = 65/650 W, 4 mTorr, 60 seconds).
- Strip the resist by soaking in warm 1165 resist stripper overnight.
- Rinse in IPA.
- Rinse in RO water for 5 minutes
- Blow dry with N_2.

3. Ohmic region Recess

- Spin-coat 12% PMMA at 5000 rpm for 60 seconds
- Soft bake at 180 °C for 5 minutes.
- Expose using EBPG with dose = 825 μC/cm², beam current = 32 nA,
- Develop in IPA: MIBK (2.5:1) for 60 seconds at 23 °C.
- Rinse in IPA for 30 seconds.
- Rinse in RO water for 5 minutes
- Blow dry with N_2.
- Etch using ICP 180 with BCl_3/Cl_2 = 5/10 sccm, RF and ICP power = 15/100 W, at 30 °C table temperature, 27°C chiller temperature and 20 mTorr for 5 minutes
- Strip the resist by soaking in warm 1165 resist stripper overnight.
- Rinse in IPA.
- Rinse in RO water for 5 minutes
- Blow dry with N_2.

4. Ohmic Contact Formation

- Spin coat 12% PMMA at 5000 rpm for 60 seconds.
- Soft bake at 180 °C for 5 minutes.
- Spin coat 2% PMMA at 5000 rpm for 60 seconds.
- Soft bake at 180 °C for 5 minutes.
- Expose using EBPG with dose = 825 μC/cm², beam current = 32 nA,
- Develop in IPA: MIBK (2.5:1) for 60 seconds at 23 °C.
- Rinse in IPA for 30 seconds.
- Rinse in RO water for 5 minutes
- Blow dry with N_2.
- Deposit Ti/Al/Ni/Au (30/180/40/100 nm).
- Perform lift off in warm acetone after 4 hours, with pipette assisted cleaning.
- Rinse in IPA.
- Rinse in RO water for 5 minutes
- Blow dry with N_2.
- Anneal at 825 °C in N_2 for 30 s.

5. T-Gate Fabrication

- Spin-coat 2% PMMA at 4000 rpm for 60 seconds
- Soft bake at 180 °C for 5 minutes.
- Spin coat 2% PMMA at 4000 rpm for 60 seconds
- Soft bake at 180 °C for 5 minutes
- Spin-coat LOR 3A at 4000 rpm for 30 seconds
- soft bake at 150 °C for 2 minutes.
- Spin-coat CSAR at 2000 rpm for 60 seconds
- soft bake at 150 °C for 2 minutes.
- Expose using EBPG (dose = 800 μC/cm², current = 4 nA).
- Develop CSAR in amyl acetate for 30 seconds at 23 °C.
- Rinse in IPA for 30 seconds
- Blow dry with N_2.
- Develop LOR in CD-26 for 20 seconds.
- Rinse in RO water for 5 minutes
- Blow dry with N_2.
- Develop PMMA in IPA: MIBK (3:1) for 30 seconds.
- Rinse in IPA for 30 seconds
- Blow dry with N_2.
- Perform O_2 plasma ashing for 1 minute.
- Deposit Ni/Au (20/300 nm).
- Lift-off in warm acetone for 4 hours.
- Rinse in IPA for 5 minutes

6. Bond Pad Metallisation

- Spin coat 15% PMMA at 5000 rpm for 60 seconds.
- Soft bake at 180 °C for 5 minutes.
- Spin coat 2% PMMA at 5000 rpm for 60 seconds.
- Soft bake at 180 °C for 5 minutes.
- Expose using EBPG with dose = 825 μC/cm², beam current = 64 nA,
- Develop in IPA: MIBK (2.5:1) for 60 seconds at 23 °C.
- Rinse in IPA for 30 seconds.
- Rinse in RO water for 5 minutes
- Blow dry with N_2.
- Deposit Ti/Au (20/400 nm).
- Perform lift off in warm acetone after 4 hours, with pipette assisted cleaning.
- Rinse in IPA.
- Rinse in RO water for 5 minutes
- Blow dry with N_2.

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