Switching Frequency Reduction in Pulse-Width Modulated Multilevel Converters and Systems

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Abstract

Multilevel converters have attracted a great deal of interest in recent years since they offer a number of advantages in many high voltage and high power applications, such as adjustable speed electric motor drives and power systems through Flexible Alternating Current Transmission Systems (FACTS) controllers and active harmonic filters. They can reach high voltages with low harmonics without the use of transformers or series-connected synchronised switching devices by their unique structures. Along with proper Pulse-Width Modulation (PWM) control scheme, they can also provide lower cost, higher performance, lower Electro-Magnetic Interference (EMI), and higher efficiency than the traditional PWM converters.

However, switching losses become a serious issue in high power applications. In order to improve the efficiency and reliability of the system, and reduce the size of the output filter, the stresses on the semiconductors and the development and manufacturing costs, reducing the switching frequency and associated losses of multilevel PWM converters and systems needs to be properly addressed.

The thesis gives an overview on multilevel converter topologies and control schemes. It then presents mathematical analysis towards further understanding of the Neutral-Point-Clamped (NPC) and the Flying Capacitor (FC) converters. The Fundamental Frequency Sinusoidal PWM (FF-SPWM) control method is examined as a potential "carrier" based approach in reducing the converter switching frequency and associated losses. The performance of multi-modular parallel connected systems based on the NPC and FC converters as a building block is reported along with the influence of the multicarrier PWM techniques. The voltage-unbalancing problem of the FC converter is addressed and a solution is provided. DSP based controllers for the three-level and the five-level FC converters have been developed and experimentally verified. Results taken from the laboratory prototype are presented to support the theoretical part of the project.

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List of Acronyms

AC	Alternating Current
A/D	Analogue to Digital
ACTR	compare Action Control
ADC	Analogue-to-Digital Converter
ADCFIFO	ADC result register
APOD	Alternative Phase Opposition Disposition
BJT	Bipolar Junction Transistor
CAL	Controlled Axial Lifetime
CAN	Controller Area Network
CD-MSPWM	Carrier Disposition Multi-carrier Sinusoidal PWM
CMOS	Complementary Metal-Oxide Semiconductor
COMCONx	COMpare CONtrol Register x
CPU	Central Processing Unit
CSI	Current-Source Inverter
CT	Current Transducer
D/A	Digital to Analogue
DAC	Digital-to-Analogue Converter
DBT	Dead Band Time
DBTCON	Dead-Band Timer Control
DBTCONx	Dead-Band Timer Control Register x
DC	Direct Current
DTC	Direct Torque Control
EMI	Electro-Magnetic Interference
EPSRC	Engineering and Physical Science Research Council
ESR	Equivalent Series Resistance
EVM	Evaluation Module
EVA	Event Manager A
EVB	Event Manager B
FACTS	Flexible Alternating Current Transmission Systems
FC	Flying Capacitor
FF-SPWM	Fundamental Frequency Sinusoidal PWM

GP	General Purpose
GPTCON	General Purpose Timer Control
GTO	Gate Turn-Off thyristor
H-MSPWM	Hybrid MSPWM
HVDC	High Voltage Direct Current
IGBT	Insulated Gate Bipolar Transistor
I/O	Input/Output
ISR	Interrupt Service Routine
JTAG	Joint Test Action Group
LED	Light Emitting Diode
LSB	Least Significant Bit
MIPS	Million Instructions Per Second
MOSFET	Metal-Oxide-Semiconductor Field Effect Transistor
MPS-SPWM	Modified Phase-Shifted Sinusoidal PWM
MSPWM	Multi-carrier Sinusoidal PWM
NPC	Neutral-Point Clamped
OCRA	Output Control Register A
PD	in-Phase Disposition
PI	Proportional Integral
PLL	Phase-Locked-Loop
POD	Phase Opposition Disposition
PS	Phase Shifted
PS-MSPWM	Phase-Shifted Multi-carrier Sinusoidal PWM
PWM	Pulse-Width Modulation
QEP	Quadrature Encoder Pulse
RAM	Random Access Memory
ROM	Read Only Memory
SCSR1	System Control and Status Register 1
SCSR2	System Control and Status Register 2
SFO-PWM	Switching Frequency Optimal PWM
SFO-PS-PWM	Switching Frequency Optimal Phase-Shifted PWM
S/H	Sample/Hold
SOC	Start-Of-Conversion

SPI	Serial Peripheral Interface
SPWM	Sinusoidal PWM
STATCOM	STATatic var COMpensator
SV-PWM	Space-Vector Pulse-Width Modulation
T2PINT	Timer 2 Period Interrupt
T2UFINT	Timer 2 Underflow Interrupt
TCSC	Thyristor Controlled Series Compensator
THD	Total Harmonic Distortion
TI	Texas Instruments
TxCON	Timer x Control Register
TxCNT	Timer x Counter Register
TxPR	Timer x Period Register
TxCMPR	Timer x Compare Register
UART	Universal Asynchronous Receiver-Transmitter
UPFC	Unified Power Flow Controller
UPS	Uninterruptible Power Supply
U.S.	United States
USA	United States of America
VSI	Voltage Source Inverter
VSC	Voltage Source Converter
VT	Voltage Transducer

List of Symbols

A	Midpoint of the phase leg A
$\hat{A}_c$	Amplitude of the carrier signal
A_k	Switch in the equivalent circuit of the FC topology
$\hat{A}_o$	Amplitude of the modulating signal
A1, A2	Operational amplifier 1 and 2
a	Coordinate
a	Coefficient for comparing the THD_v of the PD method with that of the FF-SPWM method
B	Midpoint of the phase leg B
B_k	Switch in the equivalent circuit of the FC topology, complementary of the switch A_k
b	Coordinate
b	Coefficient for comparing the potential switching losses of the PD method with that of the FF-SPWM method
C	Midpoint of the phase leg C
$C1$, $C2$, $C3$	Flying capacitor in the single-phase five-level FC converter
C_1, C_2, C_d	DC link capacitor
C_a, C_b, C_c	Flying capacitor in the phase A of the three-level FC converter
C_e	Capacitance of the flying capacitor
C1	Collector of the IGBT 2
Comp1, Comp2	Values in the compare register 1, and 2 or reference A, and B values
Comp3	Value in the compare register 3 or reference C value
C_{VCE}	Capacitor
c	Coordinate
D_1 to D_6	Antiparallel diode designator in the conventional converter
D_{a1} to D_{a4}	Antiparallel diode designator in the three-level converter
D_{b1} to D_{b4}	Antiparallel diode designator in the three-level converter
D_{c1} to D_{c4}	Antiparallel diode designator in the three-level converter
D_{a1} to D_{a8}	Antiparallel diode designator in the five-level converter
D_{ca1} to D_{ca6}	Clamping diode designator in the NPC converter
d_c	Duty cycle of i_c

d	Coordinate
E	Voltage source in the equivalent circuit of the FC topology
E_I	Output voltage of the PI regulator
E1, E2	Emitter of the IGBT 1 and 2
f_1	Fundamental frequency
f_c	Carrier frequency
f_s	Switching frequency
f_h	h-th harmonic frequency
f_o	Frequency of the modulating signal
$f_{sw,Sai}$	Switching frequency of the switch S_{ai}
G_1, G_2, G_3, G_4	Gating signals for main switches S_{a1} to S_{a4}
G_s	Gating signal
G_V	Transfer function of PI regulator
G1, G2	Gate of the IGBT
h	Harmonic order
I	Current source
$\hat{I}$	Current peak value
I^n	*n-th* harmonic load current
I^n_{Ak}	*n-th* harmonic current flowing through switch A_k
I^n_{Ck}	*n-th* harmonic current flowing through the flying capacitor C_k
I_{Ckavg}	Average current in the flying capacitor
I_o	Measured current
I_{PN}	Primary nominal rms current of the CT
I_S	Output current of the VT, CT
I_{Sai}	The rms current of the switch S_{ai}
I_{SN}	Secondary nominal rms current
I_c	Collector current of the IGBT
I_{cnom}	Normal collector current of the IGBT
I_{kavg}	Average current in switch k
i_a, i_b, i_c	Output phase current of phase A, B, and C
i_{ai1} (i=1, 2, ... N')	Fundamental part of the output current of *i-th* module
i_{af}	Fundamental component of the total output phase current
i_n	Current flowing to the negative point N of the DC rail

i_o	Load current or output current
i_{cap}	Current flowing through the capacitor
i_O	Current flowing to the neutral point O of the DC rail
i_p	Current flowing to the positive point P of the DC rail
$\bar{i}_p$, $\bar{i}_n$, $\bar{i}_O$	Average currents
i_{sa}, i_{sb}, i_{sc}	Current of phase A, B, and C in the AC side of the NPC rectifier
$i_{Sai}(t)$	The instantaneous current of the switch S_{ai}
$i_T(t)$	Current flowing through the switch, instantaneous value
K_P, K_I, K_0, K_1	Coefficients of the G_V function
K_N	Conversion ratio of the VT, CT
k_1, k_2	Coefficients of the amplifier circuit
L	Inductor
L'	Equivalent inductance in the equivalent circuit of the parallel-connected models
L	Length of the Look-up table
L_s	Reactor in the AC side of the NPC rectifier
m	Number of phase voltage levels
m_a	Amplitude modulation ratio
m_f	Frequency modulation ratio
m'_f	Switching frequency ratio for the new carrier-based SWPM scheme
N	No charging or discharging for the capacitor
N	Negative point of DC rail of the converter
N_{s1}, N_{s2}, N_{s3}, N_{s4}	Number of the switching transitions per fundamental period for main switches of the upper part of the phase A leg
N_{total}	Sum of the above N_{si}, i=1, 2, 3, 4.
N_{3total}	Total number of switching transitions per modulating period for the three-phase system.
N'	Number of modules
n	Neutral point of the three-phase AC mains in Y connection
n'	Neutral point of the three-phase loads in Y connection
O	Neutral point of DC rail of the converter
P	Positive point of DC rail of the converter
P_A, P_B, P_C	Table pointer for sinusoidal reference value A, B and C

PI, PI1, PI2, PI3	Proportional integral regulators
PWM1 to PWM8	PWM outputs, or gating signal for S_{ai}
p	Number of pairs of switches in the FC converter leg
p_T	Instantaneous power dissipation in a switch
q	Coordinate
R	Resistor
R_1 to R_8	Resistors
R'	Equivalent resistor in the equivalent circuit of the parallel-connected models
R_G	Gate resistor of the IGBT
R_L	Load resistor
R_M	Measuring resistor of the VT, CT
R_s	Resistor
R_{VCE}	Resistor between the V_{CET1} and E pins
R_1	Primary resistor of the VT
S_i, $i=a,b,c$	Switching functions
S_{ij} , $i=a,b,c$, $j=p,n,o$	Switching functions
S_{a1} to S_{a8}	Main switch designator in the five-level converter
S_{c1} to S_{c4}	Main switch designator in the three-level converter
S_7, S_8	Switches in the charging circuit
$S1$ *to* $S4$	Carriers of the new carrier-based SWPM scheme
s	Number of DC sources in the cascaded converter
THD_v	Total Harmonic Distortion of the line-to-line voltage V_{ab}
T'	Time interval, equals to one fourth of the T_s
T_{samp}	Sampling time, or equals to the carrier period T_s here
T_{max}	Maximum time width of switching states
T_o	Period of output waveform or Period of modulating signal
T_{on}	Switch conduction time interval
T_{off}	Switch off time interval
T_s	Period of triangular carrier signal
T_s'	Period of the new carrier signal
T_{sp}	Time interval between two successive peak values (positive and

	negative one) of the triangular signal
t	Time
$t_{blanking}$	Error Blanking time
$t_{c(on)}$	Switch turn-on crossover interval
$t_{c(off)}$	Switch turn-off crossover interval
$t_{d(on)}$	Switch turn-on delay interval
$t_{d(off)}$	Switch turn-off delay interval
t_{fi}	Current fall time
t_{fv}	Voltage fall time
t_j, t_{j+1}, t_{j+2}	Corresponding dwell times of the space vector V_j, V_{j+1} and V_{j+2} in the period T_{samp}
t_{on}, t_{off}	Original unadjusted time point value
t_{on}', t_{off}'	New adjusted time point value
t_{ri}	Current rise time
t_{rv}	Voltage rise time
t_0, t_1, t_2	Corresponding dwell times of the space vector V_0, V_1, V_2 in the period T_{samp}
t_{1on} t_{4on}	Switching time points when the switch S_{a1} transits from turn off to turn on
t_{1off} t_{4off}	Switching time points when the switch S_{a1} transits from turn on to turn off
Δt_c	Time interval
Δt	Adjusting time for every selected switching state
Δt_x, Δt_y	Adjusting times for t_{on} and t_{off}
Δt_1, Δt_2, Δt_3	Adjusting time period for the flying capacitors $C1$, $C2$ and $C3$
V_{ab1}	Peak value of the V_{ab} at the fundamental frequency
V_{abh}	Peak value of the V_{ab} at the h-th harmonic frequency
V_{AN}^n	n-th harmonic of V_{AN}
V_{AO1}	Fundamental component of the total output phase voltage
V_{aoi1} (i=1,2,... N')	Fundamental part of the output voltage of *i-th* module
V_{ao1}	Fundamental part of the equivalent voltage in the equivalent circuit of the parallel-connected models
V_{Ck}^n	*n-th* harmonic voltage V_{Ck}

V_{C3}, V_{C2}, V_{C1}	Actual average values of the flying capacitors
V_{CE}	Collector emitter voltage of the IGBT
V_{CES}	Collector emitter voltage of the IGBT (absolute maximum value)
V_{DD}	Power source voltage of the drive card (for the digital signal)
V_d	Voltage source in the simplified clamped inductive-switching circuit
V_{dc}	DC source voltage
V_{dc1}, V_{dc2}	DC link capacitor voltage
V_I	Input voltage of the PI regulator
V_j, V_{j+1}, V_{j+2}	Space Vectors
V_M	Voltage across the measuring resistor of the VT, CT
V_o	Output voltage of the operational amplifier A2
V_{o1}	Output voltage of the operational amplifier A1
V_{on}	On-state voltage value of the switch
V_{ref}	Reference or modulating value
V'_{ref}	Normalised reference sine value
V_S	Input voltage into operational amplifier A2 positive input pin
V_{sa}, V_{sb}, V_{sc}	AC mains voltage sources
$V_{san}, V_{sbn}, V_{scn}$	Voltages
V_0 to V_6	Space Vectors
$\hat{V}_{AO}$	Amplitude of the phase voltage
$\hat{V}_{AO1}$	Amplitude of the fundamental frequency component of the V_{AO}
$\hat{V}_{AB1}$	Amplitude of the fundamental frequency component of the line-to-line voltage V_{AB}
$\hat{V}_s$	Peak value of the line-to-neutral voltage of the mains
V^*	Reference voltage vector
V^*_{C3} V^*_{C2} V^*_{C1}	Reference voltages for the three flying capacitors in the five-level FC converter
ΔV_c	Voltage variation across the flying capacitor
v_{AB}	Instantaneous value of the line-to-line voltage
v_{AN}, v_{BN}, v_{AO}	Instantaneous value of the phase voltage
v_{Con1a}, v_{Con2a}	Phase output voltage of one unit in the cascaded converter
v_{Con3a}, v_{Con4a}	Phase output voltage of one unit in the cascaded converter

$v_{carrier}$	Carreir instantaneous value
v_o	Instantaneous value of the output voltage
v_{offset}	Instantaneous average of the maximum and minimum values of the three reference voltages
v_{ref}	Reference instantaneous value
v_{refA}, v_{refB}, v_{refC}	Reference values
$v_{refA,SFO}$, $v_{refB,SFO}$	Reference values for the SFO-PWM method
$v_{refC,SFO}$	Reference values for the SFO-PWM method
v_{ref1}, v_{ref2}	Reference instantaneous value
v_T	Blocking voltage across the switch
$W_{c(on)}$	Energy dissipated in a switch during the turn-on transition
$W_{c(off)}$	Energy dissipated in a switch during the turn-off transition
W_{on}	Energy dissipation in the switch during the on-state interval
Z^n	*n-th* harmonic load impedence
ω	Angular speed
α	Initial phase angle of the phase *A* of the voltage source
ϕ	Phase shift angle between the current and the output voltage at fundamental frequency.
ϕ_k	Fundamental frequency voltage/current displacement angle
ψ^n	*n*-th harmonic voltage/current displacement angle
θ	Angle in radium
θ_c	The angle in radians of the carrier period
θ_m	Phase shifting angle between two adjacent carriers in a module
θ_{sh}	Phase shifting angle between corresponding carriers in adjacent modules
φ	The displacement angle between the modulating signal (sinusoidal) and the first positive triangular carrier signal
$\mathcal{R}_k$	Duty cycle of switch *k*
$\mathcal{R}_{k+1}$	Duty cycle of switch (*k*+1)

Chapter 1: Introduction

1.1 Background

Recent advances in fully-controlled semiconductor switching capability and increases in their power ratings combined with the desire to improve the efficiency and performance of power electronic systems have been making these enabling technologies a fast-growing field. Nowadays, power electronic technologies influence the design of every system, from office equipment and home appliances to high-speed transportation systems and satellites to name just a few. Applications in both light and heavy industry, such as computer networks, electronic equipment, telecommunications industry, etc. are improved with power electronics support and use [1].

Power electronic circuits function by using semiconductor devices as digital switches, thereby controlling and/or modifying voltages and currents. They convert electric power from one form to another by matching the voltage and current requirements of the load to the available source. These power electronic circuits are commonly known as static converters.

Converters are generally classified by the relationship between the type of input and output as follows:

- Rectifiers (AC-DC).
- Inverters (DC-AC).
- Choppers (DC-DC).
- Cyclo-converters (AC-AC).

The inverter circuits can be mainly divided into two classes with respect to the type of source used at the input as follows: Current-Source Inverters (CSIs) and Voltage-Source Inverters (VSIs) where the DC input to the inverter is an inductor or a capacitor respectively. Some of the most promising technology for medium power levels is based on VSI technology. CSI-based systems remain the only alternative to extra high power electric motor drives mainly due to their inherent characteristic that protects them against short-circuit.

The VSIs can be divided into two general categories in terms of the control methods employed: Pulse-Width Modulated (PWM) and square-wave inverters. Among these inverters, PWM inverters show superiority and have wide applications [1]. In such

inverters, the input DC voltage is essentially constant in magnitude; therefore, the inverter must control the magnitude and the frequency of the AC output voltage. This is achieved by applying the so-called PWM control to the inverter switches. There are various schemes to control the inverter switches in order to shape the output AC voltage to be as close to a sinusoidal waveform as possible.

In terms of the characteristics of the output phase voltage typically defined between the phase mid-point and the neutral point of the DC bus, the converters can be classified into two broad categories, namely, the conventional converters (also known as two-level converters) and multilevel converters where the phase voltage waveform has m levels or steps ($m \geq 3$).

1.2 Conventional VSIs

1.2.1 Topologies of Conventional VSIs

Conventional VSIs refer to two-level inverters in which the phase voltage defined between the midpoint of each leg and the fictitious neutral point of the DC bus has only two values. In these inverters the mid-point of the DC bus may not be available for a number of applications, but it is technically created by splitting the DC bus capacitor into two. In three-phase four-leg systems such point may be used to regulate the neutral currents but in this study such cases will not be considered. For conventional inverters, there are three basic configurations as follows: the single-phase half-bridge inverter, the single-phase full-bridge inverter, and the three-phase inverter, which are shown in Figs. 1.1, 1.2, and 1.3 respectively.

A single-phase half-bridge VSI consists only of one "leg" with two switches and two antiparallel diodes. It is the basic building block of any other switch mode VSI. Specifically, the combination of the switching blocks (S_1 and the anti-parallel diode D_1) and (S_2 and D_2) can be used as a "leg" to build three-phase and other type of converters with paralleling of "legs". A single-phase full-bridge VSI consists of two "legs". The load is connected between the midpoints of the inverter "legs". The three-phase inverter has three "legs", which is commonly known as six-pulse inverter.

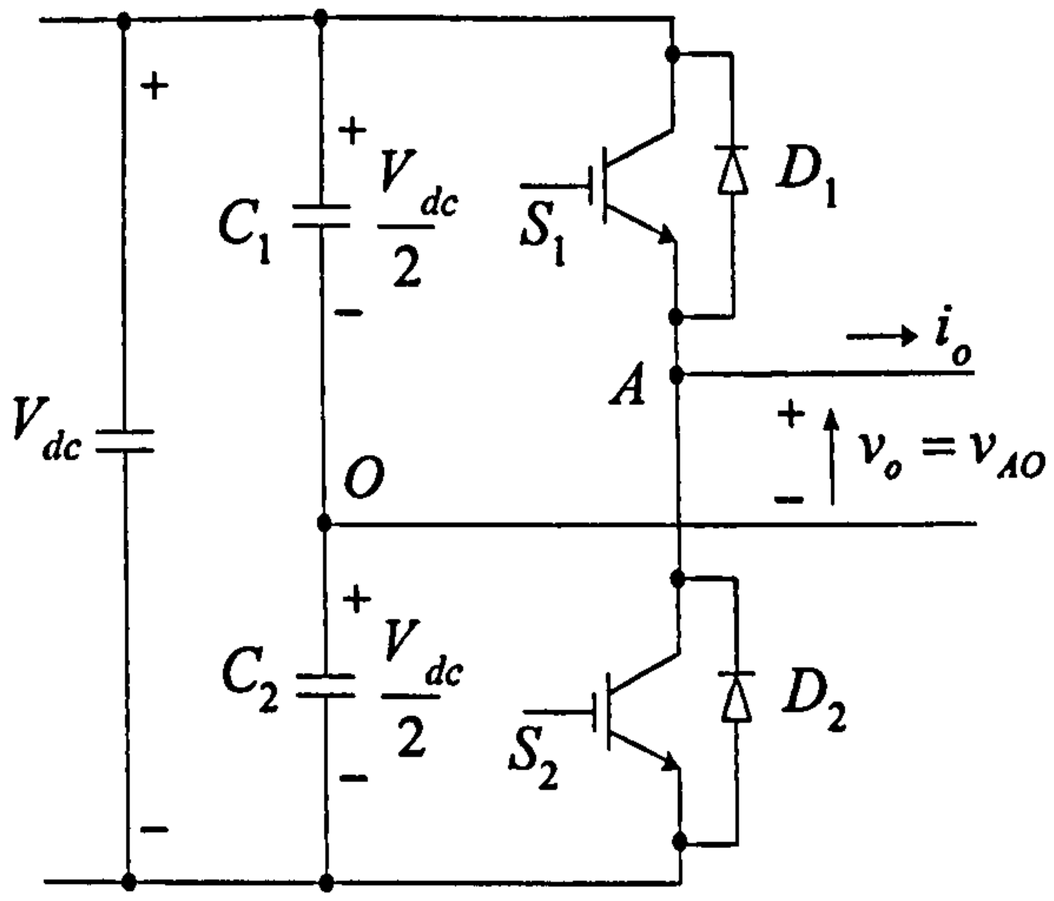


Fig. 1.1: A single-phase half-bridge VSI circuit.

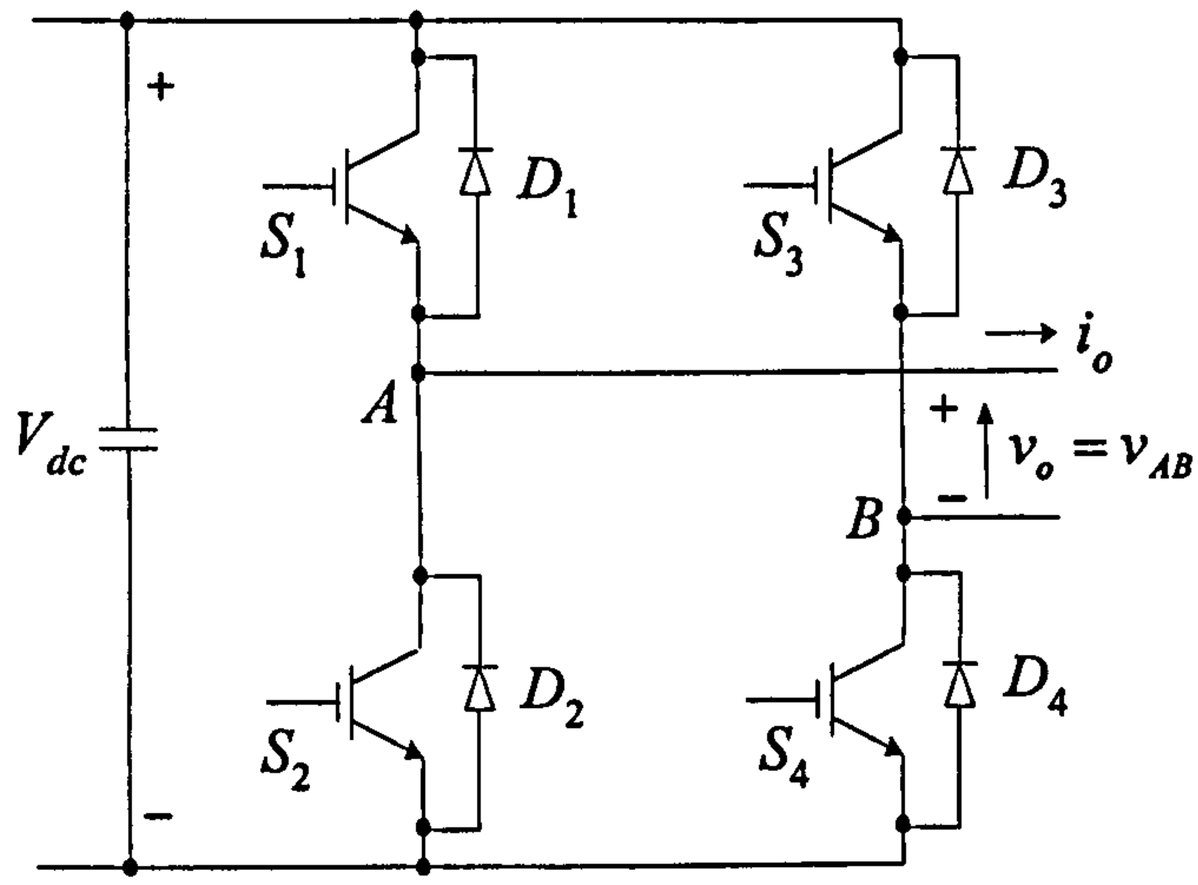


Fig. 1.2: A single-phase full-bridge VSI circuit.

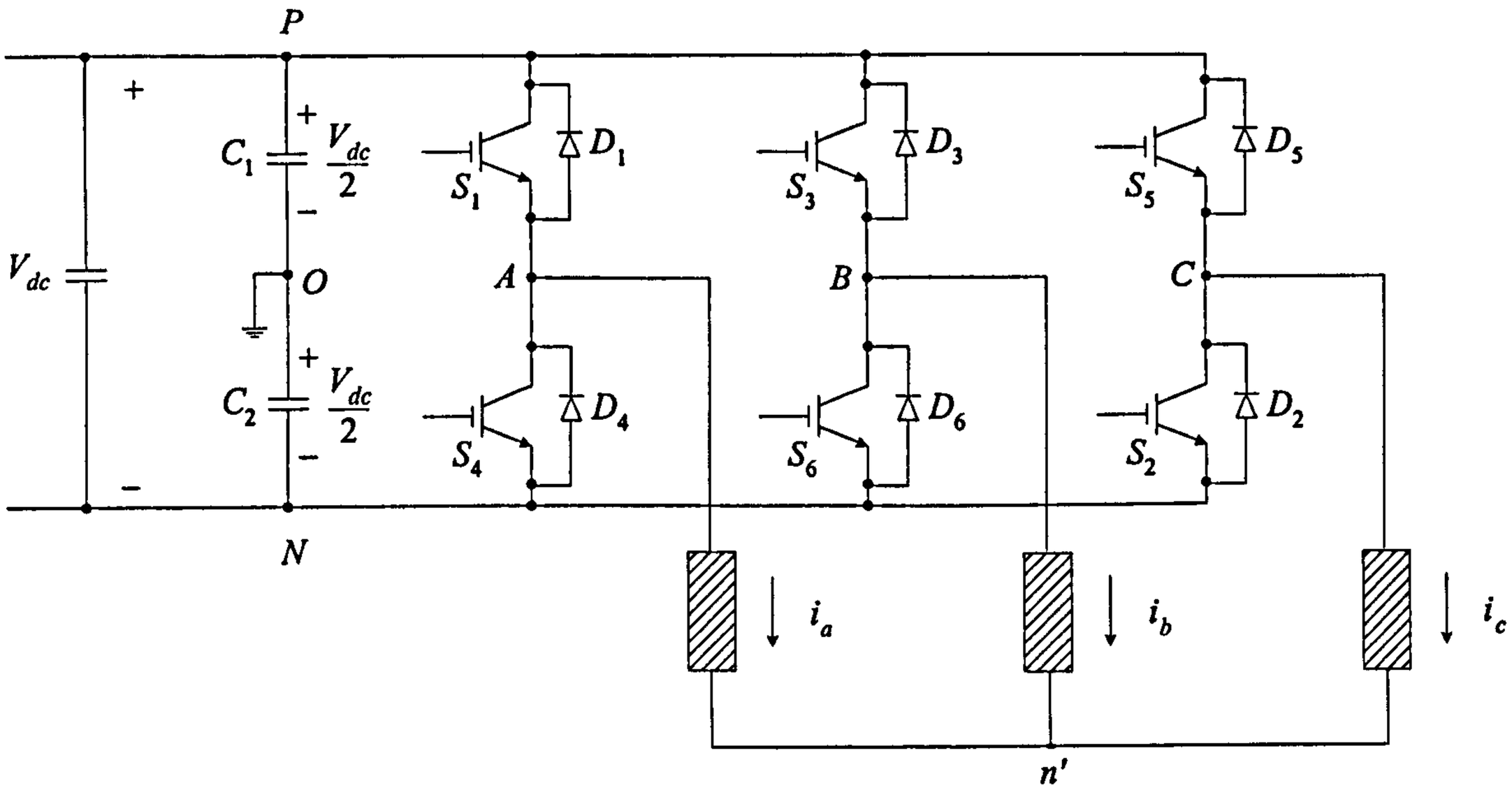


Fig. 1.3: A conventional three-phase VSI circuit.

1.2.2 Limitations of Conventional VSIs

A number of drawbacks can be identified when the standard two-level, six-pulse inverters are used in high voltage, high power applications, e.g. in utility applications [2]. Firstly, when the power handling capability of a two-level converter exceeds the ratings of an individual switching device, the six-pulse inverter must use series connected devices in order to be able to block the DC bus voltage. The number of devices, which can be placed in series, is limited by the need for dynamic and static voltage sharing. To ensure the dynamic voltage sharing, large snubber components are used and the turn-off time of each device must be carefully controlled so that all devices share equally the voltage stresses. Turn-on and turn-off coordination of long strings of semiconductor devices become difficult. The number of devices that can be successfully connected in series in this fashion is limited and device utilisation is generally poor. The snubber losses can also become significant [2].

Secondly, the harmonic performance of the inverter is poor unless the PWM control method with high switching frequencies is used. For converters designed to be used in utility applications, when high switching frequencies are employed, the switching losses can be comparatively high.

In order to overcome the limitations of a single inverter topology, six-pulse inverters have been connected together through zigzag arrangement transformers. This solution has been used in medium and high power applications. This arrangement, also called multi-pulse inverter, can reduce their harmonic content and combine their output power. However, the required custom-built transformers: [3]

(1) are the most expensive equipment in the system;

(2) produce about 50% of the total losses of the system;

(3) occupy a large area of real estate, i.e. about 40% of the total system;

(4) cause difficulties in control due to DC magnetizing and DC over-voltage of the inverters resulting from saturation of the transformers;

(5) are usually unreliable.

1.3 Multilevel Inverters

In order to address the previously mentioned problems, an alternative type of inverters known in the technical literature as multilevel inverters have been proposed [3]-[6]. The key properties of a multilevel structure are as follows [7]:

1. Its structure allows it to process high voltages while generating low harmonics without the use of transformers or series-connected synchronised switching devices.
2. The efficiency is much higher and can be more than 90%. In the technical literature [8], it is indicated that the multilevel converter has an efficiency greater than or equal to 96% for loads greater than 10% of rated power, whereas the two-level PWM inverter does not achieve 90% efficiency until it is loaded to greater than 30% of rated power. The multilevel converter had efficiency greater than 98% for loads greater than 40% of rated power, but the PWM inverter had a maximum efficiency of 95.6% which was achieved at a loading factor of 95%. The efficiency for a single multilevel inverter is greater than 90% over most of its operating range.
3. It generates an *m*-step staircase waveform of output voltage with the line frequency switching and without converter transformers for an *m*-level converter, thus reaching an almost pure sinusoidal output voltage by increasing the number of levels.
4. Electro-Magnetic Interference (EMI) level is much lower because *dv/dt* at switching is 1/(*m*-1) of that of the conventional two-level converters.
5. It can increase the voltage handling capability. If the devices operate at their full safe operating limit, then the total operating voltage will be multiplied by the number of steps in the output (*m*-1 steps for *m* level inverter). For example, a five level converter, using devices capable of blocking $V_{dc}/4$ volts will generate a total voltage of V_{dc}.

In summary, multilevel inverter technology along with proper PWM control scheme can provide lower cost, higher performance, lower EMI, and higher efficiency than its traditional two-level counterpart.

1.4 Literature Survey

The results of a patent search showed that multilevel inverter circuits have been around for more than 25 years [9]. An early traceable patent appeared in 1975 [10], in which the cascade inverter was first defined with a format that connects separately DC-sourced full-bridge cells in series to synthesise a staircase AC output voltage. Through manipulation of the cascade inverter, with diodes blocking the sources, the diode-clamped multilevel inverter was then derived [11]. The diode-clamped inverter was also called the Neutral-Point Clamped (NPC) inverter when it was first used in a three-level inverter in which the mid-voltage level was defined as the neutral point *O* as illustrated in Fig. 1.4.

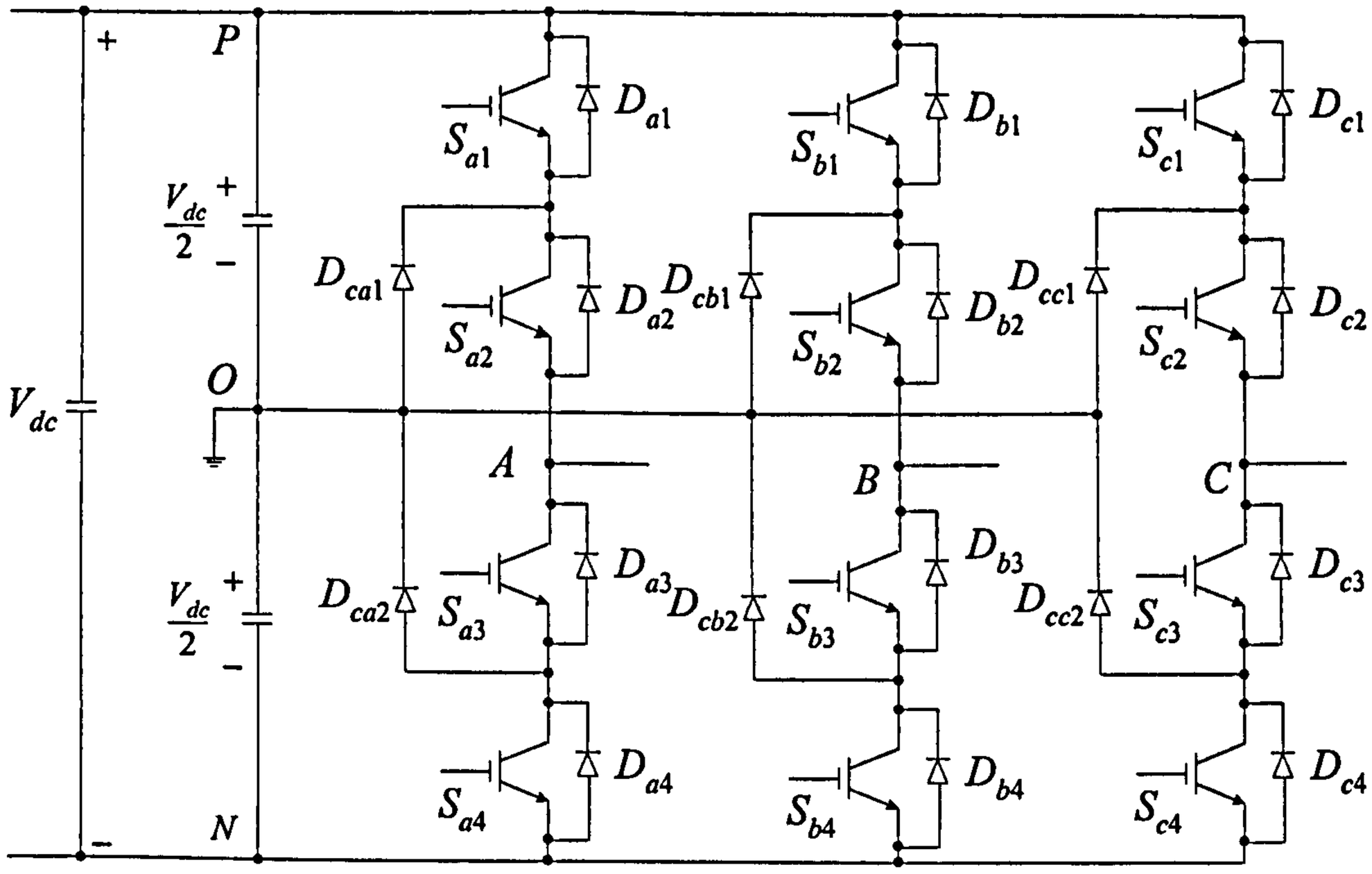


Fig. 1.4: A three-phase three-level NPC inverter.

The term multilevel starts with the three-level inverter introduced in 1980 by Nabae *et al.* [12]. In this circuit, a neutral-point diode clamp was realised in order to limit the voltage stress of one device to the value of the divided DC intermediate voltage. The leg-voltage can take three different levels. Moreover, the main switches when turning off are exposed to the stresses of $V_{dc}/2$ thus making it applicable to high power applications. Later in 1983, Bhagwat and Stefanovic extended the three-level to multilevel topologies [13]. The contributions by these researchers on multilevel topologies gave a new idea for developing high voltage and high power converters.

Additionally, the availability of improved technology of fully controlled semiconductors suitable for high-voltage high-power applications and the development of related technology such as microcomputer and control methods offered new opportunities in converter technology [14]. Since the early 1980s, it has become a popular research topic in many areas including high power electric drives and VAr compensation through FACTS controllers. This affected not only the developed theories and associated topologies but also the commercial products offered by industry in this area of technology.

In the last two decades, various multilevel concepts, topologies and control methods have been introduced [5], [16]-[21], [37]-[39]. A number of multilevel converters have been reported in the technical literature [12]-[17]. Specifically, the most promising ones

are as follows: the NPC converter [12], the Flying Capacitor (FC) converter [2], [5], [15] and the cascaded converter with separate DC sources [5], [10], [22], [23].

The three-level NPC converter effectively doubles the device voltage level without precise voltage matching, thus this topology prevailed in the 1980s. The application of the NPC converter and its extension to multilevel structures was found in [24].

Although the cascaded converter was invented earlier, its applications did not prevail until the mid–1990s. Two major patents [25], [26] were filed to indicate the superiority of cascaded inverters for motor drive and utility applications. Due to the great demand of medium-voltage high-power inverters, the cascaded converter has drawn tremendous interest ever since. For instance, several patents were found for the use of cascaded inverters in regenerative-type motor drive applications [27]–[29].

The last entries for U.S. multilevel converter patents, which were defined as the capacitor-clamped multilevel inverters, came in the 1990s [30], [31].

The converter technology highly relies on control as well. On this front numerous technical papers have been written in the last two decades. The two multilevel PWM methods most discussed in the literature are multilevel carrier-based PWM and multilevel Space-Vector PWM (SV-PWM). Both are extensions of traditional two-level PWM strategies to several levels. Some investigators have proposed carrier-based multilevel sine-triangle PWM schemes for control of a multilevel diode-clamped inverter used as a motor drive or STATic var COMpensator (STATCOM) [37]-[39]. Others have generalised the SV-PWM theory for use with multilevel inverters [21].

The applications under research cover large motor drives for electric trains [41], Thyristor Controlled Series Compensator (TCSC), High Voltage Direct Current (HVDC) systems [42], [43], renewable energy [44], STATCOMs [45] [46], controllers for Flexible Alternating Current Transmission Systems (FACTS) [47] and so on. Today, multilevel inverters are also extensively used in high-power applications with medium voltage levels. The field applications include use in laminators, mills, conveyors, pumps, fans, blowers, compressors, and so on [9].

Many well-known international electric companies such as ABB, Siemens, and Toshiba have developed three-level NPC-based products which are applied to high power electric motor drives, reactive power compensation, switched source etc. The first Unified Power Flow Controller (UPFC) in the world was based on the three-level NPC inverter [48]. GEC Alstom T&D has commercialised the cascaded multilevel converter for reactive power compensation/generation [9].

Even though in different fields of applications, multilevel inverters represent a high potential for realisation of high power controllable conversion systems of different nature such as, rectifiers, inverters, high power amplifiers etc., with certain topologies the number of achievable voltage levels is limited due to voltage unbalance problems, voltage clamping requirements, circuit layout, and packaging constraints [5]. Such problems have been addressed and a number of solutions are available either via improved control techniques [18]-[21] or topologies [5].

The voltage unbalancing problem exists in all the three multilevel topologies previously mentioned to different extent. The voltage unbalancing problem and the mechanism of the NPC converter were discussed in [50]. Reference [6] suggested that the voltage-unbalancing problem could be solved by using a back-to-back rectifier/inverter system and proper balancing control. Reference [4] suggested the use of additional voltage balancing circuits, such as a DC chopper. The cascaded inverter has inherent self-balancing characteristics because of the circuit component losses and limited controller scheme, which ensures DC voltage balance [6]. For the FC inverter, voltage unbalancing is relatively complicated and in many cases could become troublesome. [15] [51].

A number of references have addressed the voltage unbalance issue with the flying capacitors [4], [51]-[58]. A direct staircase angle control for balancing the capacitor voltage in cases where the typical PWM control does not exist, such as Direct Torque Control (DTC), sliding mode control and control by hysteresis was introduced in [52], [54], [55]. A swap technique was employed together with Carrier Disposition Multi-carrier Sinusoidal PWM (CD-MSPWM) methods to ensure capacitor voltage balancing in [53]. A spontaneous clamping capacitor current control loop under the Phase-Shifted Multi-carrier Sinusoidal PWM (PS-MSPWM) was applied to the three-level FC converter [51]. The additional voltage balancing circuit serving as DC chopper was proposed in [4]. However, most of the previously mentioned work focuses on the open-loop control and analysis of the control method properties applied to the ideal circuit. Very limited information is available regarding a possible closed-loop control to address this issue.

A number of multilevel converters have been reported in the technical literature [12]-[21], but mainly focus on their concepts, topologies and control methods as well as the harmonic performance. Little work deals with switching losses reduction. However, switching losses become a serious issue in the high power applications. In order to improve the efficiency and reliability of the system, reducing the switching frequency and associated losses of multilevel PWM converters and systems is very important.

This project, funded by EPSRC, was aimed at reducing the switching frequency and associated losses of multilevel PWM converters and systems. This was expected to reduce the size of the output filter if it provides a higher bandwidth and simultaneously to reduce the stresses on the semiconductors and the development and manufacturing costs besides improving the efficiency and reliability of the system. Furthermore, it could make the converter and system more competitive as a commercial product using Insulated Gate Bipolar Transistors (IGBTs) or similar technology.

1.5 Thesis Objectives

The objectives of the thesis based on the project research can be summarised as follows:

- To give an overview on multilevel converter topologies and control schemes (Chapter 2).
- To develop a further understanding of both the NPC converter and the FC converter circuits (Chapters 3 and 4).
- To develop an understanding of multi-modular converter systems based on the NPC and FC converters as basic modules (Chapter 6).
- To investigate the parallel-connected multi-modular multilevel NPC and FC converter systems (Chapter 6).
- To compare the performance of each system under higher switching frequency generated by the Sinusoidal PWM (SPWM) and the Fundamental Frequency SPWM (FF-SPWM) control and address critical implementation issues (Chapter 6).
- To reduce the switching frequency and associated losses in PWM multilevel converters using a simple carrier-based method (Chapter 3).
- To investigate different multi-carrier based SPWM control methods' influence on the performance of the NPC converter (Chapter 3).
- To contribute to the understanding of the PS-MSPWM control scheme suitable for the FC converter topology (Chapter 4).
- To address the voltage-unbalancing problem associated with a typical five-level FC converter (Chapter 5).
- To verify experimentally with laboratory prototypes the theoretical part of the project (Chapter 7).

In summary, this has been a challenging project, which involved analysis, design and implementation of multilevel PWM converters.

1.6 Thesis Organisation

This thesis is organised into chapters in the following way.

Chapter one introduces the background of the research work, gives the literature survey and summarises the project motivation and aims. This is followed by a section on the thesis organisation.

Chapter two gives an overview on multilevel converter topologies, along with their features and applications. The switching modulation strategies are reviewed and the SPWM is described in detail.

Chapter three focuses on the NPC converters and suitable control strategies. Firstly, the modelling of the NPC converter in both the rectifier and inverter mode is presented. Secondly, the operation principles of the NPC are described. Thirdly, different Multi-carrier SPWM (MSPWM) methods based on the CD-MSPWM switching strategy suitable for the NPC converter are analysed and compared. Attention is paid on the influence of the individual control method on the switching losses of the converter, and harmonic performance. Finally, in order to minimise the switching losses, the FF-SPWM technique is proposed and investigated.

Chapter four focuses on the FC converters and suitable control strategies. First, the principles of operation and the mathematical modelling of the FC converter are described. Then, four kinds of multi-carrier-based PWM techniques when applied to the five-level FC converter are presented. The effects of each PWM technique on each switch utilisation, switching losses of the converter, the self-balancing property for flying capacitor's voltage, and harmonic spectrum of the output line-to-line voltage are investigated. Finally, simulation results based on the performance of a five-level FC converter under different PWM techniques are given.

Chapter five proposes the Modified Phase-Shifted SPWM (MPS-SPWM) method which combines the phase-shifted SPWM with a new voltage balancing control algorithm. This method is expected to solve the voltage unbalancing problem.

Chapter six extends the NPC and FC converters to the parallel connected multi-modular converter systems. Two multi-modular systems (i.e., NPC based and FC based) are compared with FF-SPWM and higher switching frequency SPWM control methods. Simulation results for the multi-modular system based on the three-phase five-level NPC and FC converter are presented.

Chapter seven describes the construction and operation of the laboratory prototypes as follows: one three-phase three-level converter and one single-phase five-level converter. The Digital Signal Processor (DSP) based controllers are described in detail. The design and construction of the control boards, the software development methodology as well as experimental results are included.

Finally, chapter eight summarises and concludes the work of this project and gives an outlook for future work.

1.7 Thesis Contributions

The contributions of the thesis are directly linked to the thesis objectives. Specifically, the originality of this thesis can be supported by the following points.

- The influence of different control methods on the switching losses of the NPC converter is investigated and some factors associated with switching losses are found and reported. One important conclusion is that the switching losses are directly affected by the chosen control method, independently of the number of levels of the converter (Chapter 3).
- The FF-SPWM control scheme applied to the NPC converter is examined. Its feasibility range is confirmed (Chapter 3).
- A detailed analysis of the PS-MSPWM scheme is made and its suitability for the FC converter is explained. It is confirmed that the PS-MSPWM method has a self-balancing property when applied to the FC converter (Chapter 4).
- A closed-loop control method is proposed to solve the voltage unbalancing problem in the five-level FC converter. This closed-loop control consists of PI controllers and a novel balancing control algorithm based on the PS-MSPWM method. Its validity has been verified by simulations (Chapter 5).
- A multi-modular system based on the three-phase five-level FC converter is examined and compared with the NPC converter based multi-modular system. Control schemes applied on these systems are investigated (Chapter 6).
- DSP based controllers for the three-level and five-level FC converters are designed and tested experimentally (Chapter 7).

1.8 Thesis Publications

Publications at international conference proceedings have been generated from this manuscript and the chronological list is as follows.

1. C. Feng and V.G. Agelidis, "A DSP-Based Controller Design for Multilevel Flying Capacitor Converters," *IEEE 19th Annual Applied Power Electronics Conference and Exposition (APEC 2004)*, Anaheim, California, USA, February 22-26, 2004, pp. 1740-1744. (Chapter 7).
2. C. Feng, V.G. Agelidis, and J. Liang, "Multimodular Systems Based on Multilevel Flying Capacitor Converters," *IEEE International Conference on Power Electronics and Drive Systems (PEDS 2003),* Singapore, November 17-20, 2003, pp. 386-391. (Chapter 6).
3. C. Feng, J. Liang, and V.G. Agelidis, "A Novel Voltage Balancing Control Method For Flying Capacitor Multilevel Converters," *29th Annual Conference of the IEEE Industrial Electronics Society (IECON 2003),* Roanoke, Virginia, USA, November 2-6, 2003, pp. 1179-1184. (Chapter 5).
4. C. Feng and V.G. Agelidis, "PWM Control Methods for Five-level Flying Capacitor Multilevel Converters", *7th International Conference on Modeling and Simulation of Electric Machines, Converters and Systems (ELECTRIMACS 2002),* Montreal, Canada, August 18-21, 2002, CD Proceedings. (Chapter 4).
5. C. Feng and V.G. Agelidis, "On the Comparison of Fundamental and High Frequency Carrier-Based PWM Techniques for Multilevel NPC Inverters", *IEEE 33rd Annual Power Electronics Specialists Conference (PESC 2002) Proceedings,* Cairns, Australia, June 23-27, 2002, Vol. 2, pp. 520-525. (Chapter 3).

One further paper has been published at a national conference:

1. C. Feng and V.G. Agelidis, "Multimodular System Based on Multilevel Neutral-Point-Clamped Converters," *Postgraduate Research Conference in Electronics, Photonics, Communications & Networks, and Computing Science (PREP 2004)* sponsored by IEEE, EPSRC, IEE and Institute of Physics, Hertfordshire, UK, April 5-7, 2004. (Chapter 6).

Chapter 2: Multilevel Converter Topologies and Control Methods

2.1 Introduction

Multilevel converter technology using fully controlled semiconductor switches such as IGBTs for medium power and Gate Turn-Off Thyristors (GTOs) for high power applications has been attracting a great deal of research interest. The general idea behind multilevel converter technology is to create a sinusoidal voltage from several levels of DC voltages, typically obtained from capacitor voltage sources. As the number of voltage levels increases, the output waveform can be formed by more steps, producing a staircase wave which approaches the sinusoidal wave.

Fig. 2.1 shows a schematic diagram of an inverter phase leg with different number of levels. Here the action of the power semiconductors is represented by an ideal switch with several positions. For an *m* level converter, its output can be connected to *m* different levels from m-1 voltage sources as illustrated in Fig. 2.1(c). Fig. 2.1(a) shows the diagram of a conventional two-level inverter. Fig. 2.1(b) shows the three-level circuit which generates an output voltage with three values (levels) with respect to the negative terminal of the DC bus.

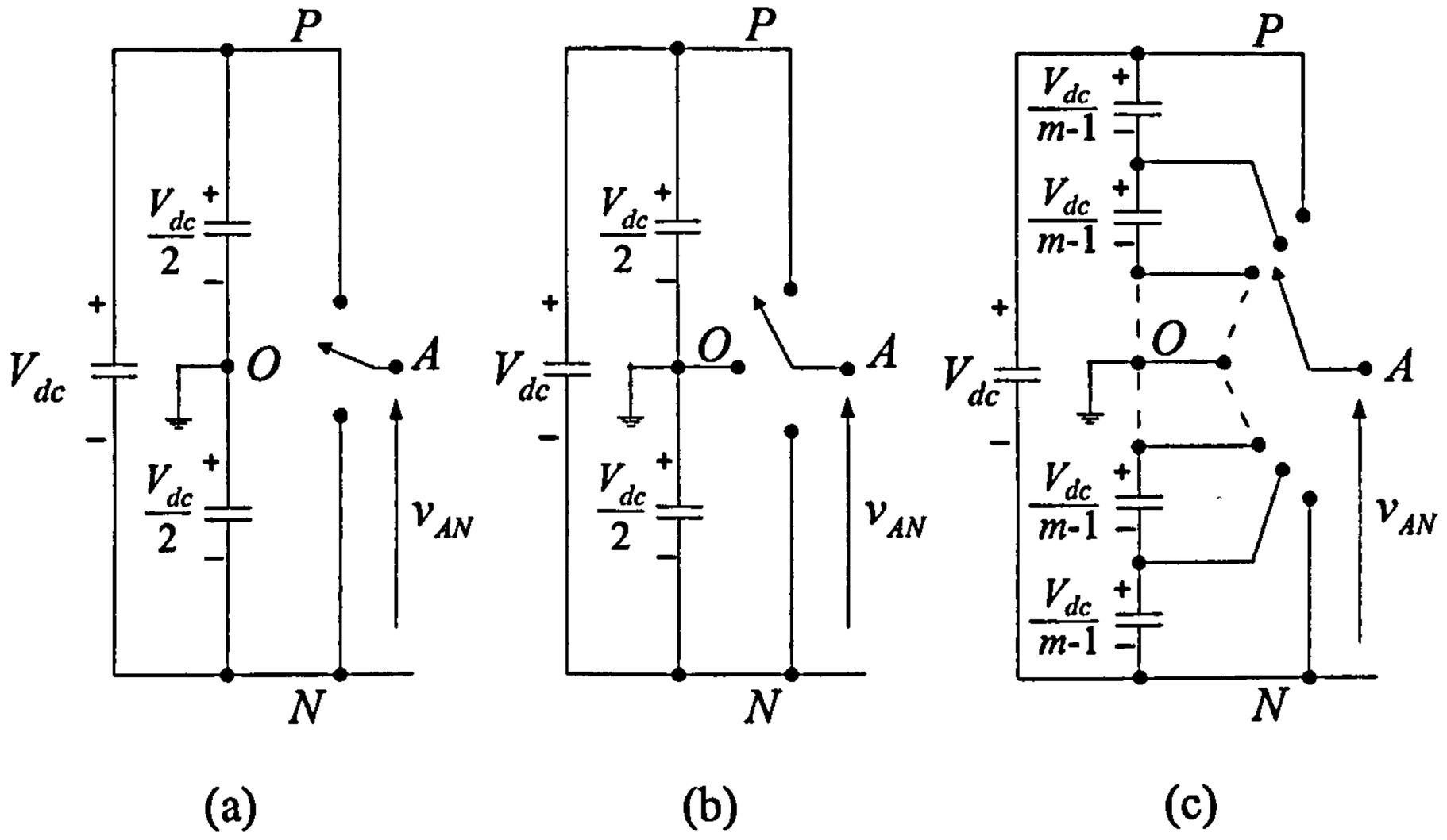


Fig. 2.1: One phase leg of an inverter with: (a) two-level; (b) three-level; (c) *m*-level.

Multilevel converters have different configurations that are illustrated in Fig. 2.2. They can also be grouped into categories according to the modulation methods employed, shown in Fig. 2.3.

In the following sections, three types of multilevel converters including their structures, features and applications as well as the switching strategies will be described in detail.

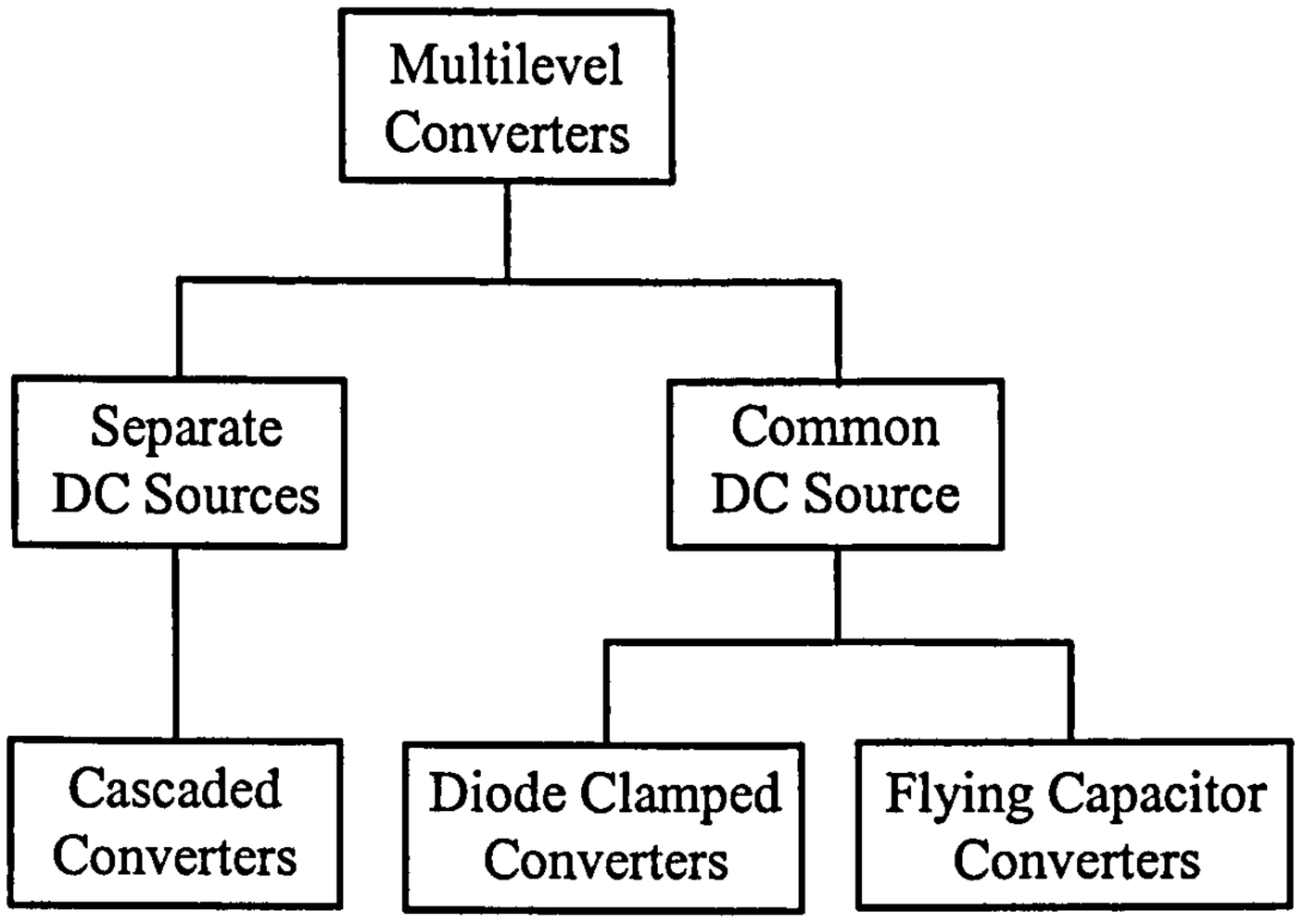


Fig. 2.2: Types of multilevel converters.

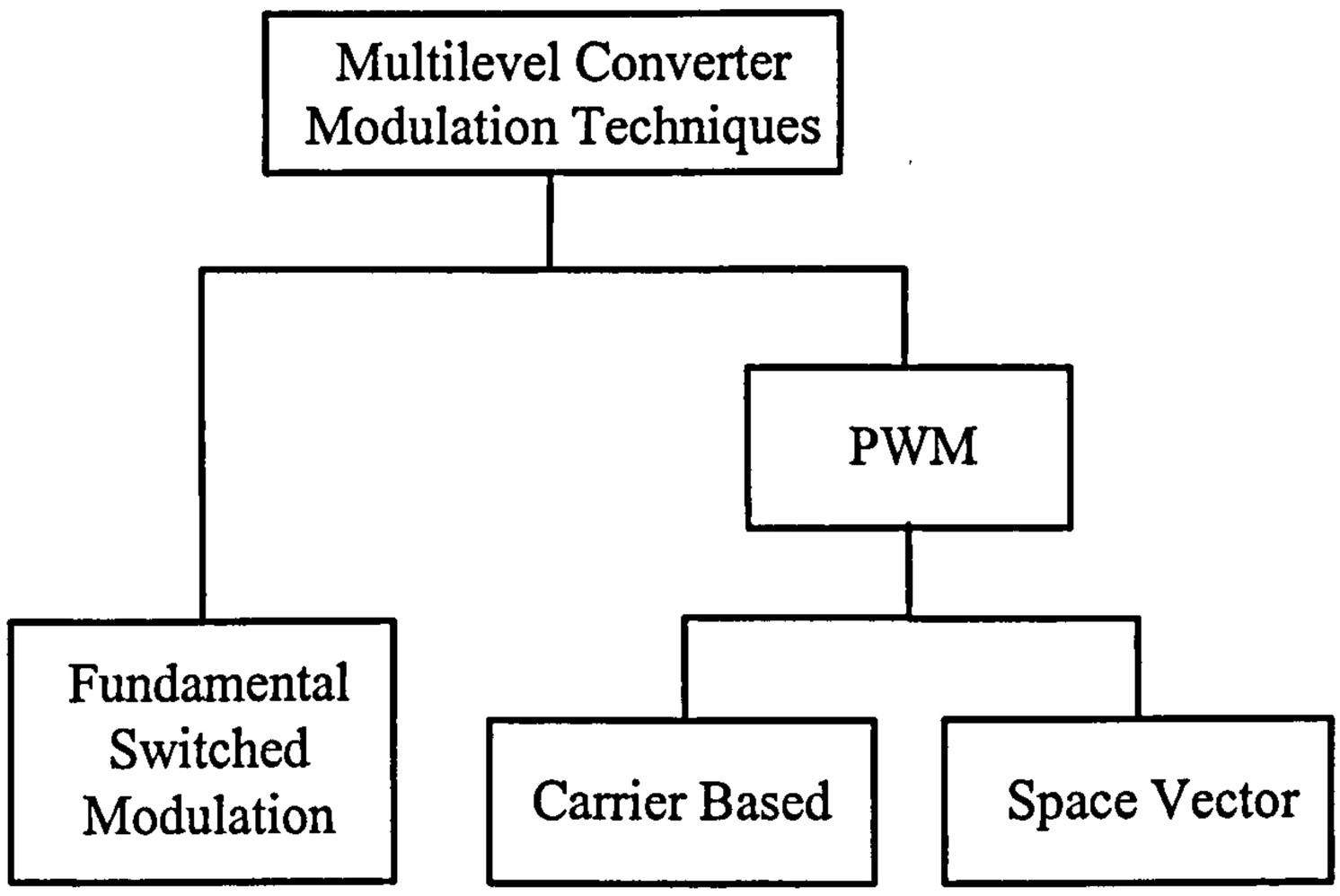


Fig. 2.3: Classification of multilevel modulation techniques.

2.2 Multilevel Converter Topologies

Multilevel inverters can generate more than two levels of the phase output voltage waveforms, which are achieved by virtue of their structures. There are three major multilevel topologies: Cascaded inverters with separate DC voltage sources, NPC inverters, and FC inverters.

2.2.1 Cascaded Converters with Separate Voltage Sources

The basic structure of this inverter is made up of multiple units connected in series in the AC terminal voltages. Each unit is actually a single-phase full-bridge inverter. Fig. 2.4 shows a nine-level cascaded inverter with four units. The phase output voltage is the sum of four inverter outputs, that is, $v_{AO} = v_{Con1a} + v_{Con2a} + v_{Con3a} + v_{Con4a}$. Here, each single-phase full-bridge inverter with unipolar PWM control scheme can generate three level outputs, $+V_{dc}$, 0, $-V_{dc}$.

It is noted that to comply with the definition of the NPC inverter and FC inverter, the level in a cascaded inverter with separate DC voltage sources is defined by $m=2s+1$, where m is the output phase voltage level, and s is the number of DC sources. For example, a nine-level cascaded inverter with separate voltage sources will have four separate DC voltage sources and four bridges. For a three-phase system, the output voltages of the cascaded inverters can be obtained in either Y(wye) or Δ(delta) configuration.

The great feature of this type of converters is its modularity, since the circuit is made up of identical units, which simplifies the manufacturing for commercial production. Another feature is that it has separate DC sources and can achieve any voltage potentially provided the unit isolation can be maintained.

Generally the advantages and disadvantages of the cascaded inverter with separate DC voltage sources, together with its applications can be summarised as follows:

Advantages:

- It can solve the size-and-weight problems of conventional transformer-based multi-pulse inverters and the high component-count problem of the multilevel diode-clamped and flying capacitor inverters. The reason being that the topology requires the lowest number of components among all multilevel converters to achieve the same number of voltage levels. Table 2.1 shows a comparison of the power components needed per phase leg for all the topologies. This comparison is based on the assumption that all devices have the same voltage ratings, and that the cascaded inverter uses a full-

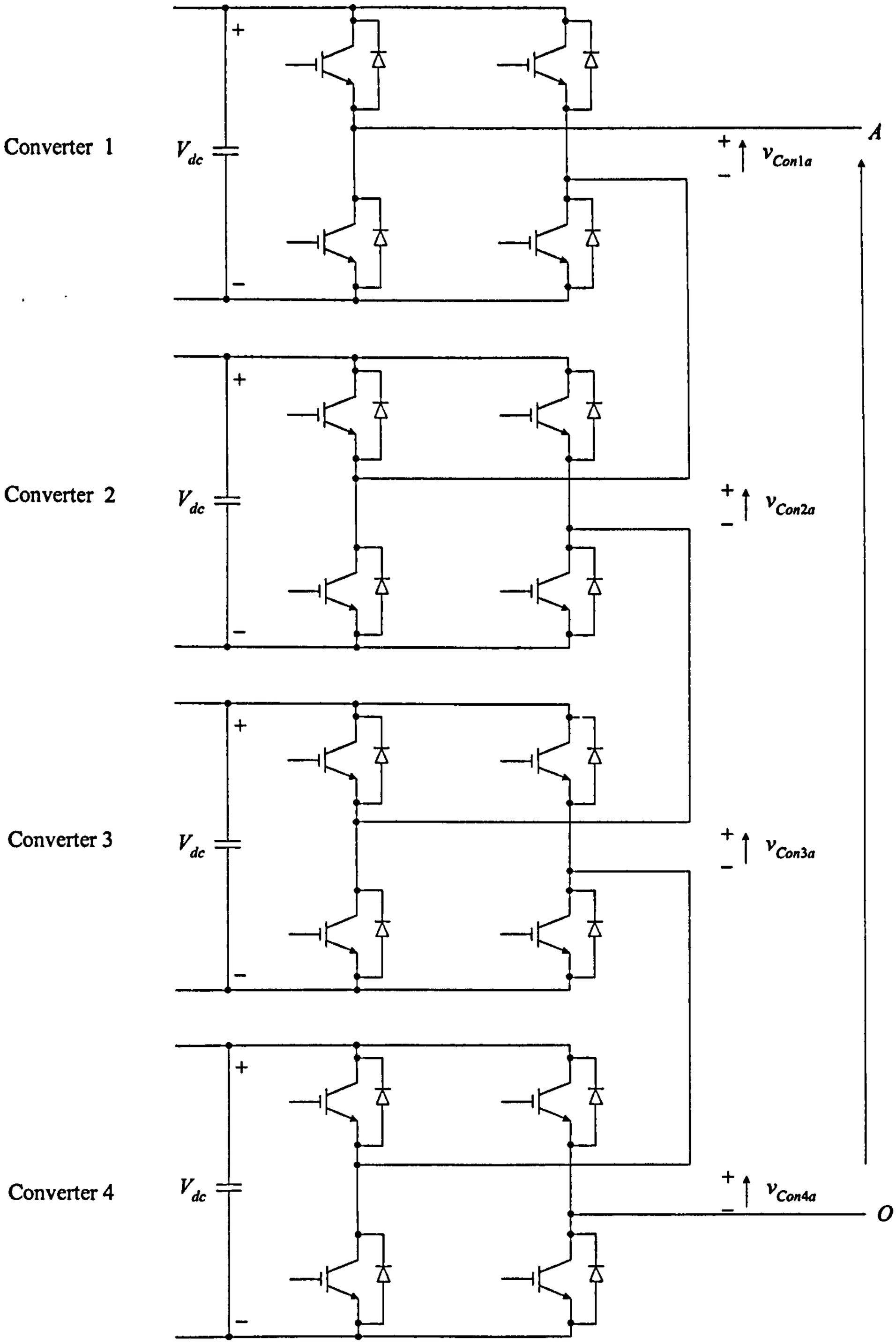


Fig. 2.4: A nine-level cascaded inverter with separate DC voltage sources.

bridge in each level as compared to the half-bridge version used in the other two types.

- The structure of separate DC sources is well suited for various renewable energy sources such as fuel cells, and photovoltaics.
- Modularised circuit layout and packaging is possible and much easier to be implemented because of the simplicity of the power structure and lower component count.

Disadvantages:

- Transformer with multiple secondary windings [22] is usually employed in practical applications such as the motor drive industry to obtain the isolated supplies. Transformers bring about some problems as mentioned before.
- For real power conversion, separate DC sources are necessary, and thus limiting its applications.
- For reactive power conversion, it has the same problem as that of the conventional two-level converter. The capacitor bank needs to be large to avoid excessive voltage fluctuation.

The modular nature of this type of inverter has received much interest from motor drive manufacturers in recent years. It is currently in commercial production and a transformer is used to provide the multiple supplies to the cells [22]. With sufficient isolation between the cells, the final output voltage can be taken far beyond any of the conventional techniques, which has promoted interest in its use for power factor correction in HV grid system [6] and utility applications [59]. Here the problems of obtaining the isolated supply become less significant since no real power transfer occurs. The separate DC sources nature makes it suitable for space and satellite AC generation systems, where the isolated supplies can be obtained naturally from the solar cells [60]. Other cases include AC rectification for electric trains [61].

Table 2.1: Comparison of power component requirements per phase leg among the three multilevel voltage source converters (m-level)

Converter type	NPC	FC	Cascaded
Main switches	$(m-1)\times 2$	$(m-1)\times 2$	$(m-1)\times 2$
Antiparallel diodes	$(m-1)\times 2$	$(m-1)\times 2$	$(m-1)\times 2$
Clamping diodes	$(m-1)\times(m-2)$	0	0
DC bus capacitors	$(m-1)$	$(m-1)$	$(m-1)/2$
Balancing capacitors	0	$(m-1)\times(m-2)/2$	0

2.2.2 Neutral-Point-Clamped (NPC) Converters

An m level diode-clamped converter typically consists of m-1 capacitors on the DC bus. Fig. 2.5 shows a single-phase half bridge five-level NPC inverter in which the DC bus consists of four capacitors. For a DC bus voltage V_{dc}, the voltage across each capacitor is $V_{dc}/4$, and each device voltage stress will be limited to one capacitor voltage level through the clamping diodes.

To explain how the staircase voltage is synthesised, let us take a five-level inverter shown in Fig. 2.4 as an example. The negative DC rail N is considered as the output phase voltage reference point. There are five switching combinations to synthesise a five level voltage from A to N. Table 2.2 lists the voltage levels and the corresponding switching states. (Here, 1 stands for switch being on, whereas, 0 for switch being off). There exist four complementary switch pairs in each phase. They are (S_{a1}, S_{a5}), (S_{a2}, S_{a6}), (S_{a3}, S_{a7}), (S_{a4}, S_{a8}). The complementary switch pair is defined such that turning on one of the pair switches will exclude the other from being turned on.

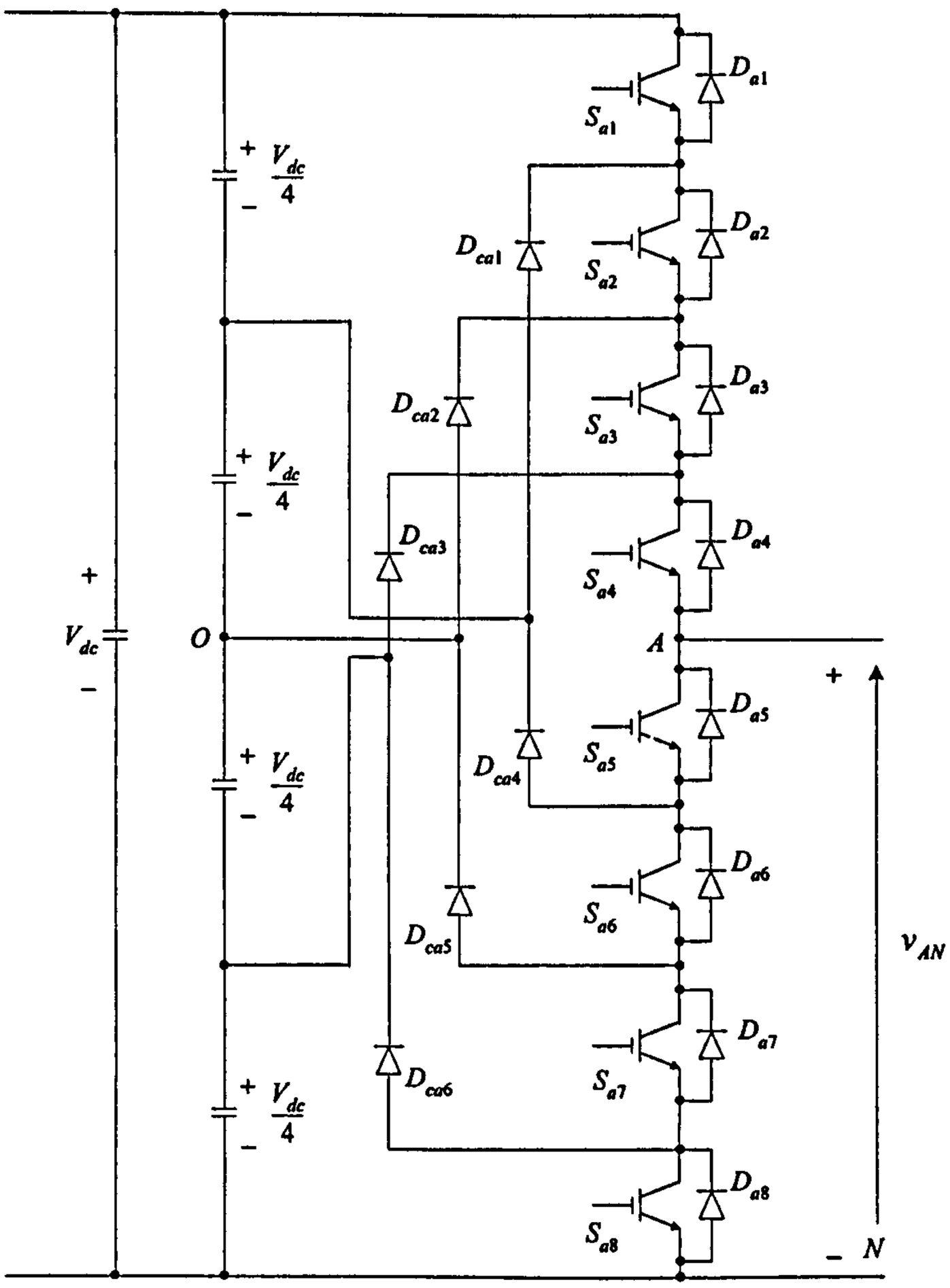


Fig. 2.5: A single-phase half bridge five-level NPC inverter.

Table 2.2: Five-level single-phase NPC inverter voltage levels and switch state

Output	Switch State							
V_{AN}	S_{a1}	S_{a2}	S_{a3}	S_{a4}	S_{a5}	S_{a6}	S_{a7}	S_{a8}
V_{dc}	1	1	1	1	0	0	0	0
$3V_{dc}/4$	0	1	1	1	1	0	0	0
$V_{dc}/2$	0	0	1	1	1	1	0	0
$V_{dc}/4$	0	0	0	1	1	1	1	0
0	0	0	0	0	1	1	1	1

For a single-phase full-bridge five-level NPC inverter, the phase voltage V_{BN} of another leg B is created in the same way. Then the output voltage $V_{AB} = V_{AN} - V_{BN}$ waveform can take nine-levels. Generally speaking, an m-level converter has an m-level output phase voltage and a ($2m$-1)-level line-to-line output voltage.

This type of converters have three features as follows [59]:

- For the clamping diodes, a high voltage rating is required. Although each active switching device is only required to block a voltage level of $V_{dc}/(m\text{-}1)$, the clamping diodes need to have different voltage ratings for reverse voltage blocking, for example, some of the interconnection diodes have to block voltage up to $(m\text{-}2)V_{dc}/(m\text{-}1)$.
- Unequal device rating: From Table 2.2, it can be seen that switch S_{a1} conducts only during $V_{AN}=V_{dc}$ while switch S_{a4} conducts over the entire cycle except during the $V_{AN}=0$. Such an unequal conduction duty requires different current ratings for switching devices.
- Capacitor voltage unbalance: In most applications, the power converter needs to transfer real power from AC to DC (rectifier operation) or DC to AC (inverter operation). When operating at unity power factor, the charging time for rectifier operation (or discharging time for inverter operation) for each capacitor is different, resulting in unbalanced capacitor voltages between the different levels. However, when operating at zero power factor, the capacitor voltages can be balanced by equal charge and discharge in one half cycle. This indicates that the converter can theoretically transfer pure reactive power without the voltage unbalance problem.

In summary, the advantages and disadvantages of the NPC inverter are as follows [59]:

Advantages:

- Reactive power flow can be controlled.

- The control method is simple for a back-to-back intertie system.

Disadvantages:

- Large numbers of clamping diodes are required when the number of levels is high. These clamping diodes not only raise cost but also cause packaging problems and exhibit parasitic inductances, thus the number of levels for a multilevel NPC inverter may be limited to seven or nine in practice.
- If the inverter runs under PWM control, the diode reverse recovery of these clamping diodes becomes the major design challenge in high power high voltage applications.
- It is difficult to do real power flow control for the individual converter.

This circuit has seen more interest than any other topology for multilevel applications since 1980. Most commercial products are based on the three-level circuit. Some research work regarding the five-level circuit has also been reported [6], [7].

2.2.3 Flying Capacitor Converters

Fig. 2.6 illustrates the fundamental building block of a single-phase half-bridge flying capacitor based five-level inverter. For a full-bridge, each phase leg has an identical structure. Assuming that each of the capacitors has the same voltage ratings as that of each of main switches, the number of capacitors connected in series indicates the voltage level between the clamping points. The capacitors connected to phase leg *A* are independent of those of phase leg *B*. Both phase legs share the main DC bus capacitor. For an *m*-level FC converter, a total of $(m\text{-}1)\times(m\text{-}2)/2$ auxiliary capacitors per phase leg are required in addition to $(m\text{-}1)$ main DC bus capacitors, with the assumption that all capacitors have the same voltage rating. However, an *m*-level NPC converter only requires $(m\text{-}1)$ capacitors.

The features of this type of the converter can be summarised as follows [59]:

- The voltage synthesis in a FC inverter has more flexibility than that in a NPC inverter. Taking a five-level FC as an example, Table 2.3 lists one of the possible switching combinations. Table 2.4 lists all possible combinations.
- There also exist complementary switch pairs that, however, are different from those in the NPC inverter. For the circuit shown in Fig. 2.6, the four complementary switch pairs are (S_{a1}, S_{a8}), (S_{a2}, S_{a7}), (S_{a3}, S_{a6}) and (S_{a4}, S_{a5}) respectively.
- Both real and reactive power flow can be controlled, although with real power flow, the capacitor voltages are unbalanced. In order to balance the capacitor charge and discharge, two or more switch combinations for middle voltage levels ($3V_{dc}/4$, $V_{dc}/2$,

$V_{dc}/4$) in one or several fundamental cycles may be employed. Thus, by proper selection of switch combinations, the converter may be used in real power conversion. However, in this case, the selection of a switch combination becomes very complicated, and the switching frequency needs to be higher than the fundamental frequency.

- A large number of storage capacitors are required for this topology, causing packaging problems and increasing the size of the inverter.

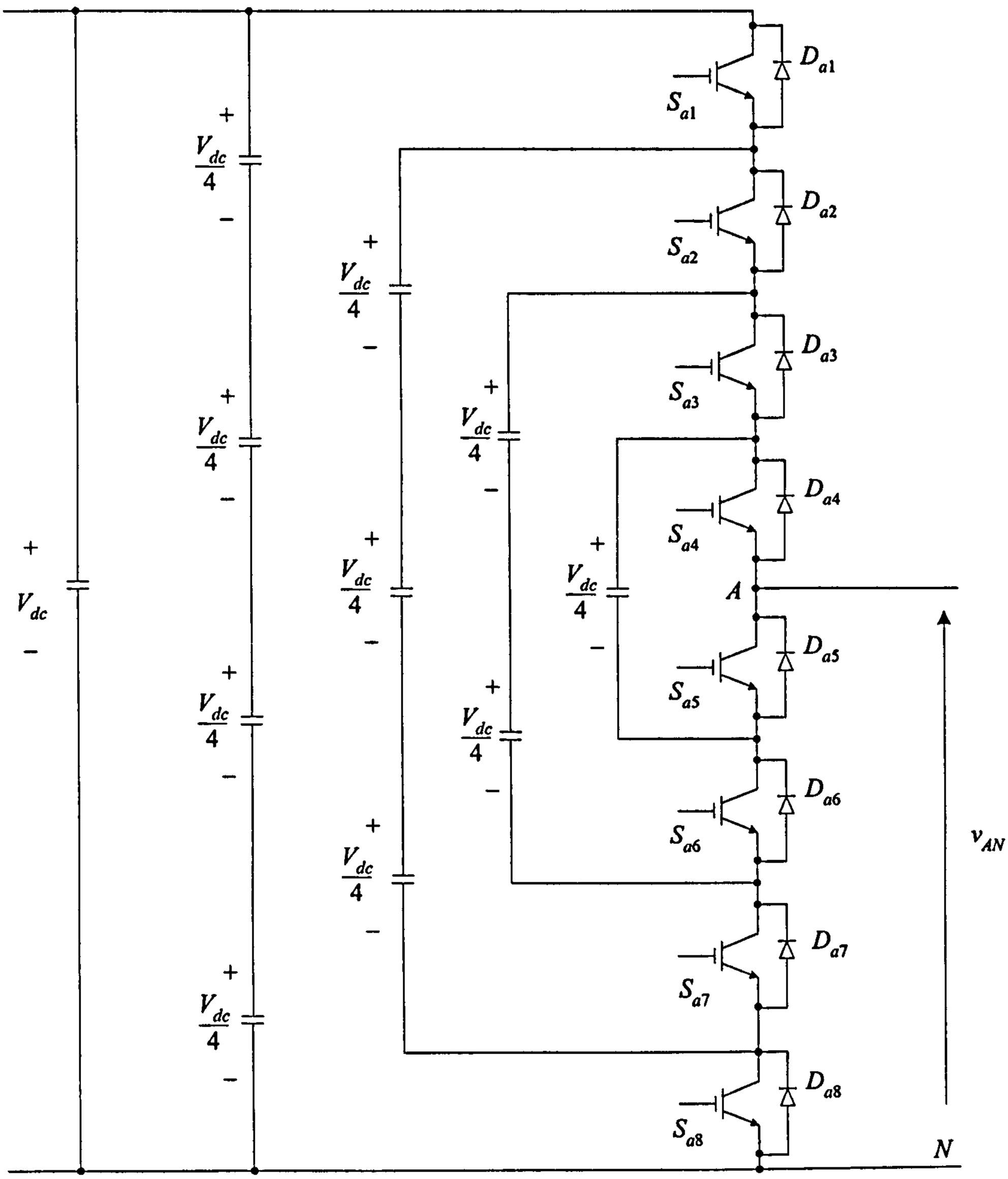


Fig. 2.6: A single-phase half-bridge flying capacitors based five-level inverter.

Table 2.3: One of a possible switching combinations of the five-level FC converter

Output V_{AN}	Switch State							
	S_{a1}	S_{a2}	S_{a3}	S_{a4}	S_{a5}	S_{a6}	S_{a7}	S_{a8}
V_{dc}	1	1	1	1	0	0	0	0
$3V_{dc}/4$	1	1	1	0	1	0	0	0
$V_{dc}/2$	1	1	0	0	1	1	0	0
$V_{dc}/4$	1	0	0	0	1	1	1	0
0	0	0	0	0	1	1	1	1

Table 2.4: Five-level FC converter voltage levels and their switch state

Output V_{AN}	Switch State							
	S_{a1}	S_{a2}	S_{a3}	S_{a4}	S_{a5}	S_{a6}	S_{a7}	S_{a8}
V_{dc}	1	1	1	1	0	0	0	0
$3V_{dc}/4$	1	1	1	0	1	0	0	0
	1	1	0	1	0	1	0	0
	1	0	1	1	0	0	1	0
	0	1	1	1	0	0	0	1
$V_{dc}/2$	1	1	0	0	1	1	0	0
	1	0	1	0	1	0	1	0
	0	1	1	0	1	0	0	1
	1	0	0	1	0	1	1	0
	0	1	0	1	0	1	0	1
	0	0	1	1	0	0	1	1
$V_{dc}/4$	1	0	0	0	1	1	1	0
	0	1	0	0	1	1	0	1
	0	0	1	0	1	0	1	1
	0	0	0	1	0	1	1	1
0	0	0	0	0	1	1	1	1

From Table 2.3, it can be seen that one of the switching combinations in the FC converter is the same as that of the NPC converter, which implies that the switching strategies suitable for the NPC converter can also suit the FC converter. In other words, NPC and FC topologies have the same output characteristics under the same switching strategy. The FC also has unequal device duty problems when the above switch combination is chosen. From Table 2.4, it can be concluded that FC has more switching redundancy than NPC topology. For example, there are four switching combinations for voltage level $V_{dc}/4$ *a*nd $3V_{dc}/4$, and six switching combinations for $V_{dc}/2$.

In summary, the advantages and disadvantages of the FC inverter are as follows [59]:

Advantages:

- The large amount of flying capacitors provides extra ride through capabilities during power outages.
- The switch combination redundancy provides the higher degrees of freedom for balancing different voltage levels.
- Both real and reactive power flow can be controlled, making it a possible candidate for HVDC power transmission.

Disadvantages:

- An excessive number of storage capacitors are required when the number of inverter levels is high. High-level systems are more difficult to package and more expensive due to the required bulky capacitors.
- The inverter control will be very complicated, and the switching frequency and switching losses will be high for real power transmission.

Little research has been done on this topology, with most interested parties taking the view that the control of the capacitor voltages through the switching strategy is too complex to be achieved on-line without excessive computational power [5]. It has been proposed by [64] that the switching pattern can be predetermined whilst still maintaining the correct voltage on the capacitors. After originally being discussed for motor drive applications with a simple RL load, a more recent publication has seen a change of application to sinusoidal rectification [65]. This slightly simplifies the control since the frequency becomes fixed, and the capacitors will only have to supply current for a predetermined interval before the direction reverses.

2.3 Switching Strategies for Multilevel Converters

2.3.1 Fundamental Switched Modulation

Fundamental switched modulation offers the simplest pattern, similar to the quasi-square wave pattern from the early conventional inverters. These methods that work with low switching frequencies generally perform one or two commutations of the power semiconductors during one cycle of the output voltages, generating a staircase waveform.

The feature of this modulation method is that the harmonics of the output are linked to the fundamental and large low order harmonics (significantly 5^{th}, 7^{th} and 11^{th}, 13^{th}, the triple harmonics cancel between phases) are produced. Representatives of this family are the multilevel selective harmonic elimination [66] [67], and the space-vector control [68]. During early work on multilevel converters, when the switching speed of the devices was limited, this was a commonly used technique.

2.3.2 Harmonic Switched Modulation

With the development of the power semiconductor switches technology, the high-speed switches appeared and thus making the use of the PWM a standard technique. Usually, a very popular method in industrial applications is the classic carrier-based SPWM. This method can be divided into basic SPWM methods applied to conventional converters and MSPWM methods.

SPWM Control Methods

In inverter circuits, the inverter output is expected to be sinusoidal with magnitude and frequency controllable. To reach this goal, the so-called SPWM control method is employed [87]. In this scheme, the PWM signals are generated from the comparison of a fundamental sinusoidal waveform and a high frequency carrier waveform, as shown in Fig. 2.7. The frequency of the triangular waveform establishes the inverter switching frequency and is generally kept constant along with its amplitude.

The amplitude modulation ratio m_a is defined as the ratio of $\hat{A}_o$, the amplitude of the modulating signal and $\hat{A}_c$, the amplitude of the carrier (triangular) signal.

$$m_a = \frac{\hat{A}_o}{\hat{A}_c} \tag{2-1}$$

The SPWM scheme has the following important basic features: (when $m_a \leq 1$)

- The amplitude of the fundamental frequency component is proportional to the amplitude modulation ratio m_a.

  For a single-phase half-bridge inverter, the peak amplitude of the fundamental frequency component $\hat{V}_{AO1}$ is expressed by:

$$\hat{V}_{AO1} = m_a \cdot \frac{V_{dc}}{2} \tag{2-2}$$

  where V_{dc} is the DC voltage. For a single-phase full-bridge inverter, the line-to-line voltage output peak amplitude of the fundamental frequency component $\hat{V}_{AB1}$ is expressed by:

$$\hat{V}_{AB1} = m_a \cdot V_{dc} \tag{2-3}$$

  For a three-phase two-level conventional inverter, the line-to-line voltage output peak amplitude of the fundamental frequency component $\hat{V}_{AB1}$ is expressed by:

$$\hat{V}_{AB1} = m_a \cdot \frac{\sqrt{3}}{2} V_{dc} \tag{2-4}$$

- The harmonics in the inverter output voltage waveform appear as sidebands, centred around the switching frequency f_c and its multiples, that is, around harmonics f_c, $2f_c$, $3f_c$ and so on. Theoretically, the frequencies at which voltage harmonics occur can be indicated as

$$f_h = j \cdot f_c \pm k \cdot f_1 \tag{2-5}$$

  where f_1 is the fundamental frequency, j and k are integers. When j is odd, k is even. When j is even, k is odd.

For a single-phase half-bridge inverter shown in Fig. 1.1, a so-called bipolar SPWM scheme can be employed, which is illustrated in Fig. 2.7 [49].

For a single-phase full-bridge inverter shown in Fig. 1.2, two types of SPWM schemes can be chosen. One is SPWM with bipolar voltage switching in which the diagonally opposite switches S_1 and S_4 switch on and off simultaneously (i.e., they are regarded as a switch), S_2 and S_3 are regarded as another complementary switch pair of S_1 and S_4 switches. The output voltage changes between $+V_{dc}$ and $-V_{dc}$, the waveform is similar to the output voltage in half-bridge inverter, as shown in Fig. 2.8 [49]. Another is SPWM with unipolar voltage switching. With this type of scheme, the switches in the two legs are not switched simultaneously. The legs A and B are controlled separately by comparing one triangular signal with two sinusoidal control signals respectively as shown in Fig. 2.9 [49]. The

output voltage changes between $+V_{dc}$ and zero or zero and $-V_{dc}$. This scheme has the advantage of effectively doubling the switching frequency as far as the output harmonics are concerned, compared to the bipolar voltage-switching scheme. The harmonics can be written as:

$$f_h = j \cdot (2 \cdot f_c) \pm k \cdot f_1 \tag{2-6}$$

where f_1 is the fundamental frequency, j and k are integers. When j is odd, k is even. When j is even, k is odd.

Also, the voltage jumps in the output voltage at each switching are reduced to V_{dc}, as compared to $2V_{dc}$ in bipolar voltage switching scheme.

For a three-phase inverter shown in Fig. 1.3, to obtain balanced three-phase output voltages, the same triangular voltage waveform is compared with three sinusoidal control voltages that are 120° out of phase, as shown in Fig. 2.10 [49].

Multi-Carrier SPWM Control Methods

MSPWM methods are derived from the basic SPWM method only with multiple carriers forming a continuous set. The comparison of the sinusoidal modulation wave with the different triangular carriers determines the corresponding switches action. Basically, there are two MSPWM strategies. One is the CD-MSPWM method; another is the PS-MSPWM method. They will be dealt with in the following chapter (Section 3.3).

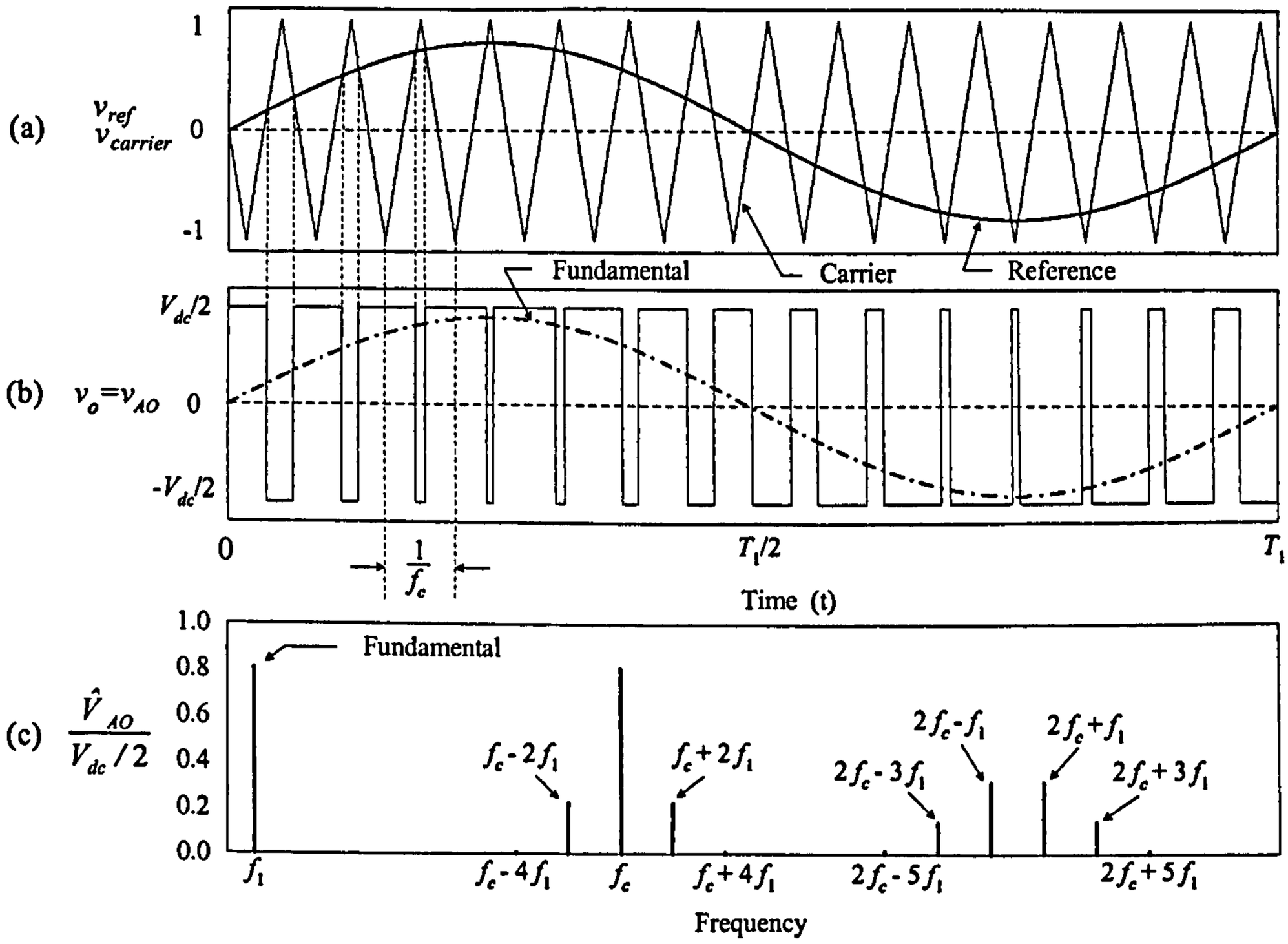


Fig. 2.7: Bipolar SPWM method applied to the single-phase half-bridge inverter. (a) Reference (sinusoidal) and carrier (triangular) signals (f_c=15f_1 and m_a=0.8). (b) Output voltage waveform v_{AO}. (c) Normalised harmonic amplitude of the voltage waveform v_{AO}.

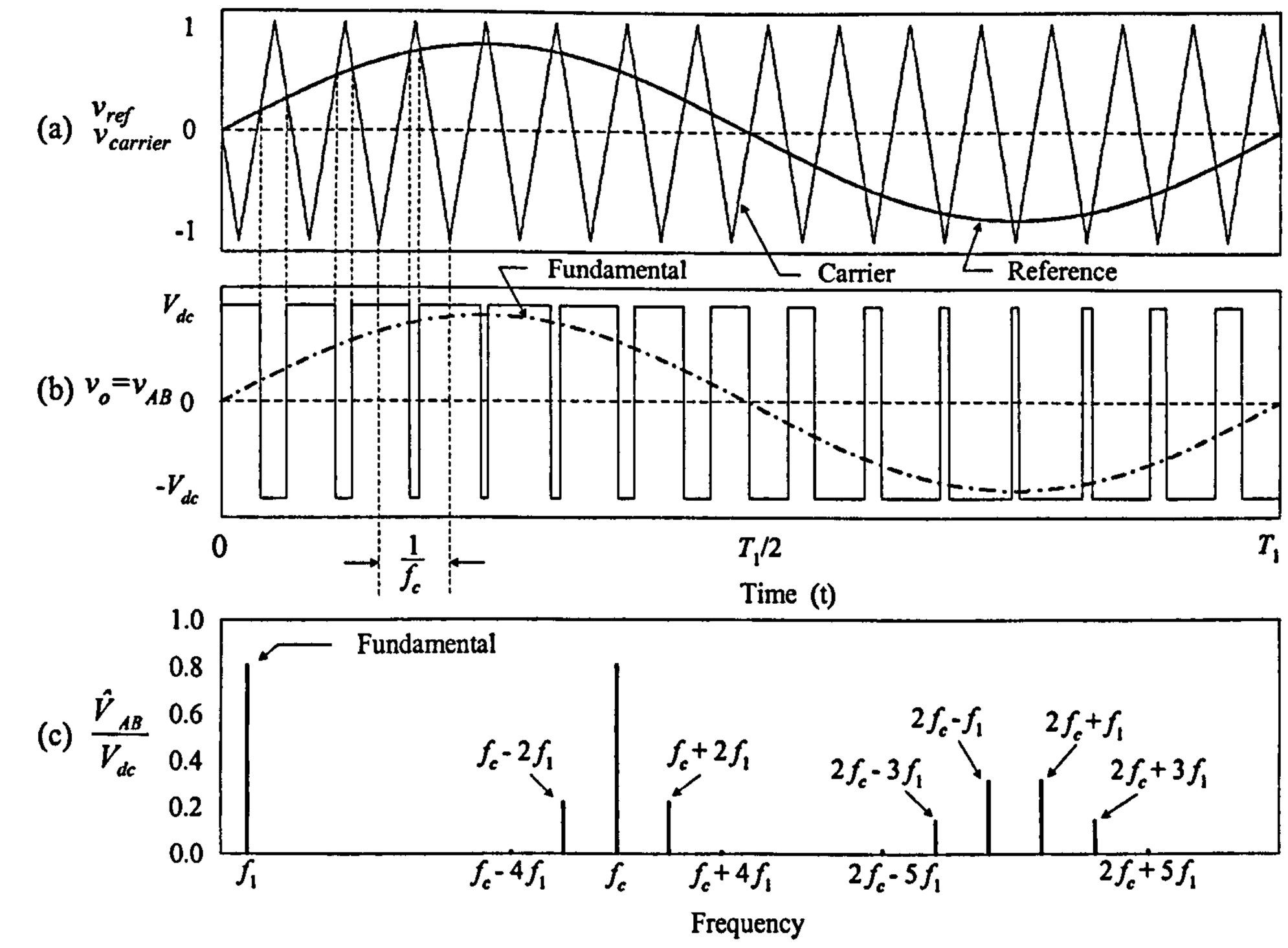


Fig. 2.8: Bipolar SPWM method for the single-phase full-bridge inverter. (a) Reference (sinusoidal) and carrier (triangular) signals (f_c=15f_1 and m_a=0.8). (b) Output voltage waveform v_{AB}. (c) Normalised harmonic amplitude of the voltage waveform v_{AB}.

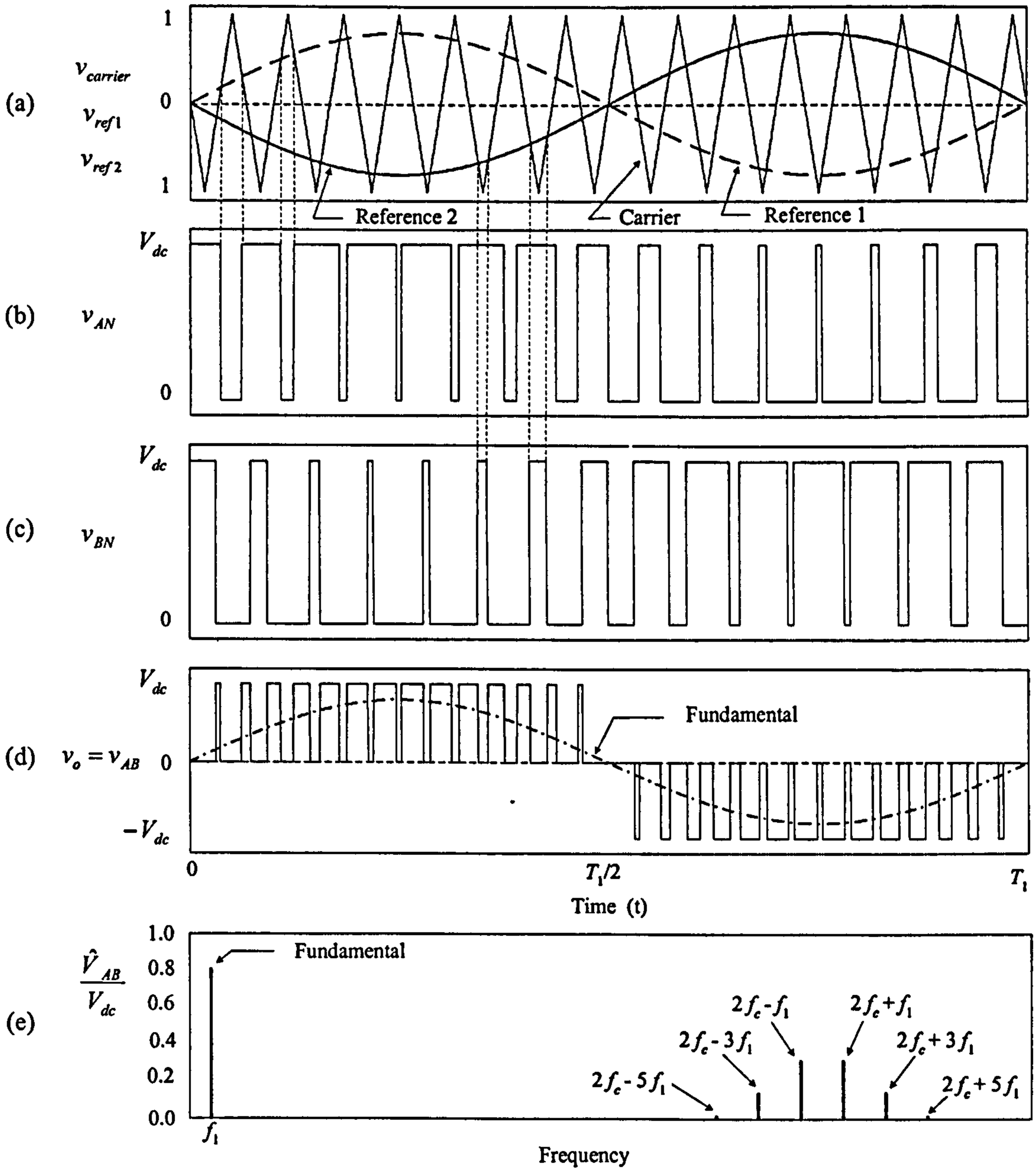


Fig. 2.9: Unipolar SPWM for the single-phase full-bridge inverter. (a) Two reference signals (sinusoidal) and one carrier (triangular) signal (f_c=15f_1 and m_a=0.8). (b) Output voltage waveform v_{AN}. (c) Output voltage waveform v_{BN}. (d) Output voltage waveform v_{AB}. (d) Normalised harmonic amplitude of the voltage waveform v_{AB}.

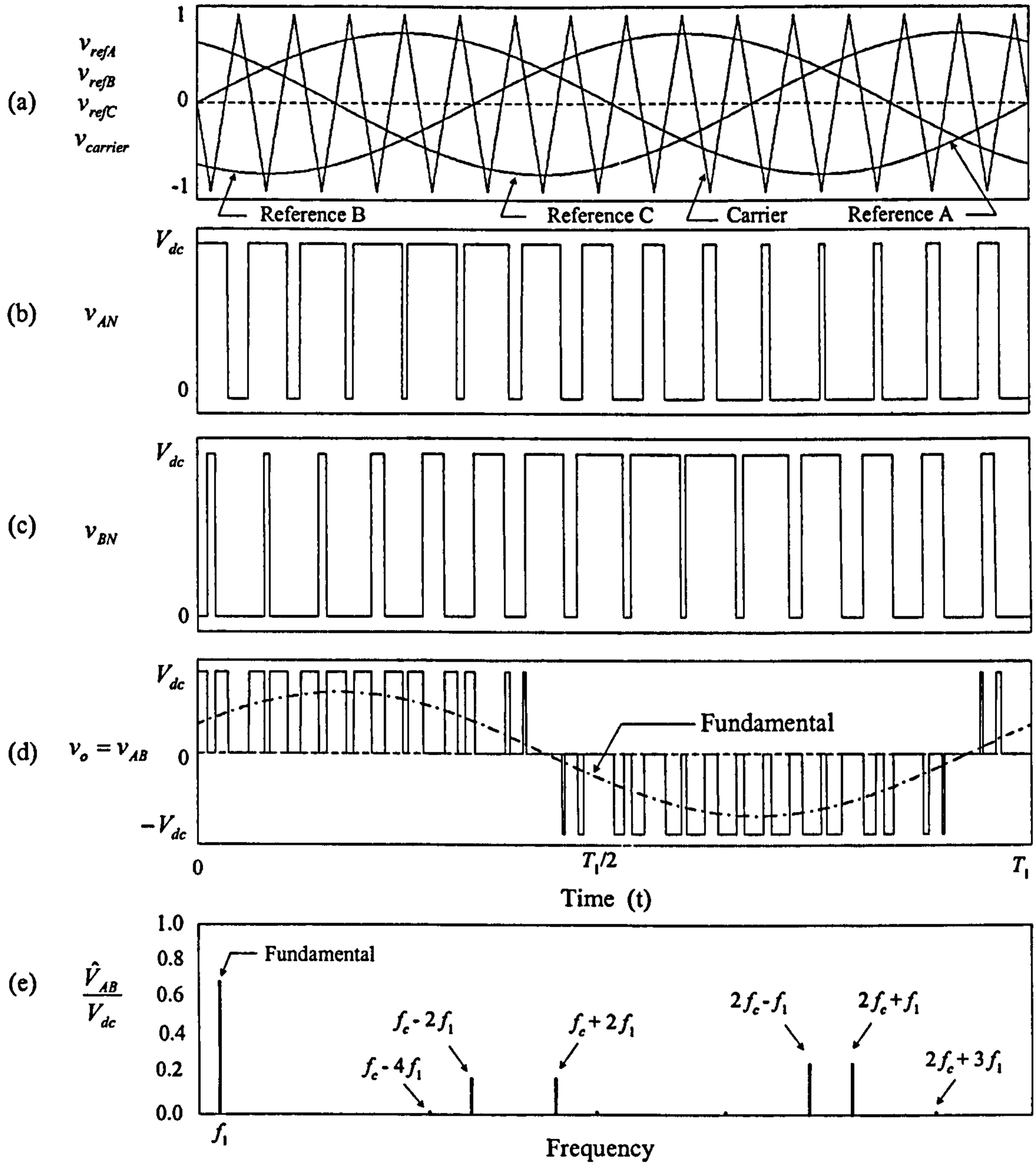


Fig. 2.10: Bipolar SPWM for the conventional two-level three-phase inverter. (a) Reference signals (sinusoidal) and carrier (triangular) signal (f_c=15f_1 and m_a=0.8). (b) Output voltage waveform v_{AN}. (c) Output voltage waveform v_{BN}. (d) Output voltage waveform v_{AB}. (d) Normalised harmonic amplitude of the voltage waveform v_{AB}.

2.3.3 Space Vector PWM

The SV-PWM technique refers to a special switching scheme for three-phase power converters. It has the following distinguished features: good utilisation of DC-link voltage, low current ripple, and relatively easy hardware implementation in a DSP. These features make it suitable for high-voltage high-power applications [69].

Fig. 2.11 shows space voltage vectors and switching patterns representative diagram for the traditional three-phase two-level converters. *P* and *N* represent the possible output phase terminal voltages of the inverter shown in Fig. 1.3, respectively, $+V_{dc}/2$ and $-V_{dc}/2$ if *O* is the ground reference. (*NNP*) denotes the S_4, S_6 and S_5 switches in Fig. 1.3 are on states and the other switches are off states. V^* is a desired reference output vector.

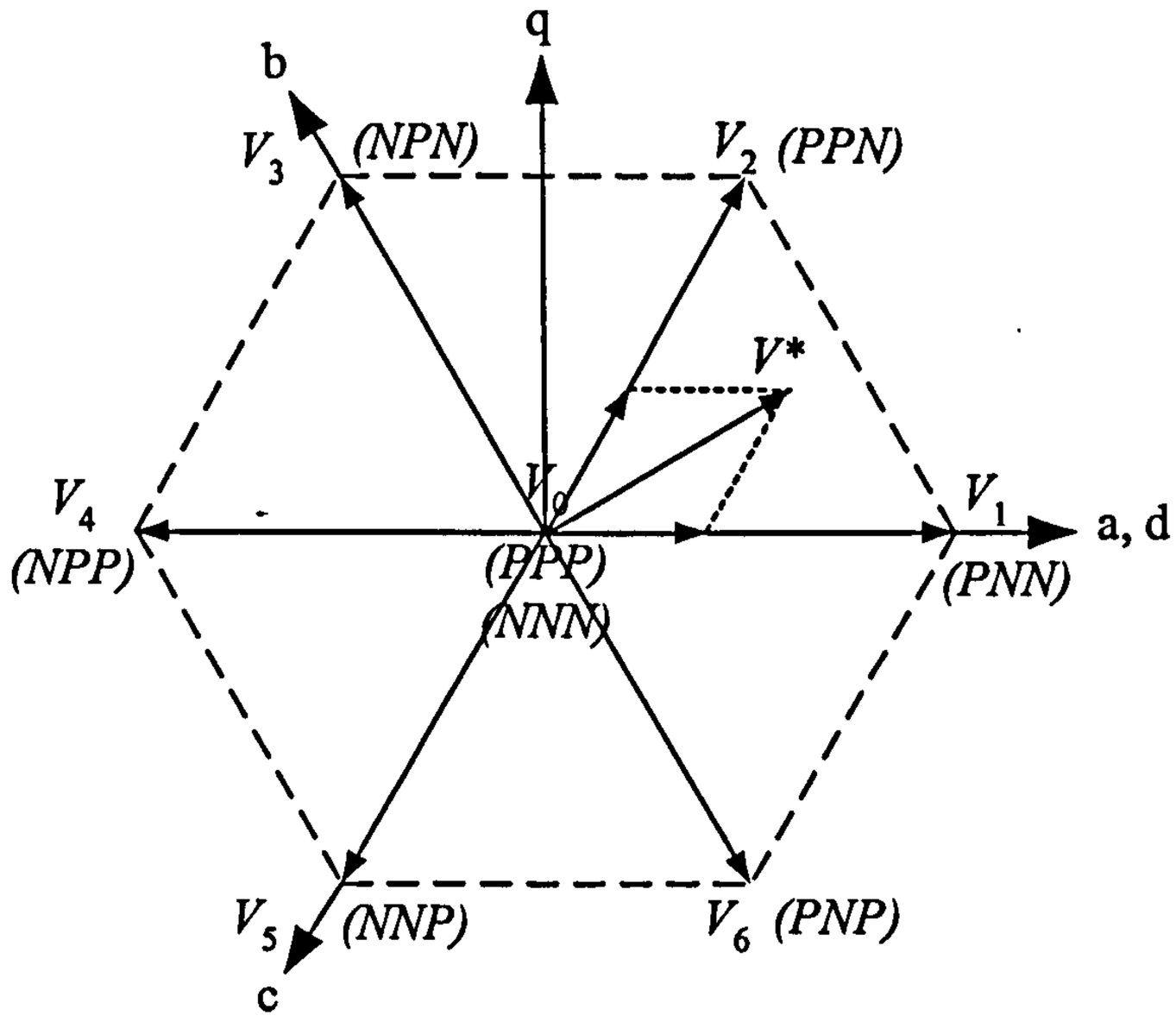


Fig. 2.11: Space voltage vectors and switching patterns representative diagram for three-phase two-level converters.

It can be seen from Fig. 2.11 that there are eight basic space vectors for two-level converters. The objective of the SV-PWM method is to approximate the desired reference voltage vector V^* by a combination of these basic space vectors. V^*, *a*t any given time, falls in one of the six sectors. Thus, for any PWM period, it can be approximated by the vector sum of two vector components lying on the two adjacent basic vectors. For example, when the reference vector V^* falls into the region shown in Fig. 2.11, it can be synthesised by:

$$V^{*} = \frac{(V_1 t_1 + V_2 t_2 + V_0 t_0)}{T_{samp}} \tag{2-7}$$

$$T_{samp} = t_1 + t_2 + t_0 \tag{2-8}$$

where T_{samp} is the sampling time period, t_1, t_2 and t_0 are the corresponding dwell times of V_1, V_2 and V_0 in the period T_{samp}. The inclusion of zero vector V_0 helps to control the value of the reference generated.

The SV-PWM technique can be easily extended to all multilevel inverters [69]–[76]. Fig. 2.12 shows a space vectors representative diagram for the three-phase three-level inverters shown in Fig. 1.4. *P*, *O* and *N* represent the possible output phase terminal voltages of the inverter respectively, $+V_{dc}/2$, 0 and $-V_{dc}/2$ if *O* is the ground reference. The output of the three-level converter has 19 independent space vectors among 27 different vectors.

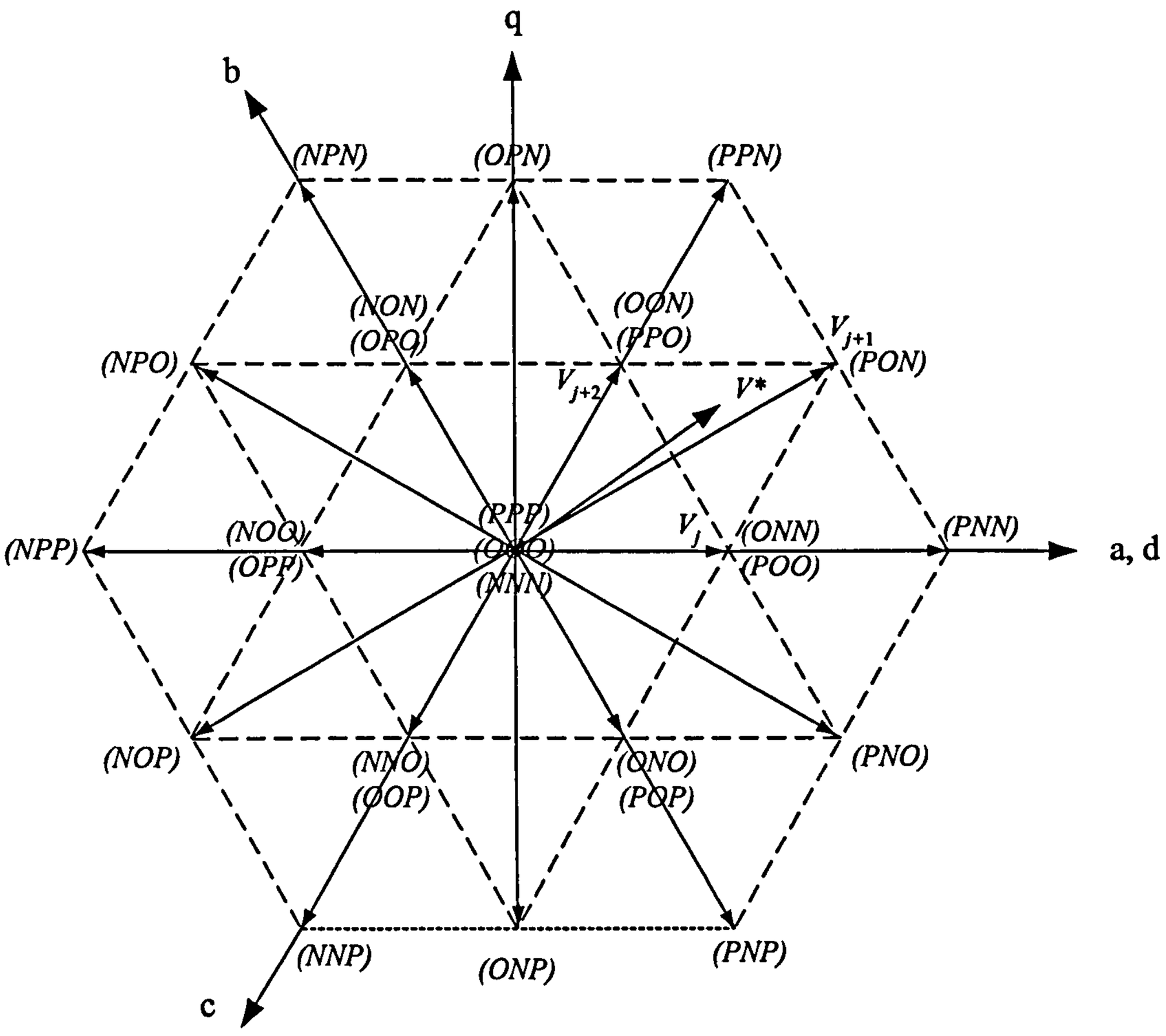


Fig. 2.12: Space voltage vectors and switching patterns representative diagram for three-phase three-level converters.

These vector diagrams are universal regardless of the type of multilevel inverter. In other words, Fig. 2.12 is valid for the three-level diode-clamped, capacitor-clamped, or cascaded inverter. The adjacent three vectors can synthesise a desired voltage vector V^* by

$$V^* = \frac{(V_j t_j + V_{j+1} t_{j+1} + V_{j+2} t_{j+2})}{T_{samp}} \tag{2-9}$$

Where, t_j, t_{j+1}, and t_{j+2} are the corresponding dwell times of V_j, V_{j+1} and V_{j+2} in the period T_{samp}.

The SV-PWM technique has become the standard control method for the conventional inverter with the microcontroller because it is simple to implement. However, as the number of levels increases, redundant switching states and the complexity of selecting switching states increase dramatically. It becomes very complicated and difficult to implement when three-levels are exceeded. Some researchers have used decomposition of the five level space-vector diagram into two three-level space-vector diagrams with a phase shift to minimize ripple and to simplify the control [72]. Additionally, a simple space-vector selection method was introduced without duty cycle computation of the adjacent three vectors [73].

2.4 Simulation Software

Computer simulations are commonly used in research to analyse the behaviour of circuits, which leads to improved understanding. In industry, they are used to shorten the overall design process, since it is usually easier to study the influence of a parameter on the system behaviour in simulation. They can be used to calculate the circuit waveforms, the dynamic and steady state performance of systems, and the voltage and current ratings of various components. In general, there are two basic types of simulators: circuit-oriented simulators and equation solvers. With the former, the user needs to supply the circuit topology and the component values. Simulators internally generate the circuit equations that are totally transparent to the user. The circuit-oriented simulators are much easier and therefore are more widely used than the equation solvers.

There are several general-purpose, circuit-oriented simulators such as SPICE, EMTDC, SABER and so on. The PSCAD/EMTDC software package has been employed in this research.

PSCAD is a collection of programs, providing a very flexible interface to electromagnetic transients simulation software. EMTDC is the library of power system

component models and procedures that constitute the simulation software provided with PSCAD. Together, these two software packages are referred to as "PSCAD/EMTDC".

The PSCAD/EMTDC software package has the following features:

- EMTDC is structured so that electric circuit parameters are easily addressed by the user during the course of a time domain simulation.
- Fourier analysis of output is sometimes desirable and MULTIPLOT is used in PSCAD to carry out this task.
- The user is able to build his/her own subroutines if models are not readily available.

It should be noted that the selection of the Time Step is very important in simulation. It must be chosen to be much smaller (at least order of two) than the shortest time constant of interest in the circuit.

2.5 Conclusions

This chapter gives an overview of multilevel Voltage Source Converter (VSC) topologies with their structure features, advantages and disadvantages as well as their applications. The review of switched modulation methods applied to multilevel converters is presented. The simulation software PSCAD/EMTDC used in the project is briefly introduced.

Three topologies introduced here are the main multilevel converter circuits which have received research and development interest from both academia and industry. Each one has its own particular advantages and disadvantages. No one is necessarily the best one for any application. Therefore, the choice of topology depends on the application. Cascaded converters with separate DC sources are favoured by the motor drive industry and for renewable energy conversion systems. They are used in medium voltage high power motor drives. NPC converters seem to have received more interest than the other two topologies since the 1980s. But most work on the NPC is focused on the three-level. The three-level NPC converter has been commercially available for many applications. The FC topology was the latest one to be introduced. The structure of the FC is similar to that of the NPC, generating a multilevel output waveform from different capacitor voltage sources, only with different clamping components. The FC uses the capacitor clamping, while the NPC uses the diode clamping.

Accompanying the topologies is a range of switching strategies which are derived from basic switching strategies used in conventional converters. These are the fundamental switched modulation, sub-harmonic PWM and space vector PWM modulation.

Fundamental switched modulation is still a useful and probably the best technique in the high power application because it minimises switching losses. Space vector PWM modulation has advantages such as increasing the linearity range of the output voltage, lower current ripple and easy hardware implementation on the DSP based controller. But this advantage is lost when the number of levels increases. Sub-harmonic PWM is widely used in industry because it is easy to implement for any levels. This type of PWM includes CD-MSPWM technique and PS-MSPWM technique.

It is expected that different switching strategies are suitable for different topologies and this will be explored in the forthcoming chapters. The switching strategies considered in this project are based on the sub-harmonic PWM modulation.

Chapter 3: Neutral-Point-Clamped Converters

3.1 Introduction

The NPC converter topology and the associated control methods are discussed in detail in this chapter. First, the mathematical modelling of the NPC converter is presented in Section 3.2. It includes two modes of operation, namely, the rectifier mode and the inverter one. The neutral-point voltage variation remains a challenging issue in NPC converters that needs to be addressed and therefore is also described. In Section 3.3 several Multi-carrier Sinusoidal Pulse-Width Modulation (MSPWM) control strategies are discussed. The importance of the semiconductor power losses especially in high-power applications is introduced. The effects of the different CD-SPWM techniques on the switching losses and the harmonic performance of the NPC converter are investigated and reported. The fundamental frequency SPWM method is proposed in Section 3.4 as a potential method to minimise the switching losses of the converter. This method is compared with high frequency MSPWM switching strategies in Section 3.5. Finally, a critical discussion on the challenges of this technology and conclusions are given in Section 3.6 and Section 3.7 respectively.

3.2 Modelling of the NPC Converter

Typically, an m level NPC converter consists of m-1 capacitors on the DC bus and produces a phase voltage with m levels. Fig. 1.4 shows a three-phase three-level NPC converter in which the DC bus consists of two capacitors. For a given value of the DC bus voltage V_{dc}, the voltage across each capacitor is $V_{dc}/2$, and each device voltage stress will be limited to one capacitor voltage level through the structure of the converter employing extra clamping diodes. Table 3.1 shows the NPC converter voltage levels and associated switching states for a three-level phase leg.

The modelling of the NPC converter is carried out mathematically in order to understand its basic principles of operation. Any switch-mode Voltage Source Converter (VSC) has a bi-directional power flow between the DC side and the AC side. The same applies for the NPC converter. Therefore, it has two modes of operation: rectifier (power flows from the AC side to the DC side) and inverter (power flows from the DC side to AC side). In the following sections, the modelling of the converter in both modes is presented.

Table 3.1: Voltage levels and associated switch states for a three-level NPC phase-leg

Output V_{AO}	Switch states			
	S_{a1}	S_{a2}	S_{a3}	S_{a4}
$V_{dc}/2$	1	1	0	0
0	0	1	1	0
$-V_{dc}/2$	0	0	1	1

The following assumptions are made in order to derive a state-space averaged model of the NPC converter:

(1) All switching devices are ideal with identical characteristics.

(2) All parasitic elements of circuit components, such as the capacitor equivalent series resistance are negligible.

(3) All snubber circuit components are omitted for simplicity.

(4) The SPWM method is employed. The frequency of the carrier is high enough so that the reference signal value can be regarded as constant.

3.2.1 Modelling of the NPC Converter in Rectifier Mode

Fig. 3.1 illustrates the schematic diagram of the three-phase three-level converter working in the rectifier mode. It is assumed that the converter is connected to the AC mains through linked reactors L_s. The resistor R_s is used to represent the effective line resistance. A pole of the three-level converter can be regarded as a multiplexer which may be switched to any DC side potentials according to the multilevel PWM strategy employed. The source voltages are assumed ideal and balanced.

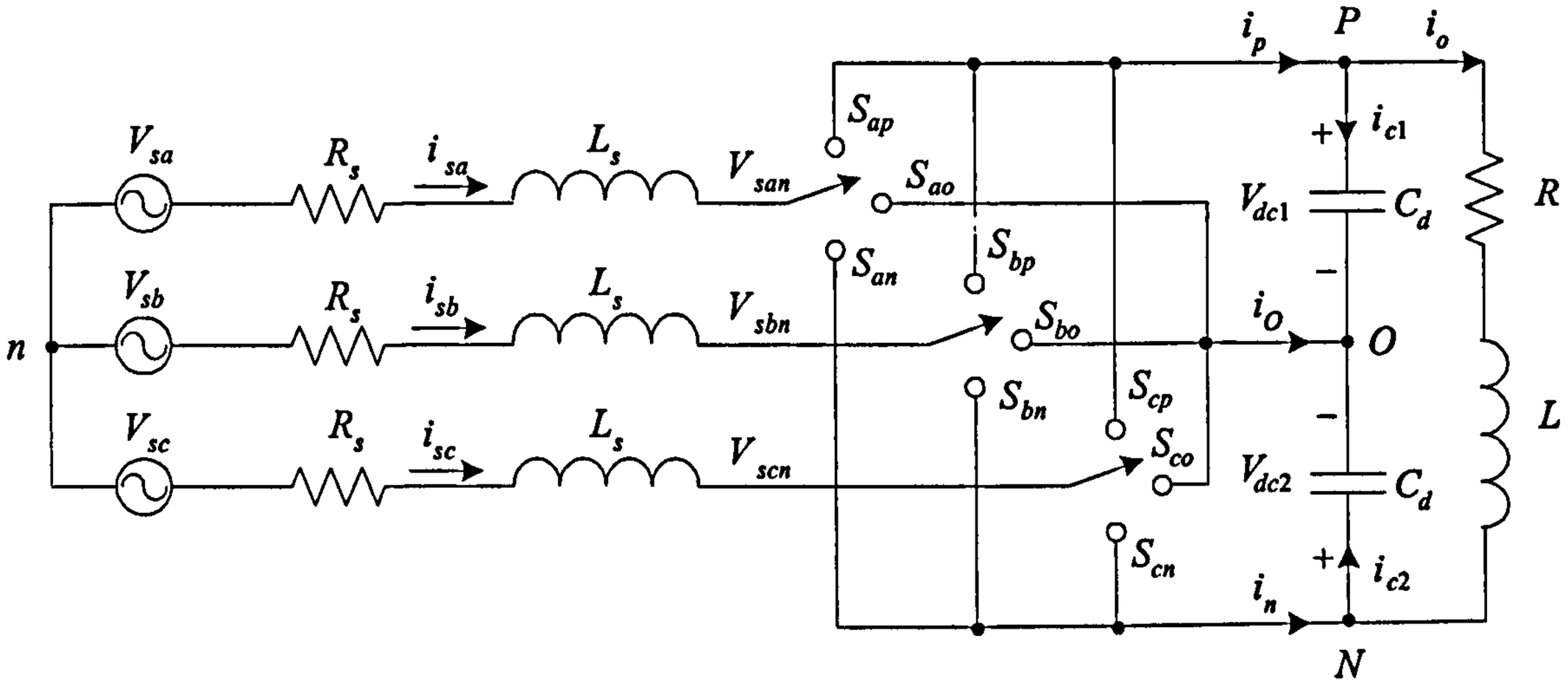


Fig. 3.1: Schematic circuit of the three-phase three-level inverter in the rectifier mode.

Switching functions S_i (i=a, b, c) are introduced to represent the semiconductor switching states shown in Table 3.1 which are determined by the PWM control technique. S_i is defined as:

$$S_i = \begin{cases} 1 & S_{i1} \text{ and } S_{i2} \text{ are on, } S_{i3} \text{ and } S_{i4} \text{ are off} \\ 0 & S_{i2} \text{ and } S_{i3} \text{ are on, } S_{i1} \text{ and } S_{i4} \text{ are off} \\ -1 & S_{i3} \text{ and } S_{i4} \text{ are on, } S_{i1} \text{ and } S_{i2} \text{ are off} \end{cases} \tag{3-1}$$

For simplicity, breaking S_i further into S_{ip}, S_{io}, S_{in}, the relationship between switching functions and switching states can be defined as shown in Table 3.2.

Table 3.2: Relationship between switching functions and switch states

Switching Functions				Switch States			
S_i	S_{ip}	S_{io}	S_{in}	S_{a1}	S_{a2}	S_{a3}	S_{a4}
1	1	0	0	1	1	0	0
0	0	1	0	0	1	1	0
-1	0	0	1	0	0	1	1

$$\begin{cases} S_{ip} + S_{io} + S_{in} = 1 \\ S_{ij} = 0 \text{ or } 1 \end{cases} \tag{3-2}$$

where i=a,b,c and j=p,o,n. Therefore, the modelling of the three-phase three-level converter can be described using the following equations.

$$\begin{cases} L_s \dfrac{di_{sa}}{dt} = V_{sa} - R_s \cdot i_{sa} - V_{san} \\ L_s \dfrac{di_{sb}}{dt} = V_{sb} - R_s \cdot i_{sb} - V_{sbn} \\ L_s \dfrac{di_{sc}}{dt} = V_{sc} - R_s \cdot i_{sc} - V_{scn} \end{cases} \tag{3-3}$$

$$V_{san} = V_{saO} + V_{On} \tag{3-4}$$

$$\begin{cases} V_{saO} = S_{ap} \cdot V_{dc1} + S_{an} \cdot V_{dc2} \\ V_{sbO} = S_{bp} \cdot V_{dc1} + S_{bn} \cdot V_{dc2} \\ V_{scO} = S_{cp} \cdot V_{dc1} + S_{cn} \cdot V_{dc2} \end{cases} \tag{3-5}$$

Since the source voltages from the mains are assumed ideal and balanced, so

$$\begin{cases} V_{sa} + V_{sb} + V_{sc} = 0 \\ i_{sa} + i_{sb} + i_{sc} = 0 \end{cases} \tag{3-6}$$

Incorporating eq. (3-6) and eq. (3-3) into eq. (3-4), V_{On} is given by:

$$V_{On} = -\frac{V_{saO} + V_{sbO} + V_{scO}}{3} \tag{3-7}$$

By combining eq. (3-4), eq. (3-5) and eq. (3-7), the following expressions are obtained:

$$\begin{cases} V_{san} = \left(S_{ap} - \dfrac{S_{ap} + S_{bp} + S_{cp}}{3} \right) \cdot V_{dc1} + \left(S_{an} - \dfrac{S_{an} + S_{bn} + S_{cn}}{3} \right) \cdot V_{dc2} \\ V_{sbn} = \left(S_{bp} - \dfrac{S_{ap} + S_{bp} + S_{cp}}{3} \right) \cdot V_{dc1} + \left(S_{bn} - \dfrac{S_{an} + S_{bn} + S_{cn}}{3} \right) \cdot V_{dc2} \\ V_{scn} = \left(S_{cp} - \dfrac{S_{ap} + S_{bp} + S_{cp}}{3} \right) \cdot V_{dc1} + \left(S_{cn} - \dfrac{S_{an} + S_{bn} + S_{cn}}{3} \right) \cdot V_{dc2} \end{cases} \tag{3-8}$$

For node P,

$$\begin{cases} i_p = i_{c1} + i_o = C_d \dfrac{dV_{dc1}}{dt} + i_o \\ i_p = S_{ap} \cdot i_{sa} + S_{bp} \cdot i_{sb} + S_{cp} \cdot i_{sc} \end{cases} \tag{3-9}$$

For node O,

$$\begin{cases} i_O = -(i_{c1} + i_{c2}) = -\left(C_d \dfrac{dV_{dc1}}{dt} + C_d \dfrac{dV_{dc2}}{dt} \right) \\ i_O = S_{ao} \cdot i_{sa} + S_{bo} \cdot i_{sb} + S_{co} \cdot i_{sc} \end{cases} \tag{3-10}$$

For node N,

$$\begin{cases} i_n = i_{c1} - i_o = C_d \dfrac{dV_{dc2}}{dt} - i_o \\ i_n = S_{an} \cdot i_{sa} + S_{bn} \cdot i_{sb} + S_{cn} \cdot i_{sc} \end{cases} \tag{3-11}$$

For the load on the DC side,

$$L\frac{di_o}{dt} = -R \cdot i_o + V_{dc1} - V_{dc2} \tag{3-12}$$

Thus the mathematical modelling of the three-phase three-level NPC converter operating as a rectifier can be written as the following state equation:

$$C \cdot \dot{X} = A \cdot X + B \cdot e \tag{3-13}$$

Here, $C = diag\left[L_s \quad L_s \quad L_s \quad C_d \quad C_d \quad L\right]$

$$X = \left[i_{sa} \quad i_{sb} \quad i_{sc} \quad V_{dc1} \quad V_{dc2} \quad i_o\right]^T$$

$$A=\begin{bmatrix} -R_s & 0 & 0 & -\left(S_{ap}-\frac{S_{ap}+S_{bp}+S_{cp}}{3}\right) & -\left(S_{an}-\frac{S_{an}+S_{bn}+S_{cn}}{3}\right) & 0 \\ 0 & -R_s & 0 & -\left(S_{bp}-\frac{S_{ap}+S_{bp}+S_{cp}}{3}\right) & -\left(S_{bn}-\frac{S_{an}+S_{bn}+S_{cn}}{3}\right) & 0 \\ 0 & 0 & -R_s & -\left(S_{cp}-\frac{S_{ap}+S_{bp}+S_{cp}}{3}\right) & -\left(S_{cn}-\frac{S_{an}+S_{bn}+S_{cn}}{3}\right) & 0 \\ S_{ap} & S_{bp} & S_{cp} & 0 & 0 & -1 \\ S_{an} & S_{bn} & S_{cn} & 0 & 0 & 1 \\ 0 & 0 & 0 & 1 & -1 & -R \end{bmatrix}$$

$$B=diag\begin{bmatrix}1 & 1 & 1 & 0 & 0 & 0\end{bmatrix}$$

$$e=diag\begin{bmatrix}V_{sa} & V_{sb} & V_{sc} & 0 & 0 & 0\end{bmatrix}$$

If the AC mains supply is balanced, the voltage sources are given as:

$$\begin{bmatrix} V_{sa} \\ V_{sb} \\ V_{sc} \end{bmatrix}=\hat{V}_s\begin{bmatrix} cos(\omega t+\alpha) \\ cos(\omega t+\alpha-120^\circ) \\ cos(\omega t+\alpha+120^\circ) \end{bmatrix} \tag{3-14}$$

Here, ω is the angular speed, α is the initial phase angle of the phase A of the voltage source, $\hat{V}_s$ is the peak value of the line-to-neutral voltage of the mains.

3.2.2 Modelling of the NPC Converter in Inverter Mode

Similarly, the modeling of the three-phase three-level converter in the inverter mode as illustrated in Fig. 3.2, can be described using the following equations: (The load is assumed to be an *RL* load in this case)

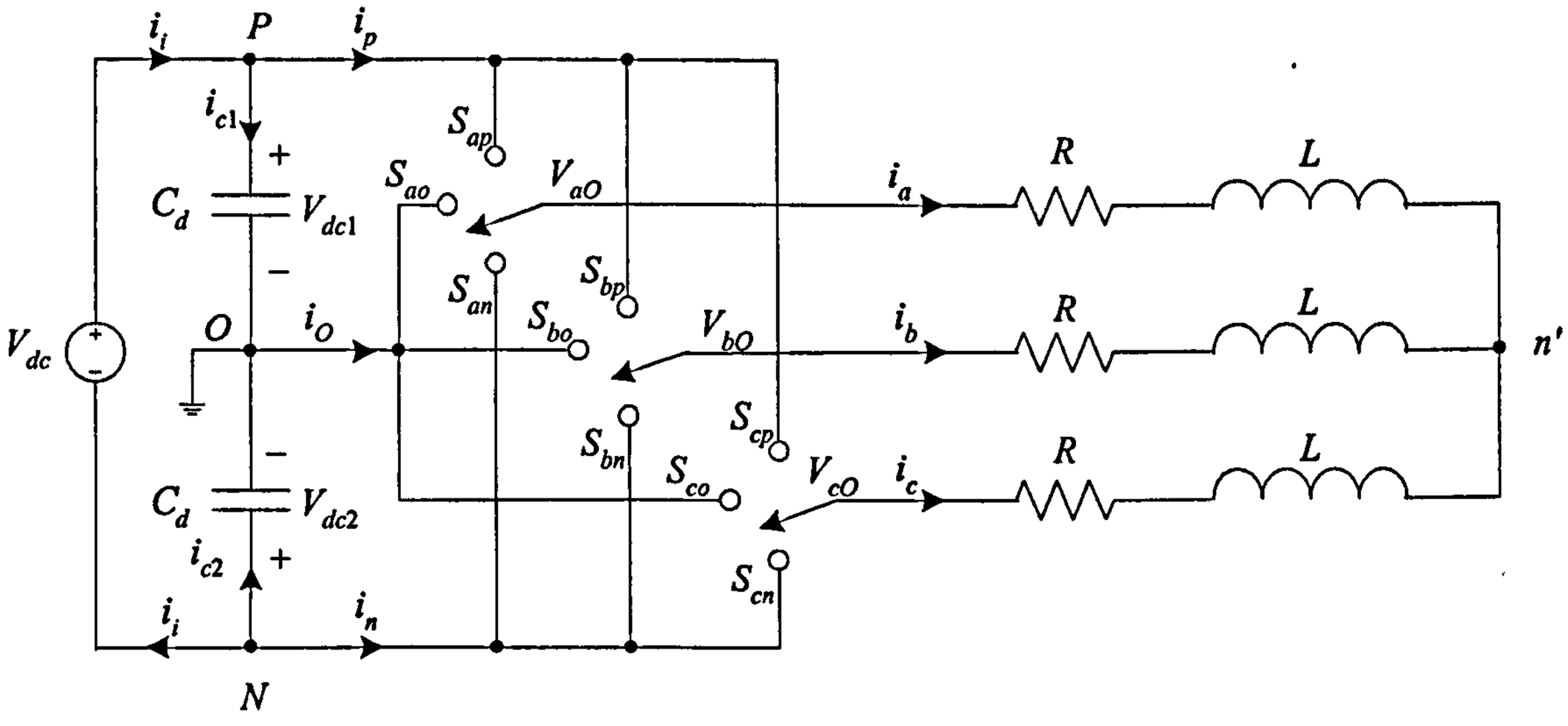


Fig. 3.2: Schematic circuit of the three-phase three-level NPC converter operating in the inverter mode.

In the AC load side,

$$\begin{cases} L\dfrac{di_a}{dt} = V_{ao} - R\cdot i_a - V_{n'O} \\ L\dfrac{di_b}{dt} = V_{bo} - R\cdot i_b - V_{n'O} \\ L\dfrac{di_c}{dt} = V_{co} - R\cdot i_c - V_{n'O} \end{cases} \tag{3-15}$$

$$\begin{cases} V_{aO} = S_{ap}\cdot V_{dc1} + S_{an}\cdot V_{dc2} \\ V_{bO} = S_{bp}\cdot V_{dc1} + S_{bn}\cdot V_{dc2} \\ V_{cO} = S_{cp}\cdot V_{dc1} + S_{cn}\cdot V_{dc2} \end{cases} \tag{3-16}$$

If the load is balanced and the harmonic components generated by the switching operation are assumed to be negligible, the following equation is true:

$$i_a + i_b + i_c = 0 \tag{3-17}$$

Substituting eq. (3-16) and eg. (3-17) into eq. (3-15), then eq. (3-16), $V_{n'O}$ is derived as:

$$V_{n'O} = \frac{S_{ap}+S_{bp}+S_{cp}}{3}V_{dc1} + \frac{S_{an}+S_{bn}+S_{cn}}{3}V_{dc2} \tag{3-18}$$

For the node *P*:

$$\begin{cases} i_{c1} = C_d\dfrac{dV_{dc1}}{dt} = i_i - i_p \\ i_p = S_{ap}\cdot i_a + S_{bp}\cdot i_b + S_{cp}\cdot i_c \end{cases} \tag{3-19}$$

For the node *N*:

$$\begin{cases} i_{c2} = C_d\dfrac{dV_{dc2}}{dt} = -i_i - i_n \\ i_n = S_{an}\cdot i_a + S_{bn}\cdot i_b + S_{cn}\cdot i_c \end{cases} \tag{3-20}$$

For the neutral point of the DC side node *O*:

$$\begin{cases} i_O = i_{c1} + i_{c2} = C_d\dfrac{dV_{dc1}}{dt} + C_d\dfrac{dV_{dc2}}{dt} \\ i_O = S_{ao}\cdot i_a + S_{bo}\cdot i_b + S_{co}\cdot i_c \end{cases} \tag{3-21}$$

The above equations can be written using the state equation as follows:

$$C\cdot\dot{X} = A\cdot X + B\cdot e \tag{3-22}$$

Here,

$$C = diag\begin{bmatrix} L & L & L & C_d & C_d & 0 \end{bmatrix}$$

$$X = \begin{bmatrix} i_a & i_b & i_c & V_{dc1} & V_{dc2} & i_i \end{bmatrix}^T$$

$$A=\begin{bmatrix} -R & 0 & 0 & \left(S_{ap}-\frac{S_{ap}+S_{bp}+S_{cp}}{3}\right) & \left(S_{an}-\frac{S_{an}+S_{bn}+S_{cn}}{3}\right) & 0 \\ 0 & -R & 0 & \left(S_{bp}-\frac{S_{ap}+S_{bp}+S_{cp}}{3}\right) & \left(S_{bn}-\frac{S_{an}+S_{bn}+S_{cn}}{3}\right) & 0 \\ 0 & 0 & -R & \left(S_{cp}-\frac{S_{ap}+S_{bp}+S_{cp}}{3}\right) & \left(S_{cn}-\frac{S_{an}+S_{bn}+S_{cn}}{3}\right) & 0 \\ -S_{ap} & -S_{bp} & -S_{cp} & 0 & 0 & 1 \\ -S_{an} & -S_{bn} & -S_{cn} & 0 & 0 & -1 \\ 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix}$$

$$B=e=0$$

3.2.3 Equivalent Circuit of NPC Converter at Fundamental Frequency

As mentioned before, the switching functions S_{ip}, S_{io}, S_{in}, (i=a, b, c) are determined by the PWM control technique. Taking phase A as an example, if the reference control signal is a pure sinusoidal wave, which is expressed as:

$$v_{ref}=\hat{A}_o\cdot sin\omega t \tag{3-23}$$

Here, $\hat{A}_o$ is the amplitude of the modulating waveform with the range of ($0<\hat{A}_o\leq 1$). Since the sinusoidal wave is repetitive, it is possible to replace the ωt term by the angle θ, in the range of $0\leq\theta<2\pi$. Then the modulation patterns (i.e., switching functions) at fundamental frequency for three nodes shown in Fig. 3.3 can be obtained as:

$$S_{ap}(\theta)=\begin{cases}\hat{A}_o\cdot sin\theta, & 0\leq\theta<\pi\\ 0, & \pi\leq\theta<2\pi\end{cases} \tag{3-24}$$

$$S_{ao}(\theta)=\begin{cases}1-\hat{A}_o\cdot sin\theta, & 0\leq\theta<\pi\\ 1+\hat{A}_o\cdot \sin\theta, & \pi\leq\theta<2\pi\end{cases} \tag{3-25}$$

$$S_{an}(\theta)=\begin{cases}0, & 0\leq\theta<\pi\\ -\hat{A}_o\cdot sin\theta, & \pi\leq\theta<2\pi\end{cases} \tag{3-26}$$

Assuming the load is linear and reactive, the load current i_a can be taken as being purely sinusoidal and be expressed as:

$$i_a(\theta)=\hat{I}\cdot sin(\theta+\phi) \tag{3-27}$$

Here, $\hat{I}$ is the current peak value, ϕ is the phase shift angle between the current and the output voltage at fundamental frequency. Then the currents drawn from the three nodes of

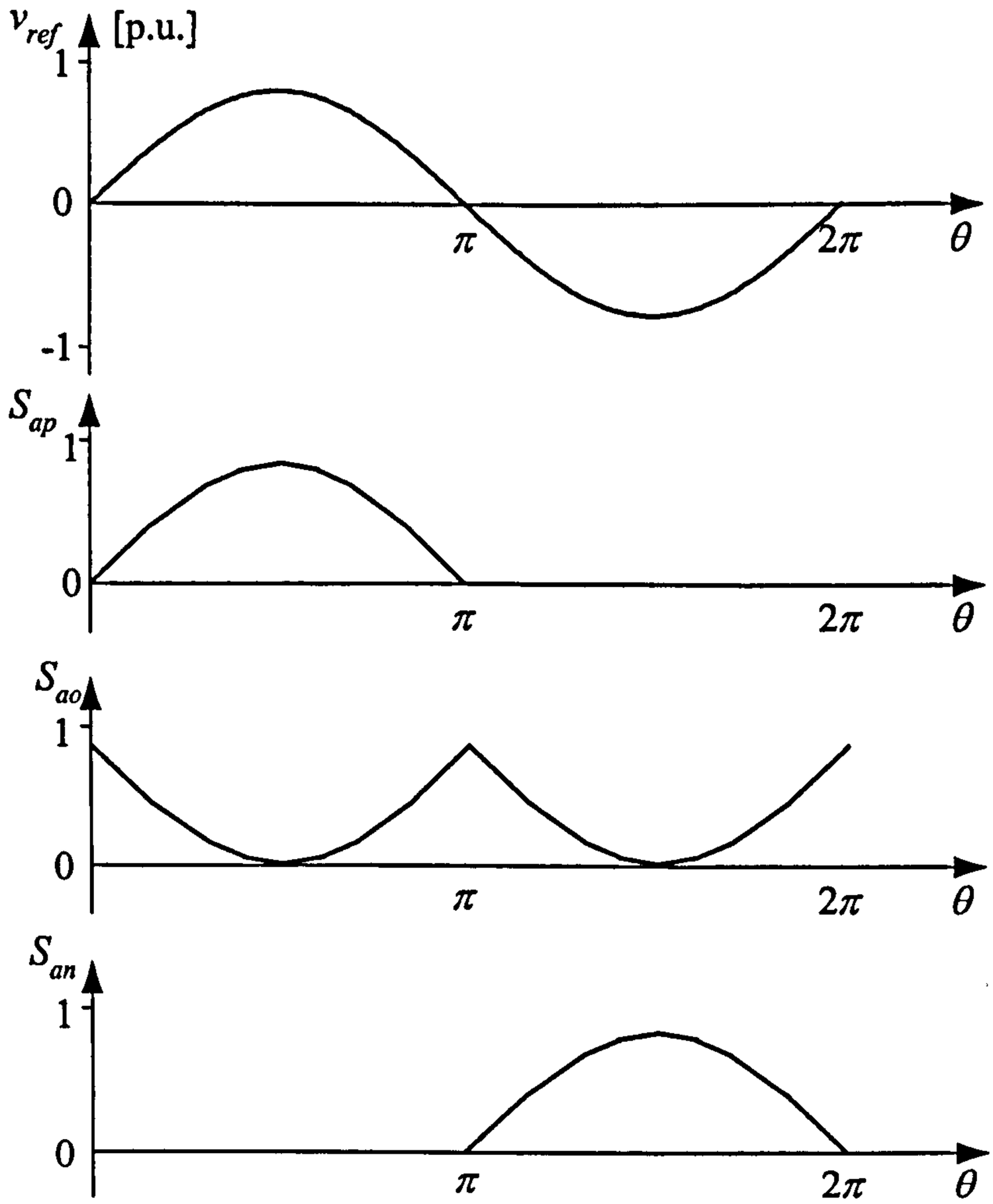


Fig. 3.3: Modulating waveforms for the switching functions.

the capacitor bank are the product of the phase current and the respective switching functions. The equations are given:

$$\begin{cases} i_p(\theta) = i_a(\theta) \cdot S_{ap}(\theta) \\ i_O(\theta) = i_a(\theta) \cdot S_{ao}(\theta) \\ i_n(\theta) = i_a(\theta) \cdot S_{an}(\theta) \end{cases} \tag{3-28}$$

By integrating the instantaneous current over the modulation cycle, the mean current of each node can be derived as:

$$\begin{cases} \overline{i_p} = \dfrac{1}{2\pi} \int_0^{2\pi} i_a(\theta) \cdot S_{ap}(\theta) \cdot d\theta = \dfrac{\hat{A}_o \hat{I}}{4} \cos\phi \\ \overline{i_n} = \dfrac{1}{2\pi} \int_0^{2\pi} i_a(\theta) \cdot S_{an}(\theta) \cdot d\theta = -\dfrac{\hat{A}_o \hat{I}}{4} \cos\phi \\ \overline{i_O} = \dfrac{1}{2\pi} \int_0^{2\pi} i_a(\theta) \cdot S_{ao}(\theta) \cdot d\theta = 0 \end{cases} \tag{3-29}$$

It can be seen that the neutral point current in the DC link has a mean value of zero; the positive point current has the same mean value as the negative point current except for opposite direction. It should be noted again that eq. (3-28) and eq. (3-29) are based on a single phase of the NPC converter.

According to the voltage and current eqs. (3-8)-(3-11), (3-16)-(3-21) and (3-29), the fundamental frequency equivalent circuit can be drawn out in Fig. 3.4.

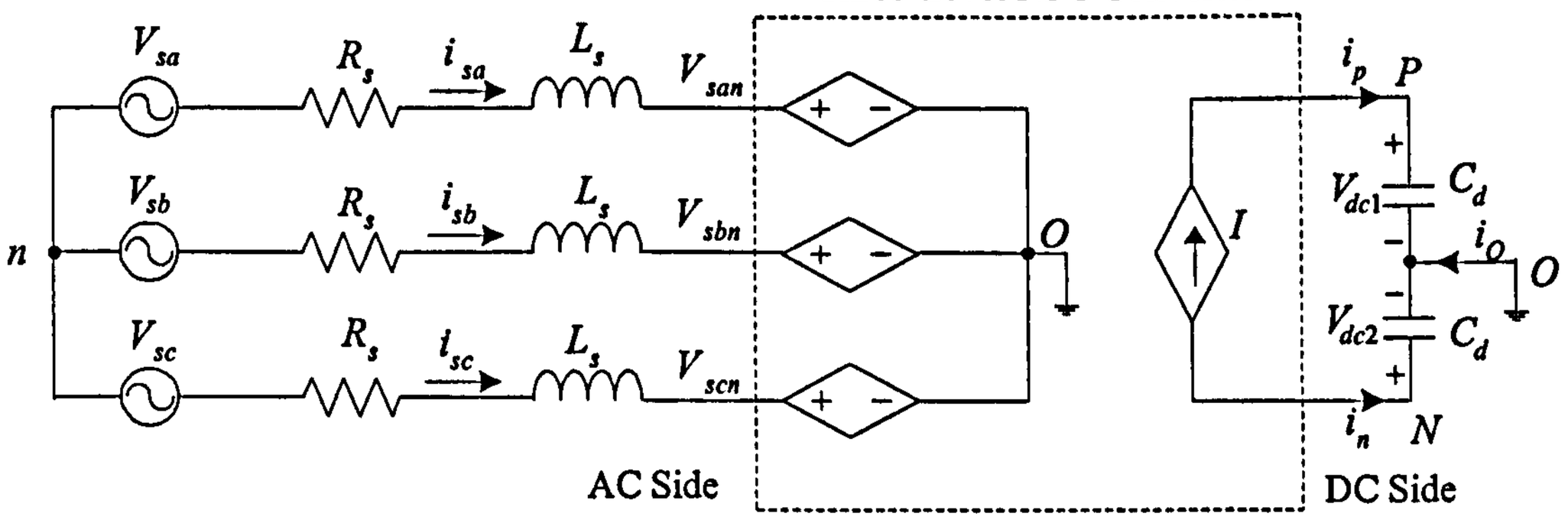


Fig. 3.4: Fundamental frequency equivalent circuit of the three-level NPC converter.

It can be seen that the three-level NPC converter can be modelled as a set of voltage controlled voltage sources in the AC side and current controlled current source on the DC side in the fundamental frequency domain. All these controlled sources are related to the switching functions, no matter what kind of sources they are.

3.2.4 Influence of the Current on the Neutral-Point Voltage

The influence of the current i_O on the inverter can be seen from eq. (3-30) derived from eq. (3-21).

$$i_O = i_{c1} + i_{c2} = C_d \frac{dV_{dc1}}{dt} + C_d \frac{dV_{dc2}}{dt} = C_d \frac{d(|V_{dc1}| - |V_{dc2}|)}{dt} \tag{3-30}$$

It can be seen that the neutral point current i_O is related with the DC link capacitor voltage balancing. If $|V_{dc1}| = |V_{dc2}|$ at any time, $i_O = 0$. Actually, i_O cannot be zero all the time due to the switching action of the converter legs. Therefore, the capacitor voltage is allowed to be on perturbation within the error band. Derived from eq. (3-30),

$$|V_{dc1}|_t - |V_{dc2}|_t = |V_{dc1}|_0 - |V_{dc2}|_0 + \frac{1}{C_d}\int_0^t i_O \, dt \tag{3-31}$$

It can be seen from eq. (3-31) that the value of the DC bus capacitors affects the variation of voltage. The higher the capacitance value, the lower the voltage variation. As analysed before, the mean current drawn from the neutral point over a modulation cycle is zero and the neutral point potential remains constant under normal operation. However, during transient operation, or if there is any imbalance in the output switching pattern, or imbalance in the characteristics of the circuit components, and/or non-ideal features of switching devices and their operation all will contribute to a non-zero mean current drawn at the neutral-point, thus resulting in variation of the neutral point voltage. Therefore, regulation is required to ensure that balance is maintained during disturbances.

One solution is to use a closed-loop control method. For example, if the values of the $|V_{dc1}|$, $|V_{dc2}|$ and i_O are known as well as the direction of i_O by measurement, the voltage balancing of the DC capacitors according to equation (3-31) can be controlled. Other solutions include the addition of zero sequence components into the modulation pattern [16], [17], [77], [78] and use of an optimal PWM [19], [79], [80], through the selection of states similar to SV-PWM.

3.3 Multi-carrier SPWM Techniques

Up to now, numerous MSPWM control techniques have been used to control the NPC inverters. They have been analysed mathematically and a number of papers have discussed their advantages and their harmonic performance [37]-[39], [81]-[83]. However, there is no detailed information available in the technical literature regarding the performance of each technique with respect to switching losses. So far only the carrier phase angle's effect on the switching losses has been reported [81].

It has been recognised that different MSPWM methods are suitable for different multilevel topologies. For instance, the PS-MSPWM method is suitable for flying capacitor converters and cascaded converters, while CD-MSPWM methods are suitable for the NPC converter [37], [38].

So the MSPWM techniques including the CD-MSPWM, the PS-MSPWM and a Hybrid MSPWM (H-MSPWM) technique [8] are described and investigated with respect to their potential application for the NPC converter.

First, in order to describe and evaluate the different methods, some definitions are given below:

- The frequency modulation ratio m_f,

$$m_f = \frac{f_c}{f_o} \tag{3-32}$$

where f_c is the frequency of the carrier signal and f_o is the frequency of the modulating signal.

- The amplitude modulation ratio m_a, with m_a defined for each modulation technique in Table 3.3, where $\hat{A}_o$ is the amplitude of the modulating signal and $\hat{A}_c$ is the amplitude of the carrier (triangular) signal, m is the number of the voltage level.
- The displacement angle φ between the modulating signal (sinusoidal) and the first positive triangular carrier signal. In this thesis only φ=0 is considered.

Table 3.3: Definition of m_a for the various MSPWM techniques

CD-MSPWM	PS-MSPWM	H-MSPWM
$m_a = \frac{\hat{A}_o}{(m-1)\cdot \hat{A}_c}$	$m_a = \frac{\hat{A}_o}{\hat{A}_c}$	$m_a = \frac{\hat{A}_o}{2\cdot \hat{A}_c}$

3.3.1 Carrier Disposition Multi-carrier SPWM Techniques

For an m-level converter, m-1 carriers with the same frequency f_c and same amplitude $\hat{A}_c$ are disposed such that the bands they occupy are contiguous. The reference, or modulation, waveform has amplitude $\hat{A}_o$ and frequency f_o, and it is centred in the middle of the carrier set. The reference is continuously compared with each of the carrier signals. If the reference is greater than a carrier signal, then the active device corresponding to that carrier is switched on, and if the reference is less than a carrier signal, then the active device corresponding to that carrier is switched off.

According to the different dispositions of carrier bands, there are three methods, provided that the number of levels of an inverter is an odd number: in-Phase Disposition (PD), Alternative Phase Opposition Disposition (APOD), and Phase Opposition Disposition (POD).

- **In-Phase Disposition Control Method**

In this method, all the carriers are in phase. For this technique, significant harmonic energy is concentrated at the carrier frequency f_c, but since it is a co-phasal component, it does not appear in the line-to-line voltage. Fig. 3.5 illustrates the PD strategy, the output voltage waveforms and their spectrum.

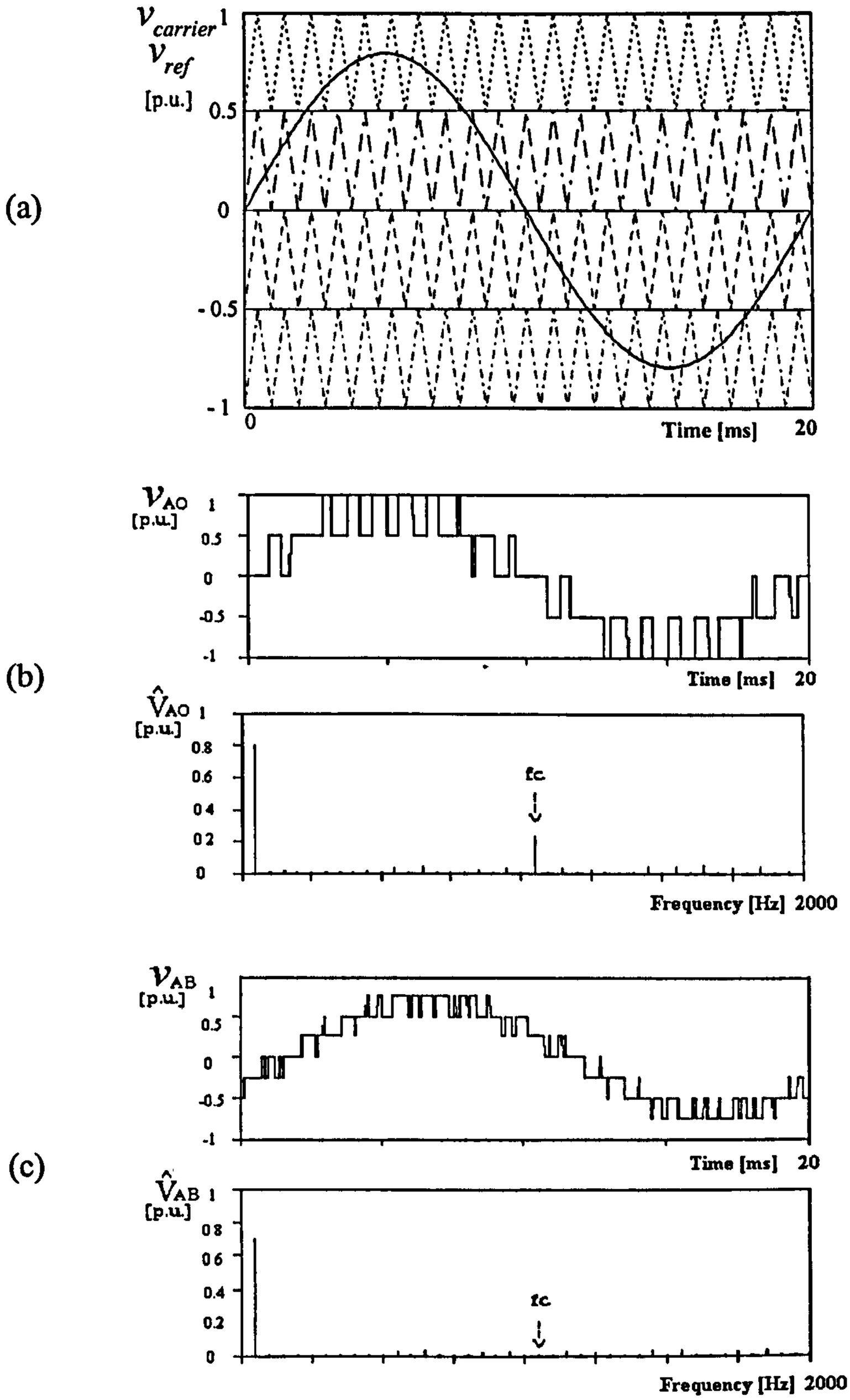


Fig. 3.5: The PD technique at m_a=0.8, m_f=21, f_o=50 Hz, m=5. (a) Carrier waveforms and modulating signal. (b) Phase voltage and its spectrum. (c) Line-to-line voltage and its spectrum.

- **Alternative Phase Opposition Disposition Control Method**

In this method, each carrier band is shifted by 180° from the adjacent bands. With this method, the most significant harmonics are centred as sidebands around the carrier frequency f_c. No harmonics occur at f_c. Figure 3.6 illustrates the APOD strategy, the output voltage waveforms and their spectra.

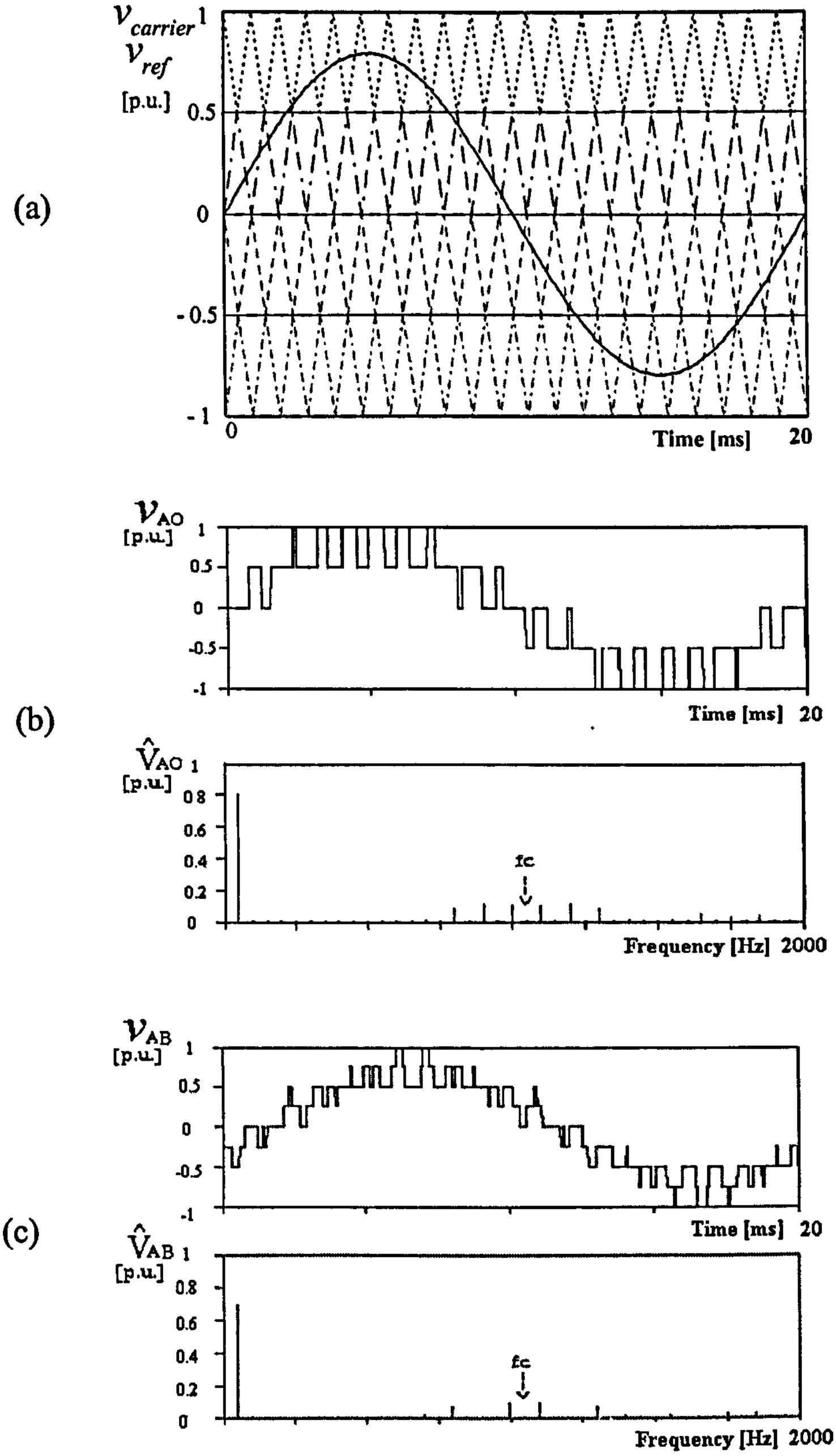


Fig. 3.6: The APOD technique at m_a=0.8, m_f=21, f_o=50 Hz, m=5. (a) Carrier waveforms and modulating signal. (b) Phase voltage and its spectrum. (c) Line-to-line voltage and its spectrum.

• **Phase Opposition Disposition Control Method**

In this method, the carriers above the zero reference are in phase, but shifted by180° from those carriers below the zero reference. The significant harmonics are located around the f_c for both the phase and line-to-line voltage waveform. Fig. 3.7 illustrates the POD strategy, the output voltage waveforms and their spectrum.

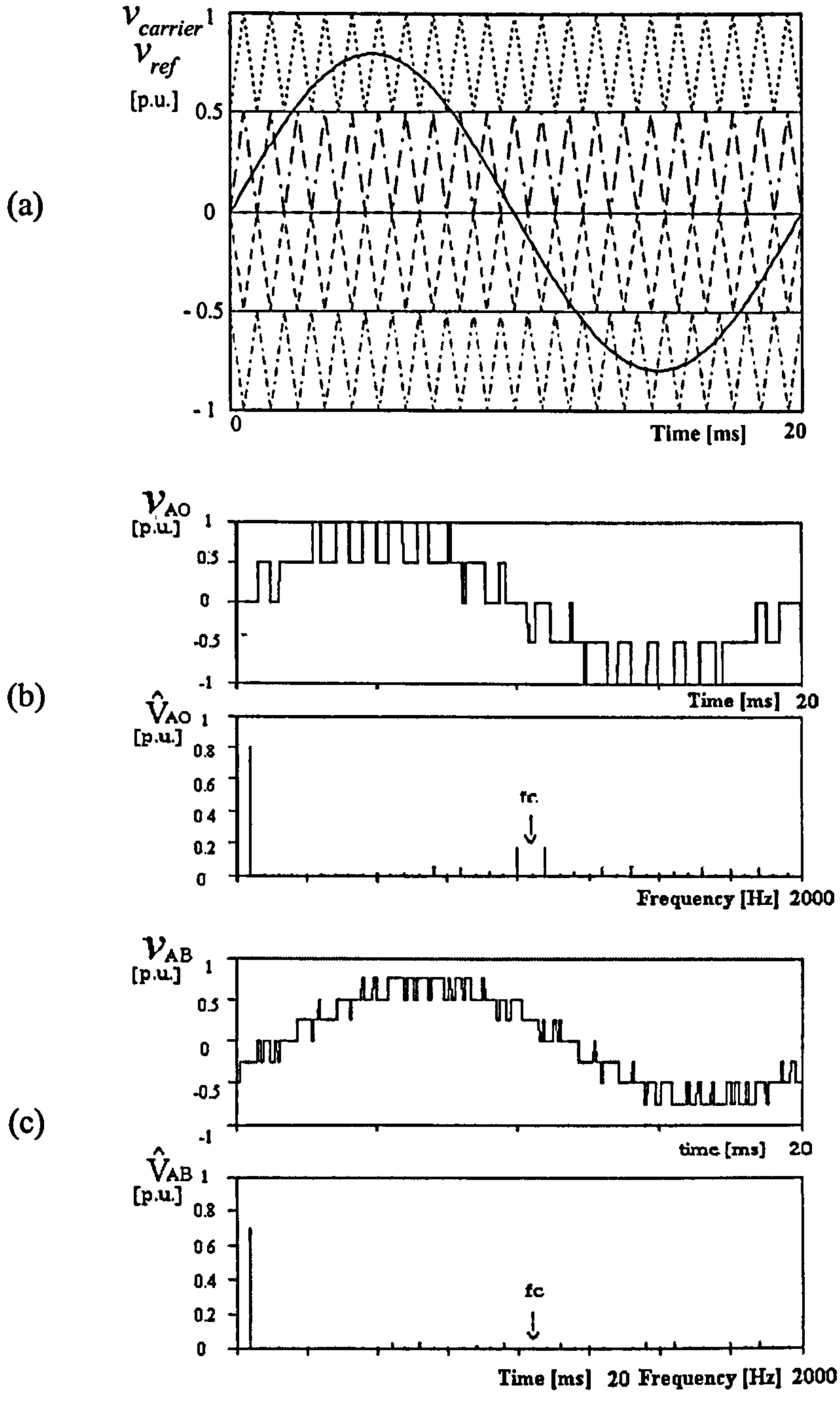


Fig. 3.7: The POD technique at m_a=0.8, m_f=21, f_o=50 Hz, m=5. (a) Carrier waveforms and modulating signal. (b) Phase voltage and its spectrum. (c) Line-to-line voltage and its spectrum.

3.3.2 Phase Shifted MSPWM Technique

For an m-level inverter, m-1 carriers with the same frequency f_c and same amplitude $\hat{A}_c$ are phase shifted by some degrees. They are compared with the modulation sinusoidal signal. For example, for a five-level FC converter, the sinusoidal modulation signal is compared with four triangular carrier signals that are phase shifted by 90 degrees (i.e., time shifted by $T_s/4$, where T_s is the period of these carrier signals). The intersections of carrier and modulation signal determine the instants of switching commutations. When the sine value is larger than the carrier value, the switch turns on and otherwise turns off. The resulting four PWM signals are used to control the corresponding switches on the upper leg. The complementary PWM signals then control the switches on the lower leg. The significant harmonics are located around the $(m\text{-}1)f_c$ for both the phase and line-to-line voltage waveform. Fig. 3.8 illustrates the PS-MSPWM strategy, the output voltage waveforms and their spectrum.

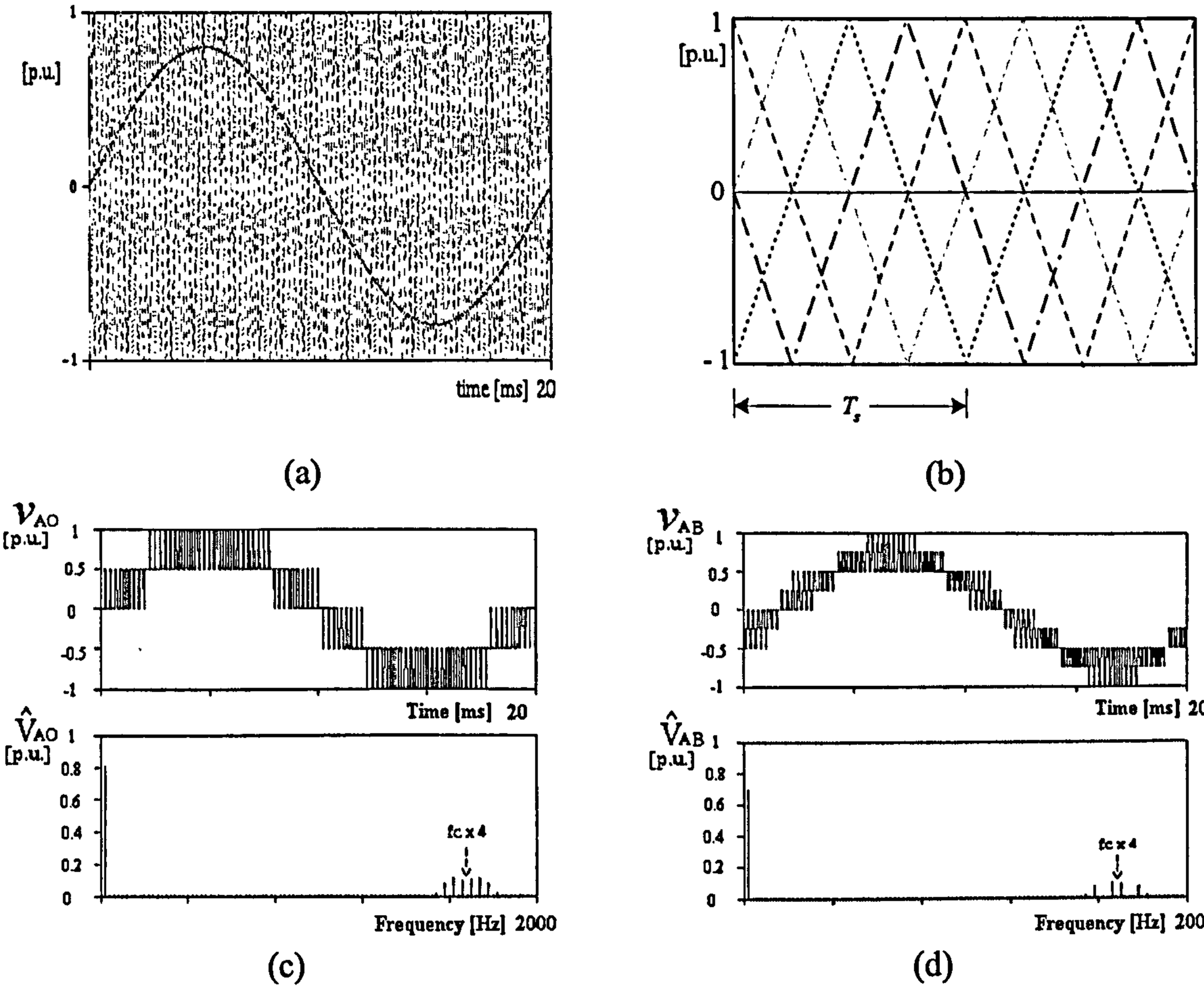


Fig. 3.8: PS-MSPWM at m_a=0.8, m_f=21, f_o=50 Hz, m=5. (a) Waveforms of carriers and modulating signal. (b) Expanding view of the PS-MSPWM. (c) Phase voltage and its spectrum. (d) Line-to-line voltage and its spectrum.

3.3.3 Hybrid MSPWM Technique

This method can be regarded as a combination of the above CD-MSPWM method and PS-MSPWM method. The bands used for modulation are only two. For an m level inverter, $(m\text{-}1)$ carriers are grouped into two parts. The first $(m\text{-}1)/2$ carriers are displaced above the zero band with phase shift by $\frac{2\pi}{(m-1)}$ degrees from each other. The remaining $(m\text{-}1)/2$ carriers are displaced below the zero band and phase shifted accordingly, like the first set of carriers. Fig. 3.9 illustrates the H-MSPWM strategy for a five-level FC converter, the output voltage waveforms and their spectrum. The two carriers above zero have the same peak-to-peak value and the same frequency f_c. However, there is a 180 degrees phase shift between them. The same applies to the two carriers below zero.

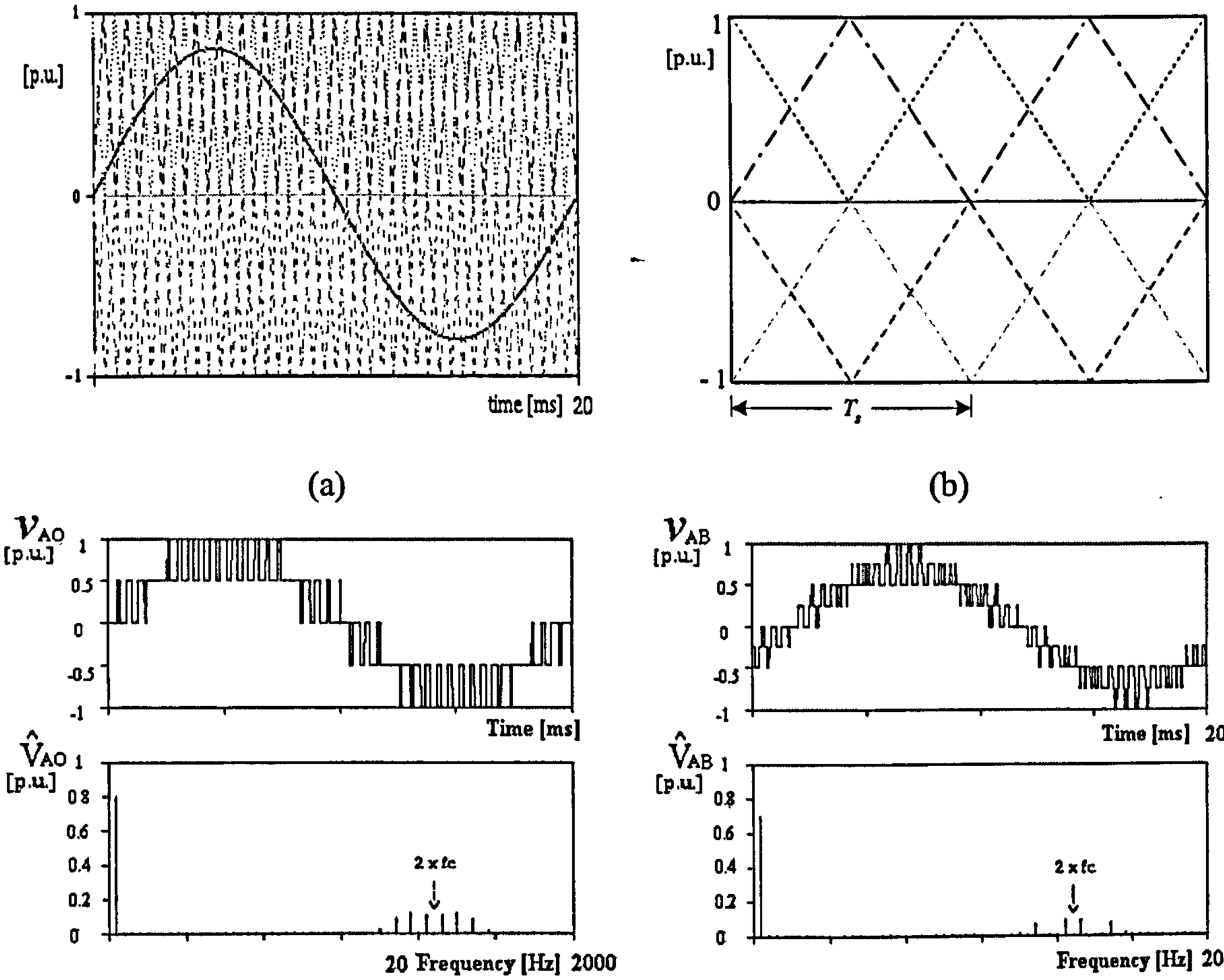


Fig. 3.9: H-MSPWM at m_a=0.8, m_f=21, f_o=50 Hz, m=5. (a) Waveforms of carriers and modulating signal. (b) Expanding view of the H-MSPWM. (c) Phase voltage and its spectrum. (d) Line-to-line voltage and its spectrum.

3.3.4 Basic Features of Multi-carrier SPWM Techniques

The multi-carrier SPWM scheme has similar basic features as the two-level SPWM method, except for the different definitions of m_a. The amplitude of the fundamental frequency component is proportional to m_a, the relationships between m_a and output voltage are the same as eqs. (2-2) to (2-4). Specifically, when $m_a \leq 1$, for a single-phase half-bridge multilevel inverter, the amplitude of the fundamental frequency component $\hat{V}_{AO1}$ is expressed by:

$$\hat{V}_{AO1} = m_a \cdot \frac{V_{dc}}{2} \tag{3-33}$$

where V_{dc} is the DC voltage on the DC side. For a single-phase full-bridge multilevel inverter, the line-to-line voltage output amplitude of the fundamental frequency component $\hat{V}_{AB1}$ is expressed by:

$$\hat{V}_{AB1} = m_a \cdot V_{dc} \tag{3-34}$$

For a three-phase multilevel inverter, the line-to-line voltage output amplitude of the fundamental frequency component $\hat{V}_{AB1}$ is expressed by:

$$\hat{V}_{AB1} = m_a \cdot \frac{\sqrt{3}}{2} V_{dc} \tag{3-35}$$

Another advantageous feature of the MSPWM techniques is that the equivalent switching frequency of the load voltage is many times higher than the switching frequency of each cell. This property allows a reduction in the switching frequency of each cell, thus reducing the switching losses [39].

For the CD-MSPWM methods, the harmonics in the inverter output voltage waveform appear as sidebands, centred around the switching frequency and its multiples. The frequencies at which voltage harmonics occur can be indicated as:

$$f_h = (j \cdot m_f \pm k) \cdot f_o \tag{3-36}$$

where j and k are integers. When j is odd, k is even. When j is even, k is odd.

For the PS-MSPWM method, the equivalent switching frequency of the load voltage is timed by the switching frequency of each cell, as determined by its carrier signal. The frequencies at which voltage harmonics occur is given as:

$$f_h = \left(j \cdot (m-1) \cdot m_f \pm k\right) \cdot f_o \tag{3-37}$$

where j and k are integers as previously defined. Here, m refers to the number of voltage levels.

For the H-MSPWM method, the frequencies at which voltage harmonics occur are:

$$f_h = \left(j \cdot (2 \cdot m_f) \pm k\right) \cdot f_o \tag{3-38}$$

where j and k are integers and defined as above.

3.3.5 Overview of the Power Losses

Power dissipation in semiconductor power devices is fairly generic in nature because the real devices do not have ideal characteristics and hence will dissipate power in practice. A simplified clamped inductive-switching circuit shown in Fig. 3.10 is used as an example to illustrate the generic-switch linearised switching characteristics. The diode here is assumed to be ideal. When the switch in on, the current I flows through the switch and the diode is reverse biased. When the switch is off, I flows through the diode and a voltage equal to the input voltage V_d appears across the switch, assuming a zero voltage drop across the ideal diode [84].

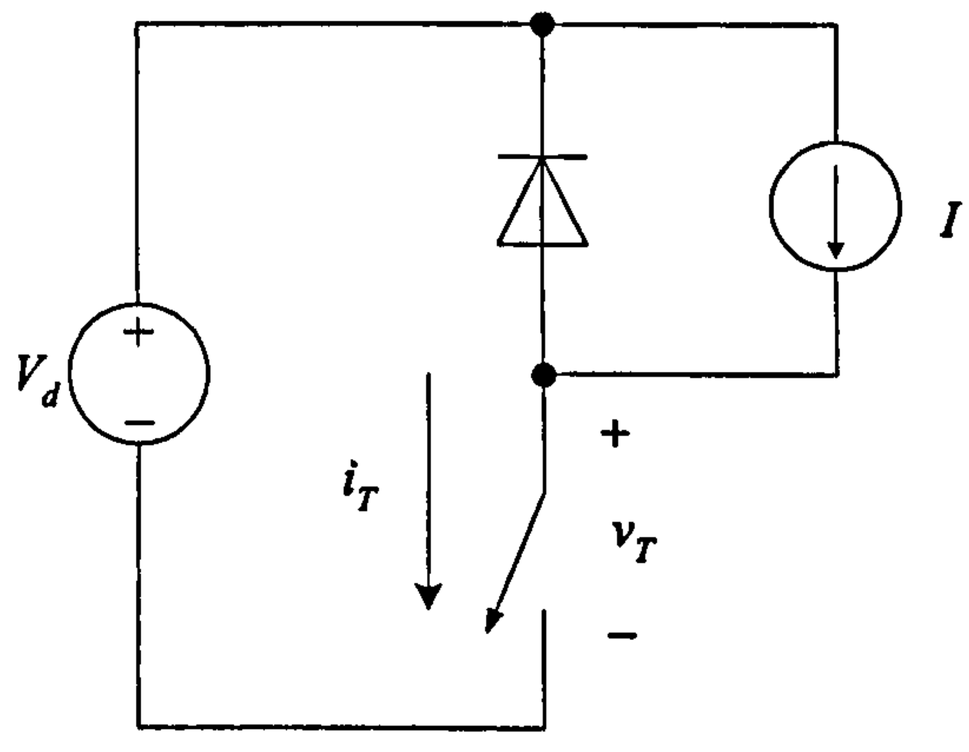


Fig. 3.10: Simplified clamped inductive-switching circuit.

The switch is controlled by the control signal shown in Fig. 3.11 (a). The switch is turned on by a positive control signal and while being off by a negative signal. During the turn-on transition of the generic switch, the current build-up consists of a short delay time $t_{d(on)}$ followed by the current rise time t_{ri}. Only after the current I flows entirely through the switch can the diode become reverse biased, and the switch voltage falls to a small on-state value of V_{on} with a voltage fall time of t_{fv}. The waveforms in Fig. 3.11 (b) indicate that large values of switch voltage and current are present simultaneously during the turn-on crossover interval $t_{c(on)}$, where

$$t_{c(on)} = t_{ri} + t_{fv} \tag{3-39}$$

The energy dissipated in a device during this turn-on transition can be approximated as:

$$W_{c(on)} = \frac{1}{2} \cdot V_d \cdot I \cdot t_{c(on)} \tag{3-40}$$

where it is recognized that no energy dissipation occurs during the turn-on delay interval $t_{d(on)}$.

Once the switch is fully on, the on-state voltage V_{on} will be of the order of one volt or so depending on the device, and it will be conducting a current I. The switch remains in conduction during the on interval t_{on}, which in general is much larger than the turn-on and turn-off transition times. The energy dissipation W_{on} in the switch during this on-state interval can be approximated as:

$$W_{on} = V_{on} \cdot I \cdot T_{on} \tag{3-41}$$

where $t_{on} >> t_{c(on)}, t_{c(off)}$).

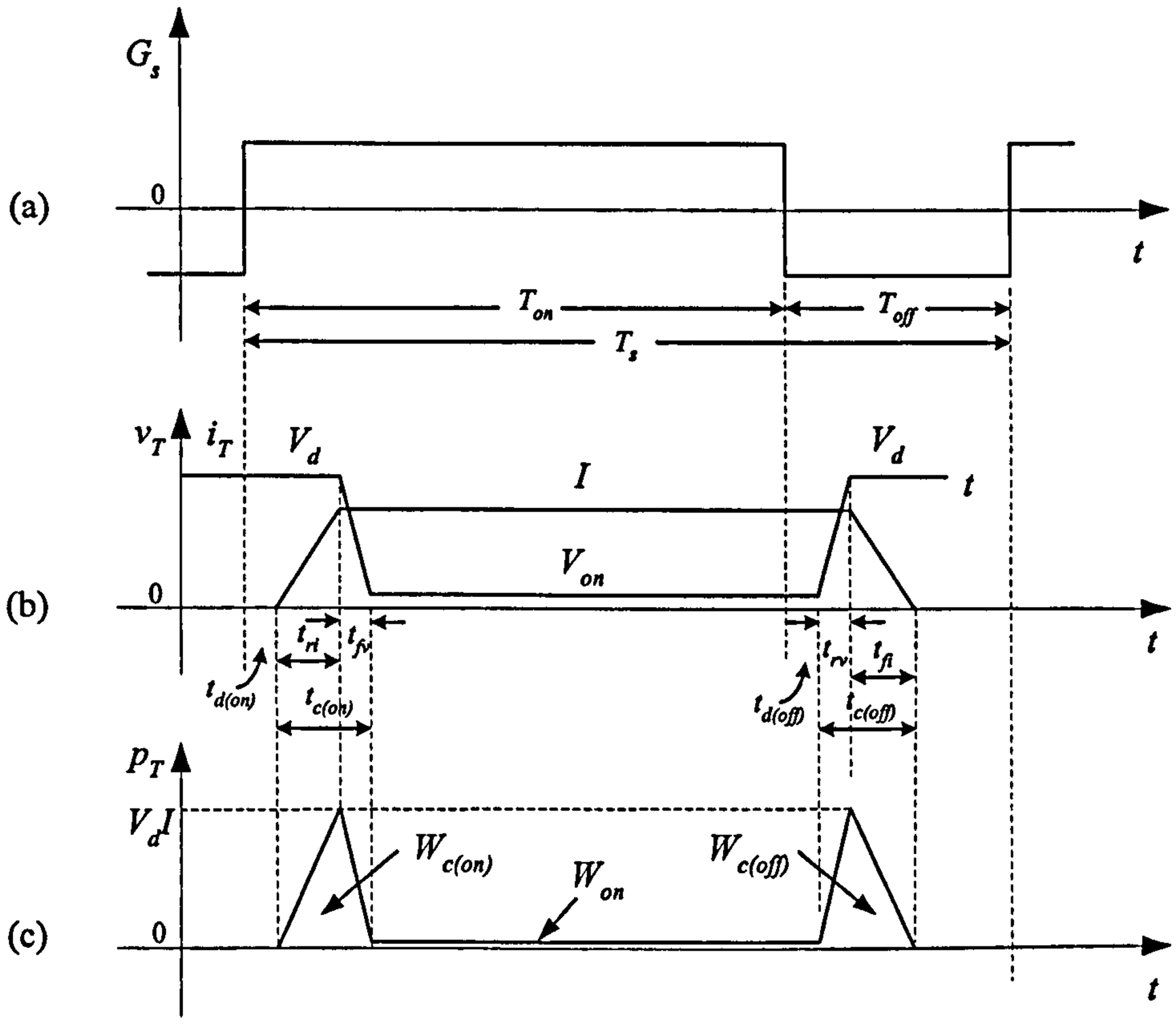


Fig. 3.11: Generic-switch linearied switching characteristics. (a) Switch control signal waveform. (b) Switch voltage and current waveforms. (c) Instantaneous switching power loss waveform.

During the turn-off transition period of the generic switch, the voltage buildup consists of a turn-off delay $t_{d(off)}$ and a voltage rise time t_{rv}. Once the voltage reaches its final value of V_d, the diode can become forward biased and begins to conduct current. The current in the switch falls to zero with a current fall time t_{fi} as the current I commutates from the switch to the diode. Large values of switch voltage and switch current occur simultaneously during the crossover interval $t_{c(off)}$, where

$$t_{c(off)} = t_{rv} + t_{fi} \tag{3-42}$$

The energy dissipated in the switch during this turn-off transition can be written as:

$$W_{c(off)} = \frac{1}{2} \cdot V_d \cdot I \cdot t_{c(off)} \tag{3-43}$$

where any energy dissipation during the turn-off delay interval $t_{d(off)}$ is ignored since it is small compared to $W_{c(off)}$.

The instantaneous power dissipation $p_T = v_T \cdot i_T$ plotted in Fig. 3.11 (c) makes it clear that large instantaneous power dissipation occurs in the switch during the turn-on and turn-off intervals. If there are f_s such turn-on and turn-off transitions per second, then the average switching power loss P_s in the switch due to these transitions can be expressed as:

$$P_s = \frac{1}{2} \cdot V_d \cdot I \cdot f_s \cdot (t_{c(on)} + t_{c(off)}) \tag{3-44}$$

It shows that switching power loss in a switch varies linearly with the switching frequency and the switching times. Therefore, it is desirable to choose switching devices with short switching times and makes them operate at lower switching frequency in order to reduce the switching losses.

The other major contribution to the power loss in the switch is the average power dissipation during the on-state P_{on}, which varies in proportion to the on-state voltage. P_{on} is given by:

$$P_{on} = V_{on} \cdot I \cdot \frac{T_{on}}{T_s} \tag{3-45}$$

which shows that the on-state voltage V_{on} in a switch should be as small as possible.

Generally speaking, the power loss in a switch can be classified as conduction loss, off state loss, and switching loss. Since the leakage current during the off state of the device is negligibly small, the power loss during the off state can be neglected in practice. Therefore, the total average power dissipation P_T in a switch equals the sum of P_s and P_{on}.

$$P_T = P_s + P_{on} \tag{3-46}$$

In theory, the conduction loss P_{on} varies in proportion to the on-state voltage V_{on} and the on-state ratio of each switching device over one switching period, while the switching loss P_s varies linearly with the switching frequency f_s and the switching times.

It can be seen that the main switch with small leakage current in the off state, small on-state voltage and short turn-on and turn-off times can be chosen to minimise the power loss. However, the switching frequency directly impacts on power losses and should be chosen carefully along with the control method. Therefore, it is necessary to examine how different control methods applied to the NPC converter perform to identify which one is optimum and could potentially result in the lower switching losses while providing the best possible harmonic performance for the output voltage.

3.3.6 The Effects of the Different Multi-carrier SPWM Techniques on the Switching Losses and the Harmonic Performance of the NPC Converter

Since the switching loss in a switch varies linearly with the switching frequency, in this thesis, the number of total switching transitions per modulating cycle of main upper switches in a leg is used to indicate the potential switching power losses of a converter. Table 3.4 lists the effects of the different control methods on the switching losses and harmonic performance for the three-phase five-level NPC converter at m_a=0.95, m_f=15, V_{dc}=12 kV. Here, THD_v is the Total Harmonic Distortion of the line-to-line voltage V_{AB}. $\hat{V}_{AB1}$ is the peak value of the V_{AB} at the fundamental frequency. N_{sn} (n=1, 2, ...4) is the number of the switching transitions per fundamental period for main switches of the upper part of the phase A leg. N_{total} is the sum of the above N_{sn}.

Table 3.4: The effects of the different control methods on the switching losses and harmonic performance for a three-phase five-level NPC (m_a=0.95, m_f=15, V_{dc}=12 kV, f_o =50 Hz)

Method	APOD	POD	PD
THD_v (%)	26.5	25.4	16.2
$\hat{V}_{AB1}$ (kV)	9.85	9.84	9.86
N_{s1}	10	10	10
N_{s2}	6	4	4
N_{s3}	4	6	4
N_{s4}	8	10	10
N_{total}	28	30	28

It can be seen from Table 3.4 that the carrier disposition techniques, i.e. APOD, POD and PD, have almost equal potential switching losses only with different THD_v. Since the H-MSPWM technique requires nearly double switching transitions of the carrier disposition techniques, which is half of the PS-MSPWM method. To compare these techniques, the APOD, H and PS methods are normalised with respect to the m_f so that they generate the same number of total switching transitions. Table 3.5 lists these values for comparison. Here, h is the order of the harmonic; $\hat{V}_{ABh}$ is the peak value of V_{AB} at the h-th harmonic frequency. The modulating frequency f_o is 50 Hz.

Table 3.5: Comparisons of the APOD, H-MSPWM and PS-MSPWM techniques at m_a=0.95, V_{dc}=12 kV, f_o =50 Hz

Method	APOD		H-MSPWM		PS-MSPWM	
m_f	24		12		6	
THD_v (%)	25.67		38.04		92.62	
	h	$\hat{V}_{ABh}$ (kV)	h	$\hat{V}_{ABh}$ (kV)	h	$\hat{V}_{ABh}$ (kV)
	1	9.82	1	9.85	1	8.32
	17	0.82	5	0.93	2	0.49
	19	1.18	7	0.76	4	0.75
	23	0.94	11	1.27	5	3.09
	25	0.95	13	1.19	7	1.65
	29	1.17	17	0.72	19	2.78
	37	0.44	19	1.09	23	3.42

From Table 3.5, it is indicated that the H-MSPWM and the PS-MSPWM method are indeed not suitable for the NPC converter. To understand the carrier disposition techniques further, Table 3.6 to 3.8 list the impacts of PD, POD and APOD methods on the harmonic performance and the switching losses of the three-phase five-level NPC at V_{dc}=12 kV, m_a=0.95 with variable m_f.

It can be concluded that the PD technique is the best control method for the NPC topology among the other techniques mentioned above in terms of the THD of the V_{AB} and switching losses. The POD technique is in turn slightly better than the APOD method. This is because with the PD method, the significant harmonic energy is concentrated at the carrier frequency f_c, but since it is a co-phasal component, it does not appear in the line-to-line voltage. (In the three-phase converters, only the harmonics in the line-to-line voltages are of concern).

Table 3.6: Summary of results for a three-phase five-level NPC with PD at m_a=0.95, V_{dc}=12 kV, f_o =50 Hz

m_f	1	15	21	31	45	61
THD_v (%)	15.89	16.9	15.75	15.56	14.41	13.18
$\hat{V}_{AB1}$ (kV)	10.27	9.85	9.84	9.79	9.83	9.83
N_{s1}	2	10	14	20	28	40
N_{s2}	2	4	6	10	14	20
N_{s3}	2	4	6	10	14	20
N_{s4}	2	10	14	20	28	40
N_{total}	8	28	40	60	84	120

Table 3.7: Summary of results for a three-phase five-level NPC with POD at m_a=0.95, V_{dc}=12 kV, f_o =50 Hz

m_f	1	15	21	31	45	61
THD_v (%)	21.05	25.89	25.30	25.29	24.42	24.07
$\hat{V}_{AB1}$ (kV)	10.10	9.83	9.84	9.82	9.83	9.80
N_{s1}	2	10	14	20	28	40
N_{s2}	2	4	6	10	14	20
N_{s3}	2	6	8	12	16	22
N_{s4}	2	10	14	20	30	38
N_{total}	8	30	42	62	88	120

Table 3.8: Summary of results for a three-phase five-level NPC with APOD at m_a=0.95, V_{dc}=12 kV, f_o =50 Hz

m_f	1	15	21	31	45	61
THD_v (%)	24.32	26.88	26.58	26.28	25.65	25.54
$\hat{V}_{AB1}$ (kV)	10.10	9.83	9.84	9.82	9.83	9.80
N_{s1}	2	10	14	20	28	40
N_{s2}	2	6	8	12	16	20
N_{s3}	2	4	6	10	14	20
N_{s4}	2	10	14	20	30	38
N_{total}	8	30	42	62	88	118

3.4 Fundamental Frequency SPWM Technique

Naturally, the aim of minimising the switching losses leads to the idea of using the fundamental frequency technique where the switch only turns on and off once per cycle. The simplest method named FF-SPWM is based on the PD method with m_f=1. If this method is applied to the traditional two-level converter, it will introduce low frequency harmonics, thus making it unsuitable for the two-level converter. It is interesting to find out though if this method can be used in a multilevel converter.

To investigate the performance of the FF-SPWM method when applied to the multilevel converter, simulations have been carried out to examine the FF-SPWM control method to understand what effect this method will have on the NPC multilevel converter. The results are presented in Fig. 3.12 (for a three-level converter), Fig. 3.13 (for a five-level converter), and Fig. 3.14 (for a seven-level converter) respectively.

This strategy makes the converter operate with the lowest possible switching losses. Moreover, comparing with other fundamental switched modulation methods, this method can establish the linear output/input relationship.

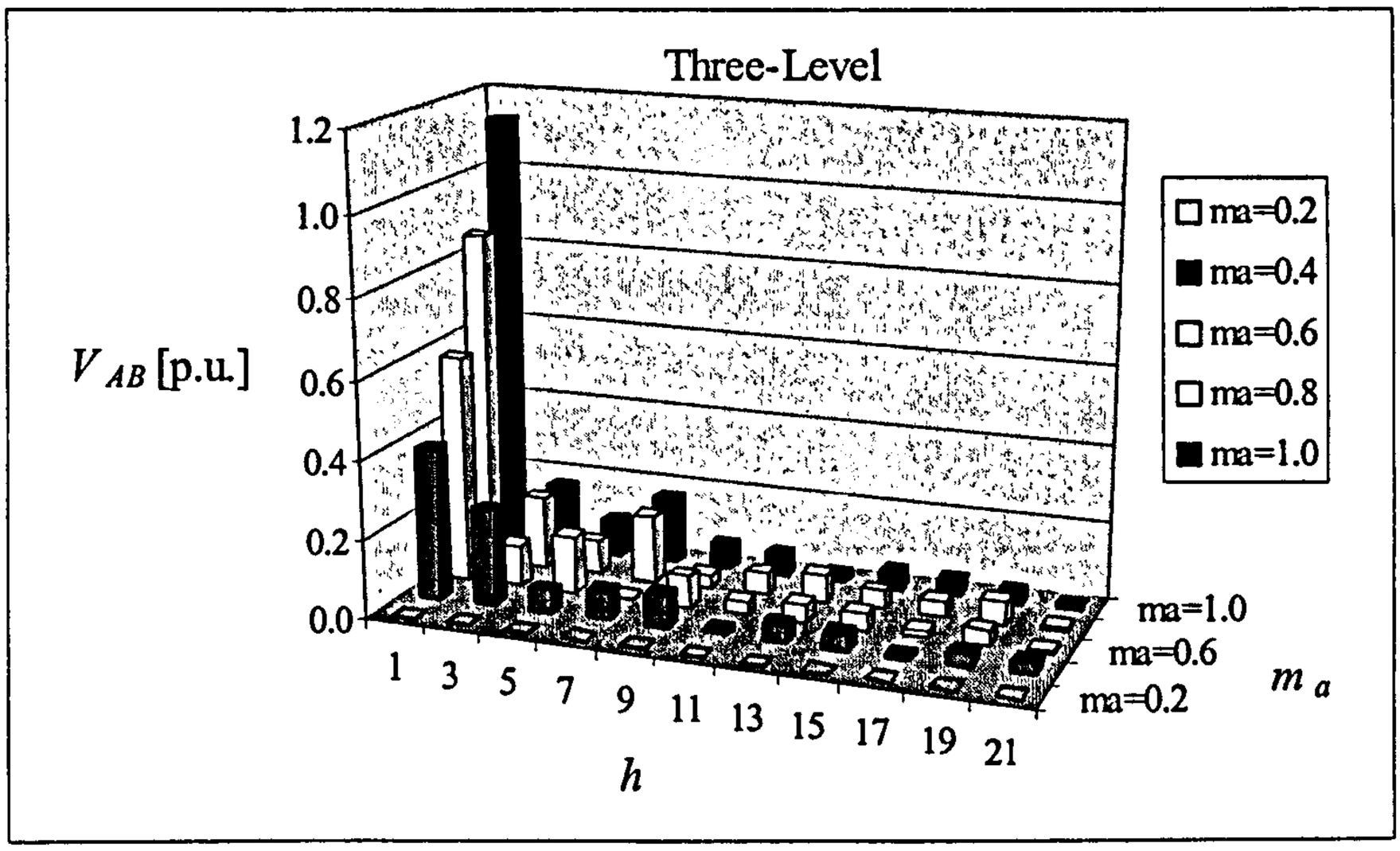


Fig. 3.12: Harmonic spectrum with different m_a for a three-level NPC using FF-SPWM.

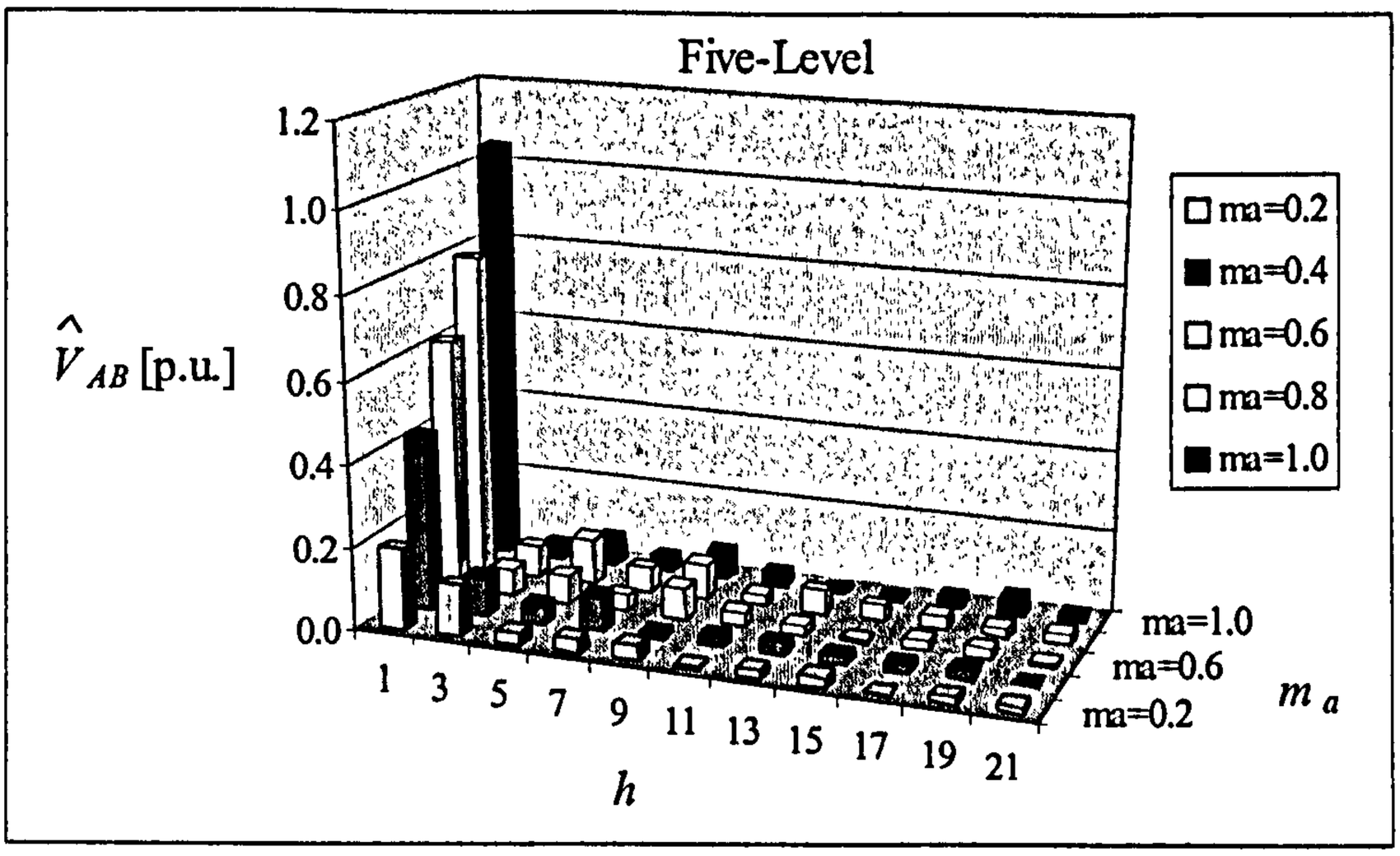


Fig. 3.13: Harmonic spectrum with different m_a for a five-level NPC using FF-SPWM.

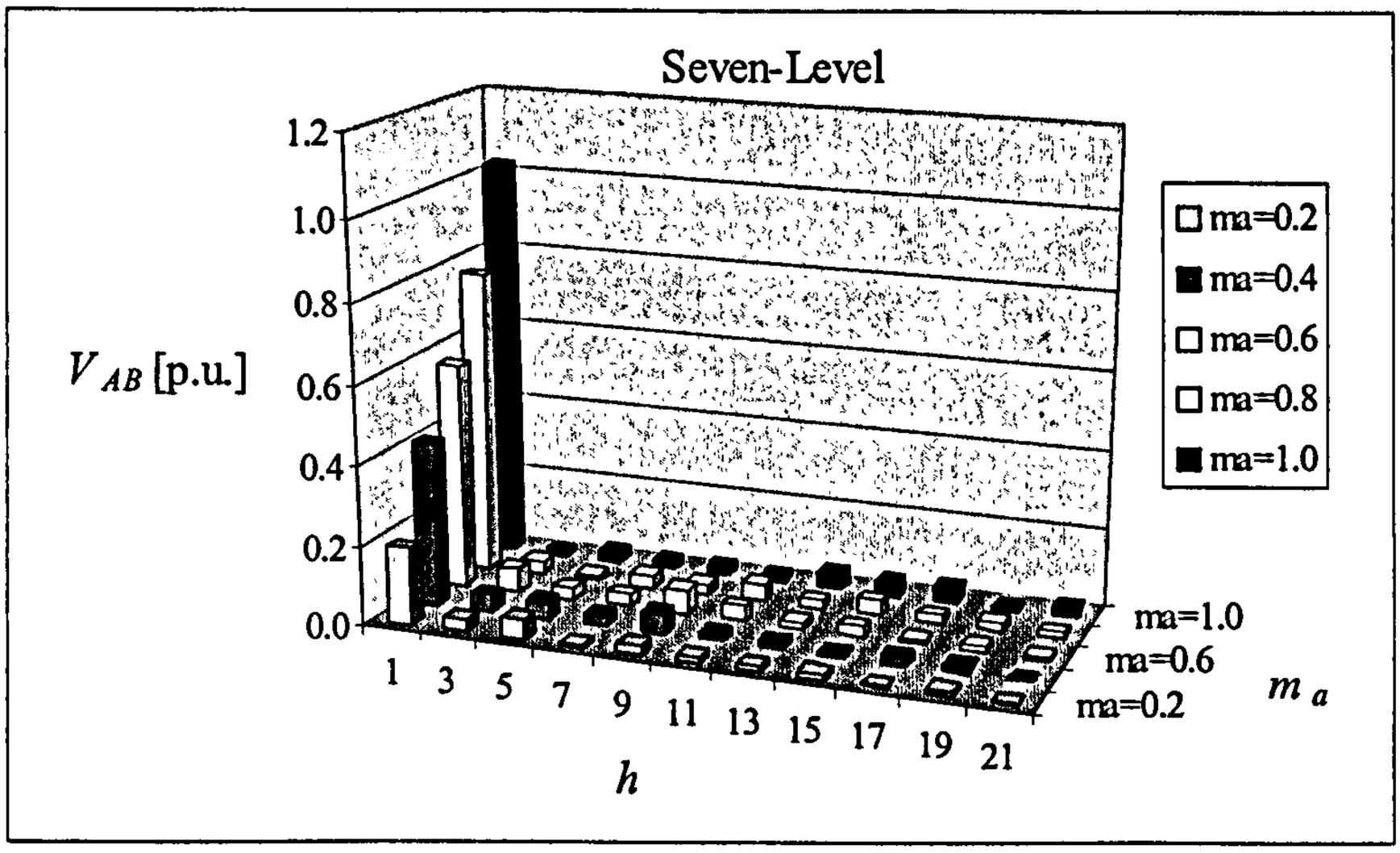


Fig. 3.14: Harmonic spectrum with different m_a for a seven-level NPC using FF-SPWM.

It is clear from Figs. 3.12 to Fig. 3.14 that the amplitude of the fundamental frequency component of the output voltage V_{AB} varies linearly with m_a (provided $m_a \leq 1$). This is the advantageous feature of the FF-SPWM method besides minimising switching losses. However, it can also be seen that the FF-SPWM method is not suitable for low m_a and low number of levels. For example, when it is applied to the three-level converter, with m_a=0.4, the line-to-line voltages include parts of the line-neutral components, thus not being able to cancel the triplen harmonics and this is considered a drawback. However, for the higher level and the higher m_a, no such a problem exists. Therefore this method only suits higher multilevel converters at high m_a.

3.5 Comparison of the FF-SPWM and High Frequency MSPWM Techniques

Different levels of NPC converters, namely, three-level, five-level, and seven-level with the PD method have been studied. For each NPC converter, with different levels, the following work is reported:

- The performance of the NPC inverter when the amplitude modulation ratio m_a remains unchanged and the frequency modulation ratio m_f changes.
- The performance of the inverter when the frequency modulation ratio m_f is unchanged, and the amplitude modulation ratio m_a changes.
- The linear behaviour of the output voltage with FF-SPWM method (when m_f=1) when m_a is changed in the range of 0.6-1.4.

Here, in order to compare the effects of the high frequency MSPWM and FF-SPWM, both based on the PD method, on the harmonic performance and switching losses respectively, two ratios a and b are defined as follows:

$$a = \frac{THD_v}{THD_{v(m_f=1)}} \tag{3-47}$$

$$b = \frac{N_{total}}{N_{total(m_f=1)}} \tag{3-48}$$

Table 3.9 and Table 3.10 summarise the simulation results for a three-phase five-level NPC and a three-phase seven-level NPC converter at m_a =0.95.

Table 3.9: Summary of results for the three-phase five-level NPC converter with the PD method at m_a=0.95, V_{dc}=12 kV, f_o =50 Hz

m_f	1	15	21	31	45	61
THD_v (%)	15.89	16.9	15.75	15.56	14.41	13.18
$\hat{V}_{AB1}$ (kV)	10.27	9.85	9.84	9.79	9.83	9.83
N_{s1}	2	10	14	20	28	40
N_{s2}	2	4	6	10	14	20
N_{s3}	2	4	6	10	14	20
N_{s4}	2	10	14	20	28	40
N_{total}	8	28	40	60	84	120
a	1	1.06	0.99	0.98	0.91	0.83
b	1	3.5	5	7.5	10.5	15

Table 3.10: Summary of results for the three-phase seven-level NPC converter with the PD method at m_a=0.95, V_{dc}=18 kV, f_o =50 Hz

m_f	1	15	21	31	45	61
THD_v (%)	13.32	10.13	10.66	10.40	9.83	8.95
$\hat{V}_{AB1}$ (kV)	14.95	14.77	14.76	14.69	14.72	14.75
N_{s1}	2	8	10	16	22	30
N_{s2}	2	4	6	8	12	16
N_{s3}	2	2	4	6	10	12
N_{s4}	2	2	4	6	10	12
N_{s5}	2	4	6	8	12	16
N_{s6}	2	8	10	16	22	30
N_{total}	12	28	40	60	88	116
a	1	0.76	0.80	0.78	0.74	0.67
b	1	2.3	3.3	5	7.3	9.7

Fig. 3.15 and Fig. 3.16 compare results for the ratios a and b using the conditions stated in Table 3.9 and Table 3.10. It should be mentioned that in both figures, 1 stands for m_f being 1, 2 for m_f being 15, 3 for m_f being 21, 4 for m_f being 31, 5 for m_f being 45, 6 for m_f being 61.

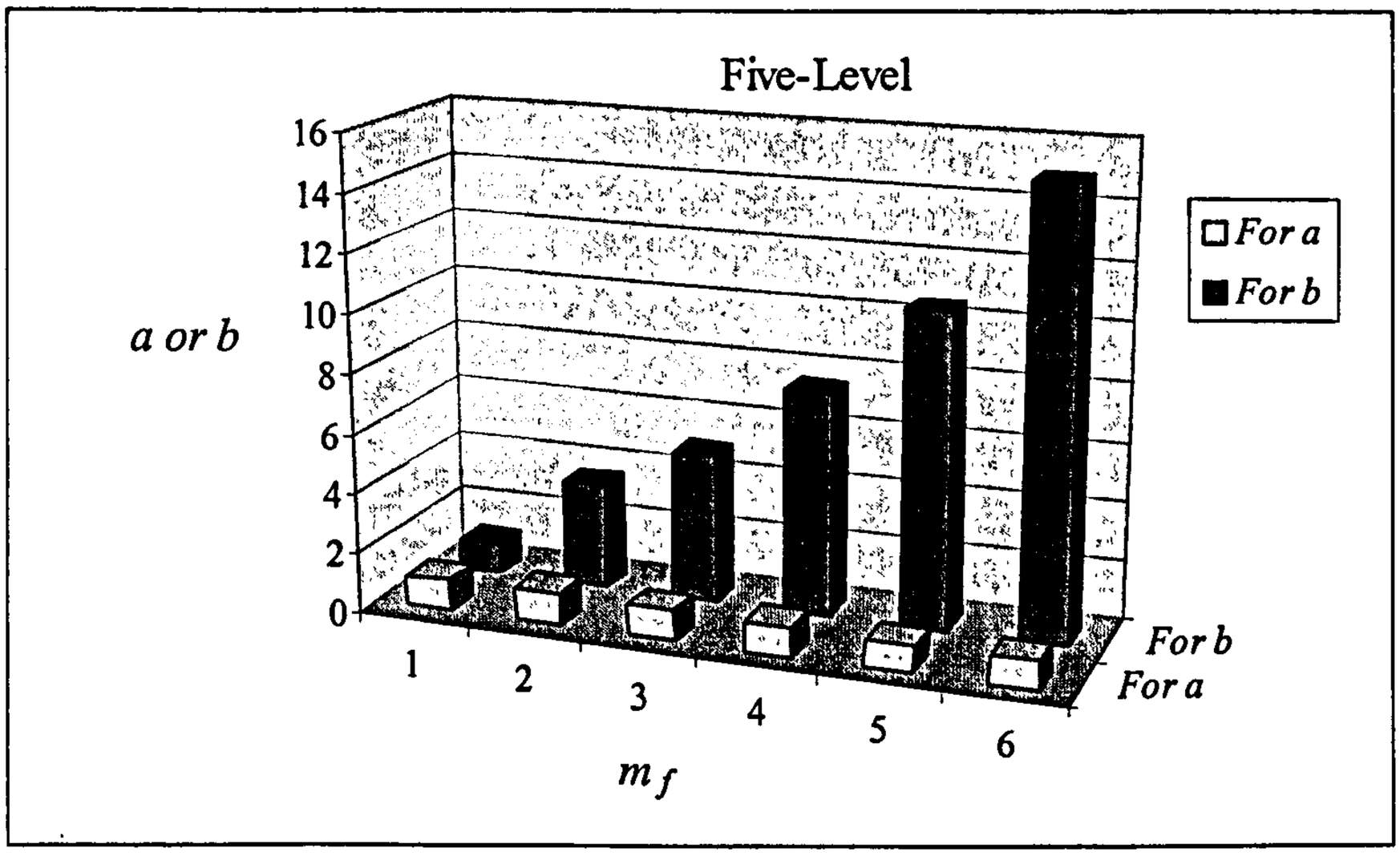


Fig. 3.15: The comparison of the effects of the high frequency MSPWM and FF-SPWM on the harmonic performance and switching losses for the five-level NPC converter at m_a=0.95, V_{dc}=12 kV, f_o =50 Hz.

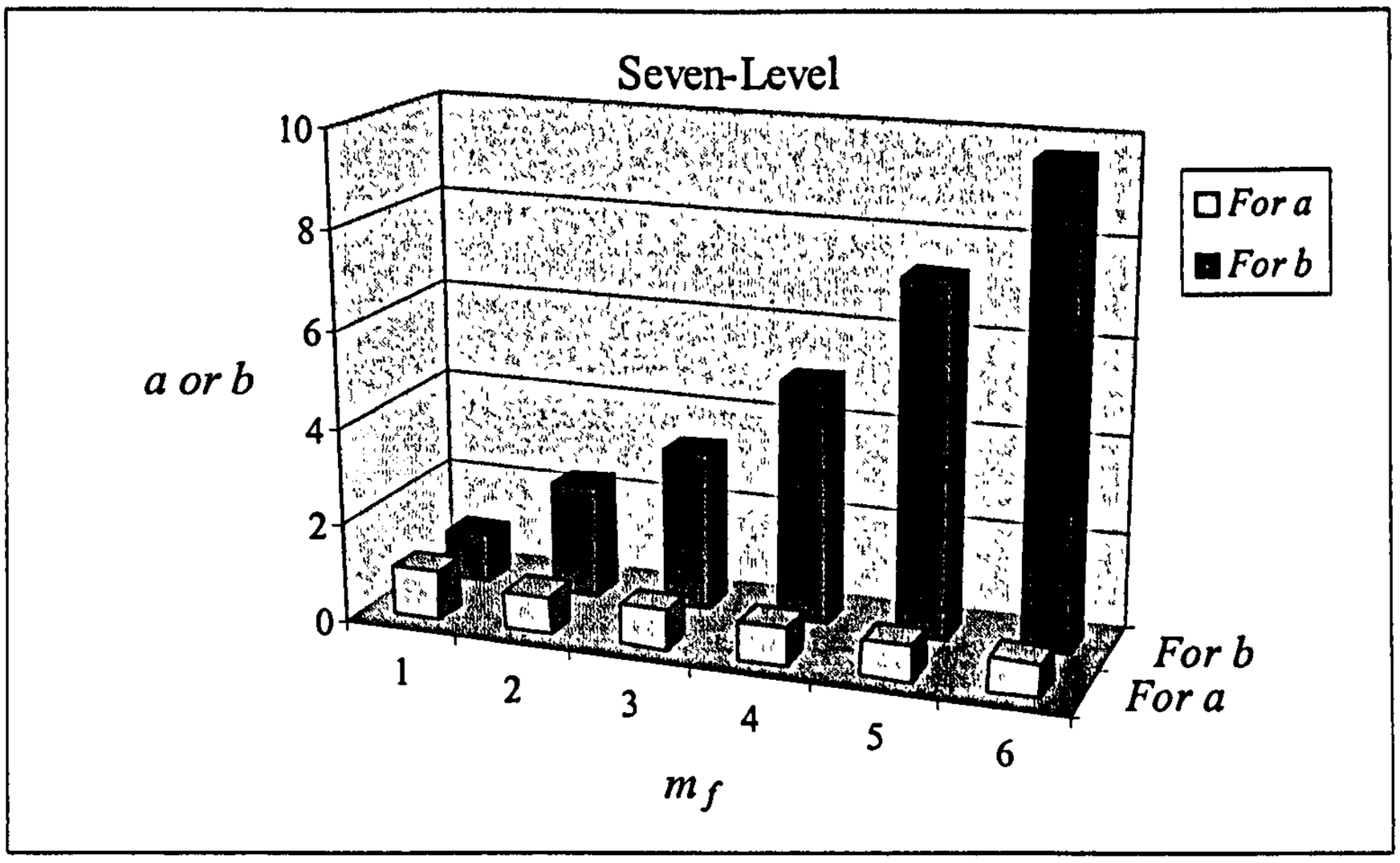


Fig. 3.16: The comparison of the effects of the high frequency MSPWM and FF-SPWM on the harmonic performance and switching losses for the seven-level NPC converter at m_a=0.95, V_{dc}=18 kV, f_o =50 Hz.

Fig. 3.17 and Fig. 3.18 depict the THD of the line-to-line voltage against m_a at different m_f for a five-level and a seven-level NPC converter respectively. Fig. 3.19 shows $\hat{V}_{AB1}$ with respect to m_a for a five-level and a seven-level NPC converter individually under the FF-SPWM control scheme to investigate the linearity. Here, $\hat{V}_{AB1}$ [p.u.] is the normalised $\hat{V}_{AB1}$ which equals the ratio of $\hat{V}_{AB1}$ to $\sqrt{3}V_{dc}/2$. Table 3.11 lists the comparison of the THD_v and the N_{total} for different voltage levels of the NPC converter at m_a =0.95.

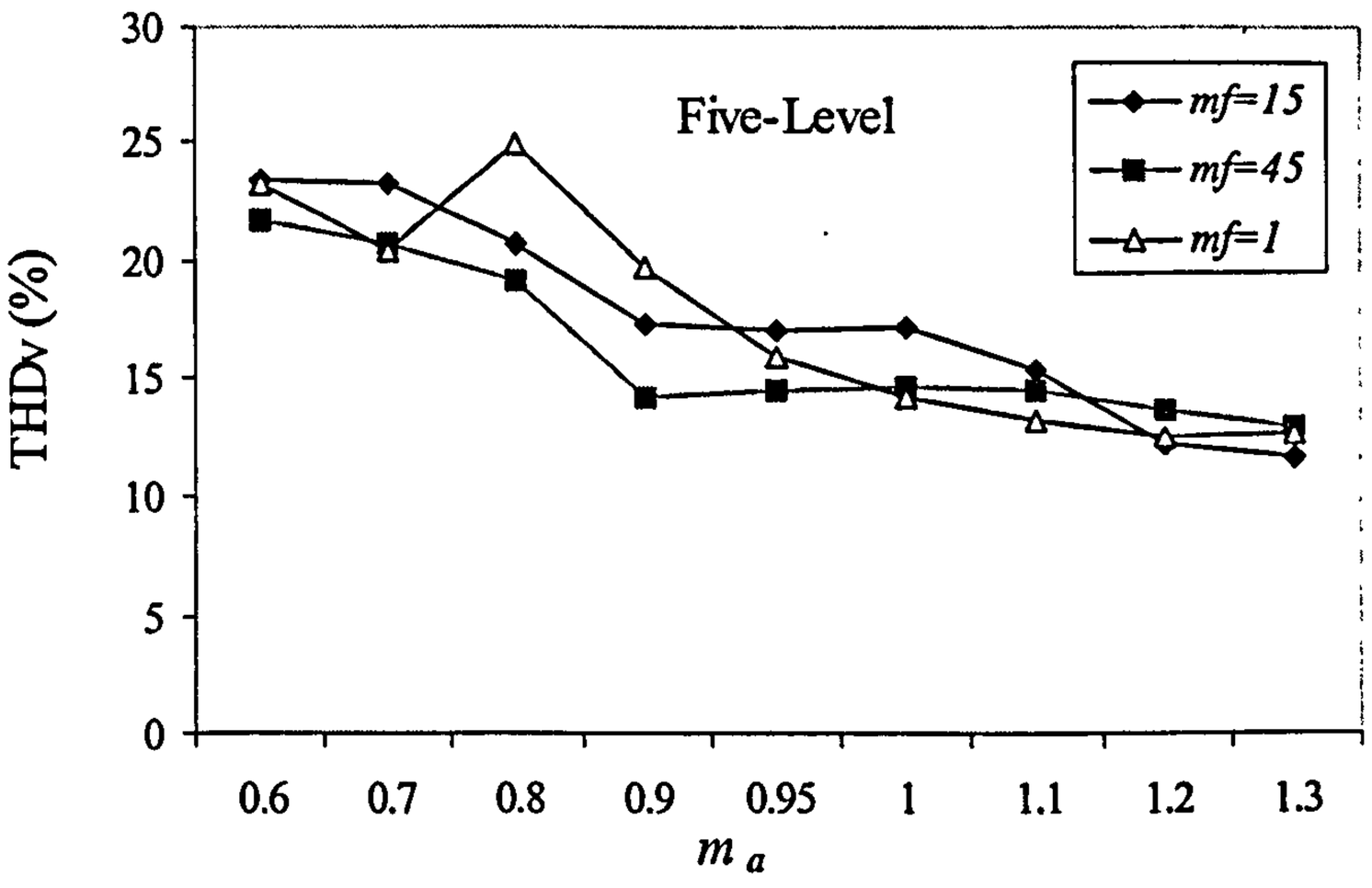


Fig. 3.17: THD_v of the five-level NPC converter against m_a for the different m_f.

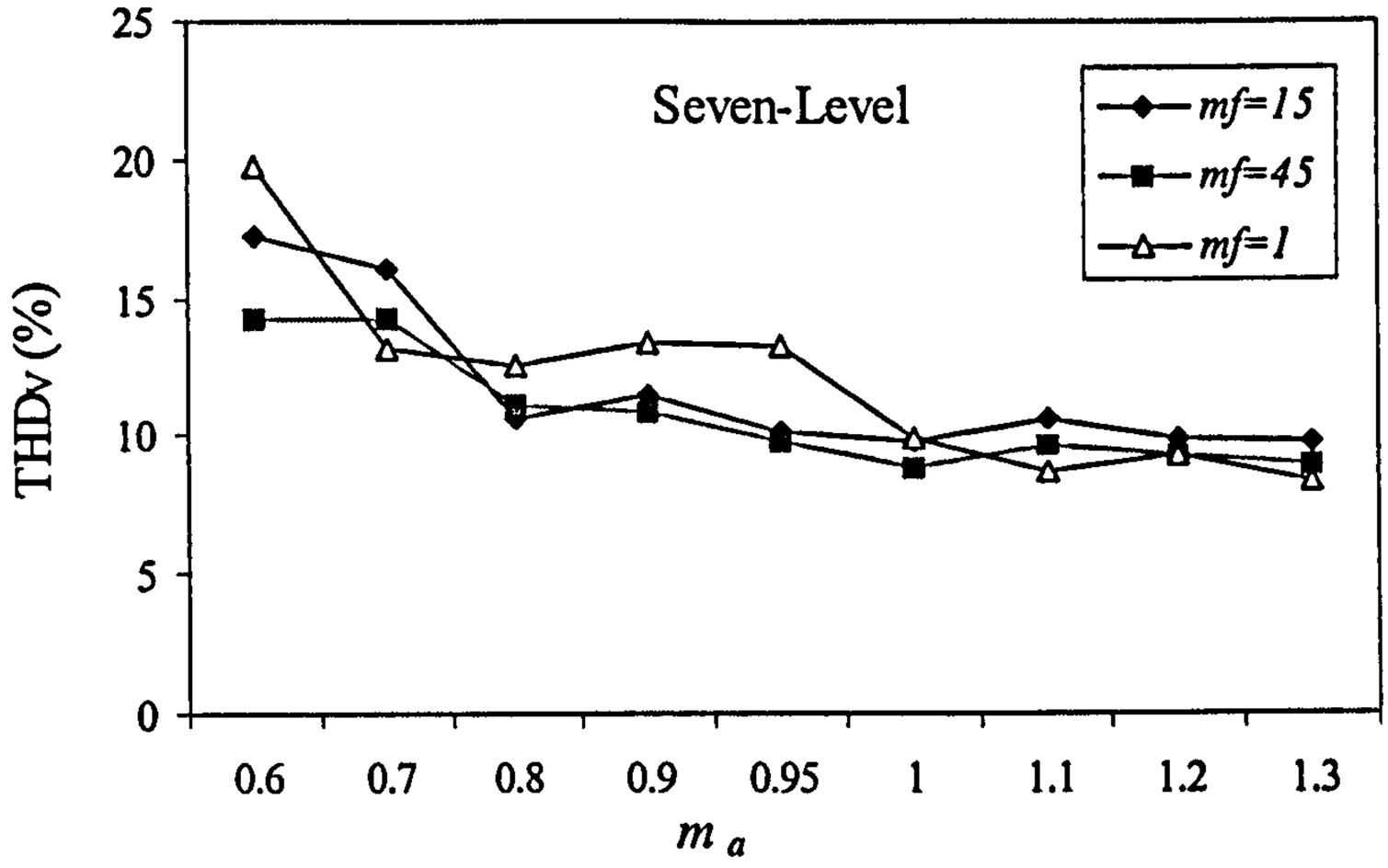


Fig. 3.18: THD_v of the seven-level NPC converter against m_a for the different m_f.

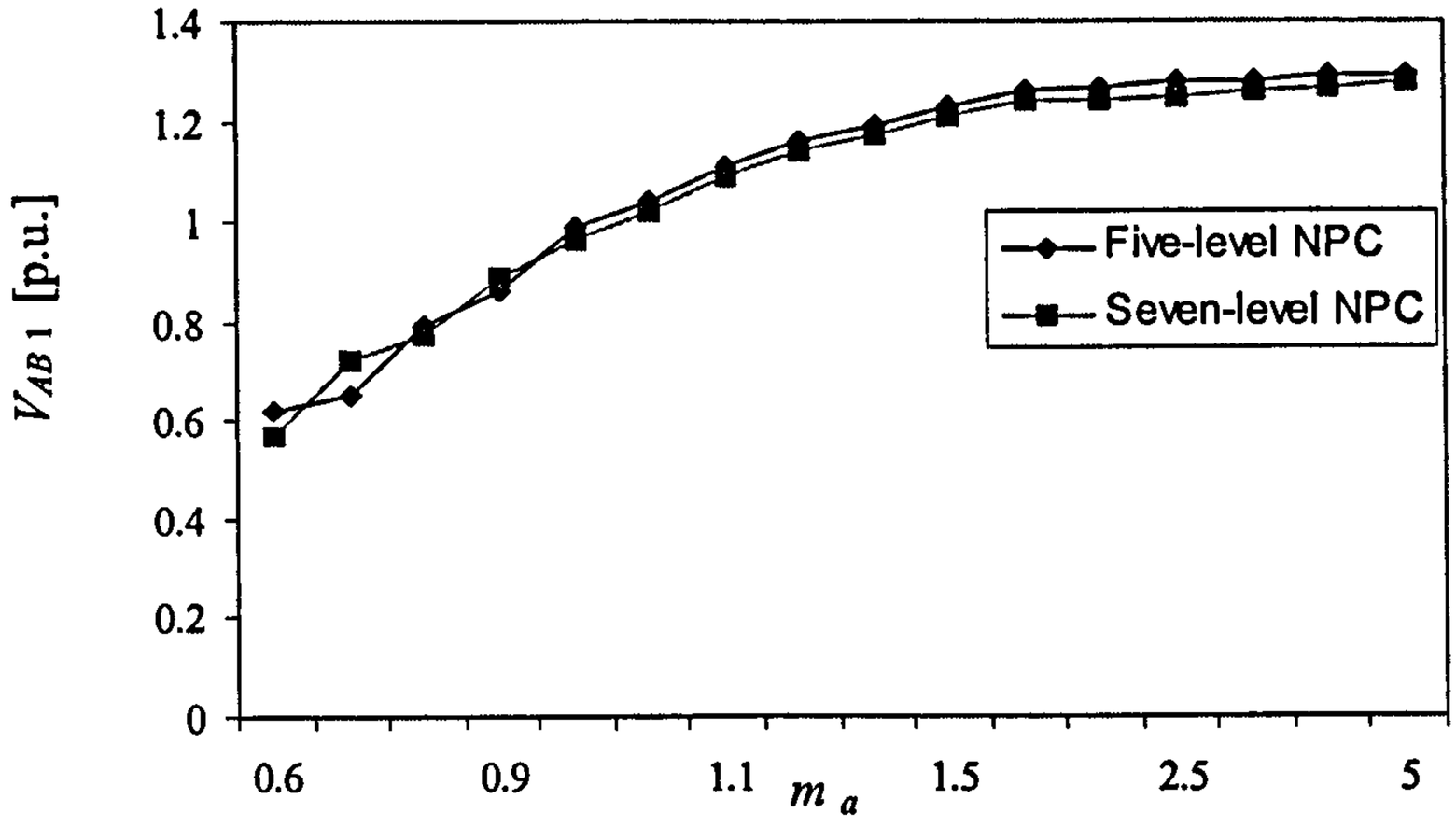


Fig. 3.19: $\hat{V}_{AB1}$ with respect to m_a for the five-level and seven-level NPC converters respectively, with the FF-SPWM method.

Table 3.11: Comparison of the THD_v and the N_{total} for different voltage levels of the NPC converter at m_a=0.95, f_o =50 Hz

m_f		Three-level	Five-level	Seven-level
1	N_{total}	4	8	12
15	N_{total}	28	28	28
45	N_{total}	88	84	88
1	THD_v (%)	27.7	15.9	13.3
15	THD_v (%)	35.8	16.9	10.1
45	THD_v (%)	32.2	14.4	9.8

It can be seen from Table 3.9, Table 3.10, Fig. 3.15 and Fig. 3.16 that as m_f increases, the harmonic content of the line-to-line output voltage decreases only slightly, but the switching losses increase much more. Fig. 3.17 and Fig. 3.18 show that THD_v decreases with the increasing number of levels, but for a fixed m_a, there is no significant effect of different m_f on the THD_v. Fig. 3.19 shows that the NPC converter has linearity under the FF-SPWM control method in the limited m_a range. It can be seen from Table 3.11 that the switching losses are related to m_f instead of the number of levels.

3.6 Discussion

Switching loss is the power dissipation during turn-on and turn-off switching transitions, which varies in proportion to switching frequency and switching times. In the high frequency PWM, switching loss can be substantial and must be considered in the converter's thermal design. It is a big drawback that results in a series of problems such as increasing the cost of the converter and decreasing its efficiency especially in high voltage and high power applications. The higher the power being processed, the more severe the effect of the switching loss becomes. Therefore, reducing the switching frequency and associated losses of multilevel PWM converters and systems is a very important design task.

Multi-carrier based PWM techniques have been investigated to find out a suitable control method that could minimise not only the harmonic content but also the switching losses. In terms of simulation results, the PD method is superior to the other two CD-MSPWM methods since it provides the lowest harmonic distortion for the line-to-line voltage and has almost equal number of total switching transitions as others. This is due to the fact that the PD method places significant harmonic energy into a carrier component for each phase leg, and relies on common mode cancellation between the inverter phase legs to eliminate this carrier energy from the line-to-line output voltage. Consequently, the harmonic sidebands (which are not fully cancelled between the phases) have less energy. This explains the improved performance of the PD strategy compared to the APOD strategy. The POD strategy is in turn better than the APOD.

For the PD implementation, the top switch of a leg is operated more often than the intermediate switch due to the different duration of time that the reference waveform exists in the different bands. With this method, N_{sn} is dependent on m_a and the switch stresses are not equal. In order to balance the number of switching actions evenly on all switches the

carrier frequency of each band may be varied based on the time duration that the reference waveform remains in the band [82].

The number of total switching transitions is used to represent the potential switching loss. It is a function of m_a, m_f and φ. It is obvious that it is related to m_a because some levels will go unused at lower m_a (for instance, m_a<0.5 in a five-level converter with the PD method). However, it is essentially related to m_f, independently of the voltage levels of the NPC converter. In other words, increasing the number of voltage levels of NPC converter does not increase the switching losses except for improving the harmonic performance when m_f is fixed (here, $m_f \neq 1$). This is summarised in Table 3.11. By choosing a phase displacement angle φ that minimises the number of active device switching for a particular m_a and m_f, switching losses can be reduced by as much as 35% [40], which increase the efficiency of the inverter considerably.

In the higher multilevel NPC inverters, the FF-SPWM control method is feasible and promising. Compared with the CD-MSPWM methods, the FF-SPWM method has many advantages. It can overcome the most significant disadvantage of the NPC topology when the CD-MSPWM methods ($m_f \neq 1$) are employed, that is, the non-equal switching frequency of the various semiconductors depending upon the amplitude modulation ratio m_a and their location with respect to the DC rail. By doing that, it equalises the switching frequency and potentially stresses all semiconductors with the same thermal load. It is confirmed that the FF-SPWM method behaves in a linear fashion in the range of $m_a \leq 1$. Thus, it can be used at higher-level systems. The alternative CD-MSPWM methods produce higher switching losses and do not necessarily result in much better harmonic performance and the techniques are not necessarily more advantageous than the simple fundamental frequency control method at higher-level converters.

However, it must be noted that FF-SPWM has quite a low THD which suggests a good current waveform only apply to the high m_a and high number of levels. This feature probably makes the FF-SPWM suitable for sinusoidal rectification, but excludes it to be used in motor drive applications. In such cases, the output must be capable of a wide frequency operating range (down to fractions of a Hertz), due to the voltage/frequency relationship of the machine, the low frequency is combined with low amplitude, which is the worst operating condition for the fundamental switching, and this leads to large distortions in the current waveform.

3.7 Conclusions

A three-phase three-level NPC converter can be modelled as a set of voltage controlled voltage sources in the AC side and current controlled current sources on the DC side at the fundamental frequency. No matter what kind of sources, all these controlled sources are related to switching functions. In theory, the mean neutral point current over a modulation cycle is zero and the neutral-point potential remains constant under normal operation (e.g., ideal circuit, balanced switching pattern and balanced load etc.).

CD-MSPWM strategies are widely used in NPC converters. Among them, the PD method is the best control method as it generates almost an equal total number of switching transitions compared with the other two methods, that is, the APOD and POD methods. Meanwhile, it produces the lowest total harmonic distortion of the line-to-line output voltage. The number of the total switching transitions representing the switching losses is related to the amplitude modulation ratio m_a and the frequency modulation ratio m_f as well as the displacement angle φ. When m_a and φ are fixed, it is determined by m_f, independently of the number of converters levels. In the higher multilevel NPC inverters, the FF-SPWM control method is feasible and promising.

Chapter 4: Flying Capacitor Converter

4.1 Introduction

The FC converter is analysed in detail in this chapter. Firstly, the principles of operation of the converter are described in Section 4.2. Secondly, the mathematical modelling of the converter is presented in Section 4.3. Issues such as average currents through the flying capacitors, the variation of the voltage and the self-balancing property of the capacitor's voltage are described with the help of mathematical equations. Thirdly, in Section 4.4, four kinds of multi-carrier based PWM techniques are presented and investigated when applied to the five-level FC converter. The focus of this work is on the effect of each PWM technique on the performance of the converter. The criteria here include the switch duty cycle, switching losses of the converter, self-balancing property for flying capacitor's voltage, and harmonic spectrum of the output line-to-line voltage. Then, simulation results based on the performance of the five-level FC converter under different PWM techniques are given in Section 4.5, followed by conclusions in Section 4.6.

4.2 Principles of Operation of the Flying Capacitor Converter

A typical phase-leg of a five-level FC converter configuration is shown in Fig. 4.1. In this circuit, two DC bus capacitors C_d are used to provide the neutral point for connection with one terminal of the load in order to make the output phase voltage V_{AO} vary between $\pm V_{dc}/2$. $C1$, $C2$ and $C3$ are termed flying capacitors because they float with respect to the DC rail (hence the term flying). They are used to provide the multilevel voltage ability to the converter. Before the FC converter is put into normal operation, the flying capacitors $C1$, $C2$ and $C3$ have to be charged to $3V_{dc}/4$, $V_{dc}/2$, $V_{dc}/4$, respectively. As a consequence, the voltage stress across any switch in this circuit equals $V_{dc}/4$. Eight switches are grouped into four complementary pairs: (S_{a1}, S_{a8}), (S_{a2}, S_{a7}), (S_{a3}, S_{a6}) and (S_{a4}, S_{a5}) respectively. Complementary switch pair means one being on while another being off, and vice versa. Considering that there exist complementary switch pairs in each leg, only the main upper four switches are given in all figures and tables in this chapter.

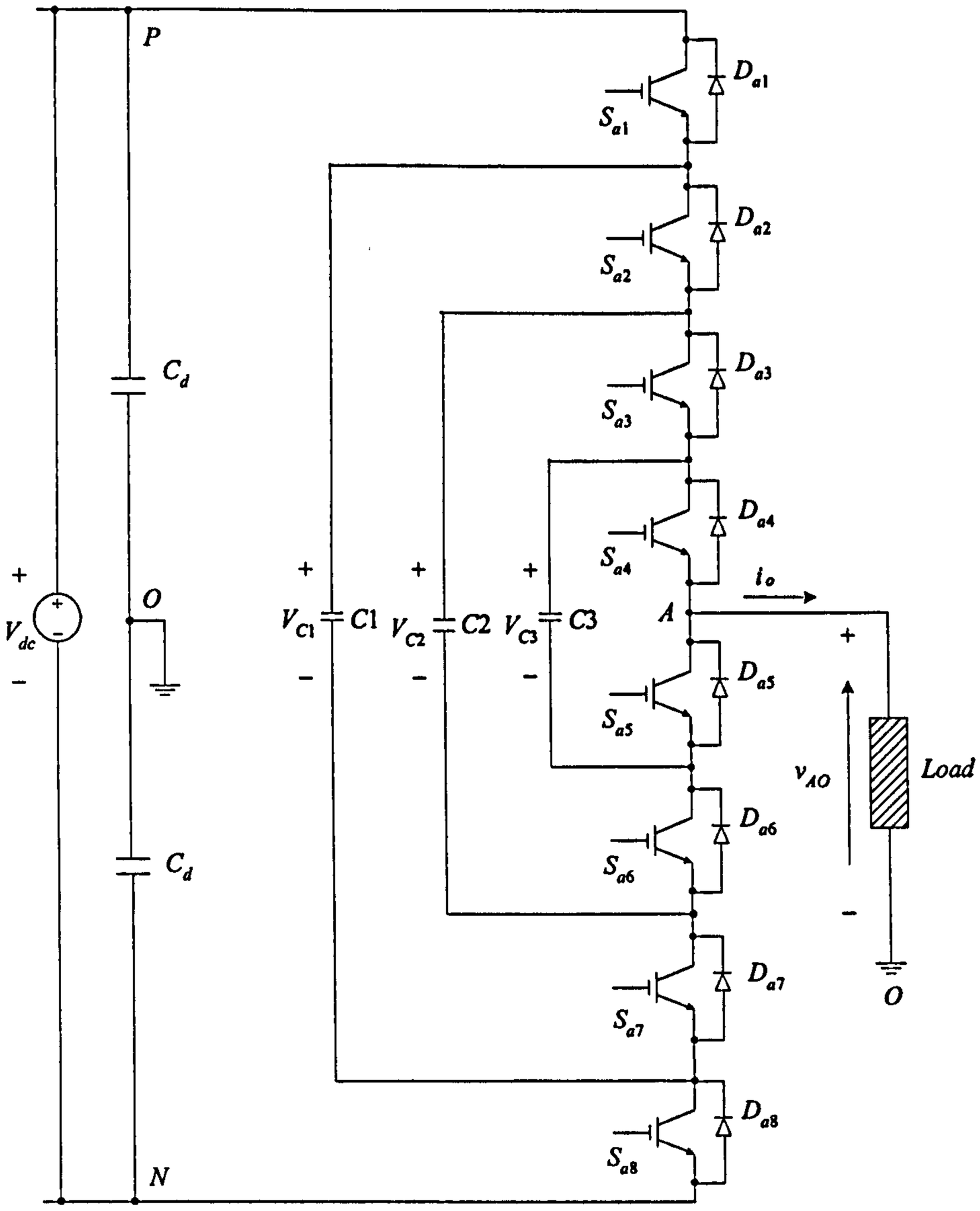


Fig. 4.1: A typical five-level FC converter leg.

Due to the structure of this circuit, five different voltage levels at each phase with respect to the neutral-point can be synthesised as follows:

(1) Voltage $+V_{dc}/2$:

Switching state: 1111;

(2) Voltage $+V_{dc}/4$:

a) Switching state: 1110; $V_{AO} = \frac{V_{dc}}{2} - V_{C3}$

b) Switching state: 1101; $V_{AO} = \frac{V_{dc}}{2} - V_{C2} + V_{C3}$

c) Switching state: 1011; $V_{AO} = \frac{V_{dc}}{2} - V_{C1} + V_{C2}$

d) Switching state: 0111; $V_{AO} = V_{C1} - \frac{V_{dc}}{2}$

(3) Voltage 0:

a) Switching state: 1100; $V_{AO} = \frac{V_{dc}}{2} - V_{C2}$

b) Switching state: 1010; $V_{AO} = \frac{V_{dc}}{2} - V_{C1} + V_{C2}$

c) Switching state: 0110; $V_{AO} = V_{C1} - V_{C3} - \frac{V_{dc}}{2}$

d) Switching state: 1001; $V_{AO} = \frac{V_{dc}}{2} - V_{C1} + V_{C3}$

e) Switching state: 0101; $V_{AO} = V_{C1} - V_{C2} + V_{C3}$

f) Switching state: 0011; $V_{AO} = V_{C2} - \frac{V_{dc}}{2}$

(4) Voltage -V_{dc}/4:

a) Switching state: 1000; $V_{AO} = \frac{V_{dc}}{2} - V_{C1}$

b) Switching state: 0100; $V_{AO} = V_{C1} - V_{C2} - \frac{V_{dc}}{2}$

c) Switching state: 0010; $V_{AO} = V_{C2} - V_{C3} - \frac{V_{dc}}{2}$

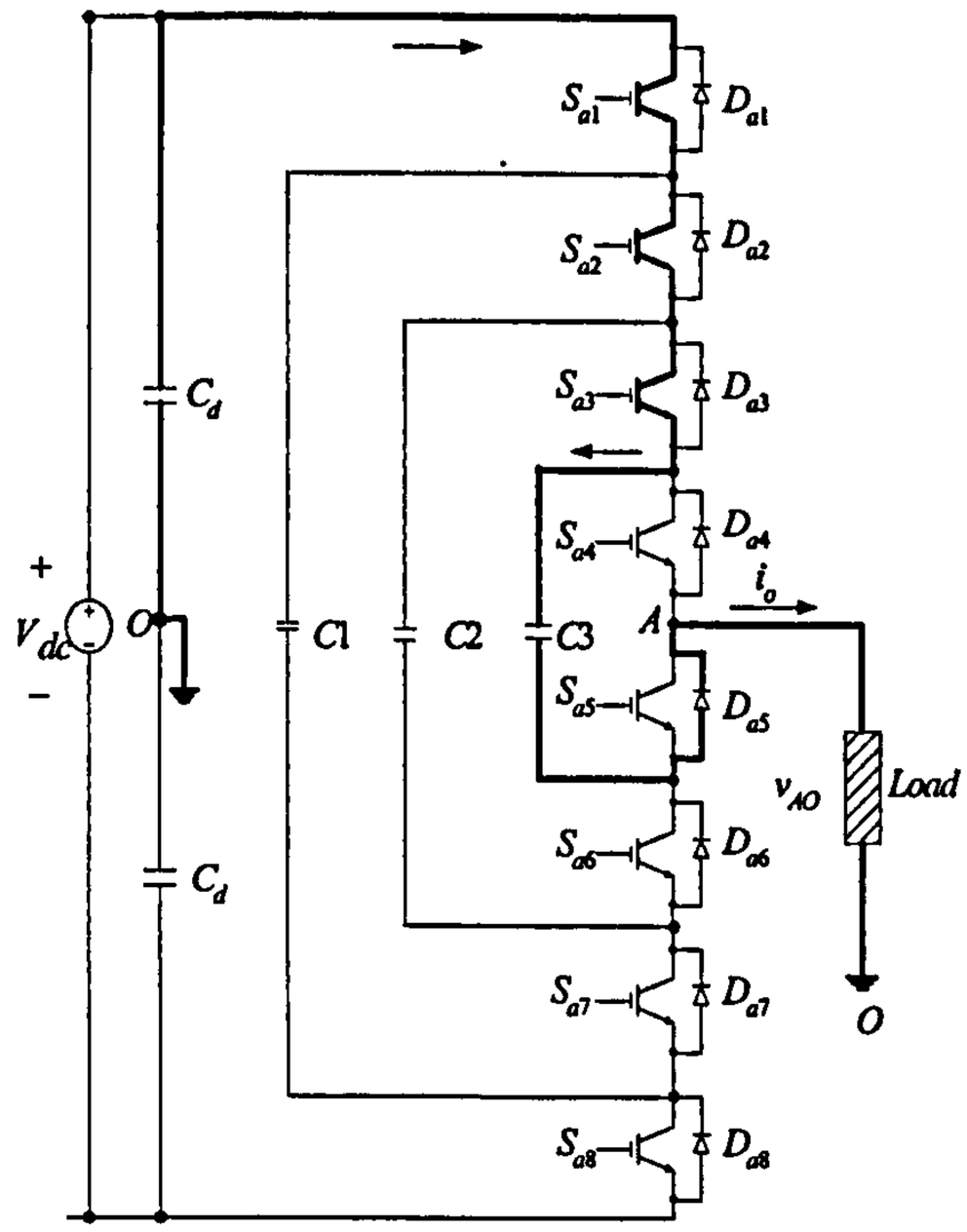
d) Switching state: 0001; $V_{AO} = V_{C3} - \frac{V_{dc}}{2}$

(5) Voltage -V_{dc}/2:

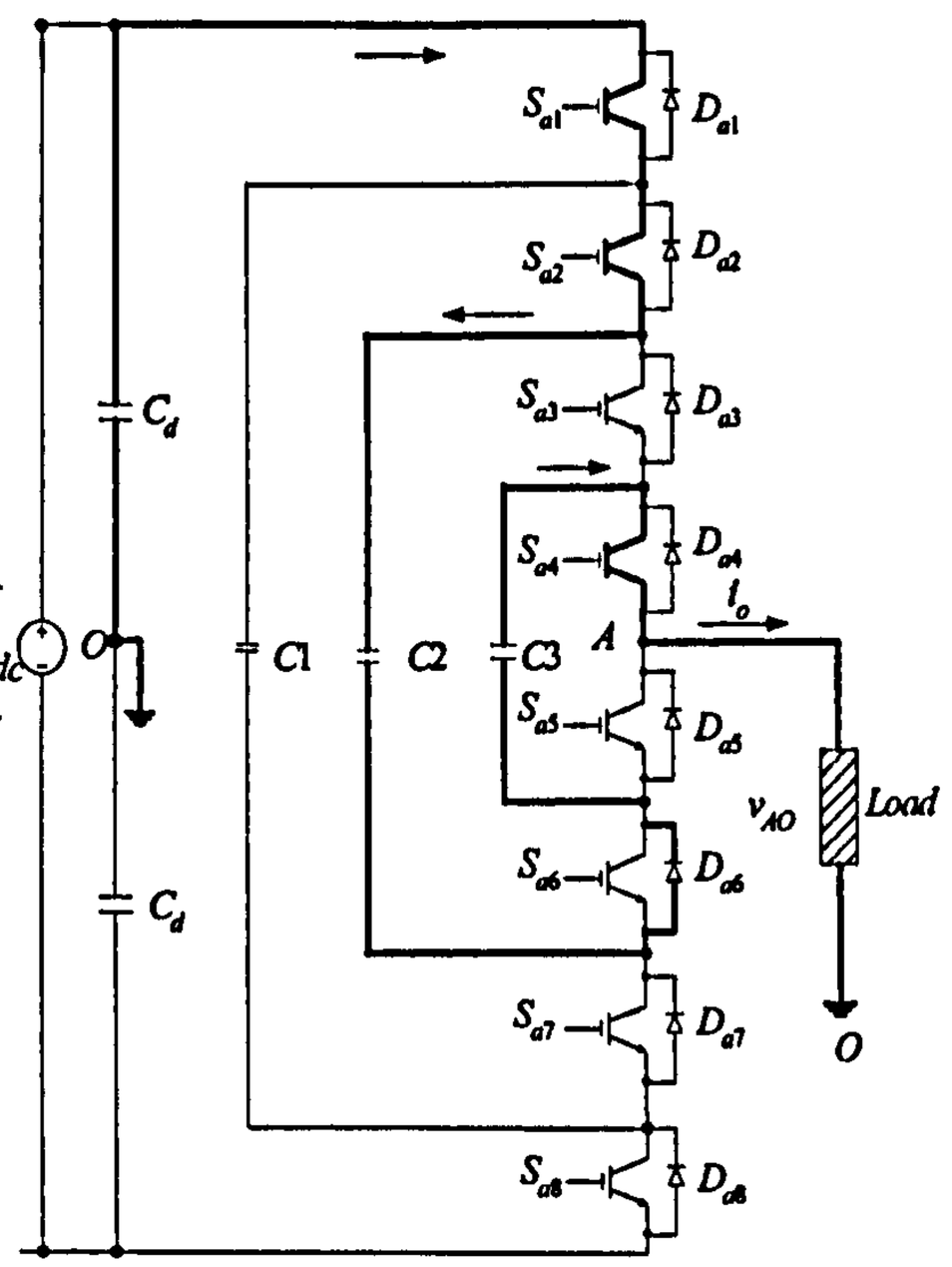
Switching state: 0000;

Here, the switching state 1111 refers to all the upper four switches $S_{a1}S_{a2}S_{a3}S_{a4}$ being on, while switching state 1110 indicates that $S_{a1}S_{a2}S_{a3}$ are on and S_{a4} is off. Its definition refers to Table 4.1. Fig. 4.2 shows the current paths for some switching states which produce the same output voltage $+V_{dc}/4$ at $i_o>0$. In the whole thesis, the current flowing from the DC side to the AC side is taken to be positive. Fig. 4.2 (a) displays the current path at 1110 switching state; (b) at 1101; (c) at 1011; and (d) at 0111. As with the negative load current, the path through which it flows is the same as that of positive load current except for opposite flowing direction.

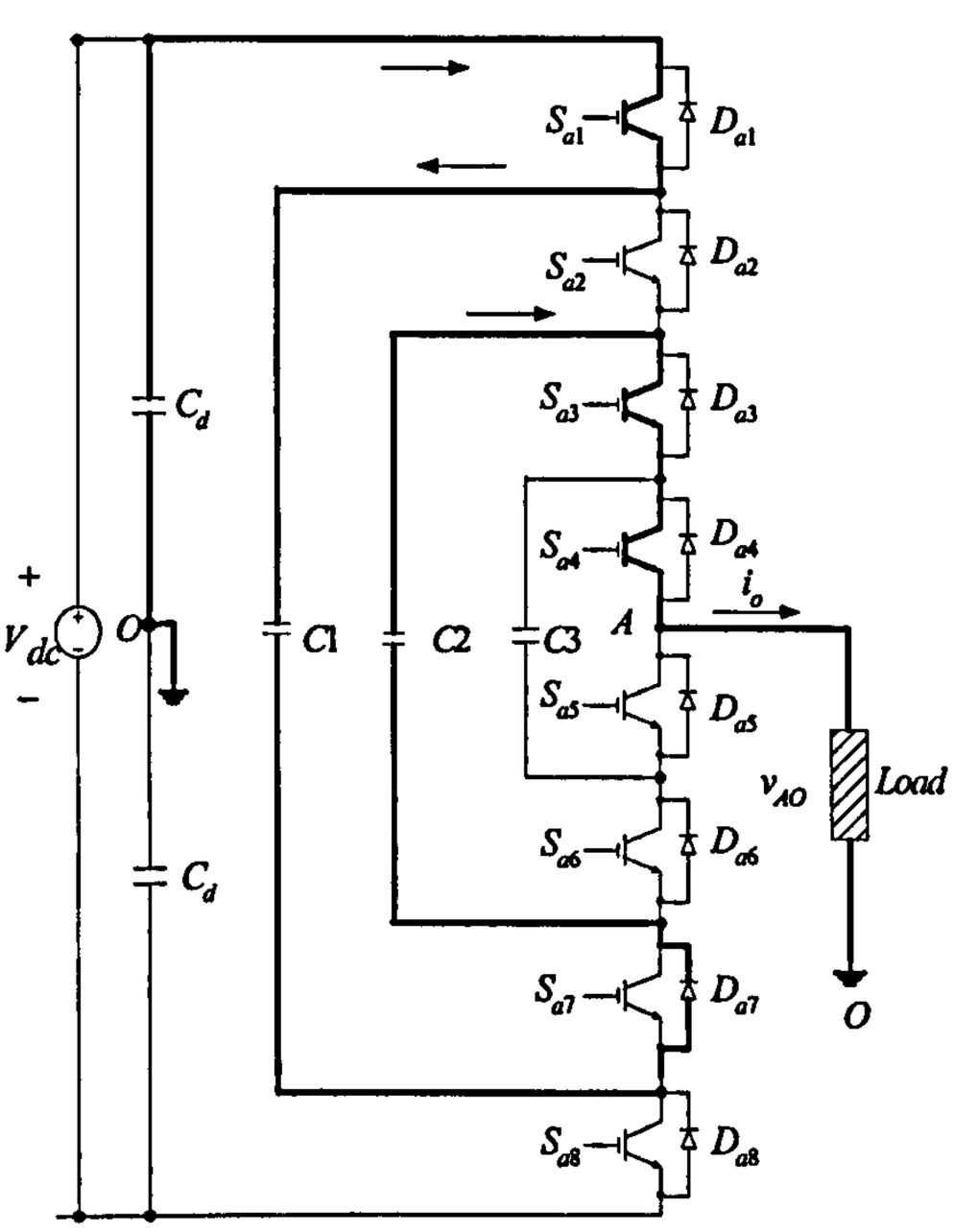
It can be seen from Fig. 4.1 and Fig. 4.2 that for a given voltage level there are several switching states (also referred to as switching redundancy) that give the same output voltage, but have different effect with respect to the charging and discharging of the flying capacitors. Table 4.1 lists all the possible switch states of a five-level FC converter, the phase output voltage level and the charging and discharging modes of each flying capacitor. The load is assumed to be inductive and the current is positive.



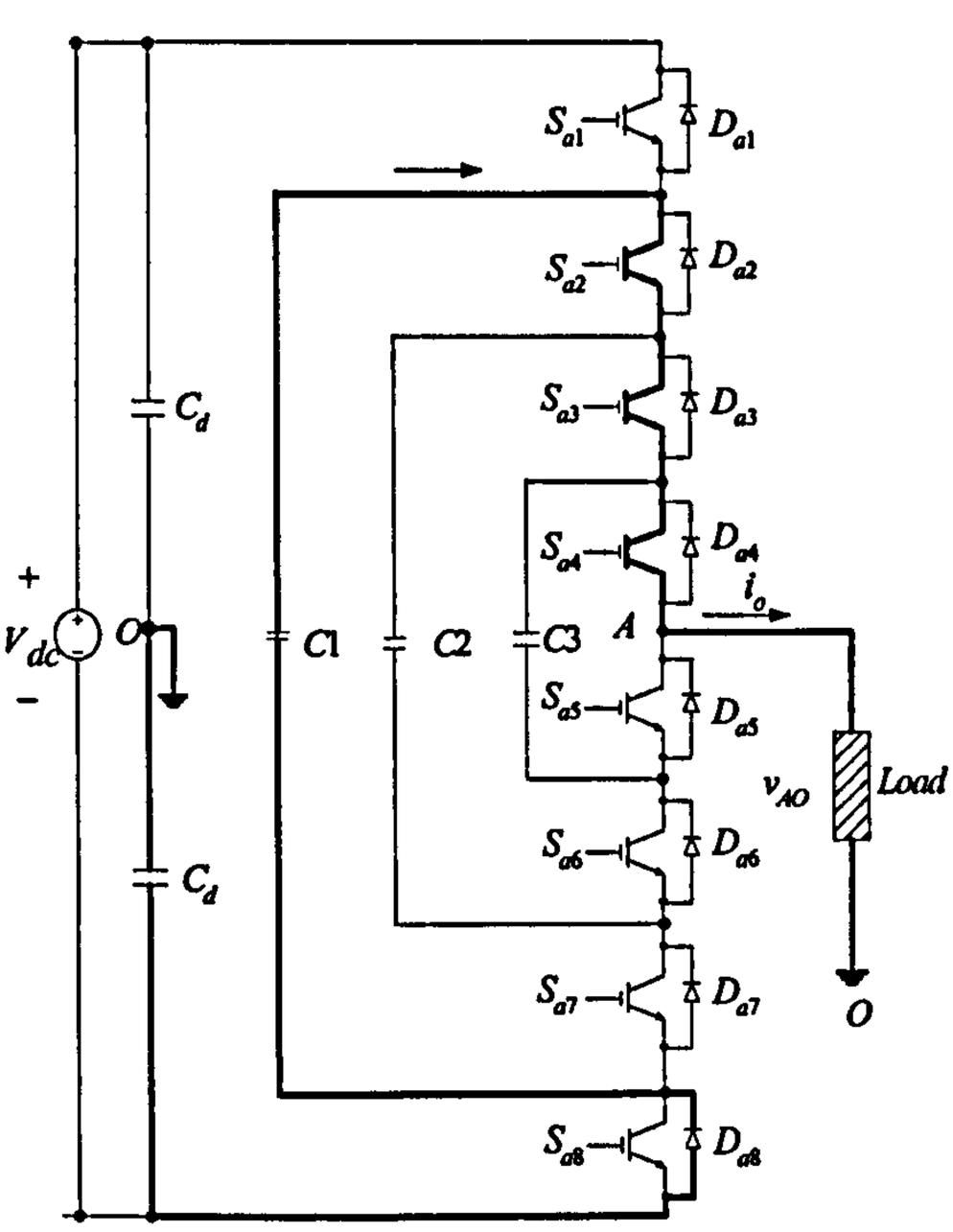
(a)



(b)



(c)



(d)

Fig. 4.2: Current paths in the five-level FC converter at $v_{AO}= +V_{dc}/4$, $i_o>0$. (a) Current path at switching state 1110. (b) Current path at 1101. (c) Current path at 1011. (d) Current path at 0111.

Table 4.1: Five-level FC converter phase voltage levels, switch states, and the charging/discharging modes of flying capacitors (i_o>0)

V_{AO}	Switch State					Capacitor Charging Mode		
	S_{a1}	S_{a2}	S_{a3}	S_{a4}	Symbol	$C1$	$C2$	$C3$
$V_{dc}/2$	1	1	1	1	4	N	N	N
$V_{dc}/4$	1	1	1	0	3_4	N	N	+
	1	1	0	1	3_3	N	+	-
	1	0	1	1	3_2	+	-	N
	0	1	1	1	3_1	-	N	N
0	1	1	0	0	2_6	N	+	N
	1	0	1	0	2_5	+	-	+
	0	1	1	0	2_4	-	N	+
	1	0	0	1	2_3	+	N	-
	0	1	0	1	2_2	-	+	-
	0	0	1	1	2_1	N	-	N
$-V_{dc}/4$	1	0	0	0	1_4	+	N	N
	0	1	0	0	1_3	-	+	N
	0	0	1	0	1_2	N	-	+
	0	0	0	1	1_1	N	N	-
$-V_{dc}/2$	0	0	0	0	0	N	N	N

In Table 4.1, 1 stands for switching on, 0 stands for switching off, sign of + refers to charging mode, sign of – means discharging mode and the label N is for no charging or discharging. When compared with the NPC topology, the FC converter has more switching combinations for a given voltage level. It can be seen from Table 4.1 that the five-level FC converter has 16 switching states for the upper four switches. Among them, four switching states represent the same phase voltage of $V_{dc}/4$, six switching states for 0, and four for -$V_{dc}/4$. This switching redundancy can be used to balance different voltage levels. For example, when the load current is positive, the switching state 3_4 charges the flying capacitor $C3$, while the switching state 1_1 discharges the flying capacitor $C3$. If the on time of all the complementary switching states is the same in the period, the amount of change in the capacitor voltage can be controlled to a zero average, thus solving the voltage unbalance problem of FC converter. This is the main advantage of the FC topology. However, a large number of storage capacitors are required for this topology, causing packaging problems, increasing its size. This is a disadvantage of the FC converter.

4.3 Modelling of the Flying Capacitor Converter

Fig. 4.3 shows an equivalent circuit of the (p+1) level FC topology leg which is composed of p pairs of switches and (p-1) capacitors. Here, the load side is represented by a current source I and the DC side is represented by a voltage source E. The switches are arranged in pairs (A_k, B_k). In this kind of multilevel converter, the flying capacitor's voltage is set to:

$$V_{Ck} = k \cdot \frac{E}{p} \tag{4-1}$$

where, k=1,2, …p, and V_{Cp}=E.

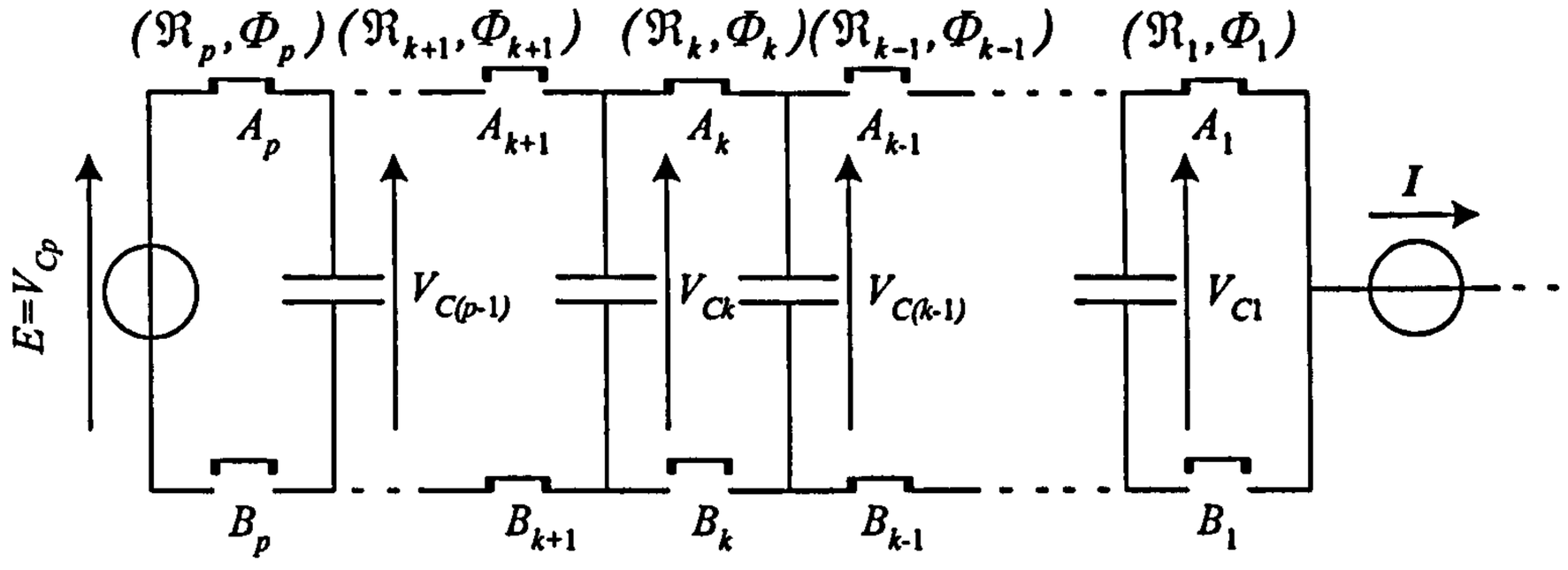


Fig. 4.3: Equivalent circuit of the *(p+1)* level FC topology.

4.3.1 Average Current through the Floating Capacitor

The instantaneous current in each switch is equal to the current in the current source when the switch is conducting and zero when the switch is blocking. So, if the current source can be taken as constant over a switching period, the average current in a switch is given by:

$$I_{kavg} = \Re_k \cdot I \tag{4-2}$$

$\Re_k$ is the duty cycle of switch k. This implies that the average current in each flying capacitor is:

$$I_{Ckavg} = (\Re_{k+1} - \Re_k) \cdot I \tag{4-3}$$

Obviously, as long as the duty cycles are equal, the DC component has no influence on the capacitors' voltages. Consequently, imposing equal duty cycles to all cells is sufficient to cancel the average current in these capacitors and keep their voltages constant.

4.3.2 Variation of the Flying Capacitor's Voltage

Since the safe operation of a multilevel converter may depend on the voltage distribution, it is very important to check the stability of this voltage distribution, i.e., determine

whether the system is capable of compensating for small (or even large) perturbations around the balanced point of operation. For this reason, the following model based on harmonics is made [20]. First of all, the following assumptions are made for the modelling presented in this section:

- The switches are ideal implying that the on-state voltage, off-state current, delays, switching times and dead-times are all considered to be zero.
- The floating capacitors are designed to limit the variations of the voltage applied to each commutation cell; in the first part of the calculation, these voltages are taken as being constant over a switching period. In the same way, the variations of voltage source are supposed to be slow compared with the switching period.
- The load has a time constant which is less than the switching period so that at each switching period, the load current is assumed to be constant.

The phase voltage V_{AN} is the sum of the voltages across the switches of the lower branch. Since the voltage across the k-th switch is zero when conducting and $V_{Ck} - V_{C(k-1)}$ when blocking (true for k=1, 2,...p with V_{C0}=E, V_{Cp}=E), V_{AN}^n , the n-th harmonic of V_{AN} is:

$$V_{AN}^n = \sum_{k=1}^{p} \frac{2}{n \cdot \pi} \cdot sin(n \cdot \pi \cdot \Re_k) \cdot (V_{Ck} - V_{C(k-1)}) \cdot e^{j \cdot n \cdot \phi_k} \tag{4-4}$$

Taking
$$G_k^n = \frac{1}{n \cdot \pi} \cdot sin(n \cdot \pi \cdot \Re_k) \cdot e^{j \cdot n \cdot \phi_k} \tag{4-5}$$

Eq. (4-4) can be written in the matrix form

$$V_{AN}^n = 2 \cdot \left[G_1^n - G_2^n ... G_{p-1}^n - G_p^n\right] \cdot \left[V_{C1} ... V_{C(p-1)}\right]^T + 2 \cdot G_p^n \cdot E \tag{4-6}$$

The load current can then be written as a function of the impedance at this frequency:

$$I^n = \frac{V_{AN}^n}{Z^n} = \left|I^n\right| \cdot e^{j \cdot n \cdot \psi^n} \tag{4-7}$$

This harmonic current generates a current through A_k that depends on duty cycle $\Re_k$ and phase shift $n \cdot \phi_k - \psi^n$. The contribution of this current harmonic to the average current in the switch is:

$$I_{Ak}^n = \frac{1}{2\pi} \cdot \int_{\phi_k - \Re_k \cdot \pi}^{\phi_k + \Re_k \cdot \pi} \left|I^n\right| \cdot cos(n \cdot \theta + \psi^n) \cdot d\theta \tag{4-8}$$

which yields

$$I_{Ak}^n = \frac{\left|I^n\right|}{n \cdot \pi} \cdot \sin(n \cdot \pi \cdot \Re_k) \cdot \cos(n \cdot \phi_k - \psi^n) \tag{4-9}$$

This quantity can be written as:

$$I_{Ak}^{n} = \mathrm{Re}\left(\frac{1}{n\cdot\pi}\cdot\sin(n\cdot\pi\cdot\Re_k)\cdot e^{-j\cdot n\cdot\phi_k}\cdot\left|I^{n}\right|\cdot e^{j\psi^{n}}\right) \tag{4-10}$$

Which, according to G_k^n defined by eq.(4-5), can be calculated by

$$I_{Ak}^{n} = Re(\mathrm{conj}(G_k^n)\cdot I^n) \tag{4-11}$$

Since
$$\dot{V}_{Ck}^{n} = \frac{1}{C_k}\cdot I_{Ck}^{n} = \frac{1}{C_k}\cdot(I_{A(k+1)}^{n} - I_{Ak}^{n}) \tag{4-12}$$

Then, we have the following matrix formulation:

$$\begin{bmatrix}\dot{V}_{C1}\\ .\\ .\\ .\\ \dot{V}_{C(p-1)}\end{bmatrix} = Re\left(\begin{bmatrix}\frac{1}{C_1}\cdot\mathrm{conj}(G_2^n - G_1^n)\\ .\\ .\\ .\\ \frac{1}{C_{p-1}}\cdot\mathrm{conj}(G_p^n - G_{p-1}^n)\end{bmatrix}\cdot I^n\right) \tag{4-13}$$

In addition, from eq.(4-6), eq.(4-7), and eq.(4-13), we have:

$$[\dot{V}_{Ck}] = 2\cdot Re\left(\begin{bmatrix}.\\ .\\ \frac{1}{C_k}\cdot\mathrm{conj}(G_{k+1}^n - G_k^n)\\ .\\ .\end{bmatrix}\cdot\frac{1}{Z^n}\cdot\left(\begin{bmatrix}. & . & G_k^n - G_{k+1}^n & . & .\end{bmatrix}\cdot[V_{Ck}] + G_p^n\cdot E\right)\right) \tag{4-14}$$

Since X and E are real, this equation can be written in standard form $\dot{X} = A\cdot X + B\cdot E$ with

$$A = 2\cdot Re\left(\begin{bmatrix}.\\ .\\ \frac{1}{C_k}\cdot\mathrm{conj}(G_{k+1}^n - G_k^n)\\ .\\ .\end{bmatrix}\cdot\frac{1}{Z^n}\cdot\begin{bmatrix}. & . & G_k^n - G_{k+1}^n & . & .\end{bmatrix}\right) \tag{4-15}$$

$$B = 2\cdot Re\left(\begin{bmatrix}.\\ .\\ \frac{1}{C_k}\cdot\mathrm{conj}(G_{k+1}^n - G_k^n)\\ .\\ .\end{bmatrix}\cdot\frac{1}{Z^n}\cdot G_p^n\right) \tag{4-16}$$

4.3.3 Calculation of the Model Taking into Account the First h Harmonics

Taking several harmonics into account, eq.(4-14) becomes:

$$\left[\dot{V}_{Ck}\right]=\sum_{n=1}^{h}2\cdot Re\left(\begin{bmatrix}\cdot\\ \cdot\\ \frac{1}{C_k}\cdot \mathrm{conj}(G_{k+1}^{n}-G_{k}^{n})\\ \cdot\\ \cdot\end{bmatrix}\cdot\frac{1}{Z^{n}}\cdot\begin{bmatrix}\cdot & \cdot & G_{k}^{n}-G_{k+1}^{n} & \cdot & \cdot\end{bmatrix}\cdot\left[V_{Ck}\right]+G_{p}^{n}\cdot E\right) \qquad (4\text{-}17)$$

4.3.4 Self-Balancing Property of the Flying Capacitor's Voltage

With this model it is very easy to determine the steady-state voltages

$$\dot{X}=0\Rightarrow X_{p}=-A(\Re)^{-1}*B(\Re)\cdot E \qquad (4\text{-}18)$$

So, the model can be readily used to demonstrate the natural balancing property (with equal duty cycles, the only stable point is $V_{Ck}=k\cdot E/p$). With this model, it can be seen that the transient behaviour of FC converter depends on the current harmonics and their phase shift with the different control signals.

4.4 Multi-Carrier Based PWM Techniques

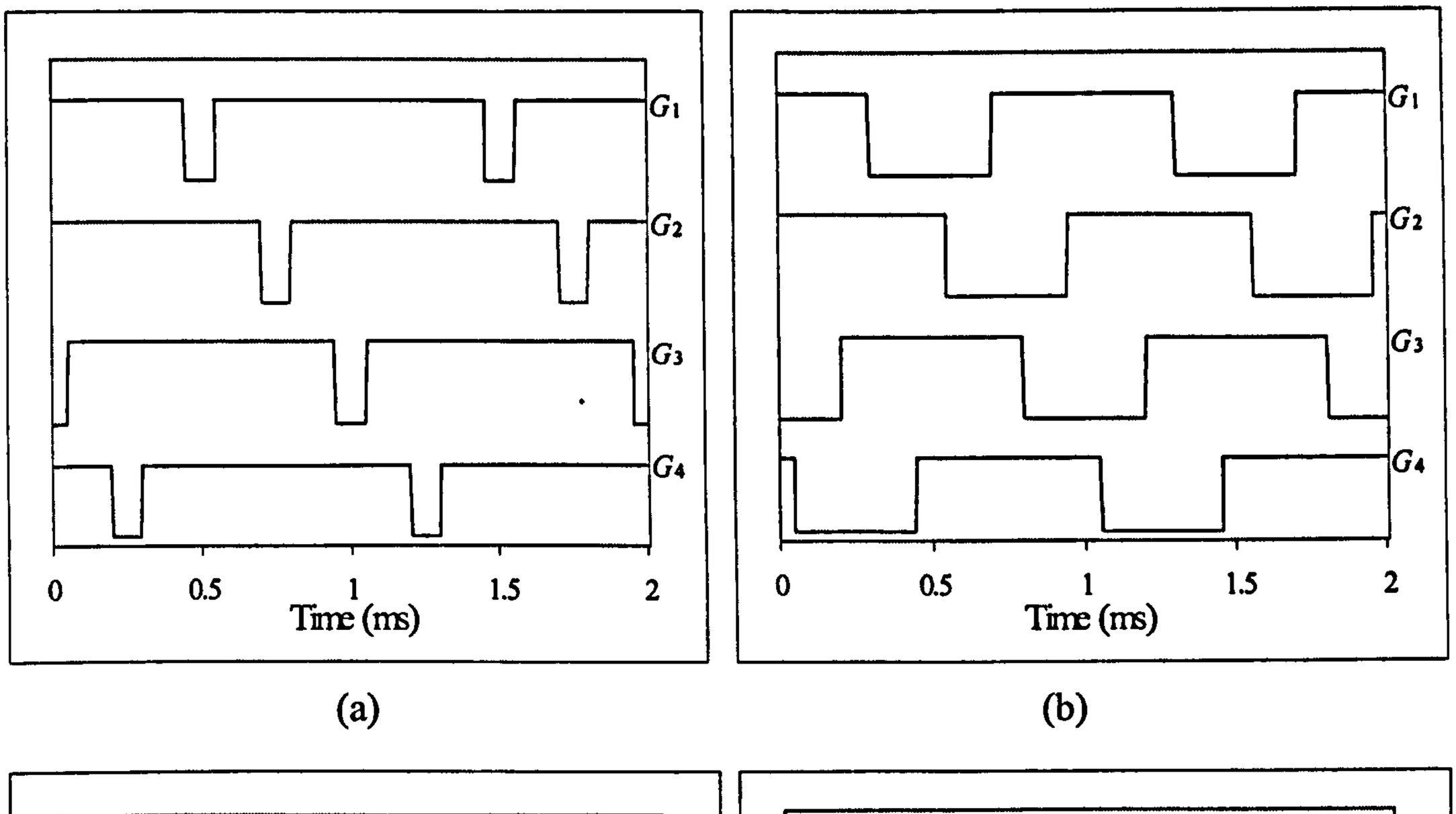
Carrier PWM strategies can be further grouped into categories as follows [85]:

- CD-MSPWM methods, where the reference waveform is sampled through a number of carrier waveforms displaced by contiguous increments of the reference waveform amplitude.
- PS-MSPWM method, where multiple carriers are phase shifted accordingly.
- Third harmonic injection PWM, also called Switching Frequency Optimal PWM control (SFO-PWM).
- A new carrier-based SPWM method, which can be considered as a combination of the CD-MSPWM and PS-MSPWM methods to some extent, but it is different from the H-MSPWM method mentioned in Section 3.3.3.

CD-MSPWM and PS-MSPWM techniques have been mentioned briefly as control methods applied to the NPC converters. In this Section, the above four carrier-based PWM techniques will be described in detail as control methods applied to the FC converters.

4.4.1 PS-MSPWM Technique

This concept was first proposed in [86] for an application of paralleling identical inverters to form a large Uninterruptible Power Supply (UPS). Basically, there are four regions in terms of the value of the reference waveform in the PS-MSPWM method. Fig. 4.4 shows the control switching signals G_1, G_2, G_3 and G_4 for the main switches S_{a1} to S_{a4} from top to bottom respectively in the different regions to explain capacitor voltage balance. Table 4.2 (a)-(d) gives the corresponding switching sequences and also the flying capacitor's charging and discharging modes for Fig. 4.4 (a)-4.4(d) respectively.



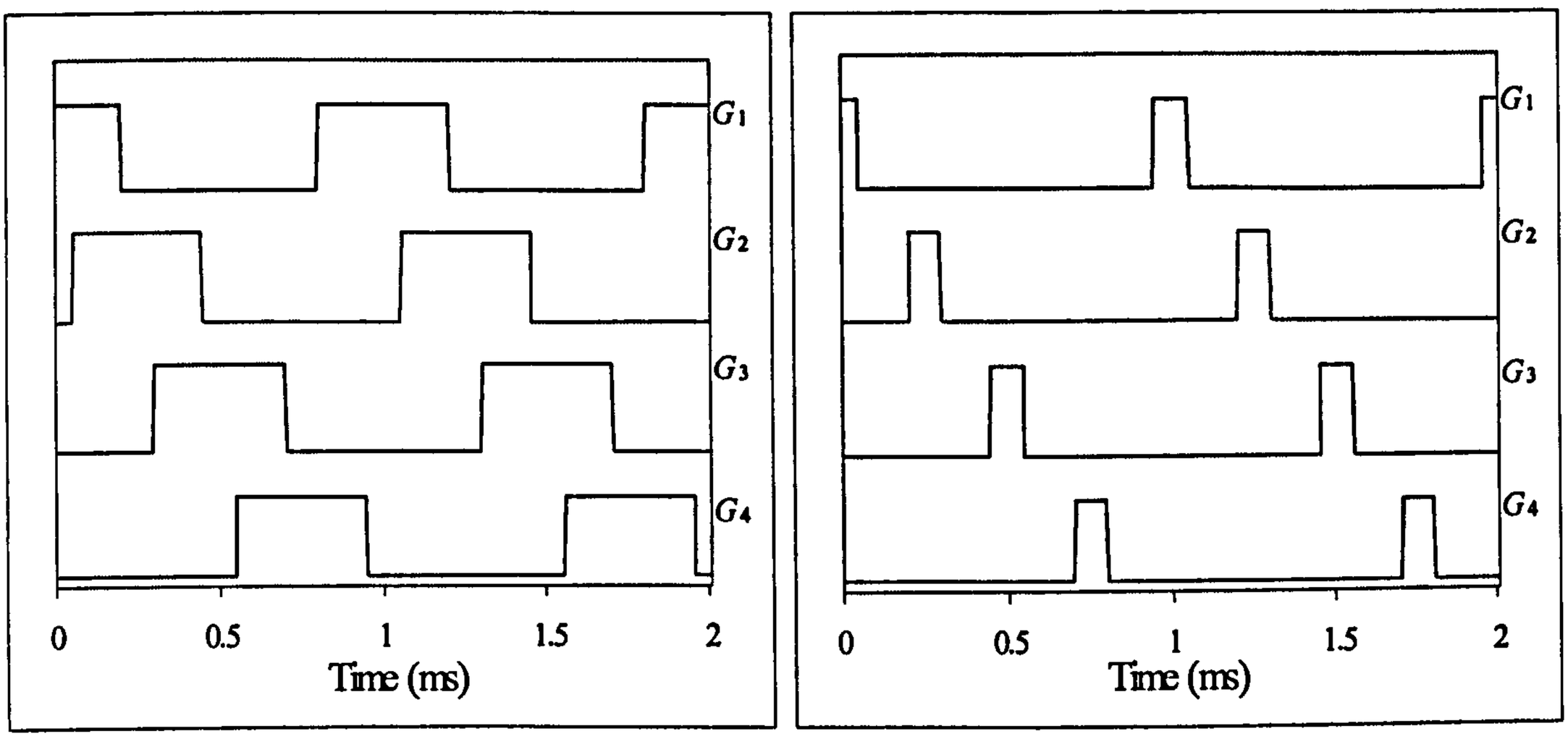


Fig. 4.4: Gate signals under the PS-MSPWM method at f_c=1kHz. (a) Gate signals at 0.5 p.u.< V_{ref}<1.0 p.u. (b) Gate signals at 0< V_{ref}<0.5 p.u. (c) Gate signals at -0.5 p.u.< V_{ref}<0 p.u. (d) Gate signals at –1.0 p.u.< V_{ref}<-0.5 p.u.

Table 4.2 (a): Switch states and flying capacitors' modes corresponding to Fig. 4.4 (a)

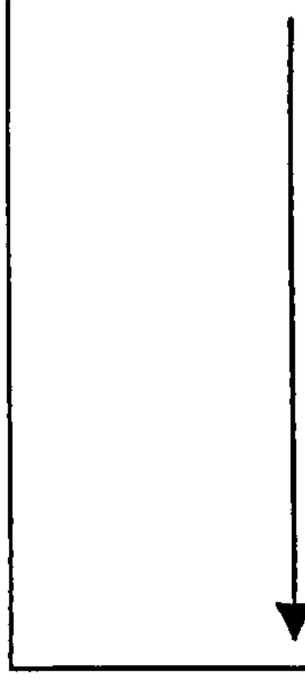
Modulation Sequence	S_{a1}	S_{a2}	S_{a3}	S_{a4}	Flying Capacitor (i_o>0)
	1	1	0	1	$C2$ charging, $C3$ discharging
	1	1	1	1	
	1	1	1	0	$C3$ charging
	1	1	1	1	
	0	1	1	1	$C1$ discharging
	1	1	1	1	
	1	0	1	1	$C1$ charging, $C2$discharging
	1	1	1	1	

Table 4.2 (b): Switch states and flying capacitors' modes corresponding to Fig. 4.4 (b)

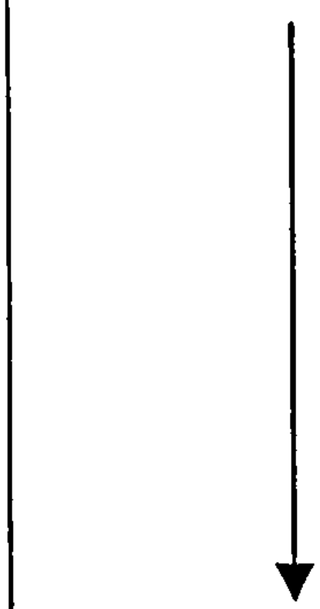
Modulation Sequence	S_{a1}	S_{a2}	S_{a3}	S_{a4}	Flying Capacitor (i_o>0)
	1	1	0	1	$C2$ charging, $C3$ discharging
	1	1	0	0	$C2$ charging
	1	1	1	0	$C3$ charging
	0	1	1	0	$C3$ charging, $C1$ discharging
	0	1	1	1	$C1$ discharging
	0	0	1	1	$C2$ discharging
	1	0	1	1	$C1$ charging, $C2$ discharging
	1	0	0	1	$C1$ charging, $C3$ discharging

Table 4.2 (c): Switch states and flying capacitors' modes corresponding to Fig. 4.4 (c)

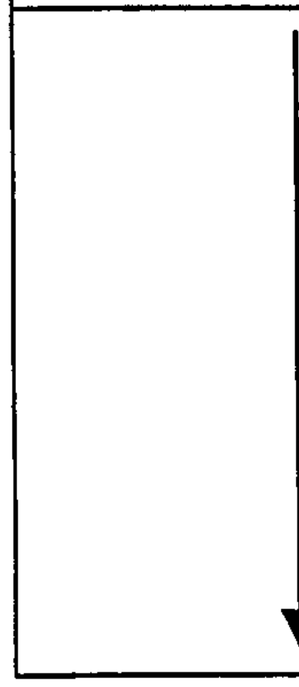
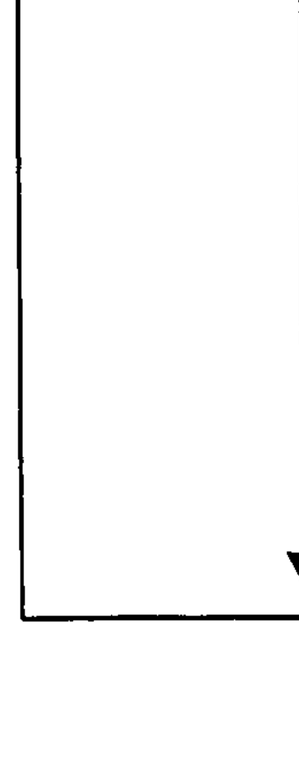
Modulation Sequence	S_{a1}	S_{a2}	S_{a3}	S_{a4}	Flying Capacitor (i_o>0)
	1	0	0	0	$C1$ charging
	1	1	0	0	$C2$ charging
	0	1	0	0	$C2$ charging, $C1$ discharging
	0	1	1	0	$C3$ charging, $C1$ discharging
	0	0	1	0	$C3$ charging, $C2$ discharging
	0	0	1	1	$C2$ discharging
	0	0	0	1	$C3$ discharging
	1	0	0	1	$C1$ charging, $C3$ discharging

Table 4.2 (d): Switch states and flying capacitors' modes corresponding to Fig. 4.4 (d)

Modulation Sequence	S_{a1}	S_{a2}	S_{a3}	S_{a4}	Flying Capacitor (i_o>0)
	1	0	0	0	$C1$ charging
	0	0	0	0	
	0	1	0	0	$C2$ charging, $C1$ discharging
	0	0	0	0	
	0	0	1	0	$C3$ charging, $C2$ discharging
	0	0	0	0	
	0	0	0	1	$C3$ discharging
	0	0	0	0	

It can be seen that the PS-MSPWM scheme uses 14 switching states out of 16 switching states except for 2_5 and 2_2 (i.e., $S_{a1}S_{a2}S_{a3}S_{a4}$=(1010) and (0101)). In one cycle of the carrier signal, all the flying capacitors' voltage will be kept balanced. If the value of the reference signal is constant within a carrier period, all the gate signals G_1 to G_4 have the same waveforms only with the time shifted by $T_s/4$. Here T_s is the period of the carrier. All the flying capacitors have the same charging and discharging times to make their average voltages zero, therefore guaranteeing the flying capacitor voltage balance, at least theoretically. Moreover, it is obvious that all switches have the same switching frequency and duty cycle, thus having the same rms current and good switch utilisation. In order to evaluate switching losses, the number of switching transitions per leg per reference modulating cycle (i.e., line cycle) is used here. The total number of switching transitions per phase per line cycle for a five-level FC converter under the PS-MSPWM method is $16m_f$. On the other hand, under this scheme, the resultant output voltage of this multilevel VSC has a very high output switching frequency, even if the switching frequency of the individual switches is not very high. As a consequence, the size of the output filter can be reduced.

4.4.2 CD-MSPWM Techniques

Fig. 4.5 shows the PD-MSPWM applied to a five-level FC converter. The number 0, 1, 2 3, 4 refers to switching states. In fact, for any CD-MSPWM techniques, their switching states, output phase voltage and related flying capacitors' charging and discharging modes are the same as those shown in Table 4.3.

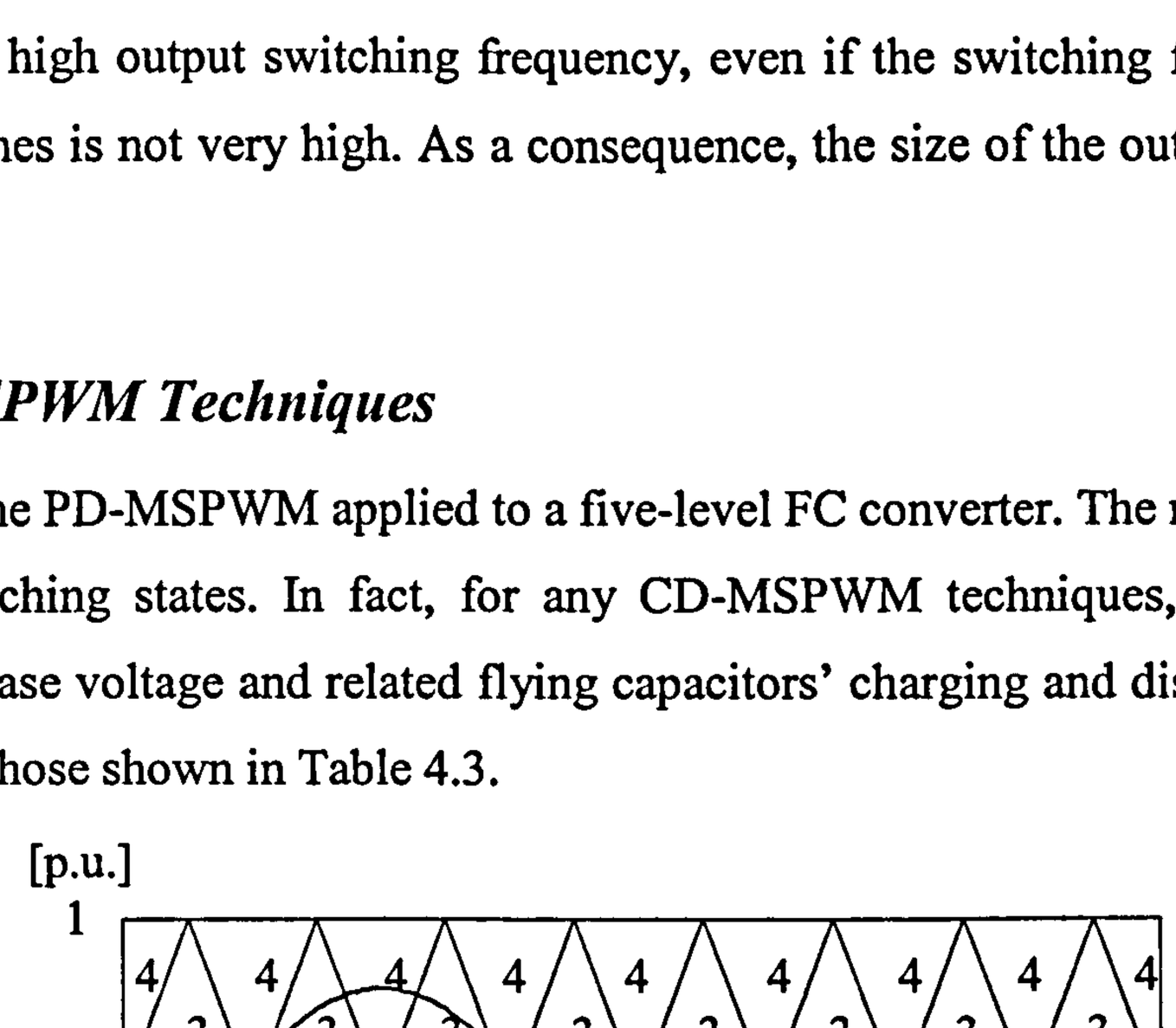


Fig. 4.5: The PD-MSPWM method for a five-level FC converter.

Table 4.3: Switching states, output voltage levels and states of the flying capacitors of a five-level FC converter with the CD-MSPWM control methods

(Assuming positive load current)

V_{ref}	V_{AO}	Symbol	Switching States				Flying Capacitor
			S_{a1}	S_{a2}	S_{a3}	S_{a4}	
0.5-1.0 p.u.	$V_{dc}/2$	4	1	1	1	1	
	$V_{dc}/4$	3	0	1	1	1	$C1$ discharging
0.0-0.5 p.u.	$V_{dc}/4$	3	0	1	1	1	$C1$ discharging
	0	2	0	0	1	1	$C2$ discharging
-0.5- 0p.u.	0	2	0	0	1	1	$C2$ discharging
	$-V_{dc}/4$	1	0	0	0	1	$C3$ discharging
-1--0.5 p.u.	$-V_{dc}/4$	1	0	0	0	1	$C3$ discharging
	$-V_{dc}/2$	0	0	0	0	0	

It can be seen from Table 4.3 and Figure 4.5 that when m_a is high (m_a >0.5), the magnitude of the switching frequency is ordered as $f_{sw,Sa1} = f_{sw,Sa4} > f_{sw,Sa2} = f_{sw,Sa3}$. In case of low m_a (e.g. m_a <0.5), it is ordered as $f_{sw,Sa2} = f_{sw,Sa3} > f_{sw,Sa1} = f_{sw,Sa4}$ =0. In this case, S_{a1} and S_{a4} have no switching and S_{a2} and S_{a3} have the same switching frequency as that of a three-level converter. Generally, the switching frequencies of switches in CD-MSPWM methods appear differently according to the number of voltage levels and m_a.

The rms current of switch I_{Sai} is defined as:

$$I_{Sai} = \sqrt{\frac{1}{T_o}\int_0^{T_o} i_{Sai}^2(t)\cdot dt} \tag{4-19}$$

Here, T_o is a period of the output waveform and $i_{Sai}(t)$ is the current of the switch expressed by:

$$i_{Sai}(t) = G_i(t)\cdot i_o(t) \tag{4-20}$$

Here, $G_i(t)$ is the gating signal normalized by 1(on) or 0(off). i=1,2,3,4. $i_o(t)$ is the phase load current. It can be noticed that $G_1(t) \neq G_2(t) \neq G_3(t) \neq G_4(t)$. This makes the inner switch S_{a4} maintain the longest on-duty ratio. Hence the rms current of the switches is always ordered as $I_{Sa4} > I_{Sa3} > I_{Sa2} > I_{Sa1}$ even though the rms value varies according to the load and m_a. Considering the two aspects collectively, this method makes S_{a4} have the largest loss in high m_a and S_{a3} have the largest loss in low m_a.

If the load power factor is varied for some reasons, it can make the current division problem of switches worse. Assuming that the gate signal of switch S_{a1} is the same as that shown in Fig. 4.6, the rms current of the switch decreases as the load power factor varies from (a) to (c).

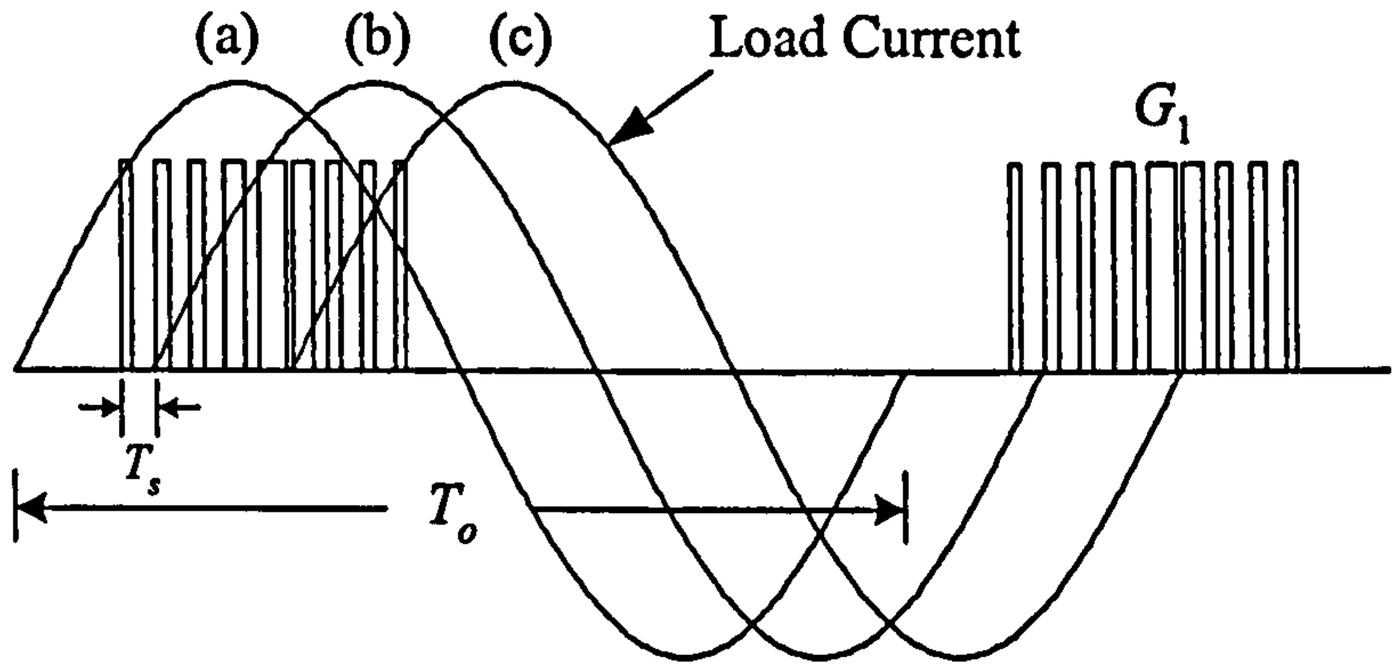


Fig. 4.6: Effect of the variations in load power factor on the rms current in the switch under the PD-MSPWM technique.

So the switching frequency and the rms current of switches depend on the amplitude modulation ration m_a and the load power factor in the CD-MSPWM method, which has the worst switch utilisation. In addition, the CD-MSPWM methods cannot keep the voltage of the flying capacitors balanced due to the lack of switching redundancies, which can be seen from Table 4.3. But they bring about lower switching losses than those of the PS-MSPWM method. This is because the total number of switching transitions per phase per line cycle for a five-level FC converter under CD-MSPWM methods is $4m_f$, one fourth of that of the PS-MSPWM method.

4.4.3 New Carrier-Based SPWM Technique

A new carrier-based SPWM technique that combines the features of the CD-MSPWM methods with the PS-MSPWM method was proposed for cascaded multilevel converters to solve the poor switch utilisation using leg voltage redundancies [75]. Fig. 4.7 shows such these carriers. Fig. 4.7 (a) represents the new carrier $S1$ for S_{a1}, 4.7 (b) $S2$ for S_{a2}, 4.7(c) $S3$ for S_{a3}, and 4.7(d) $S4$ for S_{a4}, respectively. Here, the thin dotted line is the reference-modulating wave (providing m_f is high enough to regard V_{ref} as constant during the carrier period), the thin line is the gating pulse and the thick line is the new carrier. T_s is the period of the triangular wave, T_s' is the period of the new carrier.

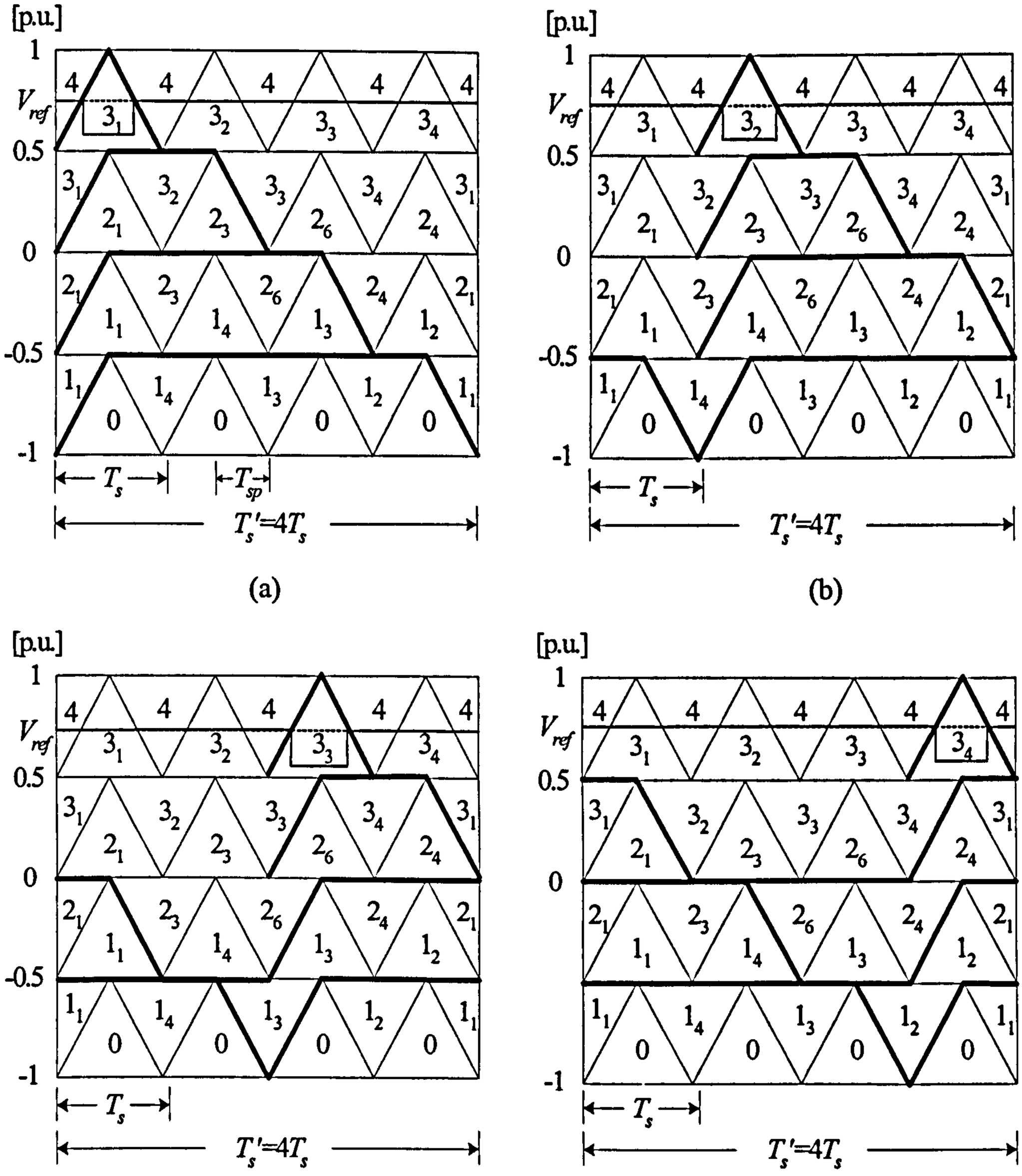


Fig. 4.7: Carriers waveforms with the new carrier-based SPWM scheme.

(a) Carrier $S1$ (b) Carrier $S2$ (c) Carrier $S3$ (d) Carrier $S4$

The carrier $S1$ for the switch S_{a1} is achieved as follows: Firstly, in case of 0.5 p.u.< V_{ref} <1.0 p.u., the switch state varies with 4-3_1- 4-3_2-4-3_3-4-3_4-4, as shown in Fig. 4.7. (a). At this time the switch sequence for S_{a1} varies with 1-0-1-1-1-1-1-1-1. Thus the switching for S_{a1} occurs only in the switch state of 4-3_1-4. Consequently, the carrier between 0.5 p.u. and 1.0 p.u. can be obtained. Secondly, in case of 0< V_{ref} <0.5 p.u., the switch state varies with 3_1-2_1-3_2-2_3-3_3-2_6-3_4-2_4-3_1. Here, the switch sequence for S_{a1} varies with 1-0-0-0-1-1-1-1-1.

Thus the switching for S_{a1} occurs only in the switch state of 3_1-2_1 and 2_3-3_4. It remains turned-on in the 3_1, 3_3, 3_4, 2_6, 2_4 and turned-off in 2_1, 3_2, 2_3. Consequently, the carrier between 0 p.u. and 0.5 p.u. can be obtained. Thirdly, in case of -0.5 p.u.< V_{ref} < 0 p.u., the switch state varies with 2_1-1_1-2_3-1_4-2_6-1_3-2_4-1_2-2_1. At this time the switch sequence for S_{a1} varies with 1-0-0-0-0-0-1-1-1. Thus the switching for S_{a1} occurs only in the switch state of 2_1-1_1 and 1_3-2_4. It remains on in the 2_1, 2_4, 1_2 and off in 1_1, 2_3, 1_4, 2_6, 1_3. Consequently, the carrier between –0.5 p.u. and 0 p.u. can be obtained. Fourthly, in case of -1.0 p.u. < V_{ref} < -0.5 p.u., the switch state varies with 1_1-0-1_4-0-1_3-0-1_2-0-1_1. At this time the switch sequence for S_{a1} varies with 1-0-0-0-0-0-0-0-1. Thus the switching for S_{a1} occurs only in the switch state of 1_1-0-1_1. It remains off in the other states except for 1_1. Thus, the carrier between -1.0 p.u. and -0.5 p.u. can be obtained. Similarly, carriers for S_{a2}, S_{a3} and S_{a4} are derived in Fig. 4.7 (b), (c) and (d) respectively. It can be observed that the new carriers of Fig. 4.7 (b), (c) and (d) are equal to carrier $S1$ shown in Fig. 4.7 (a) but shifted by $2T_{sp}$, $4T_{sp}$ and $6T_{sp}$ respectively. Here, T_{sp} is defined as the time interval between two successive peak values (positive and negative one) of the triangular signal.

This new SPWM method has different carriers from those of the PS-MSPWM method, but it generates the same control switching signals as those shown in Fig. 4.4, thus having the same switching states and flying capacitor charging/discharging modes as those shown in Table 4.2. Like the PS-MSPWM method, this new SPWM method can solve the unbalance problem of flying capacitors using switching redundancies. It may be noted that the switches always turn on and off once during $4T_s$ regardless of m_a from the new carriers in Fig. 4.7. The gating pulses having the period of $4T_s$ in the new method are distributed uniformly as shown in Fig. 4.8. Therefore, the rms currents of each switch have the same value if the load power factor varies from (a) to (c).

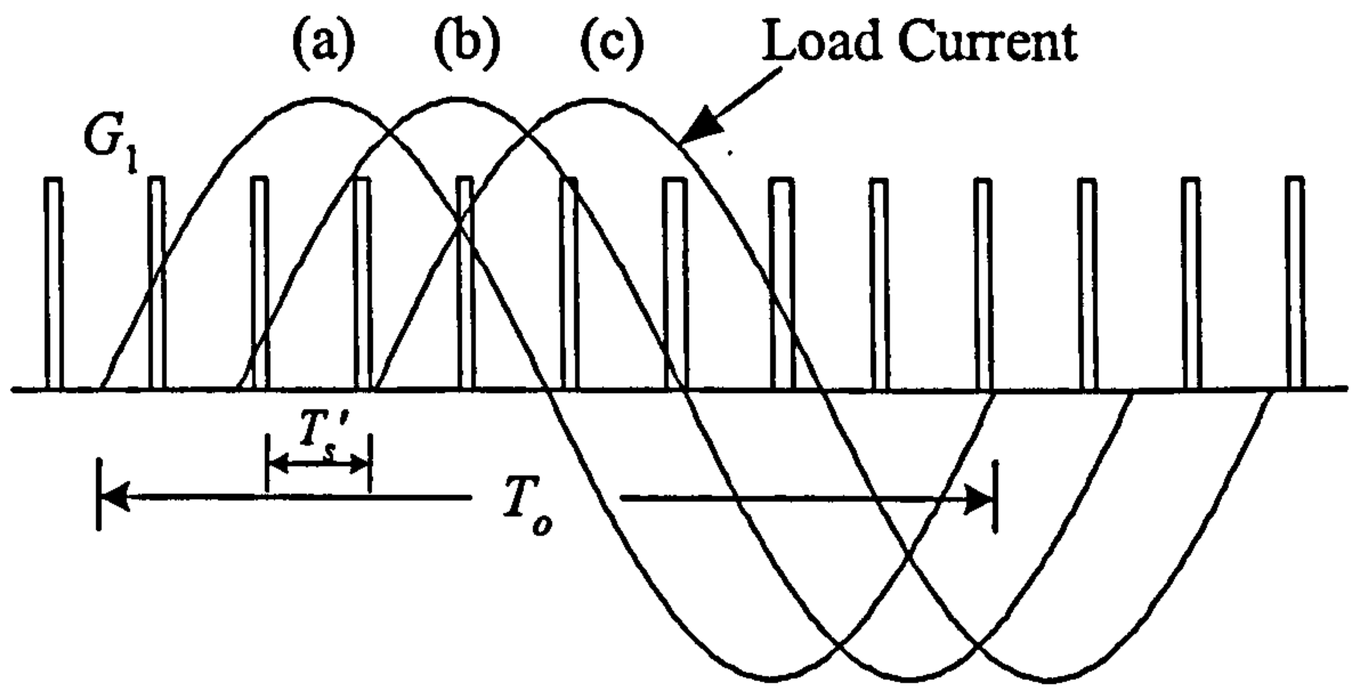


Fig. 4.8: Effect of variations in the load power factor on the rms current in a switch under the new carrier-based SPWM technique.

The main advantage of this method is the optimised utilisation of all the switches at both high and low modulation ratio m_a even if the load power factor varies.

In addition, the total number of switching transitions of the converter has no variation as compared with the CD-MSPWM methods, but the switching frequency for each switch becomes equal, unlike in the CD-MSPWM method. Because the total number of switching transitions per phase per line cycle for a five-level FC converter with this new SPWM method is $16m_f'$, i.e., $4m_f$, the same as that of the CD-MSPWM techniques, one fourth of that of the PS-MSPWM method. Provided m_f' is defined as:

$$m_f' = \frac{T_o}{T_s'} \tag{4-21}$$

$$m_f = \frac{T_o}{T_s} \tag{4-22}$$

Since $$T_s' = 4T_s \tag{4-23}$$

so $$m_f' = \frac{m_f}{4} \tag{4-24}$$

4.4.4 Switching Frequency Optimal PWM Technique (SFO-PWM)

Normally, the SPWM technique requires the peak-phase voltage must be less than half the DC bus voltage in order to avoid saturation [87].

$$\hat{V}_{AO} \le \frac{V_{dc}}{2} \qquad \text{for SPWM} \tag{4- 25}$$

where $\hat{V}_{AO} = \sqrt{2}V_{AO}$, the peak-phase voltage.

Equation (4-25) defines a limit on the value of $\hat{V}_{AO}$ for which the PWM remains out of saturation. Increasing the phase voltage beyond that defined by (4-25) causes the SPWM to enter the pulse-dropping region of operation. Besides being nonlinear, the gain of the SPWM amplifier reduces sharply in this region, resulting in distortion of the output current.

To extend the SPWM linear range, Steinke [19] proposed a carrier-based method termed SFO-PWM which was similar to Carrara's except that a zero-sequence (triplen harmonic) voltage is added to each one of the reference waveforms. This method takes the instantaneous average of the maximum and minimum of the three reference voltages and subtracts this value from each of the individual reference voltage to obtain the modulation

waveform, i.e.,

$$v_{offset} = \frac{max(v_{refA}, v_{refB}, v_{refC}) + min(v_{refA}, v_{refB}, v_{refC})}{2} \tag{4-26}$$

$$v_{refA,SFO} = v_{AO} - v_{offset} \tag{4-27}$$

$$v_{refB,SFO} = v_{BO} - v_{offset} \tag{4-28}$$

$$v_{refC,SFO} = v_{CO} - v_{offset} \tag{4-29}$$

In the SFO-PWM technique, the equivalent peak-phase voltage is:

$$\hat{V}_{AO} \leq \frac{V_{dc}}{\sqrt{3}} \tag{4-30}$$

A comparison of (4-25) and (4-30) indicates that given a DC bus voltage V_{dc}, the peak-phase voltage $\hat{V}_{AO}$ for the SFO-PWM has a value 1.1547 ($=2/\sqrt{3}$) times larger than $\hat{V}_{AO}$ for the normal SPWM without entering the non-linear region. This method has the highest line-to-line voltage utilisation ratio that is the same as SV-PWM method.

Fig. 4.9 illustrates the three modified reference waveforms at m_a=0.9 that include third harmonic and look like a saddle. It should be noted that the SFO-PWM technique can only be used for three-phase three-wire systems, and it enables the amplitude modulation ratio m_a to be increased by 15% before over modulation, or pulse dropping, occurs. If it is used in three-phase four wire systems, the output current waveform will look like a saddle rather than a sinusoidal.

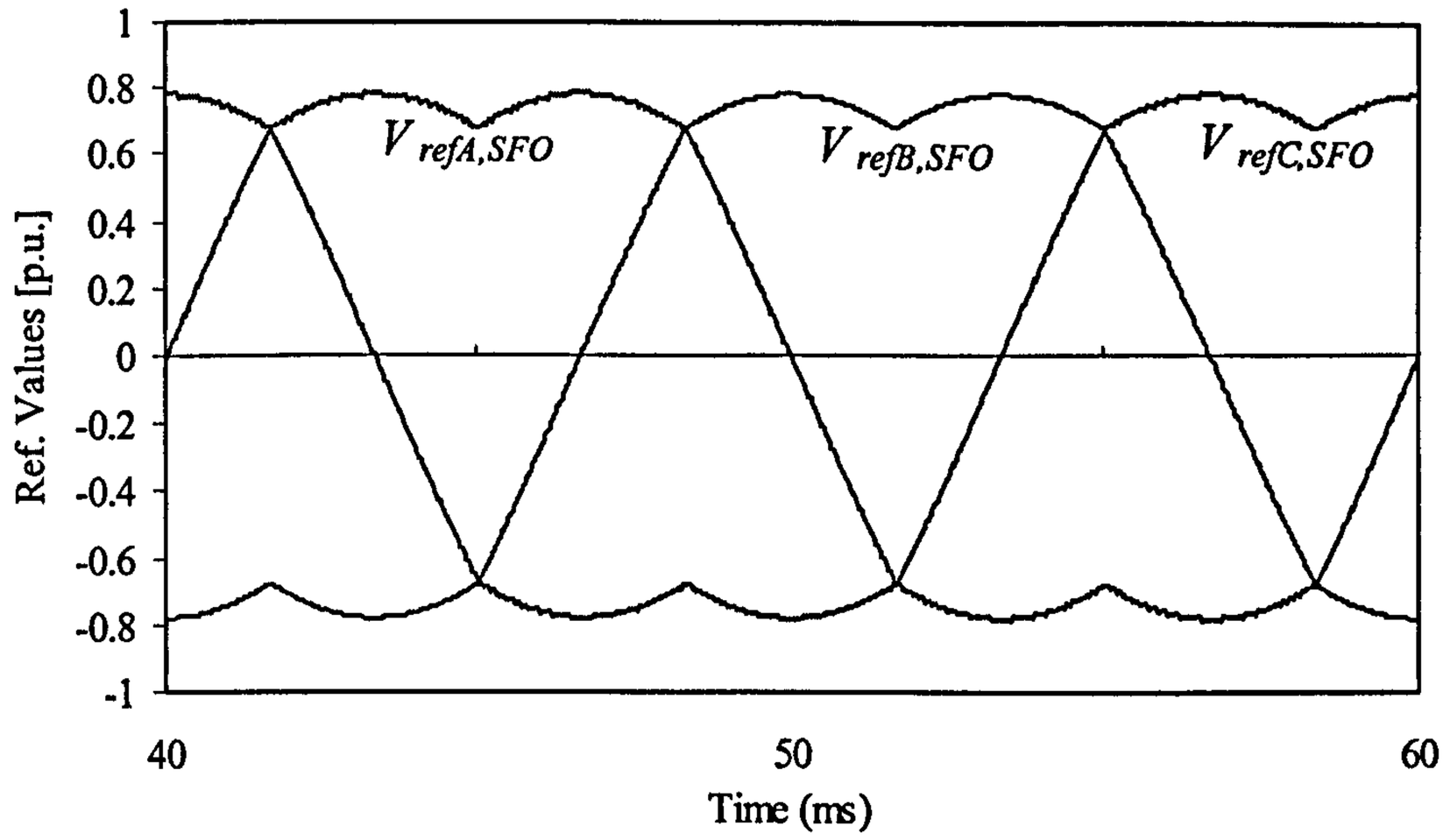


Fig. 4.9: Reference waveforms with the SFO-PWM method (m_a=0.9).

4.5 Simulation Results

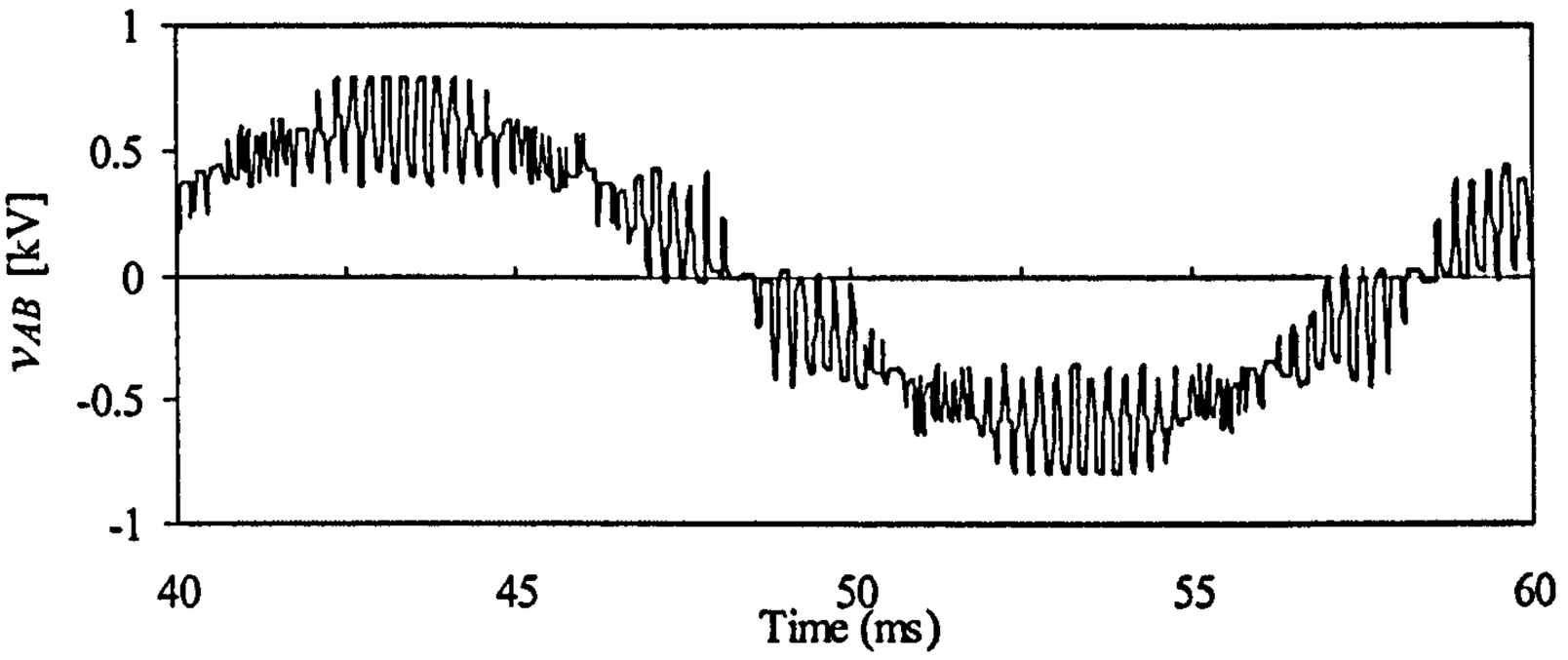
Simulations have been carried out for a three-phase five-level flying capacitor converter to compare the above four different control techniques. The parameters are as follows: V_{dc}=0.8 kV, f_o=50 Hz, f_s=1 kHz, m_f=20, m_a=0.9, $C1$=$C2$=$C3$=1000 uF, T_{sp}=125 μs (for New PWM method), Load resistance R=10 Ω, inductance L=10 mH, the load is Y connected (star).

Figs. 4.10 to Fig. 4.13 display the simulation results including the line-to-line output voltage v_{AB} waveform, harmonic spectrum of v_{AB}, load current i_a as well as the voltage waveforms of the flying capacitors for the PS-MSPWM, the new carrier-based SPWM, the CD-MSPWM and the Switching Frequency Optimal Phase-Shifted PWM (SFO-PS-PWM) technique respectively. The SFO-PS-PWM technique means that the carriers are phase-shifted and the modulating signal includes the third harmonic injection instead of a pure sinusoidal signal. Table 4.4 presents the THD for different m_a at a fixed m_f. Here, $\hat{V}_{AB1}$ represents the v_{AB} at the fundamental frequency.

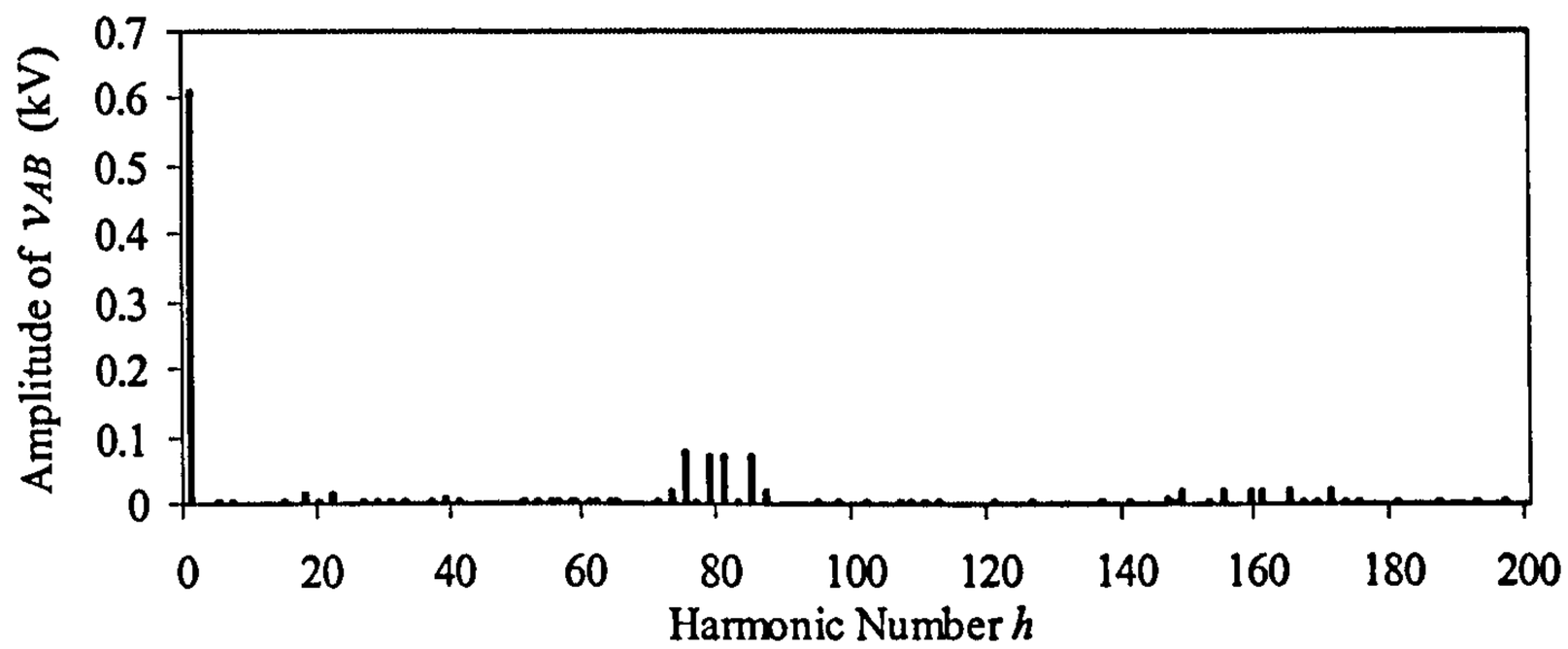
Table 4.4: Comparison of different control methods on the THD
(m_f=20, V_{dc}=800 V, f_o=50 Hz)

Method	m_a	0.3	0.6	0.9	1.0	1.15
PS-MSPWM	THD of v_{AB} (%)	90.5	19.2	26.1	22.9	18.2
	$\hat{V}_{AB1}$ (V)	196	401	611	678	739
New SPWM	THD of v_{AB} (%)	91.3	21.0	28.2	23.0	18.3
	$\hat{V}_{AB1}$ (V)	195	403	609	680	739
SFO-PS-PWM	THD of v_{AB} (%)	97.4	22.9	32.1	27.8	16.0
	$\hat{V}_{AB1}$ (V)	197	398	609	678	778

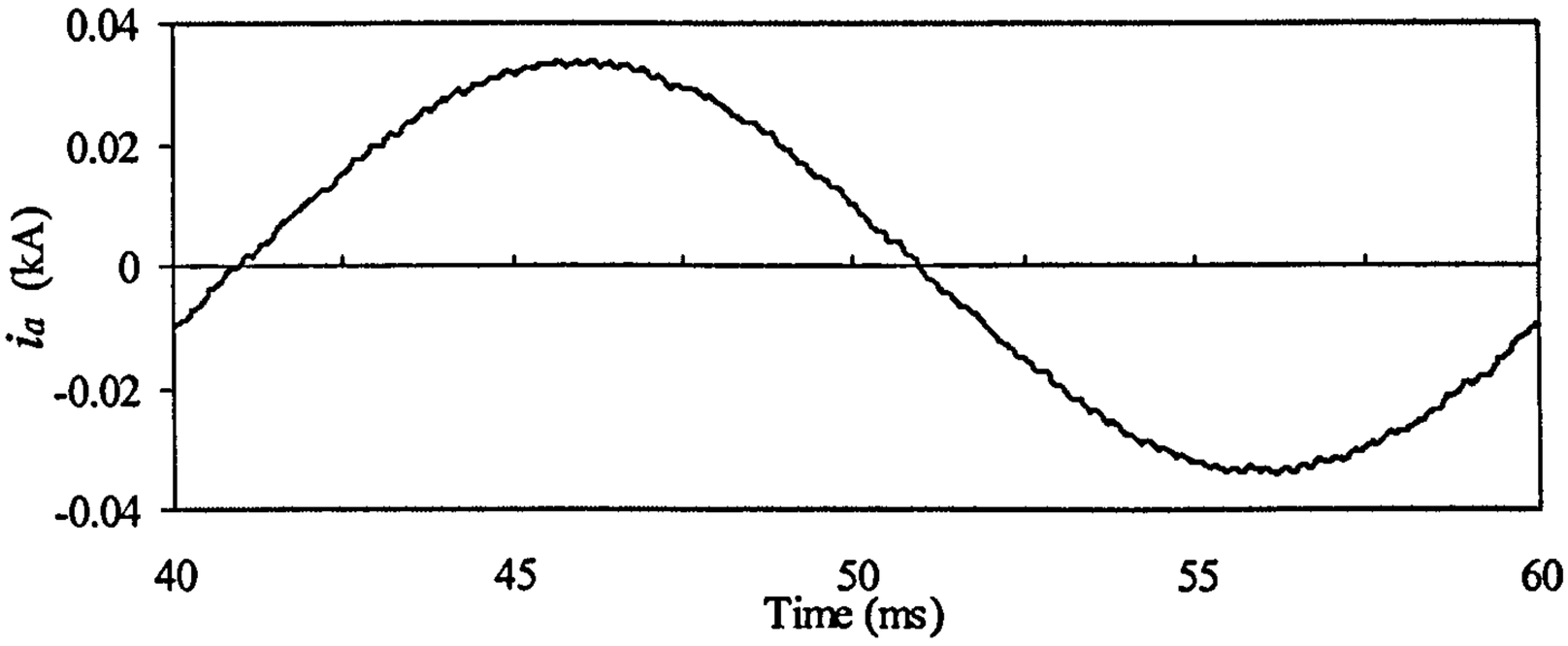
(a)



(b)



(c)



(d)

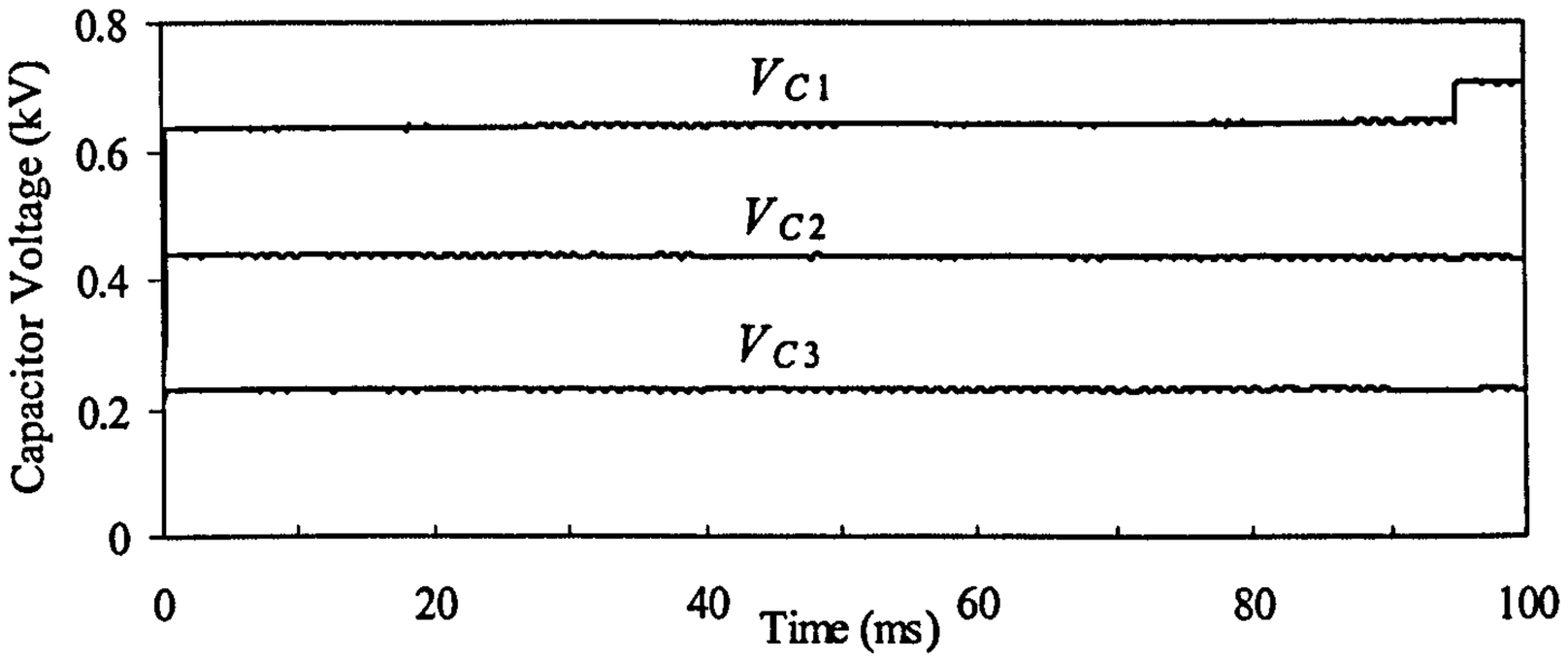
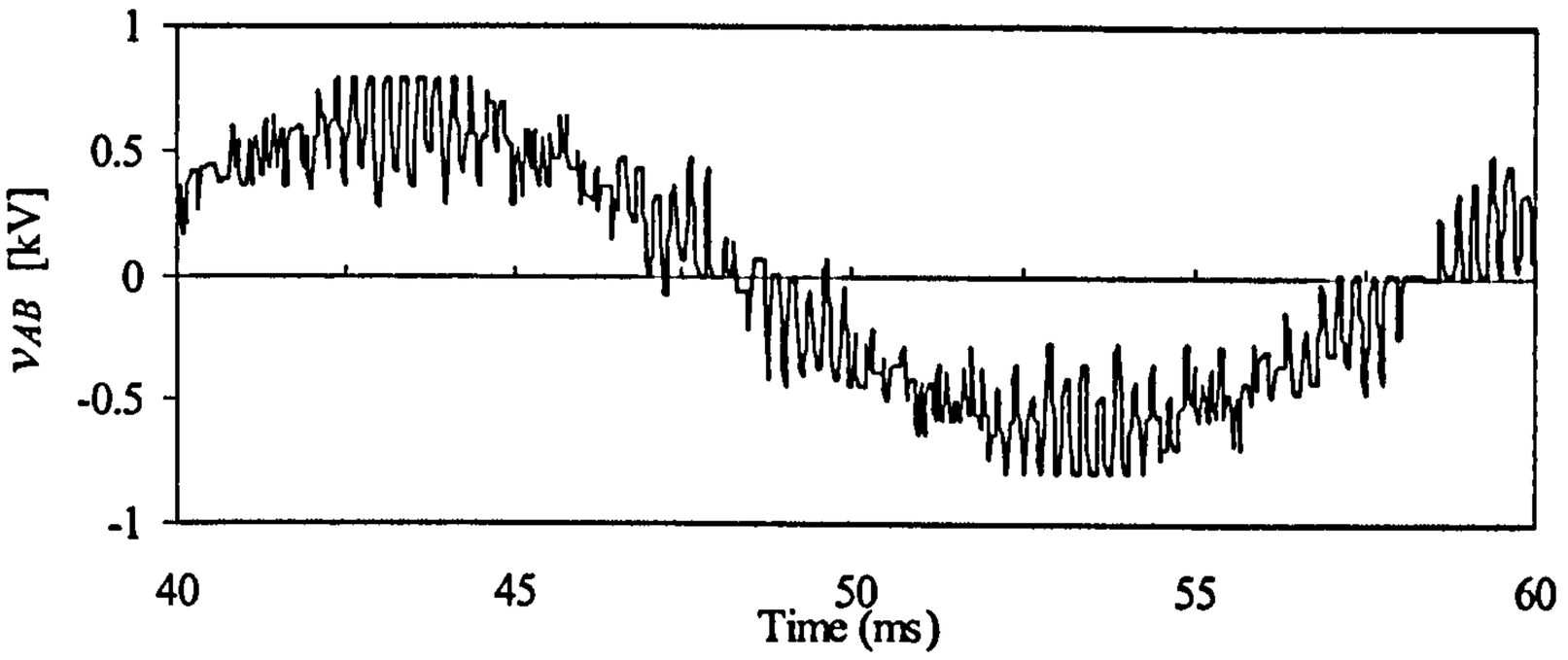
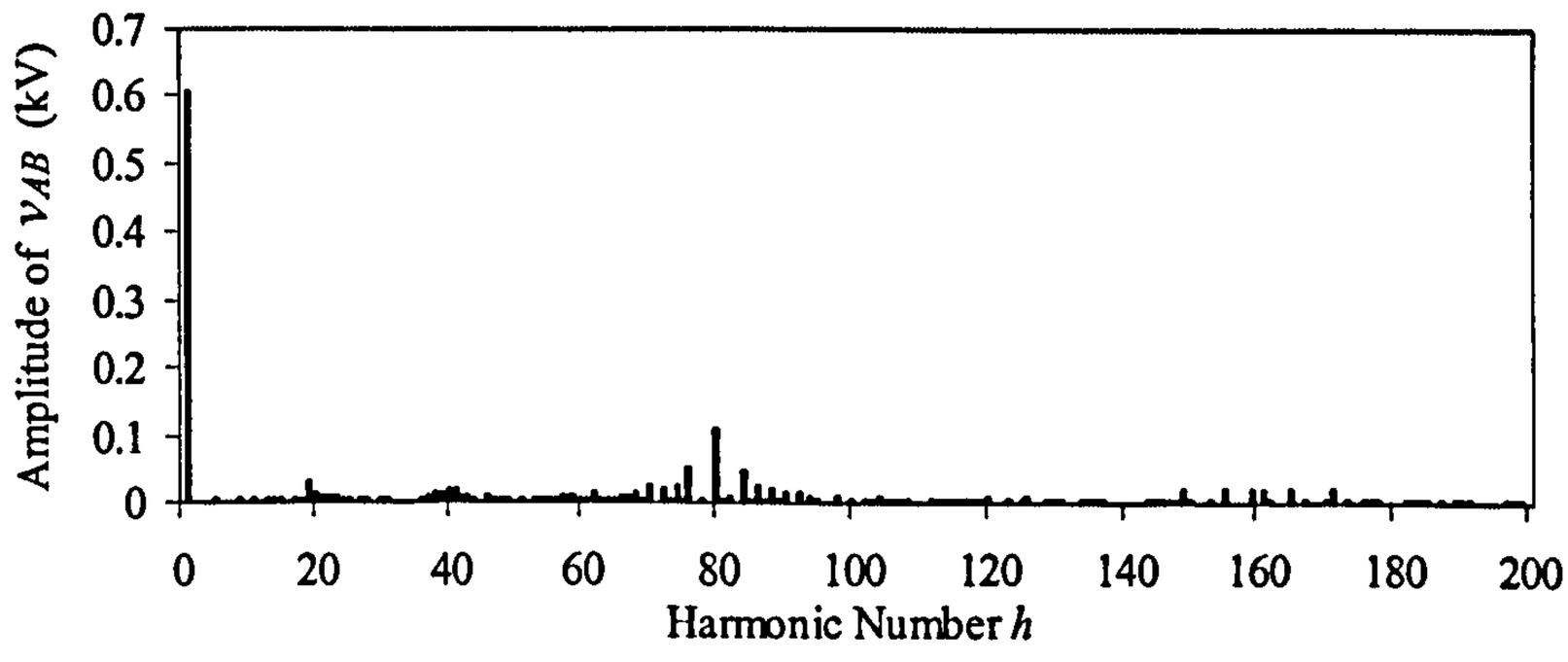


Fig. 4.10: Simulation results with the PS-MSPWM method at m_a=0.9, m_f=20, V_{dc}=800 V, f_o=50 Hz. (a) Line-to-line output voltage v_{AB} waveform. (b) Harmonic spectrum of v_{AB}. (c) Load current i_a waveform. (d) Waveforms of flying capacitor voltages.

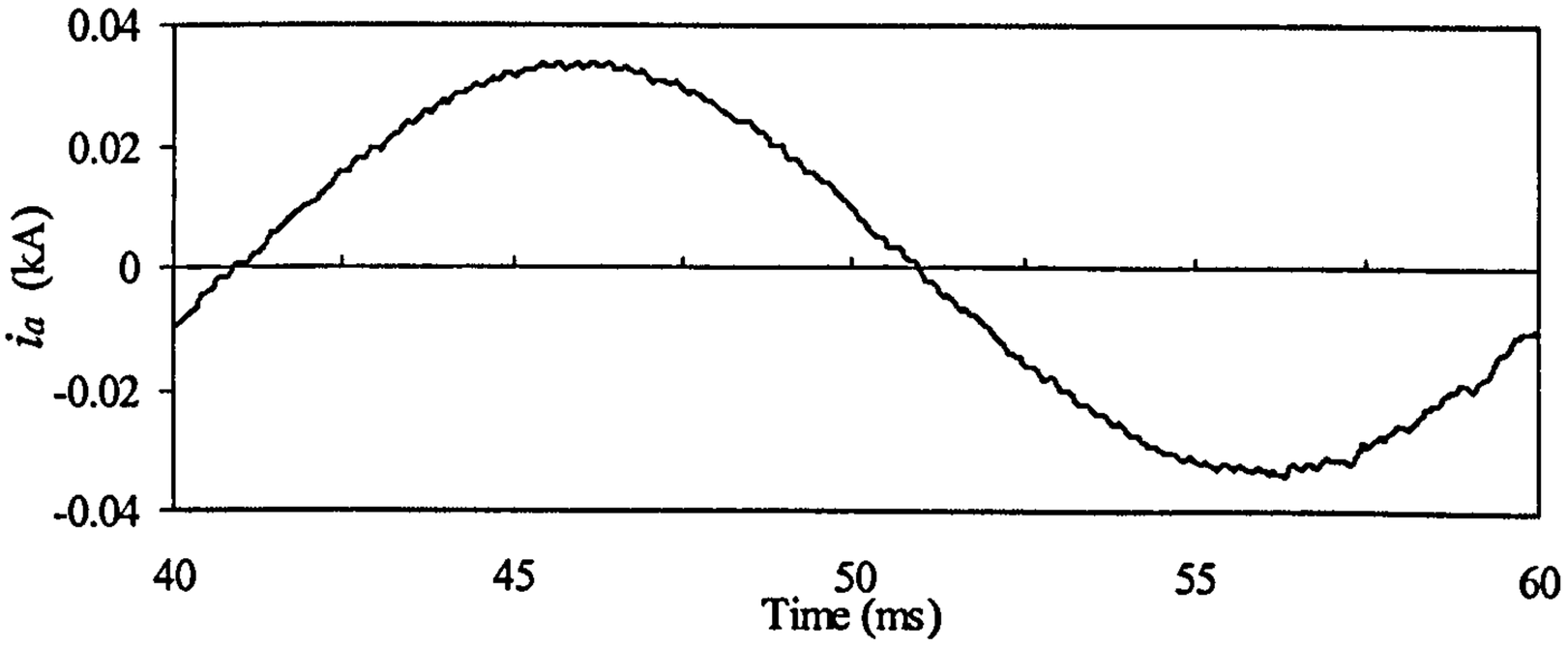
(a)



(b)



(c)



(d)

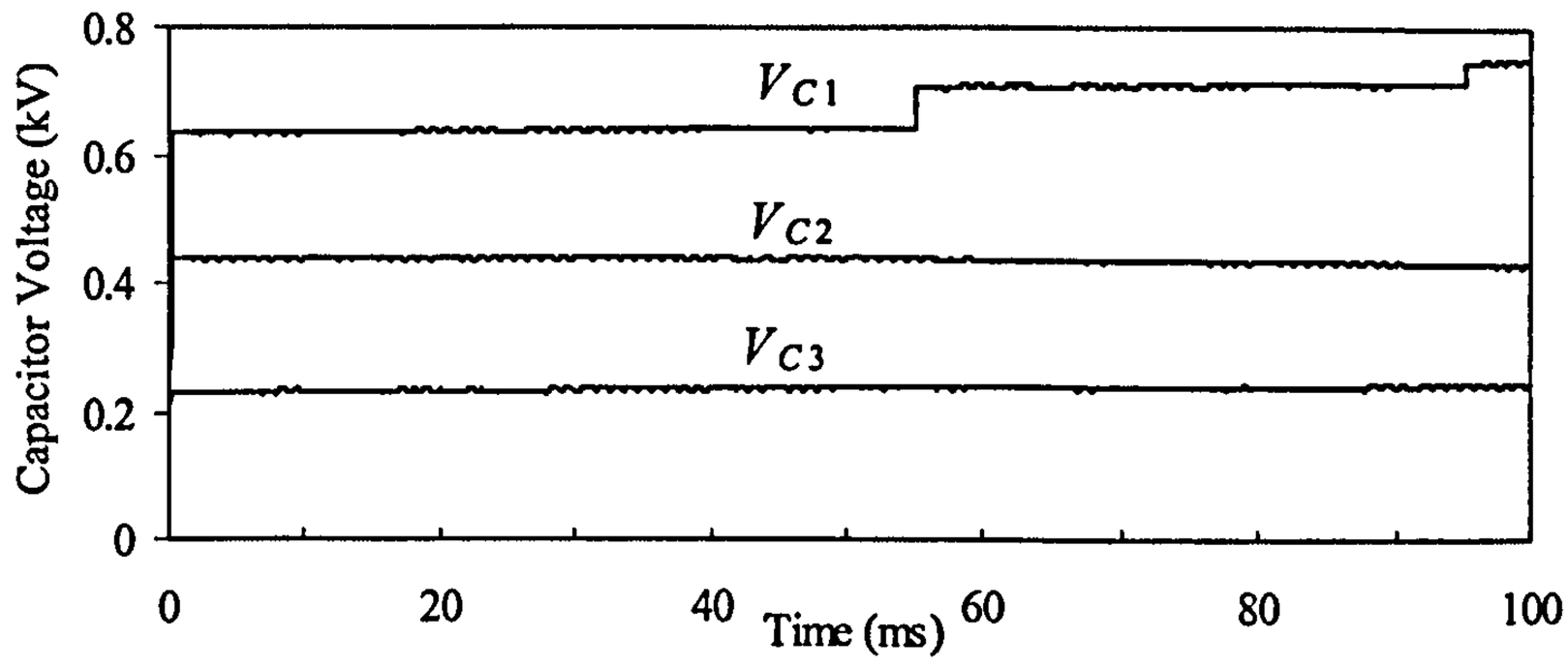
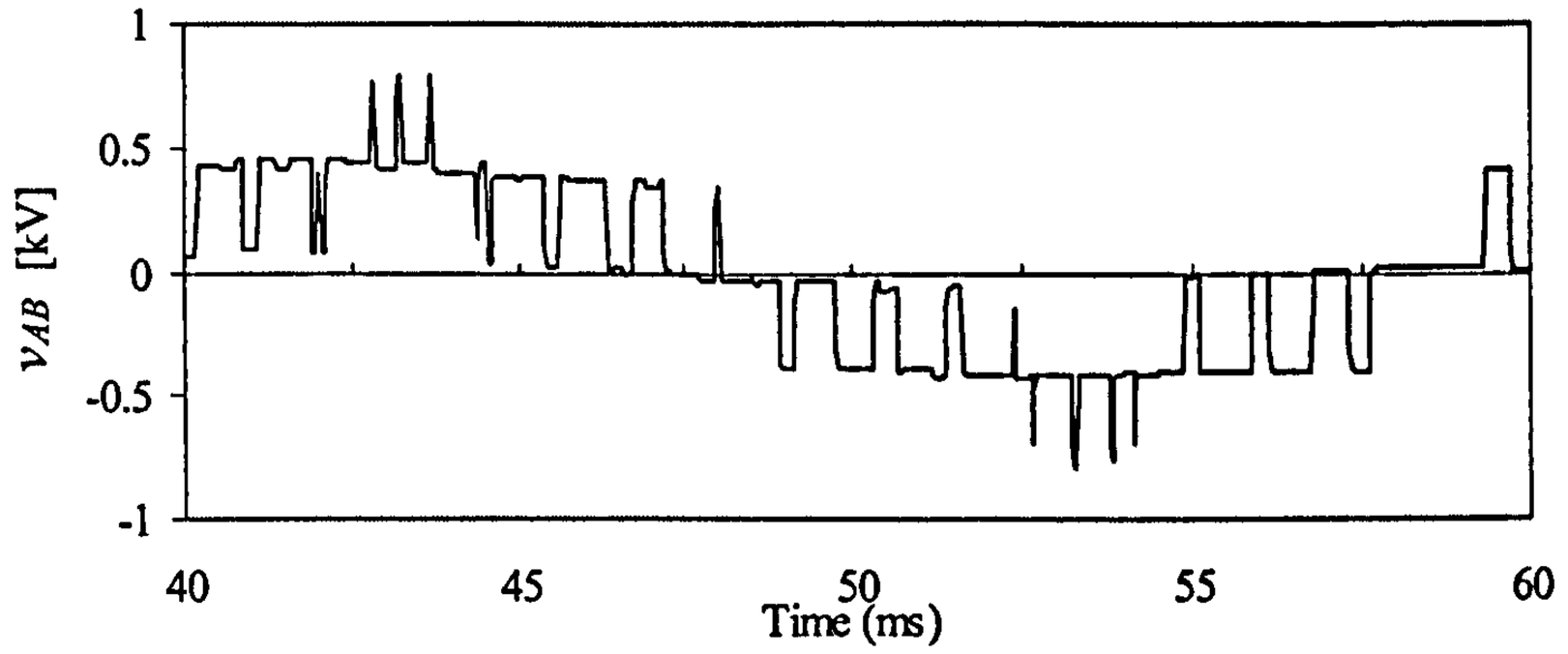
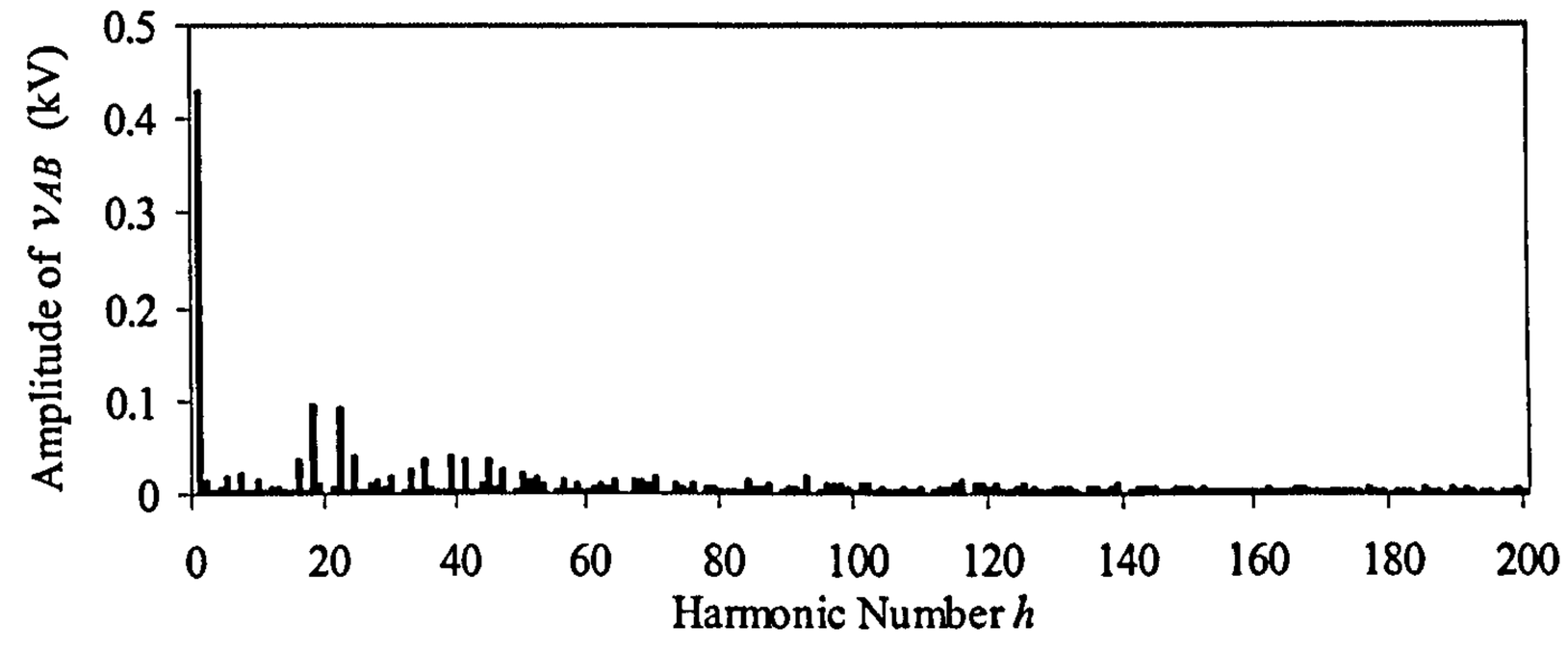


Fig. 4.11: Simulation results with the New SPWM method at m_a=0.9, m_f=20, V_{dc}=800 V, f_o=50 Hz. (a) Line-to-line output voltage v_{AB} waveform. (b) Harmonic spectrum of v_{AB}. (c) Load current i_a waveform. (d) Waveforms of flying capacitor voltages.

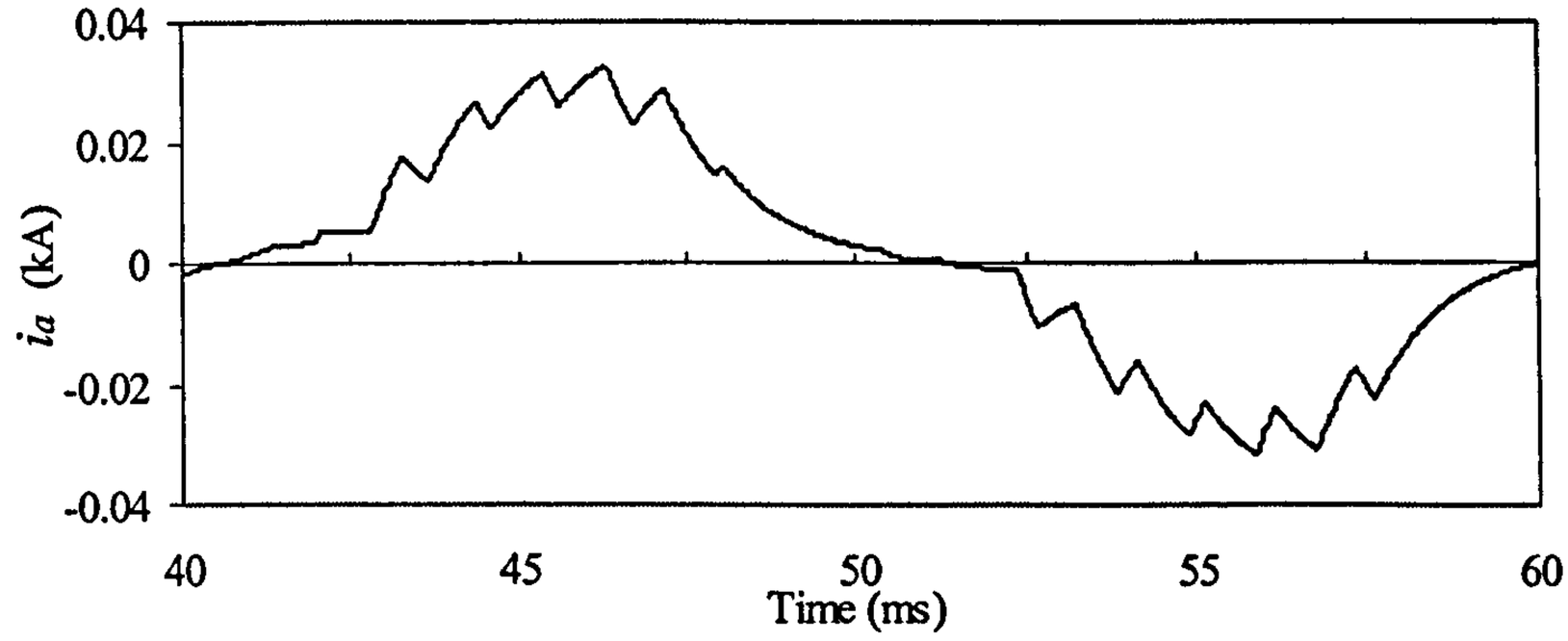
(a)



(b)



(c)



(d)

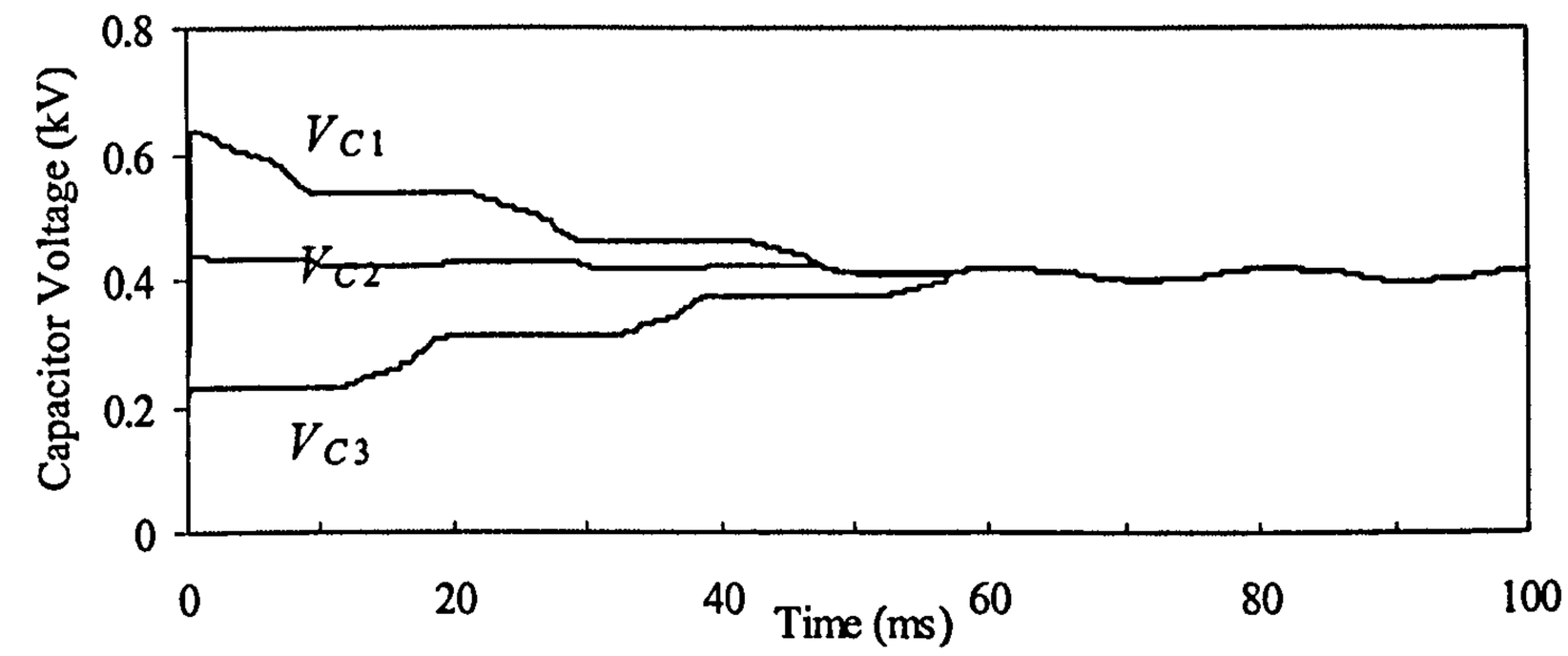
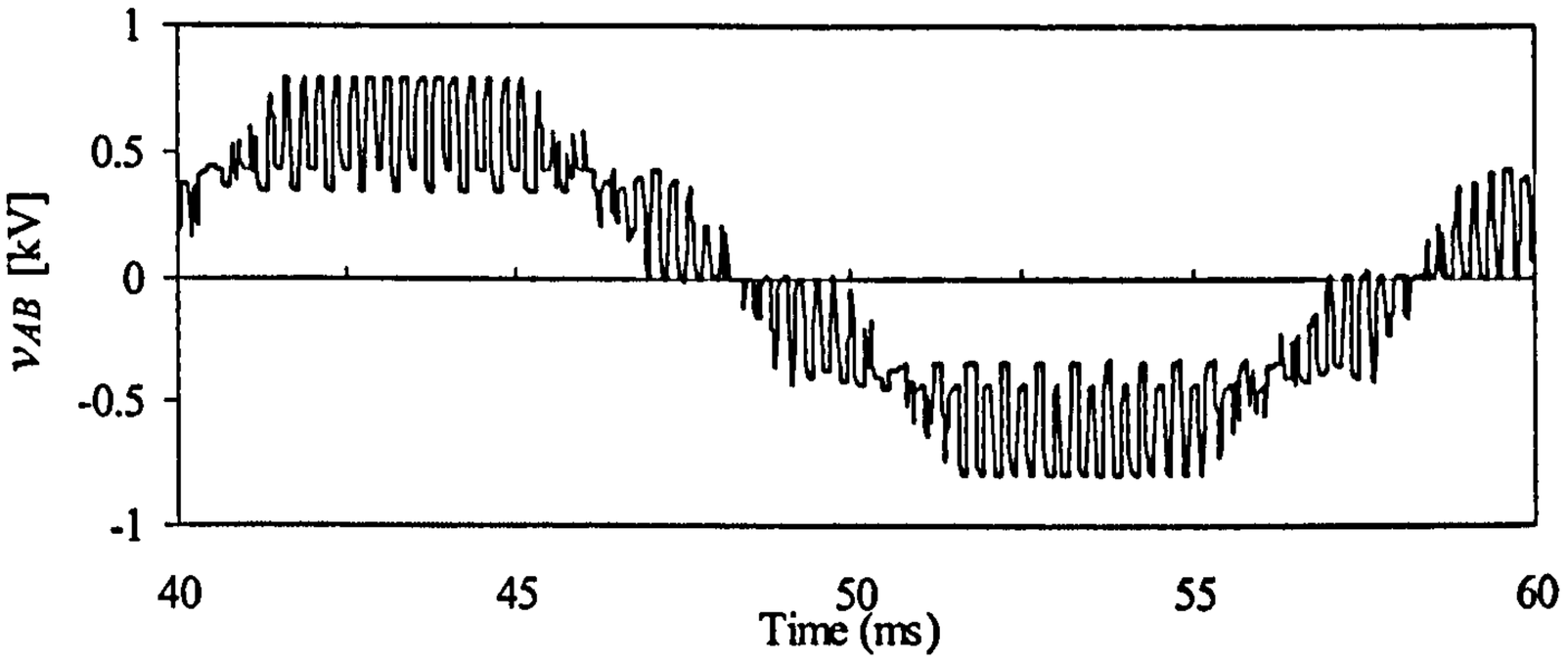
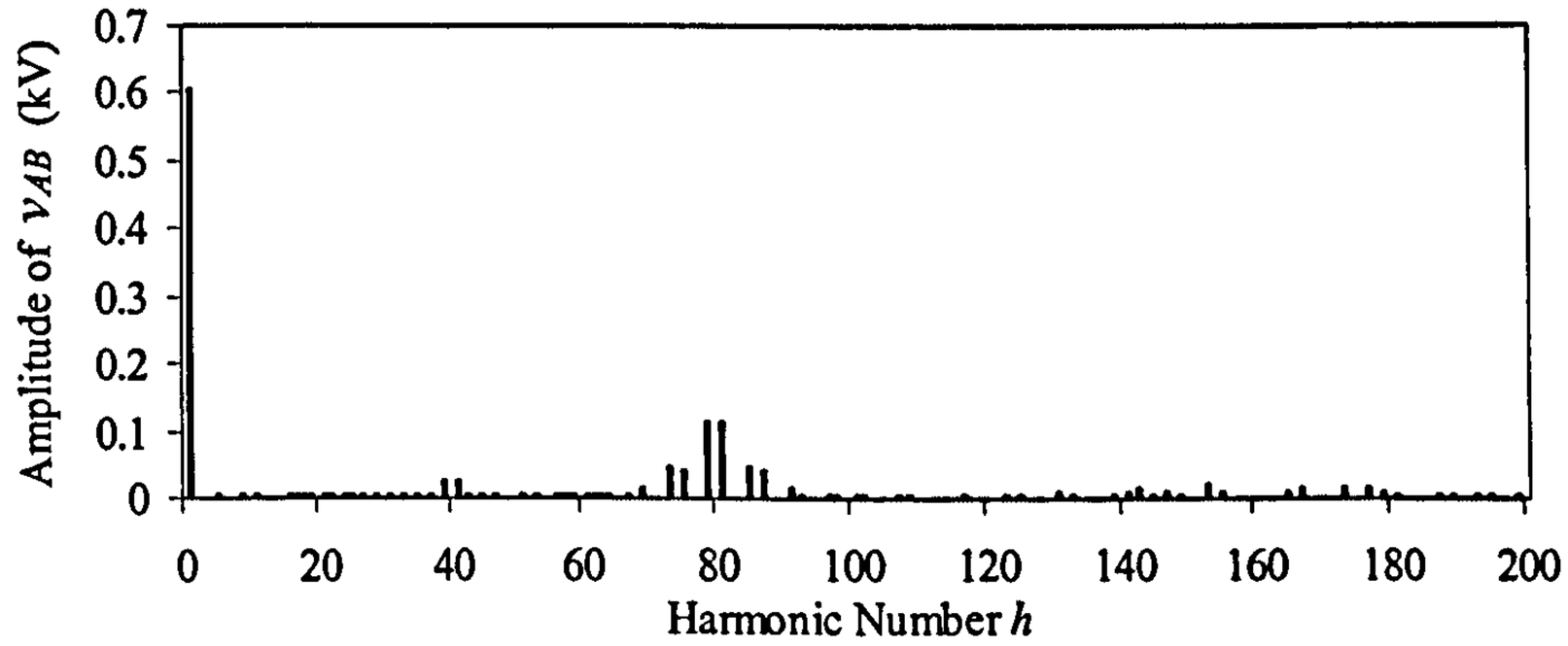


Fig. 4.12: Simulation results with the CD-MSPWM method at m_a=0.9, m_f=20, V_{dc}=800 V, f_o=50 Hz. (a) Line-to-line output voltage v_{AB} waveform. (b) Harmonic spectrum of v_{AB}. (c) Load current i_a waveform. (d) Waveforms of flying capacitor voltages.

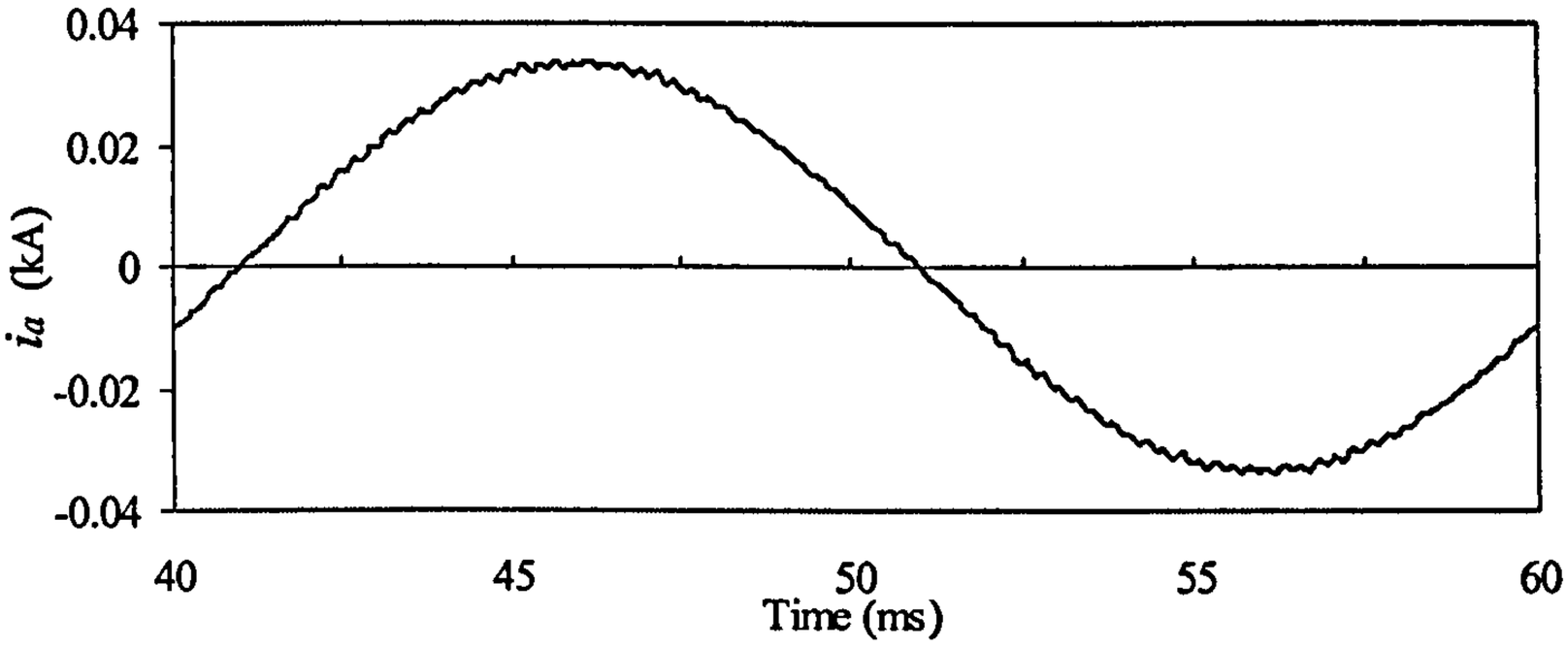
(a)



(b)



(c)



(d)

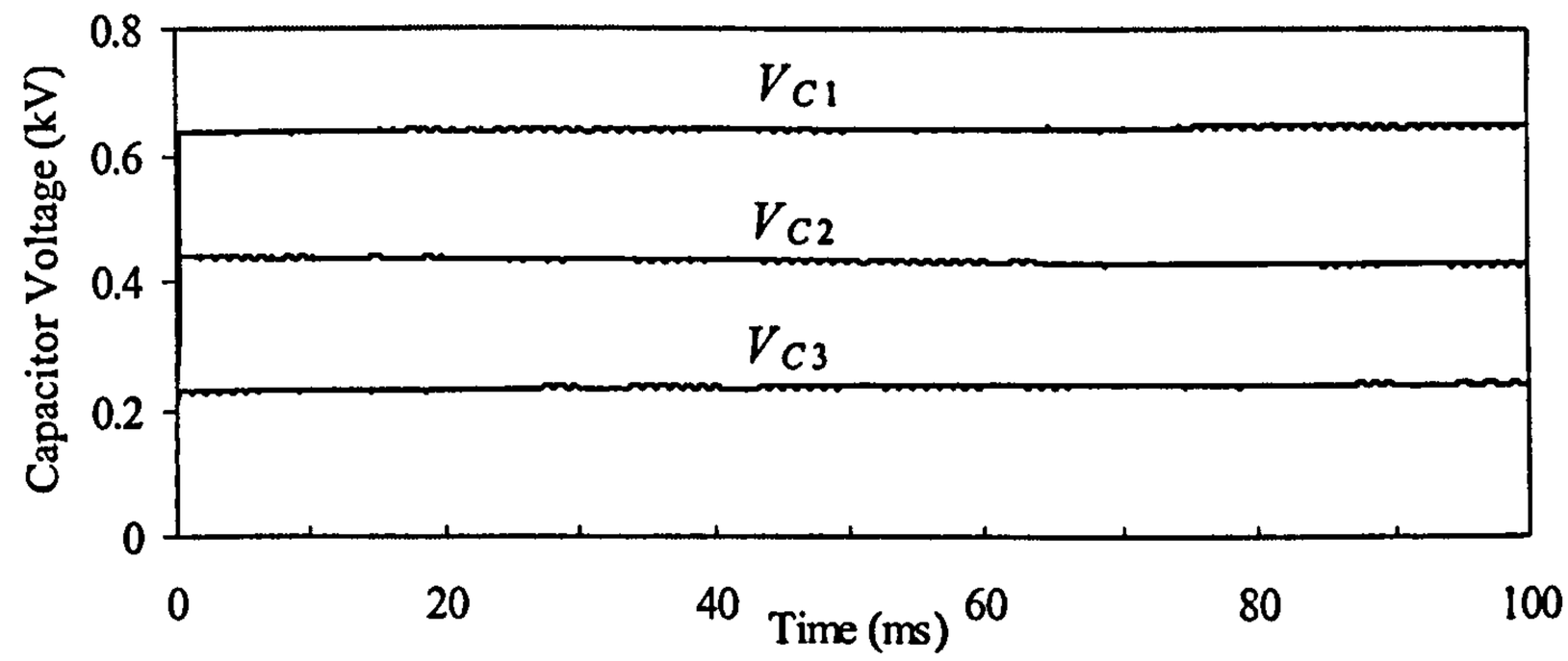


Fig. 4.13: Simulation results with the SFO-PS-PWM method at m_a=0.9, m_f=20, f_o=50 Hz, V_{dc}=800 V. (a) Line-to-line output voltage v_{AB} waveform. (b) Harmonic spectrum of v_{AB}. (c) Load current i_a waveform. (d) Waveforms of flying capacitor voltages.

It is clearly seen from these simulation results that the PS-MSPWM and the new carrier-based SPWM methods can keep the capacitor voltages reasonably balanced, while the CD-MSPWM technique does not have such a feature due to the lack of switching redundancy. Compared with the new SPWM method, the PS-MSPWM has better self-balancing property than the new SPWM method. By examining the harmonic spectrum of the line-to-line voltage v_{AB}, the first large harmonic set is located in m_f under the CD-MSPWM, in $4m_f$ under either the PS-MSPWM or the new SPWM method. Though the PS-MSPWM has slightly different harmonic spectrum from the new SPWM method, their THD is very close, which can be seen from Table 4.4 and Fig. 4.10 and Fig. 4.11. Additionally, it can be seen from Table 4.4 that SFO-PWM technique increases the output linearity range from the normal 1.0 to 1.15 p.u.

4.6 Conclusions

Unlike NPC converters, FC converters have multiple switching patterns, therefore accommodating different control methods such as the PS-MSPWM, the new SPWM method and the CD-MSPWM method. However, CD-MSPWM methods cannot keep the voltage balancing of flying capacitors. It is impractical if no other control circuitry is added to solve the voltage- balancing problem.

In contrast, the PS-MSPWM and the new SPWM methods both have self-balancing abilities due to their switching redundancy. They can make the conduction losses of the devices equal and have good switch utilisation.

Comparing with the PS-MSPWM method, the new SPWM method has similar waveform of the line-to-line output voltage as that of the PS-MSPWM method and close THD content, except for the harmonic spectrum. The new SPWM technique places high harmonic energy at $4f_c$, while the PS-MSPWM does on the sidebands of $4f_c$. Although the new SPWM does not provide better harmonic performance than the PS-MSPWM method with a little more complex implementation, it has the same switching losses as that of the CD-MSPWM technique, one quarter of that of the PS-MSPWM. Considering the switching losses reduction and the self-balancing property, the new SPWM method is a good choice to control the FC converters.

Chapter 5: Modified Phase Shifted SPWM Technique

5.1 Introduction

It is well known that the flying capacitor voltages must be carefully controlled for a number of reasons. Firstly, the quality of the output voltage waveform will deteriorate and secondly, and more importantly, the blocking voltages imposed on certain devices may increase beyond the rated values. If a voltage unbalance occurs, the power devices cannot be guaranteed safe operation and the line-to-line output voltage will have high harmonic distortion. Therefore, the balancing of flying capacitor voltages is quite important and dictates both the safe and efficient operation of the converter [91] [92].

This chapter presents a novel control strategy addressing the problem of capacitor voltage unbalancing in five-level multilevel FC converters. Since this new proposed closed-loop control method consists of the PS-MSPWM technique and a novel voltage balancing control algorithm, it is called a Modified Phase-Shifted SPWM (MPS-SPWM) technique. Firstly, the PS-MSPWM technique and its limitation are described in Section 5.2. Secondly, the MPS-SPWM technique is proposed and its implementation procedure is described in detail in Section 5.3. Then simulation results are given to verify the feasibility of the proposed new method. The effect of this new control method on the performance of the converter is examined by comparison with the PS-MSPWM technique in Section 5.4. Finally conclusions are drawn in Section 5.5.

5.2 PS-MSPWM Method's Features and Limitation

The PS-MSPWM method is regarded as an effective control method for the multilevel FC converter since it has self-balancing property when applied to an ideal and symmetrical circuit. Compared with other PWM methods, it is easier to balance the capacitor voltage in a relatively short time. However, in practice, there are influences due to the non-ideal nature of the devices, such as unequal capacitor leakage currents, unequal delays in switching and asymmetrical charging of the capacitor during transients and disturbances. These effects contribute to the divergence of the capacitor voltages from their nominal values, resulting in some being either higher or lower than their steady-state values. Thus,

an external control loop, besides the PS-MSPWM method is required to balance the voltage of the capacitors. The integration of an external loop with self-balancing properties is an issue that needs to be further investigated [51].

It can be seen from Fig. 4.4 that PS-MSPWM control scheme produces the symmetrical switching control signals which can maintain the capacitor voltage to a certain degree by applying the same time of the charging and the discharging switching states. That is why the PS-MSPWM method with the self-balancing property was suggested and widely used for FC converters [20], [57].

However, despite the symmetrical control scheme, the voltage unbalance of the flying capacitor in practical implementations may be observed as shown in Fig. 5.3. This is mainly due to unequal parameters of the converter caused by different IGBT tolerances, different *dv/dt* and different values of flying capacitors, etc. Therefore, a feedback loop is required to eliminate the accumulative error and make the capacitor voltages stabilize at the desired reference value.

5.3 Modified PS SPWM Technique

This section proposes a novel control strategy named the MPS-SPWM technique for the problem of capacitor voltage unbalancing in five-level flying capacitor multilevel converters. Specifically, the proposed closed-loop control method consists of the PS-MSPWM technique and a novel voltage balancing control algorithm that is different from the method presented in [58], which changes the duty cycle of the switching pattern.

5.3.1 Building Block of the Voltage Balancing Controller

Fig. 5.1 illustrates the building block of the controller used for voltage balancing. It consists of Proportional Integral (PI) controllers and a balancing control algorithm. This novel algorithm is addressed in this section. Here, the reference voltages V_{C3}^{*}, V_{C2}^{*}, V_{C1}^{*} for the three flying capacitors in the five-level FC converter are $V_{dc}/4$, $V_{dc}/2$ and $3V_{dc}/4$ respectively. The actual average values of V_{C3}, V_{C2}, V_{C1} measured by the sensors are compared with their reference values and their respective errors fed into the PI controllers. The outputs of the PI controllers are multiplied with the sign of the output current i_o to generate the adjusting time Δt_3, Δt_2, and Δt_1 for the flying capacitors $C3$, $C2$ and $C1$. The

load current direction must be considered since it determines the capacitor charging and discharging modes for the same switching state.

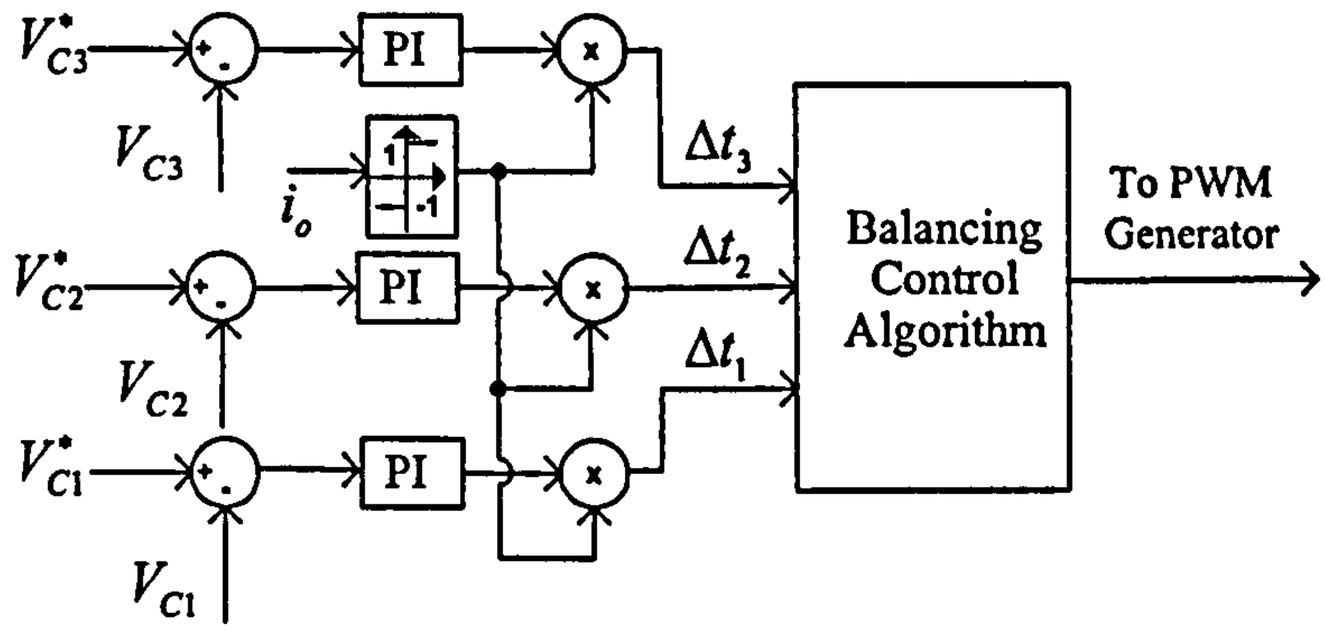


Fig. 5.1: Building block of the voltage balancing controller for the single-phase five-level FC converter.

The aims of the balancing control algorithm can be summarised as follows:

Task 1:Selecting the related switching states used for compensating the voltage perturbation for every flying capacitor in terms of different regions.

Task 2:Calculating the adjusting time Δt for every selected switching state taking Δt_3, Δt_2, Δt_1 into account.

Task 3:Calculating the time interval for every selected switching state after adjustment.

Task 4:Adjusting the time interval of selected switching state by subtracting Δt.

5.3.2 Implementation of the Voltage Balancing Control Algorithm

Task 1

As illustrated in Fig. 4.4, there are four regions in terms of the value of the modulating reference waveform. For every region, different switching states are selected to compensate the capacitor voltage variation. Taking Fig. 4.4(a) as an example, there are many combinations such as the one that implies that V_{C3} is lower than its reference value while V_{C2} and V_{C1} are balanced in a switching period. By examining the switching state in this region, 1101 discharges $C3$ and charges $C2$. We can reduce the time interval of this state by $\Delta t_3/4$ so that $C3$ discharge time is reduced by $\Delta t_3/4$ which increases V_{C3}. However, such an adjustment affects $C2$ since it makes it to charge for a shorter time. To compensate that, the 1011 switching state can be shorten by $\Delta t_3/4$. It may be noted that adjustment of 1011 leads to affecting $C1$ even though it compensates the influence of adjustment of 1101

on $C2$. Then, let us discuss what happens by changing the 0111 switching state time by $\Delta t_3/4$. By changing the switching state 1101, 1011, and 0111 by $\Delta t_3/4$, we can make the lower V_{C3} increase without affecting V_{C2} and V_{C1} values. Finally, to keep the duty cycle in a switching period unchanged; the switching state 1110 must be increased by $3\Delta t_3/4$. The adjusted waveforms are shown in Fig. 5.2.

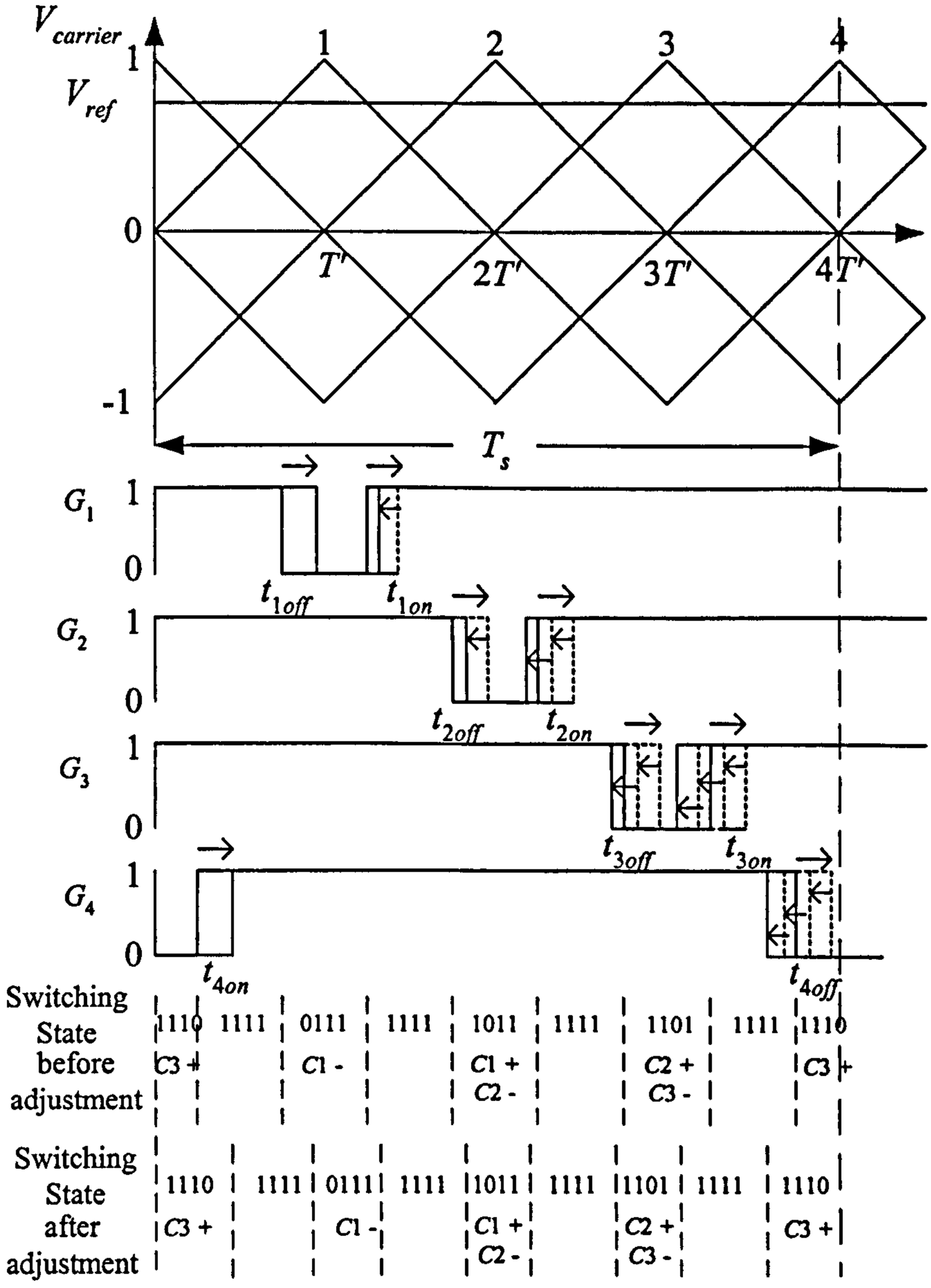


Fig. 5.2: An expanded view of selected switching waveforms after adjustment.

Similarly, V_{C2} and V_{C1} can be adjusted by selecting the appropriate switching states. When the modulating reference value is between 0.5 and 1.0 p.u., their adjustment procedure can be explained as follows:

If V_{C3} is lower then:

- Reduce the state 1101 length by $\Delta t_3/4$ (i.e. $C3$ discharging time decreases, $C2$ charging time also decreases).
- Reduce the state 1011 length by $\Delta t_3/4$ (i.e. $C2$ discharging time decreases, $C1$ charging time also decreases).
- Reduce the state 0111 length by $\Delta t_3/4$ (i.e. $C1$ discharging time decreases).
- Increase the state 1110 length by $3\Delta t_3/4$ (i.e. $C3$ charging time increases).

If V_{C2} is lower then:

- Increase the state 1101 length by $\Delta t_2/2$ (i.e. $C2$ charging time increases, $C3$ discharging time also increases).
- Increase the state 1110 length by $\Delta t_2/2$ (i.e. $C3$ charging time increases).
- Reduce the state 1011 length by $\Delta t_2/2$ (i.e. $C2$ discharging time decreases, $C1$ charging time also decreases).
- Reduce the state 0111 length by $\Delta t_2/2$ (i.e. $C1$ discharging time decreases).

If V_{C1} is lower then:

- Increase the state 1011 length by $\Delta t_1/4$ (i.e. $C1$ charging time increases, $C2$ discharging time also increases).
- Increase the state 1101 length by $\Delta t_1/4$ (i.e. $C2$ charging time increases, $C3$ discharging time also increases).
- Increase the state 1110 length by $\Delta t_1/4$ (i.e. $C3$ charging time increases).
- Reduce the state 0111 length by $3\Delta t_1/4$ (i.e. $C1$ discharging time decreases).

When the modulating reference value varies from –1.0 to 1.0 p.u., the adjustment procedure of some selected switching states is summarized in Table 5.1. The outputs of the PI controllers for different capacitors are Δt_3, Δt_2, Δt_1 respectively. Table 5.1 lists the allocation of Δt_3, Δt_2, Δt_1 to the selected switching states. Such a proposed allocation strategy can guarantee the duty cycle of the output voltage in one switching period to remain unchanged so that it does not affect the overall system characteristics. In addition, this strategy controls each capacitor voltage without affecting the others.

Task 2

From Table 5.1, the adjusting time for every selected switching state taking all the flying capacitor's influence into account can be obtained and listed in Table 5.2.

Table 5.1: Adjustment of selected switching states for individual capacitors

p.u.		Switching States/Adjusting Time					
0.5 to 1.0		1101	1011	0111	1110	1100	0011
	$C3$	$-\Delta t_3/4$	$-\Delta t_3/4$	$-\Delta t_3/4$	$3\Delta t_3/4$		
	$C2$	$\Delta t_2/2$	$-\Delta t_2/2$	$-\Delta t_2/2$	$\Delta t_2/2$		
	$C1$	$\Delta t_1/4$	$\Delta t_1/4$	$-3\Delta t_1/4$	$\Delta t_1/4$		
0.0 to 0.5	$C3$	$-\Delta t_3/4$	$-\Delta t_3/4$	$-\Delta t_3/4$	$3\Delta t_3/4$		
	$C2$					$\Delta t_2/2$	$-\Delta t_2/2$
	$C1$	$\Delta t_1/4$	$\Delta t_1/4$	$-3\Delta t_1/4$	$\Delta t_1/4$		
-0.5 to 0.0		0010	0100	1000	0001	0011	1100
	$C3$	$\Delta t_3/4$	$\Delta t_3/4$	$\Delta t_3/4$	$-3\Delta t_3/4$		
	$C2$					$-\Delta t_2/2$	$\Delta t_2/2$
	$C1$	$-\Delta t_1/4$	$-\Delta t_1/4$	$3\Delta t_1/4$	$-\Delta t_1/4$		
-1.0 to -0.5	$C3$	$\Delta t_3/4$	$\Delta t_3/4$	$\Delta t_3/4$	$-3\Delta t_3/4$		
	$C2$	$-\Delta t_2/2$	$\Delta t_2/2$	$\Delta t_2/2$	$-\Delta t_2/2$		
	$C1$	$-\Delta t_1/4$	$-\Delta t_1/4$	$3\Delta t_1/4$	$-\Delta t_1/4$		

Table 5.2: The adjusting time of selected switching states as well as their time interval

Reference Value (p.u.)	Switching States	Adjust time Δt	Maximum width T_{max}
0.5 to 1.0	1101	$-\Delta t_3/4+\Delta t_2/2+\Delta t_1/4$	$(2-2\cdot V_{ref})\cdot T'$
	1011	$-\Delta t_3/4-\Delta t_2/2+\Delta t_1/4$	$(2-2\cdot V_{ref})\cdot T'$
	0111	$-\Delta t_3/4-\Delta t_2/2-3\Delta t_1/4$	$(2-2\cdot V_{ref})\cdot T'$
	1110	$3\Delta t_3/4+\Delta t_2/2+\Delta t_1/4$	$(2-2\cdot V_{ref})\cdot T'$
0.0 to 0.5	1101	$-\Delta t_3/4+\Delta t_1/4$	$2\cdot V_{ref}\cdot T'$
	1011	$-\Delta t_3/4+\Delta t_1/4$	$2\cdot V_{ref}\cdot T'$
	0111	$-\Delta t_3/4-3\Delta t_1/4$	$2\cdot V_{ref}\cdot T'$
	1110	$3\Delta t_3/4+\Delta t_1/4$	$2\cdot V_{ref}\cdot T'$
	0011	$-\Delta t_2/2$	$(1-2\cdot V_{ref})\cdot T'$
	1100	$\Delta t_2/2$	$(1-2\cdot V_{ref})\cdot T'$
-0.5 to 0.0	0010	$\Delta t_3/4-\Delta t_1/4$	$-2\cdot V_{ref}\cdot T'$
	0100	$\Delta t_3/4-\Delta t_1/4$	$-2\cdot V_{ref}\cdot T'$
	1000	$\Delta t_3/4+3\Delta t_1/4$	$-2\cdot V_{ref}\cdot T'$
	0001	$-3\Delta t_3/4-\Delta t_1/4$	$-2\cdot V_{ref}\cdot T'$
	0011	$-\Delta t_2/2$	$(1+2\cdot V_{ref})\cdot T'$
	1100	$\Delta t_2/2$	$(1+2\cdot V_{ref})\cdot T'$
-1.0 to -0.5	0010	$\Delta t_3/4-\Delta t_2/2-\Delta t_1/4$	$(2+2\cdot V_{ref})\cdot T'$
	0100	$\Delta t_3/4+\Delta t_2/2-\Delta t_1/4$	$(2+2\cdot V_{ref})\cdot T'$
	1000	$\Delta t_3/4+\Delta t_2/2+3\Delta t_1/4$	$(2+2\cdot V_{ref})\cdot T'$
	0001	$-3\Delta t_3/4-\Delta t_2/2-\Delta t_1/4$	$(2+2\cdot V_{ref})\cdot T'$

Task 3

If the modulating reference value V_{ref} is known, T' is defined as: $T' = T_s / 4$, and it is easy to calculate the switching time points for every switch in terms of the following equations: (for the first carrier period)

$$t_{1off} = V_{ref} \cdot T' \tag{5-1}$$

$$t_{1on} = (2 - V_{ref}) \cdot T' \tag{5-2}$$

$$t_{2off} = (1 + V_{ref}) \cdot T' \tag{5-3}$$

$$t_{2on} = (3 - V_{ref}) \cdot T' \tag{5-4}$$

$$t_{3off} = (2 + V_{ref}) \cdot T' \tag{5-5}$$

$$t_{3on} = (4 - V_{ref}) \cdot T' \tag{5-6}$$

$$t_{4off} = (3 + V_{ref}) \cdot T' \tag{5-7}$$

$$t_{4on} = (1 - V_{ref}) \cdot T' \tag{5-8}$$

When V_{ref} is between 0.5 and 1.0 p.u., the switch turn on and turn off time instants are queuing from the smallest to the greatest is shown in Fig. 5.2. It can be seen that 1101 state covers (t_{3on}-t_{3off}) this period which equals to $(2 - 2 \cdot V_{ref}) \cdot T'$. The maximum width T_{max} (i.e., the switching time interval) is also listed in Table 5.2.

Task 4

Generally speaking, the adjusting time Δt for any switching state should not exceed its maximum width T_{max}. If Δt is greater than the state maximum width, it must be normalized to its maximum width T_{max} by multiply it by a coefficient of $T_{max}/\Delta t$ value. Moreover, all the other adjusting times are also multiplied by the same coefficient to guarantee the overall adjusting time in any level being zero.

5.4 Simulation Results

To verify the performance of the voltage balancing control algorithm, a simulation is carried out for the single-phase five-level FC converter under the MPS-SPWM control method and the PS-MSPWM method. The various parameters of the simulated system are:

V_{dc}=800 V, V_{C3}=200 V, V_{C2}=400 V, V_{C1}=600 V, R=10 Ω, L=0.01 H, $C1$=$C2$=$C3$=1000 μF, f_o=50 Hz, f_s=1000 Hz.

Fig. 5.3 shows the flying capacitors' average voltage values versus time with the PS-MSPWM method without the voltage balancing control algorithm. Fig. 5.4 shows the same capacitors' average voltage values versus time for 10 seconds with the MPS-SPWM method. Fig. 5.3 shows the influence of the accumulative error on the FC converter. This error makes the flying capacitor voltage balance at other point instead of the original charged value. Thus, the balancing control method must be used in practical implementation of the FC topology. Fig. 5.4 gives the average voltage values of three flying capacitors with the new balancing control method and verifies the usefulness of this method.

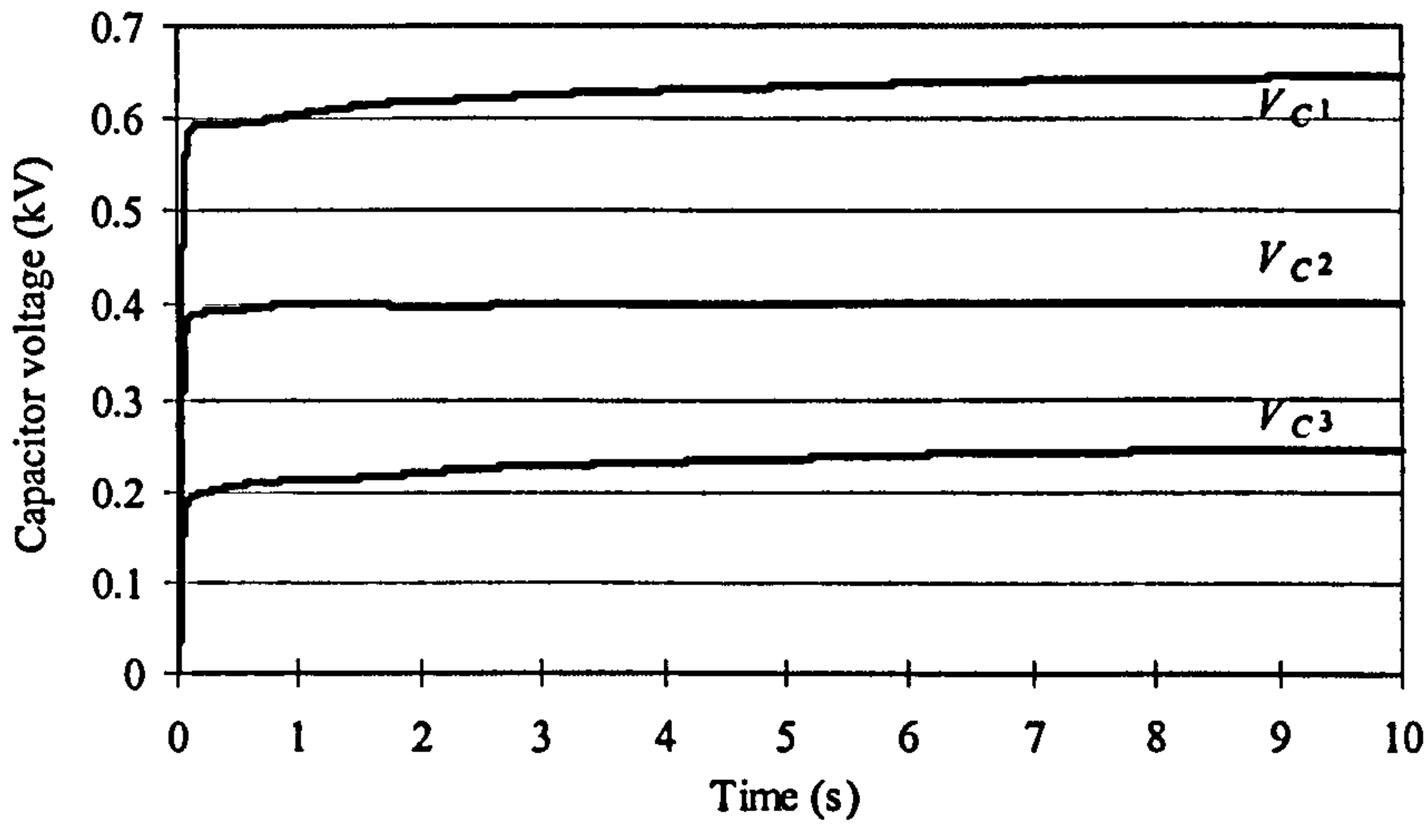


Fig. 5.3: Average voltage values of flying capacitors with the PS-MSPWM technique.
(m_f=20, m_a=0.9, f_o=50 Hz, V_{dc}=0.8 kV)

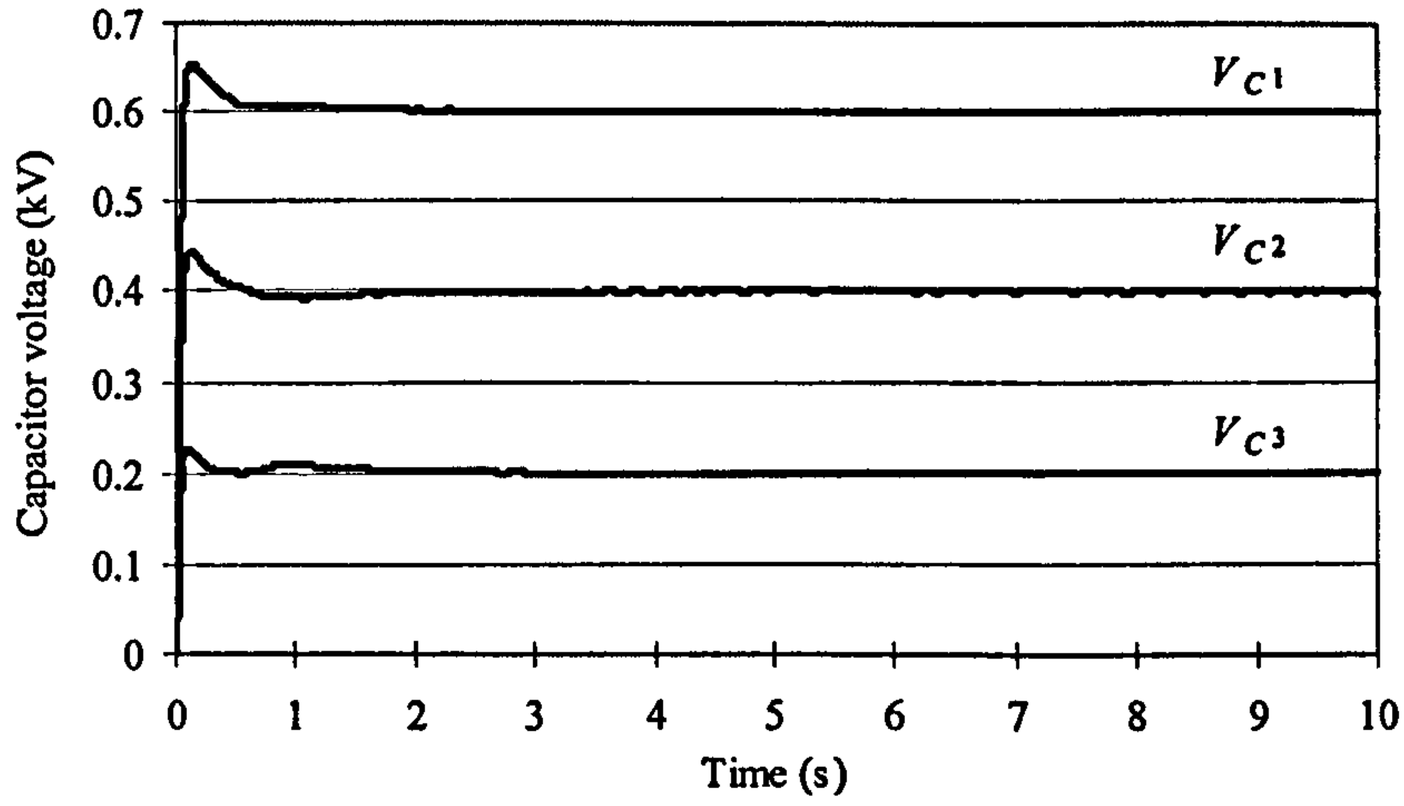


Fig. 5.4: Average voltage values of flying capacitors with the MPS SPWM technique.
(m_f=20, m_a=0.9, f_o=50 Hz, V_{dc}=0.8 kV)

Fig. 5.5 shows the output phase voltage v_{AO} waveform with the PS-MSPWM technique, while Fig. 5.6 shows the v_{AO} waveform with the MPS-SPWM technique. Fig. 5.7 illustrates the output phase current i_o waveform with the PS-MSPWM technique, while Fig. 5.8 shows the i_o waveform with the MPS-SPWM technique.

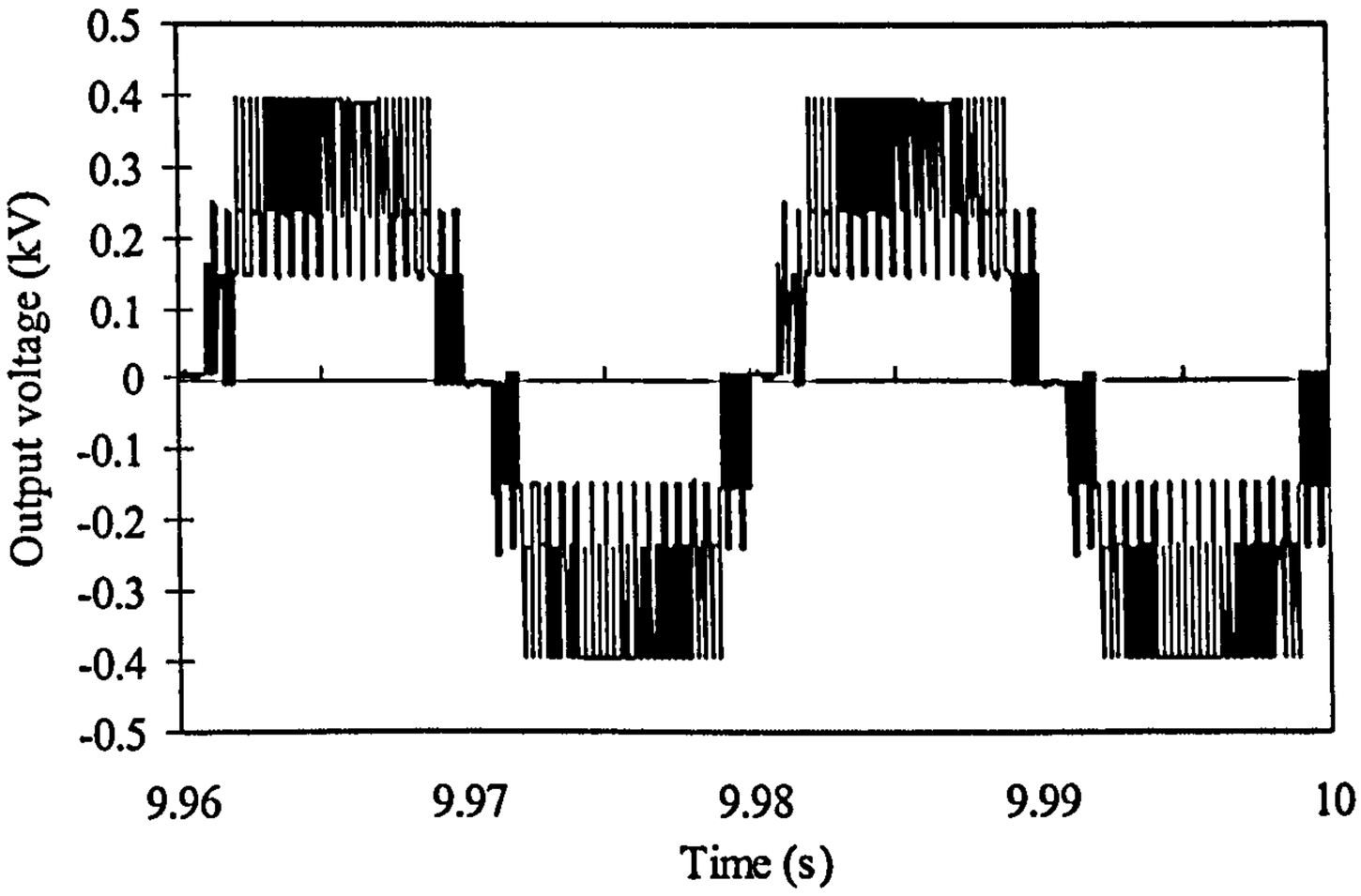


Fig. 5.5: Output phase voltage v_{AO} waveform with the PS-MSPWM technique.
(m_f=20, m_a=0.9, f_o=50 Hz, V_{dc}=0.8 kV)

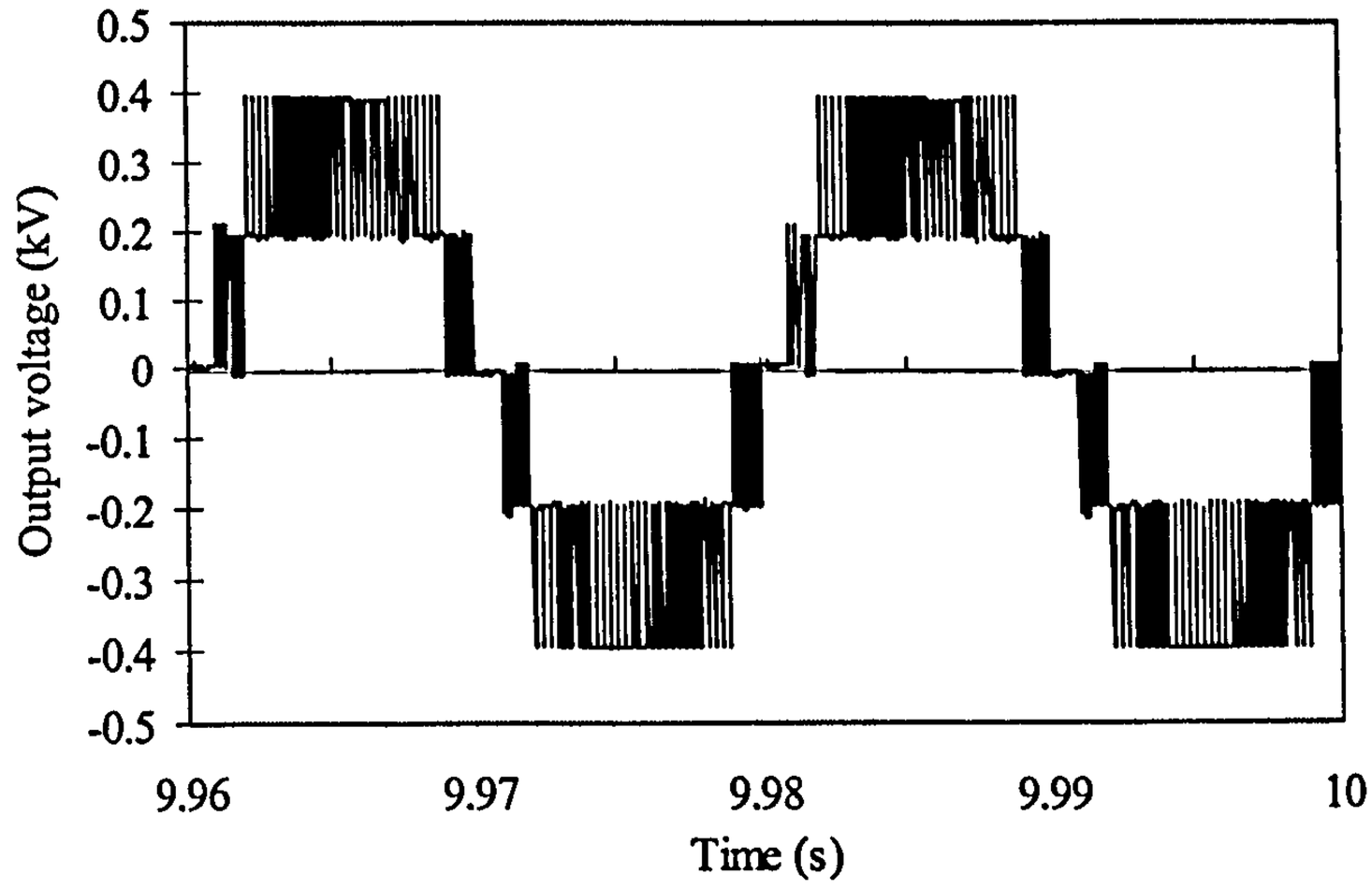


Fig. 5.6: Output phase voltage v_{AO} waveform with the MPS-SPWM technique.
(m_f=20, m_a=0.9, f_o=50 Hz, V_{dc}=0.8 kV)

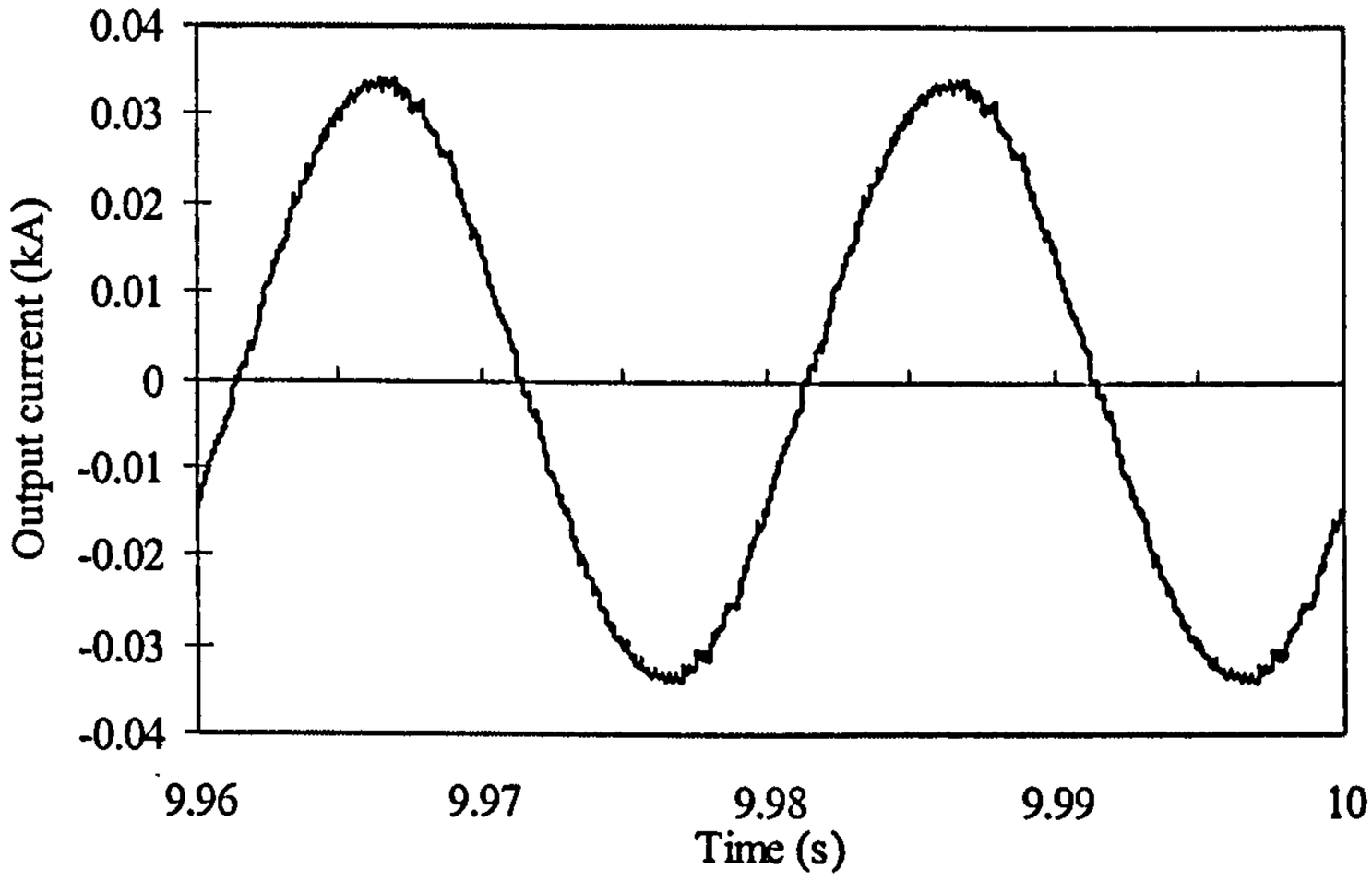


Fig. 5.7: Output phase current i_o waveform with the PS-MSPWM technique.

(m_f=20, m_a=0.9, f_o=50 Hz, V_{dc}=0.8 kV, R=10 Ω, L=0.01 H)

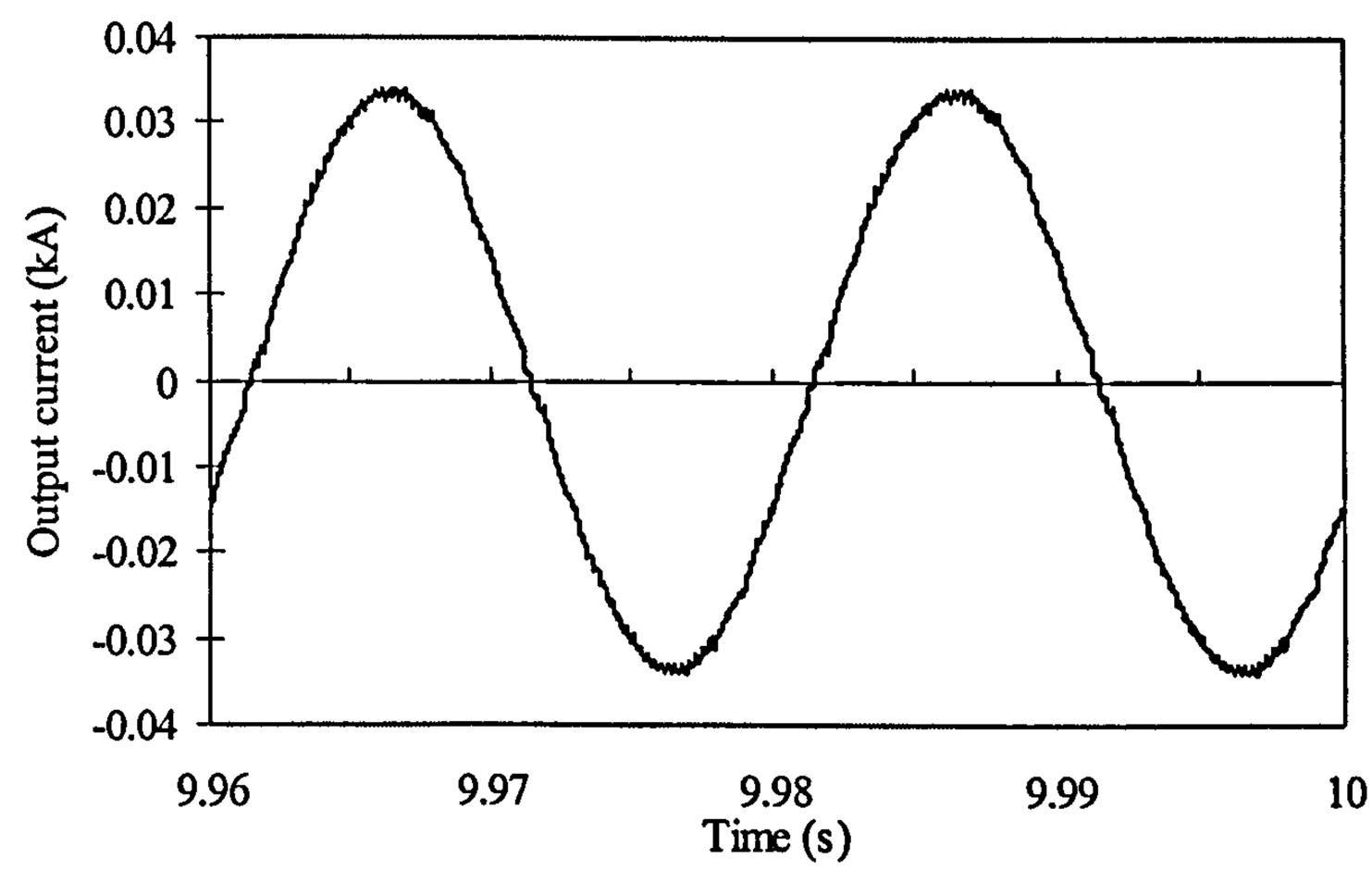


Fig. 5.8: Output phase current i_o waveform with the MPS-SPWM technique.

(m_f=20, m_a=0.9, f_o=50 Hz, V_{dc}=0.8 kV, R=10 Ω, L=0.01 H)

Simulation results shown in Figs. 5.5 to Fig. 5.8 illustrate that the new proposed MPS-SPWM control technique also decreases the voltage/current output waveform harmonic distortion. The THD of the voltage waveform decreases from 9.15% to 7.97% with the proposed control method, and similarly the THD of the current waveform decreases from 1.91% to 1.58%.

5.5 Conclusions

The unbalancing problem is observed in the five-level FC converter under the PS-MSPWM control method. A novel closed-loop MPS-SPWM method is proposed for the five-level flying capacitor converter. This closed-loop method consists of PI controllers and a voltage balancing algorithm to compensate the capacitor voltage deviation by adjusting the selected switching states' switching time interval.

In summary, this voltage-balancing algorithm has the following features:

- The overall adjusting time is zero in a switching period in order to keep the duty cycle unchanged, therefore, the output voltage performance is not affected by such an adjustment except that improves the voltage balancing property.
- Each capacitor voltage is adjusted individually; the influence on each other is nil.

This MPS-SPWM technique cannot only solve the capacitor voltage unbalancing problem existing in practical FC converters due to the non-ideal nature of the devices, but it also improves the harmonic performance of the FC converters.

Chapter 6: Multi-Modular Multilevel Converter Systems

6.1 Introduction

A multi-modular converter is usually referred to as a system that consists of many converter modules. These modules are connected in series and /or in parallel to reach higher voltage and current ratings. This kind of converter system has the following advantages [93]:

(1) The system power capacity can be easily increased by adding more converters.

(2) With an appropriate hardware arrangement and management, the overall power conversion efficiency and the life of converter can be increased.

(3) The system's reliability is greatly increased.

Multi-modular converters based on conventional two-level converter have received much interest from researchers due to the above features, as documented in the recent technical literature [19], [43], [93]-[98]. Moreover, hardware prototypes also have been applied for utility applications. For example, the existing 100MVA-size, prototype STATCOMs installation in Japan [99] and USA [100] are based on eight parallel, three-phase, two-level, GTO bridges. The GTOs turn-on once per cycle of the supply frequency and the THD standards are met by harmonic cancellations of the phase-shifted pulses of the eight GTO bridge modules.

As mentioned before, multilevel converters are suitable for high voltage and high power applications. However, it is still considered very challenging to construct a single multilevel converter of a very high number of levels. It is almost impractical and less advantageous to consider multilevel converters with higher than five levels. The reason is that the benefits associated with the harmonic improvements gained by the use of a multilevel system saturate. On the other hand, when the modular converter systems' desirable properties are considered [101], it is almost natural that the multi-modular system concept has been applied to extend the advantages and benefits of the multilevel converters into even higher power applications.

This chapter deals with two different multi-modular multilevel converter systems based on the paralleling of topologies. One is based on the five-level FC converter; the other is

based on the five-level NPC converter. It is assumed that both the FC and the NPC converters have balanced and equal capacitor voltages. The performance of these systems is examined under different control schemes. In addition, since the potential switching losses must also be considered in high power applications, it is necessary to investigate the system's performance in the lower frequency modulation ratio m_f. It is reported that when high-level NPC converters are considered, the FF-SPWM control method is more promising than the multilevel SPWM method with the lower m_f [40], [103]. Therefore, in this chapter two cases are also studied; one uses a relatively high frequency modulation ratio, and the other uses the same frequency for both the reference signal and the carrier signal, i.e. FF-SPWM (m_f=1).

6.2 Multi-modular Multilevel Converter System Circuit

Fig. 6.1 shows the schematic diagram of the multi-modular system consisting of a number of multilevel converters connected in parallel both at the input and at the output side. The reactor L is employed here to change the VSI to the CSI form for the parallel connection.

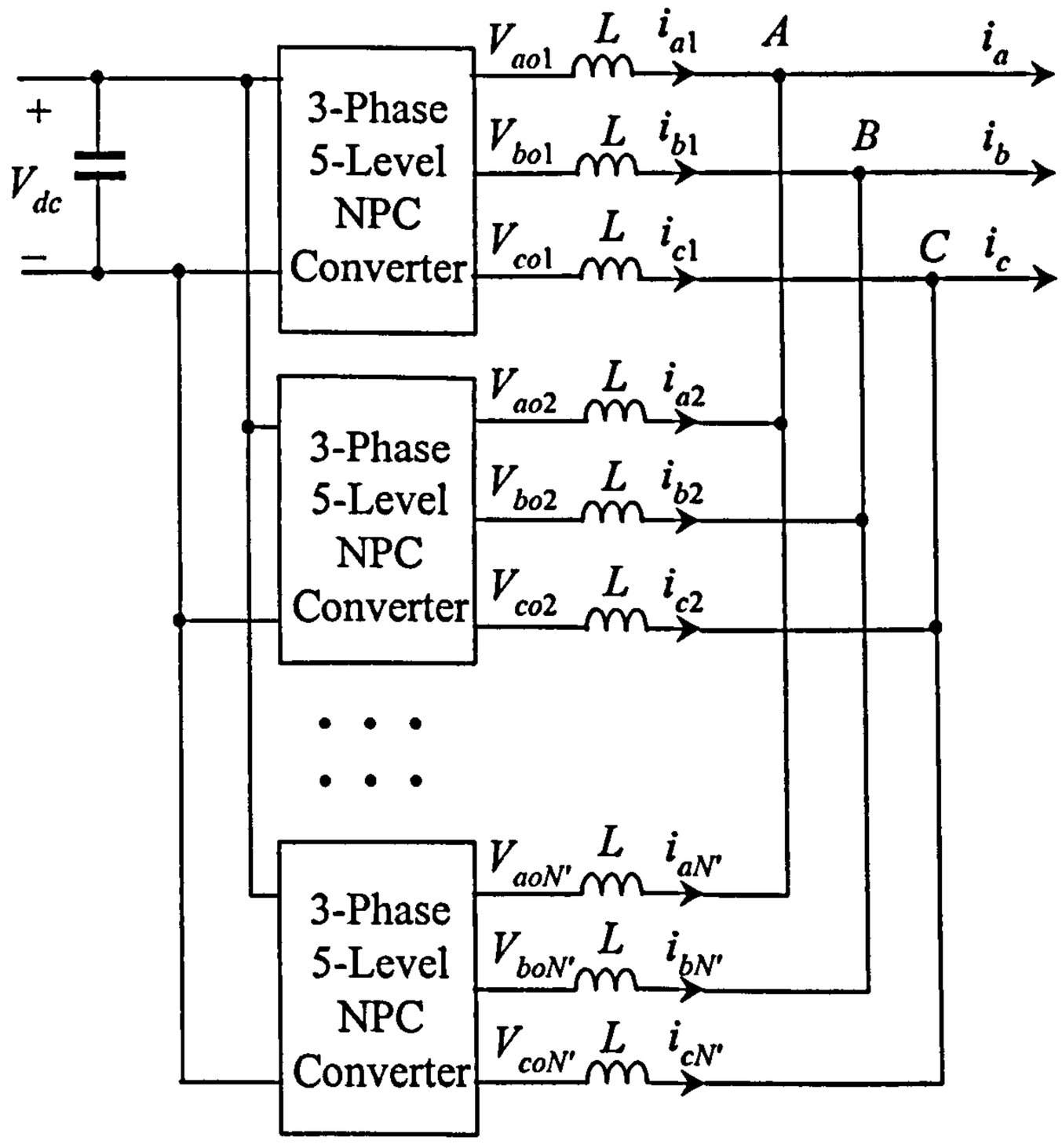


Fig. 6.1: Schematic diagram of a multi-modular converter system.

Its equivalent circuit at fundamental frequency is shown in Fig. 6.2. Here, R and L are the resistance and inductance of the reactor, respectively. V_{aoi1} and i_{ai1} (i=1, 2, ... N') are the fundamental parts of the output voltage and current of the i-th module, respectively. V_{AO1}, i_{af} is the fundamental component of the total output phase voltage and current respectively.

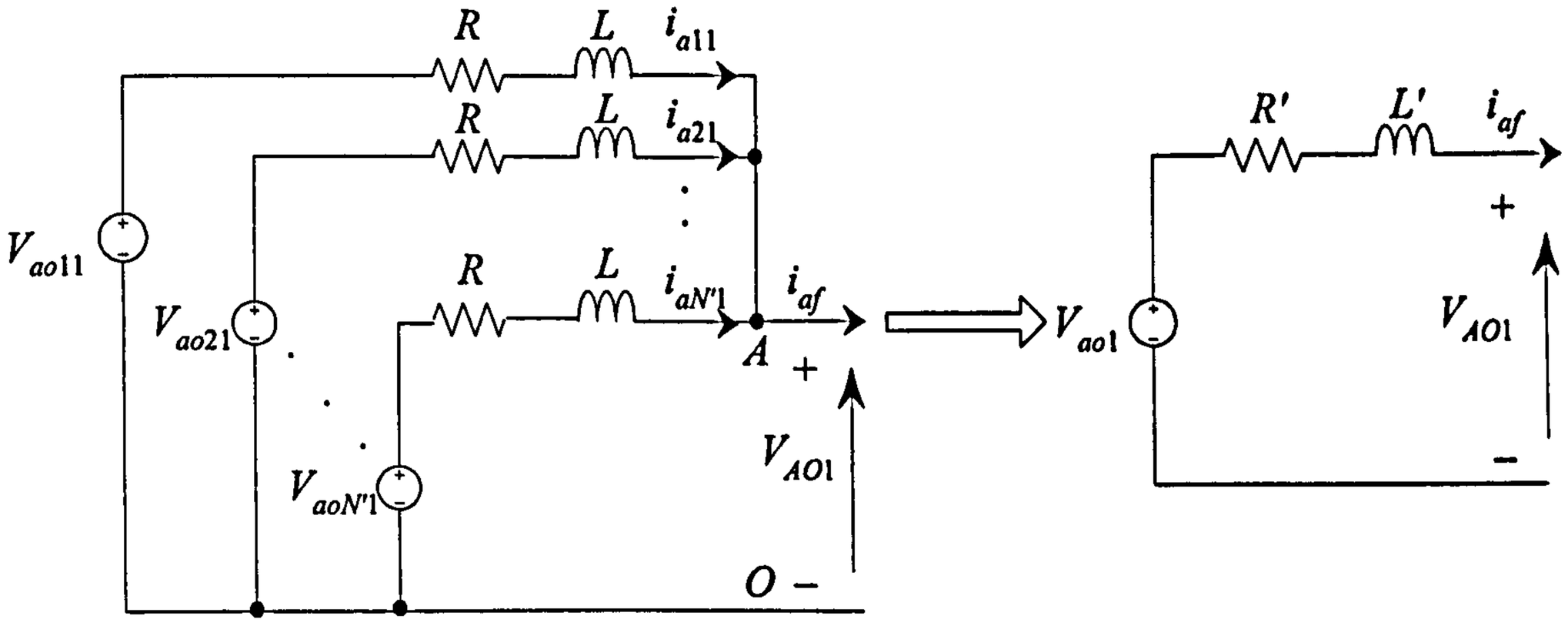


Fig. 6.2: Fundamental equivalent circuit of the parallel connected models in a phase.

$$V_{ao1} = \frac{1}{N'}\sum_{i=1}^{N'} V_{aoi1} \tag{6-1}$$

$$R' = \frac{R}{N'} \tag{6-2}$$

$$L' = \frac{L}{N'} \tag{6-3}$$

$$i_{af} = \sum_{i=1}^{N'} i_{ai1} \tag{6-4}$$

where N' is the number of modules.

6.3 Multi-Modular Flying Capacitor Converter System

Multi-modular systems based on the multilevel five-level FC converter topology are discussed in this section. Three control techniques are studied and their performance is compared against specific criteria. Different types of MSPWM techniques used for each module along with the Phase-Shifted (PS) concept among the different modules are considered. Techniques with high frequency modulation ratio and the FF-SPWM are studied. The THD of the output quantities and the current sharing issue is discussed. Simulation results are presented to support the findings.

6.3.1 Control Schemes

The most attractive feature of the FC converter is that its voltage synthesis has more flexibility than that of the NPC converter, i.e., it has more than one switching states for a given voltage. This feature makes more control methods suitable for the FC converter. On the other hand, the PS-SPWM scheme is widely used in the multiple modules due to its ability to eliminate a significant number of unwanted harmonics.

For the proposed multi-modular system the following three control combinations are examined and discussed in detail next.

PD/PS Control Scheme

This scheme refers to the PD control method for each module. This technique has been shown in Fig. 3.5.

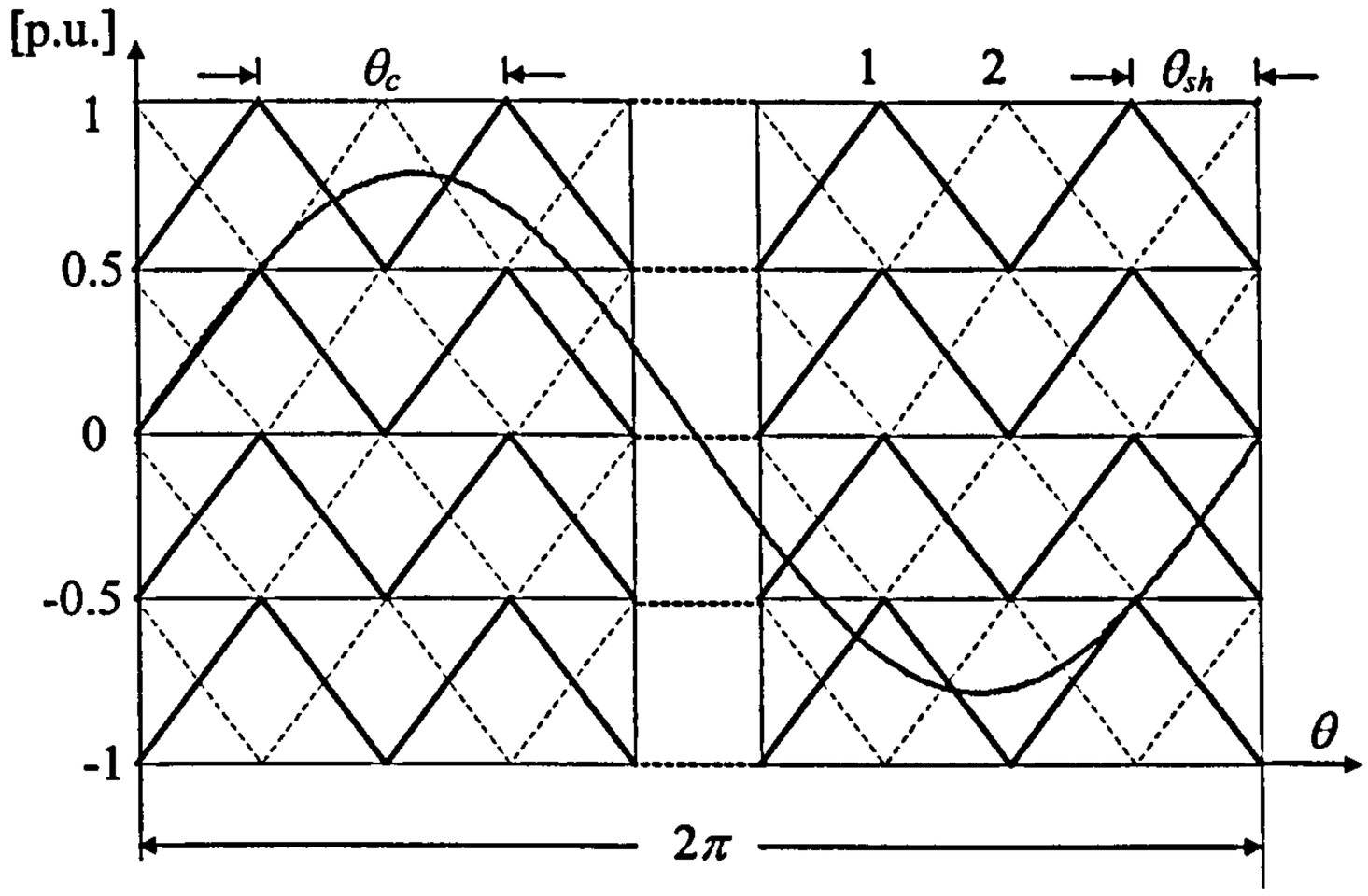


Fig. 6.3: The PD/PS method applied to two modules.

However, due to the availability of more than one module, the PS technique between the various modules is introduced in order to improve the performance of the overall system when harmonics at the system output are concerned. Fig. 6.3 illustrates the PD/PS control scheme as applied to two modules. Here, 1 stands for a set of carriers with solid lines for module 1, 2 stands for a set of carriers with dashed lines for module 2. Each module employs the PD control method. If the modulating period is regarded as 2π, the angle in radians of the carrier period θ_c can be expressed as:

$$\theta_c = \frac{2\pi}{m_f} \tag{6-5}$$

the phase shifting angle θ_{sh} between two adjacent modules is

$$\theta_{sh} = \frac{\theta_c}{N'} \tag{6-6}$$

where N' is the number of modules, and in the example shown N'=2.

PS/PS Control Scheme

The PS/PS control scheme is defined as a combination of the PS-MSPWM method shown in Fig. 3.8 in each module plus the PS technique between the various modules as illustrated in Fig. 6.4.

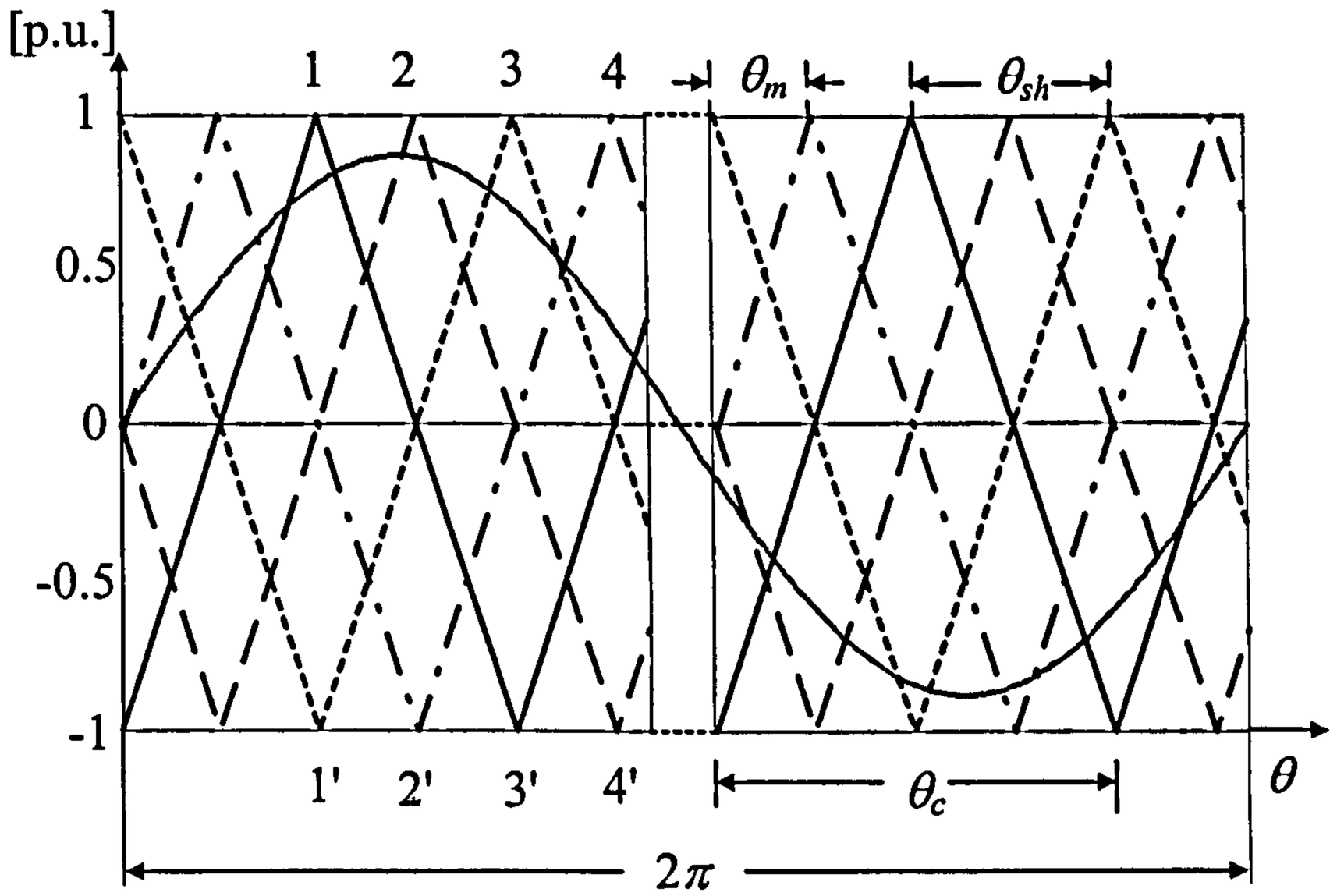


Fig. 6.4: The PS/PS method applied to two modules.

In Fig. 6.4, carriers 1 to 4 belong to module 1 which are phase shifted by θ_m

$$\theta_m = \frac{\theta_c}{4} \tag{6-7}$$

While carriers 1′ to 4′ belong to module 2 which has the same phase shifting angle as the module 1, however, the phase shifting angle between modules is

$$\theta_{sh} = \frac{\theta_c}{N'} \tag{6-8}$$

Where again N' is the number of modules. It should be noted that under the PS/PS method, when the following condition is met:

$$k \cdot N' = m - 1 \tag{6-9}$$

m is the number of levels, N' is the number of modules, k is an integer, k=1,2,3....Then each module's output voltage waveform is identical, no phase shifting exists.

PS Control Scheme

The PS method applied to the whole multi-modular system means that the carriers corresponding to all the upper switches of the system per phase are arranged in sequence and pulsed by a certain degree. Fig. 6.5 shows the PS method applied to two modules. Here, the phase shifting angle is defined as:

$$\theta_{sh} = \frac{\theta_c}{4N'} \tag{6-10}$$

Where N' is again the number of modules.

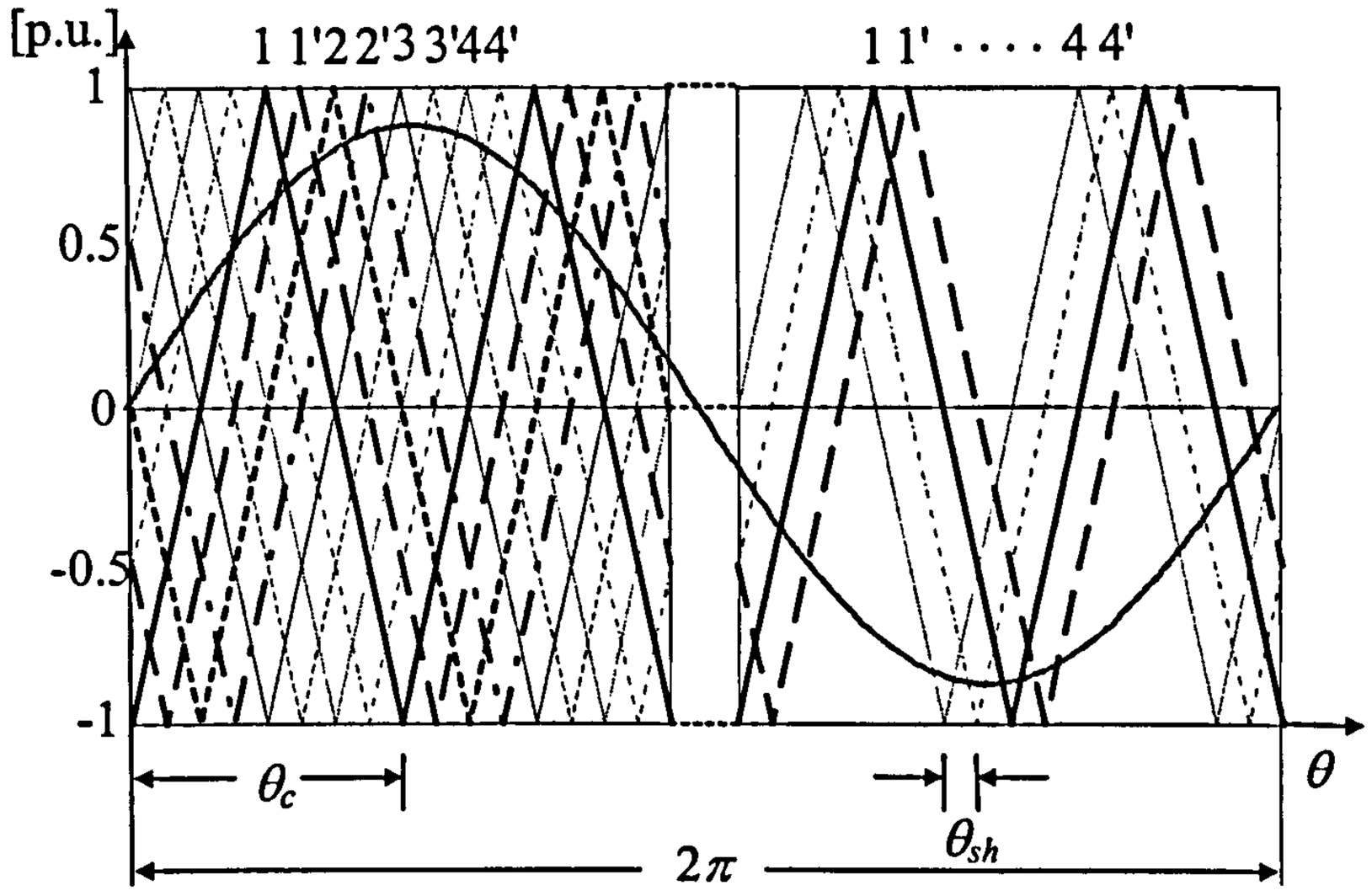


Fig. 6.5: The PS method applied to two modules.

6.3.2 Simulation Results

Simulations have been carried out for parallel connected multi-modular system based on three-phase five-level FC converters. It is assumed that each module has equal and balanced voltage levels. So all the flying capacitors are replaced by corresponding ideal DC sources in the simulation for multi-modular converter system. As mentioned earlier, in order to investigate the feasibility of the FF-SPWM control method, two cases (i.e. higher m_f and m_f=1) are studied. The parameters are as follows:

V_{dc}=0.8 kV, f_o=50 Hz, L=10 mH, Load resistance R_L=10 Ω, the load is Y-connected (star).

Table 6.1 and Table 6.2 summarize the THD and switching losses for the three control schemes at higher m_f and m_f=1. Table 6.1 shows the effect of the three control methods on a system with two modules at m_f=9 and m_a =0.8, while Table 6.2 shows results at m_f=1 and m_a =0.8. Here, N' is the number of modules; N_{3total} indicates the potential switching losses, which is defined as the total number of switching transitions per modulating period for the three-phase system. v_{AB}, v_{BC}, and v_{CA} is the line-to-line voltage, and i_a , i_b , and i_c is the output phase current. Figs. 6.6-6.17 show waveforms of the branch currents (current of each module), output current and voltage of the system, as well as their harmonic spectra with different control methods at N'=2, m_f=9 and m_a =0.8. Figs. 6.6-6.9 depict with the PS/PS method, while Figs. 6.10-6.13 depict with the PD/PS method, Figs. 6.14-6.17 depict with the PS method. Figs. 6.18-6.21 show similar waveforms with the PS method at N'=2, m_f=1 and m_a =0.8.

Table 6.1: Results with the three control methods (N'=2, m_f=9, m_a=0.8, f_o=50 Hz)

Control Methods	PS/PS	PD/PS	PS
N_{3total}	96 m_f	24m_f	96m_f
v_{AB} THD (%)	4.4	3.9	1.0
v_{BC} THD (%)	4.5	3.9	1.0
v_{CA} THD (%)	4.4	3.9	1.0
i_a THD (%)	5.9	5.4	1.4
i_b THD (%)	5.9	5.5	1.4
i_c THD (%)	5.8	5.4	1.4

Table 6.2: Results with the three control methods (N'=2, m_f=1, m_a =0.8, f_o=50 Hz)

Control Methods	PS/PS	PD/PS	PS
N_{3total}	105	92	115
v_{AB} THD (%)	14.6	9.0	14.3
v_{BC} THD (%)	62.5	5.1	61.8
v_{CA} THD (%)	58.1	9.0	58.3
i_a THD (%)	33.3	10.9	33.0
i_b THD (%)	31.8	8.6	31.8
i_c THD (%)	34.4	8.6	34.3

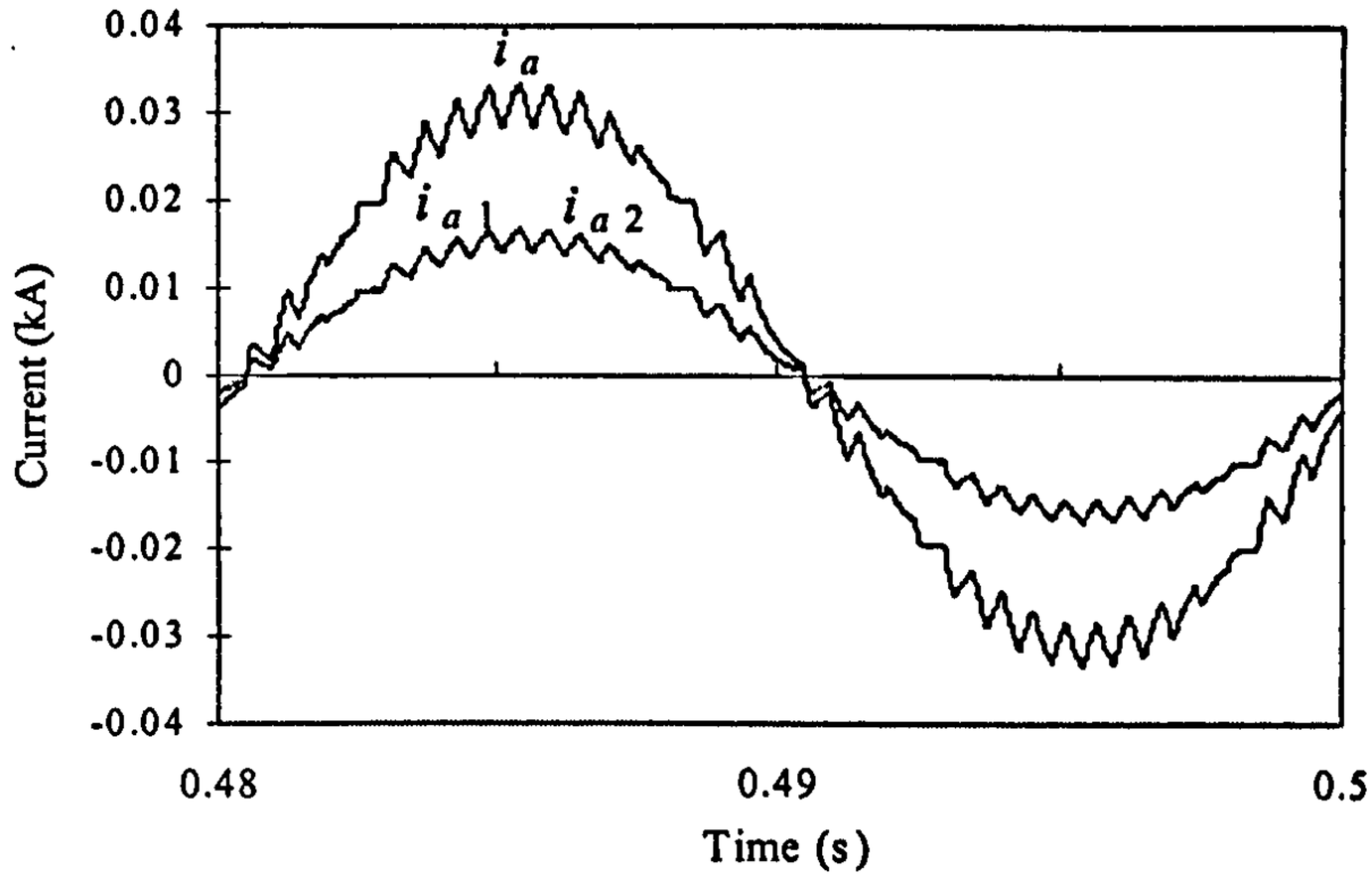


Fig. 6.6: Current waveforms with the PS/PS method at N'=2, m_f=9, m_a=0.8, f_o=50 Hz.

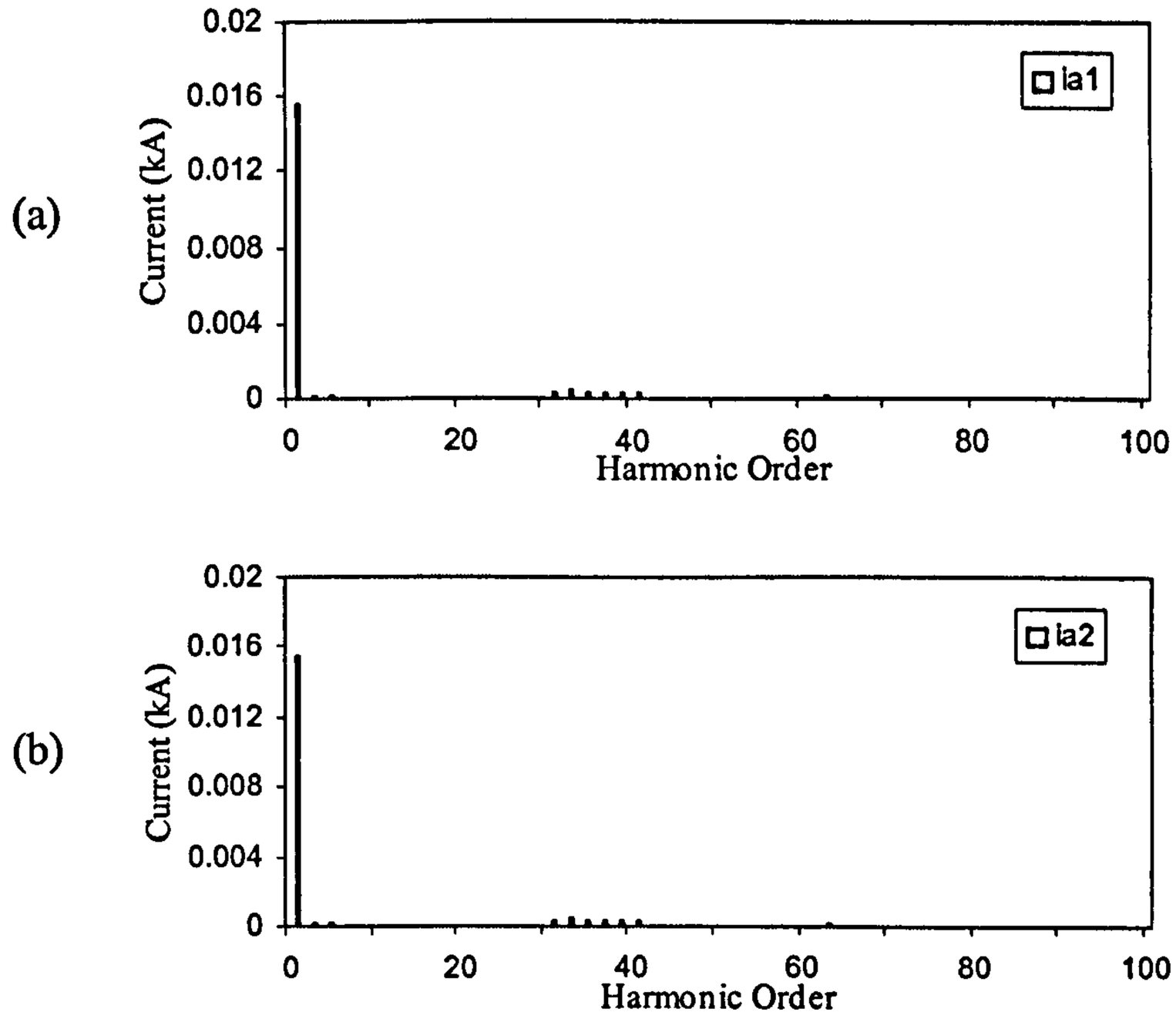


Fig. 6.7: Current harmonic spectra with PS/PS method (N'=2, m_f=9, m_a=0.8, f_o=50 Hz). (a) Harmonic spectra of i_{a1}; (b) Harmonic spectra of i_{a2}; (c) Harmonic spectra of i_a.

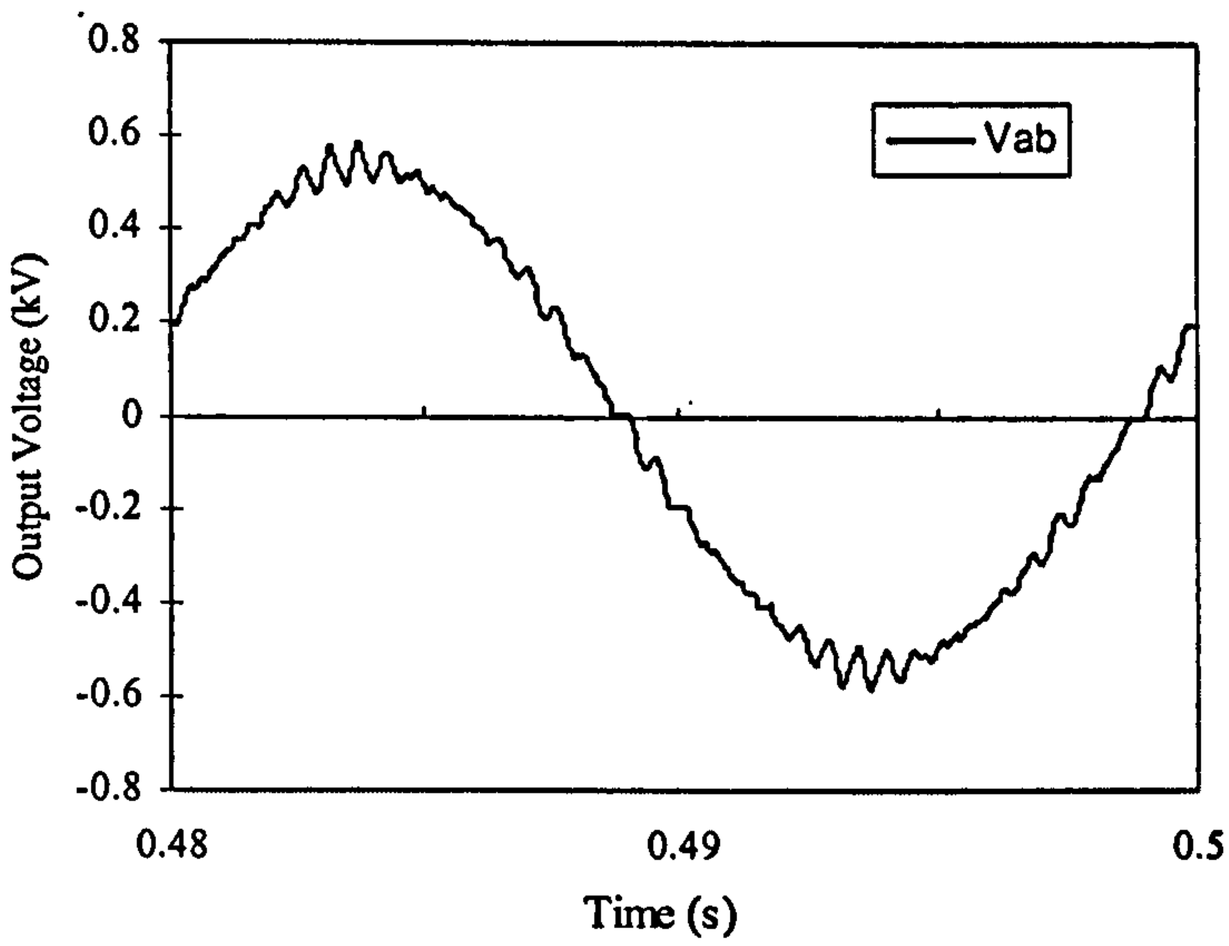


Fig. 6.8: Output line-to-line voltage waveform with the PS/PS method.

(N'=2, m_f=9, m_a=0.8, f_o=50 Hz).

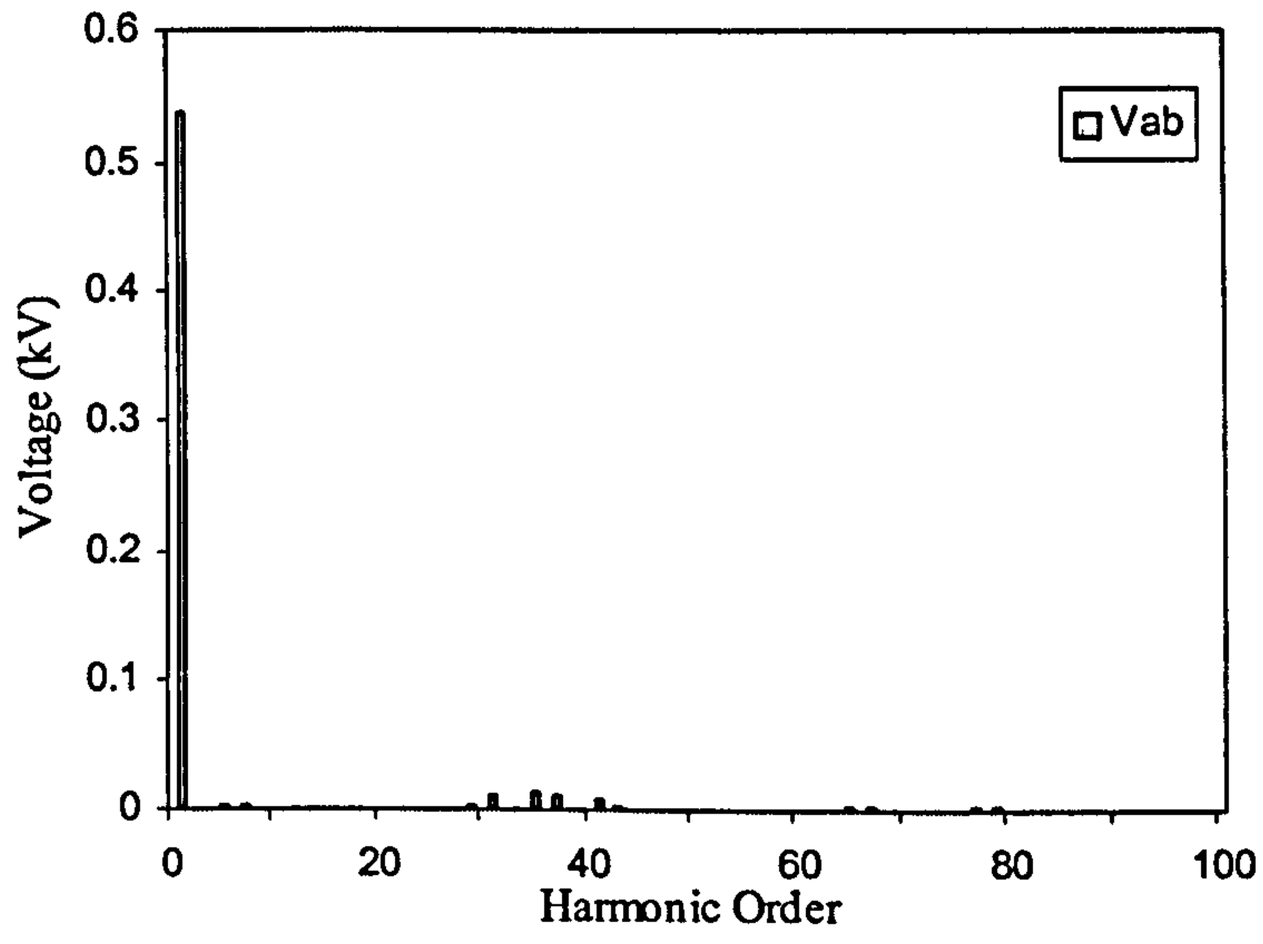


Fig. 6.9: Harmonic Spectra of v_{AB} with the PS/PS method.

(N'=2, m_f=9, m_a=0.8, f_o=50 Hz).

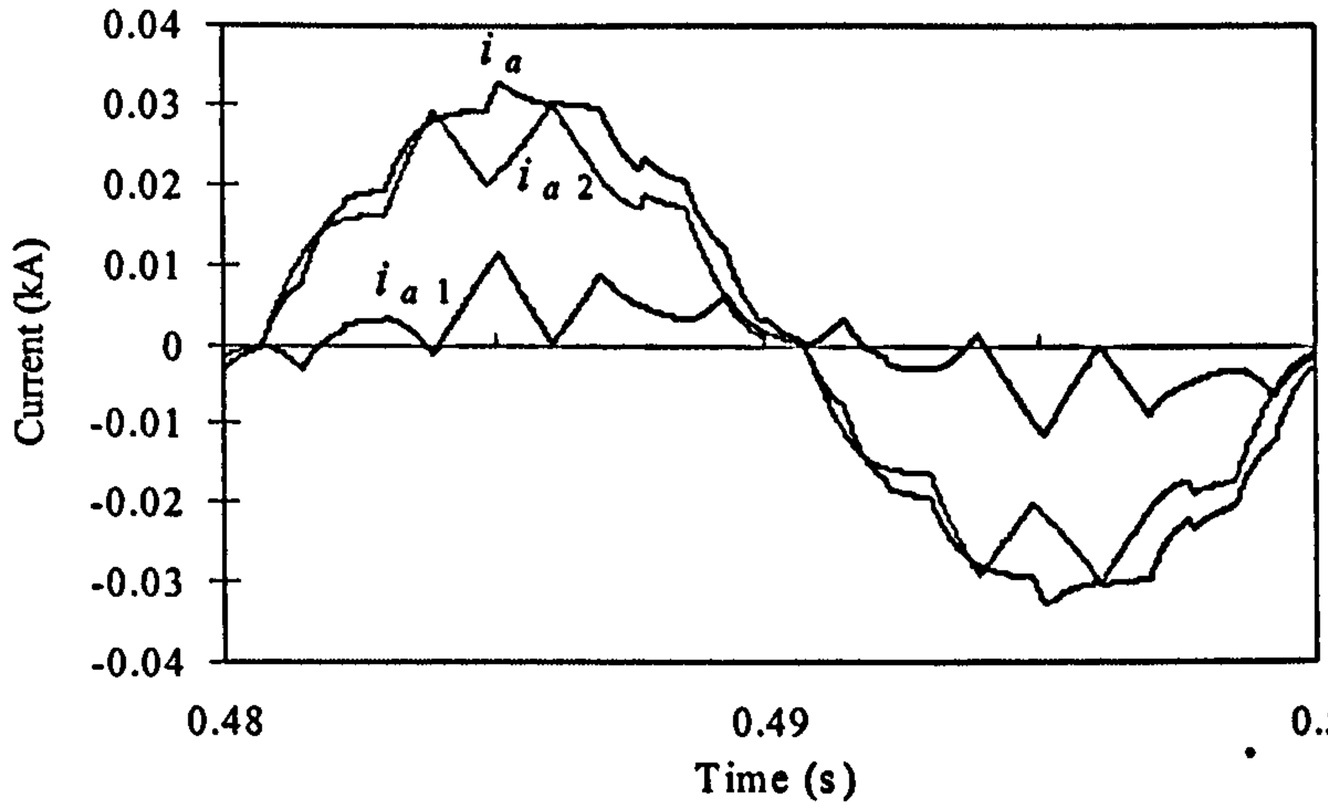


Fig. 6.10: Current waveforms with the PD/PS method at N'=2, m_f=9, m_a=0.8, f_o=50 Hz.

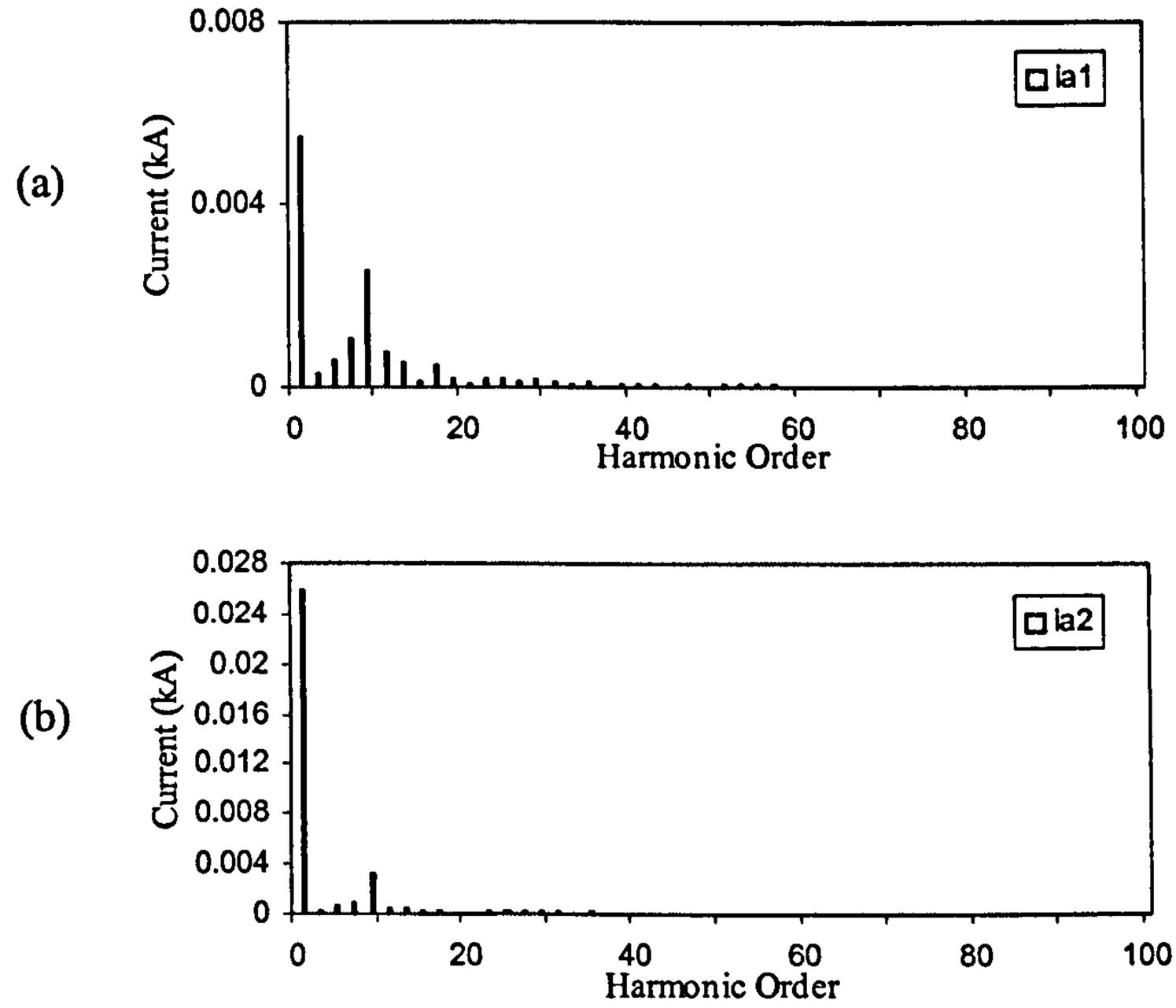


Fig. 6.11: Current harmonic spectra with PD/PS method (N'=2, m_f=9, m_a=0.8, f_o=50 Hz).
(a) Harmonic spectra of i_{a1}; (b) Harmonic spectra of i_{a2}; (c) Harmonic spectra of i_a.

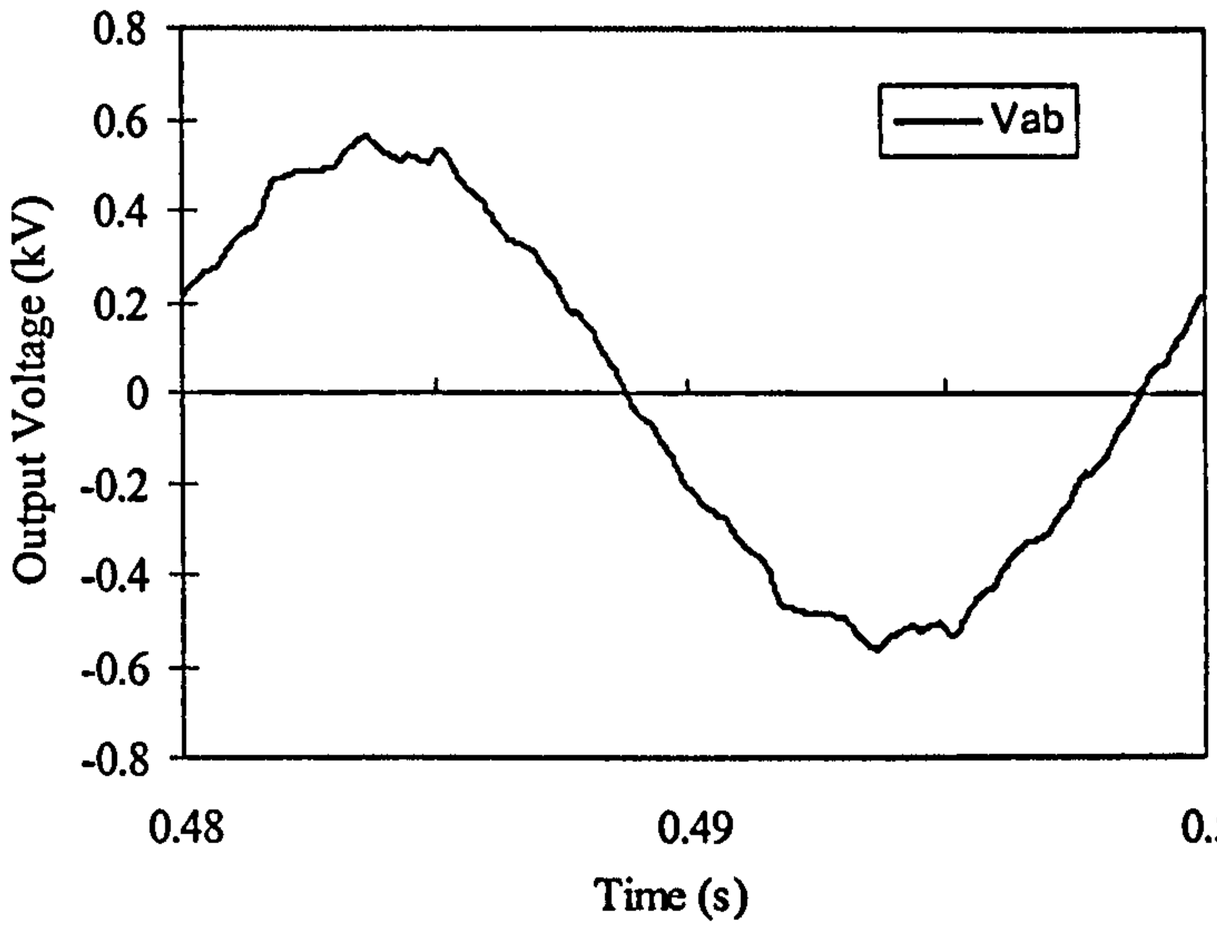


Fig. 6.12: Output line-to-line voltage waveform with the PD/PS method.

(N'=2, m_f=9, m_a=0.8, f_o=50 Hz).

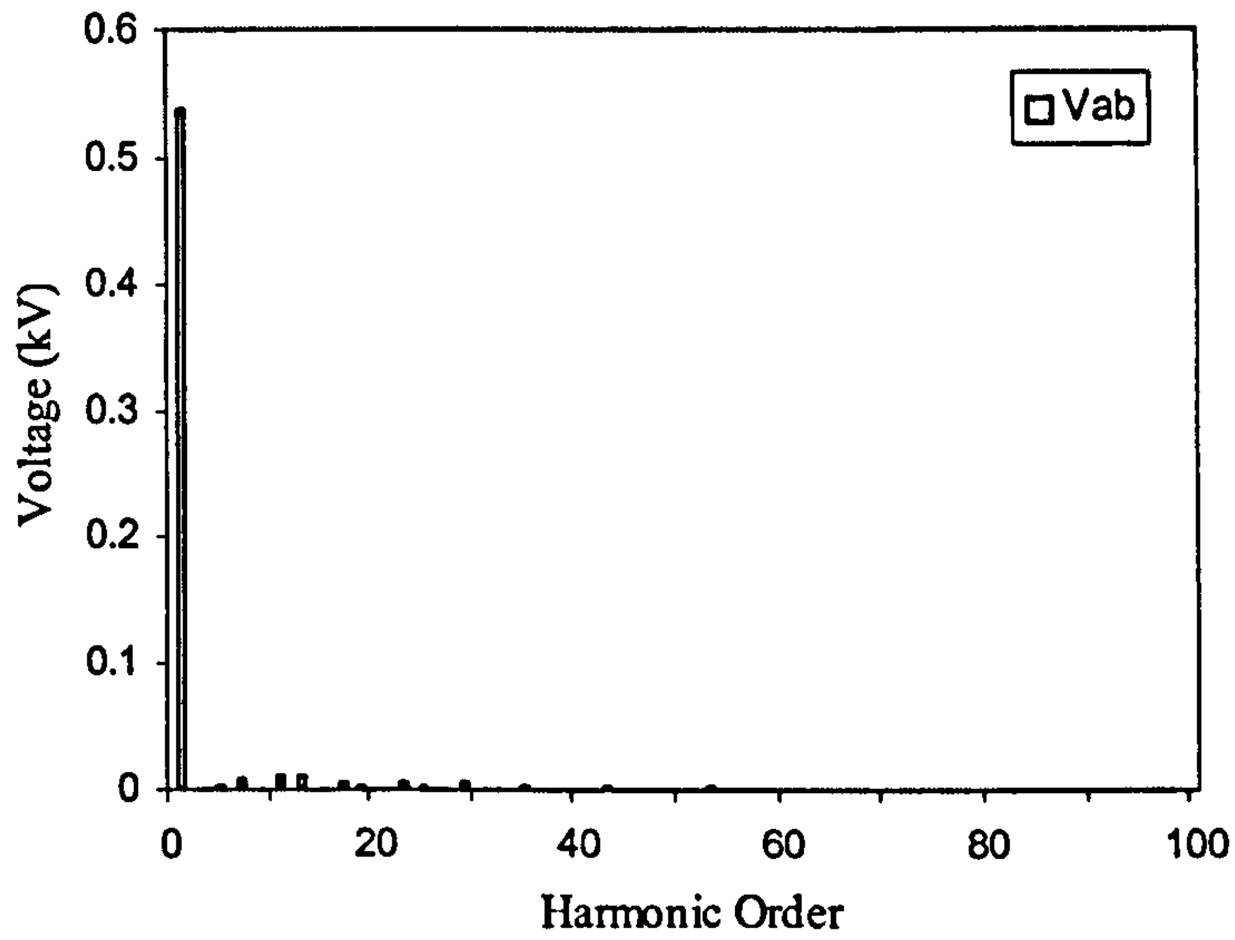


Fig. 6.13: Harmonic Spectra of v_{AB} with the PD/PS method.

(N'=2, m_f=9, m_a=0.8, f_o=50 Hz).

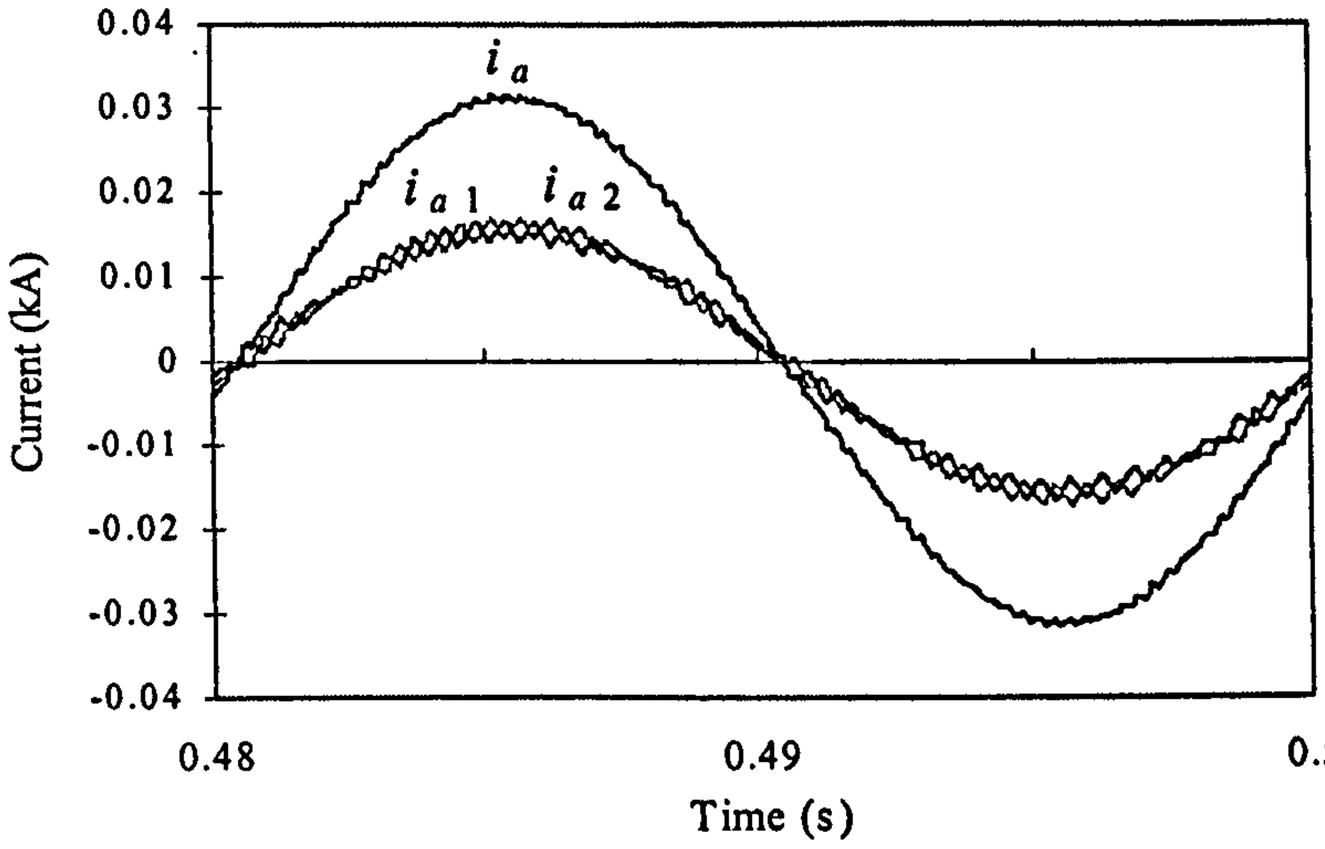
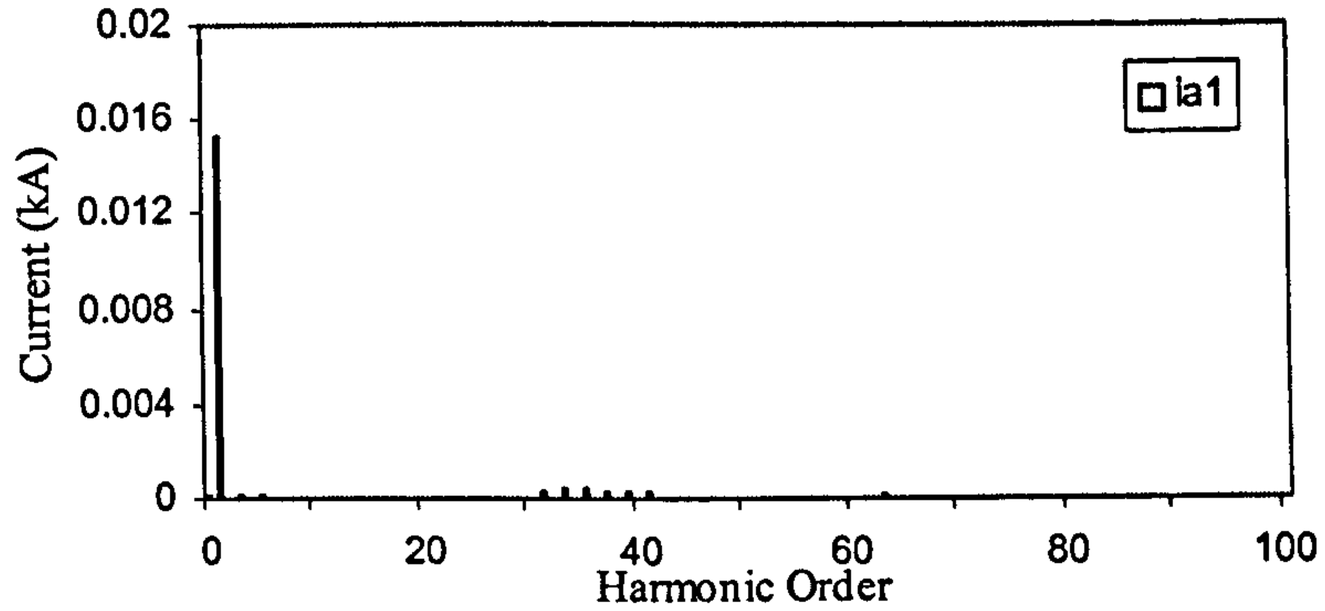
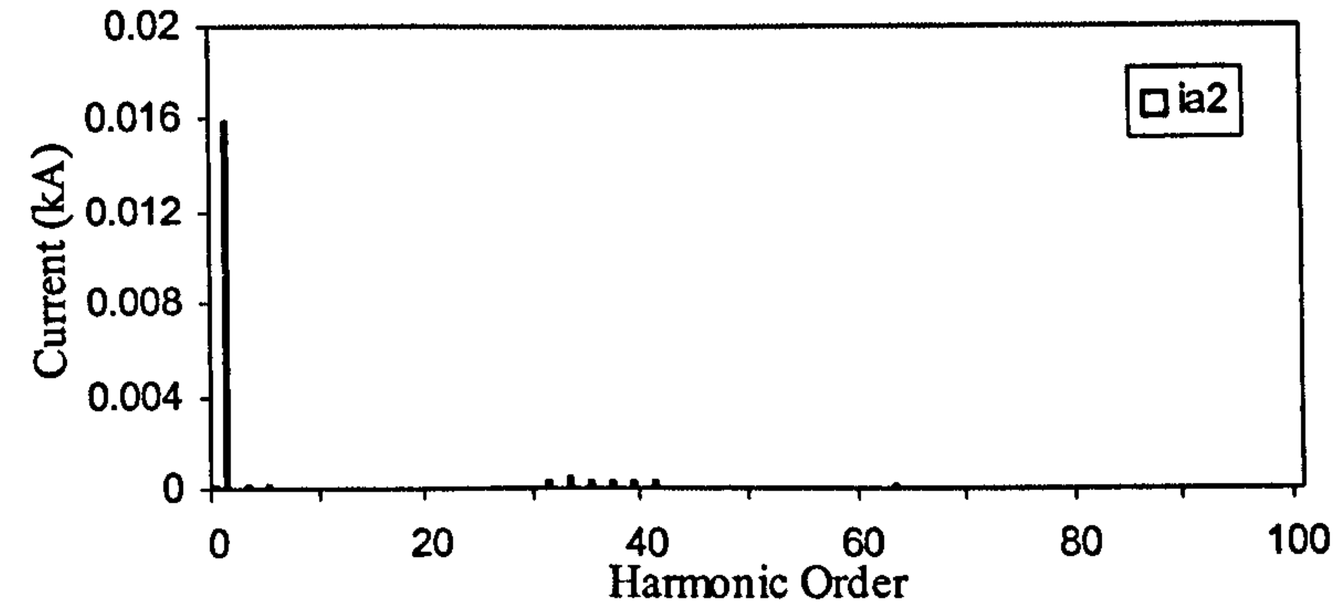


Fig. 6.14: Current waveforms with the PS method at N'=2, m_f=9, m_a=0.8, f_o=50 Hz.

(a)



(b)



(c)

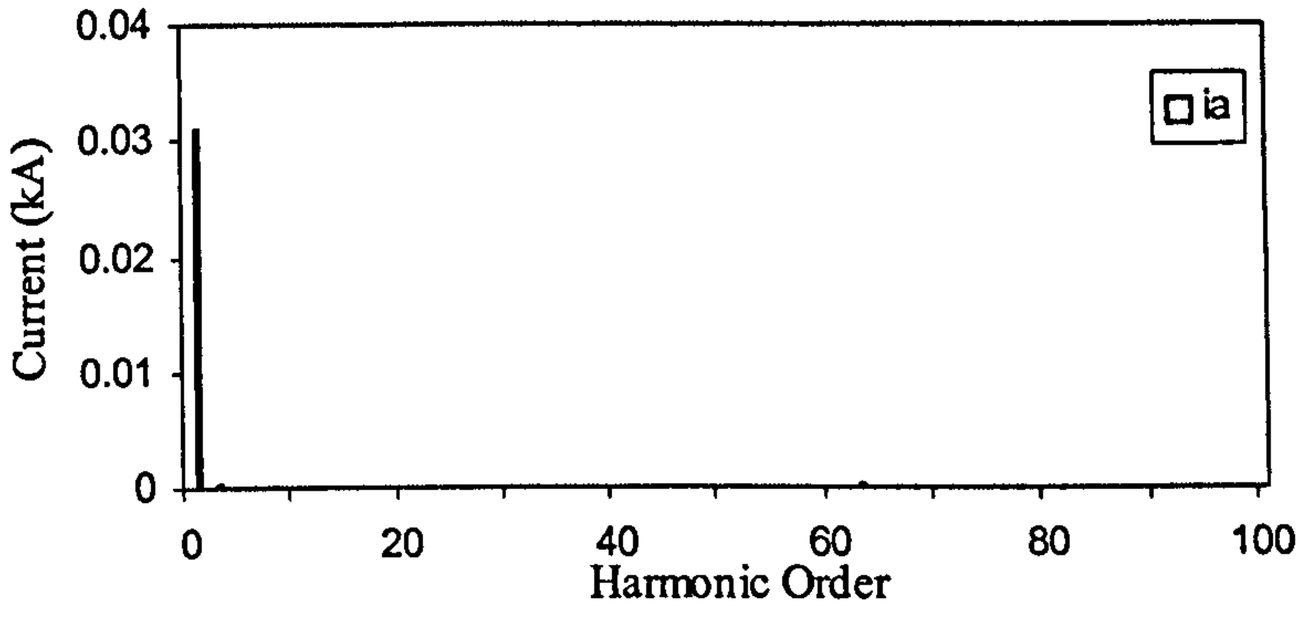


Fig. 6.15: Current harmonic spectra with the PS method (N'=2, m_f=9, m_a=0.8, f_o=50 Hz).
(a) Harmonic spectra of i_{a1}; (b) Harmonic spectra of i_{a2}; (c) Harmonic spectra of i_a.

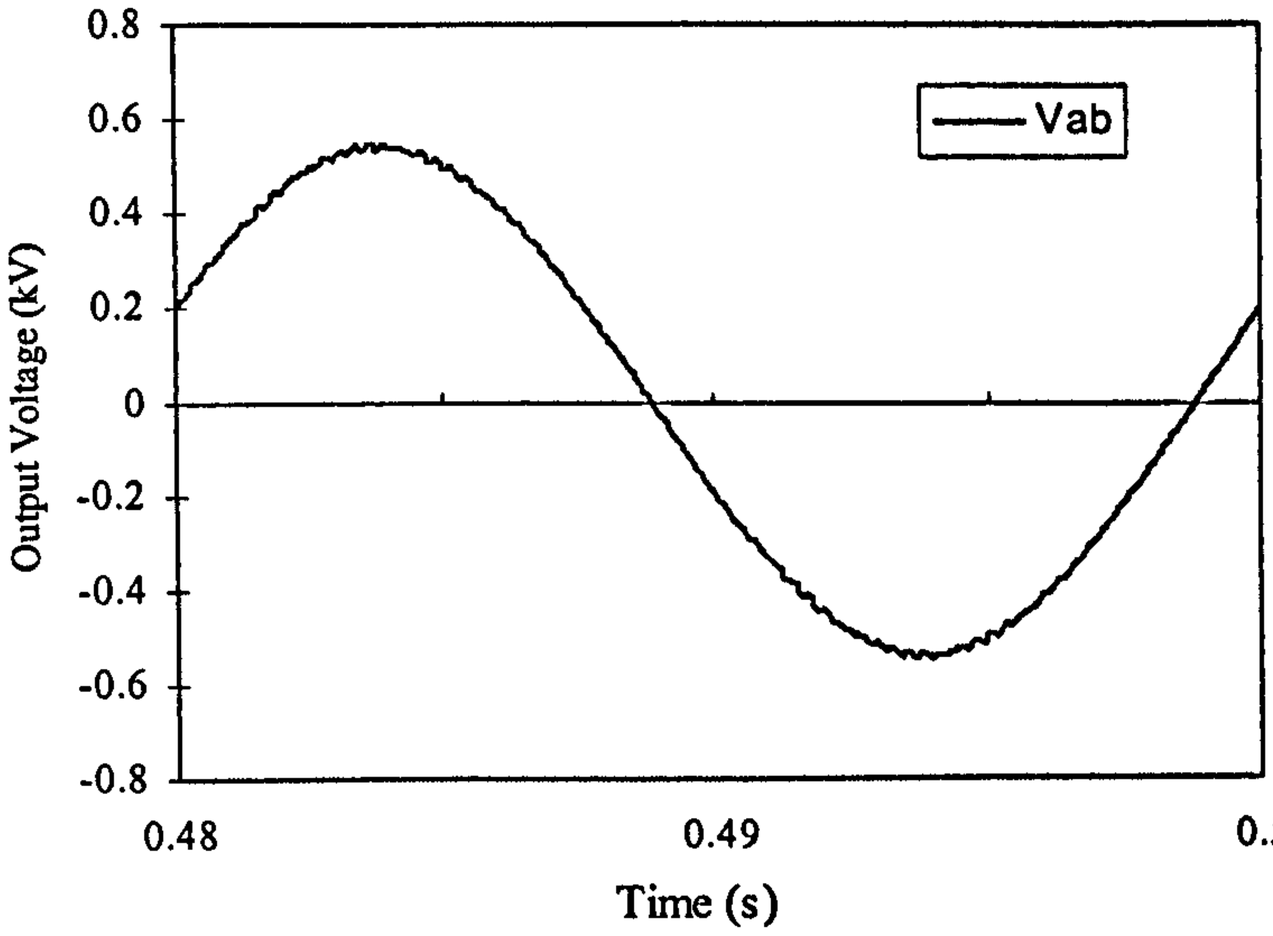


Fig. 6.16: Output line-to-line voltage waveform with the PS method.
(N'=2, m_f=9, m_a=0.8, f_o=50 Hz).

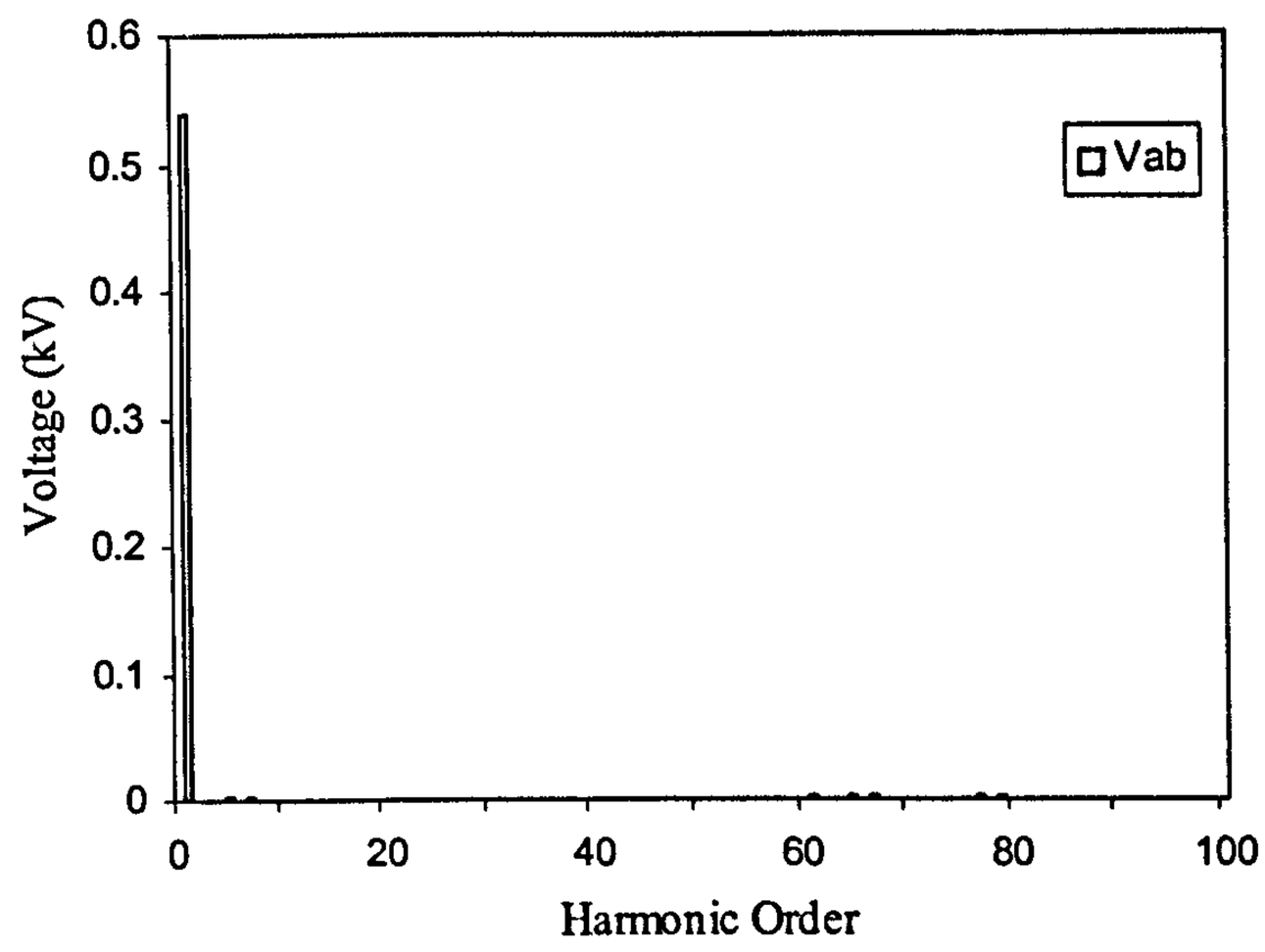


Fig. 6.17: Harmonic Spectra of v_{AB} with the PS method.
(N'=2, m_f=9, m_a=0.8, f_o=50 Hz).

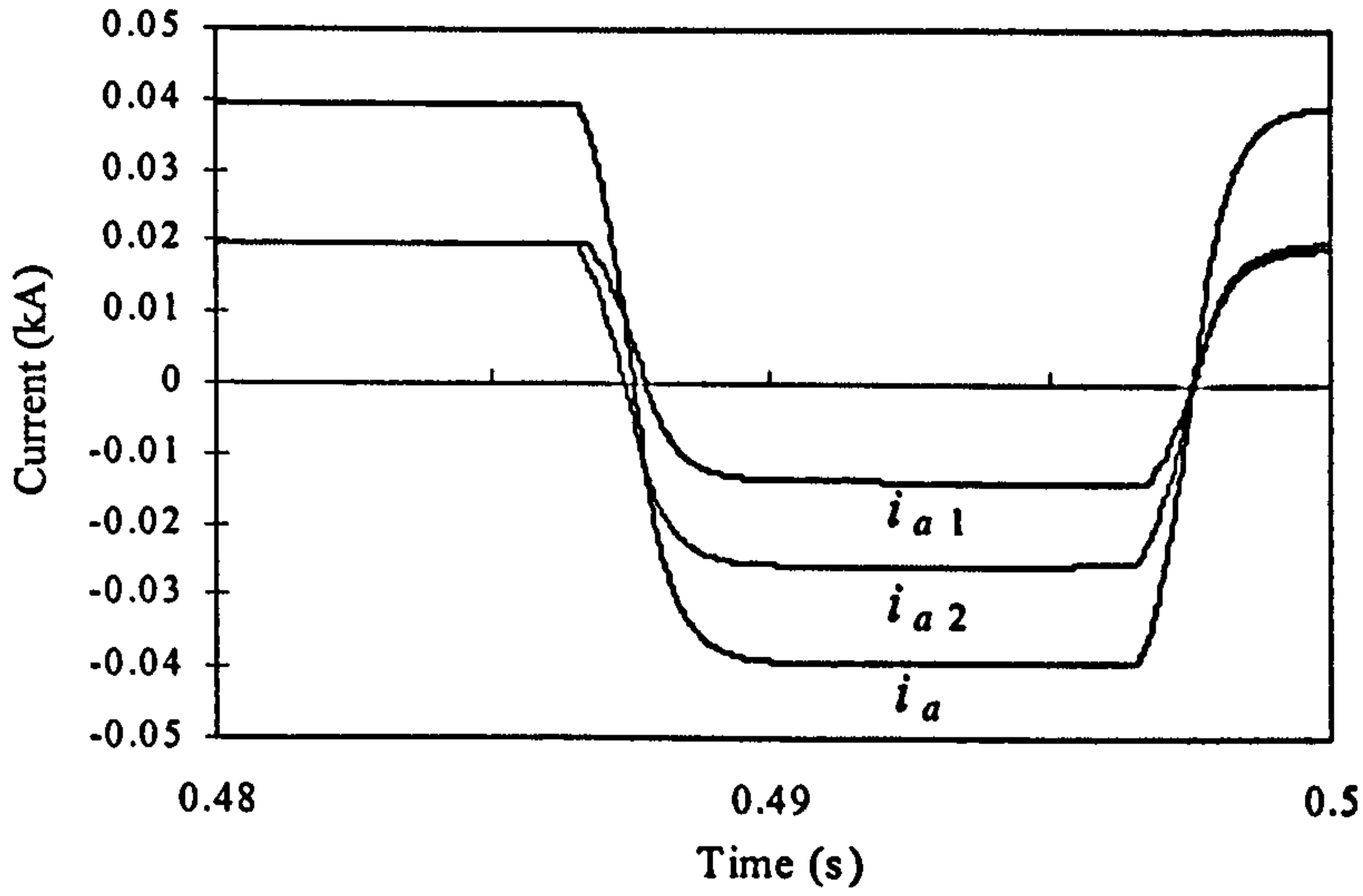
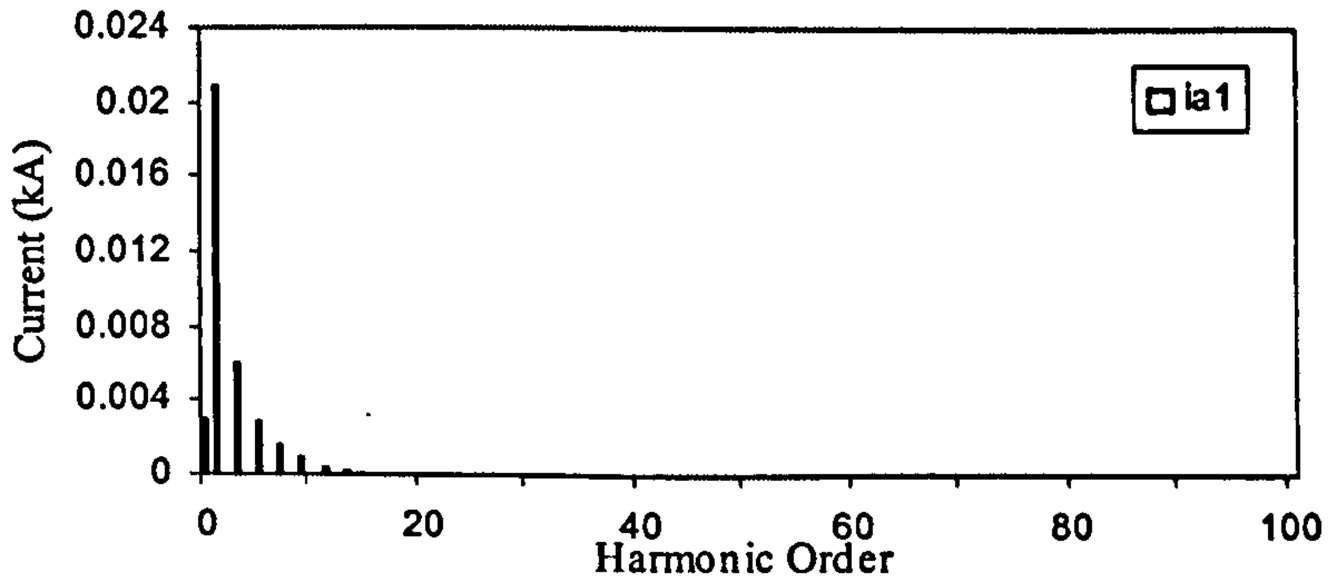
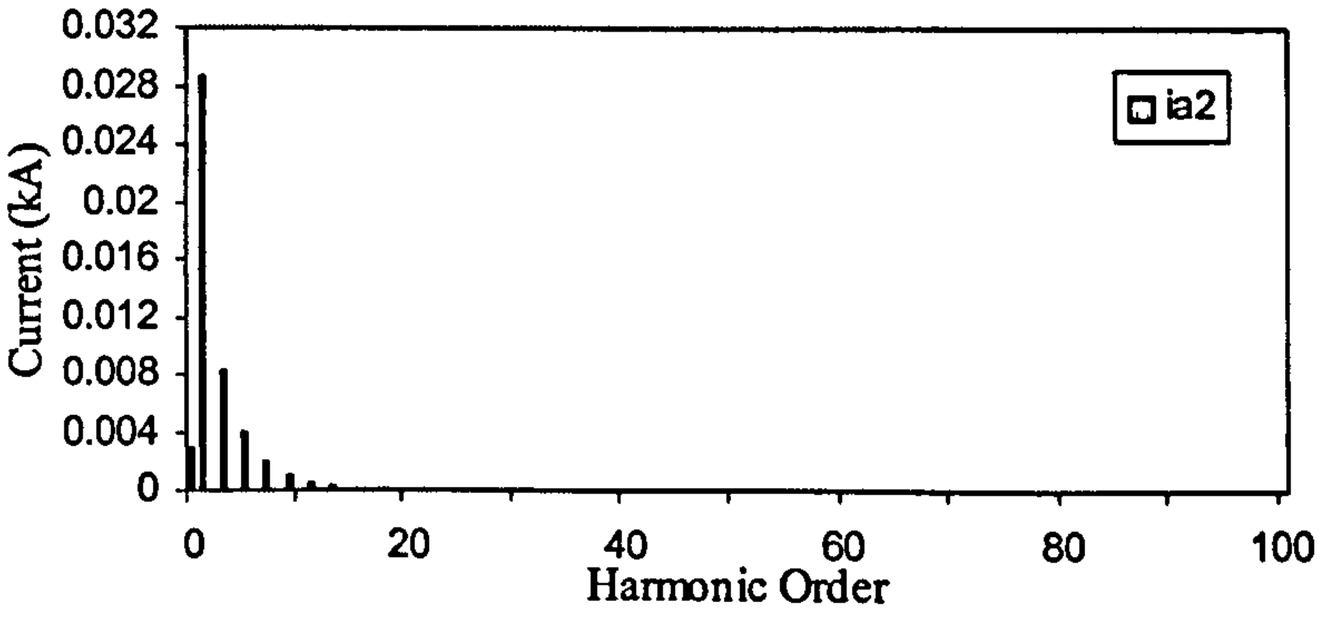


Fig. 6.18: Current waveforms with the PS method at N'=2, m_f=1, m_a=0.8, f_o=50 Hz.

(a)



(b)



(c)

Fig. 6.19: Current harmonic spectra with PS method at N'=2, m_f=1, m_a=0.8, f_o=50 Hz. (a) Harmonic spectra of i_{a1}; (b) Harmonic spectra of i_{a2}; (c) Harmonic spectra of i_a.

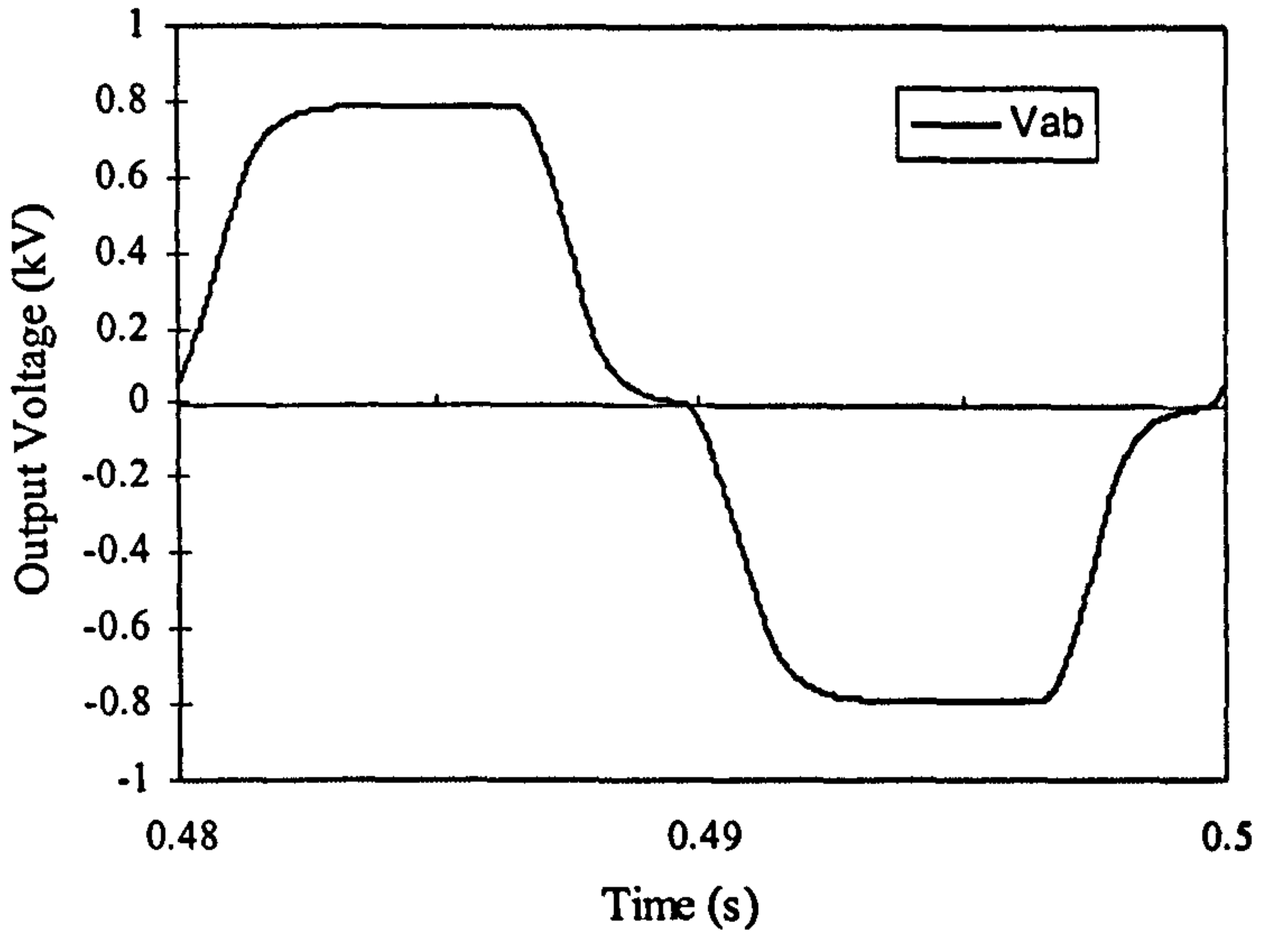


Fig. 6.20: Output line-to-line voltage waveform with the PS method.

(N'=2, m_f=1, m_a=0.8, f_o=50 Hz).

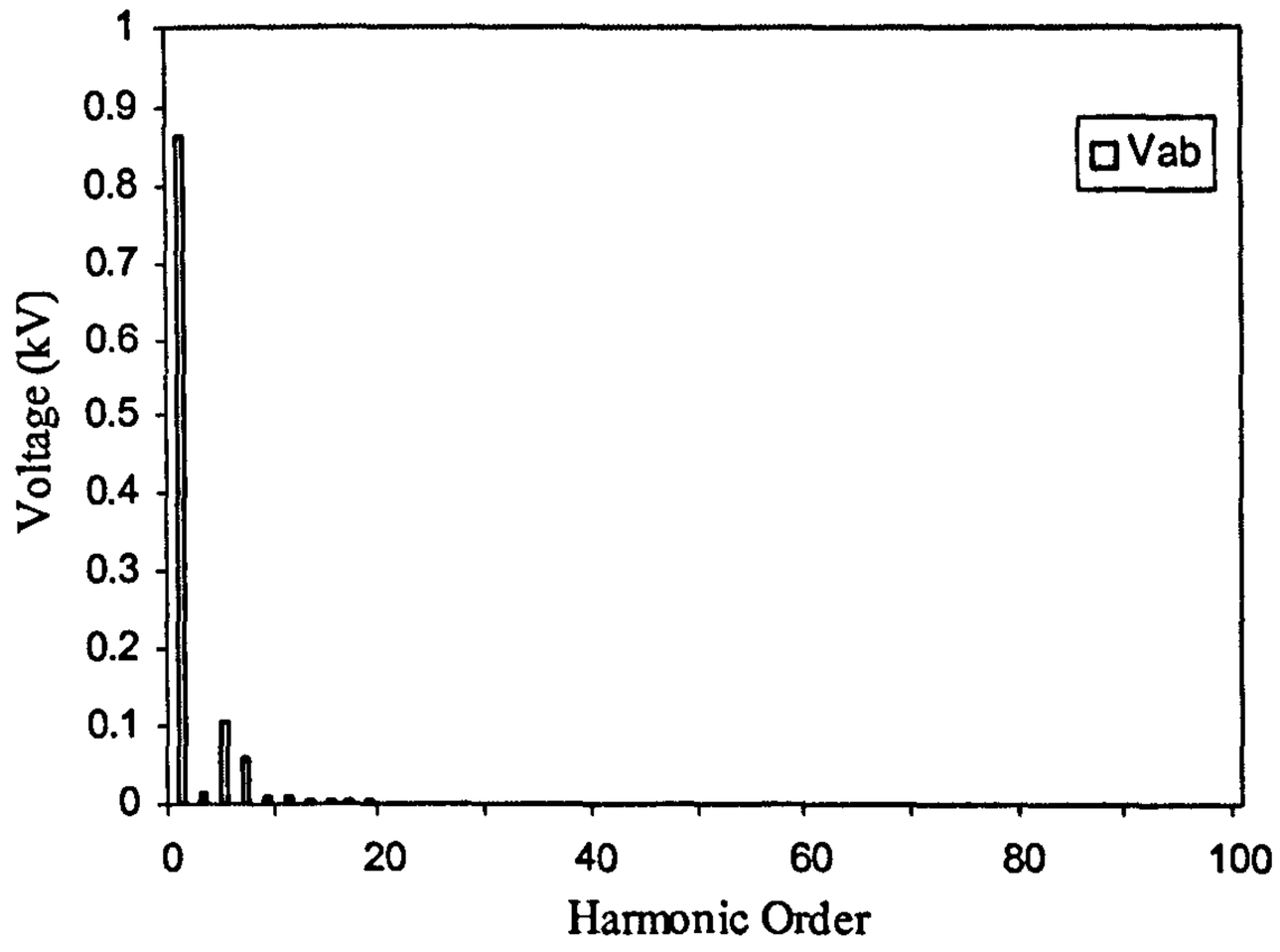


Fig. 6.21: Harmonic Spectra of v_{AB} with the PS method.

(N'=2, m_f=1, m_a=0.8, f_o=50 Hz).

Table 6.3 and Table 6.4 list the THDs of the output phase currents and line-to-line voltages with different modules at m_a=0.8, m_f=9 and at m_f=1, respectively. Table 6.5 and Table 6.6 list the current values in different modules at fundamental frequency at m_a=0.8, m_f=9 and at m_f=1, respectively.

Table 6.3: THD of the output quantities when module number varies
(m_f=9, m_a=0.8, f_o=50 Hz, L=10 mH, R_L=10 Ω, V_{dc}=800 V, PS method)

	1FC	2FC	3FC	4FC
i_a THD (%)	3.1	1.4	1.0	1.0
i_b THD (%)	3.1	1.4	1.0	0.7
i_c THD (%)	3.1	1.4	1.0	0.8
v_{AB} THD (%)	26.5	1.0	0.8	0.5
v_{BC} THD (%)	26.8	1.0	0.7	0.6
v_{CA} THD (%)	26.6	1.0	0.7	0.7

Table 6.4: THD of the output quantities when module number varies
(m_f=1, m_a=0.8, f_o=50 Hz, L=10 mH, R_L=10 Ω, V_{dc}=800 V, PS method)

	1FC	2FC	3FC	4FC
i_a THD (%)	29.4	33.0	12.5	5.5
i_b THD (%)	13.5	31.8	12.3	4.7
i_c THD (%)	13.4	34.3	9.5	4.6
v_{AB} THD (%)	34.1	14.3	5.9	5.3
v_{BC} THD (%)	25.0	61.8	10.9	2.8
v_{CA} THD (%)	33.9	58.3	10.8	5.1

Table 6.5: Current values in different modules at fundamental frequency (m_f=9, m_a=0.8, f_o=50 Hz, L=10 mH, R_L=10 Ω, V_{dc}=800 V, with the PS method)

Current	1FC	2FC	3FC	4FC
i_{a1} (A)	29.9	15.3	10.1	7.6
i_{a2} (A)		15.8	10.4	8.0
i_{a3} (A)			10.8	8.1
i_{a4} (A)				7.7
i_{b1} (A)	30.1	15.7		8.0
i_{b2} (A)		15.5		7.7
i_{b3} (A)				7.7
i_{b4} (A)				8.0
i_{c1} (A)	29.9	15.7		8.1
i_{c2} (A)		15.3		7.6
i_{c3} (A)				7.6
i_{c4} (A)				8.1
i_a (A)	29.9	31.1	31.3	31.4
i_b (A)	30.1	31.2	31.3	31.4
i_c (A)	29.9	31.0	31.4	31.4

Table 6.6: Current values in different modules at fundamental frequency (m_f=1, m_a=0.8, f_o=50 Hz, L=10 mH, R_L=10 Ω, V_{dc}=800 V, with the PS method)

Current	1FC	2FC	3FC	4FC
i_{a1} (A)	31.8	20.8	7.5	8.9
i_{a2} (A)		28.6	20.3	29.3
i_{a3} (A)			6.3	8.6
i_{a4} (A)				13.0
i_{b1} (A)	31.0	19.7		6.4
i_{b2} (A)		29.5		23.5
i_{b3} (A)				38.0
i_{b4} (A)				19.1
i_{c1} (A)	30.9	21.6		19.3
i_{c2} (A)		27.9		6.9
i_{c3} (A)				23.1
i_{c4} (A)				37.7
i_a (A)	31.8	49.4	32.3	32.5
i_b (A)	31.0	49.2	32.3	31.1
i_c (A)	30.9	49.5	32.0	31.1

It can be seen from Table 6.1 that the PS method has the smallest line-to-line voltage and the phase current THD among the three control combinations at higher m_f. PS and PS/PS offer similar potential switching losses, which are four times the potential switching losses with the PD/PS. As expected when m_f=1, the three control methods produce the lower order harmonics and nearly the same potential switching losses shown in Table 6.2 and Fig. 6.19.

Fig. 6.6 shows the two modules' current waveforms are the same with the PS/PS method, whose value is the half of the total phase current. Because in this case, there is no phase shifting between two modules, the harmonic performance of the total output phase current is the same as that of each module's current shown in Fig. 6.7. Fig. 6.10 shows the two modules' current waveforms are quite different with the PD/PS method at m_f=9. But the harmonic performance of the total output phase current is improved shown in Fig. 6.11. Fig. 6.14 and Fig. 6.15 indicate that the two modules' current waveforms are nearly the same with the PS method, and the THD of the system's output current is also decreased.

Unlike Figs. 6.6-6.17, Figs. 6.18-6.21 show the related waveforms and their harmonic spectra with the PS method at m_f=1. It can be noted that at m_f=1, not only do the branch currents differ much, but also the system's harmonic performance does not be improved.

Tables 6.3 and 6.4 show the effect of the number of modules N' on the THD of the output voltage/current of the system at m_f=9 and m_f=1 with the PS method respectively. 3FC means three modules are connected in parallel. Apparently, the harmonic performance of the system is improved when the number of modules increases, as expected, but for $N' \geq 3$, such improvement is not as prominent at higher m_f as the benefits gained are saturated. Table 6.4 shows the line current and line-to-line voltage THDs are not equal at m_f=1. This is because the FF-SPWM method generates variable harmonic content between the phases. Hence, the large discrepancy between the THD for the converter line-to-line voltages occurs.

In order to investigate the current sharing issue, Table 6.5 and 6.6 show the comparison of the current values (the fundamental component only) in the different modules with the PS method at m_f=9 and m_f=1 respectively. It can be seen that multi-modular systems with the PS method have balanced three-phase total output current waveforms at both cases (higher m_f and m_f=1), however, their module currents are quite different. At higher m_f, the current in each module has the same value; their sum equals the system's total current further confirming that each module processes the same power level. But when m_f=1 is considered, each module carries different value of current. In some cases the module

current is even greater than total current. This indicates that some modules counteract the overall configuration absorbing power and this result in loss of many advantages associated with the multi-modular system.

6.4 Multi-Modular Multilevel NPC Converter System

The multi-modular converter system based on the three-phase five-level NPC converter topology is discussed. The schematic diagram of the system is the same as shown in Fig. 6.1. Unlike the FC converter topology, the NPC converter has no switching redundancies. So there are few control schemes available for the NPC than for the FC converter. Below, its control scheme is described. Similarly, the feasibility of the FF-SPWM on the NPC converter system is also investigated and simulated results are given in this section.

6.4.1 Control Schemes

Since the PS method cannot be used for the NPC topology, only the CD method can be used in the NPC topology. As confirmed in the previous chapter, the PD control method is superior to other control methods (such as the APOD, POD) in the CD category. So the PD control method is employed in each NPC converter and the PS method is used in the multi-modular system. This method is called the PD/PS method which has been described in the previous section.

6.4.2 Simulation Results

Simulations have been carried out for the parallel-connected multi-modular system based on three-phase five-level NPC converters. Again, it is assumed that each module has equal and balanced voltage levels, so the DC bus capacitors are replaced with ideal DC sources in the simulations. The parameters of system are as follows:

V_{dc}=0.8 kV, f_o=50 Hz, L=10 mH, Load resistance R_L=10 Ω, the load is Y-connected (star).

Simulation results for the multi-modular system based on the NPC converter with the PD/PS at m_a=0.8, m_f=9 and m_f=1 are very similar to results shown in Figs. 6.10-6.13 for the FC converter system under the same control conditions. Therefore, they are not presented here again to avoid the overlap.

Table 6.7 and Table 6.8 list the THDs of the output phase currents and line-to-line voltages with different modules at m_f=20 and m_f=1, respectively. Table 6.9 and Table 6.10 list the current values in different modules at the fundamental frequency, respectively.

Table 6.7: THD of the output quantities when module number varies

(m_f=20, m_a=0.95, f_o=50 Hz, L=10 mH, R_L=10 Ω, V_{dc}=800 V, with the PD/PS method)

	1NPC	2NPC	3NPC	4NPC
i_a THD (%)	4.6	2.4	1.7	1.4
i_b THD (%)	4.7	2.4	1.7	1.4
i_c THD (%)	4.6	2.4	1.7	1.4
v_{AB} THD (%)	2.1	1.8	1.3	1.0
v_{BC} THD (%)	2.1	1.8	1.3	1.0
v_{CA} THD (%)	2.1	1.8	1.3	1.0

Table 6.8: THD of the output quantities when module number varies

(m_f=1, m_a=0.95, f_o=50 Hz, L=10 mH, R_L=10 Ω, V_{dc}=800 V, with the PD/PS method)

	1NPC	2NPC	3NPC	4NPC
i_a THD (%)	6.1	5.8	6.7	4.2
i_b THD (%)	13.2	8.6	6.8	4.5
i_c THD (%)	5.4	8.6	6.6	4.5
v_{AB} THD (%)	5.9	5.2	6.0	3.8
v_{BC} THD (%)	7.1	6.4	6.1	4.0
v_{CA} THD (%)	5.2	5.4	6.0	3.8

Table 6.7 and 6.8 show the effect of the number of modules N' on the THD of the output voltage/current of the system at m_f =20 and m_f =1 with the PD/PS method respectively. 3NPC means three NPC converter modules are connected in parallel. Apparently, the harmonic performance of the system is improved when the number of modules increases, as expected.

Table 6.9 and 6.10 show the comparison of the current values (the fundamental component only) in different modules with the PD/PS method at m_f =20 and m_f =1 respectively. It can be seen that the same phenomena occur in the NPC converter system. The multi-modular systems have balanced three-phase total output current waveforms at both cases (higher m_f and m_f=1), however, their module currents are quite different. At higher m_f, the current in each module has the same value; their sum equals the system's total current further confirming that each module processes the same power level. But when m_f=1 is considered, each module carries different value of current.

Table 6.9: Current values in different modules at the fundamental frequency (m_f=20, m_a=0.95, f_o=50 Hz, L=10 mH, R_L=10 Ω, V_{dc}=800 V, with the PD/PS method)

Current	1NPC	2NPC	3NPC	4NPC
i_{a1} (A)	35.2	18.1	12.4	9.4
i_{a2} (A)		18.1	12.3	9.1
i_{a3} (A)			12.1	9.2
i_{a4} (A)				9.1
i_{b1} (A)	35.2	18.3	12.4	9.1
i_{b2} (A)		18.2	11.9	9.4
i_{b3} (A)			12.5	9.1
i_{b4} (A)				9.3
i_{c1} (A)	35.2	18.3	12.6	9.5
i_{c2} (A)		18.2	12.1	8.9
i_{c3} (A)			12.1	9.5
i_{c4} (A)				9.0
i_a (A)	35.2	36.5	36.8	36.9
i_b (A)	35.2	36.5	36.8	36.9
i_c (A)	35.2	36.5	36.8	36.9

Table 6.10: Current values in different modules at the fundamental frequency (m_f=1, m_a=0.95, f_o=50 Hz, L=10 mH, R_L=10 Ω, V_{dc}=800 V, with the PD/PS method)

Current	1NPC	2NPC	3NPC	4NPC
i_{a1} (A)	38.4	46.5	39.7	37.8
i_{a2} (A)		9.0	19.5	24.6
i_{a3} (A)			18.1	21.1
i_{a4} (A)				40.6
i_{b1} (A)	30.0	15.7	19.0	20.2
i_{b2} (A)		38.1	18.7	33.8
i_{b3} (A)			39.0	27.1
i_{b4} (A)				20.3
i_{c1} (A)	41.1	23.2	18.1	17.3
i_{c2} (A)		33.4	39.8	16.1
i_{c3} (A)			18.7	30.2
i_{c4} (A)				35.7
i_a (A)	38.4	39.3	37.9	36.6
i_b (A)	30.0	36.7	38.0	38.2
i_c (A)	41.1	36.7	37.9	38.2

6.5 Discussions

The following points summarise the work reported in this chapter.

(1) There are more control schemes available for the multi-modular FC converter system than the multi-modular NPC converter. Only the PD/PS method can be used for the NPC-based multi-modular system, while the PD/PS, PS/PS, PS control schemes can be used for the FC-based system.

(2) Generally speaking, when N' modules of an m-level converter are controlled with the phase shifting technique, the equivalent carrier frequency is increased. Its value varies and depends upon the method employed. Specifically, the equivalent carrier frequency is $N' \cdot (m-1) \cdot m_f$ with the PS or PS/PS methods, while it is only $N' \cdot m_f$ with the PD/PS method if the phase shifting acts.

(3) When the switching losses are considered, the PD/PS is better than the PS or PS/PS methods because the switching losses in a system using the PS or PS/PS methods are four times that of a system using the PD/PS method.

(4) For the PS/PS method, when $k \cdot N' = m-1$, all the output voltage/current in each module have the same waveform, no phase shifting exists and thus no harmonics are eliminated in the total output voltage/current. In this case, the advantages of the phase shifting technique are traded off.

(5) At higher m_f, every module current fundamental component is almost equal and their sum builds up the total phase current of the multi-module system. However, with the FF-SPWM (m_f=1), every module current fundamental component is no longer equal. In other words, some module currents may be higher than others. This situation should be considered when designing the multi-modular system under the FF-SPWM method.

6.6 Conclusions

In this chapter, multi-modular systems based on the FC converter and NPC converter topologies have been discussed. Three control methods that are all combinations of carrier based PWM methods have been considered. The methods generate harmonic spectral that are of variable quality. When the FF-SPWM method is considered, in order to minimise the switching losses, a number of interesting results have been noticed. However, such techniques need to be carefully considered as in some cases they may result in a loss of many advantages that could be gained from phase-shifting concepts, when it comes to

harmonic elimination. Sharing of the currents can also present an issue if the techniques are not considered with care.

Specifically, for a higher m_f, no serious AC current sharing problem exists, converters can be connected in parallel directly as shown in Fig. 6.1. The FF-SPWM or lower m_f is desirable for reducing the switching losses, but they also result in large circulating currents. When employing lower m_f, converters must be connected through transformers.

Chapter 7: Development of Laboratory Flying Capacitor Converter Prototypes

7.1 Introduction

In this chapter, the development of the laboratory prototypes is described. Specifically, the key components of the prototype are introduced in Section 7.2. Section 7.3 presents the background and the methodology for the DSP-based PWM generator. Section 7.4 describes the development of a three-phase three-level FC converter prototype. Initially, the converter power circuit is introduced. Next, the PWM signal generation is described in detail. The design of the single-phase five-level FC converter prototype, including its power circuitry, charging circuit, and DSP-based controller are presented from the practical point of view at length in Section 7.5. Then experimental results are presented in Section 7.6 and finally, conclusions are drawn in Section 7.7.

7.2 Main Components of the FC Converter System

The block diagram of a DSP-based FC converter system is shown in Fig. 7.1. It is composed of the following components and subsystems:

- Power circuit;
- TMSLF2407 DSP Evaluation Module (EVM) Board;
- JTAG Emulator;
- Code Composer operating environment installed in a typical PC;
- IGBT drive card;
- Interface board between the DSP and the drive card.

These are the main building blocks of the converter with open-loop control. If a closed-loop control is needed, Voltage Transducers (VT) and Current Transducers (CT), together with the signal conditional circuits must be included. The building block diagram of the converter with the closed-loop control will be presented in a later section.

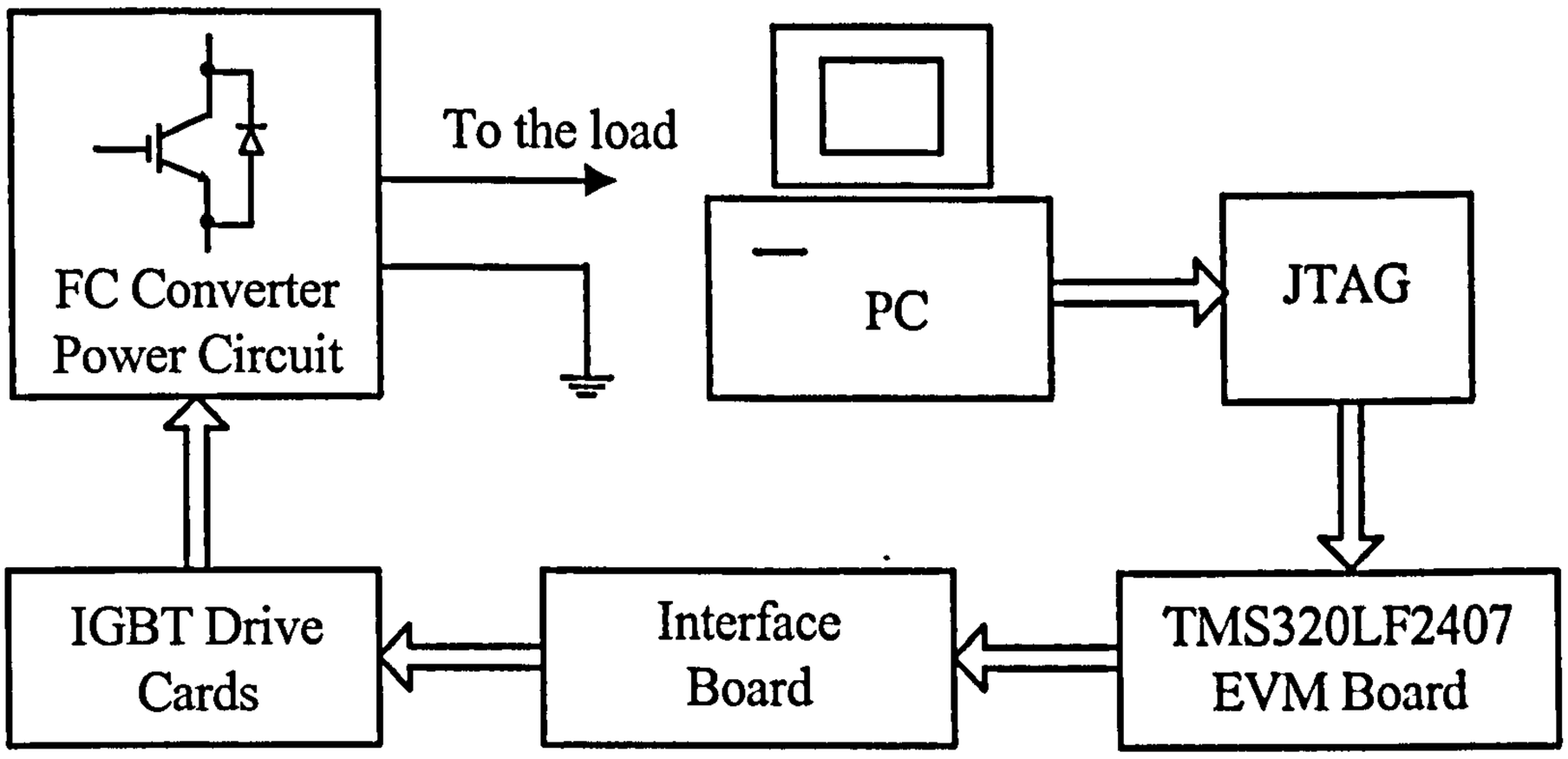


Fig. 7.1: Block diagram of the DSP-based FC converter system with open-loop control.

7.2.1 Power Switches

There have been major advances in recent years in the fully-controlled switching technology. Unlike diodes and thyristors, this kind of switches are turned on and off by control signals. Several device types are available such as Bipolar Junction Transistors (BJTs), Metal-Oxide-Semiconductor Field Effect Transistors (MOSFETs), IGBTs, and GTOs.

The IGBT has some of the advantages of the MOSFET, BJT, and the GTO combined. Similar to the MOSFET, the IGBT has a high impedance gate, which requires only a small amount of energy to switch the device. Like the BJT, the IGBT has a small on-state voltage even in devices with large blocking voltage ratings (for example, V_{on} is 2-3 V in a 1000V device). Similar to the GTO, IGBTs are designed to block negative voltages. They have brought about great control flexibility and improved device performance [104].

IGBTs have been chosen as power switches for the FC converter prototype. Specifically, the SKM 75GB 123D SEMIKRON IGBT modules are used to build the power circuit of the converter. The ratings of the module are 1200V/75A. This kind of IGBT module is a voltage controlled device, it has features such as low inductance case, very low tail current with low temperature dependence, high short circuit capability, self limiting to $6I_{cnom}$, latch-up free, fast and soft inverse CAL diodes. Fig. 7.2 shows the case outline and circuit diagrams of the IGBT module. Each module incorporates an IGBT with an antiparallel diode. Two modules are assembled in a case. It should be noted from Fig. 7.2 that each IGBT has two emitter terminals. One is the power terminal and the other one

is used to connect the drive circuit. It is imperative that any stray inductance is minimised in order to avoid problems with the safe operation of the switch.

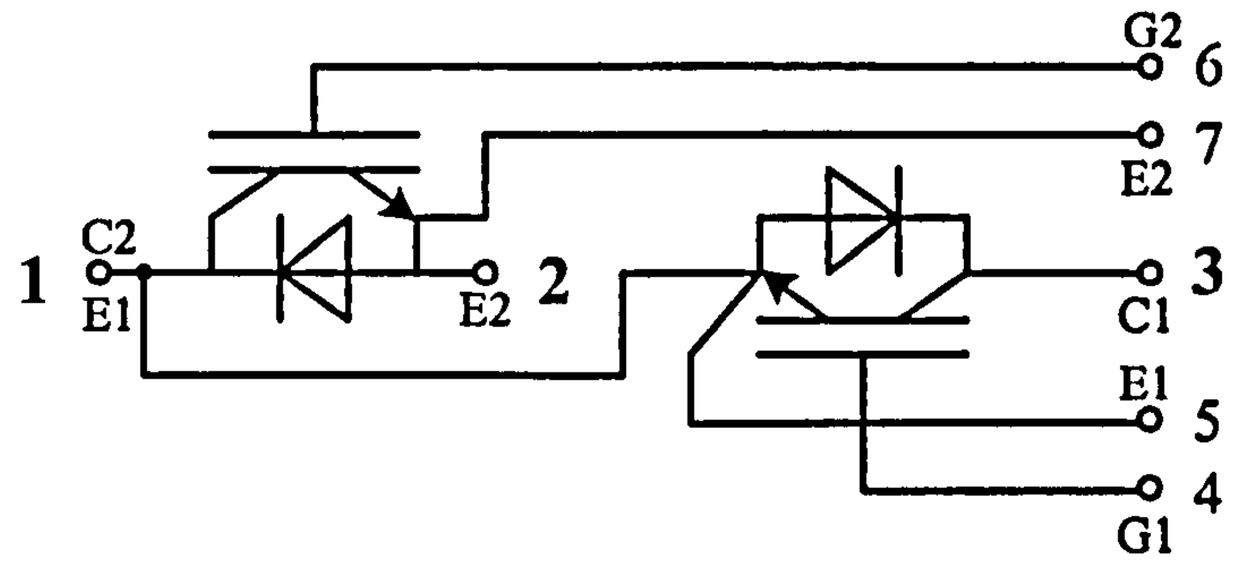


Fig. 7.2: SKM 75GB 123D IGBT Module.

7.2.2 Capacitors

In power electronic circuits, there are three basic types of capacitors being used: electrolytic, metallised polypropylene, and ceramic [106].

- Aluminium Electrolytic Capacitors

Electrolytic capacitors offer a large capacitance per unit volume and are polarized. The large capacitance is due to the fact that the aluminium foil connected to the positive terminal is etched so that its surface is porous like a sponge. This results in an increase in its surface area by as much as a factor of 100 compared to its original unetched area. On this etched foil, an insulating layer of aluminium oxide is formed electrochemically. The negative terminal of the capacitor is connected to another aluminium foil that is in electrical contact with the liquid electrolyte that is an electrically conducting material.

Because of the resistance of the electrolyte, these capacitors have a significant Equivalent Series Resistance (ESR). These capacitors should not be used at temperatures below the specified minimum temperature since the tendency of the electrolyte to crystallise results in a larger resistance.

The capacitor package or can is sealed at the top with an insulating layer that surrounds the electrical terminals. The rate of evaporation of the electrolyte through the seal increases significantly with temperature. Therefore the capacitor lifetime decreases significantly with temperature. It should be noted that the electrolytic capacitors have by far the shortest lifetime of any element, active or passive, used in power electronic converters. The temperature within the capacitor depends on the power loss. For a given current, the ripple voltage across the dielectric decreases with increasing frequency. Therefore the dielectric power loss decreases with increasing frequency. For a given lifetime of the capacitor, its

current-carrying capacity increases with increasing frequency and decreasing ambient temperature.

- Metallised polypropylene capacitors

In snubbers and thyristor commutation circuits, capacitors must handle large currents, but the capacitance value required is small. Metallised polypropylene capacitors are a good choice for such applications due to the very small loss coefficient of the polypropylene dielectric material. The dielectric losses are proportional to the square of the voltage and frequency. Since the voltage across the dielectric is proportion to the current and inversely proportional to the frequency, the dielectric power loss is proportional to the square of the current and inversely proportional to the frequency. Therefore, for a specified temperature, the current-handling capability increases slightly with frequency.

- Ceramic capacitors

Ceramic capacitors have extremely low series inductance. They are used as filters, for example, on printed circuit boards to reduce ripple in the supply voltage.

In the FC converter, more capacitors are needed than in other multilevel topologies. Two kinds of capacitors in terms of functionality are needed. They are DC link capacitors and flying capacitors. Based on the required capacitance, operating voltage, rms current, and frequency in the application, aluminium electrolytic capacitors made by Phillips are selected as DC link capacitors and flying capacitors in the prototype. They are 1500 μF, 350 V AC.

7.2.3 Drive Card

The Drive Circuit is the interface between the control circuit and the power switch. The drive circuit amplifies the control signals to levels required to drive the power switch and provides electrical isolation when required between the power switch and the logical-level signal processing/control circuits. Often the drive circuit has significant power capabilities compared to the logic-level control/signal processing circuits.

The drive card employed here is the SEMIDRIVER 6-Pack IGBT and MOSFET Driver SKHI 61 and SKHI 71. It has the following features:

- CMOS-compatible input buffers at V_{DD}=5 V
- Short-circuit protection by V_{CE}-monitoring and Soft-Turn-Off
- Monitoring and turn-off

- Drive interlock top/bottom (optional)
- Signal transmission by opto-couplers
- Supply under-voltage protection (13 V)
- Error latch/output
- Suitable adapter PCB SKPC6006 as EVA-BOARD available

The SKHI 61 and SKHI 71 drivers are designed for IGBT- and MOSFET-modules. Since all subassemblies necessary for operation have been integrated, there is no need for external components except for the gate resistors and the V_{CE}-circuitry. V_{CE}-thresholds and the blanking time are adjustable by integrating additional resistors and capacitors according to the customer specifications.

The interlocking time can be adjusted by simple bridging of connector pins. The driver is equipped with a separate error input for immediate turn-off when receiving error signals from external components (e.g. over-temperature).

IGBT driver signals

There are two control pins in every power switch from the driver, one gate and one emitter input pin. Since the earth connection of the driver is directly connected to the IGBT's emitter via the emitter input, a resistor of at least 10 Ω has to be connected to the gate circuit. This resistance is the minimum limit value controlled by the driver output buffer in order to limit the pulse currents to their peak value. A 20 kΩ resistor has been interconnected between the gate and the emitter (for the case when the supply voltage breaks down).

V_{CE}-threshold and V_{CE}-monitoring

V_{CE}-monitoring is done by connection of the driver collector pin to the collector of the power semiconductor. If the turn-off threshold for short-circuit protection is to be reduced (standard 5.8 V), a resistor has to be connected, whose value is calculated by eq. (7-1). The time between turn-on of the power semiconductor and V_{CE}-registration called blanking time is adapted by attaching a capacitor whose value is calculated by eq. (7-2). Fig. 7.3 shows the connection of a power switch with a specifically adjusted V_{CE}-threshold.

$$R_{VCE}[k\Omega] = \frac{11.86}{5.4 - 0.93V_{CE}} - 4.75 \tag{7-1}$$

$$C_{VCE}[nF] = \frac{t_{blank}[\mu s] \cdot (72.75 + R_{VCE}[k\Omega])}{(R_{VCE}[k\Omega] + 4.75) \cdot 36.08} - 0.1 \tag{7-2}$$

According to eq. (7-1), the V_{CE}-threshold can only be adjusted in the range between 3.12 V and 5.8 V using R_{VCE}. This is when R_{VCE}=0, V_{CE}=3.12 V, while R_{VCE}=∞, V_{CE}=5.8 V.

In the prototype, the following parameters are set:

- V_{CE}-threshold: 4.8 V
- Interlocking dead time: 2 µs of the dead time is chosen for both converters. The 2 µs of dead time is set in the DSP board for the three-phase three-level FC converter. However, since no dead time is inserted in the DSP board for the single-phase five-level FC converter, the 2 µs of interlocking dead time is set in the drive cards.
- Error blanking time for V_{CE}-threshold: 4 µs
- Gate resistor: R_G=33 Ω

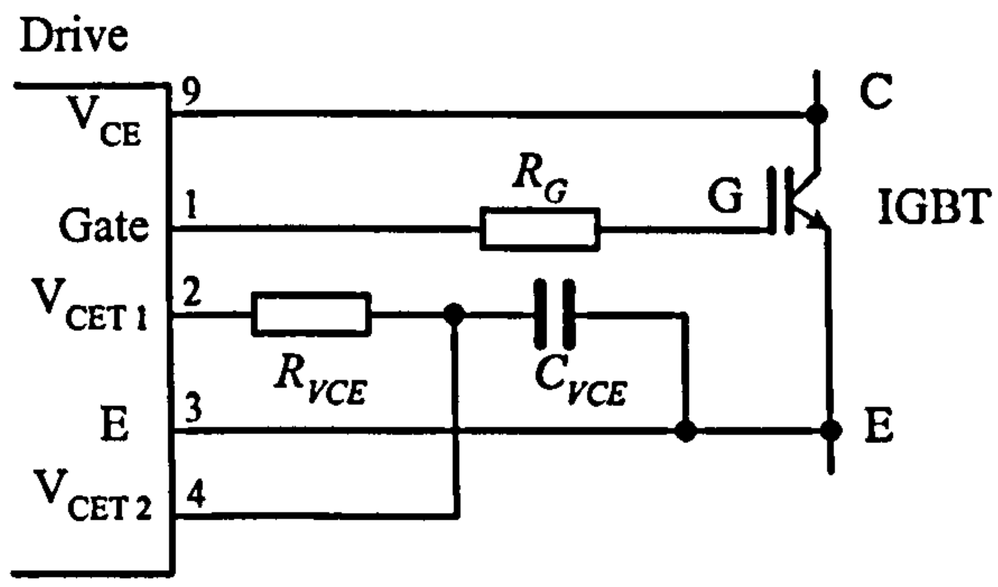


Fig. 7.3: Connection of a power switch with a specifically adjusted V_{CE}-threshold.

To adjust different V_{CE} thresholds, an additional resistor R_{VCE} and a capacitor C_{VCE} for each switch are needed. V_{CE}-threshold resistor: intended V_{CE}=4.8 V, applying eq. (7-1) R_{VCE} will result in R_{VCE}=7.92 kΩ. The closest value from the E24-range: 8.25 kΩ is chosen. The threshold voltage is recalculated with 8.25 kΩ, V_{CE}-threshold at 4.82 V. For the capacitor the blanking time may be calculated as: $t_{blanking}$=4 µs, C_{VCE}=689 pF, thus a capacitor of 680 pF can be chosen.

V_{CE}-monitoring can also be suppressed by connecting the collector pin V_{CE} of one driver to the belonging emitter pin E and not to the collector of the power semiconductor.

7.2.4 DSP Evaluation Module Board

The TMS320LF2407 EVM board from Texas Instruments (TI) is utilised to provide the control solution to the FC converter. It is a stand-alone card that allows evaluators to examine certain characteristics of the LF2407 DSP to determine if the DSP meets their application requirements. Furthermore, the module is an excellent platform to develop and run software on the LF240x family of processors.

The LF2407 EVM is shipped with a TMS320LF2407 DSP. The EVM allows full speed verification of LF2407 code. With 544 words of on-chip data memory, 128K words of onboard memory, on-chip flash Read Only Memory (ROM), on chip UART, and an MP7680 Digital to Analogue Converter (DAC), the board can solve a variety of problems as shipped. Four expansion connectors are provided to interface to any necessary evaluation circuitry [107].

Fig. 7.4 shows a picture of the LF2407 EVM board. The major interfaces of the EVM include the target Random Access Memory (RAM), analogue interface, Controller Area Network (CAN) interface, serial boot ROM, user leads and switches, RS232 interface, Serial Peripheral Interface (SPI) data logging interface, and expansion interface. The LF2407 interfaces to 128K words of zero wait-state static memory. An external I/O interface supports 65,000 parallel I/O ports. An onchip CAN and RS232 serial port are available on the expansion connector.

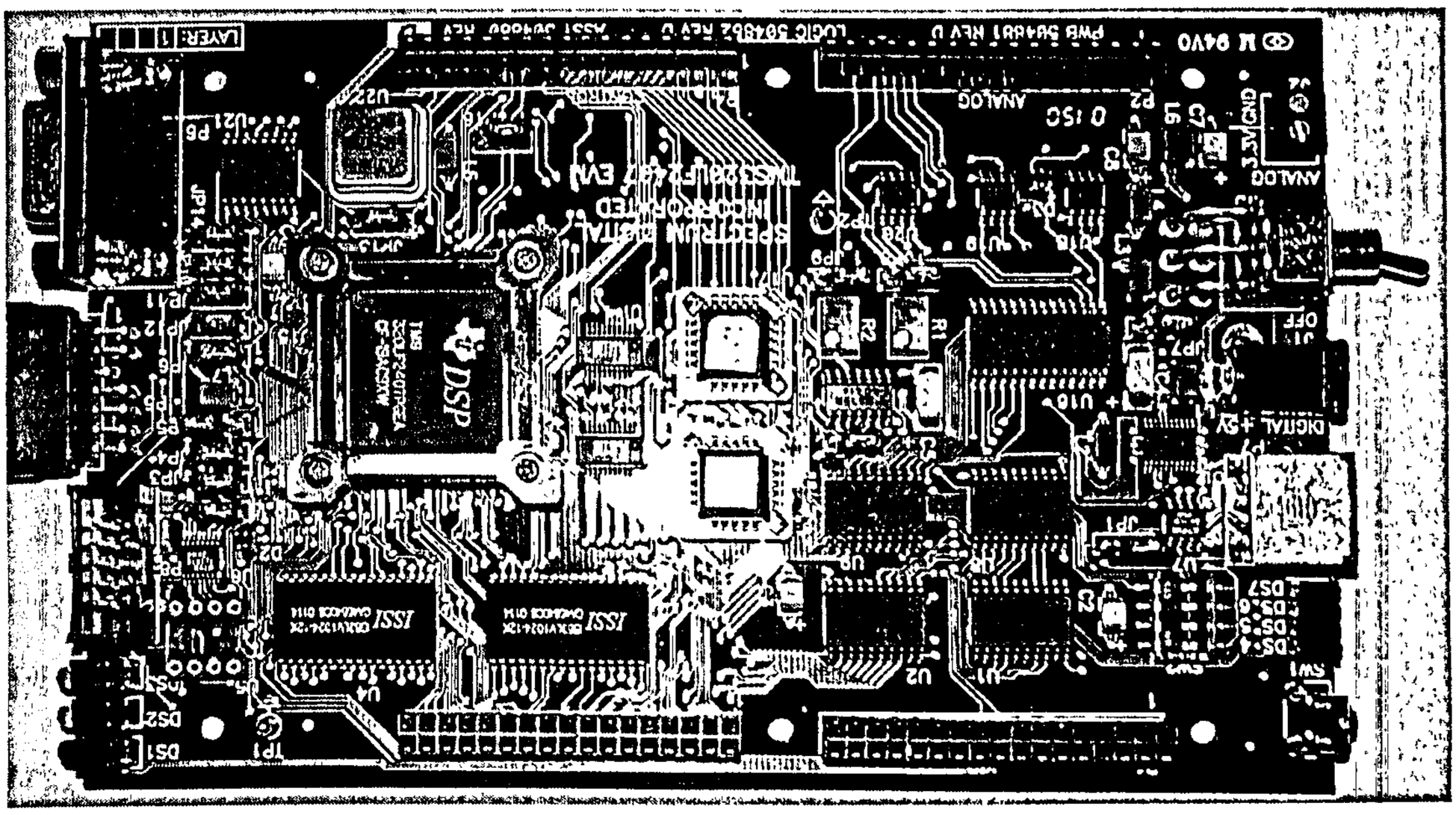


Fig. 7.4: TS320 LF2407 DSP EVM Board.

The Key Features of the TMS320LF2407 EVM include:

- 30 MIP's 16 bit fixed point DSP core with up to 30 MHz CPU frequency.
- LF2407 operating at 30 MIPS with 128K words of zero wait state memory.
- 16 channels of 10 bit onchip Analog to Digital (A/D) conversion with auto sequencer.
- Dual event managers multiple PWM and capture channels on chip.
- DAC7625 Four Channel Digital to Analogue (D/A) converter.

- On chip UART with RS232 Drivers.
- 32K words of on chip Flash ROM.
- CAN Interface with drivers.
- User Switches and LEDs.
- 4 Expansion Connectors (data, address, I/O, and control).
- On board IEEE 1149.1 JTAG Connection for Optional Emulation.
- 5 Volt power input, (onboard 3.3 Volt regulators).

7.2.5 Interface Board

The TMS320LF2407 DSP is a low power 3.3 V design. Its PWM Complementary Metal-Oxide Semiconductor (CMOS) output swings from 0 V to 3.3 V. However, SEMIDRIVER SKHI 61 and SKHI 71 have CMOS compatible input buffers at V_{DD}=5 V. Its input threshold voltage (High) V_{iT+} minimum value is 4.0 V, typical value is 5.0 V, while its input threshold voltage (Low) V_{iT-} maximum value is 1.5 V. If the output of the DSP is connected to the input of the driver directly, all the outputs from the DSP are below the minimum input threshold high voltage, thus they will be regarded as low voltage from the driver and can not drive the switches.

So a level shifting circuit must be required between the 3.3 V DSP CMOS output and 5V CMOS input of IGBT driver. One low-cost technique is to use a standard 5 V CMOS buffer such as the 74HCT04 (or 74AHCT04) hex inverter or the 74HCT240 (74AHCT240) octal buffer, or MM74HCT541N Octal 3-State Buffer to translate the 3.3 V CMOS output up to a 5 V CMOS level.

7.3 Background and Methodology for the PWM Generator

7.3.1 Dead-band Control Method

The Dead-band control method provides a convenient means of combating current shoot-through problems in a conventional power converter of voltage-source type. Shoot-through occurs when both the upper and lower switches of the same phase of a power converter are closed simultaneously. This condition shorts the power supply and results in a large current draw. The shoot-through problem occurs because transistors turn on faster than they shut off, and because the high-side and the low-side power converter switches are typically switched in a complementary fashion. Although the duration of the shoot-through current

path is finite during the PWM cycle, even brief periods of a short circuit condition can produce excessive heating and over stress in the power converter and the power supply.

Like conventional two-level converters, the multilevel FC converter has complementary switching pairs. If these switching pairs turn on during some time, they will cause the flying capacitor short or two flying capacitors with different voltages are connected in parallel directly, which not only produces excessive heating and over stress in the power switches, but also damage the operation of the converter. Therefore, dead-band control must be incorporated in the PWM controller of the FC converter.

Generally, dead-band control separates transitions on complementary PWM signals for a fixed period of time. While it is possible to perform software implementation of dead-band, the DSP LF2407 offers on-chip hardware for this purpose that requires no additional CPU overhead. It offers more precise control of gate timing requirements. Moreover, it is specified with a single program variable that is easily changed for different power converters or adapted on-line. Additionally, the Semidrivers SKHI61 and SKHI71 provide the interlock dead time as an optional feature. It is very convenient to add a dead-band time by making use of either the DSP or the driver.

7.3.2 Modulo Method

In the design of the prototype, the generation of the sine wave is performed using a look up table for simplicity. In order to be able to control the frequency of the modulation with some accuracy, a method based on the modulo mathematical operation is used (i.e. any overflow is disregarded and only the remainder is kept) [108].

In this application a 16-bit counter is used to determine the location of the next value. A step value is added to the counter every time a new value from the sine table is to be loaded. By changing the value of the step, one can accurately control the frequency of the sine wave.

Although a 16-bit counter is used, the upper byte determines the location of the next sine value to be used; thus, by changing how quickly values overflow from the lower byte (i.e., manipulating the step value), the frequency of the sine wave can be changed. The modulo mathematical operation is used when there is an overflow in the accumulator from the lower word to the upper word. When an overflow occurs, only the remainder (lower word) is stored.

For example, the counter is set to 0000h and the step value is set to 40h shown in Table 7.1. Every time a value is to be looked up in the table, the value 40h is added to the counter; however, since the upper byte is used as the pointer on the look up table, the first, second, and third values will point to the same location. In the fourth step, which results in an overflow into the upper byte, the loaded value will change. Because the upper byte is used as the pointer, the look-up table has 256 values, which is equivalent to the number of possibilities for an 8-bit number: 0 to 255. Additionally, since the upper word of the accumulator is disregarded, the pointer for the sine look up table does not need to be reset.

Table 7.1: Look-up Table example

Step	Accumulator	Counter	Pointer	Step Value=40h
0	0000 0000h	0000 h	00 h	1st value of sine table
1	0000 0040h	0040h	00h	
2	0000 0080h	0080h	00h	
3	0000 00C0h	00C0h	00h	
4	0000 0100h	0100h	01h	2nd value of sine table
•	•	•	•	•
•	•	•	•	•
n	0000 FFC0h	FFC0h	FFh	256th value of sine table
n+1	0001 0000h	0000h	00h	1st value of sine table
n+2	0001 0040h	0040h	00h	

The step size controls the output frequency. As a result, the larger the step, the quicker the overflow into the upper byte, and the faster the pointer traverses through the sine look-up table. Although the step size indicates how quickly the pointer moves through the look up table, the step size does not provide much information about the approximate frequency that the sine wave will be modulating the PWM signal. In order to determine the frequency of the sine wave, information about how often the value in the compare register is modified must be known.

If the routine to load a new value in the compare register is accessed every time that the timer value matches the value in the period register, the routine is accessed at the same frequency as the PWM signal. Because the compare register is updated each time that the period register and the timer values are equal, the routine that modifies the compare register is implemented as an interrupt service routine.

The frequency of the sinusoidal waveform to be modulated can be calculated from the following formula:

$$f_o = \frac{step\ size}{T_s \times 2^n} \tag{7-3}$$

where f_o is the desired frequency of the modulating waveform, T_s is the time period between each update (in this case, the PWM period), n is the number of bits in the counter register (here, n=16).

It can be seen from eq. (7-3) that the frequency of the PWM signal to be modulated is proportional to the step size and inversely proportional to the size of the counter register and the period at which the routine is accessed. Thus, to change the resolution in order to increase or decrease the frequency of the PWM, one needs to have a larger counting register or access the routine at a slower frequency by increasing the period.

7.4 Three-Phase Three-Level FC Converter

7.4.1 Power Circuit

Fig. 7.5 shows the schematic diagram of the three-phase three-level FC converter.

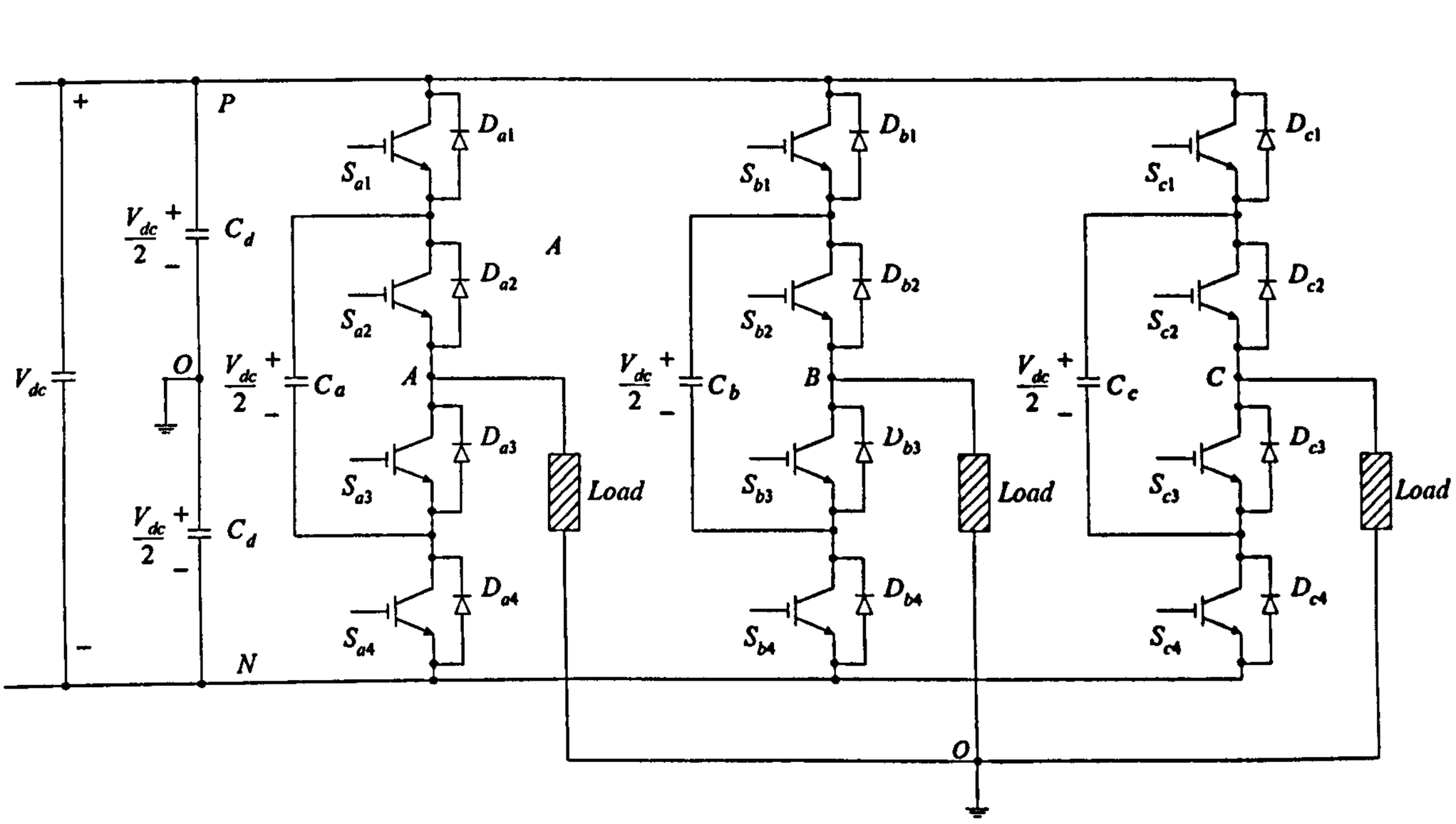


Fig. 7.5: Schematic diagram of the three-phase three-level FC converter.

C_d is the DC link capacitor. Two DC link capacitors are used to provide the neutral point of the V_{dc}, thus splitting the V_{dc} to $\pm V_{dc}/2$. C_a, C_b, C_c are the so-called flying capacitors. Before the converter is put into normal operation, the flying capacitors must be pre-

charged to their respective voltage i.e., $V_{dc}/2$. (S_{x1}, S_{x4}), (S_{x2}, S_{x3}) are complementary switching pairs, $x=a, b, c$. The operating principle can be explained with the help of the following Table 7.2. Through the different switch states of IGBTs, each phase voltage can take up three values as follows: - $V_{dc}/2$, 0, $+V_{dc}/2$.

Table 7.2: Switch state and phase output of the three-level FC converter

Switch State				Phase output
S_{x1}	S_{x2}	S_{x3}	S_{x4}	V_{xo}
1	1	0	0	$+V_{dc}/2$
1	0	1	0	0
0	1	0	1	0
0	0	1	1	$-V_{dc}/2$

Fig. 7.6 illustrates the PS-MSPWM control method. There are two carriers which are phase-shifted by 180° (i.e., half of the carrier period), and three sinusoidal reference signals which are phase shifted by 120° (i.e., one third of the modulating period). The PWM gate signal for any individual switch is determined by comparison of the corresponding triangular carrier with the modulating reference sinusoidal signal. T_s is the carrier period, T_o is a period of the sinusoidal wave. Taking phase A as an example, the PWM gate signal for S_{a1} is generated by the direct comparison of carrier 1 with reference A, while the gating signal for S_{a2} results from the direct comparison of carrier 2 with reference B. The same rule applies to all other phases and the required phase-shifts must be adhered to.

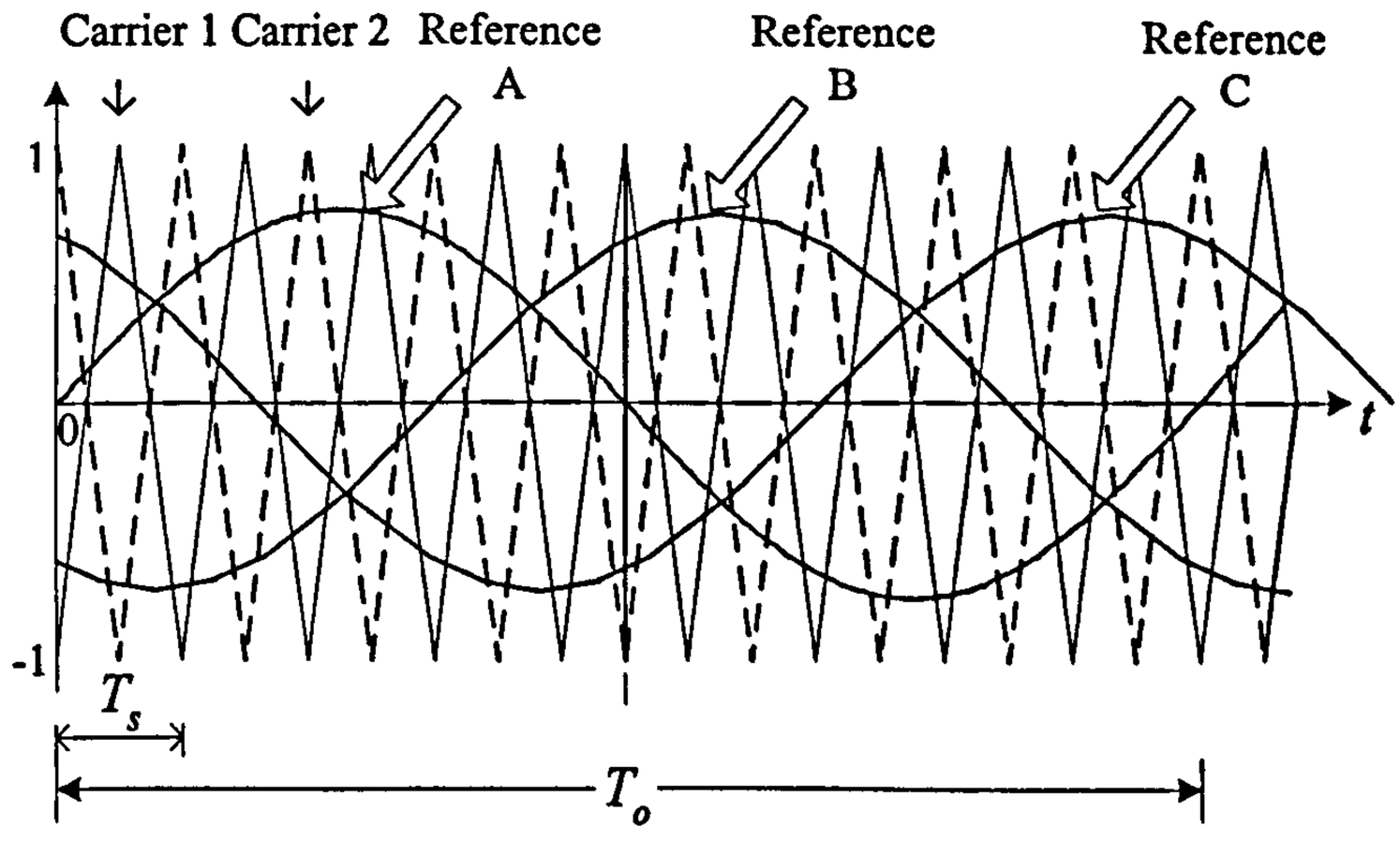


Fig. 7.6: PS-MSPWM method for the three-phase three-level FC converter.

7.4.2 PWM Generator

LF2407 DSP provides the PWM waveform generation via its event managers. There are two event managers, named EVA and EVB in the peripherals of the LF2407 DSP. They are identical to each other in terms of functionality. Register mapping and bit definitions are also identical, with the exception of naming conventions and register addresses. The block diagram of the EVA is shown in Fig. 7.7. Each event manager consists of General-Purpose (GP) timers, full compare units, capture units, and Quadrature Encoder Pulse (QEP) circuit. It is very convenient to make use of the GP timers and the compare units of the event manager to generate PWM waveforms.

PWM Channels Assignment

The three-phase three-level FC converter needs 6 pairs of complementary PWM signals with the dead band to avoid shoot through fault. Two full compare units in the EVA and EVB can undertake this task. This is possible because there are three full compare units in each event manager module. Each full compare unit has three compare registers, called full compare and associated with each PWM channel pair. It also has software programmable dead band modules. Fig. 7.8 illustrates the assignment of PWM channels to 12 switches on the three-phase three-level FC converter.

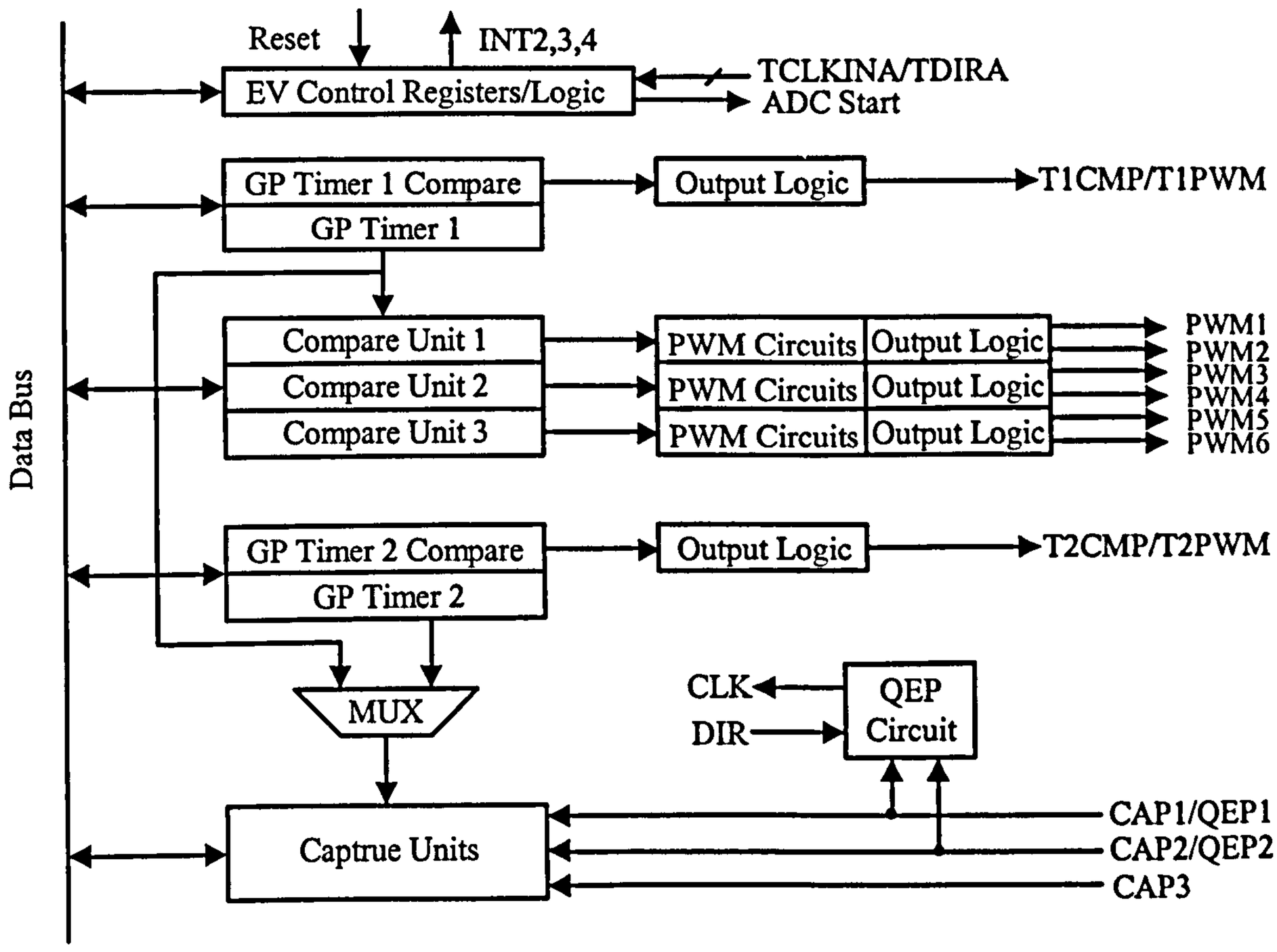


Fig. 7.7: Block diagram of the event manager EVA.

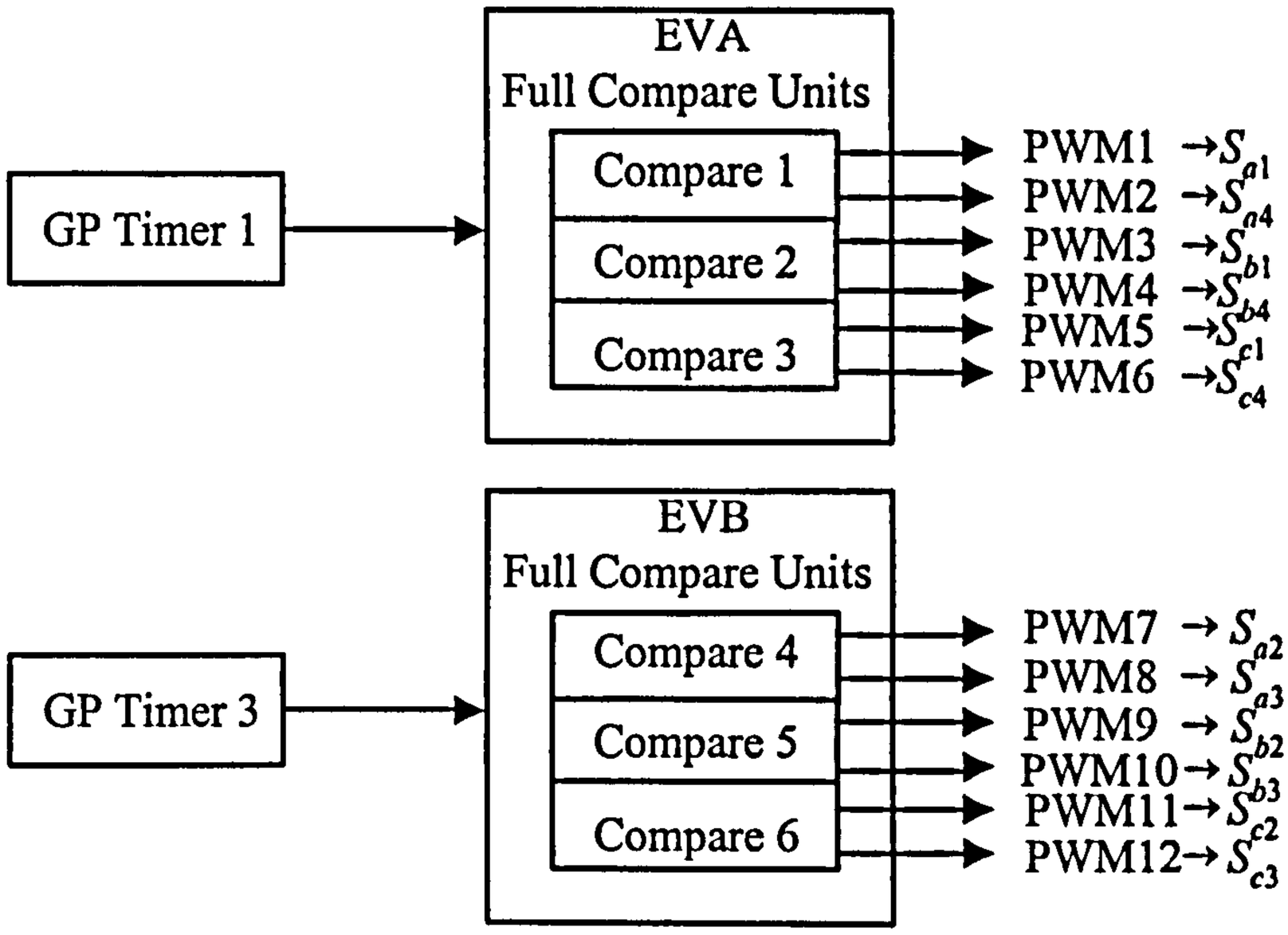


Fig. 7.8: The assignment of PWM channels for a three-phase three-level converter.

As mentioned before, the complementary switches of the FC converter need the dead band control that can be easily realised by the software dead band generator modules associated with the full compare units. The DSP controller TMS320F2407 has such a programmable dead band generator to insert a dead band between two PWM outputs (PWM1&2, PWM3&4, and PWM5&6). The polarity of PWM channels (active high or active low) can be controlled using the compare Action Control (ACTR) register. The appropriate dead band between two PWM outputs can be inserted using the Dead Band Timer CONtrol (DBTCON) register. The dead band circuitry of the TMS320F2407 reduces the active portion of the odd PWM channels (PWM1, PWM3, and PWM5) from the leading transition end. However, the dead band circuitry of TMS320F240 increases the active portion of the even PWM channels (PWM2, PWM4, and PWM6) from the lagging transition end.

Regular PS-MSPWM Implementation

Usually, the regular sampling of the SPWM method is used in the DSP controller. Unlike naturally sampling SPWM method, this method takes regular periodic samplings and uses the sample-and-hold data as the modulation signals in the predictions of the pulse widths in the SPWM strategy. By making use of regular sampling, the DSP can be free to perform computational functions, including the computation of the switching times which are then

loaded onto the counters. It should be indicated that the accuracy of regular SPWM method relies on the value of the frequency modulation ratio m_f which is defined as the ratio of the switching frequency f_c to the modulating reference frequency f_o. The higher the m_f, the higher accuracy. Since m_f is reasonably large, the reference value can be assumed to be constant over the entire switching period.

Fig. 7.9 illustrates the regular sampling PS-MSPWM for the three-phase three-level FC converter. The timer counter is operating in continuous up/down mode. The sampling instants occur at timer 1 period interrupt (i.e. counter value equals to one half of the period of the carrier 1). The sampling frequency is f_c. Applying sample and hold, the original modulation signal becomes the stepped waveform, the modulation value is held constant in the sampling period T_s. The sine value is read from a look up table and then the computed reference values are loaded into compare registers. When compare match event happens, i.e., when the value of the counter is found to be equal to the value loaded in the compare register, a PWM waveform will be generated automatically. Here, DBT refers to the dead-band time between the complementary PWM outputs which are configured as active high and active low respectively.

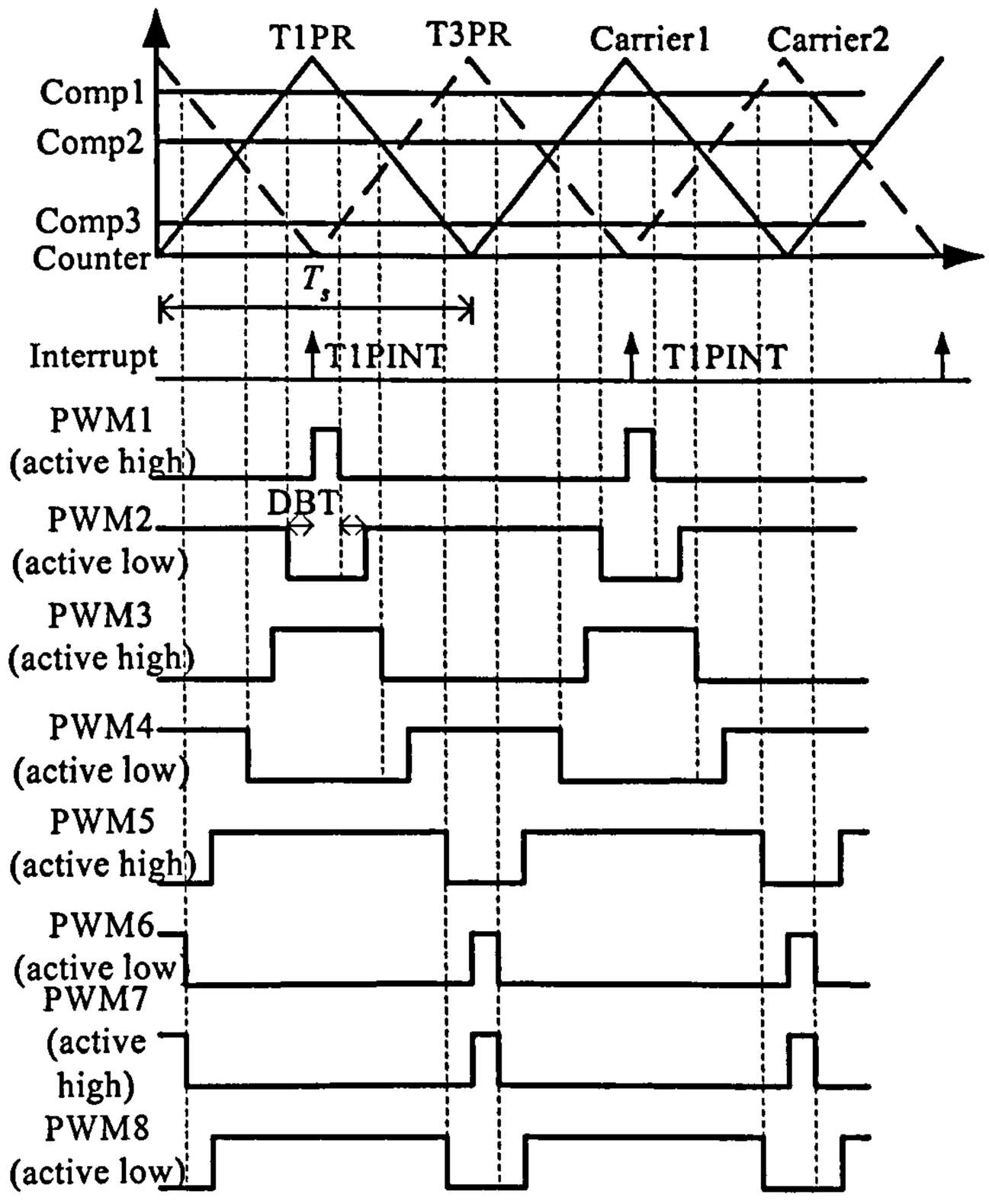


Fig. 7.9: Regular PS-MSPWM implementation on the DSP Event manager.

Software Organisation

The software implementation is illustrated in Figs. 7.10 and 7.11. In Fig. 7.10, x stands for A or B. The main program shown in Fig. 7.10 consists of LF2407 DSP CPU and its peripheral initialisations, for example, Phase-Locked-Loop (PLL), watchdog, event manager, interrupt and so, together with some parameters associated with the sine wave value. The Interrupt Service Routine (ISR) shown in Fig. 7.11 is invoked every 625 μs (1.6 kHz) by the GP Timer 1 period interrupt, in which compare registers are updated with normalised sine values to generate the sine wave modulated PWM signals. Normalisation of the sine value is to prevent the compare value from being negative.

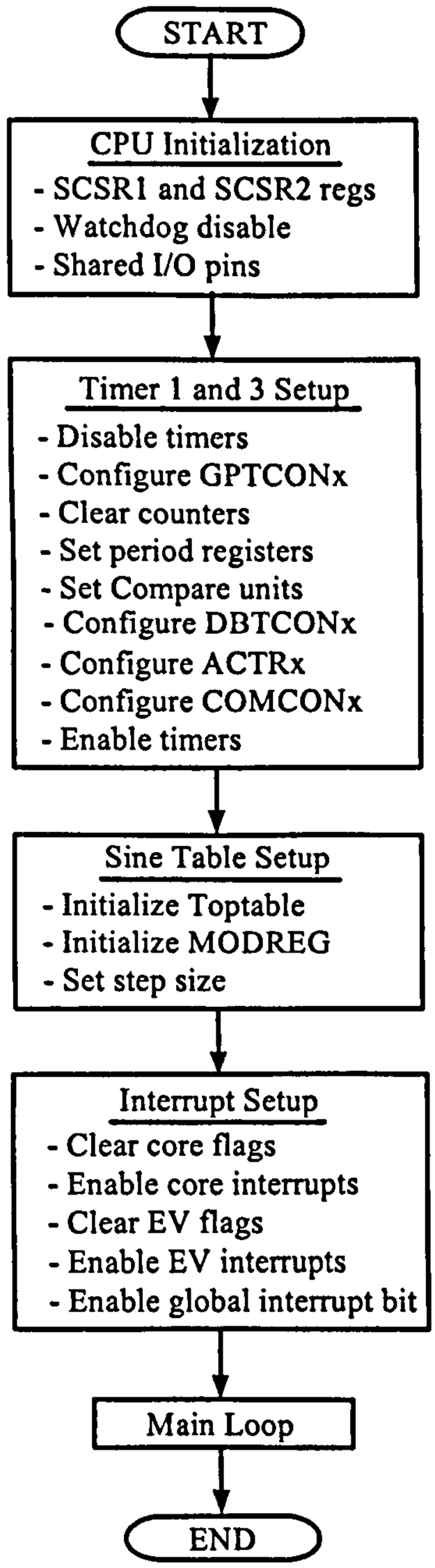


Fig. 7.10: Main program flowchart of the DSP controller for the three-phase three-level FC converter.

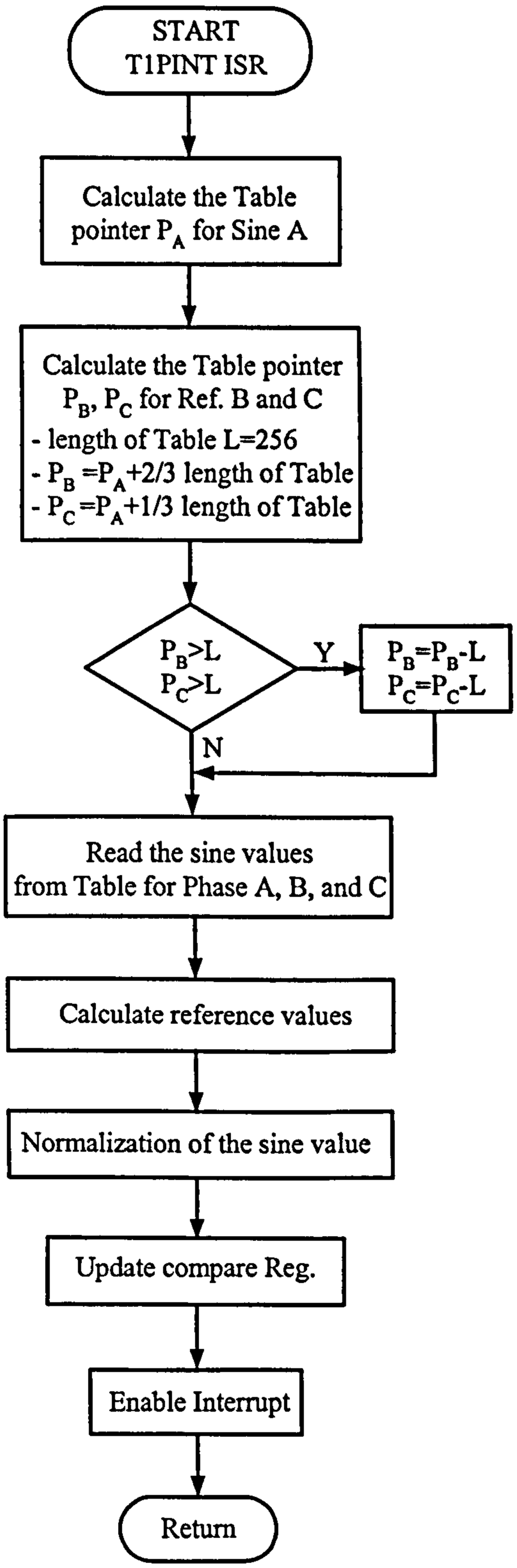


Fig.7.11: T1PINT interrupt service routine flowchart of the DSP controller for the three-phase three-level FC converter.

In the main program, the initialisation of some related modules covers:

PLL Module

The first module that needs to be configured is the PLL module. The PLL clock module provides all the necessary clock signals for the LF2407. It is important to know the speed of the CPUCLK in order to create the proper PWM frequency. Since the TMS320LF2407 EVM is equipped with a 15 MHz crystal oscillator. The core CPU receives CLKIN/2 as CPUCLK by hardware setting. After reseting the PLL clock module defaults to CPUCLK*4, the resulting CPUCLK frequency is 30 MHz. System Control and Status Register 1 and 2 (SCSR1 & SCSR2) are used to configure the PLL module.

$$\text{CPUCLK (Hz)} = \text{CLKIN(OSC)} \times \frac{\text{PLL Multiplication Ratio}}{\text{PLL Divide by 2}} \qquad (7\text{-}4)$$

Digital I/O Ports

Because the Digital I/O Ports pins are shared with pins of other peripherals of the TMS320F2407, the pins necessary to output the PWM signal need to be configured. Specifically, the Output Control Register A (OCRA) needs to be configured.

Event Manager Module–General Purpose Timer

Once the CPUCLK frequency has been determined from the PLL module and the output pin has been configured for the PWM outputs, the GP Timer 1 and Timer 3 in the Event Manager Module can be configured. To create a PWM signal, the registers General Purpose Timer Control Register (GPTCON), Timer x Counter Register (TxCNT), Timer x Period Register Buffer (TxPR), Timer x Control Register (TxCON), Dead-Band Timer Control Register x (DBTCONx), Compare Action Control Register x (ACTRx), and Compare Control Register x (COMCONx) need to be set.

To create an asymmetric PWM signal, the timer is set to the continuous-up count mode, while if a symmetric PWM signal is desired, then the timer should be set to the continuous-up/down count mode. Since the CPUCLK is 30 MHz, it is easy to obtain a 1.6kHz signal without pre-scaling the input clock, thus the prescale is set to divide by 1.

$$\text{PWMCLK (Hz)} = \frac{\text{CPUCLK}}{\text{Input Clock Prescaler}} \qquad (7\text{-}5)$$

In addition, some parameters have to be calculated in advance before programming as follows:

- **The value loaded into the timer period register TxPR** (here, x=1 or 3)

This value is determined by the PWM carrier frequency and the frequency of the clocking signal. Suppose it is desired to generate 1.6 kHz PWM (625 μs) using a 30 MHz (33.3 ns) CPU clock to drive the GP timer with the ÷1 prescale option. The value needed in the period register is then:

Symmetric PWM:

$$\text{TxPR} = \frac{\text{switching period}}{2\,(\text{timer period})} = \frac{625\mu s}{2\times(33.3ns)} = 9384 = 24A8h \tag{7-6}$$

Asymmetric PWM:

$$\text{TxPR} = \frac{\text{switching period}}{\text{timer period}} - 1 = \frac{625\mu s}{33.3ns} - 1 = 18767 = 494Fh \tag{7-7}$$

Since the GP Timers start counting from zero, to calculate the value that should be loaded into the period register, 1 should be subtracted from the calculated value obtained to input into register T1PR. Similarly, to find the correct value in the compare register, 1 should also be subtracted from the calculated value obtained to input into compare register.

- **Step value**

To be able to control the frequency of the modulation with some accuracy, a method based on the modulo mathematical operation is used (i.e. any overflow is disregarded and only the remainder is kept). Here, a 16-bit counter named MODREG is used to determine the location of the next value. A step value is added to the counter every time a new value from the sine table is to be loaded.

$$\text{Step Value} = \frac{T_s \cdot 2^n}{T_o} \tag{7-8}$$

where, T_o is the desired modulating wave period, T_s is the time period between each update (in this case, the PWM carrier period), n is the number of bits in the counter register (n=16). The above formula also means that the frequency of the modulated PWM signal is proportional to the step value and inversely proportional to the size of the counter register and the period at which the routine is accessed.

- **Normalised reference sine value V'_{ref}**

$$V'_{ref} = \frac{TxPR}{2} \cdot (V_{ref} + 1) \tag{7-9}$$

Here, V_{ref} is the original sine value from the look-up table.

The generation of the sine wave is performed using a look up table. Three reference sine waves share a look-up table that has 256 entries, angle range of 0-360 degree and Q15 number format with range [-1, 1].

Since this program is interrupt driven, once the registers have been set for the PWM signal, the program can be ended with an unconditional branch and the output will continue because of the interrupt structure. The output will stop when the user halts the program or the software masks the corresponding interrupt levels.

7.5 Single-Phase Five-Level FC Converter

A single-phase five-level flying capacitor converter prototype based on the TMS320LF2407 DSP and IGBT VSI was developed. Its building block diagram is shown in Fig. 7.12. The system is composed of the power circuit, the charging circuit, voltage and current transducers, voltage and current sense amplifier circuit, signal conditional interface board, and drives. In the following sections, each main circuit design and some practical issues encountered during the development are discussed.

7.5.1 Power Circuit Design

A generic circuit diagram of single-phase five-level flying capacitor converter has been shown in Fig. 4.1. Its operating principle has been described in Chapter 6. When designing the practical power circuit, the following issues need to be considered.

Latchup in IGBTs

When the continuous on-state current exceeds a critical value, it may latch up at drain current values less than the static current value under dynamic conditions when the IGBT is switching from on to off. Once the IGBT is in latchup, the gate no longer has any control of the drain current. If latchup is not terminated quickly, the IGBT will be destroyed by the excessive power dissipation.

There are several steps that can be taken to avoid latchup. One step is to design circuits where the possibilities of overcurrents that exceed I_{DM} are minimised. However, it is impossible to eliminate this possibility entirely. Another step that can be taken is to slow down the IGBT at turn off. This increase in the turn-off time is easily accomplished by using a larger value of series gate resistance R_G.

In the prototype, a latch-up free SEMIKRON IGBT module was employed.

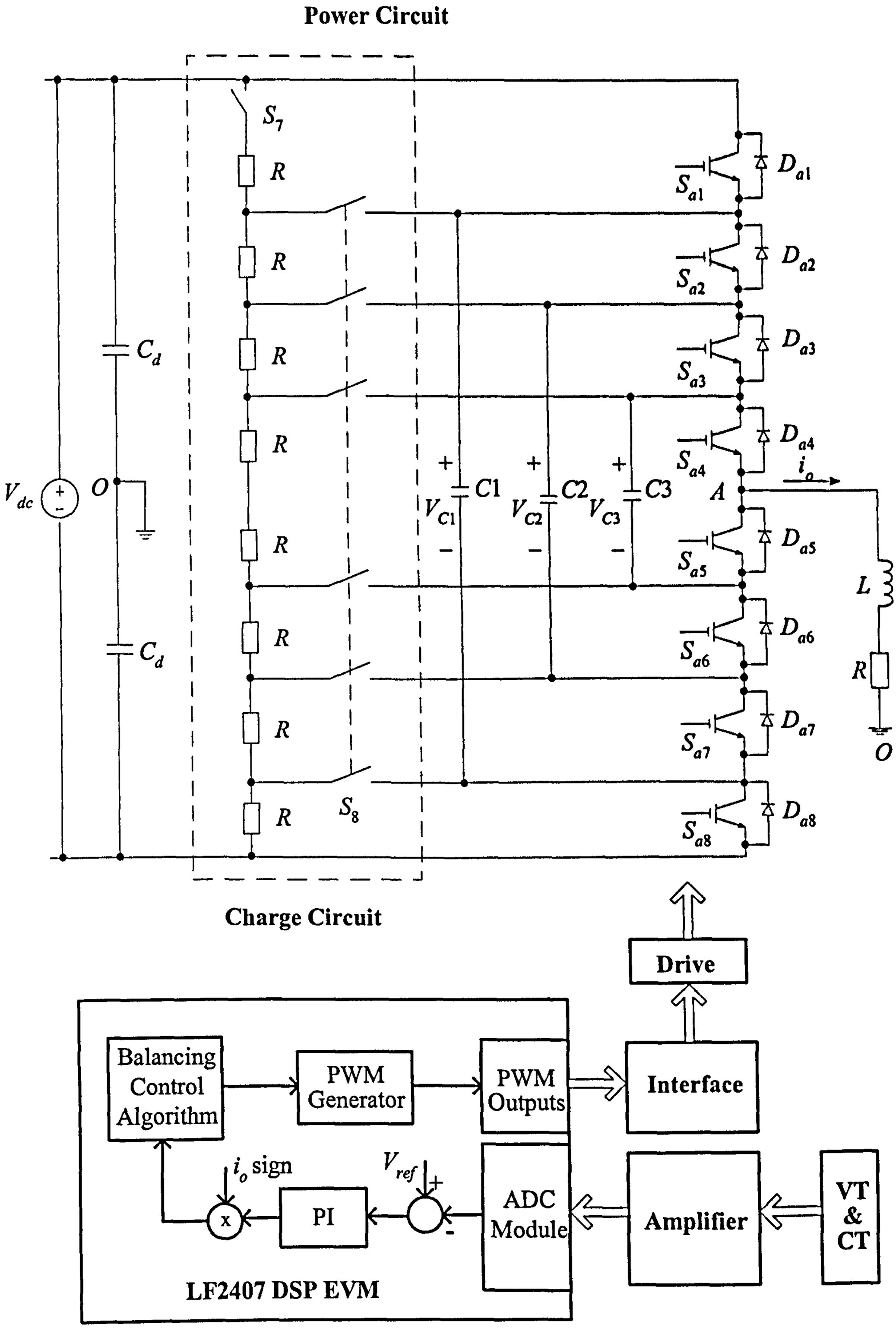


Fig. 7.12: Building block of a single-phase five-level FC converter.

Reduction of Stray Inductance

Care must be taken when designing the layout of the power circuit, high *di/dt* exists during the IGBT turn-on and turn-off and high over voltages will be generated in the event of a substantial high stray inductance. Some steps of reducing the stray inductance can be made in drive circuit, bus bar, and leads in the circuits or circuit layout. For example, to minimise stray inductances, the floating capacitor must be arranged as close as possible to the IGBT modules. These modules are connected with multi-layer busbars instead of cables [15].

(1) Minimise stray inductance in drive circuits

In minimising the stray inductance, all power devices should be treated as four terminal devices having two control terminals and two power terminals. To facilitate the reduction of the stray inductance, in high-power switch modules, manufacturers provide a separate emitter terminal for the connection of the drive circuit.

(2) Reduction of stray inductance in the bus bar

Leakage or stray inductance in power supply leads (bus bars) can be a problem in circuits that experience large values of *di/dt*. Copper strips, with a thin insulator sandwiched between them comprises a transmission line and provides an excellent means of reducing the stray inductance. Moreover, they have the added benefit of reducing stray magnetic flux and hence EMI. Using such strips establishes the upper limit in reducing stray inductance, but it may be clumbersome in practice. The actual design then can be adapted to meet the manufacturing and cost constraints.

(3) Minimise stray inductance in leads connecting drive with power switches

In many designs, the basic drive circuit may be on a printed circuit board at some distance away from the power switch, which is mounted on a heat sink. A twisted pair should be used to minimise the stray inductance and the inductive pick up of noise in the base and emitter terminals to avoid oscillations and the problem of retriggering at the turn-off of the IGBT.

Reduction of Over-Voltage

During the IGBT turn-on and turn-off, large over-voltages may develop across due to large values of *di/dt* if high stray inductance exists. To reduce the over-voltage, besides careful circuit layout considerations to reduce the stray inductance existing in circuits, snubber circuits or control of the turn-off times can be used to further reduce the over-voltage.

Additionally, a polypropylene capacitor with very low inductance can be mounted directly across the IGBT to reduce voltage sparks across the IGBTs.

The voltage variation across the flying capacitor is inversely proportional to the capacitance and proportional to the load current which is related to the load conditions in terms of eq. (7-10).

$$\Delta V_c = \frac{i_{cap}}{C_e} \cdot \Delta t_c = \frac{d_c i_o}{C_e} \cdot \frac{1}{f_s} \tag{7-10}$$

Here, ΔV_c is the voltage variation across the flying capacitor, i_{cap} is the current flowing through the capacitor, C_e is the capacitance, Δt_c is the variation time, i_o is the load current, f_s is the switching frequency, d_c is the duty cycle of i_{cap}. It can be seen from the above equation that the capacitor's voltage inevitably varies in some range around the average nominal voltage. Large capacitance value, high switching frequency, and/or low output current all contribute to low voltage variation. However, when a large capacitance is chosen, the volume is increased along with cost and packaging.

In addition, as mentioned before, the average voltage across the flying capacitors inevitably deviates from the nominal value due to the non-ideal power switches. So the voltage balancing regulator is necessary. It could be implemented via hardware or software. In this design, the flying capacitor voltage balancing is completed through the software via a DSP controller. Its principle has been given in Chapter 5. Table 7.3 lists the main parameters of the prototype.

Table 7.3: Parameters of the prototype of single-phase five-level FC converter

Items	Description
DC Voltage	V_{dc}=120 V
DC bus capacitors	*C1*=*C2*=1500 μF, 350 V
Flying capacitors	*C3*=*C4*=*C5*=1500 μF, 350 V
Load	R=45 Ω, L=10 mH
Switching frequency	f_c=1600 Hz
Line frequency	f_o=50 Hz
Power device (IGBT)	SKM75GB123D, I_c=75 A, V_{CES}=1200 V

7.5.2 Charging Circuit Design

The structure of a flying capacitor multilevel is built in such a way that the flying capacitor need to be charged to their desired voltage levels prior to switching of the inverter. As shown in Fig. 4.1, V_{C1}, V_{C2}, *and* V_{C3} need to be charged to $3V_{dc}/4$, $V_{dc}/2$, $V_{dc}/4$ respectively before the converter moving into the normal operation. Fig. 7.12 illustrates a five-level FC converter with a pre-charging circuit. There is a pre-charging circuit inside the dotted box.

This pre-charging circuit is composed of eight resistors with the same value, switch S_7, and switch S_8. Switch S_8 includes six switches, formed by two relays, each with three switches. These six switches are controlled by one signal and can be regarded as one switch labelled S_8. The eight resistors are connected in series to form a voltage divider. This series of resistors is connected with main power circuit through S_7, and with three flying capacitors through S_8. The operation of the pre-charging circuit is realised in terms of the following procedures. First, turn off all the power switches S_{a1} to S_{a8}, turn on the S_7, then turn on the S_8. The charging circuit begins to charge $C1$, $C2$ and $C3$. Second, when the voltages across flying capacitors V_{C1}, V_{C2}, *and* V_{C3} are measured to reach the desired value $3V_{dc}/4$, $V_{dc}/2$, $V_{dc}/4$ respectively, turn off S_8, then turn off S_7, to remove the charging circuit from the main power circuit. Third, run the DSP program and output the PWM gating signals to the power switches, thus the converter enters into the normal operation.

Additionally, it should be noted that it is not enough to turn off all the power switches to stop the operation of the converter. Since there is energy in flying capacitors, the energy stored in the capacitors must be released before a new operation begins for safety. It can be completed with the help of this charging circuit, but now acting as a discharging circuit. The procedure is similar to the charging procedure. First, turn off all the power switches, then turn off the power supply. Second, turn on S_7, then turn on S_8, and the flying capacitors will discharge through the eight resistors quickly. Third, turn off S_8, then turn off S_7 after that V_{C1}, V_{C2}, *and* V_{C3} decrease to 0 Volts.

7.5.3 Voltage and Current Measurement

The three voltages across flying capacitors, V_{C1}, V_{C2}, V_{C3} and load current i_o need to be measured for the voltage balancing controller.

Voltage Measurement

The voltage transducer LV 25-P from LEM is employed for voltage measurement. This PCB mounting VT, based on the use of Hall effect, is suitable for the electronic

measurement of voltage associated with DC, AC, and impulse circuits. The unit provides galvanic isolation between the primary and secondary circuits. In order to enable a voltage to be measured a current proportional to the measured voltage must be collected through an external resistor R_1, selected by the user, in series with the primary circuit of the unit. This type of VT provides an instantaneous output and has the advantage of high accuracy, good linearity, fast response and good isolation. Its circuit connection is shown in Fig. 7.13.

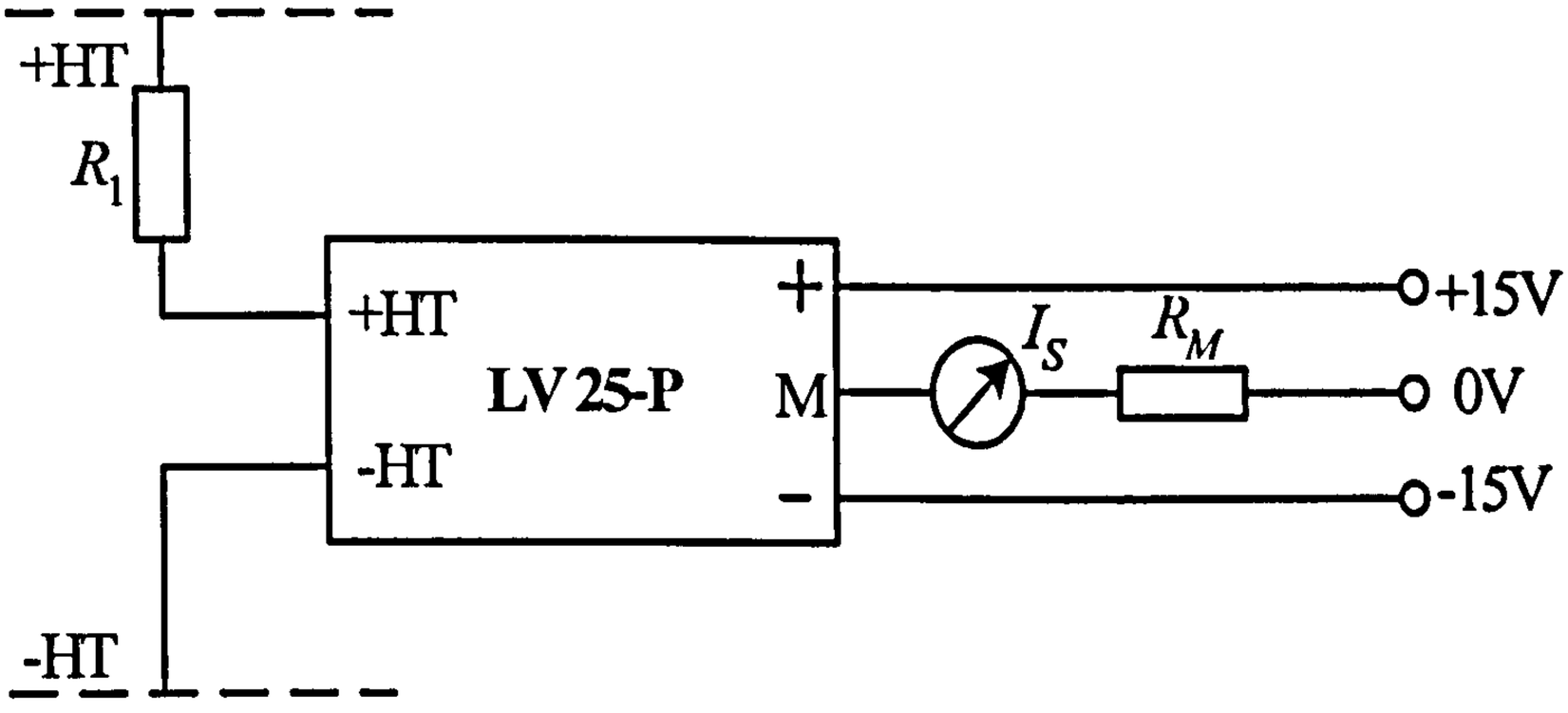


Fig. 7.13: Circuit connection of the voltage transducer.

Here, the primary circuit of the transducer must be linked to the connections where the voltage has to be measured. A positive output current is obtained on terminal M (i.e. I_S is positive) when a positive voltage is applied on terminal +HT of the primary circuit. The selection of the primary resistor R_1 is based on two rules: accuracy and operating range of the VT. Since the transducer's optimum accuracy is obtained with the nominal primary current, as far as possible, R_1 should be calculated so that the nominal voltage to be measured corresponds to a primary current of 10 mA.

For example: Voltage to be measured V_n=250 V

(1) R_1=25kΩ/10W, I_{prim}=10 mA, Accurary=±0.6% of V_n at 25 °C.

(2) R_1=50kΩ/5W, I_{prim}=5 mA, Accurary=±1.2% of V_n at 25 °C.

Operating range: Taking into account the resistance of the primary windings (which is 250 Ω, must remain low compared to R_1, in order to keep thermal deviation as low as possible) and the isolation, this transducer is suitable for measuring nominal voltage of 10 V to 500 V.

In the secondary side, there are three terminals that are used to provide the power supply and measure terminal. Here, the power supply is ±15 V, the measuring resistor R_M=160 Ω (the range should be 100 to 350 Ω, with ±15V@±10mA$_{max}$), conversion ratio

K_N is 2500:1000, Primary nominal rms current I_{PN}=10 mA, Secondary nominal rms current I_{SN}=25 mA. Primary nominal rms voltage V_{PN}=500 V, Maximum measurable voltage V_P=700 V, overall accuracy at 25 °C is ±0.6% of I_N, linearity <0.2%, response time< 40 µs. A 27 kΩ fixed resistor and a 5 kΩ variable resistor is chosen as R_1 for the prototype.

Current Measurement

Often in high-power applications, electronics isolation is required between the current to be measured and the control electronics. For AC current, current transformers can be used. If there is a DC bias in the current, the current transformer will not work. The instantaneous current must be measured that includes the DC bias. In such cases, the current can be measured by a Hall-effect current sensor. In this current sensor, the secondary winding is applied a compensating current such that the field in the toroid is kept at zero. In this way, current from DC up to 100 kHz bandwidth can be measured.

The current transducer LA 125-P from LEM is employed. This compact, low profile PCB mountable CT employs the Hall effect principle to accurately measure AC, DC, or complex current. The transducer uses the feedback operating technique and has high accuracy analogue outputs. The primary current is sensed by passing the conductor through a hole. This type of CT has such advantages as excellent accuracy; very good linearity; low temperature drift; optimised response time; wide frequency band with; no insertion losses; high immunity to external interface; current overloaded capability. Its circuit connection diagram is shown in Fig. 7.14.

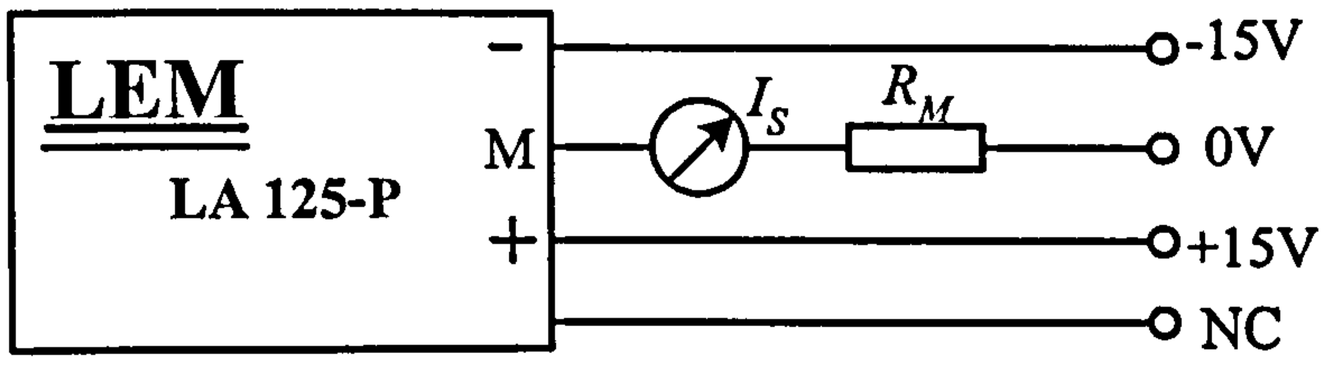


Fig. 7.14: Circuit connection of the current transducer.

In the secondary side, there are four terminals. One terminal named NC is useless, the other three terminals are used to provide the power supply and the measure terminal. Here, power supply is ±15 V, measuring resistor R_M=50 Ω (the range should be 25 to 74 Ω, with ±15V@±125A_{max}), conversion ratio K_N is 1:1000, Primary nominal rms current I_{PN}=125 A, Secondary nominal rms current I_{SN}=125 mA. Measuring range is limited to I_{PN}=±200 A, overall accuracy at 25 °C is ±0.6% of I_{PN}, linearity <0.15%, response time< 1 µs.

When using the above CT, care must be taken. For example, dynamic performances (*di/dt* and response time) are best with a primary bar in low position in the through hole. In order to achieve the best magnetic coupling, the primary windings have to be wound over the top edge of the device. When measuring lower currents than the nominal 125 A, an increase in sensitivity can be achieved by increasing the number of times the primary current conductor passes through the centre hole. For example, to measure 12.5 A using I_{PN} =125 A CT, 10 passes of the cable can be arranged giving 125 ampere turns and a full output current or voltage signals is derived.

7.5.4 Voltage and Current Sense Amplifier Circuit

Usually, the measured voltages and current need to be scaled and/or level shifted to bring them into the range of Analogue-to-Digital Converter (ADC) by using the voltage and current sense amplifier circuit shown in Fig. 7.15.

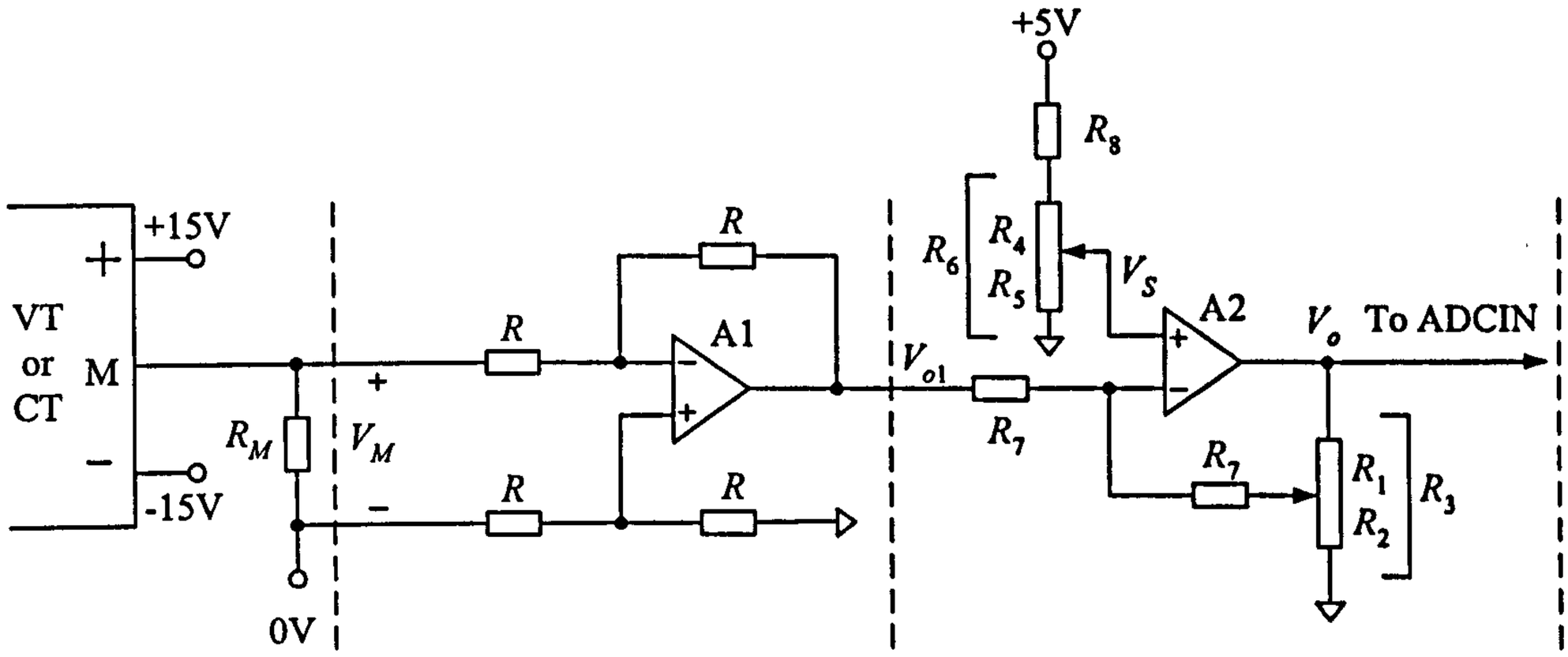


Fig. 7.15: The voltage and current sense amplifier circuit.

The above voltage and current sense amplifier circuit consists of two amplifiers. The first one employs difference amplifier whose input is measuring voltage from the CT or the VT. The objective of employing such a difference amplifier is to minimize the impact of the measuring circuit in the measured quantity. Because the input impedance of the difference amplifier can be regarded as infinitely large so that it does not affect the measuring voltage, thus increasing the accuracy of the measurement. The second one acts as proportional amplifier and level shifting. The output functions of the two amplifiers are expressed as:

$$V_{o1} = -V_M \tag{7-11}$$

$$V_o = -\frac{(500 + R_1 R_2)}{10R_2} V_{o1} + \frac{(1000 + R_1 R_2)}{10R_2} V_S \tag{7-12}$$

$$V_S = \frac{5 \cdot R_5}{R_8 + R_6} \tag{7-13}$$

Replace eqs. (7-11) and (7-13) into (7-12), the total relationship between the input and output is expressed as:

$$V_o = \frac{(500 + R_1 R_2)}{10R_2} V_M + \frac{(1000 + R_1 R_2)}{10R_2} \cdot \frac{5R_5}{R_8 + R_6} = k_1 \cdot V_M + k_2 \tag{7-14}$$

For the voltage amplifier, no level shifting is needed because the voltages are DC values. So let V_S becomes zero via adjusting the resistor R_6. Adjust the resistor R_3 (R_3 is the sum of the R_1 and R_2) to change the k_1. For the current amplifier, input current needs to be scaled and level shifted to bring the output voltage into the range of ADC because the input current is AC current, while the ADC inputs require the range of 0V to 3.3 V. The output current, the corresponding sensor output voltage V_M, the input voltage to ADC channel, and the resulting ADC data register values are listed in Table 7.4. The counterpart of the voltage scaling is listed in Table 7.5.

Table 7.4: Output current scaling and level shifting

I_o (A)	V_M (V)	V_o (V)	ADCFIFO
+3	1.25	3.3	FFC0h
0	0	1.65	7FC0h
-3	-1.25	0	0000h

Table 7.5: Voltage scaling

V_{C1} (V)	V_M (V)	V_o (V)	ADCFIFO
+100	2	3.3	FFC0h
0	0	0	0000h

7.5.5 DSP-Based Controller Design

The block diagram of a DSP-based controller with some interfaces is shown in Fig. 7.16. As mentioned before, four signals are required to implement the control algorithm: three voltages across flying capacitors, and output current. These instantaneous signals i_o, V_{C1}, V_{C2}, V_{C3}, are all sensed and conditioned by the voltage and current amplifiers inside the block labelled Voltage and Current Sense Amplifier. The sensed signals are then fed back

to the DSP by the four ADC channels ADCIN0, ADCIN1, ADCIN2, and ADCIN3, respectively. The digitised sensed voltages V_{C1}, V_{C2}, V_{C3}, are each compared with their desired reference voltages V_{C1}*, V_{C2}*, V_{C3}*, and the differences are fed into the PI regulators PI1, PI2, and PI3, respectively. The outputs of PI regulators multiply the sign of the output current i_o which has positive sign when it is greater than zero, while it has negative sign when it is lower than zero. The products of the outputs of PI regulators and the sign of the current i_o are inputs for the Balancing Control Algorithm block. The final adjusted new reference modulating values from balancing control algorithm block are sent to the PWM generator which produces four PWM outputs. Below, each used module in the controller is explained.

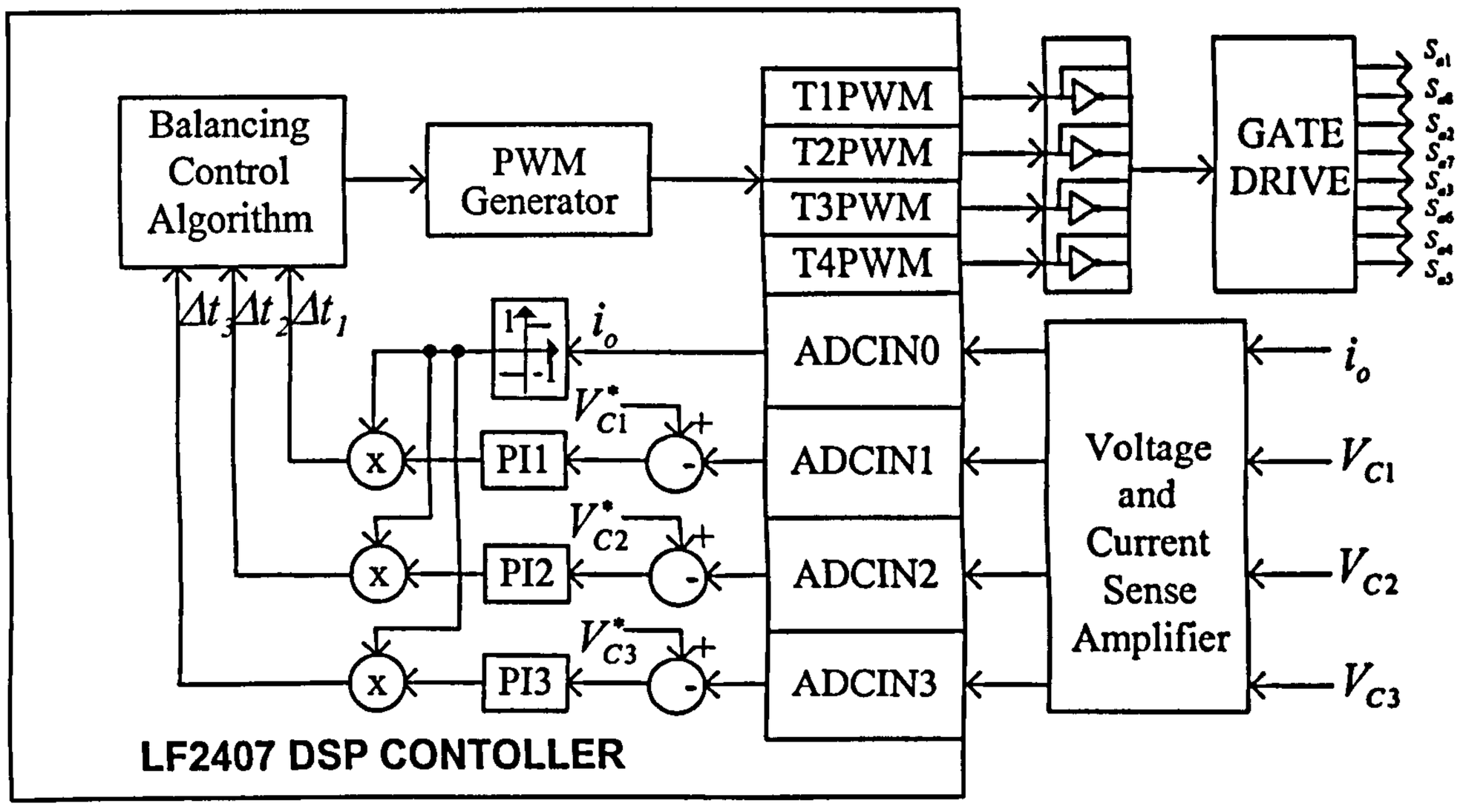


Fig. 7.16: Block diagram of a DSP-based FC converter controller for the single-phase five-level FC converter.

ADC Module

The ADC module in the 2407 provides a flexible interface to event managers A and B. The ADC interface is built around a fast, 10-bit ADC module with total conversion time of 500 ns (S/H + conversion). The ADC module has 16 channels, configurable as two independent 8-channel modules to service event managers A and B. The two independent 8-channel modules can be cascaded to form a 16-channel module. Although there are multiple input channels and two sequencers, there is only one converter in the ADC module.

Some main functions of the ADC module is listed as follows:

- 10-bit ADC core with built-in S/H.

- Fast conversion time (S/H + Conversion) of 500 ns.
- 16-channel, mixed inputs.
- Autosequencing capability provides up to 16 "auto conversions" in a single session. Each conversion can be programmed to select any 1 of 16 input channels.
- Sequencer can be operated as two independent 8-state sequencers or as one large 16-state sequencer (i.e., two cascaded 8-state sequencers).
- Sixteen result registers (individually addressable) to store conversion values.
- Input Analogue Voltage Reference: VREFLO and VREFHI.
- Multiple triggers as sources for the Start-Of-Conversion (SOC) sequence.

– S/W – software immediate start.
– EVA – Event manager A (multiple event sources within EVA).
– EVB – Event manager B (multiple event sources within EVB).

Fig. 7.17 shows the simplified functional block diagram of the 2407 ADC module. The two 8-channel modules have the capability to autosequence a series of conversions; each module has the choice of selecting any one of the respective eight channels available through an analogue mux. In the cascaded mode, the autosequencer functions as a single 16-channel sequencer. On each sequencer, once the conversion is complete, the selected channel value is stored in its respective RESULT register. Autosequencing allows the system to convert the same channel multiple times, allowing the user to perform oversampling algorithms. This gives increased resolution over traditional single-sampled conversion results.

Since ADC only has a resolution of 10 bits, while the registers of timer are 16 bits. Scaling has to be done for Result Registers ADCFIFOs before the values in them involve the calculation. This is realized by shifting the ADCFIFO register result to the right so that the Least Significant Bit (LSB), which resided at bit 6, now resides at bit 0. By shifting ADCFIFO, the maximum values go from FFC0h to 3FFh, and the minimum value (above 0) goes from 40h to 1h.

To obtain the specified accuracy of the ADC, proper board layout is very critical. To the best extent possible, traces leading to the ADCINn pins should not run in close proximity to the digital signal paths. This is to minimise switching noise on the digital lines from getting coupled to the ADC inputs. Furthermore, proper isolation techniques must be used to isolate the ADC module power pins (such as VCCA, VREFHI, and VSSA) from the digital supply.

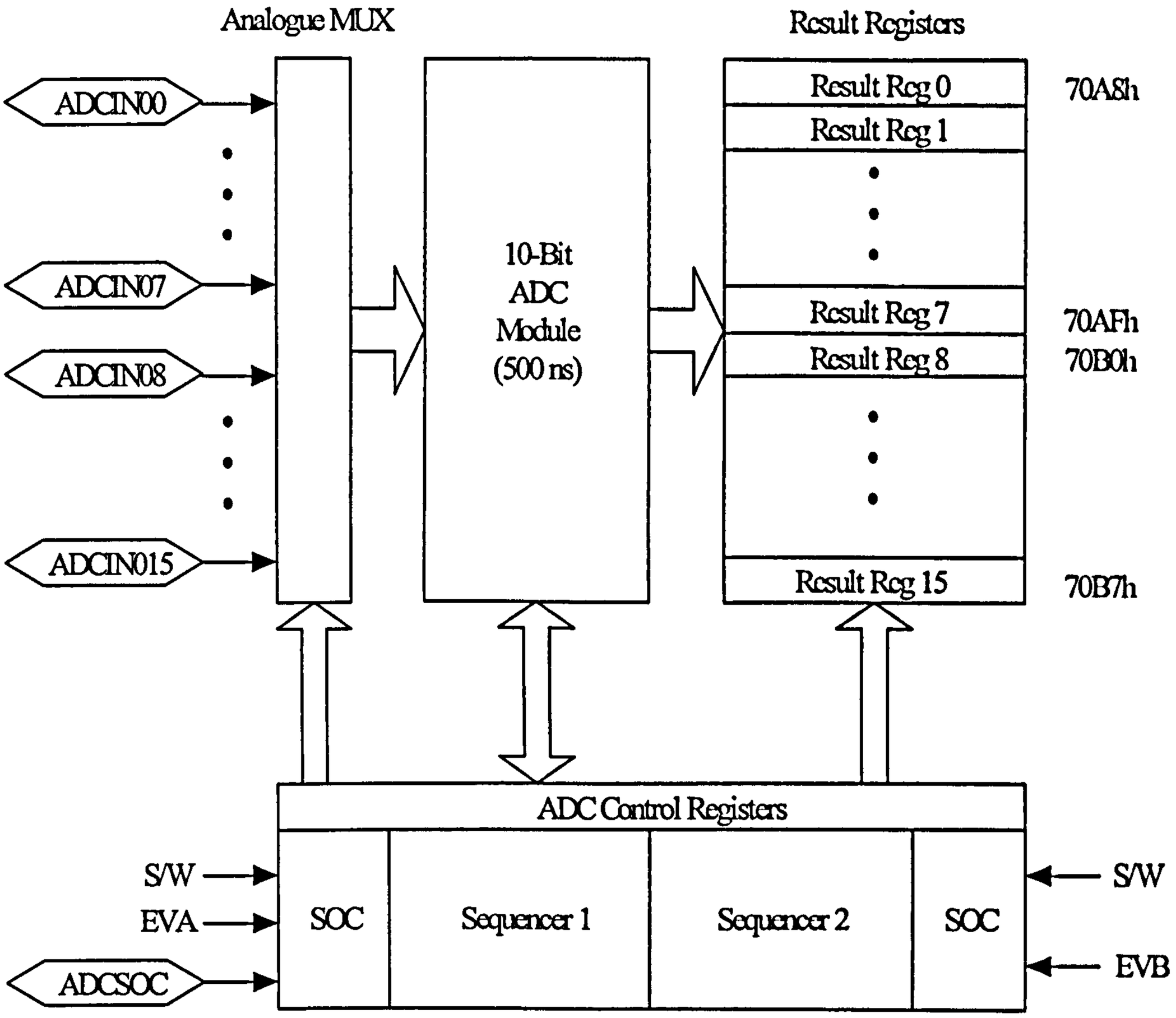


Fig. 7.17: Block Diagram of the 2407 ADC Module.

The PI Controller Implementation in the DSP

The PI regulator PI1, PI2 and PI3 are based on transform function $G_V(s)$:

$$G_V(s) = \frac{V_I(s)}{E_I(s)} = K_P + \frac{K_I}{s} \tag{7-15}$$

This is an analogue form and need to be transformed to the equivalent digital form before being implemented by the DSP controller. Using bilinear transformation, the PI regulator can be expressed as:

$$G_V(s) = \frac{V_I(s)}{E_I(s)} = \frac{K_0 + K_1 z^{-1}}{1 - z^{-1}} \tag{7-16}$$

Therefore the final form of the digital PI controller is:

$$V_I(n) = K_0 E_I(n) + K_1 E_I(n-1) + V_I(n-1) \tag{7-17}$$

where $$K_0 = K_P + \frac{K_I \cdot T_{samp}}{2} \tag{7-18}$$

$$K_1 = -K_P + \frac{K_I \cdot T_{samp}}{2} \tag{7-19}$$

T_{samp}= 1/1600=6.25x10^{-4} (s), T_{samp} is the sampling time, here equals to the carrier period T_s.

Voltage Balancing Control Algorithm

The principle of the voltage balancing control algorithm and its detailed implementation steps have been presented in Chapter 5. Now it should be mentioned that there are two important rules needed in the PWM adjustment.

(1) The adjusting time for any switching states should not exceed its maximum width.

(2) For every individual switching points, its new value after adjustment must not be greater than the value in the period register and not less than zero. Fig. 7.18 illustrates this rule.

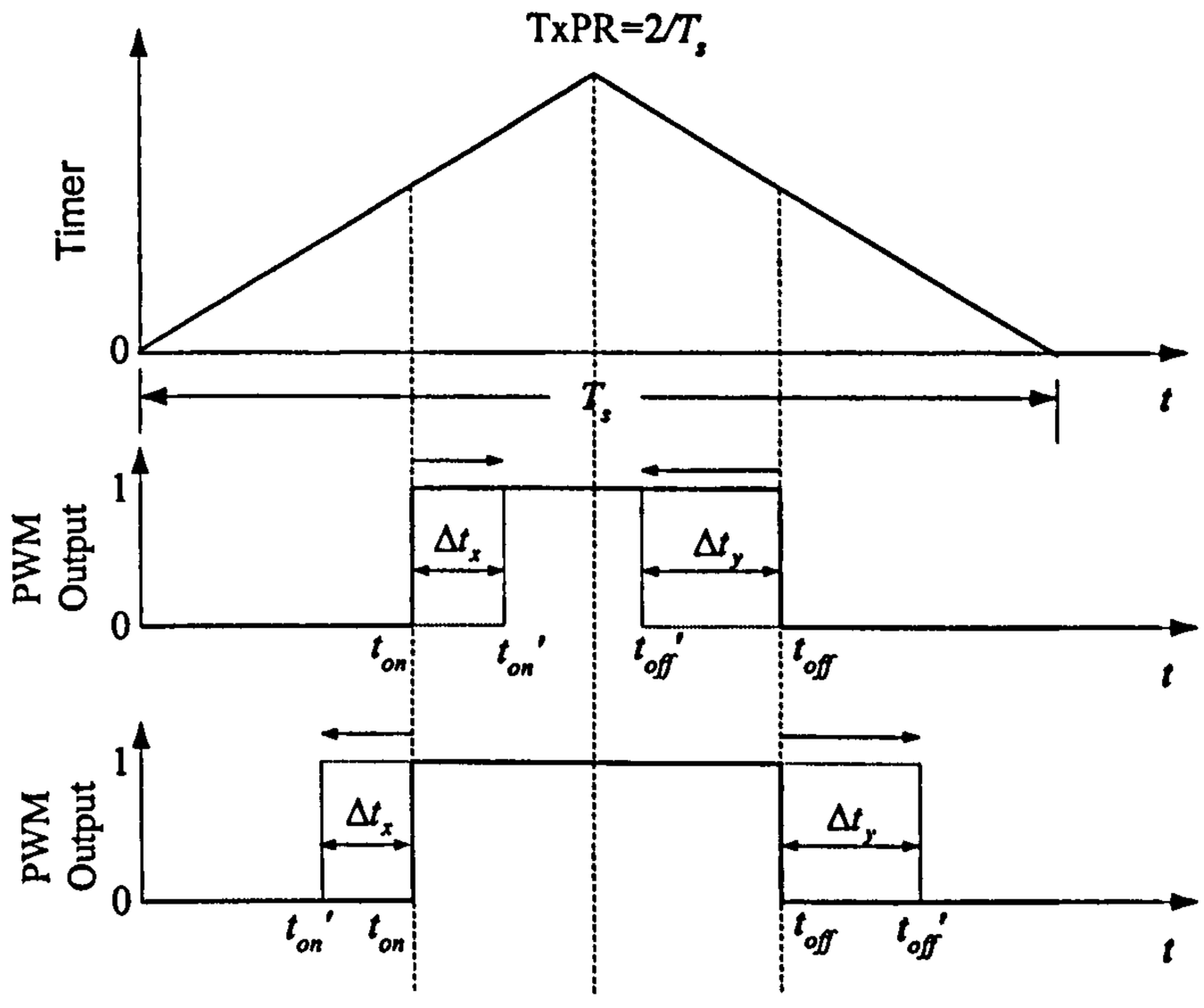


Fig. 7. 18: PWM adjustment limitation.

Here, t_{on}, t_{off} are original unadjusted values, Δt_x, Δt_y are adjusting times for t_{on} and t_{off} respectively. t_{on}', t_{off}' are new adjusted values. Δt_x, Δt_y are must satisfy the following conditions: (provided Δt_x, Δt_y are greater than zero.)

$$\begin{cases} \Delta t_x < \dfrac{T_s}{2} - t_{on} \text{ and } \Delta t_x < t_{on} \\ \Delta t_y < \dfrac{T_s}{2} - t_{off} \text{ and } \Delta t_y < t_{off} \end{cases} \tag{7-20}$$

PWM Generator

The DSP LS2407 has four GP Timers which are just used to generate four triangular carrier signals. In order to produce four carrier signals which are phase-shifted by 90 degrees, Timer 1 and Timer 2 are set to be synchronized to start with different counter start value. Similarly, Timer 3 and Timer 4 are also set to be synchronized to start with different counter start value. Timer 3 and Timer 4 begin to start only with $T_s/2$ delay after Timer 1 and Timer 2 start counting. For simplicity, the reference sine value is read from the look-up table. The comparison of carriers and reference signal generate four PWM signals which output to an interface board which provides complementary four signals for PWM inputs. These four complementary pairs of PWM signals are then carried to the two IGBT drive cards (SEMIKRON Semidriver SKHI61). The drive cards can generate all complementary signals with added interlock times of the lower switches and include the fast error shut down for all gate signals for power switches.

Software Organisation

Fig. 7.19 shows the interrupt structure on the controller for the single-phase five-level FC converter. Timers 1 to Timer 4 are used to generate four carriers. Two interrupts are used: Timer 2 Period Interrupt (T2PINT) and Timer 2 Underflow Interrupt (T2UFINT).

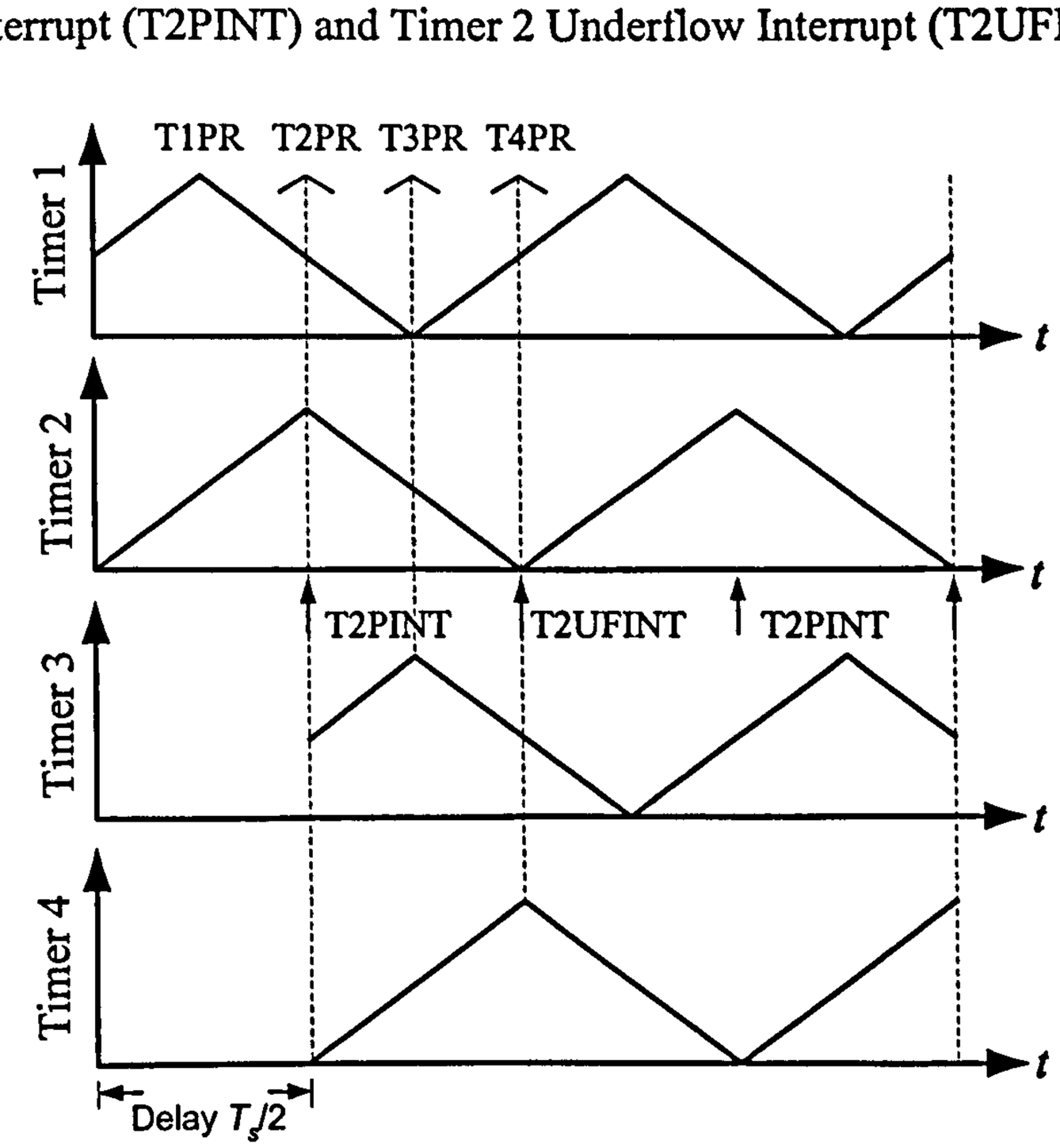


Fig. 7.19: Interrupt structure for the closed-loop control of the single-phase five-level FC converter.

Fig. 7.20 shows the flowchart for the main program. First, the program initialises the system and all the variables. As mentioned before, such initialisation includes system initialisation (i.e. CPU initialisation), event manager (EVA and EVB) setup, sine table setup, which is the same as the description in the main flowchart of the three-phase three-level FC converter shown in Fig. 7.10. Then it enables the desired interrupt, starts the timers, and loops in the background routine performing all the non-time critical functions. One of the CPU core interrupts INT3 stops execution of this background routine and the program branches to the interrupt service routine. The main program is interrupt driven. Once the proper registers have been set to create the PWM signal, the program can be ended (i.e., with an unconditional branch) and the PWM signal will continue to be output until the program stops the signal through software or the program is halted by the user.

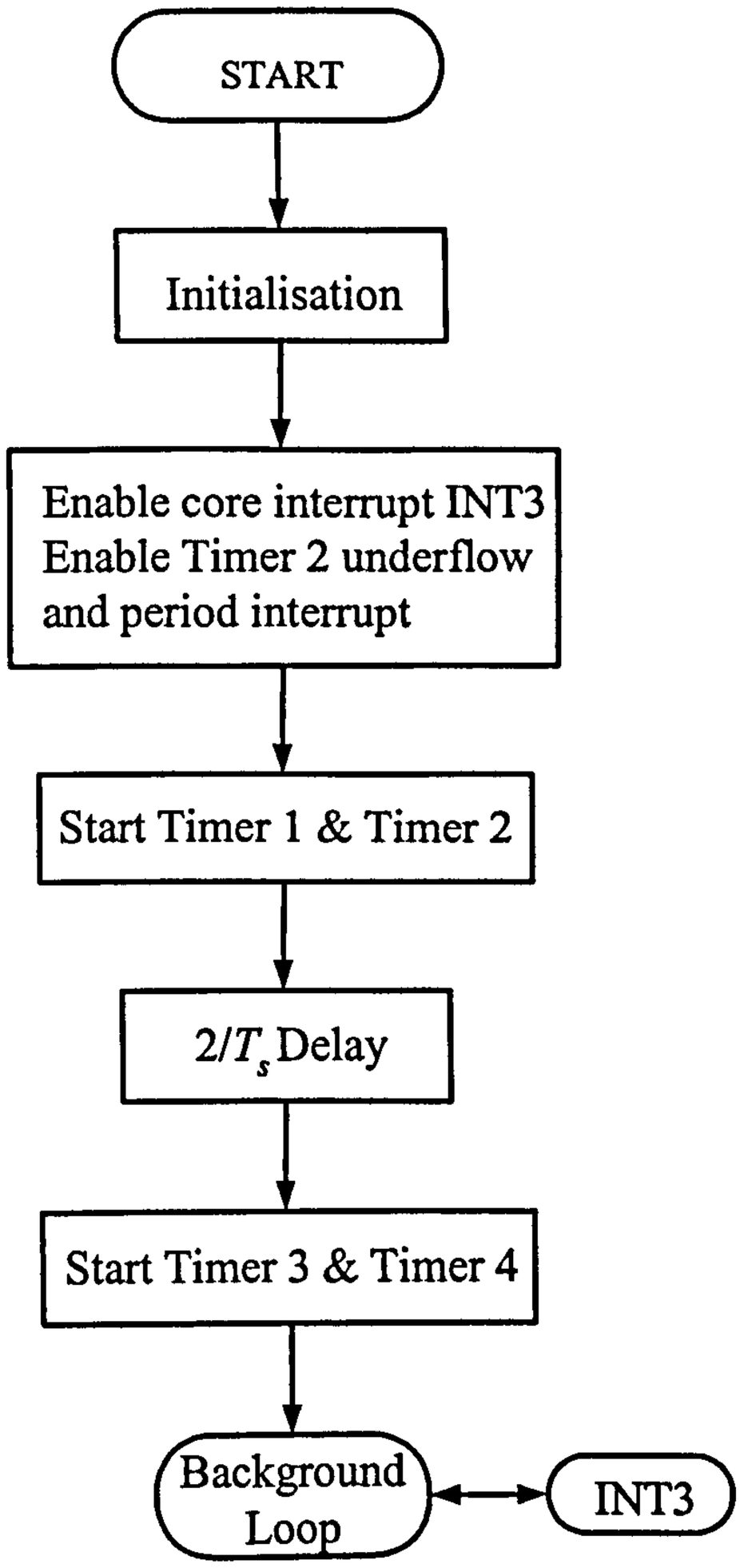


Fig. 7.20: Main program flowchart of the DSP controller for the single-phase five-level FC converter.

INT3 interrupt sources are Timer 2 underflow and period interrupt. As shown in Fig. 7.21, once this is determined, the program branches to the corresponding interrupt service routine.

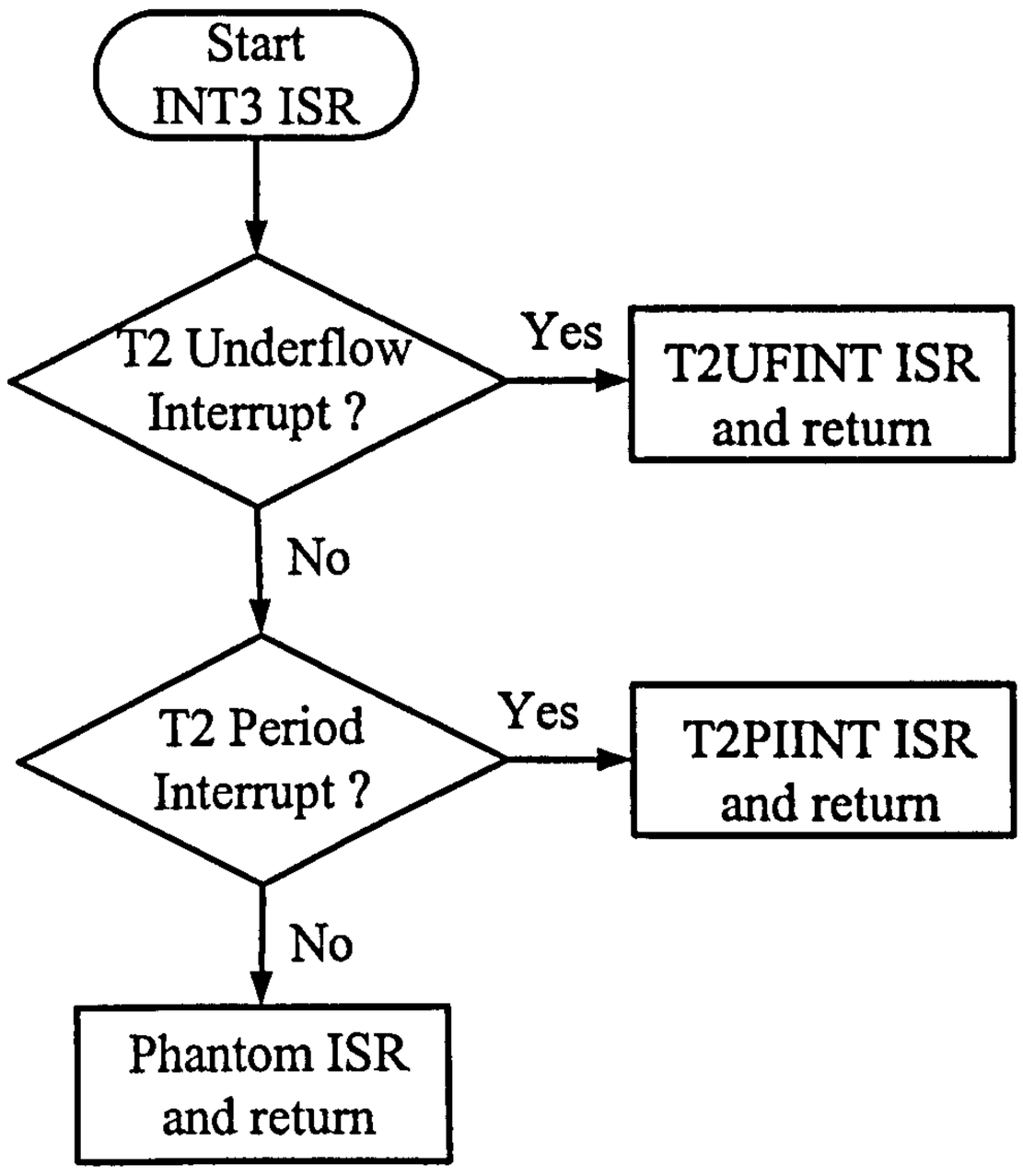


Fig. 7.21: INT3 interrupt dispatcher flowchart of the DSP controller for the single-phase five-level FC converter.

In the T2UFINT ISR shown in Fig. 7.22, the program mainly completes the calculation of the sine reference value, and then update the compare registers to make DSP automatically generate the PWM outputs. Firstly, the program reads the sine value from the look-up table, and then calculates the sine reference value by multiplying the sine value collected from the table by the amplitude modulation ratio m_a. Secondly, the program normalises the V_{ref} to guarantee the value to compare register being positive. Finally, the program updates the compare registers with the normalised $V_{ref}^{\cdot}$. This is the DSP-based open-loop controller without flying capacitors voltages control. If flying capacitors voltages control is wanted, the program call AD_Read subprogram in which V_{C1}, V_{C2}, V_{C3}, and i_o are read from ADCFIFO. Since AD conversion is set to start by Timer 2 underflow in the main program. When T2UFINT happens, AD conversion begins. In the AD_Read subprogram, every value is sampled four times and their average is taken as the final AD value to increase the accuracy of the measurement. Next, the error value E_V is calculated which is difference between the reference value and the value from AD module. Following that, executes PI_Controller and Voltage Balancing Controller subprogram to modify the PWM

switching points which are transformed to the corresponding sine reference values. After completing the calculation, the four values related with t_{1on}, t_{2on}, t_{3on} and t_{4on} are loaded to T1CMPR, T2CMPR, T3CMPR and T4CMPR respectively.

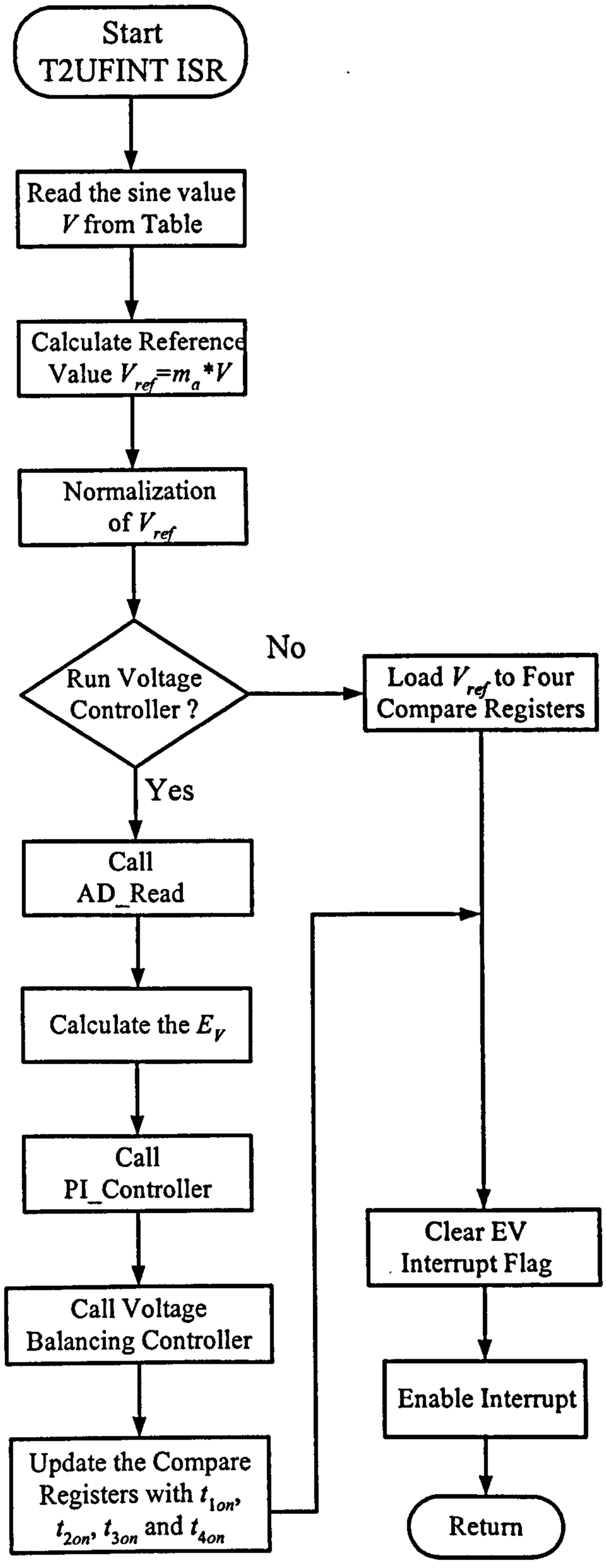


Fig. 7.22: T2UFINT ISR flowchart of the DSP controller for the single-phase five-level FC converter.

In the T2PINT ISR whose flowchart is demonstrated in Fig. 7.23, the program loads T1CMPR, T2CMPR, T3CMPR and T4CMPR with t_{1off}, t_{2off}, t_{3off} and t_{4off} respectively.

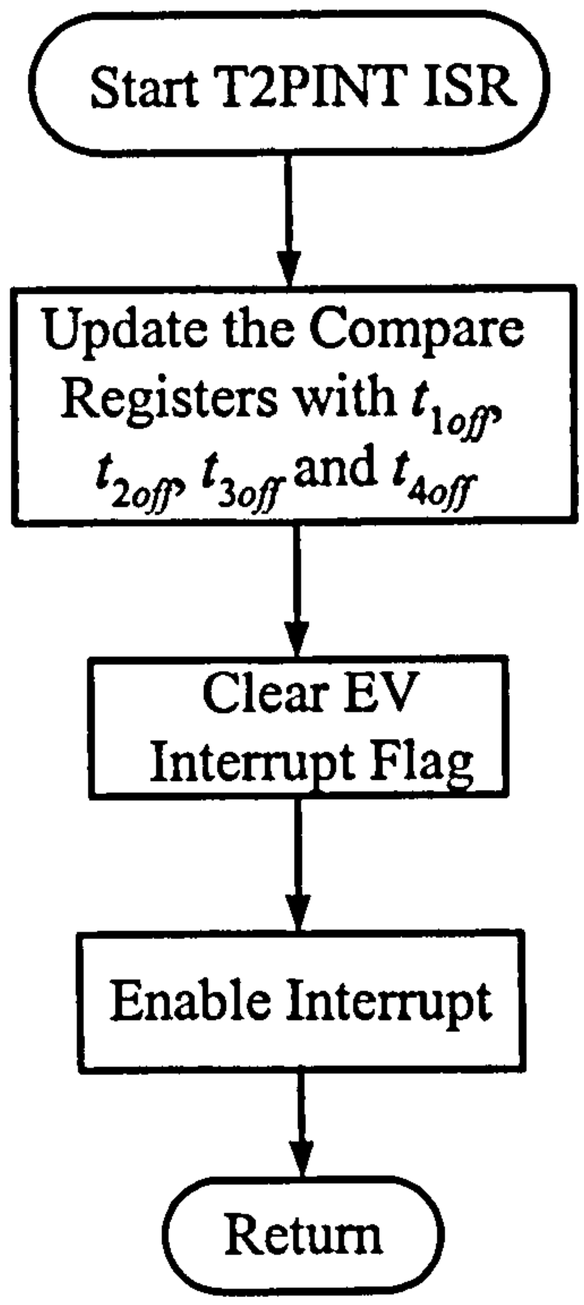


Fig. 7.23: T2PINT ISR flowchart of the DSP controller for the single-phase five-level FC converter.

7.6 Experimental Results

The experiments were carried out on the low-power three-level and five-level FC converter test circuits to evaluate the open-loop DSP controller. Fig. 7.24 shows the test circuit.

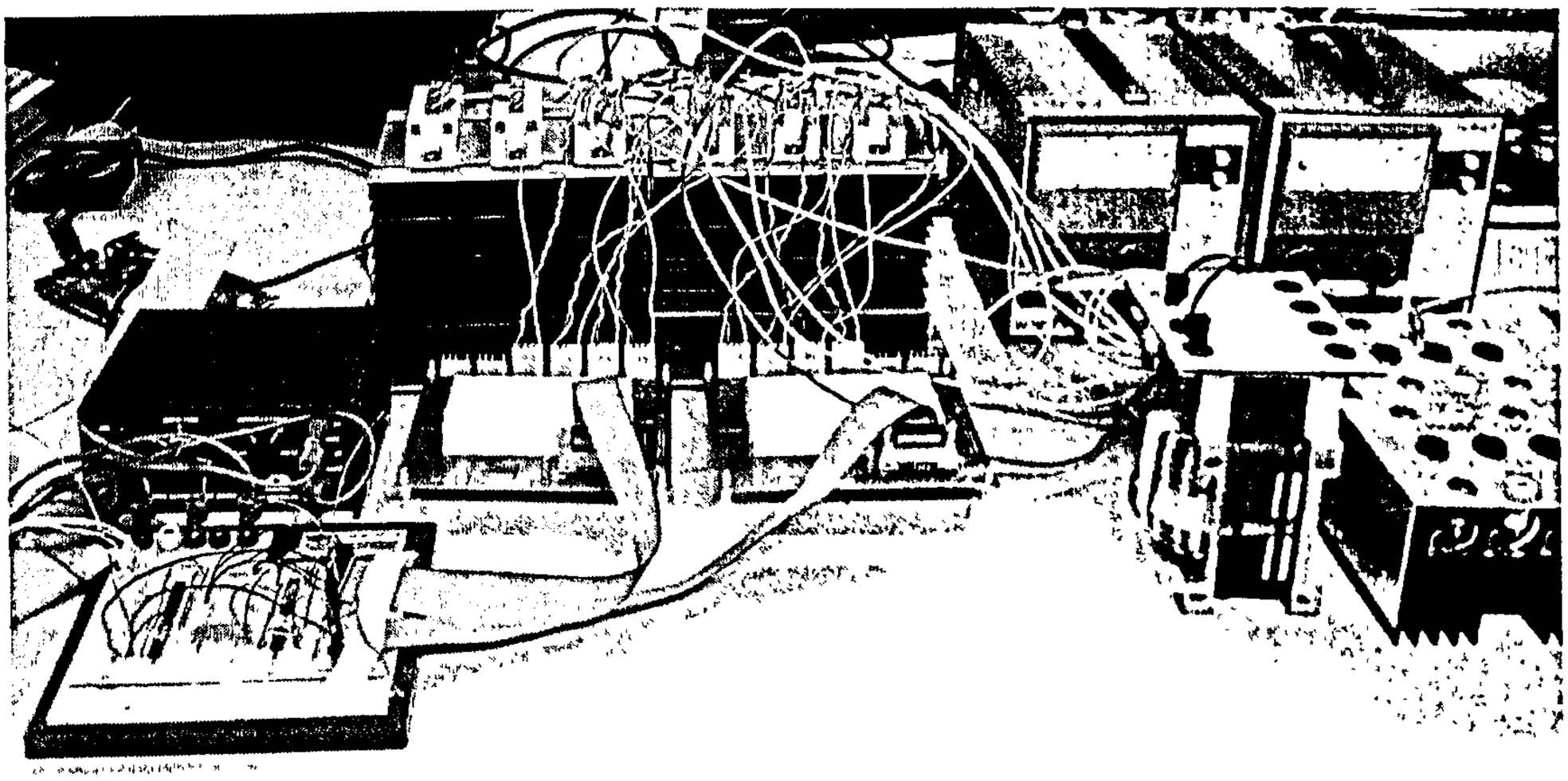


Fig. 7.24: The developed test circuit.

Fig. 7.25 and Fig. 7.26 show the PWM signal outputs taken from the DSP card. Fig. 7.25 illustrates the switching signals for S_{a1} and S_{a2} on the three-level FC converter. The switching signals for S_{a3} and S_{a4} are complementary to S_{a1} and S_{a2} respectively; therefore, their signals are not shown here. Fig. 7.26 illustrates a close view of switching signals for S_{a1}, S_{a2}, S_{a3} and S_{a4} on the five-level FC converter. The phase output voltage V_{AO} and phase output current i_o waveforms with pure resistive load and inductive load respectively on the three-level FC converter are shown in Fig. 7.27 and Fig. 7.28. Fig. 7.29 and Fig. 7.30 give the corresponding experimental results on the five-level FC converter.

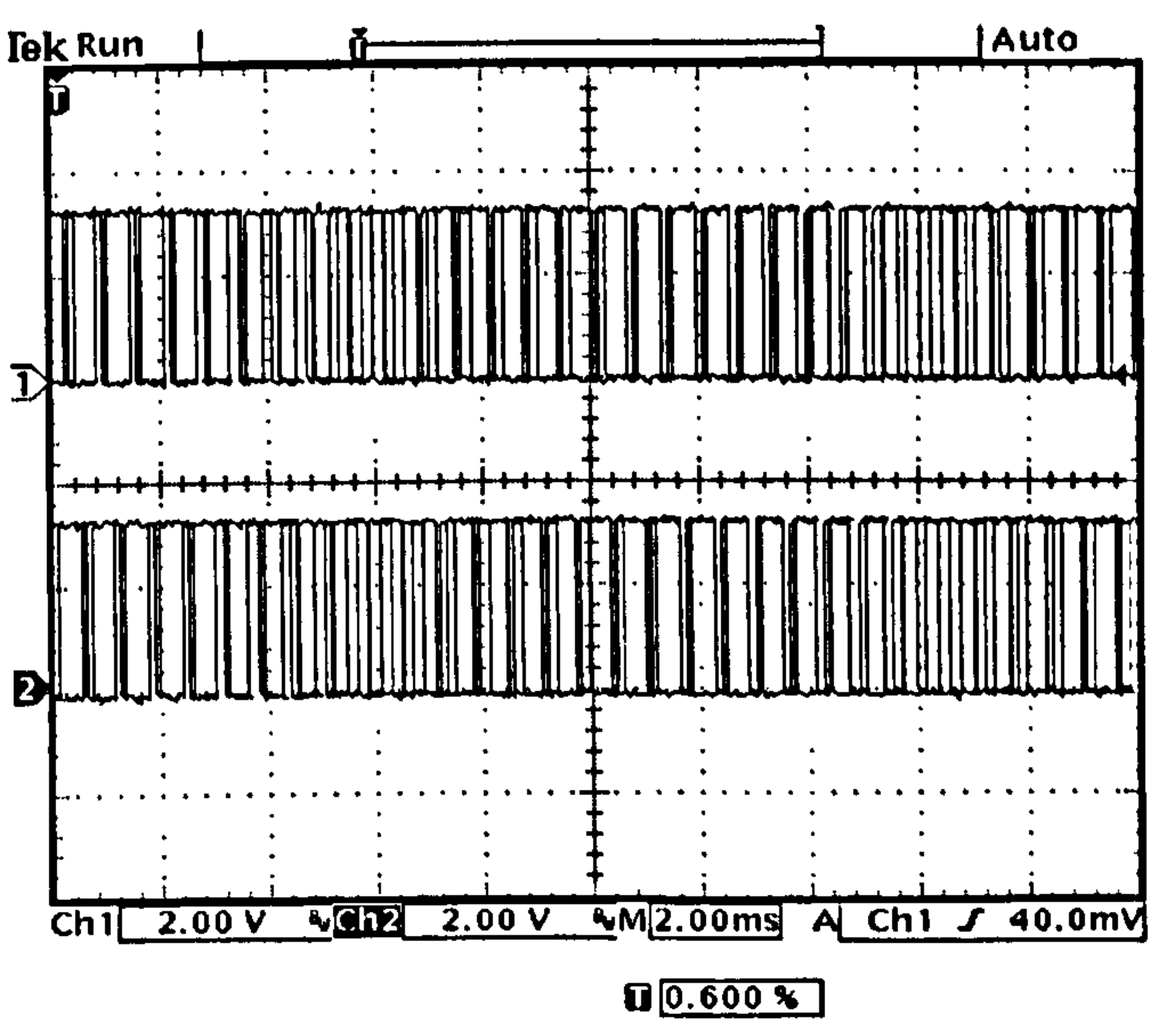


Fig. 7.25: PWM signal outputs for the three-level FC converter from the DSP (f_s=1.6 kHz, f_o=50 Hz, m_a=1.0). Ch1: Switching signal for S_{a1}; Ch2: Switching signal for S_{a2}.

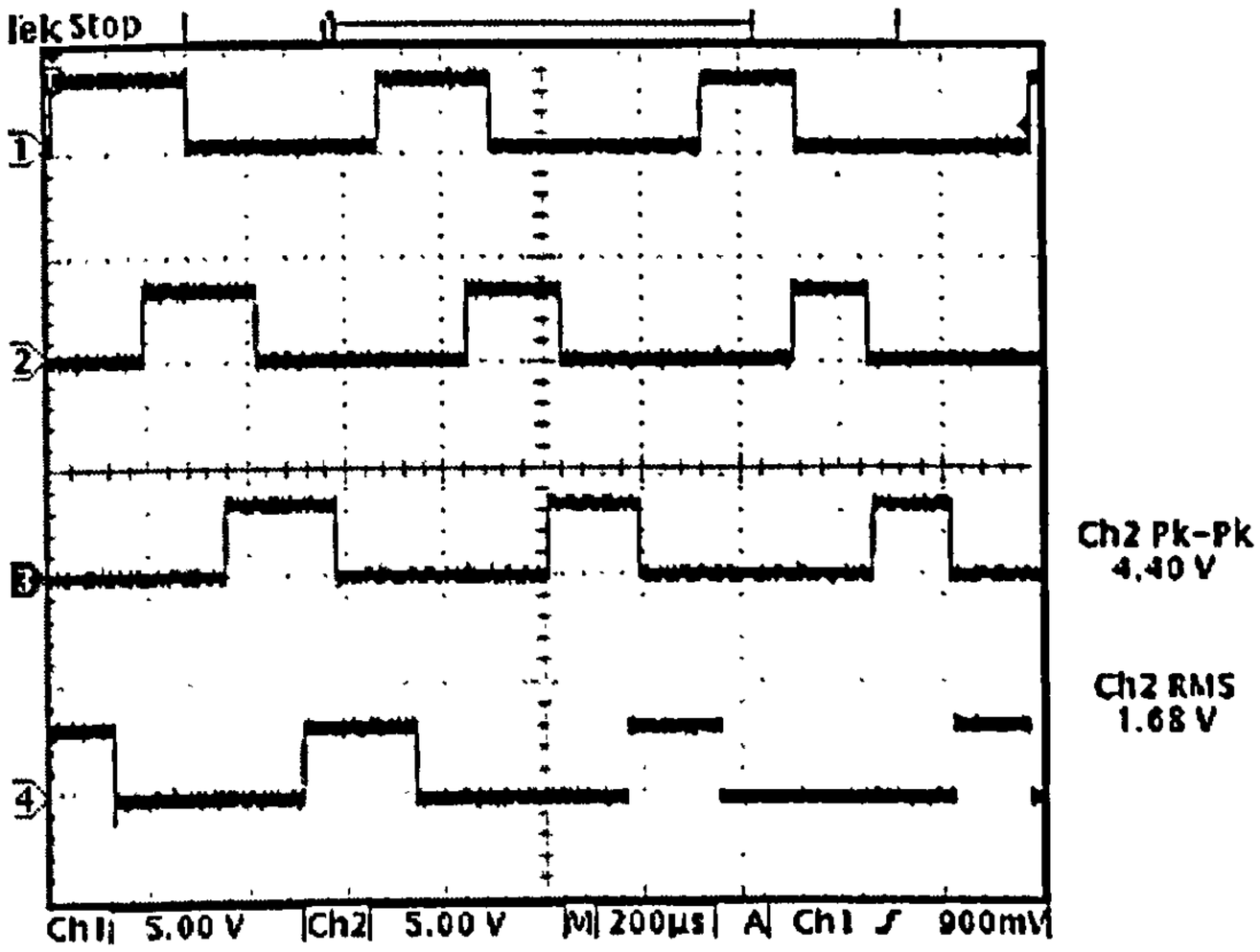


Fig. 7.26: PWM signal outputs for the five-level FC converter from the DSP (f_s=1.6 kHz, f_o=50 Hz, m_a=1.0). Ch1: Switching signal for S_{a1}; Ch2: Switching signal for S_{a2}; Ch3 Switching signal for S_{a3}; Ch4: Switching signal for S_{a4}.

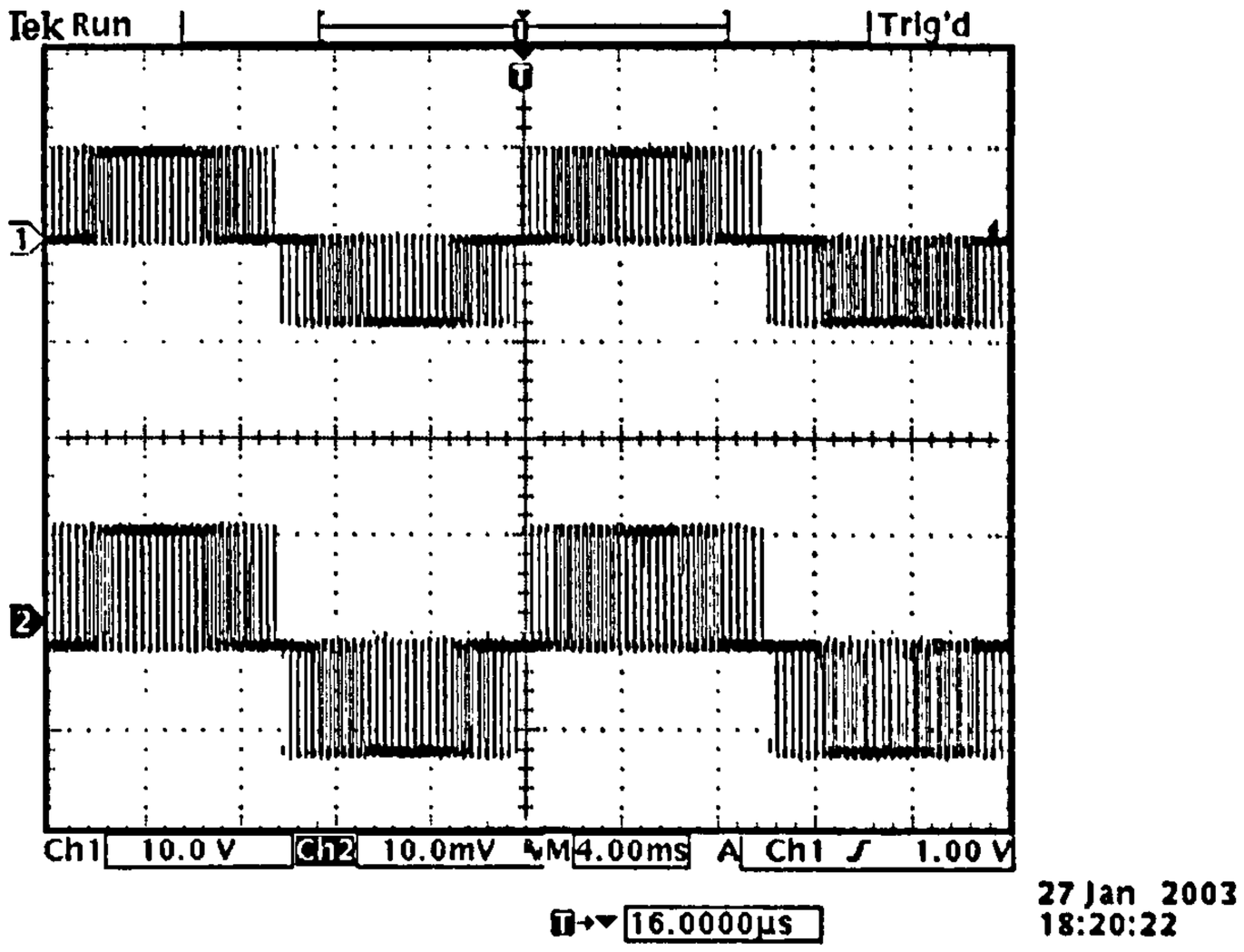


Fig. 7.27: Output waveforms of the three-level FC converter with the pure resistive load (f_s=1.6 kHz, f_o=50 Hz, m_a=1.0, V_{dc}=20 V, R=15 Ω). Ch1: Phase output voltage v_{AO}; Ch2: Phase output current i_o.

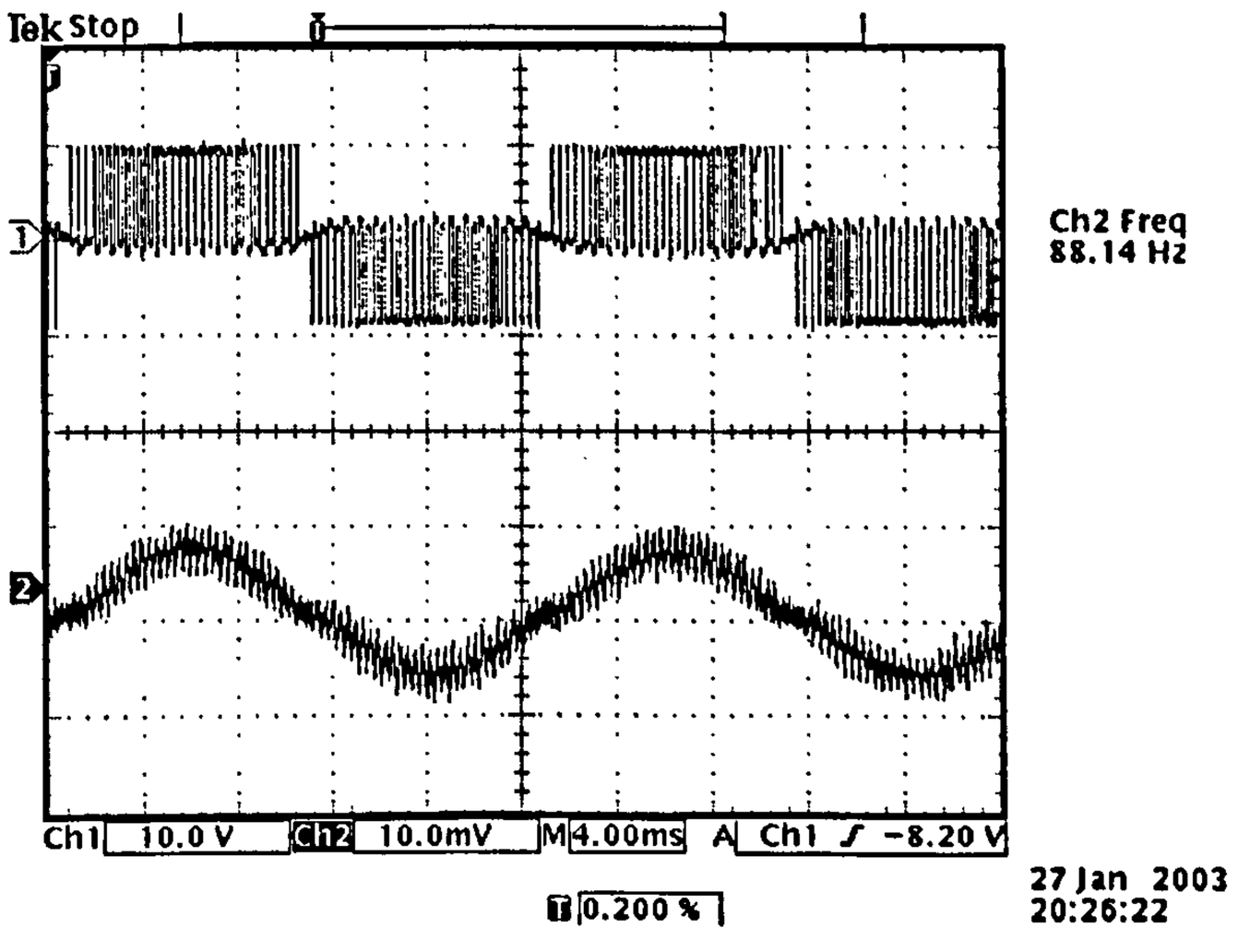


Fig. 7.28: Output waveforms of the three-level FC converter with the inductive load (f_s=1.6 kHz, f_o=50 Hz, m_a=1.0, V_{dc}=20 V, R=45 Ω, L=10 mH). Ch1: Phase output voltage v_{AO}; Ch2: Phase output current i_o.

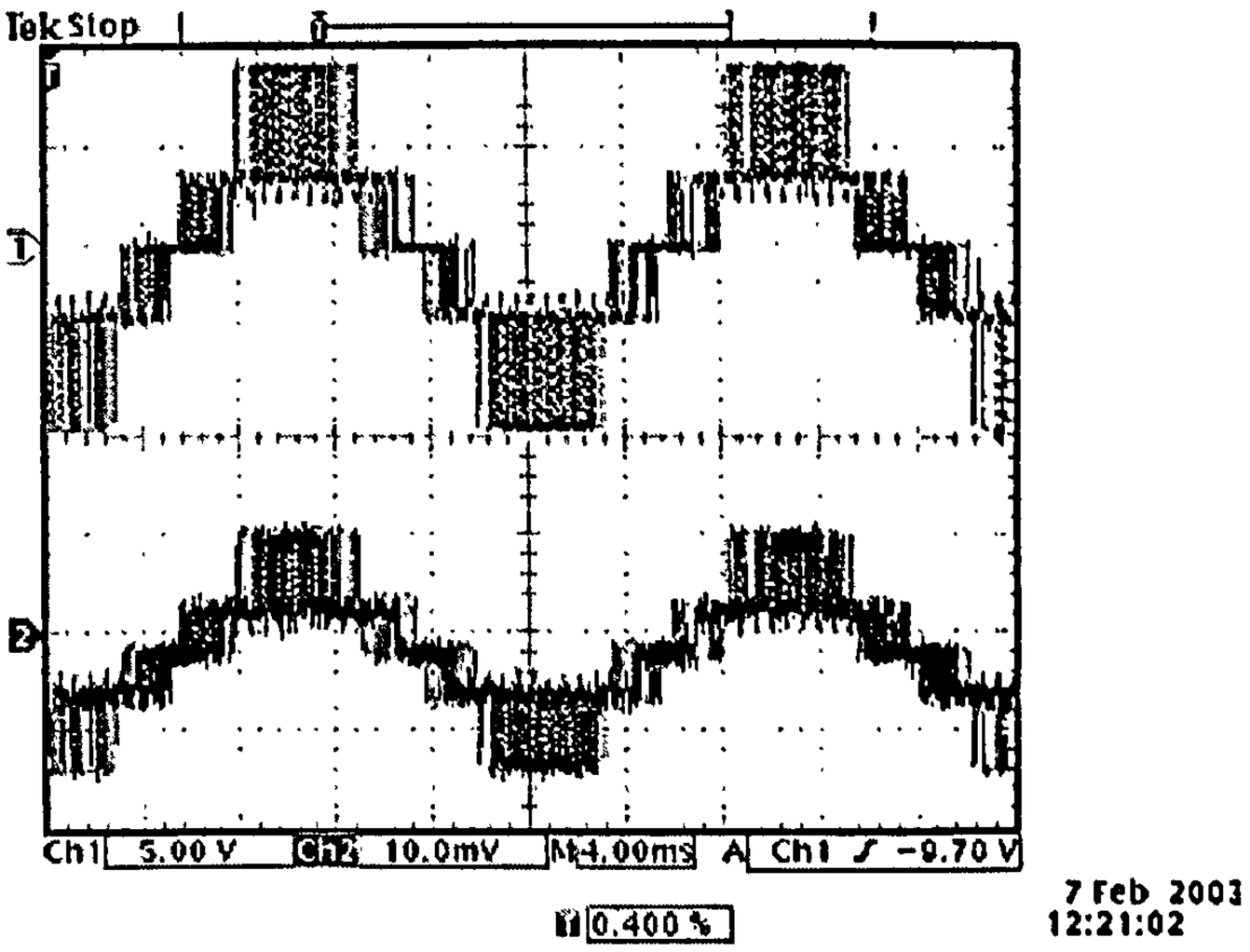


Fig. 7.29: Output waveforms of the five-level FC converter with the pure resistive load (f_s=1.6 kHz, f_o=50 Hz, m_a=1.0, V_{dc}=24 V, R=15 Ω). Ch1: Phase output voltage v_{AO}; Ch2: Phase output current i_o.

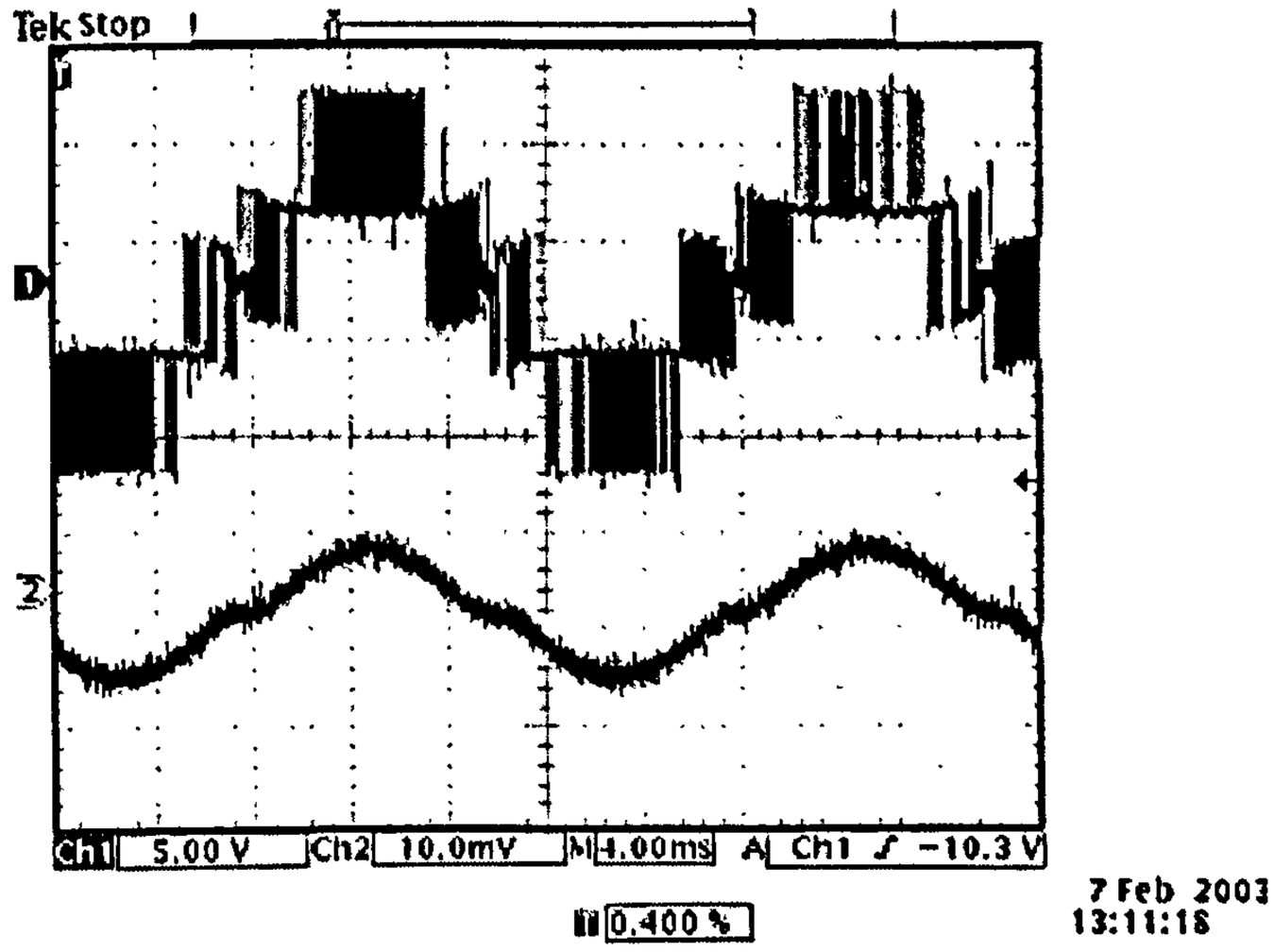


Fig. 7.30: Output waveforms of the five-level FC converter with the inductive load (f_s=1.6 kHz, f_o=50 Hz, m_a=1.0, V_{dc}=24 V, R=45 Ω, L=10 mH). Ch1: Phase output voltage v_{AO}; Ch2: Phase output current i_o.

It can be seen from Fig. 7.26 that the four switching signals for the five-level FC converter are phase shifted by $T_s/4$. Their switching frequencies are about 1.6 kHz. The phase output voltage v_{AO} of the three-level FC converter shown in Fig. 7.27 illustrates v_{AO} has three

voltage values. It varies between $+V_{dc}/2$ and 0 in the half modulating cycle and then varies between 0 and $-V_{dc}/2$ in the next half cycle. Fig. 7.29 shows that v_{AO} of the five-level FC converter has five voltage values. The Experimental results agree with the simulation results and verifies the validity of the designed open-loop DSP controllers for the three-level FC converter and the five-level FC converter.

7.7 Conclusions

This chapter has dealt with the development of the three-phase three-level FC capacitor converter prototype as well as the single-phase five-level one. The main components of the prototype are presented and discussed from the practical point of view. Different controllers are designed. An open-loop controller is designed for the three-phase three-level FC converter. A closed-loop controller is designed for the single-phase five-level FC converter. TMS320LF2407 DSP EVM is employed as the basis of the controllers. Its two general timers and two full compare units are used to generate the six complementary PWM outputs as gating signals for twelve power switches in the three-phase three-level FC converter. But one 2407 DSP EVM cannot meet the requirement of three-phase five-level FC converter. This is because the three-phase five-level FC converter needs twelve pairs of complementary PWM signals. However, the LF2407 DSP has only ten independent PWM channels out of sixteen PWM channels. So two DSP chips are needed for the three-phase five-level FC converter, one DSP chip can only satisfy a single-phase five-level FC converter since its four general timers can be used to generate four triangular waveforms phase-shifted by 90 degrees from each other. After comparing the sine value stored in the look-up table, the DSP generates four PWM signals as gating signals for the upper switches of a leg, their complementary PWM signals are generated through another interface board.

Chapter 8: Conclusions

8.1 Summary

Compared with conventional two-level converters, multilevel converters can synthesise high voltage levels with low harmonics without the use of transforms, thus being suitable for high voltage high power applications. Basically, there are three main types of multilevel converters, namely: cascaded converters with separate DC sources, NPC converters and FC converters. Each kind of converter has its own features, advantages and disadvantages as well as its range of application.

Switching strategies for multilevel converters were derived from PWM methods used in conventional two-level converters. The multi-carrier SPWM technique was employed here due to its ease of implementation. The various control methods have a different effect on the harmonic performance and switching losses of converters, thus suiting different multilevel topologies. CD-MSPWM strategies were widely used in the NPC converter. Among them, the PD method was superior to the APOD and the POD methods because it provided the lowest harmonic distortion for the line-to-line output voltage and had almost the same number of total switching transitions as others. The PS-MSPWM technique was suitable for FC converters. It was also suggested that the CD-MSPWM, a new SPWM method can also be suitable for the FC converters. However, CD-MSPWM methods cannot keep the voltage balancing of flying capacitors. In fact, it becomes impractical if no additional control circuitry is added to solve the voltage balancing problem. The PS-MSPWM and the new SPWM method both had self-balancing ability due to their switching redundancy. They can make conduction losses of the device equal and had good switch utilisation. Moreover, the new SPWM method generated a similar output voltage as that of the PS-MSPWM method with similar THD content but with a different harmonic spectrum. It had the same switching losses as that of the CD-MSPWM technique, one quarter of that of the PS-MSPWM. From the point of view of switching losses reduction and the self-balancing property, the new SPWM method is probably a good choice to control FC converters.

Since switching losses vary with switching frequency and switching times proportionally, in high frequency PWM, switching losses can be substantial, which is a big disadvantage. The FF-SPWM method was considered to minimise the switching losses.

The number of total switching transitions was used to indicate the potential switching losses. It is a function of m_a, m_f and φ. When m_a and φ were fixed, it is only determined by m_f, independently of the number of levels in the converter. In higher multilevel NPC inverters with higher m_a, the FF-SPWM control method is feasible.

An MPS-SPWM method was proposed as a solution to the problem of capacitor voltage unbalancing in five-level FC converters. The closed-loop method proposed consists of PI controllers and a voltage balancing algorithm to compensate the capacitor voltage deviation by adjusting switching time intervals of selected switching states. This MPS-SPWM technique can not only solve the capacitor voltage unbalancing problem existing in practical FC converters due to the non-ideal devices being used, but also improves the harmonic performance of FC converters.

The multi-modular system based on the FC converter had more control combinations than the NPC converter based system. No matter what kind of converter systems they are, for a higher m_f, no serious AC current sharing problem existed, therefore converters can be parallelled directly. The FF-SPWM or lower m_f was desirable for reducing the switching losses, but they also resulted in large circulating currents. When employing lower m_f, converters must be connected through transformers.

A three-phase three-level FC capacitor converter prototype as well as the single-phase five-level one was developed. Different controllers were designed: an open-loop controller for the three-phase three-level FC converter and a closed-loop controller for the single-phase five-level FC converter. The TMS320LF2407 DSP EVM was employed as a basis for the development of the controllers. The experimental results from low power test circuits verified the validity of the designed controllers.

8.2 Recommendations for Future Work

Based on the research work completed and reported in this thesis, the following possible areas for future investigations are suggested:

- Develop an inverter at a higher operating voltage and current.
- Test single-phase five-level FC converter with the MPS-SPWM method. Further work includes completing the DSP programming for the MPS-SPWM method and investigating its robustness by examining its performance under different loading conditions.

- Apply the multilevel converters to power systems and motor drives applications, such as active harmonic filters, distributed generation, and power quality.
- Investigate the harmonic elimination control method on high power converters to reduce switching losses and compare it with the FF-SPWM scheme.

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Appendix

A.1 DSP Program Code for the Three-Level FC Converter

```
;*****************************************************************************
; File Name:        Lab8.asm
; File Title:       DSP program for the open-loop control for the three-phase three-level FC
;                   converter
; Originator:       Chunmei Feng
; Target System: LF2407 Evaluation Board
; Description:      Pulse Width Modulator - Sets up the registers for a symmetric PWM output.
; The output is a square wave with a sine wave modulated duty cycle for six PWM pairs.
; Deadband of about 2us is set. PWM Period Ts is 625us => 1.6kHz, CPU clock is 30MHz
; (33.3ns). Frequency of the sinusoidal waveform is fo=50Hz (i.e.To=20ms), when
; frequency step is 2048 since fo =FREQSTEP/(Ts*2**16)
; Uesed Modules: EVMA: T1 Timer, PWM1,2--Sa1+,Sa1_
;                                 PWM3,4--Sb1+,Sb1_
;                                 PWM5,6--Sc1+,Sc1_
;                EVMB: T3 Timer, PWM7,8--Sa2+,Sa2_
;                                 PWM9,10--Sb2+,Sb2_
;                                 PWM11,12--Sc2+,Sc2_
;*****************************************************************************
                .include LF2407.h
;-----------------------------------------------------------------------------
; Vector address declarations
;-----------------------------------------------------------------------------
                        .sect   "vectors"
Reset           B START         ; Reset Vector
INT1            B PHANTOM ; Interrupt Level 1
INT2            B SINE          ; Interrupt Level 2
INT3            B PHANTOM ; Interrupt Level 3
INT4            B PHANTOM ; Interrupt Level 4
INT5            B PHANTOM ; Interrupt Level 5
INT6            B PHANTOM ; Interrupt Level 6
RESERVED        B PHANTOM ; Reserved
SW_INT8         B PHANTOM ; User S/W Interrupt
SW_INT9         B PHANTOM ; User S/W Interrupt
SW_INT10        B PHANTOM ; User S/W Interrupt
SW_INT11        B PHANTOM ; User S/W Interrupt
SW_INT12        B PHANTOM ; User S/W Interrupt
SW_INT13        B PHANTOM ; User S/W Interrupt
SW_INT14        B PHANTOM ; User S/W Interrupt
SW_INT15        B PHANTOM ; User S/W Interrupt
SW_INT16        B PHANTOM ; User S/W Interrupt
TRAP            B PHANTOM ; Trap vector
NMINT           B PHANTOM ; Non-maskable Interrupt
EMU_TRAP    B PHANTOM ; Emulator Trap
SW_INT20        B PHANTOM ; User S/W Interrupt
SW_INT21        B PHANTOM ; User S/W Interrupt
SW_INT22        B PHANTOM ; User S/W Interrupt
SW_INT23        B PHANTOM ; User S/W Interrupt
;-----------------------------------------------------------------------------
;       Address definitions
;-----------------------------------------------------------------------------
        .include LF2407.h
;-----------------------------------------------------------------------------
;       Constant definitions
```

```
;-----------------------------------------------------------------------------
        T1COMPARE  .set         0       ;T1Compare Initialised to 0
        pwm_half_per  .set 9384  ;T1Period/2 initialised to 18768/2,
        ; Ts=625us(1.6kHz signal) symmetric PWM with a 30MHz CPUCLK
*****************************************************************
;MAINROUTINE
*****************************************************************
        .text
START:  NOP
         SETC   INTM            ;Disable interrupts INTM
        SPLK    #0002H, IMR     ;Mask all core interrupts except INTM
        LACC    IFR             ;Read Interrupt flags
        SACL    IFR             ;Clear all interrupt flags
        CLRC    SXM             ;Clear Sign Extension Mode
        CLRC    OVM             ;Reset Overflow Mode
        CLRC    CNF             ;Config Block B0 to Data mem
;-----------------------------------------------------------------------------
;Configure the System Control and Status Registers
;-----------------------------------------------------------------------------
        LDP #00E0h ;set data page
        SPLK #0000000011111101b, SCSR1; =#00FDh
 * bit 15 0: reserved
* bit 14 0: CLKOUT = CPUCLK
* bit 13-12 00: IDLE1 selected for low-power mode
* bit 11-9 000: PLL x4 mode
* bit 8 0: reserved
* bit 7 1: 1 = enable ADC module clock
* bit 6 1: 1 = enable SCI module clock
* bit 5 1: 1 = enable SPI module clock
* bit 4 1: 1 = enable CAN module clock
* bit 3 1: 1 = enable EVB module clock
* bit 2 1: 1 = enable EVA module clock
* bit 1 0: reserved
* bit 0 1: clear the ILLADR bit

        LACC SCSR2 ;ACC = SCSR2 register
        OR #0000000000001011b ;OR in bits to be set (=#000Bh)
        AND #0000000000001111b ;AND out bits to be cleared (=#000Fh)
* bit 15-6          0's: reserved
* bit 5    0: do NOT clear the WD OVERRIDE bit
* bit 4    0: XMIF_HI-Z, 0=normal mode, 1=Hi-Z'd
* bit 3    1: disable the boot ROM, enable the FLASH
* bit 2    no change MP/MC* bit reflects the state of the MP/MC* pin
* bit 1-0           11: 11 = SARAM mapped to prog and data (default)

        SACL SCSR2      ;store to SCSR2 register
;-----------------------------------------------------------------------------
;Disable the watchdog timer
;-----------------------------------------------------------------------------
;       LDP #00E0h ;set data page
        SPLK #0000000011101000b, WDCR  ;=#00E8h
* bits 15-8         0's reserved
* bit 7    1: clear WD flag
* bit 6    1: disable the dog
* bit 5-3          101: must be written as 101
* bit 2-0          000: WDCLK divider = 1

        KICK_DOG                ;Reset Watchdog
;-----------------------------------------------------------------------------
;Setup shared I/O pins
```

```
;-----------------------------------------------------------------------------------------
        LDP #00E1h ;set data page
        SPLK #0000111111000000b,MCRA ;group A pins
* bit 15 0: 0=IOPB7, 1=TCLKINA
* bit 14 0: 0=IOPB6, 1=TDIRA
* bit 13 0: 0=IOPB5, 1=T2PWM/T2CMP
* bit 12 0: 0=IOPB4, 1=T1PWM/T1CMP
* bit 11 1: 0=IOPB3, 1=PWM6
* bit 10 1: 0=IOPB2, 1=PWM5
* bit 9  1: 0=IOPB1, 1=PWM4
* bit 8  1: 0=IOPB0, 1=PWM3
* bit 7  1: 0=IOPA7, 1=PWM2
* bit 6  1: 0=IOPA6, 1=PWM1
* bit 5  0: 0=IOPA5, 1=CAP3
* bit 4  0: 0=IOPA4, 1=CAP2/QEP2
* bit 3  0: 0=IOPA3, 1=CAP1/QEP1
* bit 2  0: 0=IOPA2, 1=XINT1
* bit 1  0: 0=IOPA1, 1=SCIRXD
* bit 0  0: 0=IOPA0, 1=SCITXD

        SPLK #1111111000000000b,MCRB ;group B pins (=#FE00h)
* bit 15  1: 0=reserved, 1=TMS2 (always write as 1)
* bit 14  1: 0=reserved, 1=TMS (always write as 1)
* bit 13  1: 0=reserved, 1=TD0 (always write as 1)
* bit 12  1: 0=reserved, 1=TDI (always write as 1)
* bit 11  1: 0=reserved, 1=TCK (always write as 1)
* bit 10  1: 0=reserved, 1=EMU1 (always write as 1)
* bit 9   1: 0=reserved, 1=EMU0 (always write as 1)
* bit 8   0: 0=IOPD0, 1=XINT2/ADCSOC
* bit 7   0: 0=IOPC7, 1=CANRX
* bit 6   0: 0=IOPC6, 1=CANTX
* bit 5   0: 0=IOPC5, 1=SPISTE
* bit 4   0: 0=IOPC4, 1=SPICLK
* bit 3   0: 0=IOPC3, 1=SPISOMI
* bit 2   0: 0=IOPC2, 1=SPISIMO
* bit 1   0: 0=IOPC1, 1=BIO*
* bit 0   0: 0=IOPC0, 1=W/R*

        SPLK #0000000001111111b,MCRC ;group C pins
* bit 15 0: reserved
* bit 14 0: 0=IOPF6, 1=IOPF6
* bit 13 0: 0=IOPF5, 1=TCLKINB
* bit 12 0: 0=IOPF4, 1=TDIRB
* bit 11 0: 0=IOPF3, 1=T4PWM/T4CMP
* bit 10 0: 0=IOPF2, 1=T3PWM/T3CMP
* bit 9 0: 0=IOPF1, 1=CAP6
* bit 8 0: 0=IOPF0, 1=CAP5/QEP4
* bit 7 0: 0=IOPE7, 1=CAP4/QEP3
* bit 6 0: 1=IOPE6, 1=PWM12
* bit 5 0: 1=IOPE5, 1=PWM11
* bit 4 0: 1=IOPE4, 1=PWM10
* bit 3 0: 1=IOPE3, 1=PWM9
* bit 2 0: 1=IOPE2, 1=PWM8
* bit 1 0: 1=IOPE1, 1=PWM7
* bit 0 0: 1=IOPE0, 1=CLKOUT
;-----------------------------------------------------------------------------------------
;Setup timers 1 and the PWM configuration
;-----------------------------------------------------------------------------------------
        LDP #00E8h ;set data page  (=232)
        SPLK #0000h, T1CON ;disable timer 1
```

```
        SPLK #0000h, T2CON ;disable timer 2
        SPLK #0000h, T3CON ;disable timer 3
        SPLK #0000h, T4CON ;disable timer 4
        SPLK #0000000000000000b, GPTCONA
* bit 15  0: reserved
* bit 14  0: T2STAT, read-only
* bit 13  0: T1STAT, read-only
* bit 12-11        00: reserved
* bit 10-9         00: T2TOADC, 00 = no timer2 event starts ADC
* bit 8-7          00: T1TOADC, 00 = no timer1 event starts ADC
* bit 6    0: TCOMPOE, 0 = Hi–z all timer compare outputs
* bit 5-4          00: reserved
* bit 3-2          00: T2PIN, 00 = forced low
* bit 1-0          00: T1PIN, 00 = forced low

;Timer 1: Configure to clock the PWM on PWM1 pin.
;Symmetric PWM, 20KHz carrier frequency, duty cycle is modulated by sine wave
        SPLK #pwm_half_per, T1PR        ;set timer period
        SPLK #0000h, T1CNT              ;clear timer counter
;       SPLK #0000h, DBTCONA                    ;deadband units off
        SPLK #T1COMPARE, CMPR1    ;Initialize CMPR1 for PWM1/PWM2
        SPLK #T1COMPARE, CMPR2    ;Initialize CMPR2 for PWM3/PWM4
        SPLK #T1COMPARE, CMPR3    ;Initialize CMPR3 for PWM5/PWM6
        SPLK #0000111111101000b, DBTCONA ;
* bit 15-12 0000: reserved
* bit 11-8          1111: DB Timer Period=15
* bit 7       1: EDBT3  0=disable; 1=enable
* bit 6       1: EDBT2  0=disable; 1=enable
* bit 5       1: EDBT1  0=disable; 1=enable
* bit 4-2     010: DB Timer Prescaler=32. 000=1;  001=2;  010=4;  011=8;
*                          100=16; 101=32; 110=32; 111=32
* bit 1-0           00: Reserved
* Dead time=DB Period*DB Prescaler*CPUCLK Period=15*4*33.3ns=1998ns=2us

        SPLK #0000011001100110b, ACTRA        ;(=#0444h)
* bit 15  0: space vector dir is CCW (don't care)
* bit 14-12         000: basic space vector is 000 (dont' care)
* bit 11-10 01: PWM6/IOPB3 pin active low. 00=forced low; 01=active low;
*           10=active high; 11=forced high
* bit 9-8           10: PWM5/IOPB2 pin active high
* bit 7-6           01: PWM4/IOPB1 pin active low
* bit 5-4           10: PWM3/IOPB0 pin active high
* bit 3-2           01: PWM2/IOPA7 pin active low
* bit 1-0           10: PWM1/IOPA6 pin active high

        SPLK #1000001000000000b, COMCONA  ;(=#8040h)
* bit 15     1: 1 = enable compare operation
* bit 14-13 00: 00 = reload CMPRx regs on timer 1 underflow
* bit 12     0: 0 = space vector disabled
* bit 11-10 00: 00 = reload ACTR on timer 1 underflow
* bit 9      1: 1 = enable PWM pins
* bit 8-0  0's: reserved

        SPLK #0000100000000000b, T1CON        ;(=0840h)
* bit 15-14 00: stop immediately on emulator suspend
* bit 13  0: reserved
* bit 12-11         01: 01 = continous-up/down count mode; 10=coutinous up mode
* bit 10-8          000: 000 = x/1 prescaler
* bit 7    0: reserved in T1CON
* bit 6    0: TENABLE, 1 = enable timer
```

```
* bit 5-4          00: 00 = CPUCLK is clock source
* bit 3-2          00: 00 = reload compare reg on underflow
* bit 1    0: 0 = disable timer compare
* bit 0    0: reserved in T1CON

;         LDP #00E8h
;         SPLK #0000100001000000b, T1CON  ;(=0840h)
* bit 15-14 00: stop immediately on emulator suspend
* bit 13  0: reserved
* bit 12-11        01: 01 = continous-up/down count mode; 10=coutinous up mode
* bit 10-8         000: 000 = x/1 prescaler
* bit 7    0: reserved in T1CON
* bit 6    1: TENABLE, 1 = enable timer
* bit 5-4          00: 00 = CPUCLK is clock source
* bit 3-2          00: 00 = reload compare reg on underflow
* bit 1    0: 0 = disable timer compare
* bit 0    0: reserved in T1CON

         LDP #00EAh
         SPLK #0000000000000000b, GPTCONB
* bit 15  0: reserved
* bit 14  0: T4STAT, read-only
* bit 13  0: T3STAT, read-only
* bit 12-11        00: reserved
* bit 10-9         00: T4TOADC, 00 = no timer4 event starts ADC
* bit 8-7          00: T3TOADC, 00 = no timer3 event starts ADC
* bit 6    0: TCOMPOE, 0 = Hi-z all timer compare outputs
* bit 5-4          00: reserved
* bit 3-2          00: T4PIN, 00 = forced low
* bit 1-0          00: T3PIN, 00 = forced low

         SPLK #pwm_half_per, T3PR ;set timer period
         SPLK #0000h, T3CNT ;clear timer 3 counter
         SPLK #9344, T3CNT   ;T/2-delay error=9384-40
;        SPLK #0000h, DBTCONB ;deadband units off
         SPLK #T1COMPARE, CMPR4 ;Initialize CMPR4 for PWM7/PWM8
         SPLK #T1COMPARE, CMPR5 ;Initialize CMPR5 for PWM9/PWM10
         SPLK #T1COMPARE, CMPR6 ;Initialize CMPR6 for PWM11/PWM12
         SPLK #0000111111101000b, DBTCONB ;
* bit 15-12 0000: reserved
* bit 11-8         1111: DB Timer Period=15
* bit 7       1: EDBT6  0=disable; 1=enable
* bit 6       1: EDBT5  0=disable; 1=enable
* bit 5       1: EDBT4  0=disable; 1=enable
* bit 4-2          010: DB Timer Prescaler=32. 000=1;  001=2;  010=4;  011=8;
*                       100=16; 101=32; 110=32; 111=32
* bit 1-0          00: Reserved
* Dead time=DB Period*DB Prescaler*CPUCLK Period=15*4*33.3ns=1998ns=2us

         SPLK #0000011001100110b, ACTRB ;(=#0444h)
* bit 15  0: space vector dir is CCW (don't care)
* bit 14-12        000: basic space vector is 000 (dont' care)
* bit 11-10 01: PWM12/IOPB3 pin active low. 00=forced low; 01=active low;
*          10=active high; 11=forced high
* bit 9-8          10: PWM11/IOPB2 pin active high
* bit 7-6          01: PWM10/IOPB1 pin active low
* bit 5-4          10: PWM9/IOPB0 pin active high
* bit 3-2          01: PWM8/IOPA7 pin active low
* bit 1-0          10: PWM7/IOPA6 pin active high
```

```
        SPLK #1000001000000000b, COMCONB ;(=#8040h)
* bit 15     1: 1 = enable compare operation
* bit 14-13 00: 00 = reload CMPRx regs on timer 1 underflow
* bit 12     0: 0 = space vector disabled
* bit 11-10 00: 00 = reload ACTR on timer 1 underflow
* bit 9      1: 1 = enable PWM pins
* bit 8-0  0's: reserved

;       SPLK #0000100001000000b, T3CON
* bit 15-14 00: stop immediately on emulator suspend
* bit 13  0: reserved
* bit 12-11        01: 01 = continous-up/down count mode; 10=coutinous up mode
* bit 10-8         000: 000 = x/1 prescaler
* bit 7    0: reserved in T3CON
* bit 6    1: TENABLE, 1 = enable timer
* bit 5-4          00: 00 = CPUCLK is clock source
* bit 3-2          00: 00 = reload compare reg on underflow
* bit 1    0: 0 = disable timer compare
* bit 0    0: reserved in T3CON

        SPLK #0000100000000000b, T3CON
* bit 15-14 00: stop immediately on emulator suspend
* bit 13  0: reserved
* bit 12-11        01: 01 = continous-up/down count mode; 10=coutinous up mode
* bit 10-8         000: 000 = x/1 prescaler
* bit 7    0: reserved in T3CON
* bit 6    0: TENABLE, 1 = enable timer
* bit 5-4          00: 00 = CPUCLK is clock source
* bit 3-2          00: 00 = reload compare reg on underflow
* bit 1    0: 0 = disable timer compare
* bit 0    0: reserved in T3CON
;-----------------------------------------------------------------------------
; Generate Sine Wave Modulated PWM
;-----------------------------------------------------------------------------
        .bss TABLEA,1           ;Keeps address of the pointer A in SINE Table
        .bss TABLEB,1           ;Keeps address of the pointer B in SINE Table
        .bss TABLEC,1           ;Keeps address of the pointer C in SINE Table
        .bss TOPTABLE,1             ;Keeps the reset value for the pointer
        .bss COMPARET1,1            ;A register to do calculations since the T1CMPR
                                    ;register is double buffered
        .bss FREQSTEP,1             ;Frequency modulation of the sine wave
        .bss MODREGA,1              ;Rolling Modulo Register
        .bss MODREGB,1              ;Rolling Modulo Register
        .bss MODREGC,1              ;Rolling Modulo Register
        .bss SINEVALA,1             ;Value for phase a from look up table
        .bss SINEVALB,1             ;Value for phase b from look up table
        .bss SINEVALC,1             ;Value for phase c from look up table
        .bss VALA,1
        .bss VALB,1
        .bss VALC,1

NORMAL  .set 4692               ; NORMAAL=T1PERIOD/4=18768/4

        .text
        LDP     #0                      ;DP = 0
        SPLK #0000h,TABLEA   ;Initialize Pointer to Top
        SPLK #STABLE,TOPTABLE ;Initialize TOPTABLEA to address of sine table
        SPLK #2048, FREQSTEP            ;Set the step size
        SPLK #0000h,MODREGA             ;Initialize the 16 bit counter register
;-----------------------------------------------------------------------------
```

```
; Setup the core interrupts
;-------------------------------------------------------------------------------
        LDP #0000h
        SPLK #0000h, IMR                ;Clear the IMR register
        SPLK #111111b, IFR              ;Clear any pending core interrupts
* bit 15-6          00: Reserved
* bit 5    1: Int6 write a 1 to clear the flag
* bit 4    1: int5
* bit 3    1: int4
* bit 2    1: int3
* bit 1    1: int2
* bit 0    1: int1

        SPLK #000010b, IMR              ;Enable desired core interrupt INT2
* bit 15-6          00: Reserved
* bit 5    0: Int6 0=disabled; 1=enabled
* bit 4    0: int5 disabled
* bit 3    0: int4 disabled
* bit 2    0: int3 disabled
* bit 1    1: int2 enabled
* bit 0    0: int1 disabled

;-------------------------------------------------------------------------------
;  Setup the event Manager interrupts
;-------------------------------------------------------------------------------
        LDP     #232                    ;DP=232 Data Page for the Event Manager
        SPLK #0FFFFh,EVAIFRA            ;Clear all EVA group A Interrupt
        SPLK #0FFFFh,EVAIFRB            ;Clear all EVA group B Interrupt
        SPLK #0FFFFh,EVAIFRC            ;Clear all EVA group C Interrupt
        SPLK #0000000010000000b, EVAIMRA    ;Enable Timer 1 Period Interrupt
* bit 15-11  00000: reserved
* bit 10  0: T1OFINT 1=enable; 0=disable
* bit 9    0: T1UFINT
* bit 8    0: T1CNT
* bit 7    1: T1PINT, enable GP timer 1 period interrupt
* bit 6    0: SCMP3INT
* bit 5     0: SCMP2INT
* bit 4    0: SCMP1INT
* bit 3     0: CMP3INT
* bit 2    0: CMP2INT
* bit 1    0: CMP1INT
* bit 0    0: PDPINT

        SPLK #0000000000000000h,EVAIMRB     ;Clear all EVA groupall B
* bit 15-8  00000000: reserved
* bit 7    0: T3OFINT 1=enale; 0=disable
* bit 6    0: T3UFINT
* bit 5    0: T3CNT
* bit 4    0: T3PINT
* bit 3    0: T2OFINT
* bit 2     0: T2UFINT
* bit 1    0: T2CINT
* bit 0     0: T2PINT

        SPLK #0000h,EVAIMRC  ;Clear all EVA groupall C for disable/enable
                                        ;various capture interrupts
;-------------------------------------------------------------------------------
; Eanble the Tiemr 1 and Timer 3
;-------------------------------------------------------------------------------
        LDP #00EAh
```

```
        SBIT1 T3CON,B6_MSK  ;Enable Timer 3 operation
        LDP #00E8h
        SBIT1 T1CON,B6_MSK  ;Enable Timer 1 operation
;-------------------------------------------------------------------------------
; Enable global interrupts
;-------------------------------------------------------------------------------
        CLRC INTM           ;Enable global interrupt (INTM is located in ST0 BIT 9)
;-------------------------------------------------------------------------------
; Main Loop
;-------------------------------------------------------------------------------
Loop:   NOP
        B Loop              ; Branch to loop
;-------------------------------------------------------------------------------
; Generate PWM Sine Wave ISR
;-------------------------------------------------------------------------------
        SINE    LDP #0      ; DP = 0
        LACC MODREGA        ; ACC = 16 bit Counter Register
        ADD FREQSTEP        ; ACC = Counter + Step
        SACL MODREGA        ; Counter assigned new value
        LACC MODREGA,8      ; ACC = Counter shifted to left by 8
        SACH TABLEA         ; TABLEA = upper byte of counter = pointer
        LACC TABLEA         ;Calculate the table pointer for phase b
        ADD #170
        SACL MODREGB
        SUB #256
        BLEZ A
        SACL MODREGB
A:      LACC MODREGB
        SACL TABLEB
        LACC TABLEA         ;Calculate the table pointer for phase c
        ADD #85
        SACL MODREGC
        SUB #256
        BLEZ B
        SACL MODREGC
B:      LACC MODREGC
        SACL TABLEC
;For Phase A
        LACC TABLEA         ; ACC = TABLEA = Pointer
        ADD TOPTABLE        ; Offset Addr from top of table
        TBLR SINEVALA       ; Read sine value and store to SINEVAL
;-------------------------------------------------------------------------------
;Normalization of the Sine value A to prevent the compare value from being negative
;-------------------------------------------------------------------------------
        LT SINEVALA         ; TREG = SINEVAL (Q15)
        MPY #NORMAL         ; PREG = TREG * NORMAL (Q30)
                            ; NORMAL = T/2
        PAC                 ; ACC = PREG (Q30)
        SACH COMPARET1,1    ; COMPARET1 = PREG (Q15)
        LACC COMPARET1      ; ACC = COMPARET1
        ADD #NORMAL         ; ACC = COMPARET1 + NORMAL
        SACL VALA

        LDP #232            ; DP = 232
        SACL CMPR1          ; CMPR1 = ACC = Normalize Sine value
        LDP #00EAh
        SACL CMPR4
;For Phase B
        LDP #0000h
```

```
        LACC TABLEB
        ADD TOPTABLE                ; Offset Addr from top of table
        TBLR SINEVALB               ; Read sine value and store to SINEVAL
;---------------------------------------------------------------------------------------
;Normalization of the Sine value B to prevent the compare value from being negative
;---------------------------------------------------------------------------------------

        LT  SINEVALB          ; TREG = SINEVAL (Q15)
        MPY #NORMAL                 ; PREG = TREG * NORMAL (Q30)
                                    ; NORMAL = T/2
        PAC                         ; ACC = PREG (Q30)
        SACH COMPARET1,1      ; COMPARET1 = PREG (Q15)
        LACC COMPARET1        ; ACC = COMPARET1
        ADD  #NORMAL                ; ACC = COMPARET1 + NORMAL
        SACL VALB
        LDP #00E8h                  ; DP = 232
        SACL CMPR2            ; CMPR2 = ACC = Normalize Sine value
        LDP #00EAh
        SACL CMPR5
;For Phase C
        LDP #0000h
        LACC TABLEC
        ADD TOPTABLE                ; Offset Addr from top of table
        TBLR SINEVALC               ; Read sine value and store to SINEVAL
;---------------------------------------------------------------------------------------
;Normalization of the Sine value C to prevent the compare value from being negative
;---------------------------------------------------------------------------------------

        LT  SINEVALC          ; TREG = SINEVAL (Q15)
        MPY #NORMAL                 ; PREG = TREG * NORMAL (Q30)
                                    ; NORMAL = T/2
        PAC                         ; ACC = PREG (Q30)
        SACH COMPARET1,1      ; COMPARET1 = PREG (Q15)
        LACC COMPARET1        ; ACC = COMPARET1
        ADD  #NORMAL                ; ACC = COMPARET1 + NORMAL
        SACL VALC
        LDP #00E8h                  ; DP = 232
        SACL CMPR3            ; CMPR3 = ACC = Normalize Sine value
        LDP #00EAh
        SACL CMPR6
;---------------------------------------------------------------------------------------
;Clear the interrupt flags of the Event Manager Module
;---------------------------------------------------------------------------------------
        LDP #00E8h
        LACC EVAIFRA                ; ACC = EVAIFRA
        SACL EVAIFRA          ; EVAIFRA = ACC; resets the interrupt flag
        CLRC INTM                   ; Enable core interrupts
        RET                         ; Return to end of program
;---------------------------------------------------------------------------------------
; I S R - PHANTOM
; Description: Dummy ISR, used to trap spurious interrupts.
;---------------------------------------------------------------------------------------
                PHANTOM     KICK_DOG    ;Resets WD counter
                B PHANTOM
```

A.2 DSP Program Code for the Five-Level FC Converter

```
;*****************************************************************
; File Name: Lab9.asm
; Originator: Chunmei  Feng
; Target System: LF2407 Evaluation Board
;
; Description: Pulse Width Modulator - Sets up the registers for an symmetric PWM ;output. The output is a square wave with a sine wave modulated duty cycle for  four PWM ;outputs. NO Deadband is set. PWM Period Ts is 625us => 1.6kHz, CPU clock is ;30MHz(33.3ns), Frequency of the sinesoidal waveform is fo=50Hz(i.e.To=20ms), when ;frequency step is 2048 since fo=FREQSTEP/(Ts*2**16)
;
; Uesed Modules:          EVMA: T1 Timer, T1PWM/T1CMP--Sa1+
;                                 T2 Timer, T2PWM/T2CMP--Sa2+
;                         EVMB: T3 Timer, T3PWM/T3CMP--Sa3+
;                                 T4 Timer, T4PWM/T4CMP--Sa4+
; T1 Timer and T2 Timer are set to be synchronized to start  T3 Timer and T4 Timer are set ; to be synchronized to start. After a half carrier period when T1 Timer and T2 Timer start, ; T3 Timer and T4 Timer begin to start, that is, in the Timer 2 period  interrupt ISR, start
; Timer 3 and Timer 4, and then disable T2PINT. In the T3PINT ISR, pick up the sine
; value from the look-up table.
;*****************************************************************
                .include LF2407.h
;-----------------------------------------------------------------------------
; Vector address declarations
;-----------------------------------------------------------------------------
                        .sect   "vectors"

Reset           B START         ; Reset Vector
INT1            B PHANTOM ; Interrupt Level 1
INT2            B SINE          ; Interrupt Level 2
INT3            B STARTT1       ; Interrupt Level 3
INT4            B PHANTOM ; Interrupt Level 4
INT5            B PHANTOM ; Interrupt Level 5
INT6            B PHANTOM ; Interrupt Level 6
RESERVED        B PHANTOM ; Reserved
SW_INT8         B PHANTOM ; User S/W Interrupt
SW_INT9         B PHANTOM ; User S/W Interrupt
SW_INT10        B PHANTOM ; User S/W Interrupt
SW_INT11        B PHANTOM ; User S/W Interrupt
SW_INT12        B PHANTOM ; User S/W Interrupt
SW_INT13        B PHANTOM ; User S/W Interrupt
SW_INT14        B PHANTOM ; User S/W Interrupt
SW_INT15        B PHANTOM ; User S/W Interrupt
SW_INT16        B PHANTOM ; User S/W Interrupt
TRAP            B PHANTOM ; Trap vector
NMINT           B PHANTOM ; Non-maskable Interrupt
EMU_TRAP    B PHANTOM ; Emulator Trap
SW_INT20        B PHANTOM ; User S/W Interrupt
SW_INT21        B PHANTOM ; User S/W Interrupt
SW_INT22        B PHANTOM ; User S/W Interrupt
SW_INT23        B PHANTOM ; User S/W Interrupt

;-----------------------------------------------------------------------------
;Address definitions
;-----------------------------------------------------------------------------
        .include LF2407.h
;-----------------------------------------------------------------------------
;Constant definitions
;-----------------------------------------------------------------------------
```

```
T1COMPARE       .set    0           ;T1Compare Initialized to 0
pwm_half_per    .set 9384;T1Period/2 initialized to 18768/2, Ts=625us
                                    ; (1.6kHz signal) symmetric PWM with a 30MHz CPUCLK

*************************************************************************
*MAINROUTINE*
*************************************************************************
                .text

START:  NOP
        SETC    INTM            ;Disable interrupts INTM
        SPLK    #0002H, IMR     ;Mask all core interrupts except INT2--it does not matter to
; set anything here since the new setting about IMR will be made later
        LACC    IFR             ;Read Interrupt flags
        SACL    IFR             ;Clear all interrupt flags
        CLRC    SXM             ;Clear Sign Extension Mode
        CLRC    OVM             ;Reset Overflow Mode
        CLRC    CNF             ;Config Block B0 to Data mem

;-----------------------------------------------------------------------------
;Configure the System Control and Status Registers
;-----------------------------------------------------------------------------
        LDP #00E0h ;set data page
        SPLK #0000000011111101b, SCSR1; =#00FDh
* bit 15 0: reserved
* bit 14 0: CLKOUT = CPUCLK
* bit 13-12 00: IDLE1 selected for low-power mode
* bit 11-9 000: PLL x4 mode
* bit 8 0: reserved
* bit 7 1: 1 = enable ADC module clock
* bit 6 1: 1 = enable SCI module clock
* bit 5 1: 1 = enable SPI module clock
* bit 4 1: 1 = enable CAN module clock
* bit 3 1: 1 = enable EVB module clock
* bit 2 1: 1 = enable EVA module clock
* bit 1 0: reserved
* bit 0 1: clear the ILLADR bit

        LACC SCSR2 ;ACC = SCSR2 register
        OR #0000000000001011b ;OR in bits to be set (=#000Bh)
        AND #0000000000001111b ;AND out bits to be cleared (=#000Fh)
* bit 15-6          0's: reserved
* bit 5   0: do NOT clear the WD OVERRIDE bit
* bit 4   0: XMIF_HI-Z, 0=normal mode, 1=Hi-Z'd
* bit 3   1: disable the boot ROM, enable the FLASH
* bit 2   no change MP/MC* bit reflects the state of the MP/MC* pin
* bit 1-0           11: 11 = SARAM mapped to prog and data (default)
        SACL SCSR2 ;store to SCSR2 register

;-----------------------------------------------------------------------------
;Disable the watchdog timer
;-----------------------------------------------------------------------------
;       LDP #00E0h              ;set data page
        SPLK #0000000011101000b, WDCR  ;=#00E8h
* bits 15-8        0's reserved
* bit 7   1: clear WD flag
* bit 6   1: disable the dog
* bit 5-3          101: must be written as 101
* bit 2-0          000: WDCLK divider = 1
```

```
        KICK_DOG                ;Reset Watchdog

;-----------------------------------------------------------------------------
;Setup shared I/O pins
;-----------------------------------------------------------------------------
        LDP #00E1h ;set data page
        SPLK #0011000000000000b,MCRA ;group A pins (=#3000h)
* bit 15 0: 0=IOPB7, 1=TCLKINA
* bit 14 0: 0=IOPB6, 1=TDIRA
* bit 13 1: 0=IOPB5, 1=T2PWM/T2CMP
* bit 12 1: 1=IOPB4, 1=T1PWM/T1CMP
* bit 11 0: 0=IOPB3, 1=PWM6
* bit 10 0: 0=IOPB2, 1=PWM5
* bit 9 0: 0=IOPB1, 1=PWM4
* bit 8 0: 0=IOPB0, 1=PWM3
* bit 7 0: 0=IOPA7, 1=PWM2
* bit 6 0: 0=IOPA6, 1=PWM1
* bit 5 0: 0=IOPA5, 1=CAP3
* bit 4 0: 0=IOPA4, 1=CAP2/QEP2
* bit 3 0: 0=IOPA3, 1=CAP1/QEP1
* bit 2 0: 0=IOPA2, 1=XINT1
* bit 1 0: 0=IOPA1, 1=SCIRXD
* bit 0 0: 0=IOPA0, 1=SCITXD

        SPLK #1111111000000000b,MCRB ;group B pins (=#FE00h)
* bit 15  1: 0=reserved, 1=TMS2 (always write as 1)
* bit 14  1: 0=reserved, 1=TMS (always write as 1)
* bit 13  1: 0=reserved, 1=TD0 (always write as 1)
* bit 12  1: 0=reserved, 1=TDI (always write as 1)
* bit 11  1: 0=reserved, 1=TCK (always write as 1)
* bit 10  1: 0=reserved, 1=EMU1 (always write as 1)
* bit 9   1: 0=reserved, 1=EMU0 (always write as 1)
* bit 8   0: 0=IOPD0, 1=XINT2/ADCSOC
* bit 7   0: 0=IOPC7, 1=CANRX
* bit 6   0: 0=IOPC6, 1=CANTX
* bit 5   0: 0=IOPC5, 1=SPISTE
* bit 4   0: 0=IOPC4, 1=SPICLK
* bit 3   0: 0=IOPC3, 1=SPISOMI
* bit 2   0: 0=IOPC2, 1=SPISIMO
* bit 1   0: 0=IOPC1, 1=BIO*
* bit 0   0: 0=IOPC0, 1=W/R*

        SPLK #0000110000000000b,MCRC ;group C pins
* bit 15 0: reserved
* bit 14 0: 0=IOPF6, 1=IOPF6
* bit 13 0: 0=IOPF5, 1=TCLKINB
* bit 12 0: 0=IOPF4, 1=TDIRB
* bit 11 1: 0=IOPF3, 1=T4PWM/T4CMP
* bit 10 1: 0=IOPF2, 1=T3PWM/T3CMP
* bit 9 0: 0=IOPF1, 1=CAP6
* bit 8 0: 0=IOPF0, 1=CAP5/QEP4
* bit 7 0: 0=IOPE7, 1=CAP4/QEP3
* bit 6 0: 0=IOPE6, 1=PWM12
* bit 5 0: 0=IOPE5, 1=PWM11
* bit 4 0: 0=IOPE4, 1=PWM10
* bit 3 0: 0=IOPE3, 1=PWM9
* bit 2 0: 0=IOPE2, 1=PWM8
* bit 1 0: 0=IOPE1, 1=PWM7
* bit 0 0: 0=IOPE0, 1=CLKOUT
```

```
;-----------------------------------------------------------------------------------------
;Setup timer 1 and Timer 2, Timer 3 and Timer 4 as well as the PWM configuration
;-----------------------------------------------------------------------------------------
        LDP #00E8h                          ;set data page  (=232)
        SPLK #0000h, T1CON      ;disable timer 1
        SPLK #0000h, T2CON      ;disable timer 2
        SPLK #0000000001001010b, GPTCONA    ;=#0045h
* bit 15  0: reserved
* bit 14  0: T2STAT, read-only
* bit 13  0: T1STAT, read-only
* bit 12-11          00: reserved
* bit 10-9           00: T2TOADC, 00 = no timer2 event starts ADC
* bit 8-7            00: T1TOADC, 00 = no timer1 event starts ADC
* bit 6    1: TCOMPOE, 0 = Hi-z all timer compare outputs
* bit 5-4            00: reserved
* bit 3-2            10: T2PIN, T2PWM/T2CMP Output Pin Conditioning,
*           00=forced low; 01=active low; 10=active high; 11=forced high
* bit 1-0            10: T1PIN, T1PWM/T1CMP Output Pin Conditioning,
*           00=forced low; 01=active low; 10=active high; 11=forced high

;Timer 1: Configure to clock the PWM on T1PWM/T1CMP pin.
;Symmetric PWM, 1.6KHz carrier frequency, duty cycle is modulated by sinewave

        SPLK #pwm_half_per, T1PR        ;set timer period
        SPLK #4692, T1CNT               ;since the carrier 1 produced by Timer 1 is ;Ts/4, ahead of
carrier 2 produced by Timer 2
        SPLK #T1COMPARE,T1CMPR  ;Initialize T1CMPR for T1PWM/T1CMP
        SPLK #0000100000000010b, T1CON          ;(=#1046h)
* bit 15-14 00: stop immediately on emulator suspend
* bit 13  0: reserved
* bit 12-11 01: 10 = continous-up count mode;01=continous-up/down mode
* bit 10-8           000: 000 = x/1 prescaler
* bit 7    0: reserved in T1CON
* bit 6    0: TENABLE, 0=disable timer; 1 = enable timer
* bit 5-4            00: 00 = CPUCLK is clock source
* bit 3-2            00: 01=reload compare reg when counter is 0 or equals period
;           register value; 00 = reload compare reg on underflow;
* bit 1    1: 1 = enable timer compare
* bit 0    0: reserved in T1CON

;Timer 2: Configure to clock the PWM on T2PWM/T2CMP pin.
;Symmetric PWM, 20KHz carrier frequency, duty cycle is modulated by sinewave
        SPLK #pwm_half_per, T2PR ;set timer period
        SPLK #0000h, T2CNT              ;clear timer counter
        SPLK #T1COMPARE,T2CMPR  ;Initialize T1CMPR for T1PWM/T1CMP
        SPLK #0000100010000010b, T2CON          ;(=#1046h)
* bit 15-14 00: stop immediately on emulator suspend
* bit 13  0: reserved
* bit 12-11 01: 00=stop/hold; 01=continous-up/down mode;
*           10 = continous-up count mode; 11=directional-up/down
* bit 10-8           000: 000 = x/1 prescaler
* bit 7    1: TSWT1,Start with Timer 1, 0=use own TENABLE; 1=use Timer 1 TENABLE
*           (bit reserved in T1CON)
* bit 6    0: TENABLE, 0=disable Timer; 1 = enable timer
* bit 5-4            00: 00 = CPUCLK is clock source
* bit 3-2            00: 01=reload compare reg when counter is 0 or equals period
;           register value; 00 = reload compare reg on underflow;
* bit 1    1: 1 = enable timer compare
* bit 0    0: SELTIPR, Period Register Select, 0=use own per. reg. ;
*           1=use Timer 1 per. reg.(bit reserved in T1CON)
```

```
;Set Timer 3 and Timer 4 for EVAB
        LDP #00EAh                          ;set data page
        SPLK #0000h, T3CON     ;disable timer 3
        SPLK #0000h, T4CON     ;disable timer 4
        SPLK #0000000001001010b, GPTCONB    ;=#0045h
* bit 15  0: reserved
* bit 14  0: T4STAT, read-only
* bit 13  0: T3STAT, read-only
* bit 12-11        00: reserved
* bit 10-9         00: T4TOADC, 00 = no timer4 event starts ADC
* bit 8-7          00: T3TOADC, 00 = no timer3 event starts ADC
* bit 6    1: TCOMPOE, 0 = Hi-z all timer compare outputs
* bit 5-4          00: reserved
* bit 3-2          10: T4PIN, T4PWM/T4CMP Output Pin Conditioning,
*          00=forced low; 01=active low; 10=active high; 11=forced high
* bit 1-0          10: T3PIN, T3PWM/T3CMP Output Pin Conditioning,
*          00=forced low; 01=active low; 10=active high; 11=forced high

;Timer 3: Configure to clock the PWM on T3PWM/T3CMP pin.
;Symmetric PWM, 1.6KHz carrier frequency, duty cycle is modulated by sinewave
        SPLK #pwm_half_per, T3PR        ;set timer period
        SPLK #4692, T3CNT               ;since the carrier 3 produced by Timer 3 is ;Ts/4,ahead of carrier
4 produced by Timer 4
        SPLK #T1COMPARE,T3CMPR    ;Initialize T3CMPR for T3PWM/T3CMP
        SPLK #0000100000000010b, T3CON        ;(=#1046h)
* bit 15-14 00: stop immediately on emulator suspend
* bit 13  0: reserved
* bit 12-11 01: 10 = continous-up count mode;01=continous-up/down mode
* bit 10-8         000: 000 = x/1 prescaler
* bit 7    0: reserved in T3CON
* bit 6    0: TENABLE, 0=disable Timer; 1 = enable timer
* bit 5-4          00: 00 = CPUCLK is clock source
* bit 3-2          00: 01=reload compare reg when counter is 0 or equals period
;          register value; 00 = reload compare reg on underflow;
* bit 1    1: 1 = enable timer compare
* bit 0    0: reserved in T3CON

;Timer 4: Configure to clock the PWM on T4PWM/T4CMP pin.
;Symmetric PWM, 1.6KHz carrier frequency, duty cycle is modulated by sinewave
        SPLK #pwm_half_per, T4PR        ;set timer period
        SPLK #0, T4CNT                          ;clear timer counter
        SPLK #T1COMPARE,T4CMPR    ;Initialize T4CMPR for T4PWM/T4CMP
        SPLK #0000100010000010b, T4CON;
* bit 15-14 00: stop immediately on emulator suspend
* bit 13  0: reserved
* bit 12-11 01: 00=stop/hold; 01=continous-up/down mode;
*          10 = continous-up count mode; 11=directional-up/down
* bit 10-8         000: 000 = x/1 prescaler
* bit 7    1: TSWT1,Start with Timer 3, 0=use own TENABLE; 1=use Timer 3 TENABLE
*          (bit reserved in T3CON)
* bit 6    0: TENABLE, 0=disable Timer; 1 = enable timer
* bit 5-4          00: 00 = CPUCLK is clock source
* bit 3-2          00: 01=reload compare reg when counter is 0 or equals period
;          register value; 00 = reload compare reg on underflow;
* bit 1    1: 1 = enable timer compare
* bit 0    0: SELTIPR, Period Register Select, 0=use own per. reg. ;
*          1=use Timer 3 per. reg.(bit reserved in T3CON)
;-------------------------------------------------------------------------------
; Generate Sine Wave Modulated PWM
```

```
;-------------------------------------------------------------------------------
        .bss TABLE,1            ;Keeps address of the pointer in SINE Table
        .bss TOPTABLE,1                 ;Keeps the reset value for the pointer
        .bss COMPARET1,1                ;A register to do calculations since the T1CMPR
                                        ;register is double buffered
        .bss FREQSTEP,1                 ;Frequency modulation of the sine wave
        .bss MODREG,1           ;Rolling Modulo Register
        .bss SINEVAL,1          ;Value from look up table

        NORMAL  .set 4692       ; NORMAAL=T1PERIOD/4=18768/4

        .text
        LDP     #0                      ;DP = 0
        SPLK #0000h,TABLE       ;Initialize Pointer to Top
        SPLK #STABLE,TOPTABLE           ;Initialize TOPTABLE to address of sine table
        SPLK #2048, FREQSTEP            ;Set the step size
        SPLK #0000h,MODREG  ;Initialize the 16 bit counter register

;-------------------------------------------------------------------------------
; Setup the core interrupts
;-------------------------------------------------------------------------------
        LDP #0000h
        SPLK #0000h, IMR                ;Clear the IMR register
        SPLK #111111b, IFR              ;Clear any pending core interrupts
* bit 15-6          00: Reserved
* bit 5    1: Int6 write a 1 to clear the flag
* bit 4    1: int5
* bit 3    1: int4
* bit 2    1: int3
* bit 1    1: int2
* bit 0    1: int1

        SPLK #000110b, IMR              ;Enable desired core interrupt INT2,INT3
* bit 15-6          00: Reserved
* bit 5    0: Int6 0=disabled; 1=enabled
* bit 4    0: int5 disabled
* bit 3    0: int4 disabled
* bit 2    1: int3 enabled
* bit 1    1: int2 enabled
* bit 0    0: int1 disabled

;-------------------------------------------------------------------------------
; Setup the event Manager interrupts
;-------------------------------------------------------------------------------
        LDP     #232                    ;DP=232 Data Page for the Event Manager
        SPLK #0FFFFh,EVAIFRA            ;Clear all EVA group A Interrupt
        SPLK #0FFFFh,EVAIFRB            ;Clear all EVA group B Interrupt
        SPLK #0FFFFh,EVAIFRC            ;Clear all EVA group C Interrupt
        SPLK #0000000000000000b, EVAIMRA
* bit 15-11  00000: reserved
* bit 10  0: T1OFINT 1=enable; 0=disable
* bit 9    0: T1UFINT
* bit 8    0: T1CNT
* bit 7    0: T1PINT, enable GP timer 1 period interrupt
* bit 6-4           000: reserved
* bit 3     0: CMP3INT
* bit 2    0: CMP2INT
* bit 1    0: CMP1INT
* bit 0    0: PDPINTA
```

```
        SPLK #0000000000000001b,EVAIMRB      ;Enable Timer 2 Period Interrupt
* bit 15-4  000000000000: reserved
* bit 3     0: T2OFINT
* bit 2     0: T2UFINT
* bit 1     0: T2CINT
* bit 0     1: T2PINT

        SPLK #0000h,EVAIMRC  ;Clear all EVA groupall C for disable/enable          ; various
capture interrupts
* bit 15-3 0000000000000: reserved
* bit 2     0: CAP3INT
* bit 1     0: CAP2INT
* bit 0     0: CAP1INT

        LDP #234
        SPLK #0FFFFh,EVBIFRA         ;Clear all EVB group A Interrupt
        SPLK #0FFFFh,EVBIFRB         ;Clear all EVB group B Interrupt
        SPLK #0FFFFh,EVBIFRC         ;Clear all EVB group C Interrupt
        SPLK #0000000010000000b, EVBIMRA  ;Enable Timer 3 Period Interrupt
* bit 15-11  00000: reserved
* bit 10  0: T3OFINT 1=enable; 0=disable
* bit 9     0: T3UFINT
* bit 8     0: T3CNT
* bit 7     1: T3PINT
* bit 6-4          000: reserved
* bit 3      0: CMP6INT
* bit 2     0: CMP5INT
* bit 1     0: CMP4INT
* bit 0     0: PDPINTB

        SPLK #0000000000000000b,EVBIMRB
* bit 15-4  000000000000: reserved
* bit 3     0: T4OFINT
* bit 2     0: T4UFINT
* bit 1     0: T4CINT
* bit 0     0: T4PINT

        SPLK #0000h,EVBIMRC  ;Clear all EVB groupall C for disable/enable
;               various capture interrupts
* bit 15-3 0000000000000: reserved
* bit 2     0: CAP6INT
* bit 1     0: CAP5INT
* bit 0     0: CAP4INT

;-------------------------------------------------------------------------------
; Eanble the Tiemr 1 and Timer 2
;-------------------------------------------------------------------------------
        LDP #00E8h
        SBIT1 T1CON,B6_MSK  ;Enable Timer 1 operation


;-------------------------------------------------------------------------------
; Enable global interrupts
;-------------------------------------------------------------------------------
        CLRC INTM                    ;Enable global interrupt (INTM is located in ST0 BIT 9)

;-------------------------------------------------------------------------------
; Main Loop
;-------------------------------------------------------------------------------
Loop:   NOP
```

```
        B Loop                  ;Branch to loop

;-----------------------------------------------------------------------------
; Enable the Timer 3 and Timer 4 ISR after the interrupt of T2PINT(INT3)
;-----------------------------------------------------------------------------
STARTT1: LDP #00EAh
        SBIT1 T3CON,B6_MSK  ;Enable Timer 3 operation
        LDP     #232                    ;DP=232 Data Page for the Event Manager
        SPLK #0FFFFh,EVAIFRB            ;Clear all EVA group A Interrupt flag
        SPLK #0000000000000000b,EVAIMRB     ;disable Timer 2 Period Interrupt
* bit 15-4  000000000000: reserved
* bit 3     0: T2OFINT
* bit 2     0: T2UFINT
* bit 1     0: T2CINT
* bit 0     0: T2PINT

        CLRC INTM               ; Enable core interrupts
        RET                     ; Return to end of program

;-----------------------------------------------------------------------------
; Generate PWM Sine Wave ISR
;-----------------------------------------------------------------------------
SINE    LDP #0                  ; DP = 0
        LACC MODREG                     ; ACC = 16 bit Counter Register
        ADD FREQSTEP                    ; ACC = Counter + Step
        SACL MODREG             ; Counter assigned new value
        LACC MODREG,8                   ; ACC = Counter shifted to left by 8
        SACH TABLE              ; TABLE = upper byte of counter = pointer
        LACC TABLE              ; ACC = TABLE = Pointer
        ADD TOPTABLE                    ; Offset Addr from top of table
        TBLR SINEVAL                    ; Read sine value and store to SINEVAL

;-----------------------------------------------------------------------------
;Normalization of the Sine value to prevent the compare value from being negative
;-----------------------------------------------------------------------------
        LT  SINEVAL                     ; TREG = SINEVAL (Q15)
        MPY #NORMAL                     ; PREG = TREG * NORMAL (Q30)
                                        ; NORMAL = T/2
        PAC                             ; ACC = PREG (Q30)
        SACH COMPARET1,1    ; COMPARET1 = PREG (Q15)
        LACC COMPARET1      ; ACC = COMPARET1
        ADD  #NORMAL                    ; ACC = COMPARET1 + NORMAL

        LDP #232                        ; DP = 232
        SACL T1CMPR             ; T1CMPR = ACC = Normalize Sine value
        SACL T2CMPR             ; T2CMPR = ACC = Normalize Sine value

        LDP #234                ; DP = 234
        SACL T3CMPR             ; T3CMPR = ACC = Normalize Sine value
        SACL T4CMPR             ; T4CMPR = ACC = Normalize Sine value

;Clear the interrupt flags of the Event Manager Module
        LDP #234                ; DP = 234
        LACC EVBIFRA                    ; ACC = EVBIFRA
        SACL EVBIFRA            ; EVBIFRA = ACC; resets the
        CLRC INTM                       ; Enable core interrupts
        RET                             ; Return to end of program

;-----------------------------------------------------------------------------
; Sine Look-Up Table
```

```
; Number of Entries          : 256
; Angle Range      : 360 deg
; Number format  : Q15 with range -1 < N < +1
;-------------------------------------------------------------------------------------------------
;SINVAL ; Index Angle Sin(Angle)
                    .data
STABLE              .word     0 ; 0 0 0.0000
                    .word 804 ; 1 1.41 0.0245
                    .word 1608 ; 2 2.81 0.0491
                    .word 2410 ; 3 4.22 0.0736
                    .word 3212 ; 4 5.63 0.0980
                    .word 4011 ; 5 7.03 0.1224
                    .word 4808 ; 6 8.44 0.1467
                    .word 5602 ; 7 9.84 0.1710
                    .word 6393 ; 8 11.25 0.1951
                    .word 7179 ; 9 12.66 0.2191
                    .word 7962 ; 10 14.06 0.2430
                    .word 8739 ; 11 15.47 0.2667
                    .word 9512 ; 12 16.88 0.2903
                    .word 10278 ; 13 18.28 0.3137
                    .word 11039 ; 14 19.69 0.3369
                    .word 11793 ; 15 21.09 0.3599
                    .word 12539 ; 16 22.50 0.3827
                    .word 13279 ; 17 23.91 0.4052
                    .word 14010 ; 18 25.31 0.4276
                    .word 14732 ; 19 26.72 0.4496
                    .word 15446 ; 20 28.13 0.4714
                    .word 16151 ; 21 29.53 0.4929
                    .word 16846 ; 22 30.94 0.5141
                    .word 17530 ; 23 32.34 0.5350
                    .word 18204 ; 24 33.75 0.5556
                    .word 18868 ; 25 35.16 0.5758
                    .word 19519 ; 26 36.56 0.5957
                    .word 20159 ; 27 37.97 0.6152
                    .word 20787 ; 28 39.38 0.6344
                    .word 21403 ; 29 40.78 0.6532
                    .word 22005 ; 30 42.19 0.6716
                    .word 22594 ; 31 43.59 0.6895
                    .word 23170 ; 32 45.00 0.7071
                    .word 23731 ; 33 46.41 0.7242
                    .word 24279 ; 34 47.81 0.7410
                    .word 24811 ; 35 49.22 0.7572
                    .word 25329 ; 36 50.63 0.7730
                    .word 25832 ; 37 52.03 0.7883
                    .word 26319 ; 38 53.44 0.8032
                    .word 26790 ; 39 54.84 0.8176
                    .word 27245 ; 40 56.25 0.8315
                    .word 27683 ; 41 57.66 0.8449
                    .word 28105 ; 42 59.06 0.8577
                    .word 28510 ; 43 60.47 0.8701
                    .word 28898 ; 44 61.88 0.8819
                    .word 29268 ; 45 63.28 0.8932
                    .word 29621 ; 46 64.69 0.9040
                    .word 29956 ; 47 66.09 0.9142
                    .word 30273 ; 48 67.50 0.9239
                    .word 30571 ; 49 68.91 0.9330
                    .word 30852 ; 50 70.31 0.9415
                    .word 31113 ; 51 71.72 0.9495
                    .word 31356 ; 52 73.13 0.9569
                    .word 31580 ; 53 74.53 0.9638
```

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.word 31785 ; 54 75.94 0.9700
.word 31971 ; 55 77.34 0.9757
.word 32137 ; 56 78.75 0.9808
.word 32285 ; 57 80.16 0.9853
.word 32412 ; 58 81.56 0.9892
.word 32521 ; 59 82.97 0.9925
.word 32609 ; 60 84.38 0.9952
.word 32678 ; 61 85.78 0.9973
.word 32728 ; 62 87.19 0.9988
.word 32757 ; 63 88.59 0.9997
.word 32767 ; 64 90.00 1.0000
.word 32757 ; 65 91.41 0.9997
.word 32728 ; 66 92.81 0.9988
.word 32678 ; 67 94.22 0.9973
.word 32609 ; 68 95.63 0.9952
.word 32521 ; 69 97.03 0.9925
.word 32412 ; 70 98.44 0.9892
.word 32285 ; 71 99.84 0.9853
.word 32137 ; 72 101.25 0.9808
.word 31971 ; 73 102.66 0.9757
.word 31785 ; 74 104.06 0.9700
.word 31580 ; 75 105.47 0.9638
.word 31356 ; 76 106.88 0.9569
.word 31113 ; 77 108.28 0.9495
.word 30852 ; 78 109.69 0.9415
.word 30571 ; 79 111.09 0.9330
.word 30273 ; 80 112.50 0.9239
.word 29956 ; 81 113.91 0.9142
.word 29621 ; 82 115.31 0.9040
.word 29268 ; 83 116.72 0.8932
.word 28898 ; 84 118.13 0.8819
.word 28510 ; 85 119.53 0.8701
.word 28105 ; 86 120.94 0.8577
.word 27683 ; 87 122.34 0.8449
.word 27245 ; 88 123.75 0.8315
.word 26790 ; 89 125.16 0.8176
.word 26319 ; 90 126.56 0.8032
.word 25832 ; 91 127.97 0.7883
.word 25329 ; 92 129.38 0.7730
.word 24811 ; 93 130.78 0.7572
.word 24279 ; 94 132.19 0.7410
.word 23731 ; 95 133.59 0.7242
.word 23170 ; 96 135.00 0.7071
.word 22594 ; 97 136.41 0.6895
.word 22005 ; 98 137.81 0.6716
.word 21403 ; 99 139.22 0.6532
.word 20787 ; 100 140.63 0.6344
.word 20159 ; 101 142.03 0.6152
.word 19519 ; 102 143.44 0.5957
.word 18868 ; 103 144.84 0.5758
.word 18204 ; 104 146.25 0.5556
.word 17530 ; 105 147.66 0.5350
.word 16846 ; 106 149.06 0.5141
.word 16151 ; 107 150.47 0.4929
.word 15446 ; 108 151.88 0.4714
.word 14732 ; 109 153.28 0.4496
.word 14010 ; 110 154.69 0.4276
.word 13279 ; 111 156.09 0.4052
.word 12539 ; 112 157.50 0.3827
.word 11793 ; 113 158.91 0.3599
```

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.word 11039 ; 114 160.31 0.3369
.word 10278 ; 115 161.72 0.3137
.word 9512 ; 116 163.13 0.2903
.word 8739 ; 117 164.53 0.2667
.word 7962 ; 118 165.94 0.2430
.word 7179 ; 119 167.34 0.2191
.word 6393 ; 120 168.75 0.1951
.word 5602 ; 121 170.16 0.1710
.word 4808 ; 122 171.56 0.1467
.word 4011 ; 123 172.97 0.1224
.word 3212 ; 124 174.38 0.0980
.word 2410 ; 125 175.78 0.0736
.word 1608 ; 126 177.19 0.0491
.word 804 ; 127 178.59 0.0245
.word 0 ; 128 180.00 0.0000
.word 64731 ; 129 181.41 -0.0245
.word 63927 ; 130 182.81 -0.0491
.word 63125 ; 131 184.22 -0.0736
.word 62323 ; 132 185.63 -0.0980
.word 61524 ; 133 187.03 -0.1224
.word 60727 ; 134 188.44 -0.1467
.word 59933 ; 135 189.84 -0.1710
.word 59142 ; 136 191.25 -0.1951
.word 58356 ; 137 192.66 -0.2191
.word 57573 ; 138 194.06 -0.2430
.word 56796 ; 139 195.47 -0.2667
.word 56023 ; 140 196.88 -0.2903
.word 55257 ; 141 198.28 -0.3137
.word 54496 ; 142 199.69 -0.3369
.word 53742 ; 143 201.09 -0.3599
.word 52996 ; 144 202.50 -0.3827
.word 52256 ; 145 203.91 -0.4052
.word 51525 ; 146 205.31 -0.4276
.word 50803 ; 147 206.72 -0.4496
.word 50089 ; 148 208.13 -0.4714
.word 49384 ; 149 209.53 -0.4929
.word 48689 ; 150 210.94 -0.5141
.word 48005 ; 151 212.34 -0.5350
.word 47331 ; 152 213.75 -0.5556
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.word 46016 ; 154 216.56 -0.5957
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.word 43530 ; 158 222.19 -0.6716
.word 42941 ; 159 223.59 -0.6895
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.word 38745 ; 167 234.84 -0.8176
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.word 37852 ; 169 237.66 -0.8449
.word 37430 ; 170 239.06 -0.8577
.word 37025 ; 171 240.47 -0.8701
.word 36637 ; 172 241.88 -0.8819
.word 36267 ; 173 243.28 -0.8932
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.word 35579 ; 175 246.09 -0.9142
.word 35262 ; 176 247.50 -0.9239
.word 34964 ; 177 248.91 -0.9330
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.word 34422 ; 179 251.72 -0.9495
.word 34179 ; 180 253.13 -0.9569
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.word 33750 ; 182 255.94 -0.9700
.word 33564 ; 183 257.34 -0.9757
.word 33398 ; 184 258.75 -0.9808
.word 33250 ; 185 260.16 -0.9853
.word 33123 ; 186 261.56 -0.9892
.word 33014 ; 187 262.97 -0.9925
.word 32926 ; 188 264.38 -0.9952
.word 32857 ; 189 265.78 -0.9973
.word 32807 ; 190 267.19 -0.9988
.word 32778 ; 191 268.59 -0.9997
.word 32768 ; 192 270.00 -1.0000
.word 32778 ; 193 271.41 -0.9997
.word 32807 ; 194 272.81 -0.9988
.word 32857 ; 195 274.22 -0.9973
.word 32926 ; 196 275.63 -0.9952
.word 33014 ; 197 277.03 -0.9925
.word 33123 ; 198 278.44 -0.9892
.word 33250 ; 199 279.84 -0.9853
.word 33398 ; 200 281.25 -0.9808
.word 33564 ; 201 282.66 -0.9757
.word 33750 ; 202 284.06 -0.9700
.word 33955 ; 203 285.47 -0.9638
.word 34179 ; 204 286.88 -0.9569
.word 34422 ; 205 288.28 -0.9495
.word 34683 ; 206 289.69 -0.9415
.word 34964 ; 207 291.09 -0.9330
.word 35262 ; 208 292.50 -0.9239
.word 35579 ; 209 293.91 -0.9142
.word 35914 ; 210 295.31 -0.9040
.word 36267 ; 211 296.72 -0.8932
.word 36637 ; 212 298.13 -0.8819
.word 37025 ; 213 299.53 -0.8701
.word 37430 ; 214 300.94 -0.8577
.word 37852 ; 215 302.34 -0.8449
.word 38290 ; 216 303.75 -0.8315
.word 38745 ; 217 305.16 -0.8176
.word 39216 ; 218 306.56 -0.8032
.word 39703 ; 219 307.97 -0.7883
.word 40206 ; 220 309.38 -0.7730
.word 40724 ; 221 310.78 -0.7572
.word 41256 ; 222 312.19 -0.7410
.word 41804 ; 223 313.59 -0.7242
.word 42365 ; 224 315.00 -0.7071
.word 42941 ; 225 316.41 -0.6895
.word 43530 ; 226 317.81 -0.6716
.word 44132 ; 227 319.22 -0.6532
.word 44748 ; 228 320.63 -0.6344
.word 45376 ; 229 322.03 -0.6152
.word 46016 ; 230 323.44 -0.5957
.word 46667 ; 231 324.84 -0.5758
.word 47331 ; 232 326.25 -0.5556
.word 48005 ; 233 327.66 -0.5350
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.word 48689 ; 234 329.06 -0.5141
.word 49384 ; 235 330.47 -0.4929
.word 50089 ; 236 331.88 -0.4714
.word 50803 ; 237 333.28 -0.4496
.word 51525 ; 238 334.69 -0.4276
.word 52256 ; 239 336.09 -0.4052
.word 52996 ; 240 337.50 -0.3827
.word 53742 ; 241 338.91 -0.3599
.word 54496 ; 242 340.31 -0.3369
.word 55257 ; 243 341.72 -0.3137
.word 56023 ; 244 343.13 -0.2903
.word 56796 ; 245 344.53 -0.2667
.word 57573 ; 246 345.94 -0.2430
.word 58356 ; 247 347.34 -0.2191
.word 59142 ; 248 348.75 -0.1951
.word 59933 ; 249 350.16 -0.1710
.word 60727 ; 250 351.56 -0.1467
.word 61524 ; 251 352.97 -0.1224
.word 62323 ; 252 354.38 -0.0980
.word 63125 ; 253 355.78 -0.0736
.word 63927 ; 254 357.19 -0.0491
.word 64731 ; 255 358.59 -0.0245
.word 65535 ; 256 360.00 0.0000
;-------------------------------------------------------------------------------
; I S R - PHANTOM
; Description: Dummy ISR, used to trap spurious interrupts.
;-------------------------------------------------------------------------------
PHANTOM     KICK_DOG            ;Resets WD counter
            B PHANTOM
```